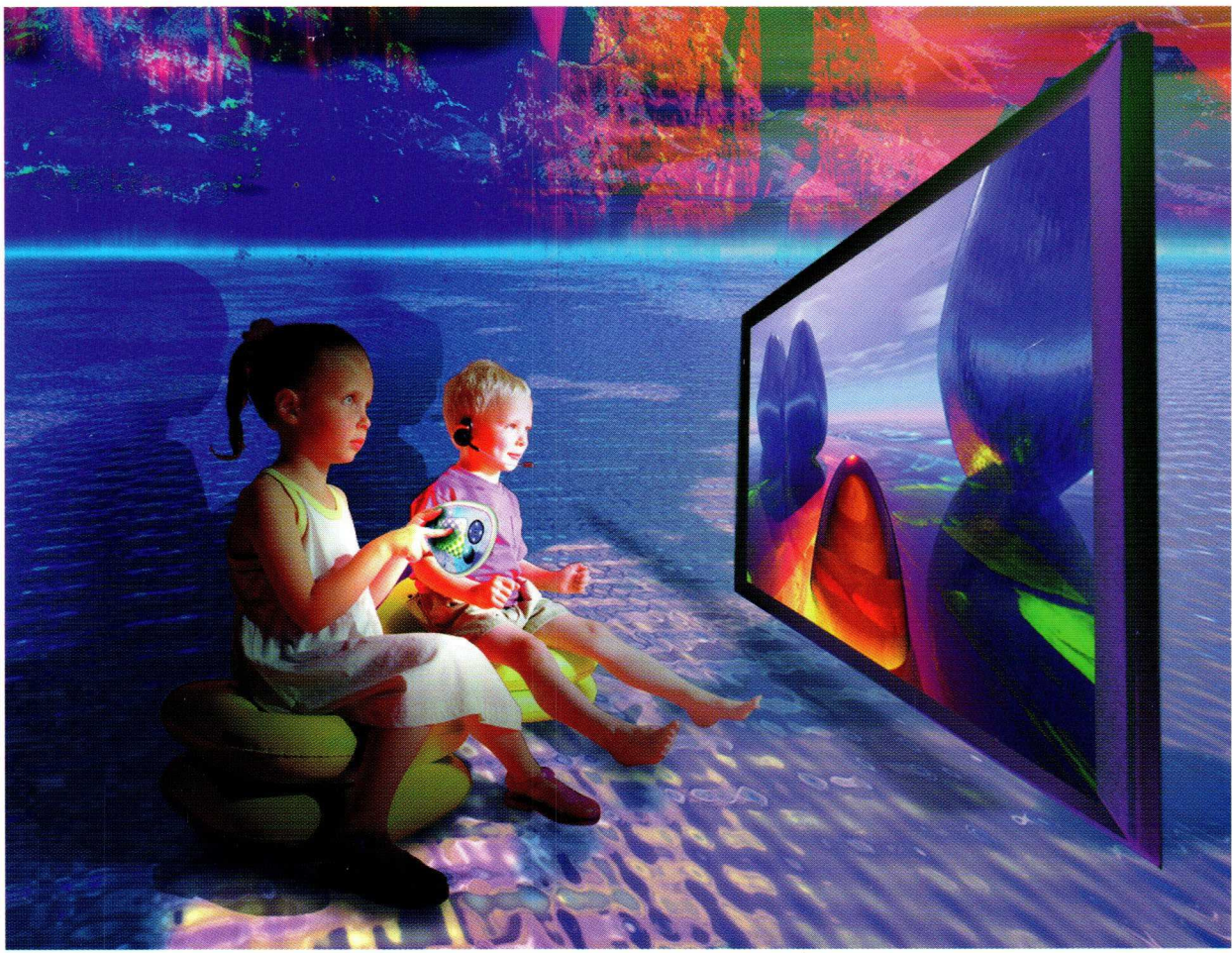
INTEGRATED CIRCUITS

Semiconductors for Television and Video Systems



1998

Data Handbook IC02

CD-ROM included

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

The audio/video market is characterized by a continuing demand for innovation to increase the functionality of ICs by achieving ever higher levels of integration, reducing power consumption, minimizing the number of peripheral components and reducing the need for circuit alignment during assembly. We achieve these goals by extensive use of computer control via the I^2C-bus, and by designing analog, digital and mixed signal circuits using the very latest signal processing techniques. We then fabricate the ICs with state-of-the-art production processes so we can offer you complete `systems-on-silicon' which help you maintain your competitive edge by staying one step ahead of the competition.

An innovative and reliable supplier

A total systems approach, embracing both hardware and software, is the foundation on which we have built our unrivalled reputation as an innovative and reliable supplier of high quality semiconductors for the audio/video segments of the consumer electronics market.

Our strengths in this field stem not only from being a large multinational organization with the resources to stay the course, but also from our dedication to research and to forming true and lasting partnerships with our customers.

World-class manufacturing, resources and customer support

Philips Semiconductors is a global supplier. We employ some 20,000 people, have more than 100 sales offices worldwide, are represented in 44 countries, and manufacture over 14,000 different products. Philips also has a level of commitment to research matched by very few companies, not just in terms of resources but in their focus on researching solutions for customers. Philips Semiconductors collaborates very closely with Philips Corporate Research Laboratories, one of the largest privately funded research organisations in the world. Five major research laboratories serve the whole group, in the Netherlands, UK, France, Germany and the USA.

As you would expect from a worldwide organization, our support doesn't end with the timely delivery of ICs and discretes to our audio/video customers. We are also dedicated to the aim of zero-defects quality for our semiconductors, and to offering unequalled service. There are Philips customer support and application centres in every major market area (Europe, Asia-Pacific, North America) to ensure that you can take full advantage of our extensive applications know-how and broad product range. Five System Laboratories are involved in programs and activities relevant to audio/video: Eindhoven, the Netherlands (TV, monitors and radio/audio); Hamburg, Germany (TV and radio/audio); Southampton, UK (teletext and digital audio, including CD technology); Taipei, Taiwan (TV, monitors and radio/audio).

They support all audio/video applications and work closely with customers, meeting and often anticipating their needs.

Many key developments have come from Philips laboratories - one-chip TV signal processors, ICs for memory-based TV features, a TV microcontroller with on-chip teletext, a two-chip receiver module for car radio, and a one-chip self-tuned radio are just a few examples. In addition, there are also Product Development groups in all the above locations.

Partnership

Since the spur for many of the ICs and discrete semiconductors in this databook have come from a cross-fertilisation of ideas with customers, we are fully aware that we need to be not only semiconductor suppliers, but also partners who are willing to work with customers to find solutions and help keep them at the leading edge of their field. At Philips Semiconductors, we work very closely with our audio/video customers and are determined to maintain a reputation for being the world's most customer-oriented supplier.

WHAT THIS BOOK AND CD-ROM CONTAIN

This book is a supplement to the existing databook IC02 - Semiconductors for Television and Video Systems, and contains the functional and alphanumeric indices for all data sheets contained on the accompanying CD-ROM. The data sheet files on the CD-ROM are in Adobe's Portable Document Format (PDF) - a cross-platform file format that requires Acrobat Reader to view (we have also supplied Acrobat Reader on the CD-ROM). Acrobat Reader enables you to view and print pages, and perform basic searches. Please refer to the README.1st file on the CD-ROM to find information on the CD's contents and organization, as well as instructions on how to install and use Acrobat Reader.

FOR MORE INFORMATION

Although the information in this databook is up-to-date at the time of going to press, the world of audio/video is so fast moving it is possible that some very recent developments may not have made it into this edition. For the latest information contact your local Philips organization (see the back page of this databook for addresses), or visit our Internet home page at: http://www.semiconductors.philips.com

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BF720; BF722	NPN high-voltage transistors	
BF721; BF723	PNP high-voltage transistors	
BF857; BF858; BF859	NPN high-voltage transistors	
BF869; BF871	NPN high-voltage transistors	
BF870; BF872	PNP high-voltage transistors	
BFV420	NPN high voltage transistor	
BFV421	PNP high voltage transistor	
BFV469	NPN high-voltage transistor	
SYNC/DEFLECTION		
Sync/deflection		
BY228	Damper diode	
BY328	Damper diode	
BY8000 series	Fast high-voltage soft-recovery controlled avalanche rectifiers	
BY8100 series	Very fast high-voltage soft-recovery controlled avalanche rectifiers	
BY8400 series	Fast high-voltage soft-recovery rectifiers	
BYD33 series	Fast soft-recovery controlled avalanche rectifiers	
BYW54 to BYW56	Controlled avalanche rectifiers	
TDA1082	East-West correction driver circuit	
TDA2579B	Horizontal/vertical synchronization circuit	
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	
TDA2595	Horizontal combination	
TDA2653A	Vertical deflection circuit; large screen colour TV	
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90 °)	
TDA3654; TDA 3654Q	Vertical deflection and guard circuit (110 °)	

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	TDA4800	Vertical deflection circuit for monitor applications	
	TDA4820T	Sync separation circuit for video applications	
	TDA4858	Economic Autosync Deflection Controller EASDC	
	TDA4866	Full bridge current driven vertical deflection booster	
*	TDA8350Q	DC-coupled vertical deflection and East-West output circuit	235
	TDA8351A	DC-coupled vertical deflection output circuit	
	TDA8351	DC-coupled vertical deflection circuit	
	TDA8356	DC-coupled vertical deflection circuit	
	TDA8433	Deflection processor for computer controlled TV receivers	
	TDA9150B	Programmable deflection controller	
	TDA9151B	Programmable deflection controller	
	Power supply		
	BYV95 series	Fast soft-recovery controlled avalanche rectifiers	
	TDA1023/T	Proportional-control triac triggering circuit	
	TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	
	TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	
	COMBI ICs		
	TDA8303; TDA8303A	Small signal combination IC for black/white TV	
	TDA8310	PAL/NTSC colour processor for PIP applications	
	TDA8315T	Integrated NTSC decoder and sync processor	
	TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	
	TDA8366	I²C-bus controlled PAL/NTSC TV processor	
*	**TDA837x fam**	I²C-bus controlled economy PAL/NTSC and NTSC TV-processors	238
	CONTROL		
	Clock/calendar		
	PCF8573	Clock/calendar with Power Fail Detector	
	PCF8583	Clock calendar with 240 x 8-bit RAM	
	PCF8593	Clock/calendar with 240 x 8-bit RAM	
	Display drivers		
	PCF1303T	18-element bar graph LCD driver	

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	PCF2116 family	LCD controller/drivers	
	PCF8558	Universal LCD driver for small graphic panels	
	PCF8566	Universal LCD driver for low multiplex rates	
	PCF8576C	Universal LCD driver for low multiplex rates	
	PCF8577C	LCD direct/duplex driver with I²C-bus interface	
	PCF8578	LCD row/column driver for dot matrix graphic displays	
	PCF8579	LCD column driver for dot matrix graphic displays	
	LED driver		
	SAA1064	4-digit LED-driver with I²C-bus interface	
	On Screen Display (OSD)		
*	PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application	65
*	PCA8514	Stand-alone OSD	79
*	PCA8515	Stand-alone OSD	84
	PCB8517	Stand-alone OSD for monitor applications	
	PCE84C882	Microcontroller for monitor OSD and auto-sync applications	
	PCE84C886	Microcontroller for monitor OSD and auto-sync applications	
	SAA5252	Line twenty-one acquisition and display (LITOD)	
	SAA5288	TV microcontroller with full screen On Screen Display (OSD)	
	Memories - SRAM		
	PCF8570	256 x 8-bit static low-voltage RAM with I²C-bus interface	
	EEPROM		
	PCA8581; PCA8581C	128 x 8-bit EEPROM with I²C-bus interface	
	PCB2421	1K dual mode serial EEPROM	
	PCF85116-3	2048 x 8-bit CMOS EEPROM with I²C-bus interface	
	PCF85xxC-2 family	256 to 1024 x 8-bit CMOS EEPROMs with I²C-bus interface	
	Microcontrollers general		
	80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	
	80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	
	83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	
	87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	
	87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	
	87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	

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*	83C145; 83C845; 83C055; 87C055	Microcontrollers for TV and video (MTV)	48
*	84C44X; 84C64X; 84C84X	8-bit microcontrollers with OSD and VST	54
	PCF84C12A;PCF84C22A; PCF84C42A	8-bit microcontroller	
	PCF84C21A;PCF84C41A; PCF84C81A	Telecom microcontroller	
	PCF84C85A	Microcontroller with extended I/O	
*	PCF84CxxxA family	8-bit microcontrollers	93
	Microcontrollers for TV		
*	PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application	65
	Microcontrollers for Monitors		
	PCE84C486; PCE84C487	Microcontrollers for digital auto-sync and VST TV controller applications	
	PCE84C882	Microcontroller for monitor OSD and auto-sync applications	
	PCE84C886	Microcontroller for monitor OSD and auto-sync applications	
	Digital Control		
	PCE84C486; PCE84C487	Microcontrollers for digital auto-sync and VST TV controller applications	
	PCE84C882	Microcontroller for monitor OSD and auto-sync applications	
	PCE84C886	Microcontroller for monitor OSD and auto-sync applications	
	Remote I/O expanders		
	PCF8574	Remote 8-bit I/O expander for I2C-bus	
	PCF8584	I^2C-bus controller	
	Remote control transmitter		
*	PCA84C122; C222; C422; C622; C822	8-bit microcontrollers for remote control transmitters	59
*	PCA84C922; PCA84C923	Microcontrollers for universal infrared remote transmitter applications	71
*	PCA8521	Infrared remote control transmitter RC5	
	SAA3004	Remote control transmitter	
	SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	

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	SAA3010	Infrared remote control transmitter RC-5	
	TELETEXT		
*	**SAA5700**	Chinese Character System Teletext (CCST) decoder	120
*	**SAA5X9X_fam_1**	Economy teletext and TV microcontrollers	125
	SAA5191	Teletext video processor	
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	SAA5246A	Integrated VIP and Teletext (IVT1.0)	
	SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX)	
	SAA5250	Interface for data acquisition and control (for multi-standard teletext systems)	
*	SAA5254	Integrated VIP and teletext decoder (IVT1.1X)	110
*	SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*)	114
	SAA5290	One-page Economy Teletext/TV microcontroller (ETT1.1)	
	SAA5355	Single-chip colour CRT controller (FTFROM)	
	SATELLITE TV		
	BB901	VHF variable capacitance diode	
*	TDA8010M; TDA8010AM	Low power mixers/oscillators for satellite tuners	212
*	TDA8012M	Low power PLL FM demodulator for satellite TV receivers	215
	TDA8730	PLL FM demodulator for DBS signals	
	TDA8735	PLL frequency synthesizer	
	TDA8740; TDA8740H	Satellite sound circuit with noise reduction	
	TDA8741; TDA 8741H	Satellite sound circuit with noise reduction	
	TDA8745	Satellite sound receiver with I^2C-bus control	
	TSA5055T	2.5 GHz bi-directional I^2C-bus controlled synthesizer	
	PAY TV		
*	TDA8000; TDA8000T	Smart card interface	197
	TDA8001	Smart card interface	
*	TDA8002	IC card interface	200
*	TDA8005	Low power smart card coupler	205
	VCR/Camera/Recorder		
	SAA1101	Universal sync generator (USG)	
	SAA1310	Control interface for VHS video recorders	

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	SAA4700T	VPS dataline processor	
	SAA4700	VPS dataline processor	
*	**SAA8110G**	Digital Signal Processor (DSP) for cameras	148
	SAA9740H	Advanced Auto Control Function (A2CF)	
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	TDA5140A	Brushless DC motor drive circuit	
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	TDA5142T	Brushless DC motor drive circuit	
	TDA5143T	Brushless DC motor drive circuit	
	TDA5144	Brushless DC motor drive circuit	
	TDA5145	Brushless DC motor drive circuit	
	TDA9615H	Audio processor for VHS hi-fi	
	TDA9725	Y/C automatic adjustment processor (VHS standard)	

MONITOR CIRCUITS

Sync

TDA2595	Horizontal combination
TDA4820T	Sync separation circuit for video applications
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors
TDA4852	Horizontal and vertical deflection controller for autosync monitors

Deflection

TDA2653A	Vertical deflection circuit; large screen colour TV
TDA4800	Vertical deflection circuit for monitor applications
TDA4855	Autosync Deflection Controller (ASDC)
TDA4858	Economic Autosync Deflection Controller EASDC
TDA4860	Vertical deflection power amplifier for monitors
TDA4861	Vertical deflection power amplifier for monitors
TDA4866	Full bridge current driven vertical deflection booster

SMPS

TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)

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Video control

TDA3504	Video control combination circuit
TDA3505; TDA3506	Video control combination circuit with automatic cut-off control
TDA3508	Video control combination circuit with automatic cut-off control
TDA4680	Video processor with automatic cut-off and white level control
TDA4780	RGB video processor with automatic cut-off control and gamma adjust
TDA4881	Advanced monitor video controller
TDA4882	Advanced monitor video controller for OSD
TDA4884	Three gain control video pre-amplifier for OSD

MISCELLANEOUS

NE/SA5204A	Wide-band high-frequency amplifier
NE/SA/SE5205A	Wide-band high-frequency amplifier
NE/SA5209	Wide-band variable gain amplifier
NE/SE5539	High frequency operational amplifier
NE5592	Video amplifier
NE592	Video amplifier
TDA4565	Colour transient improvement circuit
TDA4566	Colour transient improvement circuit
TDA4671	Picture Signal Improvement (PSI) circuit
TDA4672	Picture Signal Improvement (PSI) circuit with enhanced peaking function
TDA8442	I^2C-bus interface for colour decoders
TDA8444	Octuple 6-bit DAC with I^2C-bus
TDA8501	PAL/NTSC encoder
TDA8505	SECAM encoder
uA733; 733C	Differential video amplifier

REPLACEMENT/WITHDRAWAL TYPES

The following type numbers were in the previous issue of IC02, but not in the current version:

TYPE NUMBER	REASON FOR DELETION
83CE654	Replaced by C654 type
BA483	Discontinued
BB215	Discontinued
BF721	Discontinued
P8xCE528	Replaced by C528 type
PCA8516	Discontinued
PCF8522E	Replaced by PCF85xxC2/PCF8582C-2
PCF8524	Discontinued. Replaced by PCF85xxC2/PCF8594C-2
PCF8582X-2 family, PCx8594X-2 family, PCx8598X-2 family	Replaced by family data sheet PCF85xxC2
SAA4951WP	Removed from handbook
SAA7158	Removed from handbook
SAA7167A	Removed from handbook
SAD1009	Discontinued
SAF1135	Discontinued
TDA2555: TDA2557	Removed from handbook
TDA2654	Removed from handbook
TDA2658	Discontinued
TDA3507	Discontinued
TDA3561A	Removed from handbook
TDA3565	Removed from handbook
TDA3566	Removed from handbook
TDA3755	Discontinued
TDA3825	Discontinued
TDA3826	Discontinued
TDA3827	Discontinued
TDA3833	Removed from handbook
TDA3840	Removed from handbook
TDA3842	Removed from handbook
TDA3853T	Removed from handbook
TDA3868T	Removed from handbook
TDA4504B	Discontinued
TDA4560	Discontinued
TDA4568	Removed from handbook
TDA4580	Discontinued
TDA4655	Removed from handbook
TDA4663T	Removed from handbook
TDA4661	Discontinued
TDA4670	Removed from handbook

TYPE NUMBER	REASON FOR DELETION
TDA4672	Removed from handbook
TDA4685	Removed from handbook
TDA4686	Removed from handbook
TDA4688	Removed from handbook
TDA4691	Removed from handbook
TDA8304	Discontinued
TDA8349A	Removed from handbook
TDA8385	Discontinued
TDA8742; TDA8742H	Removed from handbook
TDA8762	Removed from handbook
TDA9715H/A	Removed from handbook
TDA9803	Removed from handbook
TDA9804	Discontinued
TEA7650H	Discontinued

GENERAL

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits
T Analog circuits
U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit
MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.
(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C –55 to +125 °C

D –25 to + 70 °C

E –25 to + 85 °C

F –40 to + 85 °C

G –55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

General

Rating systems

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

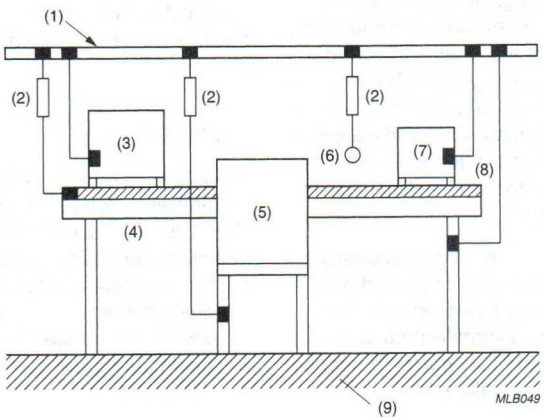
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

in alphanumeric sequence

All data sheets in this booklet are abstracts from full form data sheets.

In the abstracts reference might be made to e.g. figure numbers or tables that are not in the abstract data sheet. The full form data sheet, with all references, is on the CD-ROM

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1 FEATURES

- Masked ROM sizes:
  - 8 kbytes (83C845)
  - 12 kbytes (83C145)
  - 16 kbytes (83C055)
  - 16 kbytes OTP (87C055)
- RAM: 256 bytes
- On Screen Display (OSD) controller
- Three digital video outputs
- Multiplexer/mixer and background intensity controls
- Flexible formatting with OSD New Line option
- 128 × 10 bits display RAM
- Designed for reduced Radio Frequency Interference (RFI)
- Character generator ROM:
  - character format 18 lines × 14 dots
  - 60 visible characters
  - 4 special characters
- Eight text shadowing modes
- Text colour selectable per character
- Background colour selectable per word
- Background colour versus video selectable per character
- Eight 6-bit Pulse Width Modulators (PWM) for analog voltage integration
- One 14-bit PWM for high-precision voltage integration
- Digital-to-analog converter and comparator with 3 inputs multiplexer
- Nine dedicated I/Os plus 28 port bits (15 port bits with alternative uses)
- 4 high current open-drain port outputs
- 12 high voltage (+12 V) open-drain outputs
- Programmable video input and output polarities
- 80C51 instruction set
- No external memory capability
- Plastic shrink dual in-line package (0.07 inch centre pins)
- High-speed CMOS technology
- Power supply: 5 V ±10%.

2 DESCRIPTION

The 83C055, Microcontroller for Television and Video (MTV) applications, is a derivative of Philips' industry standard 80C51 microcontroller.

The 83C055 is intended for use as the central control mechanism in a television receiver or tuner.

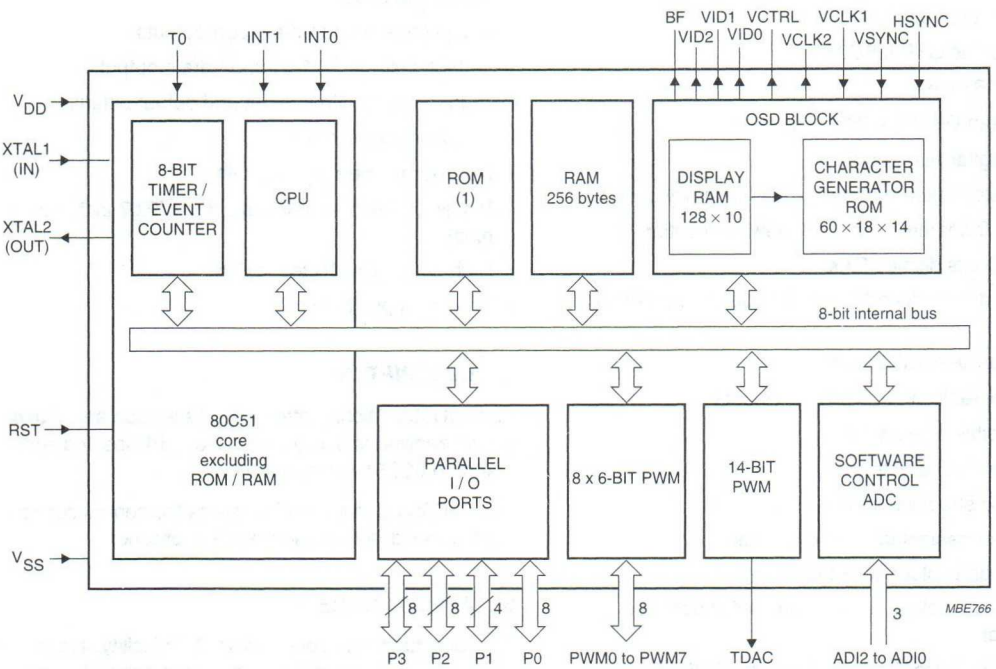
3 APPLICATIONS

Providing tuner functions and an OSD facility, it represents a next generation replacement for the currently available parts.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMP. RANGE (°C)	FREQ. (MHz)
	NAME	DESCRIPTION	VERSION		
P83C055BBP	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	0 to +70	3.5 to 12
P87C055BBP					
P83C145BBP					
P83C845BBP					

5 BLOCK DIAGRAM



(1) ROM sizes: see Table 1.

Fig.1 Block diagram.

5.1 Part options

Table 1 Differences between the types

MEMORY	TYPES			
	83C845	**83C145**	**83C055**	**87C055**
ROM	8 kbytes	12 kbytes	16 kbytes	–
EPROM (OTP)	–	–	–	16 kbytes

6 PINNING INFORMATION

6.1 Pinning

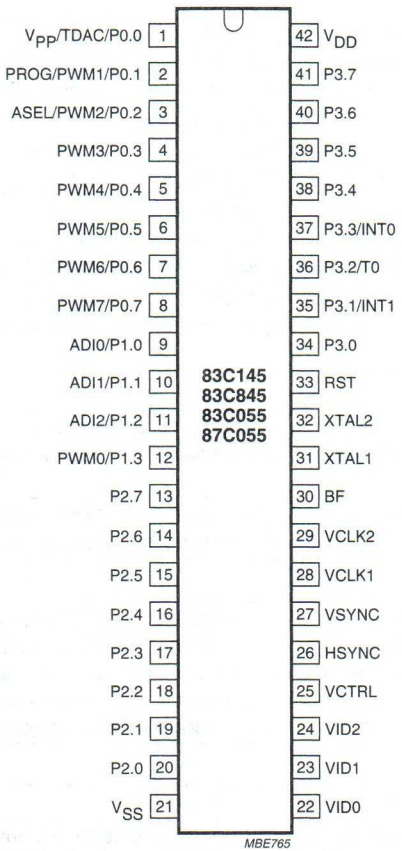


Fig.2 Pin configuration (SOT270-1).

6.2 Pin description

Table 2 Pin description SDIP42 (SOT270-1)

SYMBOL	PIN	DESCRIPTION
Port 0 (notes 1, 2 and 4)		
P0.0/TDAC/V_{PP}	1	**P0.0**: open-drain bidirectional port line; **TDAC**: output for the 14-bit high-precision PWM; V_{PP}: 12 V programming supply voltage during EPROM programming.
P0.1/PWM1/PROG	2	**P0.1**: open-drain bidirectional port line; **PWM1**: output for the 6-bit lower-precision PWM; **PROG**: input for EPROM programming pulses.
P0.2/PWM2/ASEL	3	**P0.2**: open-drain bidirectional port line; **PWM2**: output for the 6-bit lower-precision PWM; **ASEL**: input indicating the EPROM address bits that are applied to Port 2.
P0.3/PWM3 to P0.7/PWM7	4 to 8	**P0.3 to P0.7**: 5 open-drain bidirectional port lines; **PWM3 to PWM7**: 5 outputs for the 6-bit lower-precision PWM.
Port 1 (notes 1, 2 and 5)		
P1.0/ADI0 to P1.2/ADI2	9 to 11	**P1.0 to P1.2:** 3 open-drain bidirectional port lines; **ADI0 to ADI2**: inputs for the software analog-to-digital facility.
P1.3/PWM0	12	**P1.3**: open-drain bidirectional port line; **PWM0**: output for the 6-bit lower-precision PWM. PWM0 can be externally pulled up as high as +12 V ±5%
Port 2		
P2.7 to P2.0	13 to 20	**Port 2**: 8-bit open-drain bidirectional port; P2.3 to P2.0 have high current capability (10 mA at 0.5 V) for driving LEDs. Port 2 pins that have logic 1s written to them float, and in that state can be used as high-impedance inputs. Any of the Port 2 pins are driven LOW if the port register bit is written as a logic 0. The state of the pin can always be read from the port register by the program.
Port 3 (note 1 and 3)		
P3.0	34	**P3.0**: open-drain bidirectional port line.
P3.1/INT1	35	**P3.1**: open-drain bidirectional port line; **INT1**: External interrupt 1.
P3.2/T0	36	**P3.2**: open-drain bidirectional port line; **T0**: Timer 0 external input.
P3.3/INT0	37	**P3.3**: open-drain bidirectional port line; **INT0**: External interrupt 0.
P3.4 to P3.7	38 to 41	**P3.4 to P3.7**: 4 open-drain bidirectional port lines.
General		
V_{SS}	21	**Ground**: 0 V reference.
VID2 to VID0	22 to 24	**Digital Video bus**: Three totem-pole outputs comprising digital RGB (or other colour encoding) from the OSD facility. The polarity of these outputs is controlled by a programmable register bit (register OSCON; bit Po).
VCTRL	25	**Video Control**: A totem-pole output indicating whether the OSD facility is currently presenting active video on the VID2 to VID0 outputs. Signal is used to control an external multiplexer (mixer) between normal video and the video derived from VID2 to VID0. The polarity of this output is controlled by a programmable register bit (register OSCON; bit Pc).

SYMBOL	PIN	DESCRIPTION
HSYNC	26	**Horizontal Sync**: A dedicated input for a TTL-level version of the horizontal sync pulse. The polarity of this pulse is programmable; its trailing edge is used by the OSD facility as the reference for horizontal positioning.
VSYNC	27	**Vertical Sync**: A dedicated input for a TTL-level version of the vertical sync pulse. The polarity of this pulse is programmable, and either edge can serve as the reference for vertical timing.
VCLK1	28	**VCLK1: Video Clock 1**; input for the horizontal timing reference for the OSD facility. **VCLK2: Video Clock 2**; output from the on-chip video oscillator. VCLK1 and VCLK2 are intended to be used with an external LC circuit to provide an on-chip oscillator. The period of the video clock is determined such that the width of a pixel in the OSD is equal to the inter-line separation of the raster.
VCLK2	29	
BF	30	**Background/Foreground**: A totem-pole output which, when VCTRL is active, indicates whether the current video data represents a Foreground (LOW) or Background (HIGH) dot in a character. This signal can be used to reduce the intensity of the background colour and thus emphasize the text.
XTAL1	31	**XTAL1**: Input to the inverting (oscillator) amplifier and clock generator circuit that provides the timing reference for all 83C055 logic other than the OSD facility. **XTAL2**: Oscillator output terminal for system clock. XTAL1 and XTAL2 can be used with a quartz crystal or ceramic resonator to provide an on-chip oscillator. Alternatively, XTAL1 can be connected to an external clock, and XTAL2 left unconnected.
XTAL2	32	
RST	33	**Reset**: If this pin is HIGH for two machine cycles (24 oscillator periods) while the oscillator is running, the MTV is reset. This pin is also used as a serial input to enter a test or EPROM programming mode, as on the 87C751.
V_{DD}	42	**Power supply**: for normal and Power-down operation.

Notes

1. Port 0, Port 1 , and Port 3 pins that have logic 1s written to them float, and in that state can be used as high-impedance inputs.
2. The state of the pin can always be read from the port register by the program.
3. P3.0, P3.4, and P3.7 can be externally pulled up as high as +12 V ±5%; while P3.5 and P3.6 have 10 mA drive capability.
4. For each PWM block, a register bit (register PWMn; bit PWnE; n = 0 to 7) controls whether the corresponding pin is controlled by the block or by Port 0; Port 0 controls the pin immediately after a reset. Regardless of how each pin is controlled, it can be externally pulled up as high as +12 V ±5%.
5. Any of the Port 1 pins are driven LOW if the corresponding port register bit is written as a logic 0, or for P1.3 only, if the TDAC module presents a logic 0.

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1 FEATURES

1.1 PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O in a single 42 leads shrink DIL package
- Over 80 instructions all of 1 or 2 cycles
- 29 quasi-bidirectional standard I/O port lines
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0 and T1
- 8-bit programmable timer/event counter
- 3 single level vectored interrupts (external, timer/counter, I²C-bus)
- Power-on-reset and low voltage detector
- Single power supply
- 2 power reduction modes: Idle and Stop
- Operating temperature range: –20 to +70 °C
- Silicon gate CMOS fabrication process (SAC2).

1.2 Derivative features PCA84C640

Although the **PCA84C640** is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C640 and the other devices are specified in the text and also highlighted in Chapter 6.

The PCA84C640 comprises:

- The PCF84CXXXA processor core
- 6 kbytes mask-programmable program ROM
- 128 bytes RAM
- Multi-master I²C-bus interface
- AFC input for Voltage Synthesized Tuning (VST; with 3-bit DAC and comparator)
- On Screen Display (OSD) facility for two rows of 16-characters
- On Screen Display character set of 64 types
- Four programmable display dot sizes
- Half dot character rounding
- Seven colours for each character
- One 14-bit PWM output for VST
- Five 6-bit PWM outputs for analog controls
- Eight port lines with 10 mA LED drive capability
- 18 general purpose bidirectional I/O lines plus 11 function-combined I/O lines
- 2 direct testable lines
- Programmable VSYNCN and HSYNCN input polarity
- RC oscillator for OSD function.

2 GENERAL DESCRIPTION

The 84C44X; 84C64X; 84C84X denotes the types:

- PCA84C440; 84C441; 84C443; 84C444
- PCA84C640; 84C641; 84C643; 84C644
- PCA84C840; 84C841; 84C843; 84C844.

which are 8-bit microcontrollers with On Screen Display (OSD) and Voltage Synthesized Tuning (VST) functions. All are members of the 84CXXX microcontroller family.

There are two oscillator types for the OSD function in the various types, i.e.,

- RC oscillator: PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843
- LC oscillator: PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

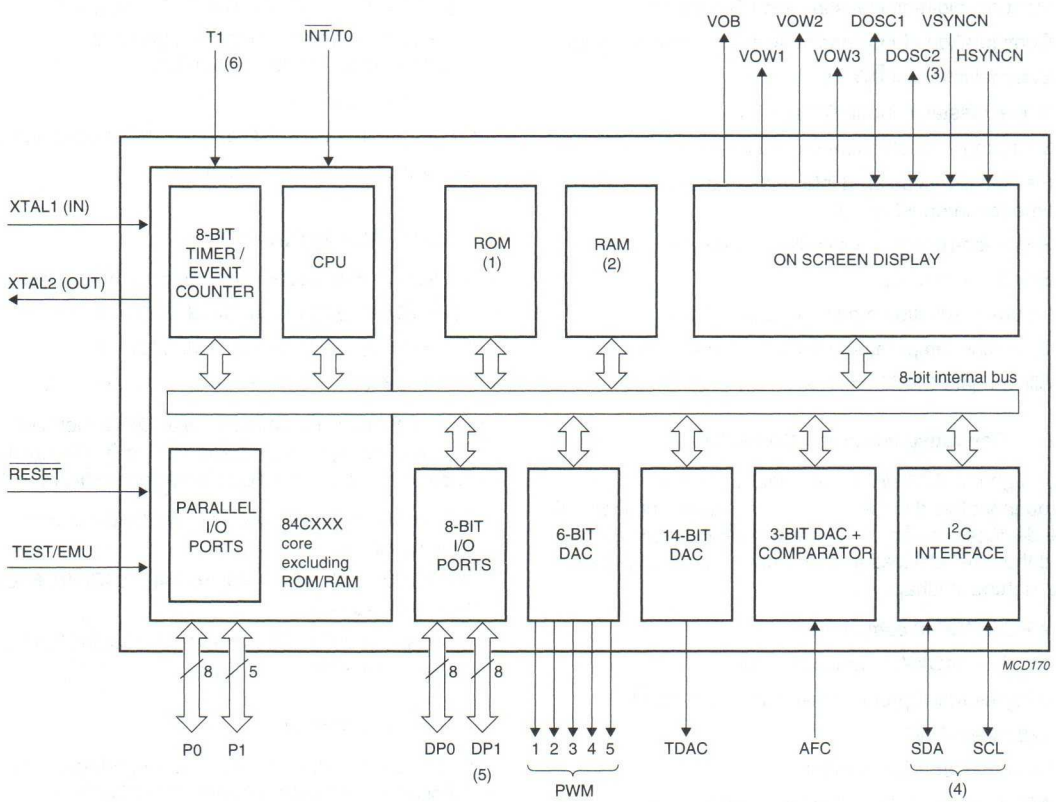
2.1 Important note

This data sheet details the specific properties of the PCA84C44X, PCA84C64X and PCA84C84X.
The shared characteristics of the PCA84CXXX family of microcontrollers are described in the PCF84CXXXA Family single-chip 8-bit Microcontroller of *"Data Handbook IC14"*, which should be read in conjunction with this data sheet.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	–20 to +70
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844				

4 BLOCK DIAGRAM



(1) 4 kbytes for the PCA84C440; 84C441; 84C443; 84C444.
6 kbytes for the PCA84C640; 84C641; 84C643; 84C644.
8 kbytes for the PCA84C840; 84C841; 84C843; 84C844.

(2) 128 bytes for the PCA84C440; 84C441; 84C443; 84C444; 84C640; 84C641; 84C643; 84C644.
192 bytes for the PCA84C840; 84C841; 84C843; 84C844.

(3) For use with an LC oscillator, only available with the:
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

(4) I^2C-bus interface not available with the:
PCA84C443; 84C444; 84C643; 84C644; 84C843; 84C844.

(5) DP1.4 only available for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.

(6) T1 = pin 29 for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.
T1 = pin 34 for PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

Fig.1 Block diagram.

5 PINNING INFORMATION

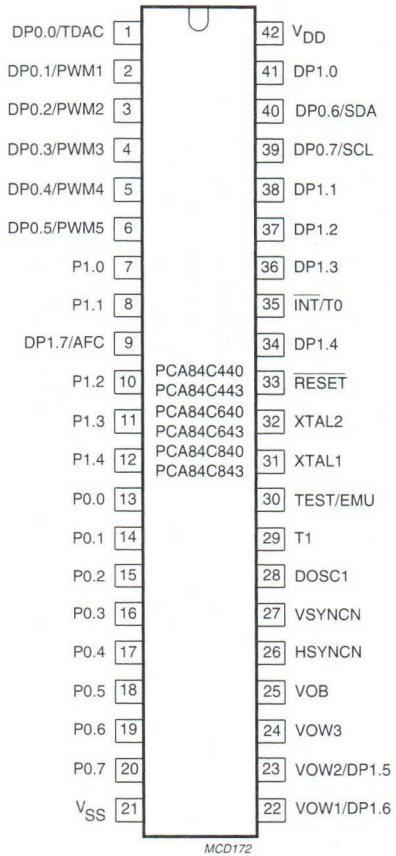


Fig.2 Pinning diagram for PCA84CX40; 84CX43.

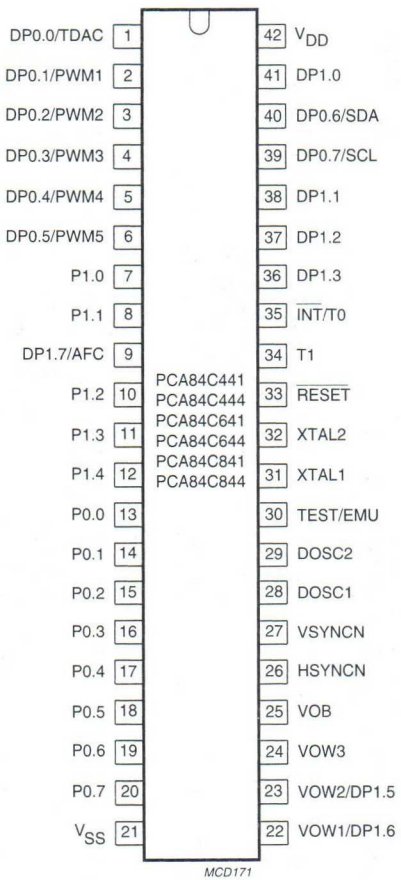


Fig.3 Pinning diagram for PCA84CX41; 84CX44.

Table 1 Pin description

SYMBOL[1]		PIN[1]		DESCRIPTION
84CX40; 84CX43	**84CX41; 84CX44**	**84CX40; 84CX43**	**84CX41; 84CX44**	
Deviating pinning				
DP1.0 to DP1.4	DP1.0 to DP1.3	41, 38, 37, 36, 34	41, 38, 37, 36	Derivative Port 1: quasi-bidirectional I/O lines.
T1	T1	29	34	Direct testable pin and event counter input.
DOSC1	–	28	–	Connection to RC oscillator of OSD clock.
–	DOSC1/DOSC2	–	28, 29	Connections to LC oscillator of OSD clock.
Mutual pinning				
DP0.0/TDAC		1		Derivative Port 0: quasi-bidirectional I/O line or 14-bit DAC PWM.
DP0.1 to DP0.5/PWM1 to PWM5		2 to 6		Derivative Port 1: quasi-bidirectional I/O lines or 6-bit DAC PWM.
P1.0 to P1.4		7, 8, 10, 11 and 12		Port 1: quasi-bidirectional I/O lines.
P0.0 to P0.7		13 to 20		Port 0: quasi-bidirectional I/O port.
DP1.7/AFC		9		Derivative Port 1: quasi-bidirectional I/O line or comparator input with 3-bit DAC.
DP0.6/SDA		40		Derivative open drain I/O port or I^2C-bus data line.
DP0.7/SCL		39		Derivative open drain I/O port or I^2C- bus clock line.
$\overline{INT}$/T0		35		External interrupt or direct testable line.
DP1.5 and DP1.6/VOW2 and VOW1		23, 22		Derivative Port 1: quasi-bidirectional I/O lines or character video output.
$\overline{RESET}$		33		Initialize input, active LOW.
XTAL2, XTAL1		32, 31		Oscillator output or input terminal for system clock.
TEST/EMU		30		Control input for testing and emulation mode. Ground for normal operation.
VSYNCN		27		Vertical synchronous signal input.
HSYNCN		26		Horizontal synchronous signal input.
VOB		25		Blanking output.
VOW3		24		Character video output of OSD.
V_{SS}		21		Ground.
V_{DD}		42		Power supply.

Note

1. **84CX40; 84CX43** denotes the types: PCA84C440, PCA84C443, PCA84C640, PCA84C643, PCA84C840 and PCA84C843.
   84CX41; 84CX44 denotes the types: PCA84C441, PCA84C444, PCA84C641, PCA84C644, PCA84C841 and PCA84C844.

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1 FEATURES

- 84CXXX CPU
- ROM, RAM and I/O configurations are device dependent; see Chapter 3
- Two test inputs: T0 (ANDed with Port 1 input lines) and T1
- 3 single-level vectored interrupt sources:
  - external (T0/$\overline{INT}$ and Port 1, for keypad press wake-up function)
  - timer/counter (TI)
  - hardware modulator interrupt
- 8-bit programmable timer/counter with 5-bit pre-scaler
- Power saving: Idle and Stop modes are provided
- Hardware Modulator providing pulse bursts, with:
  - programmable duty factor for each pulse
  - programmable number of pulses
- One output line from the Hardware Modulator to control the driver transistor for the infrared LED (IR-LED). Capable of sinking 27 mA at V_{DD} = 2.0 V, $V_{\overline{OUT}}$ = 1.0 V
- Watchdog Timer to keep the transmitter from being locked or malfunction
- Available packages: SO and DIP types (SO20, SO24, SO28, SDIP24 and DIP20); see Chapter 4
- On-chip oscillator: 455 kHz to 6 MHz
- Single supply voltage: 2.0 V to 5.5 V
- Operating temperature: –20 to +50 °C.

2 GENERAL DESCRIPTION

The PCA84C122 is a stand-alone microcontroller designed for use in remote control transmitters for a wide range of applications.

The PCA84C122 provides a number of dedicated hardware functions for remote controller applications. These functions include the following additional blocks to the 84CXXX core:

- Interrupt Gate
- Hardware Modulator
- Output Driver
- Watchdog Timer.

Although the PCA84C122 is specifically referred to throughout this data sheet, the information applies to all the devices. The differences between the PCA84C122 and the other devices are specified in Chapter 3.

Figure 2 shows the general block diagram of the device. The 84CXXX core plus 8 kbytes ROM and 64 bytes RAM has the same function as described in the PCF84CXXX family description (see *"Data Handbook IC14"*).

When the transmitter is not in use the microcontroller is in Stop mode and the oscillator is halted. The AND gate connected to the Port 1 (P10 to P17) lines provides the wake-up to end the Stop mode.

The Hardware Modulator produces pulse bursts according to the required protocol. The ON-time and OFF-time of each pulse (i.e. duty factor) and the number of pulses are controlled by software.

The Watchdog Timer (WDT) will reset the PCA84C122 when it has not been reloaded (reset) in time, because the program has run out of sequence (endless loop, continuous Idle mode, etc.). During Stop mode the oscillator is halted, therefore the Watchdog Timer is not running.

Automatic system reset is generated by the WDT if the timer is not reset before overflow from counting within a certain period of time.

The Output Driver can handle sufficient current to drive a single transistor, that provides the required current for the IR-LED.

2.1 Important note

This data sheet details the specific properties of the PCA84C122; PCA84C222; PCA84C422; PCA84C622 and PCA84C822. The shared characteristics of the family of microcontrollers are described in the PCF84CXXXA Family single-chip 8-bit Microcontroller of *"Data Handbook IC14"*, which should be read in conjunction with this data sheet.

3 MEMORY AND I/O CONFIGURATIONS

DEVICE	I/O LINES	ROM	RAM
PCA84C122A	16	1K	32 bytes
PCA84C122B	12		
PCA84C222A	16	2K	
PCA84C222B	12		
PCA84C422A	16	4K	
PCA84C422B	12		
PCA84C622A	16	6K	64 bytes
PCA84C622B	12		
PCA84C622C	20[1]		
PCA84C822A	16	8K	
PCA84C822B	12		
PCA84C822C	20[1]		

Note

1. 4 I/O lines with 10 mA sink capability.

4 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84CX22AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84CX22AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84CX22BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCA84CX22BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA84C622CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm; low stand-off height	SOT136-1
PCA84C822CT			

Note

1. 'X' in the type number denotes the numbers: 1, 2, 4, 6 and 8.

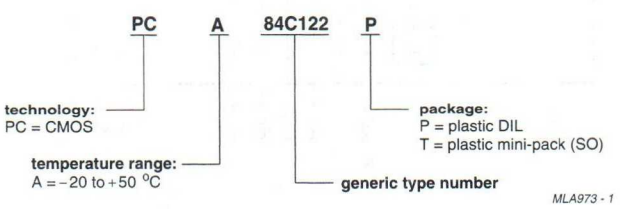


Fig.1 Numbering scheme.

5 BLOCK DIAGRAM

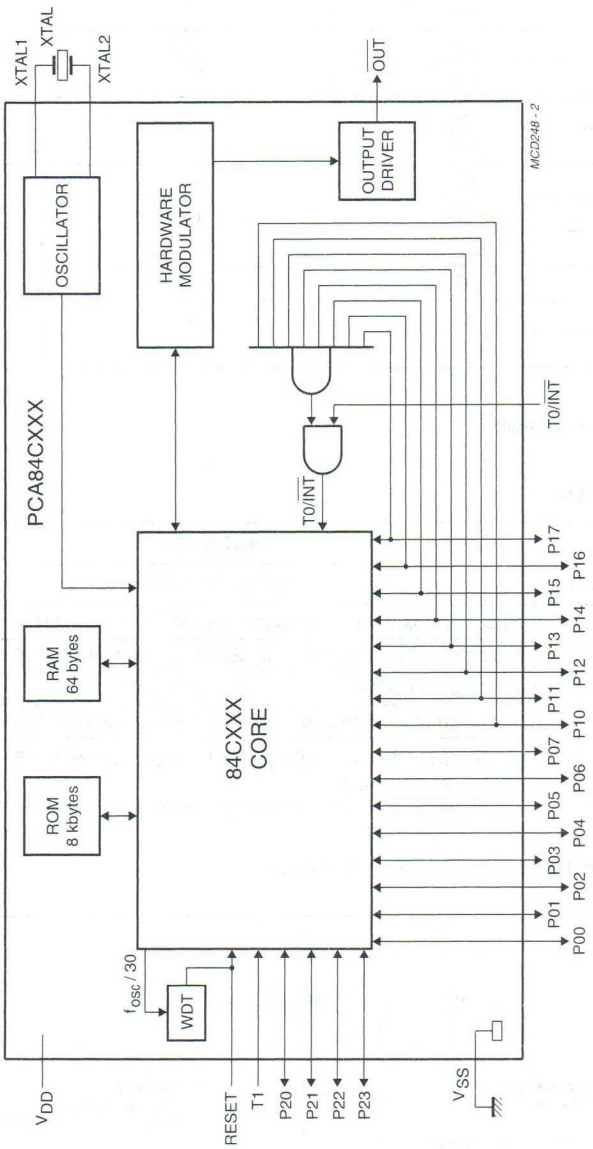


Fig.2 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

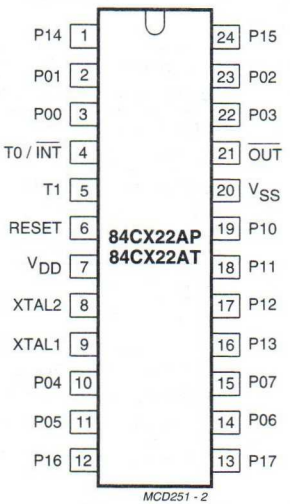


Fig.3 Pin configurations PCA84CX22AP (SDIP24) and PCA84CX22AT(SO24).

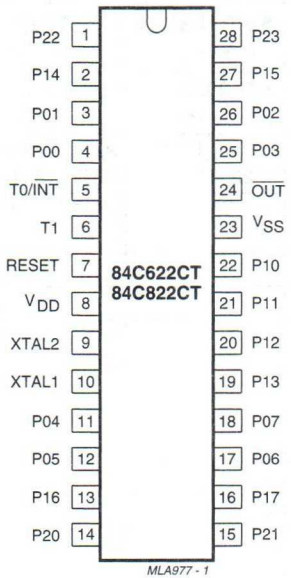


Fig.4 Pin configuration PCA84CX22CT (SO28).

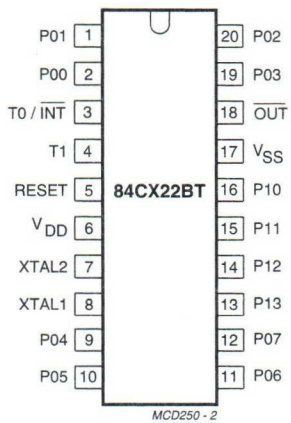


Fig.5 Pin configuration PCA84CX22BT (SO20).

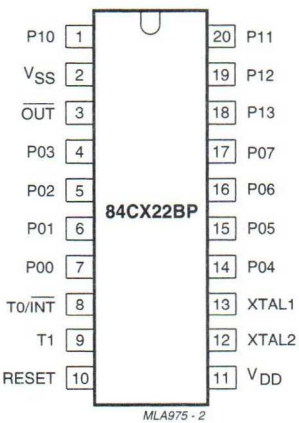


Fig.6 Pin configuration PCA84CX22BP (DIP20).

6.2 Pin description

Table 1 Pin description for PCA84CX22AP, PCA84CX22AT, PCA84CX22BP, PCA84CX22BT and PCA84CX22CT

SYMBOL	PIN				DESCRIPTION
	SDIP24/SO24 (see Fig.3)	**SO28** (see Fig.4)	**SO20** (see Fig.5)	**DIP20** (see Fig.6)	
P00 to P07	3, 2, 23, 22, 10, 11, 14, 15	4, 3, 26, 25, 11, 12, 17, 18	2, 1, 20, 19, 9, 10, 11, 12	7, 6, 5, 4, 14, 15, 16, 17	standard I/O Port lines, generally used for keypad scanning
P10 to P17	19, 18, 17, 16, 1, 22, 12, 13	22, 21, 20,19, 2, 27, 13, 16	16, 15, 14, 13	1, 20,19, 18	standard I/O Port lines, generally used for keypad sensing
P20 to P23	–	14, 15, 1, 28	–	–	standard I/O Port lines, generally used for visible LED's
T0/$\overline{\text{INT}}$	4	5	3	8	test T0 and external interrupt input
T1	5	6	4	9	test T1 input
RESET	6	7	5	10	active HIGH reset; normally connected to V_{SS}. For further information see PCF84CXXXA description in *"Data Handbook IC14"*.
XTAL1	9	10	8	13	crystal or ceramic resonator
XTAL2	8	9	7	12	
$\overline{\text{OUT}}$	21	24	18	3	pulse train output pin, capable of sinking 27 mA
V_{DD}	7	8	6	11	power supply
V_{SS}	20	23	17	2	ground

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1 FEATURES

1.1 PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O and derivative logic in one package
- Over 80 instructions
- All instructions of 1 or 2 cycles
- Quasi-bidirectional standard I/O port lines (P0, P1)
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0, T1
- 8-bit timer/event counter
- Single level vectored interrupt: external ($\overline{INT}$), counter/timer, I²C-bus and $\overline{VSYNC}$
- Configuration of optimal on-chip oscillator transconductance by mask
- On-chip oscillator clock frequency: 1 to 10 MHz
- Power-on-reset and low-voltage detector
- Low standby voltage and current in Idle and Stop modes
- Single power supply: 4.5 to 5.5 V
- Operating temperature: –20 to +70 °C.

1.2 VST and OSD derivative

- 6 kbytes (PCA84C646) or 8 kbytes (PCA84C846) system ROM, 192 bytes system RAM
- A multi-master I²C-bus interface
- One 14-bit PWM output for VST
- Three AFC inputs with 4-bit DAC and comparator
- Four 6-bit PWM and four 7-bit PWM outputs (DACs for analog controls)
- Eight port lines with 10 mA LED drive (at ≤1.2 V) capability
- Programmable active level polarities of $\overline{VSYNC}$/$\overline{HSYNC}$
- Display RAM: 64 × 10-bit
- Display character fonts: 64 (62 customized + 2 special reserved codes)
- Display starting position: 64 different positions by software control, both vertical and horizontal
- Character size: 4 different character sizes, line-by-line basis, 1 dot = 1H/1V, 2H/2V, 3H/3V, 4H/4V. (H: OSD clock period, V: number of horizontal scan line height)
- Character matrix: 12 × 18 with no spacing between characters
- Foreground colours: 8, character-by-character basis
- Background colours: 8, word-by-word basis. Available when background is either in North-west shadowing, Box shadowing and Frame shadowing mode
- Background/shadowing modes: 4, No background, North-west shadowing, Box shadowing, Frame shadowing (raster blanking), frame basis
- On-chip oscillator for On Screen Display (OSD) function
- Character blinking rate: 1 : 1, 1 : 3, 3 : 1 (frequency: $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}, programmable), character basis
- Display format: flexible display format by using Carriage Return (CR) code
- Spacing between lines: 4 different choices, from 0, 4, 8 or 12 horizontal scan lines
- Auto display character RAM address post increment when writing data
- On-chip Power-on-reset
- $\overline{VSYNC}$ leading edge can generate interrupt (programmable enable/disable by software)
- 8-bit counter triggered by external pulse input.

2 GENERAL DESCRIPTION

The PCA84C646 and PCA84C846 are 8-bit microcontrollers with enhanced OSD and VST functions. The PCA84C646 and PCA84C846 are members of the PCA84C640 CMOS microcontroller family. They include the PCF84CXXXA processor core, 6 or 8 kbytes of ROM and 192 bytes of RAM.

I/O requirements are adequately catered for with 13 general purpose bidirectional I/O lines plus 16 function combined I/O lines. One 14-bit PWM analog control, 3 AFC inputs (4-bit DAC + comparator) for VST and four 6-bit and 7-bit PWM analog control outputs are provided.

In addition to all these features a master-slave I^2C-bus interface, 2 directly testable lines and an enhanced OSD facility for flexible screen format (maximum of 64 character types) are also provided.

The on-chip Phase-Locked Loop (PLL) oscillator for OSD operation considerably reduces the radiation generated by the RC or LC oscillator. An 8-bit timer is integrated on-chip with a 5-bit prescaler. Another 8-bit counter with Schmitt-trigger input is used for clock/timer function application.

Figure 1 shows the block diagram of the PCA84C646 and PCA84C846.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84C646P	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
PCA84C846P			

4 BLOCK DIAGRAM

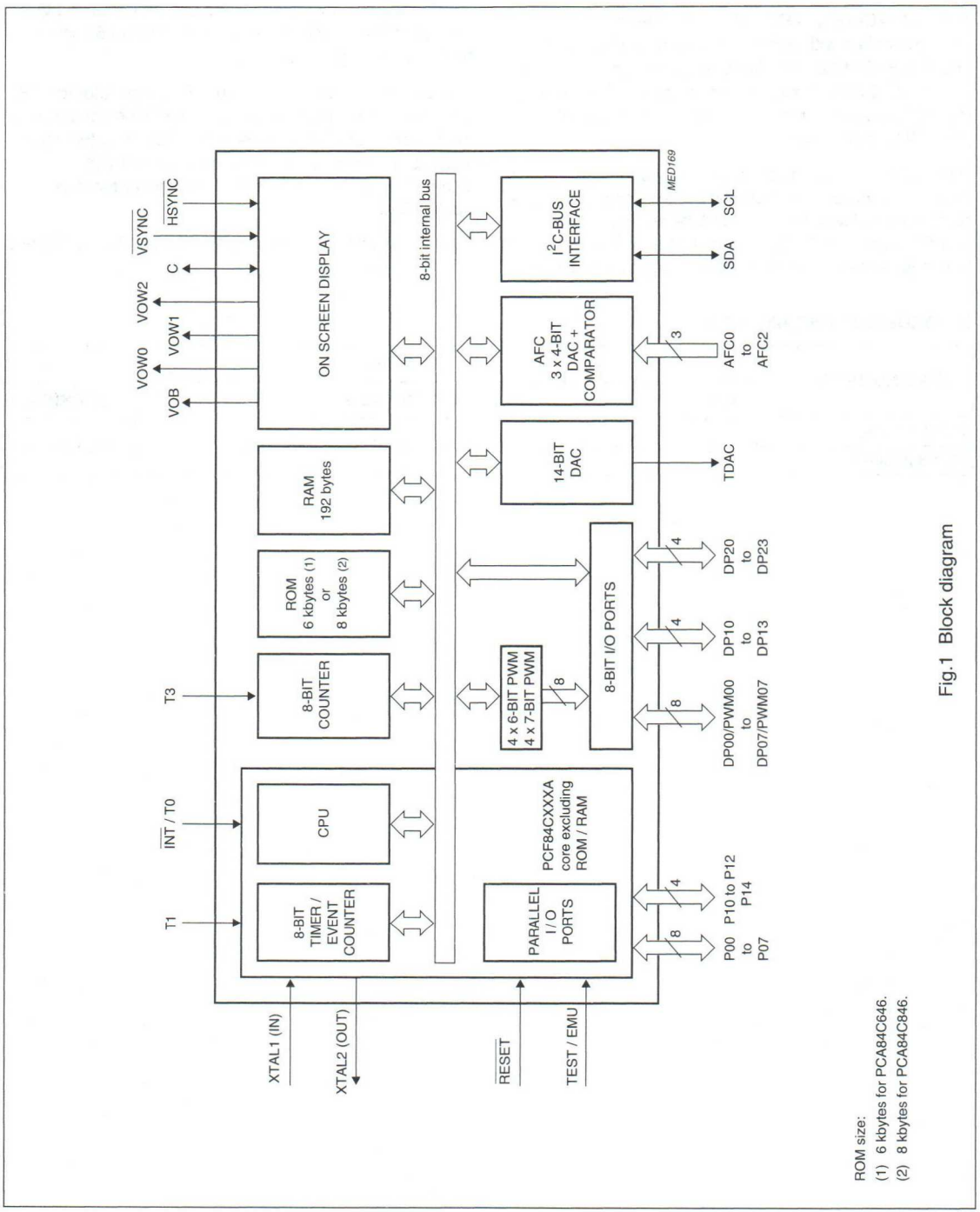


Fig.1 Block diagram

ROM size:
(1) 6 kbytes for PCA84C646.
(2) 8 kbytes for PCA84C846.

5 PINNING INFORMATION

5.1 Pinning

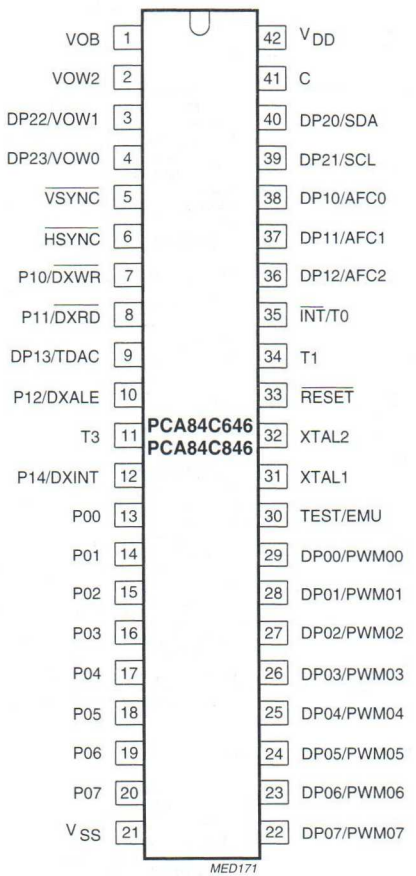


Fig.2 Pin configuration PCA84C646P and PCA84C846P (SDIP42; SOT270-1).

5.2 Pin description

Table 1 Pin description for PCA84C646P and PCA84C846P; SDIP42 (see Fig.2)

SYMBOL	PIN	DESCRIPTION
VOB	1	Video fast blanking output signal.
VOW2	2	Video character outputs or derivative port lines.
DP22/VOW1	3	
DP23/VOW0	4	
$\overline{\text{VSYNC}}$	5	Vertical synchronization signal input, active LOW.
$\overline{\text{HSYNC}}$	6	Horizontal synchronization signal input, active LOW.
P10/$\overline{\text{DXWR}}$	7	Port line 10 or emulation $\overline{\text{DXWR}}$ signal input.
P11/$\overline{\text{DXRD}}$	8	Port line 11 or emulation $\overline{\text{DXRD}}$ signal input.
DP13/TDAC	9	Derivative I/O port or 14-bit D/A PWM.
P12/DXALE	10	Port line 12 or emulation DXALE signal input.
T3	11	Secondary 8-bit counter input pin (Schmitt-trigger).
P14/DXINT	12	Port line 14 or emulation DXINT signal input.
P00 to P07	13 to 20	General I/O port lines (10 mA).
V_{SS}	21	Ground.
DP00/PWM00 to DP07/PWM07	29, 28, 27, 26, 25, 24, 23, 22	Derivative I/O port; 6-bit PWM (PWM04 to 07) or 7-bit PWM (PWM00 to 03).
TEST/EMU	30	Control input of testing and emulation mode, normally LOW.
XTAL1	31	Oscillator input terminal for system clock.
XTAL2	32	Oscillator output terminal for system clock.
$\overline{\text{RESET}}$	33	Initialize input, active LOW.
T1	34	Direct testable pin and event counter input.
$\overline{\text{INT}}$/T0	35	External interrupt/direct testable pin.
DP12/AFC2	36	Derivative I/O port or comparator input with 4-bit DAC.
DP11/AFC1	37	
DP10/AFC0	38	
DP21/SCL	39	Derivative port line or I^2C-bus clock line.
DP20/SDA	40	Derivative port line or I^2C-bus data line.
C	41	External capacitor input for on chip PLL OSD oscillator.
V_{DD}	42	Power supply.

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1 FEATURES

- 84CXXX CPU
- ROM, RAM, I/O and keypad configurations are device dependent; see Table 1
- Two test inputs: T0 and T1
- 3 single-level vectored interrupt sources:
  - external (T0/$\overline{\text{INT}}$ and Port 1, for keypad press Wake-up function)
  - Timer/counter (TI)
  - Hardware Modulator interrupt
- 8-bit programmable timer/counter with 5-bit prescaler
- Power saving Idle and Stop modes
- Low power operation: 2 V
- Hardware Modulator
- Watchdog timer
- On-chip oscillator: 1 to 6 MHz
- Single supply voltage: 2.0 to 5.5 V
- Operating temperature: –20 to +70 °C
- Available packages: SO24, SO28, VSO56 and SDIP24.

2 GENERAL DESCRIPTION

The PCA84C922A, PCA84C922C, PCA84C923A, PCA84C923C and PCA84C923D are members of the PCF84CXXXA CMOS family of microcontrollers and have been designed for use in universal infrared remote commander applications. The term PCA84C92X is used throughout this data sheet to refer to all devices in the range, differences between devices are shown in Table 1 and also highlighted in the text. In addition to the common functions of the PCF84CXXXA family of microcontrollers the PCA84C92X also provides:

- a Hardware Modulator that generates programmable pulse trains for driving an infrared LED
- an on-chip Coding Table specifically for the storage of code data
- a modified interrupt architecture that will wake-up the CPU from the Idle or Stop modes when any key is pressed
- a Watchdog Timer to prevent CPU lock-up.

The PCA84C923D has been designed as the emulation chip for both the PCA84C92X and the PCA84CX22 range of microcontrollers (both ranges being pin compatible).

Table 1 The PCA84C92X range of microcontrollers

FUNCTION	PCA84C923D	PCA84C923C	PCA84C923A	PCA84C922C	PCA84C922A
System ROM	8 kbytes	8 kbytes	8 kbytes	8 kbytes	8 kbytes
System RAM	256 bytes	256 bytes	256 bytes	128 bytes	128 bytes
Coding Table ROM	16 kbytes	16 kbytes	16 kbytes	8 kbytes	8 kbytes
Coding Table extension	up to 64 kbytes	no	no	no	no
Maximum number of keys	189	117	81	117	81
I/O	36	20	16	20	16
Emulation device	PCA84C923D	PCA84C923D	PCA84C923D	PCA84C923D	PCA84C923D
Package	VSO56	SO28	SO24 and SDIP24	SO28	SO24 and SDIP24

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84C922AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84C922AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84C922CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCA84C923AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84C923AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84C923CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCA84C923DT	VSO56	plastic very small outline package; 56 leads	SOT190-1

4 BLOCK DIAGRAMS

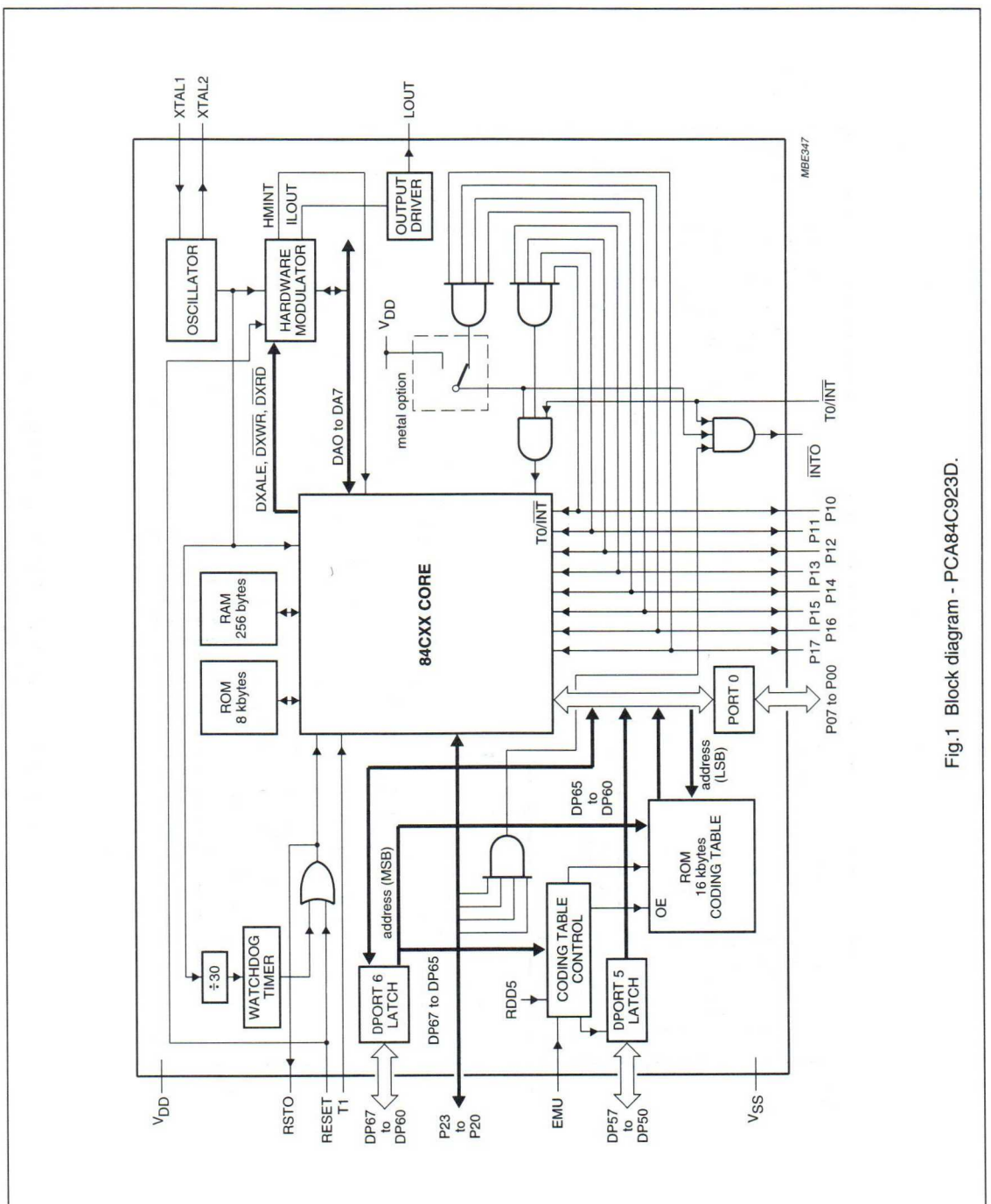


Fig.1 Block diagram - PCA84C923D.

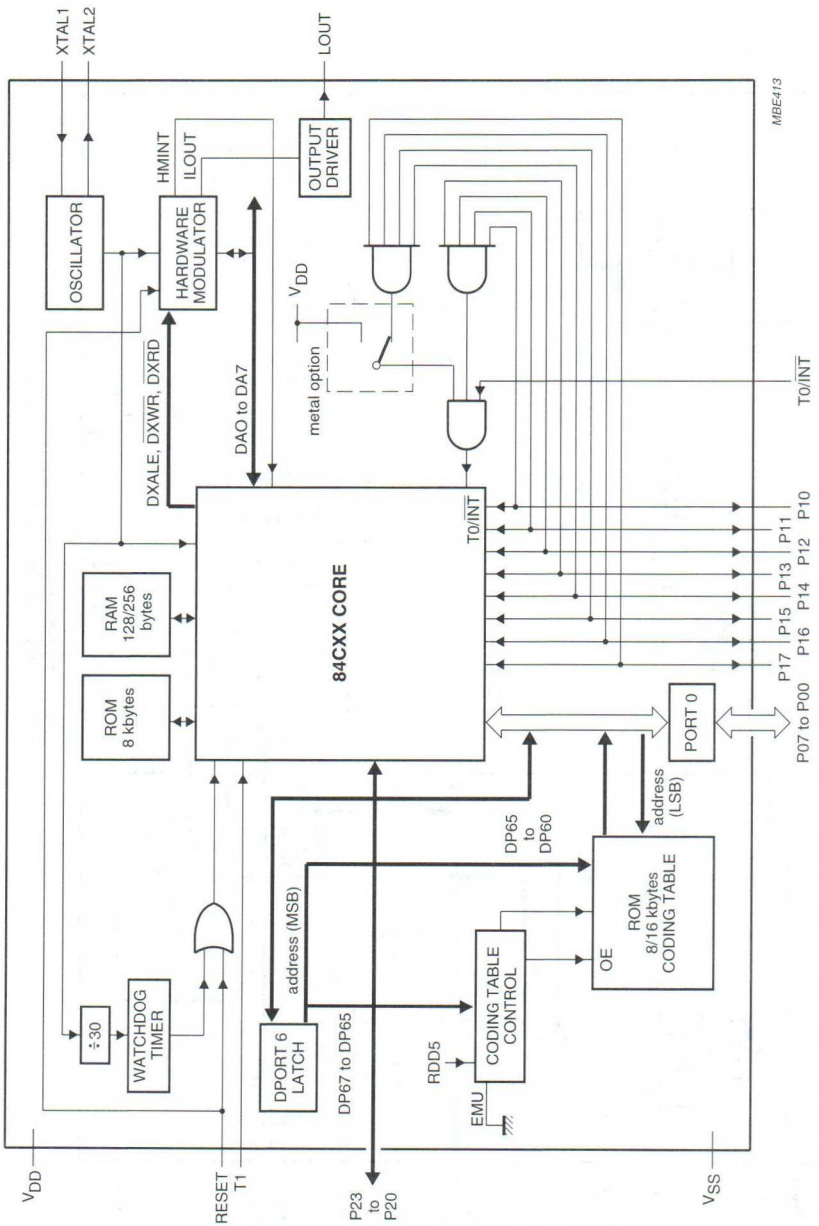


Fig.2 Block diagram - PCA84C922C and PCA84C923C.

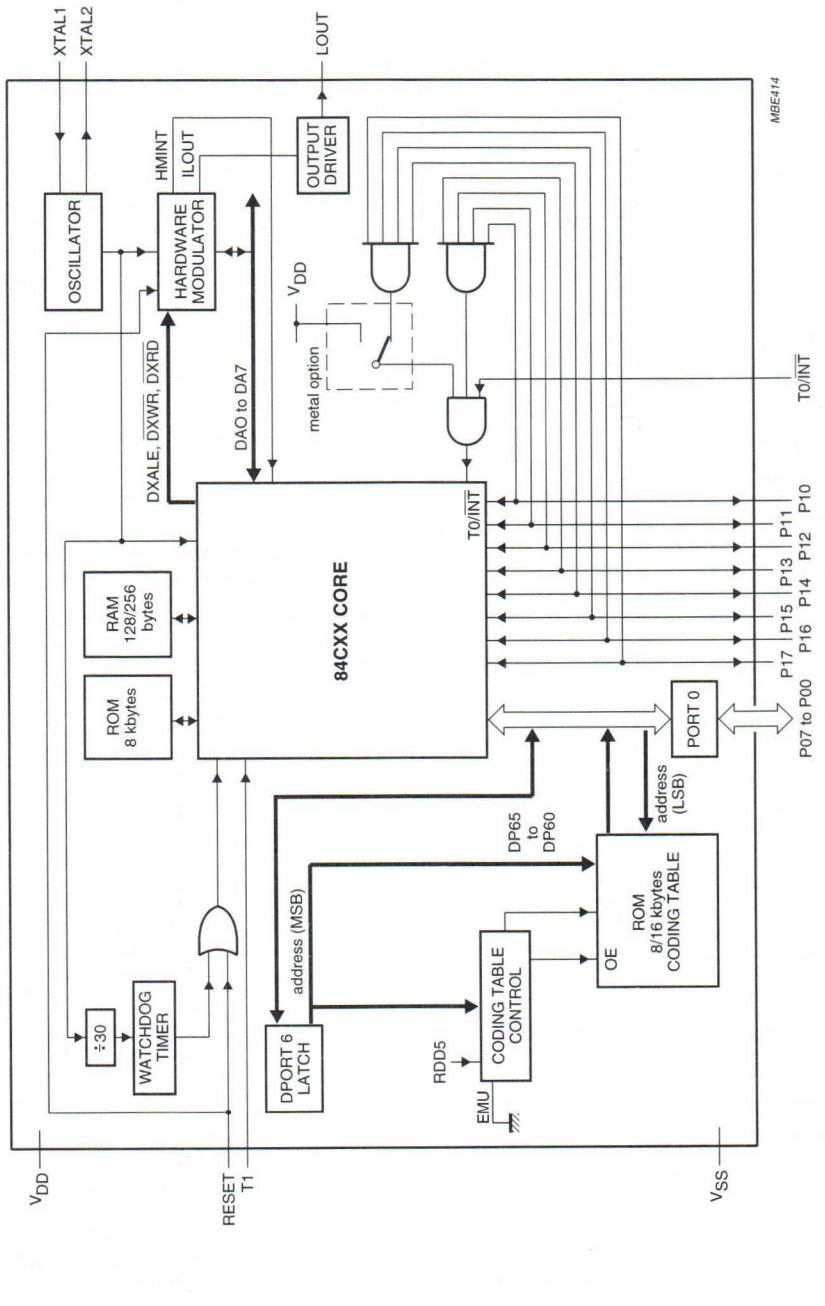


Fig.3 Block diagram - PCA84C922A and PCA84C923A.

5 PINNING INFORMATION

5.1 Pinning

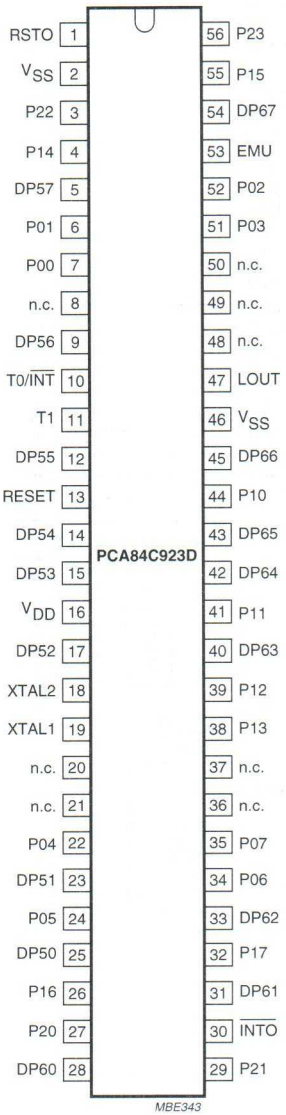


Fig.4 Pin configuration of PCA84C923D (VSO56).

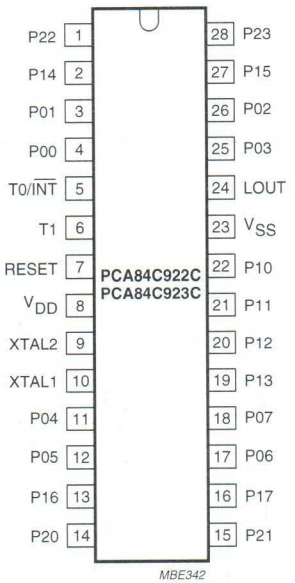


Fig.5 Pin configuration of PCA84C922C (SO28) and PCA84C923C (SO28).

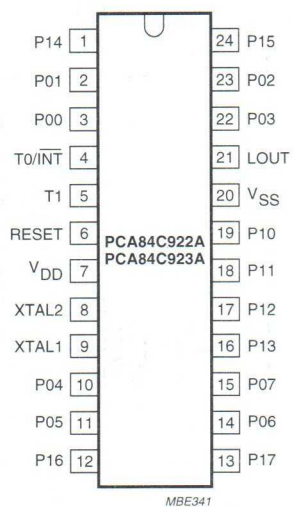


Fig.6 Pin configuration of PCA84C922A (SO24/SDIP24) and PCA84C923A (SO24/SDIP24).

5.2 Pin description

Table 2 PCA84C923D (VS056)

SYMBOL	PIN	DESCRIPTION
P00 to P07	7, 6, 52, 51, 22, 24, 34 and 35	Standard I/O Port lines, generally used for keypad scanning or for LSB address lines of coding table.
P10	44	Port line 10 or emulation $\overline{DXWR}$ signal input.
P11	41	Port line 11 or emulation $\overline{DXRD}$ signal input.
P12	39	Port line 12 or emulation DXALE signal input.
P13	38	Port line 13 or emulation $\overline{EXDI}$ signal input.
P14 to P17	4, 55, 26 and 32	Standard I/O port lines, generally used for keypad sensing, the wake-up function can be removed by mask option.
P20 to P23	27, 29, 3 and 56	Standard I/O port lines with 10 mA sink capability.
DP50 to DP57	25, 23, 17, 15, 14, 12, 9 and 5	Standard I/O port lines, generally used for the data bus of Coding Table.
DP60 to DP67	28, 31, 33, 40, 42, 43, 45 and 54	Standard I/O Port lines, generally used for keypad scanning or for MSB address lines of Coding Table.
RSTO	1	Used for emulation purposes only. This output is the result of the OR operation carried out internally on the RESET input and the Watchdog Timer reset and is connected to the RESET pin of the 84C00.
T0/$\overline{INT}$	10	Test pin T0 or external interrupt input.
T1	11	Test pin T1 or timer/counter input (T1).
RESET	13	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	18	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	19	
$\overline{INTO}$	30	Used for emulation purposes only and is connected to the T0/$\overline{INT}$ pin of the 84C00.
LOUT	47	Pulse train output pin, capable of sinking 30 mA.
EMU	53	Emulation mode control pin; for normal operation this pin is connected to V_{SS}.
V_{DD}	16	Power supply.
V_{SS}	2 and 46	Ground.

Table 3 PCA84C922C (SO28) and PCA84C923C (SO28)

SYMBOL	PIN	DESCRIPTION
P00 to P07	4, 3, 26, 25, 11, 12, 17, 18	Standard I/O port lines, generally used for keypad scanning or for LSB address byte of code data.
P10 to P17	22, 21, 20, 19, 2, 27, 13, 16	Standard I/O port lines, generally used for keypad sensing, the wake-up function of P14 to P17 can be removed by mask option.
P20 to P23	14, 15, 1, 28	Standard I/O port lines with 10 mA sink capability.
T0/$\overline{\text{INT}}$	5	Test pin T0 or external interrupt input.
T1	6	Test pin T1 or timer/counter input (T1).
RESET	7	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	9	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	10	
LOUT	24	Pulse train output pin, capable of sinking 30 mA.
V_{DD}	8	Power supply.
V_{SS}	23	Ground.

Table 4 PCA84C922A (SO24/SDIP24) and PCA84C923A (SO24/SDIP24)

SYMBOL	PIN	DESCRIPTION
P00 to P07	3, 2, 23, 22, 10, 11, 14, 15	Standard I/O port lines, generally used for keypad scanning or for LSB address byte of code data.
P10 to P17	19,18, 17, 16, 1, 24,12,13	Standard I/O port lines, generally used for keypad sensing, the wake-up function of P14 to P17 can be removed by mask option.
T0/$\overline{\text{INT}}$	4	Test pin T0 or external interrupt input.
T1	5	Test pin T1 or timer/counter input (T1).
RESET	6	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	8	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	9	
LOUT	21	Pulse train output pin, capable of sinking 30 mA.
V_{DD}	7	Power supply.
V_{SS}	20	Ground.

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1 FEATURES

- Display RAM: 256 × 12 bits
- Display character fonts: 128 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 16 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends upon the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address auto-post-increment when writing data
- Fast I²C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camcorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: −20 to +70 °C
- Package: SDIP24 or SO24.

2 GENERAL DESCRIPTION

The PCA8514 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I²C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camcorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8514P	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA8514T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

4 BLOCK DIAGRAM

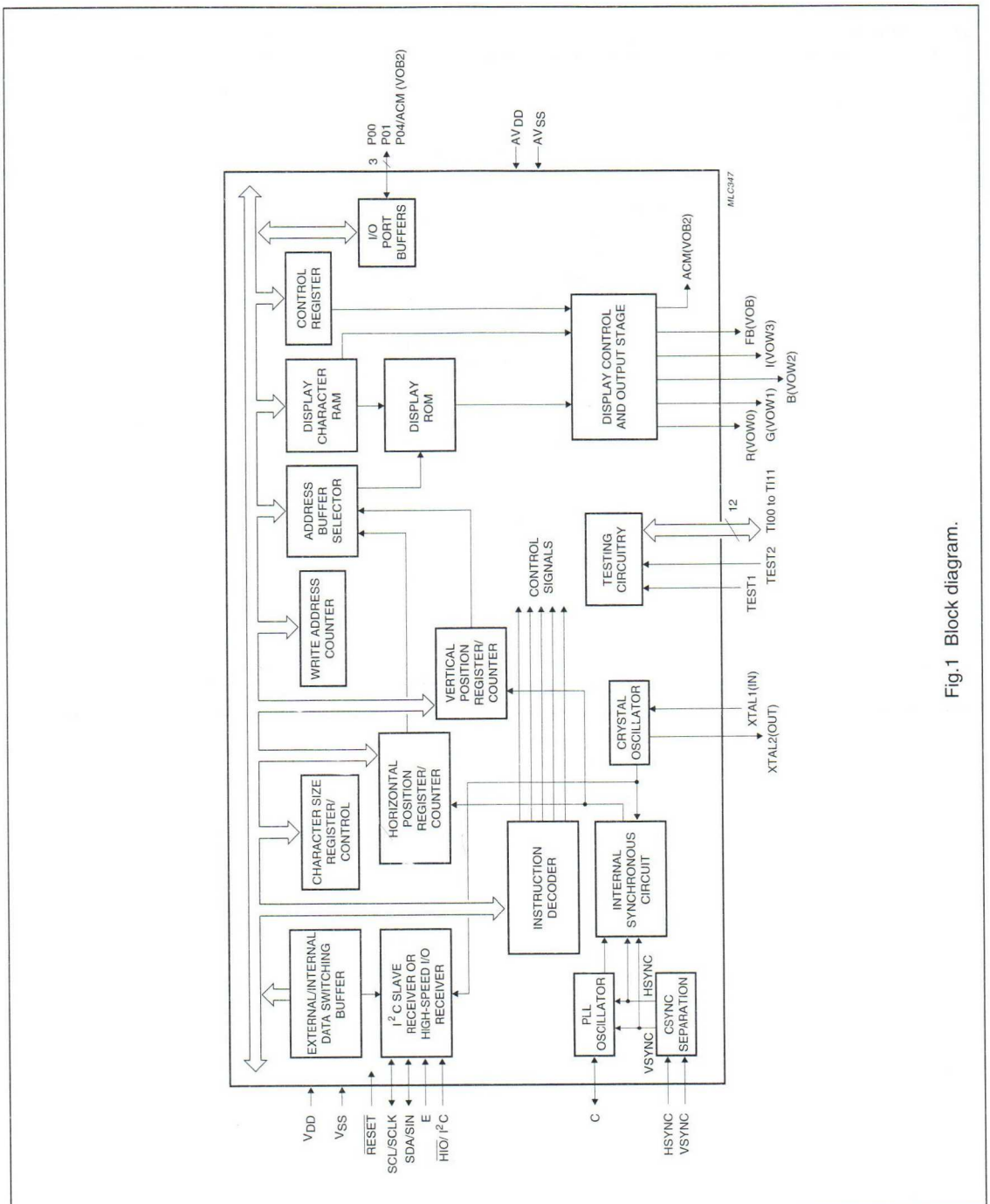


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

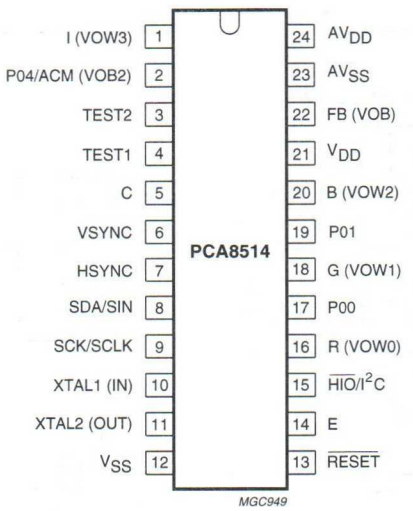


Fig.2 Pin configuration for SDIP24 and SO24.

5.2 Pin description

Table 1 SDIP24 and SO24 packages

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control.
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2).
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to V_{SS}.
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator.
VSYNC	6	I	Vertical synchronization input, active polarity programmable.
HSYNC	7	I	Horizontal synchronization input, active polarity programmable.
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface.
SCL/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface.
XTAL1 (IN)	10	I	System clock input.
XTAL2 (OUT)	11	O	System clock output.
V_{SS}	12	I	Ground, digital.
$\overline{RESET}$	13	I	Master reset input (active LOW).
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{HIO}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red.
P00	17	I/O	General purpose I/O Port 00.
G (VOW1)	18	O	Character output signal: VOW1 for Green.
P01	19	I/O	General purpose I/O Port 01.
B (VOW2)	20	O	Character output signal: VOW2 for Blue.
V_{DD}	21	I	Power supply, digital.
FB (VOB)	22	O	Fast Blanking output (VOB).
AV_{SS}	23	I	Ground, analog.
AV_{DD}	24	I	Power supply, analog.

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1 FEATURES

- Display RAM: 256 × 13 bits
- Display character fonts: 253 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 16 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends on the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address-auto-post increment when writing data
- Fast I²C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camrecorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: −20 to +70 °C
- Package: SDIP24 or SO24.

2 GENERAL DESCRIPTION

The PCA8515 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I²C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camrecorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8515P	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA8515T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

4 BLOCK DIAGRAM

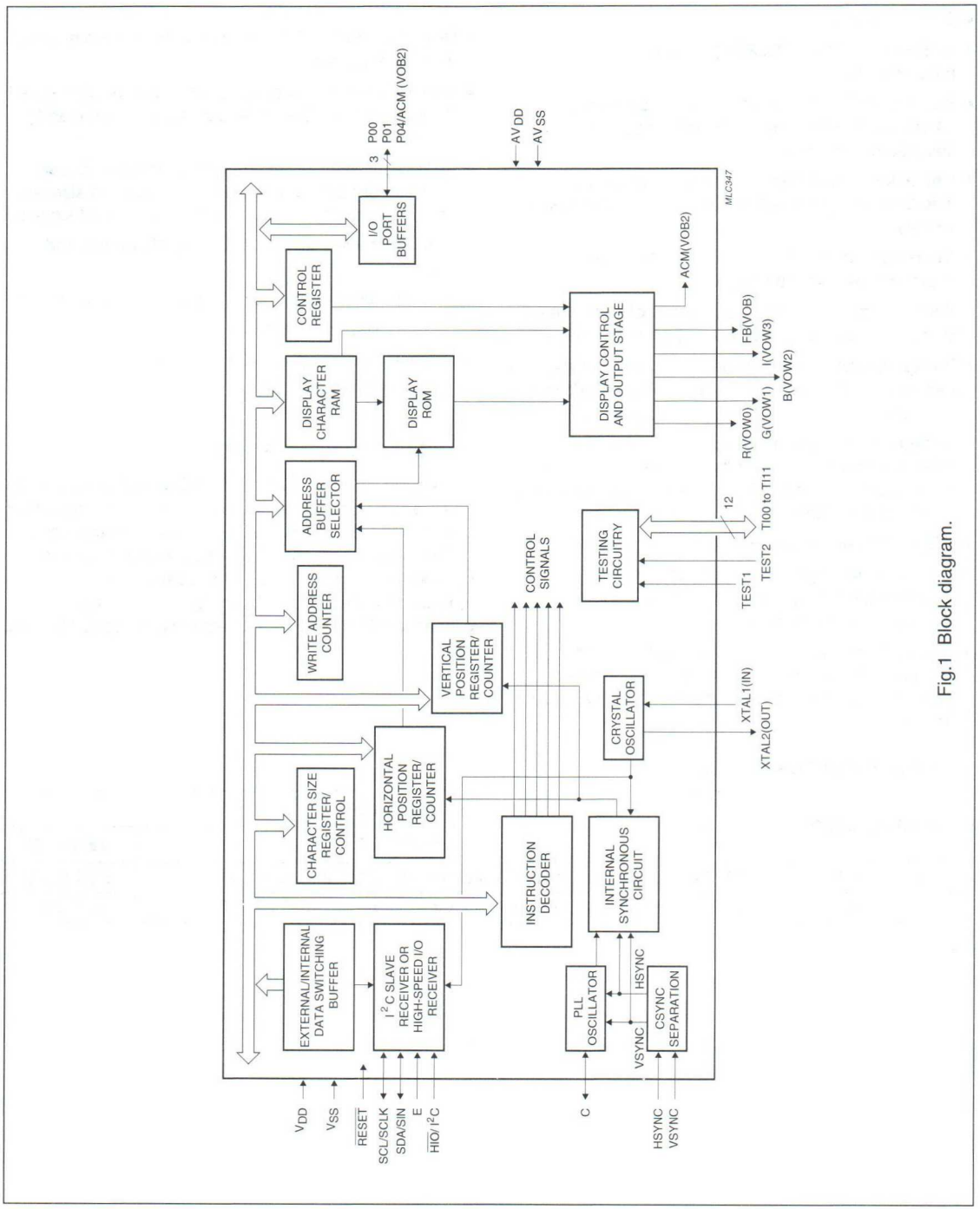


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

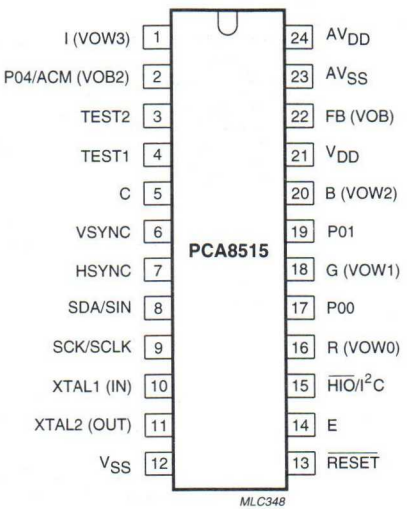


Fig.2 Pin configuration for SDIP24.

5.2 Pin description

Table 1 SDIP24 and SO24 packages

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control.
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2).
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to V_{SS}.
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator.
VSYNC	6	I	Vertical synchronization input, active polarity programmable.
HSYNC	7	I	Horizontal synchronization input, active polarity programmable.
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface.
SCK/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface.
XTAL1 (IN)	10	I	System clock input.
XTAL2 (OUT)	11	O	System clock output.
V_{SS}	12	I	Ground, digital.
$\overline{RESET}$	13	I	Master Reset input (active LOW).
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{HIO}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red.
P00	17	I/O	General purpose I/O Port 00.
G (VOW1)	18	O	Character output signal: VOW1 for Green.
P01	19	I/O	General purpose I/O Port 01.
B (VOW2)	20	O	Character output signal: VOW2 for Blue.
V_{DD}	21	I	Power supply, digital.
FB (VOB)	22	O	Fast Blanking output (VOB).
AV_{SS}	23	I	Ground, analog.
AV_{DD}	24	I	Power supply, analog.

Infrared remote control transmitter RC5 PCA8521

FEATURES

- RC5 protocol
- Maximum of:
  - 56 keys (20-pin version)
  - 30 keys (16-pin version)
- Option of multi-system or single system transmitter
  - Multi-system: maximum 8 systems, selection by key
  - Single system: maximum 8 different systems per IC, selection by jumper wire or switch
- Power-down and key wake-up
- High output current (≤ 45 mA)
- Oscillator frequency of 432 kHz or 4 MHz
- Multiple key protection
- Option of 25% or 33% duty factor
- Contained in DIP16, SO16, DIP20 or SO20 packages.

GENERAL DESCRIPTION

The PCA8521 can be used in infrared remote control transmitters. It generates output pulses, in accordance with the RC5 protocol, when a key is pressed. The IC does not contain a software programmable processor. However, it does contain a ROM in which the codes that have to be transmitted are stored. An example of an application diagram using a 20-pin IC is illustrated in Fig. 7. The oscillator frequency may be optionally chosen as 432 kHz or 4 MHz. For 432 kHz additional external capacitors must be connected. The capacitors for a 4 MHz oscillator is integrated. When a key in the key-matrix is pressed a drive line will be connected to a sense line. This causes the oscillator to start and a corresponding code will be generated conforming to the RC5 protocol.

Seven drive lines ($\overline{DR0}$ to $\overline{DR6}$) and eight sense lines (SN0 to SN7) may be connected via the key matrix to scan the keys (see Fig.1).

When two or more keys are activated simultaneously no transmission will take place.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8521FP	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-4
PCA8521FT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA8521BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCA8521BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

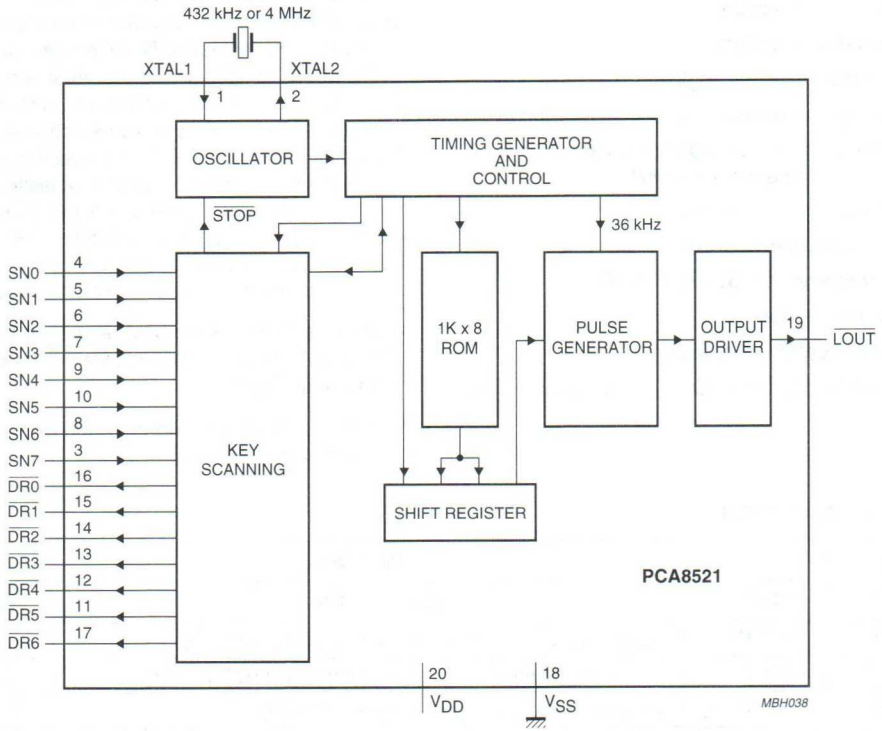


Fig.1 Block diagram (for DIP20 and SO20 packages).

PINNING

16-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN0	3	sense line 0 for key matrix
SN1	4	sense line 1 for key matrix
SN2	5	sense line 2 for key matrix
SN3	6	sense line 3 for key matrix
SN4	7	sense line 4 for key matrix
SN5	8	sense line 5 for key matrix
$\overline{DR4}$	9	drive line 4 for key matrix (active LOW)
$\overline{DR3}$	10	drive line 3 for key matrix (active LOW)
$\overline{DR2}$	11	drive line 2 for key matrix (active LOW)
$\overline{DR1}$	12	drive line 1 for key matrix (active LOW)
$\overline{DR0}$	13	drive line 0 for key matrix (active LOW)
V_{SS}	14	ground
$\overline{LOUT}$	15	output signal (active LOW)
V_{DD}	16	power supply

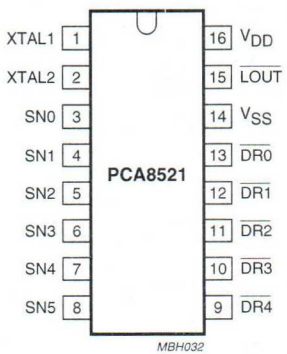


Fig.2 Pin configuration (DIP/SO16).

20-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN7	3	sense line 7 for key matrix
SN0	4	sense line 0 for key matrix
SN1	5	sense line 1 for key matrix
SN2	6	sense line 2 for key matrix
SN3	7	sense line 3 for key matrix
SN6	8	sense line 6 for key matrix
SN4	9	sense line 4 for key matrix
SN5	10	sense line 5 for key matrix
$\overline{DR5}$	11	drive line 5 for key matrix (active LOW)
$\overline{DR4}$	12	drive line 4 for key matrix (active LOW)
$\overline{DR3}$	13	drive line 3 for key matrix (active LOW)
$\overline{DR2}$	14	drive line 2 for key matrix (active LOW)
$\overline{DR1}$	15	drive line 1 for key matrix (active LOW)
$\overline{DR0}$	16	drive line 0 for key matrix (active LOW)
$\overline{DR6}$	17	drive line 6 for key matrix (active LOW)
V_{SS}	18	ground
$\overline{LOUT}$	19	output signal (active LOW)
V_{DD}	20	power supply

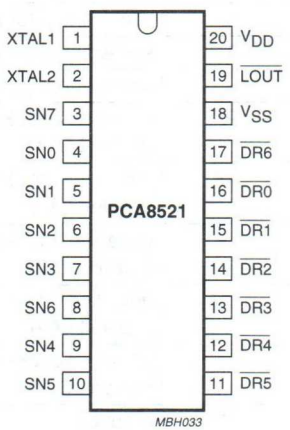


Fig.3 Pin configuration (DIP/SO20).

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1 INTRODUCTION

This data sheet describes the shared properties of the PCF84CxxxA family of microcontrollers. The family currently consists of:

- PCF84C00
- PCF84C12A; 22A; 42A
- PCF84C21A; 41A; 81A
- PCF84C85A
- PCF84C122; 222; 422; 622; 822
- PCF84C44x; 64x; 84x
- PCF84C846.

For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device. Data sheets can be found in *"Data Handbook IC14, "8048-based 8-bit microcontrollers"*.

The PCD33xxA family of microcontrollers has similar characteristics to the PCF84CxxxA family, but with lower minimum operating voltage, DTMF/modem/musical tone generation and (for most devices) on-chip EEPROM. This family should be considered for telecom-specific applications. Please refer to the *"PCD33xxA family"* data sheet.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 2 or 3 single-level vectored interrupts: external, timer/event counter, (I^2C-bus/derivative)
- Two test inputs, one of which also serves as the external interrupt input
- I^2C-bus serial data interface (most devices)
- Derivative logic (most devices)
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 2.5 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C
- Manufactured in silicon gate CMOS process.

3 GENERAL DESCRIPTION

The PCF84CxxxA family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. Most devices feature I^2C-bus compatibility. The instruction set is based on that of the well-known MAB8048. Some of the devices have functional equivalents in the MAB84xx family of NMOS controllers. Where the lower power consumption and higher speed of CMOS provide advantages, the PCF84CxxxA devices can be used as direct replacements for their MAB84xx equivalents.

A range of prototyping devices with external program memory and 'Piggy-backs', as well as emulation probes and prototyping systems are available.

4 BLOCK DIAGRAM

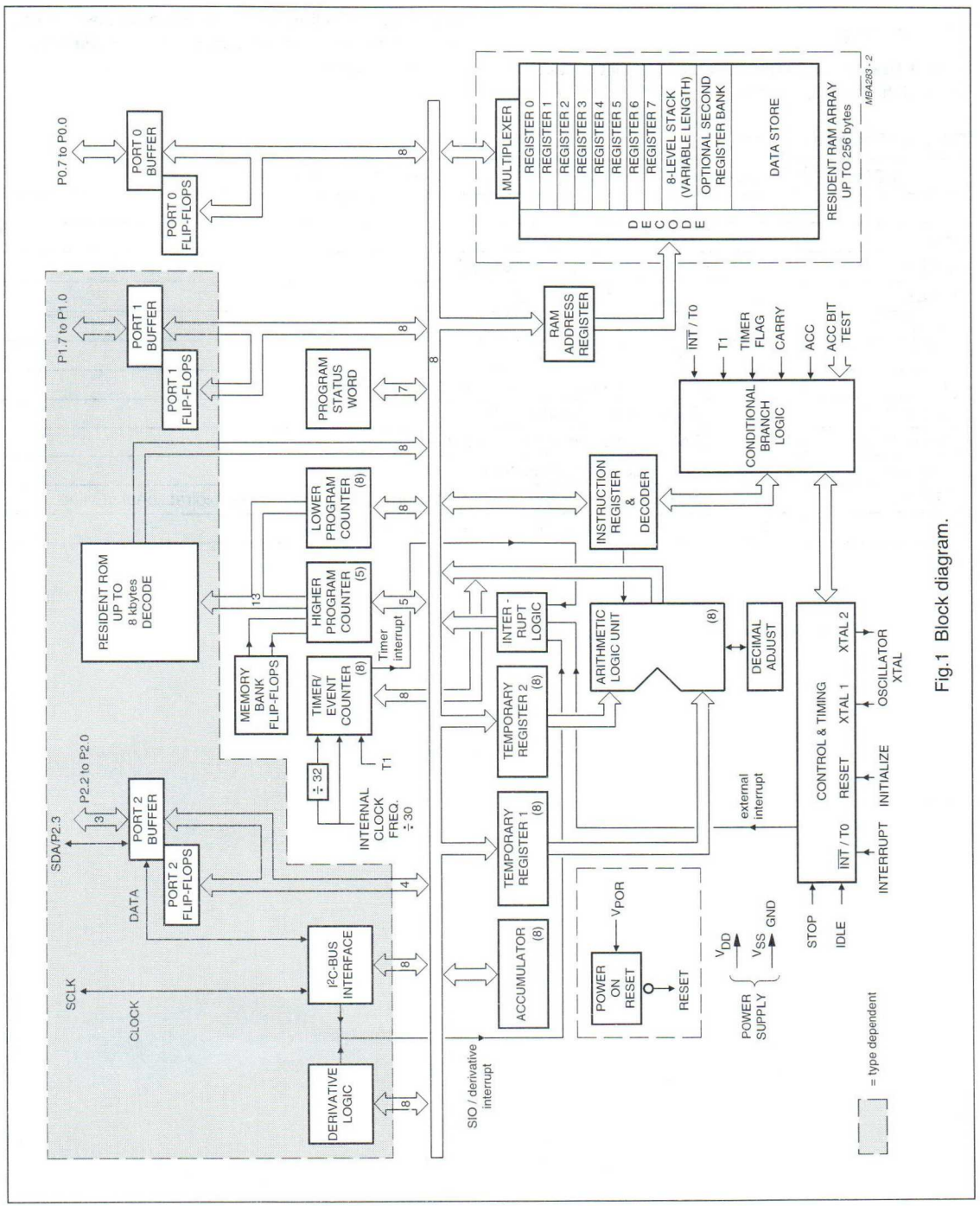


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

For individual pinning configurations consult the data sheet of the specific device.

5.2 Pin description

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	ground
V_{DD}	P	positive supply voltage
XTAL1	I	crystal oscillator/external clock input
XTAL2	O	crystal oscillator output
RESET	I	Reset input
$\overline{INT}$/T0	I	Interrupt/Test 0 input
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.2	I/O	Port 2: quasi-bidirectional I/O lines
SDA/P2.3	I/O	bidirectional data line of the I^2C-bus interface/Port 2: quasi-bidirectional I/O line
SCLK	I/O	bidirectional clock line of the I^2C-bus interface

LIne MEmory noise Reduction IC (LIMERIC)

SAA4945H

FEATURES

- 2-D adaptive vertically recursive noise reduction
- Noise reduction for Y, U and V signals in 4 : 1 : 1 format
- Single 5 V ±10% power supply
- Communication by means of serial communication protocol 83C654 (SNERT bus)
- Via SNERT bus, 10 different types of noise reduction selectable; the noise reduction function can also be disabled
- Phase relation write enable input/output signal simultaneously switchable over one clock period w.r.t. input/output samples
- 8-bit wide data processing for Y, U and V; in unsigned format (Y signal) and in 2's complement (U and V signals)
- One fixed line locked clock operation frequency up to 16 MHz (typical)
- Exactly one line delay.

GENERAL DESCRIPTION

The SAA4945H, LIMERIC (LIne MEmory noise Reduction IC) is a 2-D recursive noise reduction filter for both luminance and colour difference signals. The noise reduction is automatically adapted to the global noise level in the image. Ten different preferences of noise reduction can be set using a synchronous receiver transmitter bus; SNERT (Synchronous No parity Eight bit Receive Transmit) bus. Alternatively, the noise reduction can be switched off. The LIMERIC is generally placed directly after the ADC in the feature box and works fully in the $1f_h$ (50/60 Hz) domain.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 29 and 30)		4.5	5.0	5.5	V
I_{DD}	supply current		–	70	–	mA
P	power dissipation		–	350	–	mW
f_{CLK}	clock frequency	±7%; note 1	10	16	17.1	MHz
f_{SNERT}	bus clock frequency		–	–	1	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

Note

1. Maximum number of clocks per line is 1024.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4945H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

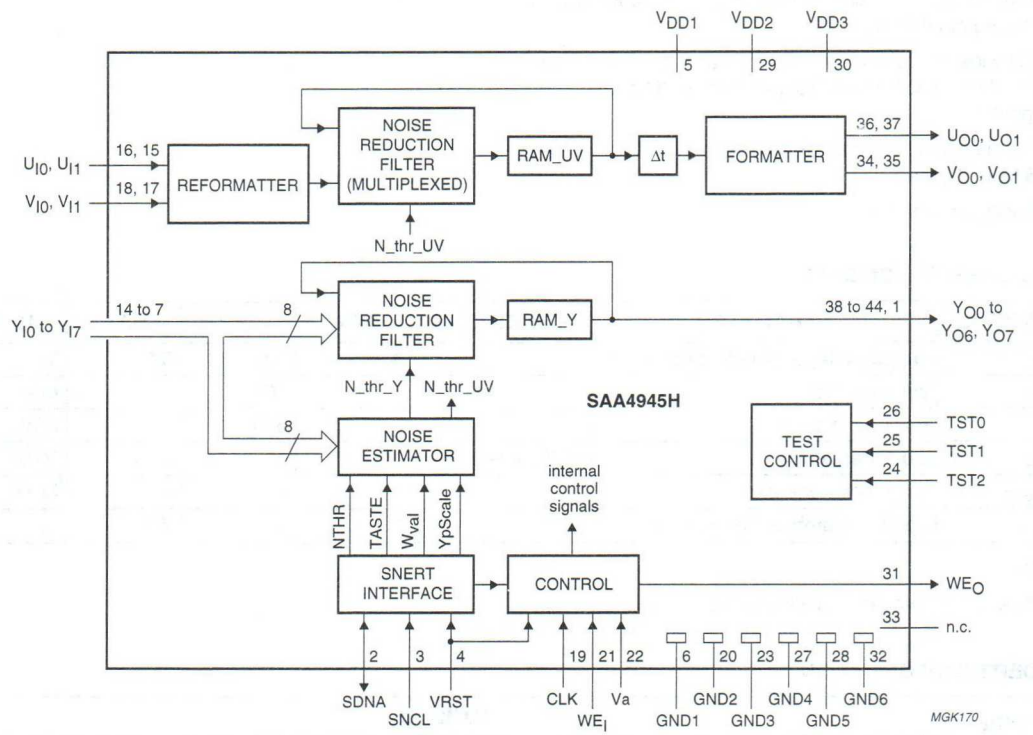


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Y_{O7}	1	output	luminance output bit 7
SNDA	2	input/output	data from interface SNERT bus
SNCL	3	input	clock from interface SNERT bus
VRST	4	input	reset in the vertical blanking interval
V_{DD1}	5	supply	supply voltage 1
GND1	6	ground	ground 1
Y_{I7}	7	input	luminance input bit 7 from analog-to-digital converter
Y_{I6}	8	input	luminance input bit 6 from analog-to-digital converter
Y_{I5}	9	input	luminance input bit 5 from analog-to-digital converter
Y_{I4}	10	input	luminance input bit 4 from analog-to-digital converter
Y_{I3}	11	input	luminance input bit 3 from analog-to-digital converter
Y_{I2}	12	input	luminance input bit 2 from analog-to-digital converter
Y_{I1}	13	input	luminance input bit 1 from analog-to-digital converter
Y_{I0}	14	input	luminance input bit 0 from analog-to-digital converter
U_{I1}	15	input	U input bit 1 from analog-to-digital converter
U_{I0}	16	input	U input bit 0 from analog-to-digital converter
V_{I1}	17	input	V input bit 1 from analog-to-digital converter
V_{I0}	18	input	V input bit 0 from analog-to-digital converter
CLK	19	input	master clock
GND2	20	ground	ground 2
WE_I	21	input	write enable input
Va	22	input	vertical blanking pulse
GND3	23	ground	ground 3
TST2	24	input	test pin 2
TST1	25	input	test pin 1
TST0	26	input	test pin 0
GND4	27	ground	ground 4
GND5	28	ground	ground 5
V_{DD2}	29	supply	supply voltage 2
V_{DD3}	30	supply	supply voltage 3
WE_O	31	output	write enable output
GND6	32	ground	ground 6
n.c.	33	–	not connected
V_{O0}	34	output	V output bit 0
V_{O1}	35	output	V output bit 1
U_{O0}	36	output	U output bit 0
U_{O1}	37	output	U output bit 1
Y_{O0}	38	output	luminance output bit 0
Y_{O1}	39	output	luminance output bit 1
Y_{O2}	40	output	luminance output bit 2

SYMBOL	PIN	TYPE	DESCRIPTION
Y_{O3}	41	output	luminance output bit 3
Y_{O4}	42	output	luminance output bit 4
Y_{O5}	43	output	luminance output bit 5
Y_{O6}	44	output	luminance output bit 6

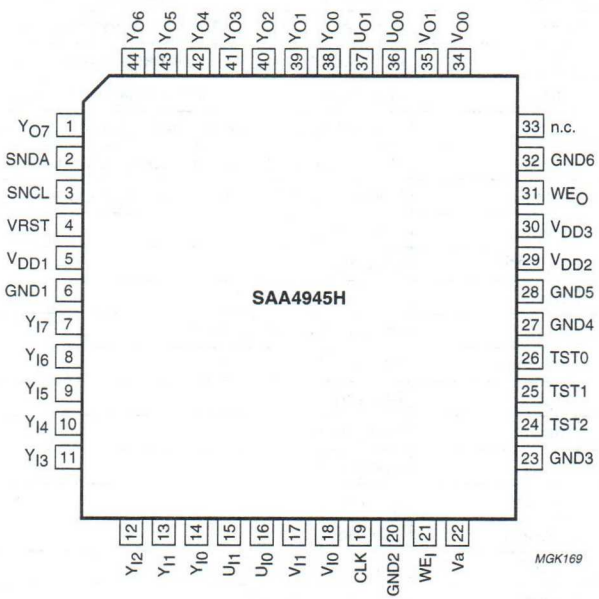


Fig.2 Pin configuration.

Progressive scan-Zoom and Noise reduction IC (PROZONIC)

SAA4990H

FEATURES

- Progressive scan conversion (262.5 to 525 or 312.5 to 625 lines/field)
- Field rate up-conversion (50 to 100 Hz or 60 to 120 Hz)
- Line flicker reduction
- Noise and cross-colour reduction
- Variable vertical sample rate conversion
- Movie phase detection
- Synchronous No parity Eight bit Reception and Transmission (SNERT) interface.

GENERAL DESCRIPTION

The Progressive scan-Zoom and Noise reduction IC, abbreviated as PROZONIC, is designed for applications together with:

SAA4951WP Economy Controller (ECO3)

SAA4952H (memory controller)

SAA7158WP Back END IC (BENDIC)

SAA4995WP PANorama IC (PANIC)

SAA4970T ECOnomical video processing Back END IC (ECOBENDIC)

TMS4C2970/71 (serial field memories)

TDA8755/8753A (A/D converter 4 : 1 : 1 format)

83C652/54 type of microcontroller.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.5	V
T_{amb}	operating ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4990H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

BLOCK DIAGRAM

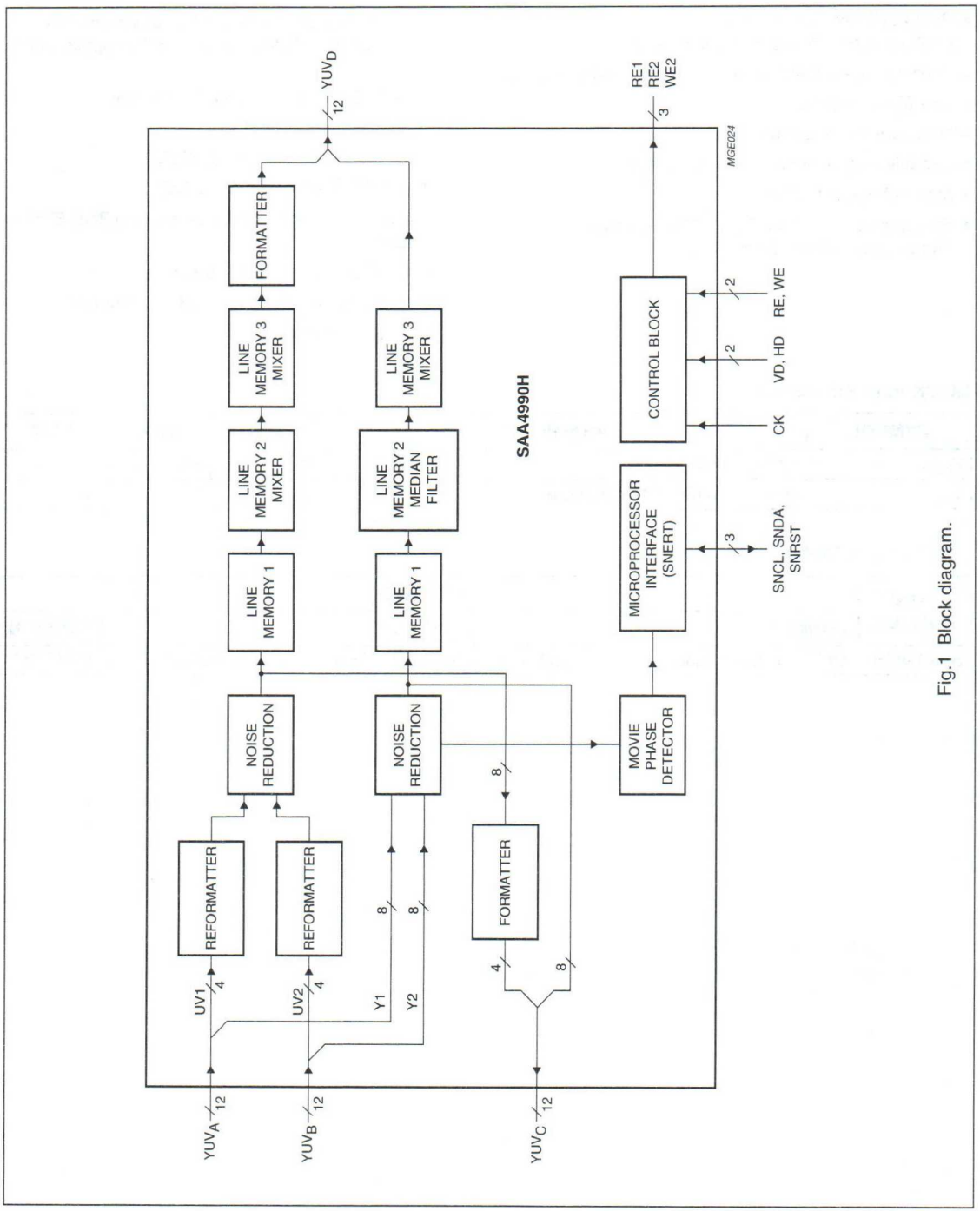


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
TEST1/AP	1	input	action pin for testing, to be connected to V_{SS}
TEST2/SP	2	input	shift pin for testing, to be connected to V_{SS}
RE1	3	output	read enable to FM1
V_{SS1}	4	ground	ground 1
V_{DD1}	5	supply	supply voltage 1
YUV_{C7}	6	output	Y bit 7 to FM2
YUV_{C6}	7	output	Y bit 6 to FM2
YUV_{C5}	8	output	Y bit 5 to FM2
YUV_{C4}	9	output	Y bit 4 to FM2
YUV_{C3}	10	output	Y bit 3 to FM2
V_{SS2}	11	ground	ground 2
V_{DD2}	12	supply	supply voltage 2
YUV_{C2}	13	output	Y bit 2 to FM2
YUV_{C1}	14	output	Y bit 1 to FM2
YUV_{C0}	15	output	Y bit 0 to FM2
YUV_{C11}	16	output	UV bit 3 to FM2
YUV_{C10}	17	output	UV bit 2 to FM2
YUV_{C9}	18	output	UV bit 1 to FM2
YUV_{C8}	19	output	UV bit 0 to FM2
CK	20	input	master clock, nominal 27 or 32 MHz
V_{SS3}	21	ground	ground 3
V_{DD3}	22	supply	supply voltage 3
WE2	23	output	write enable to FM2
RE2	24	output	read enable to FM2
YUV_{B8}	25	input	UV bit 0 from FM2
YUV_{B9}	26	input	UV bit 1 from FM2
YUV_{B10}	27	input	UV bit 2 from FM2
YUV_{B11}	28	input	UV bit 3 from FM2
YUV_{B0}	29	input	Y bit 0 from FM2
YUV_{B1}	30	input	Y bit 1 from FM2
YUV_{B2}	31	input	Y bit 2 from FM2
YUV_{B3}	32	input	Y bit 3 from FM2
V_{DD4}	33	supply	supply voltage 4
V_{SS4}	34	ground	ground 4
YUV_{B4}	35	input	Y bit 4 from FM2
YUV_{B5}	36	input	Y bit 5 from FM2
YUV_{B6}	37	input	Y bit 6 from FM2
YUV_{B7}	38	input	Y bit 7 from FM2
RE	39	input	master read enable
VD	40	input	field frequent reset, vertical display

SYMBOL	PIN	TYPE	DESCRIPTION
HD	41	input	horizontal reference signal
YUV_{D8}	42	output	UV bit 0
YUV_{D9}	43	output	UV bit 1
YUV_{D10}	44	output	UV bit 2
V_{DD5}	45	supply	supply voltage 5
V_{SS5}	46	ground	ground 5
YUV_{D11}	47	output	UV bit 3
YUV_{D0}	48	output	Y bit 0
YUV_{D1}	49	output	Y bit 1
YUV_{D2}	50	output	Y bit 2
V_{DD6}	51	supply	supply voltage 6
V_{SS6}	52	ground	ground 6
YUV_{D3}	53	output	Y bit 3
YUV_{D4}	54	output	Y bit 4
YUV_{D5}	55	output	Y bit 5
YUV_{D6}	56	output	Y bit 6
YUV_{D7}	57	output	Y bit 7
V_{DD7}	58	supply	supply voltage 7
V_{SS7}	59	ground	ground 7
SNRST	60	input	field frequent reset from microcontroller; reset for SNERT interface
SNDA	61	I/O	data for SNERT interface
SNCL	62	input	clock for SNERT interface
AUX	63	output	spare output from line-sequencer
H_O	64	output	output hold to e.g. LC display
n.c.	65	–	not connected
n.c.	66	–	not connected
YUV_{A7}	67	input	Y bit 7 from FM1
YUV_{A6}	68	input	Y bit 6 from FM1
YUV_{A5}	69	input	Y bit 5 from FM1
YUV_{A4}	70	input	Y bit 4 from FM1
YUV_{A3}	71	input	Y bit 3 from FM1
YUV_{A2}	72	input	Y bit 2 from FM1
V_{SS8}	73	ground	ground 8
V_{DD8}	74	supply	supply voltage 8
YUV_{A1}	75	input	Y bit 1 from FM1
YUV_{A0}	76	input	Y bit 0 from FM1
YUV_{A11}	77	input	UV bit 3 from FM1
YUV_{A10}	78	input	UV bit 2 from FM1
YUV_{A9}	79	input	UV bit 1 from FM1
YUV_{A8}	80	input	UV bit 0 from FM1

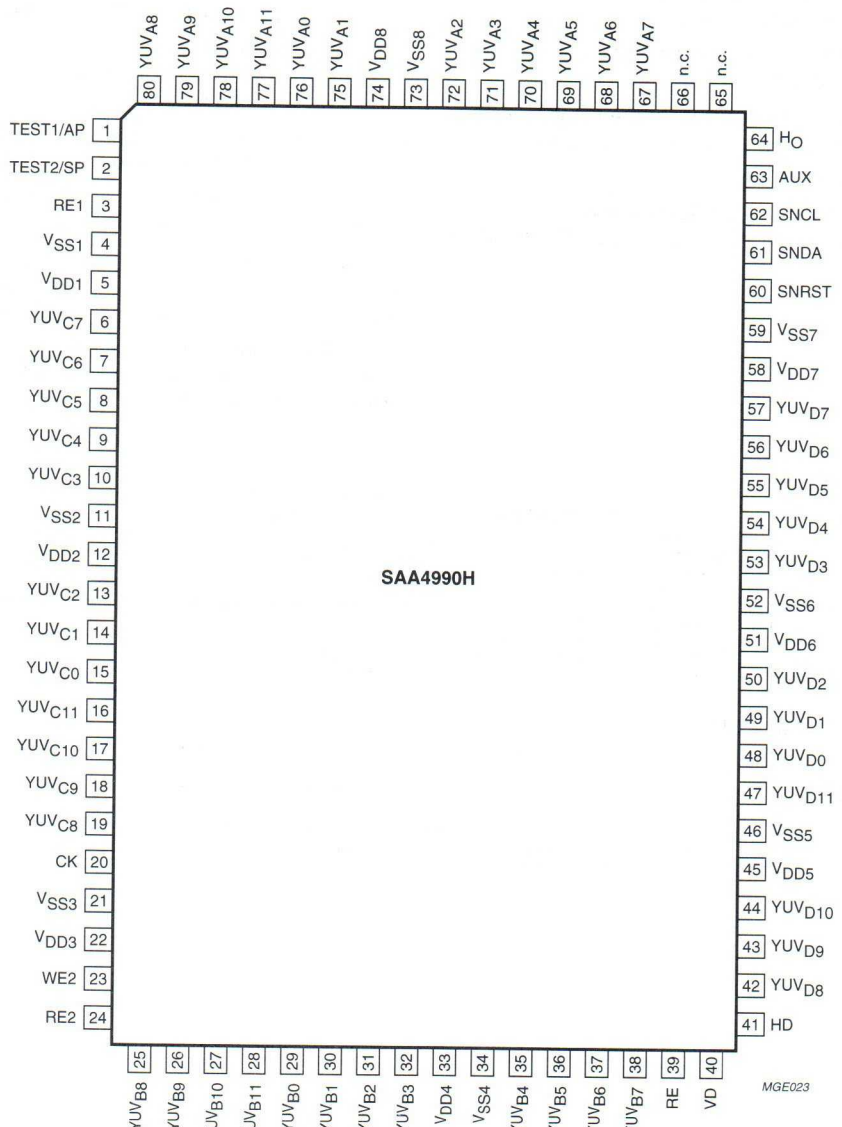


Fig.2 Pin configuration.

PANorama-IC (PAN-IC) SAA4995WP

FEATURES

- Horizontal sample rate conversion in both zoom and compress direction, with a sample rate conversion factor between 0.5 and 2 (in 384 steps)
- Dynamic sample rate conversion for panorama mode display e.g. 4 : 3 material on a 16 : 9 display
- Dynamic sample rate conversion for amaronap mode display of e.g. 16 : 9 material on a 4 : 3 display
- Operates with $1f_h$ and $2f_h$
- Programmable via microcontroller SNERT (Synchronous No parity Eight bit Receive Transmit) bus.

GENERAL DESCRIPTION

The PAN-IC is an add-on IC to be used, for example, between analog-to-digital conversion and a serial (field) memory. The device performs the following tasks:

- Linear horizontal sample rate conversion in both zoom and compress direction, with a sample rate conversion factor between 0.5 and 2
- Dynamic sample rate conversion for panorama mode display of e.g. 4 : 3 material on a 16 : 9 display
- Dynamic sample rate conversion for amaronap mode display of e.g. 16 : 9 material on a 4 : 3 display.

The PAN-IC has the ability to increase the data rate from the ADC to a maximum of twice the data rate at the output. To achieve this a clock rate at twice the normal output clock rate is needed to write data to the memory.
All actions to generate a lower data rate, produces disable cycles in Write Enable (WE).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	110	–	mA
f_{CLK}	operating clock frequency	–	–	33	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4995WP	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

BLOCK DIAGRAM

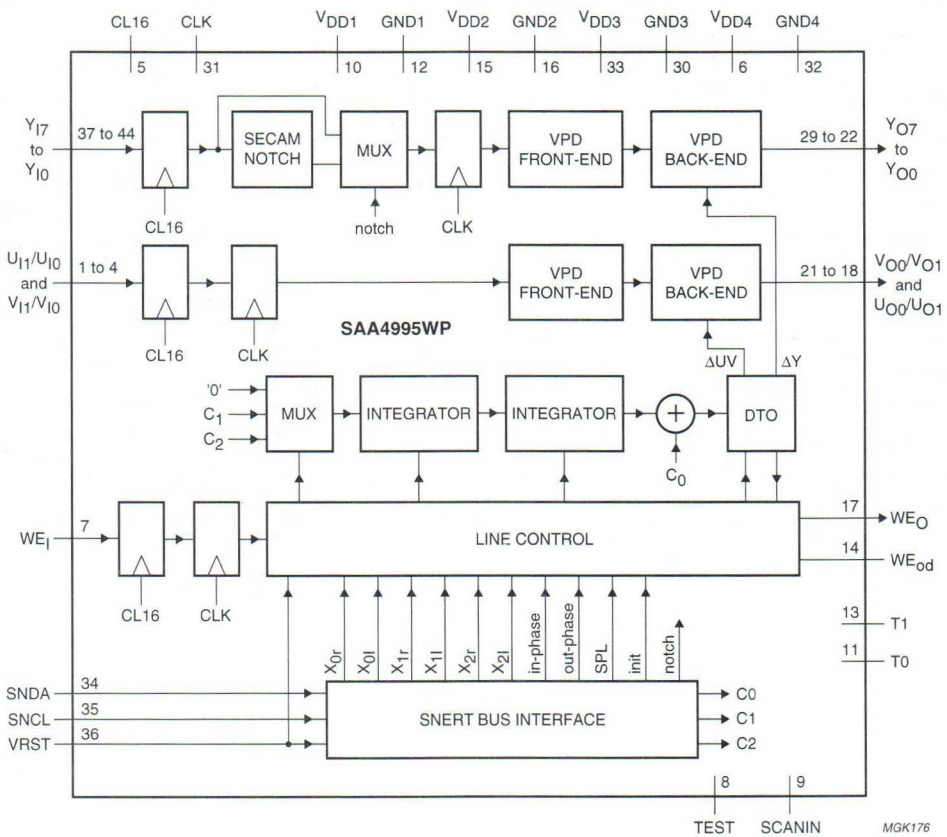


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
U_{I1}	1	U input bit 1
U_{I0}	2	U input bit 0
V_{I1}	3	V input bit 1
V_{I0}	4	V input bit 0
CL16	5	half system clock
V_{DD4}	6	supply voltage 4
WE_I	7	write enable input
TEST	8	test mode switch
SCANIN	9	input for scan chain
V_{DD1}	10	supply voltage 1
T0	11	test mode switch 0
GND1	12	ground 1
T1	13	test mode switch 1
WE_{od}	14	write enable odd samples
V_{DD2}	15	supply voltage 2
GND2	16	ground 2
WE_O	17	write enable output
V_{O0}	18	V output bit 0
V_{O1}	19	V output bit 1
U_{O0}	20	U output bit 0
U_{O1}	21	U output bit 1
Y_{O0}	22	luminance output bit 0
Y_{O1}	23	luminance output bit 1

SYMBOL	PIN	DESCRIPTION
Y_{O2}	24	luminance output bit 2
Y_{O3}	25	luminance output bit 3
Y_{O4}	26	luminance output bit 4
Y_{O5}	27	luminance output bit 5
Y_{O6}	28	luminance output bit 6
Y_{O7}	29	luminance output bit 7
GND3	30	ground 3
CLK	31	system clock
GND4	32	ground 4
V_{DD3}	33	supply voltage 3
SNDA	34	data input from interface SNERT bus
SNCL	35	clock input from interface SNERT bus
VRST	36	reset input in the vertical blanking interval
Y_{I7}	37	luminance input bit 7
Y_{I6}	38	luminance input bit 6
Y_{I5}	39	luminance input bit 5
Y_{I4}	40	luminance input bit 4
Y_{I3}	41	luminance input bit 3
Y_{I2}	42	luminance input bit 2
Y_{I1}	43	luminance input bit 1
Y_{I0}	44	luminance input bit 0

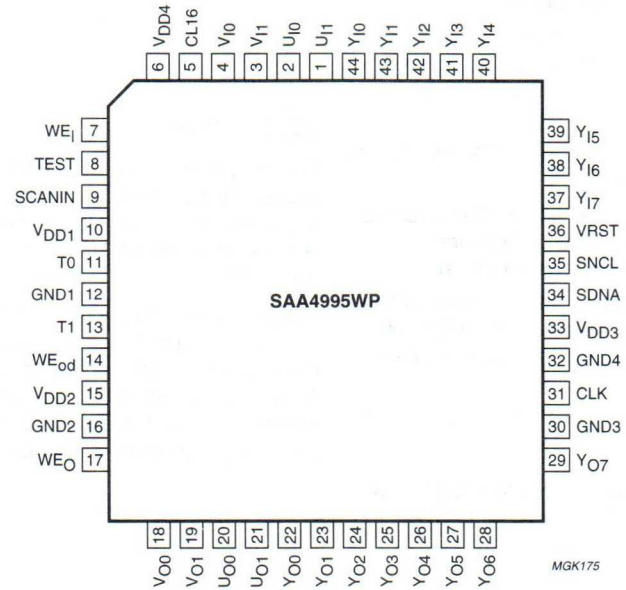


Fig.2 Pin configuration.

Integrated VIP and teletext decoder (IVT1.1X)

SAA5254

FEATURES

- Complete teletext decoder including page memory and FASTEXT links in a 40-pin DIP package
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and language option is readable via I²C-bus
- 100% hardware compatible with the SAA5244A; plug-in replacement and extra market
- 100% hardware compatible with the SAA5244A, except if the special OSD symbols were used with the SAA5244A, except ROM identification number
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5280 and the SAA5249, making one hardware solution for the full range
- Low software overhead for the control microprocessor
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Separate text and video signal quality detectors.

DESCRIPTION

The Integrated VIP and Teletext decoder (IVT1.1X) is designed to decode 625-line based World System Teletext transmissions. This single-chip teletext decoder hardware is based on the SAA5244A with which it is completely compatible.

Like the SAA5244A the device contains all the hardware necessary to decode the teletext, but the SAA5254 also contains extra hardware to process the extension packet 26 characters automatically, extending the markets to which the TV chassis can be shipped and opening the possibility of many more language options.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5254P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
V_{video}	video voltage amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C

BLOCK DIAGRAM

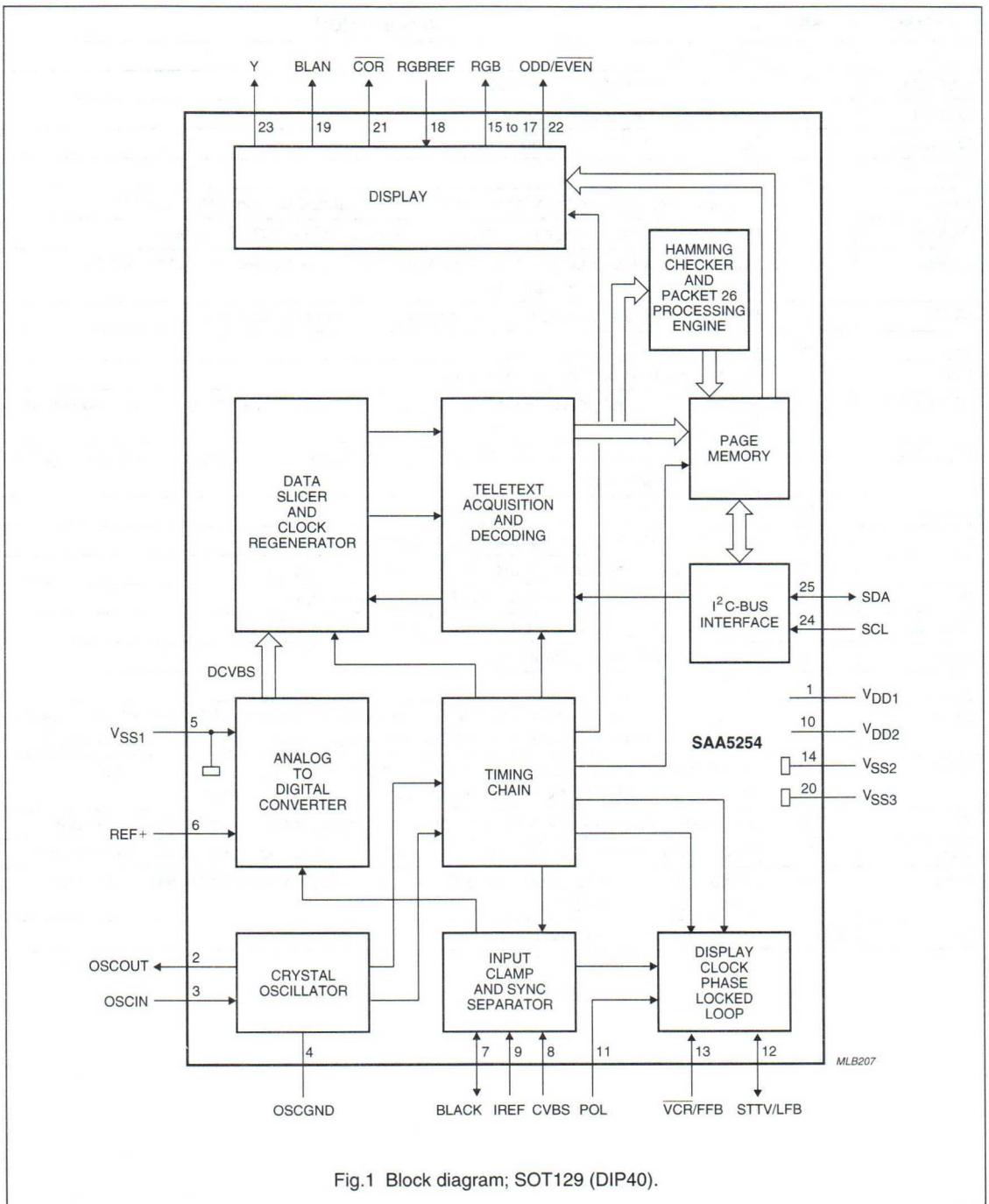


Fig.1 Block diagram; SOT129 (DIP40).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD1}	1	+5 V supply 1
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS1}	5	0 V ground 1
REF+	6	Positive reference voltage for the ADC. This pin should be connected to +5 V.
BLACK	7	Video black level storage pin, connected to ground via a 100 nF capacitor.
CVBS	8	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	Reference current input pin, connected to ground via a 27 kΩ resistor.
V_{DD2}	10	+5 V supply 2
POL	11	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	13	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	14	0 V ground 2
R	15	Dot rate character output of the RED colour information.
G	16	Dot rate character output of the GREEN colour information.
B	17	Dot rate character output of the BLUE colour information.
RGBREF	18	DC input voltage to define the output high level on the RGB pins.
BLAN	19	Dot rate fast blanking output.
V_{SS3}	20	0 V ground 3
$\overline{COR}$	21	Programmable active LOW output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output.
ODD/$\overline{EVEN}$	22	25 Hz output synchronized with the CVBS inputs field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
Y	23	Dot rate character output of teletext foreground colour information; open drain output.
SCL	24	Serial clock input for the I^2C-bus. It can still be driven during power-down of the device.
SDA	25	Serial input/output data port for the I^2C-bus; open drain output. It can still be driven during power-down of the device.
i.c.	26 to 40	Internally connected. Must be left open-circuit in application.

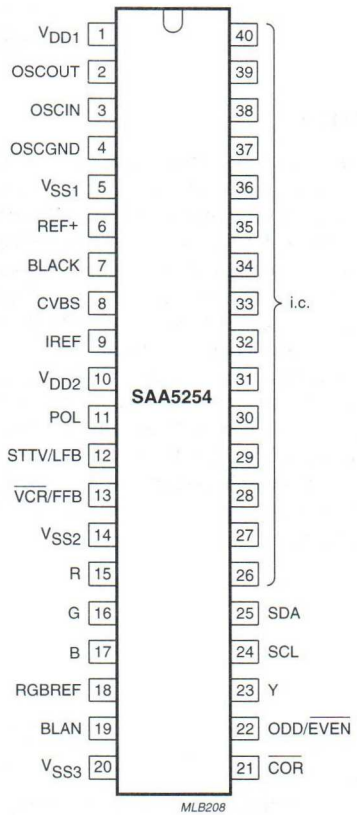


Fig.2 Pin configuration; SOT129 (DIP40).

Integrated Video input processor and Teletext decoder (IVT1.8*)

SAA5281

FEATURES

- Complete Teletext and VPS decoding in a single package
- Built-in 8K × 8 memory for up to 8 page storage
- Enhanced mode allows 7 Fastext pages and 8 pages of TOP to be captured
- Ability to request only subtitle pages
- Acquisition and decoding of VPS data
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data
- Software and hardware compatible with SAA5246 and SAA5248
- Meshing display within boxes
- Separate data checking algorithms and pointers for each acquisition channel
- 24 : 18 Hamming checker
- Automatic packet 26 extension character processing
- Indication of Line 23 for external use
- 13.5 MHz clock output to drive external microcontroller
- Detection of Spanish transmissions to disable flicker-stopper
- Compatible with Philips' one-chip TV IC (TDA836X) for scan-locking applications.

DESCRIPTION

The IVT1.8* is a single-chip Teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on IVT1.0VPS and has reception facilities for the 5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR programming via Teletext). With suitable software both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission. Automatic processing of packet 26 transmissions is also possible. No external memory is required as an 8K × 8 DRAM is included on-chip for up to 8 page storage. An enhanced mode allows 7 Fastext pages to be stored, with one chapter used to store extension packets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5281P	DIP48	plastic shrink dual in-line package; 32 leads (400 mil)	SOT240-1
SAA5281ZP	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5281GP	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

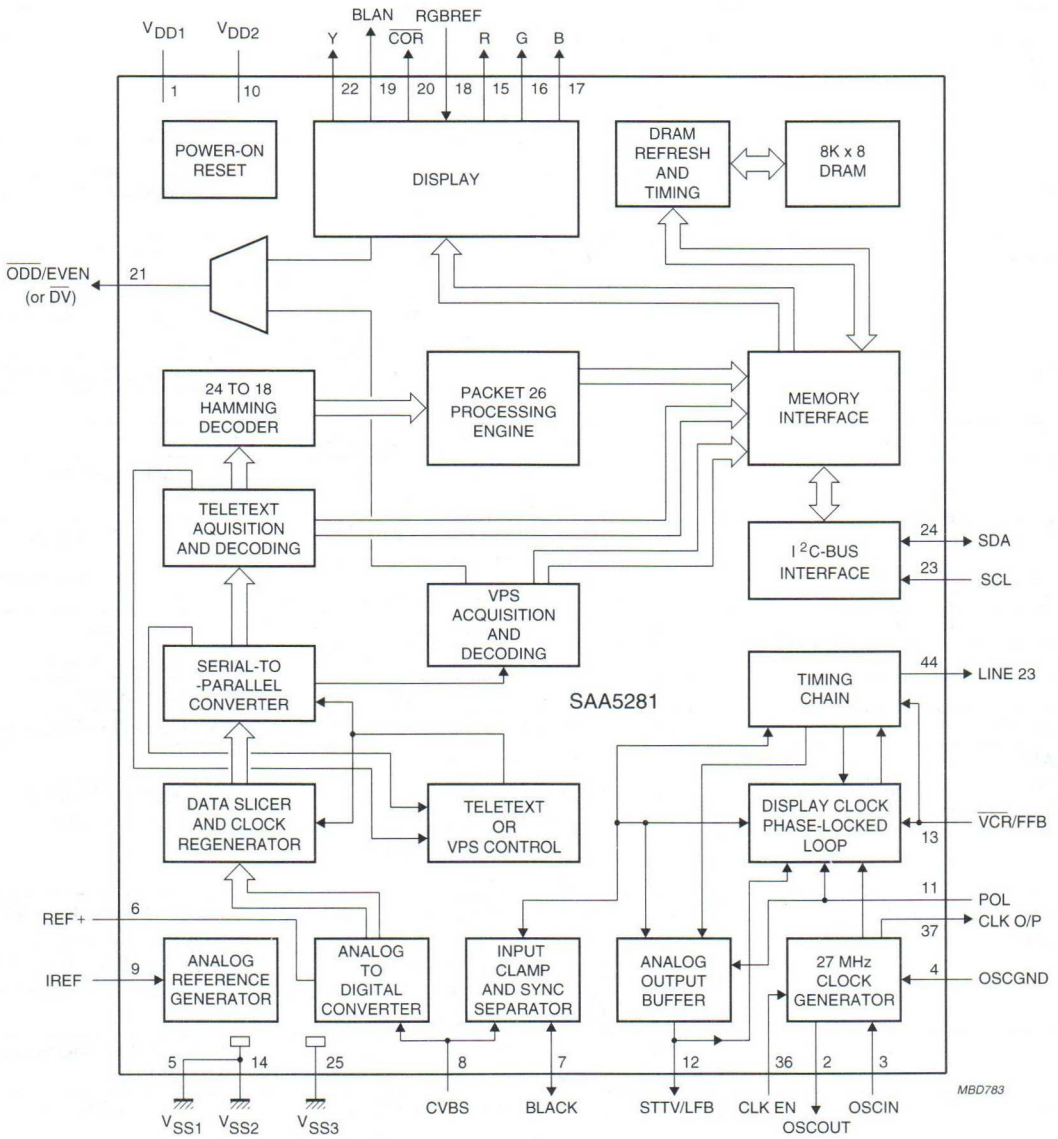


Fig.1 Block diagram; pin numbers for DIP48 (SOT240-1).

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240-1	SOT247-1	SOT319-2	
V_{DD1}	1	52	11	+5 V supply 1
OSCOUT	2	1	13	27 MHz crystal oscillator output
OSCIN	3	2	14	27 MHz crystal oscillator input
OSCGND	4	3	15	0 V crystal oscillator ground
V_{SS1}	5	4 and 5	16	0 V ground
REF+	6	6	18	positive reference voltage for ADC; this pin should be connected to ground via a 100 nF capacitor
BLACK	7	8	19	video black level storage input/output; this pin should be connected to ground via a 100 nF capacitor
CVBS	8	9	20	composite video input; a positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	21	reference current input, connected to ground via a 27 kΩ resistor
V_{DD2}	10	11	22	+5 V supply 2
POL	11	12	23	STTV/LFB/FFB polarity selection input
STTV/LFB	12	13	24	sync to TV output line flyback input; function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	27	PLL time constant switch/field input; function controlled by an internal register bit (scan sync mode)
V_{SS2}	14	15	28	0 V ground; connected to V_{SS1} for normal operation
R	15	16	30	dot rate character output of the RED colour information
G	16	17	32	dot rate character output of the GREEN colour information
B	17	18	33	dot rate character output of the BLUE colour information
RGBREF	18	19	34	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	35	dot rate fast blanking output
$\overline{COR}$	20	21	36	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open-drain output
$\overline{ODD}$/EVEN (or $\overline{DV}$)	21	22	37	in $\overline{ODD}$/EVEN mode a 25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents; in $\overline{DV}$ mode a VPT data valid signal is used to indicate reception of error-free VPS or 8/30 format 2 data
Y	22	23	38	dot rate character output of teletext foreground colour information; open-drain output
SCL	23	24	39	serial clock input for I²C-bus; it can still be driven HIGH during power-down of the device
SDA	24	25	40	serial data port for the I²C-bus, open-drain output; it can still be driven HIGH during power-down of the device
V_{SS3}	25	26	44	0 V ground

SYMBOL	PIN			DESCRIPTION
	SOT240-1	SOT247-1	SOT319-2	
i.c.	26 to 35, 38 to 43, 45 to 48	27 to 32, 35 to 38, 41 to 46, 48 to 51	1 to 3, 5 to 8, 45 to 53, 55, 61, 63 to 64	internally connected; normally open-circuit
CLK EN	36	39	56	clock enable input to enable the clock output (CLP O/P pin 37); internal pull-down normally disables clock
CLK O/P	37	40	59	13.5 MHz clock output to drive an external microcontroller
LINE 23	44	47	4	output for indication of Line 23 for use with external circuitry
n.c.	–	7, 33, 34	9, 10, 12, 17, 25, 26, 29, 31, 41 to 43, 54, 57, 58, 60, 62	not connected; normally open-circuit

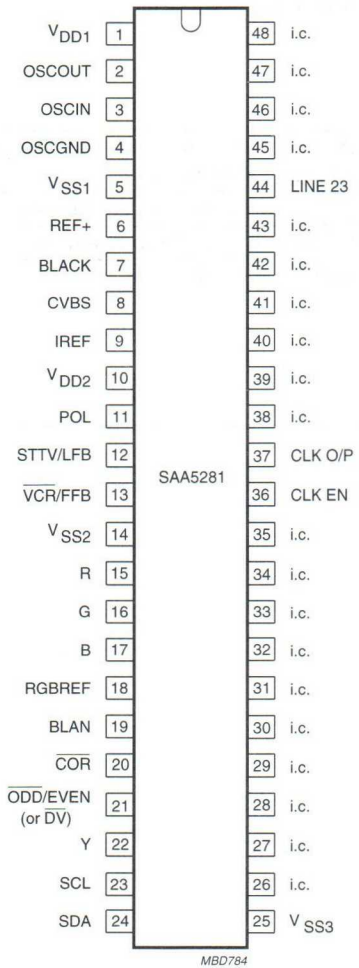


Fig.2 Pin configuration; SOT240-1 (DIP48).

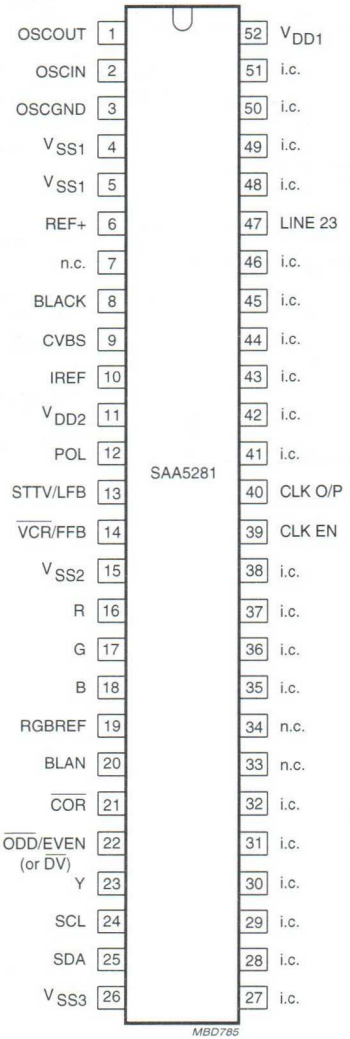


Fig.3 Pin configuration; SOT247-1 (SDIP52).

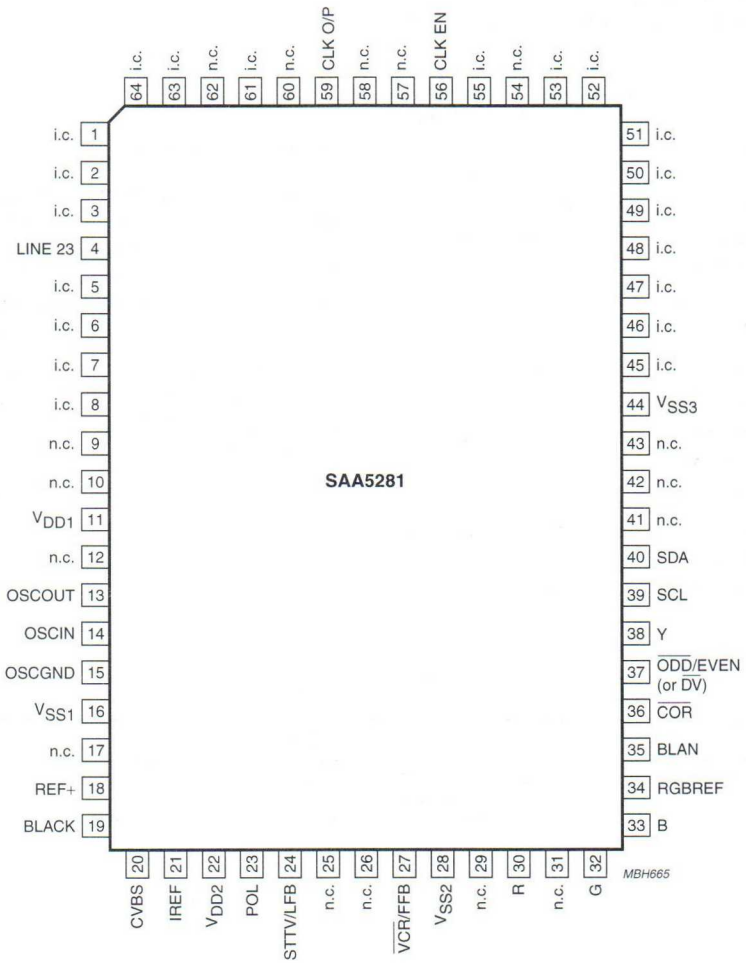


Fig.4 Pin configuration; SOT319-2 (QFP64).

Chinese Character System Teletext (CCST) decoder

SAA5700

FEATURES

- Acquisition and display of the 625-line PAL CCST Chinese standard for teletext, with Chinese and Latin character sets
- Supports multiple DRAM sizes: 256K × 4 bits, 1M × 4 bits, 4M × 4 bits and 2 × 1M × 4 bits with an additional decoder/demultiplexer IC
- Acquires and stores in background up to (typically) 400 pages with 1M × 4 bits external DRAM
- CCST Fastext, with capability of displaying Chinese characters on Fastext prompt row
- Meshing for reduced contrast video background in subtitles and boxes
- Full line and screen colour to all edges of screen
- Supports 625-line 50/100 Hz display modes
- Scan-locked and stand-alone sync modes; supports video-locked sync modes with external PLL
- Easy control via high level I²C-bus SAFARI commands
- Sync mode switching and picture centring via I²C-bus SAFARI commands
- Supports external decryption unit for encrypted data.

GENERAL DESCRIPTION

The SAA5700 is a Chinese teletext decoder suitable for TV and multimedia applications. It incorporates all the data slicing, acquisition and display circuitry on-chip, as well as the logic for memory management. An external DRAM is used to store the currently displayed page and also the precaptured teletext pages.

An external ROM is used to store the ideographic Chinese character set. There is a high level software interface with easy commands for the control of the decoder. Control is achieved via the I²C-bus.

The device is available in a QFP64 package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5700GP	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

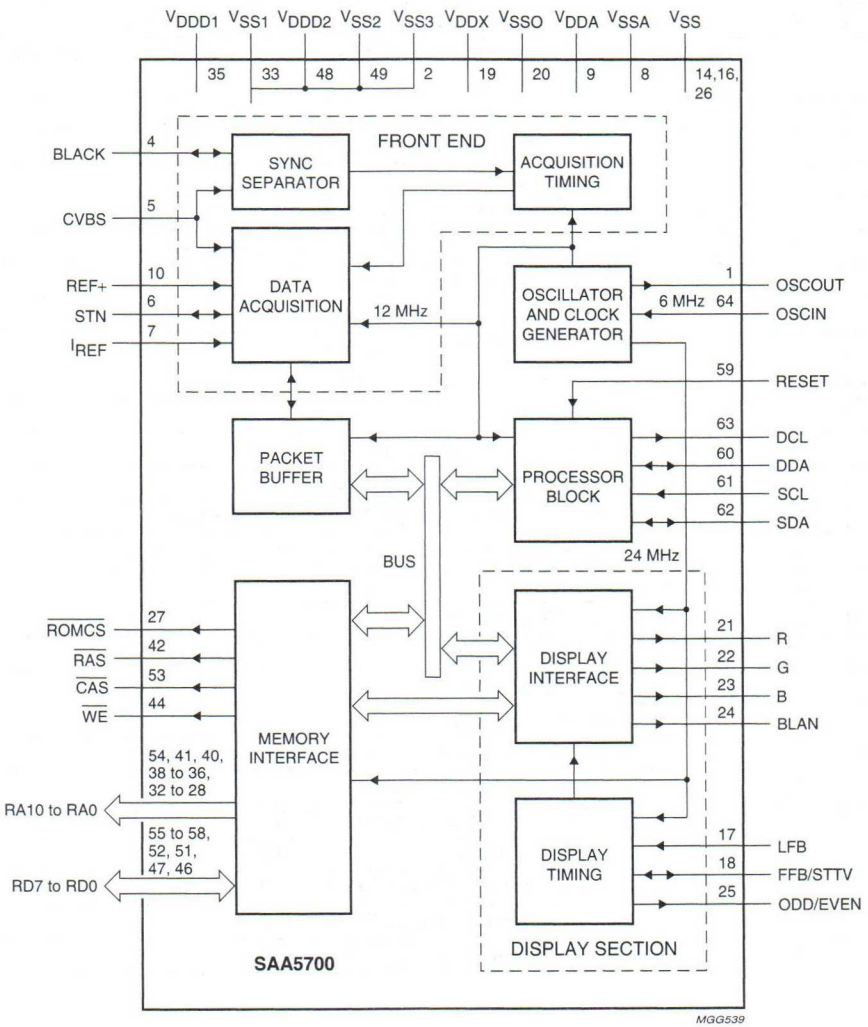


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
OSCOUT	1	O	oscillator output to crystal
V_{SS3}	2	ground	ground for I/O pad buffers connect to V_{SS}; internally connected to V_{SS1} and V_{SS2}
n.c.	3	–	not connected
BLACK	4	I/O	black level sample and hold capacitor; 100 nF to V_{SSA}
CVBS	5	I	video signal input; 100 nF series capacitor, 250 Ω source impedance maximum, reference to V_{SSA}
STN	6	I/O	ADC current reference decoupling; 100 nF to V_{SSA}
I_{REF}	7	I	current reference input; 10 kΩ to V_{SSA}
V_{SSA}	8	ground	0 V power supply; analog
V_{DDA}	9	supply	+5 V power supply; analog
REF+	10	I	ADC voltage reference decoupling; 100 nF to V_{SSA}
i.c.	11	–	internally connected; do not use
i.c.	12	–	internally connected; do not use
i.c.	13	–	internally connected; do not use
V_{SS}	14	ground	connect to V_{SS} for normal use
n.c.	15	–	not connected
V_{SS}	16	ground	connect to V_{SS} for normal use
LFB	17	I	scan line flyback input (HSYNC)
FFB/STTV	18	I/O	scan field flyback input (VSYNC)/sync to TV output
V_{DDX}	19	supply	+5 V power supply; connect to V_{DD} for normal use
V_{SSO}	20	ground	output stage current return and 0 V
R	21	O	analog Red output
G	22	O	analog Green output
B	23	O	analog Blue output
BLAN	24	O	fast blanking (VDS)
ODD/EVEN	25	O	frame rate signal for hardware de-interlace (FRAME)
V_{SS}	26	ground	connect to V_{SS} for normal use
$\overline{\text{ROMCS}}$	27	O	chip select (address decode) for ROM
RA0	28	O	bit 0 of address to DRAM, ROM and IC
RA1	29	O	bit 1 of address to DRAM, ROM and IC
RA2	30	O	bit 2 of address to DRAM, ROM and IC
RA3	31	O	bit 3 of address to DRAM, ROM and IC

SYMBOL	PIN	I/O	DESCRIPTION
RA4	32	O	bit 4 of address to DRAM, ROM and IC
V_{SS1}	33	ground	0 V power supply digital; connected internally to V_{SS2} and V_{SS3}
n.c.	34	–	not connected
V_{DDD1}	35	supply	+5 V power supply digital; connected internally to V_{DD2}
RA5	36	O	bit 5 of address to DRAM, ROM and IC
RA6	37	O	bit 6 of address to DRAM, ROM and IC
RA7	38	O	bit 7 of address to DRAM, ROM and IC
n.c.	39	–	not connected
RA8	40	O	bit 8 of address to DRAM, ROM and IC
RA9	41	O	bit 9 of address to DRAM, ROM and IC
$\overline{RAS}$	42	O	row address strobe to DRAM; active LOW
n.c.	43	–	not connected
$\overline{WE}$	44	O	write enable to DRAM and IC; active LOW
i.c.	45	–	internally connected; do not use
RD0	46	I/O	bit 0 of data bus to/from DRAM, ROM and IC
RD1	47	I/O	bit 1 of data bus to/from DRAM, ROM and IC
V_{DDD2}	48	supply	+5 V power supply digital; connected internally to V_{DD1}
V_{SS2}	49	ground	0 V power supply digital; connected internally to V_{SS1} and V_{SS3}
n.c.	50	–	not connected
RD2	51	I/O	bit 2 of data bus to/from DRAM, ROM and IC
RD3	52	I/O	bit 3 of data bus to/from DRAM, ROM and IC
$\overline{CAS}$	53	O	column address strobe to DRAM; active LOW
RA10	54	O	bit 10 of address to DRAM, ROM and IC
RD7	55	I/O	bit 7 of data bus to/from DRAM, ROM and IC
RD6	56	I/O	bit 6 of data bus to/from DRAM, ROM and IC
RD5	57	I/O	bit 5 of data bus to/from DRAM, ROM and IC
RD4	58	I/O	bit 4 of data bus to/from DRAM, ROM and IC
RESET	59	I	chip/processor reset input (active HIGH)
DDA	60	I/O	bidirectional serial data to/from optional Decryptor
SCL	61	I	primary I^2C-bus serial clock input
SDA	62	I/O	primary I^2C-bus serial data
DCL	63	O	serial clock to optional Decryptor
OSCIN	64	I	oscillator input from crystal/external clock input

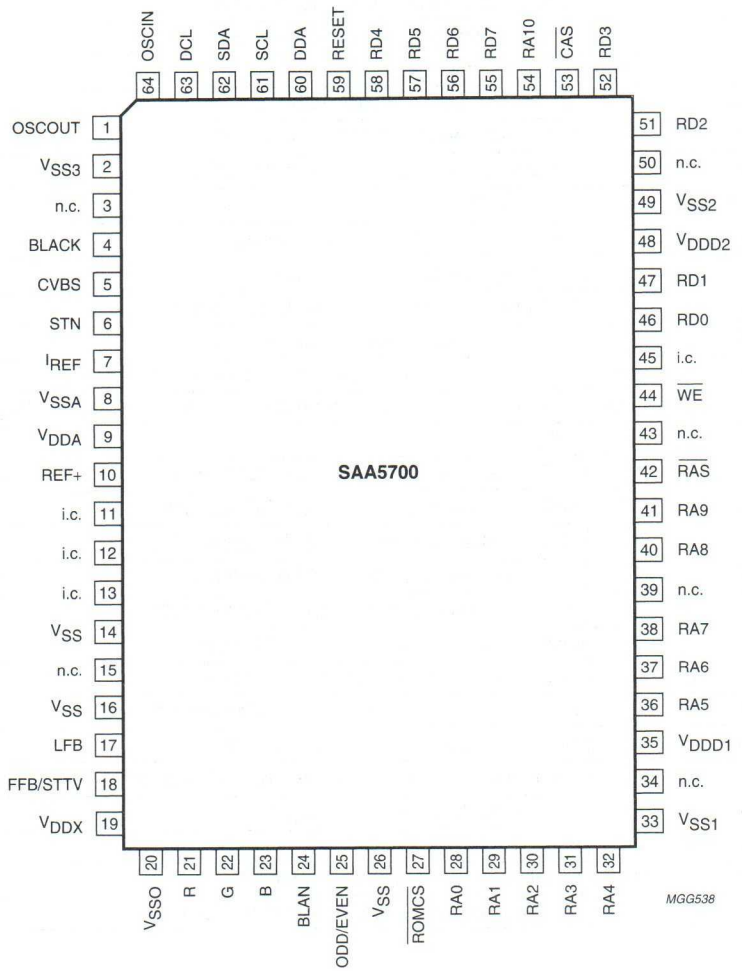


Fig.2 Pin configuration.

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1 FEATURES

1.1 General

- Single chip microcontroller with integrated teletext decoder
- Single +5 V power supply
- Single crystal oscillator for teletext decoder, display and microcontroller
- Teletext function can be powered-down independently of microcontroller function for reduced power consumption in stand-by
- Pin compatibility throughout family.

1.2 Microcontroller

- 80C51 microcontroller core
- 16/32/64 kbyte mask programmed ROM
- 256/768/1280 bytes of microcontroller RAM
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner control
- Four 8-bit Analog-to-Digital converters
- 2 high current open-drain outputs for directly driving LED's etc.
- I^2C-bus interface
- External ROM and RAM capability on QFP80 package version.

1.3 Teletext acquisition

- 1 page and 10 page Teletext version
- Acquisition of 525-line and 625-line World System Teletext, with automatic selection
- Acquisition and decoding of VPS data (PDC system A)
- Page clearing in under 64 µs (1 TV line)
- Separate storage of extension packets (SAA5296/7, SAA5296/7A and SAA5496/7)
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT) (SAA5296/7, SAA5296/7A and SAA5496/7)
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine for processing accented (and other) characters
- Comprehensive Teletext language coverage
- Video signal quality detector.

1.4 Teletext Display

- 525-line and 625-line display
- 12 × 10 character matrix
- Double height, width and size On-Screen Display (OSD)
- Definable border colour
- Enhanced display features including meshing and shadowing
- 260 characters in mask programmed ROM
- Automatic FRAME output control with manual override
- RGB push pull output to standard decoder ICs
- Stable display via slave synchronisation to Horizontal Sync and Vertical Sync.

1.5 Additional features of SAA529xA devices

- Wide Screen Signalling (WSS) bit decoding (line 23).

1.6 Additional features of SAA549x devices

- Wide Screen Signalling bit decoding (line 23)
- Quad width OSD capability
- 32 additional OSD characters in mask programmed ROM
- 8 foreground and 8 background colours definable from a palette of 64.

2 GENERAL DESCRIPTION

The SAA529x, SAA529xA and SAA549x family of microcontrollers are a derivative of the Philips' industry-standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system and include an integrated teletext function.

The teletext hardware has the capability of decoding and displaying both 525-line and 625-line World System Teletext. The same display hardware is used both for Teletext and On-Screen Display, which means that the display features give greater flexibility to differentiate the TV set.

The family offers both 1 page and 10 page Teletext capability, in a range of ROM sizes. Increasing display capability is offered from the SAA5290 to the SAA5497.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			PROGRAM MEMORY (ROM)
	NAME	DESCRIPTION	VERSION	
SAA5290PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	16 kbytes
SAA5291PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	32 kbytes
SAA5291APS/nnn				
SAA5296PS/nnn				
SAA5296APS/nnn				
SAA5491PS/nnn				
SAA5496PS/nnn				
SAA5291H/nnn	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	32 kbytes and external
SAA5291AH/nnn				
SAA5296H/nnn				
SAA5296AH/nnn				
SAA5491H/nnn				
SAA5496H/nnn				
SAA5297PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	64 kbytes
SAA5297APS/nnn				
SAA5497PS/nnn				
SAA5297H/nnn	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	64 kbytes or external
SAA5297AH/nnn				
SAA5497H/nnn				

Note

1. 'nnn' is a three-digit number uniquely referencing the microcontroller program mask and OSD mask.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	supply voltages	4.5	5.0	5.5	V
V_{DDM}					
V_{DDT}					
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C
I_{DDM}	microcontroller supply current	–	20	35	mA
SAA5290, SAA5291, SAA5291A and SAA5491					
I_{DDA}	analog supply current	–	35	50	mA
I_{DDT}	teletext supply current	–	40	65	mA
SAA5296, SAA5296A, SAA5297, SAA5297A, SAA5496 and SAA5497					
I_{DDA}	analog supply current	–	35	50	mA
I_{DDT}	teletext supply current	–	50	80	mA

5 BLOCK DIAGRAM

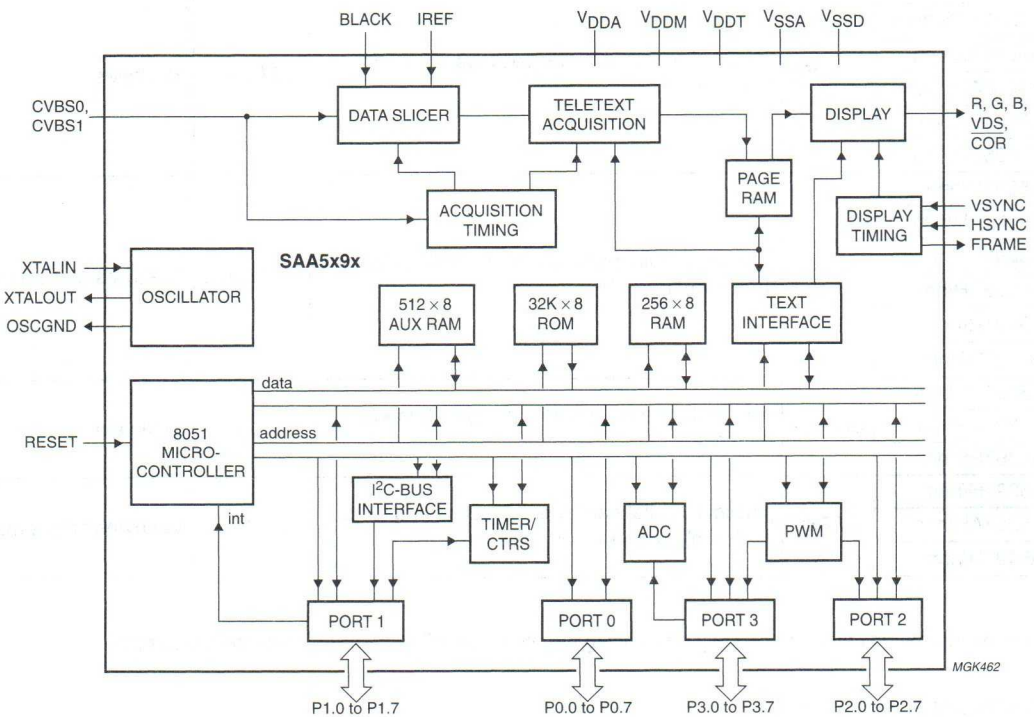


Fig.3 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

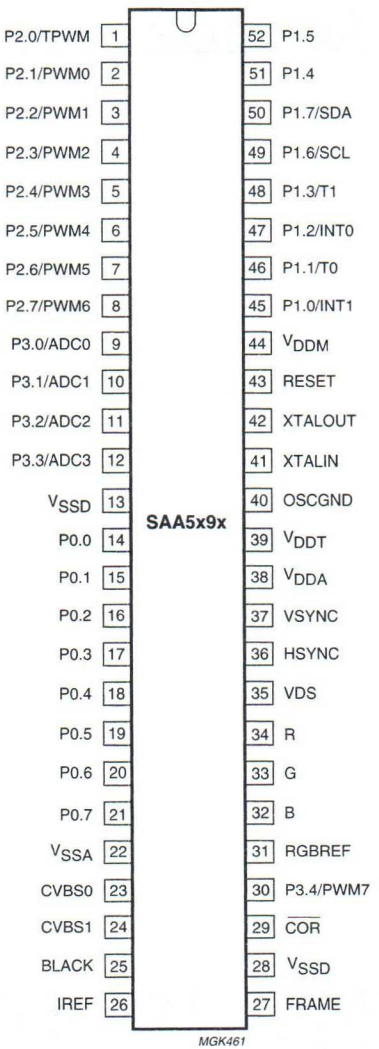


Fig.4 Pin configuration (SDIP52).

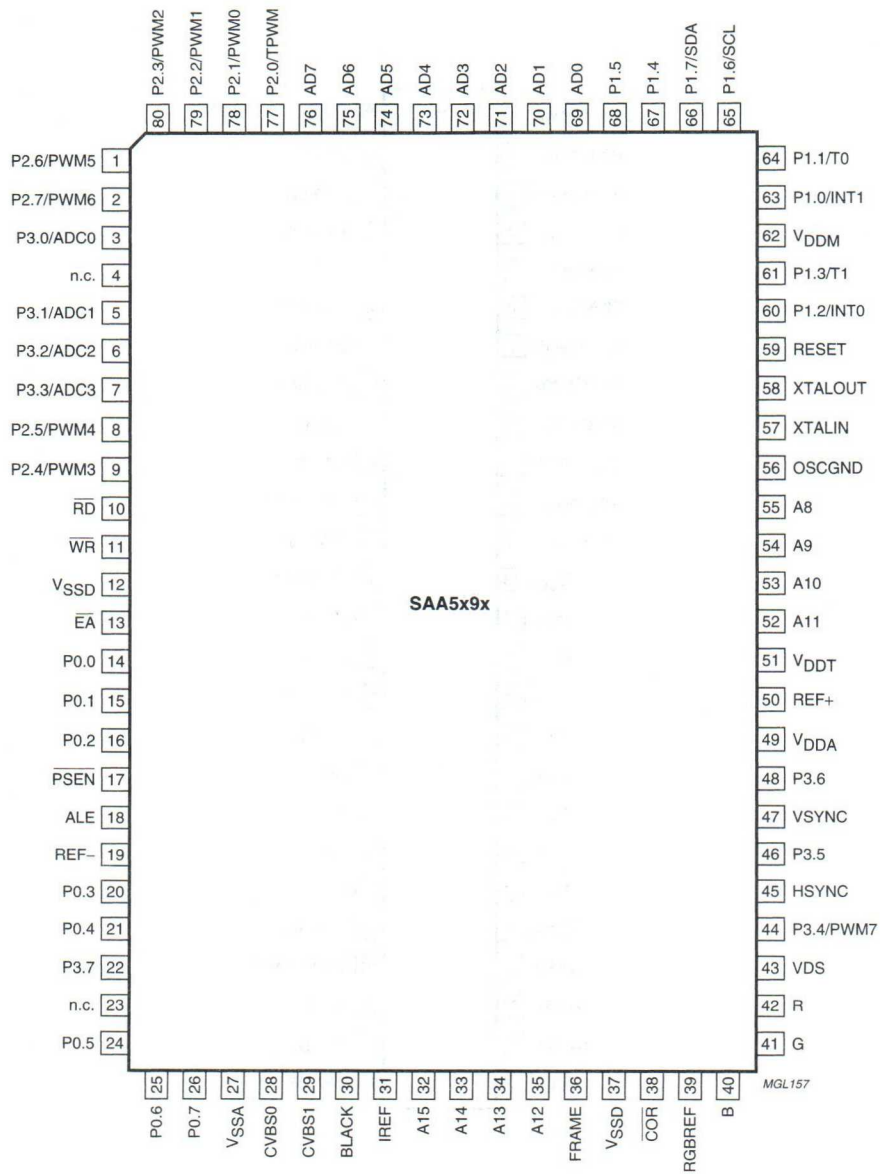


Fig.5 Pin configuration (QFP80).

6.2 Pin description

Table 1 SDIP52 and QFP80 packages

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP80	
P2.0/TPWM	1	77	**Port 2**: 8-bit open-drain bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM. P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6.
P2.1/PWM0	2	78	
P2.2/PWM1	3	79	
P2.3/PWM2	4	80	
P2.4/PWM3	5	9	
P2.5/PWM4	6	8	
P2.6/PWM5	7	1	
P2.7/PWM6	8	2	
P3.0/ADC0	9	3	**Port 3**: 8-bit open-drain bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility. P3.4/PWM7 is the output for the 6-bit PWM7.
P3.1/ADC1	10	5	
P3.2/ADC2	11	6	
P3.3/ADC3	12	7	
P3.4/PWM7	30	44	
P3.5	–	46	
P3.6	–	48	
P3.7	–	22	
V_{SSD}	13	12	Digital ground.
P0.0	14	14	**Port 0**: 8-bit open-drain bidirectional port. P0.5 and P0.6 have 10 mA current sinking capability for direct drive of LEDs.
P0.1	15	15	
P0.2	16	16	
P0.3	17	20	
P0.4	18	21	
P0.5	19	24	
P0.6	20	25	
P0.7	21	26	
V_{SSA}	22	27	Analog ground.
CVBS0	23	28	Composite video inputs; a positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
CVBS1	24	29	
BLACK	25	30	Video black level storage input: this pin should be connected to V_{SSA} via a 100 nF capacitor.
IREF	26	31	Reference current input for analog circuits, connected to V_{SSA} via a 27 kΩ resistor.
FRAME	27	36	De-interlace output synchronised with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits.
V_{SSD}	28	37	Internally connected; this pin should be connected to digital ground.
$\overline{COR}$	29	38	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP80	
LRGBREF	31	39	DC input voltage to define the output HIGH level on the RGB pins.
B	32	40	Pixel rate output of the BLUE colour information.
G	33	41	Pixel rate output of the GREEN colour information.
R	34	42	Pixel rate output of the RED colour information.
VDS	35	43	Video/data switch push-pull output for dot rate fast blanking.
HSYNC	36	45	Schmitt trigger input for a TTL level version of the horizontal sync pulse; the polarity of this pulse is programmable by register bit TXT1.H POLARITY.
VSYNC	37	47	Schmitt trigger input for a TTL level version of the vertical sync pulse; the polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V_{DDA}	38	49	+5 V analog power supply.
V_{DDT}	39	51	+5 V teletext power supply.
OSCGND	40	56	Crystal oscillator ground.
XTALIN	41	57	12 MHz crystal oscillator input.
XTALOUT	42	58	12 MHz crystal oscillator output.
RESET	43	59	If the reset input is HIGH for at least 3 machine cycles (36 oscillator periods) while the oscillator is running, the device is reset; this pin should be connected to V_{DDM} via a 2.2 µF capacitor.
V_{DDM}	44	62	+5 V microcontroller power supply.
P1.0/INT1	45	63	**Port** 1: 8-bit open-drain bidirectional port with alternate functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse. P1.1/T0 is the counter/timer 0. P1.2/INT0 is external interrupt 0. P1.3/T1 is the counter/timer 1. P1.6/SCL is the serial clock input for the I²C-bus. P1.7/SDA is the serial data port for the I²C-bus.
P1.1/T0	46	64	
P1.2/INT0	47	60	
P1.3/INT1	48	61	
P1.6/SCL	49	65	
P1.7/SDA	50	66	
P1.4	51	67	
P1.5	52	68	
REF+	–	50	Positive reference voltage for software driven ADC.
REF–	–	19	Negative reference voltage for software driven ADC.
RD	–	10	Read control signal to external Data Memory.
$\overline{WR}$	–	11	Write control signal to external Data Memory.
$\overline{PSEN}$	–	17	Enable signal for external Program Memory.
ALE	–	18	External latch enable signal; active HIGH.
$\overline{EA}$	–	13	Control signal used to select external (LOW) or internal (HIGH) Program Memory.
AD0 to AD7	–	69 to 76	Address lines A0 to A7 multiplexed with data lines D0 to D7.
A8 to A15	–	55 to 52, 35 to 32	Address lines A8 to A15.

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1 FEATURES

- Input data fully compliant with the Transport Stream (TS) definition of the MPEG-2 systems specification (International Standard; November 1994)
- Input data signals: Forward Error Correction (FEC) or descrambler interface
  - modem data input bus (8-bit wide) PKTDAT7 to PKTDAT0
  - valid input data indicator (PKTDATV)
  - erroneous packet indicator ($\overline{\text{PKTBAD}}$/PKTBAD)
  - first packet byte indicator (PKTSYNC)
  - byte strobe signal [for the asynchronous mode only (PKTBCLK)]
- The interface can be configured to either of two modes:
  - asynchronous mode; PKTBCLK < 9 MHz, for connection to a modem (e.g. FEC)
  - synchronous mode; PKTBCLK is not used for connection to an external descrambler operating at 9 MHz. The descrambler chip clock (9 MHz; 33% duty cycle) is generated and output to the demultiplexer.

  The descrambler chip clock [DCLK (9 MHz, 33% duty cycle)] is generated and output by the demultiplexer
- External memory; standard 32K × 8-bit static RAM. Required typical access time ≤ 50 ns, write pulse width (t_{WP}) ≤ 35 ns.
- Effective bit rate: $f_{bit} \leq 72$ MHz
- Control Interface; 8-bit multiplexed data/address (MDAT7 to MDAT0), memory mapped I/O (P90CE201 microcontroller parallel bus compatible), in combination with two microcontroller interrupt signals ($\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$). In addition, a number of address input pins (MA9 to MA2) allow direct access to a selected set of demultiplexer registers.
- Output ports:

  Video; two alternative applications;
  - third party video decoder compatible (master or slave horizontal or vertical sync generation)
  - Philips SAA7201 compatible (via general purpose output)

  Audio; third party audio decoder, or Philips SAA2500 compatible

  Audio/video; third party combined A/V decoder compatible, (programmable)

  Teletext; a Teletext Clock/Teletext Data (TTC/TTD) based serial interface to selected teletext decoders (e.g. SAA9042). Alternatively, this interface can be programmed to provide data for Vertical Blanking Interval (VBI) insertion of teletext data. The interface therefore includes a teletext data request input (TTR). In this mode, the interface is compatible with the SAA7183 (EURO-DENC) TXT interface.

  HS Data; high-speed data output, outputting entire transport packets, packet payloads, PES packet payloads, or sections (programmable) at byte clock frequency (9 MHz). In the test mode it is capable of outputting copies of either video, audio or other data streams (programmable).

  HS pins are combined with the general purpose interface. The general purpose interface is bidirectional, and can therefore, be used as an alternative transport stream input.
- Descrambler; 8-bit wide data input interface, combined with the modem input bus. A descrambler device may output a descrambled transport stream at 9 MByte/s. A 9 MHz descrambler clock is generated and output by the demultiplexer.
- Microcontroller support; only for control, no specific demultiplexing tasks are performed by the microcontroller. However, parsing and processing of Program Specific Information (PSI), and Service Information (SI) is left to the microcontroller.
- Error handling; stream dependent error handling algorithms, invoked either if the $\overline{\text{PKTBAD}}$/PKTBAD input signal is set, or if the transport_error_indicator bit (MPEG-2 syntax) is set or if the parser detects an MPEG-2 syntax error. Different handling algorithms are applied for the various output ports.

2 GENERAL DESCRIPTION

This document specifies the MPEG-2 systems demultiplexer IC, SAA7205H, for use in MPEG-2 based digital TV receivers, possibly incorporating conditional access. Such receivers are to be implemented in, for instance, a Digital Video Broadcasting (DVB) set-top box, or Integrated Receiver Decoder (IRD). An example of a demultiplexer/descrambler system configuration, containing a channel decoder module, source decoders, a system microcontroller and a conditional access system is shown in Fig.1. The main function of the demultiplexer is to separate relevant data from an incoming MPEG-2 systems compliant data stream and pass it to both the individual source decoders and to the system microcontroller. To support descrambling, the demultiplexer interfaces with the descrambler part of a conditional access system (optional). The demultiplexer therefore generates a 9 MHz descrambler chip clock.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for core		3.0	3.3	3.6	V
P_{tot}	total power consumption		–	–	380	mW
f_{CLK}	clock frequency	$f_{byte} \leq 9$ MHz	–	–	27	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7205H	QFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT320-2

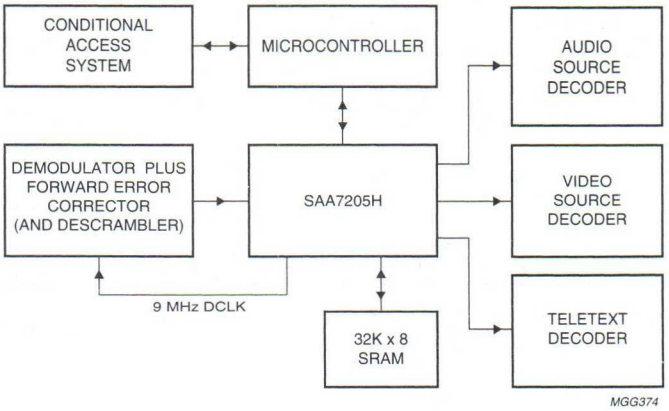


Fig.1 Demultiplexer system configuration.

5 BLOCK DIAGRAM

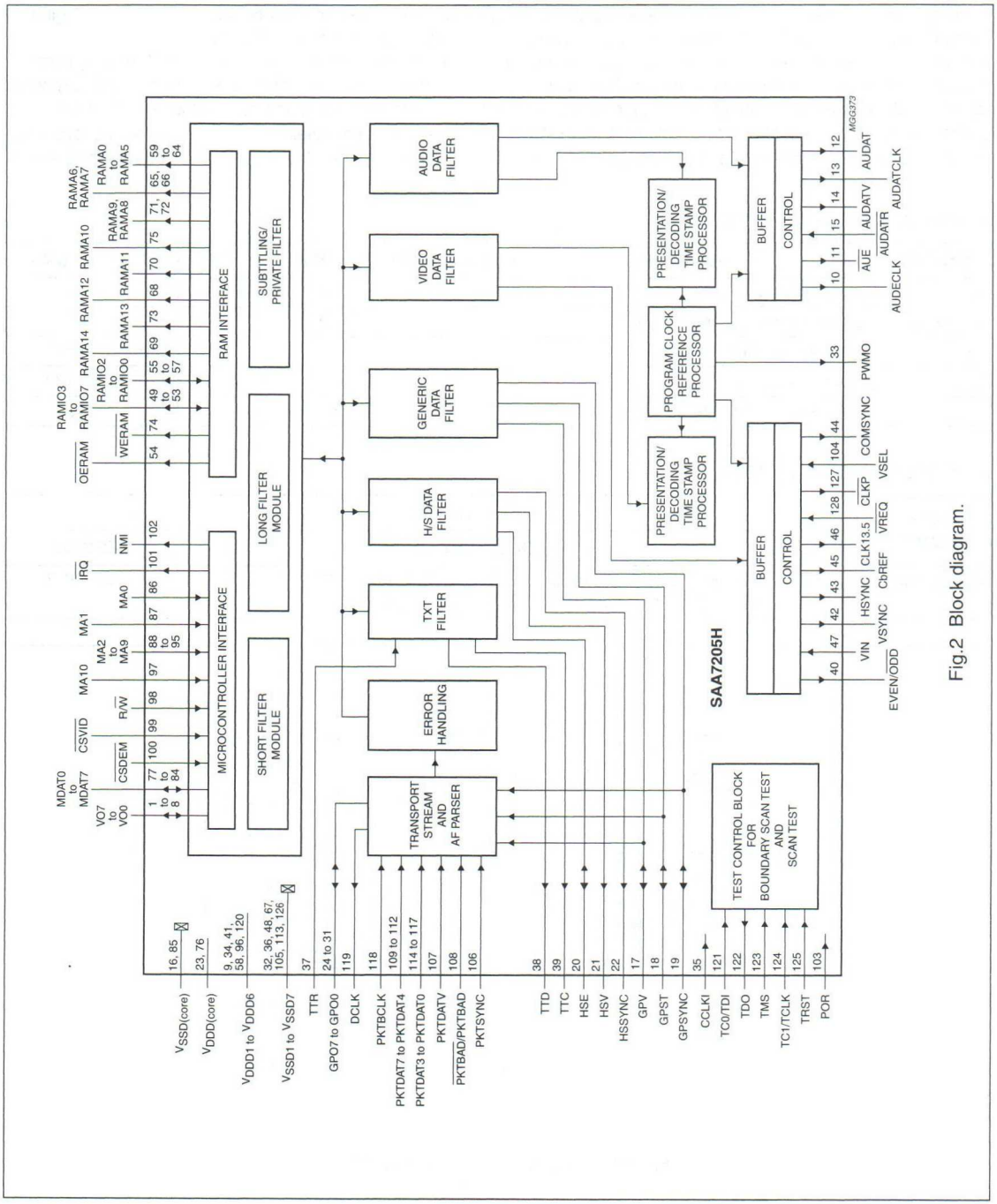


Fig.2 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
VO7	1	I/O	data output bit 7 to video decoder (shared with microcontroller data)
VO6	2	I/O	data output bit 6 to video decoder (shared with microcontroller data)
VO5	3	I/O	data output bit 5 to video decoder (shared with microcontroller data)
VO4	4	I/O	data output bit 4 to video decoder (shared with microcontroller data)
VO3	5	I/O	data output bit 3 to video decoder (shared with microcontroller data)
VO2	6	I/O	data output bit 2 to video decoder (shared with microcontroller data)
VO1	7	I/O	data output bit 1 to video decoder (shared with microcontroller data)
VO0	8	I/O	data output bit 0 to video decoder (shared with microcontroller data)
V_{DDD1}	9	supply	digital supply voltage 1 (+5 V)
AUDECLK	10	O	audio decoder clock output [equals CCLKI/M (programmable)]
$\overline{AUE}$	11	O	audio data error indicator output (active LOW)
AUDAT	12	O	data output to audio decoder (elementary stream)
AUDATCLK	13	O	audio data clock output (frequency range 32 to 448 kHz; 9 Mbit/s)
AUDATV	14	O	audio data valid indicator output
$\overline{AUDATR}$	15	I	audio data request input (active LOW)
$V_{SSD1(core)}$	16	GND	digital ground 1 for core
GPV	17	I/O	valid data byte indicator input/output
GPST	18	I/O	byte strobe signal input/output (equals 9 MHz gated byte clock)
GPSYNC	19	I/O	packet sync byte indicator input/output
HSE	20	I/O	indicates erroneous HS data input/output
HSV	21	O	valid high speed data indicator
HSSYNC	22	O	indicates the first output byte of either a packet or payload
$V_{DDD1(core)}$	23	supply	digital supply voltage 1 for core (+3.3 V)
GPO7	24	I/O	high speed byte output bit 7 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO6	25	I/O	high speed byte output bit 6 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO5	26	I/O	high speed byte output bit 5 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO4	27	I/O	high speed byte output bit 4 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO3	28	I/O	high speed byte output bit 3 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO2	29	I/O	high speed byte output bit 2 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO1	30	I/O	high speed byte output bit 1 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
GPO0	31	I/O	high speed byte output bit 0 for transport packets/general purpose byte output (e.g. for SAA7201)/alternative transport stream input
V_{SSD1}	32	GND	digital ground 1
PWMO	33	O	pulse width modulated VCO control signal output (local STC)

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD2}	34	supply	digital supply voltage 2 (+5 V)
CCLKI	35	I	27 MHz demultiplexer chip clock Input
V_{SSD2}	36	GND	digital ground 2
TTR	37	I	teletext data request input (for VBI insertion of TXT)
TTD	38	O	serial teletext data output (6.75 or 6.9375 Mbit/s)
TTC	39	O	TXT clock (6.75 MHz = CCLKI/4)
EVEN/$\overline{ODD}$	40	O	field parity output, internally generated, locked to COMSYNC
V_{DDD3}	41	supply	digital supply voltage 3 (+5 V)
VSYNC	42	O	vertical sync output, locked to CCLKI and optionally VIN
HSYNC	43	O	horizontal sync output, internally generated
COMSYNC	44	O	(CCIR601) composite sync (50 and 60 Hz)
CbREF	45	O	indicating U samples in UY and VY video decoder output
CLK13.5	46	O	equals CCLKI/2
VIN	47	I	receiver local vertical sync input, locked to CCLKI (optional)
V_{SSD3}	48	GND	digital ground 3
RAMIO3	49	I/O	external SRAM input/output bus bit 3
RAMIO4	50	I/O	external SRAM input/output bus bit 4
RAMIO5	51	I/O	external SRAM input/output bus bit 5
RAMIO6	52	I/O	external SRAM input/output bus bit 6
RAMIO7	53	I/O	external SRAM input/output bus bit 7
$\overline{OERAM}$	54	O	output enable for external 32K × 8 SRAM (active LOW)
RAMIO2	55	I/O	external SRAM input/output bus bit 2
RAMIO1	56	I/O	external SRAM input/output bus bit 1
RAMIO0	57	I/O	external SRAM input/output bus bit 0
V_{DDD4}	58	supply	digital supply voltage 4 (+5 V)
RAMA0	59	O	external SRAM address bus output bit 0
RAMA1	60	O	external SRAM address bus output bit 1
RAMA2	61	O	external SRAM address bus output bit 2
RAMA3	62	O	external SRAM address bus output bit 3
RAMA4	63	O	external SRAM address bus output bit 4
RAMA5	64	O	external SRAM address bus output bit 5
RAMA6	65	O	external SRAM address bus output bit 6
RAMA7	66	O	external SRAM address bus output bit 7
V_{SSD4}	67	GND	digital ground 4
RAMA12	68	O	external SRAM address bus output bit 12
RAMA14	69	O	external SRAM address bus output bit 14
RAMA11	70	O	external SRAM address bus output bit 11
RAMA9	71	O	external SRAM address bus output bit 9
RAMA8	72	O	external SRAM address bus output bit 8
RAMA13	73	O	external SRAM address bus output bit 13
$\overline{WERAM}$	74	O	write enable output for external SRAM (active LOW)

SYMBOL	PIN	I/O	DESCRIPTION
RAMA10	75	O	external SRAM address bus output bit 10
$V_{DDD2(core)}$	76	supply	digital supply voltage 2 for core (+3.3 V)
MDAT0	77	I/O	microcontroller bidirectional data bus bit 0
MDAT1	78	I/O	microcontroller bidirectional data bus bit 1
MDAT2	79	I/O	microcontroller bidirectional data bus bit 2
MDAT3	80	I/O	microcontroller bidirectional data bus bit 3
MDAT4	81	I/O	microcontroller bidirectional data bus bit 4
MDAT5	82	I/O	microcontroller bidirectional data bus bit 5
MDAT6	83	I/O	microcontroller bidirectional data bus bit 6
MDAT7	84	I/O	microcontroller bidirectional data bus bit 7
$V_{SSD2(core)}$	85	GND	digital ground 2 for core
MA0	86	I	microcontroller MSByte/$\overline{\text{LSByte}}$ indicator input bit 0
MA1	87	I	microcontroller address/$\overline{\text{data}}$ indicator input bit 1
MA2	88	I	microcontroller address input bit 2 for direct access to selected registers
MA3	89	I	microcontroller address input bit 3 for direct access to selected registers
MA4	90	I	microcontroller address input bit 4 for direct access to selected registers
MA5	91	I	microcontroller address input bit 5 for direct access to selected registers
MA6	92	I	microcontroller address input bit 6 for direct access to selected registers
MA7	93	I	microcontroller address input bit 7 for direct access to selected registers
MA8	94	I	microcontroller address input bit 8 for direct access to selected registers
MA9	95	I	microcontroller address input bit 9 for direct access to selected registers
V_{DDD5}	96	supply	digital supply voltage 5 (+5 V)
MA10	97	I	microcontroller direct addressing/indirect addressing indicator input bit 10
R/$\overline{\text{W}}$	98	I	read/$\overline{\text{write}}$ input selection
$\overline{\text{CSVID}}$	99	I	(audio)/video decoder chip select input (active LOW)
$\overline{\text{CSDEM}}$	100	I	demultiplexer chip select input (active LOW)
$\overline{\text{IRQ}}$	101	O	interrupt request output for microcontroller (active LOW, open-drain)
$\overline{\text{NMI}}$	102	O	non-maskable interrupt output for VOUT bus access handling (open-drain)
POR	103	I	power-on reset input
VSEL	104	I	video input select signal (bus control by microcontroller)
V_{SSD5}	105	GND	digital ground 5
PKTSYNC	106	I	indicates the first input byte (sync) of a transport packet
PKTDATV	107	I	valid input data indicator
$\overline{\text{PKTBAD}}$/ PKTBAD	108	I	packet error indicator input (programmable polarity)
PKTDAT7	109	I	8-bit wide modem data input bit 7
PKTDAT6	110	I	8-bit wide modem data input bit 6
PKTDAT5	111	I	8-bit wide modem data input bit 5
PKTDAT4	112	I	8-bit wide modem data input bit 4
V_{SSD6}	113	GND	digital ground 6
PKTDAT3	114	I	8-bit wide modem data input bit 3

SYMBOL	PIN	I/O	DESCRIPTION
PKTDAT2	115	I	8-bit wide modem data input bit 2
PKTDAT1	116	I	8-bit wide modem data input bit 1
PKTDAT0	117	I	8-bit wide modem data input bit 0
PKTBCLK	118	I	byte strobe input signal (< 9 MHz)
DCLK	119	O	9 MHz descrambler chip clock output (33% duty cycle)
V_{DDD6}	120	supply	digital supply voltage 6 (+5 V)
TC0/TDI	121	I	scan test data input/boundary scan test data input
TDO	122	O	boundary scan test data output
TMS	123	I	boundary scan test input mode select
TC1/TCLK	124	I	scan test clock input/ boundary scan test clock input
TRST	125	I	boundary scan test reset input (LOW in normal operation)
V_{SSD7}	126	GND	digital ground 7
$\overline{CLKP}$	127	O	gated clock output signal indicating valid data (9 MHz = CCLKI/3; active LOW)
$\overline{VREQ}$	128	I	video data request input (active LOW)

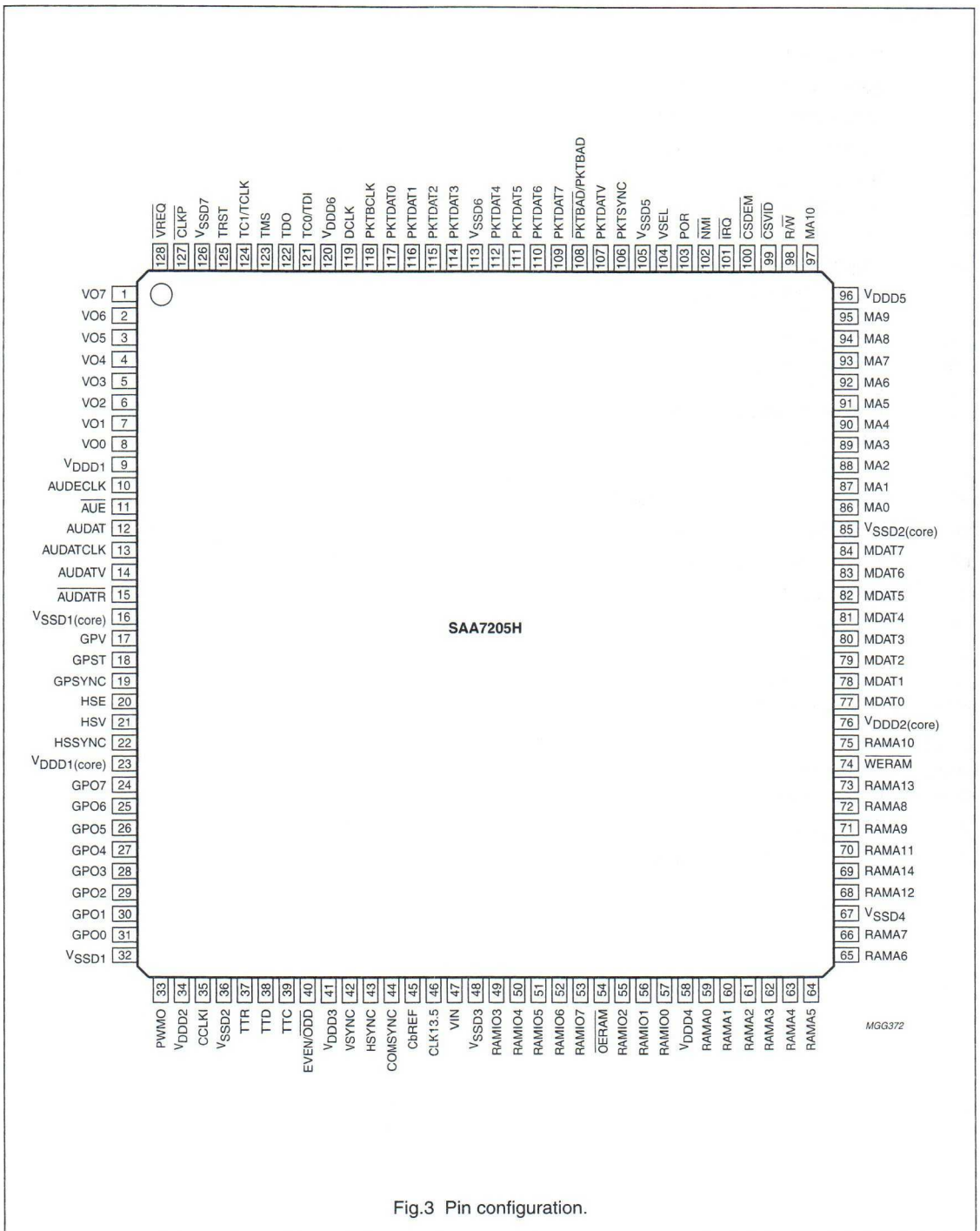


Fig.3 Pin configuration.

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DVB compliant descrambler SAA7206H

1 FEATURES

- Input data fully compliant with the Transport Stream (TS) definition of the MPEG-2 systems specification
- Input data signals; [Forward Error Correction (FEC) Interface]
  - modem data input bus (8-bit wide)
  - valid input data indicator
  - erroneous packet indicator
  - first packet byte indicator
  - byte strobe signal (for asynchronous mode only).

  The interface can be programmed to one of two modes:
  - Asynchronous mode; byte strobe input signal (MBCLK) < 9 MHz, for connection to a modem (FEC)
  - Synchronous mode; MBCLK is not used. Data is delivered to the descrambler synchronized with the chip clock (DCLK) [9 MHz (typ.) with a 33% duty cycle].
- No external memory
- Effective bit rate; $f_{bit} \leq 72$ MHz
- Control interface; 8-bit multiplexed data/address, memory mapped I/O (90CE201 microcontroller parallel bus compatible), in combination with a microcontroller interrupt signal ($\overline{IRQ}$)
- Output ports are identical to the input data interface (demultiplexer interface)
  - except for the packet error indicator ($\overline{MB}$/MB), as the descrambler translates an active MB signal to the 'transport_error_indicator' bit in the transport stream
  - except for the byte strobe input signal (MBCLK), as data is delivered to the demultiplexer, synchronized with the descrambler chip clock which is generated by the demultiplexer
- Descrambler, based on the super descrambler mechanism algorithm with stream decipher and block decipher. The descrambler is initialized with a 64-bit Control Word (CW) at the beginning of a transport stream packet payload of a selected Packet Identification (PID). The descrambler operates on transport stream packet or Packetized Elementary Stream (PES) packet payloads
- Microcontroller support; only for control, no specific descrambling tasks are performed by the microcontroller. However, parsing and processing of conditional access information (such as EMM and ECM data) is left to the system microcontroller
- Boundary scan test port for boundary scan.

2 GENERAL DESCRIPTION

The SAA7206H (DVB compliant) is designed for use in MPEG-2 based digital TV receivers, incorporating conditional access filters. Such receivers are to be implemented in, for instance, a digital video broadcasting top set box, or an integrated digital TV receiver.
An example of a demultiplexer/descrambler system configuration, containing a channel decoder module, a demultiplexer, a system controller and a conditional access system is shown in Fig.3.. The main function of the descrambler is to descramble the payloads of MPEG-2 TS packets or PES packets. In addition, the descrambler retrieves Conditional Access (CA) data [such as Entitlement Management Messages (EMM) and Entitlement Control Messages (ECM) etc.] from the stream and passes it to the system microcontroller for processing.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7206H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	–	5.5	V
$V_{DDD(core)}$	digital supply voltage for core		–	–	3.6	V
P_{tot}	total power dissipation	$V_{DDD(core)}$ = 3.3 V, V_{DDD} = 5 V, C_L = 15 pF	–	–	250	mW
f_{clk}	clock frequency	duty cycle = 30 to 55%	–	–	9	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

5 BLOCK DIAGRAM

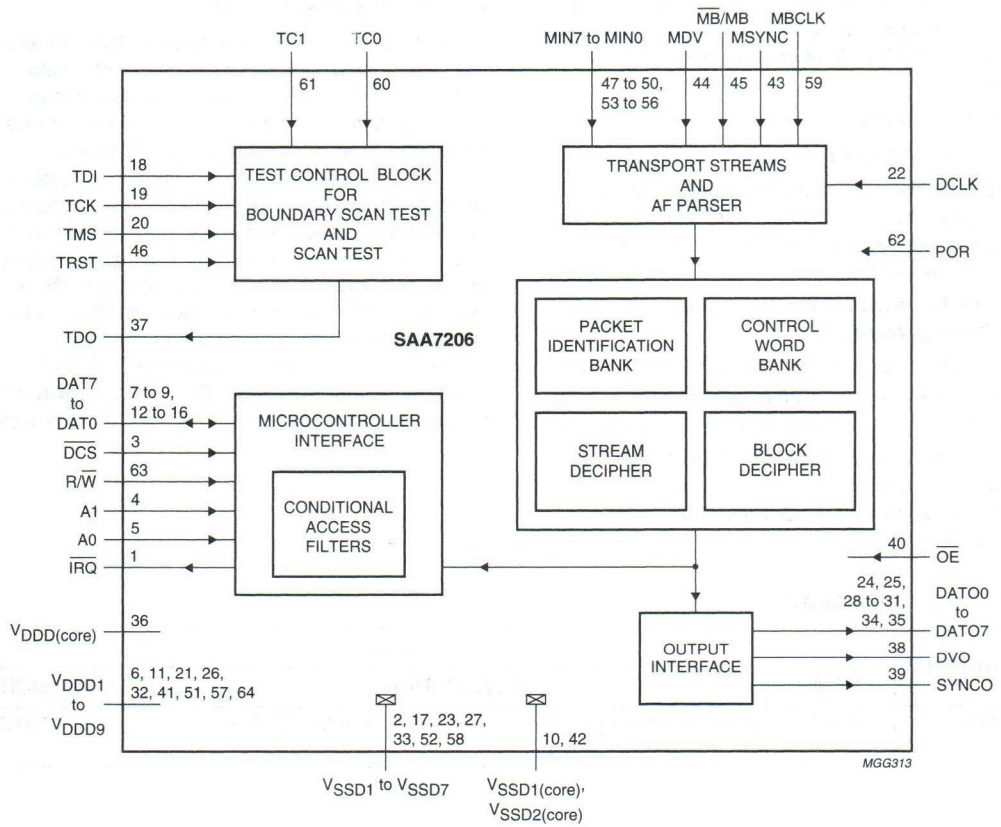


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
$\overline{IRQ}$	1	O	interrupt request output for microcontroller (active LOW, open-drain output)
V_{SSD1}	2	GND	digital ground 1
$\overline{DCS}$	3	I	descrambler chip select input (active LOW)
A1	4	I	A1 = address/data indicator input
A0	5	I	A0 = MSByte indicator input
V_{DDD1}	6	supply	digital supply voltage 1 (+5 V)
DAT7	7	I/O	microcontroller bidirectional data bus bit 7
DAT6	8	I/O	microcontroller bidirectional data bus bit 6
DAT5	9	I/O	microcontroller bidirectional data bus bit 5
$V_{SSD1(core)}$	10	GND	digital ground 1 for core
V_{DDD2}	11	supply	digital supply voltage 2 (+5 V)
DAT4	12	I/O	microcontroller bidirectional data bus bit 4
DAT3	13	I/O	microcontroller bidirectional data bus bit 3
DAT2	14	I/O	microcontroller bidirectional data bus bit 2
DAT1	15	I/O	microcontroller bidirectional data bus bit 1
DAT0	16	I/O	microcontroller bidirectional data bus bit 0
V_{SSD2}	17	GND	digital ground 2
TDI	18	I	boundary scan test data input
TCK	19	I	boundary scan test clock input
TMS	20	I	boundary scan test mode select input
V_{DDD3}	21	supply	digital supply voltage 3 (+5 V)
DCLK	22	I	9 MHz descrambler chip clock input (duty cycle range: 30 to 55%)
V_{SSD3}	23	GND	digital ground 3
DATO0	24	O	data output to demultiplexer bit 0
DATO1	25	O	data output to demultiplexer bit 1
V_{DDD4}	26	supply	digital supply voltage 4 (+5 V)
V_{SSD4}	27	GND	digital ground 4
DATO2	28	O	data output to demultiplexer bit 2
DATO3	29	O	data output to demultiplexer bit 3
DATO4	30	O	data output to demultiplexer bit 4
DATO5	31	O	data output to demultiplexer bit 5
V_{DDD5}	32	supply	digital supply voltage 5 (+5 V)
V_{SSD5}	33	GND	digital ground 5
DATO6	34	O	data output to demultiplexer bit 6
DATO7	35	O	data output to demultiplexer bit 7
$V_{DDD(core)}$	36	supply	digital supply voltage for core (+3.3 V)
TDO	37	O	boundary scan test data output
DVO	38	O	valid output data indicator
SYNCO	39	O	indicates the first output byte (sync) of a transport packet

SYMBOL	PIN	I/O	DESCRIPTION
$\overline{OE}$	40	I	output enable (active LOW), if HIGH, device outputs are high impedance, (connected to logic 0 in normal operation)
V_{DDD6}	41	supply	digital supply voltage 6 (+5 V)
$V_{SSD2(core)}$	42	GND	digital ground 2 for core
MSYNC	43	I	indicates the first input byte (sync) of a transport packet
MDV	44	I	valid input data indicator
$\overline{MB}$/MB	45	I	packet error indicator input (programmable polarity)
TRST	46	I	boundary scan reset input (LOW in normal operation)
MIN7	47	I	8-bit wide modem data input bit 7
MIN6	48	I	8-bit wide modem data input bit 6
MIN5	49	I	8-bit wide modem data input bit 5
MIN4	50	I	8-bit wide modem data input bit 4
V_{DDD7}	51	supply	digital supply voltage 7 (+5 V)
V_{SSD6}	52	GND	digital ground 6
MIN3	53	I	8-bit wide modem data input bit 3
MIN2	54	I	8-bit wide modem data input bit 2
MIN1	55	I	8-bit wide modem data input bit 1
MIN0	56	I	8-bit wide modem data input bit 0
V_{DDD8}	57	supply	digital supply voltage 8 (+5 V)
V_{SSD7}	58	GND	digital ground 7
MBCLK	59	I	byte strobe input signal < 9 MHz
TC0	60	I	test control input 0 (not connected in normal operation)
TC1	61	I	test control input 1 (not connected in normal operation)
POR	62	I	power-on reset, must be active HIGH during at least 5 DCLK pulses
R/$\overline{W}$	63	I	read/$\overline{write}$ input selection
V_{DDD9}	64	supply	digital supply voltage 9 (+5 V)

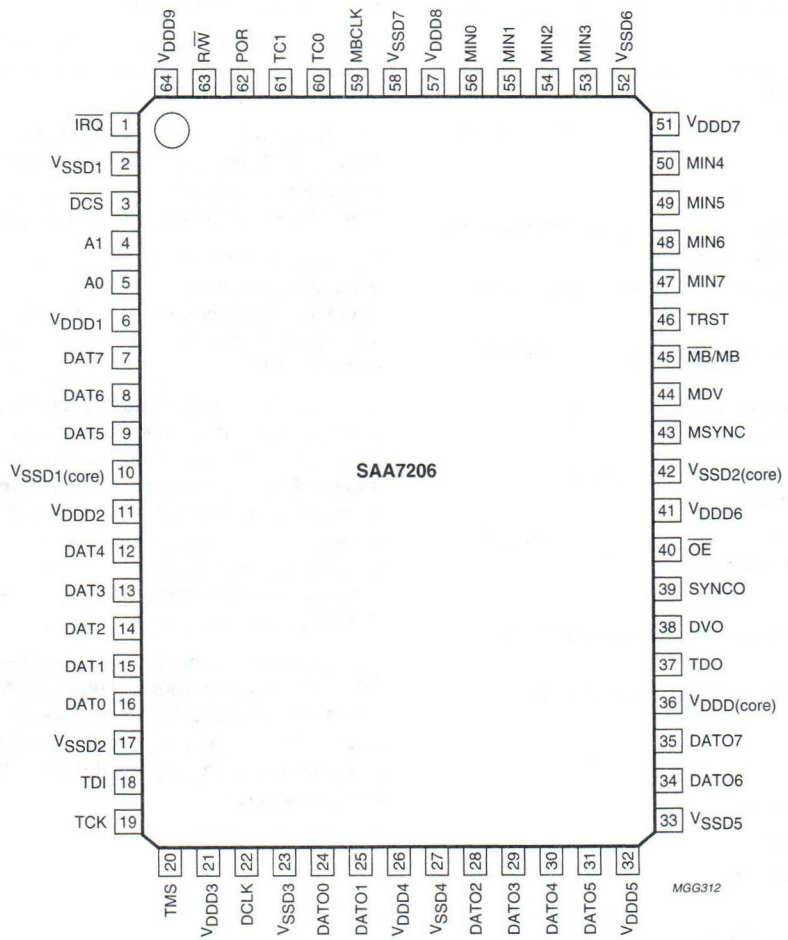


Fig.2 Pin configuration.

Digital Signal Processor (DSP) for cameras

SAA8110G

FEATURES

- High precision digital processing with 9 or 10 bit input
- Different types of CCDs (PAL, NTSC and CIF) (progressive, interlaced and non-interlaced)
- Black offset preprocessing (including optical black offset control)
- RGB-separation (with contour and white clip signals generation)
- RGB-processing (colour space matrix, black control, knee and gamma)
- RGB-to-YUV conversion (including down-sampling filters)
- White balance control
- Y-processing (contour processing, false colour detector, filters and noise reduction)
- UV-processing (false colour correction and noise reduction)
- Digital output formatter (including CIF-formatter, DTV2, D1)
- Analog output preprocessing (including PAL/NTSC-encoder and DACs)
- Measurement engine (prepared for auto-exposure and auto-white balance features)
- Miscellaneous functions (e.g. switched mode power supply pulse generator, control DAC)
- VH-reference and window timing
- Serial interface (selectable I²C-bus or 80C51 UART interface)
- Mode control (including power management).

APPLICATIONS

- Desktop video applications
- Surveillance systems
- Video-phone systems.

GENERAL DESCRIPTION

The SAA8110G is designed for desktop video applications (teleconferencing, video grabbing), surveillance and video-phone systems.

The SAA8110G may be applied together with an analog front-end (TDA8786 including CDS/AGC/ADC), a timing generator and a microcontroller as shown in Figs 18 and 19. Other configurations are also possible.

The CCD-sensor can be of PAL, NTSC or CIF type (with complementary mosaic colour filter). The maximum number of active pixels is limited to 800 samples/line. The 10-bits digital input may have a pixel frequency of up to 14.318 MHz.

The SAA8110G output data is available in a digital and an analog output format. Two digital output formats are selectable: DTV2 (CCIR-601 at the input pixel frequency) and D1 (CCIR-656 at twice the input pixel frequency). It is also possible to generate the CIF and QCIF formats as subsets from the processed CCD-image. The analog output is available in one of four formats: RGB, YUV, YC or CVBS. The SAA8110G includes a digital PAL/NTSC-encoder and 3 DACs for this purpose.

Two types of serial interface are selectable: a fast 400 kHz I²C-bus interface or a 80C51 UART interface (with bit rates from 1 Mbit/s up to 3.75 Mbit/s depending on the system clock used). The power dissipation of the SAA8110G can be optimized for each application using the built-in power management function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8110G	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3	5	5.25	V
V_{DDA}	analog supply voltage		3	5	5.25	V
V_{IL}	LOW level digital input voltage		0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level digital input voltage		$0.6V_{DDD}$	–	V_{DDD}	V
V_{OL}	LOW level digital output voltage	$I_{OL} = -20\ \mu A$	–	–	0.5	V
V_{OH}	HIGH level digital output voltage	$I_{OH} = 20\ \mu A$	$V_{DDD} - 0.1$	–	–	V
$I_{DDD(tot)}$	total digital supply current	$f_{clk} = 14.3$ MHz; $V_{DDD} = 5$ V	–	180	200	mA
		$f_{clk} = 14.3$ MHz; $V_{DDD} = 3.3$ V	–	80	100	mA
$I_{DDA(tot)}$	total analog supply current	$f_{clk} = 14.3$ MHz; $V_{DDA} = 5$ V	–	30	40	mA
		$f_{clk} = 14.3$ MHz; $V_{DDA} = 3.3$ V	–	22	35	mA
T_{amb}	operating ambient temperature		0	–	75	°C
I_{DMD}	supply current in digital output mode	$f_{clk} = 14.3$ MHz; $V_{DDD} = 5$ V; note 1	–	185	–	mA
		$f_{clk} = 14.3$ MHz; $V_{DDD} = 3.3$ V	–	85	–	mA

Note

1. When digital mode is selected, V_{DDA} supply pins can be connected to ground.

BLOCK DIAGRAM

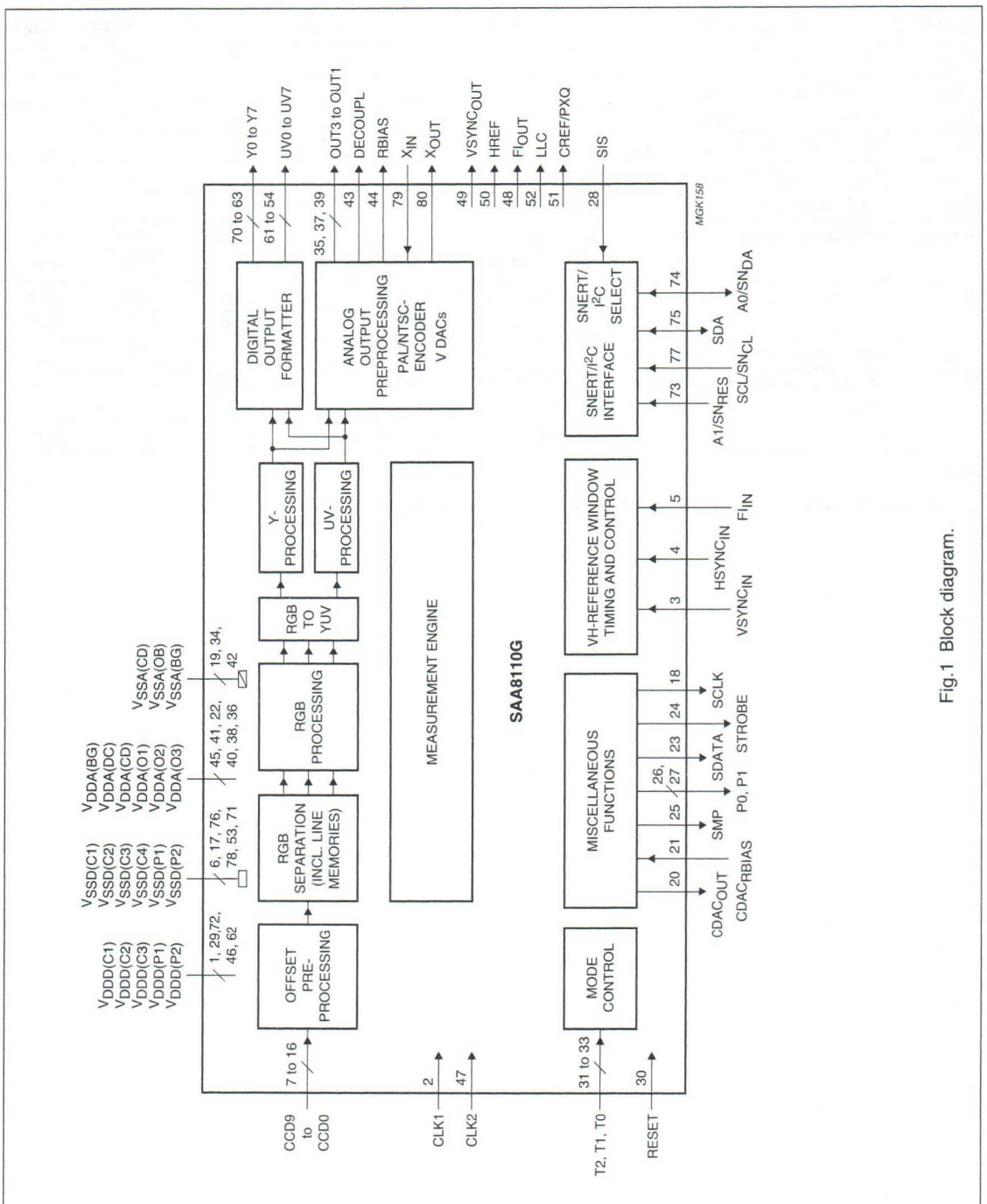


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
$V_{DDD(C1)}$	1	I	digital supply 1 for digital core and CLK1 related peripherals
CLK1	2	I	system- or pixel clock
$VSYNC_{IN}$	3	I	vertical synchronization input
$HSYNC_{IN}$	4	I	horizontal synchronization input
FI_{IN}	5	I	field identification signal input
$V_{SSD(C1)}$	6	I	digital ground 1 for digital core and CLK1 related peripherals
CCD9	7	I	(preprocessed) AD-converted CDD-signal bit 9 (MSB)
CCD8	8	I	(preprocessed) AD-converted CDD-signal bit 8
CCD7	9	I	(preprocessed) AD-converted CDD-signal bit 7
CCD6	10	I	(preprocessed) AD-converted CDD-signal bit 6
CCD5	11	I	(preprocessed) AD-converted CDD-signal bit 5
CCD4	12	I	(preprocessed) AD-converted CDD-signal bit 4
CCD3	13	I	(preprocessed) AD-converted CDD-signal bit 3
CCD2	14	I	(preprocessed) AD-converted CDD-signal bit 2
CCD1	15	I	(preprocessed) AD-converted CDD-signal bit 1
CCD0	16	I	(preprocessed) AD-converted CDD-signal bit 0 (LSB)
$V_{SSD(C2)}$	17	I	digital ground 2 for digital core and CLK1 related peripherals
SCLK	18	O	serial clock to TDA8786
$V_{SSA(CD)}$	19	I	analog ground for control DAC
$CDAC_{OUT}$	20	O	output control DAC
$CDAC_{RBIAS}$	21	I	pin to connect external bias resistor for control DAC
$V_{DDA(CD)}$	22	I	analog supply for control DAC
SDATA	23	O	serial data to TDA8786
STROBE	24	O	strobe to TDA8786
SMP	25	O	switch mode pulse for DC-DC
P0	26	O	quasi-static control output pin 0
P1	27	O	quasi-static control output pin 1
SIS	28	I	SNERT/I^2C-bus select input signal
$V_{DDD(C2)}$	29	I	digital supply 2 for digital core and CLK1 related peripherals
RESET	30	I	reset input
T2	31	I	test mode control signal bit 2
T1	32	I	test mode control signal bit 1
T0	33	I	test mode control signal bit 0
$V_{SSA(OB)}$	34	I	analog ground for the three output buffers
OUT3	35	O	output buffer 3 (R, V or CVBS)
$V_{DDA(O3)}$	36	I	analog supply for output buffer OUT3
OUT2	37	O	output buffer 2 (B, U or C)
$V_{DDA(O2)}$	38	I	analog supply for output buffer OUT2
OUT1	39	O	output buffer 1 (G or Y)
$V_{DDA(O1)}$	40	I	analog supply for output buffer OUT1

SYMBOL	PIN	I/O	DESCRIPTION
$V_{DDA(DC)}$	41	I	analog supply for analog core of triple DAC
$V_{SSA(BG)}$	42	I	analog ground for to band gap
DECOUPL	43	O	pin to be used for external decoupling of band gap
RBIAS	44	O	external bias resistor connection for band gap
$V_{DDA(BG)}$	45	I	analog supply for band gap
$V_{DDD(P1)}$	46	I	digital supply 1 for CLK2 related peripherals
CLK2	47	I	output clock (CLK2 frequency is 2 × CLK1 frequency)
FI_{OUT}	48	O	field identification output pulse
$VSYNC_{OUT}$	49	O	vertical synchronization output
HREF	50	O	horizontal reference output for YUV-port
CREF/PXQ	51	O	clock/pixel qualifier output for YUV-port
LLC	52	O	line-locked system clock output
$V_{SSD(P1)}$	53	I	digital ground 1 for CLK2 related peripherals
UV7	54	O	multiplex chrominance UV bit 7 (MSB)
UV6	55	O	multiplex chrominance UV bit 6
UV5	56	O	multiplex chrominance UV bit 5
UV4	57	O	multiplex chrominance UV bit 4
UV3	58	O	multiplex chrominance UV bit 3
UV2	59	O	multiplex chrominance UV bit 2
UV1	60	O	multiplex chrominance UV bit 1
UV0	61	O	multiplex chrominance UV bit 0 (LSB)
$V_{DDD(P2)}$	62	I	digital supply for CLK2 related peripherals
Y7	63	O	luminance Y or multiplexed YUV bit 7 (MSB)
Y6	64	O	luminance Y or multiplexed YUV bit 6
Y5	65	O	luminance Y or multiplexed YUV bit 5
Y4	66	O	luminance Y or multiplexed YUV bit 4
Y3	67	O	luminance Y or multiplexed YUV bit 3
Y2	68	O	luminance Y or multiplexed YUV bit 2
Y1	69	O	luminance Y or multiplexed YUV bit 1
Y0	70	O	luminance Y or multiplexed YUV bit 0 (LSB)
$V_{SSD(P2)}$	71	I	digital ground 2 for to CLK2 related peripherals
$V_{DDD(C3)}$	72	I	digital supply 3 for digital core and CLK1 related peripherals
$A1/SN_{RES}$	73	I	I^2C-bus address select pin A1 or SNERT reset input
$A0/SN_{DA}$	74	I	I^2C-bus address select pin A0 or SNERT data input/output
SDA	75	I	I^2C-bus data input/output
$V_{SSD(C3)}$	76	I	digital ground 3 for digital core and CLK1 related peripherals
SCL/SN_{CL}	77	I	I^2C-bus clock/SNERT clock input
$V_{SSD(C4)}$	78	I	digital ground 4 for digital core and CLK1 related peripherals
X_{IN}	79	I	input crystal oscillator for subcarrier lock applications
X_{OUT}	80	O	output crystal oscillator for subcarrier lock applications

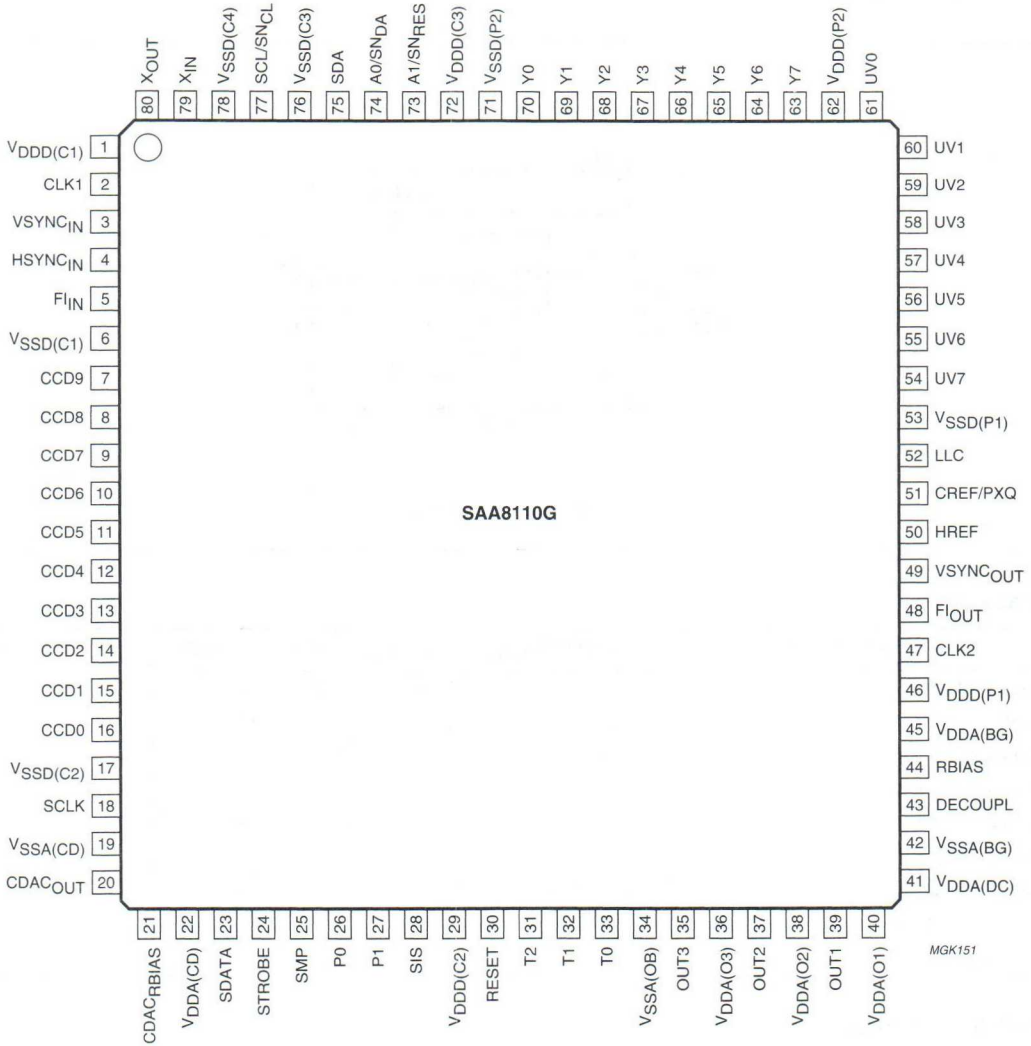


Fig.2 Pin configuration.

Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler

SAB6456 SAB6456T

GENERAL DESCRIPTION

The SAB6456/SAB6456T is a prescaler for UHF/VHF tuners. It can be switched to divide-by-64 or divide-by-256 by the mode-control (MC) pin. The circuit has an input frequency range of 70 MHz to 1 GHz, has high input sensitivity and good harmonic suppression.

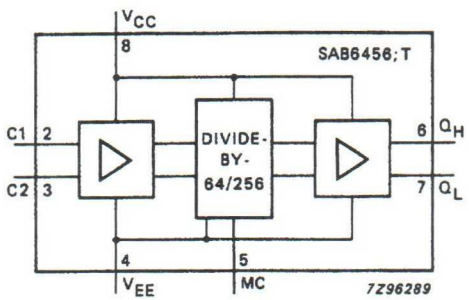


Fig.1 Block diagram.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	pin 8 to pin 4	V_{CC}	4,5	5,0	5,5	V
Supply current	pin 8	I_{CC}	–	21	–	mA
Input frequency range	pins 2 and 3	f_i	70	–	1000	MHz
Sensitivity to input voltage (r.m.s. value)		$V_{i(rms)}$	–	–	10	mV
Output voltage (peak-to-peak value)	pins 6 and 7	$V_{o(p-p)}$	–	1	–	V
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINES

SAB6456 : 8-lead DIL; plastic (SOT97); SOT97-1; 1996 November 18.
SAB6456T: 8-lead mini-pack (SO8; SOT96A); SOT96-1; 1996 November 18.

Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler

SAB6456
SAB6456T

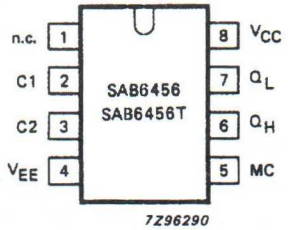


Fig.2 Pinning diagram.

PINNING

1.	n.c.	not connected
2.	C1	differential inputs
3.	C2	
4.	V_{EE}	ground (0 V)
5.	MC	mode control
6.	Q_H	complementary outputs
7.	Q_L	
8.	V_{CC}	positive supply voltage

Picture-In-Picture (PIP) controller SAB9076H

FEATURES

Display

- Twin PIP in interlaced mode at 8-bit resolution
- Sub-title mode features built in
- Large display fine positioning area, both channels independent
- Only 2 Mbit required as external VDRAM (2×1 Mbit or 1×2 Mbit)
- Four 8-bit Analogue Digital Converters (ADCs; > 7-bit performance) with clamp circuit
- Most PIP modes handle interlaced pictures without joint line error
- Two PLLs which generate the line-locked clocks for the acquisition channels
- Display PLL to generate line-locked clock for the display
- Three 8-bit Digital Analogue Converters (DACs)
- 4 : 1 : 1 data format
- Data reduction factors 1 to 1, 1 to 2, 1 to 3 and 1 to 4, horizontal and vertical independent.

I²C-bus programmable

- Single and double PIP modes can be set
- Full field still mode available
- Several aspect ratios can be handled
- Reduction factors can be set freely
- Selection of vertical filtering type
- Freeze of live pictures
- Fine tuned display position, H (8-bit), V (8-bit), both channels independent
- Fine tuned acquisition area, H (4-bit), V (8-bit), both channels independent
- Eight main borders, sub-borders and background colours selectable
- Border and background brightness adjustable, 30%, 50%, 70% and 100% IRE
- Several type of decoder input signals can be set.

GENERAL DESCRIPTION

The SAB9076H is a picture-in-picture controller for NTSC TV-sets. The circuit contains ADCs, reduction circuitry, memory control, display control and DACs.

The device inserts one or two live video signals with original or reduced sizes into a live video signal. All video signals are expected to be analog baseband signals. The conversion into the digital environment and back to the analog environment is carried out on chip. Internal clocks are generated by two acquisition PLLs and a display PLL.

Due to the two PIP channels and a large external memory a wide range of PIP modes are offered. The emphasis is put on single-PIP, double-PIP, split-screen mode and a many multi-PIP modes.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	200	–	mA
f_{sys}	system frequency	note 1	–	27	–	MHz
f_{loop}	PLL loop bandwidth frequency		4	–	–	kHz
t_{jitter}	PLL short term stability time	jitter during 1 line (64 µs)	–	–	4	ns
ς	PLL damping factor		–	0.7	–	–

Note

1. The internal system frequency is 1728 times the H_{Sync} input frequency for both the Acquisition and Display PLLs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9076H	QFP100[1]	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

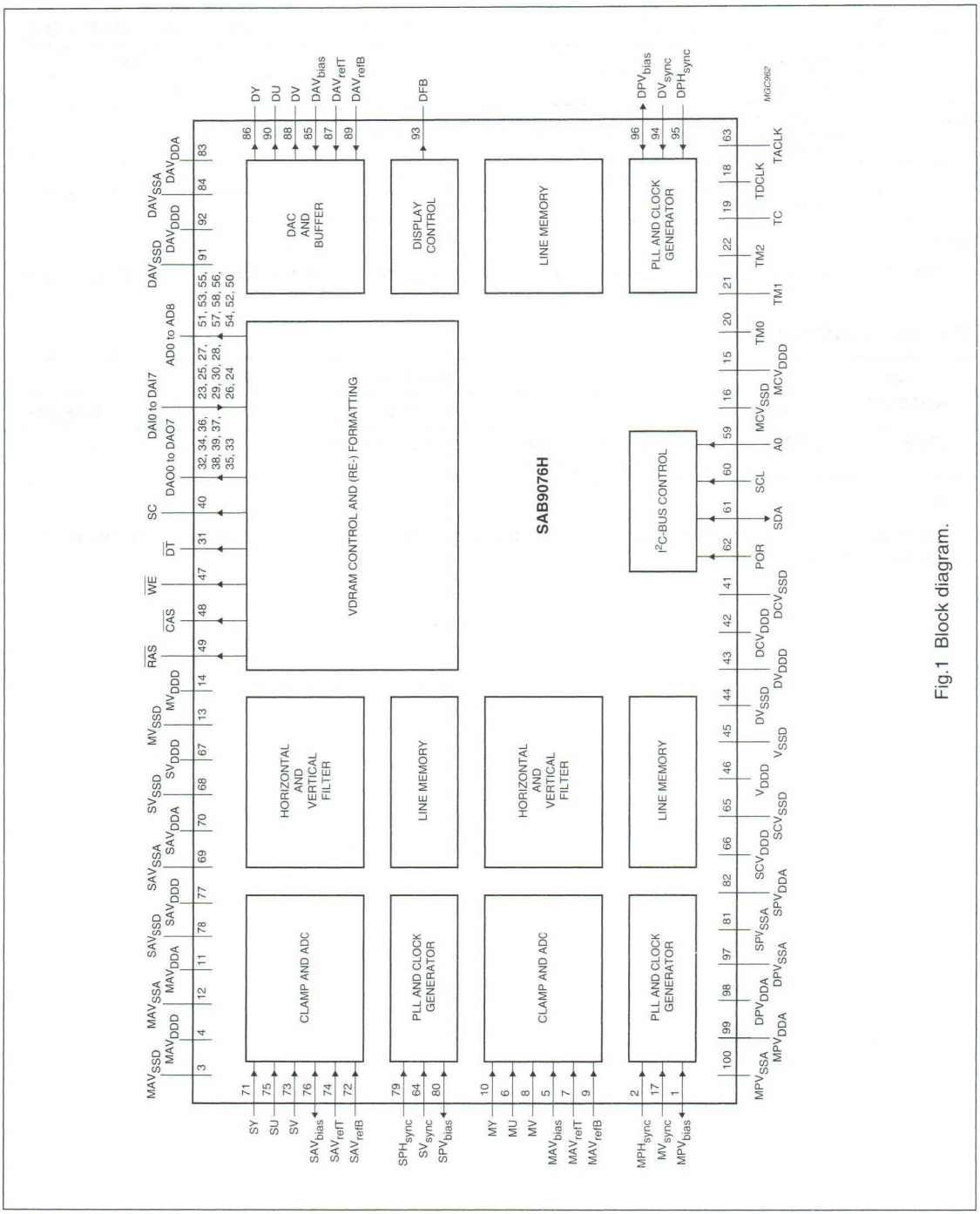


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
MPV_{bias}	1	I/O	E027	analog bias reference for main channel
MPH_{sync}	2	I	HPP01	horizontal synchronization input for main channel
MAV_{SSD}	3	I/O	E009	digital ground for main channel ADCs and PLLs
MAV_{DDD}	4	I/O	E030	digital positive power supply for main channel ADCs and PLLs
MAV_{bias}	5	I	E027	analog bias reference input for main channel ADCs
MU	6	I	E027	analog U input for main channel
MAV_{refT}	7	I	E027	analog top reference voltage input for main channel ADCs
MV	8	I	E027	analog V input for main channel
MAV_{refB}	9	I	E027	analog bottom reference voltage input for main channel ADCs
MY	10	I	E027	analog Y input for main channel
MAV_{DDA}	11	I/O	E030	analog positive power supply for main channel ADCs
MAV_{SSA}	12	I/O	E009	analog ground for main channel ADCs
MV_{SSD}	13	I/O	E009	digital ground for main-channel core
MV_{DDD}	14	I/O	E030	digital positive power supply for main-channel core
MCV_{DDD}	15	I/O	E030	digital positive power supply for main-clock buffer
MCV_{SSD}	16	I/O	E009	digital ground for main-clock buffer
MV_{sync}	17	I	HPP01	vertical synchronization input for main channel
TDCLK	18	I	HPP01	test clock input for display
TC	19	I	HPP01	test control input
TM0	20	I	HPP01	test mode 0 input
TM1	21	I	HPP01	test mode 1 input
n.c.	22	–	–	not connected
DAI0	23	I	HPP01	data bus input from memory; bit 0
DAI7	24	I	HPP01	data bus input from memory; bit 7
DAI1	25	I	HPP01	data bus input from memory; bit 1
DAI6	26	I	HPP01	data bus input from memory; bit 6
DAI2	27	I	HPP01	data bus input from memory; bit 2
DAI5	28	I	HPP01	data bus input from memory; bit 5
DAI3	29	I	HPP01	data bus input from memory; bit 3
DAI4	30	I	HPP01	data bus input from memory; bit 4
$\overline{DT}$	31	O	OPF20	memory data transfer output; active LOW
DAO0	32	O	OPF20	data bus output to memory; bit 0
DAO7	33	O	OPF20	data bus output to memory; bit 7
DAO1	34	O	OPF20	data bus output to memory; bit 1
DAO6	35	O	OPF20	data bus output to memory; bit 6
DAO2	36	O	OPF20	data bus output to memory; bit 2
DAO5	37	O	OPF20	data bus output to memory; bit 5
DAO3	38	O	OPF20	data bus output to memory; bit 3
DAO4	39	O	OPF20	data bus output to memory; bit 4
SC	40	O	OPF20	memory shift clock output

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DCV_{SSD}	41	I/O	E009	digital ground for display-clock buffer
DCV_{DDD}	42	I/O	E030	digital positive power supply for display-clock buffer
DV_{DDD}	43	I/O	E030	digital positive power supply for display core
DV_{SSD}	44	I/O	E009	digital ground for display core
V_{SSD}	45	I/O	E009	digital ground for peripherals
V_{DDD}	46	I/O	E030	digital positive power supply for peripherals
$\overline{WE}$	47	O	OPF20	memory write enable output; active LOW
$\overline{CAS}$	48	O	OPF20	memory column address strobe output; active LOW
$\overline{RAS}$	49	O	OPF20	memory row address strobe output; active LOW
AD8	50	O	OPF20	memory address bus output; bit 8
AD0	51	O	OPF20	memory address bus output; bit 0
AD7	52	O	OPF20	memory address bus output; bit 7
AD1	53	O	OPF20	memory address bus output; bit 1
AD6	54	O	OPF20	memory address bus output; bit 6
AD2	55	O	OPF20	memory address bus output; bit 2
AD5	56	O	OPF20	memory address bus output; bit 5
AD3	57	O	OPF20	memory address bus output; bit 3
AD4	58	O	OPF20	memory address bus output; bit 4
A0	59	I	HPF01	I^2C-bus address 0 selection input
SCL	60	I	HPF01	shift clock input for I^2C-bus
SDA	61	I/O	IOI41	shift I^2C-bus input data; acknowledge I^2C-bus output data
POR	62	I	HUP07	power-on reset input
TACLK	63	I	HPP01	test clock input for acquisition
SV_{sync}	64	I	HPP01	vertical synchronization input for sub-channel
SCV_{SSD}	65	I/O	E009	digital ground for sub-clock buffer
SCV_{DDD}	66	I/O	E030	digital positive power supply for sub-clock buffer
SV_{DDD}	67	I/O	E030	digital positive power supply for sub-channel core
SV_{SSD}	68	I/O	E009	digital ground for sub-channel core
SAV_{SSA}	69	I/O	E009	analog ground for sub-channel ADCs
SAV_{DDA}	70	I/O	E030	analog positive power supply for sub-channel ADCs
SY	71	I	E027	analog Y input for sub-channel
SAV_{refB}	72	I	E027	analog bottom reference input voltage for sub-channel ADCs
SV	73	I	E027	analog V input for sub-channel
SAV_{refT}	74	I	E027	analog top reference input voltage for sub-channel ADCs
SU	75	I	E027	analog U input for sub-channel
SAV_{bias}	76	I/O	E027	analog bias reference input/output for sub-channel ADCs
SAV_{DDD}	77	I/O	E030	digital positive power supply for sub-channel ADCs and PLLs
SAV_{SSD}	78	I/O	E009	digital ground for sub-channel ADCs and PLLs
SPH_{sync}	79	I	HPP01	horizontal synchronization input for sub-channel
SPV_{bias}	80	I/O	E027	analog bias reference input/output for sub-channel
SPV_{SSA}	81	I/O	E009	analog ground for sub-channel PLL

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SPV_{DDA}	82	I/O	E030	analog positive power supply for sub-channel PLL
DAV_{DDA}	83	I/O	E030	analog positive power supply for DACs
DAV_{SSA}	84	I/O	E009	analog ground for DACs
DAV_{bias}	85	I	E027	analog bias voltage reference input for DACs
DY	86	O	E027	analog Y output of DAC
DAV_{refT}	87	I	E027	analog top reference input voltage for DACs
DV	88	O	E027	analog V output of DAC
DAV_{refB}	89	I	E027	analog bottom reference input voltage for DACs
DU	90	O	E027	analog U output of DAC
DAV_{SSD}	91	I/O	E009	digital ground for DACs
DAV_{DDD}	92	I/O	E030	digital positive power supply for DACs
DFB	93	O	OPF20	fast blanking control output signal
DV_{sync}	94	I	HPP01	vertical synchronization input for display channel
DPH_{sync}	95	I	HPP01	horizontal synchronization input for display PLL
DPV_{bias}	96	I/O	E027	analog bias voltage reference input/output for display PLL
DPV_{SSA}	97	I/O	E009	analog ground for display PLL
DPV_{DDA}	98	I/O	E030	analog positive power supply for display PLL
MPV_{DDA}	99	I/O	E030	analog positive power supply for main channel PLL
MPV_{SSA}	100	I/O	E009	analog ground for main channel PLL

Table 1 Pin type explanation

PIN TYPE	DESCRIPTION
E030	V_{DD} pin; diode to V_{SS}
E009	V_{SS} pin; diode to V_{DD}
E027	analog input pin; diode to V_{DD} and V_{SS}
HPF01	digital input pin; CMOS levels, diode to V_{SS}
HPP01	digital input pin; CMOS levels, diode to V_{DD} and V_{SS}
HUP07	digital input pin; CMOS levels with hysteresis, pull-up resistor to V_{DD}, diode to V_{DD} and V_{SS}
IOI41	I^2C-bus pull-down output stage; CMOS input levels, diode to V_{SS}
OPF20	digital output pin; CMOS levels

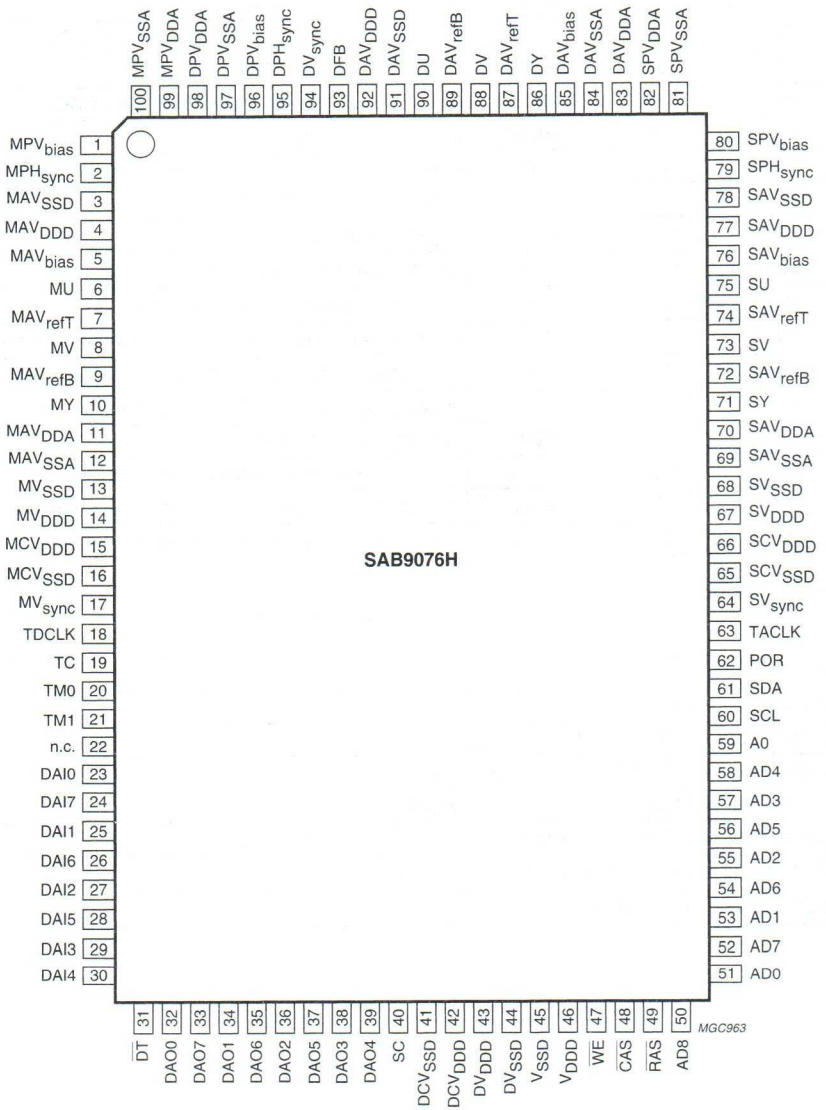


Fig.2 Pin configuration.

VHF, UHF and Hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5330T

GENERAL DESCRIPTION

The TDA5330T is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small 3-band tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B and C
- Balanced oscillator for band B and C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with an output impedance of 100 Ω
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		$V_{19-2,\ 26}$	–	12	–	V
Band A frequency range		f_A	48	–	180	MHz
Band B frequency range		f_B	160	–	470	MHz
Band C frequency range		f_C	430	–	860	MHz
Conversion noise		F	7	–	11	dB
Band A input voltage	1% cross-modulation	V_{24-26}	–	100	–	dBμV
Band B and C input power	1% cross-modulation	P_I	–	–21	–	dBm
Band A voltage gain		G_v	–	24	–	dB
Band B voltage gain		G_v	–	37	–	dB
Band C voltage gain		G_v	–	36	–	dB

PACKAGE OUTLINE

28-lead mini-pack , plastic (SO20; SOT163A); SOT 163-1; 1996 November 28.

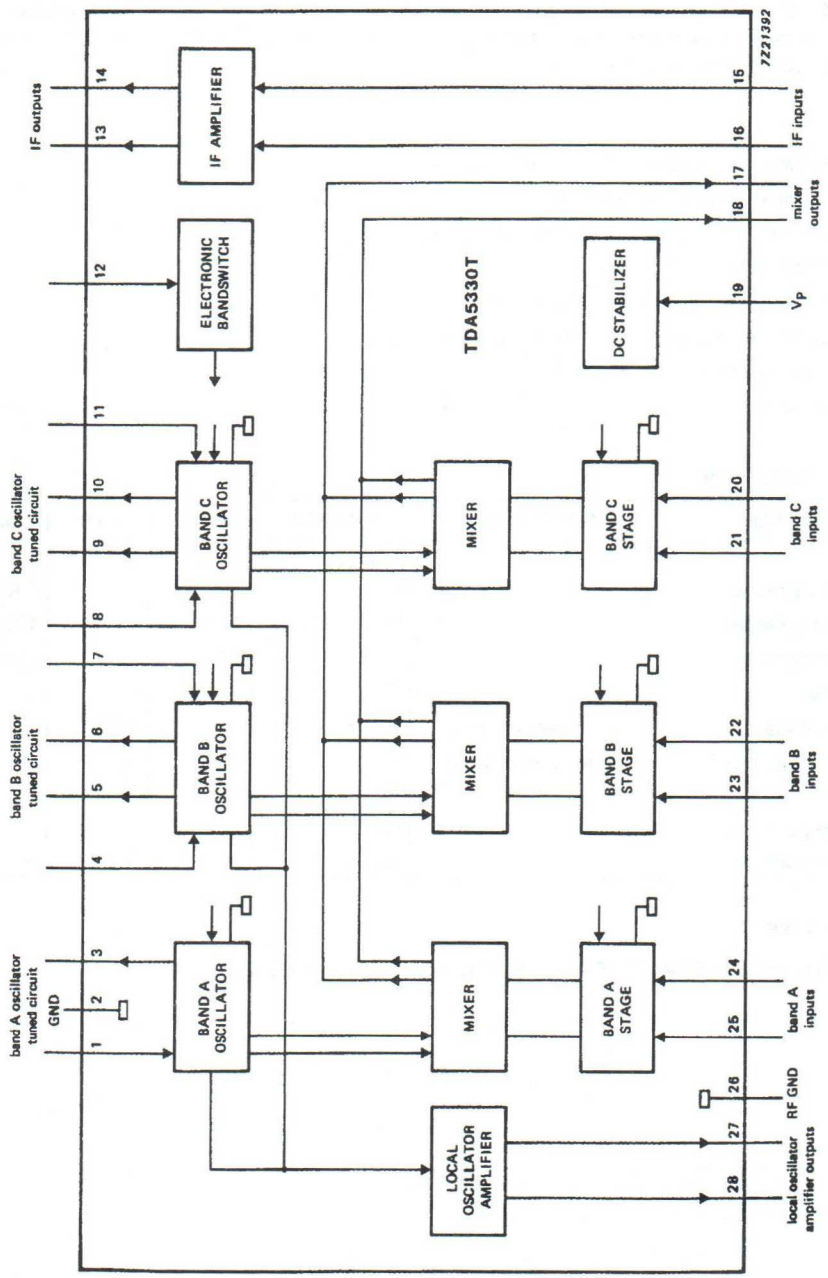


Fig.1 Block diagram.

VHF, UHF and Hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5330T

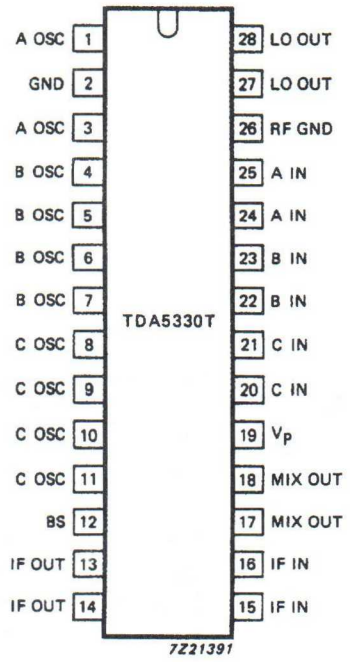


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	C OSC	band C oscillator input
9	C OSC	band C oscillator output
10	C OSC	band C oscillator output
11	C OSC	band C oscillator input
12	BS	electronic bandswitch
13	IF OUT	IF amplifier output
14	IF OUT	IF amplifier output
15	IF IN	IF amplifier input
16	IF IN	IF amplifier input
17	MIX OUT	mixer output
18	MIX OUT	mixer output
19	V_P	positive supply voltage
20	C IN	band C input
21	C IN	band C input
22	B IN	band B input
23	B IN	band B input
24	A IN	band A input
25	A IN	band A input
26	RF GND	ground for RF inputs
27	LO OUT	local oscillator amplifier output
28	LO OUT	local oscillator amplifier output

Double mixer/oscillator for TV and VCR tuners

TDA5332T

GENERAL DESCRIPTION

The TDA5332T is an integrated circuit that performs the mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B
- Balanced oscillator for band B
- SAW filter preamplifier with an output impedance of 75 Ω in application
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_P	–	12	–	V
Band A frequency range	depending on application	f_A	45	–	470	MHz
Band B frequency range	depending on application	f_B	160	–	860	MHz
Band A noise factor	50 MHz	NF_A	–	7.5	–	dB
Band B noise factor	860 MHz	NF_B	–	9	–	dB
Band A input voltage	1% cross-modulation	V_{18-20}	–	100	–	dBμV
Band B input power	1% cross-modulation note 5	P_I	–	–21	–	dBm
Band A voltage gain		G_{VA}	–	25	–	dB
Band B voltage gain		G_{VB}	–	36	–	dB

PACKAGE OUTLINE

20-lead mini-pack, plastic (SO20L; SOT163A); SOT163-1; 1996 November 29.

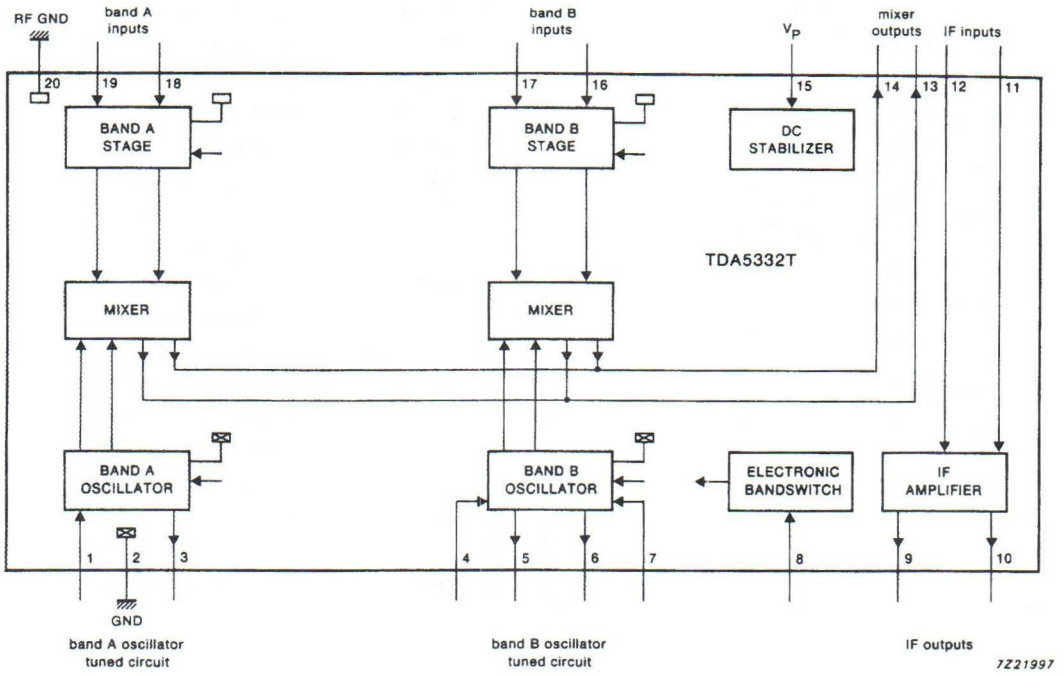


Fig.1 Block diagram.

Double mixer/oscillator for TV and VCR tuners

TDA5332T

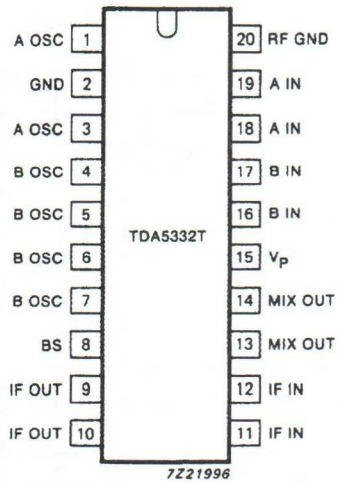


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	BS	electronic bandswitch
9	IF OUT	IF amplifier output
10	IF OUT	IF amplifier output
11	IF IN	IF amplifier input
12	IF IN	IF amplifier input
13	MIX OUT	mixer output
14	MIX OUT	mixer output
15	V_P	positive supply voltage
16	B IN	band B input
17	B IN	band B input
18	A IN	band A input
19	A IN	band A input
20	RF GND	ground for RF inputs

9 V VHF, hyperband and UHF mixer/oscillator for TV and VCR 3-band tuners

TDA5630; TDA5631

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

APPLICATIONS

- 3-band all channel TV and VCR tuners
- Any standard.

GENERAL DESCRIPTION

The TDA5630 and TDA5631 are monolithic integrated circuits that perform the mixer/oscillator functions for bands A, B and C in TV and VCR tuners. These low-power mixer/oscillators require a power supply of 9 V and are available in a very small package.

The devices give the designer the capability to design an economical and physically small 3-band tuner.

They are suitable for European standards, as illustrated in Fig.12, with the following RF bands: 48.25 to 168.25 MHz, 175.25 to 447.25 MHz and 455.25 to 855.25 MHz. With an appropriate tuned circuit, they are also suitable for NTSC all channel tuners (USA and Japan).

The tuner development time can be drastically reduced by using these devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	35	–	mA
f_{RF}	frequency range	RF input; band A; note 1	45	–	180	MHz
		RF input; band B; note 1	160	–	470	MHz
		RF input; band C; note 1	430	–	860	MHz
G_v	voltage gain	band A	–	25	–	dB
		band B	–	36	–	dB
		band C	–	36	–	dB
NF	noise figure	band A	–	7.5	–	dB
		band B	–	8	–	dB
		band C	–	9	–	dB
V_o	output voltage to get 1% cross modulation in channel	band A	–	118	–	dBμV
		band B	–	118	–	dBμV
		band C	–	118	–	dBμV

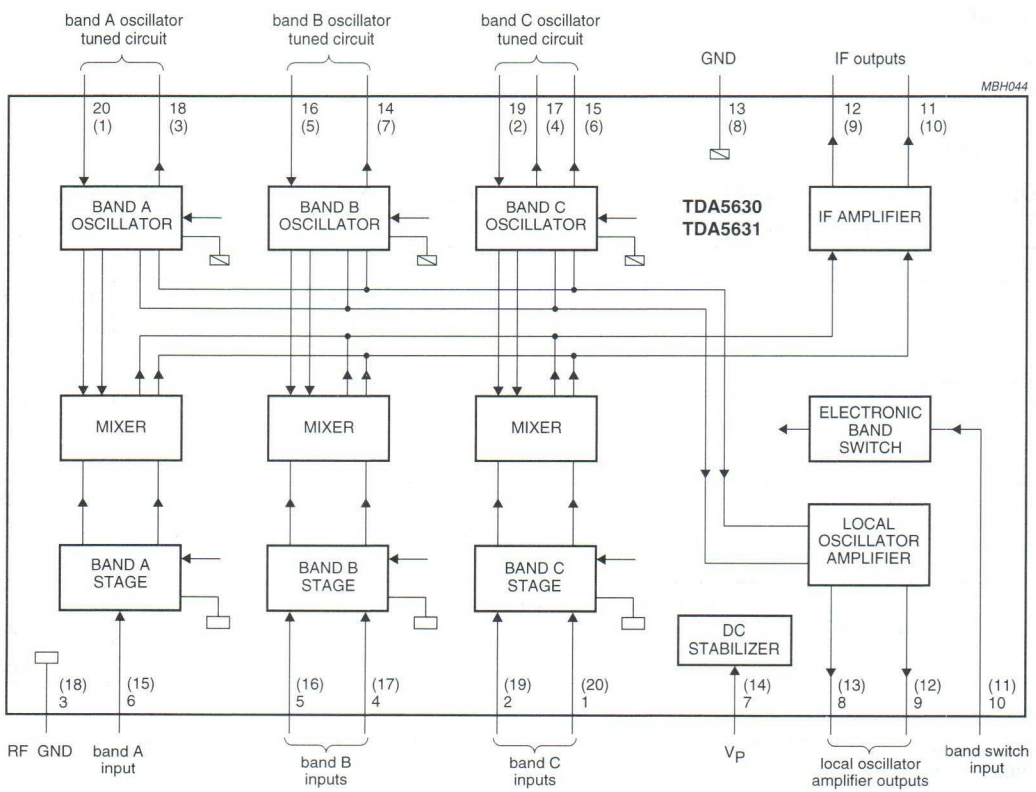
Note

1. The limits are related to the tank circuits used in Fig.12 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5630T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5630M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TDA5631T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5631M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM



The numbers given in parenthesis represent the TDA5631.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA5630	TDA5631	
CIN1	1	20	band C input 1
CIN2	2	19	band C input 2
RFGND	3	18	ground for RF inputs
BIN1	4	17	band B input 1
BIN2	5	16	band B input 2
AIN	6	15	band A input
V_P	7	14	supply voltage
LOOUT1	8	13	local oscillator amplifier output 1
LOOUT2	9	12	local oscillator amplifier output 2
BS	10	11	band switch input
IFOUT1	11	10	IF amplifier output 1
IFOUT2	12	9	IF amplifier output 2
GND	13	8	ground (0 V)
BOSCOC	14	7	band B oscillator output collector
COSCOC1	15	6	band C oscillator output collector 1
BOSCIB	16	5	band B oscillator input base
COSCOC2	17	4	band C oscillator output collector 2
AOSCOC	18	3	band A oscillator output collector
COSCIB	19	2	band C oscillator input base
AOSCIB	20	1	band A oscillator input base

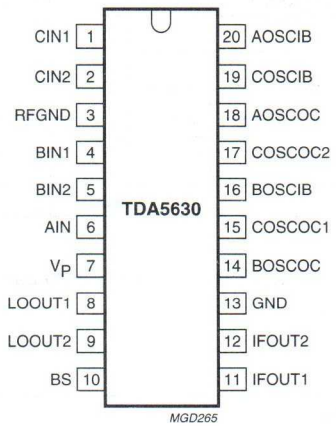


Fig.2 Pin configuration (TDA5630).

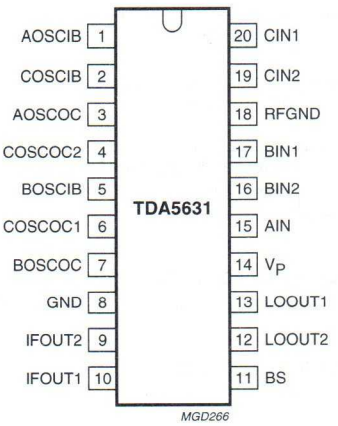


Fig.3 Pin configuration (TDA5631).

9 V VHF and UHF mixer/oscillator for TV and VCR cable tuners

TDA5630BT

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- Balanced mixer with a common base input for band C
- 3-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive a SAW filter
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

APPLICATIONS

- Cable tuners for TV and VCR (switched concept for VHF)
- Recommended RF bands for Europe: 48.25 to 105.25 MHz, 112.25 to 294.25 MHz and 471.25 to 855.25 MHz
- Recommended RF bands for the USA: 55.25 to 133.25 MHz, 139.25 to 361.25 MHz and 367.25 to 801.25 MHz.

GENERAL DESCRIPTION

The TDA5630BT is a monolithic integrated circuit that performs VHF and UHF mixer/oscillator functions in TV and VCR cable tuners. With a proper oscillator application and by using a switchable inductor to split the VHF band into two sub-bands, the full VHF/UHF TV bands can be covered. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small cable tuner.

The tuner development time can be drastically reduced by using this device.

Frequency bands are determined by the external tank circuit. They can be adapted to various standards.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	48	–	mA
f_{RF}	frequency range (picture carrier)	RF input; band A; note 1	45	–	470	MHz
		RF input; band C; note 1	430	–	860	MHz
G_v	voltage gain	band A	–	25	–	dB
		band C	–	36	–	dB
NF	noise figure	band A	–	7.5	–	dB
		band C	–	9.0	–	dB
V_o	output voltage to get 1% cross modulation in channel	band A	–	118	–	dBμV
		band C	–	120	–	dBμV

Note

1. The limits are related to the tank circuits used in Fig.11 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5630BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

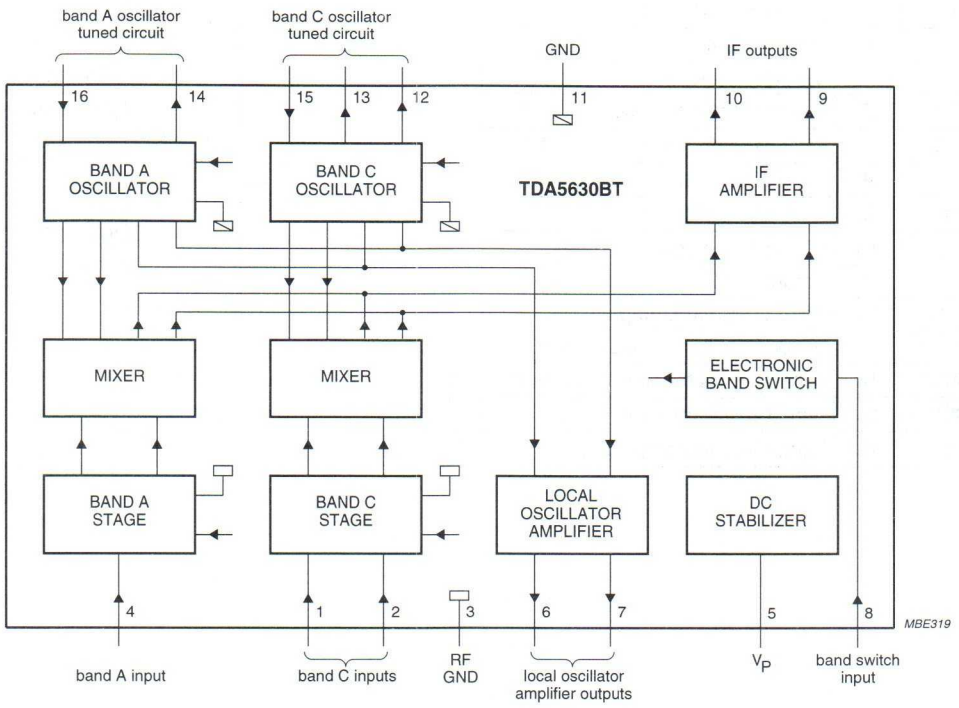


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CIN1	1	band C input 1
CIN2	2	band C input 2
RFGND	3	ground for RF inputs
AIN	4	band A input
V_P	5	supply voltage
LOOUT1	6	local oscillator amplifier output 1
LOOUT2	7	local oscillator amplifier output 2
BS	8	band switch input
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
GND	11	ground (0 V)
COSCOC1	12	band C oscillator output collector 1
COSCOC2	13	band C oscillator output collector 2
AOSCOC	14	band A oscillator output collector
COSCIB	15	band C oscillator input base
AOSCIB	16	band A oscillator input base

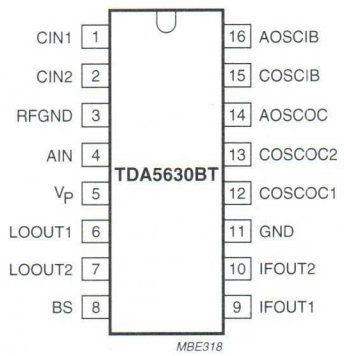


Fig.2 Pin configuration.

9 V VHF and UHF mixers/oscillators for TV and VCR cable tuners

TDA5632; TDA5633

FEATURES

- Balanced mixer with a common emitter input for band A
- 2-pin oscillator for band A
- Balanced mixer with a common base input for band C
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive a 75 Ω load
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter connected between the mixer output and the IF amplifier input.

APPLICATIONS

- Cable tuners for TV and VTR; switched concept for VHF
- Recommended RF bands for Europe: 48.25 to 105.25 MHz, 112.25 to 294.25 MHz and 471.25 to 855.25 MHz
- Recommended RF bands for the USA: 55.25 to 133.25 MHz, 139.25 to 361.25 MHz and 367.25 to 801.25 MHz.

DESCRIPTION

The TDA5632 and TDA5633 are monolithic integrated circuits that perform VHF and UHF mixer/oscillator functions in TV and VCR cable tuners. With correct oscillator application and by using a switchable inductor to split the VHF band into two sub-bands, the full VHF/UHF TV bands can be covered. These low-power mixers/oscillators require a power supply of 9 V and are available in a very small package.

The devices provide the designer with the capability to design an economical and physically small cable tuner.

The tuner development time can be drastically reduced by using this device.

Frequency bands are determined by the external tank circuit. They can be adapted to various standards.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	40	–	mA
f_{RF}	frequency range (picture carrier)	RF input; band A; note 1	57.5	–	357.5	MHz
		RF input; band C; note 1	469.5	–	887.5	MHz
G_v	voltage gain	band A (75 Ω load)	–	19	–	dB
		band C (75 Ω load)	–	30	–	dB
NF	noise figure	band A (75 Ω load)	–	10	–	dB
		band C (75 Ω load)	–	9.5	–	dB
V_o	output voltage to obtain 1% cross modulation in channel	band A (75 Ω load)	–	110	–	dBμV
		band C (75 Ω load)	–	110	–	dBμV

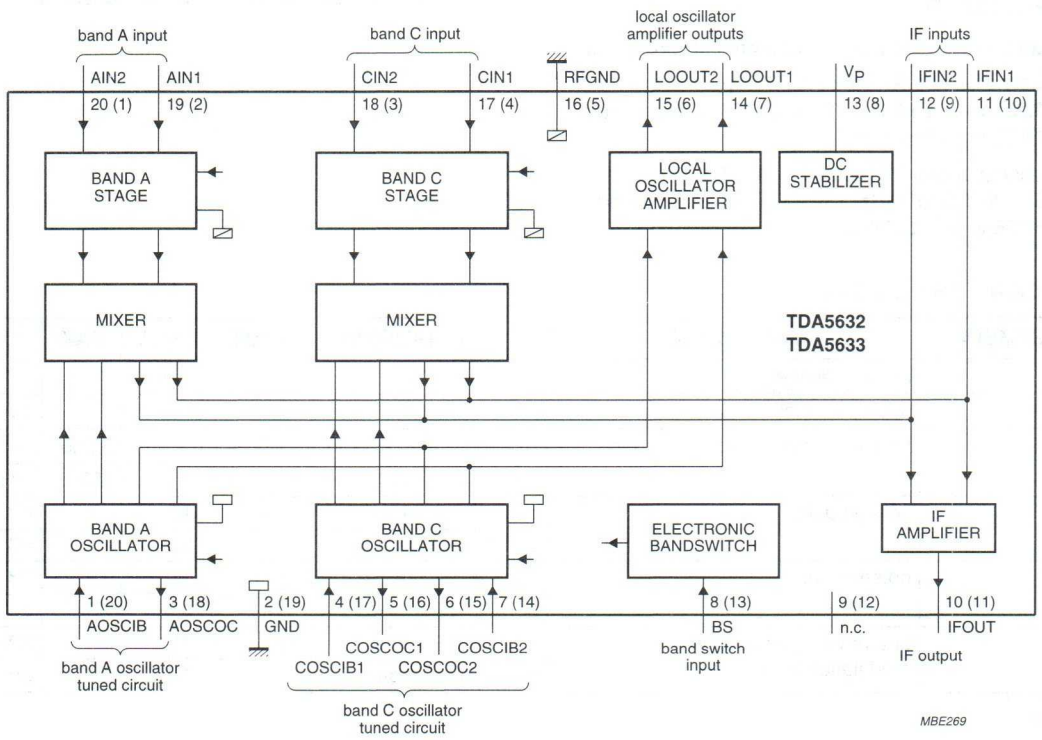
Note

1. The limits are related to the tank circuits used in Fig.10 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components. Another UHF frequency range is available by modifying the tank circuit. The modification enables the following frequency range:
   a) RF frequencies from 361.25 to 801.25 MHz (picture carrier).
   b) Oscillator frequencies from 407 to 847 MHz. For this UHF range, L4 = 3 turns (diameter = 3.5 mm).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5632T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5632M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TDA5633T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5633M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA5633.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA5632	TDA5633	
AOSCIB	1	20	band A oscillator input base
GND	2	19	ground (0 V)
AOSCOC	3	18	band A oscillator output collector
COSCIB1	4	17	band C oscillator input base 1
COSCOC1	5	16	band C oscillator output collector 1
COSCOC2	6	15	band C oscillator output collector 2
COSCIB2	7	14	band C oscillator input base 2
BS	8	13	band switch input
n.c.	9	12	not connected
IFOUT	10	11	IF amplifier output
IFIN1	11	10	IF amplifier input 1
IFIN2	12	9	IF amplifier input 2
V_P	13	8	supply voltage
LOOUT1	14	7	local oscillator amplifier output 1
LOOUT2	15	6	local oscillator amplifier output 2
RFGND	16	5	ground for RF inputs
CIN1	17	4	band C input 1
CIN2	18	3	band C input 2
AIN1	19	2	band A input 1
AIN2	20	1	band A input 2

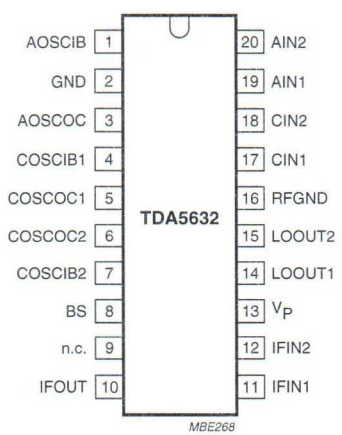


Fig.2 Pin configuration (TDA5632).

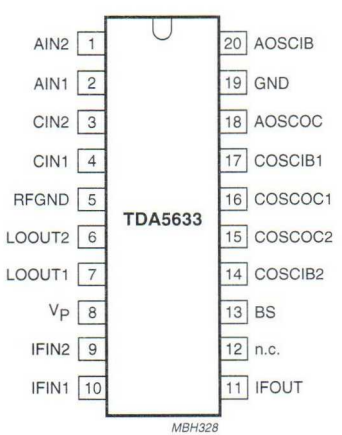


Fig.3 Pin configuration (TDA5633).

9 V VHF hyperband and UHF mixer/oscillator for TV and VCR 3-band

TDA5636B; TDA5637B

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter between the mixer output and the IF amplifier input
- Pin-to-pin compatible with TDA5636; TDA5637 family (same function with asymmetrical IF output).

APPLICATIONS

- 3-band all channel TV and VCR tuners
- Any standard.

GENERAL DESCRIPTION

The TDA5636B and TDA5637B are monolithic integrated circuits that perform the mixer/oscillator functions for bands A, B and C in TV and VCR tuners. These low-power mixer/oscillators require a power supply of 9 V and are available in a very small package.

The devices give the designer the capability to design an economical and physically small 3-band tuner.

They are suitable for European standards, as illustrated in Fig.17, with the following RF bands:

- 48.25 to 168.25 MHz
- 175.25 to 447.25 MHz
- 455.25 to 855.25 MHz.

With an appropriate tuned circuit, they are also suitable for NTSC all channel tuners (USA and Japan). The tuner development time can be drastically reduced by using these devices.

These circuits belong to the TDA5636/TDA5737 family which has exactly the same function with an IF amplifier having an asymmetrical IF output to drive a 75 Ω load. It is possible to build tuners with either an asymmetrical or a symmetrical IF output with one main tuner lay-out.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current	band A	–	43	–	mA
		band B	–	39	–	mA
		band C	–	42	–	mA
f_{RF}	frequency range	RF input; band A; note 1	45	–	180	MHz
		RF input; band B; note 1	160	–	470	MHz
		RF input; band C; note 1	430	–	860	MHz
G_v	voltage gain	band A	–	25	–	dB
		band B	–	36	–	dB
		band C	–	36	–	dB
NF	noise figure	band A	–	7.5	–	dB
		band B	–	6	–	dB
		band C	–	7	–	dB
V_o	output voltage to get 1% cross modulation in channel	band A	–	121	–	dBμV
		band B	–	120	–	dBμV
		band C	–	119	–	dBμV

Note

1. The limits are related to the tank circuits used in Fig.17 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5636BT[1]	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA5636BM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA5637BT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA5637BM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

Note

1. The TDA5636BT is available on request.

BLOCK DIAGRAM

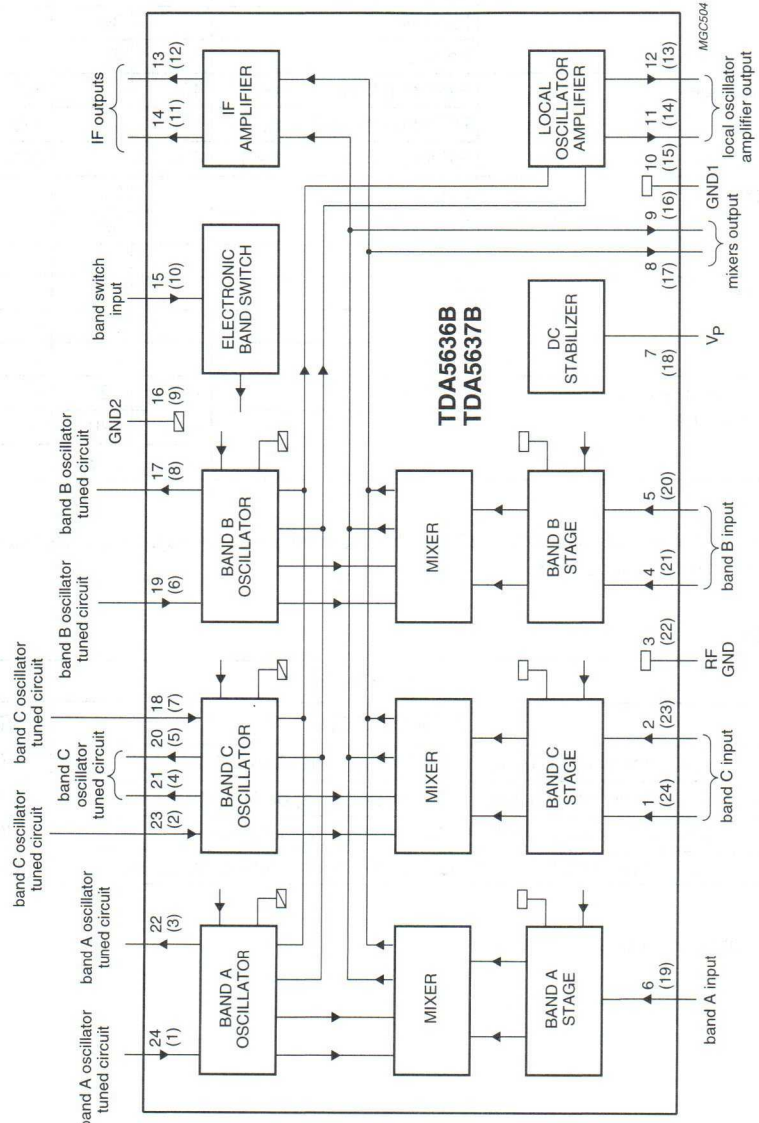


Fig.1 Block diagram.

The numbers given in parenthesis represent the TDA5637B.
The TDA5636B and TDA5637B are pin compatible with the TDA5636 and TDA5637 respectively.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA5636B	TDA5637B	
CIN1	1	24	band C input 1
CIN2	2	23	band C input 2
RFGND	3	22	ground for RF inputs
BIN1	4	21	band B input 1
BIN2	5	20	band B input 2
AIN	6	19	band A input
V_P	7	18	supply voltage
MIXOUT1	8	17	mixers output 1
MIXOUT2	9	16	mixers output 2
GND1	10	15	ground 1 (0 V)
LOOUT1	11	14	local oscillator amplifier output 1
LOOUT2	12	13	local oscillator amplifier output 2
IFOUT1	13	12	IF amplifier output 1
IFOUT2	14	11	IF amplifier output 2
BS	15	10	electronic band switch input
GND2	16	9	ground 2 (0 V)
BOSCOC	17	8	band B oscillator output collector
COSCIB1	18	7	band C oscillator input base 1
BOSCIB	19	6	band B oscillator input base
COSCOC1	20	5	band C oscillator output collector 1
COSCOC2	21	4	band C oscillator output collector 2
AOSCOC	22	3	band A oscillator output collector
COSCIB2	23	2	band C oscillator input base 2
AOSCIB	24	1	band A oscillator input base

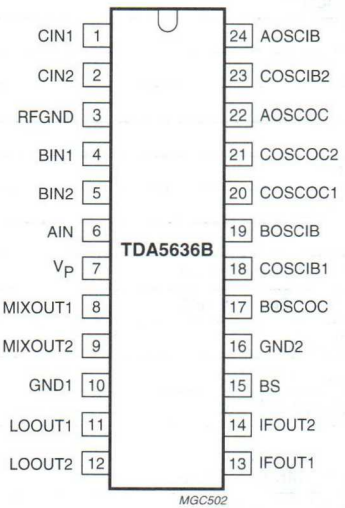


Fig.2 Pin configuration (TDA5636B).

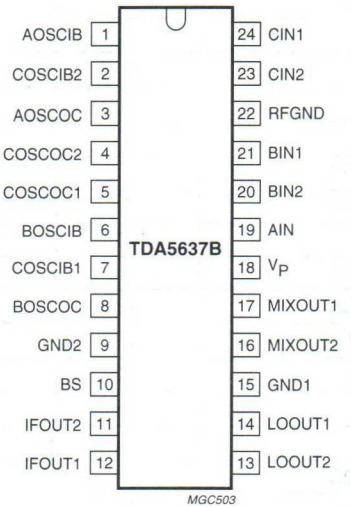


Fig.3 Pin configuration (TDA5637B).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5731M

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- 3-pin oscillator for band C
- Balanced mixer with a common base input for band B and C (balanced input)
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Electronic band switch.

GENERAL DESCRIPTION

The TDA5731M is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 5 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

In addition, when hyperband is not required, the TDA5731M may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHFI and VHFIII in band A and the tuned circuit of band C for UHF.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	36	–	mA
f_R	frequency range	band A	42	–	180	MHz
		band B	160	–	470	MHz
		band C	430	–	860	MHz
N	noise figure	band A	–	7.5	–	dB
		band B	–	8.0	–	dB
		band C	–	9.0	–	dB
IP	intermodulation	band A	–	–66	–	dB
		band B	–	–66	–	dB
		band C	–	–66	–	dB
G_v	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	33	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5731M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

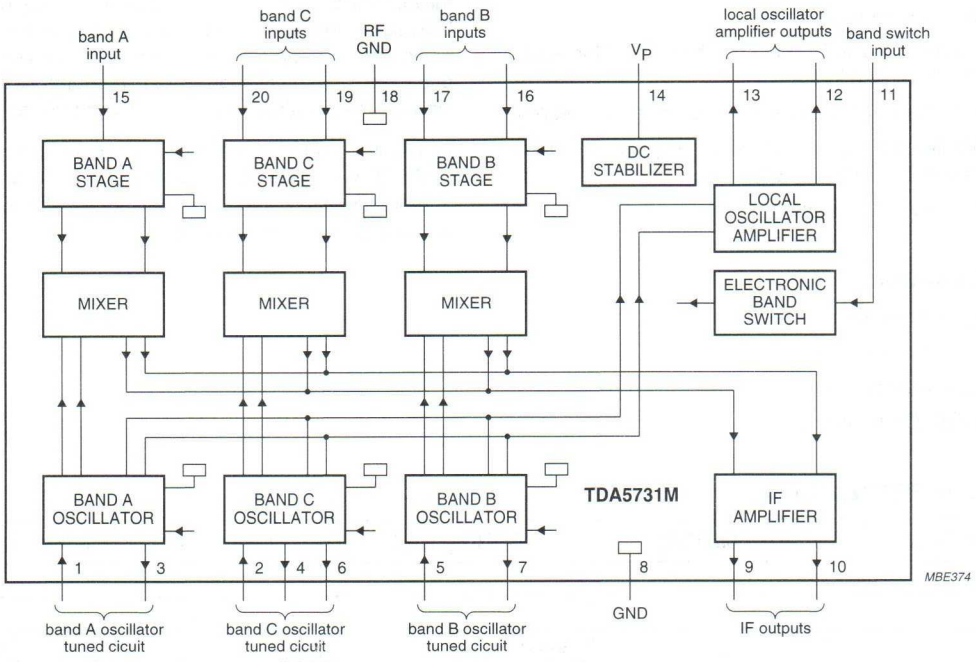


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
COSCIB	2	band C oscillator input base
AOSCOC	3	band A oscillator output collector
COSCOC1	4	band C oscillator output collector 1
BOSCIB	5	band B oscillator input base
COSCOC2	6	band C oscillator output collector 2
BOSCOC	7	band B oscillator output collector
GND	8	ground (0 V)
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
BS	11	band switch input
LOOUT1	12	local oscillator amplifier output 1
LOOUT2	13	local oscillator amplifier output 2
V_P	14	supply voltage
AIN	15	band A input
BIN1	16	band B input 1
BIN2	17	band B input 2
RFGND	18	ground for RF input
CIN1	19	band C input 1
CIN2	20	band C input 2

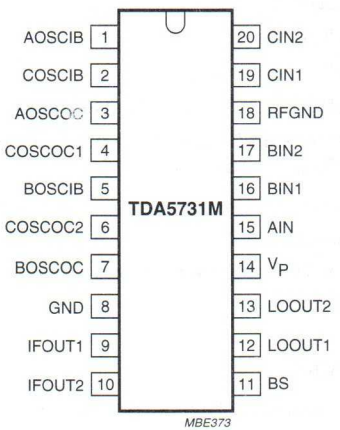


Fig.2 Pin configuration.

5 V VHF, hyperband and UHF mixers/oscillators for TV and VCR 3-band tuners

TDA5736; TDA5737

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band B
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter between the mixer output and the IF amplifier input.

GENERAL DESCRIPTION

The TDA5736 and TDA5737 are monolithic integrated circuits that perform the mixer/oscillator functions for bands A, B and C in TV and VCR tuners. These low power mixer/oscillators require a power supply of 5 V and are available in a very small package.

These devices give the designer the capability to design an economical and physically small 3-band tuner.

They are suitable for European standards, as illustrated in Fig.17, with the following RF bands: 48.25 to 168.25 MHz, 175.25 to 447.25 MHz and 455.25 to 855.25 MHz. With an appropriate tuned circuit, they are also suitable for NTSC all channel tuners (USA and Japan).

The tuner development time can be drastically reduced by using these devices.

APPLICATIONS

- 3-band all channel TV and VCR tuners
- Any standard.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	50	–	mA
f_{RF}	frequency range	RF input; band A; note 1	41	–	171	MHz
		RF input; band B; note 1	166	–	451	MHz
		RF input; band C; note 1	446	–	861	MHz
G_V	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	34	–	dB
NF	noise figure	band A	–	7.5	–	dB
		band B	–	8	–	dB
		band C	–	9	–	dB
V_o	output voltage level causing 1% cross modulation in channel	band A	–	116	–	dBμV
		band B	–	115	–	dBμV
		band C	–	115	–	dBμV

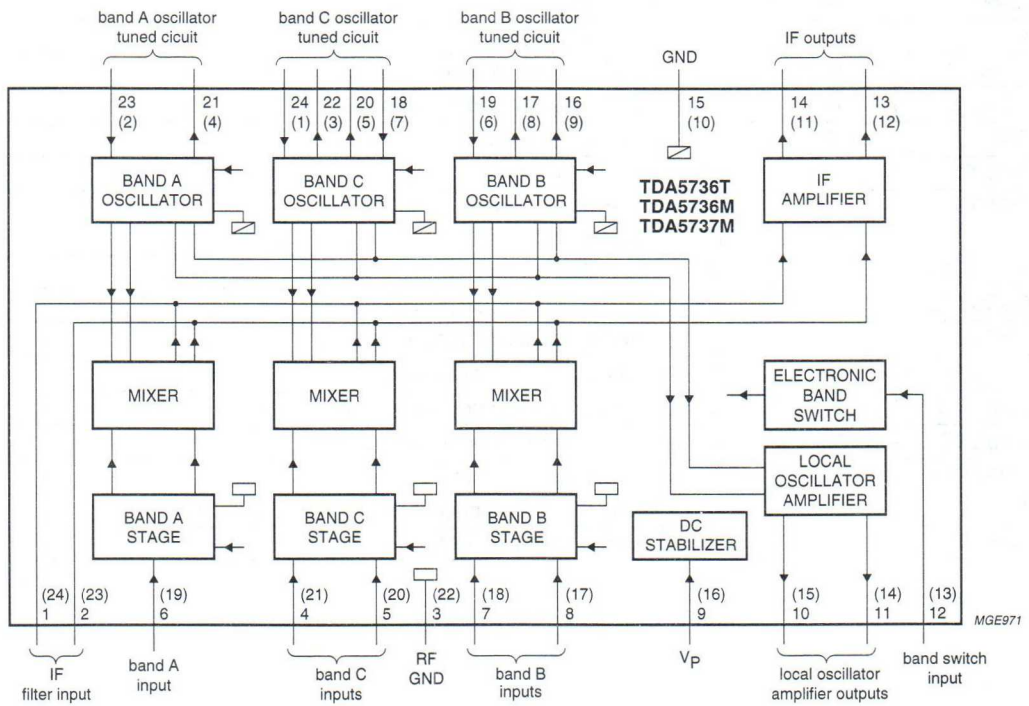
Note

1. The limits are related to the tank circuits used in Fig.17 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5736T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA5736M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA5737M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM



The numbers in parenthesis represent the TDA5737M.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA5736	TDA5737	
IFIN1	1	24	IF filter input 1
IFIN2	2	23	IF filter input 2
RFGND	3	22	ground for RF inputs
CIN1	4	21	band C input 1
CIN2	5	20	band C input 2
AIN	6	19	band A input
BIN1	7	18	band B input 1
BIN2	8	17	band B input 2
V_P	9	16	supply voltage
LOOUT1	10	15	local oscillator amplifier output 1
LOOUT2	11	14	local oscillator amplifier output 2
BS	12	13	band switch input
IFOUT1	13	12	IF amplifier output 1
IFOUT2	14	11	IF amplifier output 2
GND	15	10	ground (0 V)
BOSCOC1	16	9	band B oscillator output collector 1
BOSCOC2	17	8	band B oscillator output collector 2
COSCIB1	18	7	band C oscillator input base 1
BOSCIB	19	6	band B oscillator input base
COSCOC1	20	5	band C oscillator output collector 1
AOSCOC	21	4	band A oscillator output collector
COSCOC2	22	3	band C oscillator output collector 2
AOSCIB	23	2	band A oscillator input base
COSCIB2	24	1	band C oscillator input base 2

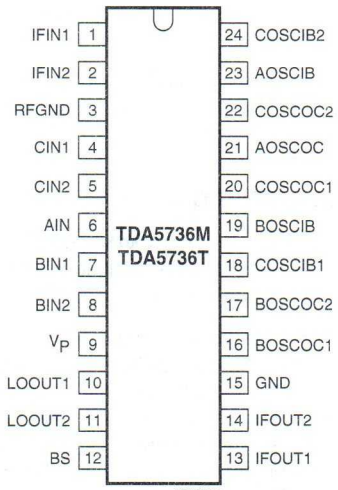


Fig.2 Pin configuration (TDA5736M, TDA5736T).

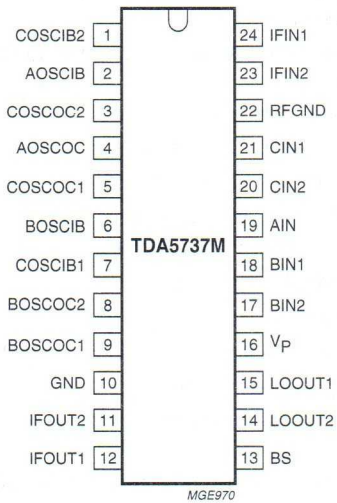


Fig.3 Pin configuration (TDA5737M).

5 V mixers/oscillators and synthesizers for cable TV and VCR 2-band tuners

TDA6402; TDA6402A; TDA6403; TDA6403A

FEATURES

- Single-chip 5 V mixer/oscillator and synthesizer for cable TV and VCR tuners
- Synthesizer function compatible with existing TSA5526
- Universal bus protocol (I^2C-bus or 3-wire bus)
  - bus protocol for 18 or 19-bit transmission (3-wire bus)
  - extra protocol for 27-bit transmission (test modes and features for 3-wire bus)
  - address + 4 data bytes transmission (I^2C-bus 'write' mode)
  - address + 1 status byte (I^2C-bus 'read' mode)
  - 4 independent I^2C-bus addresses
- 1 PNP buffer for UHF band selection (25 mA)
- 3 PNP buffers for general purpose, e.g. 2 VHF sub-bands, FM sound trap (25 mA)
- 33 V tuning voltage output
- In-lock detector
- 5-step A/D converter (3 bits in I^2C-bus mode)
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge pump current (60 or 280 μA)
- Programmable automatic charge pump current switch
- Varicap drive disable
- Mixer/oscillator function compatible with existing TDA5732
- Balanced mixer with a common emitter input for VHF (single input)
- Balanced mixer with a common base input for UHF (balanced input)
- 2-pin common emitter oscillator for VHF
- 4-pin common emitter oscillator for UHF
- IF preamplifier with asymmetrical 75 Ω output impedance to drive a low-ohmic impedance (75 Ω)
- Low power
- Low radiation
- Small size
- The TDA6402A and TDA6403A differ from the TDA6402 and TDA6403 by the UHF port protocol in the I^2C bus mode (see Tables 3 and 4).

APPLICATIONS

- Cable tuners for TV and VCR (switched concept for VHF)
- Recommended RF bands for the USA: 55.25 to 133.25 MHz, 139.25 to 361.25 MHz and 367.25 to 801.25 MHz.

GENERAL DESCRIPTION

The TDA6402, TDA6402A, TDA6403 and TDA6403A are programmable 2-band mixers/oscillators and synthesizers intended for VHF/UHF cable tuners (see Fig.1).

The devices include two double balanced mixers and two oscillators for the VHF and UHF band respectively, an IF amplifier and a PLL synthesizer. The VHF band can be split-up into two sub-bands using a proper oscillator application and a switchable inductor. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling. Four PNP ports are provided. Band selection is provided by using pin PUHF. When PUHF is 'ON', the UHF mixer-oscillator is active and the VHF band is switched off. When PUHF is 'OFF', the VHF mixer-oscillator is active and the UHF band is 'OFF'. PVHFL and PVHFH are used to select the VHF sub-bands. FMST is a general purpose port, that can be used to switch an FM sound trap. When it is used, the sum of the collector currents has to be limited to 30 mA.

The synthesizer consists of a divide-by-eight prescaler, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 7.8125 kHz, 6.25 kHz or 3.90625 kHz with a 4 MHz crystal.

The device can be controlled according to the I²C-bus format or 3-wire bus format depending on the voltage applied to pin SW (see Table 2). In the 3-wire bus mode (SW = HIGH), pin LOCK/ADC is the lock output. The LOCK output is LOW when the PLL loop is locked. In the I²C-bus mode (SW = LOW), the lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (Status Byte; SB) during a READ operation in I²C-bus mode only. The Analog-to-Digital Converter (ADC) input is available on pin LOCK/ADC for digital AFC control in the I²C-bus mode only. The ADC code is read during a READ operation on the I²C-bus (see Table 11). In test mode, pin LOCK/ADC is used as a TEST output for f_{REF} and $\frac{1}{2}f_{DIV}$, in both I²C-bus mode and 3-wire bus mode (see Table 7).

When the automatic charge-pump current switch mode is activated and when the loop is phase-locked, the charge-pump current value is automatically switched to LOW. This action is taken to improve the carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a READ operation on the I²C-bus (see Table 9).

I²C-bus format (SW = GND)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four ports, set the charge-pump current and set the reference divider ratio. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage on input CE (see Table 6).

3-wire bus format (SW = V_{CC} or OPEN)

Data is transmitted to the devices during a HIGH-level on input CE (enable line). The device is compatible with 18-bit and 19-bit data formats, as shown in Figs 4 and 5. The first four bits are used to program the PNP ports and the remaining bits control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes (see Fig.6).

It is not allowed to address the devices with words whose length is different from 18, 19 or 27 bits.

Table 1 Data word length for 3-wire bus

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER(1)	FREQUENCY STEP
TDA6402; TDA6402A; TDA6403; TDA6403A	18-bit	512	62.50 kHz
TDA6402; TDA6402A; TDA6403; TDA6403A	19-bit	1024	31.25 kHz
TDA6402; TDA6402A; TDA6403; TDA6403A	27-bit	programmable	programmable

Note

1. The selection of the reference divider is given by an automatic identification of the data word length. When the 27-bit format is used, the reference divider is controlled by RSA and RSB bits (see Table 8). More details are given in Chapter "PLL functional description", Section "3-wire bus mode (SW = OPEN or V_{CC})".

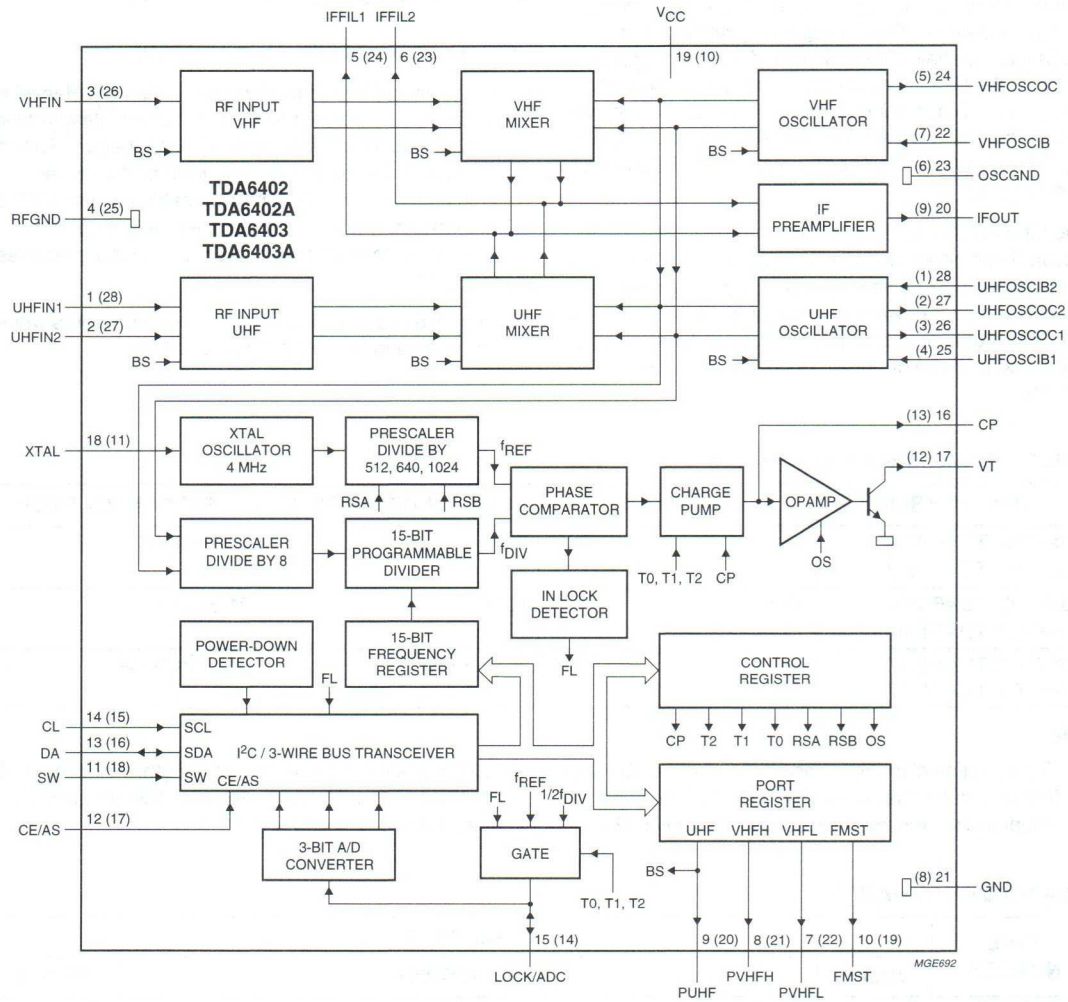
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6402M; TDA6402AM(1)	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1
TDA6403M; TDA6403AM	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

Note

1. The TDA6402AM is available on request.

BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA6403 and TDA6403A.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6402; TDA6402A	TDA6403; TDA6403A	
UHFIN1	1	28	UHF RF input 1
UHFIN2	2	27	UHF RF input 2
VHFIN	3	26	VHF RF input
RFGND	4	25	RF ground
IFFIL1	5	24	IF filter output 1
IFFIL2	6	23	IF filter output 2
PVHFL	7	22	PNP port output, general purpose (e.g. VHF low sub-band)
PVHFH	8	21	PNP port output, general purpose (e.g. VHF high sub-band)
PUHF	9	20	PNP port output, UHF band
FMST	10	19	PNP port output, general purpose (e.g. FM sound trap)
SW	11	18	bus format selection input (I^2C-bus/3-wire bus)
CE/AS	12	17	Chip Enable/Address Selection input
DA	13	16	serial data input/output
CL	14	15	serial clock input
LOCK/ADC	15	14	lock detector output (3-wire bus)/ADC input (I^2C-bus)
CP	16	13	charge pump output
VT	17	12	tuning voltage output
XTAL	18	11	crystal oscillator input
V_{CC}	19	10	supply voltage
IFOUT	20	9	IF output
GND	21	8	digital ground
VHFOSCIB	22	7	VHF oscillator input base
OSCGND	23	6	oscillator ground
VHFOSCOC	24	5	VHF oscillator output collector
UHFOSCIB1	25	4	UHF oscillator input base 1
UHFOSCOC1	26	3	UHF oscillator output collector 1
UHFOSCOC2	27	2	UHF oscillator output collector 2
UHFOSCIB2	28	1	UHF oscillator input base 2

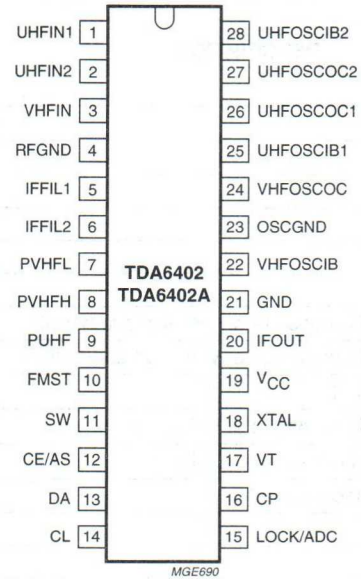


Fig.2 Pin configuration for TDA6402 and TDA6402A.

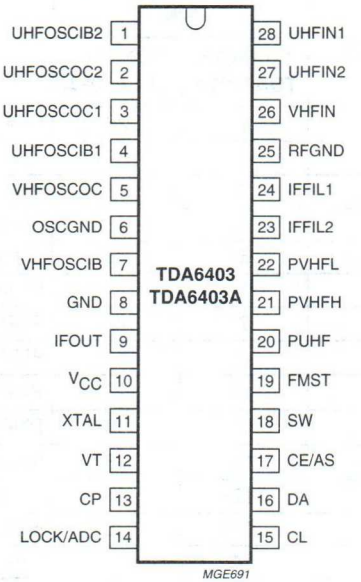


Fig.3 Pin configuration for TDA6403 and TDA6403A.

3 W mono BTL audio output amplifier TDA7056

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	2.5	3	–	W
G_V	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	–	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110[1]

Note

1. SOT110-1; 1996 August 21.

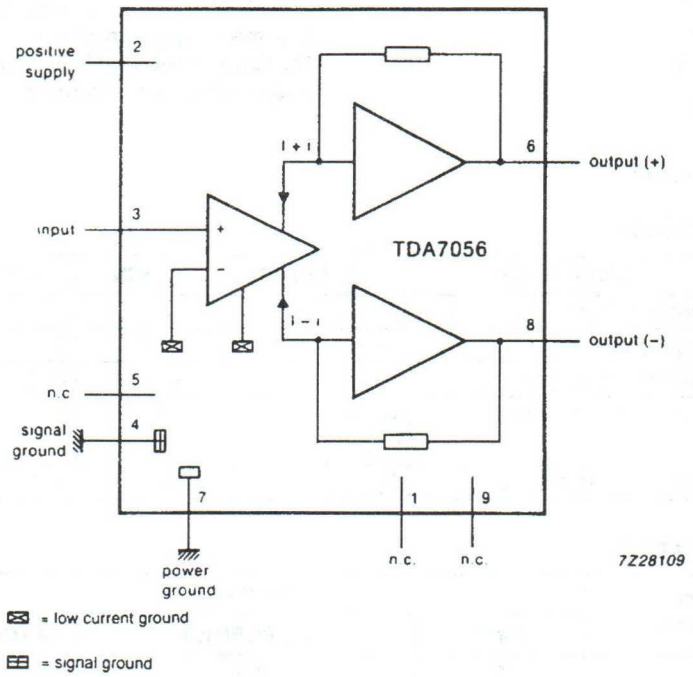


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (−)
9	n.c.

Smart card interface TDA8000; TDA8000T

FEATURES

- Two protected I/O lines
- V_{CC} regulation (5 V ±4%, 100 mA max. with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V ±2.5%, 50 mA max. programmable by two bits, with controlled rise and fall times)
- Clock generation (up to 8 MHz)
- Short-circuit, thermal and card extraction protections
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and deactivation sequences via an independent internal clock
- Enhanced ESD protections on card connections (4 kV min.)
- ISO 7816 approval.

APPLICATIONS

- Pay TV
- Telematics
- Cashless payment
- Multipurpose card-readers, etc.

GENERAL DESCRIPTION

The TDA8000 is a complete, low-cost analog interface which can be positioned between a smart card or a memory card (ISO 7816) and a microcontroller. It is approved for banking, telecom and pay TV applications.

The complete supply, protection and control functions are realized with only a few external components, which makes the TDA8000 very attractive for consumer applications. Application suggestions and support is available on request (see examples in Chapter "Application information").

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; V_{DD} = 12 V	–	25	–	mA
		active modes; unloaded	–	32	–	mA
V_{th2}	threshold voltage on V_{SUP}		4.5	–	4.68	V
V_{CC}	card supply voltage		4.8	5.0	5.2	V
I_{CC}	card supply current		–	–	–100	mA
V_H	high voltage supply for V_{PP}		–	–	30	V
I_{PP}	programming current	read mode; V_{PP} = 5 V	–	–	–50	mA
		write mode; V_{PP} > 5 V	–	–	–50	mA
t_{de}, t_{act}	deactivation/activation cycle duration		–	–	500	µs
P_{tot}	continuous total power dissipation	TDA8000; T_{amb} = +70 °C; see Fig.10	–	–	2	W
		TDA8000T; T_{amb} = +70 °C; see Fig.11	–	–	0.92	W
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8000	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8000T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

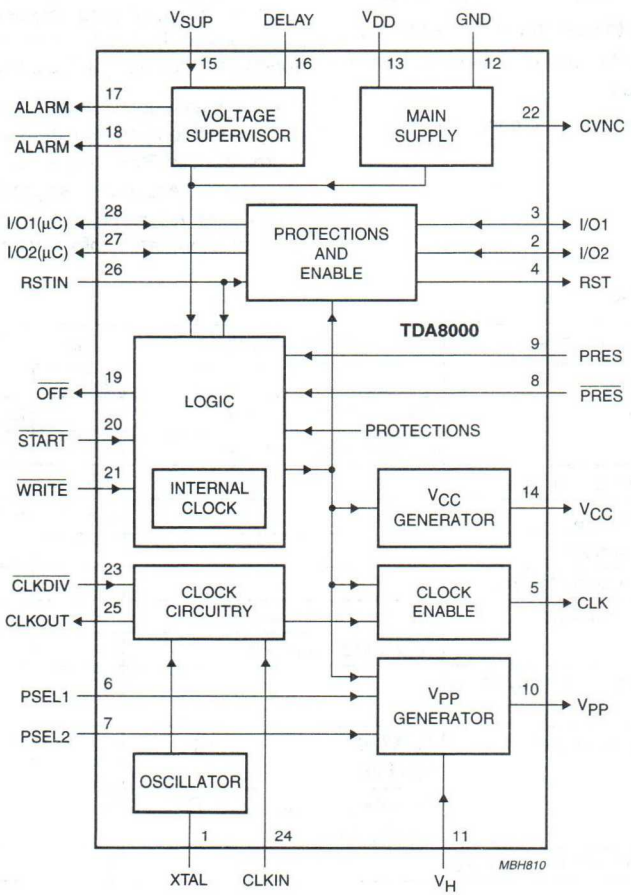


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal connection
I/O2	2	data line to/from the card
I/O1	3	data line to/from the card
RST	4	card reset output
CLK	5	clock output to the card
PSEL1	6	programming voltage selection input (see Table 1)
PSEL2	7	programming voltage selection input (see Table 1)
$\overline{PRES}$	8	card presence contact input (active LOW)
PRES	9	card presence contact input (active HIGH)
V_{PP}	10	card programming voltage output
V_H	11	high voltage supply for V_{PP} generation
GND	12	ground
V_{DD}	13	positive supply voltage
V_{CC}	14	card supply output voltage
V_{SUP}	15	voltage supervisor input
DELAY	16	external capacitor connection for delayed reset timing
ALARM	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{ALARM}$	18	open-collector reset output for the microcontroller (active LOW)
$\overline{OFF}$	19	interrupt output to the microcontroller (active LOW)
$\overline{START}$	20	microcontroller input for starting session (active LOW)
$\overline{WRITE}$	21	control input for applying programming voltage to the card (active LOW)
CVNC	22	internally generated 5 V reference, present when V_{DD} is on; to be decoupled externally (47 nF)
$\overline{CLKDIV}$	23	input for dividing/not dividing the CLKOUT frequency by two (active LOW)
CLKIN	24	external clock signal input
CLKOUT	25	clock output to the microcontroller, or another TDA8000
RSTIN	26	card reset input from the microcontroller (active HIGH)
I/O2(μC)	27	data line to/from the microcontroller; must not be left open-circuit, tie to CVNC if not used
I/O1(μC)	28	data line to/from the microcontroller; must not be left open-circuit, tie to CVNC if not used

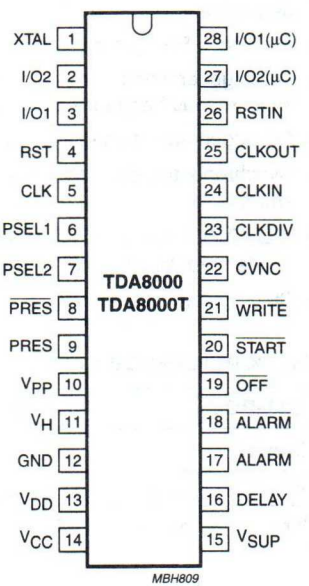


Fig.2 Pin configuration.

IC card interface TDA8002

FEATURES

- Single supply voltage interface (3.3 or 5 V environment)
- Low-power sleep mode
- Three specific protected half-duplex bidirectional buffered I/O lines
- V_{CC} regulation (5 V ±5%; I_{CC} < 65 mA at V_{DD} = 5 V, with controlled rise and fall times
- Thermal and short-circuit protections with current limitations
- Automatic ISO 7816 activation and deactivation sequences
- Enhanced ESD protections on card side (>6 kV)
- Clock generation for the card up to 12 MHz with synchronous frequency changes
- Clock generation up to 20 MHz (auxiliary clock)
- Synchronous and asynchronous cards (memory and smart cards)
- ISO 7816, GSM11.11 compatibility and EMV (Europay, Mastercard, Visa) compliant
- Step-up converter for V_{CC} generation
- Supply supervisor for spikes elimination and emergency deactivation.

APPLICATIONS

- IC card readers for:
  - GSM applications
  - banking
  - electronic payment
  - identification
  - Pay TV
  - road tolling.

GENERAL DESCRIPTION

The TDA8002 is a complete low-power, analog interface for asynchronous and synchronous cards. It can be placed between the card and the microcontroller. It performs all supply, protection and control functions. It is directly compatible with ISO 7816, GSM11.11 and EMV specifications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		3.0	5	6.5	V
I_{DD}	supply current	sleep mode	–	–	150	µA
		Idle mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	5	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	9	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 3 V	–	–	12	mA
Card supply						
$V_{CC(O)}$	output voltage	DC load <65 mA	4.75	–	5.25	V
$I_{CC(O)}$	output current	V_{CC} short-circuited to GND	–	–	100	mA
General						
f_{clk}	card clock frequency		0	–	12	MHz
T_{de}	deactivation sequence duration		60	80	100	µs
P_{tot}	continuous total power dissipation					
	TDA8002AT; TDA8002BT	T_{amb} = –25 to +85 °C	–	–	0.56	W
	TDA8002G	T_{amb} = –25 to +85 °C	–	–	0.46	W
T_{amb}	operating ambient temperature		–25	–	+85	°C

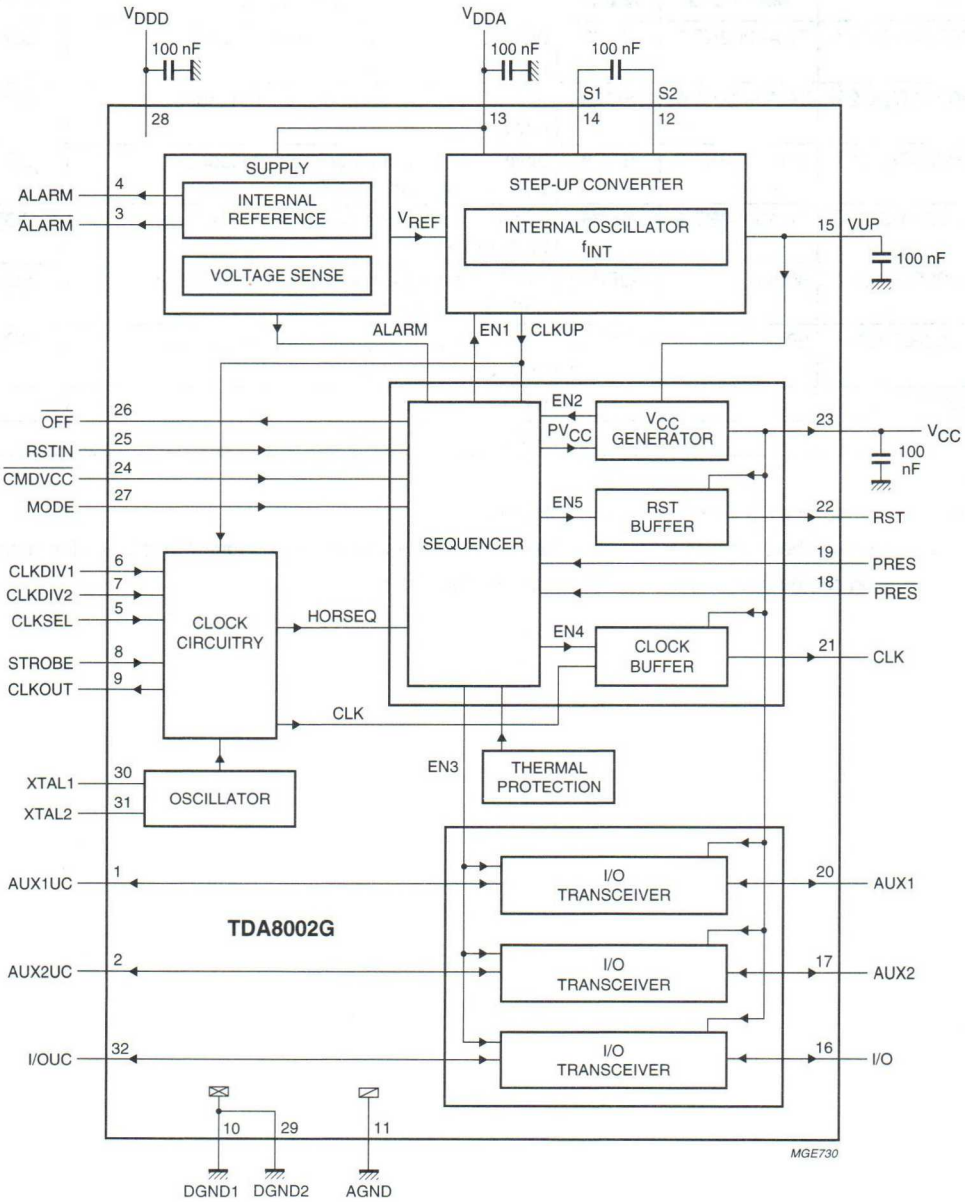
ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			
	MARKING	NAME	DESCRIPTION	VERSION
TDA8002AT/3/C2[2]	TDA8002AT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002AT/5/C2[3]	TDA8002AT/5	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002BT/3/C2[2]	TDA8002BT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002BT/5/C2[3]	TDA8002BT/5	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002G/3/C2[2]	80023	LQFP32	plastic low profile quad flat pack; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1
TDA8002G/5/C2[3]	80025	LQFP32	plastic low profile quad flat pack; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1
TDA8002U/3/C2[2]	–	–	wafer	–
TDA8002U/5/C2[3]	–	–	wafer	–

Notes

1. The /3 or /5 suffix indicates the voltage supervisor option.
2. The /3 version can be used with a 3 or 5 V power supply environment (see Chapter "Functional description").
3. The /5 version can be used with a 5 V power supply environment.

BLOCK DIAGRAM



All capacitors are mandatory.

Fig.1 Block diagram (TDA8002G in LQFP32 package).

PINNING

SYMBOL	PIN			I/O	DESCRIPTION
	TYPE A SO28	TYPE B SO28	TYPE G LQFP32		
XTAL1	1	1	30	I/O	crystal connection or input for external clock
XTAL2	2	2	31	I/O	crystal connection
I/OUC	3	3	32	I/O	data I/O line to and from microcontroller
AUX1UC	4	4	1	I/O	auxiliary line to and from microcontroller for synchronous applications
AUX2UC	5	–	2	I/O	auxiliary line to and from microcontroller for synchronous applications
$\overline{\text{ALARM}}$	–	5	3	O	open drain NMOS reset for microcontroller (active LOW)
ALARM	6	6	4	O	open drain PMOS reset for microcontroller (active HIGH)
CLKSEL	7	7	5	I	control signal for CLK (LOW = XTAL oscillator; HIGH = STROBE input)
CLKDIV1	8	8	6	I	control with CLKDIV2 for choosing CLK frequency
CLKDIV2	9	9	7	I	control with CLKDIV1 for choosing CLK frequency
STROBE	10	10	8	I	external clock input for synchronous applications
CLKOUT	11	11	9	O	clock output (see Table 1)
DGND1	12	12	10	supply	digital ground 1
AGND	13	13	11	supply	analog ground
S2	14	14	12	I/O	capacitance connection for voltage doubler
V_{DDA}	15	15	13	supply	analog supply voltage
S1	16	16	14	I/O	capacitance connection for voltage doubler
VUP	17	17	15	I/O	output of voltage doubler (connect to 100 nF)
I/O	18	18	16	I/O	data I/O line to and from card
AUX2	19	–	17	I/O	auxiliary I/O line to and from card
$\overline{\text{PRES}}$	20	19	18	I	active LOW card presence contact
PRES	–	20	19	I	active HIGH card presence contact
AUX1	21	21	20	I/O	auxiliary I/O line to and from card
CLK	22	22	21	O	clock to card (C3) (see Table 1)
RST	23	23	22	O	card reset (C2)
V_{CC}	24	24	23	O	supply for card (C1) (decouple with 100 nF)
$\overline{\text{CMDVCC}}$	25	25	24	I	active LOW start activation sequence from microcontroller
RSTIN	26	26	25	I	card reset from microcontroller
$\overline{\text{OFF}}$	27	27	26	O	open drain NMOS interrupt to microcontroller (active LOW)
MODE	28	28	27	I	operating mode selection (HIGH = normal; LOW = sleep)
V_{DDD}	–	–	28	supply	digital supply voltage
DGND2	–	–	29	supply	digital ground 2

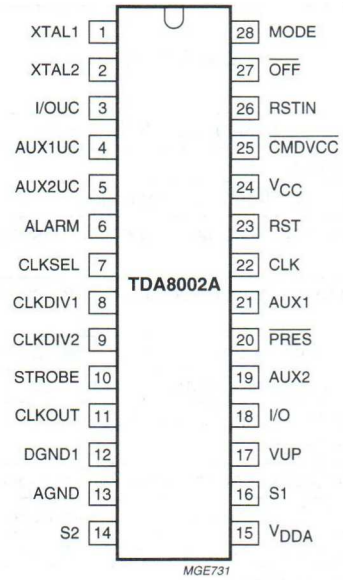


Fig.2 Pin configuration (TDA8002A; SO28).

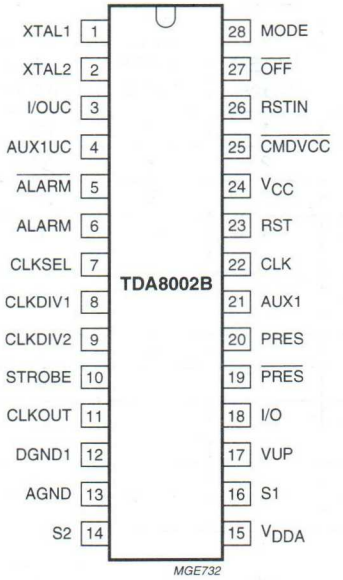


Fig.3 Pin configuration (TDA8002B; SO28).

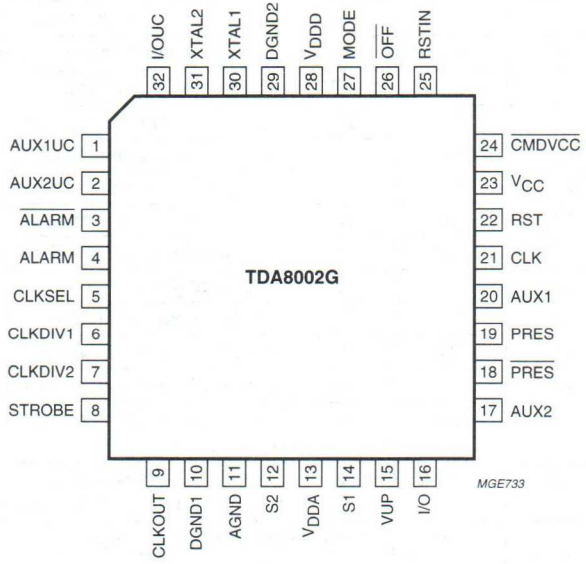


Fig.4 Pin configuration (TDA8002G; LQFP32).

Low-power smart card coupler TDA8005

FEATURES

- V_{CC} generation (5 V ±5%, 20 mA maximum with controlled rise and fall times)
- Clock generation (up to 8 MHz), with two times synchronous frequency doubling
- Clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816, GSM11.11 requirements (Global System for Mobile communication); and EMV banking specification approved for Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications (doubler or tripler DC/DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads and take-off protections
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low-power consumption
- Enhanced ESD protections on card side (6 kV minimum)
- Control and communication through a standard RS232 full duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- 80CL51 microcontroller core with 4 kbytes ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005 is a low cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11-11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low-power consumption in Power-down and sleep modes saves battery power. A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a standard 80CL51 microcontroller.

Development tools, application report and support (hardware and software) are available.

The device can be supplied either as a masked chip with standard software handling all communication between smart card and a master controller in order to make the application easier, or as a maskable device.

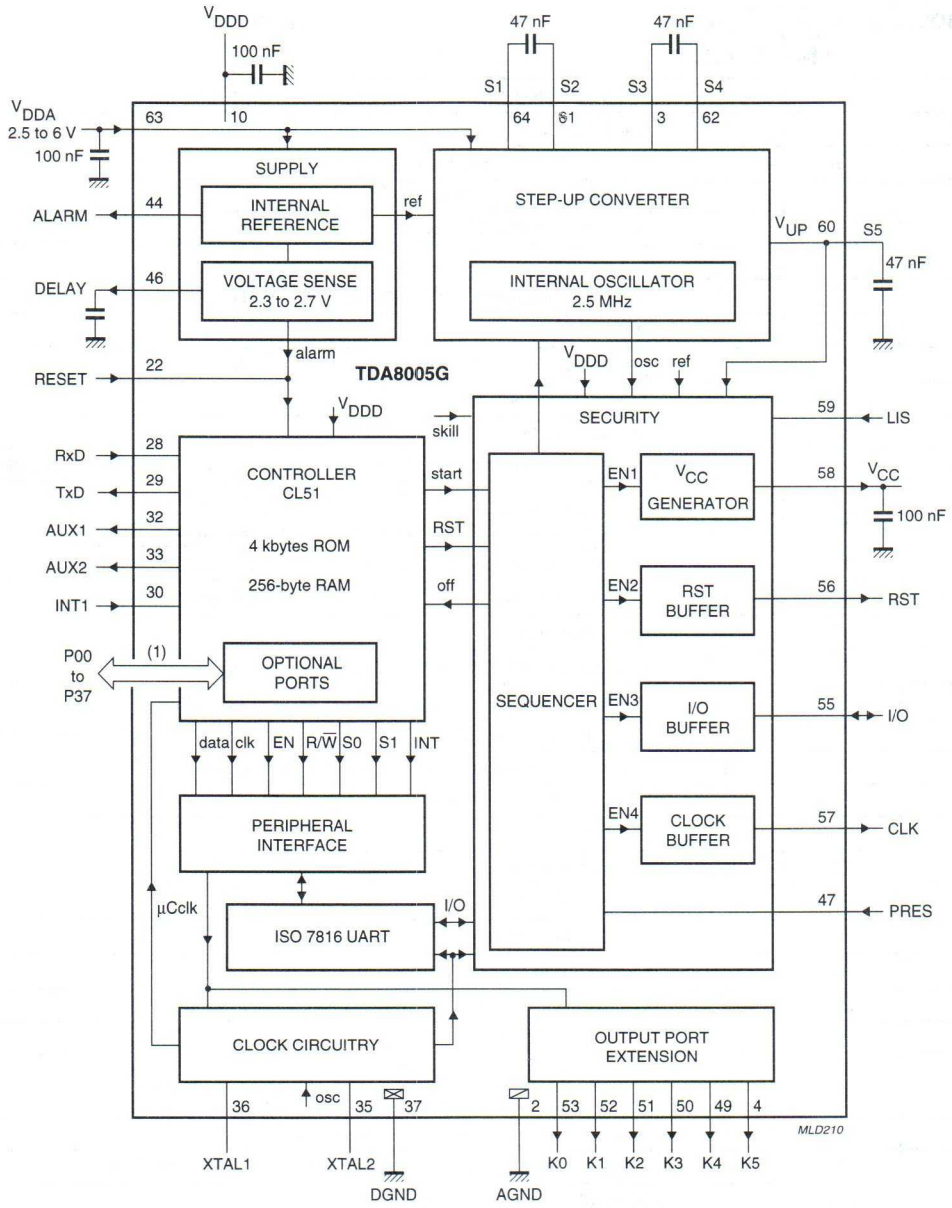
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	doubler and tripler option	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive	–	–	100	µA
$I_{DD(sm)}$	supply current in sleep mode doubler	card powered but clock stopped	–	–	500	µA
$I_{DD(sm)}$	supply current in sleep mode tripler	card powered but clock stopped	–	–	500	µA
$I_{DD(om)}$	supply current in operating mode	unloaded; f_{xtal} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	–	5.5	mA
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	30	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 150 nF (including typical 100 nF decoupling)	0.05	0.1	0.15	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	100	µs
f_{xtal}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005G	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM



(1) For details see Chapter "Pinning".

Fig.1 Block diagram (LQFP64; SOT314-2).

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to P03)
P02	6	4	general purpose I/O port (connected to P02)
P01	7	5	general purpose I/O port (connected to P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to P11)
P12	14	10	general purpose I/O port or interrupt (connected to P12)
P13	15	11	general purpose I/O port or interrupt (connected to P13)
P14	16	12	general purpose I/O port or interrupt (connected to P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to P15)
P16	19	14	general purpose I/O port or interrupt (connected to P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to P33)
T0	31	21	general purpose I/O port (connected to P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer P36)
P37	34	24	general purpose I/O port (connected to P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to P20)
P21	41	–	general purpose I/O port (connected to P21)
P22	42	29	general purpose I/O port (connected to P22)
P23	43	30	general purpose I/O port (connected to P23)
ALARM	44	–	open-drain output for Power-On Reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

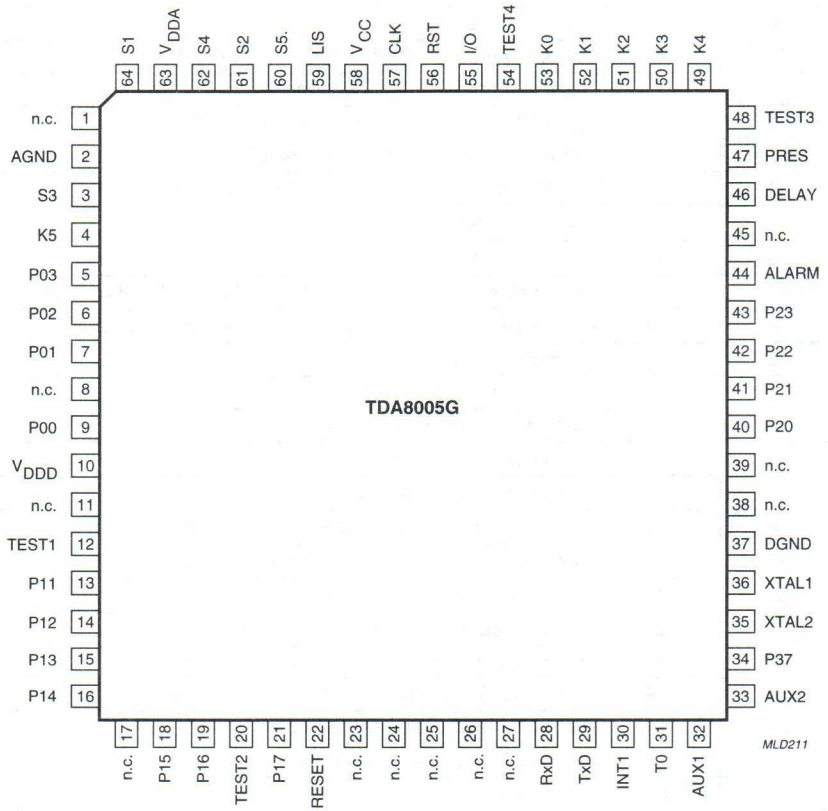


Fig.2 Pin configuration (LQFP64; SOT314-2).

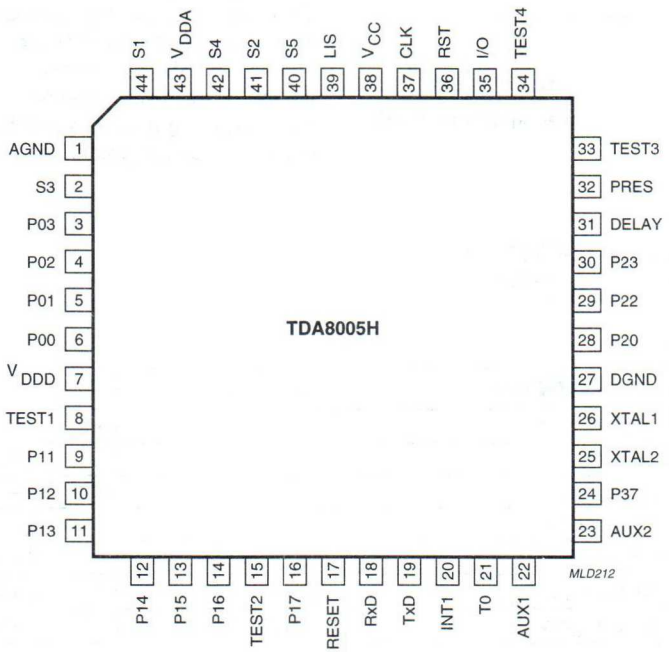


Fig.3 Pin configuration (QFP44; SOT307-2).

Low power mixers/oscillators for satellite tuners

TDA8010M; TDA8010AM

FEATURES

- Fully balanced mixer with common base input
- Wide input power and frequency range
- One-band 2 pin oscillator
- Local oscillator buffer and prescaler
- SAW filter IF preamplifier with gain control input and switchable output
- Bandgap voltage stabilizer for oscillator stability
- External IF filter between the mixer output and the IF amplifier input.

GENERAL DESCRIPTION

The TDA8010M; TDA8010AM are integrated circuits that perform the mixer/oscillator function in satellite tuners. The devices include a gain controlled IF amplifier that can directly drive two single-ended SAW filters or a differential SAW filter using a three function switchable output. They contain an internal LO prescaler and buffer that is compatible with the input of a terrestrial or satellite frequency synthesizer. They are also suitable for digital TV tuners. These devices are available in small outline packages that give the designer the capability to design an economical and physically small satellite tuner.

APPLICATIONS

- Down frequency conversion in DBS (Direct Broadcasting Satellite) satellite receivers.

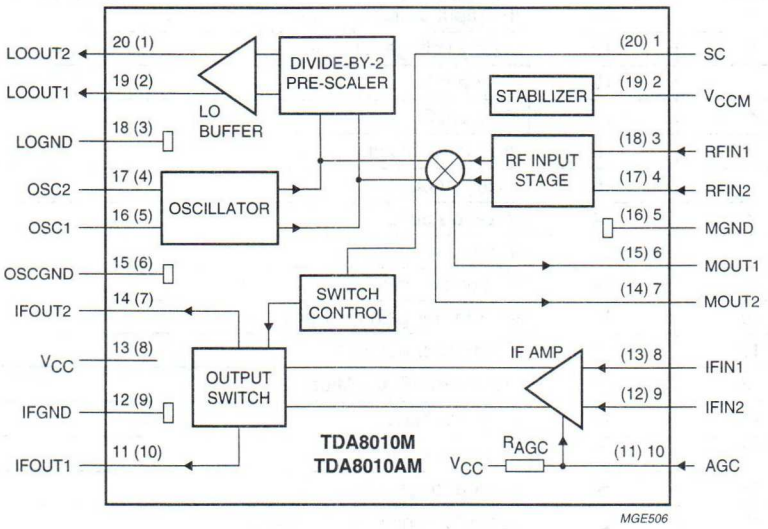
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current		–	70	–	mA
f_{RF}	RF frequency range		700	–	2150	MHz
f_{osc}	oscillator frequency		1380	–	2650	MHz
NF_M	mixer noise figure	corrected for image	–	10	–	dB
G_{max}	maximum total gain	mixer plus IF	–	40	–	dB
G_{min}	minimum total gain	mixer plus IF	–	–17	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8010M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TDA8010AM			

BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA8010AM.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	TDA8010M	TDA8010AM	
SC	1	20	IF output switch control
V_{CCM}	2	19	supply voltage for mixer
RFIN1	3	18	RF input 1
RFIN2	4	17	RF input 2
MGND	5	16	ground for mixer
MOUT1	6	15	mixer output 1
MOUT2	7	14	mixer output 2
IFIN1	8	13	IF amplifier input 1
IFIN2	9	12	IF amplifier input 2
AGC	10	11	IF amplifier gain control input
IFOUT1	11	10	IF amplifier output 1
IFGND	12	9	ground for IF amplifier
V_{CC}	13	8	supply voltage
IFOUT2	14	7	IF amplifier output 2
OSCGND	15	6	ground for oscillator
OSC1	16	5	oscillator tuning circuit input 1
OSC2	17	4	oscillator tuning circuit input 2
LOGND	18	3	ground for local oscillator buffer
LOOUT1	19	2	local oscillator output 1
LOOUT2	20	1	local oscillator output 2

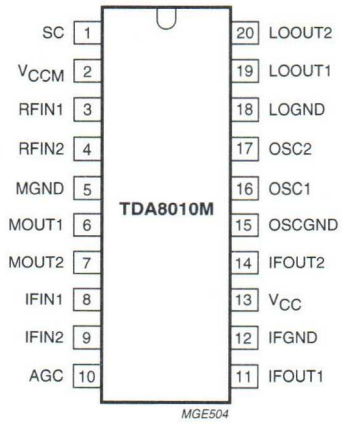


Fig.2 Pin configuration (TDA8010M).

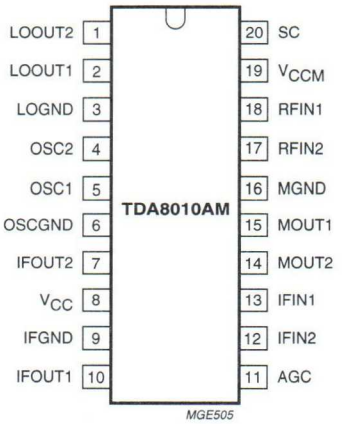


Fig.3 Pin configuration (TDA8010AM).

Low power PLL FM demodulator for satellite TV receivers

TDA8012M

FEATURES

- High input sensitivity
- Fully balanced two-pin Voltage Controlled Oscillator (VCO)
- Low input impedance (50 Ω)
- Low impedance video baseband output
- Internal voltage stabilizer
- Keyed AFC or peak-to-peak AFC
- Carrier detector
- AGC output
- Suitable for High Definition TV (HDTV).

APPLICATIONS

- Direct Broadcast Satellite (DBS) receivers.

GENERAL DESCRIPTION

The TDA8012M is a sensitive PLL FM demodulator which is used for the second IF in satellite receivers. It provides Automatic Gain Control (AGC) and Automatic Frequency Control (AFC) outputs that can be used to optimize the level and frequency of the input signal. During the searching procedure, the AFC output provides a signal which is used for carrier detection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	V_{CC} = 5 V; T_{amb} = 25 °C	50	60	70	mA
V_i	input signal voltage level		53	57	61	dBμV
$V_{o(p-p)}$	video output signal voltage amplitude (peak-to-peak value)	Δf_o = 25 MHz (p-p)	–	1	–	V
f_i	operating input frequency		–	480	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGES		
	NAME	DESCRIPTION	VERSION
TDA8012M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

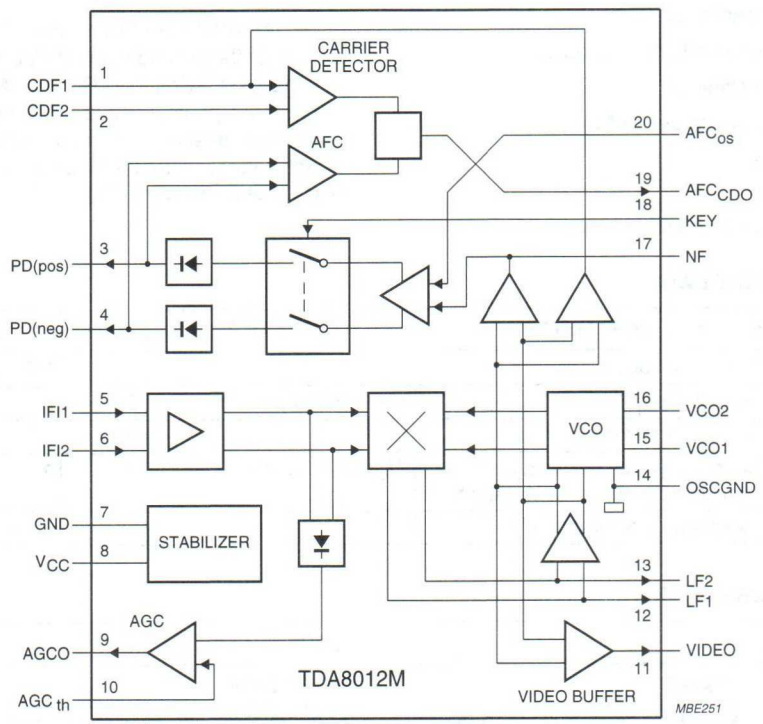


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CDF1	1	carrier detector filter 1 input
CDF2	2	carrier detector filter 2 input
PD(pos)	3	positive peak detector output
PD(neg)	4	negative peak detector output
IFI1	5	IF input 1
IFI2	6	IF input 2
GND	7	ground
V_{CC}	8	supply voltage
AGCO	9	AGC output
AGC_{th}	10	AGC threshold voltage input
VIDEO	11	baseband signal output
LF1	12	loop filter 1 input
LF2	13	loop filter 2 input
OSCGND	14	oscillator ground
VCO1	15	oscillator tank circuit 1 input
VCO2	16	oscillator tank circuit 2 input
NF	17	noise filter input
KEY	18	key pulse input
AFC_{CDO}	19	AFC and carrier detector output
AFC_{os}	20	AFC offset input

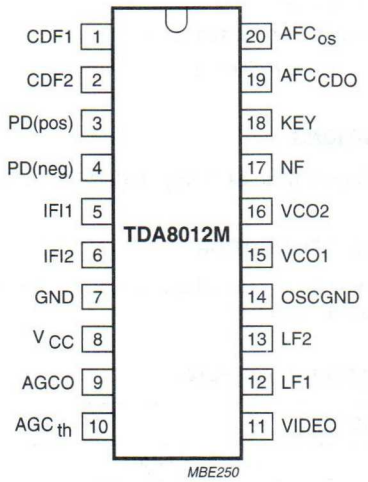


Fig.2 Pin configuration.

Quadrature demodulator TDA8040T

FEATURES

- +5 V supply voltage
- Bandgap internal reference voltage
- Low crosstalk between I (in-phase) and Q (quadrature) channel outputs
- High operating input sensitivity
- High Carrier-to-Noise Ratio (CNR) of the VCO.

APPLICATIONS

- Quadrature Phase Shift Keying (QPSK) demodulation.

GENERAL DESCRIPTION

The TDA8040T is a monolitic bipolar IC dedicated for quadrature demodulation.

It has been designed to operate in conjunction with the TDA8041H to provide a complete QPSK demodulator.

The design of this circuit has been optimized to provide the best quadrature accuracy necessary for digital receiver applications and particularly for digital television.

The TDA8040T includes two matched mixers, an RF amplifier, a symmetrical Voltage Controlled Oscillator (VCO), a frequency divider and two matched amplifiers. Two external filters are required for the baseband filtering.

The VCO requires an external LC tank circuit with two varicap diodes. This oscillator operates at twice the IF carrier frequency and can be used in a carrier recovery AFC loop.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
$I_{CC(tot)}$	total supply current	V_{CC} = 5 V	70	79	90	mA
$V_{i(RF)}$	operating input voltage level		64	67	70	dBμV
$f_{i(RF)}$	RF input signal frequency		10.7	–	150	MHz
$V_{olQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.5	–	V
$E\phi_{(IQ)}$	phase error between the I and Q channels		–	–	3	deg
$E_{G(IQ)}$	gain error between the I and Q channels		–	–	1	dB
$E_{G(tilt)}$	gain tilt error in the I and Q channels		–	–	1	dB
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels		30	–	–	dB
IM3	intermodulation distortion in the I and Q channels		40	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8040T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

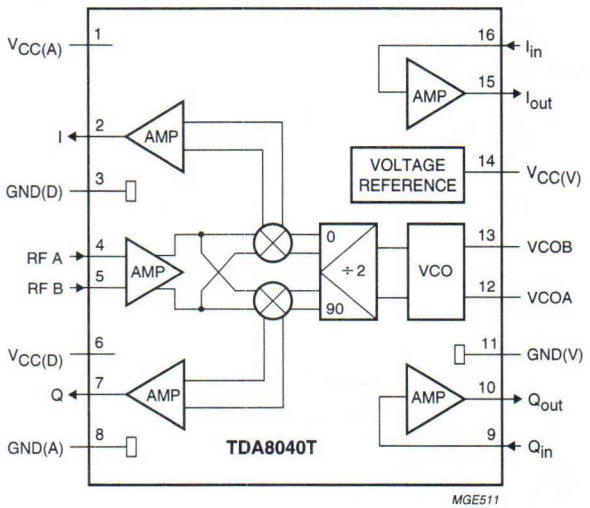


Fig.1 Block diagram.

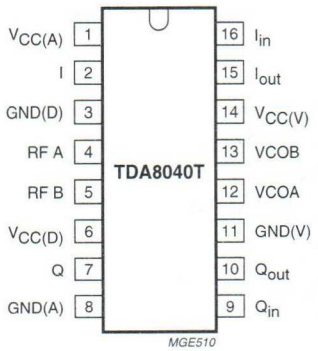


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{CC(A)}$	1	supply voltage for I and Q amplifiers
I	2	I channel buffer output
GND(D)	3	demodulator ground
RF A	4	RF input A
RF B	5	RF input B
$V_{CC(D)}$	6	supply voltage for demodulator
Q	7	Q channel buffer output
GND(A)	8	I and Q amplifiers ground
Q_{in}	9	Q channel amplifier input
Q_{out}	10	Q channel amplifier output
GND(V)	11	VCO ground
VCOA	12	VCO tank circuit A
VCOB	13	VCO tank circuit B
$V_{CC(V)}$	14	supply voltage for VCO
I_{out}	15	I channel amplifier output
I_{in}	16	I channel amplifier input

Quadrature demodulator TDA8042M

FEATURES

- 5 V supply voltage
- Internal voltage reference
- 350 to 650 MHz input frequency range
- On-chip 0° and 90° phase shifter
- Symbol rate up to 45 Msymbols/s
- High input sensitivity
- Built-in voltage stabilizer
- AGC amplifier with 21 dB control range
- AGC detector.

APPLICATION

- Binary Phase-Shift Keying (BPSK) and Quadrature Phase-Shift Keying (QPSK) demodulation.

GENERAL DESCRIPTION

The TDA8042M is a monolitic bipolar IC dedicated for BPSK and QPSK demodulation. It is designed to be used together with the TDA8043 as part of a complete BPSK/QPSK satellite demodulator and decoder.
The bandwidth of the TDA8042M allows symbol rates up to 45 Msymbols/s. It includes two matched mixers, an IF gain controlled amplifier, a symmetrical oscillator, a 0°/90° phase shifter, two low-pass filters and two matched baseband amplifiers.

The high input sensitivity makes interfacing with various sources easy. The input sensitivity can be adjusted by means of an internal AGC amplifier.

The oscillator operates at half the IF frequency. The local oscillator signal driving the mixers is made by doubling the oscillator frequency by an internal frequency multiplier. The oscillator frequency can be set by the appropriate external LC tank circuit. The internal wideband phase shifter provides two oscillator signals which are 90 degrees out of phase to drive the mixers.

An AGC detector at the I and Q outputs makes it possible to keep the I and Q signals at a constant level to drive the analog-to-digital converters of the TDA8043.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	V_{CC} = 5.0 V	54	67.5	81	mA
$V_{i(RF)}$	operating input level		–	57	–	dBμV
$f_{i(RF)}$	RF input signal frequency		350	–	650	MHz
$V_{oIQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.8	–	V
$\Delta E_{\Phi(I-Q)}$	phase matching error between I and Q channels		–	0.7	2	deg
$\Delta E_{G(I-Q)}$	gain matching error between I and Q channels		–	0.15	0.8	dB
ΔG_{tilt}	gain tilt error between I and Q channels		–	0.3	0.5	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8042M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

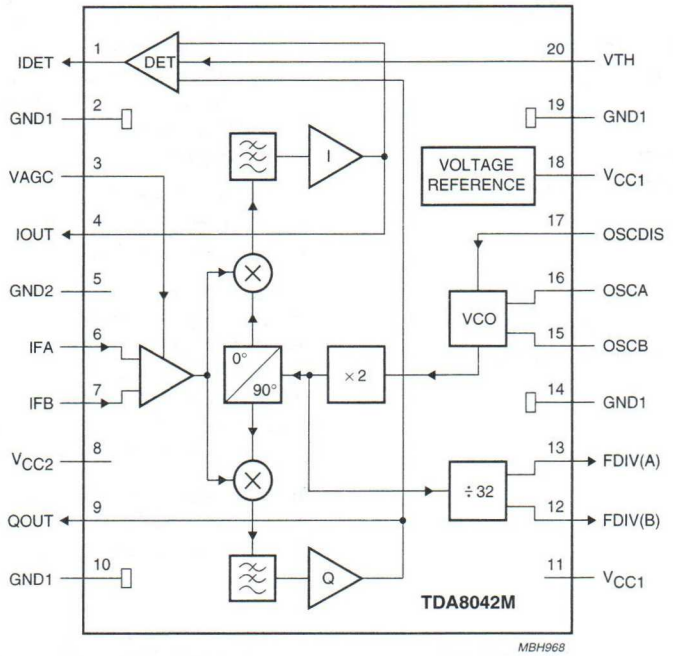


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IDET	1	AGC detector output signal
GND1	2	ground
VAGC	3	gain control input voltage
IOUT	4	I channel amplifier output
GND2	5	ground
IFA	6	IF input A
IFB	7	IF input B
V_{CC2}	8	supply voltage 2
QOUT	9	Q channel amplifier output
GND1	10	ground
V_{CC1}	11	supply voltage 1
FDIV(B)	12	prescaler output B
FDIV(A)	13	prescaler output A
GND1	14	ground
OSCB	15	oscillator tank circuit B
OSCA	16	oscillator tank circuit A
OSCDIS	17	oscillator disable input
V_{CC1}	18	supply voltage 1
GND1	19	ground
VTH	20	AGC threshold voltage input

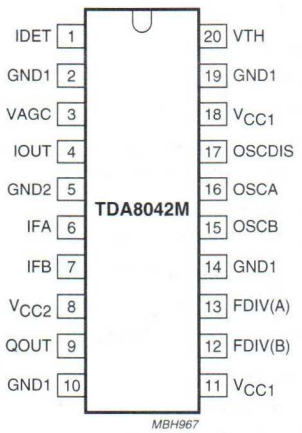


Fig.2 Pin configuration.

Satellite Demodulator and Decoder (SDD) TDA8043

FEATURES

- One chip Digital Video Broadcasting (DVB) compliant demodulator and concatenated Viterbi/Reed-Solomon decoder with de-interleaver and de-randomizer
- 3.3 V supply voltage (up to 5 V allowed)
- Internal clock divider
- On-chip crystal oscillator
- QPSK/BPSK demodulator:
  - Interpolator to handle variable symbol rates without an external anti-aliasing filter
  - On-chip Automatic Gain Control (AGC) of the analog input I and Q baseband signals or tuner AGC control
  - Two on-chip matched A/D converters (7 bits)
  - Square-Root Raised-Cosine Nyquist filter with programmable roll-off factor
  - High maximum symbol frequency: 32 Msymbols/s
  - Can be used at low channel Es/No (Symbol energy-to-noise ratio)
  - Internal carrier recovery, clock recovery and AGC loops with programmable loop filters
  - Two carrier recovery loops enabling phase tracking of the incoming symbols
  - Different modulation schemes: Quarter Phase Shift Keying (QPSK) and Bi-phase Shift Keying (BPSK)
  - Signal-to-noise ratio (S/R) estimation
  - External indication of demodulator lock
- Viterbi decoder:
  - Rate $\frac{1}{2}$ convolutional code based
  - Constraint length K = 7 with $G_1 = 171_{oct}$ and $G_2 = 133_{oct}$
  - Supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
  - 4 bit inputs for 'soft decision' for both I and Q
  - Truncation length: 144
  - Automatic synchronization
  - Channel BER (Bit Error Rate) estimation
  - External indication of Viterbi sync lock
  - Differential decoding supported



- Reed Solomon (RS) decoder:
  - (204, 188, T = 8) Reed Solomon code
  - Automatic (I^2C-bus configurable) synchronization of bytes, transport packets and frames
  - Internal convolutional de-interleaving (I = 12; using internal memory)
  - De-randomizer based on Pseudo Random Binary Sequence (PRBS)
  - External indication of RS decoder sync lock
  - External indication of uncorrectable errors (transport error indicator is set)
  - Indication of the number of lost blocks
  - Indication of the number of corrected blocks/bytes
- I^2C-bus interface:
  - I^2C-bus interface initializes and monitors the demodulator and Forward Error Correction (FEC) decoder with stand-by mode; when no I^2C-bus is used, default mode is defined
  - 4 bits I/O expander for flexible access to and from the I^2C-bus
- Package: PLCC84
- Boundary scan test.

APPLICATIONS

- Demodulation and error correction for digital satellite TV.

Satellite Demodulator and Decoder (SDD) TDA8043

GENERAL DESCRIPTION

This document specifies a DVB compliant demodulator and error correction decoder IC for reception of QPSK and BPSK modulated signals for satellite applications.
The SDD (Satellite Demodulator and Decoder) can handle variable symbol rates without adapting the analog filters within the tuner. Typical applications for this device are:

- **Single-cast**: one QPSK/BPSK modulated signal in a single channel
- **Multi-cast**: two or more QPSK/BPSK modulated signals in a single channel
- **Simul-cast**: QPSK/BPSK modulated signal together with a Frequency Modulated (FM) signal in a single channel.

The SDD requires the two I and Q analog quadrature demodulated baseband signals as an input and provides 8-bit wide MPEG2 transport packet data at the output. The output of the SDD can be directly connected to the descrambler (SAA7206) or the demultiplexer (SAA7205).

The output can also be used to monitor internal data, for example I/Q after demodulation, data after Viterbi decoding and data after de-interleaving.

The SDD requires a single clock frequency which is independent to the received symbol rate as long as the clock frequency is slightly higher than twice the highest symbol frequency. This makes it possible to use a clock signal which already exists within the complete system.

All loops to recover the data from the received symbols are internal. No external loop components are required. Loop parameters for the clock and carrier recovery can be controlled by I²C-bus.

The SDD can be controlled and monitored by I²C-bus. An I²C-bus default mode is specified which makes it possible to use the device with a minimum of software control. A 4-bit bidirectional I/O expander and an interrupt line is available. By sending an interrupt signal, the SDD can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS[1]	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	V_{DD} = 3.3 V; note 2	–	480	–	mA
f_{clk}	clock frequency		–	–	65	MHz
r_s	symbol rate		3	–	32	Msymbols/s
IL	implementation loss	note 2	–	0.3	–	dB
α	Nyquist roll-off (programmable)		–	35 or 50	50	%
P_{tot}	total power dissipation	T_{amb} = 70°C; note 2	–	1.5	tbf	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–	–	70	°C
T_j	operating junction temperature	T_{amb} = 70°C	–	–	125	°C
S/N	signal-to-noise ratio for locking the SDD (QPSK)		tbf	–	–	dB

Notes

1. This implementation was measured in a laboratory environment.
2. These values are specified for a symbol rate of 27.5 MSymbols/s.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8043K	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD1}	1	–	digital supply voltage 1
V_{SSD1}	2	–	digital ground 1
V_{AGC}	3	O	AGC output voltage
V_{DDD2}	4	–	digital supply voltage 2
V_{DDD3}	5	–	digital supply voltage 3
OUTSD	6	O	general purpose Sigma-Delta output
I0	7	I	digital bypass I-input ADC (bit 0)
I1	8	I	digital bypass I-input ADC (bit 1)
I2	9	I	digital bypass I-input ADC (bit 2)
I3	10	I	digital bypass I-input ADC (bit 3)
V_{SSD2}	11	–	digital ground 2
I4	12	I	digital bypass I-input ADC (bit 4)
I5	13	I	digital bypass I-input ADC (bit 5)
I6	14	I	digital bypass I-input ADC (bit 6)
Q0	15	I	digital bypass Q-input ADC (bit 0)
V_{DDD4}	16	–	digital supply voltage 4
Q1	17	I	digital bypass Q-input ADC (bit 1)
Q2	18	I	digital bypass Q-input ADC (bit 2)
Q3	19	I	digital bypass Q-input ADC (bit 3)
Q4	20	I	digital bypass Q-input ADC (bit 4)
V_{SSD3}	21	–	digital ground 3
Q5	22	I	digital bypass Q-input ADC (bit 5)
Q6	23	I	digital bypass Q-input ADC (bit 6)
V_{SSD4}	24	–	digital ground 4
V_{DDD5}	25	–	digital supply voltage 5
V_{DDD6}	26	–	digital supply voltage 6
PRESET	27	I	set device into default mode
P3	28	I/O	quasi-bidirectional I/O port (bit 3)
P2	29	I/O	quasi-bidirectional I/O port (bit 2)
P1	30	I/O	quasi-bidirectional I/O port (bit 1)
P0	31	I/O	quasi-bidirectional I/O port (bit 0)
V_{DDD7}	32	–	digital supply voltage 7
PKTBCLK	33	O	output clock for transport stream bytes (to SAA7205H)
PKTDAT0	34	O	parallel data output to SAA7205H (bit 0)
PKTDAT1	35	O	parallel data output SAA7205H (bit 1)
PKTDAT2	36	O	parallel data output SAA7205H (bit 2)
V_{SSD5}	37	–	digital ground 5
PKTDAT3	38	O	parallel data output SAA7205H (bit 3)
PKTDAT4	39	O	parallel data output SAA7205H (bit 4)
PKTDAT5	40	O	parallel data output SAA7205H (bit 5)

SYMBOL	PIN	I/O	DESCRIPTION
PKTDAT6	41	O	parallel data output SAA7205H (bit 6)
V_{DDD8}	42	–	digital supply voltage 8
V_{SSD6}	43	–	digital ground 6
V_{DDD9}	44	–	digital supply voltage 9
V_{DDD10}	45	–	digital supply voltage 10
PKTDAT7	46	O	parallel data output SAA7205H (bit 7)
PKTBAD	47	O	transport error indicator SAA7205H
PKTDATV	48	O	data valid indicator SAA7205H
PKTSYNC	49	O	transport packet synchronisation signal SAA7205H
V_{SSD7}	50	–	digital ground 7
SCL	51	I	serial clock of I^2C-bus
SDA	52	I/O	serial data of I^2C-bus
$\overline{INT}$	53	O	interrupt output (active LOW)
A0	54	I	I^2C hardware address
RSLOCK	55	O	Reed-Solomom lock indicator
VLOCK	56	O	Viterbi lock indicator
DLOCK	57	O	demodulator lock indicator
V_{DDD11}	58	–	digital supply voltage 11
TEST	59	I	test pin (normally connected to ground)
TRST	60	I	optional asynchronous resettlement (normally connected to ground)
TCK	61	I	dedicated test clock (normally connected to ground)
V_{DDD12}	62	–	digital supply voltage 12
V_{DDD13}	63	–	digital supply voltage 13
V_{SSD8}	64	–	digital ground 8
V_{SSD9}	65	–	digital ground 9
TMS	66	I	input control signal (normally connected to ground)
TDO	67	O	serial test data out
TDI	68	I	serial test data in (normally connected to ground)
V_{DDD14}	69	–	digital supply voltage 14
V_{SSD10}	70	–	digital ground 10
$V_{SSD(AD)}$	71	–	digital ground A/D converter
$V_{DDD(AD)}$	72	–	digital supply A/D converter
$V_{ref(N)}$	73	I	negative reference voltage for ADC
V_{SSA1}	74	–	analog ground 1
QA	75	I	analog input Q
$V_{ref(M)}$	76	I	mid-range reference voltage for ADC
IA	77	I	analog input I
V_{SSA2}	78	–	analog ground 2
I_{BIAS}	79	I	external reference current for ADC
V_{DDA}	80	–	analog supply voltage
V_{DDCL}	81	–	supply voltage for crystal oscillator

SYMBOL	PIN	I/O	DESCRIPTION
XTALI	82	I	clock oscillator input
XTALO	83	O	clock oscillator output
V_{DDXTAL}	84	–	supply voltage for crystal oscillator

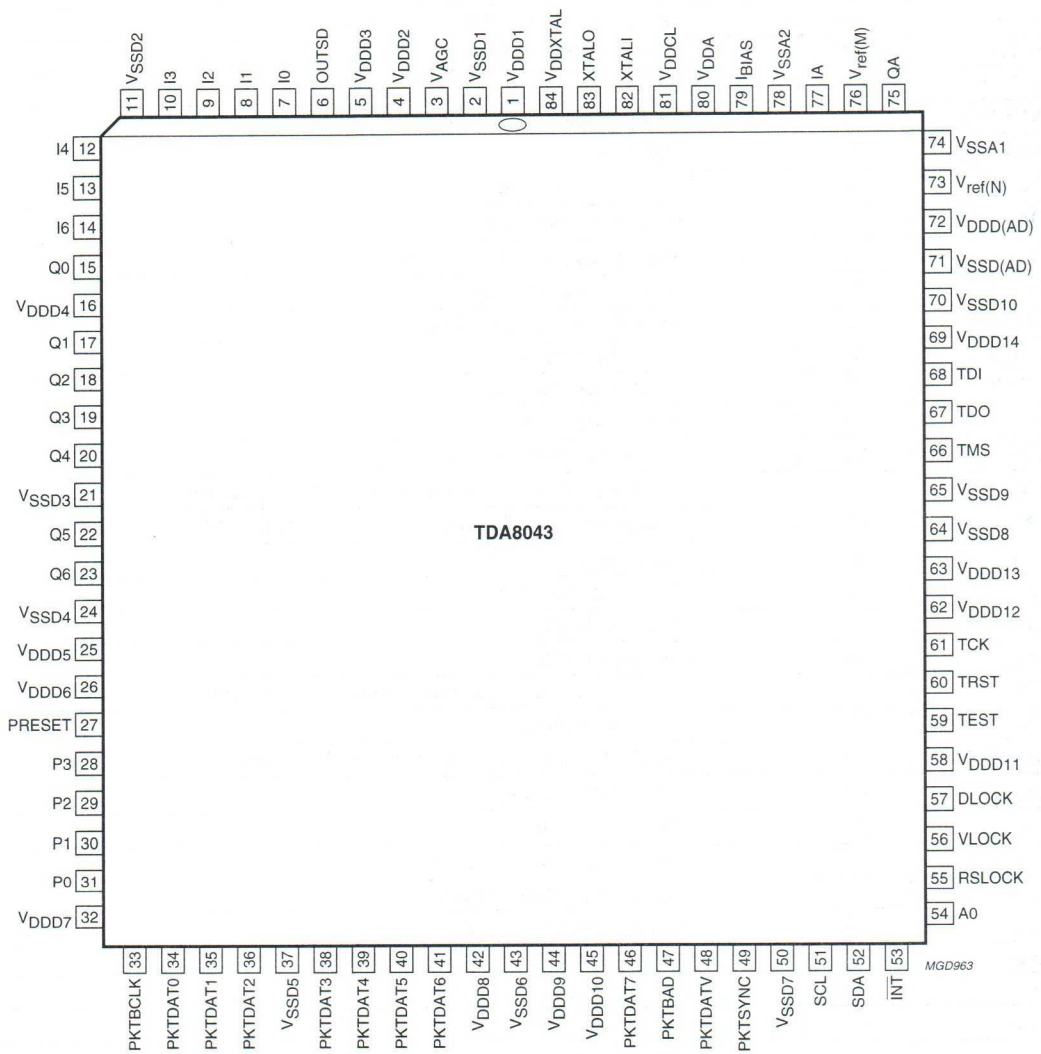
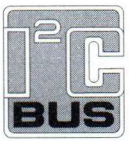


Fig.1 Pin configuration.

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Multi-mode QAM demodulator TDA8046

1 FEATURES

- Different modulation schemes: 4, 16, 32, 64 and 256-QAM
- Digital demodulator and square root raised cosine Nyquist filter with roll-off of 15% or 20%
- High performance adaptive equalizer (no training sequence needed)
- Digital detectors for generation of required control voltages for carrier recovery, clock recovery and AGC
- Digital-to-analog converters and operational amplifiers allowing high flexibility for selection of the (PLL) loop time constants
- High maximum symbol rate (r_s) of 7 Msymbols/s
- Input format: Straight binary or 2's complement (up to 9 bits, TTL compatible)
- Output format: 8-bit wide bus (CMOS compatible)
- I^2C-bus interface to initialize and monitor the demodulator. When no I^2C-bus usage; 64-QAM, 20% roll-off factor in default mode
- 5 V peripheral and analog supply voltage
- 3.3 V core supply voltage
- Boundary scan test.

2 APPLICATION

Demodulation for digital cable TV and cable modem.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(core)}$	core supply voltage		3.00	3.30	3.60	V
V_{DDD}	digital peripheral supply voltage		4.75	5.00	5.25	V
V_{DDA}	analog supply voltage		4.75	5.00	5.25	V
$I_{DDD(core)}$	core supply current	$V_{DDD(core)}$ = 3.3 V; note 1	–	100	–	mA
I_{DDD}	digital peripheral supply current	V_{DDD} = 5 V; note 1	–	14	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; note 1	–	16	–	mA
r_s	symbol rate		–	–	7	Msym/s
IL	implementation loss	note 2	–	0.7	–	dB
α	Nyquist roll-off (programmable)		–	15 or 20	–	%
SNR_{lock}	signal-to-noise ratio for locking a 64-QAM constellation		21	–	–	dB
	signal-to-noise ratio for locking a 256-QAM constellation		27	–	–	dB

Notes

1. The supply currents are specified for the maximum symbol frequency.
2. The implementation loss (IL) of the demodulator is defined as the distance between the measured and theoretical BER curve as function of signal-to-noise ratio at a BER = 10^{-6} for a back-to-back measurement at the IF frequency. This performance depends on the chosen loop parameters (see *Application notes*).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8046H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

5 BLOCK DIAGRAM

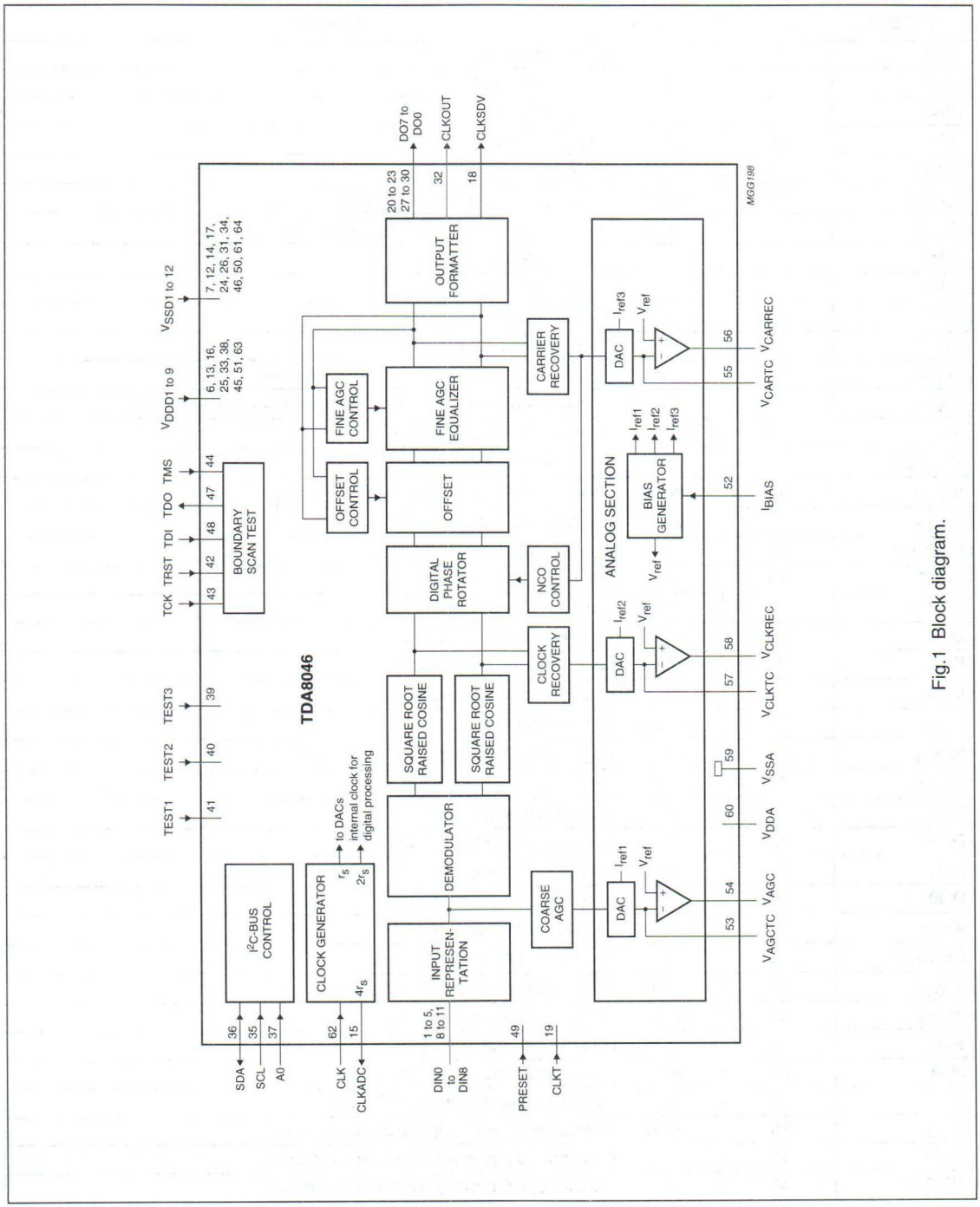


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DIN0	1	I	digital input bit 0 (LSB)
DIN1	2	I	digital input bit 1
DIN2	3	I	digital input bit 2
DIN3	4	I	digital input bit 3
DIN4	5	I	digital input bit 4
V_{DDD1}	6	supply	digital peripheral supply voltage 1 (+5 V)
V_{SSD1}	7	supply	digital ground 1; for input peripheral and core
DIN5	8	I	digital input bit 5
DIN6	9	I	digital input bit 6
DIN7	10	I	digital input bit 7
DIN8	11	I	digital input bit 8 (MSB)
V_{SSD2}	12	supply	digital ground 2; for core and clock buffers
V_{DDD2}	13	supply	digital supply voltage 2; for core and clock buffers (+3.3 V)
V_{SSD3}	14	supply	digital peripheral ground 3
CLKADC	15	O	clock output to ADC ($4 \times r_s$)
V_{DDD3}	16	supply	digital peripheral supply voltage 3 (+5 V)
V_{SSD4}	17	supply	digital ground 4; for core
CLKSDV	18	O	clock symbol data valid output
CLKT	19	I	for test purpose only
DO7	20	O	parallel data output (bit 7)
DO6	21	O	parallel data output (bit 6)
DO5	22	O	parallel data output (bit 5)
DO4	23	O	parallel data output (bit 4)
V_{SSD5}	24	supply	digital peripheral ground 5
V_{DDD4}	25	supply	digital peripheral supply voltage 4 (+5 V)
V_{SSD6}	26	supply	digital ground 6; for core
DO3	27	O	parallel data output (bit 3)
DO2	28	O	parallel data output (bit 2)
DO1	29	O	parallel data output (bit 1)
DO0	30	O	parallel data output (bit 0)
V_{SSD7}	31	supply	digital peripheral ground 7
CLKOUT	32	I	output formatter clock output
V_{DDD5}	33	supply	digital peripheral supply voltage 5 (+5 V)
V_{SSD8}	34	supply	digital peripheral ground 8
SCL	35	I	serial clock input (I^2C-bus)
SDA	36	I/O	serial data input/output (I^2C-bus)
A0	37	I	hardware address input (I^2C-bus)
V_{DDD6}	38	supply	digital peripheral supply voltage 6 (+5 V)
TEST3	39	I	test input 3 (normally connected to ground)
TEST2	40	I	test input 2 (normally connected to ground)

SYMBOL	PIN	I/O	DESCRIPTION
TEST1	41	I	test input 1 input (normally connected to ground)
TRST	42	I	optional asynchronous reset input
TCK	43	I	dedicated test clock input
TMS	44	I	input control signal
V_{DDD7}	45	supply	digital supply voltage 7; for core (+3.3 V)
V_{SSD9}	46	supply	digital ground 9; for core
TDO	47	O	serial test data output
TDI	48	I	serial test data input
PRESET	49	I	set device into default mode input
V_{SSD10}	50	supply	digital ground 10; for the digital section of the analog block
V_{DDD8}	51	supply	digital supply voltage 8; for the digital section of the analog block (+5 V)
I_{BIAS}	52	I	input bias current for DACs
V_{AGCTC}	53	O	inverted operational amplifier input voltage for loop filtering
V_{AGC}	54	O	analog output voltage for AGC
V_{CARTC}	55	O	inverted operational amplifier input voltage for carrier recovery loop filtering
V_{CARREC}	56	O	analog output voltage for carrier recovery
V_{CLKTC}	57	O	inverted operational amplifier input voltage for clock recovery loop filtering
V_{CLKREC}	58	O	analog output voltage for clock recovery
V_{SSA}	59	supply	analog ground
V_{DDA}	60	supply	analog supply voltage (+5 V)
V_{SSD11}	61	supply	digital ground 11; for clock
CLK	62	I	clock input ($4 \times r_s$)
V_{DDD9}	63	supply	digital supply voltage 9; for clock
V_{SSD12}	64	supply	digital peripheral ground 12

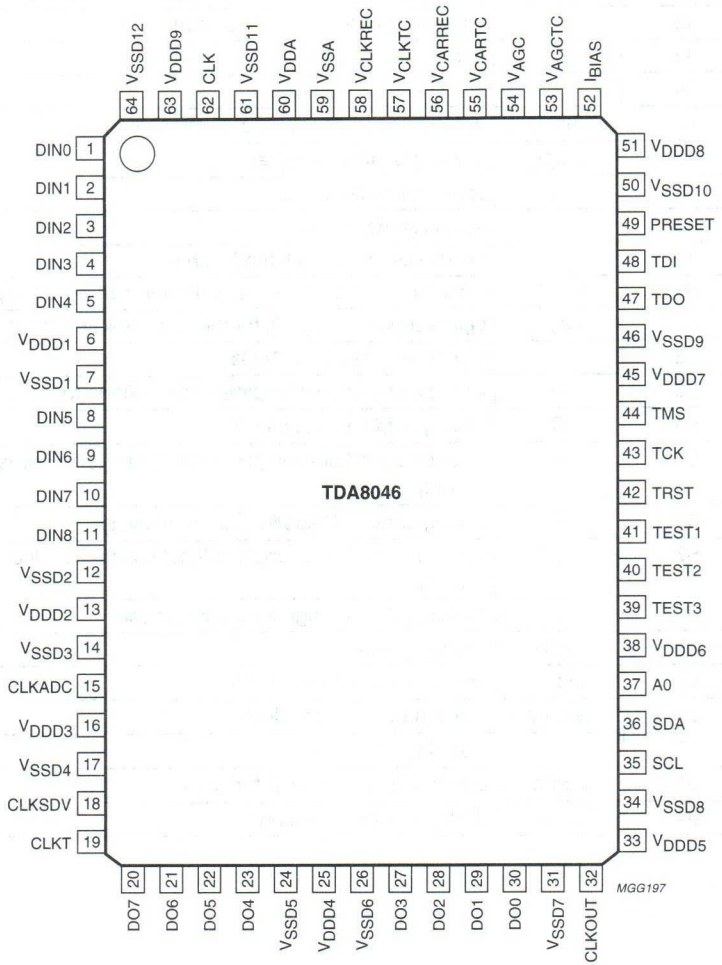


Fig.2 Pin configuration.

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins
  - short-circuit of the output pins to V_P
- High EMC immunity due to common mode inputs
- Temperature (thermal) protection
- East-West output stage with one single conversion resistor.

GENERAL DESCRIPTION

The TDA8350Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system and an East-West driver for sinking the diode modulator current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_P	quiescent current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
East-West amplifier						
$I_{O(sink)}$	output current (sink only)		–	–	500	mA
$V_{O(sink)}$	peak output voltage	$I_{O(sink)}$ = 10 μA	–	–	40	V
I_{bias}	input bias current		–	–	1	μA
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–65	–	150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8350Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

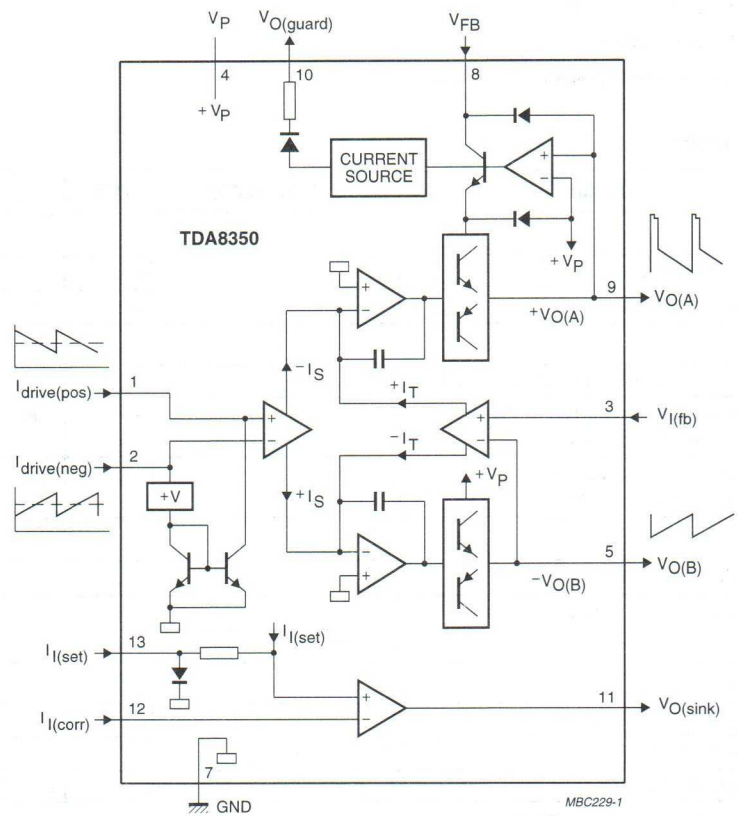


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
$V_{I(fb)}$	3	feedback voltage input
V_P	4	supply voltage
$V_{O(B)}$	5	output voltage B
n.c.	6	not connected
GND	7	ground
V_{FB}	8	flyback supply voltage
$V_{O(A)}$	9	output voltage A
$V_{O(guard)}$	10	guard output voltage
$V_{O(sink)}$	11	East-West amplifier driver (sink) output voltage
$I_{I(corr)}$	12	East-West amplifier input correction current (negative)
$I_{I(set)}$	13	East-West amplifier set input current (positive)

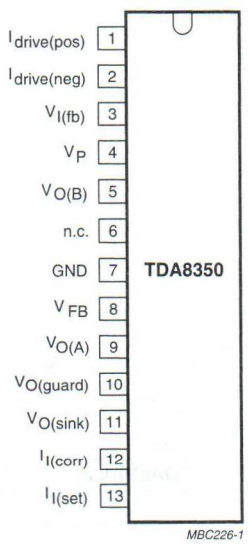


Fig.2 Pin configuration.

I²C-bus controlled economy PAL/NTSC and NTSC TV-processors

TDA837x family

FEATURES

Available in all ICs:

- Vision IF amplifier with high sensitivity and good figures for differential phase and gain
- PLL demodulator for the IF signal
- Alignment-free sound demodulator
- Flexible source selection with a CVBS input for the internal signal and Y/C or CVBS input for the external signal
- Audio switch
- The output signal of the CVBS (Y/C) switch is externally available
- Integrated chrominance trap and band-pass filters (auto-calibrated)
- Luminance delay line integrated
- A symmetrical peaking circuit in the luminance channel
- Black stretching of non-standard CVBS or luminance signals
- RGB control circuit with black current stabilization and white point adjustment
- Linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Slow start and slow stop of the horizontal drive pulses
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- I²C-bus control of various functions
- Low dissipation
- Small amount of peripheral components compared with competition ICs.

GENERAL DESCRIPTION

The various versions of the TDA837x series are I²C-bus controlled single-chip TV processors which are intended to be applied in PAL/NTSC (TDA8374 and TDA8375) and NTSC (TDA8373 and TDA8377) television receivers. All ICs are available in an SDIP56 package and some versions are also available in a QFP64 package. The ICs are pin compatible so that with one application board NTSC and PAL/NTSC (or multistandard together with the SECAM decoder TDA8395) receivers can be built.

Functionally this IC series is split in to 2 categories:

- Versions intended to be used in economy TV receivers with all basic functions
- Versions with additional functions such as E-W geometry control, horizontal and vertical zoom function and YUV interface which are intended for TV receivers with 110° picture tubes.

The various type numbers are given in Table 1.

The detailed differences between the various ICs are given in Table 2.

Table 1 TV receiver versions

TV RECEIVERS	SDIP56 PACKAGE		QFP64 PACKAGE	
	ECONOMY	MID/HIGH END	ECONOMY	MID/HIGH END
PAL only	TDA8374B	–	TDA8374BH	–
PAL/NTSC (SECAM)	TDA8374 and TDA8374A	TDA8375 and TDA8375A	TDA8374AH	TDA8375AH
NTSC	TDA8373	TDA8377 and TDA8377A	–	–

Table 2 Differences between the various ICs

CIRCUITS	IC VERSION (TDA)							
	8373	8374	8374A(H)	8374B(H)	8375	8375A(H)	8377	8377A
Multistandard IF	–	X	–	–	X	X	–	–
Automatic Volume Levelling (AVL)	X	X	–	–	–	–	–	–
PAL decoder	–	X	X	X	X	X	–	–
SECAM interface	–	X	X	X	X	X	–	–
NTSC decoder	X	X	X	X	X	X	X	X
Colour matrix PAL/NTSC (Japan)	–	X	X	X	X	X	–	–
Colour matrix NTSC (USA/Japan)	X	–	–	–	–	–	X	X
YUV interface	–	–	–	–	X	X	X	X
Horizontal geometry	–	–	–	–	X	X	X	X
Horizontal and vertical zoom	–	–	–	–	X	X	X	X

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage		–	8.0	–	V
I_P	supply current		–	110	–	mA
Input voltages						
$V_{48,49(rms)}$	video IF amplifiers sensitivity (RMS value)		–	70	–	μV
$V_{1(rms)}$	sound IF amplifiers sensitivity (RMS value)		–	1.0	–	mV
$V_{2(rms)}$	external audio input voltage (RMS value)		–	500	–	mV
$V_{11(p-p)}$	external CVBS/Y input voltage (peak-to-peak value)		–	1.0	–	V
$V_{10(p-p)}$	external chrominance input voltage (burst amplitude) (peak-to-peak value)		–	0.3	–	V
$V_{23-25(p-p)}$	RGB input voltage (peak-to-peak value)		–	0.7	–	V
Output signals						
$V_{6(p-p)}$	IF video output voltage (peak-to-peak value)		–	2.5	–	V
I_{54}	tuner AGC output current range		0	–	5	mA
V_{oVSW}	output signal level of video switch (peak-to-peak value)		–	1.0	–	V
$V_{30(p-p)}$	–(R – Y) output voltage (peak-to-peak value)		–	525	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{29(p-p)}$	–(B – Y) output voltage (peak-to-peak value)		–	675	–	mV
$V_{28(p-p)}$	luminance output voltage (peak-to-peak value)		–	1.4	–	V
$V_{19-21(p-p)}$	RGB output signal amplitudes (peak-to-peak value)		–	2.0	–	V
I_{40}	horizontal output current		–	10	–	mA
$I_{46,47(p-p)}$	vertical output current (peak-to-peak value)		–	1	–	mA
$I_{45(peak)}$	E-W output current (peak value)	TDA8375A, TDA8377A, TDA8375 and TDA8377	–	1.2	–	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA837xA	SDIP56	plastic shrink dual in-line package; 56 leads (600 mil)	SOT400-1
TDA837xH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

BLOCK DIAGRAM

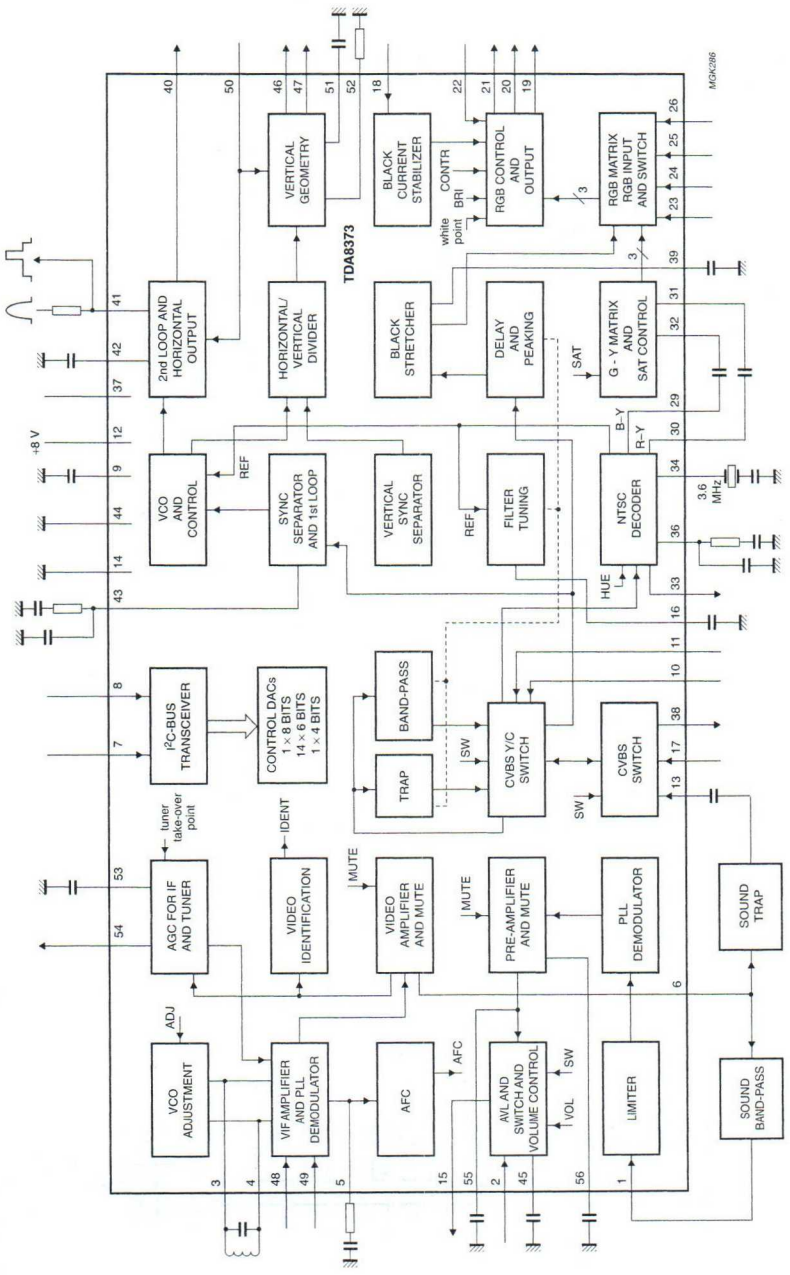


Fig.1 Block diagram of bus-controlled economy NTSC TV-processor TDA8373.

The TDA8373 is only supplied in an SDIP package.

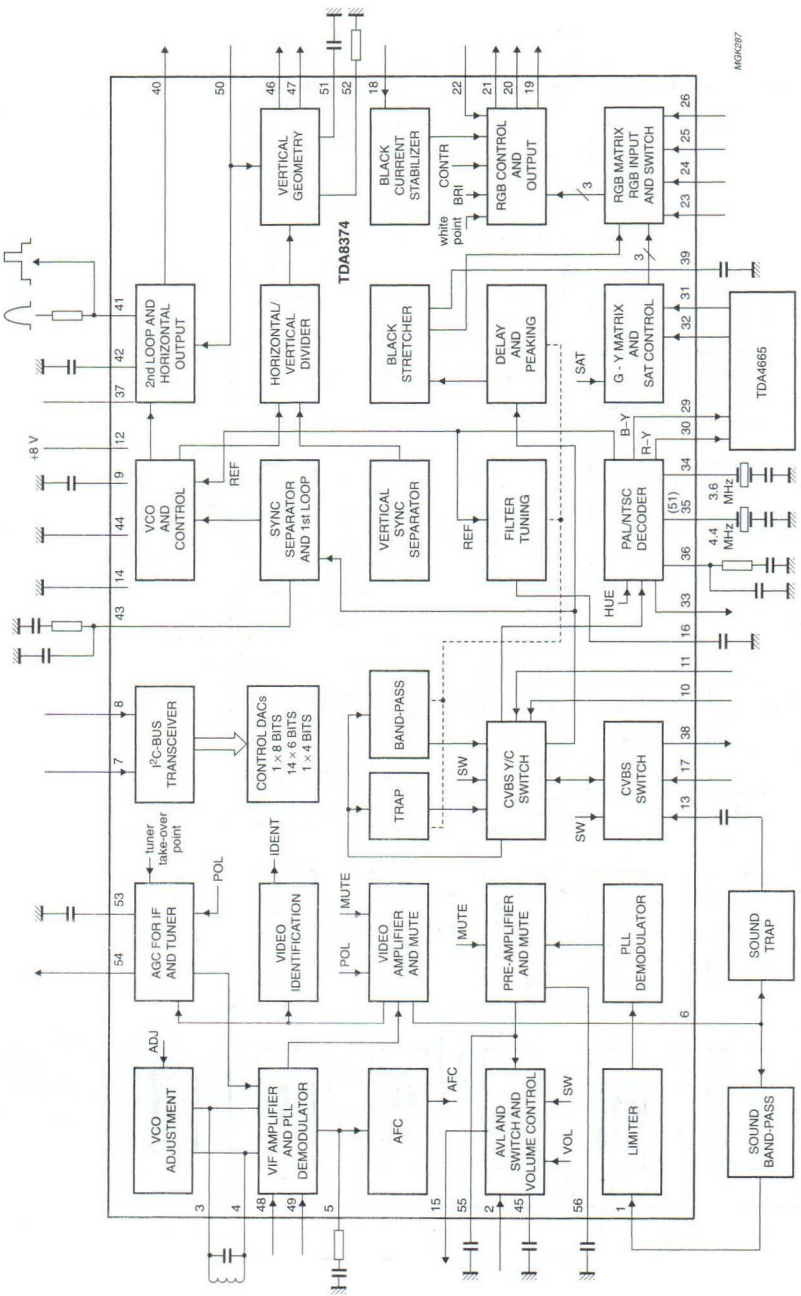


Fig.2 Block diagram of bus-controlled economy PAL/NTSC TV processor TDA8374.

For most pins the QFP64 pinning is not indicated.

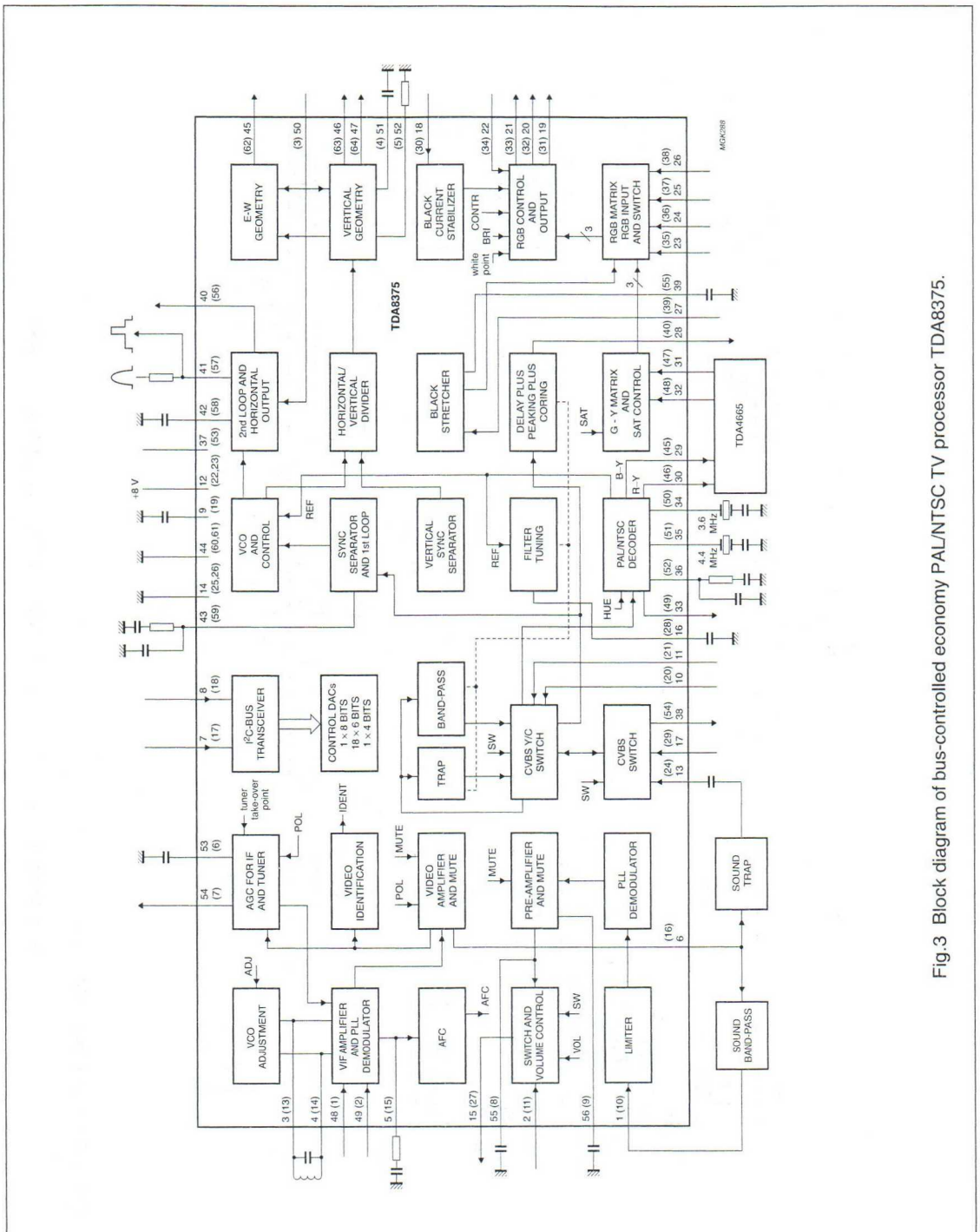


Fig.3 Block diagram of bus-controlled economy PAL/NTSC TV processor TDA8375.

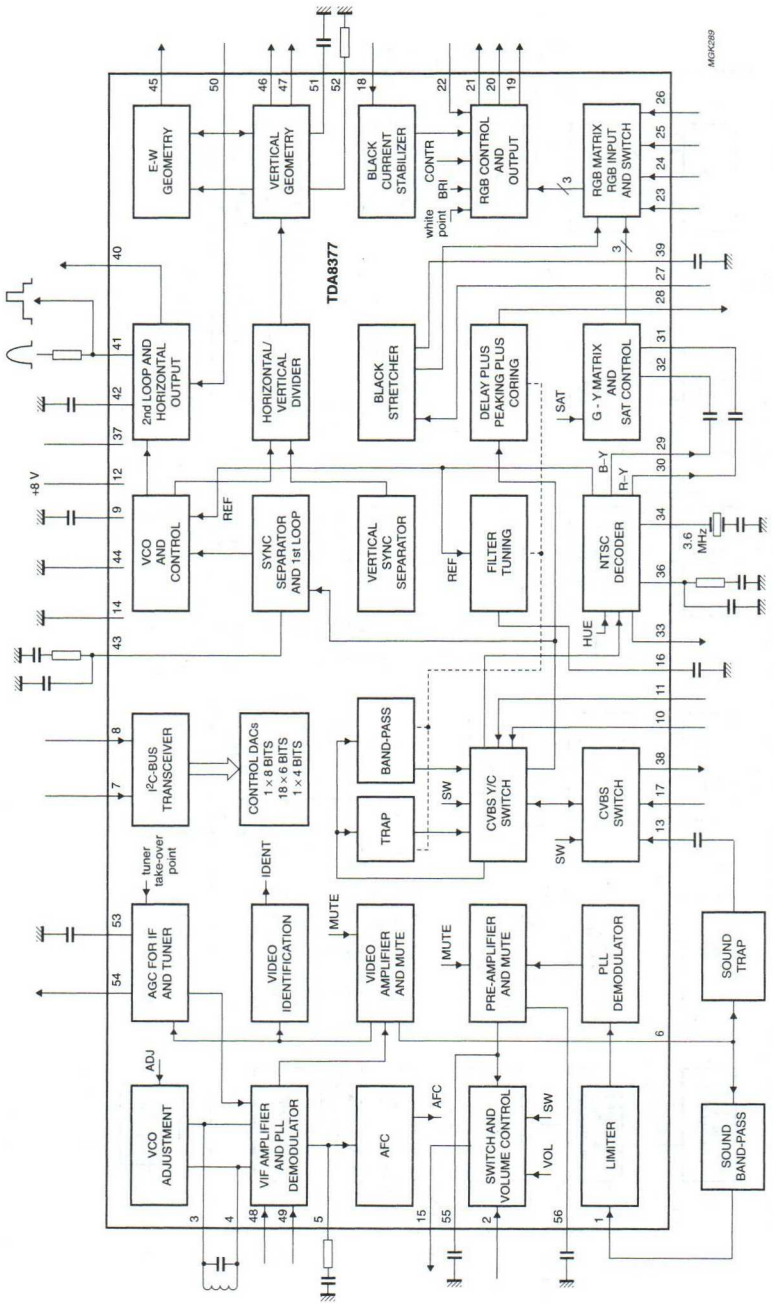


Fig.4 Block diagram of bus-controlled economy NTSC TV processor TDA8377.

The TDA8377 is only supplied in an SDIP package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP56	QFP64	
SIF	1	10	sound IF input
AUDI	2	11	external audio input
VCO1	3	13	IF VCO 1 tuned circuit
VCO2	4	14	IF VCO 2 tuned circuit
PLL	5	15	PLL loop filter
IFVO	6	16	IF video output
SCL	7	17	serial clock input (I²C-bus)
SDA	8	18	serial data input/output (I²C-bus)
DEC_{BG}	9	19	band gap decoupling
CHROMA	10	20	chrominance input
CVBS/Y	11	21	CVBS/Y input
V_{P1}	12	22 and 23	main supply voltage (+8 V)
$CVBS_{int}$	13	24	internal CVBS input
GND1	14	25 and 26	ground
AUDO	15	27	audio output
DEC_{FT}	16	28	decoupling filter tuning
$CVBS_{ext}$	17	29	external CVBS input
BLKIN	18	30	black current input
BO	19	31	blue output
GO	20	32	green output
RO	21	33	red output
BCLIN	22	34	beam current input
RI	23	35	red input
GI	24	36	green input
BI	25	37	blue input
RGBIN	26	38	RGB insertion input
YIN	27[2]	39	luminance input
YOUT	28	40	luminance output
BYO	29	45	(B – Y) output
RYO	30	46	(R – Y) output
RYI	31	47	(R – Y) input
BYI	32	48	(B – Y) input
SEC_{ref}	33[1]	49	SECAM reference output
XTAL1	34	50	3.58 MHz crystal connection
XTAL2	35[1]	51	4.43 MHz crystal connection
LFBP	36	52	loop filter burst phase detector
V_{P2}	37	53	horizontal oscillator supply voltage (+8 V)
CVBSO	38	54	CVBS output

SYMBOL	PIN		DESCRIPTION
	SDIP56	QFP64	
BLPH	39	55	black peak hold capacitor
HOUT	40	56	horizontal drive output
FBI/SCO	41	57	flyback input and sandcastle output
PH2	42	58	phase 2 filter/protection
PH1	43	59	phase 1 filter
GND2	44	60 and 61	ground 2
EWD	45[2]	62	east-west drive output
VDOB	46	63	vertical drive output B
VDOA	47	64	vertical drive output A
IFIN1	48	1	IF input 1
IFIN2	49	2	IF input 2
EHT/PRO	50	3	EHT/overvoltage protection input
VSAW	51	4	vertical sawtooth capacitor
I_{ref}	52	5	reference current input
DEC_{AGC}	53	6	AGC decoupling capacitor
AGCOUT	54	7	tuner AGC output
AUDEEM	55	8	audio deemphasis
DEC	56	9	decoupling sound demodulator
i.c.	–	12	internally connected
i.c.	–	41	internally connected
i.c.	–	42	internally connected
i.c.	–	43	internally connected
i.c.	–	44	internally connected

Notes

1. In the TDA8373 and TDA8377 pin 35 (4.43 MHz crystal) is internally connected and pin 33 is just a subcarrier output which can be used as a reference signal for comb filter ICs.
2. In the TDA8373 and TDA8374 the following pins are different (SDIP56): Pin 27: not connected; Pin 45: AVL capacitor.

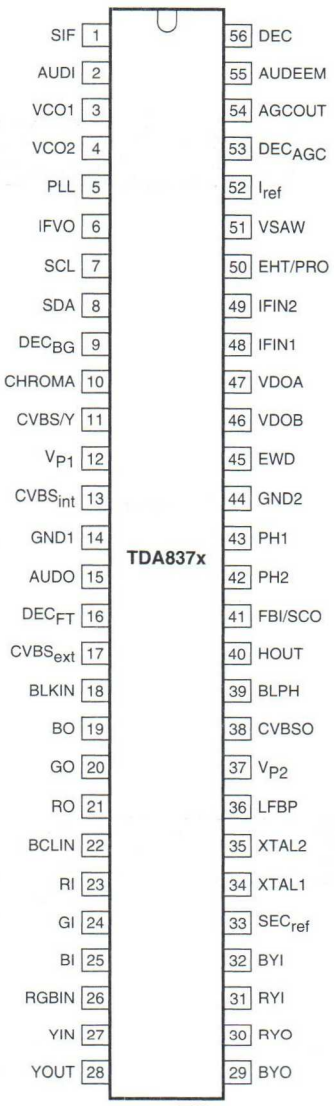


Fig.5 Pin configuration (SDIP56).

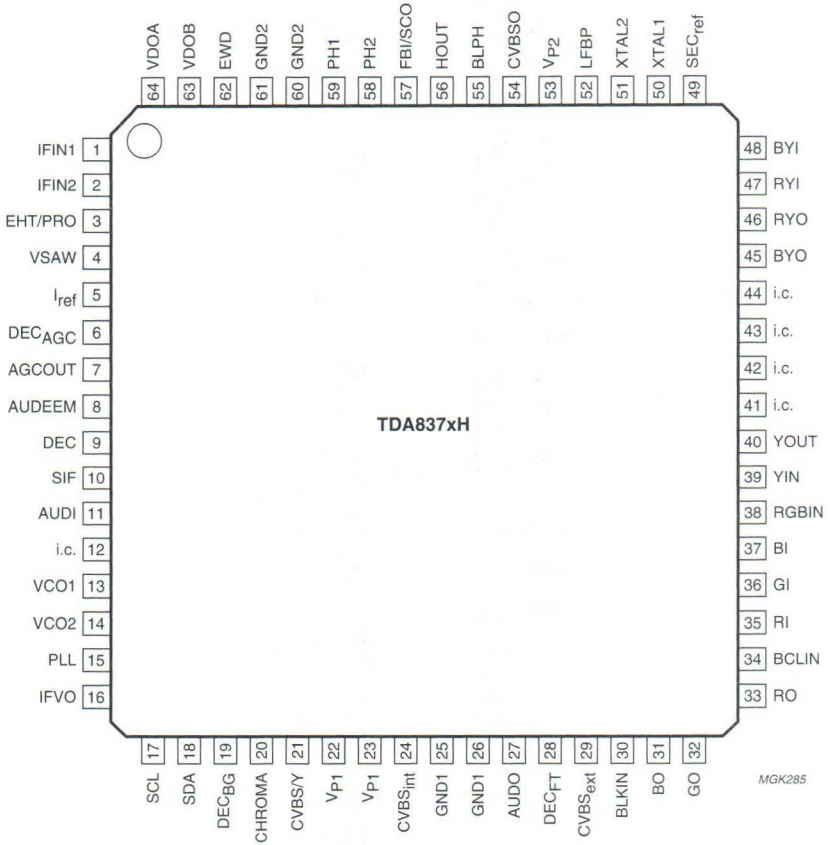


Fig.6 Pin configuration (QFP64).

Multi-purpose power amplifier TDA8580

FEATURES

General

- Operating voltage from 5 to 32 V
- Very low quiescent current
- Dynamic quiescent current control
- Low distortion
- Few external components, fixed again
- High output power
- Can be used as a stereo amplifier in bridge-tied load (BTL) or quad single-ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode with one or two pin operation (at low supply voltage only two pin operation)
- Diagnostic information for Dynamic Distortion Detector (DDD), thermal protection and short-circuit
- No switch on/off plops when switching between standby to mute and from mute to on
- Low offset variation at outputs between mute and on
- Fast mute on supply voltage drops.

Protection

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (positive supply line can be connected to ground)
- Short-circuit proof to ground, positive supply voltage on all pins and across load
- ESD protected on all pins
- Thermal protection over 150 °C
- Load dump protection
- Protected against open-circuit ground pins and output short-circuited to supply ground.

GENERAL DESCRIPTION

The TDA8580 is a stereo bridge-tied load (BTL) or a quad single-ended amplifier that operates over a wide supply voltage range from 5 to 32 V and consumes a very low quiescent current. This makes it suitable for many applications, such as battery fed applications, car radios, television and home-sound systems.

Because of an internal voltage buffer, this device can be used with, or without, a capacitor connected in series with the load (SE application). A combined BTL and 2 × SE application can also be configured.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8580	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		5.0	–	32	V
$I_{q(tot)}$	total quiescent current	V_P = 14.4 V	–	15	30	mA
I_{stb}	standby supply current	V_P = 14.4 V	–	1	50	μA
G_v	closed loop voltage gain	single-ended	25	26	27	dB
		bridge-tied load	31	32	33	dB
Single-ended application						
P_o	output power	THD = 0.5%; V_P = 14.4 V; R_L = 4 Ω	–	5	–	W
		THD = 0.5%; V_P = 32 V; R_L = 4 Ω	–	25	–	W
V_{os}	DC output offset voltage	V_P = 14.4 V; mute	–	–	20	mV
		V_P = 14.4 V; on	–	–	50	mV
V_{no}	noise output voltage	single-ended; R_s = 0 Ω	–	70	100	μV
SVRR	supply voltage ripple rejection	on and mute	50	–	–	dB
Bridge-tied load application						
P_o	output power	THD = 0.5%; V_P = 14.4 V; R_L = 4 Ω	–	17	–	W
		THD = 0.5%; V_P = 32 V; R_L = 8 Ω	–	40	–	W
THD	total harmonic distortion	f_i = 1 kHz; P_o = 1 W; V_P = 14.4 V; R_L = 8 Ω	–	0.05	–	%
		f_i = 1 kHz; P_o = 20 W; V_P = 32 V; R_L = 8 Ω	–	0.05	–	%
V_{os}	DC output offset voltage	V_P = 14.4 V; mute	–	–	20	mV
		V_P = 14.4 V; on	–	–	60	mV
V_{no}	noise output voltage	single-ended; R_s = 0 Ω	–	100	150	μV
SVRR	supply voltage ripple rejection	on and mute	55	–	–	dB

BLOCK DIAGRAM

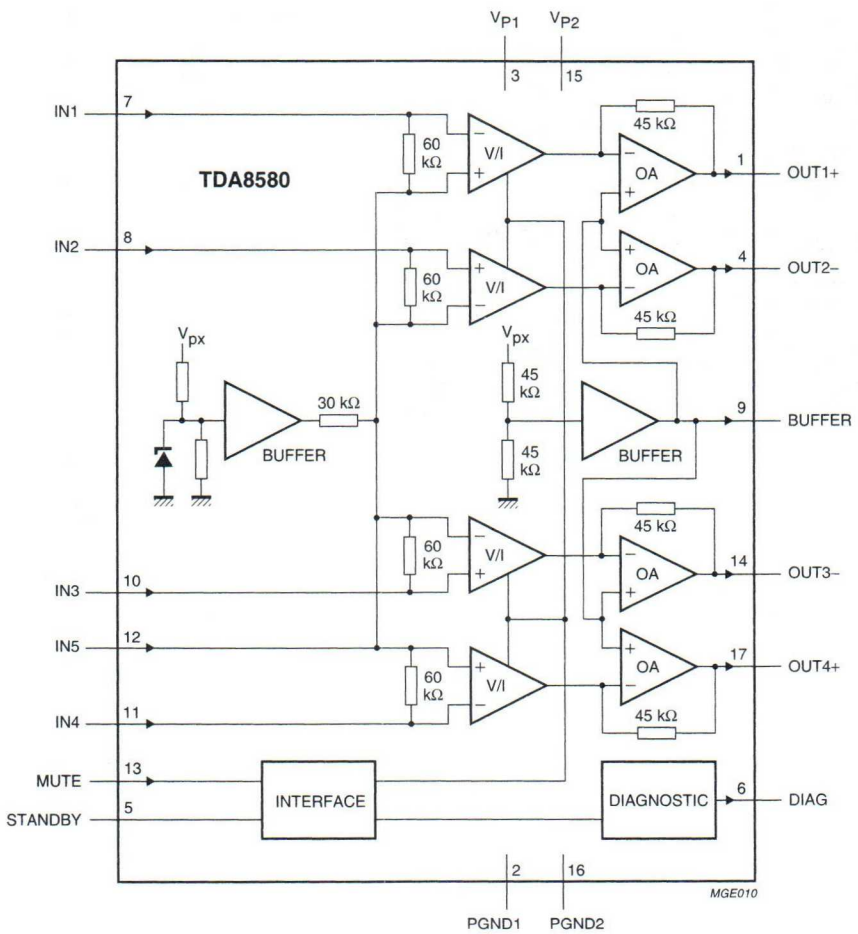


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT1+	1	non-inverting output 1
PGND1	2	power ground 1
V_{P1}	3	supply voltage 1
OUT2–	4	inverting output 2
STANDBY	5	standby/mute/on
DIAG	6	diagnostic
IN1+	7	non-inverting input 1
IN2+	8	inverting input 2
BUFFER	9	buffer output (single-ended output buffer)
IN3+	10	inverting input 3
IN4+	11	non-inverting input 4
IN5–	12	inverting input 5; signal ground
MUTE	13	mute/on
OUT3–	14	inverting output 3
V_{P2}	15	supply voltage 2
PGND2	16	power ground 2
OUT4+	17	non-inverting output 4

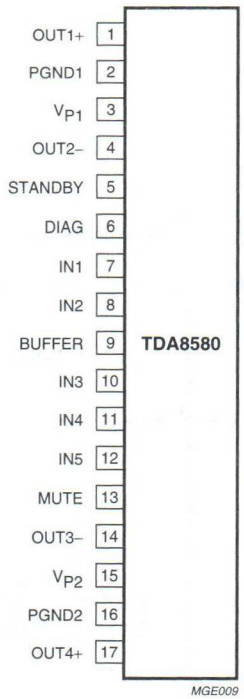


Fig.2 Pin configuration.

8-bit video digital-to-analog converter TDA8702

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

GENERAL DESCRIPTION

The TDA8702 is an 8-bit Digital-to-Analog Converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 kΩ	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	30	MHz
B	–3 dB analog bandwidth	f_{CLK} = 30 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Note

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8702	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8702T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

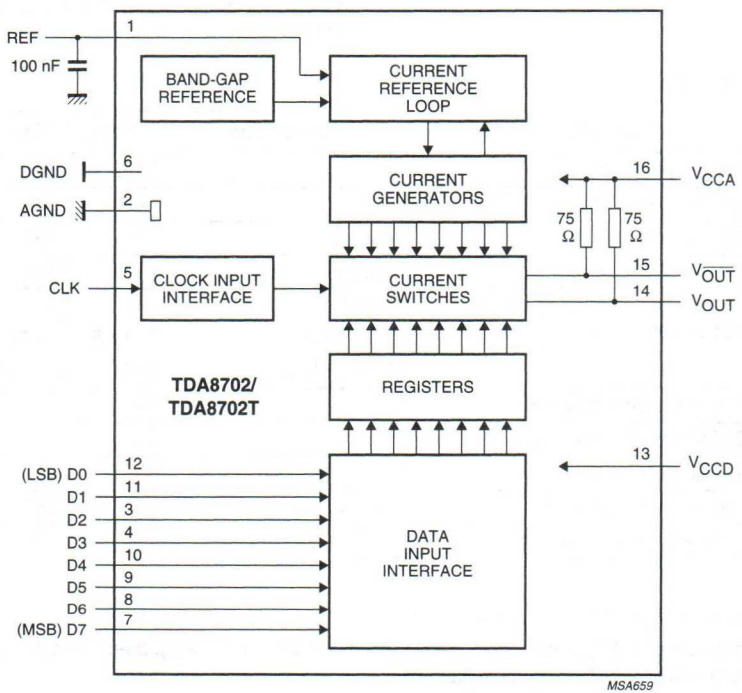


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

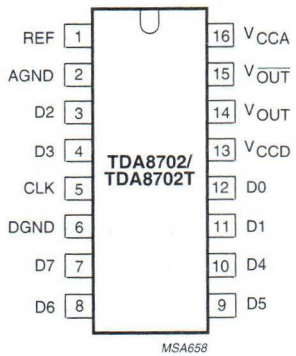


Fig.2 Pin configuration.

6-bit high-speed dual Analog-to-Digital Converter (ADC) TDA8705A

FEATURES

- 2 times 6-bit resolution
- Sampling rate up to 80 MHz
- High signal-to-noise ratio over a large analog input frequency range (5.5 effective bits at 20 MHz full-scale input at f_{clk} = 80 MHz)
- TTL output
- Two separated inputs (AC-coupling)
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference regulation possible)
- Power dissipation only 250 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- DBS (Digital Broadcast Satellite)
- QPSK (Quadrature Phase Shift Keying) demodulation
- Video.

GENERAL DESCRIPTION

The TDA8705A is a 6-bit high-speed dual analog-to-digital converter (ADC) for satellite video and other applications. It converts the two analog input signals into two 6-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		20	27	32	mA
I_{CCD}	digital supply current		10	14	18	mA
I_{CCO}	output stages supply current		10	14	18	mA
ILE	DC integral linear error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
P_{tot}	total power dissipation		–	250	–	mW

Note

1. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8705AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

6-bit high-speed dual Analog-to-Digital Converter (ADC)

TDA8705A

BLOCK DIAGRAM

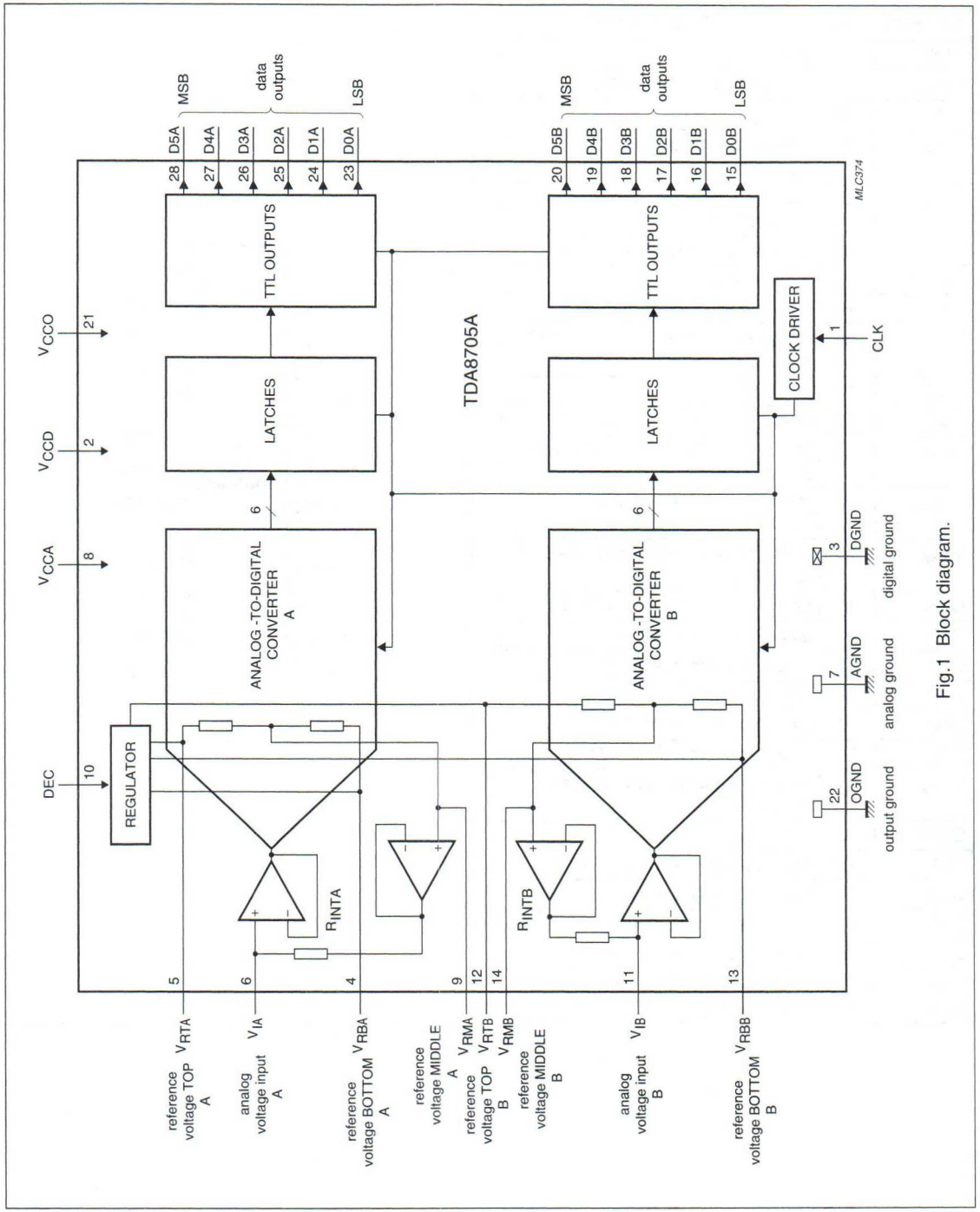


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
V_{CCD}	2	digital supply voltage (+5 V)
DGND	3	digital ground
V_{RBA}	4	reference voltage BOTTOM for ADC A (decoupling)
V_{RTA}	5	reference voltage TOP for ADC A (decoupling)
V_{IA}	6	analog input voltage for ADC A
AGND	7	analog ground
V_{CCA}	8	analog supply voltage (+5 V)
V_{RMA}	9	reference voltage MIDDLE for ADC A (decoupling)
DEC	10	decoupling input
V_{IB}	11	analog input voltage for ADC B
V_{RTB}	12	reference voltage TOP for ADC B (decoupling)
V_{RBB}	13	reference voltage BOTTOM for ADC B (decoupling)
V_{RMB}	14	reference voltage MIDDLE for ADC B (decoupling)
D0B	15	data output; bit 0 (LSB), ADC B
D1B	16	data output; bit 1, ADC B
D2B	17	data output; bit 2, ADC B
D3B	18	data output; bit 3, ADC B
D4B	19	data output; bit 4, ADC B
D5B	20	data output; bit 5 (MSB), ADC B
V_{CCO}	21	supply voltage for output stages (+5 V)
OGND	22	output ground
D0A	23	data output; bit 0 (LSB), ADC A
D1A	24	data output; bit 1, ADC A
D2A	25	data output; bit 2, ADC A
D3A	26	data output; bit 3, ADC A
D4A	27	data output; bit 4, ADC A
D5A	28	data output; bit 5 (MSB), ADC A

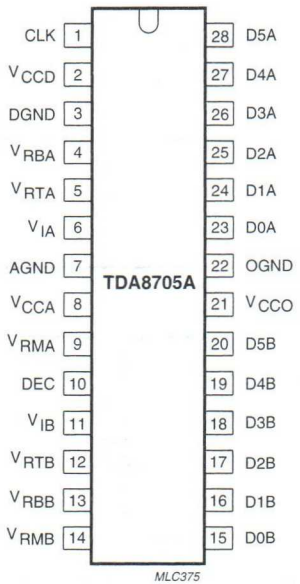


Fig.2 Pin configuration.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706A

FEATURES

- 6-bit resolution
- Binary 3-state CMOS outputs
- CMOS compatible digital inputs
- 3 multiplexed video inputs
- R, G and B clamps on code 0
- Single 6-bit ADC operation allowed up to 40 MSPS
- External control of clamping level
- Internal reference voltage (external reference allowed)
- Power dissipation only 36 mW (typical)
- Operating temperature of −40 to +85 °C
- Operating between 2.7 and 5.5 V.

APPLICATIONS

- General purpose video applications
- R, G and B signals
- Automotive (car navigation)
- LCD systems
- Frame grabber.

GENERAL DESCRIPTION

The TDA8706A is a 6-bit analog-to-digital converter (ADC) with 3 analog multiplexed inputs. Each input has an analog clamp on code 0 for RGB video processing. Clamping level can also be adjusted externally up to code 20. It can also be used as a single 6-bit ADC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.0	5.5	V
V_{DDD}	digital supply voltage		2.7	3.0	5.5	V
V_{DDO}	output stages supply voltage		2.7	3.0	5.5	V
I_{DDA}	analog supply current		–	7	10	mA
I_{DDD}	digital supply current		–	4	6	mA
I_{DDO}	output stages supply current	f_{clk} = 40 MHz; ramp input	–	1	1.5	mA
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input; T_{amb} = 25 °C	–	±0.25	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input; T_{amb} = 25 °C	–	±0.20	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 40 MHz; ramp input				
		3 V supplies	–	36	–	mW
		5.5 V supplies	–	–	96	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8706AM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

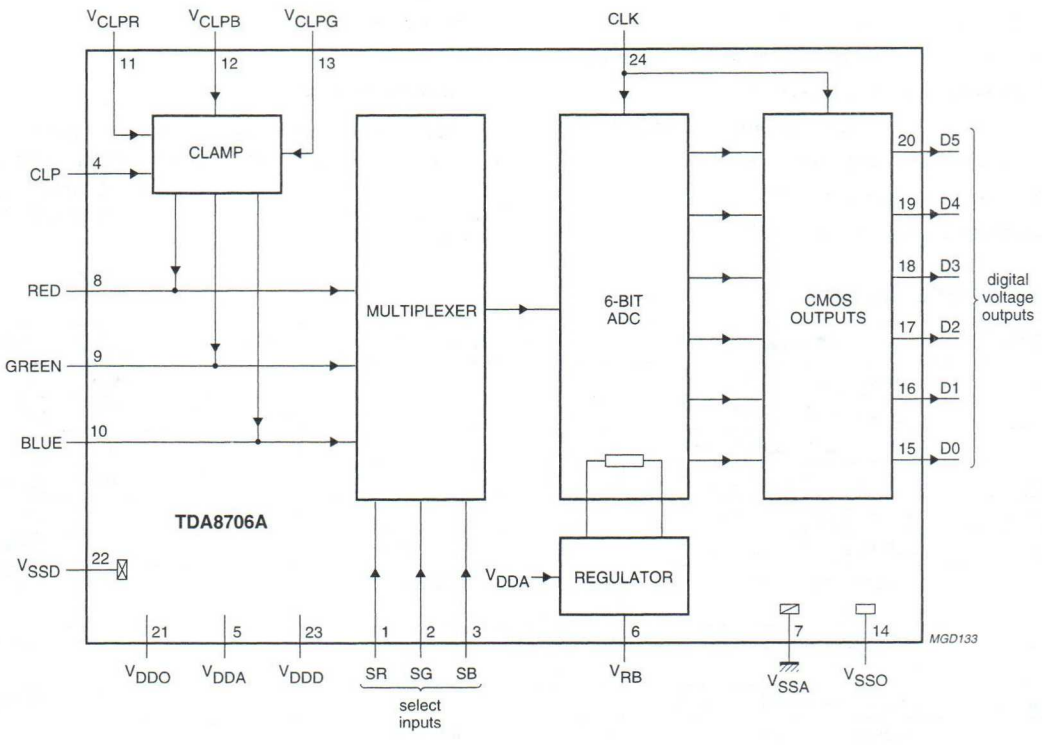


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SR	1	select input RED
SG	2	select input GREEN
SB	3	select input BLUE
CLP	4	clamping pulse input (positive pulse)
V_{DDA}	5	analog supply voltage
V_{RB}	6	reference voltage BOTTOM input
V_{SSA}	7	analog ground
RED	8	RED input
GREEN	9	GREEN input
BLUE	10	BLUE input
V_{CLPR}	11	RED clamping voltage level input
V_{CLPB}	12	BLUE clamping voltage level input
V_{CLPG}	13	GREEN clamping voltage level input
V_{SSO}	14	digital output ground
D0	15	digital voltage output; bit 0 (LSB)
D1	16	digital voltage output; bit 1
D2	17	digital voltage output; bit 2
D3	18	digital voltage output; bit 3
D4	19	digital voltage output; bit 4
D5	20	digital voltage output; bit 5
V_{DDO}	21	supply voltage for output stage
V_{SSD}	22	digital ground
V_{DDD}	23	digital supply voltage
CLK	24	clock input

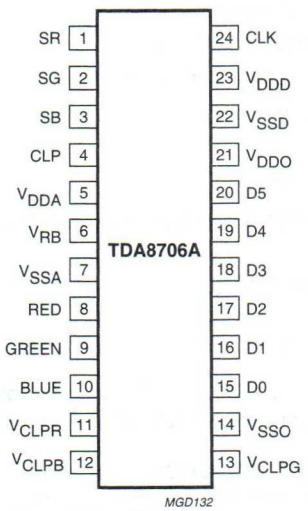


Fig.2 Pin configuration.

Triple RGB 6-bit video analog-to-digital interface

TDA8707

FEATURES

- Triple analog-to-digital converter (ADC)
- 6-bit resolution
- Sampling rate up to 35 MHz
- Power dissipation of 335 mW (typical)
- Internal clamping function
- TTL compatible digital inputs
- −40 to +85 °C operating temperature
- CMOS digital outputs.

APPLICATIONS

- High-speed analog-to-digital conversion for video signals
- VGA signal treatment.

DESCRIPTION

The TDA8707 is a CMOS triple 6-bit video low-power analog-to-digital converter (ADC) for RGB signals. It converts the analog inputs into 6-bit binary coded digital words at a sampling rate of 35 MHz. All analog signal inputs are clamped.

Analog-to-digital converter

The TDA8707 implements 3 independent 6-bit analog-to-digital converters in CMOS process. These converters use a full-flash approach.

Clamping feature

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INR, ING and INB are switched, through series capacitors, to on-chip clamping levels during an active pulse on the clamp input CLP. Clamping level in the R, G and B channels is Code 0.

Input buffers

Internal buffers are provided to drive the analog-to-digital converter inputs. Their ratio can be adjusted externally at 1.5 or 2.0 with select input SLT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	60	80	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	5	8	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
EB	effective bits	note 1	–	5.3	–	bits
f_{clk}	maximum clock conversion rate		35	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 35 MHz; note 2	–	335	485	mW

Notes

1. The number of effective bits is measured with a clock frequency of 35 MHz. This value is given for a 4.43 MHz frequency on the R, G and B channels.
2. The external resistor (value 15 kΩ) between V_{DDA} and CLREF, fixing internal static currents, influences P_{tot}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8707H	QFP44	plastic quad flat package; 44 leads; lead length 1.3 mm; body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

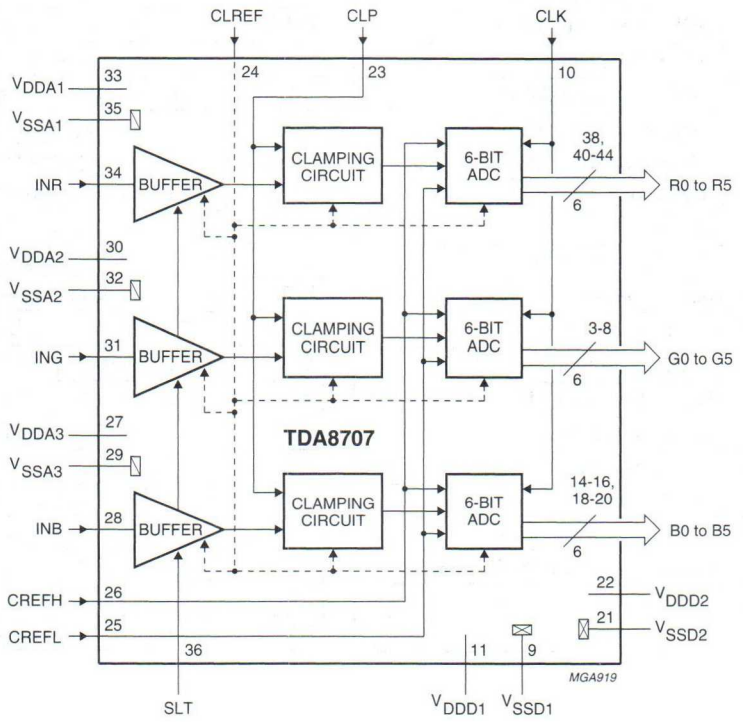


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
G0	3	GREEN data output; bit 0 (LSB)
G1	4	GREEN data output; bit 1
G2	5	GREEN data output; bit 2
G3	6	GREEN data output; bit 3
G4	7	GREEN data output; bit 4
G5	8	GREEN data output; bit 5 (MSB)
V_{SSD1}	9	digital supply ground 1
CLK	10	clock input
V_{DDD1}	11	digital supply voltage 1
n.c.	12	not connected
n.c.	13	not connected
B0	14	BLUE data output; bit 0 (LSB)
B1	15	BLUE data output; bit 1
B2	16	BLUE data output; bit 2
n.c.	17	not connected
B3	18	BLUE data output; bit 3
B4	19	BLUE data output; bit 4
B5	20	BLUE data output; bit 5 (MSB)
V_{SSD2}	21	digital supply ground 2
V_{DDD2}	22	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
CLP	23	clamping input
CLREF	24	ADCs current reference level input
CREFL	25	converter reference LOW level input
CREFH	26	converter reference HIGH level input
V_{DDA3}	27	analog supply voltage 3
INB	28	BLUE analog input
V_{SSA3}	29	analog supply ground 3
V_{DDA2}	30	analog supply voltage 2
ING	31	GREEN analog input
V_{SSA2}	32	analog supply ground 2
V_{DDA1}	33	analog supply voltage 1
INR	34	RED analog input
V_{SSA1}	35	analog supply ground 1
SLT	36	select input buffer ratio
n.c.	37	not connected
R0	38	RED data output; bit 0 (LSB)
n.c.	39	not connected
R1	40	RED data output; bit 1
R2	41	RED data output; bit 2
R3	42	RED data output; bit 3
R4	43	RED data output; bit 4
R5	44	RED data output; bit 5 (MSB)

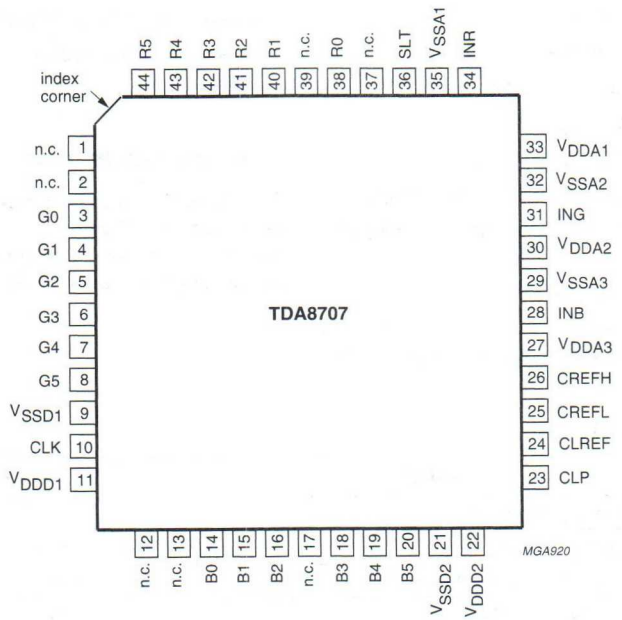


Fig.2 Pin configuration.

Video analog input interface TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

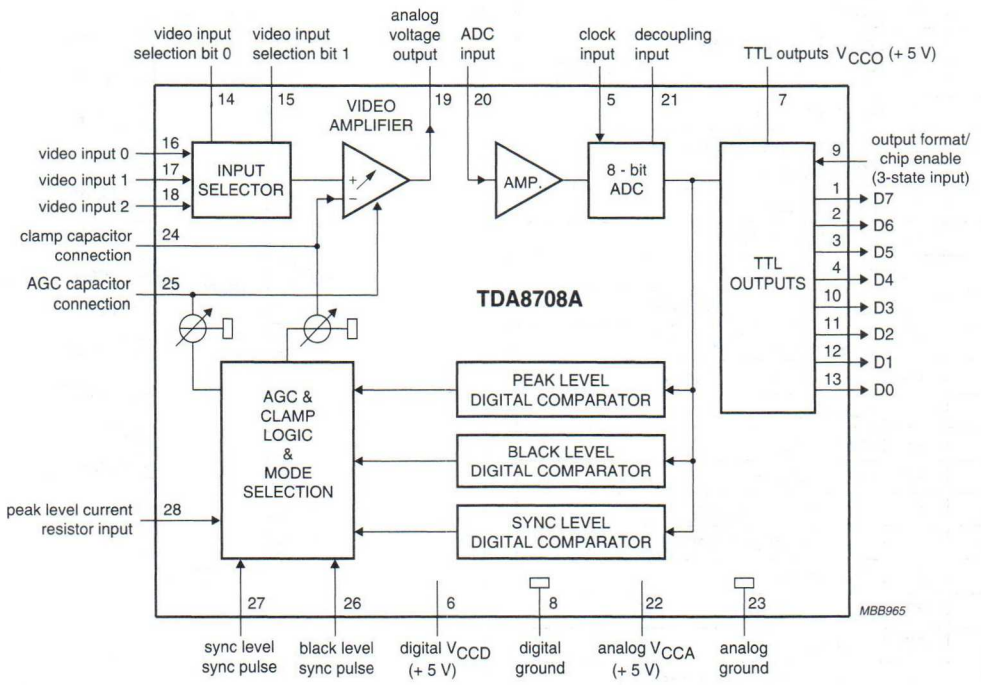


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

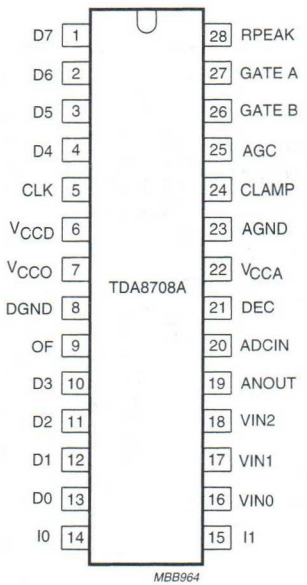


Fig.2 Pin configuration.

Video analog input interface TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

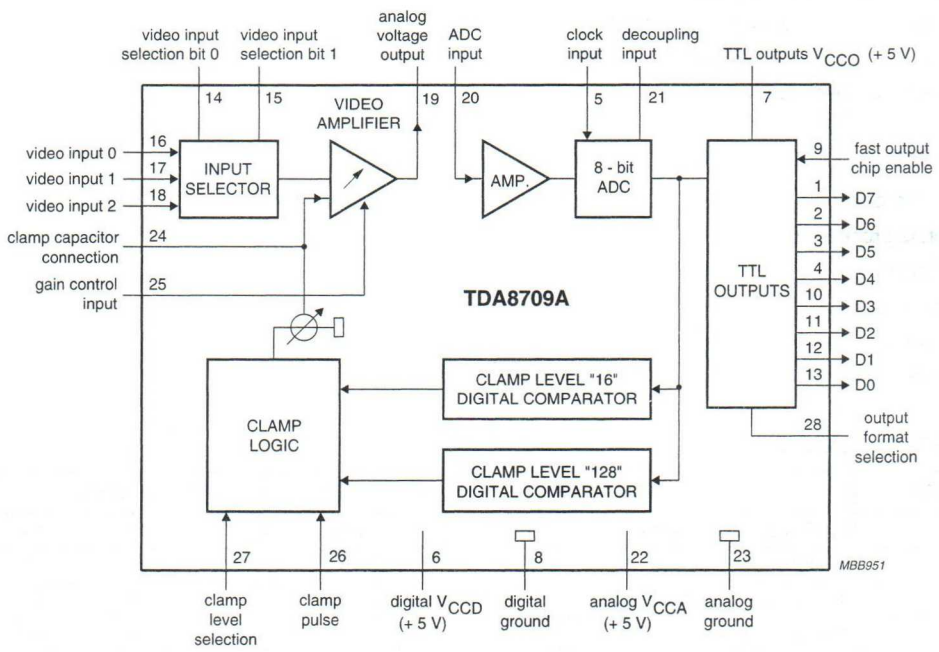


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

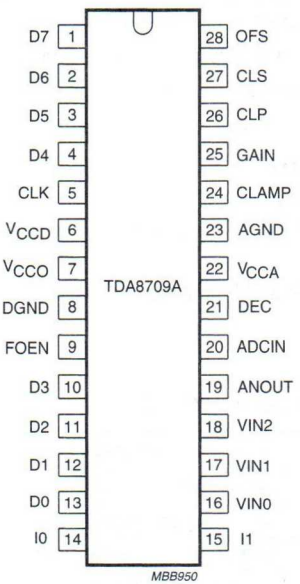


Fig.2 Pin configuration.

8-bit high-speed analog-to-digital converter

TDA8714

FEATURES

- 8-bit resolution
- Sampling rate up to 75 MHz
- No missing codes guaranteed
- High signal-to-noise ratio over a large analog input frequency range (7.7 effective bits at 4.43 MHz full-scale input at f_{clk} = 75 MHz)
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 340 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- video data digitizing
- radar pulse analysis
- transient signal analysis
- high energy physics research
- ΣΔ modulators
- medical imaging.

GENERAL DESCRIPTION

The TDA8714 is an 8-bit high-speed Analog-to-Digital Converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 75 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	25	30	mA
I_{CCD}	digital supply current		–	27	33	mA
I_{CCO}	output stages supply current		–	16	20	mA
INL	DC integral non-linearity		–	±0.4	±0.5	LSB
DNL	DC differential non-linearity		–	±0.2	±0.35	LSB
AINL	AC integral non-linearity	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8714/7		75	–	–	MHz
	TDA8714/6		60	–	–	MHz
	TDA8714/4		40	–	–	MHz
P_{tot}	total power dissipation		–	340	435	mW

Note

1. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 75 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8714T/4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	40
TDA8714T/6	SO24		SOT137-1	60
TDA8714T/7	SO24		SOT137-1	75
TDA8714M/4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	40
TDA8714M/6	SSOP24		SOT340-1	60
TDA8714M/7	SSOP24		SOT340-1	75

BLOCK DIAGRAM

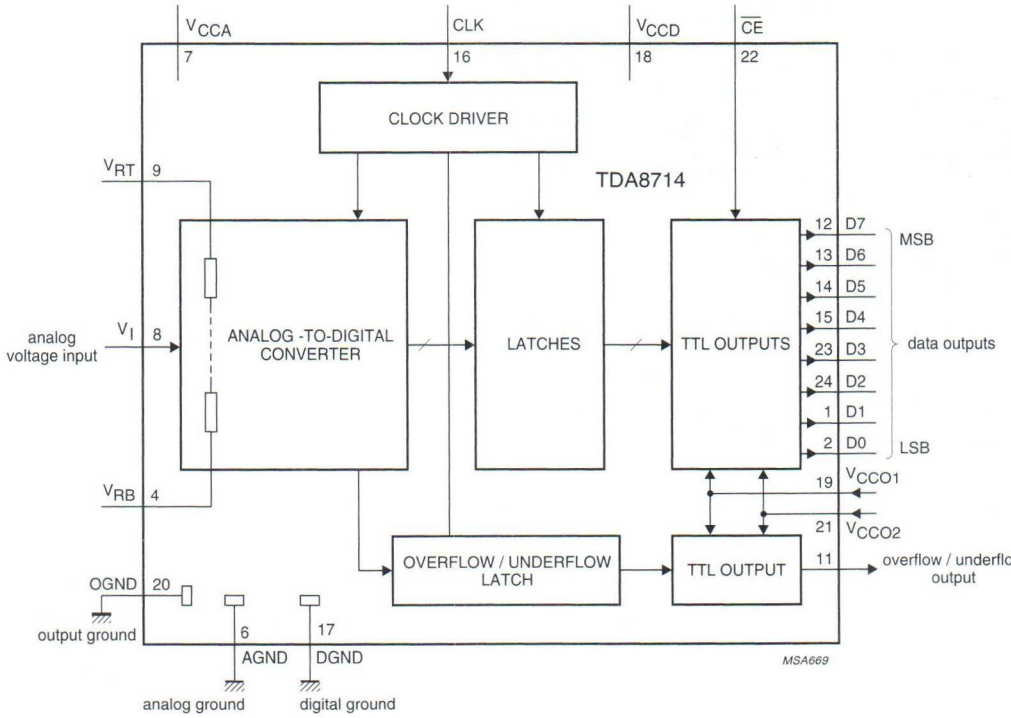


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage BOTTOM input
n.c.	5	not connected
AGND	6	analog ground
V_{CCA}	7	analog supply voltage (+5 V)
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	digital supply voltage (+5 V)
V_{CCO1}	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

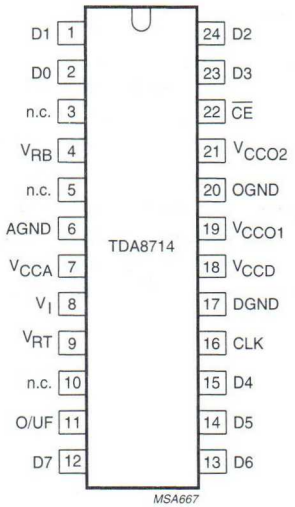


Fig.2 Pin configuration.

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

FEATURES

- Video amplifier with clamp and white clip circuits
- FM sound modulator
- Asymmetrical and symmetrical RF outputs available
- Symmetrical RF oscillator using only a few external components
- External adjusting of modulation depth and level of the sound subcarrier
- I²C-bus receiver for frequency setting and test-mode selection
- One I²C programmable output port
- On-chip Phase-Locked Loop (PLL) frequency synthesizer
- On-chip power supply regulator
- Bus switchable oscillator
- On-chip Test Pattern Signal Generator (TPSG).

GENERAL DESCRIPTION

The TDA8722 is a programmable modulator which generates an RF TV channel from a baseband video signal and a baseband audio signal in the event of negative video and FM sound standards (PAL B/G, I, D/K and NTSC).

It is especially suited for satellite receivers, video recorders and cable converters. The video carrier frequency is set exactly to the correct channel frequency by a PLL synthesizer which is programmed in accordance with the I²C-bus format.

APPLICATIONS

- Video recorders
- Cable converters
- Satellite receivers.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8722T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA8722M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

QUICK REFERENCE DATA

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C after the IC has reached thermal equilibrium; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DD}	total supply current	normal mode	41	52	63	mA
Δm	typical modulation depth range	video level (pin 19) = 0.5 V (p-p); note 1; see Fig.10	65	–	90	%
$\Delta P/S$	typical picture-to-sound level range	note 2; see Fig.11	−18	–	−10	dB
V_{RF}	RF output voltage level asymmetrical on a 75 Ω load	frequency between 471.25 and 855.25 MHz	77	80	83	dBμV
δf	FM deviation on audio subcarrier	$f_i = 400$ Hz; $V_1 = 0.5$ V (RMS); before pre-emphasis filter	20	25	30	kHz

Notes

1. Value depends on value of resistor R17 (see Fig.7).
2. Value depends on value of capacitor C17 (see Fig.7).

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

BLOCK DIAGRAM

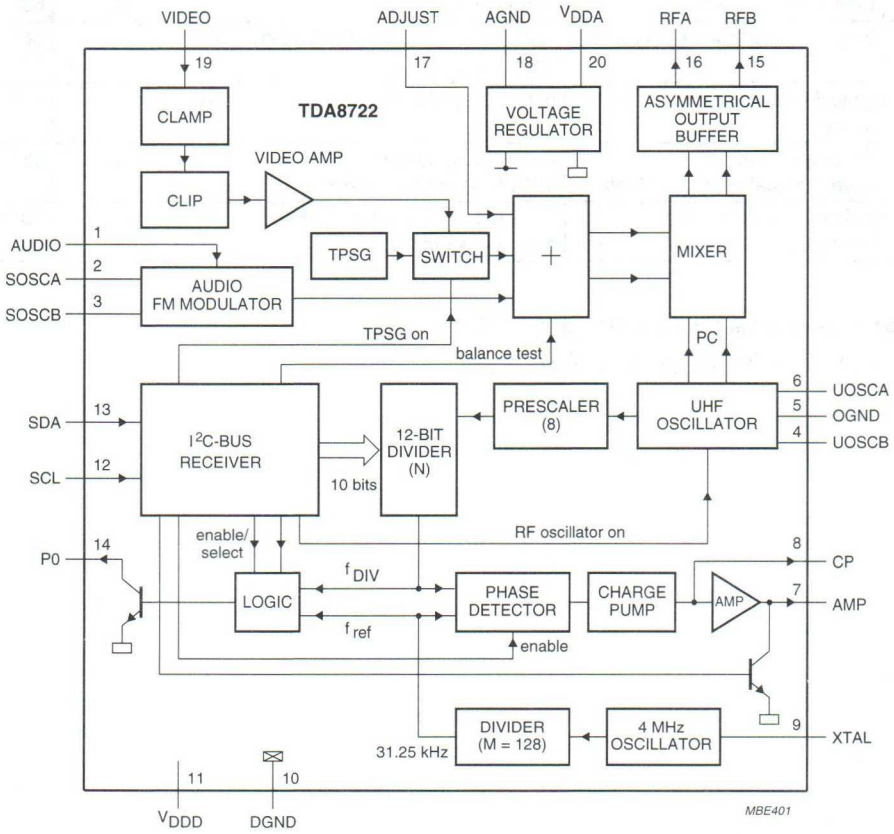


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AUDIO	1	audio input
SOSCA	2	sound oscillator A
SOSCB	3	sound oscillator B
UOSCB	4	UHF oscillator B
OGND	5	RF oscillator ground
UOSCA	6	UHF oscillator A
AMP	7	tuning amplifier output
CP	8	charge pump output
XTAL	9	crystal oscillator
DGND	10	digital ground
V_{DDD}	11	digital supply voltage
SCL	12	serial clock input (I²C-bus)
SDA	13	serial data input (I²C-bus)
P0	14	NPN open-collector output Port
RFB	15	asymmetrical RF output B
RFA	16	asymmetrical RF output A
ADJUST	17	modulation depth and picture-to-sound distance adjustment pin
AGND	18	analog ground
VIDEO	19	video input
V_{DDA}	20	analog supply voltage

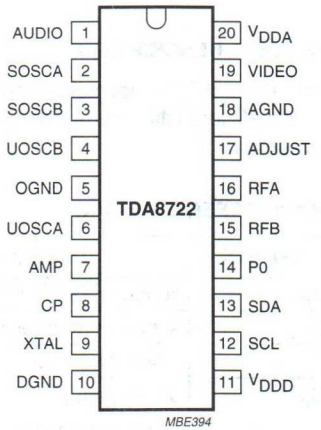


Fig.2 Pin configuration.

Antenna signal processor TDA8725T

FEATURES

- 75 Ω antenna input stage
- 75 Ω VCR RF input stage
- 75 Ω VCR tuner output
- 75 Ω TV tuner output.

GENERAL DESCRIPTION

The TDA8725T has been designed to split and combine RF signals for Picture-In-Picture (PIP) and VCR applications.

For PIP applications, the antenna input signal is split and fed to the main TV tuner and the PIP tuner. Good signal suppression between the two outputs enables good quality of the main picture when the PIP tuner is in use.

For VCR applications, the antenna input signal is split and then fed directly to the VCR tuner and the TV tuner after being combined with the VCR - RF signal. Good signal suppression between the two outputs enables good quality pictures when the TV and VCR tuners are both operating. Good signal suppression between the VCR input and the antenna input reduces the amount of unwanted signal on the antenna.

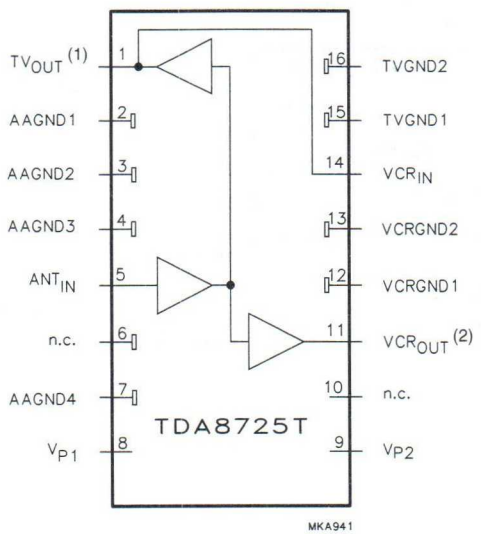
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 8 and 9)		4.75	5.0	5.25	V
I_P	supply current (pins 8 and 9)		–	65	–	mA
f_i	input frequency		40	–	860	MHz
G_p	power gain					
	from antenna to VCR		3.5	5.0	6.5	dB
	from antenna to TV		4	5.5	7	dB
	from VCR		–	0	–	dB
F	noise figure		6.5	9.0	10	dB
IP2	antenna linearity 2nd order intercept point	at 40 MHz	137	140	–	dBμV
		at 860 MHz	119	124	–	dBμV
IP3	antenna linearity 3rd order intercept point	at 40 MHz	121	124	–	dBμV
		at 860 MHz	108	111	–	dBμV
s_{sup}	signal suppression					
	VCR input to antenna	0 to 1 GHz	32	37	–	dB
		1 to 3 GHz	25	30	–	dB
	VCR output to TV output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
	TV output to VCR output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
VSWR	voltage standing wave ratio					
	at the antenna input		–	2.5	4	
	at the outputs		–	1.5	3	
$P_{i(max)}$	maximum input power on antenna for 1 dB gain compression		–	−10	–	dBm

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8725T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) TV tuner or main tuner.
(2) VCR tuner or PIP tuner.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TV_{OUT}	1	output to TV tuner (VCR+TV) and to main tuner (PIP)
AAGND1	2	antenna amplifier ground 1
AAGND2	3	antenna amplifier ground 2
AAGND3	4	antenna amplifier ground 3
ANT_{IN}	5	antenna input
n.c.	6	not connected
AAGND4	7	antenna amplifier ground 4
V_{P1}	8	power supply for the antenna amplifier
V_{P2}	9	power supply for the VCR output amplifier
n.c.	10	not connected
VCR_{OUT}	11	output to VCR and PIP tuner
VCRGND1	12	VCR amplifier ground 1
VCRGND2	13	VCR amplifier ground 2
VCR_{IN}	14	VCR RF input
TVGND1	15	TV amplifier ground 1
TVGND2	16	TV amplifier ground 2

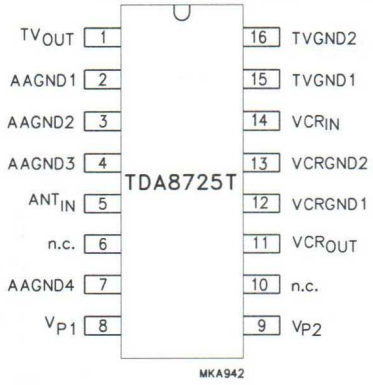


Fig.2 Pin configuration.

Triple high speed Analog-to-Digital Converter (ADC)

TDA8752

FEATURES

- Triple 8-bit ADC
- Sampling rate up to 80 MHz
- IC controllable via a serial interface, which can be either I²C-bus or 3-wire, selected via a TTL input pin
- IC analog voltage input from 0.4 to 1.2 V (p-p) to produce full-scale ADC input of 1 V (p-p)
- 3 clamps for programming a clamping code between −63.5 and +64 in steps of ½LSB
- 3 controllable amplifiers: gain controlled via the serial interface to produce a full scale resolution of ½LSB peak-to-peak
- Amplifier bandwidth of 250 MHz
- Low gain variation with temperature
- PLL, controllable via the serial interface to generate the ADC clock, which can be locked to a line frequency from 15 to 280 kHz
- Integrated PLL divider
- Programmable phase clock adjustment cells
- Internal voltage regulators
- TTL compatible digital inputs and outputs
- Chip enable high-impedance ADC output
- Power-off mode
- Possibility to use up to four ICs in the same system, using the I²C-bus interface, or more, using the 3-wire serial interface
- 1 W power dissipation.

APPLICATIONS

- R, G and B high speed digitizing
- LCD panels drive
- LCD projection systems
- VGA and higher resolutions
- Using two ICs in parallel, higher display resolution can be obtained; 160 MHz pixel frequency.

GENERAL DESCRIPTION

The TDA8752 is a triple 8-bit ADC with controllable amplifiers and clamps for the digitizing of large bandwidth RGB signals.

The clamp level, the gain and all of the other settings are controlled via a serial interface (either I²C-bus or 3-wire serial bus, selected via a logic input).

The IC also includes a PLL that can be locked on the horizontal line frequency and generates the ADC clock. The PLL jitter is minimized for high resolution PC graphics applications. An external clock can also be input to the ADC.

It is possible to set the TDA8752 serial bus address between four fixed values, in the event that several TDA8752 ICs are used in a system, using the I²C-bus interface (for example, two ICs used in an odd/even configuration).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8752H/6	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2	60
TDA8752H/8				80

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	for R, G and B channels	4.75	5.0	5.25	V
V_{DDD}	logic supply voltage	for I^2C-bus and 3-wire	4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage	for R, G and B channels	4.75	5.0	5.25	V
$V_{CCA(PLL)}$	analog PLL supply voltage		4.75	5.0	5.25	V
$V_{CCO(PLL)}$	output PLL supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	120	–	mA
I_{DDD}	logic supply current	for I^2C-bus and 3-wire	–	1.0	–	mA
I_{CCD}	digital supply current		–	40	–	mA
I_{CCO}	output stages supply current	f_{CLK} = 80 MHz; ramp input	–	6	–	mA
$I_{CCA(PLL)}$	analog PLL supply current		–	28	–	mA
$I_{CCO(PLL)}$	output PLL supply current		–	5	–	mA
f_{CLK}	maximum clock frequency	TDA8752/6	60	–	–	MHz
		TDA8752/8	80	–	–	MHz
$f_{ref(PLL)}$	PLL reference clock frequency		15	–	280	kHz
f_{VCO}	VCO output clock frequency		12	–	80	MHz
INL	DC integral non linearity	from analog input to digital output; full-scale; ramp input; f_{CLK} = 80 MHz	–	±0.5	tbf	LSB
DNL	DC differential non linearity	from analog input to digital output; full-scale; ramp input; f_{CLK} = 80 MHz	–	±0.5	tbf	LSB
$\Delta G_{amp}/T$	amplifier gain stability as a function of temperature	V_{ref} = 2.5 V with 100 ppm/°C maximum	–	–	200	ppm/°C
B	amplifier bandwidth	–3 dB; T_{amb} = 25 °C	250	–	–	MHz
t_{set}	settling time of the ADC block plus AGC	input signal settling time < 1 ns; T_{amb} = 25 °C	–	–	6	ns
$j_{PLL(rms)}$	maximum PLL phase jitter (RMS value)		–	0.2	–	ns
DR_{PLL}	PLL divider ratio	without divide-by-2	15	–	2047	
P_{tot}	total power consumption	f_{CLK} = 80 MHz; ramp input	–	1.0	tbf	W

BLOCK DIAGRAM

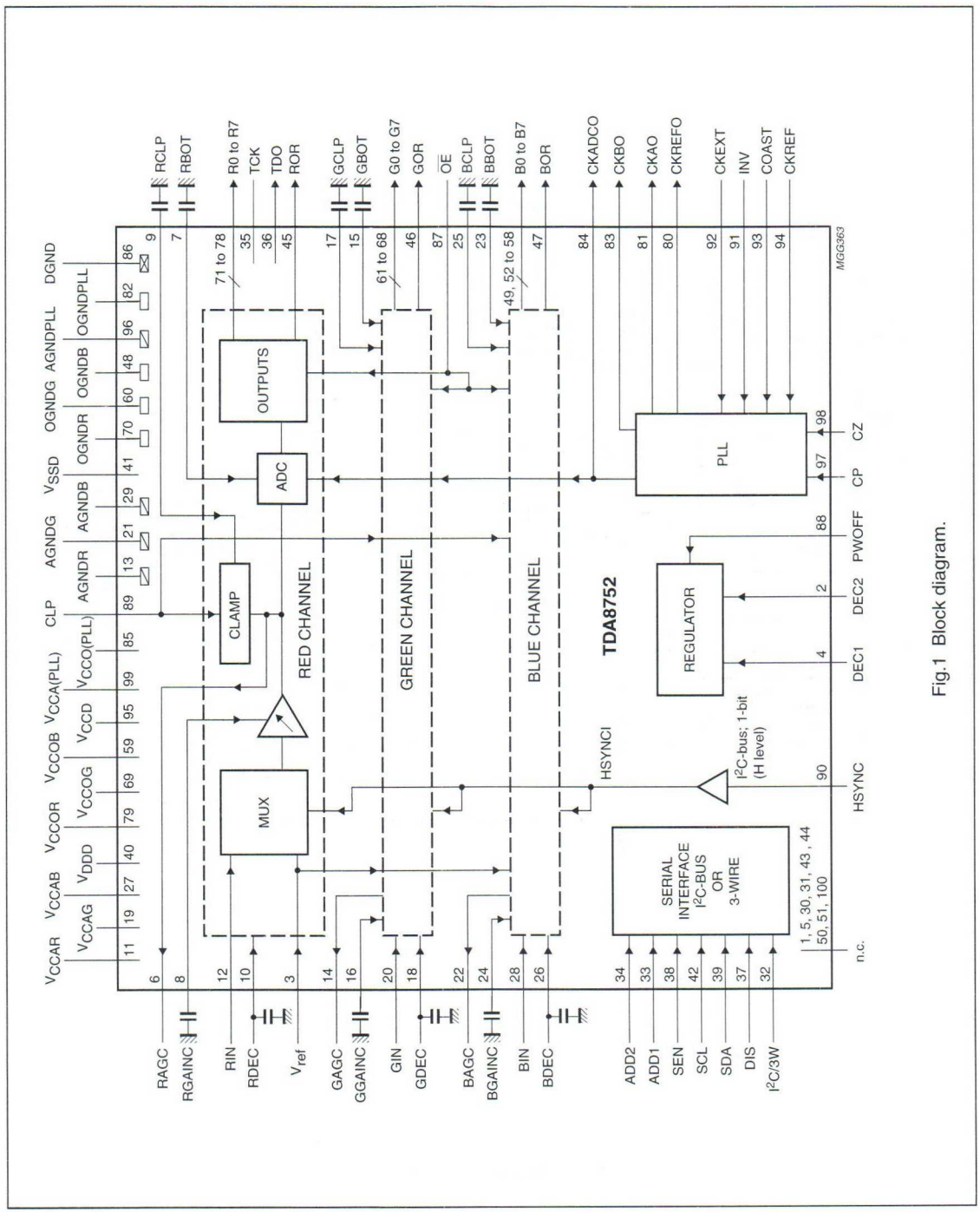


Fig.1 Block diagram.

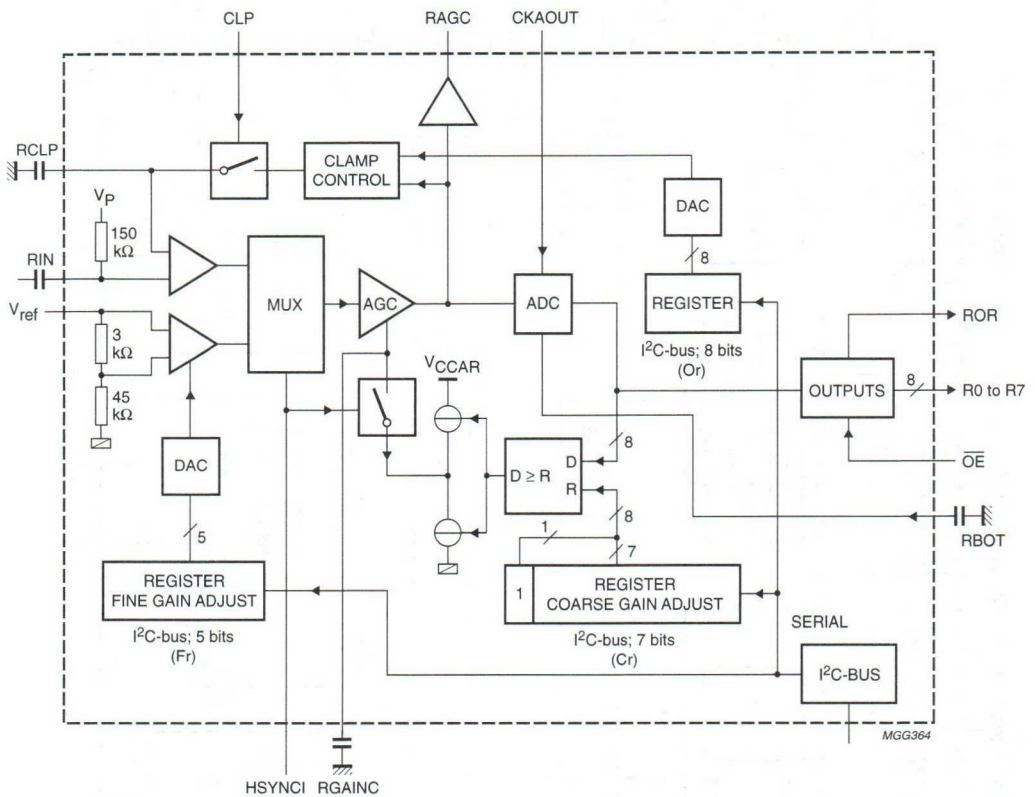


Fig.2 Red channel diagram.

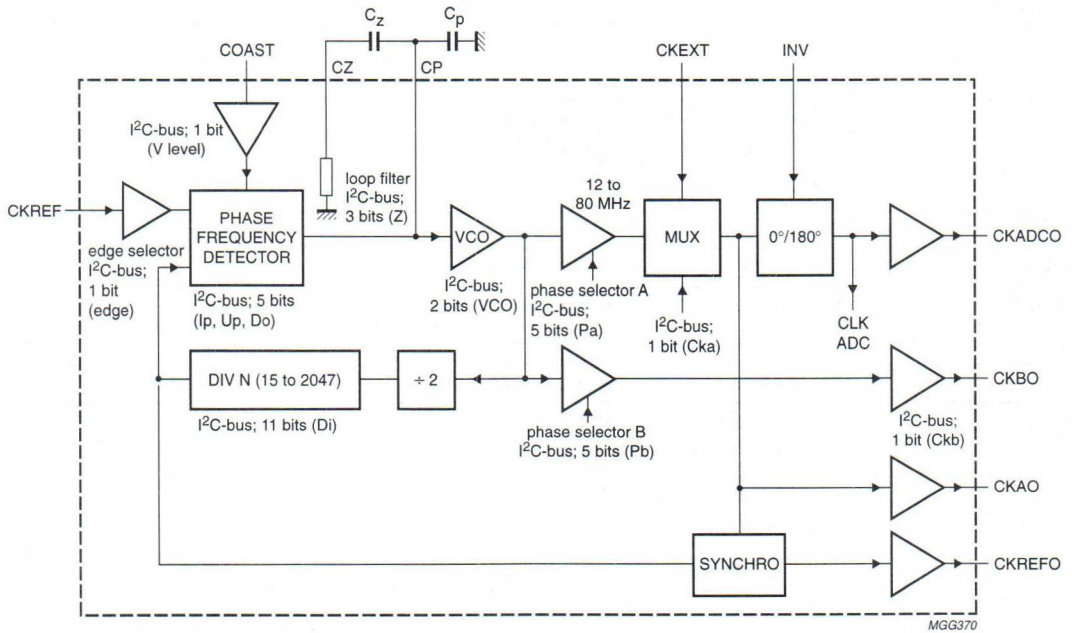


Fig.3 PLL diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DEC2	2	main regulator decoupling input
V_{ref}	3	gain stabilizer voltage reference input
DEC1	4	main regulator decoupling input
n.c.	5	not connected
RAGC	6	red channel AGC output
RBOT	7	red channel ladder decoupling input (BOT)
RGAINC	8	red channel gain capacitor input
RCLP	9	red channel gain clamp capacitor input
RDEC	10	red channel gain regulator decoupling input
V_{CCAR}	11	red channel gain analog power supply
RIN	12	red channel gain analog input
AGNDR	13	red channel gain analog ground
GAGC	14	green channel AGC output
GBOT	15	green channel ladder decoupling input (BOT)
GGAINC	16	green channel gain capacitor input
GCLP	17	green channel gain clamp capacitor input
GDEC	18	green channel gain regulator decoupling input
V_{CCAG}	19	green channel gain analog power supply
GIN	20	green channel gain analog input
AGNDG	21	green channel gain analog ground
BAGC	22	blue channel AGC output
BBOT	23	blue channel ladder decoupling input (BOT)
BGAINC	24	blue channel gain capacitor input
BCLP	25	blue channel gain clamp capacitor input
BDEC	26	blue channel gain regulator decoupling input
V_{CCAB}	27	blue channel gain analog power supply
BIN	28	blue channel gain analog input
AGNDB	29	blue channel gain analog ground
n.c.	30	not connected
n.c.	31	not connected
I^2C/3W	32	selection input between I^2C-bus (active HIGH) and 3-wire serial bus (active LOW)
ADD1	33	I^2C-bus address control input 1
ADD2	34	I^2C-bus address control input 2
TCK	35	scan test mode (active HIGH)

SYMBOL	PIN	DESCRIPTION
TDO	36	scan test output
DIS	37	I^2C and 3W disable control input (disable at HIGH level)
SEN	38	select enable for 3-wire serial bus input (see Fig.9)
SDA	39	I^2C/3W serial data input
V_{DDD}	40	logic I^2C/3W digital power supply
V_{SSD}	41	logic I^2C/3W digital ground
SCL	42	I^2C/3W serial clock input
n.c.	43	not connected
n.c.	44	not connected
ROR	45	red channel ADC output bit overflow
GOR	46	green channel ADC output bit overflow
BOR	47	blue channel ADC output bit overflow
OGNDB	48	blue channel ADC output ground
B0	49	blue channel ADC output bit 0 (LSB)
n.c.	50	not connected
n.c.	51	not connected
B1	52	blue channel ADC output bit 1
B2	53	blue channel ADC output bit 2
B3	54	blue channel ADC output bit 3
B4	55	blue channel ADC output bit 4
B5	56	blue channel ADC output bit 5
B6	57	blue channel ADC output bit 6
B7	58	blue channel ADC output bit 7 (MSB)
V_{CCOB}	59	blue channel ADC output power supply
OGNDG	60	green channel ADC output ground
G0	61	green channel ADC output bit 0 (LSB)
G1	62	green channel ADC output bit 1
G2	63	green channel ADC output bit 2
G3	64	green channel ADC output bit 3
G4	65	green channel ADC output bit 4
G5	66	green channel ADC output bit 5
G6	67	green channel ADC output bit 6
G7	68	green channel ADC output bit 7 (MSB)
V_{CCOG}	69	green channel ADC output power supply
OGNDR	70	red channel ADC output ground
R0	71	red channel ADC output bit 0 (LSB)

SYMBOL	PIN	DESCRIPTION
R1	72	red channel ADC output bit 1
R2	73	red channel ADC output bit 2
R3	74	red channel ADC output bit 3
R4	75	red channel ADC output bit 4
R5	76	red channel ADC output bit 5
R6	77	red channel ADC output bit 6
R7	78	red channel ADC output bit 7 (MSB)
V_{CCOR}	79	red channel ADC output power supply
CKREFO	80	reference output clock
CKAO	81	PLL clock output 3 (in phase with reference output clock)
OGNDPLL	82	PLL digital ground
CKBO	83	PLL clock output 2
CKADCO	84	PLL clock output 1 (in phase with internal ADC clock)
$V_{CCO(PLL)}$	85	PLL output power supply
DGND	86	digital ground
$\overline{OE}$	87	output enable not (when $\overline{OE}$ is HIGH, the outputs are in high-impedance)
PWOFF	88	power off control input (IC is in power-down mode when this pin is HIGH)
CLP	89	clamp pulse input (clamp active HIGH)
HSYNC	90	horizontal synchronization input pulse
INV	91	PLL clock output inverter command input (invert when HIGH)
CKEXT	92	external clock input
COAST	93	PLL coast command input
CKREF	94	PLL reference clock input
V_{CCD}	95	digital power supply
AGNDPLL	96	PLL analog ground
CP	97	PLL filter input
CZ	98	PLL filter input
V_{CCAPLL}	99	PLL analog power supply
n.c.	100	not connected

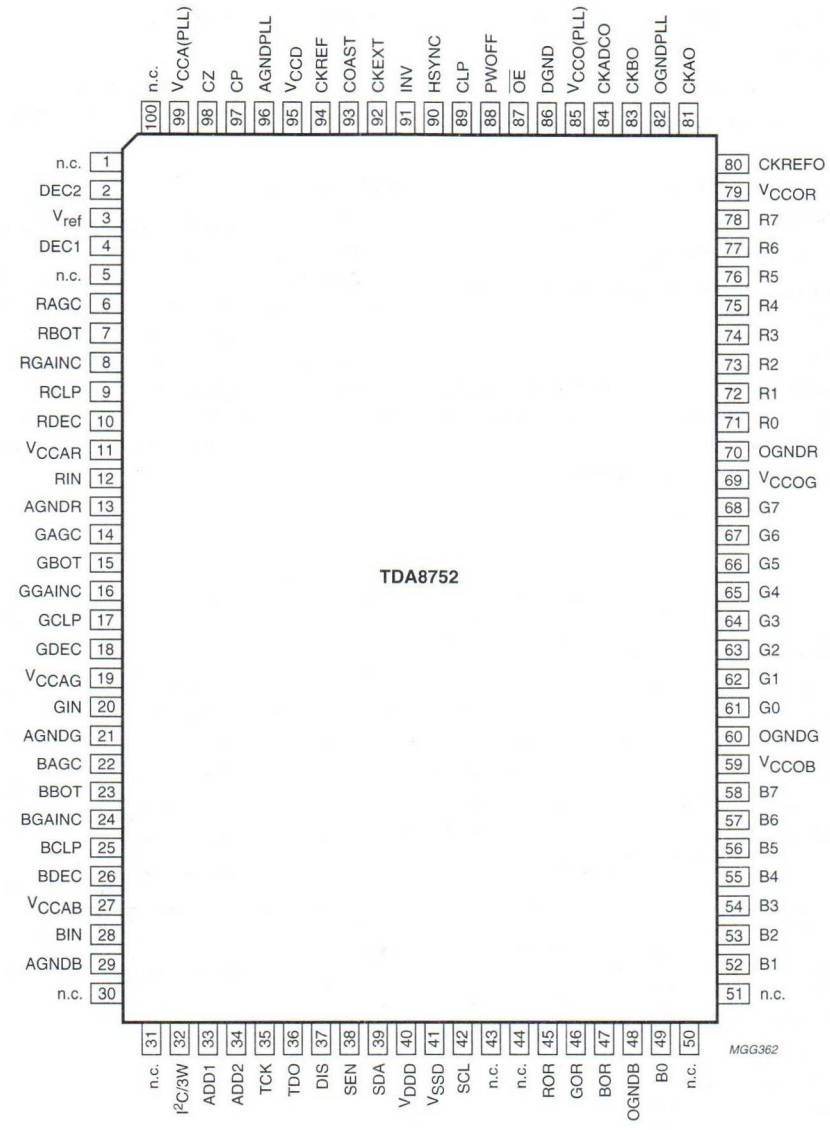


Fig.4 Pin configuration.

YC 8-bit low-power analog-to-digital video interface

TDA8758

FEATURES

- Two 8-bit ADCs:
  - one Luminance or CVBS channel
  - one Chrominance channel
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs for each channel
- Internal reference voltage regulator
- TTL-compatible digital inputs and outputs
- Power dissipation of 530 mW (typical)
- Input selector circuit (five selectable video inputs for CVBS or YC processing)
- Peak white enable input
- Clamp and Automatic Gain Control (AGC) functions for Y/CVBS channel (clamping on code 64 and Peak White level control at code 255)
- Clamp function for C channel (code 128)
- No sample-and-hold circuit required.

APPLICATIONS

- Video signal decoding
- Digital picture processing
- Frame grabbing
- Multimedia with the Philips Desktop Video chip set (and especially SAA7196 multistandard decoder and scaler).

GENERAL DESCRIPTION

The TDA8758 is an 8-bit video high-speed low-power analog-to-digital conversion (ADC) interface for YC and CVBS signal processing. It converts 1-of-3 CVBS input signals or 1-of-2 YC input signals into binary or two's complement words at a sampling rate of 32 MHz.
All analog signal inputs are digitally clamped and an ADC interface is provided on the Y/CVBS channel. A fast precharge on clamp and AGC is provided for start-up.
All digital inputs and outputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	59	70	mA
I_{CCD}	digital supply current		–	28	40	mA
I_{CCO}	output supply current	C_L = 15 pF	–	19	28	mA
ILE	DC integral linearity error		–	±0.75	±1.5	LSB
DLE	DC differential linearity error		–	±0.4	±1.0	LSB
EB	effective bits (from video input to digital outputs)	f_{clk} = 32 MHz; f_i = 4.43 MHz	–	7.1	–	bits
$f_{clk(max)}$	maximum clock frequency		30	32	–	MHz
B	maximum –3 dB bandwidth (input preamplifier)	full-scale; 0 dB gain	–	15	–	MHz
α_{ct}	crosstalk between Y and C channels and each video input		–	–63	–55	dB
P_{tot}	total power dissipation		–	530	724	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8758G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

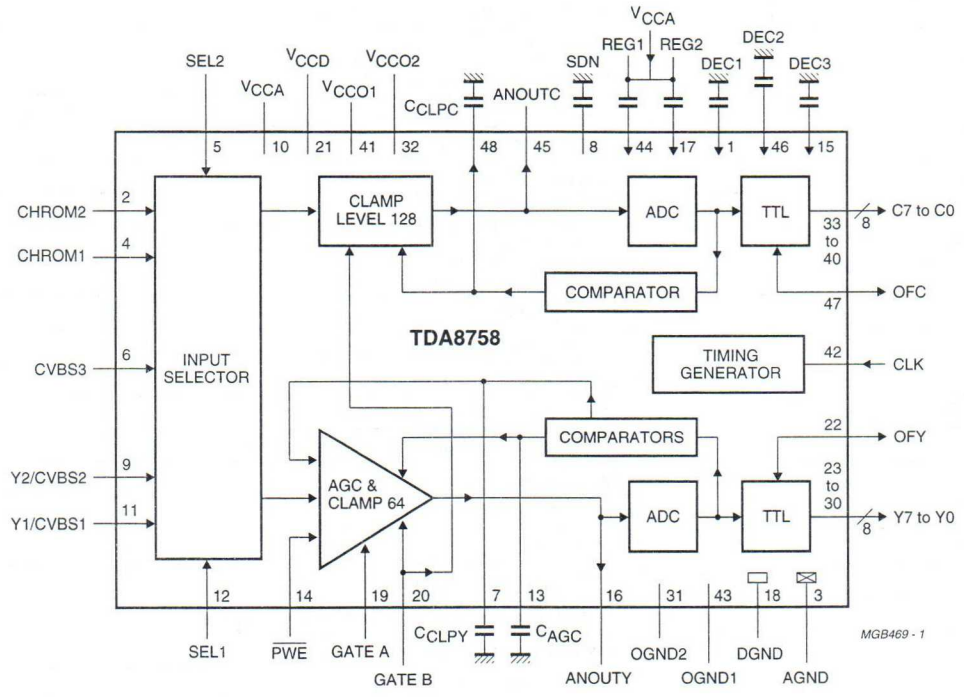


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DEC1	1	decoupling input 1
CHROM2	2	chrominance analog voltage input 2
AGND	3	analog ground
CHROM1	4	chrominance analog voltage input 1
SEL2	5	selection control input 2
CVBS3	6	luminance analog voltage input 3
C_{CLPY}	7	Y channel clamping capacitor
SDN	8	stabilizer decoupling node
Y2/CVBS2	9	luminance analog voltage input 2
V_{CCA}	10	analog supply voltage (+5 V)
Y1/CVBS1	11	luminance analog voltage input 1
SEL1	12	selection control input 1
C_{AGC}	13	AGC capacitor
$\overline{PWE}$	14	peak white enable input (active LOW)
DEC3	15	decoupling input 3
ANOUTY	16	analog output for Y channel
REG2	17	decoupling input 2 (internal stabilization loop decoupling)
DGND	18	digital ground
GATE A	19	AGC control input
GATE B	20	clamp control input
V_{CCD}	21	digital supply voltage (+5 V)
OFY	22	Y channel output format/chip enable (3-state input)
Y7	23	Y channel data output; bit 7 (MSB)
Y6	24	Y channel data output; bit 6
Y5	25	Y channel data output; bit 5
Y4	26	Y channel data output; bit 4
Y3	27	Y channel data output; bit 3
Y2	28	Y channel data output; bit 2
Y1	29	Y channel data output; bit 1
Y0	30	Y channel data output; bit 0 (LSB)
OGND2	31	output ground 2
V_{CCO2}	32	output supply voltage 2 (+5 V)
C7	33	C channel data output; bit 7 (MSB)
C6	34	C channel data output; bit 6
C5	35	C channel data output; bit 5
C4	36	C channel data output; bit 4
C3	37	C channel data output; bit 3
C2	38	C channel data output; bit 2
C1	39	C channel data output; bit 1
C0	40	C channel data output; bit 0 (LSB)

SYMBOL	PIN	DESCRIPTION
V_{CCO1}	41	output supply voltage 1 (+5 V)
CLK	42	clock input
OGND1	43	output ground 1
REG1	44	decoupling input 1 (internal stabilization loop decoupling)
ANOUTC	45	analog output for C channel
DEC2	46	decoupling input 2
OFC	47	C channel output format/chip enable (3-state input)
C_{CLPC}	48	C channel clamping capacitor

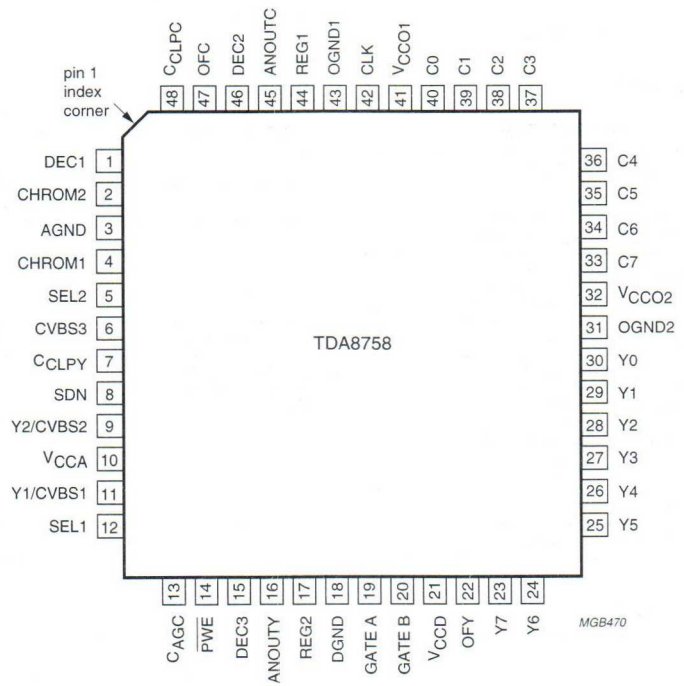


Fig.2 Pin configuration.

10-bit high-speed low-power analog-to-digital converter

TDA8762A

FEATURES

- 10-bit resolution
- Sampling rate up to 80 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 80 MHz)
- No missing codes guaranteed
- In range (IR) TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- ΣΔ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8762A is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
I_{CCA}	analog supply current		–	29	36	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output stages supply current	C_L = 15 pF; ramp input	–	23	30	mA
INL	integral non-linearity	f_{clk} = 80 MHz; ramp input	–	±0.75	±1.5	LSB
DNL	differential non-linearity	f_{clk} = 80 MHz; ramp input	–	±0.3	±0.7	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8762AM/6		60	–	–	MHz
	TDA8762AM/8		80	–	–	MHz
P_{tot}	total power dissipation		–	380	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8762AM/6	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	60
TDA8762AM/8	SSOP28		SOT341-1	80

BLOCK DIAGRAM

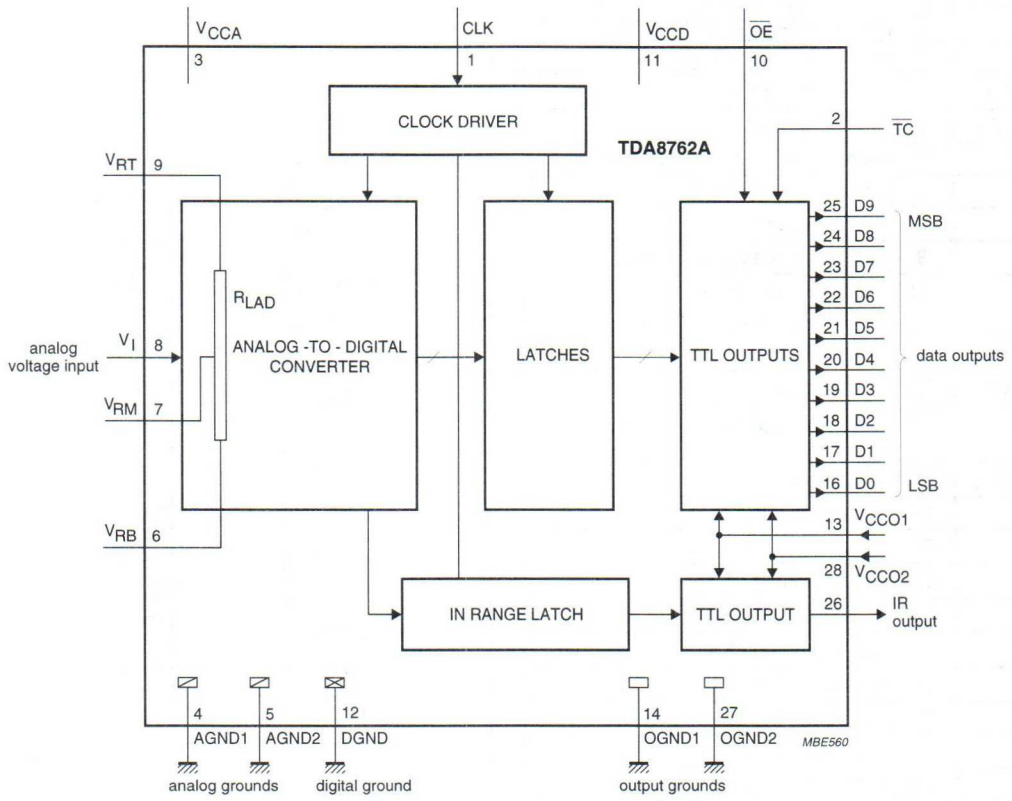


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (TTL level input, active LOW)
V_{CCD}	11	digital supply voltage (5 V)
DGND	12	digital ground
V_{CCO1}	13	supply voltage for output stages 1 (5 V)
OGND1	14	output ground 1
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
V_{CCO2}	28	supply voltage for output stages 2 (5 V)

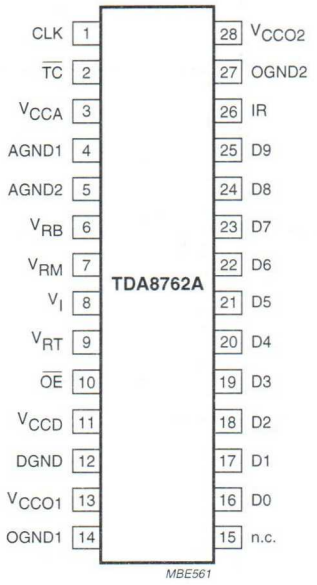


Fig.2 Pin configuration.

10-bit high-speed low-power ADC TDA8763A

FEATURES

- 10-bit resolution
- Sampling rate up to 50 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.4 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz)
- No missing codes guaranteed
- In range (IR) CMOS output
- TTL compatible digital inputs
- 3 to 5 V CMOS digital outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 180 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- ΣΔ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8763A is a 10-bit high-speed low-power analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine-wave clock input signal is allowed.

The device requires an external source to drive its reference ladder. If the application requires that the reference is driven via internal sources the recommendation is to use the TDA8763.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8763AM/3	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	30
TDA8763AM/4	SSOP28		SOT341-1	40
TDA8763AM/5	SSOP28		SOT341-1	50

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	18	24	mA
I_{CCD}	digital supply current		–	16	21	mA
I_{CCO}	output stages supply current	f_{clk} = 40 MHz; ramp input	–	2	4	mA
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.8	±2.0	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.5	±0.9	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8763AM/3		30	–	–	MHz
	TDA8763AM/4		40	–	–	MHz
	TDA8763AM/5		50	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 40 MHz; ramp input	–	180	258	mW

BLOCK DIAGRAM

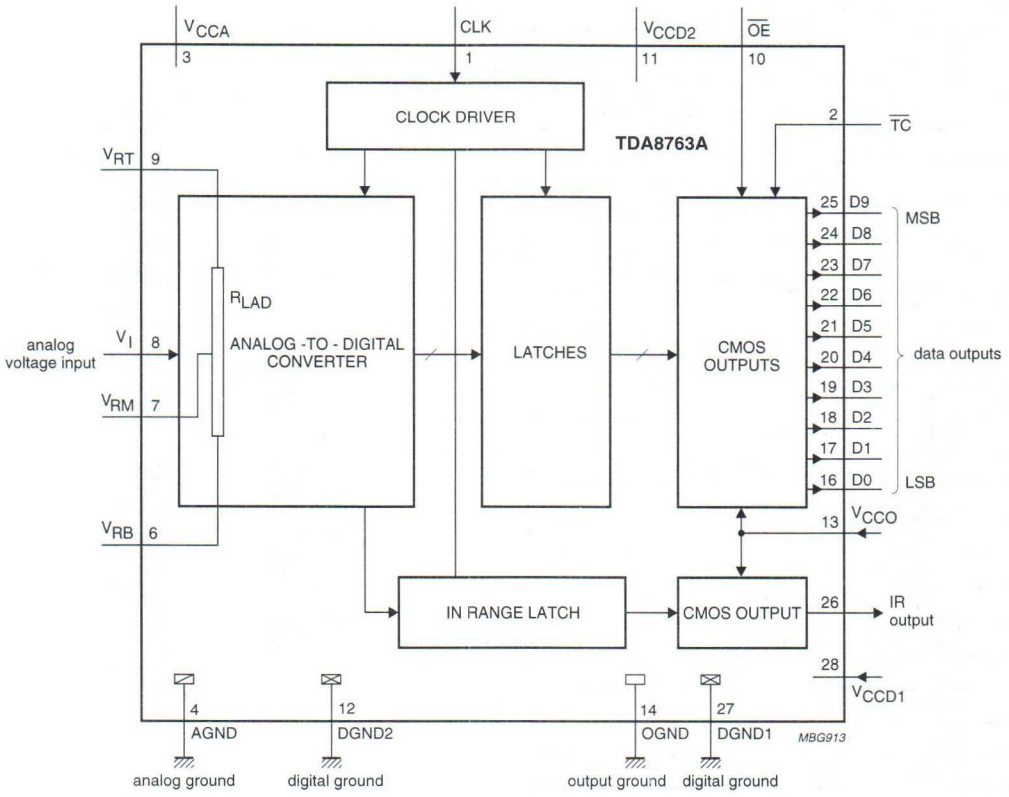


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (+5 V)
AGND	4	analog ground
n.c.	5	not connected
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE input
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (CMOS level input, active LOW)
V_{CCD2}	11	digital supply voltage 2 (+5 V)
DGND2	12	digital ground 2
V_{CCO}	13	supply voltage for output stages (+3 to +5 V)
OGND	14	output ground
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
DGND1	27	digital ground 1
V_{CCD1}	28	digital supply voltage 1 (+5 V)

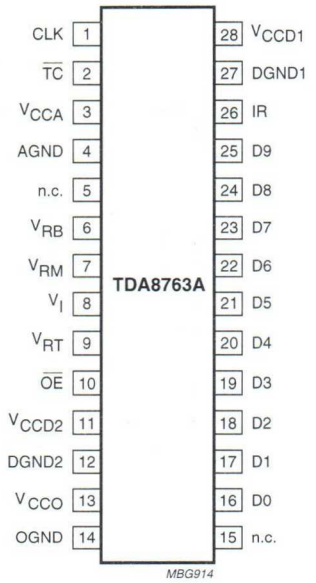


Fig.2 Pin configuration.

10-bit high-speed 2.7 to 5.25 V analog-to-digital converter

TDA8766

FEATURES

- 10-bit resolution
- 2.7 to 5.25 V operation
- Sampling rate up to 20 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 1.0 MHz full-scale input at f_{clk} = 20 MHz)
- In range (IR) CMOS output
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 53 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Standby mode
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

GENERAL DESCRIPTION

The TDA8766 is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts with 2.7 to 5.25 V operation the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 20 MHz. All digital inputs and outputs are CMOS compatible. A standby mode allows reduction of the device power consumption down to 4 mW.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.3	5.25	V
V_{DDD1}	digital supply voltage 1		2.7	3.3	5.25	V
V_{DDD2}	digital supply voltage 2		2.7	3.3	5.25	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.25	V
I_{DDA}	analog supply current		–	7.5	10	mA
I_{DDD}	digital supply current		–	7.5	10	mA
I_{DDO}	output stages supply current	f_{clk} = 20 MHz; C_L = 20 pF; ramp input	–	1	2	mA
INL	integral non-linearity	f_{clk} = 20 MHz; ramp input	–	±1	±2	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; ramp input	–	±0.25	±0.7	LSB
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	–	53	73	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8766G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

BLOCK DIAGRAM

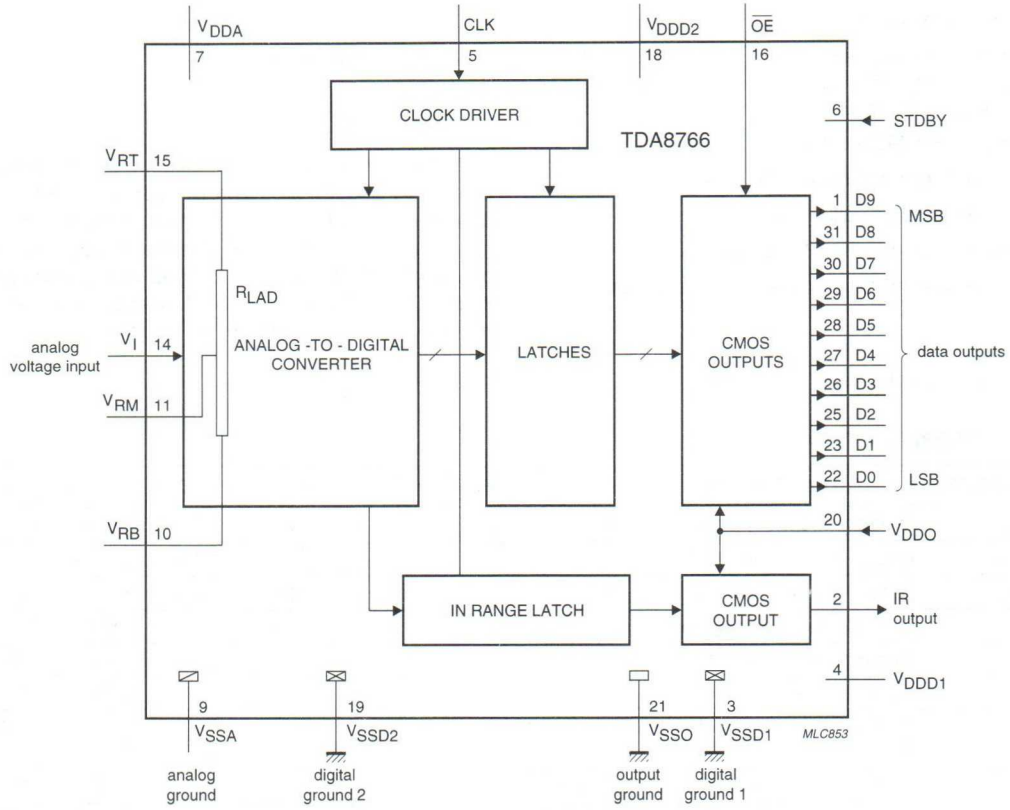


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D9	1	data output; bit 9 (MSB)
IR	2	in range data output
V_{SSD1}	3	digital ground 1
V_{DDD1}	4	digital supply voltage 1 (2.7 to 5.25 V)
CLK	5	clock input
STDBY	6	standby mode input
V_{DDA}	7	analog supply voltage (2.7 to 5.25 V)
n.c.	8	not connected
V_{SSA}	9	analog ground
V_{RB}	10	reference voltage BOTTOM input
V_{RM}	11	reference voltage MIDDLE
n.c.	12	not connected
n.c.	13	not connected
V_I	14	analog input voltage
V_{RT}	15	reference voltage TOP input
$\overline{OE}$	16	output enable input
n.c.	17	not connected

SYMBOL	PIN	DESCRIPTION
V_{DDD2}	18	digital supply voltage 2 (2.7 to 5.25 V)
V_{SSD2}	19	digital ground 2
V_{DDO}	20	positive supply voltage for output stage (2.5 to 5.25 V)
V_{SSO}	21	digital output ground
D0	22	data output; bit 0 (LSB)
D1	23	data output; bit 1
n.c.	24	not connected
D2	25	data output; bit 2
D3	26	data output; bit 3
D4	27	data output; bit 4
D5	28	data output; bit 5
D6	29	data output; bit 6
D7	30	data output; bit 7
D8	31	data output; bit 8
n.c.	32	not connected

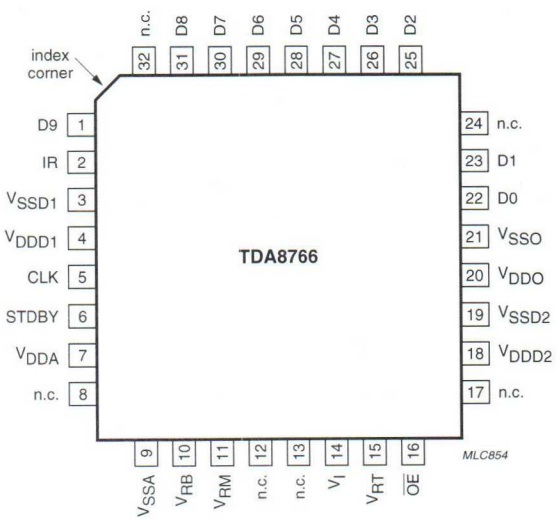


Fig.2 Pin configuration.

12-bit high-speed Analog-to-Digital Converter (ADC)

TDA8767

FEATURES

- 12-bit resolution
- Sampling rate up to 30 MHz
- −3 dB bandwidth of 18 MHz
- No missing codes guaranteed
- 5 V power supplies
- Binary or two's complement CMOS outputs
- In-range CMOS output
- TTL compatible digital inputs
- 3 to 5 V CMOS digital outputs
- TTL compatible clock input; low-level AC allowed
- Power dissipation 335 mW (typ.)
- Low analog input capacitance (typ. 2 pF), no buffer amplifier required
- No external sample-and-hold circuit required
- Differential or single analog Input
- External amplitude range control
- Voltage controlled regulator included.

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Imaging (camera, scanner)
  - Medical imaging
  - Telecommunication
  - Base-station receiver.

GENERAL DESCRIPTION

The TDA8767 is a bipolar 12-bit Analog-to-Digital Converter (ADC) for imaging or other applications. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 30 MHz. All digital inputs and outputs are CMOS compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	40	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output supply current	ramp input	–	12	tbf	mA
ILE	integral non-linearity	f_{clk} = 4 MHz; ramp input	–	±3.0	±4.0	LSB
DLE	differential non-linearity	f_{clk} = 4 MHz; ramp input; no missing codes	–	±0.6	±1	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8767H/1		10	–	–	MHz
	TDA8767H/2		20	–	–	MHz
	TDA8767H/3		30	–	–	MHz
P_{tot}	total power dissipation		–	335	–	mW

12-bit high-speed Analog-to-Digital Converter (ADC) TDA8767

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8767H/1	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	10
TDA8767H/2				20
TDA8767H/3				30

BLOCK DIAGRAM

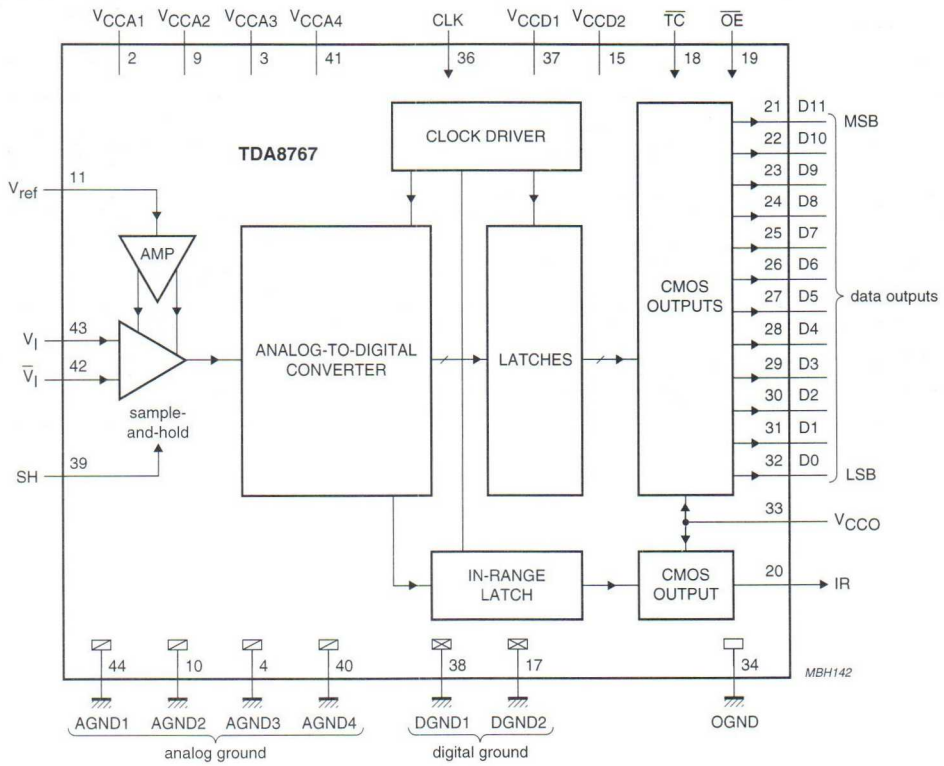


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_{CCA1}	2	analog supply voltage 1 (+5 V)
V_{CCA3}	3	analog supply voltage 3 (+5 V)
AGND3	4	analog ground 3
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
V_{CCA2}	9	analog supply voltage 2 (+5 V)
AGND2	10	analog ground 2
V_{ref}	11	reference voltage
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (+5 V)
n.c.	16	not connected
DGND2	17	digital ground 2
$\overline{TC}$	18	output two's complement
$\overline{OE}$	19	output enable input (CMOS level; active LOW)
IR	20	in-range output
D11	21	data output; bit 11 (MSB)
D10	22	data output; bit 10

SYMBOL	PIN	DESCRIPTION
D9	23	data output; bit 9
D8	24	data output; bit 8
D7	25	data output; bit 7
D6	26	data output; bit 6
D5	27	data output; bit 5
D4	28	data output; bit 4
D3	29	data output; bit 3
D2	30	data output; bit 2
D1	31	data output; bit 1
D0	32	data output; bit 0 (LSB)
V_{CCO}	33	output supply voltage (3 to 5.25 V)
OGND	34	output ground
n.c.	35	not connected
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (+5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (+5 V)
$\overline{V_I}$	42	complementary analog input voltage
V_I	43	analog input voltage
AGND1	44	analog ground 1

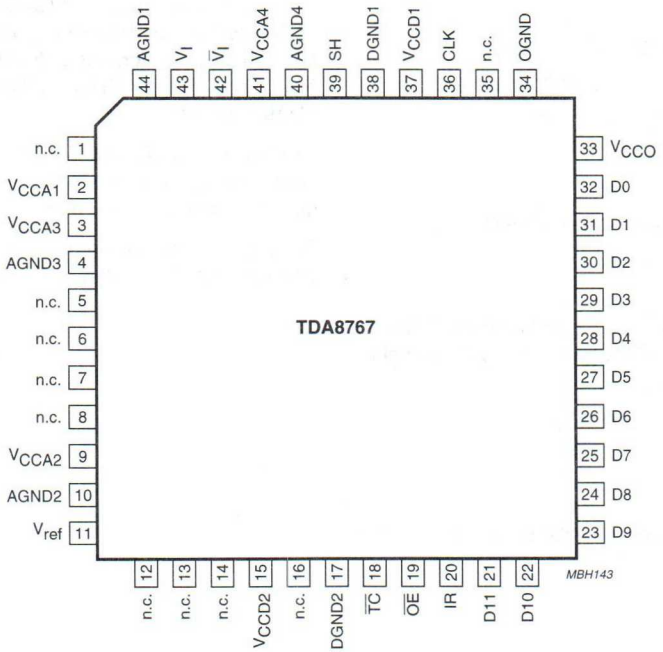


Fig.2 Pin configuration.

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

FEATURES

- 8-bit resolution
- Sampling rate up to
  35 MHz for TDA8772H/3, TDA8772AH/3
  85 MHz for TDA8772H/8, TDA8772AH/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{SYNC}$, $\overline{BLANK}$ control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75 Ω output load
- TDA8772A has $\overline{BLANK}$ control input on the GREEN channel only while TDA8772 has it on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772, TDA8772A are triple 8-bit video digital-to-analog converters (DACs). They convert the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3, TDA8772AH/3) and 85 MHz (TDA8772H/8, TDA8772AH/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3[1]	44	QFP44	plastic	SOT307B	35 MHz
TDA8772AH/3[1]	44	QFP44	plastic	SOT307B	35 MHz
TDA8772H/8[1]	44	QFP44	plastic	SOT307B	85 MHz
TDA8772AH/8[1]	44	QFP44	plastic	SOT307B	85 MHz

Note

1. Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; (SOT307B); SOT307-2; 1996 Oct 29.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 75 Ω; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
INL	integral non-linearity2	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
		f_{clk} = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	±0.5	±0.75	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
P_{tot}	total power dissipation	note 1				
	TDA8772H/3, TDA8772AH/3	R_L = 75 Ω; f_{clk} = 35 MHz	180	360	640	mW
	TDA8772H/8, TDA8772AH/8	R_L = 75 Ω; f_{clk} = 85 MHz	180	405	700	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

BLOCK DIAGRAMS

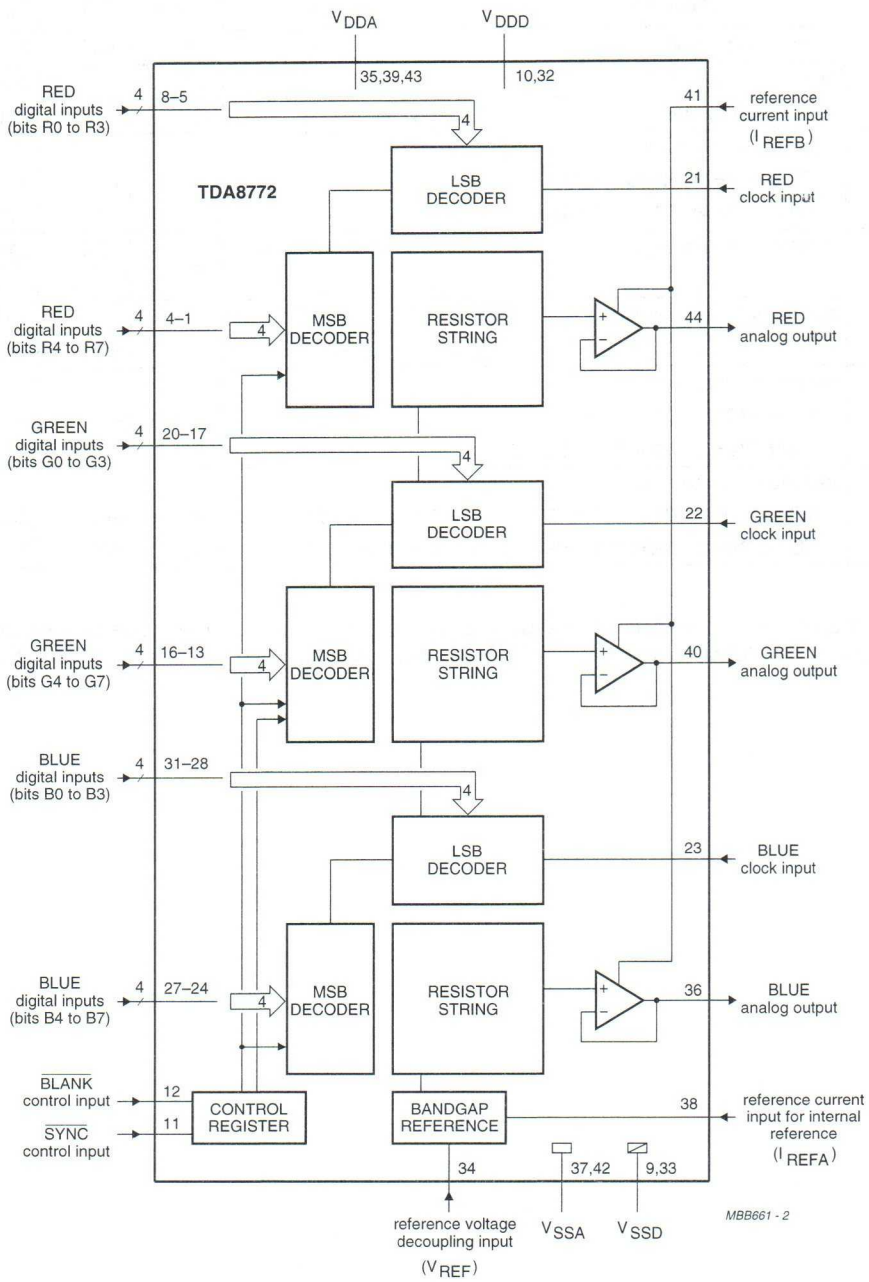


Fig.1 Block diagram for TDA8772.

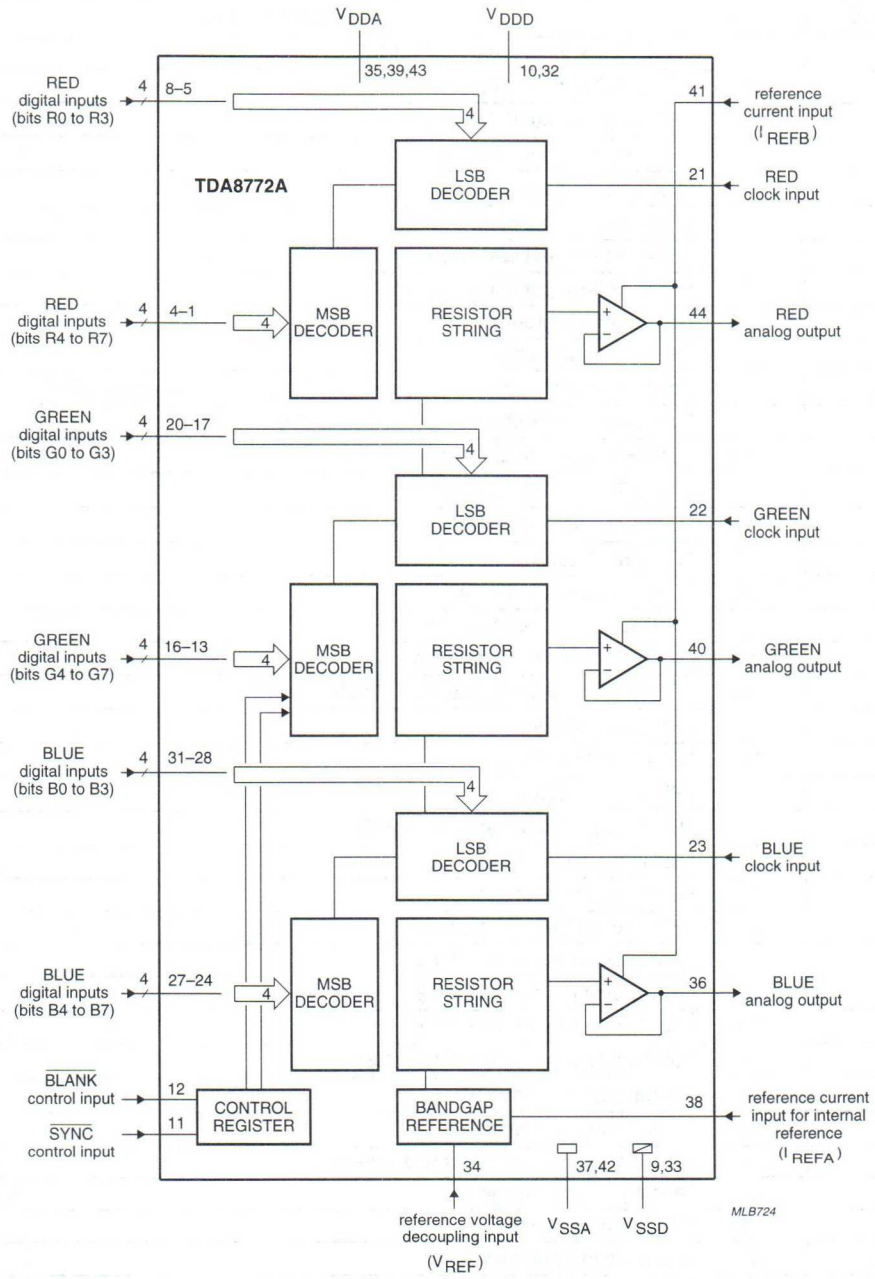


Fig.2 Block diagram for TDA8772A.

PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

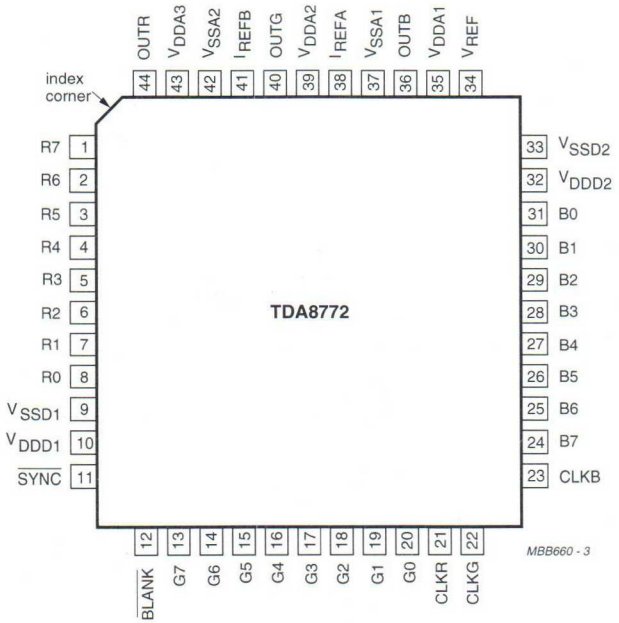


Fig.3 Pin configuration.

Triple 10-bit video Digital-to-Analog Converter (DAC)

TDA8775

FEATURES

- 10-bit resolution
- Sampling rate up to:
  - 50 MHz for normal mode; R_L = 37.5 Ω
  - 35 MHz for LOW power mode; R_L = 150 Ω
- Internal current reference
- Current reference selector for:
  - normal mode, R_L = 37.5 Ω (typ.)
  - low-power mode, R_L = 150 Ω (typ.)
- No deglitching circuit required
- $\overline{SYNC}$ and $\overline{BLANK}$ control inputs
- 0.66 V output voltage range on red and blue channels
- 1 V output voltage range on green channel (including sync)
- $\overline{BLANK}$ control input on the 3 channels
- + 5 V power supply.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8775 consists of three 10-bit video Digital-to-Analog Converters (DACs). They convert the digital input signals into current outputs at a maximum conversion rate of 50 MHz.

The DACs are based on current source architecture with selectable current reference.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	SLT = 1; R_L = 37.5 Ω	–	67	tbf	mA
		SLT = 0; R_L = 150 Ω	–	16	tbf	mA
I_{DDD}	digital supply current	SLT = 1; R_L = 37.5 Ω	–	15	tbf	mA
		SLT = 0; R_L = 150 Ω	–	10	tbf	mA
INL	DC integral non-linearity		–	±1	±2	LSB
DNL	DC differential non-linearity		–	±0.7	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency	SLT = 1; R_L = 37.5 Ω	50	–	–	MHz
		SLT = 0; R_L = 150 Ω	35	–	–	MHz
P_{tot}	total power dissipation	SLT = 1; R_L = 37.5 Ω; f_{clk} = 50 MHz	–	410	tbf	mW
		SLT = 0; R_L = 150 Ω; f_{clk} = 35 MHz	–	130	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8775G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

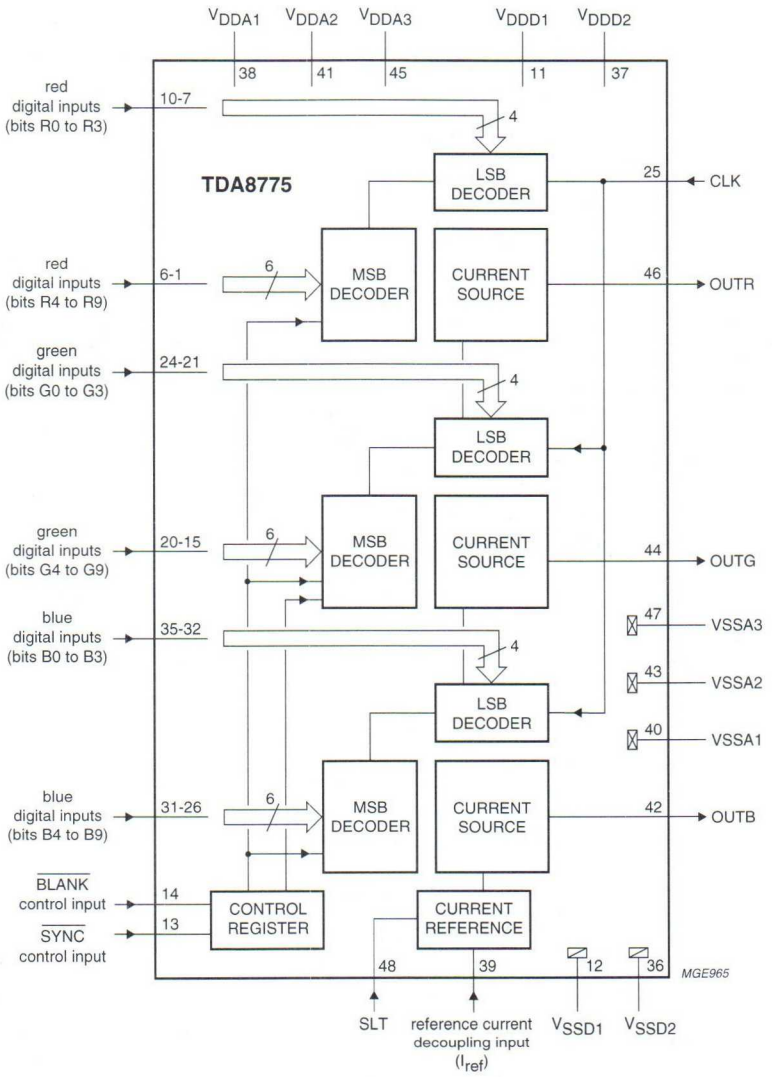


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
R9	1	red digital input data; bit 9 (MSB)
R8	2	red digital input data; bit 8
R7	3	red digital input data; bit 7
R6	4	red digital input data; bit 6
R5	5	red digital input data; bit 5
R4	6	red digital input data; bit 4
R3	7	red digital input data; bit 3
R2	8	red digital input data; bit 2
R1	9	red digital input data; bit 1
R0	10	red digital input data; bit 0 (LSB)
V_{DDD1}	11	digital supply voltage 1
V_{SSD1}	12	digital supply ground 1
$\overline{SYNC}$	13	composite sync control input; for green channel only (active LOW)
$\overline{BLANK}$	14	composite blank control input (active LOW)
G9	15	green digital input data; bit 9 (MSB)
G8	16	green digital input data; bit 8
G7	17	green digital input data; bit 7
G6	18	green digital input data; bit 6
G5	19	green digital input data; bit 5
G4	20	green digital input data; bit 4
G3	21	green digital input data; bit 3
G2	22	green digital input data; bit 2
G1	23	green digital input data; bit 1
G0	24	green digital input data; bit 0 (LSB)
CLK	25	clock input
B9	26	blue digital input data; bit 9 (MSB)
B8	27	blue digital input data; bit 8
B7	28	blue digital input data; bit 7
B6	29	blue digital input data; bit 6
B5	30	blue digital input data; bit 5
B4	31	blue digital input data; bit 4
B3	32	blue digital input data; bit 3
B2	33	blue digital input data; bit 2
B1	34	blue digital input data; bit 1
B0	35	blue digital input data; bit 0 (LSB)
V_{SSD2}	36	digital supply ground 2
V_{DDD2}	37	digital supply voltage 2
V_{DDA1}	38	analog supply voltage 1
I_{ref}	39	decoupling pin for reference current
V_{SSA1}	40	analog supply ground 1

SYMBOL	PIN	DESCRIPTION
V_{DDA2}	41	analog supply voltage 2
OUTB	42	blue analog output
V_{SSA2}	43	analog supply ground 2
OUTG	44	green analog output
V_{DDA3}	45	analog supply voltage 3
OUTR	46	red analog output
V_{SSA3}	47	analog supply ground 3
SLT	48	mode selection; normal mode, R_L = 37.5 Ω (active HIGH); low power mode, R_L = 150 Ω (active LOW)

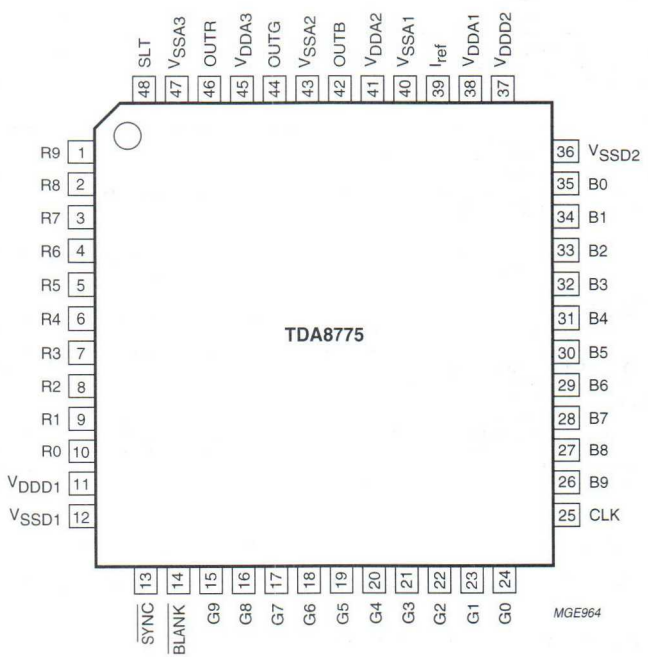


Fig.2 Pin configuration.

10-bit, 1000 Msps Digital-to-Analog Converter (DAC)

TDA8776A

FEATURES

- 10-bit resolution
- Conversion rate up to 1000 MHz
- 10K/100K ECL input levels
- Internal reference voltage generator
- No deglitching circuit required
- Internal input register
- Power dissipation only 925 mW (typical)
- Internal 50 Ω output load (connected to the analog ground)
- Very few external components required.

APPLICATIONS

High-speed digital-to-analog conversion for:

- High resolution video and graphics
- Direct digital synthesis (DDS)
- Telecommunication
- High-speed modems.

GENERAL DESCRIPTION

The TDA8776A is a 10-bit Digital-to-Analog Converter (DAC) for high resolution video and other high frequency applications. It converts the digital input signal into an analog output voltage at a maximum conversion rate of 1000 Msps. No external reference voltage is required and all digital inputs are 10K/100K-ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−5.46	−5.20	−4.94	V
V_{EED}	digital supply voltage		−5.46	−5.20	−4.94	V
V_{EEI}	input stages digital supply voltage	note 1	−5.46	−5.20	−4.94	V
I_{EEA}	analog supply current	note 1	–	108	145	mA
I_{EED}	digital supply current	note 1	–	60	85	mA
I_{EEI}	input stages digital supply current	note 1	–	10	15	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	notes 1 and 2; Z_L = 50 Ω	1.7	2.0	2.5	V
INL	DC integral non-linearity	note 3	–	±0.3	±0.5	LSB
DNL	DC differential non-linearity	note 3	–	±0.2	±0.45	LSB
$f_{clk(max)}$	maximum clock frequency		1000	–	–	MHz
t_{S1}	settling time (differential)	10% to 90% full scale; Fig.9	–	0.5	–	ns
P_{tot}	total power dissipation		–	925	–	mW

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{CLK}$ is LOW.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω.
3. A warm-up time is necessary to reach optimal performances.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8776AK	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2

BLOCK DIAGRAM

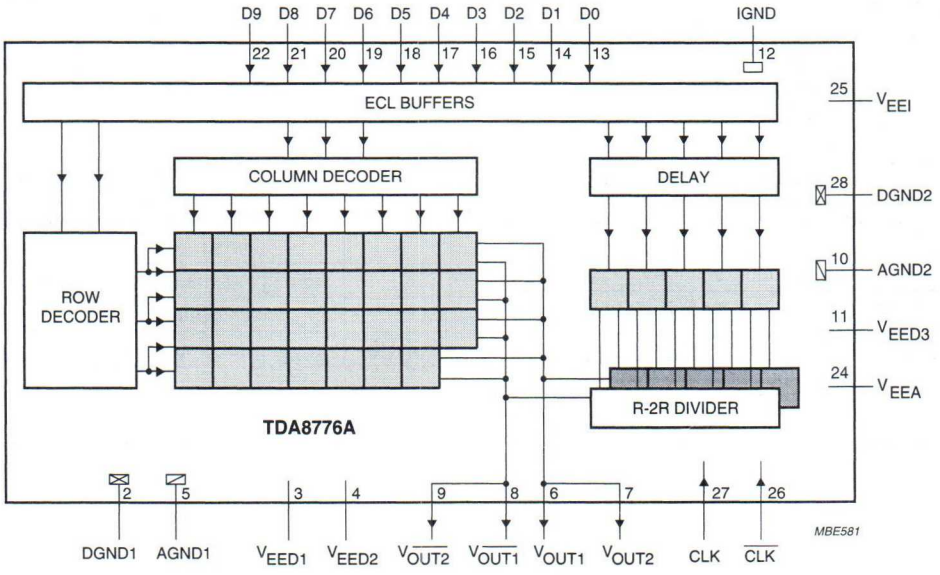


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DGND1	2	digital ground 1
V_{EED1}	3	digital supply voltage 1 (−5.2 V)
V_{EED2}	4	digital supply voltage 2 (−5.2 V)
AGND1	5	analog ground 1
V_{OUT1}	6	analog voltage output 1
V_{OUT2}	7	analog voltage output 2
$V_{\overline{OUT1}}$	8	complementary analog voltage output 1
$V_{\overline{OUT2}}$	9	complementary analog voltage output 2
AGND2	10	analog ground 2
V_{EED3}	11	digital supply voltage 3 (−5.2 V)
IGND	12	input ground for ECL input buffers
D0	13	data input; bit 0 (LSB)
D1	14	data input; bit 1

SYMBOL	PIN	DESCRIPTION
D2	15	data input; bit 2
D3	16	data input; bit 3
D4	17	data input; bit 4
D5	18	data input; bit 5
D6	19	data input; bit 6
D7	20	data input; bit 7
D8	21	data input; bit 8
D9	22	data input; bit 9 (MSB)
n.c.	23	not connected
V_{EEA}	24	analog supply voltage (−5.2 V)
V_{EEI}	25	input supply voltage for ECL input buffers (−5.2 V)
$\overline{CLK}$	26	complementary clock input
CLK	27	clock input
DGND2	28	digital ground 2

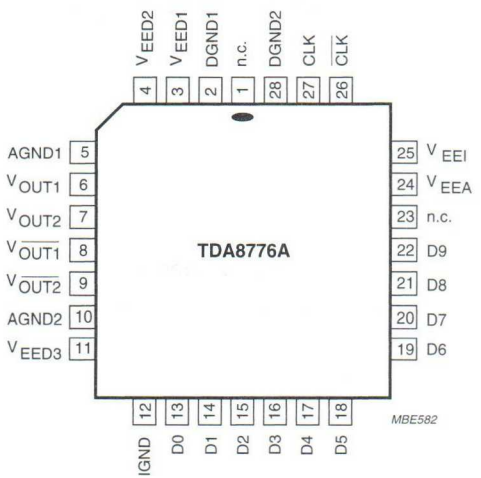


Fig.2 Pin configuration.

10-bit converter interface (ADC/DAC) for quadrature transceiver

TDA8779

FEATURES

- Two 10-bit ADCs with multiplexed outputs
- Two 10-bit DACs with multiplexed inputs
- Sampling rate for the ADCs and DACs up to 20 MHz
- Digital outputs (for the ADC) and inputs (for the DAC) are TTL/CMOS compatible (2.7 to 5.5 V)
- Internal reference voltage regulator
- Power dissipation 520 mW
- Standby mode.

APPLICATIONS

Wireless communication.

GENERAL DESCRIPTION

The TDA8779 contains two 10-bit high speed ADCs and two 10-bit DACs for wireless communication (for use in transceiver modules). This device converts two analog input signals (channels I and Q) and digital inputs (D0 to D9) at a maximum sampling rate of 20 MHz. The input bias voltages for the analog input voltages are provided internally at the middle code. The analog input and output voltages are AC coupled.

The data sampling is performed on the rising edge of the clock for ADCs and DACs.

All reference voltages are generated internally.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCD1}	digital supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCA2}	analog supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCD2}	digital supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCO}	output stage supply voltage		2.7	3.0	5.5	V
I_{CCA}	analog supply current		–	71	–	mA
I_{CCD}	digital supply current		–	31	–	mA
I_{CCO}	output stage supply current	ramp input; f_{CLK} = 20 MHz	–	2	–	mA
$f_{CLK(ADC)max}$	maximum clock frequency for the ADC part		20	–	–	MHz
INLA	integral non linearity for the ADC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±2	–	LSB
DNLA	differential non linearity for the ADC part	50% full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.3	–	LSB
$f_{CLK(DAC)max}$	maximum clock frequency for the DAC part		20	–	–	MHz
INLD	integral non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±2	–	LSB
DNLD	differential non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.75	–	LSB
P_{tot}	total power dissipation		–	520	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8779H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

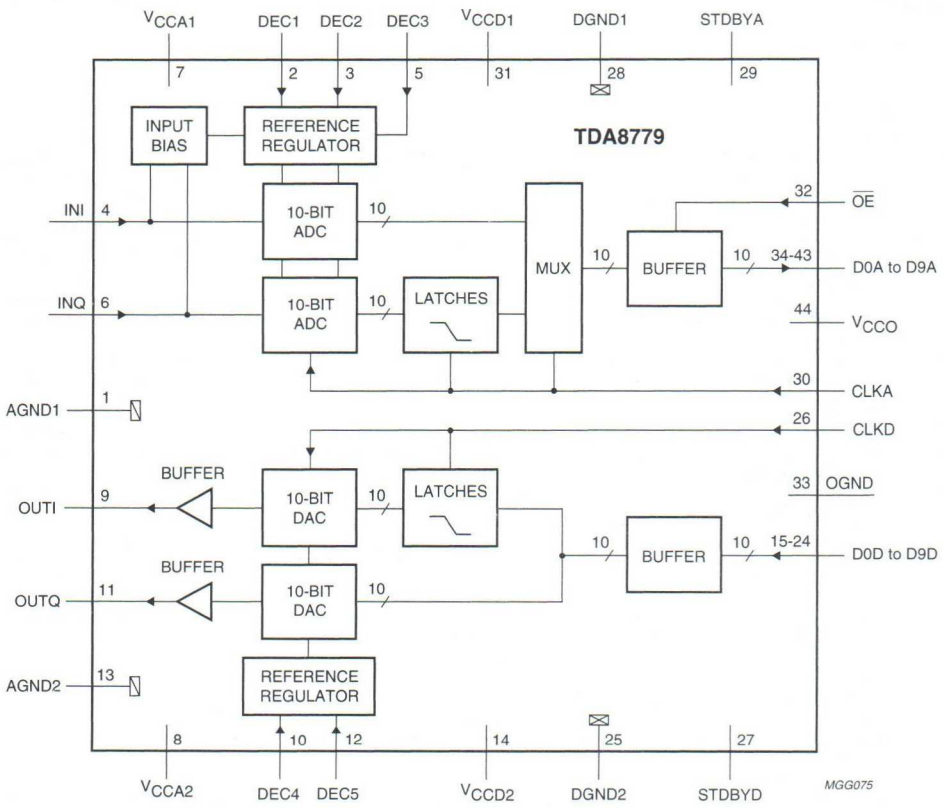


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGND1	1	analog ground 1
DEC1	2	decoupling input 1
DEC2	3	decoupling input 2
INI	4	I channel ADC input
DEC3	5	decoupling input 3
INQ	6	Q channel ADC input
V_{CCA1}	7	analog supply voltage 1 for ADC part (+5 V)
V_{CCA2}	8	analog supply voltage 2 for DAC part (+5 V)
OUTI	9	I channel DAC analog output
DEC4	10	decoupling input 4
OUTQ	11	Q channel DAC analog output
DEC5	12	decoupling input 5
AGND2	13	analog ground 2
V_{CCD2}	14	digital supply voltage 2 for DAC part (+5 V)
D0D	15	multiplexed input for the DACs; bit 0
D1D	16	multiplexed input for the DACs; bit 1
D2D	17	multiplexed input for the DACs; bit 2
D3D	18	multiplexed input for the DACs; bit 3
D4D	19	multiplexed input for the DACs; bit 4
D5D	20	multiplexed input for the DACs; bit 5
D6D	21	multiplexed input for the DACs; bit 6
D7D	22	multiplexed input for the DACs; bit 7
D8D	23	multiplexed input for the DACs; bit 8

SYMBOL	PIN	DESCRIPTION
D9D	24	multiplexed input for the DACs; bit 9
DGND2	25	digital ground 2
CLKD	26	transmission block clock
STDBYD	27	power standby for the DAC part (active HIGH)
DGND1	28	digital ground 1
STDBYA	29	power standby for the ADC part (active HIGH)
CLKA	30	reception block clock
V_{CCD1}	31	digital supply voltage 1 for ADC part (+5 V)
$\overline{OE}$	32	ADCs digital output enable (3-state output); (active LOW)
OGND	33	input/output ground
D0A	34	I and Q digital outputs; bit 0
D1A	35	I and Q digital outputs; bit 1
D2A	36	I and Q digital outputs; bit 2
D3A	37	I and Q digital outputs; bit 3
D4A	38	I and Q digital outputs; bit 4
D5A	39	I and Q digital outputs; bit 5
D6A	40	I and Q digital outputs; bit 6
D7A	41	I and Q digital outputs; bit 7
D8A	42	I and Q digital outputs; bit 8
D9A	43	I and Q digital outputs; bit 9
V_{CCO}	44	output supply voltage (2.7 to 5.5 V)

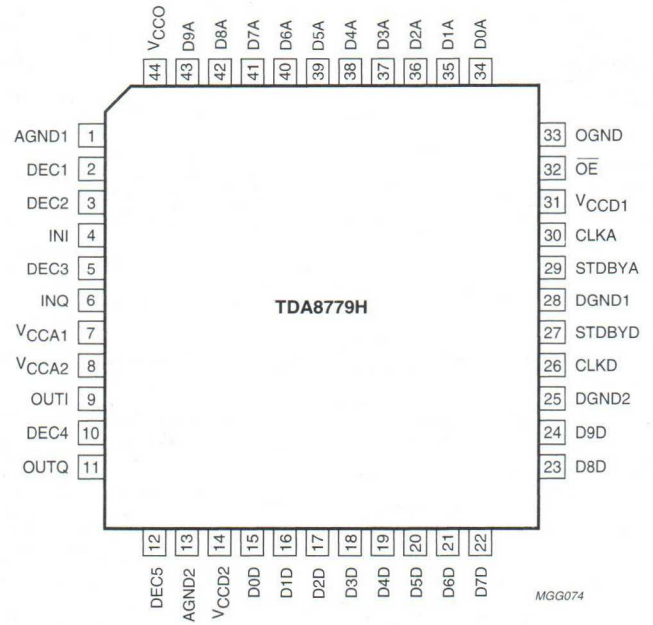


Fig.2 Pin configuration.

10-bit analog-to-digital interface for CCD cameras

TDA8786; TDA8786A

FEATURES

- Correlated double sampling (CDS), AGC, soft clipper, pre-blanking, 10-bit ADC and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 3.5 dB to 33.5 dB (in 0.1 dB steps)
- Programmable soft clipper for white compression (starting at 40% of the input signal)
- Stand-by mode available for each block for power saving applications (14 mW)
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 400 mW (typ.)
- 5 V operation and 2.5 to 5 V operation for the digital outputs
- Active control pulse: TDA8786 = HIGH; TDA8786A = LOW
- TTL compatible inputs, TTL and CMOS compatible outputs.

GENERAL DESCRIPTION

The TDA8786; TDA8786A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC, a soft clipper circuit and a low power 10-bit analog-to-digital converter (ADC) together with its reference voltage regulator.

The AGC and soft clipper circuits are controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

A pre-blanking function is also included.

An additional DAC is provided for additional system controls; its output voltage range is 1.4 V (p-p) which is available at pin OFD.

APPLICATIONS

- CCD camera systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	73	–	mA
I_{CCD}	digital supply current		–	20	–	mA
I_{CCO}	digital outputs supply current	f_{CLK} = 18 MHz; C_L = 20 pF; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{iCDS(p-p)}$	CDS input voltage (peak-to-peak value)		–	400	1200	mV
G_{CDS}	CDS output amplifier gain		–	6	–	dB
$f_{ss(max)}$	maximum clock frequency		18	–	–	MHz
AGC_{dyn}	AGC dynamic range		–	30	–	dB
S/N	total signal-to-noise ratio from CDS input to ADC output	CDS input = 600 mV (p-p)	–	55	–	dB
P_{tot}	total power consumption		–	440	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8786	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA8786A			

BLOCK DIAGRAM

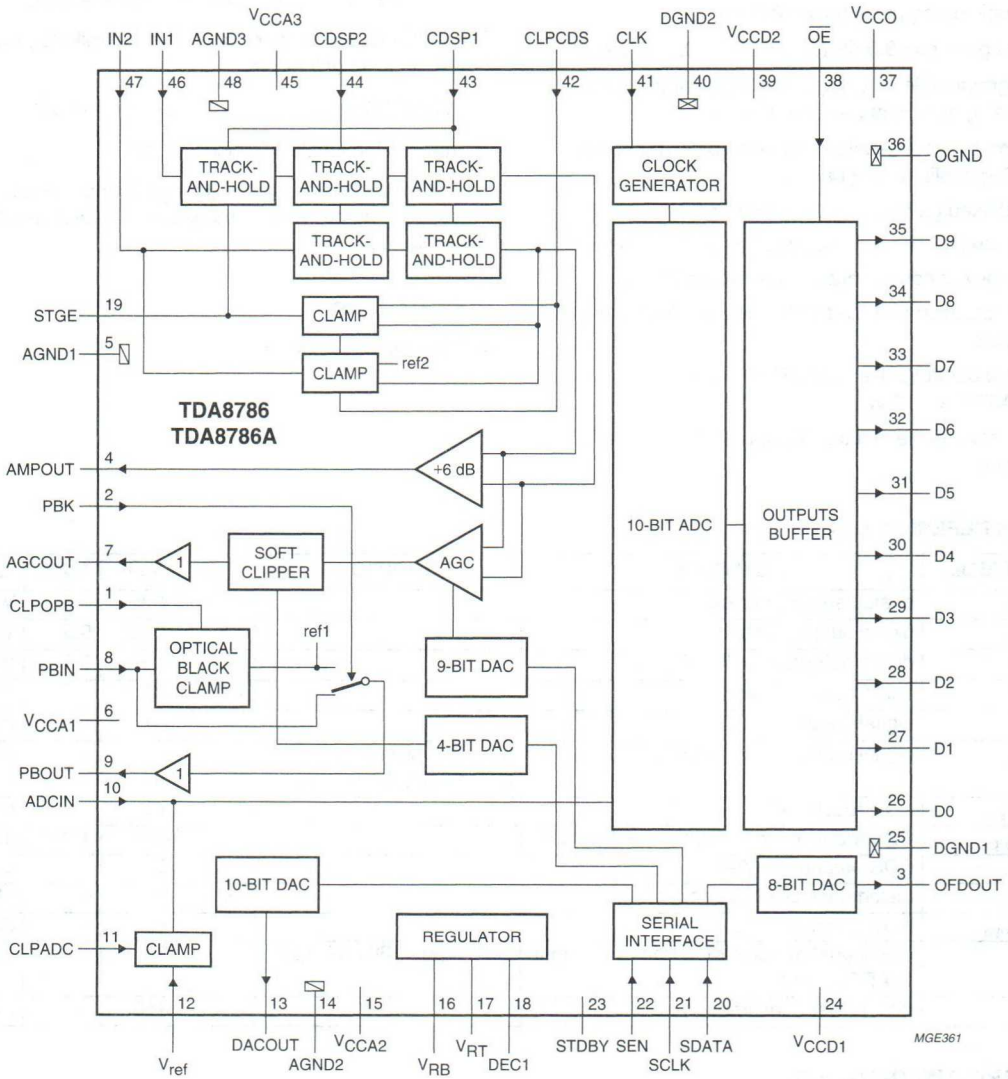


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLPOPB	1	optical black clamp control pulse input (active HIGH for TDA8786, active LOW for TDA8786A)
PBK	2	pre-blanking control pulse input; if PBK is HIGH (LOW) the signal is replaced by the optical black level for TDA8786 (TDA8786A)
OFDOUT	3	analog output of the additional 8-bit control DAC (controlled via the serial interface)
AMPOUT	4	CDS amplifier output (fixed gain = +6 dB)
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGCOUT	7	AGC and soft clipper amplifier signal output
PBIN	8	optical black clamp and pre-blanking block signal input (from AGCOUT via a capacitor)
PBOUT	9	optical black clamp and pre-blanking block signal output
ADCIN	10	ADC analog signal input (from PBOUT or AGCOUT via a capacitor)
CLPADC	11	clamp control input for ADC analog input signal clamp (active HIGH for TDA8786 and active LOW for TDA8786A)
V_{ref}	12	ADC input clamp reference voltage (normally connected to pin VRB or DACOUT)
DACOUT	13	DAC output for ADC clamp level
AGND2	14	analog ground 2
V_{CCA2}	15	analog supply voltage 2
V_{RB}	16	ADC reference voltage (BOTTOM) code 0
V_{RT}	17	ADC reference voltage (TOP) code 1023
DEC1	18	decoupling 1 (decoupled to ground via a capacitor)
STGE	19	CDS offset storage
SDATA	20	serial data input for the 4 control DACs (9-bit DAC for AGC gain, 4-bit DAC for soft clipper; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the stand-by mode per block; see Table 1)
SCLK	21	serial clock input for the control DACs and their serial interface; see Table 1
SEN	22	enable input for the serial interface shift register (active when SEN = logic 0); see Table 1
STDBY	23	stand-by control pin (active HIGH); all the output bits are logic 0 when stand-by is enabled
V_{CCD1}	24	digital supply voltage 1
DGND1	25	digital ground 1
D0	26	ADC digital output 0 (LSB)
D1	27	ADC digital output 1
D2	28	ADC digital output 2
D3	29	ADC digital output 3
D4	30	ADC digital output 4
D5	31	ADC digital output 5
D6	32	ADC digital output 6
D7	33	ADC digital output 7
D8	34	ADC digital output 8
D9	35	ADC digital output 9 (MSB)
OGND	36	digital output ground

SYMBOL	PIN	DESCRIPTION
V_{CCO}	37	digital output supply voltage
$\overline{OE}$	38	output enable (LOW: digital outputs active; HIGH: digital outputs high impedance)
V_{CCD2}	39	digital supply voltage 2
DGND2	40	digital ground 2
CLK	41	ADC clock input
CLPCDS	42	CDS clamp control input (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP1	43	CDS control pulse input 1 (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP2	44	CDS control pulse input 2 (active HIGH for TDA8786; active LOW for TDA8786A)
V_{CCA3}	45	analog supply voltage 3
IN1	46	input signal 1 from CCD (usually black channel)
IN2	47	input signal 2 from CCD (usually video channel)
AGND3	48	analog ground 3

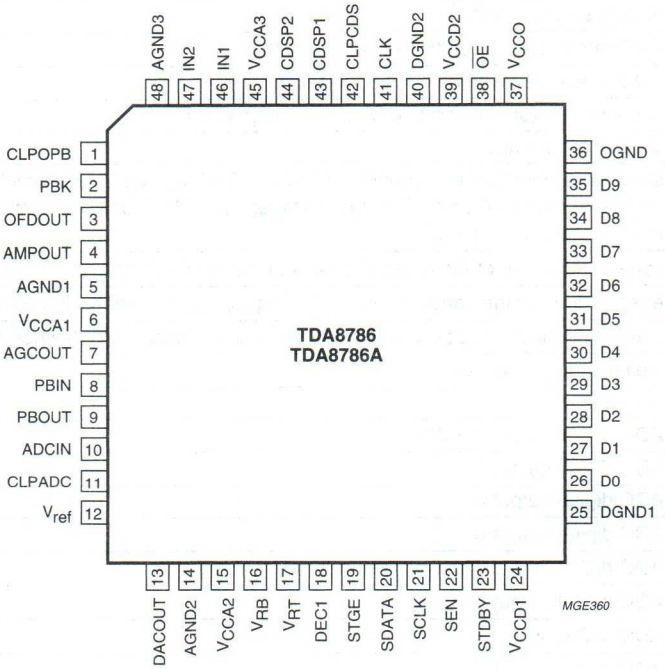


Fig.2 Pin configuration.

8-bit, 40 Msps 2.7 to 5.5 V universal analog-to-digital converter

TDA8790

FEATURES

- 8-bit resolution
- Operation between 2.7 and 5.5 V
- Sampling rate up to 40 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (7.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz)
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 30 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Sleep mode (4 mW)
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

GENERAL DESCRIPTION

The TDA8790 is an 8-bit universal analog-to-digital converter (ADC) for video and general purpose applications. It converts the analog input signal from 2.7 to 5.5 V into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are CMOS/TTL compatible. A sleep mode allows reduction of the device power consumption down to 4 mW.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.3	5.5	V
V_{DDD}	digital supply voltage		2.7	3.3	5.5	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.5	V
ΔV_{DD}	supply voltage difference					
	$V_{DDA} - V_{DDD}$		−0.2	–	+0.2	V
	$V_{DDD} - V_{DDO}$		−0.2	–	+2.25	V
I_{DDA}	analog supply current		–	4	6	mA
I_{DDD}	digital supply current		–	5	8	mA
I_{DDO}	output stages supply current	f_{clk} = 40 MHz; C_L = 20 pF; ramp input	–	1	2	mA
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.5	±0.75	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.25	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	–	30	53	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8790M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

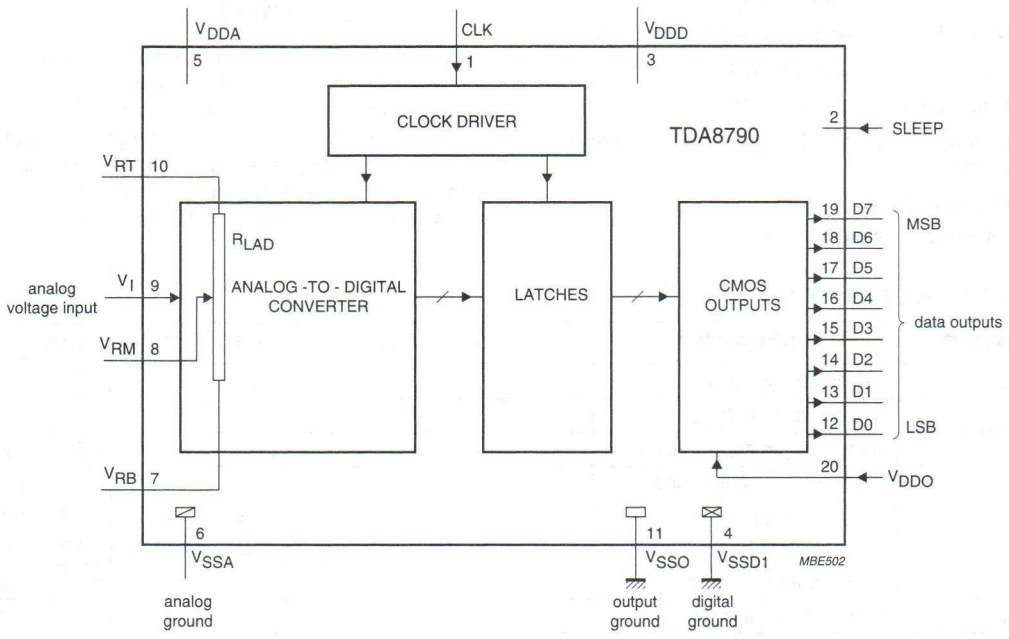


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
SLEEP	2	sleep mode input
V_{DDD}	3	digital supply voltage (2.7 to 5.5 V)
V_{SSD}	4	digital ground
V_{DDA}	5	analog supply voltage (2.7 to 5.5 V)
V_{SSA}	6	analog ground
V_{RB}	7	reference voltage BOTTOM input
V_{RM}	8	reference voltage MIDDLE
V_I	9	analog input voltage
V_{RT}	10	reference voltage TOP input
V_{SSO}	11	digital output ground
D0	12	data output; bit 0 (LSB)
D1	13	data output; bit 1
D2	14	data output; bit 2
D3	15	data output; bit 3
D4	16	data output; bit 4
D5	17	data output; bit 5
D6	18	data output; bit 6
D7	19	data output; bit 7 (MSB)
V_{DDO}	20	positive supply voltage for output stage (2.7 to 5.5 V)

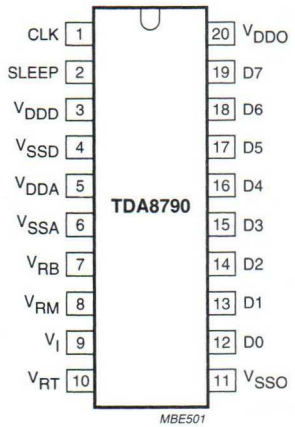


Fig.2 Pin configuration.

PAL/NTSC/SECAM decoder/sync processor TDA9160

FEATURES

- Multistandard PAL, NTSC and SECAM
- I²C-bus controlled
- I²C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Horizontal and vertical drive output
- East-West correction drive output
- Two CVBS inputs
- S-VHS input
- Vertical divider system
- H_A synchronization pulse
- Two level sandcastle pulse

GENERAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/processor. The device contains horizontal and vertical drive outputs and an east-west correction drive circuit. The TDA9160 has been designed for use with baseband chrominance delay lines and DC-coupled vertical and east-west output circuits.

The device has three inputs, two for CVBS and one for S-VHS. The main signal is available at the luminance and colour difference outputs and, also, at the TXT output (unprocessed). The signal at the PIP output can be selected independently from the main signal.

The circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an east-west drive current for the EW output stage. These signals can be used to provide geometry correction of the picture. A two level sandcastle pulse and an H_A pulse are made available for synchronization purposes .The I²C-bus address of the TDA9160 can be programmed by hardware.

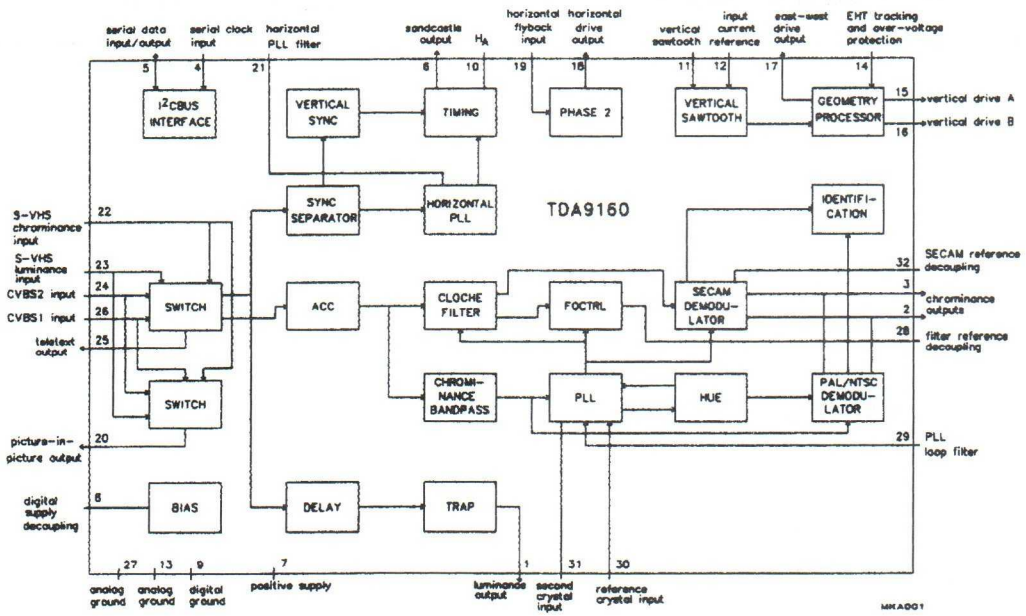


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
$V_{24,26(p-p)}$	CVBS input voltage (peak-to-peak value)		–	1.0	–	V
$V_{23(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)		–	1.0	–	V
$V_{22(p-p)}$	S-VHS chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
$V_{1(p-p)}$	luminance output voltage (peak-to-peak value)		–	0.45	–	V
$V_{25(p-p)}$	teletext output voltage (peak-to-peak value)		–	1.0	–	V
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	PAL/NTSC	–	525	–	mV
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	SECAM	–	1.05	–	V
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	PAL/NTSC	–	665	–	mV
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	SECAM	–	1.33	–	V
V_{10}	H_A output voltage		–	5.0	–	V
$I_{15,16(p-p)}$	vertical drive output current (peak-to-peak value)		–	1	–	mA
I_{18}	horizontal drive output current		–	–	10	mA
I_{17}	EW drive output current		–	–	0.9	mA
V_6	sandcastle clamping voltage level		–	4.5	–	V
V_6	sandcastle blanking voltage level		–	2.5	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9160	32	SDIL	plastic	SOT232(1)

Note

1. SOT232-1; 1996 December 2.

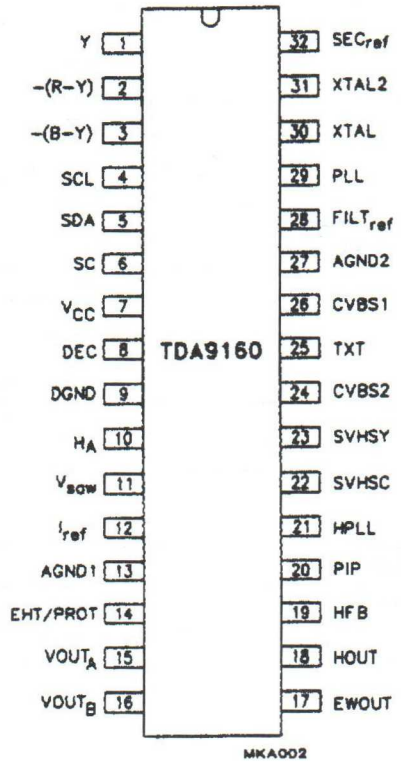


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
Y	1	luminance output
−(R-Y)	2	chrominance output
−(B-Y)	3	chrominance output
SCL	4	serial clock input
SDA	5	serial data input/output
SC	6	sandcastle output
V_{CC}	7	positive supply input
DEC	8	positive supply decoupling
DGND	9	digital ground
H_A	10	horizontal acquisition synchronization pulse
V_{saw}	11	vertical sawtooth
I_{ref}	12	input current reference
AGND1	13	analog ground
EHT/PROT	14	EHT tracking and over-voltage protection
$VOUT_A$	15	vertical drive output A
$VOUT_B$	16	vertical drive output B
EWOUT	17	east-west drive output
HOUT	18	horizontal drive output
HFB	19	horizontal flyback input
PIP	20	picture-in-picture output
HPLL	21	horizontal PLL filter
SVHSC	22	S-VHS chrominance input
SVHSY	23	S-VHS luminance input
CVBS2	24	CVBS2 input
TXT	25	teletext output
CVBS1	26	CVBS1 input
AGND2	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
PLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

YUV picture improvement processor based on histogram modification

TDA9170

FEATURES

- Picture content dependent non-linear Y and U, V processing by histogram analysis
- Adaptive and variable gamma correction controls
- Black and white stretch capabilities
- Transparent I²C-bus control
- On-chip window generator for valid histogram measurement and black detection.

GENERAL DESCRIPTION

The TDA9170 is a transparent analog video processor with a YUV interface. It offers three main luminance processing functions any combination of which can be selected.

The luminance transfer is controlled in a non-linear manner by the distribution (in 5 discrete histogram sections) of the luminance values measured in a picture. As a result, the contrast ratio of the most important parts of the picture will be improved.

Black restoration is available in the event of a set-up in the luminance signal. A variable gamma function, after the histogram conversion, offers the possibility of excellent brightness control.

To maintain a proper colour reproduction, the saturation of the U and V colour difference signals are controlled as a function of the actual non-linearity in the luminance channel.

The TDA9170 concept has maximum flexibility with the optional on-board I²C-bus (including hardwired address select) and window control. The supply voltage is 8 V. The device is mounted in a 32 pin SDIP envelope.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9170	SDIP32	plastic shrink in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

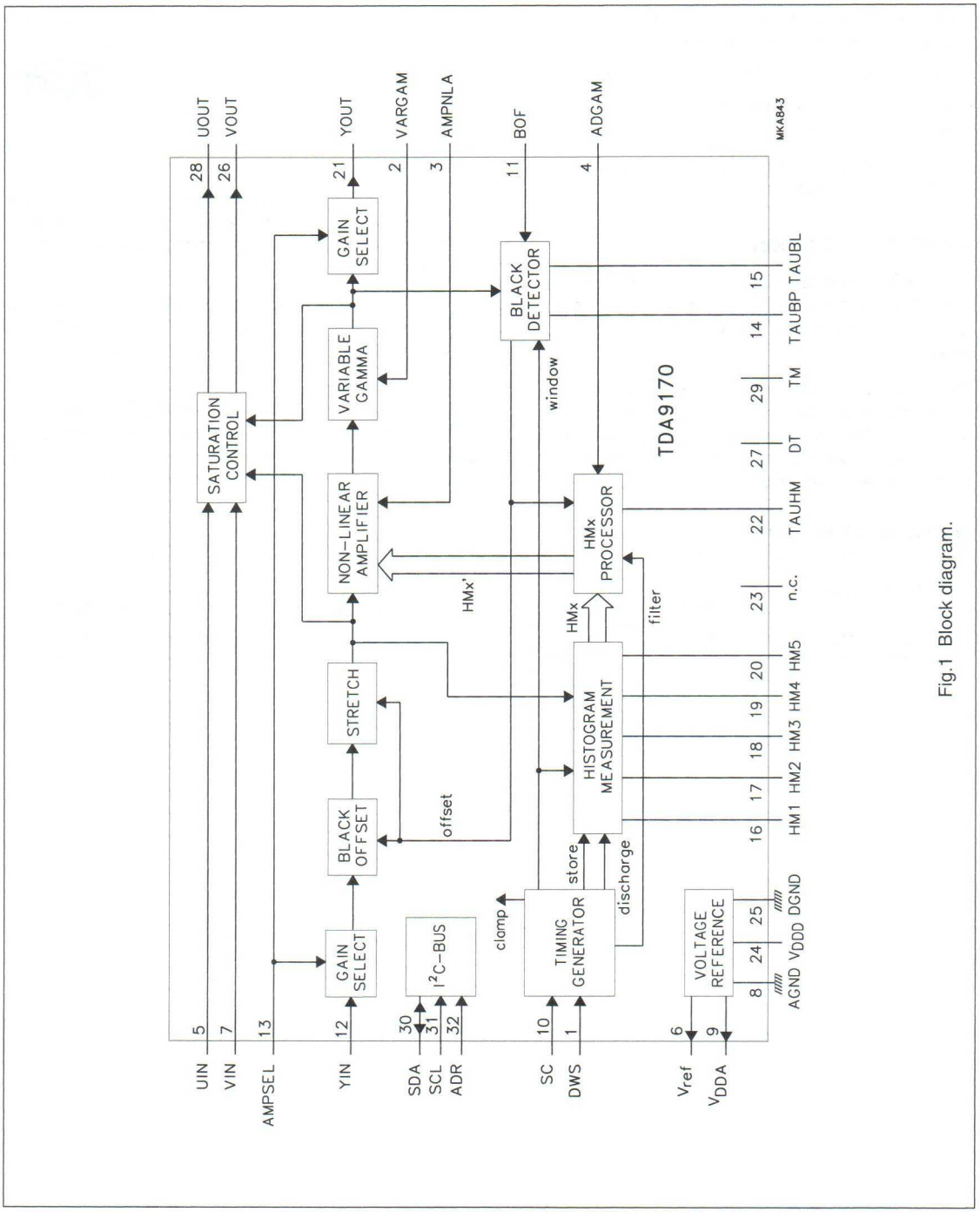


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DWS	1	default window select input
VARGAM	2	variable gamma input
AMPNLA	3	amplitude non-linearity input
ADGAM	4	adaptive gamma input
UIN	5	colour difference U input
V_{ref}	6	reference supply voltage output (+4 V)
VIN	7	colour difference V input
AGND	8	analog ground
V_{DDA}	9	analog supply voltage
SC	10	sandcastle input
BOF	11	black offset on/off input
YIN	12	luminance input
AMPSEL	13	amplitude select input
TAUBP	14	time constant black peak
TAUBL	15	time constant black loop
HM1	16	histogram segment memory 1
HM2	17	histogram segment memory 2
HM3	18	histogram segment memory 3
HM4	19	histogram segment memory 4
HM5	20	histogram segment memory 5
YOUT	21	luminance output
TAUHM	22	time constant histogram measurement loop
n.c.	23	not connected
V_{DDD}	24	digital supply voltage (+5 V)
DGND	25	digital ground
VOUT	26	colour difference V output
DT	27	test option
UOUT	28	colour difference U output
TM	29	test option
SDA	30	serial data input/output (I^2C-bus)
SCL	31	serial clock input (I^2C-bus)
ADR	32	address select input (I^2C-bus)

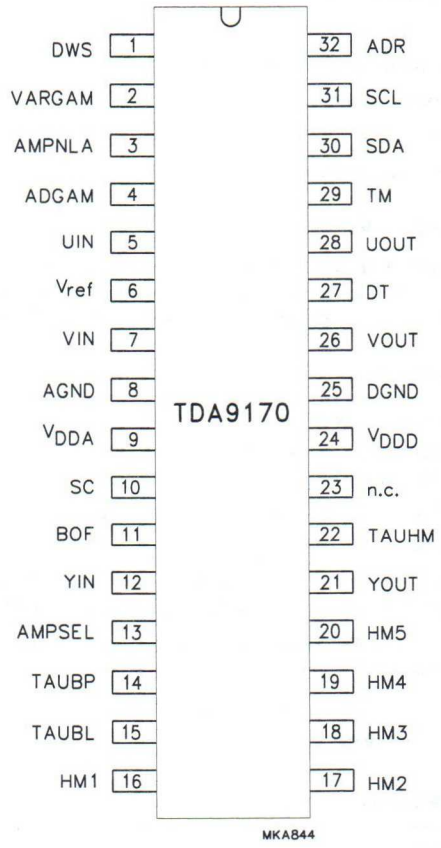


Fig.2 Pin configuration.

I²C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Power supply
- I²C-bus transceiver.

Stereo decoder

- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I²C-bus.

Audio processor

- Selector for internal and external signals (line in)
- Automatic volume level control (control range +6 to −15 dB)
- Interface for external noise reduction circuits
- Volume control (control range +16 to −71 dB)
- Special loudness characteristic automatically controlled in combination with volume setting (control range 28 dB)
- Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- Mute control via I²C-bus.

GENERAL DESCRIPTION

The TDA9852 is a bipolar-integrated BTSC stereo decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets, VCRs and multimedia.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9852	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA9852H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

LICENSE INFORMATION

A license is required for the use of this product. For further information, please contact

COMPANY	BRANCH	ADDRESS
THAT Corporation	Licensing Operations	734 Forest St. Marlborough, MA 01752 USA Tel.: (508) 229-2500 Fax: (508) 229-2590
	Tokyo Office	405 Palm House, 1-20-2 Honmachi Shibuya-ku, Tokyo 151 Japan Tel.: (03) 3378-0915 Fax: (03) 3374-5191

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		–	75	95	mA
$V_{comp(rms)}$	input signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	250	–	mV
$V_{oR,L(rms)}$	output signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	500	–	mV
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
α_{cs}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz	–	0.2	–	%
$V_{I, O(rms)}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_C	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f_i = 40 Hz	–	17	–	dB
S/N	signal-to-noise ratio	line out (mono); V_o = 0.5 V (RMS)				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_o = 2 V (RMS); gain = 0 dB				
		CCIR noise weighting filter (peak value)	–	94	–	dB
		DIN noise weighting filter (RMS value)	–	107	–	dBA

BLOCK DIAGRAM

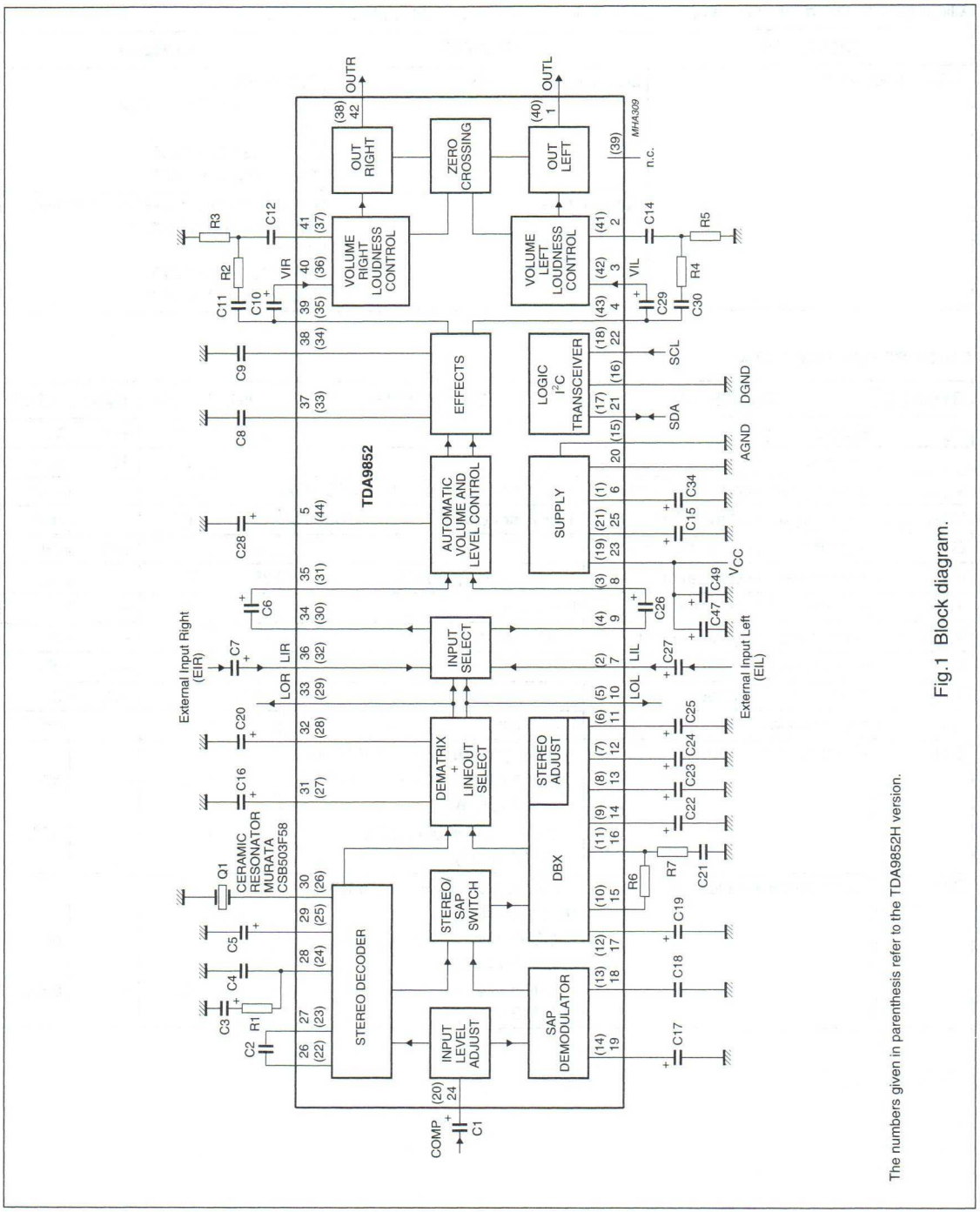


Fig.1 Block diagram.

The numbers given in parenthesis refer to the TDA9852H version.

Component list

Electrolytic capacitors ±20%; foil or ceramic capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENTS	VALUE	TYPE	REMARK
C1	10 µF	electrolytic	63 V
C2	470 nF	foil	
C3	4.7 µF	electrolytic	63 V
C4	220 nF	foil	
C5	10 µF	electrolytic	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	electrolytic	16 V
C7	2.2 µF	electrolytic	63 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	electrolytic	16 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C14	150 nF	foil	±5%
C15	100 µF	electrolytic	16 V
C16	4.7 µF	electrolytic	63 V
C17	4.7 µF	electrolytic	63 V
C18	100 nF	foil	
C19	10 µF	electrolytic	63 V
C20	4.7 µF	electrolytic	63 V
C21	47 nF	foil	±5%
C22	1 µF	electrolytic	63 V
C23	1 µF	electrolytic	63 V
C24	10 µF	electrolytic	63 V ±10%
C25	10 µF	electrolytic	63 V ±10%
C26	2.2 µF	electrolytic	16 V
C27	2.2 µF	electrolytic	63 V
C28	4.7 µF	electrolytic	63 V ±10%
C29	2.2 µF	electrolytic	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	electrolytic	16 V
C47	220 µF	electrolytic	25 V
C49	100 nF	foil or ceramic	SMD 1206
R1	2.2 kΩ	–	
R2	20 kΩ	–	
R3	2.2 kΩ	–	
R4	20 kΩ	–	
R5	2.2 kΩ	–	
R6	8.2 kΩ	–	±2%

COMPONENTS	VALUE	TYPE	REMARK
R7	160 Ω	–	±2%
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PINS		DESCRIPTION
	SDIP42	QFP44	
OUTL	1	40	output, left channel
LDL	2	41	input loudness, left channel
VIL	3	42	input volume, left channel
EOL	4	43	output effects, left channel
C_{AV}	5	44	automatic volume control capacitor
V_{ref}	6	1	reference voltage $0.5V_{CC}$
LIL	7	2	input line control, left channel
AVL	8	3	input automatic volume control, left channel
SOL	9	4	output selector, left channel
LOL	10	5	output line control, left channel
C_{TW}	11	6	capacitor timing wideband for dbx
C_{TS}	12	7	capacitor timing spectral for dbx
C_W	13	8	capacitor wideband for dbx
C_S	14	9	capacitor spectral for dbx
VEO	15	10	variable emphasis output for dbx
VEI	16	11	variable emphasis input for dbx
C_{NR}	17	12	capacitor noise reduction for dbx
C_M	18	13	capacitor mute for SAP
C_{DEC}	19	14	capacitor DC-decoupling for SAP
GND	20	–	ground
AGND	–	15	analog ground
DGND	–	16	digital ground
SDA	21	17	serial data input/output (I²C-bus)
SCL	22	18	serial clock input (I²C-bus)
V_{CC}	23	19	supply voltage
COMP	24	20	composite input signal
V_{CAP}	25	21	capacitor for electronic filtering of supply
C_{P1}	26	22	capacitor for pilot detector
C_{P2}	27	23	capacitor for pilot detector
C_{PH}	28	24	capacitor for phase detector
C_{ADJ}	29	25	capacitor for filter adjustment
CER	30	26	ceramic resonator
C_{MO}	31	27	capacitor DC-decoupling mono

SYMBOL	PINS		DESCRIPTION
	SDIP42	QFP44	
C_{SS}	32	28	capacitor DC-decoupling stereo/SAP
LOR	33	29	output line control, right channel
SOR	34	30	output selector, right channel
AVR	35	31	input automatic volume control, right channel
LIR	36	32	input line control, right channel
C_{PS2}	37	33	capacitor 2 pseudo function
C_{PS1}	38	34	capacitor 1 pseudo function
EOR	39	35	output effects, right channel
VIR	40	36	input volume, right channel
LDR	41	37	input loudness, right channel
OUTR	42	38	output, right channel
n.c.	–	39	not connected

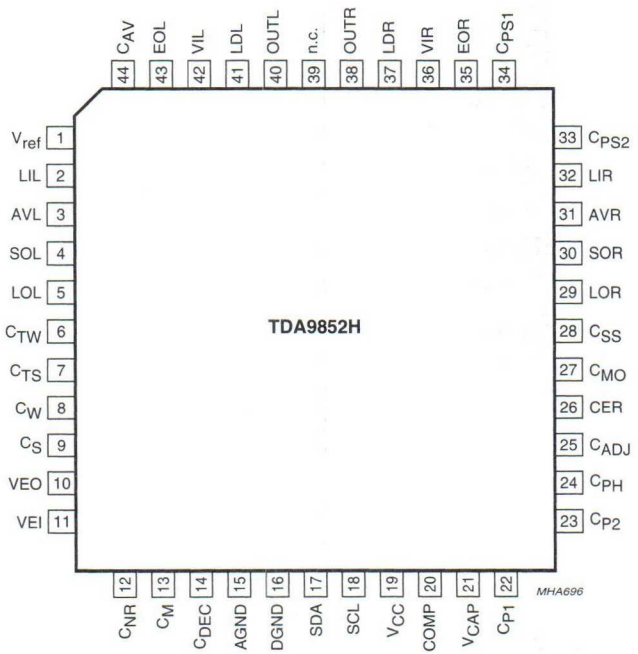


Fig.2 Pin configuration (QFP-version).

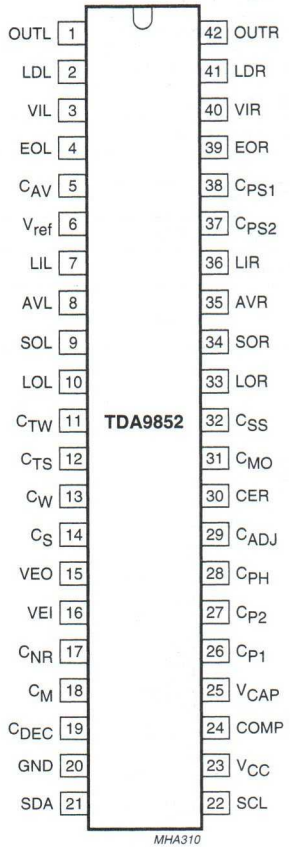


Fig.3 Pin configuration (SDIP-version).

1.3 GHz Bidirectional I²C-bus controlled synthesizer TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (3 addresses)
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 current limited outputs (1 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

GENERAL DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102(1)
TSA5511T	16	SO	plastic	SOT109A(2)
TSA5511AT	20	SO	plastic	SOT163A(3)

Note

1. SOT102-1; 1996 December 5.
2. SOT109-1; 1996 December 5.
3. SOT163-1; 1996 December 5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open-collector output current	10	–	–	mA
I_O	current–limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

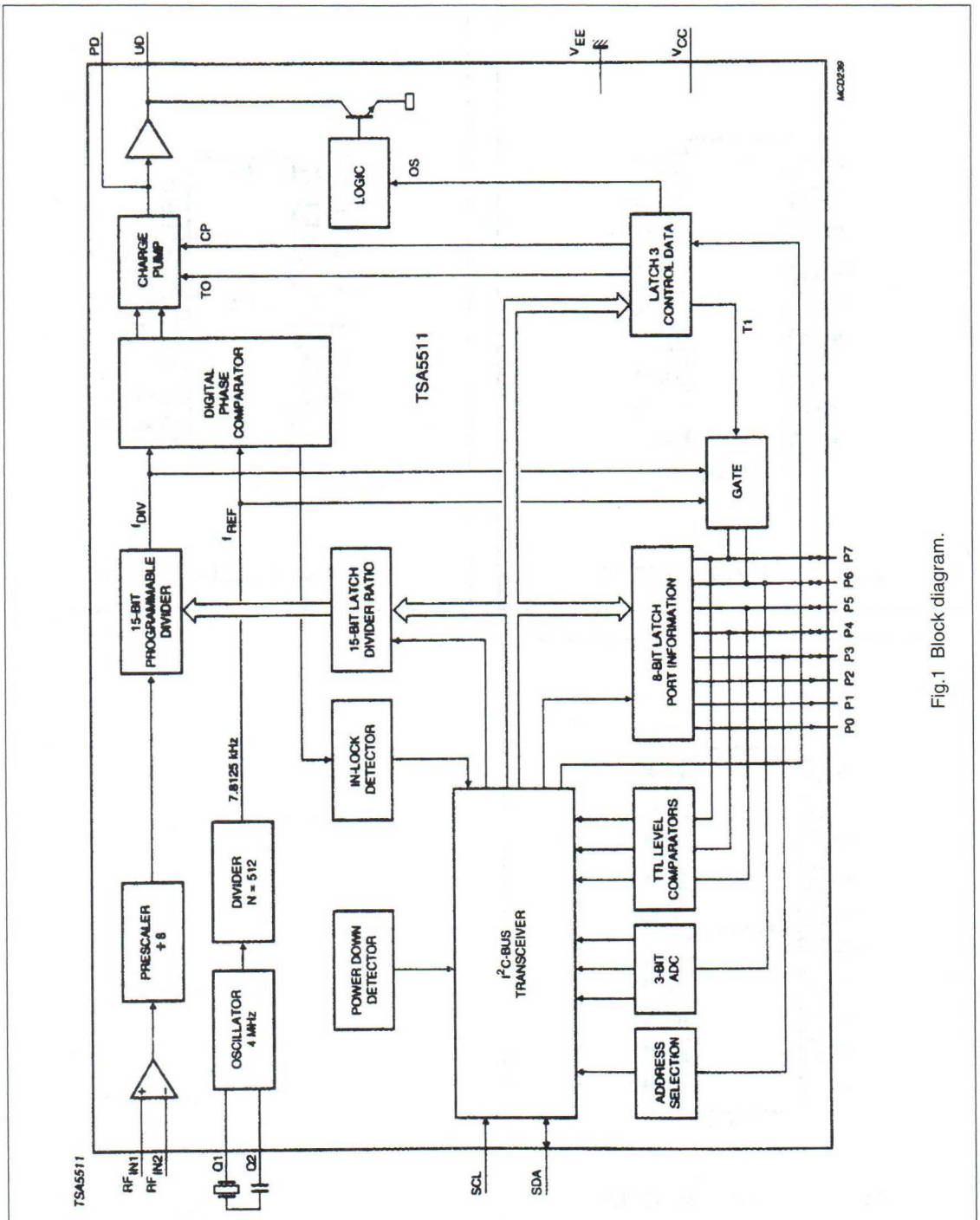


Fig.1 Block diagram.

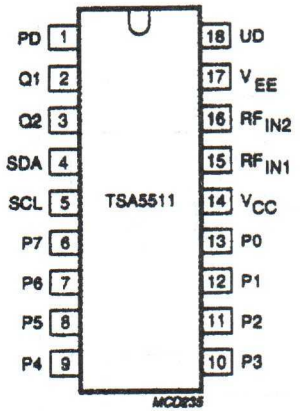


Fig.2 Pin configuration for SOT102.

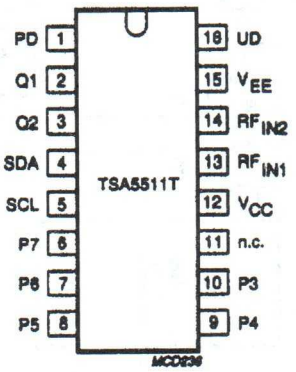


Fig.3 Pin configuration for SOT109.

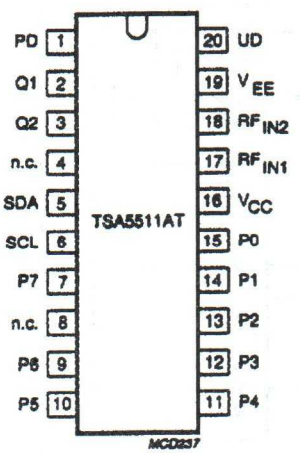


Fig.4 Pin configuration for SOT163.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	–	13	port output
n.c.	–	11	–	not connected
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

1.3 GHz Bidirectional I²C-bus controlled synthesizer TSA5512

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (3 addresses)
- Analog-to-digital converter
- 8 bus controlled ports (6 for TSA5512T), 8 open collector outputs (4 bidirectional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5512 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5512 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5512	18	DIL	plastic	SOT102(1)
TSA5512T	16	SO	plastic	SOT109A(2)
TSA5512AT	20	SO	plastic	SOT163A(3)
TSA5512M	20	SSOP	plastic	SOT266(4)

Note

1. SOT102-1; 1996 December 5.
2. SOT109-1; 1996 December 5.
3. SOT163-1; 1996 December 5.
4. SOT266-1; 1996 December 5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δfr	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open-collector output current	5	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

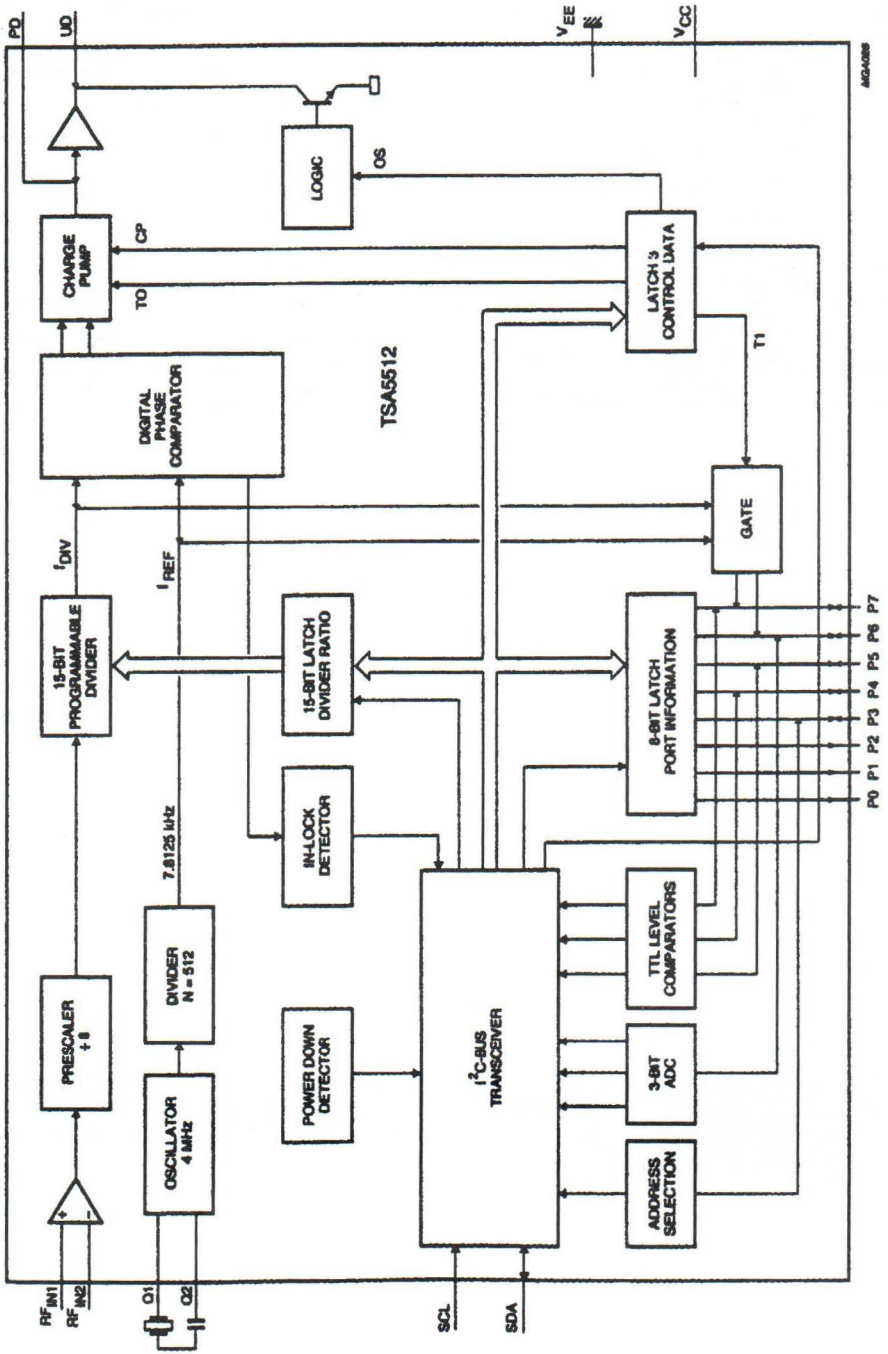


Fig.1 Block diagram.

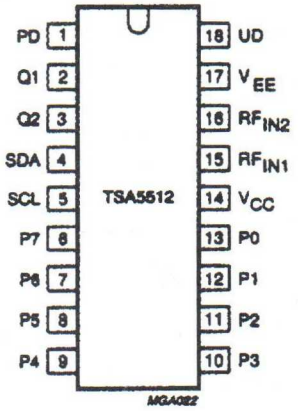


Fig.2 Pin configuration for SOT102.

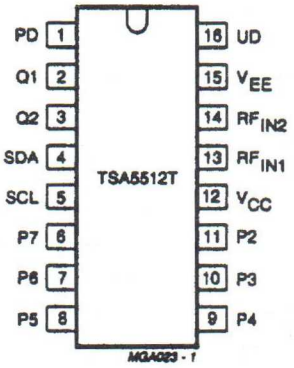


Fig.3 Pin configuration for SOT109.

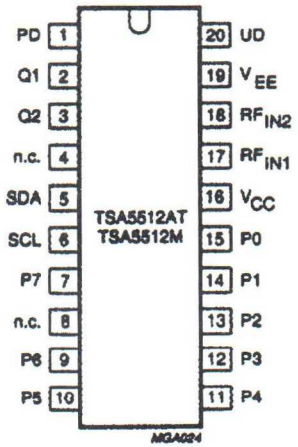


Fig.4 Pin configuration for SOT163/SOT266.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163 SOT266	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	11	13	port output
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

1.3 GHz bidirectional I²C-bus controlled synthesizer TSA5514

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (4 addresses)
- 5-level analog-to-digital converter
- 7 bus controlled ports; 3 output, 4 open collector input/output
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5514 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the seven output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5514 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage to AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{cc}	supply voltage	–	5	–	V
I_{cc}	supply current	–	35	–	mA
Δfr	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{xtal}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_o	open-collector output current	10	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5514	18	DIL	plastic	SOT102(1)
TSA5514T	16	SO	plastic	SOT109A(2)
TSA5514AT	20	SO	plastic	SOT163A(3)

Note

1. SOT102-1; 1996 December 4.
2. SOT109-1; 1996 December 4.
3. SOT 163-1; 1996 December 4.

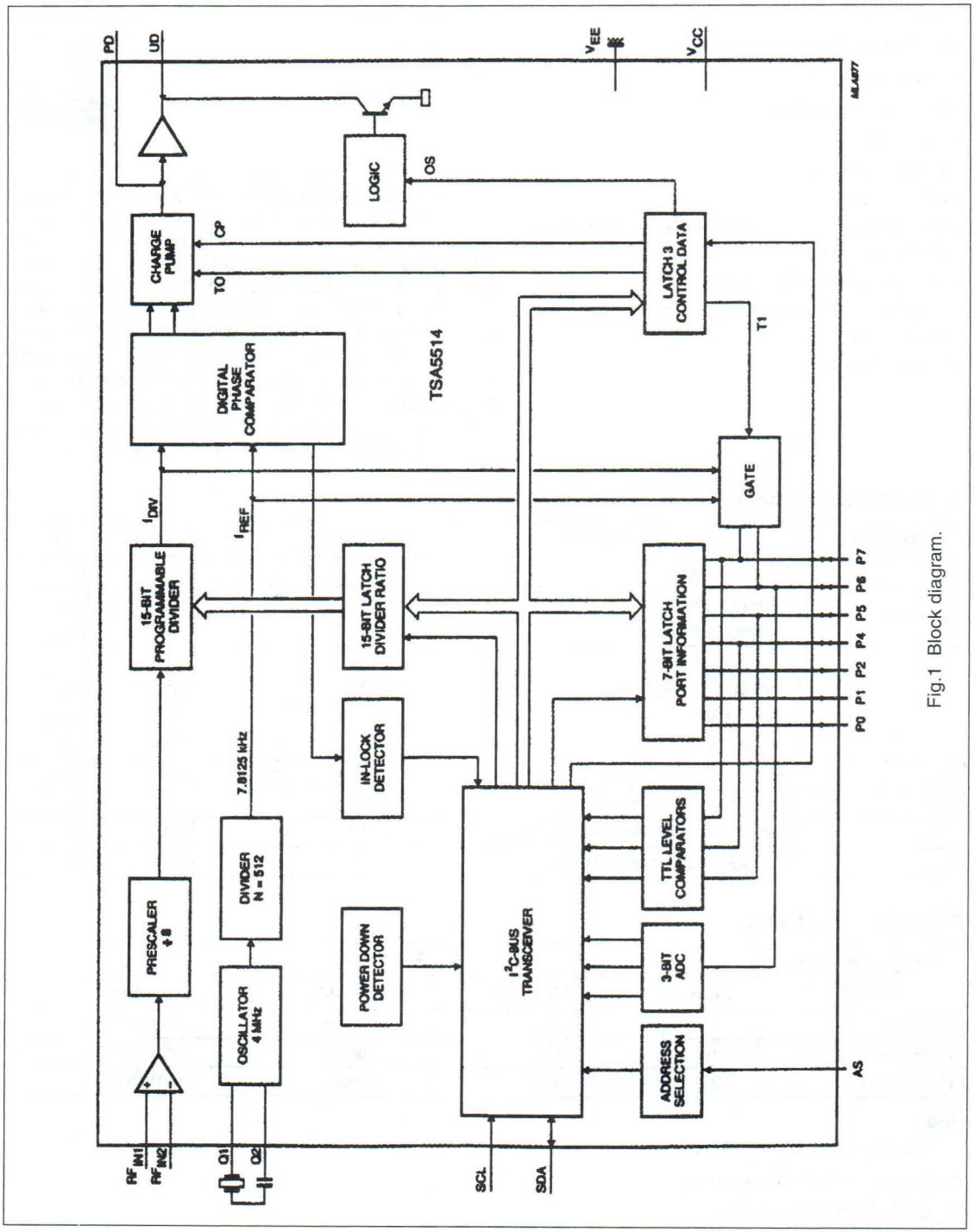


Fig.1 Block diagram.

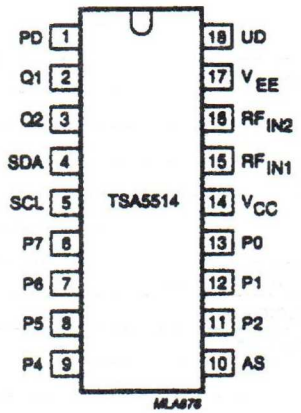


Fig.2 Pin configuration for SOT102.

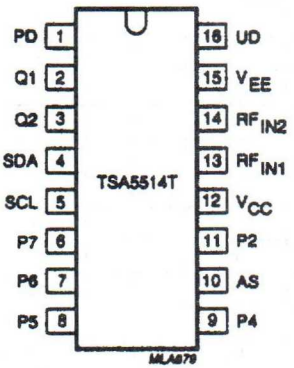


Fig.3 Pin configuration for SOT109.

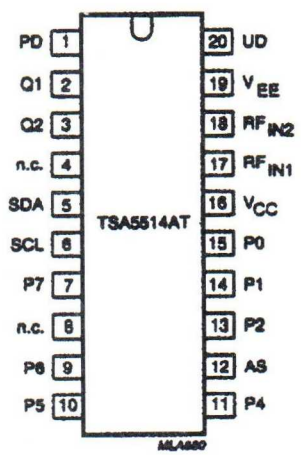


Fig.4 Pin configuration for SOT163.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
AS	10	10	12	address selection input
P2	11	11	13	port output
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

1.3 GHz bi-directional I²C-bus controlled synthesizer TSA5515T

GENERAL DESCRIPTION

The TSA5515T is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the three output ports and set the charge-pump current. A flag is set when the loop is "in-lock". Another flag is set when a power dip occurs on the supply line. These flags are read out of the TSA5515T on SDA line (one status byte) during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage on the AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 1.3 GHz single-chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 3 bus-controlled output ports
- Power-down flag
- Available in SOT108A package

APPLICATIONS

- TV tuners
- VCR tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open-collector output current				
	P7	–	–	5	mA
	P1, P2	–	–	20	mA
T_{amb}	operating ambient temperature range	−10	–	80	°C
T_{stg}	storage temperature range	−40	–	125	°C
$R_{th\ j\text{-}a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5515T	14	SO	plastic	SOT108A(1)

Note

1. SOT108-1; 1996 December 3.

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

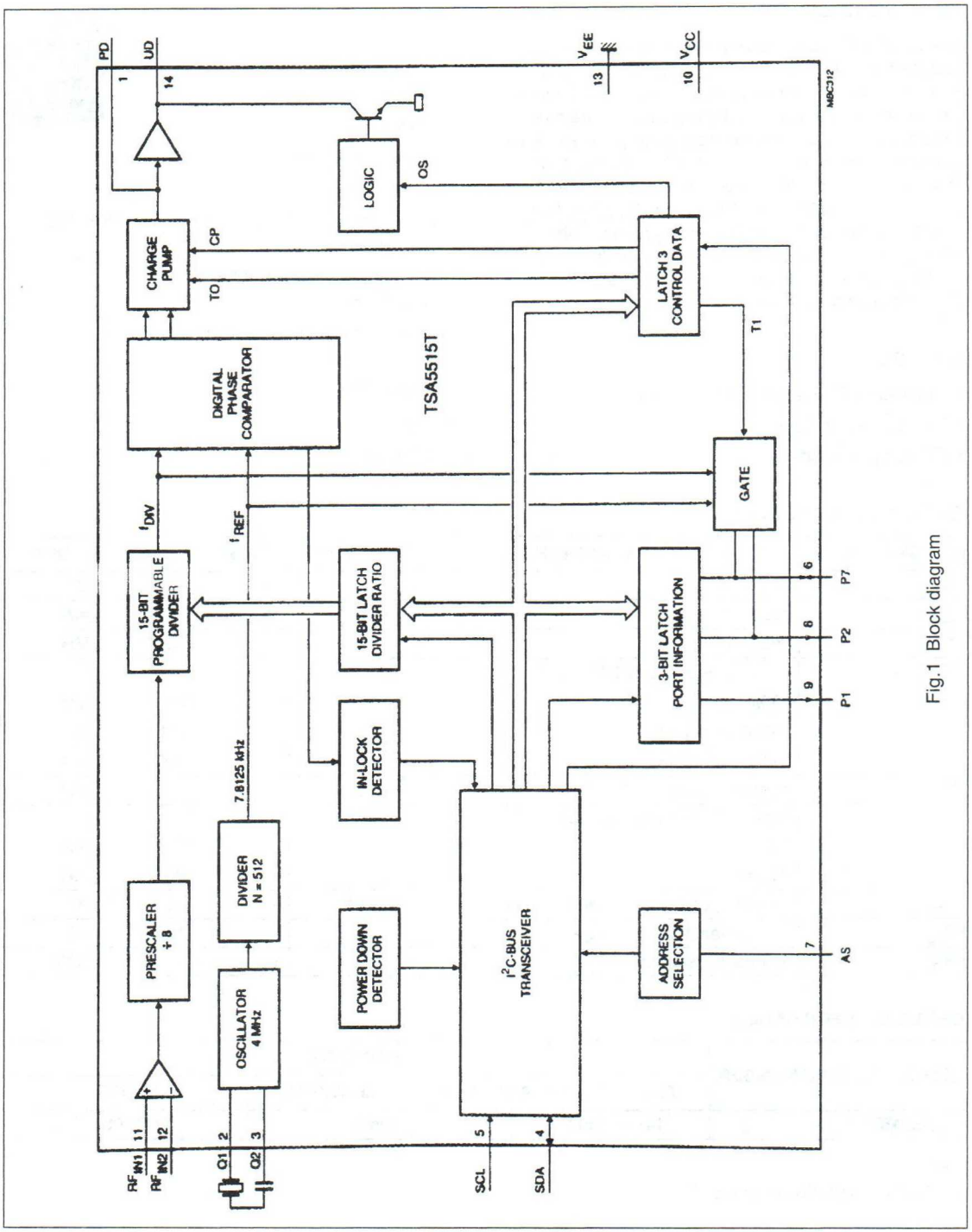


Fig.1 Block diagram

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P7}	address selection	−0.3	6	V
V_{P6}	output ports P7, P2, P1	−0.3	16	V
V_{P11}	prescaler inputs	−0.3	2.5	V
V_{P14}	drive output	−0.3	V_{CC}	V
I_{6L}	output port P7 (open collector)	−1	10	mA
I_{8L}	output port P2, P1 (open collector)	−1	25	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (> 1500 V).

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output
AS	7	input for address selection
P2	8	port output
P1	9	port output
V_{CC}	10	voltage supply
RF_{IN1}	11	UHF/VHF signal input 1
RF_{IN2}	12	UHF/VHF signal input 2 (decoupled)
GND	13	ground
UD	14	drive output

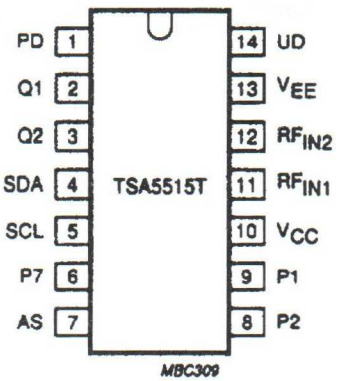


Fig.2 Pinning diagram.

1.3 GHz universal bus-controlled TV synthesizer

TSA5520; TSA5521

FEATURES

- Complete 1.3 GHz single chip system
- Four PNP band switch buffers (40 mA)
- 33 V output tuning voltage
- In-lock detector
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (60 or 280 μA)
- Varicap drive disable
- Universal bus protocol I²C-bus or 3-wire bus (the TSA5520/TSA5521 I²C-bus mode only includes the write mode; if both read and write modes are required the TSA5526/TSA5527 devices should be selected):
  - bus protocol for 18 or 19 bits transmission (3-wire bus)
  - extra protocol for 27 bits for test and features (3-wire bus)
  - address plus 4 data bytes transmission (I²C-bus)
  - three independent I²C-bus addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5520M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5520T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5521M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5521T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	20	25	mA
I_{CC2}	band switch supply current	note 1	–	50	55	mA
f_{RF}	RF input frequency		64	–	1300	MHz
$V_{i(RF)}$	RF input voltage	80 to 150 MHz	–25	–	+3	dBm
		150 MHz to 1 GHz	–28	–	+3	dBm
		1 to 1.3 GHz	–15	–	+3	dBm
f_{xtal}	crystal oscillator input frequency		3.2	4.0	4.48	MHz
$I_{o(PNP)}$	PNP band switch buffers output current	note 2	4	–	50	mA
P_{tot}	total power dissipation	note 3	–	250	400	mW
T_{stg}	IC storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C

Notes

1. One band switch buffer ON with 40 mA.
2. One buffer ON, I_o = 40 mA; two buffers ON, maximum sum of I_o = 50 mA.
3. The power dissipation is calculated as follows:

$$P_D = V_{CC1} \times I_{CC1} + V_{CC2} \times (I_{CC2} - I_o) + I_o \times V_{CE(satPNP)} + (V33/2)^2/27\ k\Omega$$

GENERAL DESCRIPTION

The device is a single-chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier and the 33 V output. Four high-current PNP band switch buffers are provided for band switching. Two PNP buffers can be switched on simultaneously. The sum of the collector currents is limited to 50 mA.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz using a 4 MHz crystal.

The lock detector output is LOW when the PLL loop is locked. In the test mode, this output is used as a test output for f_{ref} and $1/2f_{div}$ (see Table 6). The device can be controlled in accordance with the I²C-bus format or the 3-wire bus format depending on the voltage applied to the SW input (see Table 2).

I²C-bus format (SW = LOW)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four PNP band switch buffers, set the charge-pump current and the reference divider ratio.

The device has three independent I²C-bus addresses which can be selected by applying a specific voltage on the CE input (see Table 5). The general address C2 is always valid. When the I²C-bus format is fully used, TSA5520 and TSA5521 are equal.

3-wire bus format (SW = V_{CC1} or open-circuit)

Data is transmitted to the device during a HIGH level on the CE input (enable line pin 15). The device is compatible with 18-bit and 19-bit data formats. The first four bits are used to program the PNP band switch buffers and the remaining bits are used to control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes. The difference between TSA5520 and TSA5521 are given in Table 1.

When the 27-bit format is used, the TSA5520 and TSA5521 are equal and the reference divider is controlled by the RSA and RSB bits (see Table 7). More details are given in Chapter "Functional description"Section "3-wire bus mode (SW = open-circuit or V_{CC1}); see Figs 3,4 and 5".

Table 1 Differences between TSA5520 and TSA5521

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER	FREQUENCY STEP (kHz)
TSA5520	18-bit	512[1]	62.5
TSA5520	19-bit	1024[1]	31.25
TSA5521	18-bit or 19-bit	640[2]	50

Notes

1. The selection of the reference divider is given by an automatic identification of the data word length.
2. The reference divider is set to 640 at power-on reset.

BLOCK DIAGRAM

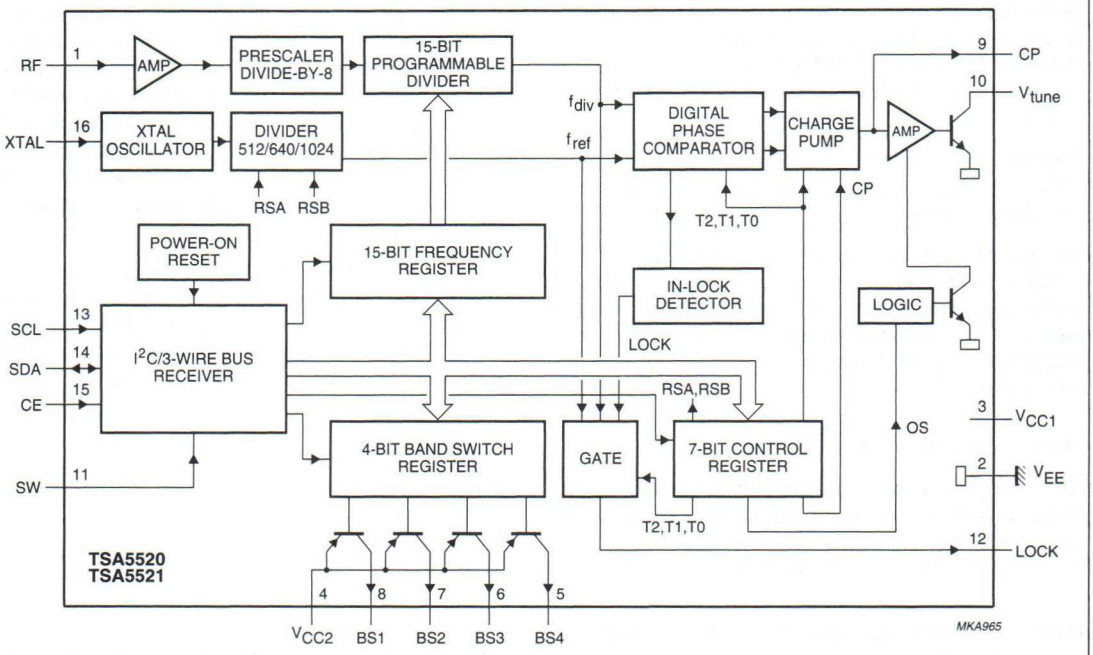


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RF	1	RF signal input
V_{EE}	2	ground
V_{CC1}	3	supply voltage (+5 V)
V_{CC2}	4	band switch supply voltage (+12 V)
BS4	5	PNP band switch buffer output 4
BS3	6	PNP band switch buffer output 3
BS2	7	PNP band switch buffer output 2
BS1	8	PNP band switch buffer output 1
CP	9	charge-pump output
V_{tune}	10	tuning voltage output
SW	11	bus format selection input, I^2C-bus or 3-wire
LOCK	12	lock detector output
SCL	13	serial clock input
SDA	14	serial data input/output
CE	15	chip enable/address selection input
XTAL	16	crystal oscillator input

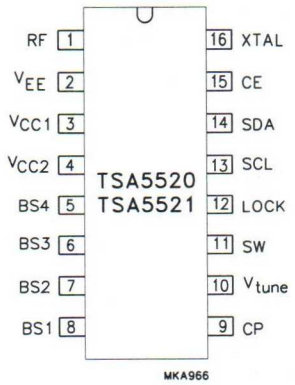


Fig.2 Pin configuration.

1.4 GHz I²C-bus controlled synthesizer TSA5522

FEATURES

- Complete 1.4 GHz single chip system
- Three PNP band switch buffers (20 mA)
- Four bus-controlled bidirectional ports (NPN open-collector outputs); only one port in 16-pin version
- 33 V tuning voltage output
- In-lock detector
- 5-step ADC
- Mixer-Oscillator (M/O) band switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250 μA)
- Varicap drive disable
- I²C-bus format
  - address plus 4 data bytes transmission (write mode)
  - address plus 1 status byte transmission (read mode)
  - three independent addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front-ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5522M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TSA5522T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (+12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	22	30	mA
I_{CC2}	band switch supply current	note 1	–	27	32	mA
f_{RF}	RF input frequency		64	–	1400	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	– 25	–	3	dBm
		f_i = 150 to 1000 MHz	– 28	–	3	dBm
		f_i = 1000 to 1400 MHz	– 26	–	3	dBm
f_{xtal}	crystal oscillator input frequency		–	4	–	MHz
$I_{o(PNP)}$	PNP band switch buffers output current		–	20	25	mA
$I_{o(NPN)}$	NPN open-collector output current		–	20	25	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
T_{stg}	storage temperature (IC)		–40	–	+150	°C

Note

1. One band switch buffer ON; I_o = 20 mA.

GENERAL DESCRIPTION (see Fig.1)

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three high-current PNP band switch buffers are provided for band switching together with four open-collector NPN outputs (only one open-collector output on 16-pin devices). These ports can also be used as input ports [one Analog-to Digital Converter (ADC) and three general purpose I/O ports (not available on 16-pin devices)]. An output is provided to control a Philips mixer/oscillator IC in combination with the PNP buffers state.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz with a 4 MHz crystal. The LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation.

The ADC is available for digital AFC control. The ADC code is read during a read operation on the I²C-bus. The ADC input is combined with the port P6. In the TEST mode, this port is also used as a TEST output for f_{ref} and $\frac{1}{2}f_{div}$ (see Table 4).

I²C-bus format

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and the reference divider ratio. The device has three independent I²C-bus addresses selected by applying a specific voltage on AS input (see Table 3). The general address C2 is always valid.

BLOCK DIAGRAM

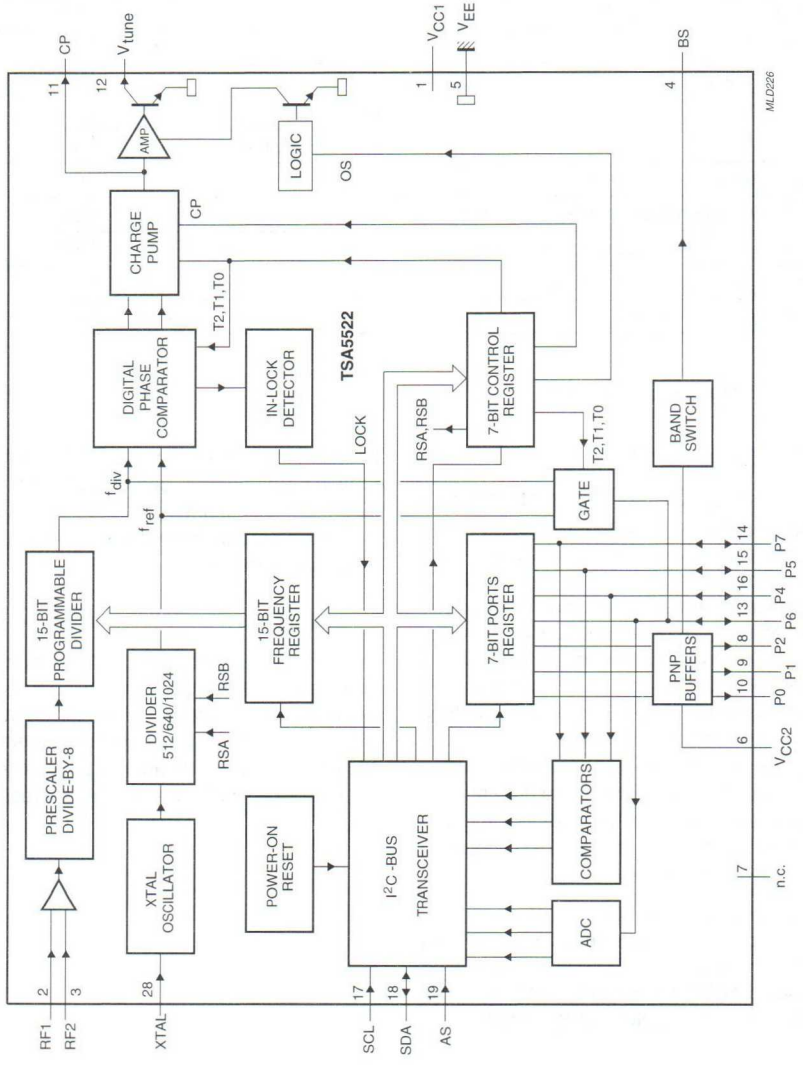


Fig.1 Block diagram (SSOP20).

PINNING

SYMBOL	SO16	SSOP20	DESCRIPTION
V_{CC1}	1	1	voltage supply (+5 V)
RF1	2	2	RF signal input 1
RF2	3	3	RF signal input 2
BS	4	4	band switch output to mixer/oscillator drive
V_{EE}	5	5	ground
V_{CC2}	6	6	voltage supply (+12 V)
n.c.	–	7	not connected
P2	7	8	PNP band switch buffer output 2
P1	8	9	PNP band switch buffer output 1
P0	9	10	PNP band switch buffer output 0
CP	10	11	charge-pump output
V_{tune}	11	12	tuning voltage output
P6	12	13	NPN open-collector output/ADC input
P7	–	14	NPN open-collector output/comparator input
P5	–	15	NPN open-collector output/comparator input
P4	–	16	NPN open-collector output/comparator input
SCL	13	17	serial clock input
SDA	14	18	serial data input/output
AS	15	19	address selection input
XTAL	16	20	crystal oscillator input

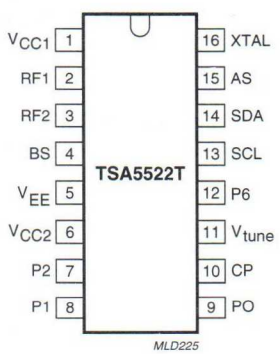


Fig.2 Pin configuration (SO16).

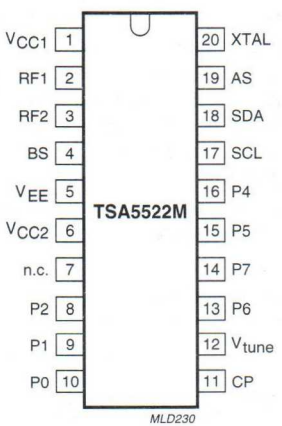


Fig.3 Pin configuration (SSOP20).

1.4 GHz I²C-bus controlled multimedia synthesizer

TSA5523M

FEATURES

- Complete 1.4 GHz single-chip system
- Adaptive DC/DC converter driver output
- On-board tuning amplifier output
- Varicap drive disable
- Four NPN open-collector output ports (10 mA)
- Four bus-controlled bidirectional ports (NPN open-collector outputs)
- In-lock detector
- 5-step Analog-to-Digital Converter (ADC)
- Mixer/Oscillator (M/O) band-switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250 μA)
- I²C-bus format
  - Address plus four data bytes transmission (write mode)
  - Address plus one status byte transmission (read mode)
  - Four independent addresses
- Low power, low radiation.

GENERAL DESCRIPTION

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider, a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three NPN open-collector outputs are provided for band switching together with five open-collector NPN outputs. Four of these ports can also be used as input ports (one ADC and three general purpose I/O ports).

An output is provided to control a Philips mixer/oscillator IC controlled by bits P7, P5 and P4. Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625, 6.25 or 7.8125 kHz with a 4 MHz crystal.

The lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC is available for digital AFC control. The ADC code is read during a read operation on the I²C-bus. The ADC input is combined with the port P6. In the test mode, this port is also used as a test output for f_{ref} and $f_{div/2}$ (see Table 4). In addition, the circuit includes a DC/DC converter driver connected to the IDC pin to control the amplitude of an external oscillator followed by a voltage rectifier.

The voltage rectifier is used to generate the correct tuning supply voltage to maintain a constant current into the tuning amplifier. The DC/DC converter driver can be disabled by setting the IDC pin to V_{CC1} in this event the tuning supply voltage is delivered by a fixed 33 V supply.

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and set the reference divider ratio. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage on the AS input (see Table 3).

APPLICATIONS

- Multimedia TV tuners and front-ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5523M/C1	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		4.5	–	5.5	V
I_{CC1}	supply current		–	22	30	mA
f_{RF}	RF frequency range		64	–	1400	MHz
V_{iRF}	RF input voltage level	80 to 150 MHz	–25	–	+3	dBm
		150 MHz to 1 GHz	–28	–	+3	dBm
		1 to 1.4 GHz	–26	–	+3	dBm
f_{XTAL}	crystal oscillator frequency		–	4	–	MHz
I_{NPN}	NPN open-collector output current		–	10	15	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
T_{stg}	IC storage temperature		–40	–	+150	°C

1.4 GHz I²C-bus controlled multimedia synthesizer

TSA5523M

BLOCK DIAGRAM

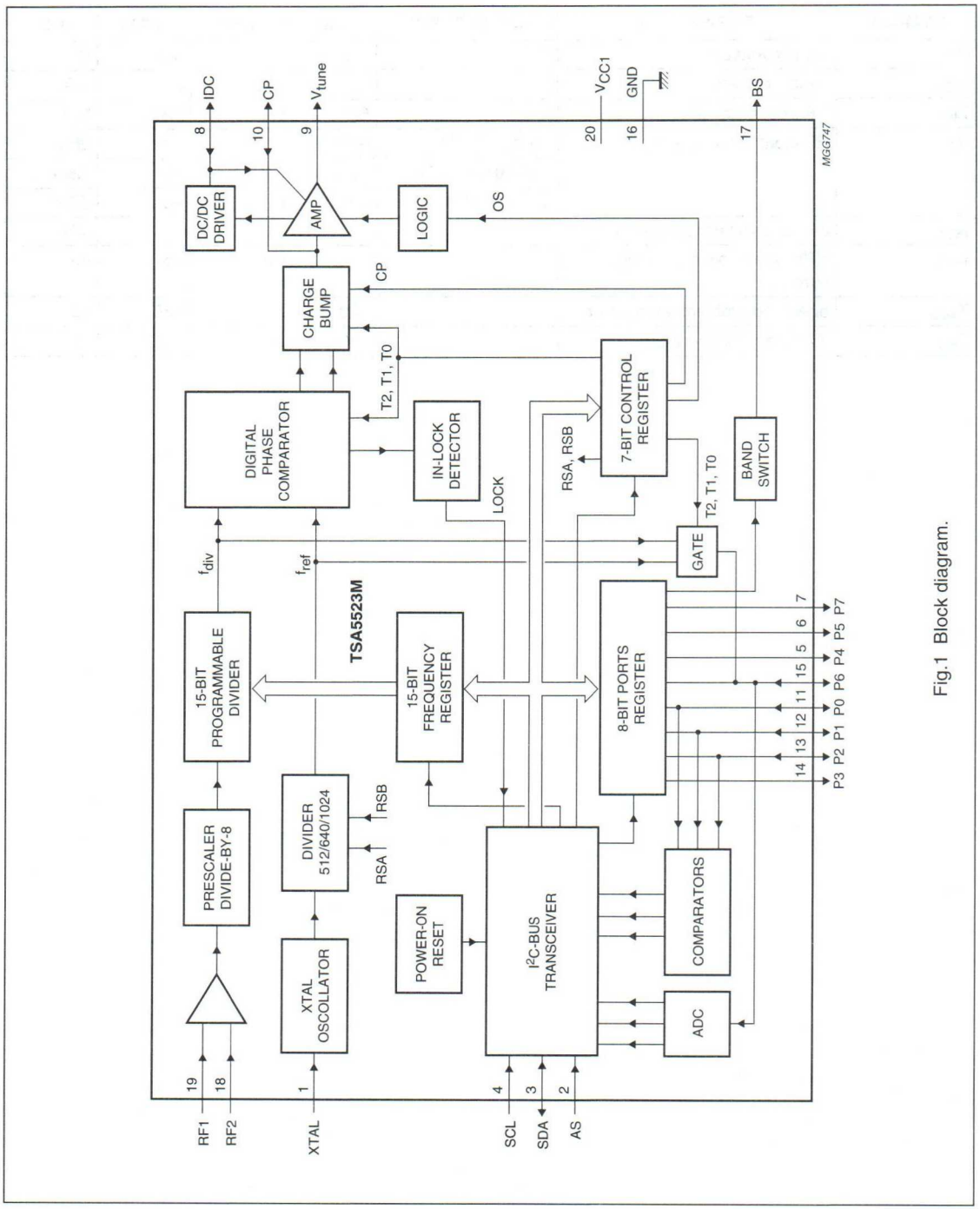


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal oscillator input
AS	2	address selection input
SDA	3	serial data input/output
SCL	4	serial clock input
P4	5	Port 4 NPN open-collector band-switch output
P5	6	Port 5 NPN open-collector band-switch output
P7	7	Port 7 NPN open-collector band-switch output
IDC	8	DC/DC converter control I/O terminal
V_{tune}	9	tuning voltage output
CP	10	NPN open-collector I/O port
P0	11	Port 0 NPN open-collector I/O port
P1	12	Port 1 NPN open-collector I/O port
P2	13	Port 2 NPN open-collector I/O port
P3	14	Port 3 NPN open-collector output
P6	15	Port 6 NPN open-collector output/ADC input
GND	16	ground
BS	17	band-switch output to mixer/oscillator driver
RF2	18	RF signal input 2
RF1	19	RF signal input 1
V_{CC1}	20	supply voltage (+5 V)

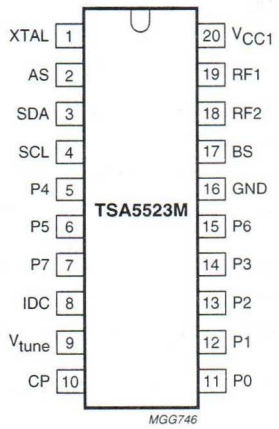


Fig.2 Pin configuration.

1.3 GHz universal bus-controlled TV synthesizers

TSA5526; TSA5527

FEATURES

- Complete 1.3 GHz single chip system
- Four PNP band switch buffers (40 mA)
- 33 V output tuning voltage
- In-lock detector
- 5-step ADC
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (60 or 280 μA)
- Programmable automatic charge-pump current switch
- Varicap drive disable
- Universal bus protocol I²C-bus or 3-wire bus:
  - bus protocol for 18 or 19 bits transmission (3-wire bus)
  - extra protocol for 27 bits for test and features (3-wire bus)
  - address plus 4 data bytes transmission (I²C-bus write mode)
  - address plus 1 status byte transmission (I²C-bus read mode)
  - three independent I²C-bus addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5526M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5526AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	20	25	mA
I_{CC2}	band switch supply current	note 1	–	50	55	mA
f_{RF}	RF input frequency		64	–	1300	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
f_{xtal}	crystal oscillator input frequency		3.2	4.0	4.48	MHz
$I_{o(PNP)}$	PNP band switch buffers output current	note 2	4	–	50	mA
P_{tot}	total power dissipation	note 3	–	250	400	mW
T_{stg}	storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C

Notes

1. One band switch buffer ON, I_o = 40 mA.
2. One band switch buffer ON, I_o = 40 mA; two buffers ON, maximum sum of I_o = 50 mA.
3. The power dissipation is calculated as follows:

$$P_D = V_{CC1} \times I_{CC1} + V_{CC2} \times (I_{CC2} - I_o) + I_o \times V_{CE(satPNP)} + (V33/2)^2/27k\Omega.$$

GENERAL DESCRIPTION

The device is a single-chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier and the 33 V output. Four high-current PNP band switch buffers are provided for band switching. Two PNP buffers can be switched on simultaneously. The sum of the collector currents is limited to 50 mA.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz using a 4 MHz crystal.

The device can be controlled in accordance with the I²C-bus format or the 3-wire bus format depending on the voltage applied to the SW input (see Table 3). In the 3-wire bus mode (SW = HIGH) pin 12 is the LOCK output. The lock output is LOW when the PLL loop is locked. In the I²C-bus mode (SW = LOW) the LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC input is available on pin 12 for AFC control in the I²C-bus mode only. The ADC code is read during a read operation on the I²C-bus. In the test mode pin 12 is used as a test output for f_{ref} and $\frac{1}{2}f_{div}$ in the I²C-bus mode and the 3-wire bus mode (see Table 6).

When the automatic charge-pump current switch mode is activated, depending on the device given in Table 6, and when the loop is phase-locked, the charge-pump current value is automatically switched to LOW. This action is taken to improve the carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a read operation on the I²C-bus (see Table 8).

I²C-bus format (SW = LOW)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four PNP band switch buffers, set the charge-pump current and the reference divider ratio.

The device has three independent I²C-bus addresses which can be selected by applying a specific voltage on the CE input (see Table 5). The general address C2 is always valid. When the I²C-bus format is fully used, TSA5526 and TSA5527 are equal.

3-wire bus format (SW = V_{CC1} or open-circuit)

Data is transmitted to the device during a HIGH level on the CE input (enable line pin 15). The device is compatible with 18-bit and 19-bit data formats. The first four bits are used to program the PNP band switch buffers and the remaining bits are used to control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes. The differences between TSA5526 and TSA5527 are given in Table 1.

When the 27-bit format is used, the TSA5526 and TSA5527 are equal and the reference divider is controlled by the RSA and RSB bits (see Table 7 and Figs 3, 4 and 5).

Table 1 Differences between TSA5526 and TSA5527

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER	FREQUENCY STEP (kHz)
TSA5526	18-bit	512[1]	62.5
TSA5526	19-bit	1024[1]	31.25
TSA5527	19-bit	640[2]	50

Notes

1. The selection of the reference divider is given by an automatic identification of the data word length.
2. The reference divider is set to 640 at power-on reset.

BLOCK DIAGRAM

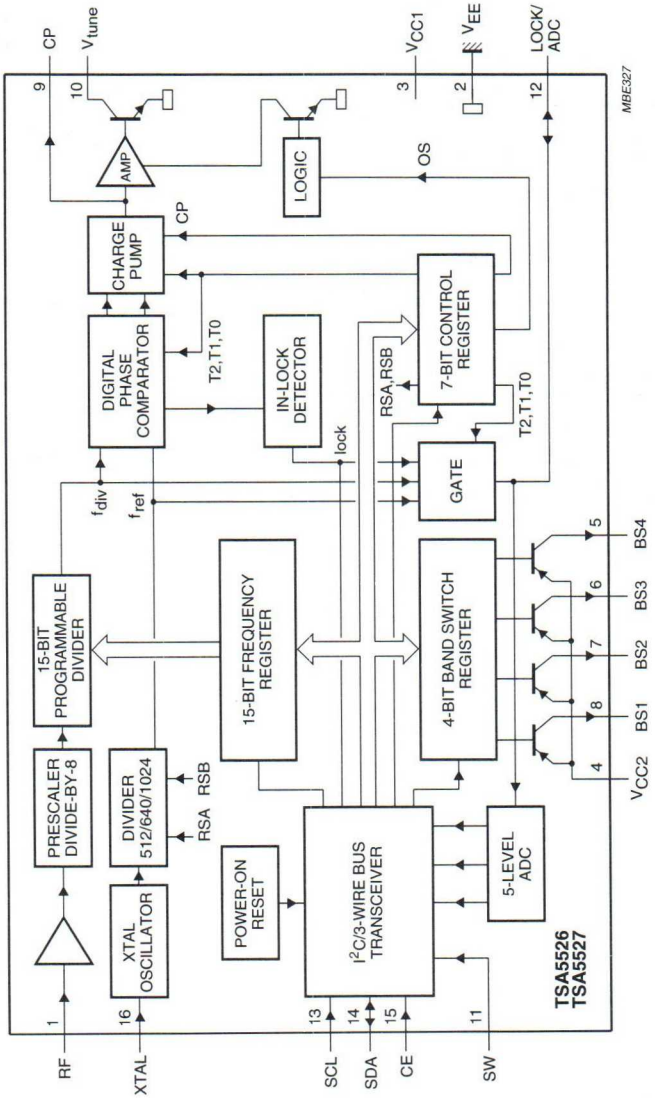


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RF	1	RF signal input
V_{EE}	2	ground
V_{CC1}	3	supply voltage (+5 V)
V_{CC2}	4	band switch supply voltage (+12 V)
BS4	5	PNP band switch buffer output 4
BS3	6	PNP band switch buffer output 3
BS2	7	PNP band switch buffer output 2
BS1	8	PNP band switch buffer output 1
CP	9	charge-pump output
V_{tune}	10	tuning voltage output
SW	11	bus format selection input, I^2C-bus or 3-wire
LOCK/ADC	12	lock detector output (3-wire bus/ ADC input (I^2C-bus)
SCL	13	serial clock input
SDA	14	serial data input/output
CE	15	chip enable/address selection input
XTAL	16	crystal oscillator input

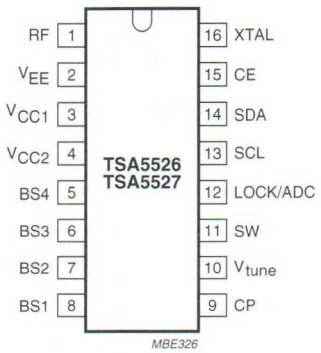


Fig.2 Pin configuration.

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DATA HANDBOOK SYSTEM

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