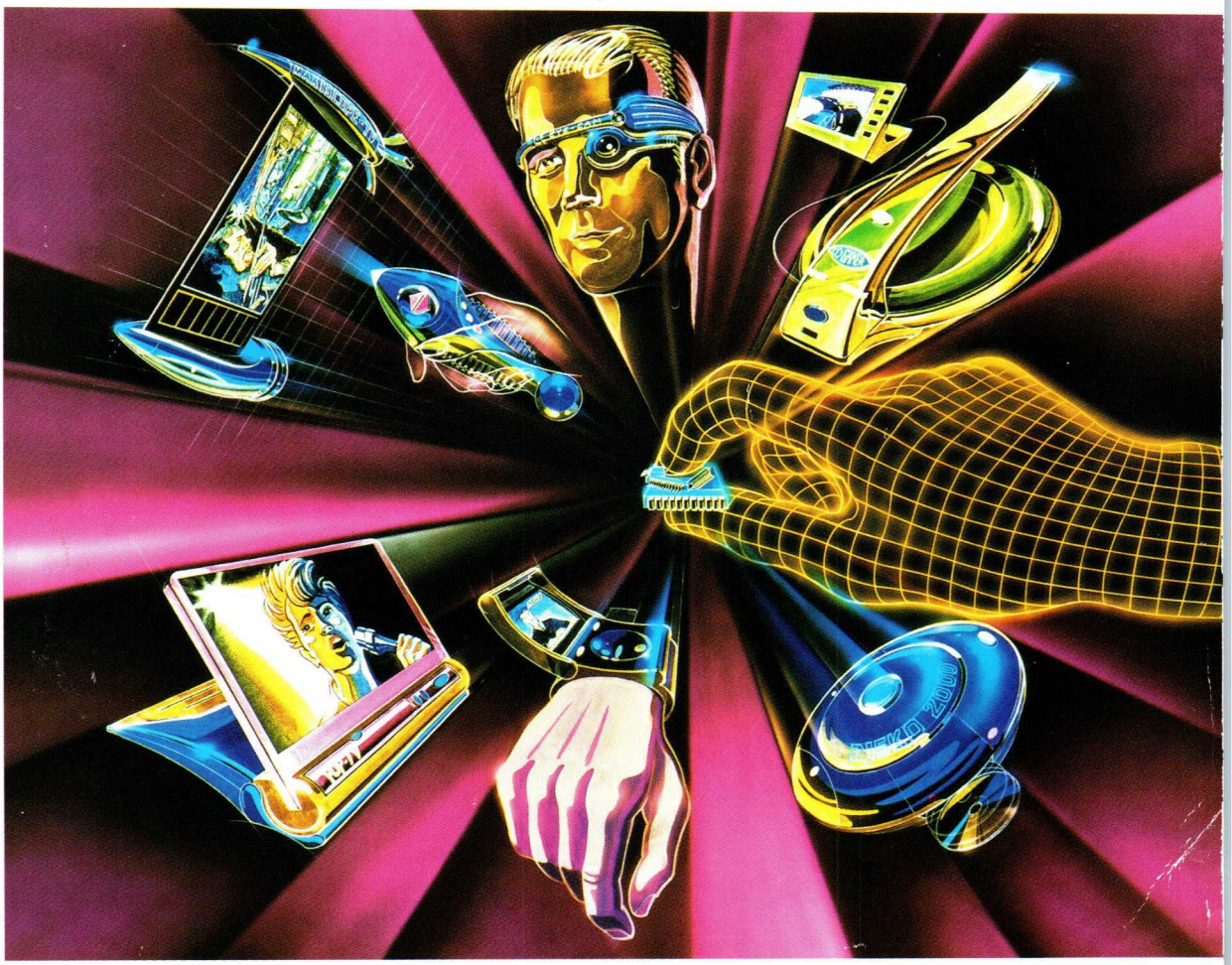
NTEGRATED CIRCUITS

Semiconductors for Television and Video Systems

TDA2578A to TDA8415



1995

DATA HANDBOOK IC02b

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Television and Video Systems

CONTENTS

	Page
PART A	
SELECTION GUIDE	
Functional index	4
Alphanumerical index	21
GENERAL	
Quality	36
Rating systems	37
Pro electron type numbering system of integrated circuits	39
Handling MOS devices	41
DEVICE DATA	
80/83C528 to TDA2555;TDA2557	44
PART B	
SELECTION GUIDE	
Functional index	1588
Alphanumerical index	1605
DEVICE DATA	
TDA2578A to TDA8415	1621
PART C	
SELECTION GUIDE	
Functional index	3236
Alphanumerical index	3253
DEVICE DATA	
TDA8416 to μA733;733C	3269
PACKAGE INFORMATION	
Package outlines	4789
Soldering	4845
DATA HANDBOOK SYSTEM	4847

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SELECTION GUIDE

	Page
Functional index	1588
Alphanumerical index	1605

		PAGE
TUNING/TUNER		
Tuning		
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8725T	Antenna signal processor	3785
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
TSA5527; TSA5527		
Tuner		
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BF547	NPN 1 GHz wideband transistor	128
BF747	NPN 1 GHz wideband transistor	133
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
SAA1300	Tuner switching circuit; I²C-bus	397
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701

		PAGE
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
Varicap		
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113

		PAGE
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BY229 series	Rectifier diodes fast, soft-recovery	156
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
Dual gate n-channel MOSFET		
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
IF		
Vision IF		
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301

		PAGE
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
Sound IF		
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
AM demodulator		
TDA9830	TV sound AM demodulator and audio source switch	4463
FM demodulator		
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
Nicam demodulator		
TDA8732	NICAM-728 demodulator (NIDEM)	3798

		PAGE
SOUND		
Sound decoding - Stereo decoder/dual language		
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
NICAM		
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SOUND		
Sound control		
TDA1029	Signal-sources switch	1461
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA9860	Universal hi-fi audio processor for TV	4607

		PAGE
Sound ADC		
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
SAD1009	Universal DAC (UDAC)	1395
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
Sound output		
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2905
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2907
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
VISION		
Colour decoding		
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027

		PAGE
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229

		PAGE
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA8395	SECAM decoder	3206
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4042
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I²C-bus	4148
TEA7650H	Video signal processor for CD-video/laser vision	4655
Video and high-speed ADC and DAC		
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636

		PAGE
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDF8704	8-bit high-speed analog-to-digital converter	4620
Memory based features		
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I^2C-bus	1359
Scan conversion		
PCF8570	256 × 8-bit static low-voltage RAM with I^2C-bus interface	308
SAA4940H	NOise reduction IC	490
SAA7158	Back END IC	1033
Video output		
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
High voltage transistors		
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127

		PAGE
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
SYNC/DEFLECTION/SMPS		
Sync and deflection		
BY228	Parallel efficiency diode	155
BY328	32 kHz parallel efficiency diode	157
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYW54 to 56	Controlled avalanche rectifier diodes	166
TDA1082	East-west correction driver circuit	1475
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4820T	Sync separation circuit for video applications	2473
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112

		PAGE
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA9150B	Programmable deflection controller; I²C-bus	4065
TDA9151B	Programmable deflection controller; I²C-bus	4094
Power supply		
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Combi		
TDA4504B	Small signal combination for multistandard colour TV	2075
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
CONTROL		
Clock/calendar		
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8593	Low power clock calendar; I²C-bus	338
Display drivers		
PCF1303T	18-element bar graph LCD driver	271
PCF2116 family	LCD controller/drivers; I²C-bus	276
PCF2114X; PCF2116X		
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326

		PAGE
LED driver		
SAA1064	4-digit LED driver with I²C-bus interface	373
On Screen Display (OSD)		
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
Memories - SRAM		
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
EEPROM		
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
MICROCONTROLLERS		
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I²C-bus	62
84C44X/84C64X/84C84X	8-bit microcontrollers with OSD and VST; I²C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	83
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontroller for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266

		PAGE
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
Remote I/O expanders		
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8584	I²C-bus controller	331
TDA8722	I²C-bus programmable modulator for negative video modulation and FM sound	3766
Remote control transmitter		
PCA84C122; 222;422; 622; 822	8-bit microcontrollers for remote control transmitters	245
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
TELETEXT		
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859

		PAGE
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SATELLITE TV		
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8735	PLL frequency synthesizer; I²C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA 8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I²C-bus control	3860
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
PAY TV		
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
Miscellaneous		
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219

		PAGE
TDA6800; TDA6800T	Video modulator circuit	2893
TDA8442	I²C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I²C-bus	3443
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
μA733; 733C	Differential video amplifier	4782
VCR/Camera/Recorder		
SAA1101	Universal sync generator (USG)	385
SAA1310	Control interface for VHS video recorders	400
SAA4700	VPS data line processor; I²C-bus	472
SAA4700T	VPS data line processor; I²C-bus	481
SAD1009	Universal DAC (UDAC)	1395
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I²C-bus	1421
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA6800; TDA6800T	Video modulator circuit	2893
TDA9610H	Audio FM processor for VHS hi-fi audio; I²C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I²C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TEA7650H	Video signal processor for CD-video/laser vision	4655

		PAGE
MONITOR CIRCUITS		
Sync		
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
Deflection		
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
SMPS		
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Video control		
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
Miscellaneous		
TDA8442	I^2C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I^2C-bus	3443

ALPHANUMERICAL INDEX

		PAGE
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I^2C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I^2C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I^2C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I^2C-bus	62
84C44X; 84C64X; 84C84X	8-bit microcontrollers with OSD and VST; I^2C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I^2C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I^2C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I^2C-bus	83
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118

		PAGE
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127
BF547	NPN 1 GHz wideband transistor	128
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF747	NPN 1 GHz wideband transistor	133
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
BY228	Parallel efficiency diode	155
BY229 series	Rectifier diodes fast, soft-recovery	156
BY328	32 kHz parallel efficiency diode	157

		PAGE
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
BYW54 to 56	Controlled avalanche rectifier diodes	166
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontrollers for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C122; 222; 422; 622; 822	8-bit microcontrollers for remote control transmitters	245
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
PCF1303T	18-element bar graph LCD driver	271
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF2116 family	LCD controller/drivers; I²C-bus	276
PCF2114X; PCF2116X		
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297

		PAGE
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8584	I²C-bus controller	331
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
PCF8593	Low power clock calendar	338
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
SAA1064	4-digit LED-driver with I²C-bus interface	373
SAA1101	Universal sync generator (USG)	385
SAA1300	Tuner switching circuit; I²C-bus	397
SAA1310	Control interface for VHS video recorders	400
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
SAA4700	VPS data line processor; I²C-bus	472
SAA4700T	VPS data line processor; I²C-bus	481
SAA4940H	NOise reduction IC	490
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635

		PAGE
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027
SAA7158	Back END IC	1033
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I²C-bus	1359
SAD1009	Universal DAC (UDAC)	1395

		PAGE
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I²C-bus	1421
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA1029	Signal-sources switch	1461
TDA1082	East-west correction driver circuit	1475
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733

		PAGE
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4504B	Small signal combination multistandard colour TV	2075
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135

		PAGE
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490

		PAGE
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/ oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773

		PAGE
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
TDA6800; TDA6800T	Video modulator circuit	2893
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2095
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2097
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072

		PAGE
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TDA8395	SECAM decoder	3206
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8442	I²C-bus interface for colour decoders	3421
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8444	Octuple 6-bit DAC with I²C-bus	3443
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646

		PAGE
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8722	I²C-bus programmable modulator for negative video modulation and FM sound	3766
TDA8725T	Antenna signal processor	3785
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8732	NICAM-728 demodulator (NIDEM)	3798
TDA8735	PLL frequency synthesizer; I²C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I²C-bus control	3860
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4042
TDA9150B	Programmable deflection controller; I²C-bus	4065
TDA9151B	Programmable deflection controller; I²C-bus	4094
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I²C-bus	4148
TDA9610H	Audio FM processor for VHS hi-fi audio; I²C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I²C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332

		PAGE
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TDA9830	TV sound AM demodulator and audio source switch	4463
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TDA9860	Universal hi-fi audio processor for TV	4607
TDF8704	8-bit high-speed analog-to-digital converter	4620
TDF8712	8-bit digital-to-analog converters	3711
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
TEA7650H	Video signal processor for CD-video/laser vision	4655
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A; TSA5527; TSA5527A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
µA733; 733C	Differential video amplifier	4782

DEVICE DATA

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0,15 to 1 V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

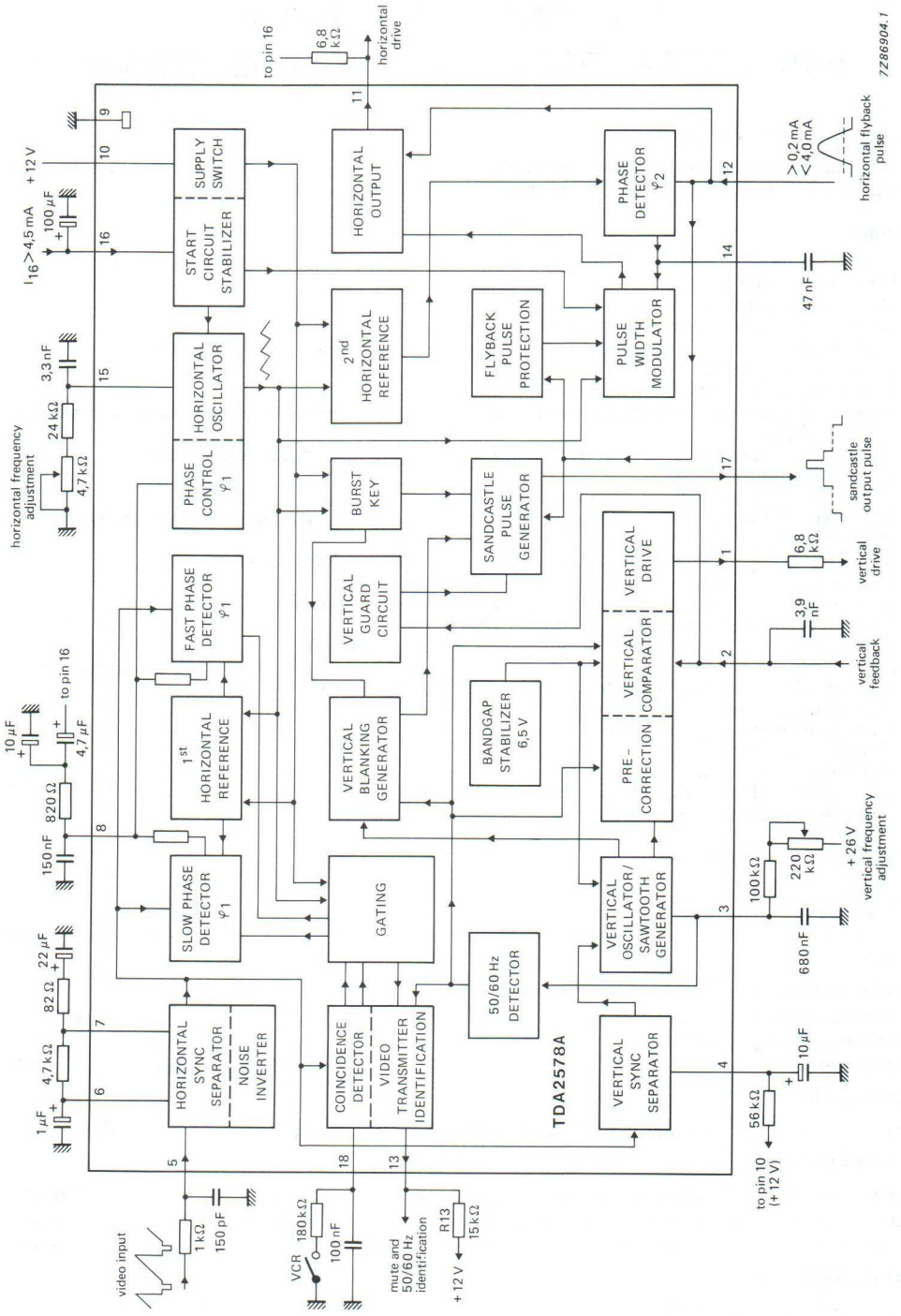


Fig. 1 Block diagram.

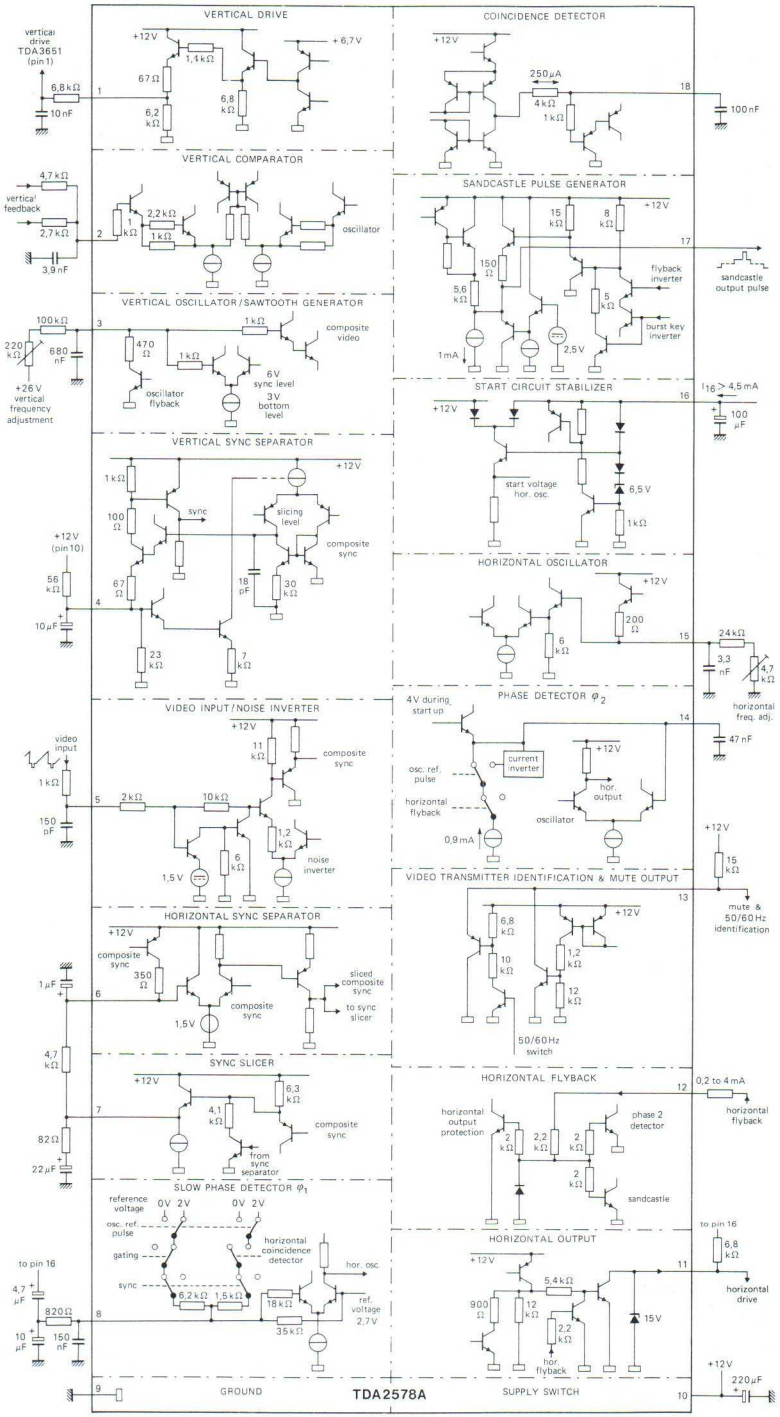


Fig. 2 TDA2578A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,1 W
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 65 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50 K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8 mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7 V
			8,0 to 9,5 V
Supply current (pin 10)	I_{10}	typ.	55 mA
		<	70 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
			10 to 13,2 V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1 V
			1,5 to 3,75 V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6 V
			0,15 to 1 V
Slicing level		typ.	50 %
			35 to 65 %
Delay between video input and detector output	t_1	typ.	0,35 μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7 V
		<	1 V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800 Hz
Catching range	Δf	typ.	± 800 Hz
			±600 to ±1100 Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse			
for slow time constant		typ.	1 kHz/μs
for fast time constant		typ.	2,75 kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	60	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ; no sync)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	$V_{11\text{-}9}$	<	13,2	V
Voltage at which protection starts	$V_{11\text{-}9}$		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	$V_{11\text{-}9}$	typ. <	0,3 0,5	V V
normal condition at I_{11} = 40 mA	$V_{11\text{-}9}$	typ. <	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ. 	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during:				
burst key	$V_{17\text{-}9}$	>	10	V
horizontal blanking	$V_{17\text{-}9}$	typ. 	4,6 4,2 to 5	V V
vertical blanking	$V_{17\text{-}9}$	typ. 	2,5 2 to 3	V V
Pulse duration				
burst key	t_p	typ. 	3,7 3,3 to 4,1	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking				
at 50 Hz	21 lines			
at 60 Hz	17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ. 4,8 to 5,6	5,2 μs μs
Delay between start of sync and trailing edge of burst key	t_2	typ. 8,1 to 9,3	8,8 μs μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ. 3,2 to 3,8	3,5 V V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ. 1,0 to 1,4	1,2 V V
vertical period counter 3 periods fast	V_{18-9}	typ. 0,08 to 0,16	0,12 V V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ. 1,5 to 1,9	1,7 V V
Switching level fast to slow (locking)	V_{18-9}	typ. 4,7 to 5,3	5,0 V V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ. 8,2 to 9,0	8,6 V V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	< typ.	0,5 V 0,3 V
Sink current active (no sync)	I_{13}	⩽	5 mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1 μA
50/60 Hz identification (pin 13)			
R13 = 15 kΩ to + 12 V (note 5) at f = 50 Hz (in sync condition)	V_{13-9}	typ.	V_{10-9} V
at f = 60 Hz (in sync condition)	V_{13-9}	typ. 7,2 to 8	7,6 V V
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	<	4 %
Synchronization range (note 6)		typ.	33 %
Input current at V_{3-9} = 6 V	I_3	<	3 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	0,8 V
Input current at V_{2-9} = 6 V	I_2	<	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	<	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)			
switching level low	V_{2-9}	typ.	3,35 V
			3,0 to 3,7 V
switching level high	V_{2-9}	typ.	5,15 V
			4,75 to 5,55 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

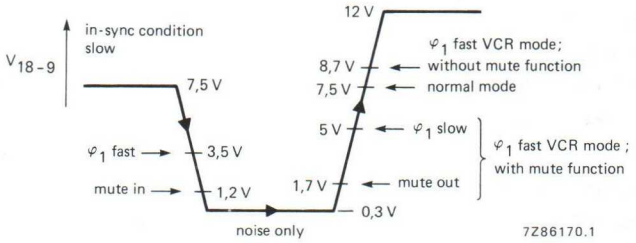


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 4,2 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

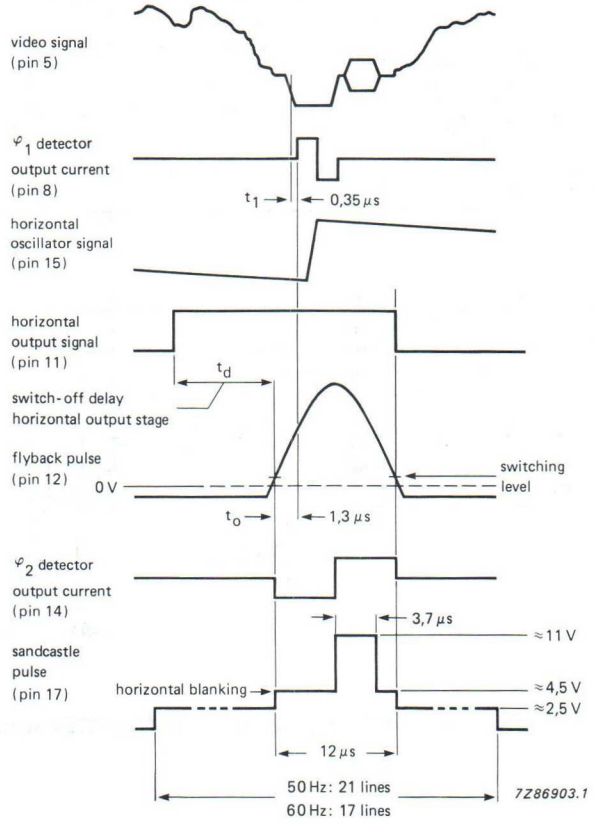
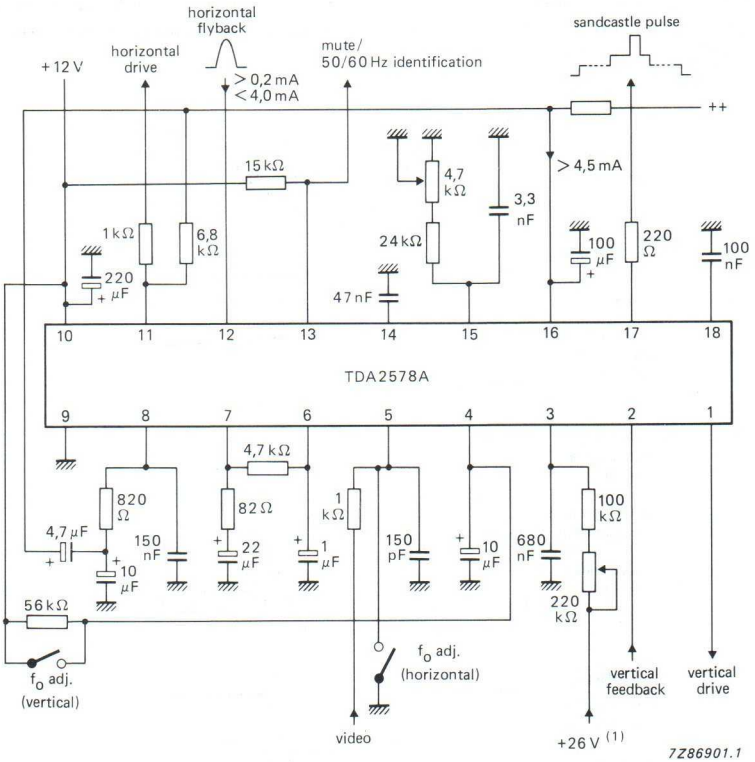


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

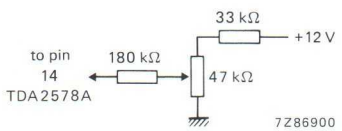


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

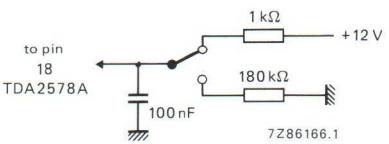


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

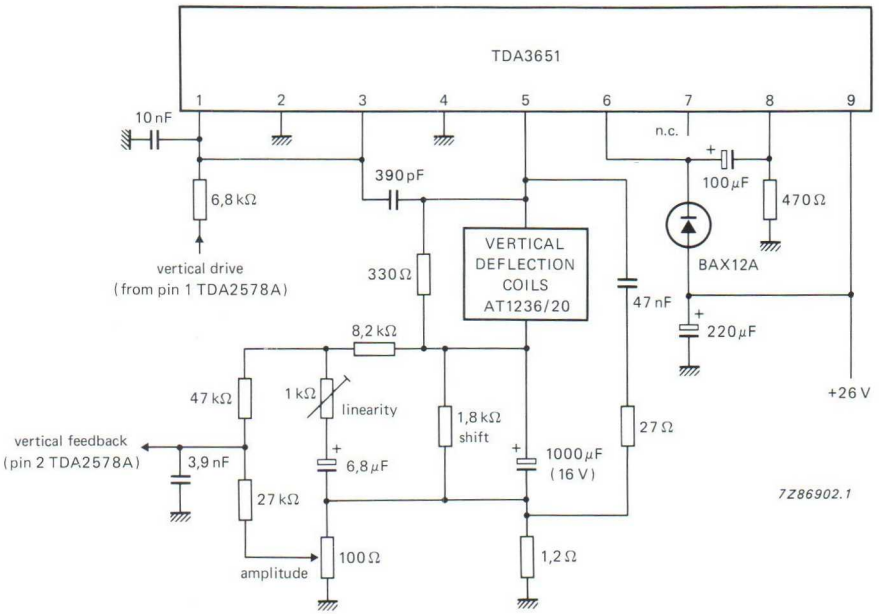


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

HORIZONTAL/VERTICAL SYNCHRONIZATION CIRCUIT

GENERAL DESCRIPTION

The TDA2579B generates and synchronizes horizontal and vertical signals. The device has a 3 level sandcastle output; a transmitter identification signal and also 50/60 Hz identification.

Features

- Horizontal phase detector, (sync to oscillator), sync separator and noise inverter
- Triple current source in the phase detector with automatic selection
- Second phase detector for storage compensation of the horizontal output
- Stabilized direct starting of the horizontal oscillator and output stage from mains supply
- Horizontal output pulse with constant duty cycle value of 29 μs
- Internal vertical sync separator, and two integration selection times
- Divider system with three different reset enable windows
- Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified
- Vertical comparator with a low DC feedback signal
- 50/60 Hz identification output combined with mute function
- Automatic amplitude adjustment for 50 and 60 Hz and blanking pulse duration
- Automatic adaption of the burst-key pulsewidth

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Minimum required current for starting horizontal oscillator and output stage		I_{16}	6.2	–	–	mA
Main supply voltage		V_{10}	–	12	–	V
Supply current		I_{10}	–	70	–	mA
Input signals						
Sync pulse input amplitude		$V_{5(p-p)}$	0.05	–	1.0	V
Horizontal flyback pulse input current		I_{12}	–	1	–	mA
Vertical comparator input signal						
Voltage AC		V_2	–	0.8	–	V
Voltage DC		V_2	–	1	–	V
Output signals						
Horizontal output (open collector) I_{11} = 25 mA		V_{11}	–	–	0.5	V
Vertical output stage driver (emitter follower) I_1 = 1.5 mA		V_1	5	–	–	V
Sandcastle output levels						
V_{17} burst-key		V_{17}	9.8	–	–	V
horizontal blanking		V_{17}	–	4.5	–	V
vertical blanking		V_{17}	–	2.5	–	V
Video transmitter identification output stage (open collector loaded with external resistor to positive supply). No sync. pulse present		V_{13}	–	–	0.5	V
		I_{13}	–	–	5	mA
Sync pulse present						
divider ratio > 576		V_{13}	–	V_{10}	–	V
divider ratio < 576		V_{13}	–	7.65	–	V

PACKAGE OUTLINE

18-lead dual in line; plastic (SOT102).

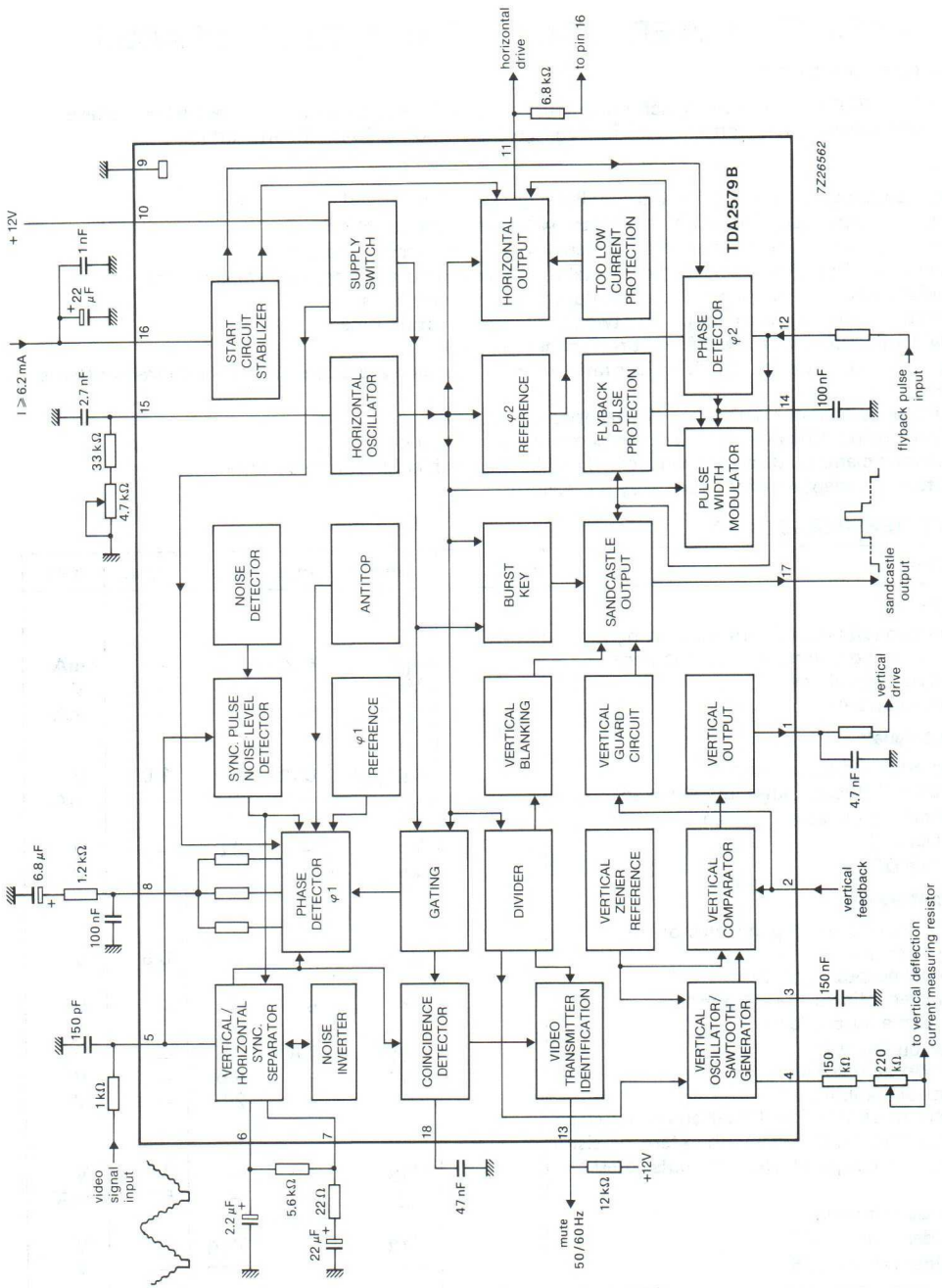


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Vertical part (pins 1,2,3,4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60 Hz to 50 Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync pulse is within the searched window. The count is decreased by 1 when the vertical sync pulse is not present.

Large (search) window: divider ratio between 488 and 722

This mode is valid for the following conditions:

1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
4. Externally setting. This can be reached by loading pin 18 with a resistor of 220 kΩ to earth or connecting a 3.6 V diode stabistor between pin 18 and ground.

Narrow window: divider ratio between 522-528 (60 Hz) or 622-628 (50 Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

Standard TV-norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14 the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No-TV-transmitter found: (pin 18 < 1.2 V)

In this condition, only noise is present, the divider is rest to count 628. In this way a stable picture display at normal height is achieved.

DEVELOPMENT DATA

Video tape recorders in feature mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no-TV-transmitter detection circuit can be activated as pin V_{18} drops below 1.2 V. This would imply a rolling picture (see Phase detector, sub paragraph d). In general VTR-machines use a re-inserted vertical sync pulse in the feature mode. Therefore the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2 V is inhibited when a vertical sync pulse is detected.

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b and c the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 8 for 50 Hz and count 10 for 60 Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines) for 60 Hz, and at count 44 (22 lines) for 50 Hz systems. The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF (see Fig. 1).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.85 V for the 50 Hz system or 4.85 V for the 60 Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source, the value of which can be set by an external resistor between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of $\approx$ 7.5 volts. The recommended operating current range is 10 to 75 μA. The resistance at pin R_4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between pin 4 and pin 3, or by connecting the pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of pin 4. The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V. Due to the automatic system adaption both values are valid for 50 Hz and 60 Hz.

The low DC voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous level of 2.5 V in the sandcastle output signal of pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 170 Ω. The output pin is also connected to an internal current source with a sink current of 0.25 mA.

Sync separator, phase detector and TV-station identification (pins 5,6,7,8 and 18)

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level value is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor between pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100 \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between pins 6 and 7 and top sync level equals 100%. The recommended resistor value is 5.6 kΩ.

Black level detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV-transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.

DEVELOPMENT DATA

Noise level detector

An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V. The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level of 19 dB is detected a counter circuit is activated. A video input signal is processed as "acceptable noise free" when 12 out of 15 sync pulses have a noise level below 19 dB for two successive frame periods. The sync pulses are processed during a 15 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse phase detection. At the same time the integration time of the vertical sync pulse separator is adapted.

$$S/N = 20 \text{ Log } \frac{\text{Video voltage (black to white}_{p\text{-}p})}{\text{Noise}_{rms}}$$

Phase detector

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync-pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by 1.5 times. In this way there is no requirement for external VTR time constant switching, and so all station numbers are suitable for signals from VTR, video games or home computers.
For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods during the vertical scan period.

The horizontal oscillator will now lock to the new TV-station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched OFF and the divider is set to the large window. In general the mute signal is switched OFF within 5 ms (pin C_{18} = 47 nF) after reception of a new TV-signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the frame counter is switched OFF and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync-noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to ≈ 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition. The current is also reduced during the vertical blanking period by 1 mA. When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect pin 18 to earth (pin 9).
b. Fast time constant TV transmitter identification circuit active, connect a resistor of 220 kΩ between pin 18 and ground.
   This condition can also be set by using a 3.6 V stabistor diode instead of a resistor.
c. Slow time constant, (with exception of frame blanking period), connect pin 18 via a resistor of 10 kΩ to + 12 V, pin 10. In this condition the transmitter identification circuit is not active.
d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8 V zener diode between pin 18 and ground.

Fig. 2 illustrates the operation of the 3 phase detector circuits.

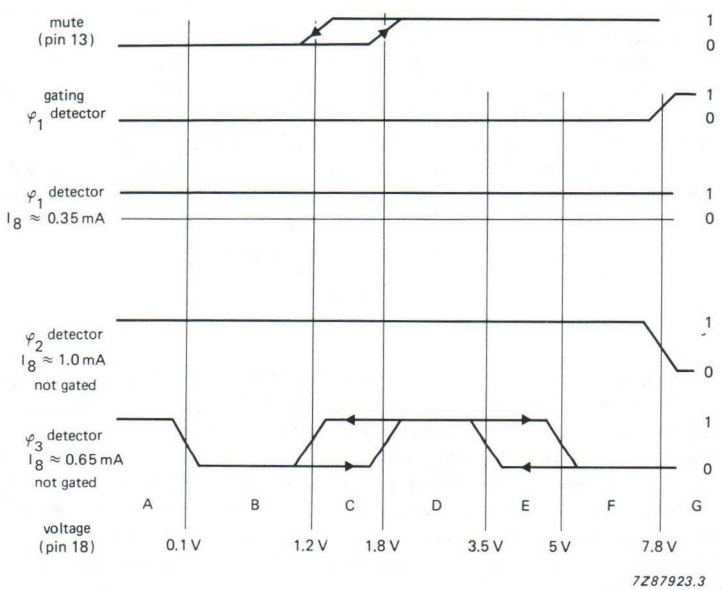


Fig. 2 Timing diagram, phase detectors.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into pin 16.

The horizontal oscillator starts at a supply current of approximately 4 mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5 mA. The circuit has been designed so that after starting the horizontal output function a current drop of $\approx$ 1 mA is allowed. The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switched mode power supplies. The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C). The main supply should be connected to pin 10, and pin 9 should be used as ground. When the voltage on pin 10 increases from zero to its final value (typically 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes, and the voltage on pin 16 will stabilize to a typical value of 9.4 V.

In a stabilized condition (pin $V_{10} > 10$ V) the minimum required supply current to pin 16 is $\approx$ 2.5 mA. All other IC functions are switched on via the main supply voltage on pin 10. When the voltage on pin 10 reaches a value of $\approx$ 7 V the horizontal phase detector circuit is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 which is typically 9.4 V.

To close the second phase detector loop, a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.

For remote switch-off pin 16 can be connected to ground (via a npn transistor with a series resistor of $\approx$ 500 Ω) which switches off the horizontal output.

Horizontal oscillator, horizontal output transistor, and second phase detector (pins 11, 12, 14 and 15)

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground, pin 9. The open collector horizontal output stage is connected to pin 11. An internal zener diode configuration limits the open voltage of pin 11 to $\approx$ 14.5 V.
The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of $\approx$ 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of $\approx$ 40% HIGH.

The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched OFF and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%.

The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration is 29 μs HIGH for storage times between 1 μs and 17 μs (flyback pulse of 12 μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 50/60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV-transmitter) the npn transistor is switched ON.
When the voltage on pin 18 increases to a level of $\approx$ 1.8 V (new TV-transmitter found) the npn transistor is switched OFF.

Pin 13 has also the possibility for 50/60 Hz identification. This function is available when pin 13 is connected to pin 10 (+ 12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV-transmitter is identified the voltage on pin 13 will be LOW ($<$ 0.5 V). When a TV-transmitter with a divider ratio $>$ 576 (50 Hz) is detected the output voltage of pin 13 is HIGH (+ 12 V).
When a TV-transmitter with a divider ratio $<$ 576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force this pin output voltage down to $\approx$ 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17, has three different voltage levels. The highest level, (10.4 V), can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12, and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 50 Hz the blanking pulse duration is 44 clock pulses and for 60 Hz it is 34 clock pulses started from the vertical divider reset. For TV-signals which have a divider ratio between 622 and 628 or between 522 and 528 the pulse is started at the first equalizing pulse. With the 50/60 Hz information the burst-key pulse width is switched to improve the behaviour in multi-norm concepts.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Start current	I_{16}	–	9.7	mA
Supply voltage	V_{10}	–	13.2	V
Total power dissipation	P_{tot}	–	1.2	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C

Thermal resistance

From junction to ambient in free air $R_{th\ j\text{-}a}$ 50 K/W

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; I_{16} = 6.2 mA; V_{10} = 12 V; unless otherwise specified
Voltage measurements are taken with respect to pin 9 (ground)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current (pin 16)						
V_{10} = 0 V		I_{16}	6.2	–	9.7	mA
V_{10} = 10 V		I_{16}	2.5	–	9.7	mA
Stabilized voltage (pin 16)		V_{16}	8.8	9.3	9.7	V
Current consumption (pin 10)		I_{10}	–	70	85	mA
Supply voltage range (pin 10)		V_P	10	12	13.2	V
Video input (pin 5)						
Top sync level		V_5	1.5	3.1	3.75	V
Sync pulse amplitude (peak-to-peak value)	note 1	$V_{5(p-p)}$	0.05	0.6	1.0	V
Slicing level	note 2		35	50	65	%
Delay between video input and detector output (see also Fig. 3)			0.2	0.3	0.55	µs
Sync pulse noise level detector circuit active	note 3	S/N	–	19	–	dB
Sync pulse						
Noise level detector circuit hysteresis			–	3	–	dB
Noise gate (pin 5)						
Switching level		V_5	–	+ 0.7	+ 1	V
First control loop (pin 8) (horizontal oscillator to sync)						
Holding range		Δf	–	± 800		Hz
Catching range		Δf	± 700	± 800	± 1100	
Control sensitivity video with respect to burst-key and flyback-pulse						
Slow time constant			–	2	–	kHz/µs
Normal time constant			–	5	–	kHz/µs
Fast time constant			–	3	–	kHz/µs
Phase modulation due to hum on the supply line (pin 10)	note 4		–	0.2	–	µs/Vtt
Phase modulation due to hum on input current (pin 16)	note 4		–	0.08	–	µs/Vtt

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Second control loop (pin 14) (horizontal flyback to horizontal oscillator)						
Control sensitivity	t_d = 10 μs	$\Delta t_d/\Delta t_o$	200	300	600	μs
Control range		t_d	1	–	>45	μs
Control range for constant duty factor horizontal output		t_d	1	29 (–t flyback pulse)		μs
Controlled edge of horizontal output signal (pin 11)				positive		
Phase adjustment (pin 14) (via second control loop)						
Control sensitivity	t_d = 10 μs		–	25	–	μA/μs
Maximum allowed control current		I_{14}	–	–	± 60	μA
Horizontal oscillator (pin 15)	C = 2.7 nF; R_{osc} = 34.8 kΩ					
Frequency (no sync)		f	–	15625	–	Hz
Spread (fixed external component, no sync)		Δf	–	–	± 4	%
Frequency deviation between starting point output signal and stabilized condition		Δf	–	+ 5	+ 8	%
Temperature coefficient		T_C	–	-1.10^{-4}	–	/K
Horizontal output (pin 11) (Open collector)						
Output voltage high		V_{11}	–	–	13.2	V
Start voltage protection (internal zener diode)		V_{11}	13	–	15.8	V
Low input current (pin 16) protection output enabled		I_{16}	–	5.0	6.2	mA
Output voltage low start condition	I_{11} = 10 mA	V_{11}	–	0.1	0.5	V
Duty factor output current during starting	I_{16} = 6.2 mA		50	60	70	%
Output voltage low normal condition	I_{11} = 25 mA	V_{11}	–	0.3	0.5	V
Duty factor output current without flyback pulse (pin 12)			45	50	55	%
Duration of the output pulse HIGH	t_d = 10 μs		27	29	31	μs
Controlled edge				positive		
Temperature coefficient horizontal output pulse			–	-5.10^{-2}	–	μs/°C
Influence of delay time on pulse width of the horizontal output signal		$\Delta H_W/t_d$	–	0.16	–	μs/μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle output signal (pin 17)	I_L = 1 mA					
Output voltage during:						
burst-key		V_{17}	9.8	10.4	–	V
horizontal blanking		V_{17}	4.1	4.5	4.9	V
vertical blanking	I_L = 0.3 mA	V_{17}	2.1	2.5	2.9	V
Zero level output voltage	I_{sink} = 0.5 mA	V_{17}	–	–	0.7	V
Pulse width:						
burst-key (50 Hz)		t_p	3.85	4.15	4.6	µs
burst-key (60 Hz)		t_p	3.40	3.65	4.0	µs
Horizontal blanking		V_{12}	–	1.0	–	V
Vertical blanking	note 5					
Phase position burstkey time between middle sync pulse at pin 5 and start of burst pulse at pin 17			2.3	2.7	3.1	µs
Time between start sync pulse and end of burst pulse at pin 17						
(50 Hz)			–	9.3	9.7	µs
(60 Hz)			–	8.8	9.2	µs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Fig. 1)						
Detector output current		I_{18}	–	0.25	–	mA
Voltage level for in sync condition (φ_1 normal)		V_{18}	5.8	6.5	7.0	V
Voltage for noisy sync pulse (φ_1 slow and gated)		V_{18}	9	10	–	V
Voltage level for noise only	note 6	V_{18}	–	0.3	–	V
Switching level normal to fast		V_{18}	< 3.2	3.5	3.8	V
Switching level mute output active and fast to normal		V_{18}	< 1.0	1.2	1.4	V
Switching level frame period counter (3 periods fast)		V_{18}	< 0.08	0.12	0.16	V
Switching level: normal to fast (locking) mute output inactive		V_{18}	> 1.5	1.75	2.0	V
Switching level fast to normal (locking)		V_{18}	> 4.7	5.0	5.3	V
Switching level normal to slow (gated sync pulse)		V_{18}	7.4	7.8	8.2	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Video transmitter identification output (pin 13)						
Output voltage active (no sync)	I_{13} = 1 mA	V_{13}	–	0.15	0.32	V
Sink current active (no sync)	$V_{13} < 1$ V	I_{13}	–	–	5	mA
Output current inactive (sync 50 Hz)		I_{13}	–	–	1	μA
50/60 Hz identification (pin 13) (R_{13} positive supply 12 kΩ)						
Emitter follower, pnp:						
60 Hz: $\frac{2 \times f_H}{f_V} <$ 576 voltage		V_{13}	7.2	7.65	8.1	V
50 Hz: $\frac{2 \times f_H}{f_V} >$ 576 voltage		V_{13}	–	V_{10}	–	V
Flyback input pulse (pin 12)						
Switching level		V_{12}	–	+1	–	V
Input current		I_{12}	+0.2	–	+3	mA
Input pulse		V_{12}	–	–	12	V_P
Input resistance			–	3.5	–	kΩ
Phase position without shift time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		t_d	2.1	2.5	2.9	μs
Vertical ramp generator (pin 3)						
Pulse width charge current		–	–	26	–	clock pulses
Charge current		I_3	–	3	–	mA
Top level ramp signal voltage						
Divider in 50 Hz mode	note 7	V_3	5.5	5.85	6.3	V
Divider in 60 Hz mode	note 7	V_3	4.55	4.85	5.25	V
Ramp amplitude	C_3 = 150 nF,					
R_4 = 330 kΩ 50 Hz	note 7		–	3.1	–	V_P
R_4 = 330 kΩ 60 Hz	note 7		–	2.5	–	V_P
Temperature coefficient	I_4 = 30 μA	I_3	–	+ 100	–	10^{-6}/K

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Current source (pin 4)						
Output voltage	$I_4 = 20\ \mu A$	V_4	7.0	7.5	7.9	V
Allowed current range		I_4	10	–	75	μA
Temperature coefficient output voltage	$I_4 = 30\ \mu A$	TC	–	+ 50	–	$10^{-6}/K$
Comparator (pin 2)	$C_3 = 150$ nF; $R_4 = 330\ k\Omega$					
Input voltage						
DC level	note 7	V_2	0.97	1.07	1.17	V
AC level		V_2	–	0.8	–	V_P
Deviation amplitude 50/60 Hz			–	1.75	2.5	%
Vertical output stage (pin 1) (npn emitter follower)						
Output voltage	I_o pin 1 = +1.5 mA note 7	V_1	5.0	5.5	6.3	V
R_S, sync separator resistor			–	170	–	Ω
Continuous sink current			–	0.25	–	mA
Vertical guard circuit (pin 2)						
Active ($V_{17} = 2.5$ V)						
Switching level LOW	note 7	V_2	> 1.7	1.85	2.0	V
Switching level HIGH	note 7	V_2	< 0.25	0.35	0.45	V

Notes to the characteristics

1. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. $S/N = 20 \log \frac{\text{video voltage black to white (p-p)}}{\text{noise (rms)}}$

   measured with 1 $V_{p\text{-}p}$ video input
4. Measured between pin 5 and sandcastle output pin 17.
5. Divider in search (large) mode:

   start: reset divider = start vertical sync plus 1 clock pulse

   stop: $n = \frac{2 \times f_H}{f_V} > 576$ clock pulse 44

   $n = \frac{2 \times f_H}{f_V} < 576$ clock pulse 34

   Divider in small window mode:

   start: clock pulse 517 (60 Hz) clock pulse 618 (50 Hz)

   stop: clock pulse 34 (60 Hz) clock pulse 44 (50 Hz)
6. Depends on DC level of pin 5, given value is valid for $V_5 \approx 5$ V.
7. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

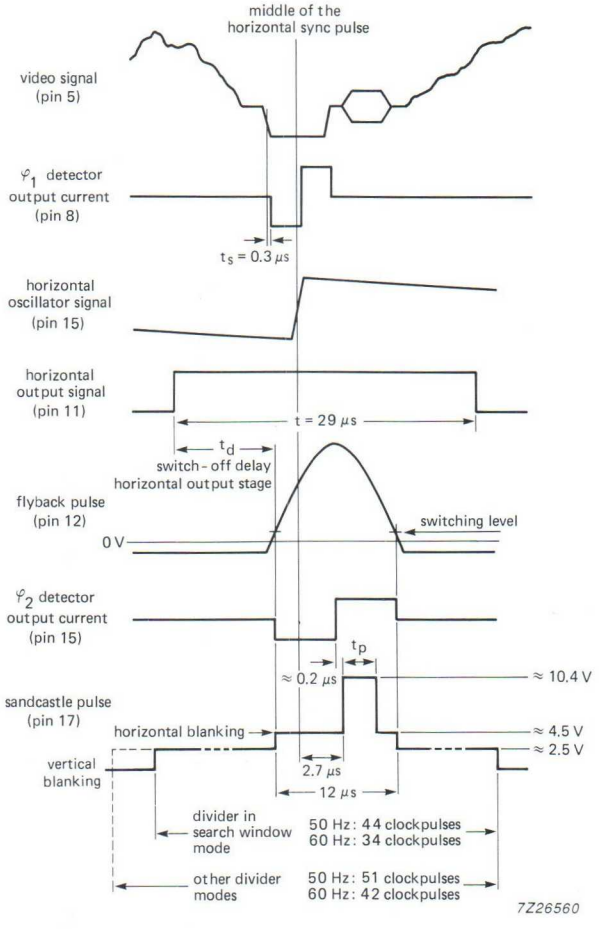


Fig.3 Timing diagram of the TDA2579B.

APPLICATION INFORMATION

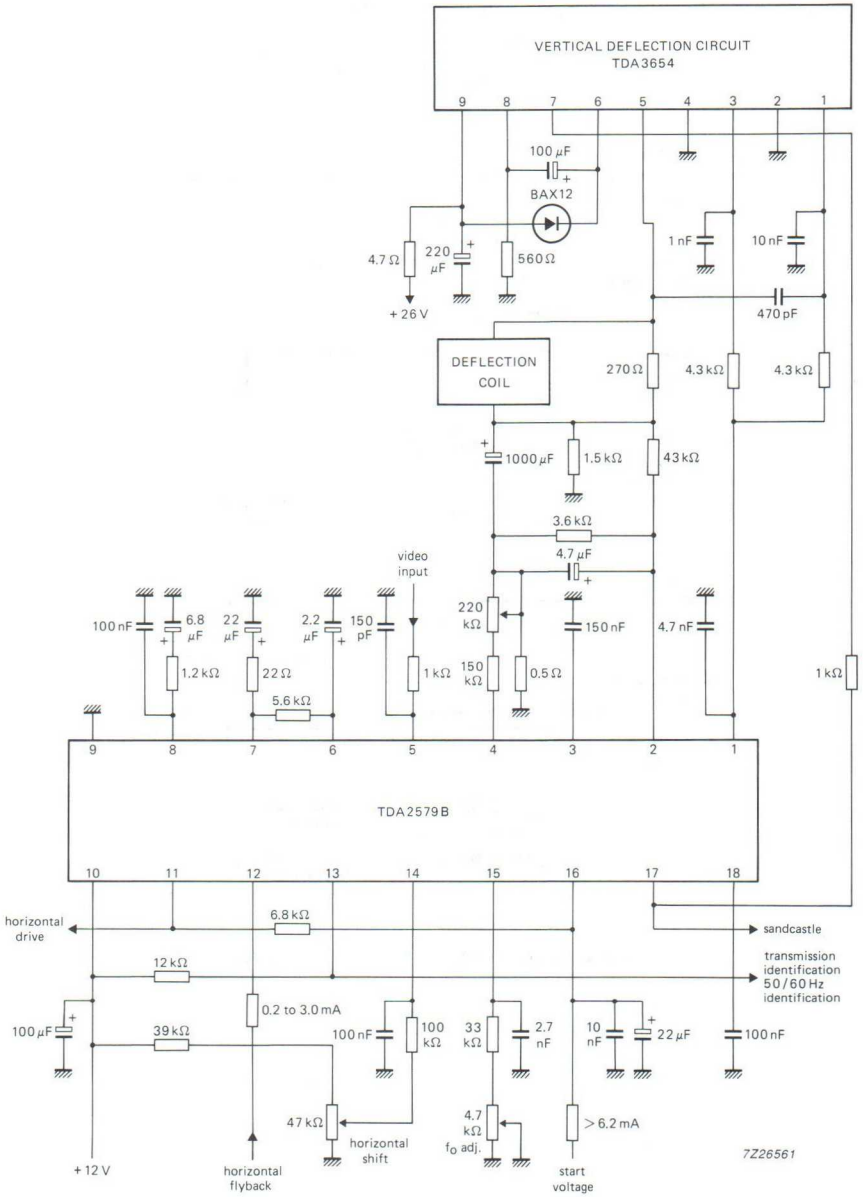


Fig.4 TDA2579B 110° application circuit (45AX).

Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

FEATURES

Synchronization and horizontal part

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Triple current source in the phase detector with automatic selection
- Normal phase detector time constant is increased to fast during the vertical blanking period (external switching for VTR conditions not necessary)
- Slow phase detector time constant and gated sync pulse operation are automatically switched on by an internal sync pulse noise level detection circuit
- Fast phase detector time is switched on for locking
- Time constant externally switchable
- Inhibit of horizontal phase detector and video transmitter identification circuit during equalizing pulses and vertical sync pulse
- Inhibit of horizontal phase detector during separated vertical sync pulse
- Second phase detector for storage compensation of the line output stage
- 3-level sandcastle pulse generator
- Automatic adaption of the burst key pulse width
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Horizontal output current with constant duty factor value of 55%
- Duty factor of the horizontal output pulse is 55% when the horizontal flyback pulse is absent.

Vertical part

- f_V = 60 Hz (M) system
- Vertical synchronization pulse separator without external components and two integration times
- Zener diode reference voltage source for the vertical sawtooth generator and vertical comparator
- Divider system with three different reset enable windows
- Synchronization is set to 528 divider ratio when no vertical sync pulse and no video transmitter is identified
- Divider window is forced to wide window when a vertical sync pulse is detected within the window provided by reset divider and end of vertical blanking period, on condition that the voltage on pin 18 is ≤1.2 V
- Divider ratio is 528 (f_V = 60 Hz) for DC signal on pin 5
- Linear negative-going sawtooth generated via the divider system (no frequency adjustment)
- Comparator with low DC level feedback signal
- Output stage driver
- f_V = 60 Hz identification output combined with mute function
- Start of vertical blanking is shifted to the start of the pre-equalizing pulses when the divider ratio is between 522 and 528 lines per picture
- Guard circuit which generates the vertical blanking pulse level on the sandcastle output pin 17 when the feedback level at pin 2 is not within the specified limits.

GENERAL DESCRIPTION

The TDA2579C is an integrated circuit generating all requirements for synchronization of its horizontal oscillator and output stage plus those of the vertical part which comprises a divider system, sawtooth generator, comparator and output stage.
The TDA2579C is almost identical to the TDA2579B. It is optimized for the M (60 Hz) TV system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2579C	18	DIL	plastic	SOT102

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{16}	minimum required current for starting horizontal oscillator and output stage		6.2	–	–	mA
V_{10}	main supply voltage		–	12	–	V
I_{10}	supply current		–	70	–	mA
Input signals						
V_{5-9}	sync pulse input amplitude		0.05	–	1	V
I_{12}	horizontal flyback pulse input current		0.2	1	–	mA
V_2	vertical comparator input voltage					
	AC (peak-to-peak value)		–	0.8	–	V
	DC		–	1	–	V
Output signals						
V_{11}	horizontal output voltage (open collector)	I_{11} = 25 mA	–	–	0.5	V
V_1	vertical output stage driver (emitter follower)	I_1 = 1.5 mA	5	–	–	V
V_{17}	sandcastle output voltage levels					
	burst key		9.8	–	–	V
	horizontal blanking		–	4.5	–	V
	vertical blanking		–	2.5	–	V
VIDEO TRANSMITTER IDENTIFICATION OUTPUT; note 1						
V_{13}	output voltage	no sync pulse present	–	–	0.32	V
I_{13}	output current	no sync pulse present	–	–	5	mA
V_{13}	output voltage	sync pulse present; divider ratio <576	–	7.6	–	V

Note

1. Open collector loaded with external resistor to positive supply.

Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

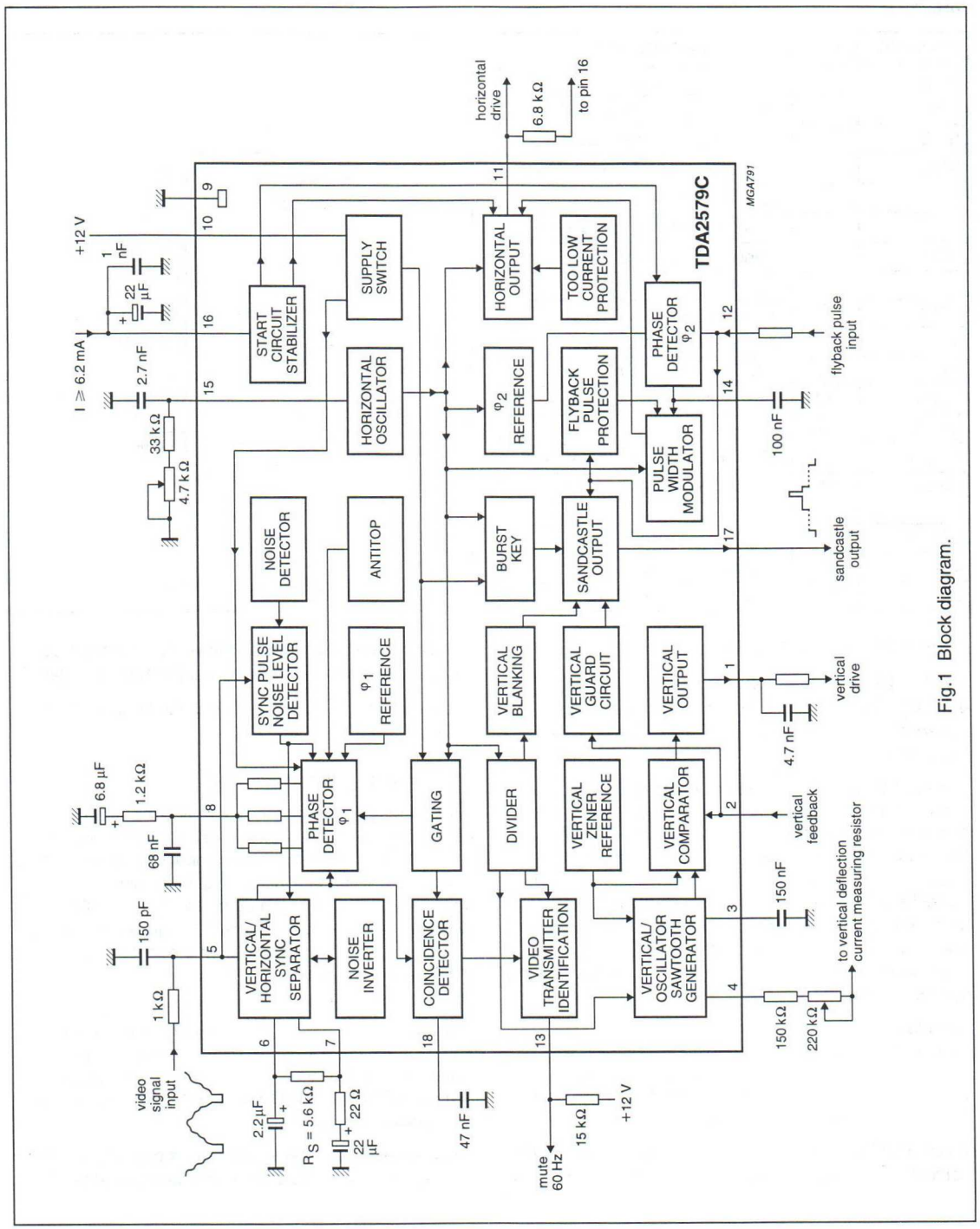


Fig.1 Block diagram.

Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

PINNING

SYMBOL	PIN	DESCRIPTION
V_{OUT}	1	vertical driver output
FB	2	vertical feedback input
SAW	3	vertical sawtooth generator
VDC	4	vertical deflection current output
VID	5	video signal input
CSL	6	slicing level storage capacitor
RSL	7	slicing level resistor
φ_1	8	phase detector φ_1
GND	9	ground (0 V)
V_P	10	main supply voltage (+12 V)
H_{OUT}	11	horizontal driver output
FLYB	12	horizontal flyback pulse input
MUTE	13	mute output
H_{SHIFT}	14	horizontal picture shift capacitor
H_{OSC}	15	horizontal oscillator frequency setting
STAB	16	start circuit stabilizer input
SC	17	sandcastle output
DET	18	coincidence detector output

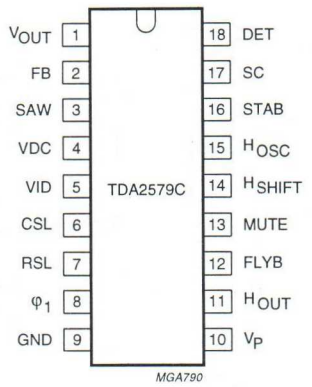


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2579C generates both horizontal and vertical drive signals, a 3-level sandcastle output pulse, a transmitter identification signal and 60 Hz window information.

The horizontal oscillator and horizontal output stage functions are started via the supply current into pin 16. The required current has a typical value of 5 mA which can be taken directly from the mains rectifier. The horizontal output transistor at pin 11 is not conducting until the supply current at pin 16 has reached its typical value. The starting circuit has a hysteresis of approximately 1 mA. The horizontal output current of pin 11 starts at a duty cycle of 60%. All other IC functions are enabled via the main supply voltage on pin 10.

The pin 16 supply system enables slaved synchronized switch mode systems in which the horizontal output signal of the TDA2579C is used as master signal. In such a system the 12 V supply (main supply at pin 10) can be generated by the line output stage.

An internal Zener diode reference voltage is used for the vertical processing part. The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. Thus no vertical frequency adjustment is required.

The circuit operation is restricted to the M (f_V = 60 Hz) system.

Vertical part (pins 1, 2, 3 and 4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, thus the horizontal oscillator is operating at its nominal line frequency and one line period equals 2 clock pulses. No vertical frequency adjustment is required due to the divider system. The divider system operates with 3 different reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its value by 1 each time the separated vertical sync pulse is within the window being searched. The count is reduced by 1 when the vertical sync pulse is not present.

The reset of the counter system (clock pulse 0) is at half a line period after the start of the vertical pulse at pin 5.

In accordance with the convention for the M system, field one line 1 number 1 starts at the first equalizing pulse, the reset of the divider system is at the start of line 4 for the first field and in the middle of line 265 for the second field.

Divider system

MODE A: LARGE (SEARCH) WINDOW

Divider ratio between 488 and 576.

This mode is valid for the following five conditions:

1. Divider is locking to a new transmitter.
2. Divider ratio found, not being within the narrow window limits.
3. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
4. External forced setting. This can be achieved by loading pin 18 with a 220 Ω resistor to earth or by connecting a 3.6 V stabistor diode between pin 18 and ground.
5. A vertical sync pulse was detected within the interval provided by reset divider (at 528) and the end of the vertical blanking while the voltage at pin 18 is ≤1.2 V.

MODE B: NARROW WINDOW

Divider ratio between 522 and 528.

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses in the large window mode. When count 12 is reached the vertical sync pulse is tested for the standard TV-norm being the divider ratio 525. When this value is valid for the 12th vertical pulse, the up/down counter is reset to 0 and the up/down counter tests for a valid 525 divider ratio. When at the 12th vertical pulse the divider ratio is not equal to n = 525 then the divider system remains in the narrow window mode and remains testing for the standard TV-norm. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

MODE C: STANDARD TV-NORM

Divider ratio 525; f_V = 60 Hz.

When the up/down counter has reached its maximum value of 12 in the narrow window mode and the divider ratio equals n = 525 the information applied to the up/down counter is changed such that now the standard divider ratio value is tested and the up/down counter is reset to 0. When the up/down counter reaches the value of 14 approved M TV-norm pulses the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition provides maximum protection for video recorders playing tapes with anti-copy guards.

MODE D: NO TV TRANSMITTER FOUND

At pin 18 the voltage level is less than 1.2 V.

In this condition, only noise is present and no vertical sync pulse is detected, the divider is reset to count 528. In this way a stable picture display at normal height is achieved.

MODE E: VIDEO TAPE RECORDERS IN FEATURE MODE

NTSC (M system) 3-speed video tape recorders

It should be noted that some VTRs operating in the picture search mode, generate such distorted pictures that the no TV transmitter detection circuit can be activated as the voltage on pin 18 drops below 1.2 V. This would imply a rolling picture (Mode D). In general VTRs do use a re-inserted vertical pulse in the feature mode. Therefore the divider system has been designed such that the divider is forced to the wide window mode when V_{18} is below 1.2 V and a vertical sync pulse is detected within the window provided by the reset divider at 528 and the end of the vertical blanking period.

General

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the divider mode A the start is generated at the reset of the divider. In modes B and C the anti-top-flutter pulse starts at the beginning of the first equalizing pulse sequence. The anti-top-flutter ends after the second equalizing pulse sequence.

The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34, the middle of line 21 of field 1 and at the end of line 283 of field 2.

The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the B or C mode.

Vertical sawtooth

To generate a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF. The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is also activated at reset. When the capacitor has reached a voltage value of 5.0 V the voltage is kept constant until the charging period ends. The charging period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source the value of which can be set by an external resistor connected between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal Zener diode reference voltage which has a typical voltage of 7.5 V. The recommended operating current range is 10 to 75 μA. The resistor at pin 4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction voltage can be set to the required value by external components connected between pins 3 and 4 or by superimposing a correction voltage in series with the earth connection of the resistor connected to pin 4.
The vertical amplitude is set by the current of pin 4.

Vertical feedback

The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V (p-p).
The low DC voltage value improves the picture bounce behaviour as less parabola compensation is required. Even a DC-coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous voltage level of 2.5 V in the sandcastle output signal of pin 17. This results in blanking of the picture displayed, thus preventing a burnt-in horizontal line.

Vertical driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 170 Ω. The output pin is also connected to an internal current source with a sink current of 0.25 mA.

Integration time of the vertical synchronization pulse separator

The vertical sync separator has two integration times:

- long time; typical 19 μs, valid for $1.8 \leq V_{18} \leq 7.8$ V (no noise detected)
- short time; typical 12 μs, valid for noise detected and $V_{18} \geq 1.2$ V.

When V_{18} drops below 1.2 V, the integration time is forced back to 19 μs to prevent switching of the divider system to the wide window mode for noise only conditions.

Sync separator, phase detector and TV-station identification (pins 5, 6, 7 and 18)

SYNC SEPARATOR

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor connected between pins 6 and 7. The value is given by the formula:

$$p = \frac{R_S}{5.3 \times R_S} \times 100 \; (R_S \text{ value in k}\Omega).$$

Where R_S is the resistor connected between pins 6 and 7 and the top sync levels equals 100%. The recommended resistor value is 5.6 kΩ.

BLACK LEVEL DETECTOR

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the vertical blanking interval the slicing detector is inhibited by a signal which starts with the anti-top-flutter pulse and ends with the reset of the vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.
An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V.

NOISE LEVEL DETECTOR

The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level (S/N) of ≤19 dB is detected a counter circuit is activated.

$$S/N = 20 \log \frac{\text{Video voltage (black-to-white signal)}}{\text{Noise (RMS)}}$$

A video input signal is processed as "acceptable noise free" when 12 out of 15 sync pulses have a noise level below 19 dB for successive field periods. The sync pulses are processed during a 15 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB. The use of a filter of 1 kΩ and 150 pF in front of pin 5 reduces the noise content of the CVBS signal by approximately 6 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse detection. At the same time the integration time of the vertical sync pulse separator is reduced providing $V_{18} > 1.2$ V.

PHASE DETECTOR (SEE FIG.3)

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by a factor of 1.4.
In this way there is no requirement for external VTR time constant switching, and thus all station numbers are suitable for signals from VTR, video games or home computers.

For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a field period counter which switches the phase detector to fast for 3 field periods during the vertical scan period.
The horizontal oscillator will now lock to the new TV station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched off and the divider is set to the large window. In general the mute signal is switched off within 5 ms (C_{18} = 47 nF) after reception of a new TV signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the field counter is switched off and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to approximately 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition.
The phase detector output current during the blanking period is now reduced from 2 mA to 1.35 mA.
When desired, most conditions of the phase detector can also be set by external means in the following way:

- fast time constant, TV transmitter identification circuit not active, connect pin 18 to ground (pin 9)
- fast time constant, TV transmitter identification circuit active, connect a 220 kΩ resistor between pin 18 and ground; this condition can also be set by using a 3.6 V stabistor diode instead of a resistor
- slow time constant (with the exception of the vertical blanking period), connect pin 18 via a 10 kΩ resistor to +12 V (pin 10); in this condition the transmitter identification circuit is not active
- no switching to slow time constant required (transmitter identification circuit active), connect a 6.8 V Zener diode between pin 18 and ground.

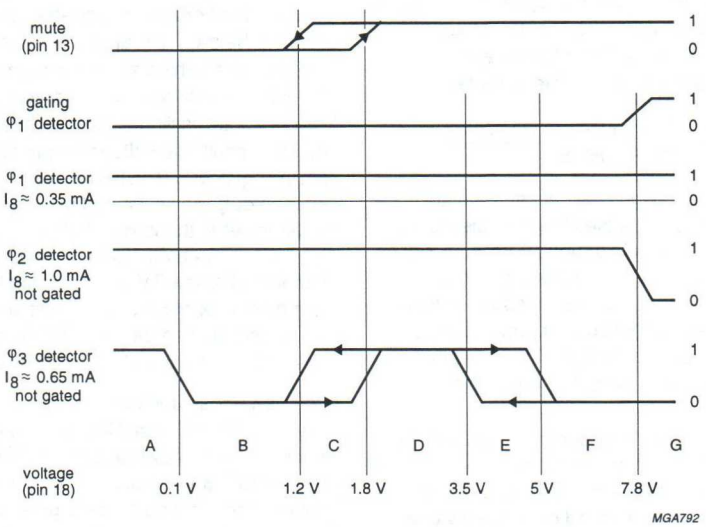


Fig.3 Operation of the three phase detector circuits.

Explanation of areas A to G shown in Fig.3

A	switching over to new TV station activates 3 field period counter
B	noise only condition
C	TV transmitter identification hysteresis range
D	fast time constant
C-E	fast time constant hysteresis range
F	normal time constant
G	sync pulse noise level detection circuit forces pin 18 to >7.8 V while signal-to-noise level <19 dB; slow time constant and gated sync pulse operation.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage operate a very low supply current into pin 16. The horizontal oscillator starts at a supply current of approximately 4 mA (V_{16} approximately 6 V). The horizontal output stage is forced into the non-conducting stage until the supply current has reached a typical value of 5 mA.

The circuit has been designed such that after starting the horizontal output function, a current drop of approximately 1 mA is allowed.

The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as oscillator signal for synchronized switched-mode power supplies.

The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C).
The main supply should be connected to pin 10 and pin 9 should be used for ground. When the voltage on pin 10 increases from zero to its final value (typ. 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes and the voltage on pin 16 will stabilize on a typical value of 9.3 V. In stabilized conditions (V_{10} > 10 V) the minimum required supply current into pin 16 is approximately 2.5 mA.
All other IC functions are switched on via the main supply voltage on pin 10. When this voltage reaches a value of approximately 7 V the horizontal phase detector is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 typical 9.3 V.

To close the second phase detector loop a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.
For remote switch-off pin 16 can be connected to ground (via a npn transistor with a collector series resistor of approximately 500 Ω) which decreases pin 16 voltage to ≤5 V and switches off the horizontal output pulse.

Horizontal oscillator, horizontal output transistor and second phase detector

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground (pin 9). The open collector horizontal output stage is connected to pin 11. An internal Zener diode configuration limits the open voltage of pin 11 to approximately 14.5 V. The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of approximately 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of approximately 40% HIGH.
The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched off and the second phase detector is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%. The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output state.

The horizontal output pulse duration is 29 µs HIGH for storage times between 1 µs and 17 µs (flyback pulse of 12 to 29 µs). A higher storage time increases the HIGH time.
Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV transmitter) the npn transistor is switched on. When the voltage on pin 18 increases to a level of approximately 1.8 V (new TV transmitter found) the npn transistor is switched off.
This function is available when pin 13 is connected to pin 10 (+12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV transmitter is identified the voltage on pin 13 will be LOW (<0.5 V).
When an M-system TV transmitter with a divider ratio <576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force the output voltage down to approximately 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17 has three different voltage levels. The highest level (10.4 V) can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12 and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 60 Hz the blanking pulse duration is 34 clock pulses started from the reset of the vertical divider system.

For TV signals which have a divider ratio between 522 and 528 the vertical blanking pulse is started at the first equalizing pulse.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{16}	start current	V_{10} = 0 V	–	9.7	mA
V_P	supply voltage		–	13.2	V
P_{tot}	total power dissipation		–	1.2	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	50 K/W

CHARACTERISTICS

$V_P = V_{10}$ = 12 V; I_{16} = 6.2 mA; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 10)		10	12	13.2	V
I_{16}	supply current (pin 16)	note 1				
		V_{10} = 0 V	6.2	–	9.7	mA
		V_{10} = 1 to 10 V; $T_{amb} \leq$ 70 °C	6.2	–	8.7	mA
		V_{10} > 10 V	2.5	–	9.7	mA
V_{16}	stabilized voltage (pin 16)		8.8	9.3	9.7	V
I_{10}	current consumption (pin 10)		–	70	85	mA
Video input (pin 5)						
V_5	top sync level		1.5	3.1	3.75	V
$V_{5(p\text{-}p)}$	sync pulse amplitude (peak-to-peak value)	note 2	0.05	0.6	1	V
SL	slicing level	note 3	35	50	65	%
t_d	delay between video input and detector output	see Fig.5	0.2	0.3	0.55	µs
S/N	signal-to-noise ratio with sync pulse noise level detector circuit active	CVBS = 1 V without filter at pin 5; note 4	–	19	–	dB
Sync pulse						
HYS	noise level detector circuit hysteresis		–	3	–	dB
Noise gate (pin 5)						
V_5	switching level		–	0.7	1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
First control loop (pin 8) horizontal oscillator to synchronization signal						
Δf	holding range		±700	±800	–	Hz
Δf	catching range		±700	±800	±1100	Hz
α_{CS}	control sensitivity video with respect to burst key and flyback pulse:					
	slow time constant	note 5	–	2	–	kHz/µs
	normal time constant	note 6	–	5	–	kHz/µs
	fast time constant	note 6	–	3	–	kHz/µs
φ_{10}	phase modulation due to hum on the supply line (peak-to-peak value)	note 7	–	0.2	–	µs/V
φ_{16}	phase modulation due to hum on the input current (peak-to-peak value)	note 8	–	0.08	–	µs/V
Second control loop (pin 14) horizontal flyback to horizontal oscillator						
$\Delta t_d/\Delta t_o$	control sensitivity	t_d = 10 µs	200	300	600	µs/µs
t_d	control range		1	–	45	µs
t_d	control range for constant duty factor horizontal output		1	29 – t_{FB}	–	µs
	control edge of horizontal output signal (pin 11)		–	positive	–	
Phase adjustment (pin 14) via second control loop						
α_{CS}	control sensitivity	t_d = 10 µs	–	25	–	µA/µs
I_{14}	maximum allowed control current		–	–	±60	µA
Horizontal oscillator (pin 15) C_{osc} = 2.7 nF; R_{osc} = 34.2 kΩ						
f_H	frequency (no sync)		–	15 625	–	Hz
Δf_H	spread (fixed external components, no sync)		–	–	±4	%
Δf_H	frequency deviation between starting point output signal and stabilized condition		–	+5	+8	%
TC	temperature coefficient		–	-1.10^{-4}	–	K
Horizontal output (pin 11) open collector						
V_{11H}	HIGH level output voltage		–	–	13.2	V
V_{11}	start voltage protection (internal Zener diode)		13	–	15.8	V
I_{16L}	LOW level input current protection output enabled		–	5.0	6.2	mA
V_{11L}	LOW level output voltage start condition	I_{11} = 10 mA	–	0.1	0.5	V
δ	duty factor output current during starting	I_{16} = 6.2 mA	50	60	70	%
V_{11L}	LOW level output voltage normal condition	I_{11} = 25 mA	–	0.3	0.5	V
δ	duty factor output current without flyback pulse pin 12		45	50	55	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{OH}	duration of output pulse HIGH	storage time horizontal deflection stage = 10 µs	27	29	31	µs
TC	temperature coefficient		–	-4.10^{-2}	–	K
$\Delta H_W/H_d$	influence of delay time on pulse width of horizontal output signal		–	0.16	–	µs/µs
	controlled edge		–	positive	–	
Sandcastle output signal (pin 17)						
V_{17}	output voltage during:					
	burst key		9.8	10.4	–	V
	horizontal blanking	I_{load} = 1 mA	4.1	4.5	4.9	V
	vertical blanking	I_{load} = 0.3 mA	2.1	2.5	2.9	V
V_{17}	zero level output voltage	I_{sink} = 0.5 mA	–	0.7	–	V
t_P	burst key pulse width	60 Hz	3.4	3.65	4	µs
V_{12}	horizontal blanking level		–	1	–	V
	vertical blanking	note 9				
t_{d1}	phase position burst key time between middle sync pulse at pin 5 and start burst key pulse at pin 17		2.3	2.7	3.1	µs
t_{d2}	phase position burst key time between start sync pulse at pin 5 and end of burst key pulse at pin 17	60 Hz	–	–	9.1	µs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see Fig.1)						
I_{18}	detector output current		–	0.25	–	mA
V_{18}	voltage level for in sync condition	φ_1 normal	5.8	6.4	7	V
V_{18}	voltage level for noisy sync pulse	φ_1 slow and gated	9	10.1	–	V
V_{18}	voltage level for noise only	note 10	–	0.3	–	V
V_{18}	switching level:					
	normal to fast		<3.2	3.5	3.8	V
	mute output active and fast to normal		<1.0	1.2	1.4	V
	field period counter	3 periods fast	<0.08	0.12	0.16	V
	normal to fast mute output inactive	locking	>1.5	1.75	2	V
	fast to normal	locking	>4.7	5	5.3	V
	normal to slow	gated sync pulse	>7.4	7.8	8.2	V
Video transmitter identification output (pin 13)						
V_{13}	output voltage active	no sync; I_{13} = 2 mA	–	0.15	0.32	V
I_{13}	sink current active	no sync; V_{13} = 1 V	–	–	5	mA
I_{13}	output current inactive	sync 60 Hz	–	–	1	µA
60 Hz identification (pin 13) R_{13} positive supply 15 kΩ						
V_{13}	pnp emitter follower voltage	note 11	7.2	7.65	8.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input pulse (pin 12)						
V_{12}	switching voltage level		–	0.9	–	V
I_{12}	input current		0.2	–	3	mA
$V_{12(p-p)}$	input pulse (peak-to-peak value)		–	–	12	V
R_{12}	input resistance		–	3.5	–	kΩ
t_d	phase position without shift; time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		2.1	2.5	2.9	µs
Vertical ramp generator (pin 3)						
t_c	charge current pulse width		–	$26t_{clk}$	–	
I_3	charge current		–	3	–	mA
V_3	top level ramp signal voltage divider in 60 Hz mode	note 12	4.55	4.85	5.25	V
$V_{3(p-p)}$	ramp amplitude (peak-to-peak value); R_4 = 330 kΩ; f_V = 60 Hz	C_3 = 150 nF; note 12	–	2.5	–	V
Current source (pin 4)						
V_4	output voltage	I_4 = 20 µA	7	7.5	7.9	V
I_4	allowed current range	T_{amb} = 25 to 70 °C	10	–	75	µA
TC	temperature coefficient output voltage	I_4 = 40 µA	–	50	–	10^{-6}/K
Current source (pin 3)						
$I_{3/4}$	current ratio pin 3/pin 4	I_4 = 35 µA; V_3 = 2 V	–	1.05	–	
TC	temperature coefficient I_3	I_4 = 40 µA; R_4 fixed	–	100	–	10^{-6}/K
Comparator (pin 2)						
V_2	input voltage DC level	R_4 = 330 kΩ; C_3 = 150 nF	0.98	1.075	1.17	V
$V_{2(p-p)}$	input voltage AC level (peak-to-peak value)	R_4 = 330 kΩ; C_3 = 150 nF	–	0.8	–	V
I_2	input current	V_2 = 0 V	–	–	1	µA
Vertical output stage (pin 1) npn emitter follower						
V_1	maximum output voltage	I_1 = +1.5 mA; note 12	5	5.5	6.3	V
R_S	sync separator resistor		–	170	–	Ω
I_{sink}	continuous sink current		–	0.25	–	mA
Vertical guard circuit (pin 2)						
V_{2H}	active switching level HIGH	V_{17} = 2.5 V; note 12	>1.7	1.85	2.0	V
V_{2L}	active switching level LOW	V_{17} = 2.5 V; note 12	<0.25	0.35	0.45	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal vertical sync pulse separator						
t_{d1}	delay between video signal at pin 5 and internally separated vertical sync pulse; normal signal condition		12	19	25	µs
t_{d2}	delay between video signal at pin 5 and internally separated vertical sync pulse; noisy signal condition	$V_{18} \geq 1.2$ V	–	–	–17	µs

Notes to the characteristics

1. Value inclusive R_L pin 11 to pin 16 = 6.8 kΩ.
2. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is fixed by the formula:

   $$p = \frac{R_s}{5.3 \times R_s} \times 100\%.$$

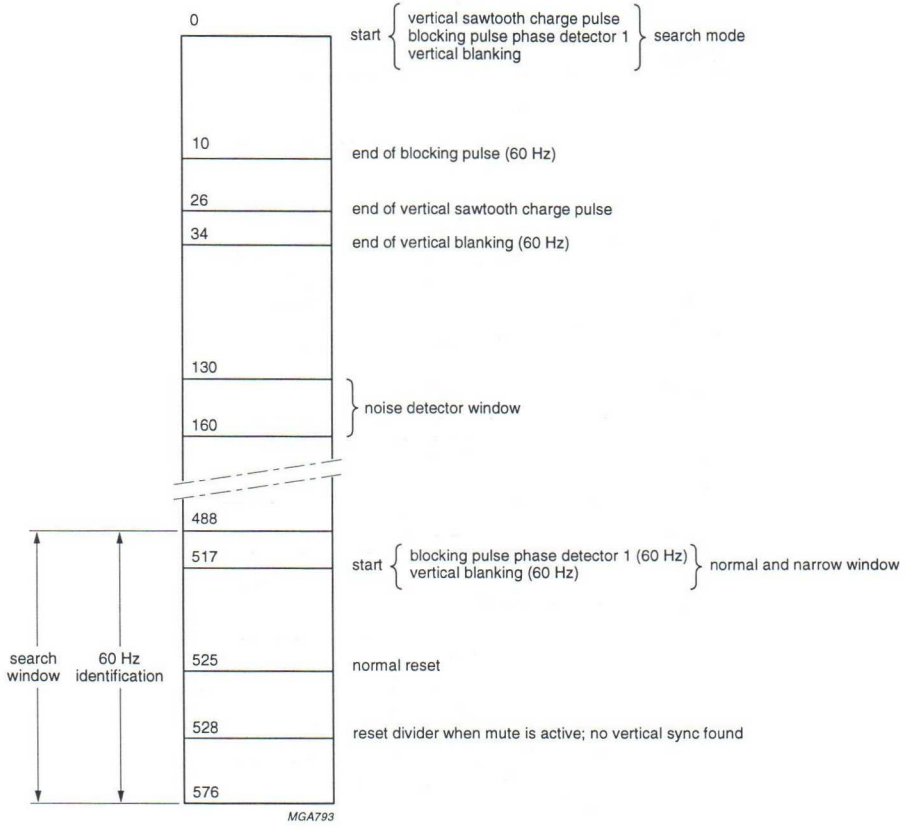
   Where R_S is the resistor between pins 6 and in kΩ; top sync = 100%.
4. $$S/N = 20 \log \frac{\text{Video voltage (black-to-white signal)}}{\text{Noise (RMS)}}$$

   A low-pass filter of 1 kΩ and 150 pF decreases the noise content of the CVBS signal by 6 dB.
5. Undercompensated.
6. Overcompensated.
7. Measured between pin 5 and sandcastle output pin 17.
8. Measured with 3.3 µF feedback capacitor between pin 16 and 6.8 µF capacitor in PLL filter pin 8.
9. Maximum divider ratio (60 Hz):

   $$n = \frac{2 \times f_H}{f_V} = 576 \text{ (2 clock pulses per video line).}$$

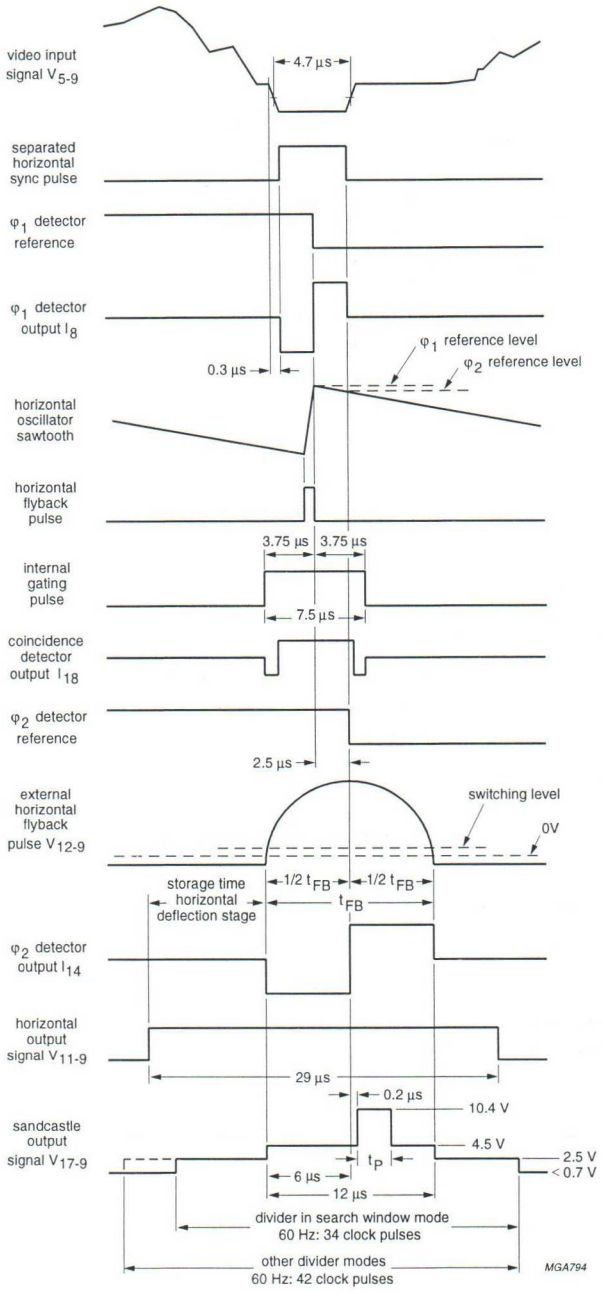
   Start vertical blanking:
   - search (large) window mode (60 Hz)
   - reset divider = start vertical sync pulse plus 1 clock pulse
   - small/standard window mode (60 Hz)
   - clock pulse 517.

   Stop vertical blanking:
   - all window modes (60 Hz)
   - clock pulse 34.
10. Depends on DC level of pin 5, value given is valid for $V_5 \approx 5$ V.
11. Valid for $\frac{2 \times f_H}{f_V} < 576$.
12. Value related to internal Zener diode reference voltage. Spread includes complete spread of reference voltage.



One video line equals two counter pulses.
Reset counter 32 µs after start of vertical sync pulse at pin 5.
Reset counter = counter state 0.

Fig.4 Counter system.



Two counter pulses equals one video line.

Fig.5 Timing diagram.

Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

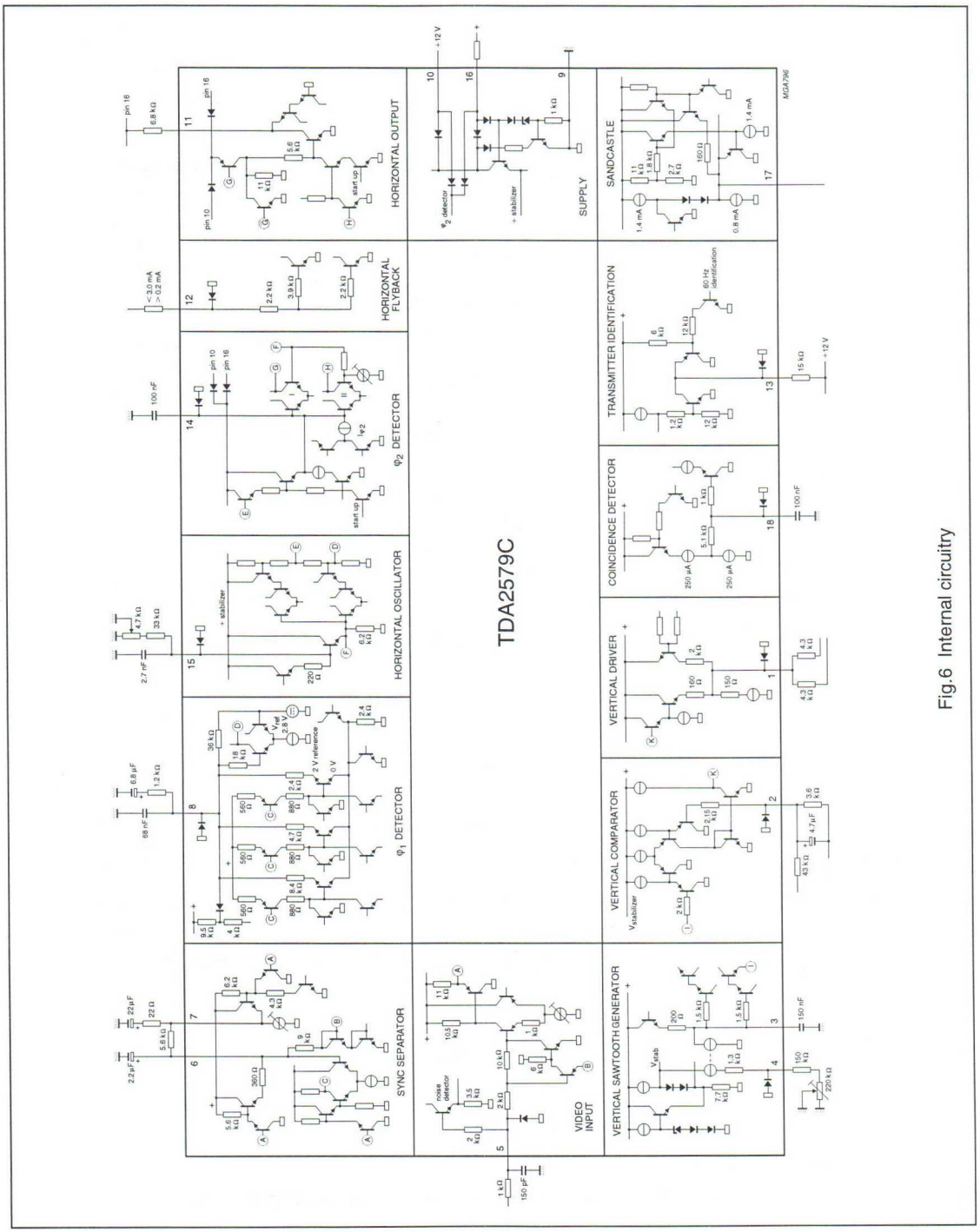
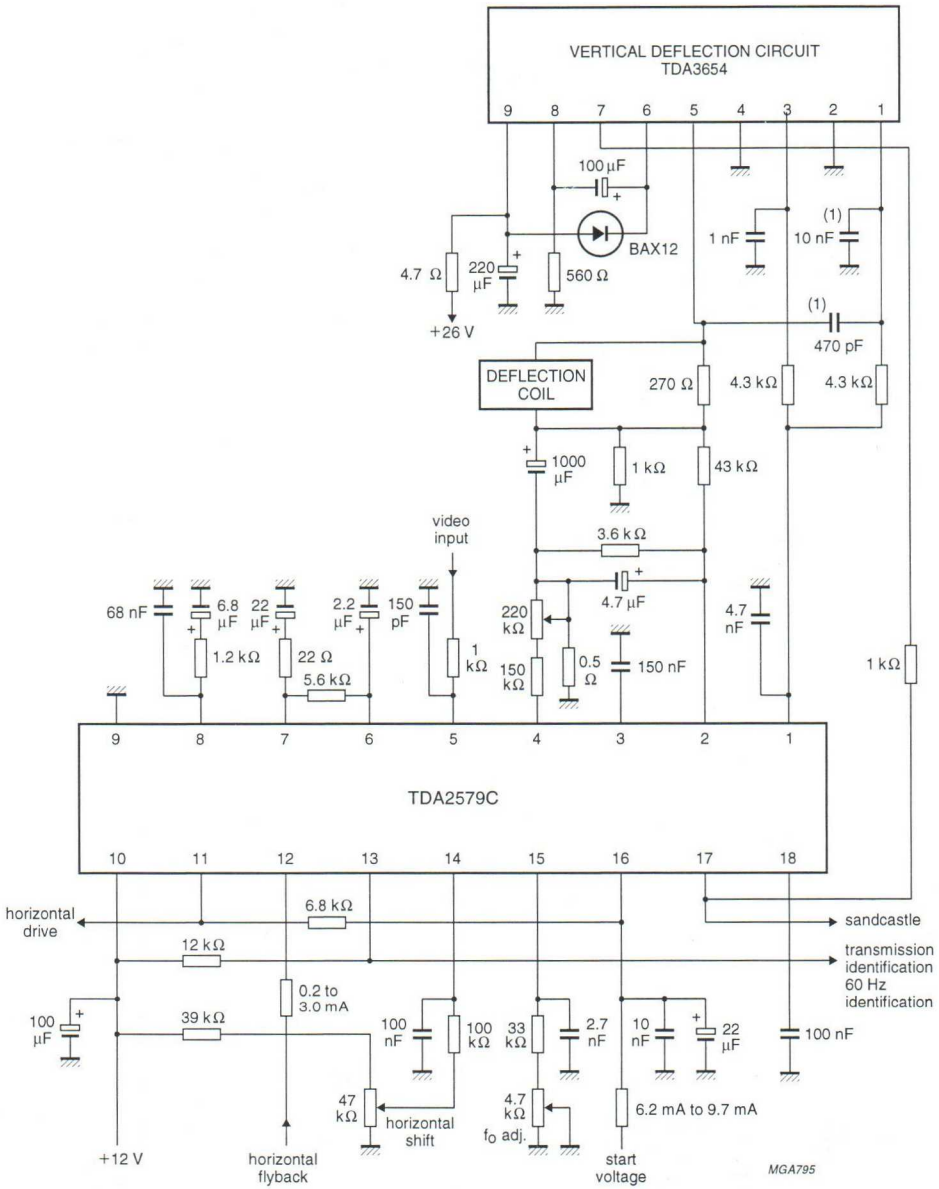


Fig.6 Internal circuitry



(1) Dependent on printed-circuit board layout.

Fig.7 TDA2579C and TDA3654 combination 110° Flat Square picture tube.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5 V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

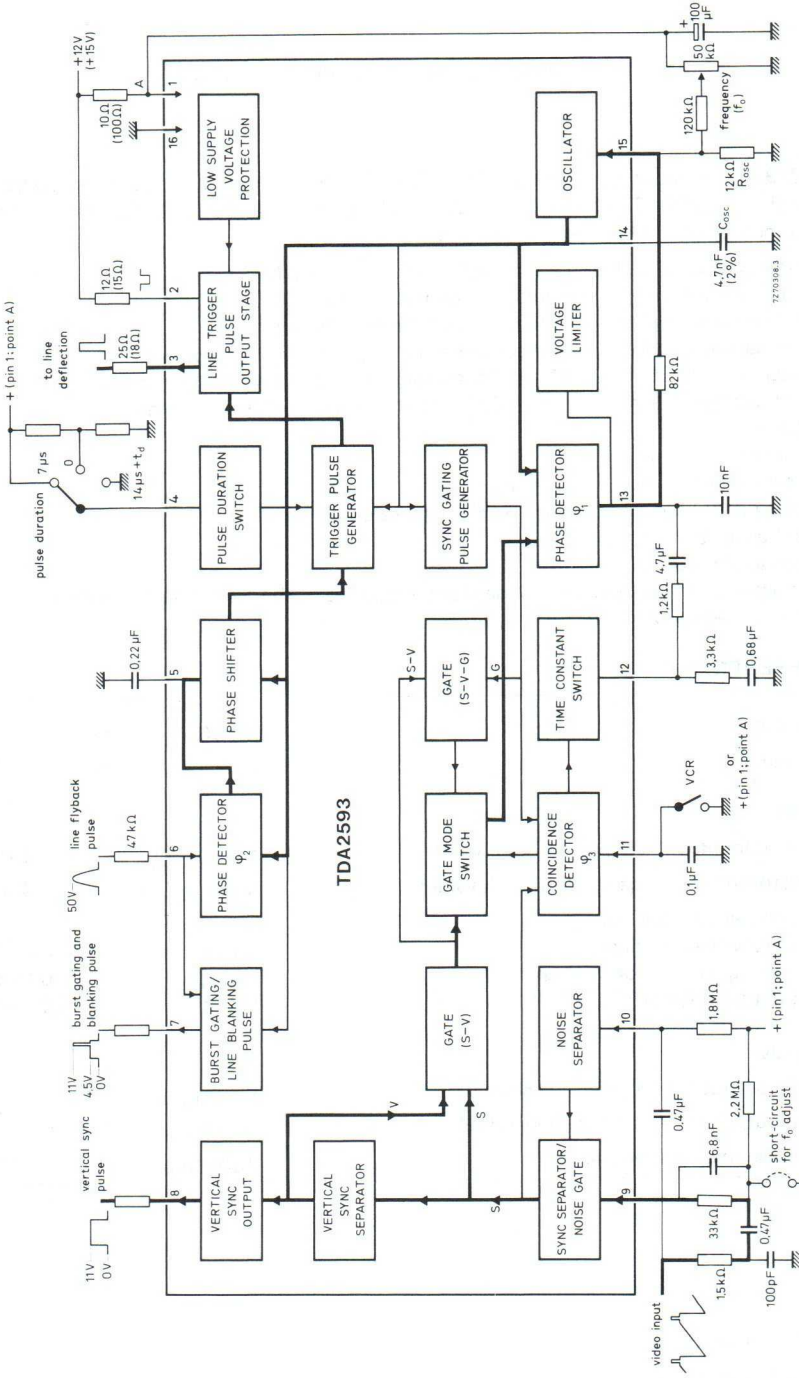


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	V_{1-16}	max.	13,2 V
at pin 2	V_{2-16}	max.	18 V
Voltages			
Pin 4	V_{4-16}	max.	13,2 V
Pin 9	$\pm V_{9-16}$	max.	6 V
Pin 10	$\pm V_{10-16}$	max.	6 V
Pin 11	V_{11-16}	max.	13,2 V
Currents			
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650 mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	10 mA
Pin 11	I_{11}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		0 to + 70 °C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8 V
Input keying current	I_9		5 to 100 μA
Input leakage current at V_{9-16} = −5 V	I_9	<	1 μA
Input switching current	I_9	⩽	5 μA
Switch off current	I_9	>	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator				
Input switching voltage	V_{10-16}	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	>	100	μA
		typ.	150	μA
Input leakage current at $V_{10-16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7	V
Line flyback pulse				
Input current	I_6	typ.	1	mA
			0,02 to 2	mA
Input switching voltage	V_{6-16}	typ.	1,4	V
Input limiting voltage	V_{6-16}		−0,7 to + 1,4	V
Switching on VCR				
Input voltage	V_{11-16}		0 to 2,5	V
	V_{11-16}		9 to V_{1-16}	V
Input current	$-I_{11}$	<	200	μA
	I_{11}	<	2	mA
Pulse duration switch				
For t = 7 μs (thyristor driving)				
Input voltage	V_{4-16}		9,4 to V_{1-16}	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	V_{4-16}		0 to 3,5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3-16} = 0$ or input pin 4 open				
Input voltage	V_{4-16}		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	$>$	10	V
		typ.	11	V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on}	μs
Burst gating pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	$>$	10	V
		typ.	11	V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}16} = 7$ V	t_p	typ.	4	μs
			3,7 to 4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16} = 7$ V	t	typ.	2,65	μs
			2,15 to 3,15	μs
Output trailing edge current	I_7	typ.	2	mA
Line flyback-blanking pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA
Line drive pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (thyristor driving) $V_{4\text{-}16} = 9{,}4$ to $V_{1\text{-}16}$ V	t_p	typ.	7	μs
			5,5 to 8,5	μs
Pulse duration (transistor driving) $V_{4\text{-}16} = 0$ to 4 V; $t_{fp} = 12$ μs	t_p		$14 + t_d$	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4	V
Overall phase relation				
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6	μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	$<$	0,7	μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration $t_{fp} = 12$ μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	$V_{14\text{-}16}$	typ.	4,4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0,05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	$V_{13\text{-}16}$		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	<	1	μA
Output resistance				
at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

Phase comparison φ_2 and phase shifter

Control voltage range	$V_{5\text{-}16}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance				
at $V_{5\text{-}16}$ = 5,4 to 7,6 V			high ohmic	*
at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V	R_5	typ.	8	kΩ
Input leakage current				
$V_{5\text{-}16}$ = 5,4 to 7,6 V	I_5	$<$	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	$<$	15	μs
Static control error	$\Delta t/\Delta t_d$	$<$	0,2	%

Coincidence detector φ_3

Output voltage	$V_{11\text{-}16}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{11M}	typ.	0,1	mA
with coincidence	$-I_{11M}$	typ.	0,5	mA

Time constant switch

Output voltage	$V_{12\text{-}16}$	typ.	6	V
Output current (limited)	$\pm I_{12}$	$<$	1	mA
Output resistance				
at $V_{11\text{-}16}$ = 2,5 to 7 V	R_{12}	typ.	0,1	kΩ
at $V_{11\text{-}16} < 1{,}5$ V or > 9 V	R_{12}	typ.	60	kΩ

Internal gating pulse

Pulse duration	t_p	typ.	7,5	μs

* Current source.

HORIZONTAL COMBINATION

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

Features

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	typ.	50 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

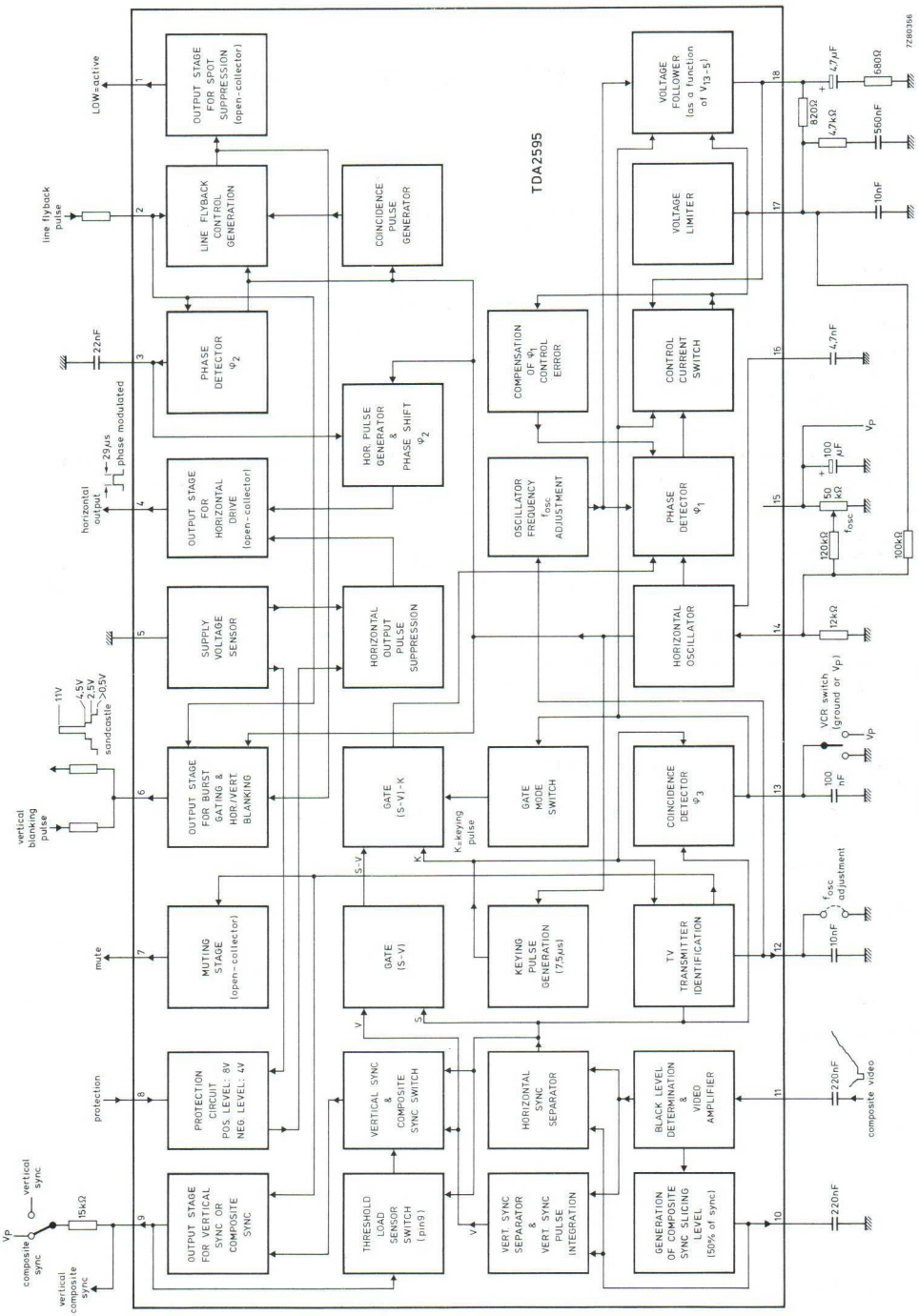


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0,5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	25	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude for $V_{11\text{-}5(p\text{-}p)} < 1{,}5$ V					
Capacitor current during:					
video	I_{10}	–	16	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	$V_{14\text{-}5}$	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15\text{-}5}/V_{15\text{-}5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
discharging	$+I_{16}$	–	1024	–	μA
charging	$-I_{16}$	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 50 mA	$V_{4\text{-}5}$	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V
Hysteresis for switching on the output pulse	ΔV_P	–	250	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3,55	–	8,3	V
Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9,5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	$\pm\Delta f_{osc}$	–	680	–	Hz
spread of catching and holding range	$\pm\Delta f_{osc}$	–	10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9,5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9,5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0{,}5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison and flyback control	V_{2-5}	–	3	–	V
Switching level for horizontal blanking	V_{2-5}	–	0,3	–	V
Input voltage limiting	V_{2-5}	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Maximum negative input current	$-I_2$	–	–	500	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2,6 ± 0,7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3	$\Delta I/\Delta t$	–	30	–	μA/μs
Burst gating pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4,1	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6) (note 3)					
Output voltage at I_6 = 2,8 mA	V_{6-5}	2,15	2,5	3	V
Minimum output current at $V_{6-5} > 2,15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12) (note 4)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0,5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0,8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0,4	–	V
Current limiting for V_{8-5} = 1 to 8,5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8,5$ V	R_{8-5}	–	3	–	kΩ
Internal response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	V_{1-5sat}	–	–	0,5	V
Output leakage current in case of disturbance of line flyback pulse	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_P the vertical output is active independent of synchronization state.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
Repetitive peak output current	I_{ORM}	< 1,5	A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ. 5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ. 0,3	%
Input impedance	$\|Z_i\|$	typ. 45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ. 25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ. 55	mV
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

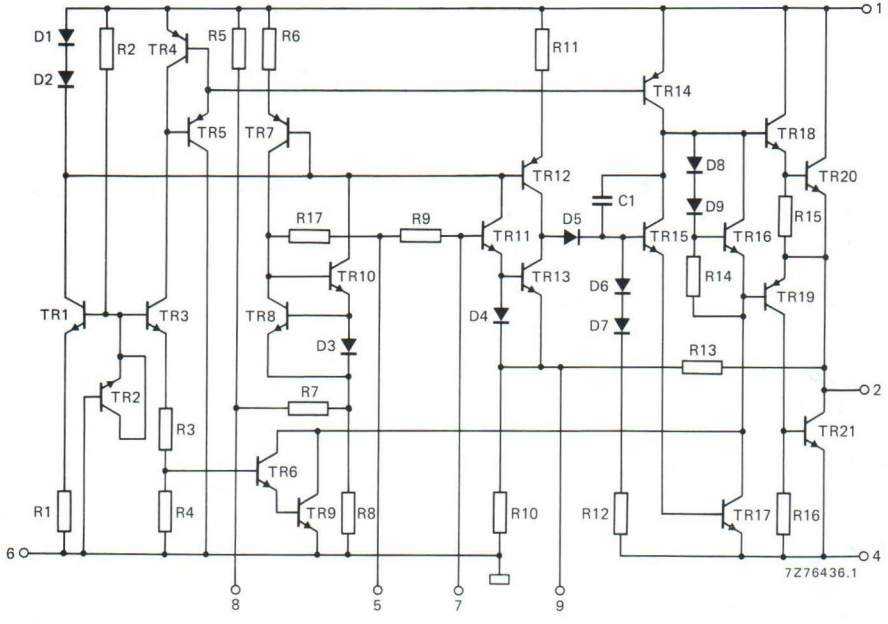


Fig. 1 Circuit diagram; pin 3 not connected.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 42 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

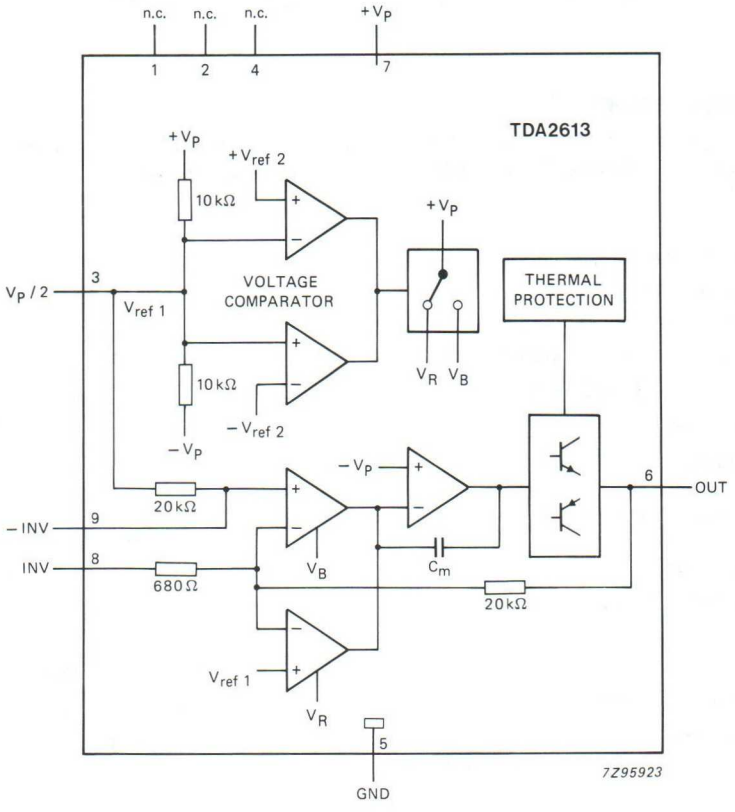


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected	5.	GND	ground (asymmetrical) / negative supply (symmetrical)
2.	n.c.	not connected	6.	OUT	output
3.	VP/2	½ VP (asymmetrical) / ground (symmetrical)	7.	+VP	positive supply
4.	n.c.	not connected	8.	INV	inverting input
			9.	−INV	non-inverting input

6 W hi-fi audio power amplifier TDA2614

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2614 is a power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as TV and radio.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		15	–	42	V
P_O	output power	V_S = 24 V; THD = 0.5%	–	6.5	–	W
G_v	internal voltage gain		–	30	–	dB
SVRR	supply voltage ripple rejection		–	45	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2614	9	SIL	plastic	SOT110

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

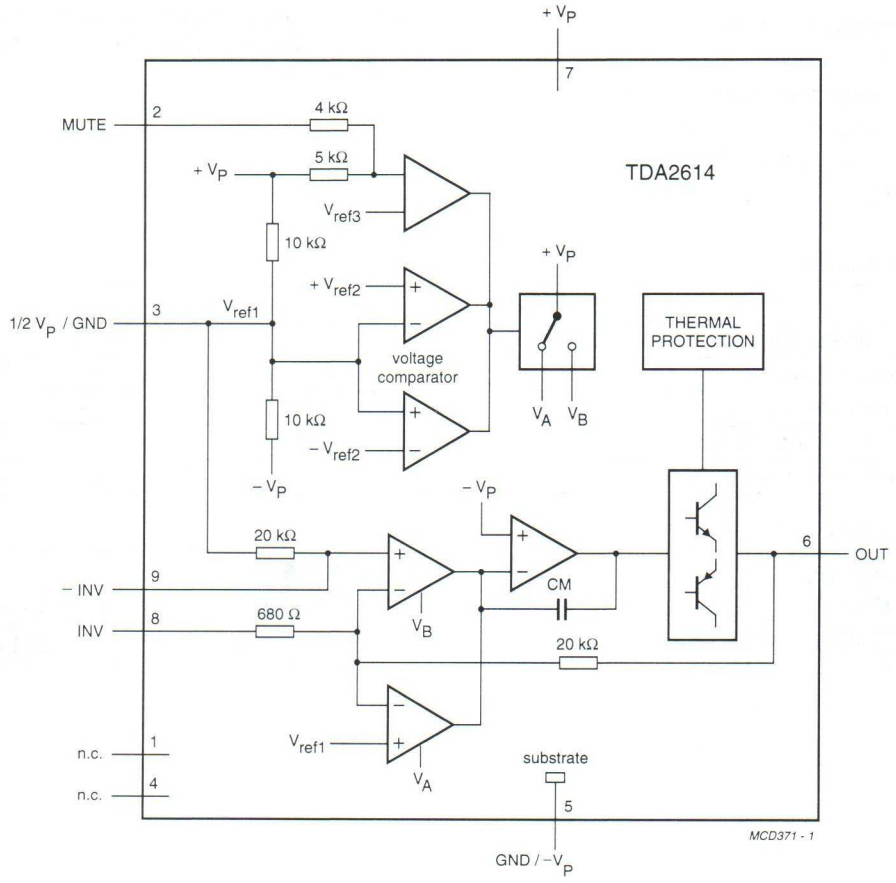


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MUTE	2	mute input
$1/2V_P$/GND	3	1/2 supply (or ground at symmetrical power supplies)
n.c.	4	not connected
GND/$-V_P$	5	ground (or negative supply rail at symmetrical power supplies)
OUT	6	output
V_P	7	supply voltage
INV	8	inverting input
–INV	9	non-inverting input

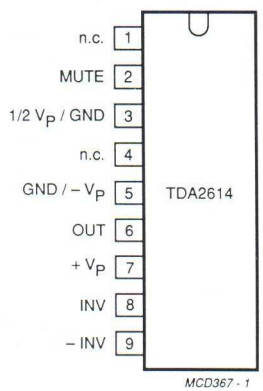


Fig.2 Pin configuration.

2 x 6 W hi-fi audio power amplifier TDA2615

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	positive supply voltage range		7.5	–	21	V
P_O	output power	$V_S = \pm 12$ V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2615	9	SIL	plastic	SOT110

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

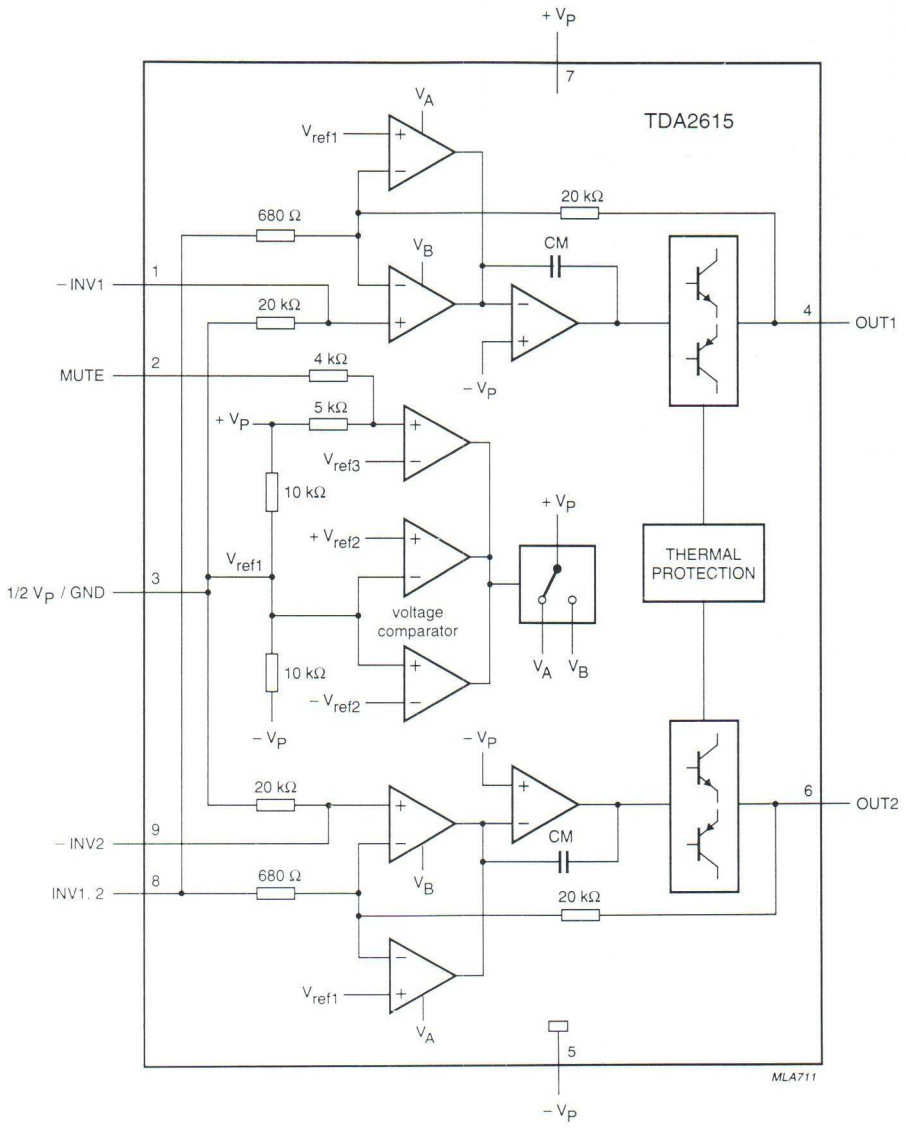


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
V_P	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

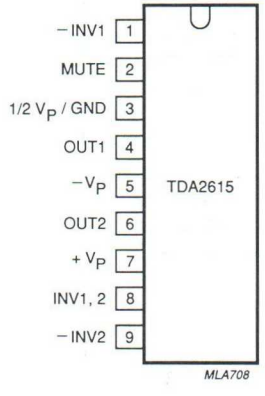


Fig.2 Pin configuration.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_P = \pm 16$ V; THD = 0.5%	–	12	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

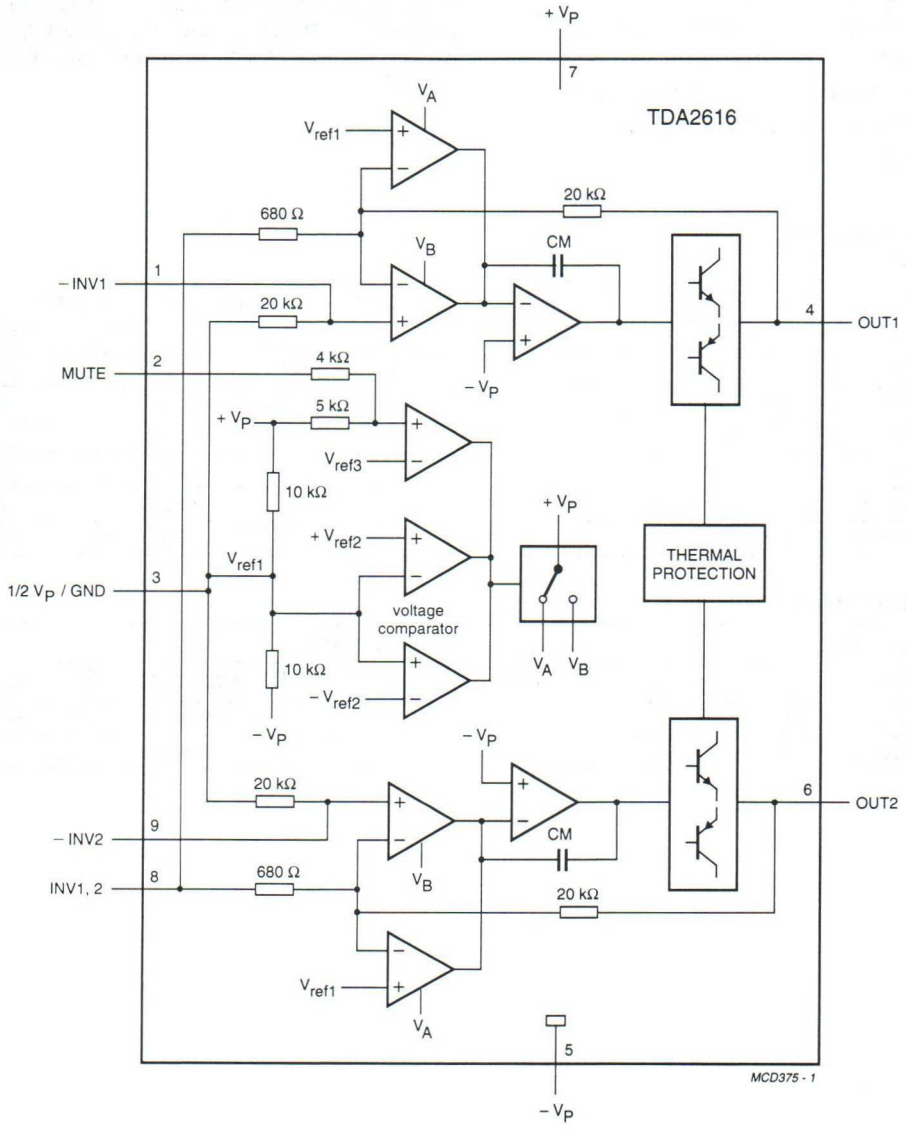


Fig.1 Block diagram.

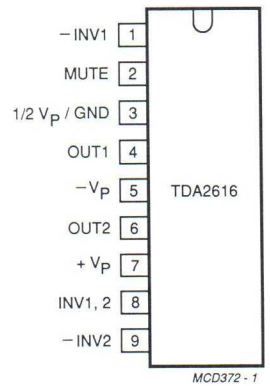


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
$+V_P$	7	supply voltage (positive)
INV1, 2	8	inverting inputs 1 and 2
−INV2	9	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA2616 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 12 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±16 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 µA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 2.5 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14.6 W.

With a maximum ambient temperature of +65 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 65}{14.6} - 2.5 = 3.3 \text{ K/W}.$$

The internal metal block has the same potential as pin 5.

VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation
- Synchronization circuit
- Blanking pulse generator with guard circuit
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with thermal and short-circuit protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26 V
Supply current (pin 5 + pin 9)*	$I_5 + I_g = I_S$	typ.	325 mA
Output current (peak-to-peak value)*	$I_{6(p-p)}$	typ.	1,7 A
Maximum output current (peak-to-peak value)	$I_{6(p-p)}$	max.	2,6 A
Picture frequency	f		50 Hz/60 Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1 V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5 K/W

* for 45 AX systems

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141RGA).

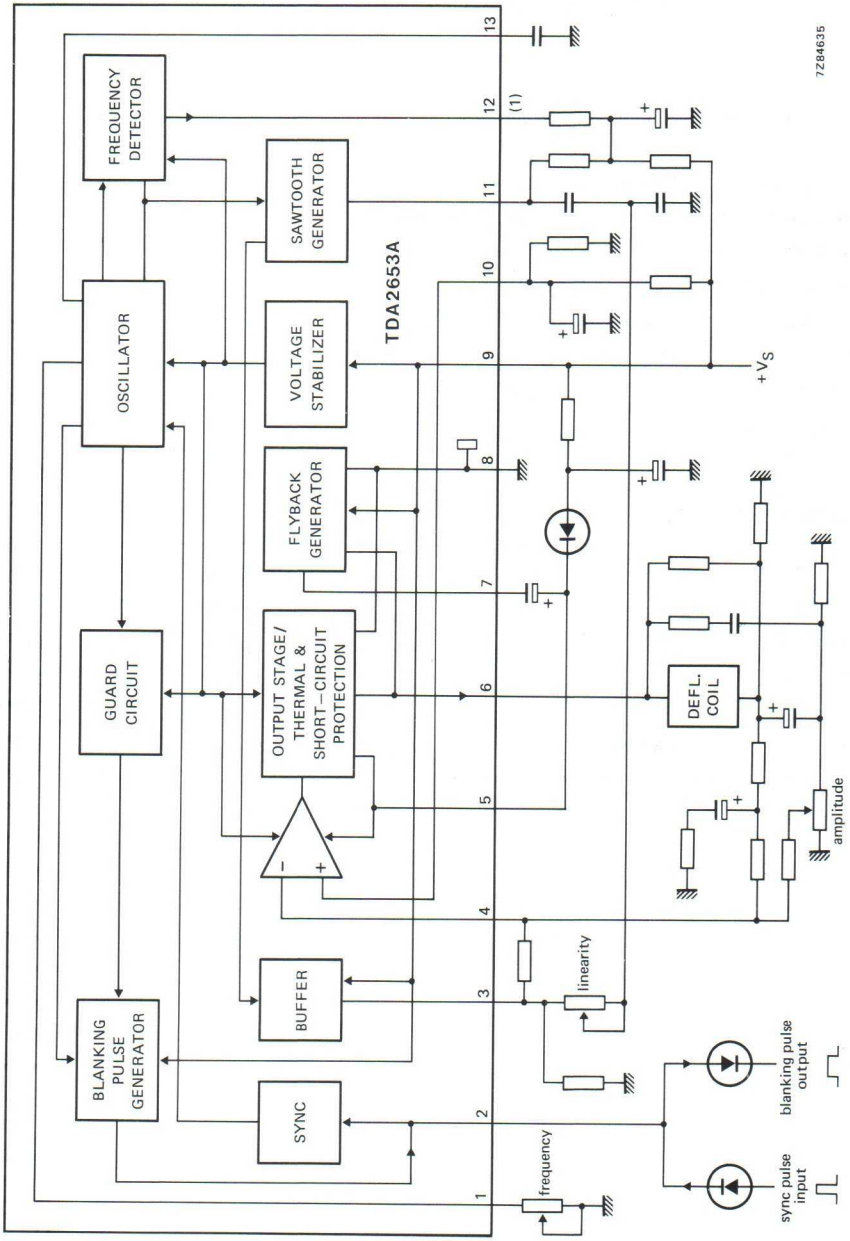


Fig. 1 Block diagram.

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	60 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	60 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1,3 A
	$-I_7$	max.	1,5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

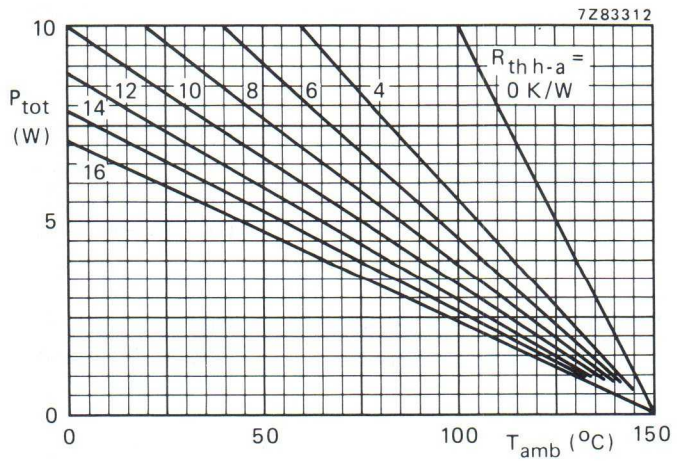


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heat-sink compound is used. $R_{th\ j\text{-}mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage at $-I_6$ = 1,1 A	V_{6-8}	⩾ typ.	$V_{5-8} - 2,2$ V $V_{5-8} - 1,9$ V
at I_6 = 1,1 A	V_{6-8}	typ. ⩽	1,3 V 1,6 V
Flyback generator output voltage at $-I_7$ = 1,1 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	1,3 A
Flyback generator peak current	$\pm I_7$	⩽	1,3 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8} V_{11-8}		0 to $V_S - 1$ V 0 to $V_S - 2$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾ ⩽	−2 μA +30 mA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

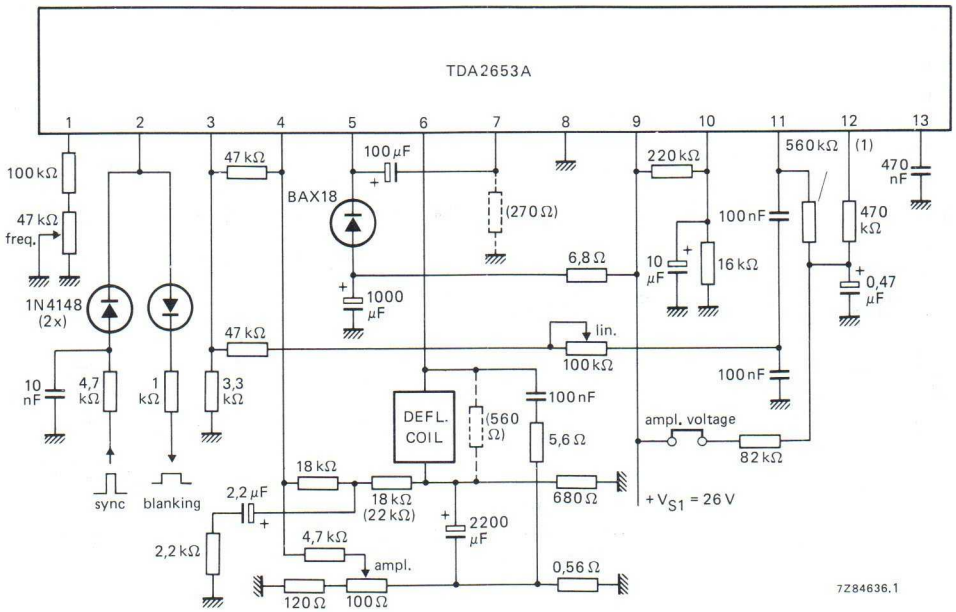
    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

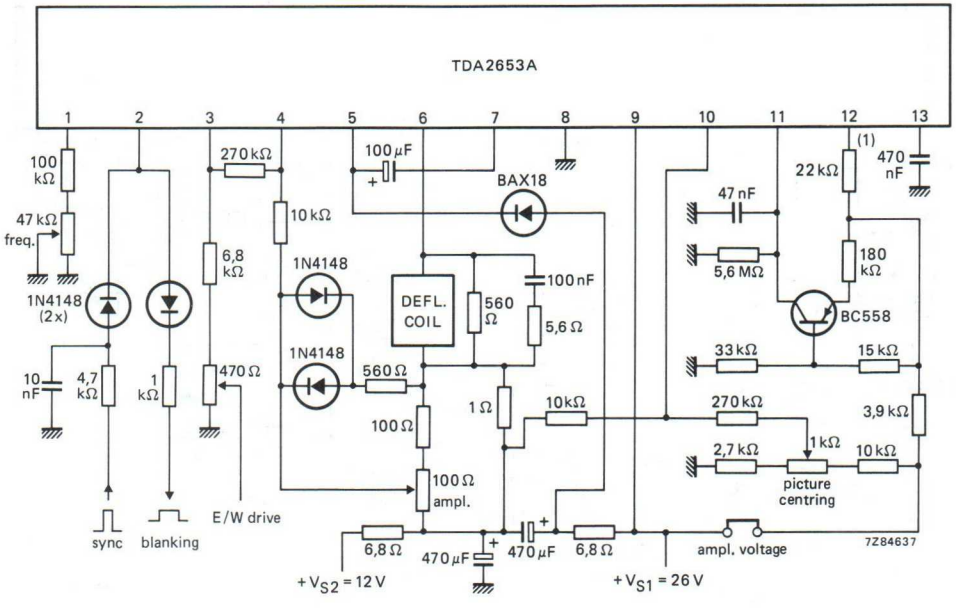
12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 45AX system (26 V).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 45 AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

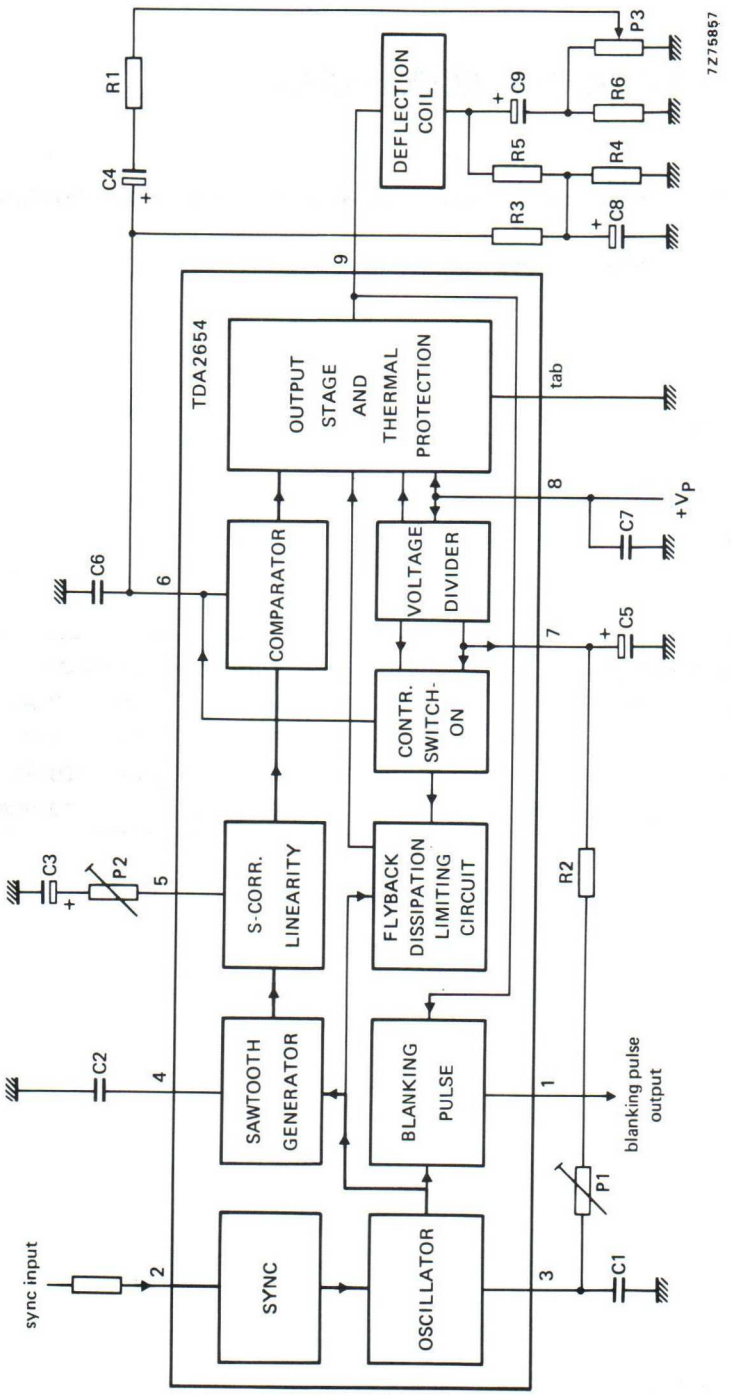


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages			
Pin 2	V_2	max.	5 V
Pin 3	V_3	max.	17 V
Pin 4	V_4	max.	17 V
Pin 5	V_5	max.	6 V
Pin 6	V_6	max.	13 V
Pin 7	V_7	max.	18 V
Pin 8	V_8 (V_P)	max.	35 V
Currents			
Pin 1	$+I_1$	max.	1 mA
	$-I_1$	max.	5 mA
Pin 2	I_2	max.	2,5 mA
Pin 3	I_3	max.	30 mA
Pin 4	I_4	max.	30 mA
Pin 5	$\pm I_5$	max.	1 mA
Pin 6	$\pm I_6$	max.	3 mA
Pin 9 (repetitive)	$\pm I_9$	max.	1 A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5 A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5 W
Storage temperature	T_{stg}		−25 to + 150 °C
Operating junction temperature	T_j	max.	150 °C

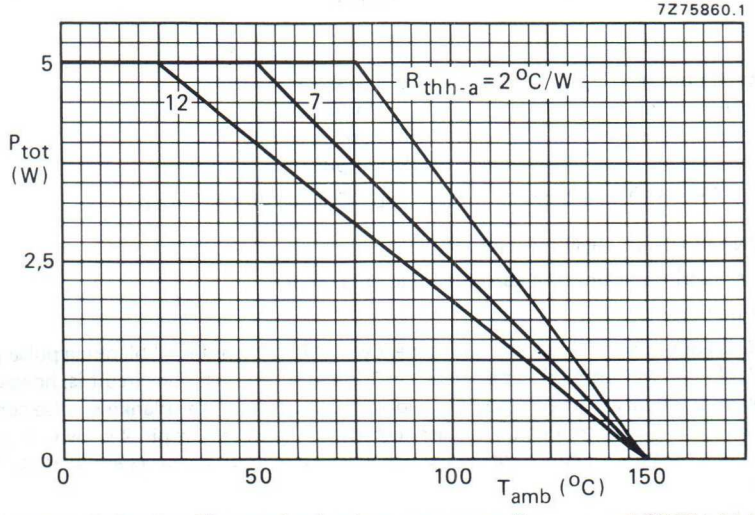


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\ tab-h}$ = 1 °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\ j-tab}$ = 12 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9\,(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9\,(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	−0,01	−0,01	Hz/°C
Oscillator voltage shift		typ.	−0,13	−0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

The value depends on the deflection coil.

9. Output

The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

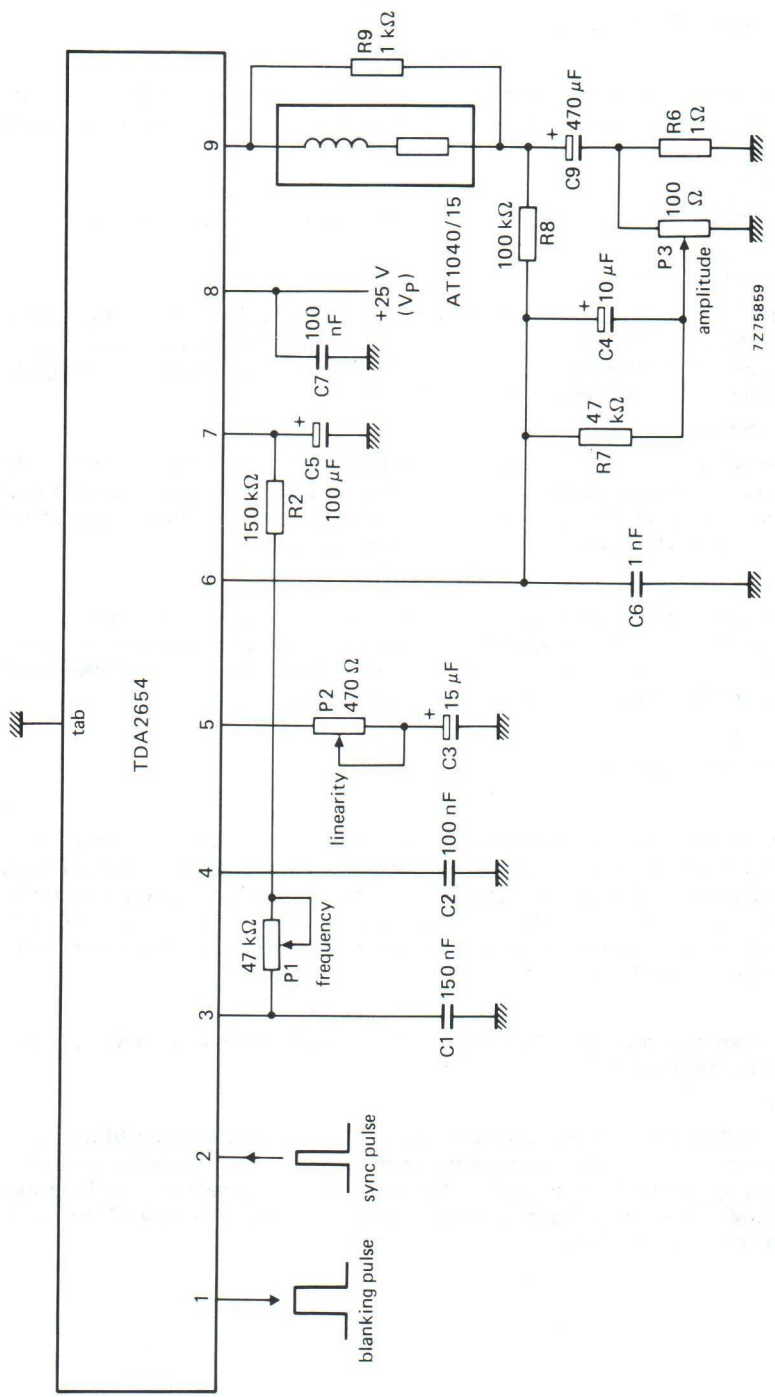
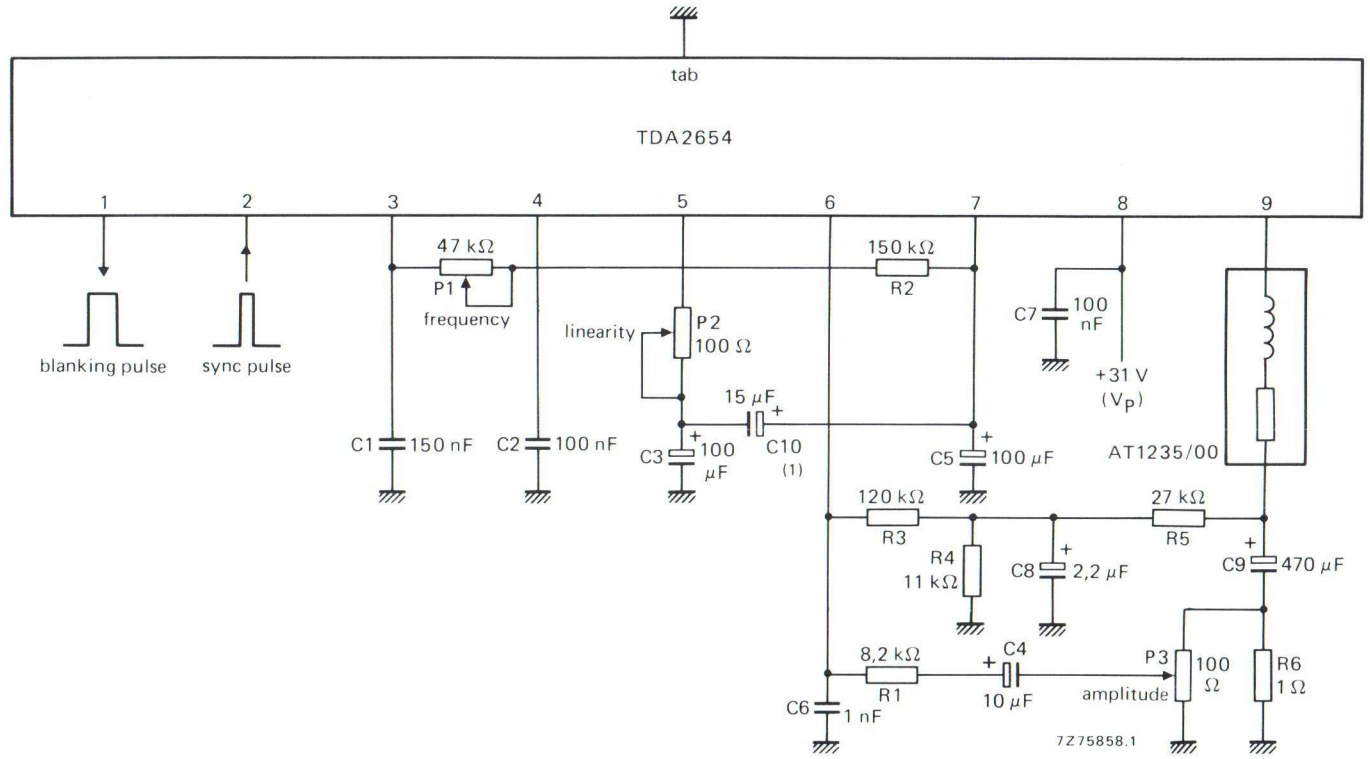


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)



(1) Only required when rapid variations in the supply voltage are expected.

Fig. 4 Colour 90° vertical deflection system.

VERTICAL DEFLECTION CIRCUIT

The TDA2658 is a monolithic integrated circuit for vertical deflection in small screen colour television receivers and monitors.

The circuit incorporates the following functions:

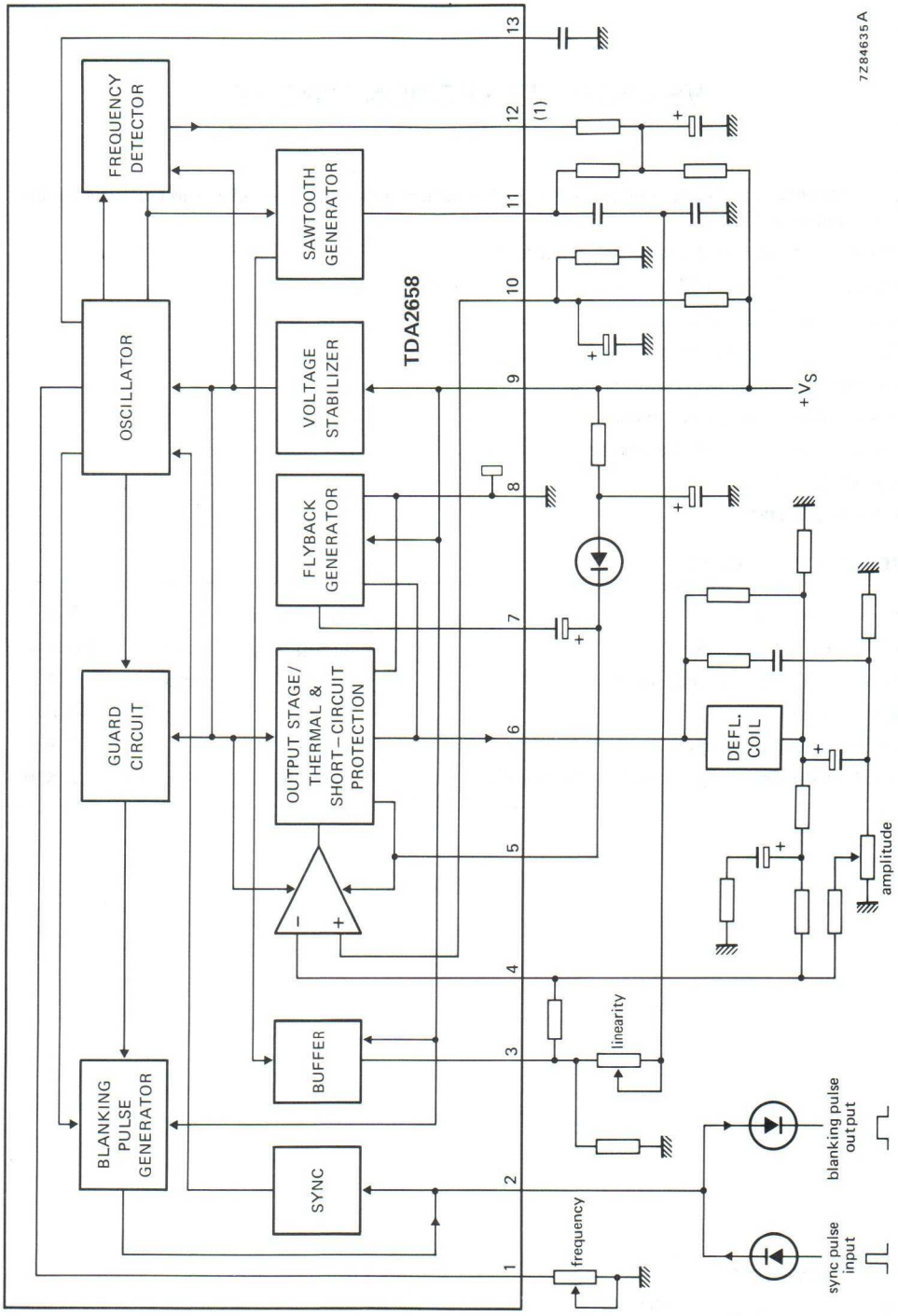
- Oscillator, switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9\text{-}8} = V_S$	typ.	26 V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	250 mA
Output current (peak-to-peak value)	$I_{6(p\text{-}p)}$	typ.	1,6 A
Picture frequency	f		50 Hz/60 Hz
Sync input pulse (peak-to-peak value)	$V_{2\text{-}8(p\text{-}p)}$	$\geqslant$	1 V
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	5 K/W

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141B).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	0,9 A
	$-I_7$	max.	1,1 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

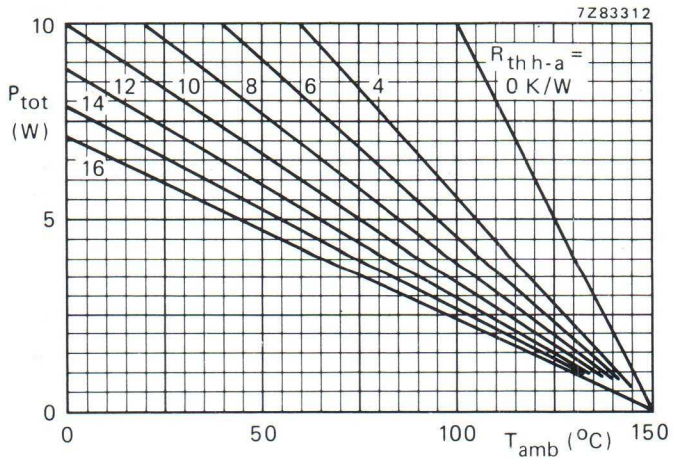


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heat-sink compound is used. $R_{th\ j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C; V_S = 26 V; unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 0,75 A	V_{6-8}	⩾ typ.	$V_{5-8} - 2,2$ V $V_{5-8} - 1,9$ V
at I_6 = 0,75 A	V_{6-8}	typ. ⩽	1,3 V 1,6 V
Flyback generator output voltage at $-I_6$ = 0,75 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	0,9 A
Flyback generator peak current	$\pm I_7$	⩽	0,9 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1,5$ V
	V_{11-8}		0 to $V_S - 1,5$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA (V_S = 26 V).

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

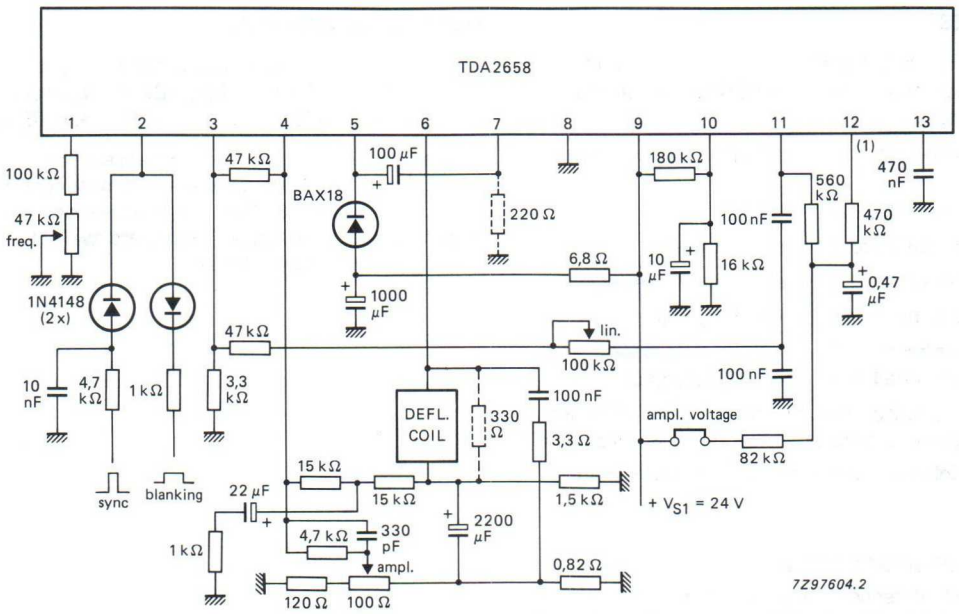
    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Fig. 3

System supply voltages	V_{S1}	typ.	24	V
System supply currents	I_{S1}	typ.	145	mA
Output voltage	V_{6-8}	typ.	14	V
Output voltage (peak value)	V_{6-8}	typ.	44	V
Deflection current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1	A
Flyback time	t_{fl}	typ.	1	ms
Total power dissipation per package	P_{tot}	typ. max.	1,7 2,2	W W
Oscillator frequency unsynchronized	f	typ.	46,5	Hz



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit.

Video control combination circuit TDA3504

FEATURES

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G–Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixes signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- Emitter-follower outputs for driving the RGB output stages.

GENERAL DESCRIPTION

The TDA3504 is an intergrated circuit which performs video control functions in a PAL/SECAM decoder for negative colour difference signals –(R–Y) and –(B–Y).

The required input signals are luminance and colour difference and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages.

QUICK REFERENCE DATA

All voltages referenced to pin 18 (ground).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 2)	–	12.0	–	V
I_P	supply current	–	95	–	mA
$V_{11(p-p)}$	video blanking sync (VBS) input signal (peak-to-peak value)	–	0.45	–	V
$V_{15(p-p)}$	–(B–Y) colour difference input signal (peak-to-peak value)	–	1.33	–	V
$V_{14(p-p)}$	–(R–Y) colour difference input signal (peak-to-peak value)	–	1.05	–	V
$V_{10, 9, 8(b-w)}$	inserted RGB signals (black-to-white value)	–	1.0	–	V
V_6	three-level sandcastle pulse				
	level 1	–	2.5	–	V
	level 2	–	4.5	–	V
	level 3	–	8.0	–	V
V_{17}	control voltage brightness	1.0	–	3.0	V
V_{16}	control voltage contrast	2.0	–	4.2	V
V_{12}	control voltage saturation	2.0	–	4.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3504	20	DIL	plastic	SOT146

BLOCK DIAGRAM

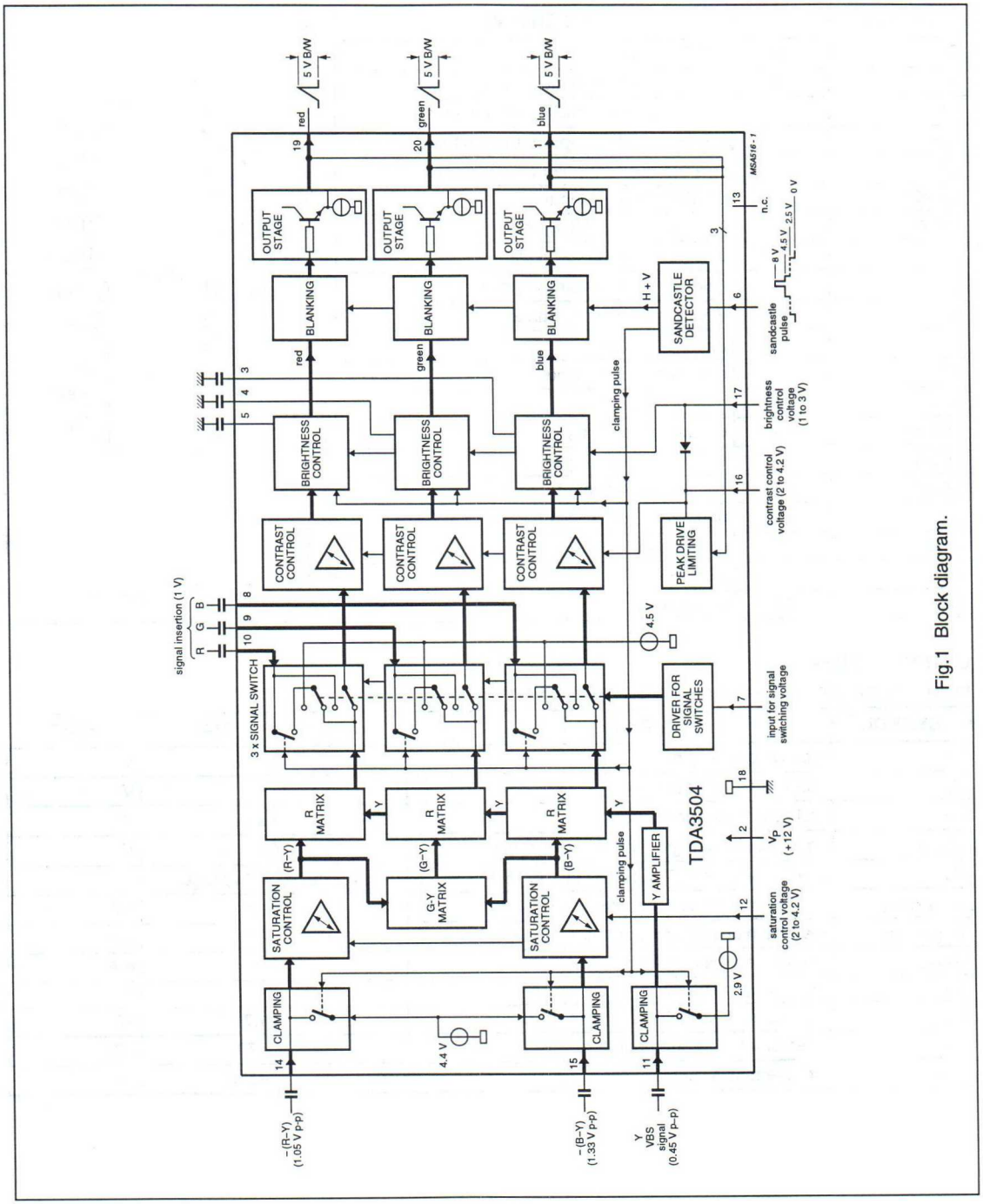


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BO	1	BLUE output
V_P	2	positive supply voltage (+12 V)
CB	3	BLUE storage capacitor for brightness
CG	4	GREEN storage capacitor for brightness
CR	5	RED storage capacitor for brightness
SAND	6	sandcastle pulse input
FSW	7	fast switch for RGB input
BI	8	BLUE input (external signal)
GI	9	GREEN input (external signal)
RI	10	RED input (external signal)
Y	11	luminance input
SAT	12	saturation control input
n.c.	13	not connected
–(R–Y)	14	colour difference input
–(B–Y)	15	colour difference input
CON	16	contrast control input
BRI	17	brightness control input
GND	18	ground (0 V)
RO	19	RED output
GO	20	GREEN output

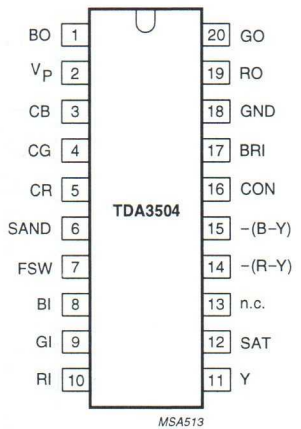


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 2)	0	13.2	V
V_6	sandcastle voltage (pin 6)	0	V_P	V
V_7	fast switch voltage (pin 7)	–0.5	3.0	V
$V_{12, 16, 17}$	control input voltage (pins 12, 16 and 17)	0	0.5 V_P	V
V_n	voltage on pins 1, 3, 4, 5, 8 to 11, 14, 15 and 19, 20	no external DC voltage		
$I_{1, 19, 20 (AV)}$	average output current (pins 1, 19 and 20)	–	–3	mA
$I_{1, 19, 20(M)}$	maximum output current (pins 1, 19 and 20)	–	–10	mA
$I_{16 (AV)}$	average output current (pin 16)	–	10	mA
I_{17}	input current (pin 17)	–	5	mA
P_{tot}	total power dissipation	–	1.7	W
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	storage temperature	–25	+150	°C

CHARACTERISTICS

V_P = 12 V; $V_{8, 9, 10(p-p)}$ = 1 V; $V_{11(p-p)}$ = 0.45 V; $V_{14(p-p)}$ = 1.05 V; $V_{15(p-p)}$ = 1.33 V; T_{amb} = 25 °C; measured in Figs 3 and 4; nominal settings of brightness, contrast and saturation; all referenced to pin 18; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 2)		10.8	12.0	13.2	V
I_P	supply current	note 1	–	95	125	mA
Colour difference inputs (pins 14 and 15)						
$V_{14(p-p)}$	–(R–Y) input signal (pin 14) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.05	1.48	V
$V_{15(p-p)}$	–(B–Y) input signal (pin 15) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.33	1.88	V
$I_{14, 15}$	input current during scanning		–	–	0.2	µA
$R_{14, 15}$	input resistance		1.0	–	–	MΩ
$V_{14, 15}$	internal DC voltage due to clamping	note 2	3.8	4.4	4.8	V
Saturation control (pin 12)						
V_{12}	control voltages (2)	maximum saturation	4.0	4.2	4.4	V
		nominal saturation 6 dB below maximum	2.9	3.1	3.3	V
		–26 dB saturation referenced to maximum	1.9	2.1	2.3	V
SAT	minimum saturation	V_{12} = 1.8 V	46	50	–	dB
I_I	input current		–	–	20	µA
(G–Y) matrix (see note 9)						
Luminance input (pin 11)						
$V_{11(p-p)}$	VBS input signal (peak-to-peak value)	note 3	–	450	630	mV
I_{11}	input current during scanning		–	–	0.4	µA
R_{11}	input resistance		1.0	–	–	MΩ
V_{11}	input DC voltage due to clamping	note 2	2.5	2.9	3.3	V
m	linearity	nominal settings	0.85	–	–	
RGB channels						
SIGNAL SWITCHING INPUT (PIN 7)						
V_7	normal state voltage; no insertion		0	–	0.4	V
V_7	voltage level for insertion on		0.9	–	3.0	V
C_I	input capacitance		–	–	10	pF
I_I	input current	V_7 = 0 to 3 V	–100	–	+450	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL INSERTION: RI (PIN 10); GI (PIN 9); BI (PIN 8)						
$V_{8, 9, 10(b\text{-}w)}$	external RGB input signals (black-to-white value)		–	1.0	1.4	V
$I_{8, 9, 10}$	input current during scanning		–	–	0.4	μA
$V_{8, 9, 10}$	internal DC voltage due to clamping	notes 2 and 4	4.0	4.5	5.0	V
Contrast control (pin 16)						
V_{16}	control voltages (2)	maximum contrast	4.0	4.2	4.4	V
		nominal contrast 3 dB below maximum	3.4	3.6	3.8	V
		–10 dB below maximum	2.6	2.8	3.0	V
CON	minimum contrast	referenced to maximum; $V_{16} = 2$ V	18	21	29	dB
RGB_{diff}	difference between RGB channels	contrast –10 dB below maximum	–	–	0.6	dB
Peak drive limiting						
V_{th}	threshold voltage	note 2	8.7	9.0	9.3	V
I_{16}	input current at contrast control input	$V_{1, 19, 20} \geq V_{th}$	10	20	30	mA
	internal signal limiting	referenced to nominal output amplitude; note 8	110	–	–	%
Brightness control (pin 17)						
V_{17}	control voltages (2)	brightness control range	1.0	–	3.0	V
		nominal brightness	–	2.0	–	V
I_I	input current		–	–	–10	μA
$\Delta V_{blk(b\text{-}w)}$	shift of black level in the control range referenced to the luminance signal (black-to-white value)	$\Delta V_{17} = 1$ V	–	40	–	%
	tracking		95	–	–	%
RGB outputs (emitter follower; pins 19, 20 and 1)						
$V_{19, 20, 1}$	output voltage	black-to-white positive	4.0	5.0	6.5	V
$\Delta V_{19, 20, 1}$	difference in black level between RGB channels due to variation of contrast control		–	–	10	mV
$I_{19, 20, 1}$	internal current source		2.0	3.0	–	mA
Gain data (at nominal brightness, contrast, saturation and white point settings)						
$G_{V19, 20, 1\text{-}11}$	voltage gain with respect to luminance input (pin 11)		22	24	26	dB
$\alpha_{19, 20, 1\text{-}11}$	frequency response of luminance path	f = 0 to 5 MHz	–	–	3	dB
$G_{V1\text{-}15}$; $G_{V19\text{-}14}$	voltage gain with respect to colour difference inputs (pins 14 and 15)		11	14	17	dB

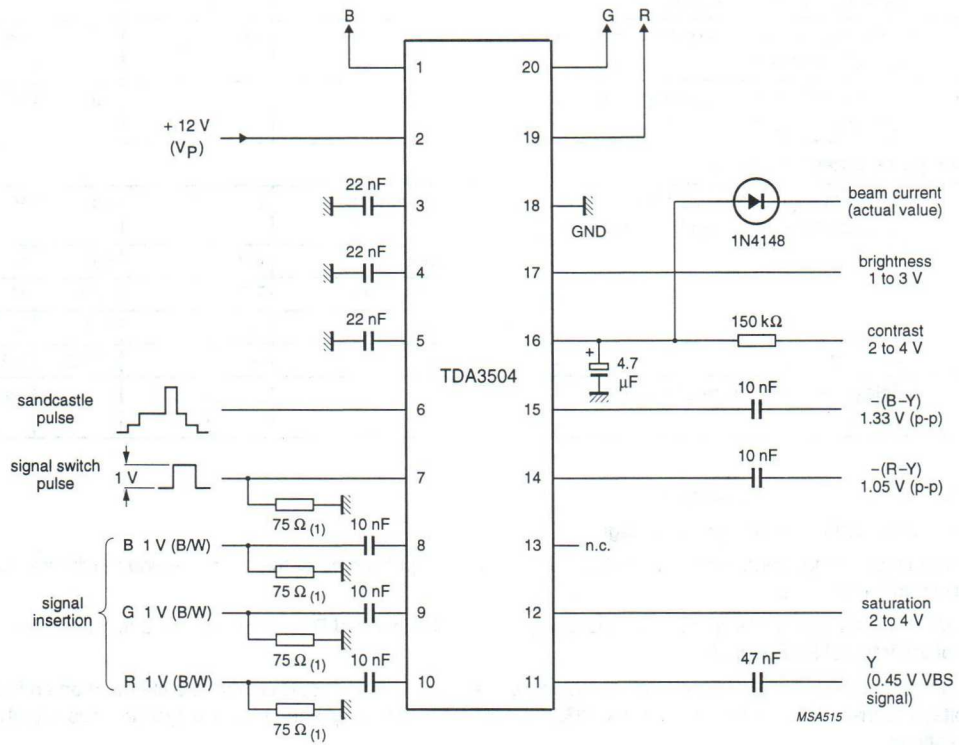
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{1-15}; α_{19-14}	frequency response of colour difference path	f = 0 to 2 MHz	–	–	3	dB
$G_{V19, 10}$; G_{V20-9}; G_{V1-8}	voltage gain with respect to inserted signals		12	14	16	dB
α_{19-10}; α_{20-9}; α_{1-8}	frequency response of inserted signal paths	f = 0 to 10 MHz	–	–	3	dB
$\Delta t_{19, 20, 1}$	difference in transition times between R, G and B channels		–	0	15	ns
t_d	delay time between signal switching and signal insertion		–25	–	+25	ns
$\Delta G_{19, 20, 1}$	difference in gain between normal and signal insertion mode		–	–	10	%
Sandcastle pulse detector (pin 6)						
V_6	the following amplitudes are required for separating the various pulses	horizontal and vertical blanking; notes 5 and 6	2.1	2.5	2.9	V
		horizontal; note 5	4.1	4.5	5.0	V
		clamping; notes 5 and 7	7.6	8.0	12.0	V
		no keying; note 5	–	–	1.0	V
I_I	input current		–	–	–110	µA
t_d	delay of leading edge of clamping pulse		–	0.5	–	µs

Notes

1. Maximum value 110 mA after warm-up.
2. Values are proportional to the supply voltage.
3. Clipping due to internal signal limitation may occur when the Y input is greater than nominal and maximum contrast and minimum brightness.
4. When $V_{7-18} < 0.4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

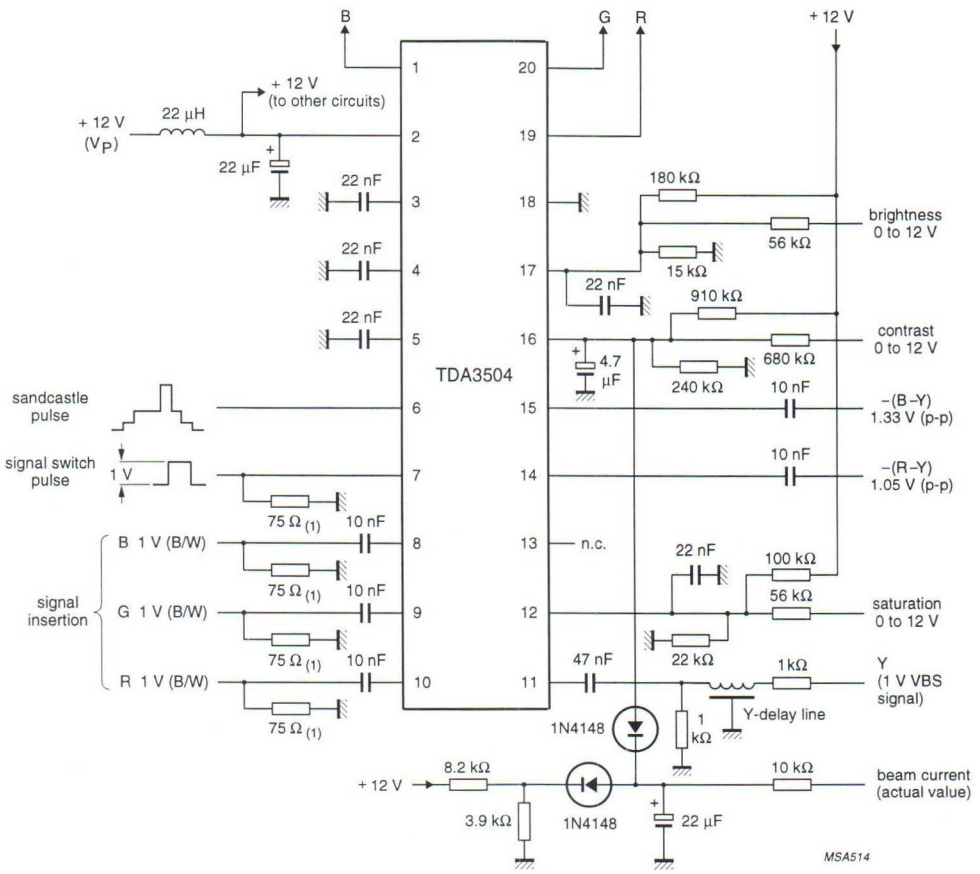
   When $V_{7-18} > 0.9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
5. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
6. Blanked to ultra-black (–25%).
7. Pulse duration ≥ 3.5 µs.
8. Internal signal limitation is allowed to start at 5.5 V after warm-up time.
9. Matrixed according to equation $V_{(G-Y)} = -0.51V_{-(R-Y)} - 0.19V_{-(B-Y)}$.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.

Fig.3 Basic application circuit diagram.



(1) When supplied via a 75 Ω line.

Fig.4 Typical application circuit diagram.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3505 and TDA3506 are monolithic integrated circuits which perform video control functions in a PAL/SECAM decoder. The TDA3505 is for negative colour difference signals −(R-Y), −(B-Y) and the TDA3506 is for positive colour difference signals +(R-Y), +(B-Y).

The required input signals are: luminance and colour difference (negative or positive) and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuits provide automatic cut-off control of the picture tube.

Features

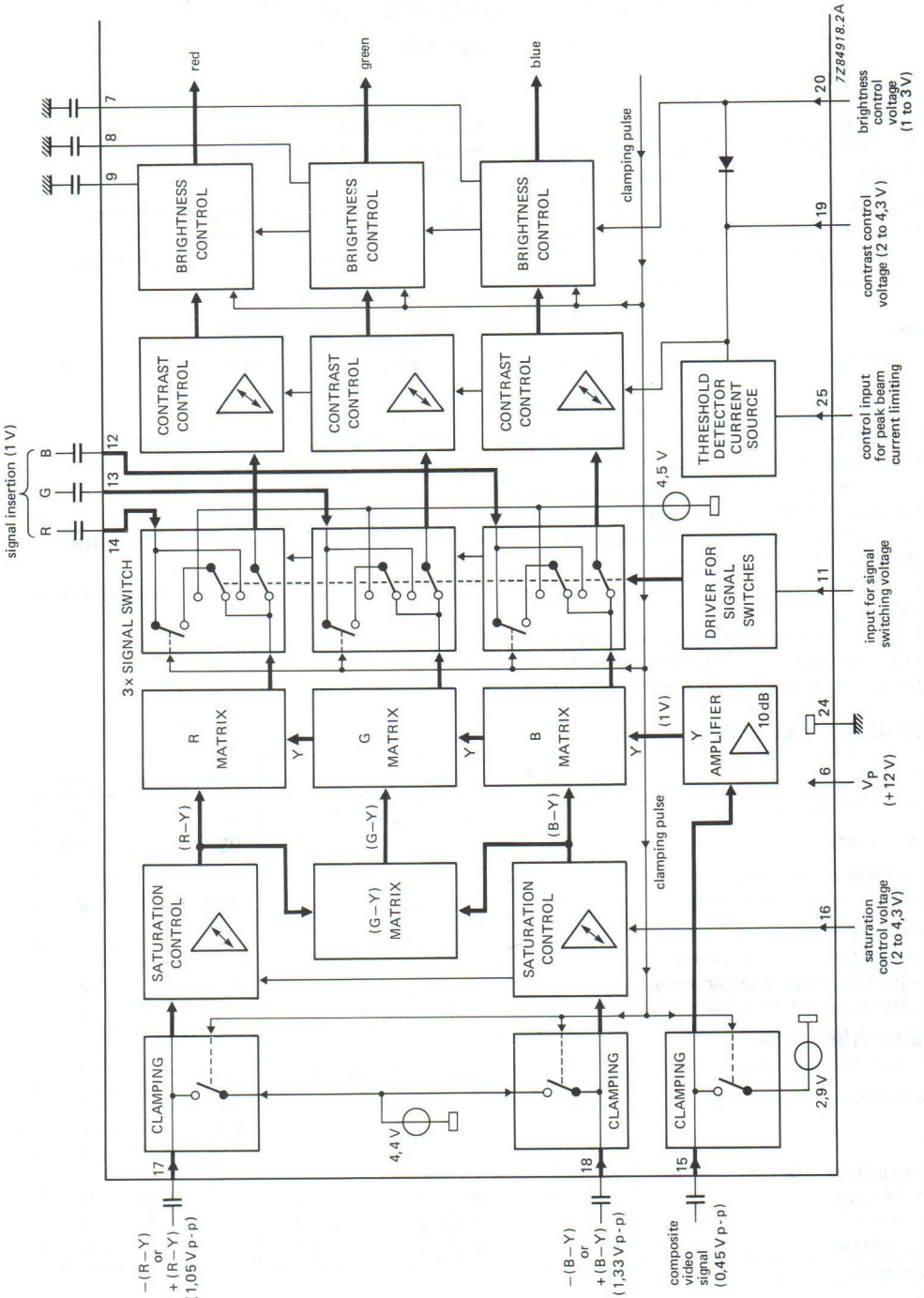
- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	95	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y) or +(B-Y) respectively		$V_{18-24(p-p)}$	–	1,33	–	V
−(R-Y) or +(R-Y) respectively		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12, 13, 14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).



Note Colour difference inputs are negative for TDA3505 or positive for TDA3506.

Fig. 1a Part of block diagram; continued in Fig. 1b.

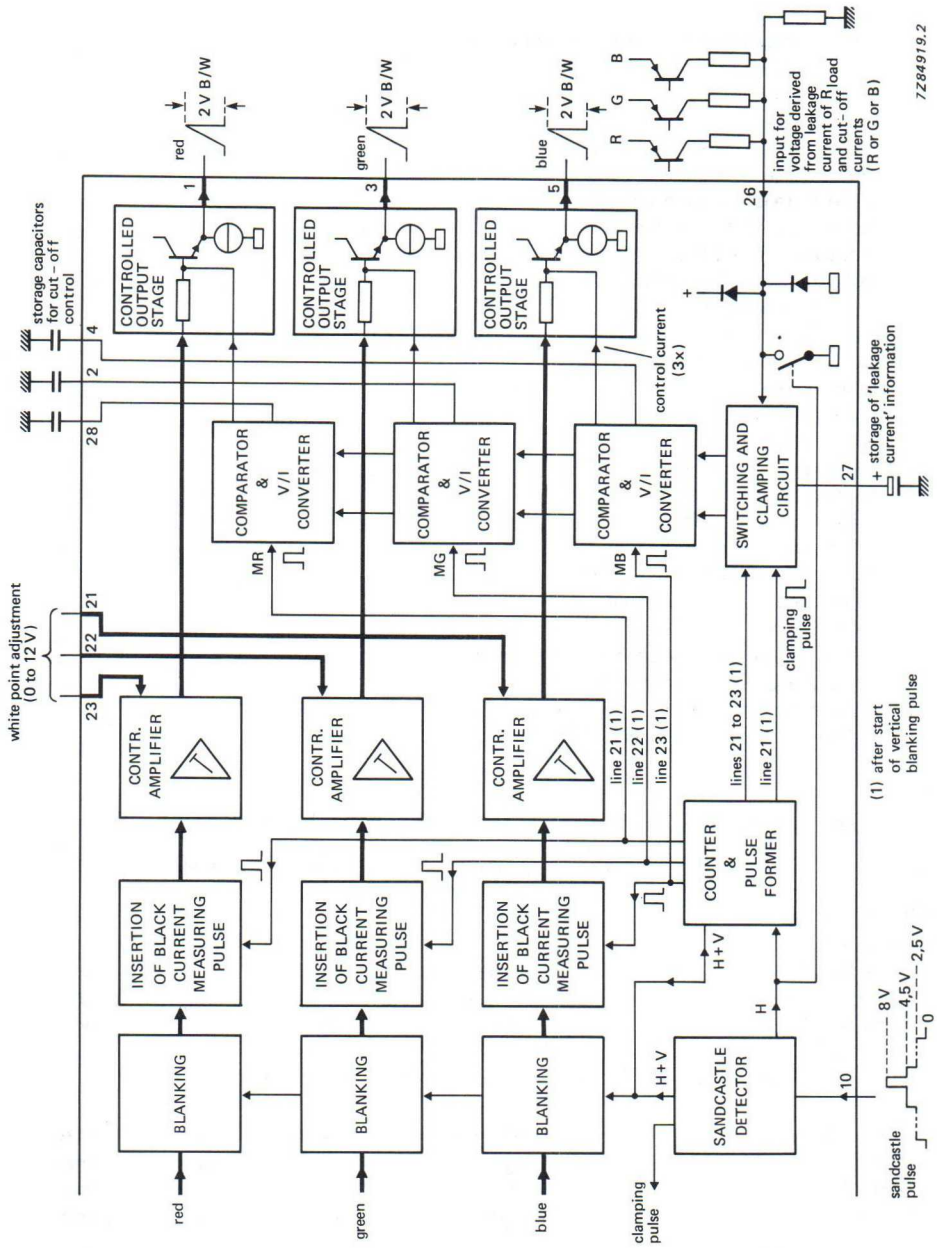


Fig. 1b Part of block diagram; continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	colour difference input –(R-Y) or +(R-Y) respectively
18	colour difference input –(B-Y) or +(B-Y) respectively
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	–0,5	3,0	V
at pins 16, 19, 20	$V_{16, 19, 20-24}$	0	0,5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1, 3, 5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1,7	W
Storage temperature range	T_{stg}	–25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12, 13, 14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	95	125*	mA
Colour difference inputs (pins 17, 18)						
(R-Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
(B-Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17, 18}$	–	–	1,0	μA
Input resistance		$R_{17, 18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17, 18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ

* < 110 mA after warm-up.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input capacitance		$C_{15\text{-}24}$	–	–	5	pF
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12, 13, 14}$	–	1,0	1,4	V
Input current during scanning		$I_{12, 13, 14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12, 13, 14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21, 22, 23}$ = 5,5 V		G_V	–	100	–	%
$V_{21, 22, 23}$ = 0 V		G_V	–35	–40	–	%
$V_{21, 22, 23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23-24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1, 3, 5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1, 3, 5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1, 3, 5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1, 3, 5}$	4,0	4,6	–	V
Internal current source		$I_{1, 3, 5}$	2,0	3,0	–	mA

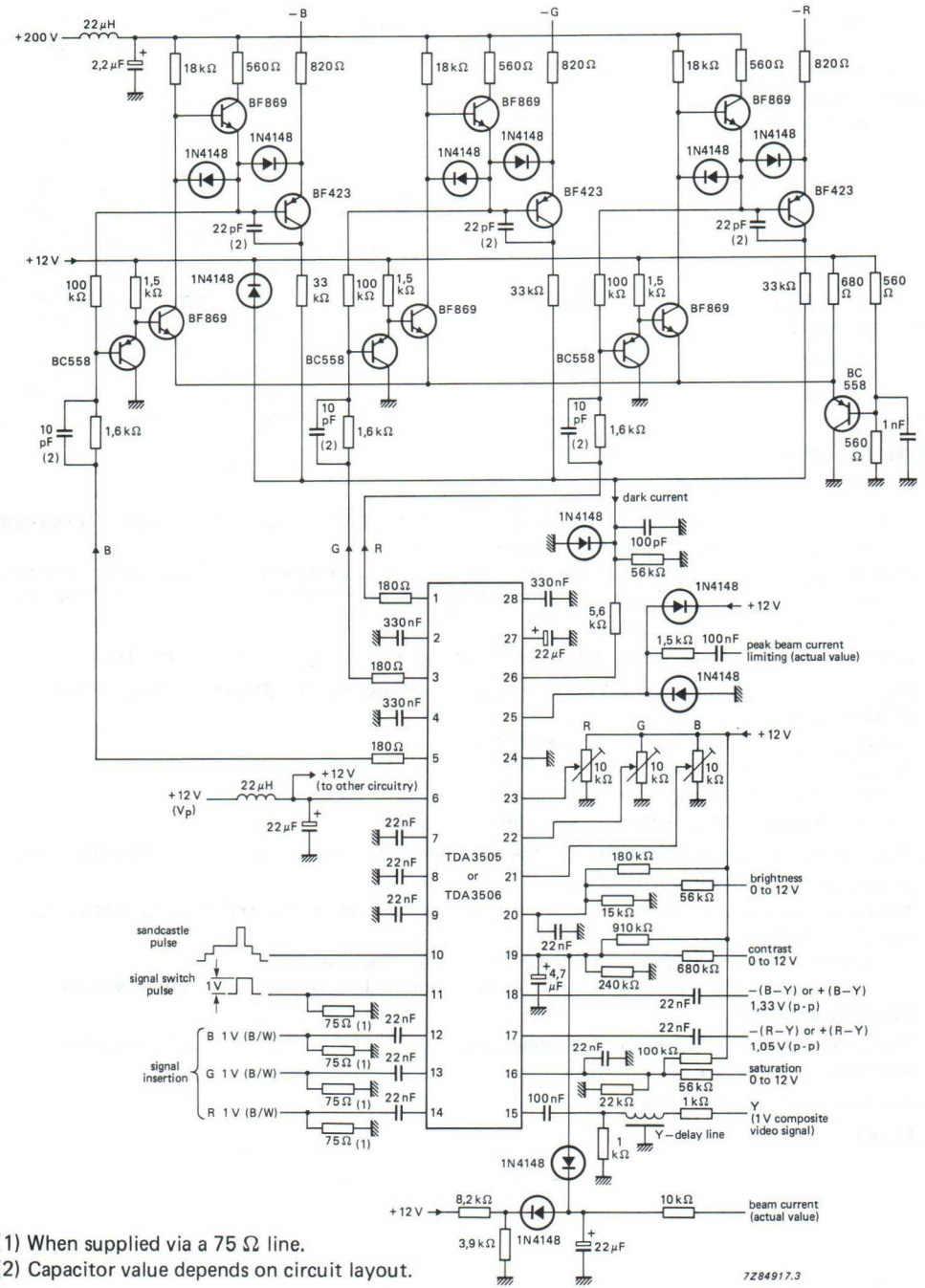
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24} > 0{,}9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5$ μs.



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using TDA3505 or TDA3506; colour difference inputs are negative for TDA3505 or positive for TDA3506.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3507 is a monolithic integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference $-(R-Y)$ and $-(B-Y)$, and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

The TDA3507 is the same as the TDA3505 but with RGB channel bandwidths of (typical) 16 MHz and an automatic cut-off cycle that ends in line 15.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G–Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1,33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

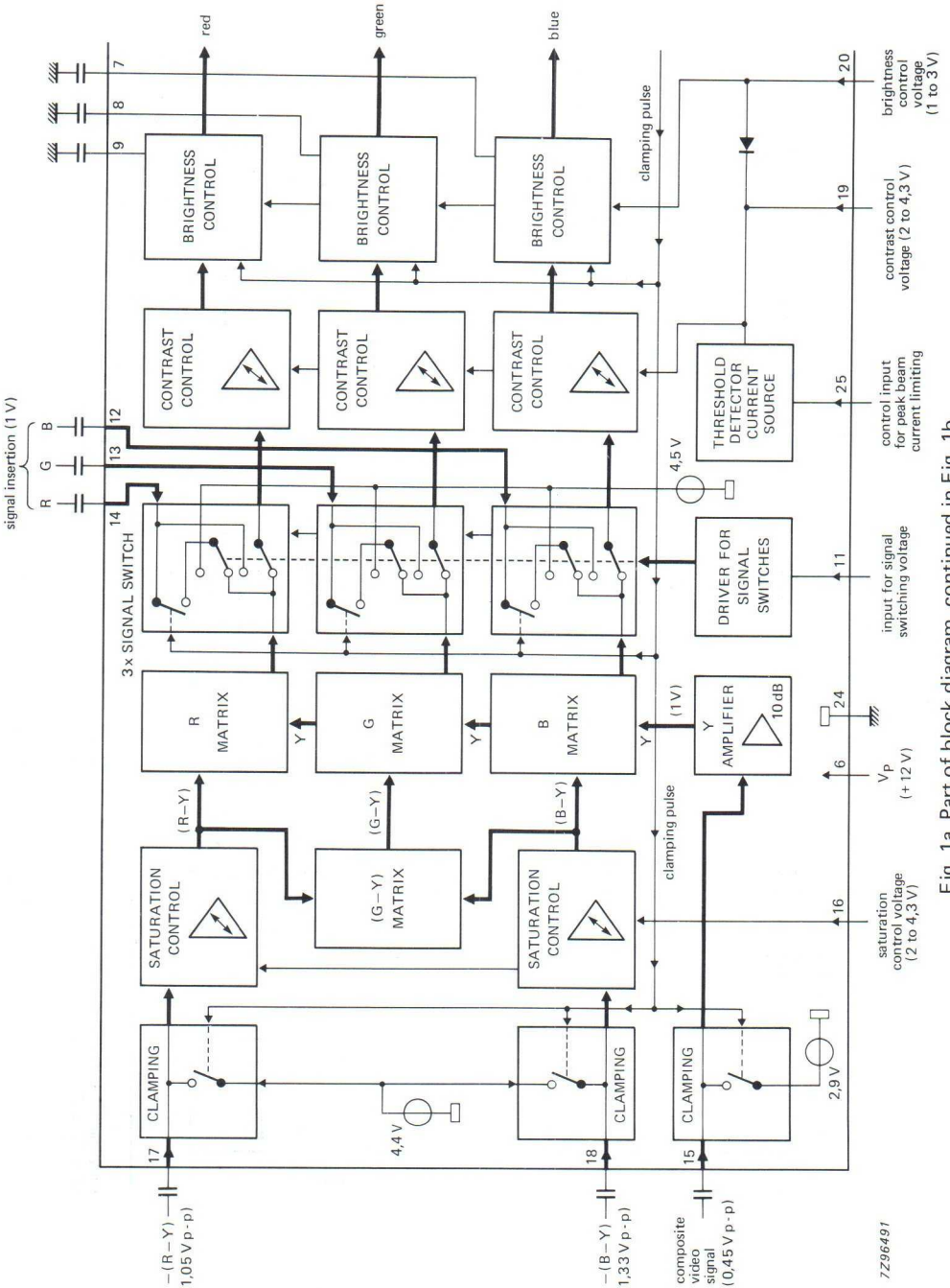


Fig. 1a Part of block diagram, continued in Fig. 1b.

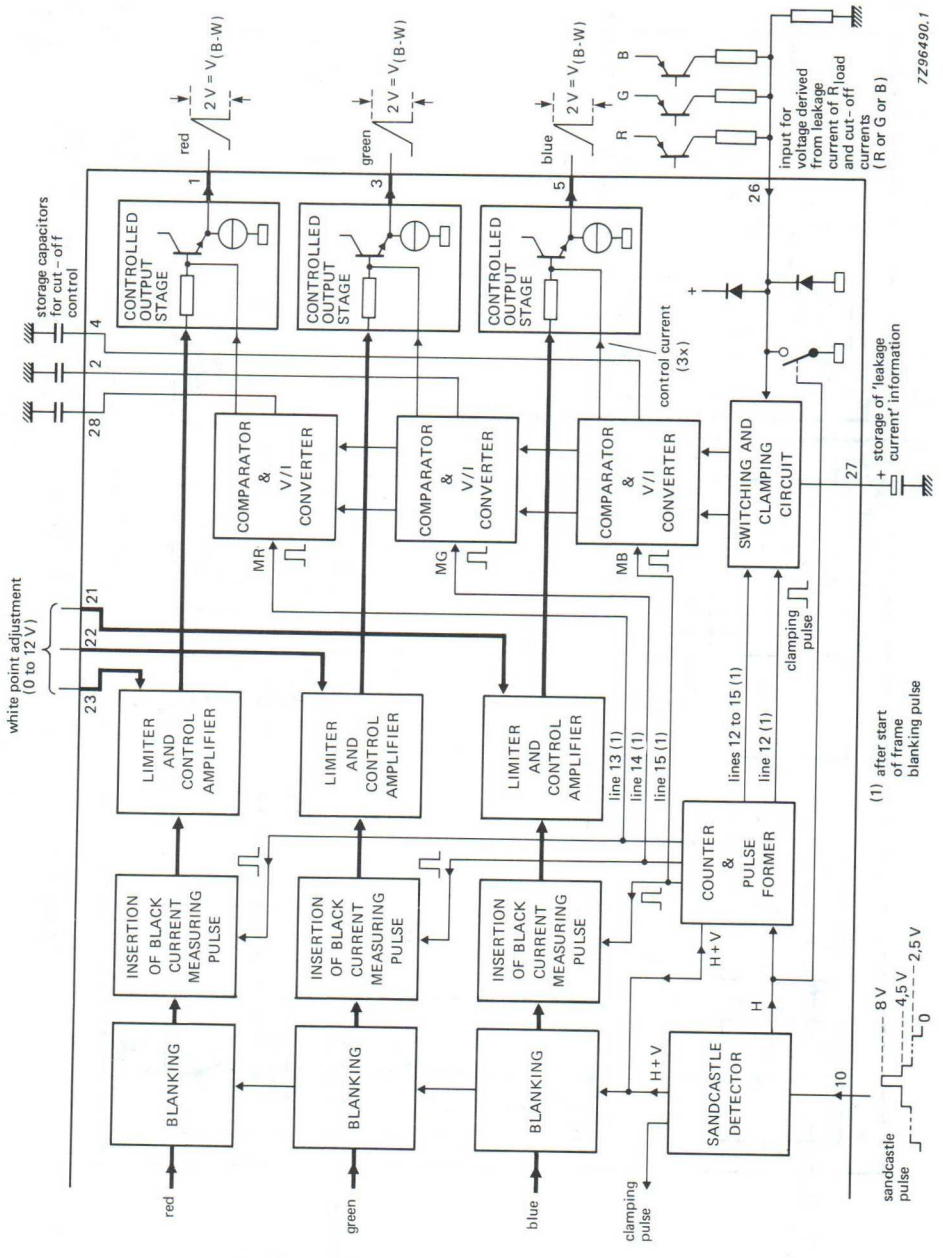


Fig. 1b Part of block diagram, continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	−	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	0,5V_P	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	−	3	mA
at pin 19	I_{19}	−	10	mA
at pin 20	I_{20}	−	5	mA
at pin 25	$-I_{25}$	−	5	mA
Total power dissipation	P_{tot}	−	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24}$ = 12,0 V; $V_{12,13,14(p-p)}$ = 1,0 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{18-24(p-p)}$ = 1,33 V; T_{amb} = 25 °C; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17,18}$	–	–	1,0	μA
Input resistance		$R_{17,18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	V_{16} = 1,8 V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* < 115 mA after warm-up

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1,0	1,4	V
Input current during scanning		$I_{12,13,14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5,5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4,0	4,6	–	V
Internal current source		$I_{1,3,5}$	2,0	3,0	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1,4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 16 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	3	–	dB
Frequency response of inserted signal paths	0 to 13 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain data (continued)						
Delay time between signal switching and signal insertion		t_d	−25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

   When $V_{11\text{-}24} > 0{,}9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:

   line 12: measurement of leakage current (R + G + B)
   line 13: measurement of red cut-off current
   line 14: measurement of green cut-off current
   line 15: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.

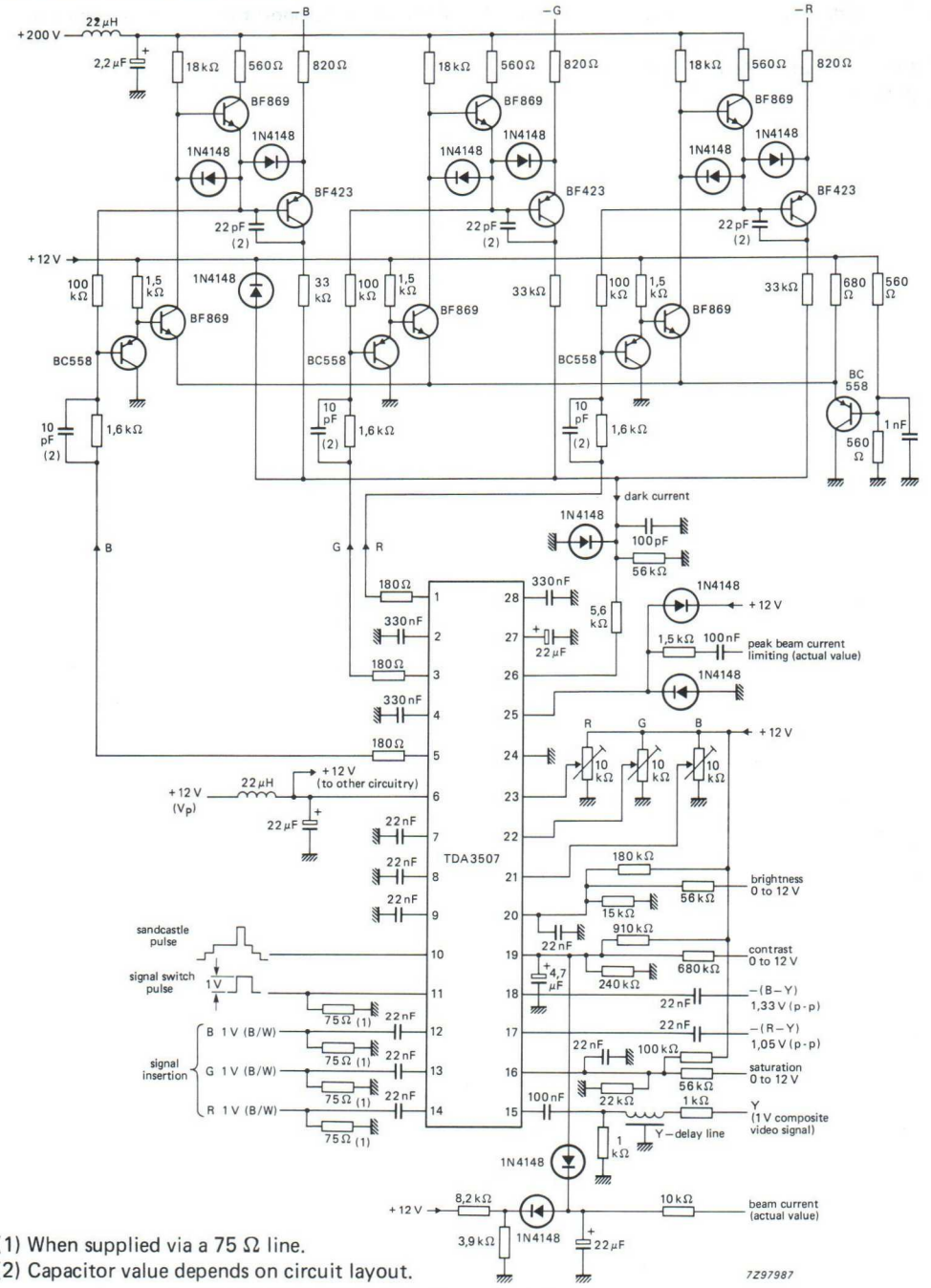
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.

   The internal blanking continues until the end of the last measured line.

   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.

7. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5\ \mu s$.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3507.

Video control combination circuit with automatic cut-off control

TDA3508

FEATURES

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G–Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube.

GENEREAL DESCRIPTION

The TDA3508 is a monolithic integrated circuit which performs video control functions in a PAL/SECAM dedoder for negative colour difference signals –(R–Y) and –(B–Y).

The required input signals are: luminance and colour difference and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuit provides automatic cut-off control of the picture tube.

QUICK REFERENCE DATA

All voltages referenced to pin 24 (ground).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 6)	–	12.0	–	V
I_P	supply current	–	95	–	mA
$V_{15(p-p)}$	composite video input signal (peak-to-peak value)	–	0.45	–	V
	colour difference input signals (peak-to-peak value)				
$V_{18(p-p)}$	–(B–Y)	–	1.33	–	V
$V_{17(p-p)}$	–(R–Y)	–	1.05	–	V
$V_{12, 13, 14(b-w)}$	inserted RGB signals (black-to-white value)	–	1.0	–	V
V_{10}	three-level sandcastle pulse				
	level 1	–	2.5	–	V
	level 2	–	4.5	–	V
	level 3	–	8.0	–	V
	control voltage ranges				
V_{20}	brightness	1.0	–	3.0	V
V_{19}	contrast	2.0	–	4.3	V
V_{16}	saturation	2.0	–	4.3	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3508	28	DIL	plastic	SOT117

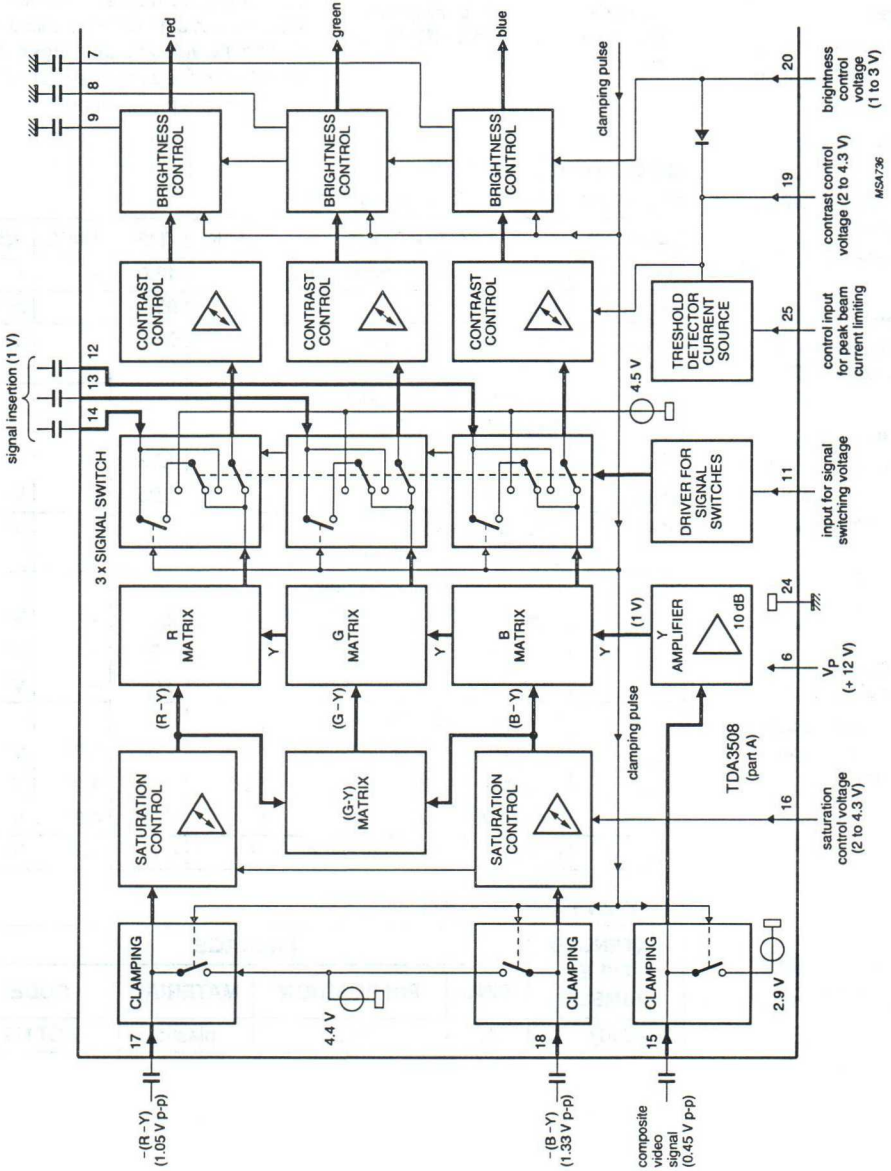


Fig.1 Part of block diagram; continued in Fig.2.

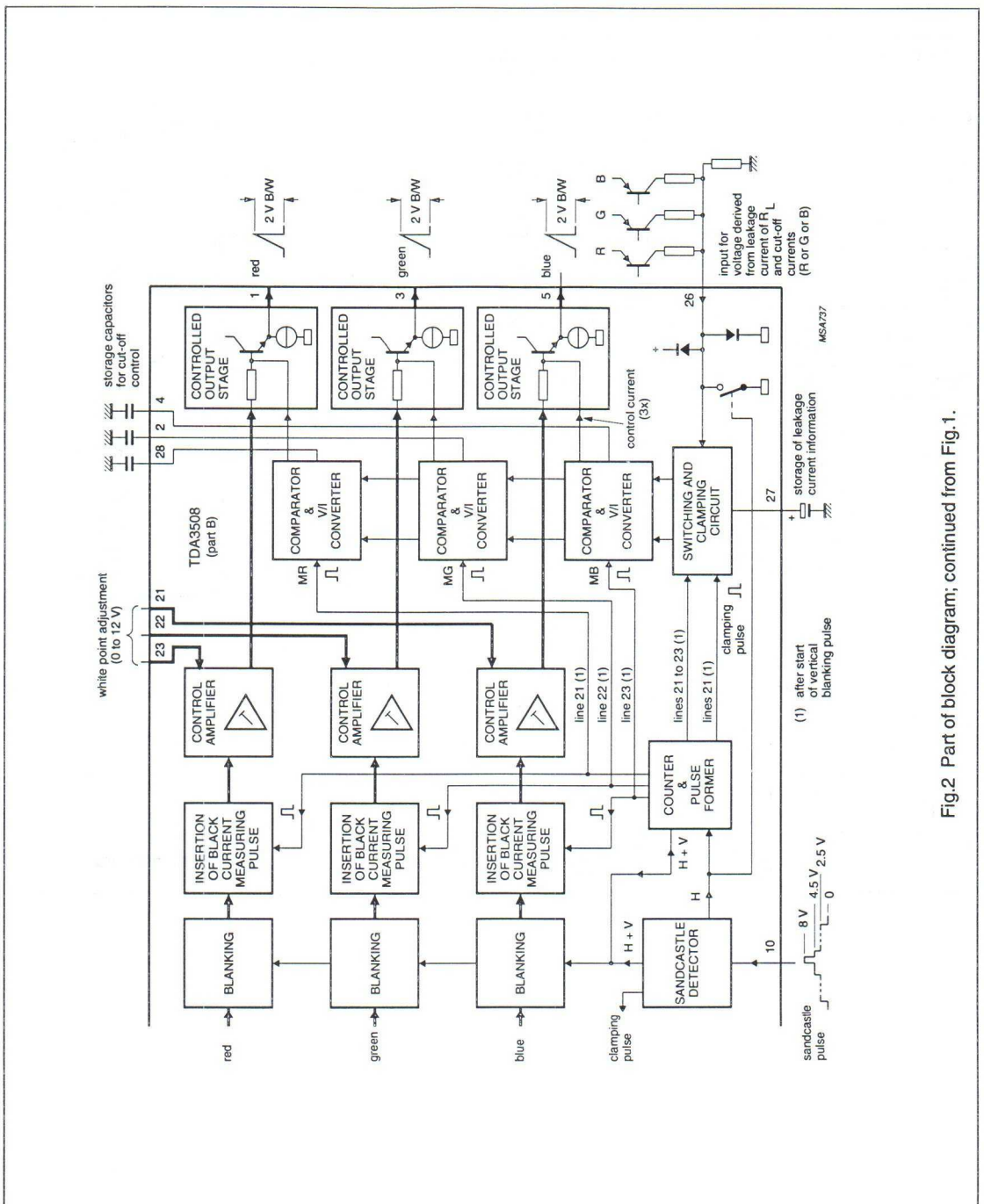


Fig.2 Part of block diagram; continued from Fig.1.

PINNING

SYMBOL	PIN	DESCRIPTION
RO	1	RED output
CGC	2	GREEN storage capacitor for cut-off control
GO	3	GREEN output
CBC	4	BLUE storage capacitor for cut-off control
BO	5	BLUE output
V_P	6	positive supply voltage (+12 V)
CB	7	BLUE storage capacitor for brightness
CG	8	GREEN storage capacitor for brightness
CR	9	RED storage capacitor for brightness
SC	10	sandcastle pulse input
FSW	11	fast switch for RGB inputs
BI	12	BLUE input (external signal)
GI	13	GREEN input (external signal)
RI	14	RED input (external signal)
Y	15	luminance input
SAT	16	saturation control input
-(R-Y)	17	colour difference input
-(B-Y)	18	colour difference input
CON	19	contrast control input
BRI	20	brightness control input
WPB	21	white point adjustment; BLUE
WPG	22	white point adjustment; GREEN
WPR	23	white point adjustment; RED
GND	24	ground (0 V)
PBL	25	control input for peak beam current limiting
ACO	26	automatic cut-off control input
CSL	27	storage capacitor for leakage current
CRC	28	RED storage capacitor for cut-off control

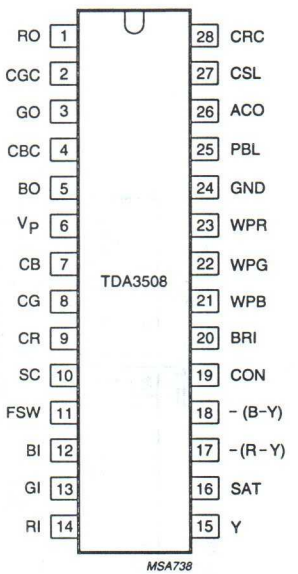


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 6)	0	13.2	V
	voltages			
V_n	pins 10, 21, 22, 23, 25 and 26	0	V_P	V
V_{11}	pin 11	−0.5	3.0	V
$V_{16, 19, 20}$	pins 16, 19 and 20	0	$0.5V_P$	V
V_n	pins 1-5, 7-9, 12-15, 17, 18, 27 and 28	no external DC voltage		
	currents			
$I_{1, 3, 5}$	pins 1, 3 and 5	−	−3	mA
I_{19}	pin 19	−	10	mA
I_{20}	pin 20	−	5	mA
I_{25}	pin 25	−	5	mA
P_{tot}	total power dissipation	−	1.7	W
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	storage temperature	−25	+150	°C
ESD	electrostatic handling (note 1)			
	pin 10	−500	+450	V
	all other pins	−500	+500	V

Note

1. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

CHARACTERISTICS

V_P = 12 V; $V_{12, 13, 14(p-p)}$ = 1 V; $V_{15(p-p)}$ = 0.45 V; $V_{17(p-p)}$ = 1.05 V; $V_{18(p-p)}$ = 1.33 V; T_{amb} = 25 °C; measured in Fig.4; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages referenced to pin 24; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 6)		10.8	12.0	13.2	V
I_P	supply current	note 1	–	95	125	mA
Colour difference inputs (pins 17 and 18)						
$V_{17(p-p)}$	–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.05	1.48	V
$V_{18(p-p)}$	–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.33	1.88	V
$I_{17, 18}$	input current during scanning		–	–	1.0	µA
$R_{17, 18}$	input resistance		1.0	–	–	MΩ
$V_{17, 18}$	internal DC voltage due to clamping	note 2	3.8	4.4	4.8	V
Saturation control (pin 16)						
V_{16}	control voltages	note 2				
	maximum saturation		4.0	4.2	4.4	V
	nominal saturation	6 dB below maximum	2.9	3.1	3.3	V
	–26 dB saturation	referenced to maximum	1.9	2.1	2.3	V
SAT	minimum saturation	V_{16} = 1.8 V	46	50	–	dB
I_{16}	input current		–	–	20	µA
(G–Y) matrix						
Matrixed according to equation $V_{(G-Y)} = -0.51\ V_{(R-Y)} - 0.19\ V_{(B-Y)}$						
Luminance input (pin 15)						
$V_{15(p-p)}$	composite video input signal (peak-to-peak value)		–	450	630	mV
I_{15}	input current during scanning		–	–	1.0	µA
R_{15}	input resistance		0.1	–	–	MΩ
C_{15}	input capacitance		–	–	5	pF
V_{15}	input DC voltage due to clamping	note 2	2.5	2.9	3.3	V
m	linearity	nominal settings	0.85	–	–	
RGB channels						
SIGNAL SWITCHING INPUT (PIN 11)						
V_{11}	normal state; no insertion		0	–	0.4	V
V_{11}	level for insertion on		0.9	–	3.0	V
C_{11}	input capacitance		–	–	10	pF
I_{11}	input current	V_{11} = 0 to 3 V	–100	–	+450	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL INSERTION: R (PIN 14); G (PIN 13); B (PIN 12)						
$V_{14, 13, 12(b-w)}$	external RGB input signals (black-to-white value)		–	1.0	1.4	V
$I_{14, 13, 12}$	input current during scanning		–	–	1.0	μA
$V_{14, 13, 12}$	internal DC voltage due to clamping	notes 2 and 3	4.0	4.5	5.0	V
Contrast control (pin 19)						
V_{19}	control voltages	note 2				
	maximum contrast		4.0	4.2	4.4	V
	nominal contrast	3 dB below maximum	3.4	3.6	3.8	V
	–10 dB below maximum		2.6	2.8	3.0	V
CON	minimum contrast	referenced to maximum; V_{19} = 2 V	18	21	29	dB
I_{19}	input current	V_{25} > 6 V	–	–	2.0	μA
	difference between RGB channels	contrast –10 dB below maximum	–	–	0.6	dB
Peak beam current limiting (pin 25)						
V_{25}	internal DC bias voltage	note 2	5.3	5.5	5.7	V
R_{25}	input resistance		–	10	–	kΩ
I_{19}	input current at contrast control input	V_{25} = 4.5 V	10	20	34	mA
Brightness control (pin 20)						
V_{20}	control voltage	note 2	1.0	–	3.0	V
I_{20}	input current		–	–	–10	μA
	shift of black level in the control range referenced to the luminance signal (black-to-white)	ΔV_{20} = 1 V	–	±50	–	%
	tracking		95	–	–	%
Internal signal limiting (RGB)						
	signal limiting referenced to nominal luminance and nominal black level					
	black		–	–25	–	%
	white		115	120	125	%
White point adjustment (pins 21, 22 and 23; note 2)						
G_v	AC voltage gain	note 4				
	$V_{21, 22, 23}$ = 5.5 V		–	100	–	%
	$V_{21, 22, 23}$ = 0 V		–35	–40	–	%
	$V_{21, 22, 23}$ = 12 V		+35	+40	–	%
$R_{21, 22, 23}$	input resistance		–	20	–	kΩ

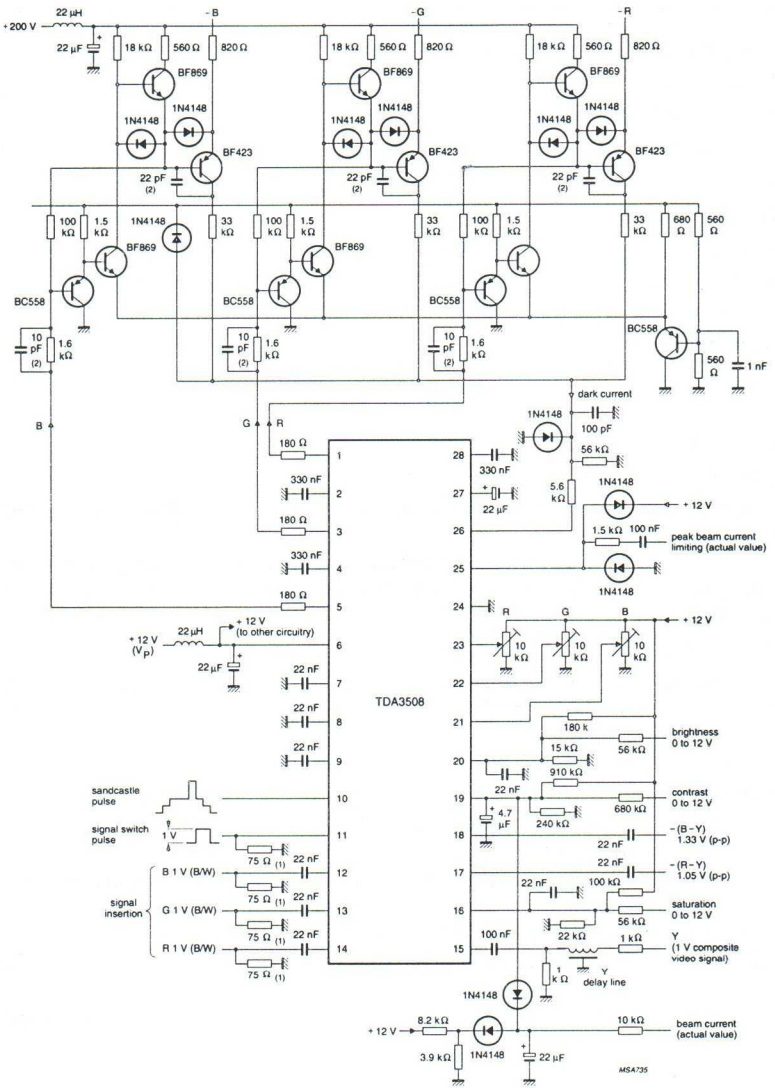
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs (emitter follower; pins 1, 3 and 5)						
$V_{1, 3, 5}$	output voltage; black-to-white		1.5	2.0	2.5	V
$V_{1, 3, 5}$	black level without automatic cut-off control	note 2; $V_{28, 2, 4} = 10$ V	6.1	6.9	7.7	V
$\Delta V_{1, 3, 5}$	difference in black level between RGB channels due to variation of contrast control		–	–	10	mV
$V_{1, 3, 5}$	cut-off control range	note 2	4.0	4.6	–	V
$I_{1, 3, 5}$	internal current source		2.0	3.0	–	mA
Automatic cut-off control (pin 26; notes 2 and 5)						
V_{26}	input voltage		0	–	6.5	V
V_{26}	voltage difference between cut-off current measurement (note 6) and leakage current measurement (note 7)		0.5	0.64	0.72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data (at nominal brightness, contrast, saturation and white point settings)						
$G_{v1, 3, 5-15}$	voltage gain with respect to luminance input (pin 15)		14	16	18	dB
$\alpha_{1, 3, 5-15}$	frequency response of luminance path	f = 0 to 5 MHz	–	–	3	dB
G_{v5-18}; G_{v1-17}	voltage gain with respect to colour difference inputs (pins 17 and 18)		3	6	9	dB
α_{5-18}; α_{1-17}	frequency response of colour difference paths	f = 0 to 2 MHz	–	–	3	dB
G_{v1-14}; G_{v3-13}; G_{v5-12}	voltage gain with respect to inserted signals		4	6	8	dB
α_{1-14}; α_{3-13}; α_{5-12}	frequency response of inserted signal paths	f = 0 to 10 MHz	–	–	3	dB
t_r, t_f	rise and fall times of RGB output signals (pins 1, 3 and 5)		–	40	–	ns
$\Delta t_{1, 3, 5}$	difference in transit times between R, G and B channels		–	0	15	ns
t_d	delay time between signal switching and signal insertion		–25	–	+25	ns
$\Delta G_{v1, 3, 5}$	difference in gain between normal and signal insertion mode		–	–	10	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (pin 10)						
V_{10}	the following amplitudes are required for separating the various pulses	note 8				
	horizontal and vertical blanking	note 9	1.0	1.5	2.0	V
	required pulses (H + V)		2.1	2.5	2.9	V
	horizontal		3.0	3.5	4.0	V
	required pulses (H)		4.1	4.5	5.0	V
	clamping	note 10	6.5	7.0	7.5	V
	required pulses		7.6	–	12.0	V
	no keying		–	–	1.0	V
I_{10}	input current		–	–	–110	µA

Notes

1. Maximum value < 110 mA after warm-up.
2. Values are proportional to the supply voltage.
3. When $V_{11\text{-}24}$ < 0.4 V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24}$ > 0.9 V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
4. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5.5 V is supplied.
5. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current.
6. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
7. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
8. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
9. Blanked to ultra-black (–25%).
10. Pulse duration ≥ 3.5 µs.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.

(2) Capacitor value depends on circuit layout

Fig.4 Typical application circuit diagram using TDA3508; colour difference inputs are negative.

PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

QUICK REFERENCE DATA

Supply voltage	V_{1-27}	type.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	5,25	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for data insertion	V_{9-27}	min.	0,9	V
Blanking input voltage	V_{8-27}	typ.	1,5	V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

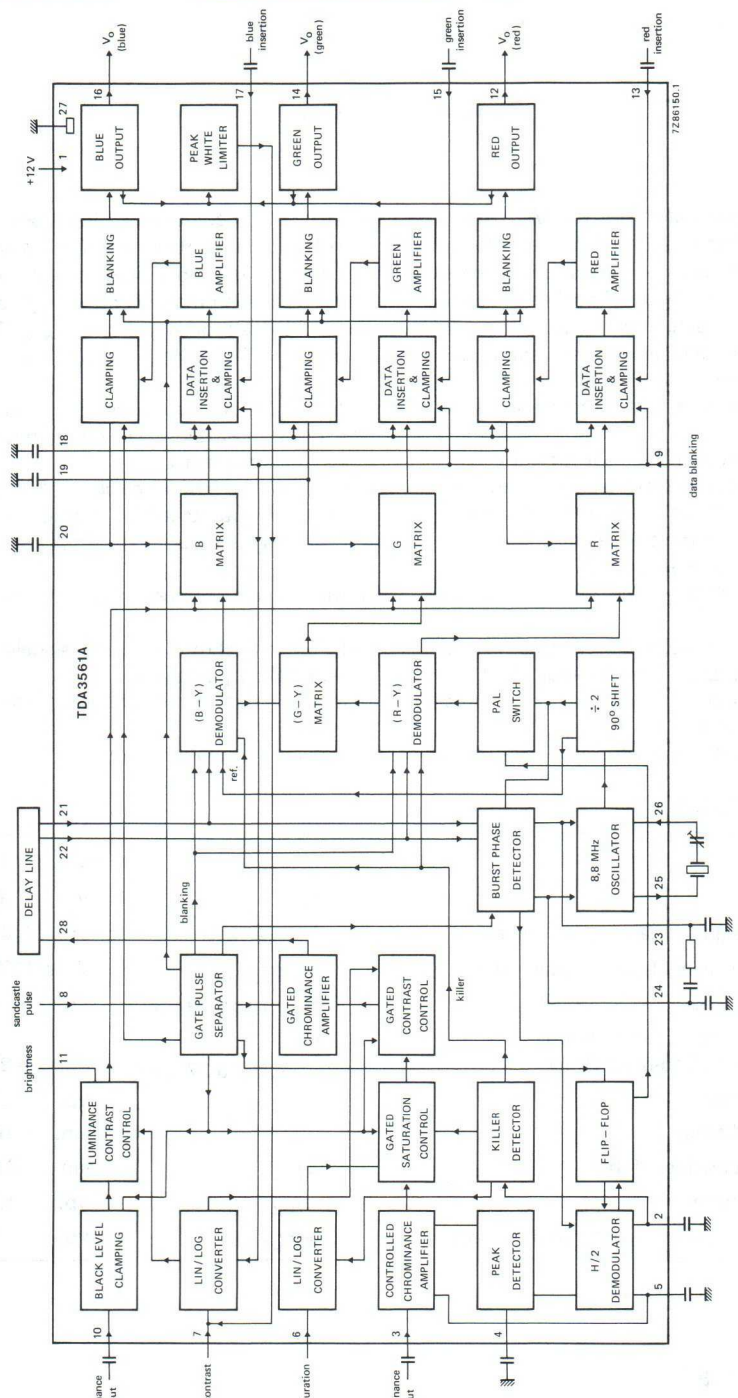


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1-27}$	max.	13,2	V
Total power dissipation; see also Fig. 2	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{1-27}$	typ.	12	V
			8 to 13,2	V
Supply current		typ.	85	mA
		<	115	mA
Total power dissipation	P_{tot}	typ.	1,0	W
		<	1,4	W
Luminance input (pin 10)				
Input voltage (peak-to-peak value); note 1	$V_{10-27(p-p)}$	typ.	0,45	V
Input level before clipping	V_{10-27}	<	2	V
Input current; input level 2 V, clamp not active	I_{10}	typ.	0,15	μA
		<	1	μA
Contrast control range (see Fig. 3)			−17 to + 3	dB
Control voltage for 40 dB attenuation	V_{7-27}	typ.	1,2	V
Input current contrast control at $V_{7-27} = 3$ V	I_7	<	10	μA
Chrominance amplifier				
Input voltage (peak-to-peak value); note 2	$V_{3-27(p-p)}$	typ.	550	mV
			55 to 1100	mV
Input impedance	$\lvert Z_{3-27}\rvert$	typ.	9	kΩ
			6 to 12	kΩ
Input capacitance	C_{3-27}	typ.	4	pF
		<	6	pF
A.C.C. control range		>	30	dB
Change of the burst signal at the output over the whole control range		<	1,5	dB
Gain at nominal contrast/saturation pin 3 to pin 28; note 3		>	32	dB
Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak	$V_{28-27(p-p)}$	typ.	1,7	V
Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ	$V_{28-27(p-p)}$	typ.	4,0	V

CHARACTERISTICS (continued)

Chrominance amplifier (continued)

Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)}$ = 2 V up to $V_{3\text{-}27(p\text{-}p)}$ = 1 V	d	typ. <	1,5 % 5 %
Frequency response between 0 and 5 MHz			−2 dB
Saturation control range (see Fig. 4)		>	50 dB
Input current saturation control at $V_{6\text{-}27}$ = 3 V	I_6	<	15 μA
Tracking between luminance and chrominance with contrast control over a range of 10 dB		<	2 dB
Cross-coupling between luminance and chrominance amplifier; note 10		<	−46 dB
Signal-to-noise ratio at nominal input signal; note 11	S/N	>	56 dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	<	± 5°
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	typ.	25 Ω
Maximum output current	I_{28}	<	15 mA

Reference part

Phase locked loop:			
– catching range; note 4		> typ.	500 Hz 700 Hz
– phase shift; note 5		<	5°
Oscillator:			
– temperature coefficient of oscillator frequency; note 4		typ.	−1,5 Hz/K
– frequency deviation for V_P changing from 10 to 13,2 V; note 4		typ.	40 Hz
– input resistance (pin 26)	$R_{26\text{-}27}$	typ. 260 to 420	340 Ω Ω
– input capacitance (pin 26)	$C_{26\text{-}27}$	<	10 pF
– output resistance (pin 25)	$R_{25\text{-}27}$	typ. 100 to 200	150 Ω Ω
– output voltage (peak-to-peak value; pin 25)	$V_{25\text{-}27(p\text{-}p)}$	typ.	700 mV
A.C.C. generation:			
– reference voltage (pin 4)	$V_{4\text{-}27}$	typ.	4,9 V
– control voltage at nominal input signal (pin 2)	$V_{2\text{-}27}$	typ.	5,1 V
– control voltage without chrominance input (pin 2)	$V_{2\text{-}27}$	typ.	2,65 V
– colour-off voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,15 V
– colour-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,4 V
– identification-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	1,9 V
– change in burst amplitude with supply voltage (± 10%)		proportional	
– change in burst amplitude with temperature		typ. <	0,1 %/K 0,25 %/K
– voltage at pin 5 at nominal input signal	$V_{5\text{-}27}$	typ.	5 V

Demodulator part

Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6	$V_{21\text{-}22(p\text{-}p)}$	typ.	100 mV
Input impedance between pins 21 and 22	$\lvert Z_{21\text{-}22}\rvert$	typ.	2 kΩ
Ratio of demodulated signals for equal input signals at pins 21 and 22 (B−Y)/(R−Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78 ± 10%
(G−Y)/(R−Y); no (B−Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	−0,51 ± 10%
(G−Y)/(B−Y); no (R−Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	−0,19 ± 25%
Frequency response between 0 and 1 MHz			−3 dB
Cross talk between colour demodulated signals		>	40 dB
Phase difference between (R−Y) signal and (R−Y) reference signal		<	5°
Phase difference between (R−Y) and (B−Y) reference signals		typ.	90° 85 to 95°

R.G.B. matrix and amplifiers

Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,4 V 4,5 to 6,3 V
Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R−Y) signal	$V_{12\text{-}27(p\text{-}p)}$	typ.	5,25 V 3,7 to 6,7 V
Maximum peak white level; note 7		typ.	9,3 V 9,0 to 9,6 V
Maximum output current	$I_{12,14,16}$	<	15 mA
Black level at the output for a brightness control voltage of 2 V	$V_{12,14,16\text{-}27}$	typ.	2,6 V
Difference in black level between the three channels at an output level of 3 V; note 8	ΔV	<	200 mV
Black level shift with vision contents		<	40 mV
Brightness control voltage range	see Fig. 5		
Input current brightness control	I_{11}	<	50 μA
Variation of black level with temperature	ΔV	typ. <	0,35 mV/K 1,0 mV/K
Variation of black level with contrast control	ΔV	typ. <	10 mV 200 mV
Relative spread between the R, G and B output signals		<	10 %
Relative black-level variation between the three channels during variation of contrast and supply voltage		typ. <	0 mV 20 mV

CHARACTERISTICS (continued)

RGB matrix and amplifier (continued)

Differential black-level drift over a temperature range of 40 °C		typ. <	0 mV 20 mV
Blanking level at the RGB outputs		typ. 1,9 to 2,3	2,1 V V
Difference in blanking level of the three channels		typ.	0 mV
Differential blanking level drift over a temperature range of 40 °C		typ.	0 mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	typ.	1,1
Signal-to-noise ratio of output signals; note 11	S/N	>	62 dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		typ. <	40 mV 150 mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		typ. <	75 mV 150 mV
Output impedance of RGB outputs	$\lvert Z_{12,14,16-27} \rvert$	typ.	50 Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3 dB

Signal insertion (pins 13,15 and 17)

Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak	$V_{13,15,17-27(p-p)}$	typ. 0,85 to 1,1	1 V V
Difference between the black levels of the RGB signals and the inserted signals at the output; note 9	ΔV	<	260 mV
Output rise time	t_r	typ. <	40 ns 80 ns
Differential delay time for the three channels	t_d	typ. <	0 ns 40 ns
Input current	$I_{13,15,17}$	<	10 μA

Data blanking (pin 9)

Input voltage for no data insertion	V_{9-27}	<	0,4 V
Input voltage for data insertion	V_{9-27}	>	0,9 V
Maximum input voltage	V_{9-27}	<	3 V
Delay of data blanking	t_d	<	20 ns
Input current	I_9	<	35 μA
Input impedance	$\lvert Z_{9-27} \rvert$	typ.	10 kΩ
Suppression of the internal RGB signals when $V_{9-27} > 0,9$ V		>	46 dB

Sandcastle input (pin 8)

Level at which the RGB blanking is activated	V_{8-27}	typ. 1,5 V 1 to 2 V
Level at which burst gating and clamping pulse are separated	V_{8-27}	typ. 7,0 V 6,5 to 7,5 V
Delay between black level clamping and burst gating pulse	t_d	typ. 0,4 μs
Input current for:		
V_{8-27} = 0 to 1 V	$-I_8$	< 1 mA
V_{8-27} = 1 to 8,5 V	I_8	typ. 20 μA
V_{8-27} = 8,5 to 12 V	I_8	< 2 mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

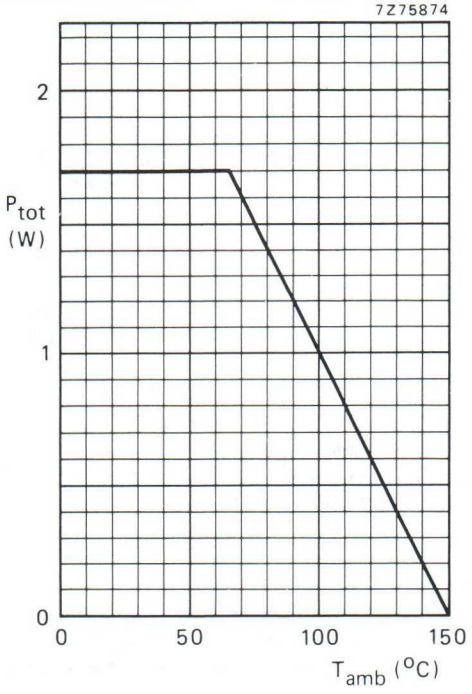


Fig. 2 Power derating curve.

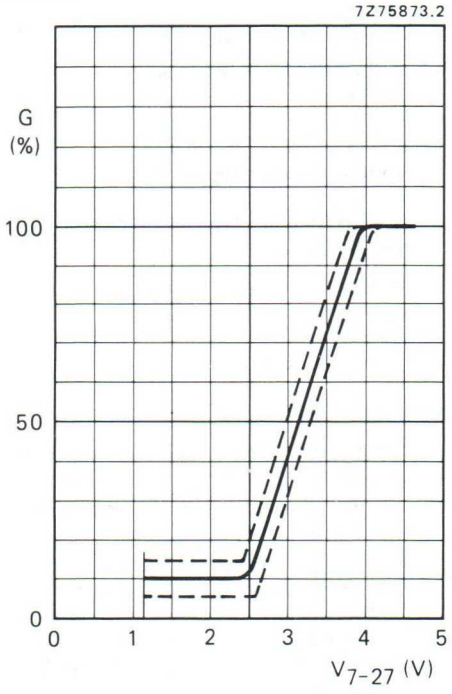


Fig. 3 Contrast control voltage range.

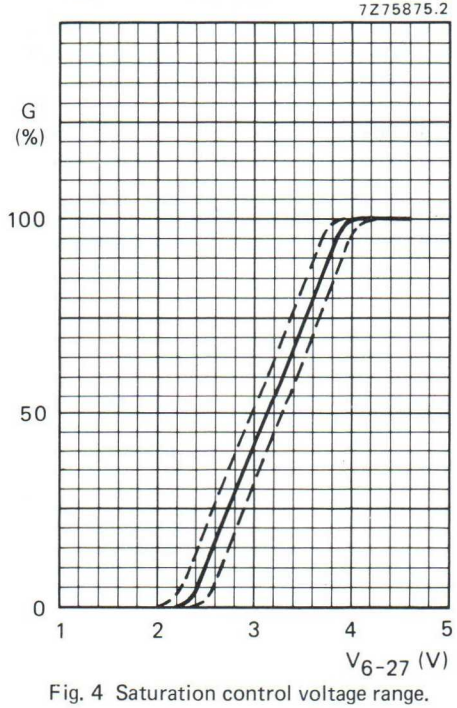


Fig. 4 Saturation control voltage range.

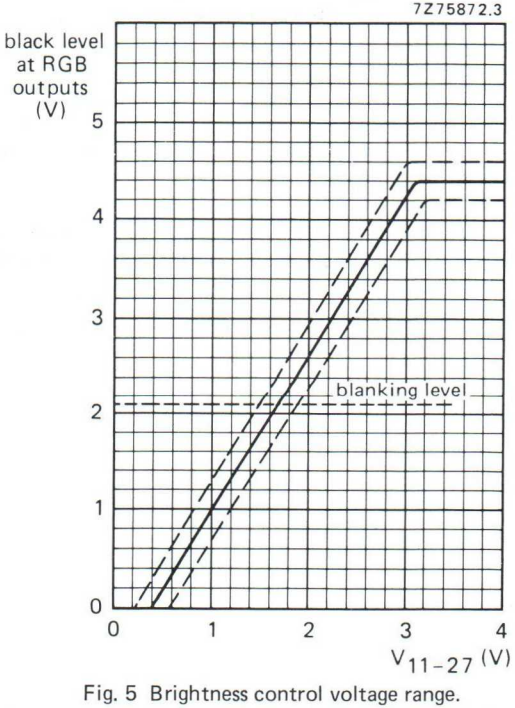


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

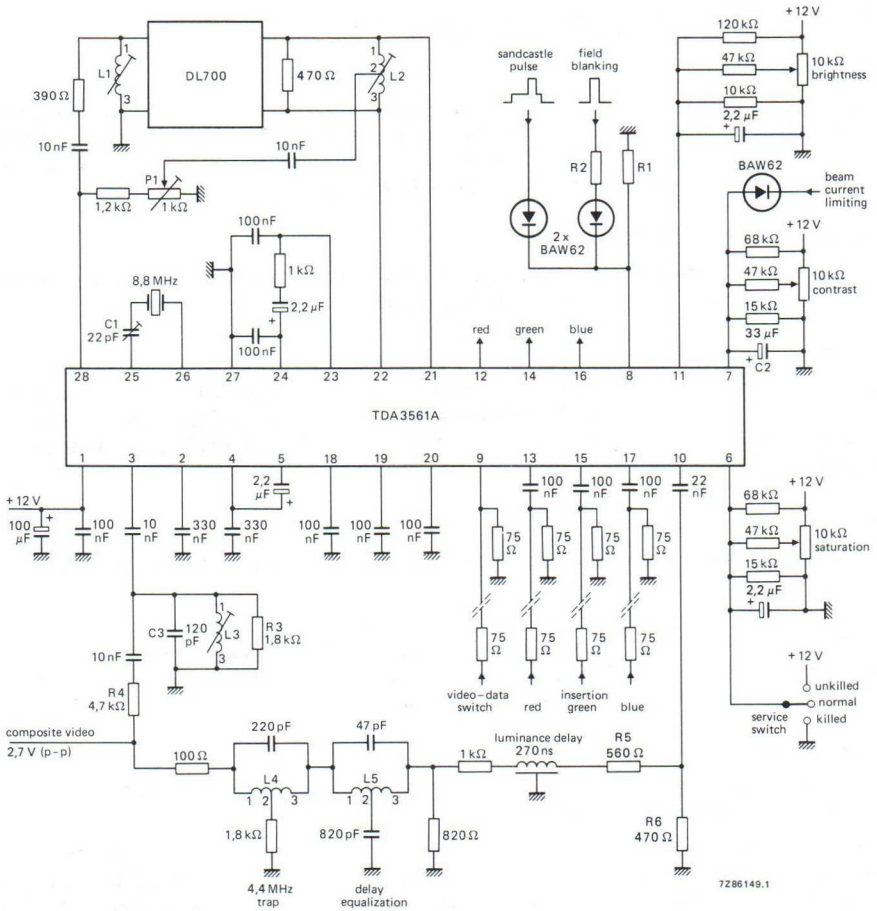


Fig. 6 Application circuit.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 µH
L2	nominal value	= 10,7 µH
L3	4,4 MHz chrominance input filter	= 10,7 µH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 µH
L5	delay equalization	= 66,1 µH
P1	amplitude of direct chroma singal	
R1 R2	field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short ($<$ 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

PAL DECODER

GENERAL DESCRIPTION

The TDA3565 PAL decoder contains all the functions required for PAL signal decoding and colour matrixing and is contained within an 18-pin package. The oscillator, a.c.c. detector and burst phase detector each have single-pin outputs and the coupling capacitor for the luminance input at pin 8 doubles as a storage capacitor for the black level clamping circuit. Black level clamping of the three colour channels is performed using feedback proportional to the red channel black level. This feedback (variable with the brightness control) controls the input level of the luminance amplifier and therefore the clamping levels of all three colour signal outputs.

QUICK REFERENCE DATA

Supply voltage	$V_p = V_{1-17}$	typ.	12 V
Supply current	$I_P = I_1$	typ.	85 mA
Luminance input signal (peak-to-peak value)	$V_{8-17(p-p)}$	typ.	0,45 V
Chrominance input signal (peak-to-peak value)	$V_{3-17(p-p)}$	typ.	550 mV
RGB output signal amplitudes (peak-to-peak value) at nominal luminance and contrast	$V_{10,11,12-17(p-p)}$	typ.	5 V
Contrast control range			−17 to +3 dB
Saturation control range		>	50 dB
A.C.C. control range		>	30 dB
Level at which RGB blanking is activated	V_{7-17}	typ.	1,5 V
Level at which burst gate/clamping pulse are separated	V_{7-17}	typ.	7 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

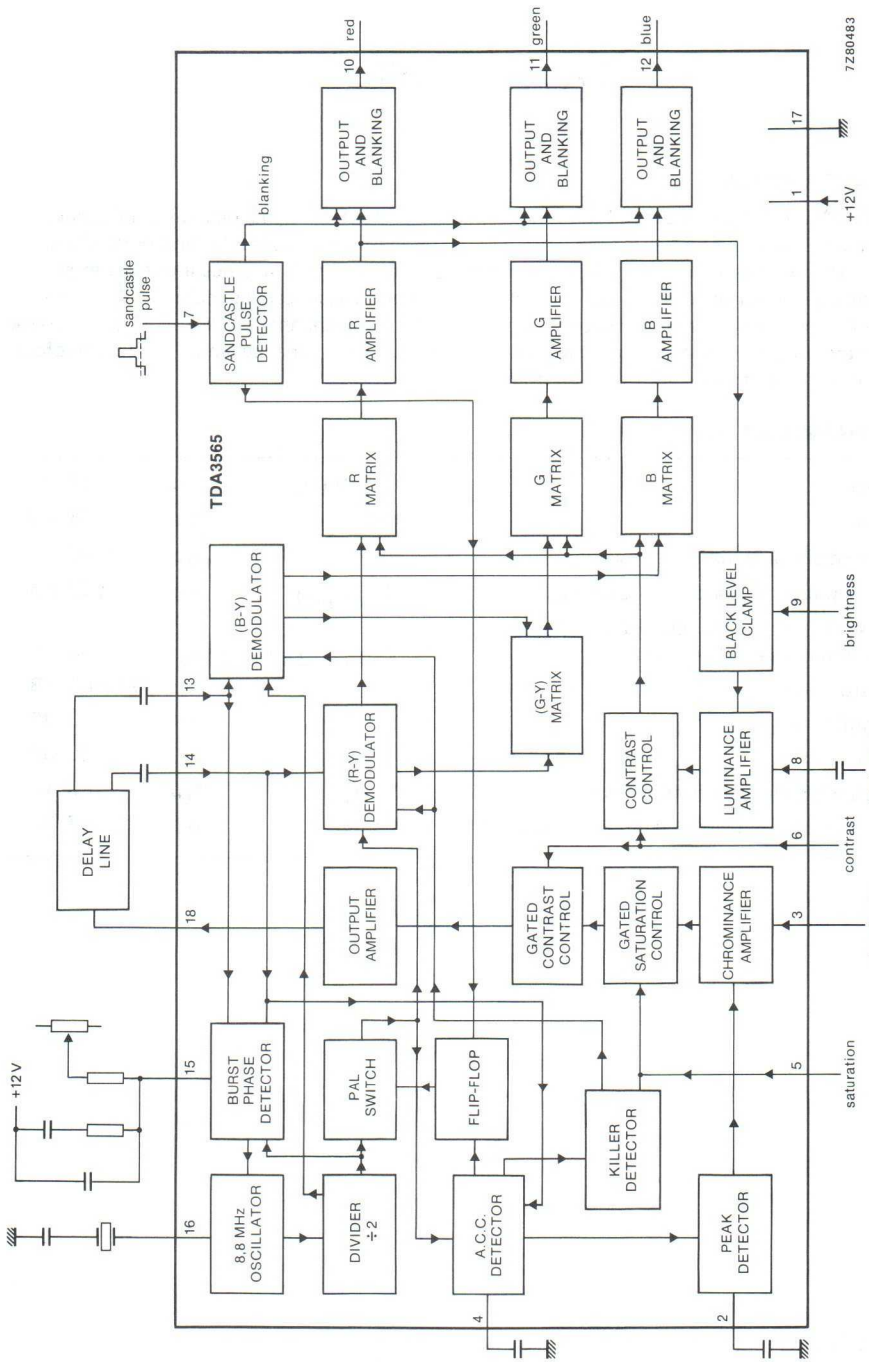


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	max.	50	K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	V_{1-17}	9,0	12,0	13,2	V
Supply current	I_1	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier					
Input signal amplitude (note 1) (peak-to-peak value)	$V_{8-17(p\text{-}p)}$	–	0,45	–	V
Input level before clipping occurs *	$V_{8-17(p\text{-}p)}$	–	–	0,7	V
Input current at $V_{8-17} = 2$ V; clamp not active	I_8	–	0,15	1,0	μA
Contrast control range (Fig. 2)		–	−17 to +3	–	dB
Input current when peak white limiter is active ($V_{6-17} = 2{,}5$ V)	I_8	–	5,5	–	mA
Input resistance $V_{6-17} > 6$ V	R_i	1,4	2,0	2,6	kΩ
Chrominance amplifier					
Input signal amplitude (note 2)	$V_{3-17(p\text{-}p)}$	55	550	1100	mV
Minimum burst signal amplitude within the control range (peak-peak)		30	–	–	mV
Input impedance	Z_{3-17}	–	8,0	–	kΩ
Input capacitance	C_{3-17}	–	4,0	6,0	pF
A.C.C. control range		30	–	–	dB
Change of burst signal at output over whole a.c.c. control range		–	–	1	dB
Amplification pin 3 to pin 18 at nominal contrast/saturation (note 3)		32	–	–	dB

* At nominal contrast and nominal brightness.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Chroma to burst ratio (note 3)		–	3,8	–	dB
Max. output voltage range (pin 18) $R_L = 2\ k\Omega$		4,0	4,5	–	V
Chrominance amplifier distortion at $V_{8\text{-}17(p\text{-}p)} = 2$ V (output) up to $V_{3\text{-}17(p\text{-}p)} = 1$ V (input)	$d_{8\text{-}3}$	–	3,0	5,0	%
Frequency response between 0 and 5 MHz		–	–	–2	dB
Saturation control range (Fig. 3)		50	–	–	dB
Saturation control input current at $V_{5\text{-}17} < 6$ V	I_5	–	1	20	μA
Input impedance for V_5 between 6 and 10 V	Z_i	1,4	2,0	2,6	kΩ
Input impedance when colour killer is active	Z_i	1,4	2,0	2,6	kΩ
Input impedance for $V_5 > 10$ V (adjustment procedure)	Z_i	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance over 10 dB of contrast control range		–	–	2	dB
Cross coupling between luminance and chrominance amplifiers (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Burst phase shift with respect to chrominance at nominal contrast/saturation (note 3)	$\Delta\varphi$	–	–	±5	deg
Chrominance amplifier output impedance	$Z_{18\text{-}17}$	–	25	–	Ω
Output current (pin 18)	I_{18}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of oscillator frequency	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency	TC_{osc}	–	2	3	Hz/K
Frequency deviation when supply voltage changes from 10 to 13,2 V	Δf_{osc}	–	200	300	Hz

parameter	symbol	min.	typ.	max.	unit
Input resistance	$R_{16\text{-}17}$	250	290	330	Ω
Input capacitance	$C_{16\text{-}17}$	–	–	10	pF
A.C.C. generation					
Voltage with nominal input signal	$V_{4\text{-}17}$	–	5,0	–	V
Voltage without chrominance input	$V_{4\text{-}17}$	–	2,5	–	V
Colour-off voltage	$V_{4\text{-}17}$	–	3,2	–	V
Colour-on voltage	$V_{4\text{-}17}$	–	3,5	–	V
Identification-on voltage	$V_{4\text{-}17}$	–	2,5	–	V
Pin 2 voltage at nominal input signal	$V_{2\text{-}17}$	–	5,1	–	V
Demodulator part					
Burst signal amplitude (peak-to-peak value) at pins 13 and 14 (note 6)	$V_{13\text{-}17(p\text{-}p)}$ $V_{14\text{-}17(p\text{-}p)}$	–	80	–	mV
Input impedance of pins 13 or 14 to pin 17	$Z_{13,\ 14\text{-}17}$	–	1,0	–	kΩ
Ratios of demodulated signals with equal signal inputs to pins 13 and 14 and no luminance input signal:					
(B-Y)/(R-Y)	$\frac{V_{12\text{-}17}}{V_{10\text{-}17}}$	–	1,78±10%	–	
(G-Y)/(R-Y) (no (B-Y) signal)	$\frac{V_{11\text{-}17}}{V_{10\text{-}17}}$	–	−0,51±10%	–	
(G-Y)/(B-Y) (no (R-Y) signal)	$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,19±10%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
Separation of colour difference channels		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output signal amplitudes (peak-to-peak value) at nominal luminance signal and contrast inputs (black-white) (note 3)	$V_{10\text{-}17(p\text{-}p)}$ $V_{11\text{-}17(p\text{-}p)}$ $V_{12\text{-}17(p\text{-}p)}$	4,5	5,0	5,5	V
Red channel output amplitude (peak-to-peak value) at nominal contrast/saturation (note 3) and no luminance signal to (R-Y)	$V_{10\text{-}17(p\text{-}p)}$	3,7	5,25	7,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Maximum peak white level (note 7)		9,0	9,3	9,6	V
Maximum output current	$I_{10,11,12}$	–	–	15	mA
Red channel black level output when brightness control $V_{9-17} = 2$ V	V_{10-17}	–	2,7	–	V
Difference between black levels in R, G and B outputs		–	–	600	mV
Black level shift with picture content		–	–	40	mV
Brightness control voltage range	V_{9-17}	see Fig. 3			
Brightness control input current at $V_{9-17} = 2$ V	I_9	–	–	–50	μA
Variation of black level with temperature		–	+0,35	1,0	mV/K
Variation of black level with contrast control		–	10	100	mV
Relative spread between the three channel outputs		–	–	10	%
Relative variation in black level between the three channels during normal variations of contrast and supply voltage		–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		–	0	20	mV
Blanking level at the three channel outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channel outputs		–	0	–	mV
Differential drift of blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black levels with variation of supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz component in output signals (peak-to-peak value)		–	25	50	mV
Residual 8,8 MHz and higher harmonic components in output signals (peak-to-peak value)		–	25	50	mV
Output impedance	$Z_{10,11,12-17}$	–	50	–	Ω
Frequency response of total luminance/ RGB amplifier circuits for 0 to 5 MHz		–	–	–3	dB

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector					
Level at which RGB blanking is activated	V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate and clamping pulse are separated	V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		–	0,4	–	μs
Input current at:					
V_{7-17} = 0 to 1 V	I_7	–	–	−1	mA
V_{7-17} = 1 to 8,5 V	I_7	–	20	40	μA
V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync pulse, amplitude includes sync pulse amplitude.
2. The signal indicated is for a colour bar with 75% saturation, so the chroma burst ratio of 2,2 : 1.
3. Nominal contrast is defined as (maximum contrast −3 dB) and nominal saturation is (maximum saturation −12 dB).
4. Cross coupling is measured under the following condition; input signals nominal and contrast/saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded the amplitude of the output signal is reduced via a discharge of the capacitor at pin 6 (contrast control). The discharge current is 5,5 mA.

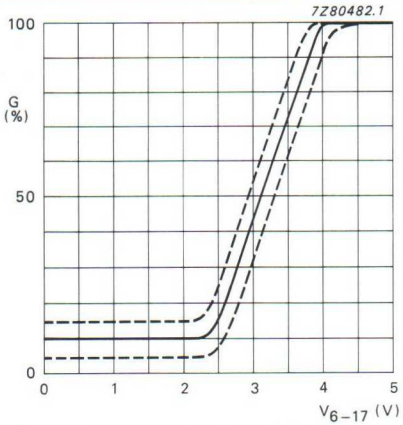


Fig. 2 Luminance contrast control voltage range.

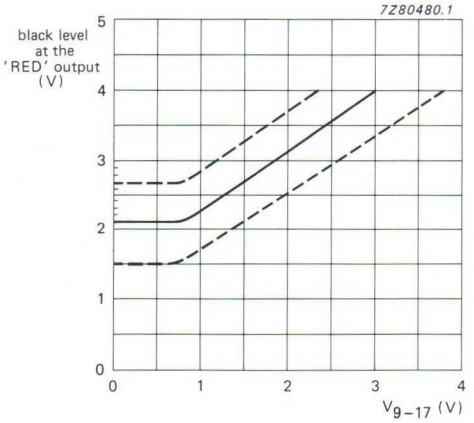


Fig. 3 Brightness control voltage range.

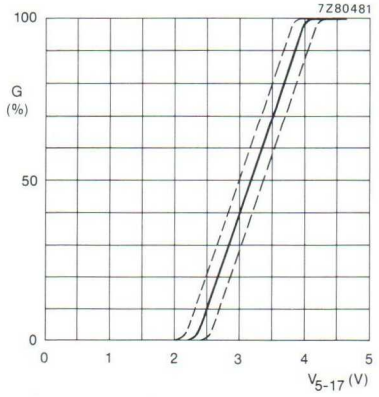


Fig. 4 Saturation control voltage range.

APPLICATION INFORMATION

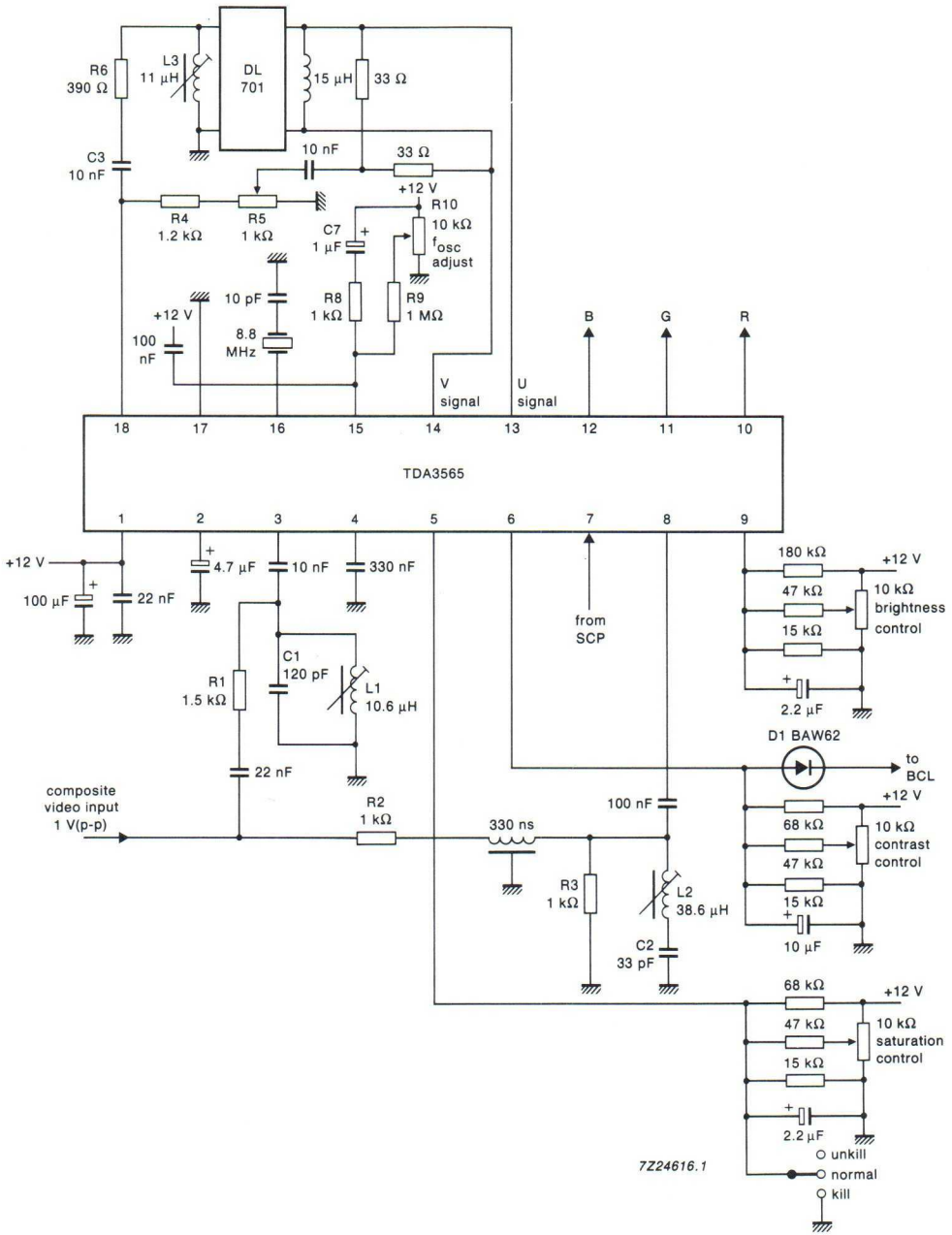


Fig. 5 Application diagram

PAL/NTSC DECODER

GENERAL DESCRIPTION

The TDA3566 is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	80 mA
Luminance amplifier (pin 8)			
Input voltage (peak-to-peak value)	$V_{8-27(p-p)}$	typ.	450 mV
Contrast control range		typ.	20 dB
Chrominance amplifier (pin 4)			
Input voltage range (peak-to-peak value)	$V_{4-27(p-p)}$	40 to	1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13, 15, 17-27(p-p)}$	typ.	4 V
Data insertion			
Input signals (peak-to-peak value)	$V_{12, 14, 16-27(p-p)}$	typ.	1 V
Data blanking (pin 9)			
Input voltage for data insertion	V_{9-27}	min.	0,9 V
Sandcastle input (pin 7)			
Blanking input voltage	V_{7-27}	typ.	1,5 V
Burst gating and clamping input voltage	V_{7-27}	typ.	7 V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

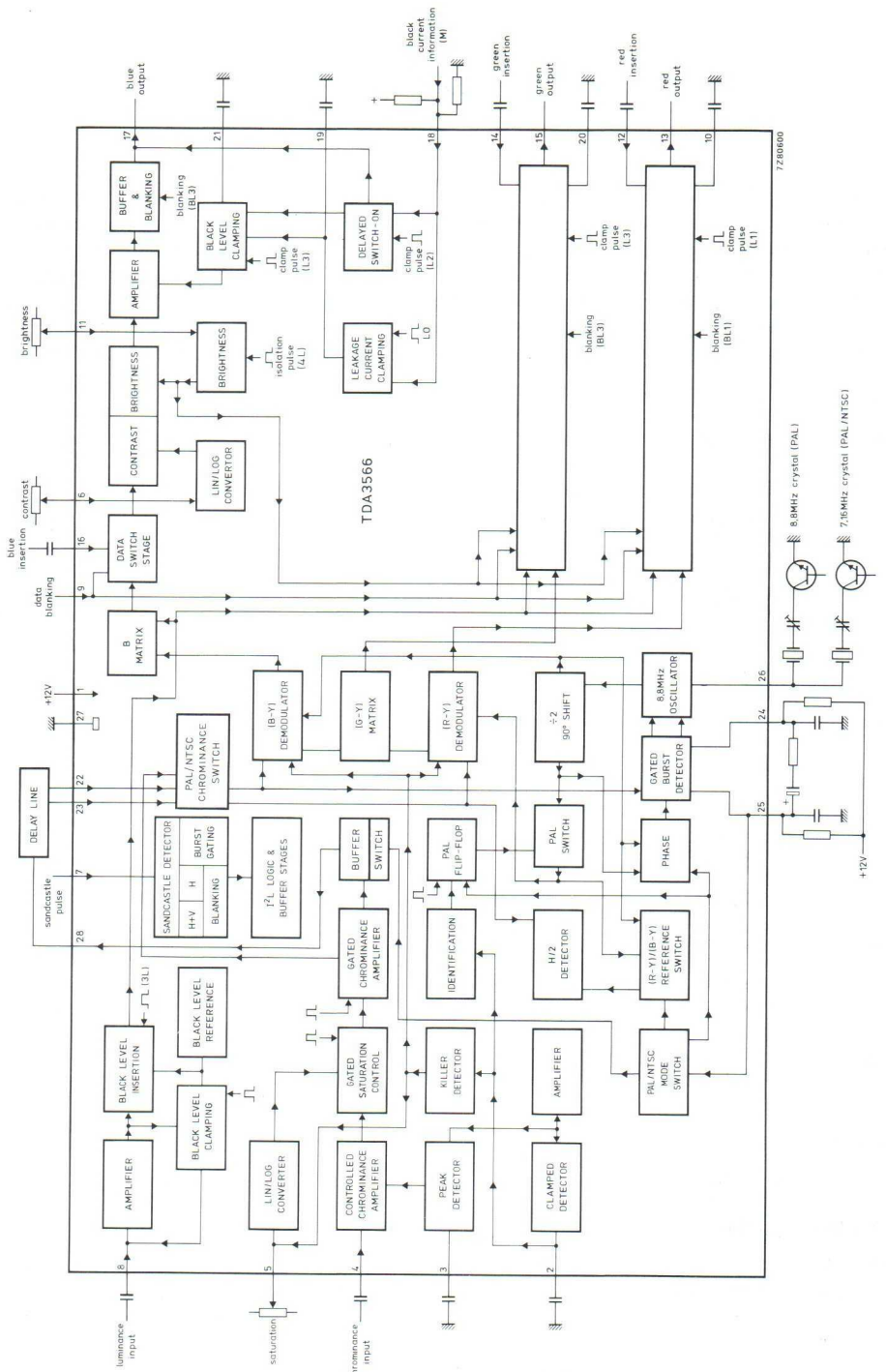


Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC-application has largely been simplified. In the case of NTSC the chroma signal is now internally coupled to the demodulators, ACC and phase detectors. The chroma output signal (pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566.
  Furthermore there is no difference between the amplitude of the colour output signals in the PAL or NTSC mode. The PAL/NTSC-switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behaviour of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the pins 10, 20 and 21 can be reduced to 100 nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10 pF.

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. Form the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.
In the case of NTSC the chroma signal is internally coupled to the demodulators, ACC and phase detector.

FUNCTIONAL DESCRIPTION (continued)

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.
The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.
Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3566 is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)
Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 V and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is + 3 dB to −17 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).
During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.
The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

DEVELOPMENT DATA

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs.
To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.
The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.
The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.
Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.
To prevent parasitic oscillations on the third overtone of the crystal the optimal tuning capacitance should be 10 pF.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to	+ 150 °C
Operating ambient temperature range	T_{amb}	−25 to	+ 70 °C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	40 K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10,8	12	13,2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0,95	1,3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8-27(p-p)}$	–	0,45	0,63	V
Input level before clipping	V_{8-27}	–	–	1.4	V
Input current	I_8	–	0,1	1	μA
Contrast control range (see Fig. 2)		–15	–	+ 5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4-27(p-p)}$	40	390	1100	mV
Input impedance (pin 4)	$\lvert Z_{4-27} \rvert$	–	10	–	kΩ
Input capacitance	C_{4-27}	–	–	6,5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range	ΔV	–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)	G	34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	$V_{28-27(p-p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	α_{28-4}	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA
Reference part					
Phase-locked-loop catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\varphi$	–	–	5	deg
Oscillator					
temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–2	–3	Hz/K
frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	100	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	280	400	520	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2)					
control voltage at nominal input signal	$V_{2\text{-}27}$	–	4,5	–	V
control voltage without chrominance input	$V_{2\text{-}27}$	–	2	–	V
colour-off voltage	$V_{2\text{-}27}$	–	2,8	–	V
colour-on voltage	$V_{2\text{-}27}$	–	3	–	V
identification-on voltage	$V_{2\text{-}27}$	–	1,7	–	V
change in burst amplitude with temperature		–	0,1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5,1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	68	80	95	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	0,7	1	1,3	kΩ
Ratio of demodulated signals (note 8)					
(B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1,78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	–0,51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	–0,19 ± 10%	–	

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Demodulator part (continued)					
Frequency response between 0 and 1 MHz	α_{17}	–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signals	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) signal and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17\text{-}27(p\text{-}p)}$	3,5	4	4,5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}27(p\text{-}p)}$	–	4,2	–	V
Maximum peak-white level	$V_{13,15,17\ (m)}$	9,7	10	10,3	V
Available output current (pins 13, 15 17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17\text{-}27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)	ΔV	–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; $V_{11\text{-}17}$ = 2 V		–	–	± 2	V
Black level shift with vision contents	ΔV	–	–	40	mV
Brightness control voltage range		see Fig. 4			
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)*	ΔV	–	0	20	mV
Differential black-level drift over a temperature range of 40 °C	ΔV	–	0	20	mV
Blanking level at the RGB outputs	V_{bl}	–	0,95	1,1	V

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Difference in blanking level of the three channels	V_{bl}	–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C	V_{bl}	–	0	10	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	0,9	1	1,1	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0,5	dB
Output signal during the clamp pulse (3L) after switch-on	V_O	7,5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	50	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17-27} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 9 MHz	α	–	−1	−3	dB
Current source of output stage	I_O	2	3	–	mA
Difference of black level at the three outputs at nominal brightness*	ΔV	–	–	10	mV
Tracking of brightness control		–	–	2	%
Signal insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for and RGB output voltage of 3.5 V (peak-to-peak) at nominal contrast	$V_{12,14,16-27(p-p)}$	0,9	1	1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	50	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA

* With respect to the measuring pulses.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	$R_{9\text{-}27}$	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V		46	–	–	dB
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	$V_{7\text{-}27}$	1	1,5	2	V
Level at which the horizontal pulses are separated	$V_{7\text{-}27}$	3	3,5	4	V
Level at which burst gating and clamping pulse are separated	$V_{7\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,6	–	μs
Input current					
at $V_{7\text{-}27}$ = 0 to 1 V	$-I_7$	–	–	1	mA
at $V_{7\text{-}27}$ = 1 to 8,5 V	I_7	–	–	50	μA
at $V_{7\text{-}27}$ = 8,5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
Bias voltage (d.c.)	$V_{18\text{-}27}$	3,5	5	7,0	V
Difference between input voltage for 'black' current and leakage current	ΔV	0,35	0,5	0,65	V
Input current during 'black' current	I_{18}	–	–	1	μA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	$V_{18\text{-}27}$	8,5	9	9,5	V
Switching threshold for 'black' current control ON	$V_{18\text{-}27}$	7,6	8	8,4	V
Input resistance during scan	$R_{18\text{-}27}$	1	1,5	2	kΩ
Input current during scan at pins 10, 20 and 21 (d.c.)	$I_{10,\ 20,\ 21}$	–	–	tbf	nA
Maximum charge/discharge current during measuring time		–	1	–	nA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	$V_{24\text{-}25}$	–	8,8	9,2	V
Average output current (note 12)	$I_{24 + 25(AV)}$	75	90	105	μA
Hue control		see Fig. 5			

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

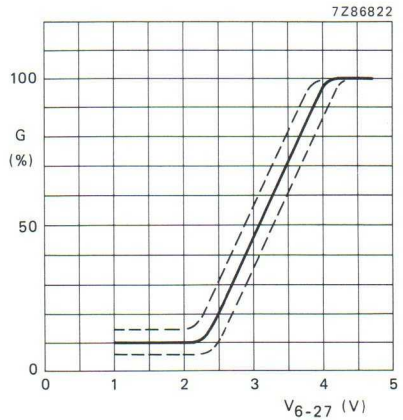


Fig. 2 Contrast control voltage range.

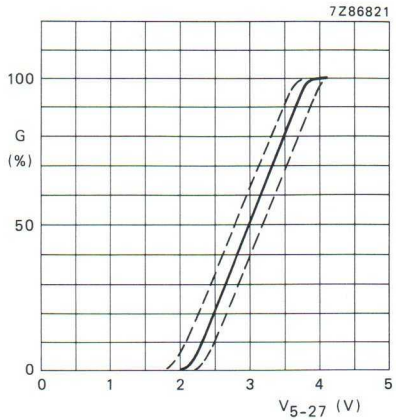


Fig. 3 Saturation control voltage range.

DEVELOPMENT DATA

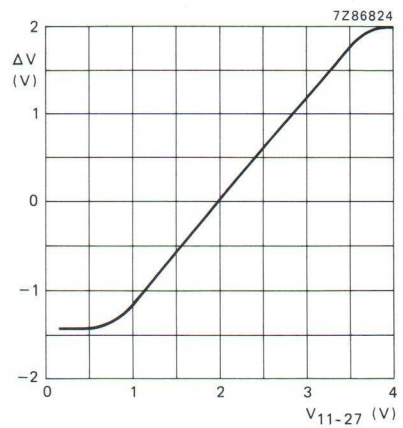


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

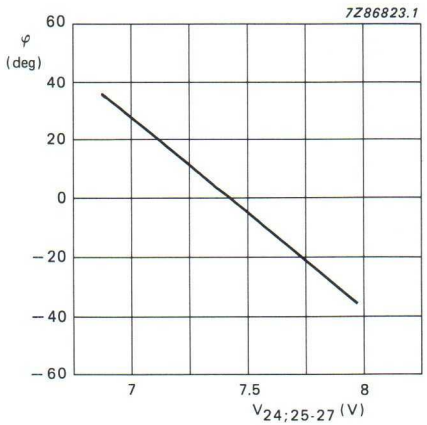


Fig. 5 Hue control voltage range.

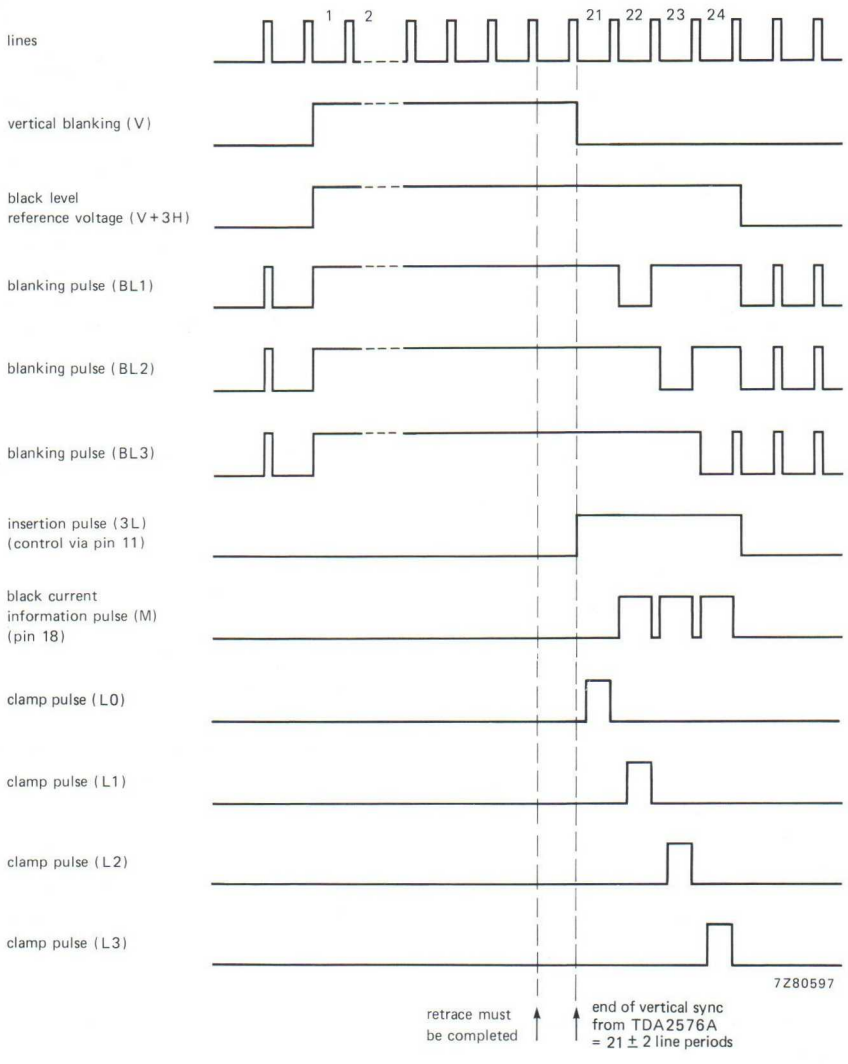


Fig. 6 Timing diagram for black-current stabilizing.

DEVELOPMENT DATA

APPLICATION INFORMATION

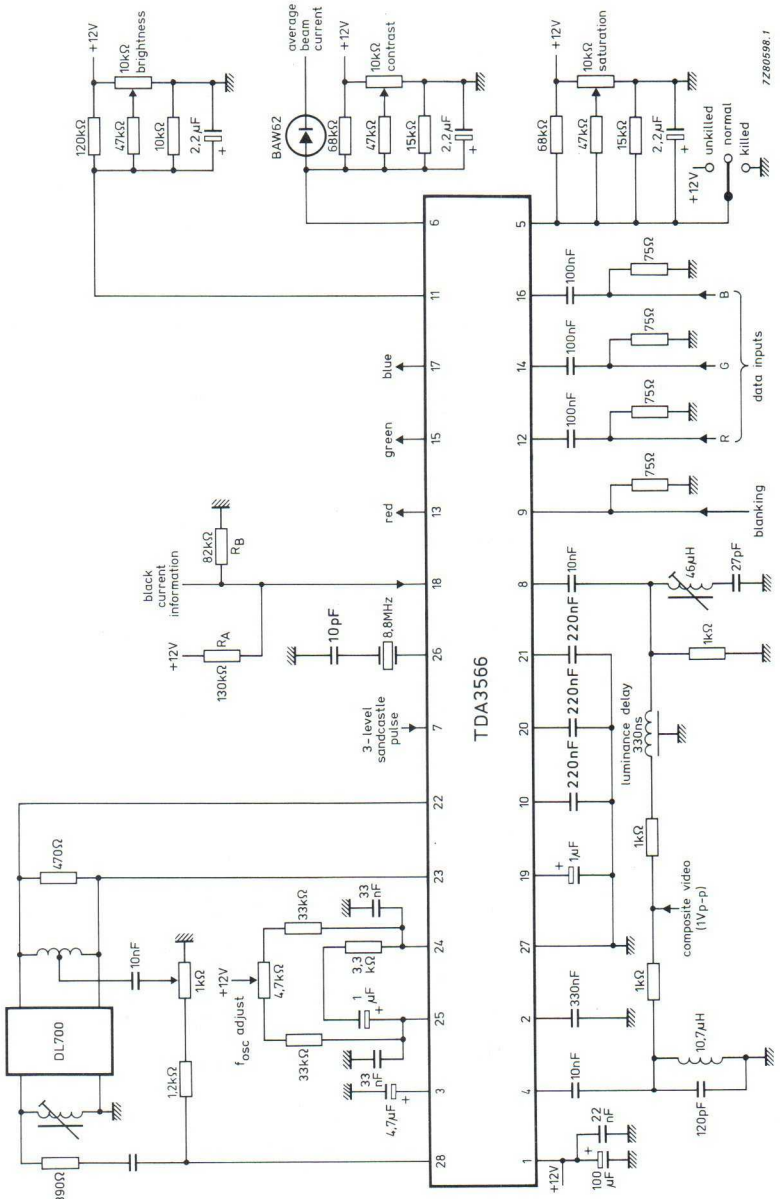


Fig. 7 Application diagram showing the TDA3566 for a PAL decoder.

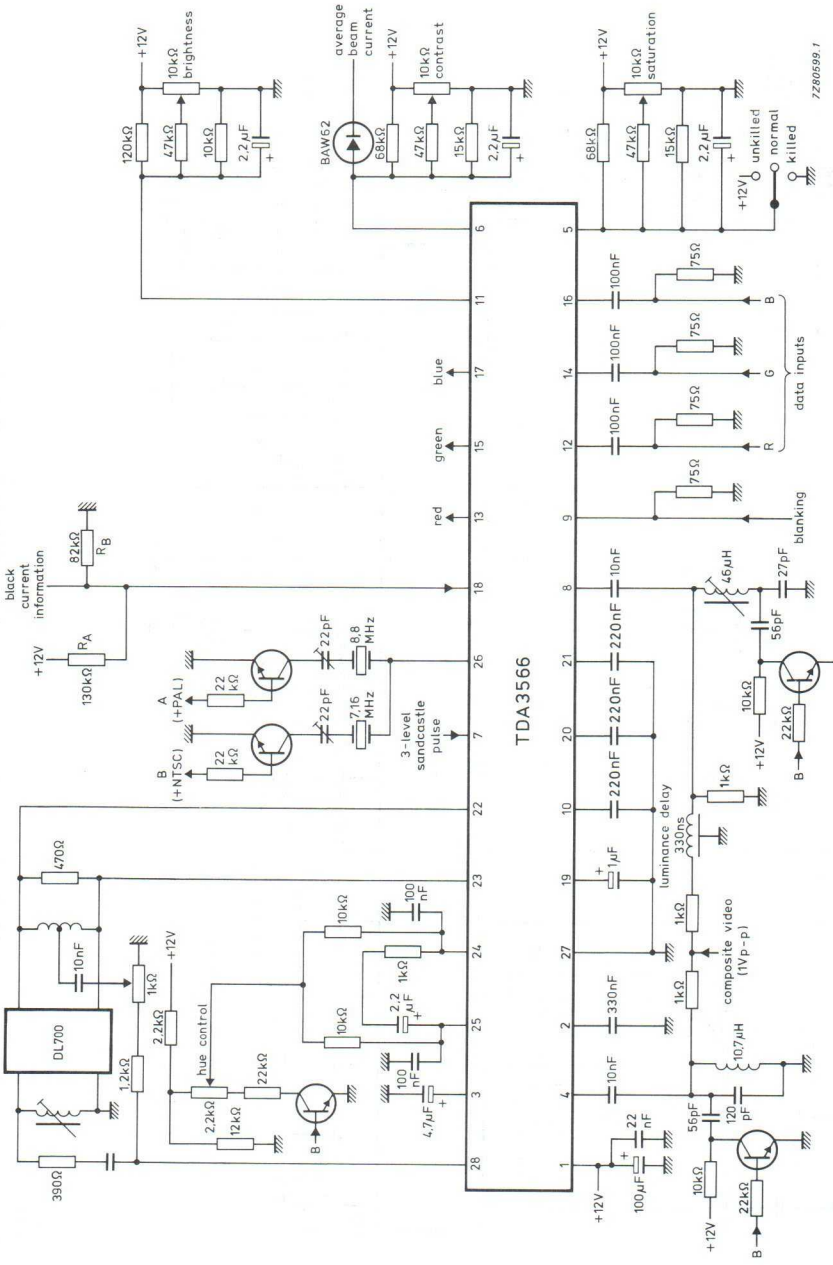


Fig. 8 Application diagram showing the TDA3566 for a PAL/NTSC decoder.

DEVELOPMENT DATA

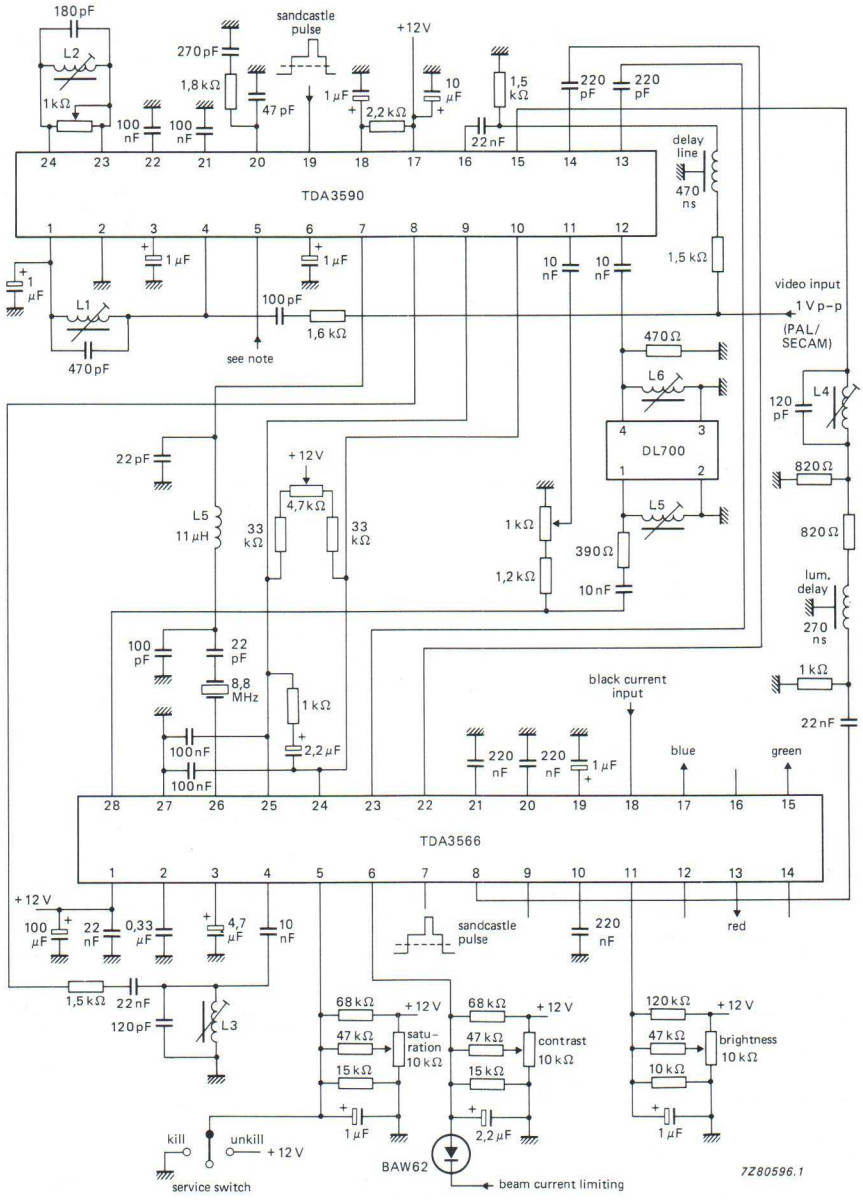


Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3566.

Note to pin 5 TDA3590:

$V_{5-2} < 1$ V; horizontal identification and black level clamping.
$V_{5-2} > 11$ V; vertical identification and artificial black level.
V_{5-2} = 5 to 7 V; horizontal identification and artificial black level.

PAL/NTSC decoder TDA3566A

FEATURES

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control.

APPLICATIONS

- Teletext/broadcast antiope
- Channel number display.

GENERAL DESCRIPTION

The TDA3566A is a decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals.

Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analog and digital, which can be used for text display systems.

QUICK REFERENCE DATA

All voltages referenced to ground.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage (pin 1)	–	12	–	V
I_P	supply current (pin 1)	–	90	–	mA
Luminance amplifier (pin 8)					
$V_{8(p-p)}$	input voltage (peak-to-peak value)	–	450	–	mV
CON	contrast control	–	16.5	–	dB
Chrominance amplifier (pin 4)					
$V_{4(p-p)}$	input voltage (peak-to-peak value)	40	–	1100	mV
SAT	saturation control	–	50	–	dB
RGB matrix and amplifiers					
$V_{13,\ 15,\ 17(p-p)}$	output voltage at nominal luminance and contrast (peak-to-peak value)	–	3.8	–	V
Data insertion					
$V_{12,\ 14,\ 16(p-p)}$	input signals (peak-to-peak value)	–	1	–	V
Data blanking (pin 9)					
V_9	input voltage for data insertion	0.9	–	–	V
Sandcastle input (pin 7)					
V_7	blanking input voltage	–	1.5	–	V
V_7	burst gating and clamping input voltage	–	7	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3566A	28	DIL	plastic	SOT117

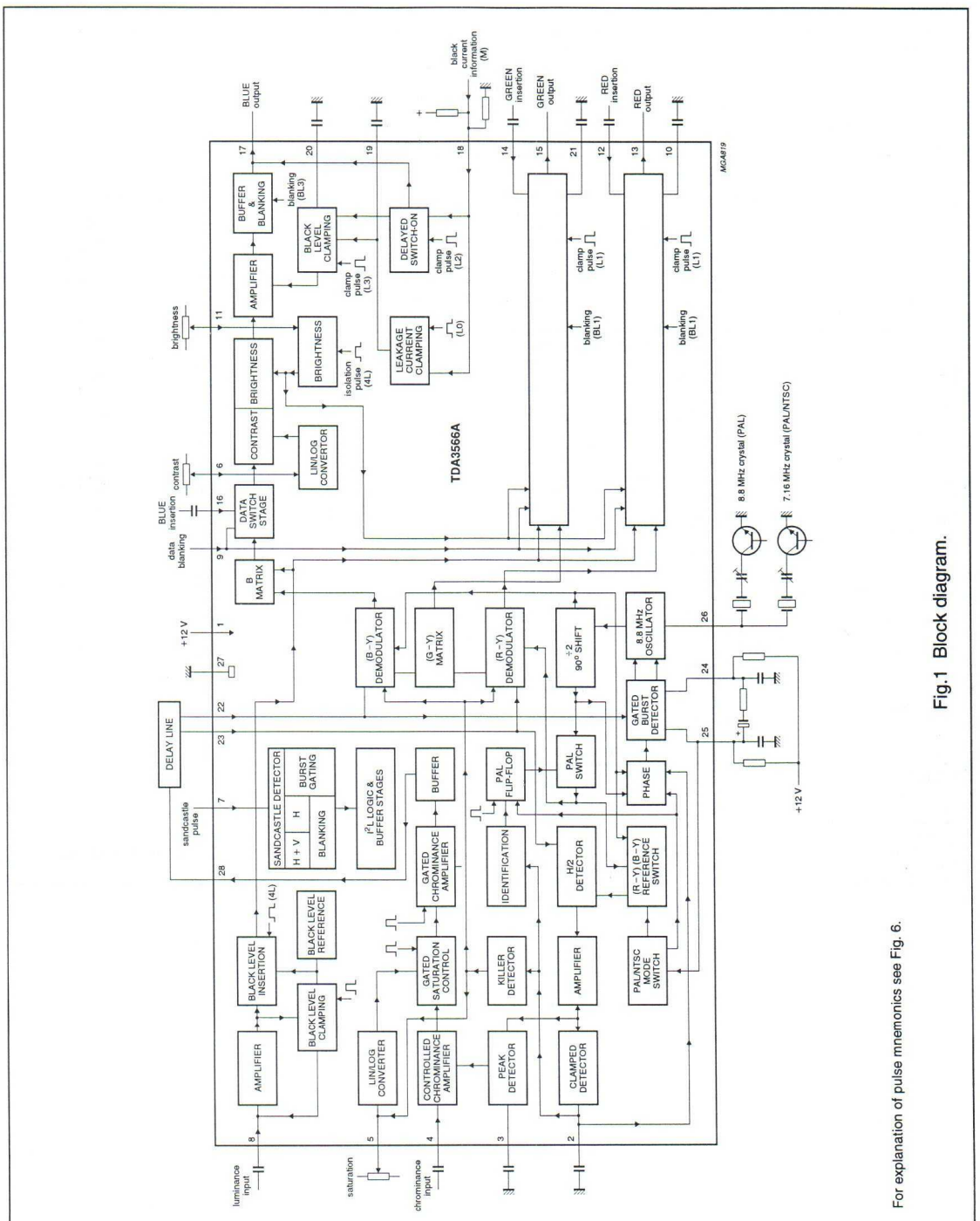


Fig.1 Block diagram.

For explanation of pulse mnemonics see Fig. 6.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
IDDET	2	identification detection level
ACCDET	3	Automatic Chrominance Control detection level
CHR_{IN}	4	chrominance control input
SAT	5	saturation control input
CON	6	contrast control input
SC	7	sandcastle input
LUM	8	luminance control input
DBL	9	data blanking input
BCL_R	10	black clamp level for RED output
BRI	11	brightness input
R_{IN}	12	RED input
R_{OUT}	13	RED output
G_{IN}	14	GREEN input
G_{OUT}	15	GREEN output
B_{IN}	16	BLUE input
B_{OUT}	17	BLUE output
BLA	18	black current input
BCL	19	black clamp level; referenced to black level
BCL_B	20	black clamp level for BLUE output
BCL_G	21	black clamp level for GREEN output
B–Y	22	demodulator input (BLUE)
R–Y	23	demodulator input (RED)
RCEXT	24	gated burst detector load network
RCEXT	25	gated burst detector load network
OSC	26	oscillator frequency input
GND	27	ground
CHR_{OUT}	28	chrominance signal output

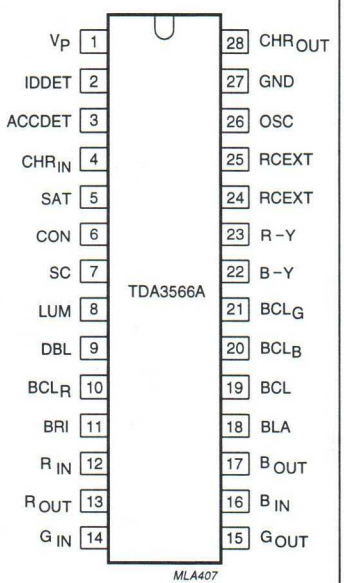


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3566A is a further development of the TDA3562A. It has the same pinning and nearly the same application. The differences between the TDA3562A and the TDA3566A are as follows:

- The NTSC-application has largely been simplified. In the event of NTSC the chrominance signal is now internally coupled to the demodulators, automatic chrominance control (ACC) and phase detectors. The chrominance output signal (pin 28) is thus suppressed. It follows that the external switches and filters which are required for the TDA3562A are not required for the TDA3566A. There is no difference between the amplitudes of the colour output signals in the PAL or NTSC mode.
- The clamp capacitor at pins 10, 20 and 21 in the black-level stabilization loop can be reduced to 100 nF provided the stability of the loop is maintained. Loop stability depends on complete application. The clamp capacitors receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. Consequently the optimum tuning capacitance must be reduced to 10 pF.
- The hue control has been improved (linear).

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the IF amplifier and the decoder.

The input signal is AC coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed DC level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit.

This black level reference voltage is controlled via pin11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be AC coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak.

The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1.1 V peak-to-peak, otherwise clipping of the input signal will occur.

From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linearly controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB.

The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst-to-chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at –6 dB.

The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector. In the event of NTSC the chrominance signal is internally coupled to the demodulators, ACC and phase detectors.

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R–Y) and (B–Y) signals are added to provide the composite burst signal again.

This composite signal is compared with the oscillator signal divided-by-2 (R–Y) reference signal. The control voltage is available at pins 24 and 25, and is also applied to the 8.8 MHz oscillator. The 4.4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B–Y) and (R–Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R–Y) reference signal coming from the PAL switch, is compared to the vertical signal (R–Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst.

When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the ACC.

To avoid 'blooming-up' of the picture under weak input signal conditions the ACC voltage is generated by peak detection of the H/2 detector output signal. The killer and identification circuits receive their information from a gated output signal of H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression.

The time constant of the saturation control (pin 5) provides a delayed switch-on after killing. Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig.8).

With this application the trimmer capacitor in series with the 8.8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R–Y) and (B–Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8.8 MHz divider circuit. The (R–Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G–Y) matrix to provide the (G–Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V.

To ensure reliable application the phase detector load resistors are external. When the TDA3566A is used only for PAL these two 33 kΩ resistors must be connected to +12 V (see Fig.8).

For PAL/NTSC application the value of each resistor must be reduced to 20 kΩ (with a tolerance of 1%) and connected to the slider of a potentiometer (see Fig.9). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit tot the NTSC mode.

The position of the PAL flip-flop ensures that the correct phase of the (R–Y) reference signal is supplied to the (R–Y) demodulator.

The drive to the H/2 detector is now provided by the (B–Y) reference signal. In the PAL mode it is driven by the (R–Y) reference signal. Hue control is realized by changing the phase of the reference drive to the burst phase detector.

This is achieved by varying the voltage at pins 24 and 25 between 7.0 V and 8.5 V, nominal position 7.65 V. The hue control characteristic is shown in Fig.6.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.

The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage.

The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is +5 dB to −11.5 dB nominal. The relationship between the control voltage and the gain is linear (see Fig.3).

During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control.

The brightness control range is 1 V to 3.6 V. While this offset level is present, the black-current input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current.

The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output.

The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10.6 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be approximately 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion.
A 1 V peak-to-peak input signal provides a 3.8 V peak-to-peak output signal.

To avoid the black-level of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore AC coupling is required for the data inputs.

To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω. The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0.9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on.

To avoid coloured edges, the data blanking switching time is short. The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.

Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1.5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of +1 V is available at the output. To prevent parasitic oscillations on the third overtone of the crystal the optimum tuning capacitance should be 10 pF.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–	13.2	V
P_{tot}	total power dissipation	–	1700	mW
T_{amb}	operating ambient temperature	−25	+70	°C
T_{stg}	storage temperature	−25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to pin 27; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		10.8	12.0	13.2	V
I_P	supply current		–	90	120	mA
P_{tot}	total power dissipation		–	1.1	1.6	W
Luminance input (pin 8)						
$V_{8(p-p)}$	input voltage (peak-to-peak value)	note 1	–	0.45	0.63	V
V_8	input voltage level before clipping occurs in the input stage		–	–	1.4	V
I_8	input current		–	0.1	1	µA
	contrast control range	see Fig.3	–11.5	–	+5	dB
I_6	input current contrast control		–	–	15	µA
Chrominance amplifier						
$V_{4(p-p)}$	input signal amplitude (peak-to-peak value)	note 2	40	390	1100	mV
$\|Z_4\|$	input impedance		–	10	–	kΩ
C_4	input capacitance		–	–	6.5	pF
	ACC control range		30	–	–	dB
ΔV	change of the burst signal at the output control range	100 mV to 1 V (p-p)	–	–	1	dB
G	amplification at nominal saturation (pin 4 to pin 28)	note 3	34	–	–	dB
	chrominance to burst ratio at nominal saturation		–	7	–	dB
$V_{28(p-p)}$	maximum output voltage range (peak-to-peak value)	R_L = 2 kΩ	4	5	–	V
d	distortion of chrominance amplifier at 2 V (p-p) output signal up to an input signal of 1 V (p-p)		–	–	5	%
α_{28-4}	frequency response between 0 and 5 MHz		–	–	–2	dB
	saturation control range	see Fig.4	50	–	–	dB
I_5	input current saturation control		–	–	20	µA
	cross-coupling between luminance and chrominance amplifier	note 4	–	–	–46	dB
S/N	signal-to-noise ratio at nominal input signal	note 5	56	–	–	dB
$\Delta\varphi$	phase shift burst with respect to chrominance at nominal saturation		–	–	±5	deg
$\|Z_{28}\|$	output impedance of chrominance amplifier		–	10	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{28}	output current		–	–	15	mA
Reference part						
Δf	phase-locked loop catching range	note 6	500	–	–	Hz
$\Delta\varphi$	phase shift for 400 Hz deviation of the oscillator frequency	note 6	–	–	5	deg
TC_{osc}	oscillator temperature coefficient with respect to oscillator frequency	note 6	–	–2	–3	Hz/K
Δf_{osc}	frequency deviation when supply voltage increases from 10 to 13.2 V	note 6	–	40	100	Hz
R_{26}	input resistance		280	400	520	Ω
C_{26}	input capacitance		–	–	10	pF
ACC generation (pin 2; note)7						
V_2	control voltage at nominal input signal		–	4.5	–	V
V_2	control voltage without chrominance input		–	2	–	V
ΔV_2	colour-on/off voltage		175	300	425	mV
V_2	colour-on voltage		3.1	3.5	3.9	V
ΔV_2	colour-on identification voltage		1.2	1.5	1.8	V
	change in burst amplitude with temperature		–	0.1	0.25	%/K
V_3	voltage at pin 3 at nominal input signal		–	4.7	–	V
Demodulator part						
$V_{23(p-p)}$	amplitude of burst signal (peak-to-peak value) between pins 23 and 27	note 8	45	63	81	mV
$\lvert Z_{22,\,23}\rvert$	input impedance between pins 22 or 23 and 27		0.7	1.0	1.3	kΩ
RATIO OF DEMODULATED SIGNALS FOR EQUIVALENT INPUT SIGNALS AT PINS 22 AND 23						
$\frac{V_{17}}{V_{13}}$	(B–Y)/(R–Y)		–	1.78 ± 10%	–	
$\frac{V_{15}}{V_{13}}$	(G–Y)/(R–Y)	no (B–Y) signal	–	–0.51 ± 10%	–	
$\frac{V_{15}}{V_{17}}$	(G–Y)/(B–Y)	no (R–Y) signal	–	–0.19 ± 25%	–	
α_{17}	frequency response between 0 and 1 MHz		–	–	–3	dB
α_{cr}	cross-talk between colour difference signals		40	–	–	dB
$\Delta\varphi$	phase difference between (R–Y) and (B–Y) reference signals		85	90	95	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta\varphi_{tot}$	total phase difference between chrominance input signals and demodulator output signals		–	–	8	deg
RGB matrix and amplifiers						
$V_{13, 15, 17(p-p)}$	output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white)	note 3	3.3	3.8	4.3	V
$V_{13(p-p)}$	output signal amplitude of the 'RED' channel (peak-to-peak value) at nominal contrast/saturation and no luminance signal to the input (R–Y signal)		–	3.7	–	V
$V_{13, 15, 17(m)}$	maximum peak-white level		9.4	10.0	10.6	V
$I_{13, 15, 17}$	available output current		10	–	–	mA
$\Delta V_{13, 15, 17}$	difference between black level and measuring level at the output for a brightness control voltage of 2 V	note 9	–	0	–	V
ΔV	difference in black level between the three channels for equal drive conditions for the three gains	note 10	–	–	100	mV
	control range of black-current stabilization at V_{black} = 3 V; V_{11} = 2 V		–	–	±2	V
ΔV	black level shift with picture content		–	–	40	mV
	brightness control voltage range	see Fig.5	–	–	–	V
I_{11}	brightness control input current		–	–	5	µA
	slope of brightness control curve		–	1.3	–	V/V
	tracking of contrast control between the three channels over a control range at 10 dB		–	–	0.5	dB
V_o	output voltage during test pulse after switch-on		6.5	7.3	–	V
$\frac{\Delta V}{\Delta T}$	variation of black level with temperature		–	0	–	mV/K
ΔV	variation of black level with contrast (+5 to –10 dB)	note 11	–	–	100	mV
	relative spread between the three output signals		–	–	10	%
ΔV	relative black level variation between the three channels during variation of contrast, brightness and supply voltage	note 11	–	0 ± 10%	20 ± 10%	mV
V_{blk}	blanking level at the RGB outputs		–	0.85	1.1	V
ΔV_{blk}	difference in blanking level of the three channels		–	0	10	mV
dV_{blk}	differential drift of the blanking levels	ΔT = 40 °C	–	0	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_{Pl}}{\Delta V_{Pl}}$	tracking of output black level with supply voltage		0.9	1.0	1.1	
S/N	signal-to-noise ratio of output signals	note 5	62	–	–	dB
$V_{R(p-p)}$	residual 4.4 MHz signal at RGB outputs (peak-to-peak value)		–	–	100	mV
$V_{R(p-p)}$	residual 8.8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	–	150	mV
$\lvert Z_o \rvert$	output impedance (pins 13, 15 and 17)		–	100	–	Ω
α_{tot}	frequency response of total luminance and RGB amplifier circuits for f = 0 MHz and 5 MHz		–	–1	–3	dB
I_o	current source of output stage		2	3	–	mA
ΔV	difference of black level at the three outputs at nominal brightness	note 11	–	–	10	mV
	tracking of brightness control		–	–	2	%
Data insertion						
$V_{12, 14, 16(p-p)}$	input signals (peak-to-peak value) for an RGB output voltage of 3.8 V (peak-to-peak) at nominal contrast	note 4	0.9	1.0	1.1	V
ΔV	difference between the black level of the RGB signals and the black level of the inserted signals at the outputs at nominal contrast	note 12	–	–	170	mV
t_r	output rise time		–	50	80	ns
t_d	difference delay for the three channels		–	0	40	ns
$I_{12, 14, 16}$	input current		–	–	10	µA
Data blanking						
V_9	input voltage for no data insertion		–	–	0.3	V
V_9	input voltage for data insertion		0.9	–	–	V
V_9	maximum input pulse voltage		–	–	3	V
t_d	delay of data blanking		–	–	20	ns
R_9	input resistance		7	10	13	kΩ
	suppression of the internal RGB signals when $V_9 > 0.9$ V		46	–	–	dB
	suppression of external RGB signals when $V_9 < 0.3$ V		46	–	–	dB
Sandcastle input (note 13)						
V_7	level at which the RGB blanking is activated		1.0	1.5	2.0	V
V_7	level at which the horizontal pulses are separated		3.0	3.5	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_7	level at which the burst gate and clamping pulse are separated		6.5	7.0	7.5	V
t_d	delay between black level clamping and burst gating pulse		–	0.6	–	µs
I_i	input current	V_i = 0 to 1 V	–	–	–1	mA
		V_i = 1 to 8 V	–	–	50	µA
		V_i = 8 to 12 V	–	–	2	mA
Black current stabilization						
V_{18}	DC bias voltage		3.5	5.0	7.0	V
ΔV	difference between input voltage for black current and leakage current		0.35	0.5	0.65	V
I_{18}	input current during black current		–	–	1	µA
I_{18}	input current during scan		–	–	10	mA
V_{18}	internal limiting at pin 18		8.5	9.0	9.5	V
V_{18}	switching threshold for black current control on		7.6	8.0	8.4	V
R_{18}	input resistance during scan		1.0	1.5	2.0	kΩ
$I_{10, 20, 21}$	DC input current during scan at pins 10, 20 and 21		–	–	30	nA
	maximum charge or discharge current during measuring time (pins 10, 20 and 21)		–	1	–	mA
	difference in drift of the blank level	note 11; ΔT = 40 °C		0	20	mV
NTSC						
V_{24-25}	level at which the PAL/NTSC switch is activated (pins 24 and 25)		–	8.8	9.2	V
$I_{24+25\ (AV)}$	average output current (pin 24 plus pin 25)	note 14	62	82.5	103	µA
HUE	hue control	see Fig.6	–	–	–	

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal with 75% colour bar, so the chrominance-to-burst ratio is 2.2 : 1.
3. Nominal contrast is specified as the maximum contrast –5 dB and nominal saturation as maximum –6 dB. This figure is valid in the PAL-condition. In the NTSC-condition no output signal is available at pin 28.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referenced to the 4.4 MHz carrier frequency. All oscillator specifications have been measured with the Philips crystal 4322 143 ... or 4322 144 ... series.
7. The change in burst with V_P is proportional.

8. These signal amplitudes are determined by the ACC circuit of the reference part.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) however, in that condition the amplitude of the available output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. With respect to the measuring pulse.
12. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 µs (sandcastle pulse). For a lower impedance the difference will be lower.
13. For correct operating of the black level stabilization loop, the leading and trailing edges of the sandcastle pulse (measured between 1.5 V and 3.5 V) must be within 200 ns and 600 ns respectively.
14. The voltage at pins 24 and 25 can be changed by connecting the load resistors (20 kΩ, 1%, in this condition) to the slider bar of the hue control potentiometer (see Fig.6). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 µs typical.

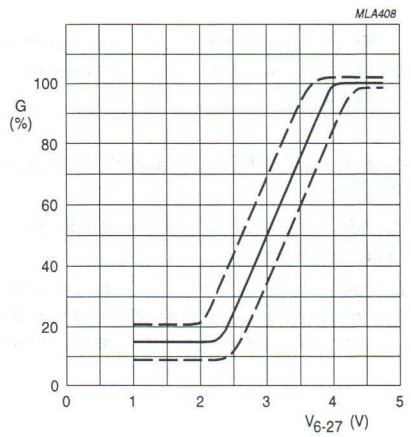


Fig.3 Contrast control voltage range.

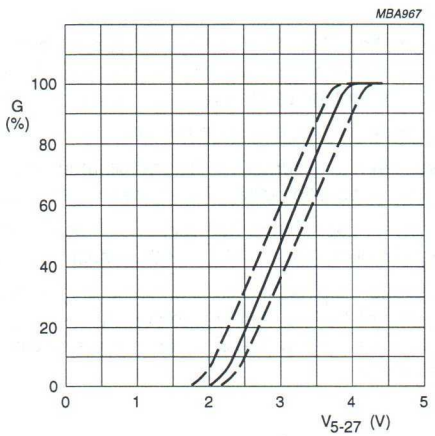


Fig.4 Saturation control voltage range.

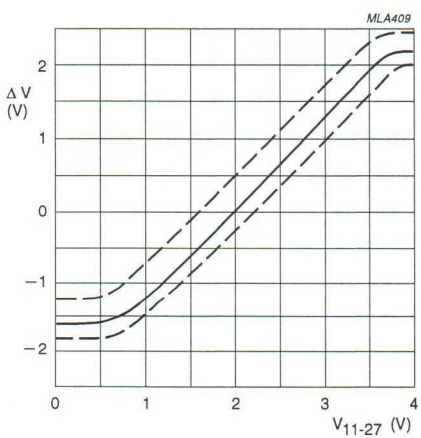


Fig.5 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11}).

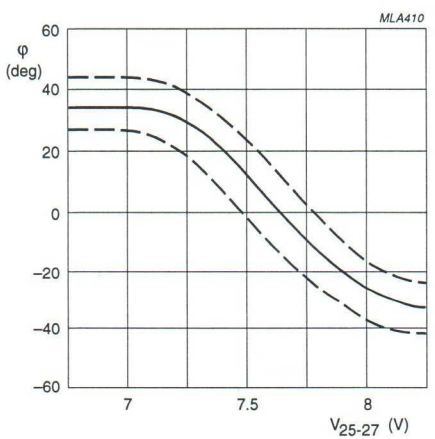


Fig.6 Hue control voltage range.

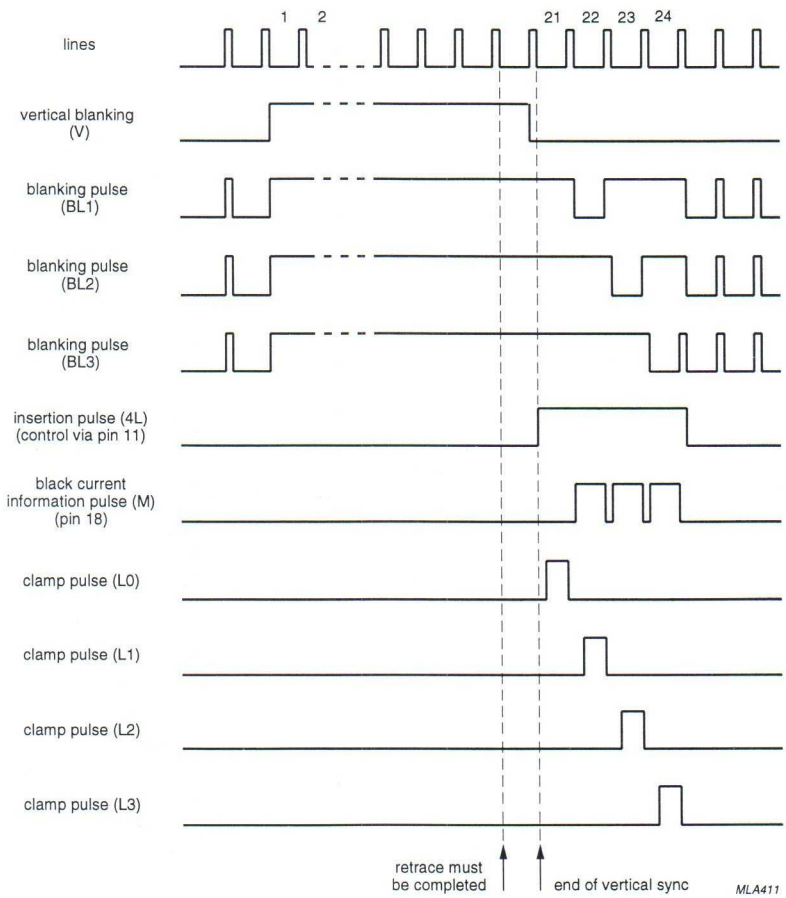


Fig.7 Timing diagram for black-current stabilization.

APPLICATION INFORMATION

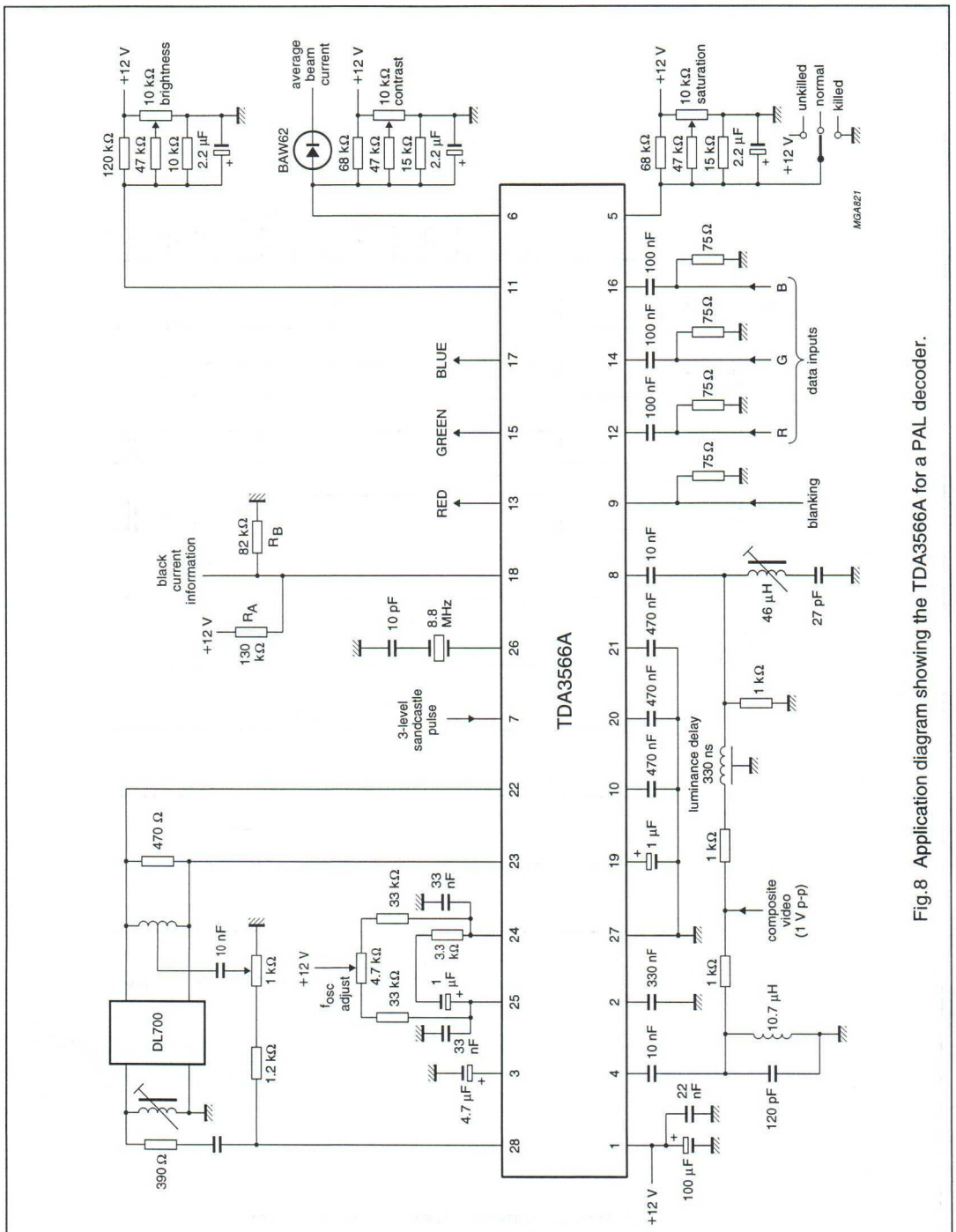


Fig.8 Application diagram showing the TDA3566A for a PAL decoder.

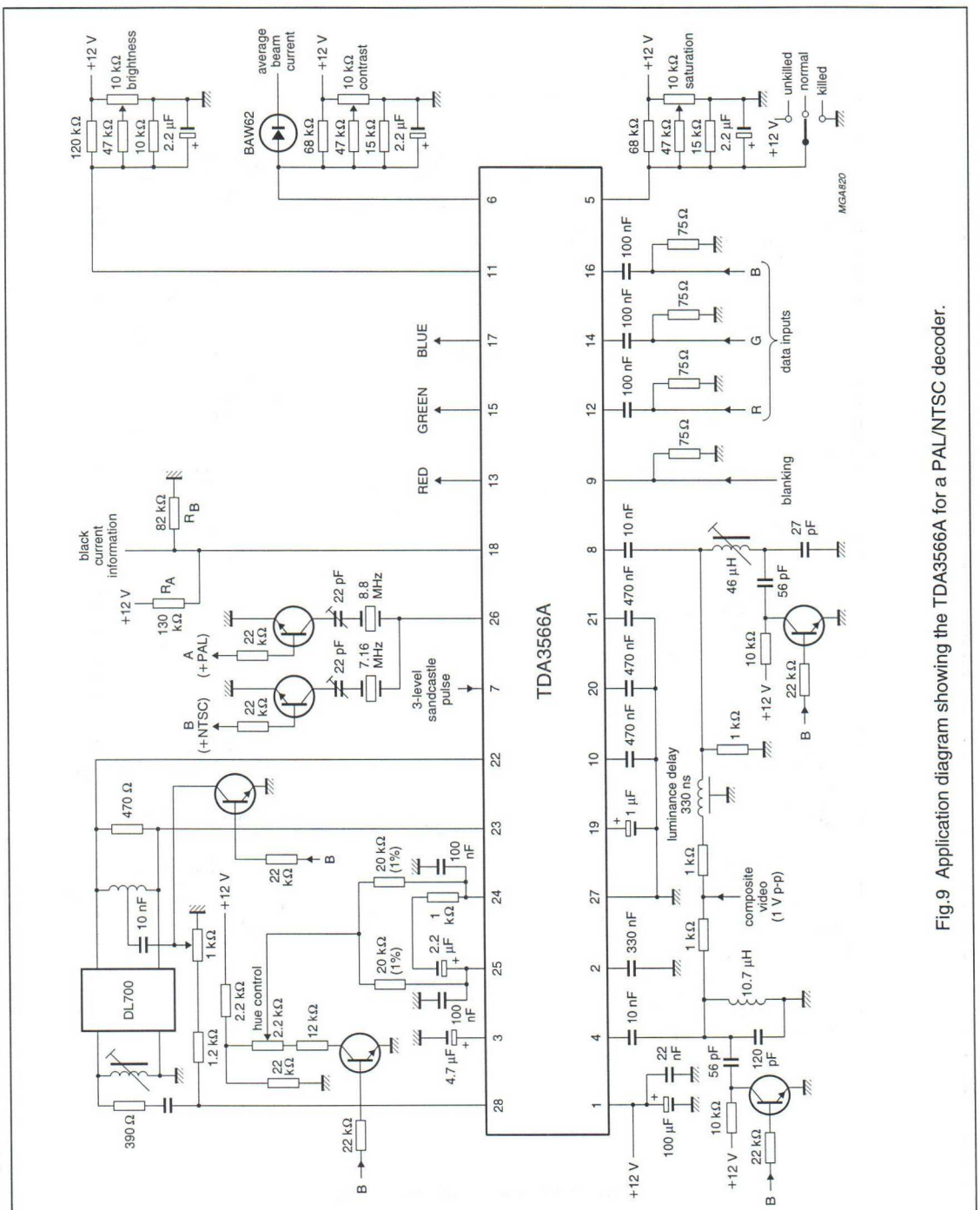


Fig.9 Application diagram showing the TDA3566A for a PAL/NTSC decoder.

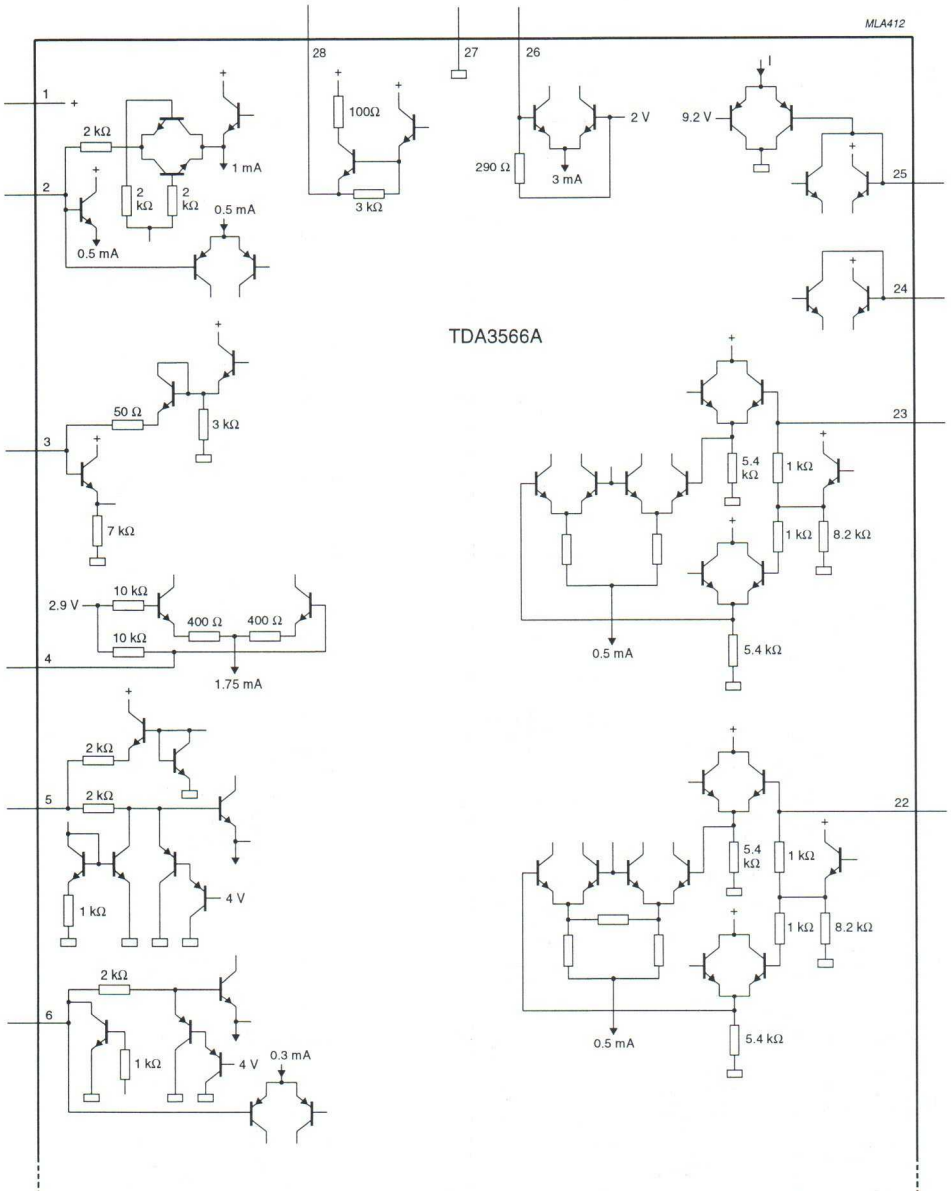


Fig.10 Internal pin circuitry (first part).

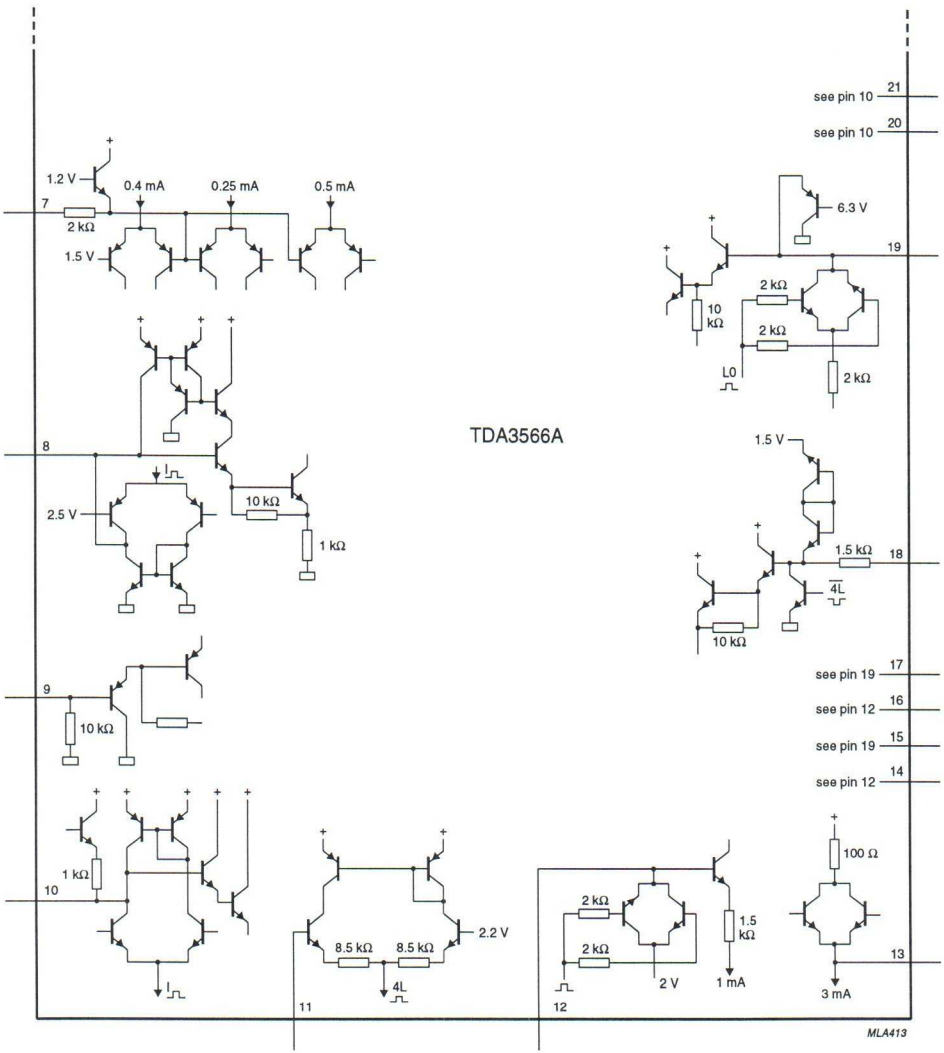


Fig.11 Internal pin circuitry (second part).

NTSC DECODER

GENERAL DESCRIPTION

The TDA3567 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Further more it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-17}$	9	12	13,2	V
Supply current	pin 1	$I_P = I_1$	–	65	–	mA
Luminance input signal	pin 8					
Input voltage (peak-to-peak value)		$V_{8-17(p-p)}$	–	0,45	–	V
Contrast control range			–	20	–	dB
Chrominance amplifier	pin 3					
Input voltage (peak-to-peak value)		$V_{3-17(p-p)}$	–	550	–	mV
Saturation control range			50	–	–	dB
RGB matrix and amplifiers						
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)		$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Sandcastle input	pin 7					
Blanking input voltage		V_{7-17}	1,0	1,5	2,0	V
Burst gating and clamping input voltage		$V_{7-17(p-p)}$	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heatspreader (SOT102).

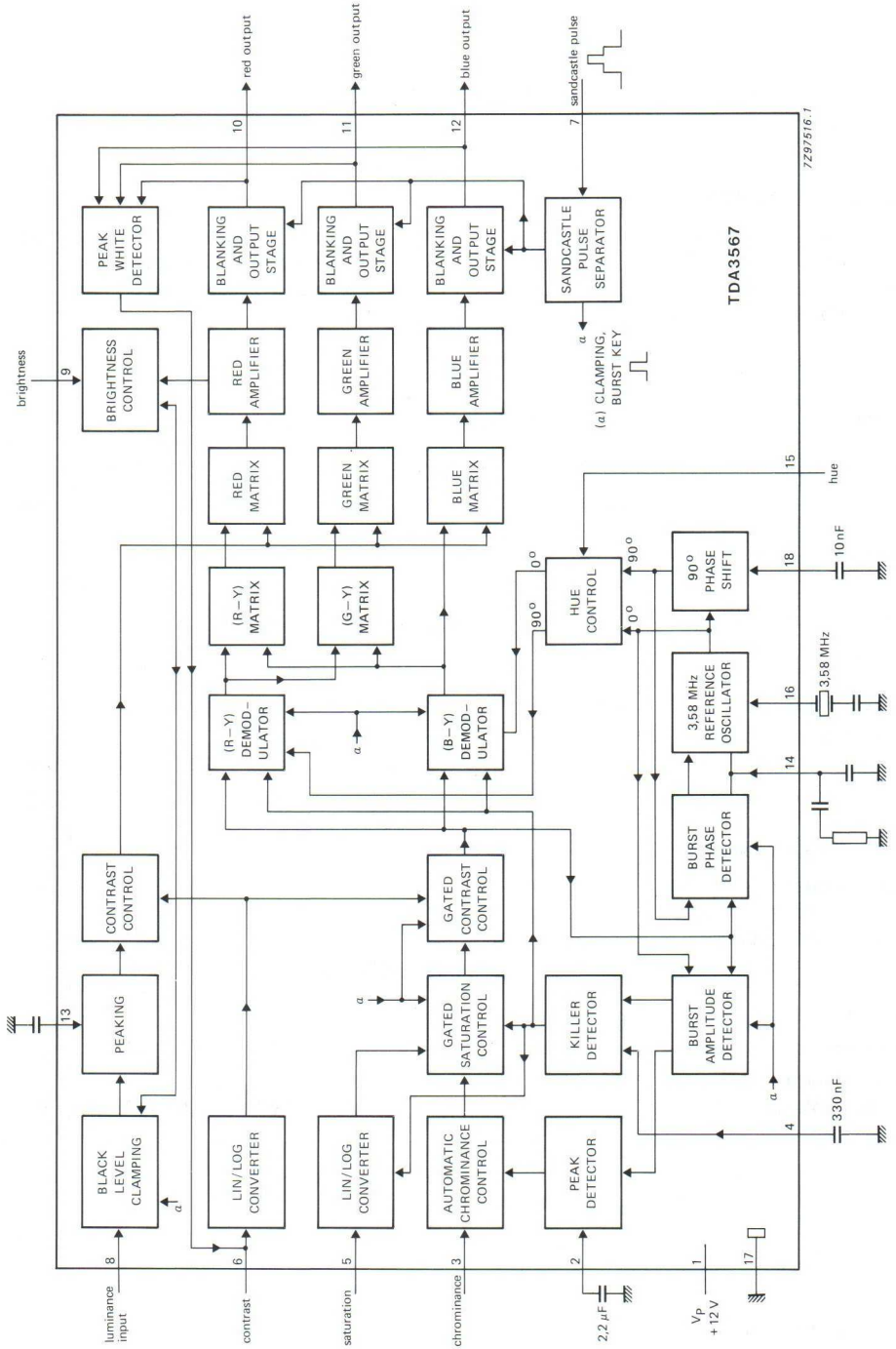


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak*. The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal must be a.c. coupled to the input pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping the signal is fed to a peaking stage. The RC network connected to pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally −17 to + 3 dB. The linear curve of the contrast control voltage is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be a.c. coupled, and must have an amplitude of 550 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V. The impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and a.c.c. detectors.

Oscillator and a.c.c. circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free running frequency of the oscillator can be checked by connecting the saturation control (pin 5) to the positive supply line. Then the loop is opened, so that the frequency can be measured. The oscillator has an internal gain limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0^{o} reference signal by the burst amplitude detector and is then amplified and fed to a peak detector for a.c.c. and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90^{o} phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0^{o} and 90^{o} before they are fed to the (R-Y) and (B-Y) demodulators. The 90^{o} phase shifted signal is provided by a miller integrator (biased by pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

* Signal with negative going sync; amplitude includes sync pulse amplitude.

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 0°, the phase angle of the (B-Y) reference signal is 90°.

For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$

$(G\text{-}Y)_{matrixed} = 0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$

$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes, when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio B-Y/R-Y = 1,78.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input 1 : 2.2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{1-17}$	9	12	13,2	V
Supply current		$I_P = I_1$	–	65	–	mA
Total power dissipation		P_{tot}	–	0,78	–	W
Luminance input signal						
Input voltage (peak-to-peak value)	note 1 pin 8	$V_{8-17(p-p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_{8-17}	–	–	1	V
Input current		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		−17	–	+ 3	dB
Input current contrast control	for $V_{6-17} < 6$ V	I_7	–	0,5	15	μA
Input current when the peak-white limiter is active	$V_{6-17} = 2,5$ V	I_7	–	5,5	–	mA
Input resistance	$V_{6-17} > 6$ V	R_{7-17}	1,4	2,0	2,6	kΩ
Peaking of luminance signal						
Output impedance	pin 13	$\lvert Z_{13-17} \rvert$	–	200	–	Ω
Ratio of internal/external current when pin 13 is short-circuited			–	3	–	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier						
Input signal amplitude (peak-to-peak value)	note 2 pin 3	$V_{3\text{-}17(p\text{-}p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3\text{-}17(p\text{-}p)}$	–	–	1,1	V
Minimum burst signal amplitude within the a.c.c. control range (peak-to-peak)			35	–	–	mV
A.C.C. control range			30	–	–	dB
Change of the burst signal at the output for the complete control range		ΔV	–	–	+ 1	dB
Input impedance	pin 3	$\lvert Z_{3\text{-}17}\rvert$	6	8	10	kΩ
Input capacitance	pin 3	$C_{3\text{-}17}$	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Input current saturation control	for $V_{5\text{-}17} > 6$ V	I_5	–	1	20	μA
Input impedance	$V_{5\text{-}17} = 6$ V to 10 V	$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance when the colour killer is active		$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance	for $V_{5\text{-}17} > 10$ V	$\lvert Z_{5\text{-}17}\rvert$	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB
Cross coupling between luminance and chrominance amplifier	note 4		–	–50	–46	dB
Reference part						
Phase locked loop						
Catching range		Δf	±400	±500	–	Hz
Phase shift for 400 Hz deviation of the carrier frequency		Δ	–	–	5	deg

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	$\Delta V_P = \pm 10\%$	Δf_{osc9}	–	150	250	Hz
Input resistance	pin 16	$R_{16\text{-}17}$	260	360	460	Ω
Input capacitance	pin 16	$C_{22\text{-}17}$	–	–	10	pF
A.C.C. generation						
Voltage at pin 4 nominal input signal		$V_{4\text{-}17}$	–	4,0	–	V
Voltage at pin 4 without burst input		$V_{4\text{-}17}$	–	1,9	–	V
Colour-off voltage		$V_{4\text{-}17}$	–	2,5	–	V
Colour-on voltage		$V_{4\text{-}17}$	–	2,8	–	V
Change in burst amplitude with temperature			–	0,1	–	%/K
Change in burst amplitude with 10% supply voltage change			–	0	–	%/V
Voltage at pin 2 at nominal input signal		$V_{2\text{-}17}$	–	5,0	–	V
Hue control						
Control voltage range				see Fig. 5		
Input current	for $V_{15\text{-}17} < 5$ V	I_{14}	–	0,5	20	μA
Input impedance	for $V_{15\text{-}17} > 5$ V	$\lvert Z_{14\text{-}17} \rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Ratio of demodulation signals (measured at the various outputs)	note 7					
(R-Y)/(B-Y); no (R-Y) signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	−0,42	–	
(R-Y)/(B-Y); colour bar signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	1,4	–	
(G-Y)/(R-Y); no (B-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,25	–	
(G-Y)/(B-Y); no (R-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,11	–	
Frequency response	0 to 0,7 MHz		–	–	−3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifier						
Output signal amplitude	at nominal luminance input signal and nominal contrast (peak-to-peak value) note 3					
	black-white	$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)	$V_{12-17(p-p)}$	–	3,8	–	V
Maximum peak-white level	note 6	$V_{10,11,12-7}$	9,0	9,3	9,6	V
Maximum output current		$I_{10,11,12-17}$	–	–	10	mA
Difference in the black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range			see Fig. 4			
Brightness control input current		I_9	–	–	–50	μA
Black level variation with temperature		V/T	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{b1}	1,95	2,15	2,35	V

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 5	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
RGB output impedance		$\lvert Z_{10,11,12-17} \rvert$	–	–	50	
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which the RGB blanking is activated		V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input currents	V_{7-17} = 0 to 1 V	I_7	–	–	–1	mA
	V_{7-17} = 1 to 8,5 V	I_7	–	–20	–40	μA
	V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Noted to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as maximum contrast –3 dB and nominal saturation as maximum saturation –10 dB.
4. Cross coupling is measured under the following condition:
   - input signals nominal;
   - contrast and saturation such that nominal output signals are obtained;
   - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
6. When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 7 (contrast control). Discharge current is 5,5 mA.
7. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

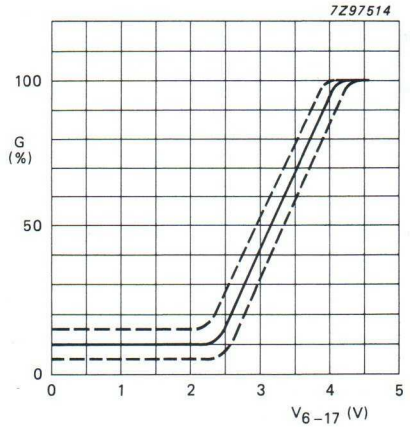


Fig. 2 Contrast control voltage range.

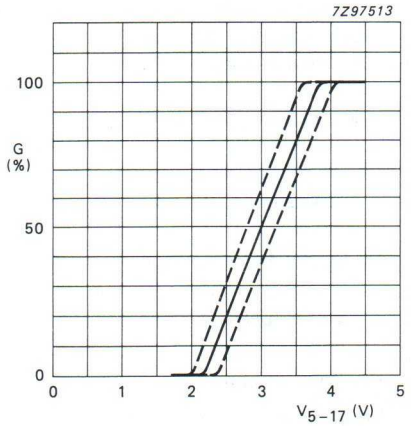


Fig. 3 Saturation control voltage range.

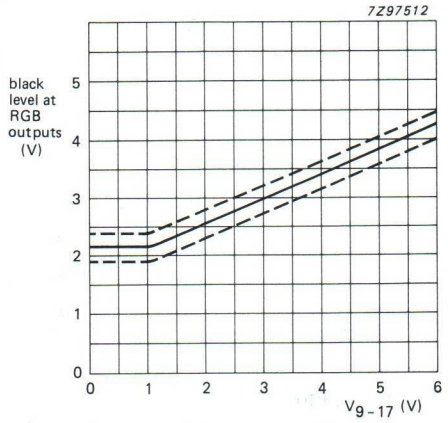


Fig. 4 Brightness control voltage range.

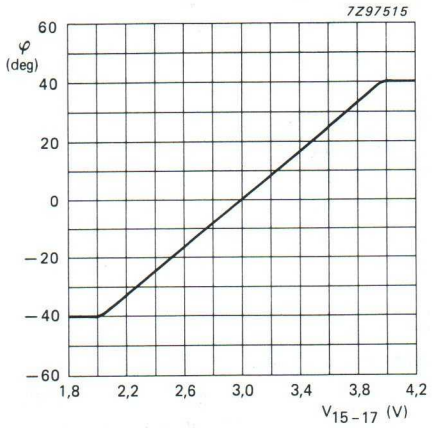


Fig. 5 Hue control voltage range.

APPLICATION INFORMATION

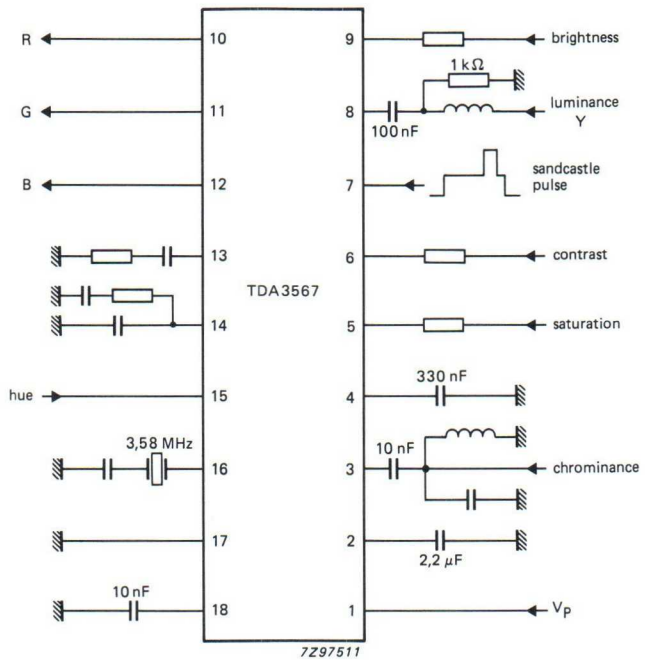


Fig. 6 Application diagram.

SECAM-PAL TRANSCODER

GENERAL DESCRIPTION

The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V: $\overline{\text{SECAM}}$ processing shuts down but $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3-1(p-p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9-1(p-p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		V_{4-1}	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		V_{4-1}	0	–	2,9	V
Identification at pin 6		V_{6-1}	–	10,6	–	V
Slicing level reference voltage (pin 5)		V_{5-1}	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		V_{19-1}	–	1,5	–	V
Horizontal blanking level		V_{19-1}	–	3,5	–	V
Burst gating level		V_{19-1}	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16-1(p-p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		G_{16-15}	–	7,0	–	dB

PACKAGE OUTLINE

24-lead DIL; plastic with heat spreader (SOT-101B).

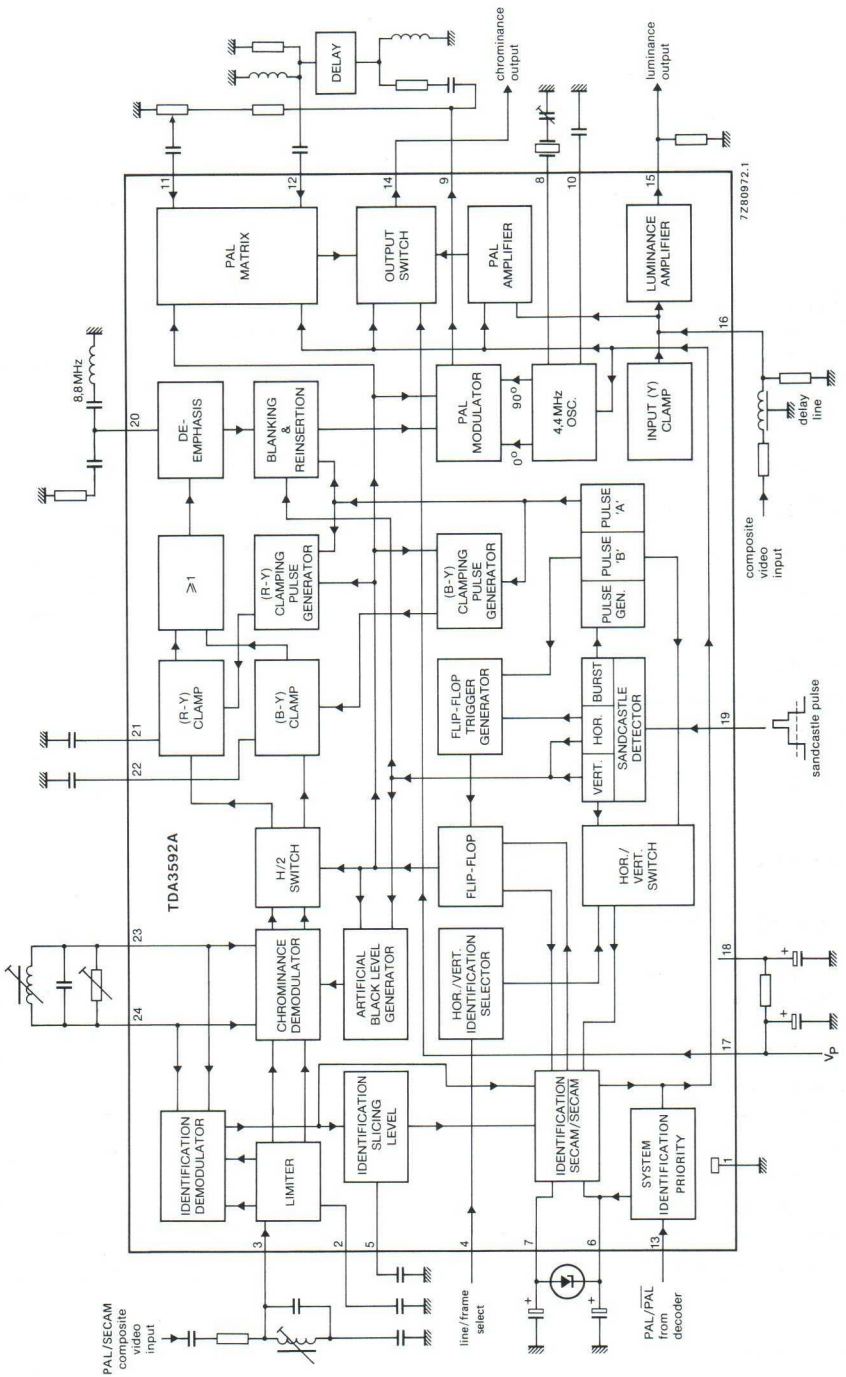


Fig. 1 Block diagram.

PINNING

1. Ground.
2. Limiter feedback.
3. Limiter input: chrominance input SECAM; identification input SECAM/$\overline{\text{SECAM}}$.
4. Identification selection input using a DC level to preset the identification mode.
   At $V_4 < 2{,}9$ V the TDA3592A is preset for frame identification.
   At $V_4 > 4{,}1$ V the TDA3592A is preset for line identification.
5. Storage capacitor input for floating level identification.
6. Storage capacitor input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
7. Double time-constant input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
8. 4,43 MHz oscillator.
9. Sequentially modulated output.
10. Decoupling capacitor for miller integrator feedback circuit.
11. Direct input chrominance signal.
12. Delayed input chrominance signal.
13. PAL/$\overline{\text{PAL}}$ input signal from PAL decoder.
14. Chrominance output signal.
15. Luminance output signal.
16. Luminance/$\overline{\text{SECAM}}$ input signal.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection: R = 560 Ω; C = 1 nF.
21. Storage capacitor connection for (R-Y) clamp.
22. Storage capacitor connection for (B-Y) clamp.
23. Demodulator reference tuned circuit: nominal frequency = 4,33 MHz; nominal $Q_L = 2{,}45$.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizontal blanking periods. This is done because of the possibility of horizontal burst signals not being available. The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and −(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90^{o} out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180^{o} out of phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse 'B' (see Fig. 2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4-1} < 2{,}9$ V;
- Vertical identification preset when $V_{4-1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse 'B' times the SECAM horizontal identification.

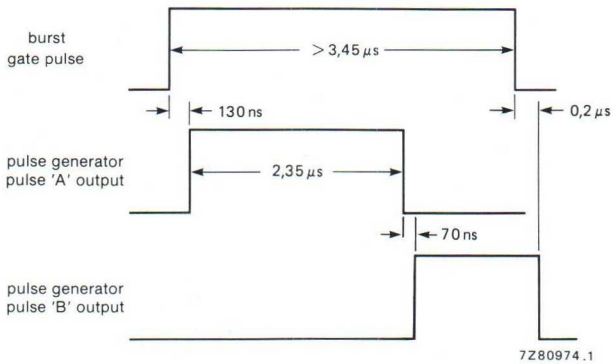


Fig. 2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90^{o} phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the −(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 µs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

FUNCTIONAL DESCRIPTION (continued)

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.

SECAM — The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of $< 1{,}1$ V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).

Black-and-white — The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL decoder mode	System operating mode
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 16 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{17-1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	μA
Decoupled supply voltage (pin 18)	$R_{ext17-18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	μF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j-a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p-p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p-p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		R_{23-24}	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		C_{23-24}	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier and demodulator (continued)						
Linearity of (B-Y) demodulation (pin 20)	note 3	–	–	94	–	%
Linearity of (R-Y) demodulation (pin 20)	note 4	–	–	100	–	%
(R-Y)/(B-Y) ratio (pin 20)		–	–	1,78	–	%
Relative deviation of reinserted black level/demodulated black level (pin 20) as a function of temperature						
(R-Y) signals	note 5	–	–	0,22	–	kHz/°C
(B-Y) signals	note 5	–	–	0,22	–	kHz/°C
Identification SECAM/$\overline{\text{SECAM}}$	note 6					
Input voltage for line identification (pin 4)		V_4	4,1	–	V_P	V
Input voltage for frame identification (pin 4)		V_4	0	–	2,9	V
Switching level for line/frame identification (pin 4)		V_4	3,0	3,5	4,0	V
Input current (pin 4)		$-I_4$	–	5	25	μA
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	10,2	–	V
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	11,5	–	V
Voltage at pin 6 during SECAM		V_6	–	7,0	–	V
Identification at pin 6		V_6	–	10,6	–	V
Colour OFF for SECAM		V_6	9,8	10,1	10,4	V
Colour ON for SECAM		V_6	8,8	9,1	9,4	V
Slicing level reference voltage (pin 5)		V_5	–	8,4	–	V
Sandcastle pulse detector and clamping pulse generator						
Voltage level at which the vertical blanking pulse is separated		V_{19}	1,0	1,5	2,0	V
Voltage level at which the horizontal blanking pulse is separated		V_{19}	3,0	3,5	4,0	V
Voltage level at which the burst gating pulse is separated		V_{19}	6,5	7,0	7,5	V

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector and clamping pulse generator (continued)						
Input current	V_{19} = 0 V	$-I_{19}$	–	30	100	μA
Width of pulse 'A' (Fig. 2)	note 7		1,85	2,35	2,85	μA
Required width of pulse 'B' (Fig. 2)	note 7		0,6	–	–	μs
Luminance amplifier						
Input signal (peak-to-peak value) (pin 16)		$V_{16(p-p)}$	–	1,2	1,7	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,5	7,5	8,5	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		Z_{15}	–	20	–	Ω
Frequency response at −3 dB (pin 15 and 16)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	6,0	7,0	8,0	dB
Frequency response at −3 dB (pin 14 and 16)		f	6,0	–	–	MHz
External load resistance (pin 15)		R_L	2,0	–	–	kΩ
Limiter, chrominance demodulator and PAL modulator	note 8					
Output resistance (pin 9)		R_9	–	25	–	Ω
DC output voltage during horizontal blanking (pin 9)		V_9	–	9,6	–	V
Internal biasing resistor for emitter follower (pin 9)			–	9,0	–	kΩ
External load resistance (pin 9)		$R_{L(9)}$	2	–	–	kΩ
Output signal (pin 9) when input to pin 3 has a Δf of 280 kHz; without external load (peak-to-peak value)		$V_{9(p-p)}$	–	0,82	–	mV
(R-Y)/(B-Y) ratio (pin 9)			1,50	1,78	2,11	
Chrominance/burst ratio for SECAM (pin 9)			2,5	3,0	3,5	
Linearity of (B-Y) signal (pin 9)	note 3		85	92	99	%
Linearity of (R-Y) signal (pin 9)	note 4		93	100	107	%
Black level shift as a function of temperature (pin 9)						
(R-Y) signals	note 9		–	0,22	–	kHz/°C
(B-Y) signals	note 9		–	0,22	–	kHz/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Limiter, chrominance demodulator and PAL modulator (continued)						
Phase relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			87	90	93	deg
Amplitude relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			−1,5	0	+1,5	dB
Black level shift as a function of supply voltage (pin 9)						
(R-Y) signal			–	−1,5	–	kHz/V
(B-Y) signal			–	1,0	–	kHz/V
Oscillator						
Oscillator frequency (pin 9) (set with series capacitor)		f_{OSC}	–	4,433619	–	MHz
Frequency deviation without spread of external components (pin 9)		Δf_{OSC}	–	–	±150	Hz
Temperature coefficient of oscillator frequency (pin 9)			–	−2	−3	Hz/°C
Frequency deviation for change of V_P from 9,0 to 13,2 V		Δf_{OSC}	–	–	150	Hz
DC voltage (pin 8)		V_8	–	4,7	–	V
Input resistance (pin 8)		R_8	–	1	–	kΩ
DC voltage (pin 10)		V_{10}	–	4,4	–	V
Input resistance (pin 10)		R_{10}	–	2	–	kΩ
PAL matrix						
Input resistance (pin 11)		R_{11}	700	900	1100	Ω
Input resistance (pin 12)		R_{12}	700	900	1100	Ω
Output resistance (pin 14) (SECAM/$\overline{\text{SECAM}}$)		R_{14}	–	40	–	Ω
Internal emitter follower load resistance (pin 14)		$R_{INT(14)}$	–	7	–	kΩ
External load resistor (pin 14)		$R_{L(14)}$	2,4	–	–	kΩ
DC voltage (pin 11)		V_{11}	–	5,0	–	V
DC voltage (pin 12)		V_{12}	–	5,0	–	V
DC voltage (pin 14)	SECAM mode	V_{14}	–	6,2	–	V
DC voltage (pin 14)	$\overline{\text{SECAM}}$ mode and line blanking	V_{14}	–	4,9	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
PAL matrix (continued)						
H/2 ripple on chrominance output (pin 14) (peak-to-peak value)	SECAM mode	$V_{14(p-p)}$	–	–	100	mV
Gain A; pin 11 to 14		G_A	9	10	11	dB
Gain B; pin 12 to 14 ((R-Y) at pin 9)		G_B	9	10	11	dB
Gain C; pin 12 to 14 ((B-Y) at pin 9)		G_C	9	10	11	dB
Gain A – gain B		G_A-G_B	–0,7	–	+0,7	dB
Gain A – gain C		G_A-G_C	–0,7	–	+0,7	dB
Gain B – gain C		G_B-G_C	–0,7	–	+0,7	dB
Phase A; pins 11, 14 to pins 12, 14 ((R-Y) at pin 9)			–	181,5	–	deg
Phase B; pins 11, 14 to pins 12, 14 ((B-Y) at pin 9)			–	1,5	–	deg
Phase A – phase B			178	180	182	deg
Identification PAL/$\overline{\text{PAL}}$						
Input condition for PAL (pin 13)		V_{13}	1,7	–	V_P	V
Input condition for $\overline{\text{PAL}}$ (pin 13)		V_{13}	–	–	1,1	V
Input current	V_{13} = 6 V	I_{13}	–	–	10	μA
Input resistance	V_{13} = 8,2 V	R_{13}	7,5	11,5	15,5	kΩ
Pin 6 internal current in PAL/$\overline{\text{SECAM}}$ mode		$-I_6$	0,24	0,4	0,58	mA
Switching level PAL/$\overline{\text{PAL}}$ (pin 13)		V_{13}	1,2	1,4	1,6	V

CHARACTERISTICS AT LOW SUPPLY VOLTAGE

$V_P = V_{17-1} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply current		$I_{17}+I_{18}$	16	20	24	mA
Supply voltage switching level for preset SECAM signal path	SECAM processing OFF	V_{17-1}	6,5	7,5	8,2	V
Luminance amplifier						
Input signal (peak-to-peak value)		$V_{16(p-p)}$	–	0,45	0,56	V
Gain (pin 16 to 15)	$f_{16} = 4,4$ MHz	G_{16-15}	6,0	7,0	8,0	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		$\lvert Z_{15-1}\rvert$	–	20	–	Ω
Minimum load resistance (pin 15)		R_L	2	–	–	kΩ
Frequency response at –3 dB (pin 16 to 15)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	$f_{16} = 4,4$ MHz	G_{16-14}	5,7	6,8	7,9	dB
Frequency response at –3 dB (pin 16 to 14)		f	6	–	–	MHz

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 3 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 14 to the PAL decoder is minimum during scan (PAL black colour information).
2. When the input signal to the limiter (pin 3) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz; f = 4,33 MHz (typ.).
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz.
5. The parameter value is equated by: $\frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y - X} \times \frac{\Delta f\ (kHz)}{^{o}C}$

   $E = \frac{E1 - E2}{2}$ $\quad F = \frac{F1 - F2}{2}$

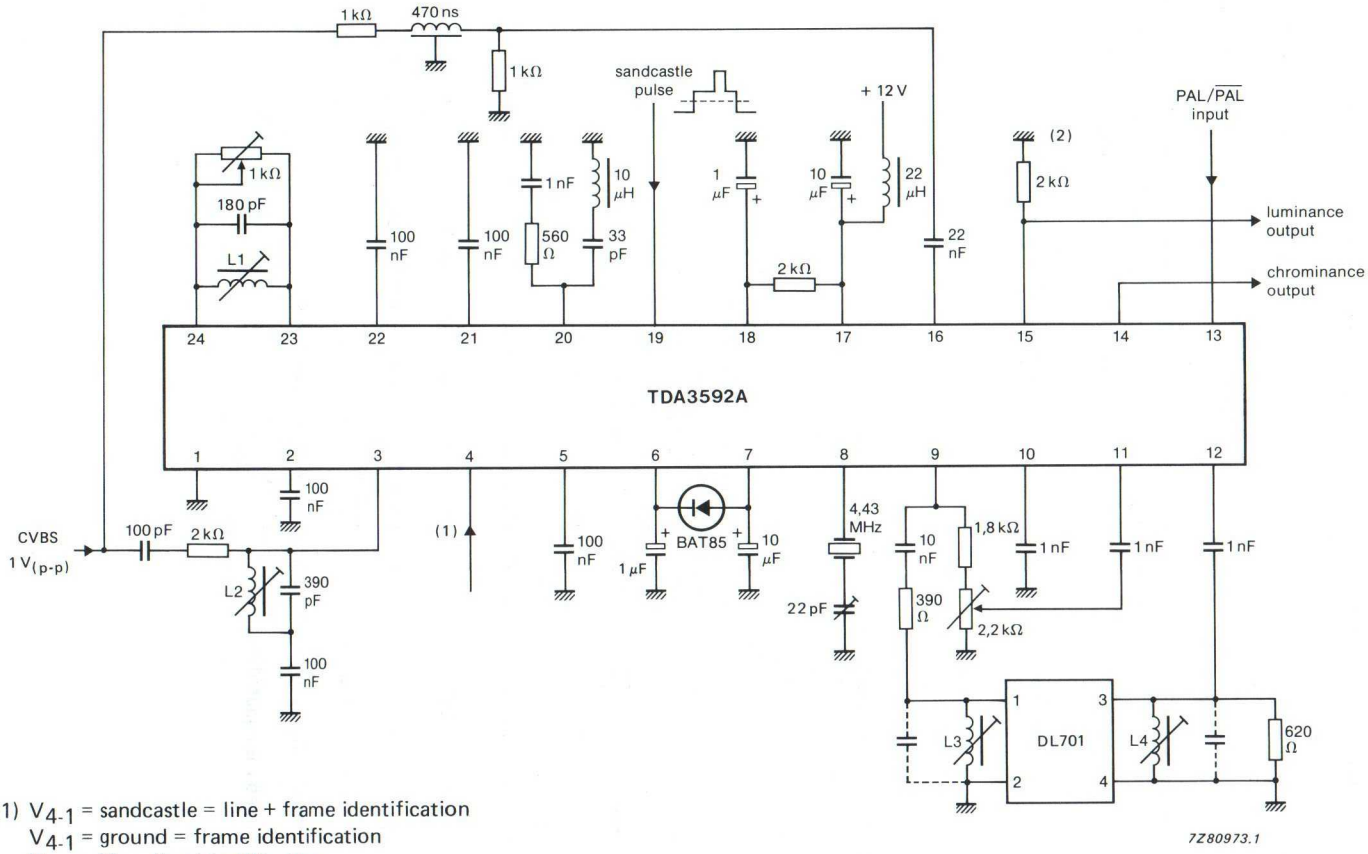
   Where A = demodulated black level at temperature X
   B = demodulated black level at temperature Y
   C = artificial black level at temperature X
   D = artificial black level at temperature Y
   E1 = demodulated output signal at temperature X ($f_o - \Delta f$)
   E2 = demodulated output signal at temperature X ($f_o + \Delta f$)
   F1 = demodulated output signal at temperature Y ($f_o - \Delta f$)
   F2 = demodulated output signal at temperature Y ($f_o + \Delta f$)

   for B-Y: $f_o = f_{ob}$ = 4,25 MHz (Δf = 230 kHz)
   for R-Y: $f_o = f_{or}$ = 4,40625 MHz (Δf = 280 kHz)
6. During stable signal conditions V_7 is always at V_F(BAT85) below V_6.
7. The burst gate pulse width > 3,45 μs.
8. The specification figures are only valid when the reference tuned circuit is aligned as indicated in note 1.
9. Ensure that the 4,433 MHz carrier is in the correct phase; black level shift at temperature X = A and at Y = B.
   Output signal (Δf = 230 kHz for B-Y; Δf = 280 kHz for R-Y) at temperature X = E and at Y = F.

   The parameter is equated by: $\frac{(B/(F\text{-}B) - A/(E\text{-}A)}{Y - X} \times 230;\ 280\ kHz$
10. Chrominance definition — burst ratio at SECAM condition (pin 9).

    The parameter is equated by: $\frac{V_{out(p\text{-}p)}\ Red\ (R\text{-}Y)}{V_{burst(p\text{-}p)}\ (R\text{-}Y)}$.

APPLICATION INFORMATION



(1) V_{4-1} = sandcastle = line + frame identification
V_{4-1} = ground = frame identification
V_{4-1} = V_P = line identification

(2) minimum load resistance at pin 15 = 2 kΩ

Fig. 3 Application circuit.

VERTICAL DEFLECTION AND GUARD CIRCUIT (90°)

GENERAL DESCRIPTION

The TDA3653B/C is a vertical deflection output circuit for drive of various deflection systems with currents up to 1.5 A peak-to-peak.

Features

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer
- Guard circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply (note 1)					
Supply voltage range					
pin 9	$V_P = V_{9-4}$	10	–	40	V
pin 6	V_{6-4}	–	–	60	V
Output (pin 5)					
Peak output voltage during flyback	V_{5-4M}	–	–	60	V
Output current	$I_{5(p-p)}$	–	1.2	1.5	A
Operating junction temperature range	T_j	−25	–	+ 150	°C
Thermal resistance junction to mounting base					
(SOT110B)	$R_{th\ j-mb}$	–	10	–	K/W
(SOT131)	$R_{th\ j-mb}$	–	3.5	–	K/W

Note to the quick reference data

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.

PACKAGE OUTLINES

TDA3653B: 9-lead SIL; plastic (SOT110B).
TDA3653C: 9-lead SIL; plastic power (SOT131).

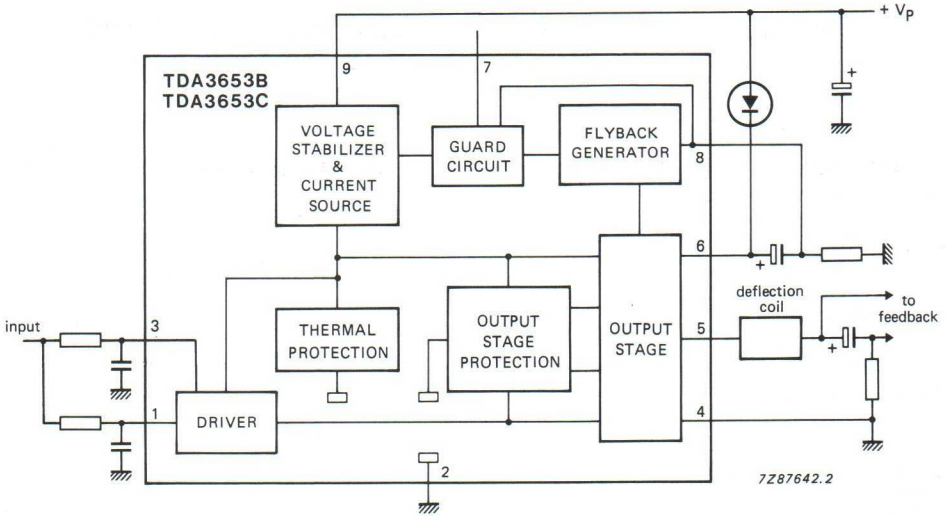


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 0.75 A maximum. The maximum voltage for pin 5 and 6 is 60 V.

The output power transistors are protected such that their operation remains within the SOAR area. This is achieved by the co-operation of the thermal protection circuit, the current-voltage detector, the short-circuit protection and the special measures in the internal circuit layout.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied via external resistors to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.

External connection of pin 1 to pin 3 allows for applications in which the pins are driven separately.

Flyback generator

During scan the capacitor connected between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig.1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is > 2.5 V, during normal operation.

Guard circuit

When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 1.8 V. The guard circuit will then produce a DC voltage at pin 7, which can be used to blank the picture tube and thus prevent screen damage.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, which prevents the drive current of the output stage being affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); pins 4 and 2 externally connected to ground.

paramater	symbol	min.	max.	unit
Supply voltage (pin 9)	$V_P = V_{9-4}$	--	40	V
Supply voltage output stage (pin 6)	V_{6-4}	–	60	V
Output voltage (pin 5)	V_{5-4}	–	60	V
Input voltage (pins 1 and 3)	$V_{1;\,3-2}$	–	V_P	V
External voltage at pin 7	V_{7-2}	–	5.8	V
Peak output current (pin 5)				
repetitive	$\pm I_{5RM}$	–	0.75	A
non-repetitive	$\pm I_{5SM}$	–	1.5	A*
Peak output current (pin 8)				
repetitive	I_{8RM}	0.85	0.75	A
non-repetitive	$\pm I_{8SM}$	–	1.5	A*
Total power dissipation	P_{tot}	see Fig. 2		
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	see Fig. 2		
Operating junction temperature range	T_j	–25	+ 150	°C

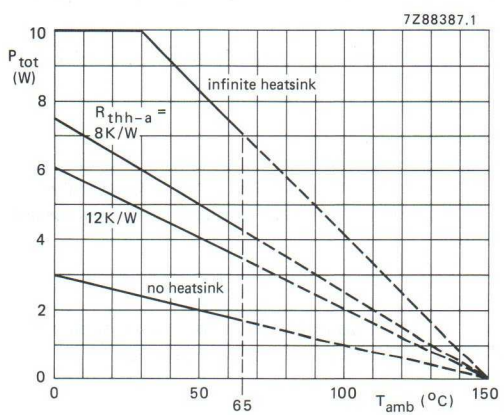


Fig. 2 Power derating curves (for SOT110B).

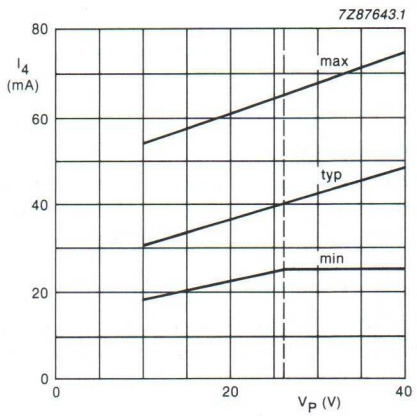


Fig. 3 Quiescent current I_4 as a function of supply voltage V_P.

* Non-repetitive duty factor maximum 3.3%.

CHARACTERISTICS

$V_P = V_{9-4} = 26$ V; $T_{amb} = 25$ °C; pins 2 and 4 externally connected to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 9)	note 1	$V_P = V_{9-4}$	10	–	40	V
Supply voltage (pin 6)	note 1	V_{6-4}	–	–	60	V
Total supply current (pin 6 and pin 9)	note 2	$I_P = I_6 + I_9$	34	50	85	mA
Quiescent current (pin 4)	see Fig. 3	I_4	25	40	65	mA
Variation of quiescent current with temperature		ΔI_4	–	−0.04	–	mA/K
Output current						
Output current (pin 5) (peak-to-peak value)		$I_{5(p-p)}$	–	1.2	1.5	A
Output current flyback generator (pin 8)		$-I_8$	–	0.7	0.85	A
Output current flyback generator (pin 8)		I_8	–	0.6	0.75	A
Output voltage						
Peak voltage during flyback		V_{5-4M}	–	–	60	V
Saturation voltage to supply						
at $-I_5 = 0.75$ A		V_{6-5sat}	–	2.5	3.0	V
at $I_5 = 0.75$ A	note 3	V_{5-6sat}	–	2.5	3.0	V
at $-I_5 = 0.60$ A		V_{6-5sat}	–	2.2	2.7	V
at $I_5 = 0.60$ A	note 3	V_{5-6sat}	–	2.3	2.8	V
Saturation voltage to ground						
at $I_5 = 0.75$ A		V_{5-4sat}	–	2.3	2.7	V
at $I_5 = 0.60$ A		V_{5-4sat}	–	2.1	2.4	V
Flyback generator						
Saturation voltage						
at $-I_8 = 0.85$ A		V_{9-8sat}	–	1.6	2.1	V
at $I_8 = 0.75$ A	note 3	V_{8-9sat}	–	2.3	2.8	V
at $-I_8 = 0.70$ A		V_{9-8sat}	–	1.4	1.9	V
at $I_8 = 0.60$ A	note 3	V_{8-9sat}	–	2.2	2.7	V
Flyback generator active if:		V_{5-9}	4.0	–	–	V
Leakage current at pin 8		$-I_8$	–	5.0	100	μA
Input						
Input current (pin 1)	$I_5 = 0.75$ A	I_1	–	0.33	0.55	mA
Input voltage during scan (pin 1)	$I_5 = 0.75$ A	V_{1-2}	–	1.5	2.4	V
Input voltage during scan (pin 3) pins 1 and 3 not connected		V_{3-2}	0.8	–	V_P	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input (continued)						
Input current during scan (pin 3)						
pins 1 and 3 not connected		I_3	0.03	–	–	mA
pins 1 and 3 connected		I_3	–	–	0.21	mA
Input resistance (pin 3)		R_3	3.9	5.3	6.7	kΩ
Input voltage during flyback (pin 1)		V_{1-2}	–	–	250	mV
Input voltage during flyback (pin 3)		V_{3-2}	–	–	250	mV
Guard circuit						
Output voltage (pin 7)	note 4					
loaded with 100 kΩ		V_{7-2}	4.4	5.1	5.8	V
loaded with 0.5 mA		V_{7-2}	3.6	4.4	5.3	V
Internal series resistance of pin 7		R_{i7}	0.95	1.35	1.7	kΩ
Guard circuit active if V_{8-2} is lower than	note 5	V_{8-2}	–	–	1.8	V
General data						
Thermal protection becomes active if junction temperature exceeds		T_j	158	175	192	°C
Thermal resistance junction to mounting base		$R_{th\ j\text{-}mb}$	–	10	12	K/W
Open loop gain at 1 kHz	note 6	G_{ol}	–	42	–	dB
Frequency response (–3 dB)	note 7	f	–	40	–	kHz

Notes to the characteristics

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.
2. When V_{5-4} = 13 V and no load at pin 5.
3. Duty factor maximum 3.3%.
4. Guard circuit is active.
5. During normal operation the voltage V_{8-2} may not be lower than 2.5 V.
6. R_{load} = 8 Ω; $I_{load(rms)}$ = 125 mA.
7. With 220 pF between pins 1 and 5.

APPLICATION INFORMATION

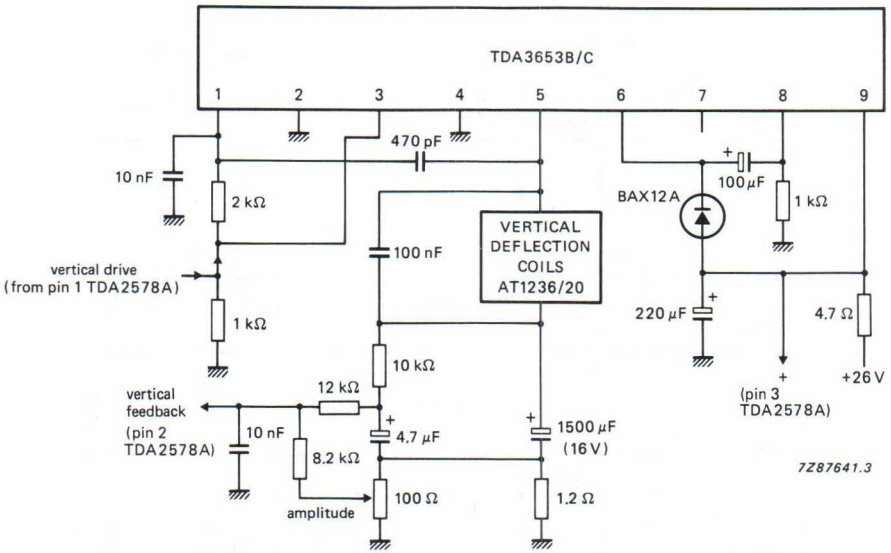


Fig. 4 Typical application circuit diagram of the TDA3653B/C (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13.6 Ω; deflection current without overscan is 0.82 A peak-to-peak and EHT voltage is 25 kV.

APPLICATION INFORMATION (continued)

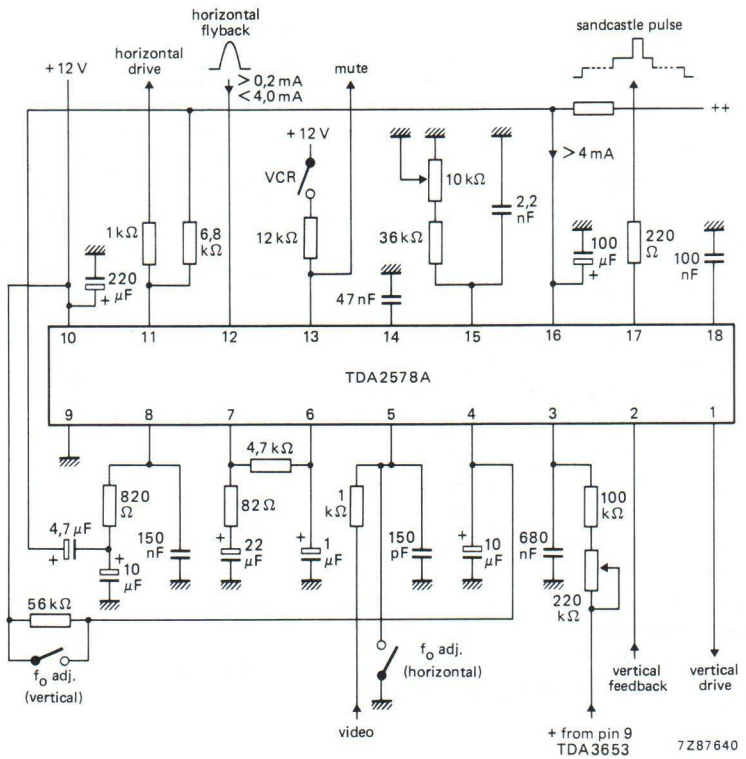
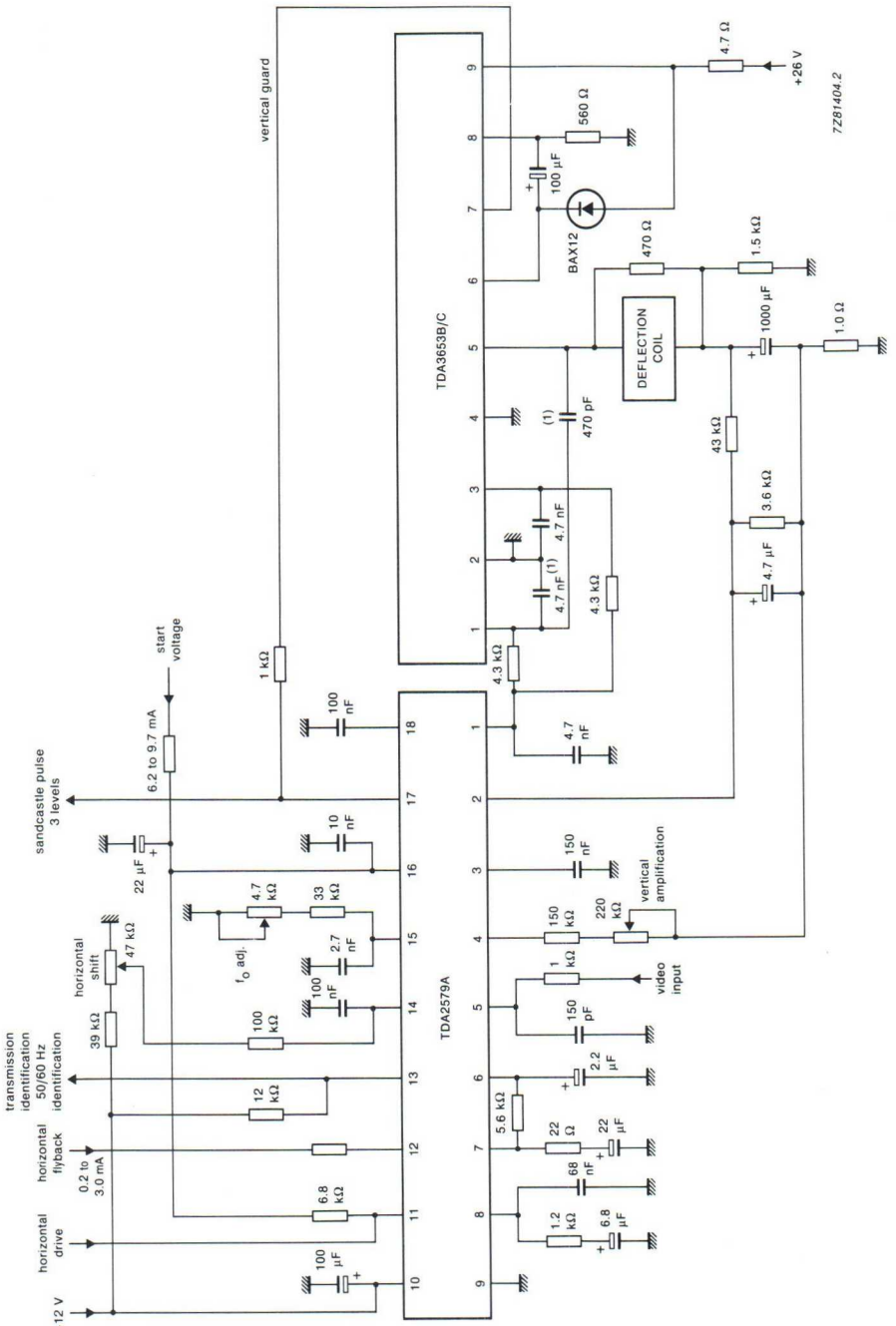


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3653B/C (see Fig. 4).



(1) Dependent on PCB layout.

Fig.6 Application circuit diagram for combination with TDA2579A for 90° picture tube.

VERTICAL DEFLECTION AND GUARD CIRCUIT (110°)

GENERAL DESCRIPTION

The TDA3654 is a full performance vertical deflection output circuit for direct drive of the deflection coils and can be used for a wide range of 90° and 110° deflection systems.
A guard circuit is provided which blanks the picture tube screen in the absence of deflection current.

Features

- Direct drive to the deflection coils
- 90° and 110° deflection system
- Internal blanking guard circuit
- Internal voltage stabilizer

QUICK REFERENCE DATA

Output voltage	V_{5-2}	max.	60 V
Output current (peak-to-peak)	$I_{5(p-p)}$	max.	3 A
Supply voltage	V_{9-2}	max.	40 V
Guard circuit output voltage	V_{7-2}	max.	5,6 V
Operating ambient temperature range	T_{amb}		−25 to +60 °C
Storage temperature	T_{stg}		−55 to +150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	3,5 to 4 K/W

PACKAGE OUTLINES

TDA3654 : 9-lead SIL; plastic power (SOT131).
TDA3654Q : 9-lead SIL bent to DIL; plastic power (SOT157).

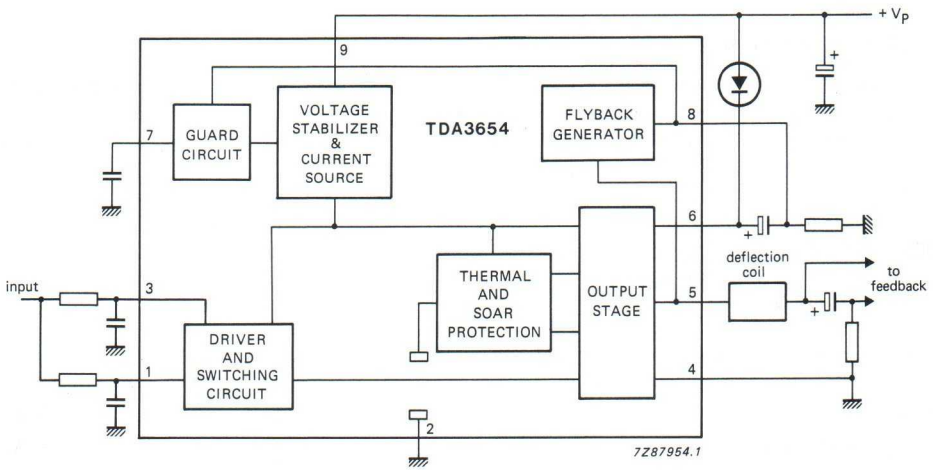


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuits

The output stage consists of two Darlington configurations in class B arrangement.
Each output transistor can deliver 1,5 A maximum and the V_{CEO} is 60 V.
Protection of the output stage is such that the operation of the transistors remains well within the SOAR area in all circumstances at the output pin, (pin 5). This is obtained by the cooperation of the thermal protection circuit, the current-voltage detector and the short circuit protection.
Special measures in the internal circuit layout give the output transistors extra solidity, this is illustrated in Fig. 5 where typical SOAR curves of the lower output transistor are given. The same curves also apply for the upper output device. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit (pin 1 and 3 are connected via external resistors).
This switching circuit rapidly turns off the lower output stage when the flyback starts and it, therefore, allows a quick start of the flyback generator. The maximum required input signal for the maximum output current peak-to-peak value of 3 A is only 3 V, the sum of the currents in pins 1 and 3 is then maximum 1 mA.

Flyback generator

During scan, the capacitor between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig. 1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is $> 1{,}5$ V, during normal operation.

Guard circuit

When there is no deflection current, for any reason, the voltage at pin 8 becomes less than 1 V, the guard circuit will produce a d.c. voltage at pin 7. This voltage can be used to blank the picture tube, so that the screen will not burn in.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, so the drive current is not affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Pins 2 and 4 are externally connected to ground.

Voltages				
Output voltage	V_{5-4}		0 to 60	V
Supply voltage	V_{9-4}		0 to 40	V
Supply voltage output stage	V_{6-4}		0 to 60	V
Input voltage	V_{1-2}		0 to V_{9-4}	V
Input voltage switching circuit	V_{3-2}		0 to V_{9-4}	V
External voltage at pin 7	V_{7-2}		0 to 5,6	V
Currents				
Repetitive peak output current	$\pm I_{5RM}$	max.	1,5	A
Non-repetitive peak output current (note 1)	$\pm I_{5SM}$	max.	3	A
Repetitive peak output current of flyback generator	I_{8RM}	max.	+ 1,5 −1,6	A A
Non-repetitive peak output current of flyback generator (note 1)	$\pm I_{8SM}$	max.	3	A
Temperatures				
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}		−25 to + 60	°C
Operating junction temperature range (the output current at pin 5 should not exceed 2.5A)	T_j		−25 to + 150	°C

CHARACTERISTICS

T_{amb} = 25 °C, supply voltage (V_{9-4}) = 26 V; unless otherwise stated; pin 1 externally connected to pin 3. Pins 2 and 4 externally connected to ground.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage, pin 9 (note 2)	V_{9-4}	10	–	40	V
Supply voltage output stage	V_{6-4}	–	–	60	V
Supply current, pins 6 and 9 (note 3)	I_6+I_9	35	55	85	mA
Quiescent current (note 4)	I_4	25	40	65	mA
Variation of quiescent current with temperature	TC	–	–0,04	–	mA/K
Output current					
Output current, pin 5 (peak-to-peak)	$I_{5(p-p)}$	–	2,5	3	A
Output current flyback generator, pin 8	$+I_{8(p-p)}$	–	1,25	1,5	A
	$-I_{8(p-p)}$	–	1,35	1,6	A
Output voltage					
Peak voltage during flyback	V_{5-4}	–	–	60	V
Saturation voltage to supply					
at I_5 = –1,5 A	$V_{6-5(sat)}$		2,5	3,2	V
at I_5 = 1,5 A (note 5)	$V_{5-6(sat)}$		2,5	3,2	V
at I_5 = –1,2 A	$V_{6-5(sat)}$		2,2	2,7	V
at I_5 = 1,2 A (note 5)	$V_{5-6(sat)}$		2,3	2,8	V
Saturation voltage to ground					
at I_5 = 1,2 A	$V_{5-4(sat)}$	–	2,2	2,7	V
at I_5 = 1,5 A	$V_{5-4(sat)}$	–	2,5	3,2	V
Flyback generator					
Saturation voltage					
at I_8 = –1,6 A	$V_{9-8(sat)}$	–	1,6	2,1	V
at I_8 = 1,5 A (note 5)	$V_{8-9(sat)}$	–	2,3	3	V
at I_8 = –1,3 A	$V_{9-8(sat)}$	–	1,4	1,9	V
at I_8 = 1,2 A (note 5)	$V_{8-9(sat)}$	–	2,2	2,7	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Flyback generator active if:	V_{5-9}	4	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Input					
Input current, pin 1, for I_5 = 1,5 A	I_1	–	0,33	0,55	mA
Input voltage during scan, pin 1	V_{1-2}	–	2,35	3	V
Input current, pin 3, during scan (note 6)	I_3	0,03	–	–	mA
Input voltage, pin 3, during scan (note 6)	V_{3-2}	0,8	–	V_{9-4}	V
Input voltage, pin 1, during flyback	V_{1-2}	–	–	250	mV
Input voltage, pin 3, during flyback	V_{3-2}	–	–	250	mV
Guard circuit					
Output voltage, pin 7 R_L = 100 kΩ (note 9)	V_{7-2}	4,1	4,5	5,8	V
Output voltage, pin 7 at I_L = 0,5 mA (note 9)	V_{7-2}	3,4	3,9	5,3	V
Internal series resistance of pin 7	Ri_7	0,95	1,35	1,7	kΩ
Guard circuit activates (note 7)	V_{8-2}	–	–	1,0	V
General data					
Thermal protection activation range	T_j	158	175	192	°C
Thermal resistance					
From junction to mounting base	$R_{th\ j\text{-}mb}$	–	3,5	4	K/W
Power dissipation	P_{tot}	–	see Fig. 3		
Open loop gain at 1 kHz; (note 8)	G_o	–	33	–	
Frequency response, –3 dB; (note 10)	f	–	60	–	kHz

Notes to the characteristics

1. Non-repetitive duty factor 3,3%.
2. The maximum supply voltage should be chosen so that during flyback the voltage at pin 5 does not exceed 60 V.
3. When V_{5-4} is 13 V and no load at pin 5.
4. See Fig. 4.
5. Duty cycle, d = 5% or d = 0,05.
6. When pin 3 is driven separately from pin 1.
7. During normal operation the voltage V_{8-2} may not be lower than 1,5 V.
8. $R_L = 8\ \Omega$; $I_L = 125$ mA (r.m.s.).
9. If guard circuit is active.
10. With a 22 pF capacitor between pins 1 and 5.

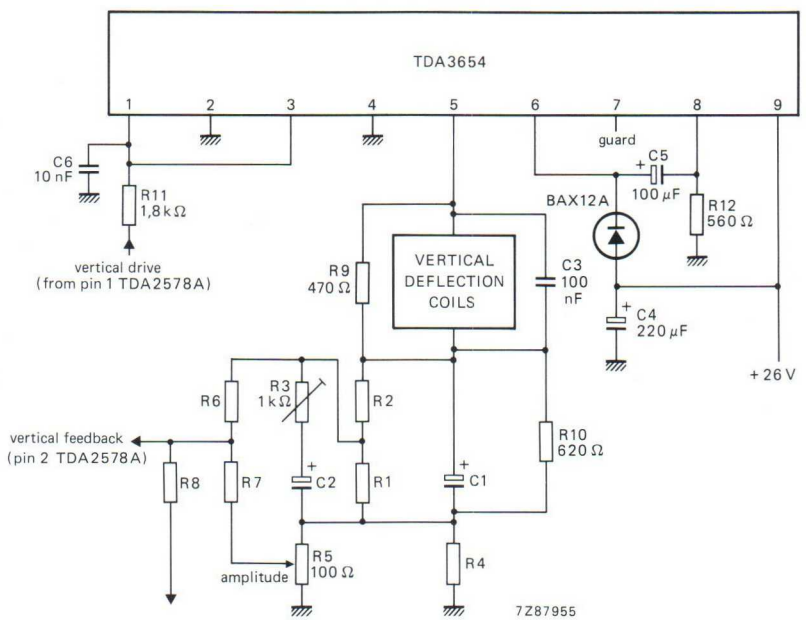


Fig. 2 Application diagram.

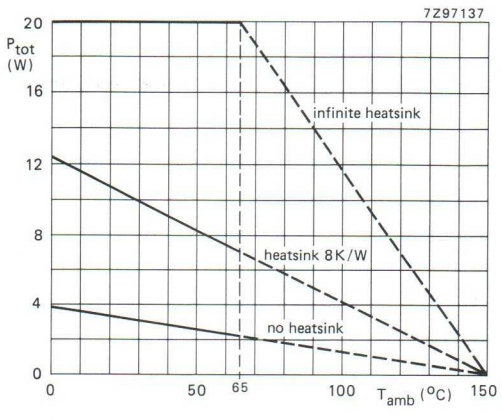


Fig. 3 Power derating curve.

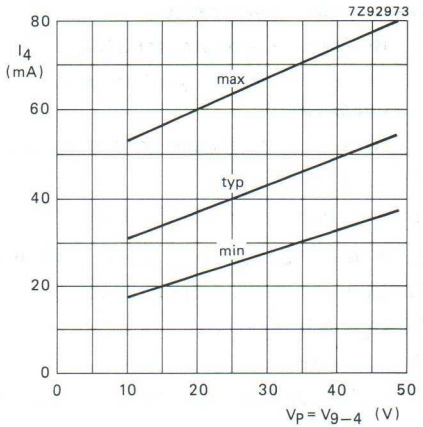
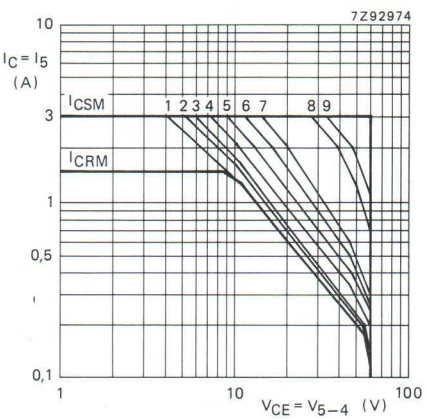


Fig. 4 Quiescent current as a function of the supply voltage.

curve	t_p	δ	peak junction temperature
1	d.c.	–	150 °C
2	10 ms	0,5	150 °C
3	10 ms	0,25	150 °C
4	1 ms	0,5	150 °C
5	1 ms	0,25	150 °C
6	1 ms	0,05	150 °C
7	1 ms	0,05	180 °C
8	0,2 ms	0,1	150 °C
9	0,2 ms	0,1	180 °C



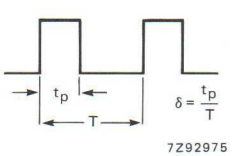


Fig. 5 Typical SOAR of lower output transistor.

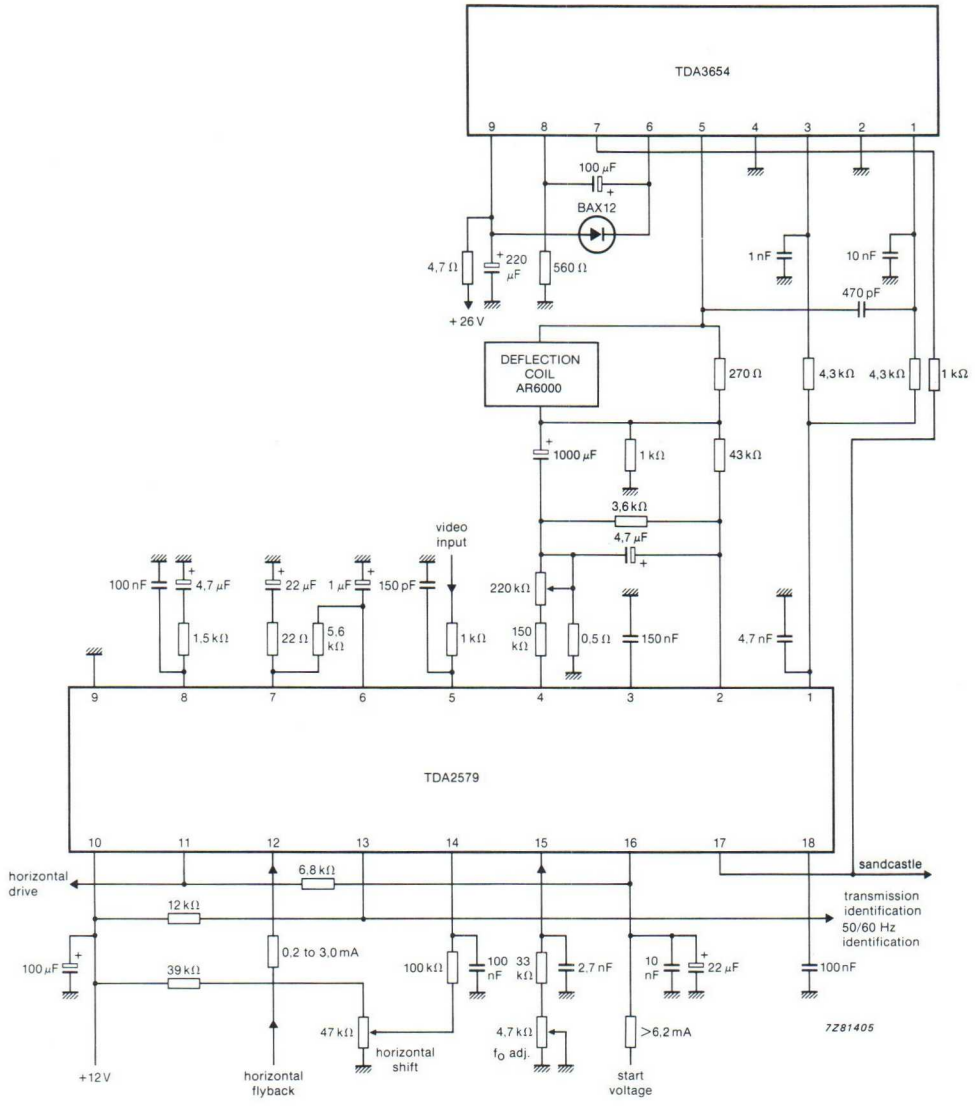


Fig. 6 Application diagram in combination with TDA2579.

PAL/NTSC/SECAM SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3755 is a monolithic integrated circuit for PAL/NTSC SECAM synchronization processing in VHS video recorders.

Features

- Adaptive sync separator
- Internal vertical sync pulse integrator
- Composite sync and vertical pulse output
- Current controlled oscillator (CCO) with 320/321 times horizontal frequency
- Horizontal phase detector with current output
- Video identification and mute circuit
- Burst gating pulse output (externally adjustable phase relationship)
- Test-picture output
- Subcarrier frequency output switched in phase in accordance with VHS standard
- Fast phase correction of subcarrier frequency
- Selection input to force PAL or NTSC function
- Still picture input

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-15}$	typ.	10 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	24 mA
Sync separator			
Sync pulse input voltage (peak-to-peak value)	$V_{3-15(p-p)}$	typ.	300 mV
Sync pulse output voltage (peak-to-peak value)	$V_{1-15(p-p)}$	min.	7,3 V
Vertical sync pulse			
Output voltage (peak-to-peak value)	$V_{18-15(p-p)}$	min.	2,7 V
Phase detector			
Catching range	Δf	min.	± 3,0 %
Oscillator			
Oscillator frequency			
PAL	f_{osc}	typ.	5,02 MHz
NTSC	f_{osc}	typ.	5,04 MHz
Output frequency			
PAL	f_o	typ.	627 kHz
NTSC	f_o	typ.	629 kHz
Output sinewave (peak-to-peak value)	$V_{8-15(p-p)}$	typ.	3 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

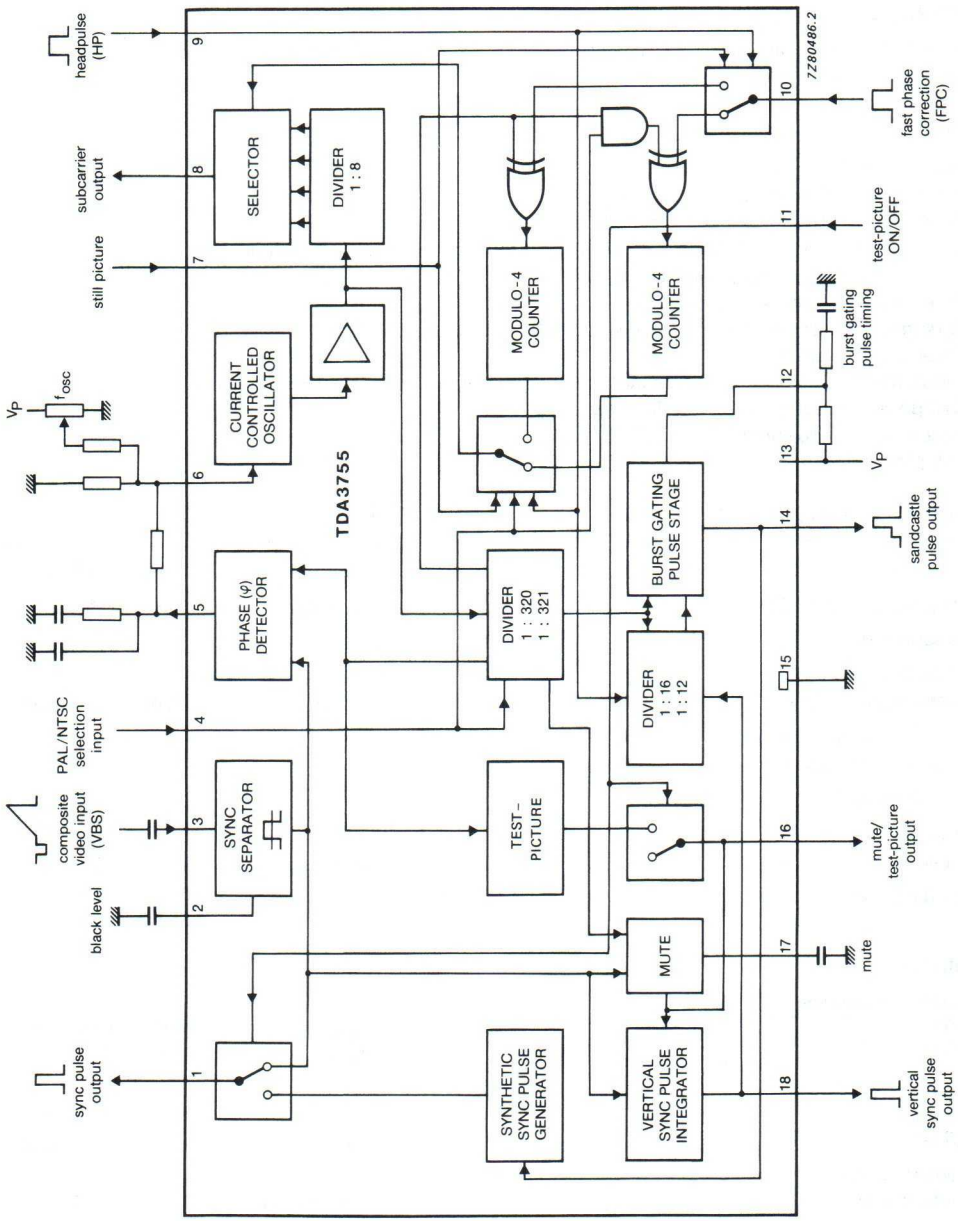


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-15}$	max.	13,2 V
Voltage range at pins 2, 3, 4, 7, 9, 10, 11, 17 to pin 15 (ground)	V_{n-15}		0 to V_P V
Voltage range at pin 12	V_{12-15}	min.	0 V
Voltage range at pin 6	V_{6-15}	max.	8 V
Currents			
at pins 1, 5, 8, 14, 16, 18	$\pm I_n$	max.	5 mA
at pin 6	$-I_6$	max.	1 mA
at pin 12	I_{12}	max.	2 mA
Total power dissipation	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-15}$	9,6	–	13,2	V
Supply current	$I_P = I_{13}$	–	24	–	mA
Sync separator (pin 3)					
Colour composite video input voltage (note 1) (peak-to-peak value)	$V_{3-15(p-p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{3-15(p-p)}$	75	–	600	mV
Slicing level, relative to sync pulse amplitude (note 2)		–	50	–	%
Internal resistance of video source	R_G	–	–	1	kΩ
Sync output voltage HIGH at $-I_1$ = 1 mA	V_{1-15}	7,8	–	–	V
Sync output voltage LOW at I_1 = 1 mA	V_{1-15}	–	–	0,5	V
Delay between signal at input pin 3 and sync pulse at output pin 1	t_d	–	0,2	–	μs
Vertical sync pulse (pin 18; note 3)					
Output voltage HIGH at $-I_{18}$ = 1 mA	V_{18-15}	2,7	–	5,0	V
Output voltage LOW at I_{18} = 1,6 mA	V_{18-15}	–	–	0,5	V
Duration of HIGH state of internally generated output pulse	t_p	–	190	–	μs
Delay between leading edge of input signal at pin 3 and leading edge of output pulse at pin 18	t_d	32	–	64	μs
Selection input (pin 4)					
Input voltage for NTSC state	V_{4-15}	–	–	0,3	V
Input current at V_{4-15} = 0 V	$-I_4$	–	–	20	μA
Input voltage for PAL state pin 4 open circuit or	V_{4-15}	2	–	–	V

parameter	symbol	min.	typ.	max.	unit
Test picture/mute/synthetic sync pulse					
Minimum voltage at pin 11 for test picture mode **active** (note 4)	$V_{11\text{-}15}$	4,8	–	–	V
Maximum voltage at pin 11 for test picture mode **inactive**	$V_{11\text{-}15}$	–	–	3,8	V
Output voltage at pin 16					
at test picture "black" or at mute	$V_{16\text{-}15}$	–	2,75	–	V
at test picture "white"	$V_{16\text{-}15}$	–	4,50	–	V
at "in sync condition"	$V_{16\text{-}15}$	–	–	0,5	V
Input current (pin 11)	$-I_{11}$	–	–	25	μA
Oscillator/phase detector					
Oscillator frequency (note 5)					
PAL	f_{osc}	–	5,02	–	MHz
NTSC	f_{osc}	–	5,04	–	MHz
Oscillator conversion gain	k_o	–	16,13	–	MHz/mA
D.C. control voltage	$V_{6\text{-}15}$	–	2,1	–	V
Input current for f = 5,016 MHz	$-I_{16}$	–	310	–	μA
Holding range (note 6)	Δf	± 3,2	–	–	%
Catching range (note 6)	Δf	± 3,0	–	–	%
Control loop gain	k_v	–	380×10^3	–	s^{-1}
Output of lower subcarrier (note 7) (peak-to-peak value)	$V_{8\text{-}15(p\text{-}p)}$	–	3	–	V
Output current	I_8	–	–	2	mA
D.C. output voltage	$V_{8\text{-}15}$	–	3,1	–	V
2nd harmonic suppression without switching	α_{2nd}	20	–	–	dB
Switching position prior to centre of sync pulse (pin 3)	t_s	–	2	–	μs
Output peak current of phase detector during sync pulse	$\pm I_5$	–	3,78	–	mA
Output voltage range (note 8)	$V_{5\text{-}15}$	1,4	–	2,8	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 14; note 9)					
Output voltage HIGH (note 10) at $-I_{14}$ = 1 mA	V_{14-15}	7,8	–	–	V
Output voltage INTERMEDIATE at $-I_{14}$ = 1 mA	V_{14-15}	2,3	3,0	3,7	V
Output voltage LOW at I_{14} = 1 mA	V_{14-15}	–	–	0,5	V
Lower part is starting prior to the centre of sync pulse at pin 3 and ending with the upper part	t_{14-3}	–	2,6	–	μs
Fast phase correction/head pulse					
Threshold voltage for fast phase correction (note 11)	V_{10-15}	–	7,2	–	V
Input current	$-I_{10}$	–	–	20	μA
Threshold voltage of head pulse input	V_{9-15}	–	1,4	–	V
Input current	$-I_9$	–	–	20	μA
D.C. input voltage	V_{7-15}	–	5,6	–	V
Input resistance	R_{7-15}	3	–	–	kΩ
Subcarrier phase switching (note 12)					
Phase switching of subcarrier phase in accordance with head pulse if	V_{7-15}	–	5,6*	–	V
LOW state of still picture input	V_{7-15}	–	–	0,5	V
Continuous phase switching regardless of head pulse if	V_{7-15}	–	V_P	–	V

* Or not connected.

Notes to characteristics

1. The sync separator input signal is shown in Fig. 2.

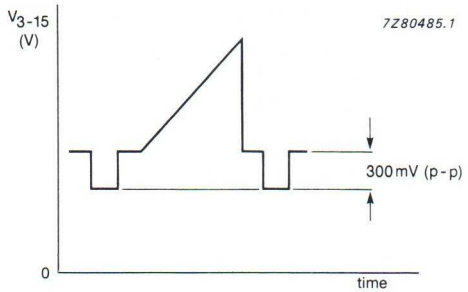
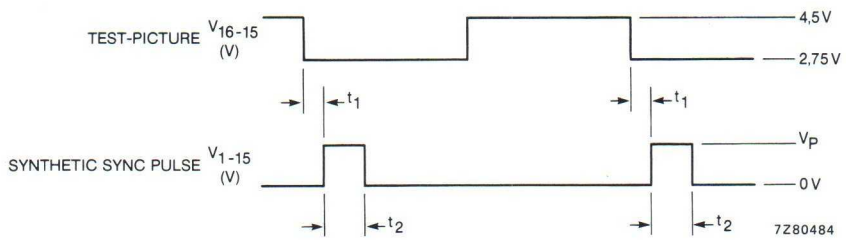


Fig. 2 Colour composite video input signal at pin 3.

2. The black level and the top sync level are detected internally and stored in capacitors at pin 2 and pin 3 respectively.
3. The vertical sync pulse output is disabled by mute.
4. In test picture mode the synthetic sync pulse is fed to output pin 1 and the vertical pulse consists of an uninterrupted block pulse of 192 μs triggering at every transition of head pulse (HP) at pin 9. The timing of test picture and synthetic sync pulse is shown in Fig. 3.



Where: The value of t_1 is dependent upon adjustment of the burst gating pulse delay.
Time t_2 is the burst gating pulse duration.

Fig. 3 Timing of test picture and synthetic sync pulse.

5. Oscillator adjustment during test picture mode made only, at $V_{11-15} > 4{,}8$ V, $V_{7-15} = 0$ V and $V_{4-15} > 2$ V or open circuit; measurement is $f_{osc}/8$ at output pin 8.
6. The holding range and catching range are both determined by the resistor connected between pin 5 and pin 6.
7. The phase of the lower subcarrier is switched in accordance with the VHS standard. PNP emitter follower, internal resistive load of 10 kΩ (typ.) to V_P.
8. The output voltage at pin 5 is disabled during test picture mode.

Notes to characteristics (continued)

9. The burst gating pulse is superimposed on an uninterrupted horizontal pulse. It is suppressed 16 times starting with every transition of the head pulse at pin 9. If a vertical pulse is detected during that time the burst gating pulses are additionally suppressed until line 12 and line 324 respectively. In any event the number of suppressed burst gating pulses is even.
10. The timing of the upper part of the sandcastle pulse is determined by the components connected to pin 12 (Fig. 4) and is independent of supply voltage variations.
11. The fast phase correction pulses have to be in the burst gating reference pulse. For any HIGH to LOW transitions of the correction pulse the phase is corrected by -90^{o} if the head pulse input is LOW and by $+90^{o}$ if the head pulse input is HIGH.
12. Subcarrier phase switching is detailed in Table 1.
    Subcarrier is 40,000 x f_H for NTSC state and 40,125 x f_H for PAL state.

Table 1 Subcarrier phase switching

still picture input	PAL		NTSC	
	HP = HIGH	HP = LOW	HP = HIGH	HP = LOW
HIGH	-90^{o}	-90^{o}	-90^{o}	-90^{o}
not connected	0^{o}	-90^{o}	$+90^{o}$	-90^{o}
LOW	0^{o}	0^{o}	$+90^{o}$	$+90^{o}$

APPLICATION INFORMATION

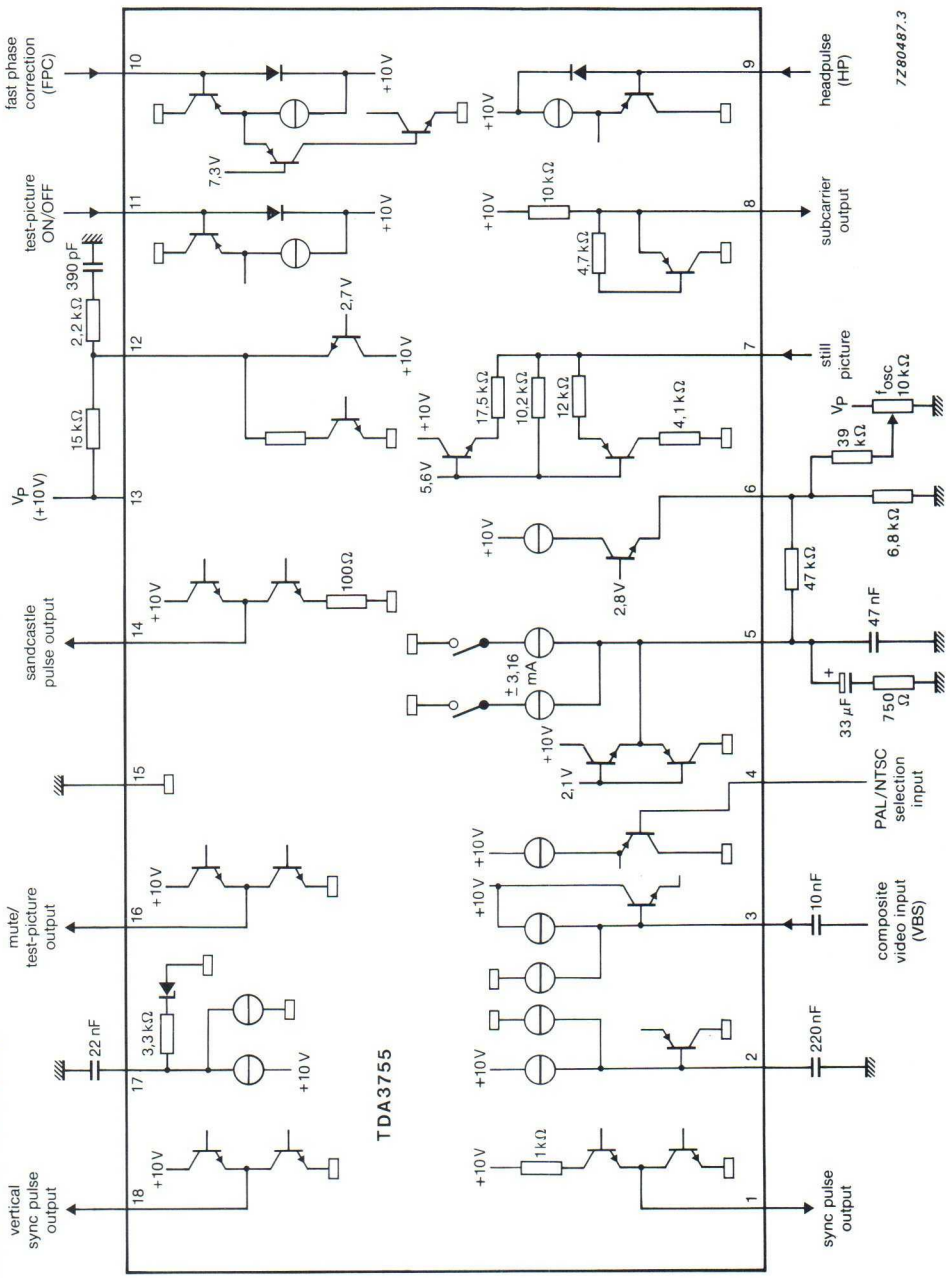


Fig. 4 Application circuit diagram.

BAND SELECTOR AND WINDOW DETECTOR

GENERAL DESCRIPTION

The TDA3791 is a monolithic integrated circuit intended for application in search-tuning systems for video recorders. It is designed to select one out of four tuners, each representing a particular band. Band selection tuning is indicated by a variable voltage V_{AFC}.

Features

- Voltage window detector
- Band switch selector
- 4 short-circuit protected band switches
- Muting circuit
- Delay circuit
- Short-circuit protection circuit
- Power-on reset

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	12 V
Supply current (pin 8)	$I_P = I_8$		
unloaded band switches ON		typ.	25 mA
all band switches OFF		typ.	12 mA
Power dissipation	P_{tot}	max.	1,8 W
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	0 to 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

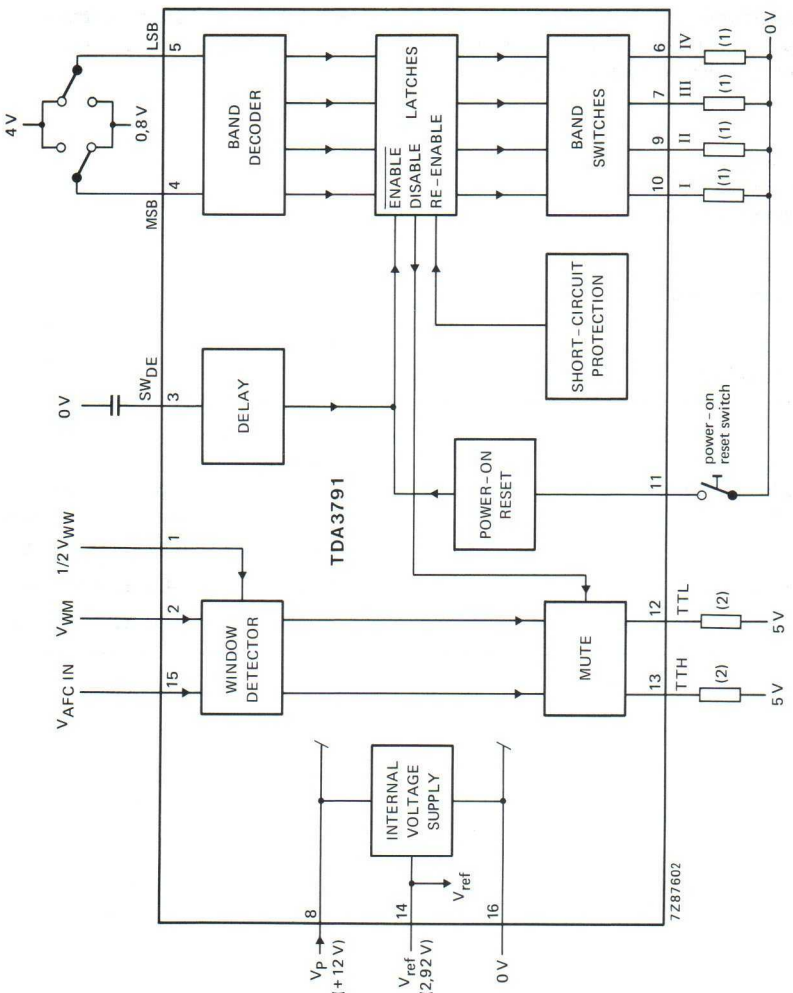


Fig. 1 Block diagram.

(1) $R = \frac{10\ V}{35\ mA}$. (2) $R = \frac{5\ V}{2\ mA}$.

FUNCTIONAL DESCRIPTION

Voltage window detector (see Table 1)

The voltage window is dependent upon two inputs; V_{WM} (pin 2) and $1/2V_{WW}$ (pin 1), which represent the centre of the window and the (window width)/2 respectively.

The voltage window range is from $V_{WM} - 1/2V_{WW}$ to $V_{WM} + 1/2V_{WW}$. A variable input voltage $V_{AFC\ IN}$ (pin 15) is compared with these window edges.

Table 1 Truth table; window detector

inputs	outputs	
$V_{AFC\ IN} = V_{15-16}$; $V_{WM} = V_{2-16}$; $V_{WW} = V_{1-16}$	V_{12-16}	V_{13-16}
$V_{AFC\ IN} < V_{WM} - 1/2V_{WW}$	HIGH	LOW
$V_{WM} - 1/2V_{WW} < V_{AFC\ IN} < V_{WM} + 1/2V_{WW}$	HIGH	HIGH
$V_{AFC\ IN} > V_{WM} + 1/2V_{WW}$	LOW	HIGH

Where: V_{12-16} = tuning too low (TTL); V_{13-16} = tuning too high (TTH).

During transitions of the outputs (V_{12-16} and V_{13-16}), a hysteresis value of approximately 20 mV is applied at the window edges.

Band-switch selector (see Table 2)

Selection of the band switches is determined by the input voltage levels of MSB (pin 4) and LSB (pin 5).

- If MSB or LSB $>$ 4 V, the input is HIGH
- If MSB or LSB $<$ 0,8 V, the input is LOW.

The band switches are selected as confirmed by Table 2.

Table 2 Truth table; band switch selector

MSB (V_{4-16})	LSB (V_{5-16})	switch	HIGH output
HIGH	HIGH	I	V_{10-16}
HIGH	LOW	II	V_{9-16}
LOW	HIGH	III	V_{7-16}
LOW	LOW	IV	V_{6-16}

Short-circuit protected band switches

A selected band switch has a minimum output voltage of $V_P - 0{,}3$ V provided the current is not more than 35 mA (I_{10}, I_9, I_7, I_6). If the output voltage at pins 10, 9, 7 or 6 is less than 9 V a short-circuit condition exists, and the output current will not be more than 80 mA. In this event the band switch is switched off, after an externally determined delay.

Muting

The muting circuit is active when a selected band switch is switched off. Both outputs TTL (pin 12) and TTH (pin 13) will then be LOW.

FUNCTIONAL DESCRIPTION (continued)

Delay circuit

After selection of a band switch, it will be in a conducting state. If after selection and a delay, the output voltage has not reached 9 V, the band is switched off. This delay is determined by an external capacitor on output SW_{DE} (pin 3).

Short-circuit protection

The short-circuit protection of each switch is provided by a flip-flop. If the condition of a band switch $V_o < 9$ V is detected, its flip-flop will be set and the band switch is switched off.

In the event of an incidental short-circuit to a band switch output, the band switch can be reset by applying 0 V to the power-on reset input (pin 11) or 0 V to the switch delay output SW_{DE} (pin 3).

Power-on reset

Before the voltage supply reaches 9,6 V, the short-circuit protection flip-flops are reset to enable the selection of a band switch.

The power-on reset circuit also supplies the voltage level for short-circuit detection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max. 13,2 V
Total power dissipation	P_{tot}	see Fig. 2
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range	T_{amb}	0 to +70 °C

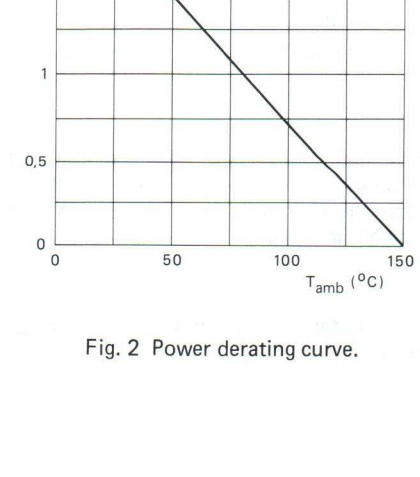


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = V_{8-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 8)	$V_P = V_{8-16}$	10	12	13,2	V
Supply current (pin 8)					
unloaded band switches ON	$I_P = I_8$	18	25	38	mA
all band switches OFF	$I_P = I_8$	9	12	16	mA
Voltage range					
$1/2V_{WW}$ (pin 1)	V_{1-16}	0,1	–	4,5	V
V_{WM} (pin 2)	V_{2-16}	1,8	–	10,5	V
$V_{WM} + 1/2V_{WW}$ at $V_{8-16} - 1{,}4$ V	$V_{2-16} \pm V_{1-16}$	1,7	–	10,6	V
$V_{AFC\ IN}$ (pin 15)	V_{15-16}	0,5	–	11,5	V
Input current					
$1/2V_{WW}$ (pin 1)	$-I_1$	–	–	2	μA
V_{WM} (pin 2)	I_2	–	–	0,2	μA
$V_{AFC\ IN}$ (pin 15)	I_{15}	–	0,2	0,4	μA
Hysteresis voltage V_{AFC}*	ΔV_{15-16}	–	20	50	mV
Delta current at $V_{AFC\ IN}$*	ΔI_{15}	–	–	25	nA
Temperature coefficient $I_{AFC\ IN}$	$TC(I_{15})$	–	–0,42	–	nA/°C
Temperature coefficient I_{WM}	$TC(I_2)$	–	–0,27	–	nA/°C
Deviation of applied voltage (pin 1)					
at $V_{1-16} = 100$ mV	ΔV_{1-16}	–35	–	+35	mV
at $V_{1-16} = 4{,}0$ V; $V_{2-16} = 6$ V	ΔV_{1-16}	–200	–	+200	mV
Input current (pin 4)					
at MSB $< 0{,}8$ V	I_4	–	–	0,1	μA
at MSB > 4 V	I_4	–	–	1,0	μA
Input current (pin 5)					
at LSB > 4 V	I_5	–	–	1,0	μA
at LSB $< 0{,}8$ V	I_5	–	–	0,1	μA
Voltage level (pin 4)					
at MSB HIGH	V_{4-16}	4	–	–	V
at MSB LOW	V_{4-16}	–	–	0,8	V
Voltage level (pin 5)					
at LSB HIGH	V_{5-16}	4	–	–	V
at LSB LOW	V_{5-16}	–	–	0,8	V
Short-circuit current of band switches I, II, III, IV (pins 10, 9, 7, 6)	$-I_{10, 9, 7, 6}$	35	50	80	mA
Voltage drop of band switches I, II, III, IV (pins 10, 9, 7, 6) at $I_{o(max)} = 35$ mA; $V_P = 10$ V	$V_{10, 9, 7, 6-16}$	–	–	0,3	V

* During switching of outputs V_{12-16} and/or V_{13-16}.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Voltage level short-circuit detection at $0{,}75V_P$	$V_{10, 9, 7, 6\text{-}16}$	8,0	9,0	9,5	V
Output voltage (pin 13) TTH at I_{13} = 2 mA (LOW)	$V_{13\text{-}16}$	–	–	0,3	V
Output voltage (pin 12) TTL at I_{12} = 2 mA (LOW)	$V_{12\text{-}16}$	–	–	0,3	V
Leakage current (pin 13) TTH at $V_{13\text{-}16}$ = 13,2 V	I_{13}	–	–	10	μA
Leakage current (pin 12) TTH at $V_{12\text{-}16}$ = 13,2 V	I_{12}	–	–	10	μA
Output current (pin 3) SW_{DE} at $V_{3\text{-}16}$ = 6 V	$-I_3$	5	12	20	μA
Maximum value of delay capacitor	C_3	–	–	40	nF
Maximum delay time at ± C_3 (nF)/(I_3/10) ms	t_d	–	–	50	ms
Power-on-reset voltage	$V_{8\text{-}16}$	6	–	9,6	V
Leakage current unswitched band switches at $V_{10, 9, 7, 6\text{-}16}$ = −12 V	$I_{10, 9, 7, 6}$	–	–	5	μA

STEREO/DUAL TV SOUND DECODER CIRCUIT

GENERAL DESCRIPTION

The TDA3803A is a stereo/dual TV sound decoder circuit with static switching for processing two AF signals in TV and VCR equipment. The LOW/HIGH static switching signals control the AF output selector. Two operational amplifiers perform bandpass filtering of the identification signals.

Features

- Amplification of the two AF input signals by integrated operational amplifiers
- Low distortion stereo de-matrix
- All operational amplifiers offset compensated
- De-emphasis with operational amplifiers, preferably applied to the output terminals
- Two output ports each with two channels for headphones and loudspeakers
- Dual sound information at one port, each port individually switchable from sound I to sound II and sound II to sound I
- Mute function; while mute is active, it is possible to connect an external mono AF input signal to pin 10 appearing at pins 20 to 23.
- Identification without additional signals (horizontal etc.)

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-12}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	28 mA
Pilot carrier amplifier gain control range	ΔG_v	>	40 dB
AF input signals; at G_v = 0 dB (r.m.s. value)	$V_{i(rms)}$	=	1 V
LED output current	I_{LED}	typ.	12 mA
Weighted signal-to-noise ratio of the a.f. signal switches (CCIR468/2)	(S+N)/N	⩾	60 dB
Crosstalk in stereo mode	α_S	>	40 dB
Crosstalk in dual sound mode	α_{DS}	>	60 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

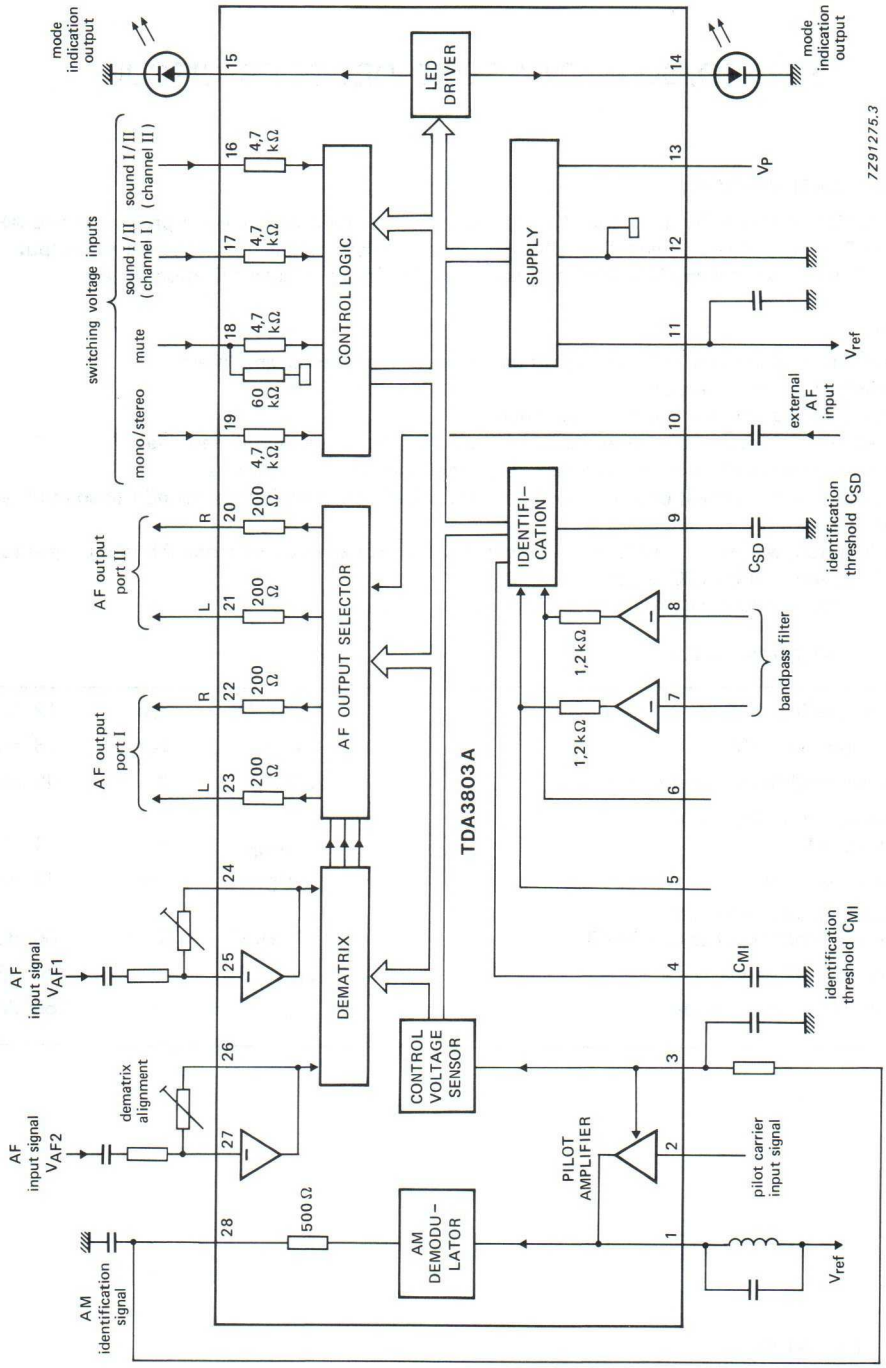


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-12}$	max.	14 V
Voltages with respect to pin 12 (ground)			
pins 25; 27 and 28	$V_{25;27;28-12}$	max.	V_P
Voltages			
pin 1 to pin 10	V_{n-12}	max.	V_P
pin 14 to pin 19	V_{n-12}	max.	V_P
Currents			
pin 11	I_{11}	max.	3 mA
pins 20; 21; 22; 23	$I_{20;21;22;23}$	max.	10 mA
pin 28	$-I_{28}$	max.	3 mA
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}		−25 to +125 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; overall voltage gain (G_v) = 1; ($R_S = R_R$); measured in Fig. 2 with a 1 kHz signal. AF input AF2 = AF1 = 0,5 V, pilot carrier input signal $V_{2\text{-}12(rms)}$ = 16 mV, m = 0,5 and with adjusted de-matrix circuit; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13\text{-}12}$	10,8	12	13,2	V
Supply current (without LED current)	$I_P = I_{13}$	–	28	35	mA
Reference voltage (pin 11)	V_{ref}	–	6	–	V
Input resistance (dynamic)	$R_{11\text{-}12}$	–	4	–	kΩ
AF part					
Amplification	G_v	–40	–	18	dB
Input signal at G_v = 1	$V_{AF1} = V_{AF2}$	–	–	1	V
Mono AF input signal (pin 10)*					
Input signal	$V_{10\text{-}12}$	–	–	2	V
DC input voltage level	$V_{10\text{-}12}$	–	6	–	V
Input resistance	$R_{10\text{-}12}$		16	–	kΩ
Stereo mode AF output port I pin 22: right pin 23: left					
AF output port II pin 20: right pin 21: left					
Output signal (THD ⩽ 0,5%)					
port I ($V_{23\text{-}12} = V_{22\text{-}12}$)	V_{oI}	–	–	2	V
port II ($V_{21\text{-}12} = V_{20\text{-}12}$)	V_{oII}	–	–	2	V
Weighted signal-to-noise ratio of the AF signal switches (in accordance with CCIR468/2)	(S+N)/N		65	–	dB
Unweighted signal-to-noise	(S+N)/N	60	–	–	dB
Total harmonic distortion ($V_{20;21;22;23\text{-}12}$ = 0,5 V; G_v = 1)	THD	–	0,05	–	%
Crosstalk attenuation (selective)					
stereo mode (f_1 = 1 kHz; f_2 = 400 Hz)	α_S	40	–	–	dB
dual sound mode (f = 250 Hz to 12,5 kHz)	α_{DS}	60	–	–	dB

* An input signal at pin 10 appears at pins 20 to 23 if the mute input (pin 18) is activated ($V_{18\text{-}12} \geqslant 2$ V).

parameter	symbol	min.	typ.	max.	unit
DC input voltage level at pins 25 and 27	$V_{25;27-12}$	–	6	–	V
DC output voltage level at pins 20; 21; 22 and 23	V_{n-12}	–	6	–	V
Output resistance at pins 20; 21; 22 and 23	V_{n-12}	–	200	–	Ω
Identification part					
Pilot carrier amplifier					
input signal (pin 2)	V_{2-12}	5	–	–	mV
gain control range	ΔG_V	40	–	–	dB
controlled output signal (pin 1) (peak-to-peak value)	$V_{1-12(p-p)}$	–	300	–	mV
Input resistance (pin 2)	R_{2-12}	–	60	–	kΩ
Output resistance (pin 1)	R_{1-12}	1	–	–	MΩ
DC input voltage level (pin 2) applied externally (see Fig. 2)	V_{2-12}	–	6	–	V
DC output voltage level (pin 28)					
without gain control	V_{28-12}	–	6	–	V
with gain control	V_{28-12}	–	7,9	–	V
Identification signal (pin 28) (peak-to-peak value)	$V_{28-12(p-p)}$	–	2,0	–	V
Filter operational amplifiers open loop gain	G_o	78	–	–	dB
Identification frequency evaluation					
No identification signal (lower threshold)	V_{4-12}	–	–	2,5	V
Identification signal (upper threshold)	V_{4-12}	4,7	–	–	V
Stereo transmission (lower threshold)	V_{9-12}	–	–	2,5	V
Dual sound transmission (upper threshold)	V_{9-12}	4,7	–	–	V
Control logic part					
Mute input voltage (pin 18)					
mute OFF	V_{18-12}	–	–	0,8	V
mute ON (see the remarks to pin 10)	V_{18-12}	2	–	–	V
Switching stereo/mono and sound I/sound II					
Stereo transmission					
switching voltage to pin 19 (pin 17 and 16 not affected)					
output ports I and II mono	V_{19-12}	–	–	0,8	V
output ports I and II stereo	V_{19-12}	2	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Control logic part (continued)					
Mono transmission both output ports I and II mono					
Dual sound transmission					
switching voltage to pin 16 (pin 19 and 17 not affected)					
output port II sound I	$V_{16\text{-}12}$	2	–	–	V
output port II sound II	$V_{16\text{-}12}$	–	–	0,8	V
switching voltage to pin 17 (pin 16 and 19 not affected)					
output port I sound I	$V_{17\text{-}12}$	–	–	0,8	V
output port I sound II	$V_{17\text{-}12}$	2	–	–	V
Mode indication (pins 14 and 15; see also Table 1)					
Output current	$-I_{14;\ 15}$	9	12	15	mA
Output voltage (note 2)	$V_{14;\ 15\text{-}12}$	0	–	8	V
Stereo/mono transmission: LED indication is valid for the transmission mode					
Dual sound transmission: LED indication is valid for port I					

Table 1 Mode indication (note 1)

transmission mode	LED pin 15	LED pin 14
mono	OFF	OFF
stereo:		
stereo selection; $V_{19\text{-}12} \geqslant 2$ V	ON	ON
mono selection; $V_{19\text{-}12} \leqslant 0{,}8$ V	ON	ON
dual sound:		
sound I selection; $V_{17\text{-}12} \leqslant 0{,}8$ V	ON	OFF
sound II selection; $V_{17\text{-}12} \geqslant 2$ V	OFF	ON

Notes to the characteristics

1. With mute (pin 18) ON both LEDs (pin 14 and 15) are switched OFF.
2. Pin 14 and 15 are also suitable as output switches to control TDA3810. At LED OFF and $I_{14,\ 15} \leqslant 100\ \mu A$, then $V_{14,\ 15\text{-}12} \leqslant 200$ mV.

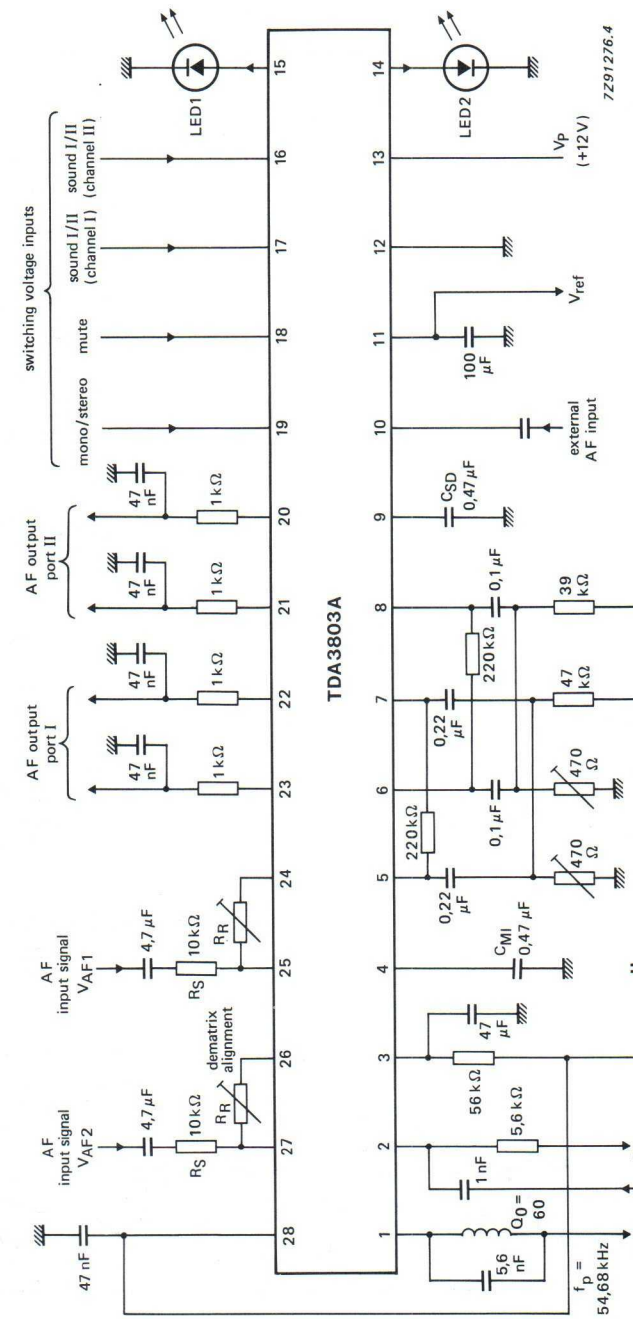


Fig. 2a Application diagram and test circuit; external components.

APPLICATION INFORMATION (continued)

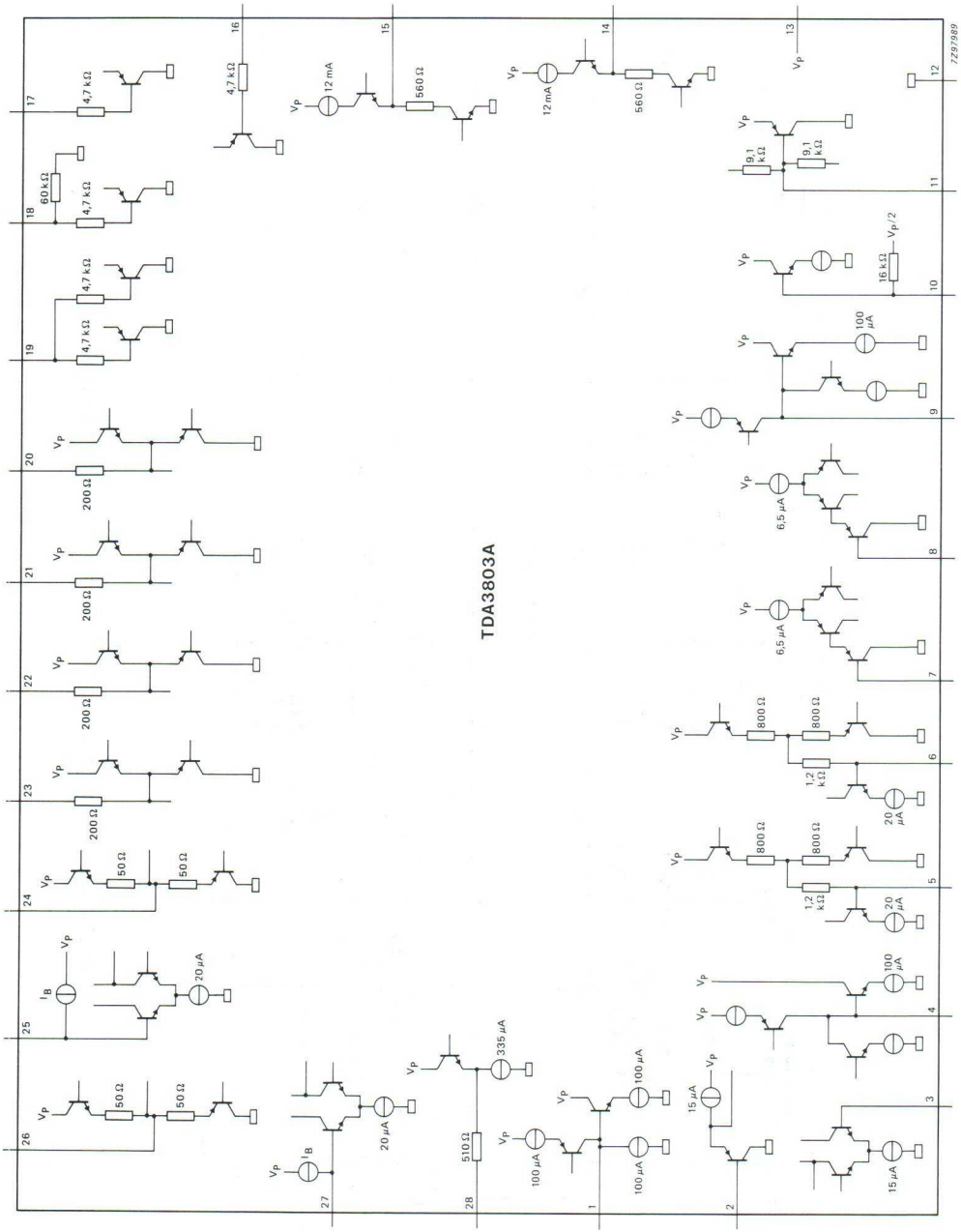


Fig. 2b Application diagram and test circuit; part of internal circuitry.

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

Features

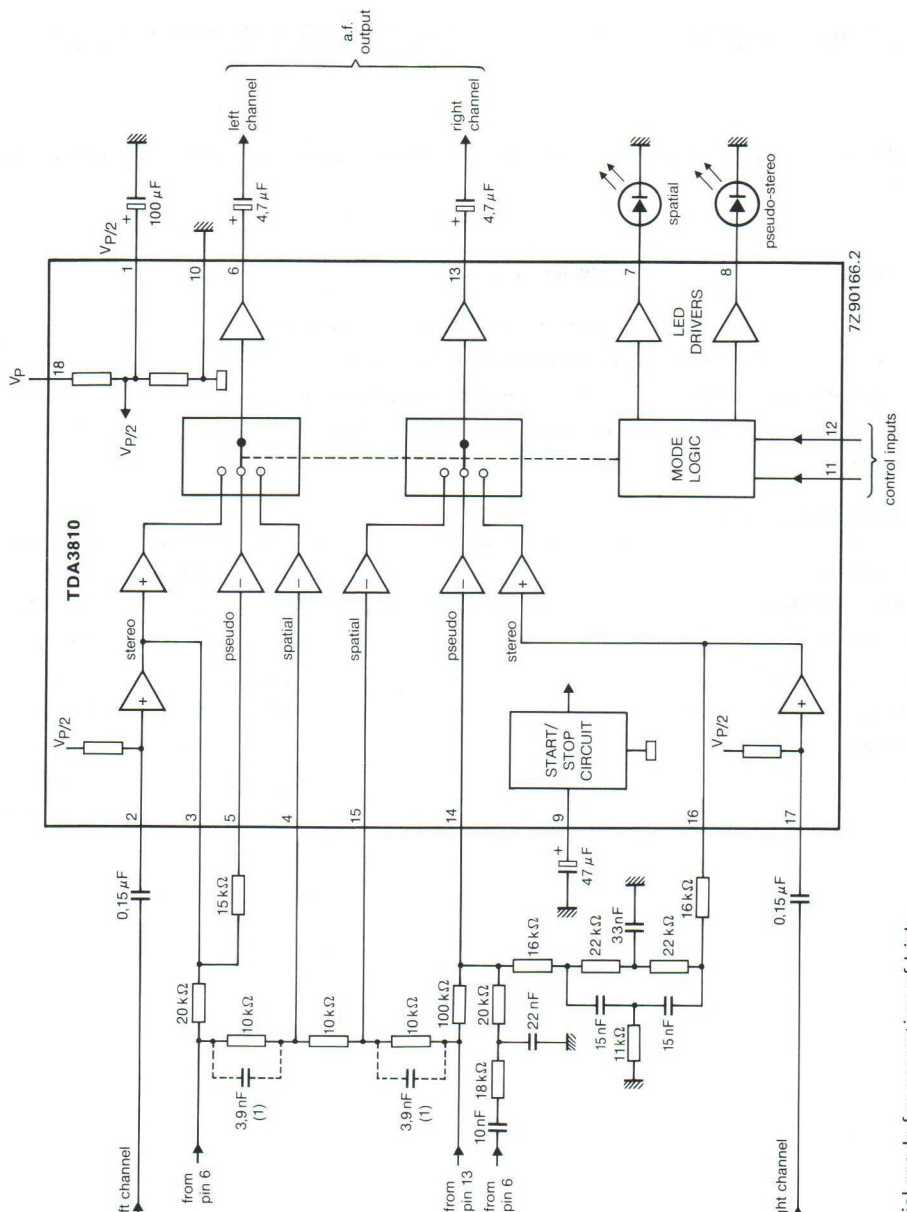
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_P	typ.	12 V
Supply current (LEDs off)	I_P	typ.	6 mA
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Input signal (r.m.s. value)	$V_{i(rms)}$	<	2 V
Total harmonic distortion (stereo)	THD	typ.	0,1 %
Channel separation (stereo)	α	typ.	70 dB
Gain (stereo)	G_v	typ.	0 dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	18 V
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10,\,13\text{-}10} \geqslant 4{,}7$ kΩ; $C_{6\text{-}10,\,13\text{-}10} \leqslant 150$ pF.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2% (stereo mode)	$V_{i(rms)}$	–	–	2	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH)					
Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	$-I_O$	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3825 is a single FM demodulator system with external AF input and mute.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- Multiple input AF operational amplifier with offset compensation
- External AF input
- High AF output voltage with low distortion
- AF gain of 0 dB without external components
- Frequency response can be determined by external components
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Source selector						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; V_u = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

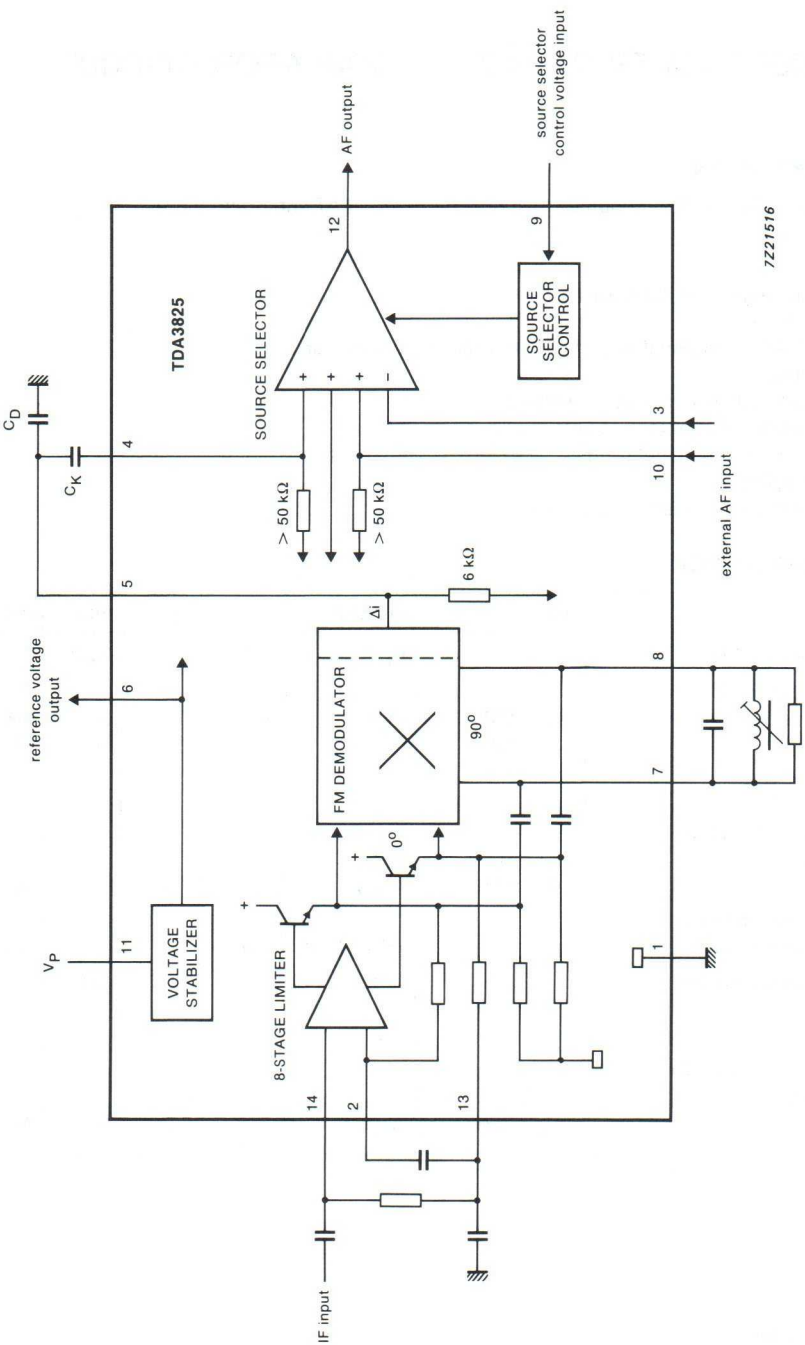


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)						
		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	15	–	–	kΩ
Input capacitance		C_{14-13}	–	–	6	pF
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Output impedance (pin 5)		$\lvert Z_{5-1} \rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz, V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ≤ 0.1%; V_u = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance (pin 4)		$\lvert Z_{4-1}\rvert$	50	–	–	kΩ
(pin 10)		$\lvert Z_{10-1}\rvert$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 6)		R_{3-6}	–	–	10	kΩ
(pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression for mute		α_{mute}	70	76	–	dB
Crosstalk attenuation		$\alpha_{4/10}$	64	70	–	dB
Offset voltage between any two source selector positions		V_{12-6}	–	–	50	mV
Source selector control	see Fig.3					
Source coltrol voltage (pin 9)						
Mute active input voltage		V_{9-1}	0	–	1/3 V_P−1	V
input current		I_9	10	–	500	μA
Input 1 active (pin 4) input voltage		V_{9-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_9	−200	–	+200	μA
Input 2 active (pin 10) input voltage		V_{9-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_9	−600	–	−40	μA
Input voltage at pin 9 for I_9 = 0 μA		V_{9-1}	–	$\frac{V_P-0.7}{2}$	–	V
Reference source (pin 6)						
Reference voltage input		V_{ref}	2.17	2.27	2.37	V
Output current		$\lvert I_6\rvert$	–	250	–	μA

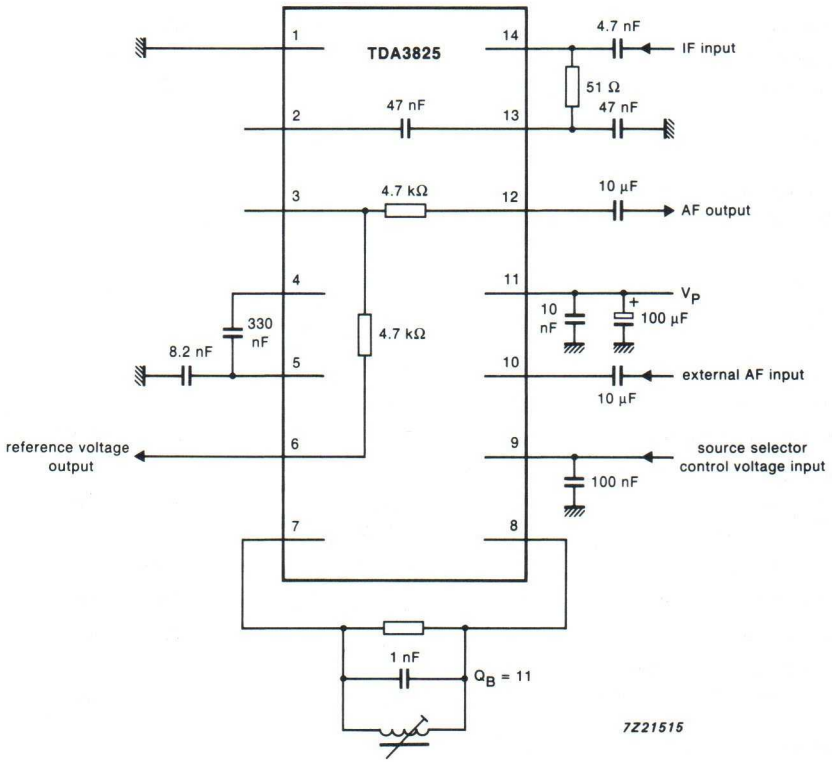


Fig. 2 Test circuit.

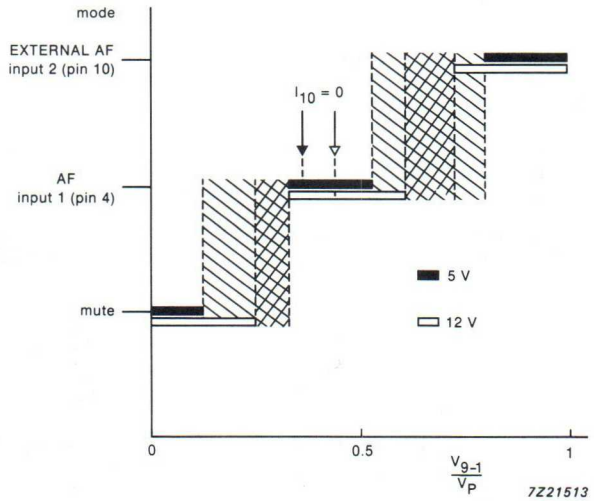


Fig. 3 Source selector logic diagram.

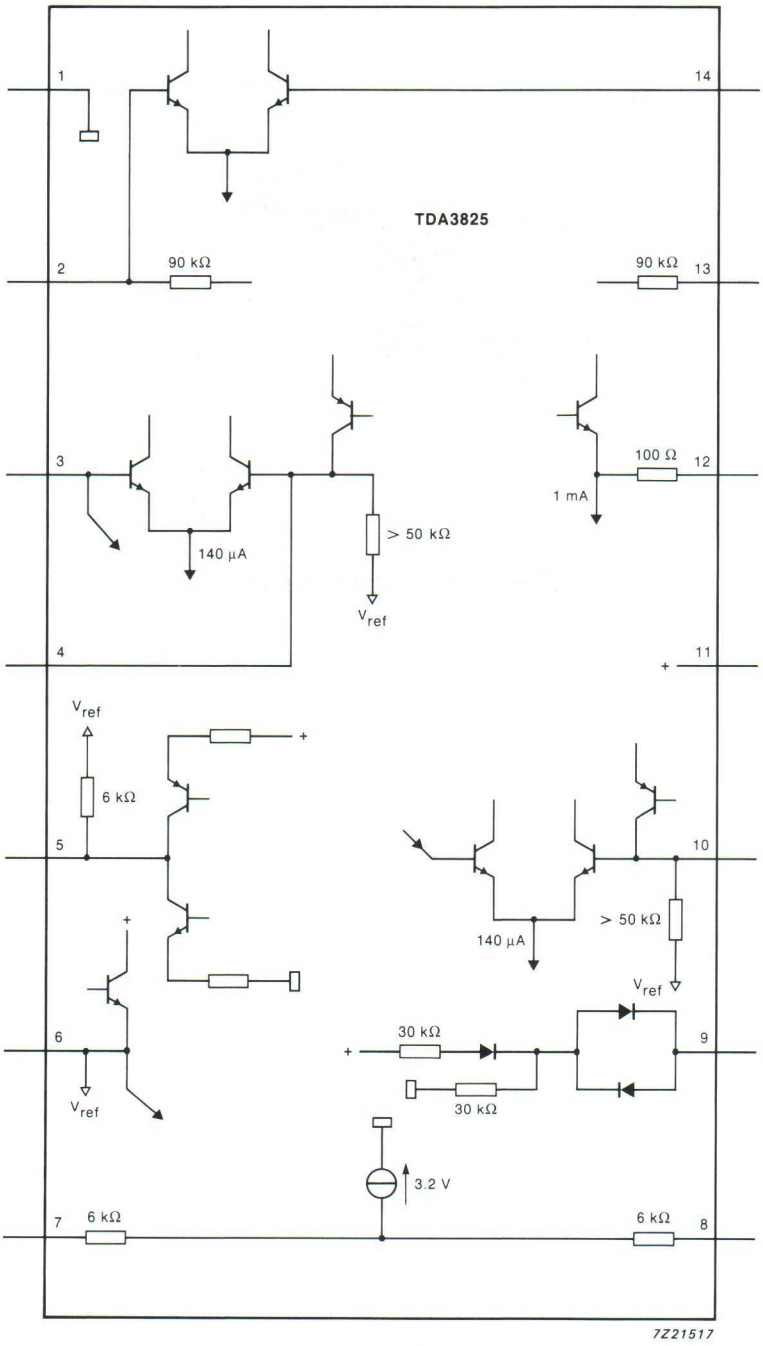


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

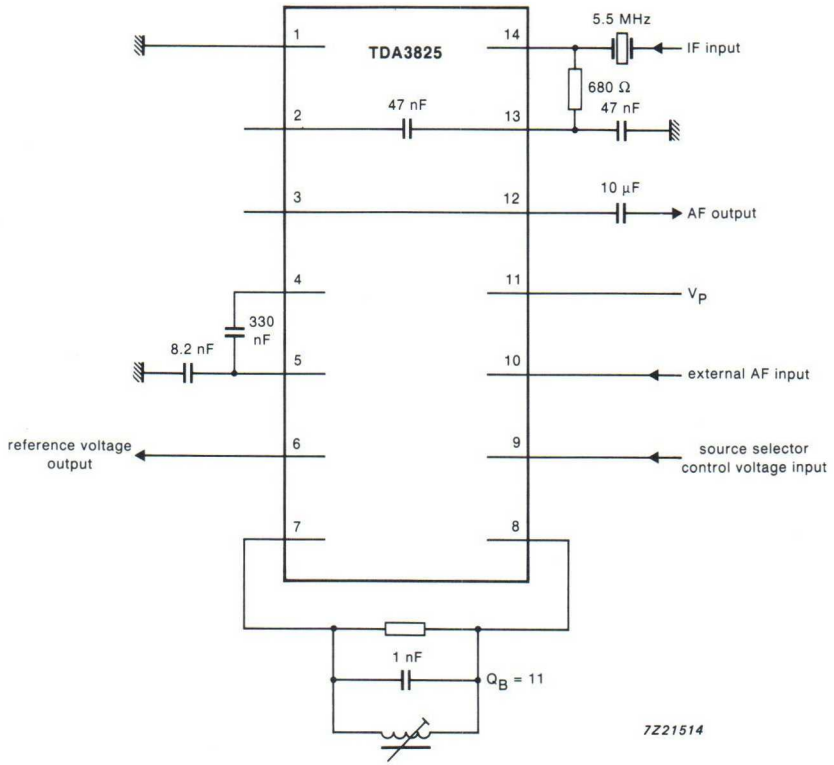


Fig. 5 Application diagram.

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3826 is a single FM demodulator system with mute and 6 dB AF amplifier.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- AF operational amplifier output with offset compensated input stage
- High AF output voltage with low distortion
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	–	%
AF switch						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; G_V = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

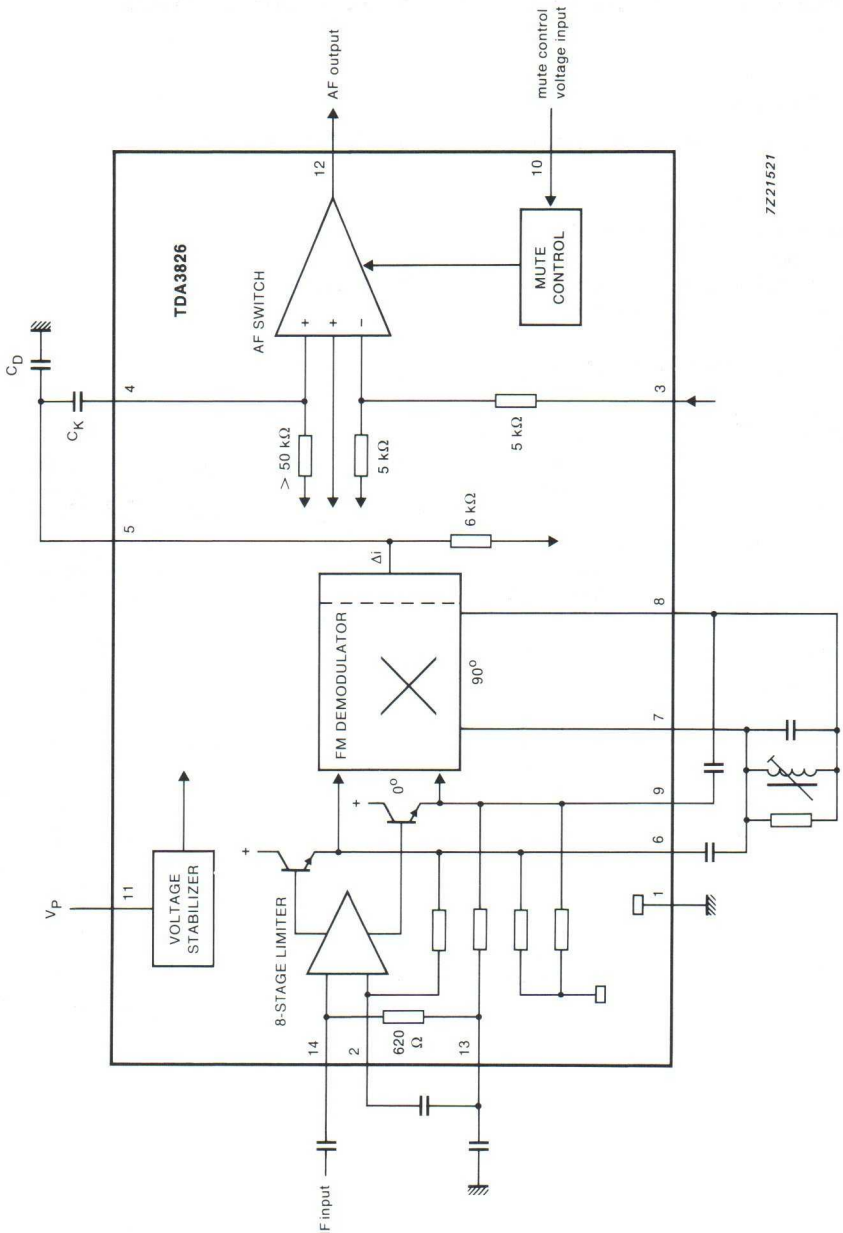


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)						
		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	–	620	–	Ω
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output impedance (pin 5)		$\lvert Z_{5-1} \rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz; V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
AF switch (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ≤ 0.1%; G_V = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance						
(pin 4)		$\|Z_{4-1}\|$	50	–	–	kΩ
(pin 10)		$\|Z_{10-1}\|$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression in case of mute		α_{mute}	70	76	–	dB
Mute control	see Fig. 3					
Mute control voltage (pin 10)						
Input (pin 4) active						
input voltage		V_{10-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_{10}	−200	–	+200	μA
Mute active						
input voltage		V_{10-1}	0	–	1/3 V_P−1	V
input current		I_{10}	10	–	500	μA
input voltage		V_{10-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_{10}	−600	–	−40	μA
Input voltage at pin 10 for I_{10} = 0 μA		V_{10-1}	–	$\frac{V_P-0.7}{2}$	–	V

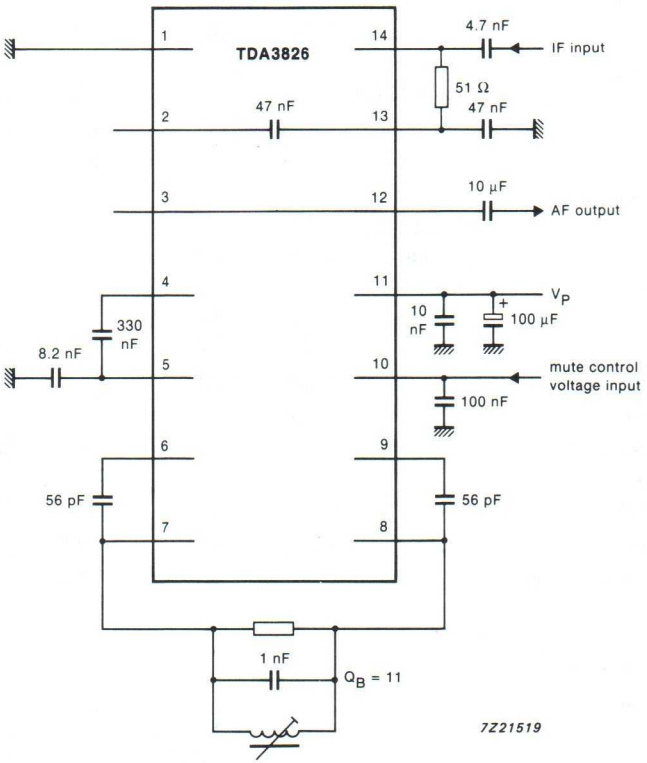


Fig. 2 Test circuit.

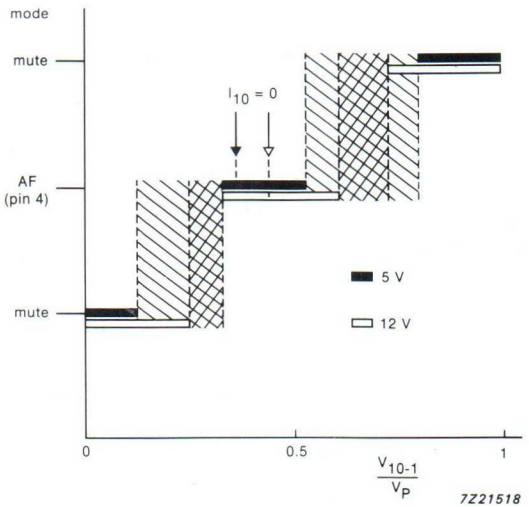


Fig. 3 Mute control logic diagram.

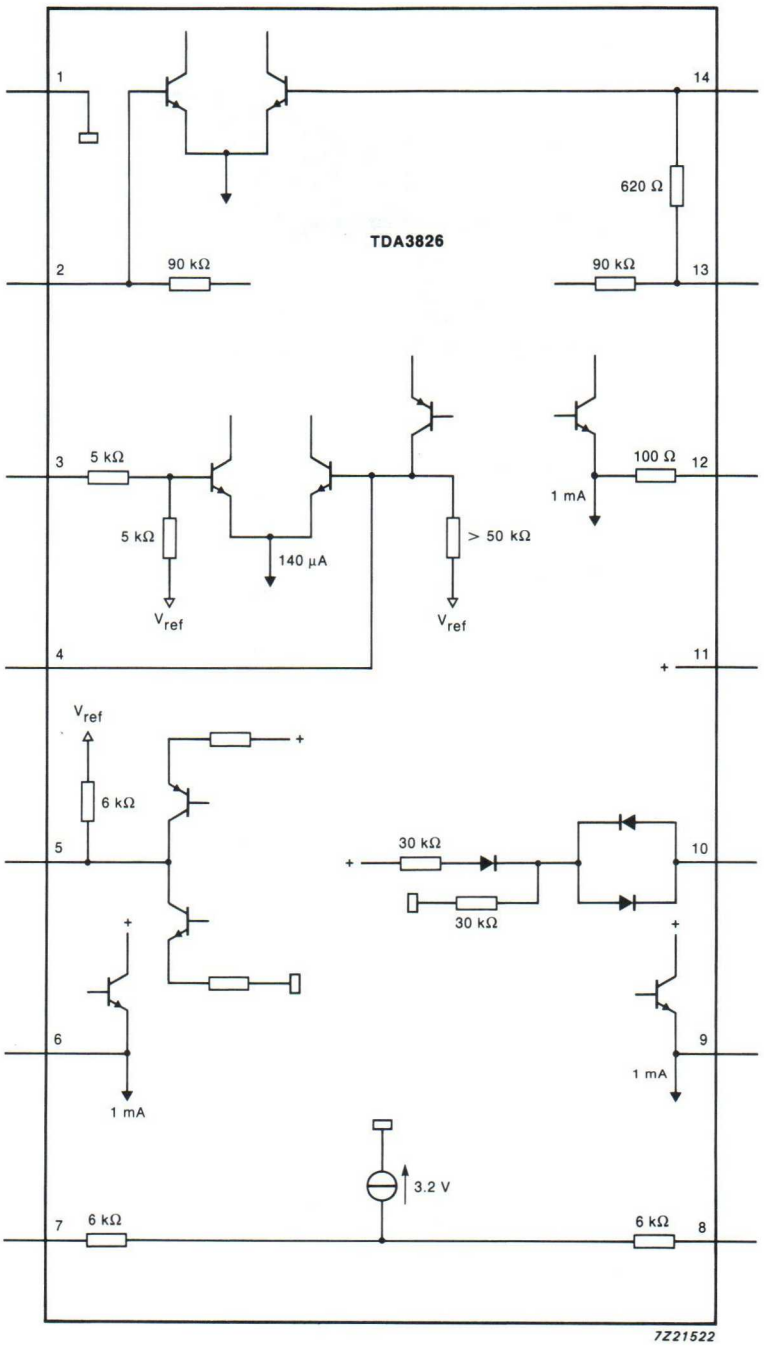


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

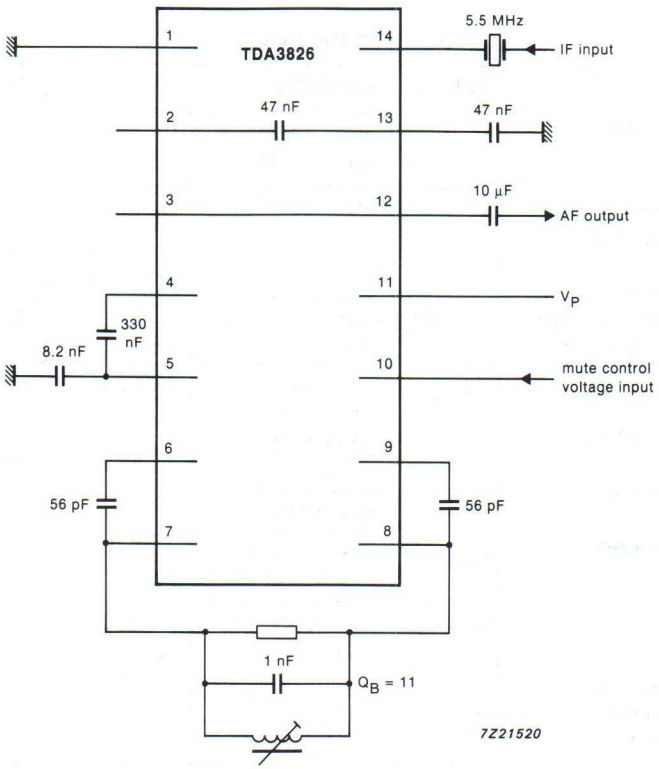


Fig. 5 Application diagram.

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA3827

TV-sound demodulator circuit with SCART switches and AF control

FEATURES

- Wide supply voltage range from 4.5 V to 13.2 V
- Wide frequency range from 4 to 12 MHz
- High ripple rejection
- High precision and temperature compensated FM-demodulator output
- Multiple-input AF operational amplifiers with offset compensation
- SCART AF input / AF output (low impedance)
- External AF input
- High-level AF output voltage with low distortion
- External selection of the source selector AF gain
- Low switching noise between AF and mute
- Wide volume-control range

GENERAL DESCRIPTION

The TDA3827 contains a single FM demodulator with SCART switches, a mute function and volume control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5 V	–	26	–	mA
		V_P = 12 V	–	28	–	mA
(S+N)/N	signal to weighted noise		73	78	–	dB
$V_{5(rms)}$	FM demodulator output voltage (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	450	500	550	mV
$V_{13(rms)}$	SCART output signal (RMS value)		–	1.0	–	V
G_v	volume control range		80	85	–	dB
$V_{17(rms)}$	AF output signal (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	–	1.0	–	V
THD	total harmonic distortion (pin 17)		–	0.5	–	%

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3827	18	DIL	plastic	SOT102

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

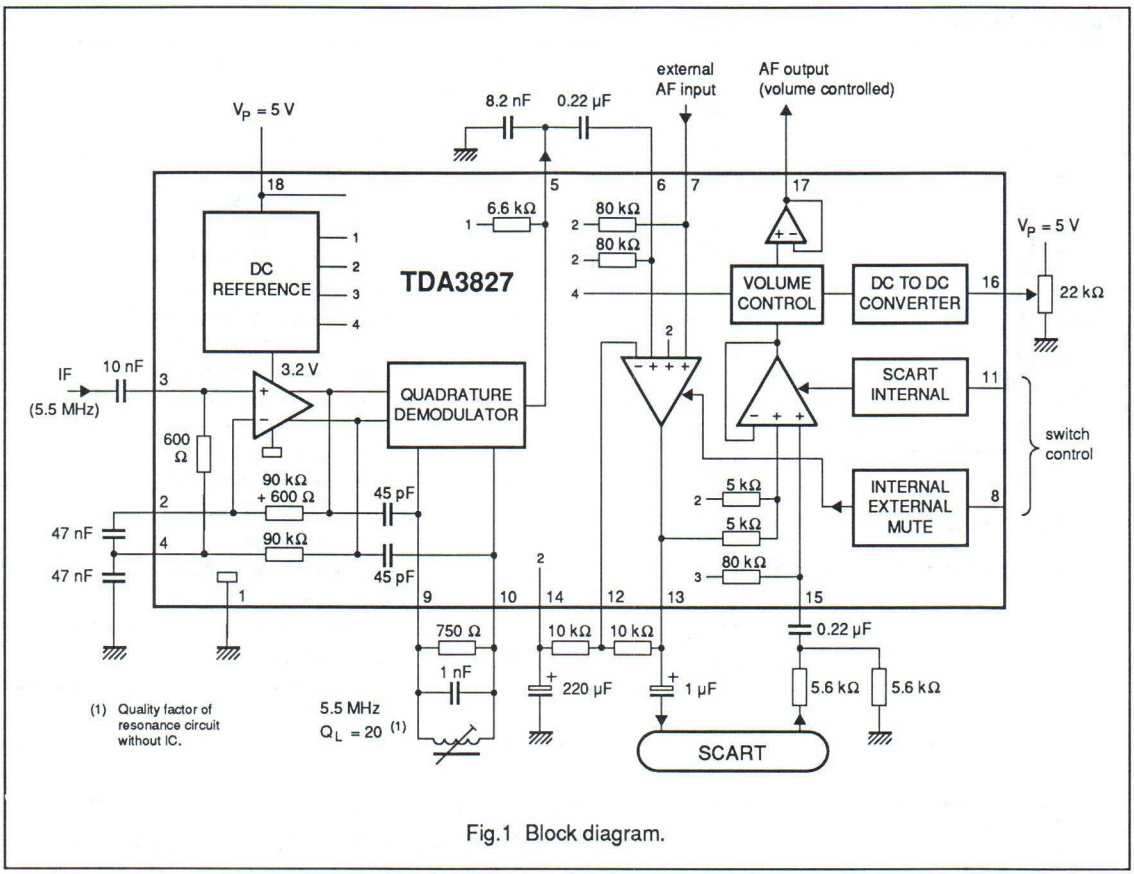


Fig.1 Block diagram.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

PIN CONFIGURATION

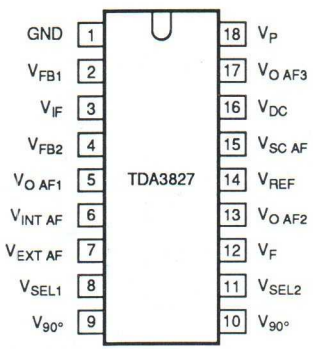


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{FB1}	2	limiter amplifier feedback
V_{IF}	3	FM IF input signal
V_{FB2}	4	limiter amplifier feedback
$V_{O\ AF1}$	5	AF output signal
$V_{INT\ AF}$	6	internal AF input signal
$V_{EXT\ AF}$	7	external AF input signal
V_{SEL1}	8	selection voltage for internal / external AF input and mute
$V_{90°}$	9	} quadrature demodulator
$V_{90°}$	10	} tuned circuit reference
V_{SEL2}	11	selection voltage for internal / external or SCART audio
V_F	12	source selector feedback
$V_{O\ AF2}$	13	output signal to SCART
V_{REF}	14	reference voltage
$V_{SC\ AF}$	15	input signal from SCART
V_{DC}	16	DC volume control voltage
$V_{O\ AF3}$	17	AF output signal from volume control
V_P	18	supply voltage

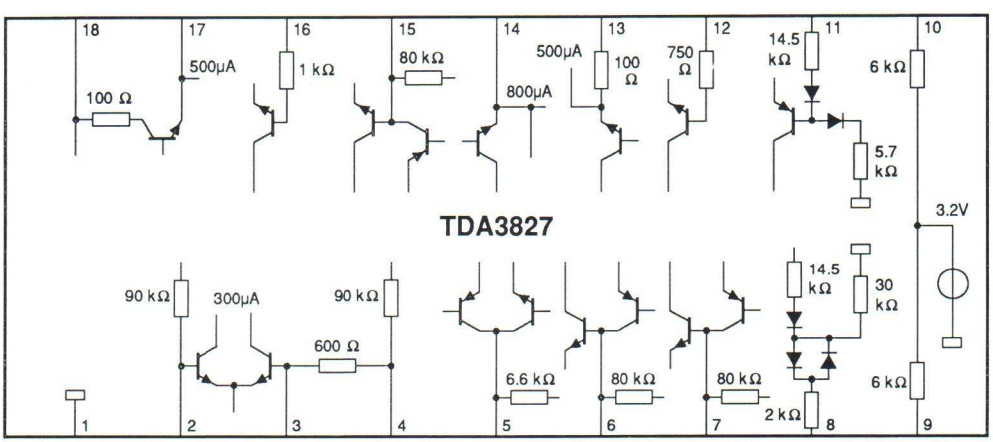


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	–0.5	V_P + 6.8	V
V_{ext}	external voltage (pins 2 to 10, 12 to 15 and 17)	–0.3	V_P – 0.7	V
	external voltage at pin 11	–0.3	13.2	V
	external voltage at pin 16	–0.3	V_P	V
R_L	external DC load resistance (pin 13 and pin 17)	5.0	–	kΩ
C_L	capacitive output load (pin 13 and pin 17)	–	1500	pF
P_{tot}	total power dissipation	–	450	mW
T_{stg}	storage temperature range	–40	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD-protection (note 1)	± 2000	–	V

Note to the limiting values

1. Measured with a 100 pF capacitor in series with a 1.5 kΩ resistor.

CHARACTERISTICS

All voltages are measured to GND (pin 1); V_P = 5 V; V_{IF} = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5.0 V	–	26	30	mA
		V_P = 12.0 V	–	28	32	mA
V_{14}	reference voltage		2.2	2.3	2.4	V
I_{14}	output current		–	± 250	–	μA
IF limiting amplifier						
$V_{i(rms)}$	input signal at pin 3 (RMS value)		–	–	200	mV
		3 dB below nominal AF level at pin 5	–	30	50	μV
R_{3-1}	input resistance		–	600	–	Ω
$V_{2,3,4}$	DC voltage		–	2.1	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator (Q_L = 20)						
$V_{5(rms)}$	AF-output signal (RMS value)		450	500	550	mV
	residual $2f_o$-signal (RMS value)	without de-emphasis	–	–	30	mV
TC	temperature coefficient (pin 5)		–	1	2	mV/K
α_{AM}	AM suppression	f_{AM} = 400 Hz, m = 0.3, $V_{i(rms)}$ = 500 µV; Fig.8	50	62	–	dB
THD	total harmonic distortion	see Fig.8	–	0.3	0.5	%
Z_o	output impedance (pin 5)		–	6.6	–	kΩ
B_{AF1}	small signal bandwidth (pin 5)	at –1 dB; without de-emphasis	100	–	–	kHz
(S+N)/N	signal to weighted noise ratio	CCIR468-3, DIN45405; see Fig.8	73	78	–	dB
RR	ripple rejection	f_R = 70 Hz, V_R = 100 $mV_{(p-p)}$	30	35	–	dB
$V_{9,10}$	DC voltage		–	3.2	–	V
Source selector						
$V_{i\ 6,7(rms)}$	input signal (RMS value)		–	500	1000	mV
$Z_{6,7}$	input impedance		50	80	–	kΩ
G_o	open loop gain		–	60	–	dB
$G_{13/6,7}$	gain	see Fig.4	–	0	–	dB
	gain (typical application)	see Fig.1	–	6	–	dB
V_{13}	DC voltage		–	2.3	–	V
I_{13}	DC output current		–	–	1.0	mA
Z_{13}	output impedance dynamic		–	–	10	Ω
C_L	capacitive output load (pin 13)		–	–	1500	pF
$V_{13(rms)}$	output signal (RMS value)	handling THD < 0.1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	20	–	µV
B_{AF2}	small signal bandwidth	at –1 dB	100	–	–	kHz
dV/dt	slew rate (pin 13)		1	–	–	V/µs
ΔV_{13}	offset-voltage between any two source selector positions		–	5	20	mV
α_{mute}	AF suppression at mute		80	90	–	dB
$\alpha_{7/6}$	crosstalk attenuation		70	76	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source selector control (see Fig.5)						
V_8	voltage for internal selection of AF-input (pin 6)		1/3 V_P	–	2/3 V_P –0.7	V
I_8	selection input current		–	–	200	µA
V_8	voltage for external selection of AF-input (pin 7)		2/3 V_P +0.7	–	V_P	V
I_8	selection input current		40	–	600	µA
V_8	voltage for mute active		0	–	1/3 V_P – 1	V
I_8	input current		–10	–	–500	µA
SCART switch and level control						
$V_{15(rms)}$	AC input signal (RMS value)		–	500	1000	mV
Z_{15}	input impedance		50	80	–	kΩ
G_{17-15}	voltage gain	V_{16} = 4.1 V	–1.5	0	+ 1.5	dB
G_{max}	maximum voltage gain	V_{16} = 5.0 V	+ 4.0	+ 5.0	+ 6.0	dB
ΔG_V	volume control range	see Fig.7	80	86	–	dB
V_{17}	DC voltage		–	2.3	–	V
I_{17}	DC output current		–	–	–1	mA
Z_{17}	dynamic output impedance		–	–	10	Ω
C_L	capacitive output load (pin 17)		–	–	1500	pF
$V_{17(rms)}$	output signal (RMS value)	THD ≤ 1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	100	–	µV
B_{AF3}	small signal bandwidth (pin 17)	at –3 dB	50	100	–	kHz
THD	distortion (pin 17)	at maximum gain	–	0.5	1.0	%
ΔV_{17}	offset voltage between internal and SCART		–	5	20	mV
V_{16}	control voltage	minimum gain –80 dB; see Fig.7	0.7	1.0	–	V
I_{16}	control current		–	–	50	µA
$\alpha_{6,7/15}$	crosstalk attenuation between IF-stage and control-stage	IF sound modulated; SCART switch on; source-selector on position input 1	80	90	–	dB
SCART switch control (see Fig.6)						
V_{11}	voltage for internal active		0	–	4/5 V_P –3	V
I_{11}	current		0	–	–100	µA
V_{11}	voltage for SCART active		4/5 V_P –1	–	13.2	V
I_{11}	current		$\frac{V_{11} - 1.4}{20.000}$	–	700	µA

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

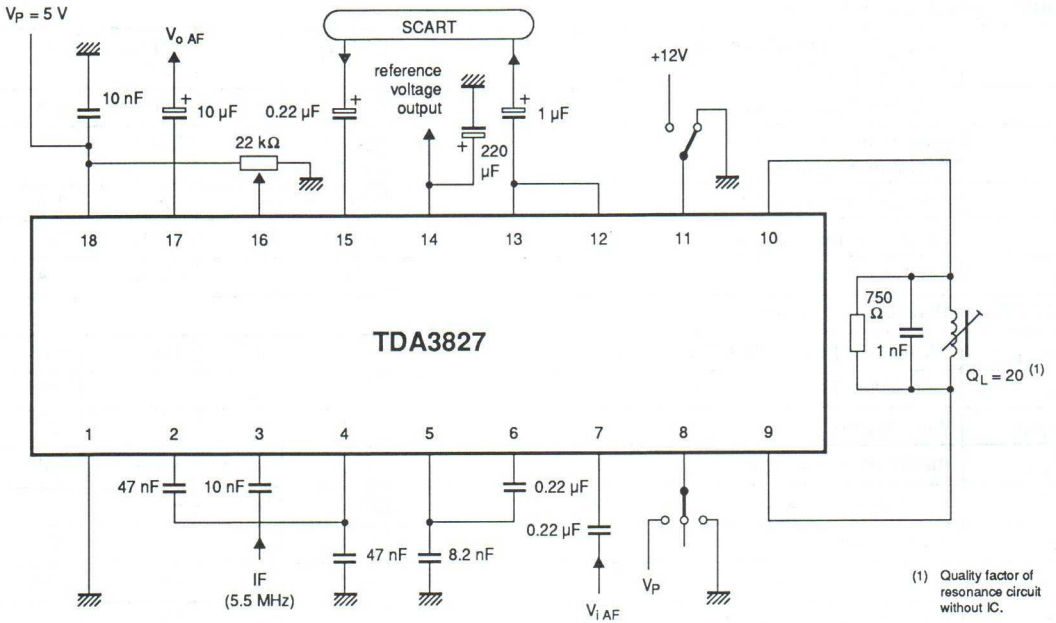


Fig.4 Test circuit.

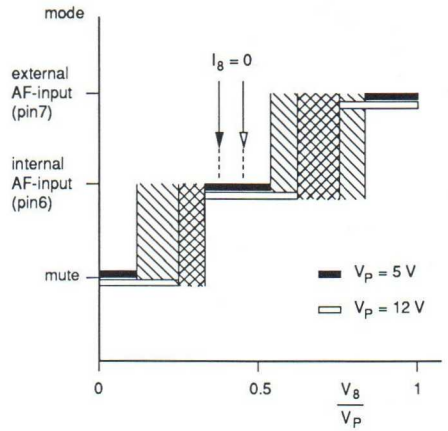


Fig.5 Source selector switching levels.

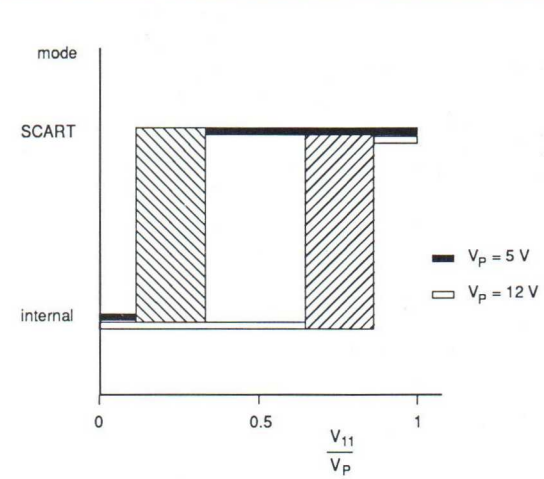


Fig.6 SCART switching levels.

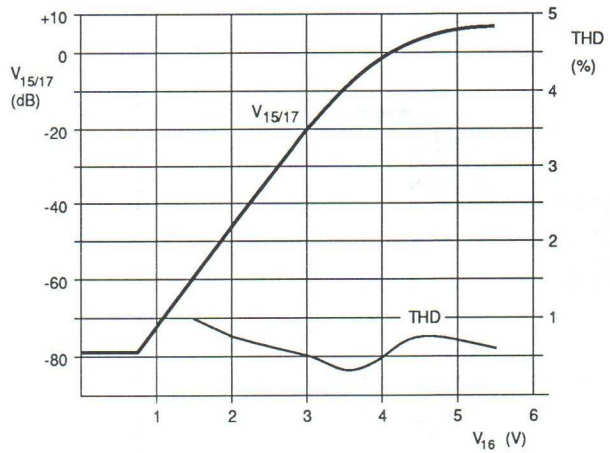


Fig.7 Volume control diagram.

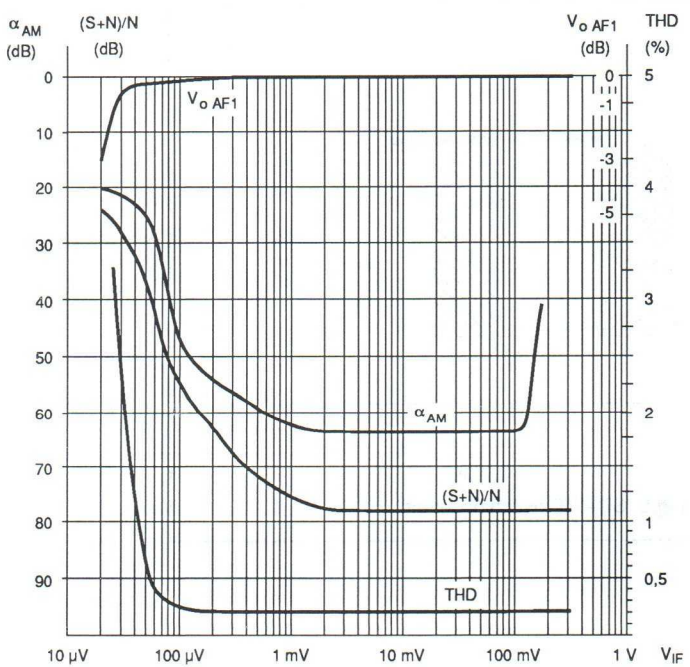


Fig.8 AF output voltage at pin 5, THD, (S+N)/N in accordance with to CCIR468-3 and AM suppression α_{AM} as functions of IF input voltage V_{IF} at pin 3.

BTSC-stereo/SAP/DBX decoder and DBX expander

TDA3833

FEATURES

- DBX decoder, MPX decoder and SAP decoder on chip
- Extensive switching possibilities for the AF outputs and the extra headphone output
- Stereo and SAP signal available simultaneously
- Reliable stereo/SAP identification by means of the noise detector
- Integrated filters
- DAC control possible for most alignments
- Few external components
- Low power consumption (200 mW)
- +5 V supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	UNIT
V_P	positive supply voltage (pin 32)	5	V
I_P	supply current	42	mA
V_i	input signal, 100% modulated, mono (RMS value, pin 1)	100	mV
V_o	AF output signal (RMS value, pins 7, 23 and 24)	550	mV
S/N(W)	signal-to-noise ratio, weighted	50	dB
S/N	signal-to-noise ratio	60	dB
α_{CH}	stereo channel separation	26	dB
α_{CR}	crosstalk attenuation	60	dB
THD	total harmonic distortion	0.2	%

GENERAL DESCRIPTION

The TDA3833 is a sound processor for stereo/second audio program (SAP) baseband signals in accordance with the BTSC standard for television receivers and video tape recorders.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3833	32	SDIL	plastic	SOT232AG
TDA3833T	32	SO	plastic	SOT287AH

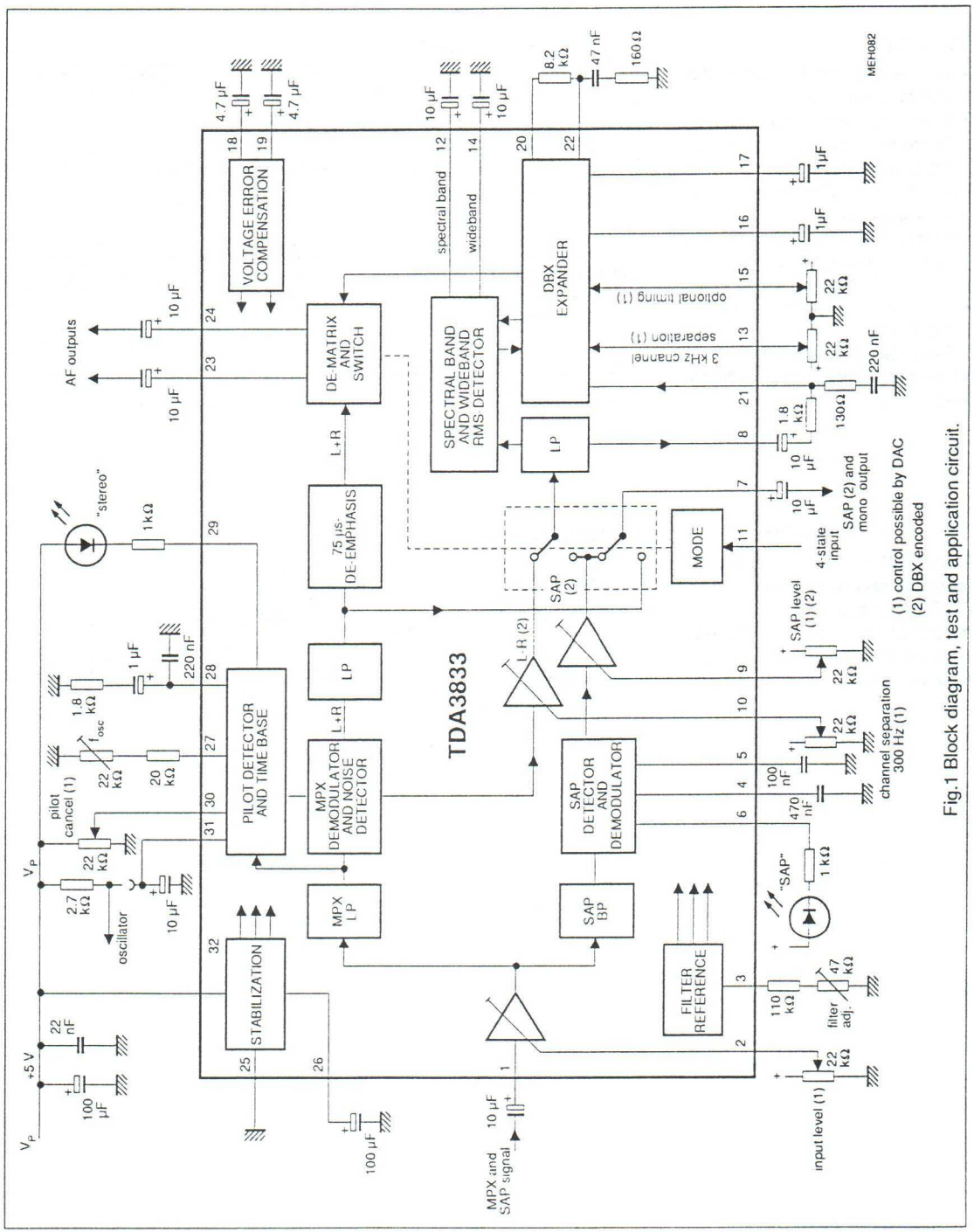


Fig.1 Block diagram, test and application circuit.

BTSC-stereo/SAP/DBX decoder and DBX expander

TDA3833

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	composite input signal (MPX/SAP)
ILV	2	input level control
f_{ref}	3	adjustment of filter reference
C_{SAP}	4	SAP identity smoothing capacitor
C_{ND}	5	SAP noise detector smoothing capacitor
SAPI	6	SAP indicator output (sink)
$V_{o\,HP}$	7	SAP/mono headphone output
$V_{o\,SAP}$	8	output signal SAP/(L – R) without DBX
SAPLV	9	SAP level control
LRLV	10	(L – R) level control
MODE	11	4-state mode control
$C1_{SPB}$	12	spectral band timing capacitor
DBXLV	13	DBX spectral adjust
$C1_{WB}$	14	wideband timing capacitor
DBXT	15	DBX timing adjust
$C2_{SPB}$	16	spectral RMS-detector smoothing capacitor
$C2_{WB}$	17	wideband RMS-detector smoothing capacitor
$C1_{DC}$	18	DC decoupling capacitor 1 for offset compensation
$C2_{DC}$	19	DC decoupling capacitor 2 for offset compensation
EMPH1	20	time constant for variable emphasis
DBXIN	21	DBX signal input
EMPH2	22	time constant for variable emphasis
V_{oAF1}	23	AF output signal right/SAP or mono
V_{oAF2}	24	AF output signal left/SAP or mono
GND	25	ground (0 V)
C_{ref}	26	smoothing capacitor for internal reference voltage
VCO	27	VCO free running frequency adjustment
LOOP	28	phase detector loop filter
STERI	29	stereo indicator output (sink)
PILOT	30	pilot cancel adjustment
C_{pil}	31	pilot detector smoothing capacitor, VCO/4 output
V_P	32	+5 V supply voltage

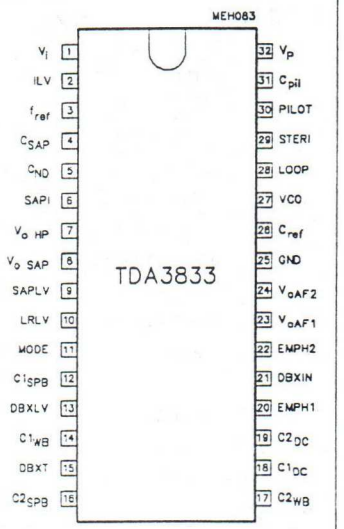


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 32)	0	8	V
V_1	composite input voltage	0	V_P	V
V_{11}	MODE input voltage	0	8	V
$I_{7,23,24}$	output current (AF outputs)	0	5	mA
$I_{6,29}$	output current (indication outputs)	0	5	mA
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−	±4000	V

Note to the Limiting Values

1. Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; for MPX: Δf = 25 kHz for L+R (100% modulation); f_{mod} = 1 kHz; and for SAP: Δf = 10 kHz; f_{mod} = 1 kHz, unless otherwise specified. Measurements taken in Fig.1 including all adjustments.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 32)		4.75	5	5.35	V
I_P	supply current		−	42	−	mA
V_n	DC input/output voltage at pins 1, 7, 8, 18, 19, 21, 23 and 24		−	$V_P/2$	−	V
MODE select 4-state input (see Table 1)						
V_{11}	input voltage for					
	mono/SAP		0	−	$V_P/2-1$	V
	SAP		$V_P/2-0.4$	−	$V_P/2+0.4$	V
	stereo		$V_P/2+1$	−	V_P	V
	mono		$V_P+1.4$	−	8	V
I_{11}	input current for					
	mono/SAP		−	−	15	µA
	SAP		−	−	15	µA
	stereo		−	−	5	µA
	mono	V_{11} = 7.2 V	−	−	300	µA
Composite input (pin 1)						
R_i	input resistance on pin 1		14	20	26	kΩ
V_i	input signal on pin 1 (RMS value)	see note 1				
	L+R (all other signals in accordance with BTSC system specification)		70	100	140	mV
	pilot threshold for MPX					
		stereo on	−	−	16	mV
		stereo off	5	−	−	mV
	hysteresis of threshold	MPX	−	2.5	−	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_i	pilot threshold for SAP					
		SAP on	–	–	37	mV
		SAP off	16	–	–	mV
	hysteresis of threshold	SAP	–	2	–	dB
G_v	gain control range	dependent on V_2	±5	±7.5	–	dB
V_2	control voltage range (pin 2)		–	1 to 4	–	V
I_2	input current (pin 2)	$V_2 = V_P/2$	–	–	5	µA
Voltage controlled oscillator (VCO) (pin 27)						
f_{VCO}	nominal VCO frequency ($4f_H$)	see note 2	–	62.94	–	kHz
Δf_{29}	capture range	nominal pilot	–	–	1	kHz
TC	temperature coefficient		–	–	50	10^{-6}/K
Stereo indication output (pin 29)						
V_{29}	output voltage range					
		stereo present	–	–	0.5	V
		stereo not present	V_P–0.5	–	V_P	V
I_{29}	output current active LOW	stereo present	3	–	–	mA
SAP/mono output (pin 7)						
V_o	output signal (RMS value, pin 7)	see note 3	–	550	–	mV
	output signal headroom	mono	–	9.5	–	dB
R_7	output resistance		–	100	200	Ω
R_L	load resistance		10	–	–	kΩ
C_L	load capacitance		–	–	500	pF
THD	total harmonic distortion					
		SAP signal	–	0.5	–	%
		mono signal	–	0.2	–	%
B	frequency response 50 to 10000 Hz	mono; external 75 µs de-emphasis	–3	–	–	dB
S/N(W)	weighted signal-to-noise ratio (CCIR468-3)	mono; external 75 µs de-emphasis	–	50	–	dB
SAP indication output (pin 6)						
V_6	output voltage range					
		SAP present	–	–	0.5	V
		SAP not present	V_P–0.5	–	V_P	V
I_6	output current active LOW	SAP present	3	–	–	mA
Audio outputs (pins 23 and 24)						
V_o	output signal (RMS value, pins 23 and 24)	see note 3	–	550	–	mV
	output signal headroom		–	9.5	–	dB
$\Delta V_{L,R}$	output signal difference between L and R	f = 250 to 6300 Hz	–	–	3	dB
ΔV_o	output signal difference after switching from L or R to SAP	f = 250 to 6300 Hz	–	–	3	dB
$\Delta V_{23,24}$	DC offset voltage after switching	stereo/mono/SAP	–	–	±100	mV
$R_{23,24}$	output resistance		–	200	300	Ω
R_L	load resistance		10	–	–	kΩ
C_L	load capacitance		–	–	500	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion					
		L and R signal	–	0.2	–	%
		SAP signal	–	0.5	–	%
B	L and R frequency response					
		f = 50 to 10000 Hz	–3	–	–	dB
		12 kHz related to 1 kHz	–	–3	–	dB
	SAP frequency response	f = 50 to 8000 Hz	–3	–	–	dB
S/N(W)	weighted signal-to-noise ratio	L + R signal; CCIR468-3	–	50	–	dB
S/N	unweighted signal-to-noise ratio (RMS value)	L + R signal; f = 20 to 20000 Hz	–	60	–	dB
α_{CR}	crosstalk					
		L or R into SAP	50	63	–	dB
		SAP into L or R	50	70	–	dB
α_{CH}	channel separation (according to DBX requirements)	f = 100 to 5000 Hz				
		10% 75 µs equivalent input modulation	20	26	–	dB
		1 to 100% 75 µs equivalent input modulation	15	20	–	dB
DBX section						
V_9	SAP level control voltage range		–	1 to 4	–	V
V_{10}	(L – R) level control voltage range		–	1 to 4	–	V
V_{13}	spectral band level control voltage range		–	1.8 to 3.2	–	V
$I_{9,10,13}$	input current	$V_I = 0.5V_P$	–	–	5	µA
S_1	spectral RMS-detector release rate		343	381	419	dB/s
I_{12}	timing current for nominal release rate of spectral RMS-detector	see note 4	–	22.5	–	µA
	current adjustment range		–	11 to 45		µA
S_2	wideband RMS-detector release rate		112.5	125	137.5	dB/s
I_{14}	timing current for nominal release rate of wideband RMS-detector	$0.33I_{12}$; see note 4	–	7.5	–	µA
	current adjustment range		–	4 to 15	–	µA
V_{15}	timing adjustment		–	1.5 to 3.8	–	V

Notes to the characteristics

1. Requirements for the MPX/SAP input signal to ensure correct system performance:
   a. Maximum variation of MPX/SAP signal under operating conditions: to be found (1 dB).
   b. 3 dB bandwidth ≥ 130 kHz (Δf = 25 kHz).
   c. THD (L + R, Δf = 25 kHz, f_{mod} = 1 kHz): 0.2%.
   d. S/N(W), weighted in accordance with CCIR468-3 (L + R, Δf = 25 kHz for sound carrier, f_{mod} = 1 kHz, 75 µs de-emphasis; with critical picture modulation): S/N(W) > 44 dB; with sync only: S/N(W) > 54 dB.
   e. Spectral spurious attenuation: 40 dB (mainly n x f_H; L + R, Δf = 25 kHz for sound carrier, f_{mod} = 1 kHz, 50 Hz to 100 kHz, no de-emphasis).
   f. Maximum white noise level (unweighted, 200 Hz to 100 kHz) to avoid malfunctioning of the identification circuits: 500 mV (RMS).
2. Adjustable on pin 27, measurement (f_H) on pin 7 with a 2.7 kΩ resistor connected between V_P and pin 31.
3. Can also be aligned to 600 mV (RMS), then identification threshold and AF output headroom will be decreased by 1.6 dB.
4. I_{12} and I_{14} can be measured via an ammeter connected to 4 V (3.5 to 4.1 V).

Table 1 MODE select; 4-state pin 11

MODE	V_{11} (V_P = 5 V) (V)	SAP CARRIER	AF OUTPUTS		SAP/MONO OUTPUT
			pin 23	pin 24	pin 7
mono	8	on	mono	mono	SAP without DBX
stereo	V_P	on	right	left	SAP without DBX
SAP	V_P/2	on	SAP	SAP	mono
mono/SAP	0	on	SAP	mono	SAP without DBX
mono	8	off	mono	mono	mono
stereo	V_P	off	right	left	mono
SAP	V_P/2	off	right	left	mono
mono/SAP	0	off	mute	mono	mono

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1991

TDA3840

TV IF amplifier and demodulator with TV signal identification

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit

GENERAL DESCRIPTION

The TDA3840 is a bipolar integrated circuit for vision IF-signal processing in TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
$V_{1\text{-}20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	f = 38.9 MHz	–	70	–	μV
	minimum IF input signal for TV signal identification at pin 6 (RMS value)	maximum G_v	–	20	40	μV
V_o	video output signal (pin 12)	buffered	–	2.0	–	V
G_v	IF voltage gain control range		–	66	–	dB
S/N	signal-to-noise ratio	$V_{1\text{-}20}$ = 10 mV	55	60	–	dB
V_8	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	μA/kHz
RR	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3840	20	DIL	plastic	SOT146
TDA3840T	20	mini-pack	plastic	SO20L; SOT163A

TV IF amplifier and demodulator with TV signal identification

TDA3840

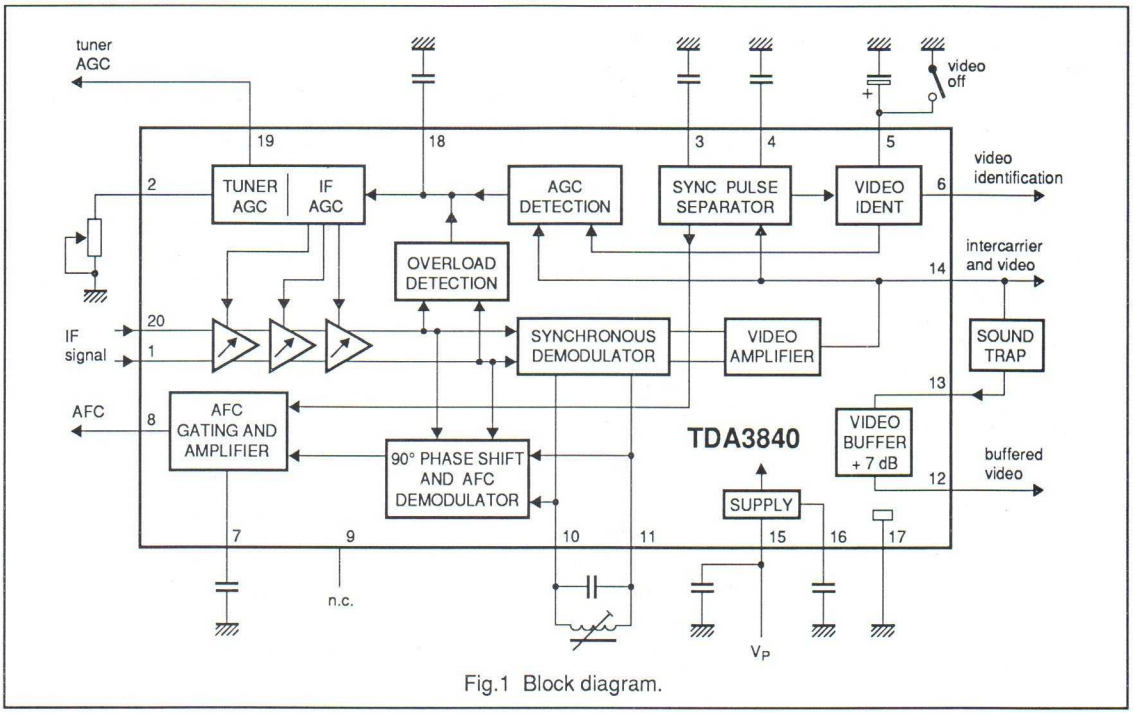


Fig.1 Block diagram.

PIN CONFIGURATION

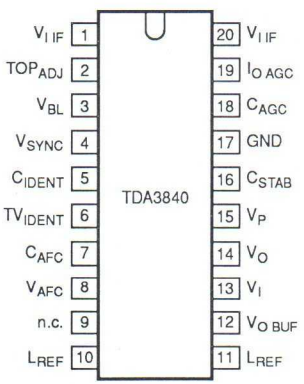


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I\,IF}$	1	IF input (balanced)
TOP_{ADJ}	2	tuner AGC take-over point adjustment
V_{BL}	3	black level voltage
V_{SYNC}	4	sync pulse amplitude voltage
C_{IDENT}	5	identification capacitor
TV_{IDENT}	6	video identification output
C_{AFC}	7	AFC capacitor
V_{AFC}	8	AFC output signal
n.c.	9	not connected
L_{REF}	10	LC reference tuned circuit
L_{REF}	11	LC reference tuned circuit
$V_{O\,BUF}$	12	buffered video output signal
V_I	13	video input signal for buffer
V_O	14	video output signal with intercarrier signal
V_P	15	supply voltage
C_{STAB}	16	supply voltage stabilization
GND	17	ground
C_{AGC}	18	AGC capacitor
$I_{O\,AGC}$	19	tuner AGC output signal
$V_{I\,IF}$	20	IF input (balanced)

TV IF amplifier and demodulator with TV signal identification

TDA3840

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video identification
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

The peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion.

To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector. The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video identification output. The bandwidth is limited to reduce the noise and increase the identification sensitivity.

11. Video identification

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier and the IF signal are fed to the AFC demodulator. The demodulated signal and the IF signal are fed to the AFC gating stage.

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector sink/source output). The AFC function can be externally switched off for test purposes. For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

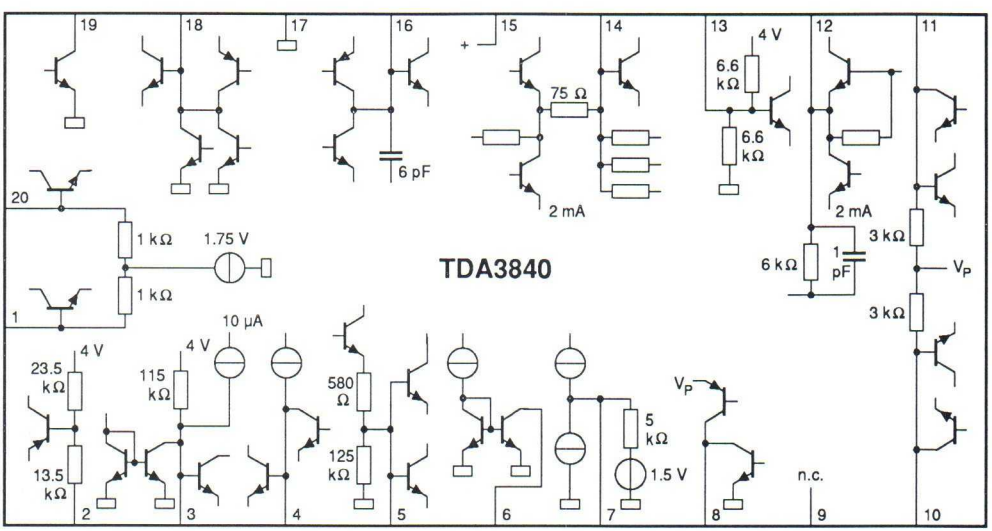


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage at pin 15: SOT146	–	8.8	V
	SOT163A	–	6.0	V
V_{19}	tuner AGC voltage	–	13.2	V
V_8	permissible voltage at AFC output	–	V_P	V
I_{15}	supply current	–	55	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD sensitivity	–	± 300	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C; f_{VC} = 38.9 MHz; all voltages are measured to GND (pin 17); measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R_I	input resistance (pins 1 and 20)		–	2	–	kΩ
C_I	input capacitance (pins 1 and 20)		–	1.5	–	pF
$V_{1\text{-}20(rms)}$	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G_v ; note 1	100	–	–	mV
G_v	gain control range		63	66	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AGC						
I_{18}	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video identification	–	13	–	μA
	charging current AGC capacitor	without video identification	–	35	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_1	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms
Tuner AGC (note 2)						
$V_{1\text{-}20(rms)}$	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I_{19}	tuner AGC output current	V_{19} = 0.5 V	1	2	–	mA
Synchronous demodulator and video amplifier (note 3)						
V_{14}	composite video output signal		0.9	1.0	1.1	V
	sync level voltage		–	1.5	–	V
	zero carrier level voltage		–	2.6	–	V
I_{14}	output current	DC and AC	–	–	± 1.0	mA
R_{14}	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	$C_{load} \leq 20$ pF	7	8	–	MHz
V_{14}	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V_{12}	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I_{12}	output current	DC and AC	–	–	± 1.0	mA
R_{12}	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	$C_{load} \leq 20$ pF	–	10	–	MHz
R_I	input resistance (pin 13)		–	3.3	–	kΩ
C_I	input capacitance (pin 13)		–	2	–	pF

TV IF amplifier and demodulator with TV signal identification

TDA3840

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall video performance (see Fig.6)						
V_o	video output signal (pin 12)	negative modulation; note 3	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	$C_{load} \leq 20$ pF	7	8	–	MHz
S/N	signal-to-noise ratio (see Fig.7)	V_{1-20} = 10 mV;note 4	55	60	–	dB
α_1	intermodulation for blue (note 5)	f = 1.1 MHz f = 3.3 MHz	56 62	58 –	– –	dB dB
α_2	intermodulation for yellow (note 5)	f = 1.1 MHz f = 3.3 MHz	53 60	56 –	– –	dB dB
α_3	signal harmonic suppression		–	26	–	dB
V_5	video switch off voltage	note 6	–	–	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	–	dB
ΔG	differential gain	EBU test line 330	–	2	–	%
$\Delta\Phi$	differential phase	EBU test line 330	–	2	–	deg
$\Delta V/V$	variation of video output signal (pin 14)	gain control 50 dB; $V_{1-20(rms)}$ = 0.3 to 100 mV	–	–	0.5	dB
V_{res1}	residual vision carrier (pin 12)		–	1	–	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		–	1	–	mV
Video identification						
$V_{1-20(rms)}$	minimum IF input signal for TV identification at pin 14 (RMS value)	maximum G_v	–	20	40	µV
V_6	video identification voltage (signal unidentified)	$V_{1-20} = < 40\ \mu V_{rms}$ I_6 = 0.5 mA	–	–	0.4	V
	video identification voltage (signal identified)	$V_{1-20} = \geq 40\ \mu V_{rms}$ $I_6 = -1\ \mu A$	4.5	–	–	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	$\times 10^{-3}$
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 7	–	8	–	dB
I_5	allowed leakage current		–	–	3	µA
α_5	sync pulse suppression for correct TV signal identification		–	–	70	%
t_d	delay time of mute output signal		–	100	150	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC (see Fig.9 and Fig.10); note 8						
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	–	4.7	V
	lower output voltage		0.3	–	0.7	V
S	control steepness	QB = 40; $V_{1\text{-}20(rms)}$ = 10 mV	–	2	–	μA/kHz
I_7	leakage current at AFC gating		–	–	± 1	μA

Notes to the characteristics

1. The video signal is still gain-controlled, $V_{14(p\text{-}p)}$ = 1 V, but intermodulation figures are degraded.
2. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
3. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.4). The IF input signal is fed from 50 Ω via a 1:1 transformer, DSB, to pins 1 and 20. With a 10 mV_{RMS} IF input signal, the residual vision carrier is:
   = 10 % for white (standard B/G).
4. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

$$S/N = \frac{V_{14\ (black\ to\ white)}}{V_{14\ noise}\ (RMS,\ black)}$$

5. Intermodulation figures are defined as follows:

$$\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

and

$$\alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

6. When $V_5 < 1$ V (short-circuited identification capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to "zero carrier level ("ultra white" (2.6V) for negative modulation).
   During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3$ μA).
7. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
8. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz. The AFC function can be switched off for test purposes when pin 7 is connected to ground (V_7 = 0 V).

TV IF amplifier and demodulator with TV signal identification

TDA3840

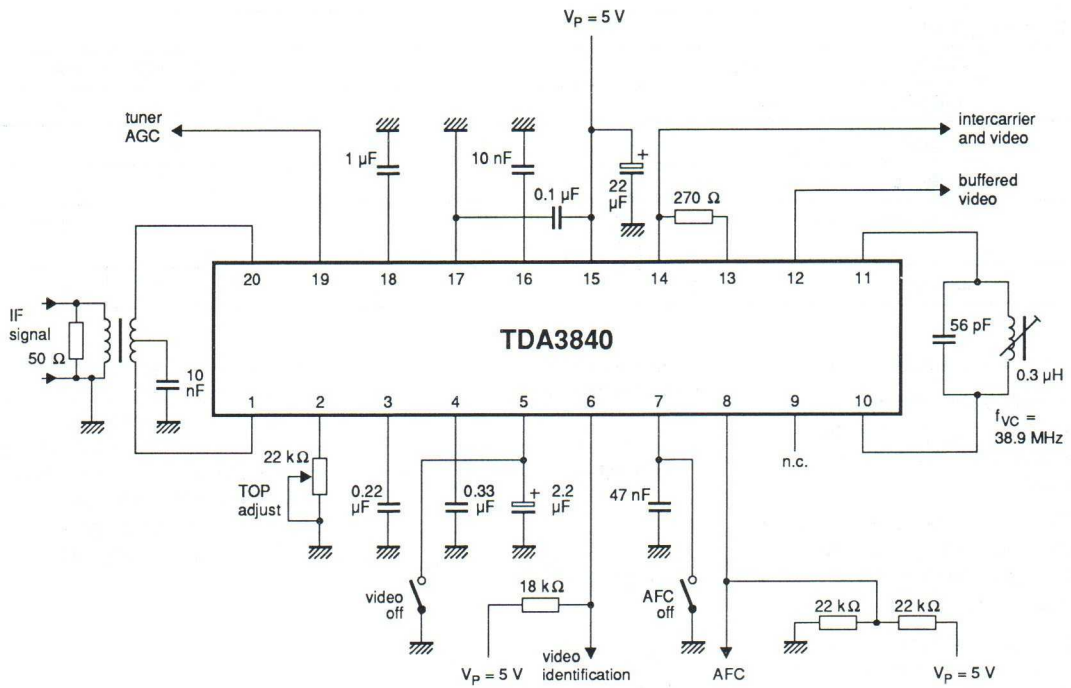


Fig.4 Test circuit.

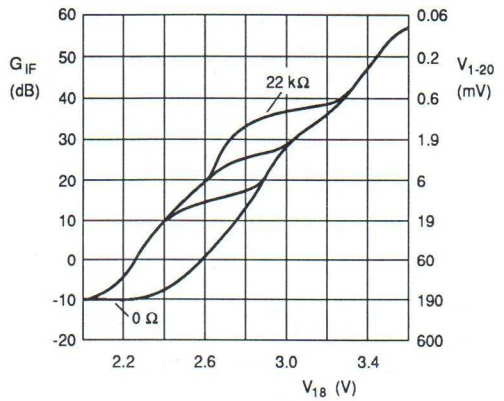


Fig.5 AGC characteristics with different values of R2.

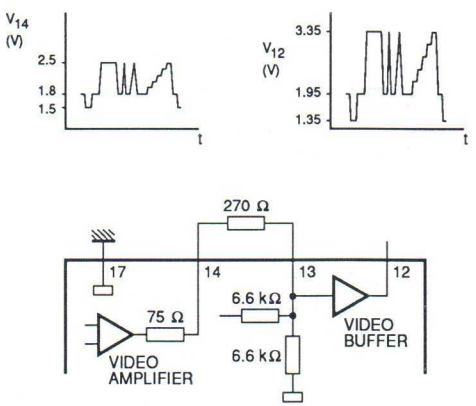


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

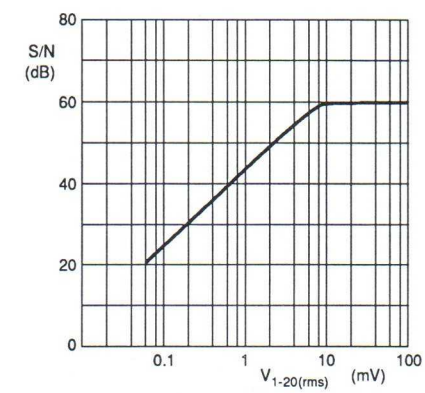
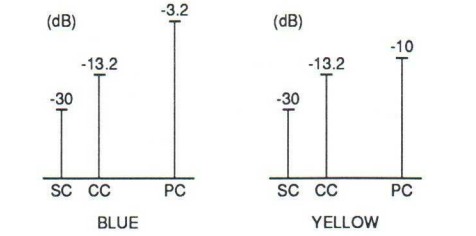


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound trap attenuation: 17 dB.

Fig.8 Input conditions for intermodulation measurements.

APPLICATION INFORMATION

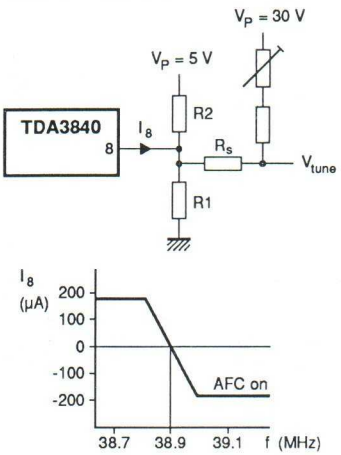


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

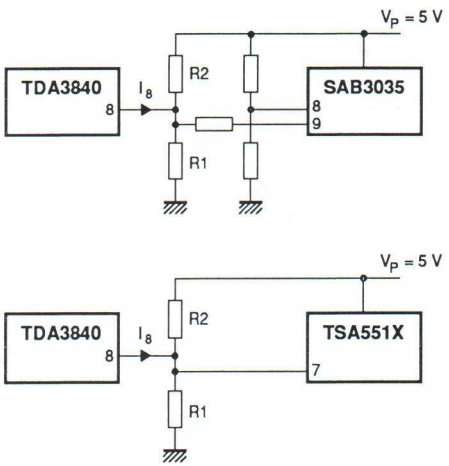


Fig.10 AFC interfacing for μP controlled systems.

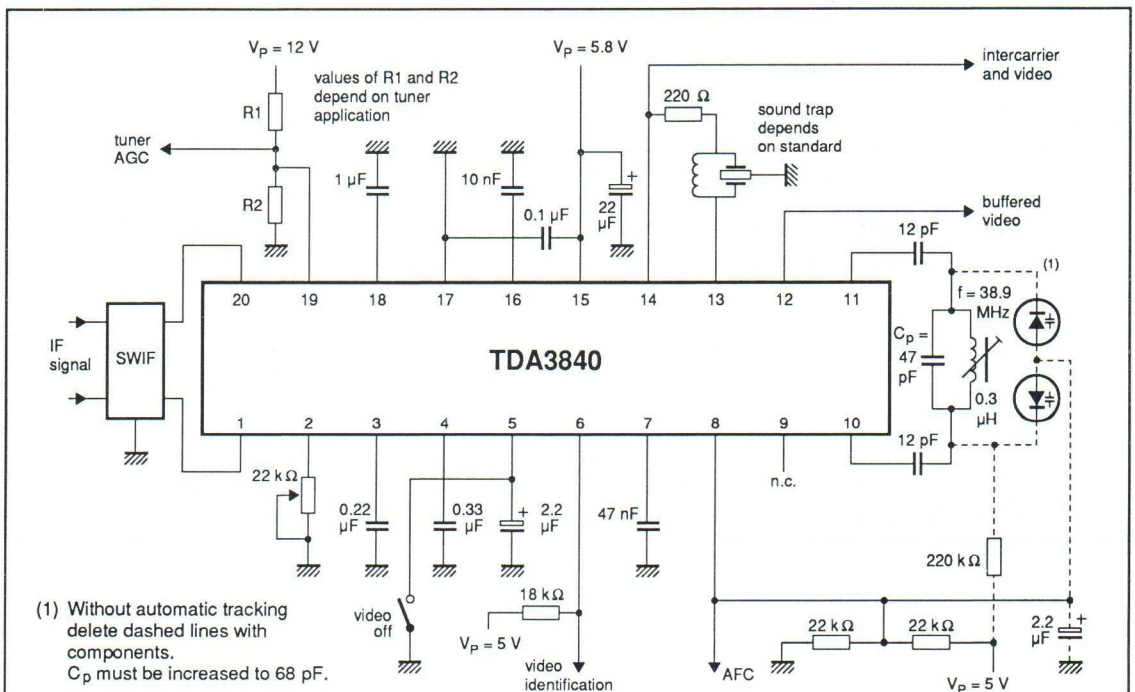


Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

APPLICATION INFORMATION (continued)

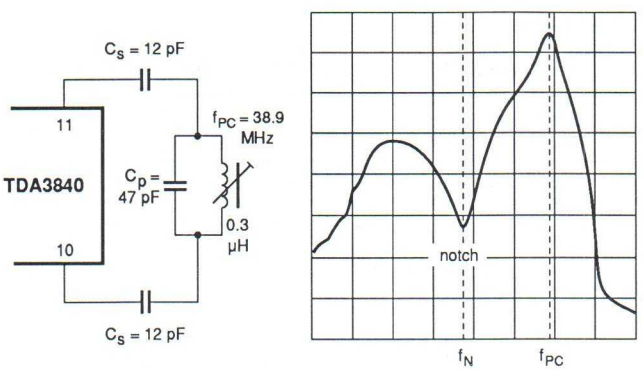


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

Note to Fig.12

Recommended for reception of data signals e.g. in Teletext. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_S and C_P are calculated as follows:

$$C_S = 2\,C_P\left\{\frac{f_{PC}^2}{f_N^2} - 1\right\}$$

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1991
Replaces the issue of August 1990.	

TDA3842

Multistandard TV IF amplifier and demodulator with TV signal identification

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC for negative modulation, e.g. B/G
- Peak white AGC for positive modulation, e.g. L
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit, suitable for MAC-on-cable

GENERAL DESCRIPTION

The TDA3842 is a bipolar integrated circuit for vision IF-signal processing in multistandard TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
$V_{1\text{-}20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	f = 38.9 MHz	–	70	–	μV
	minimum IF input signal for TV signal identification at pin 6 (RMS value)	maximum G_v	–	20	40	μV
V_o	video output signal (pin 12)	buffered	–	2.0	–	V
G_v	IF voltage gain control range		–	66	–	dB
S/N	signal-to-noise ratio	$V_{1\text{-}20}$ = 10 mV	55	60	–	dB
V_8	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	μA/kHz
RR	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3842	20	DIL	plastic	SOT146
TDA3842T	20	mini-pack	plastic	SO20L; SOT163A

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842

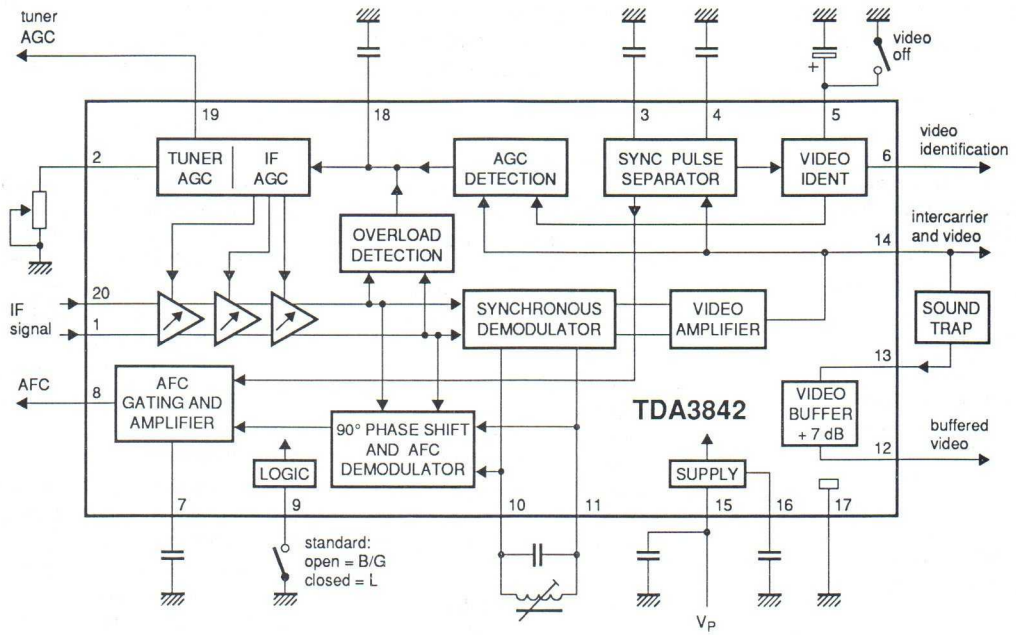


Fig.1 Block diagram.

PIN CONFIGURATION

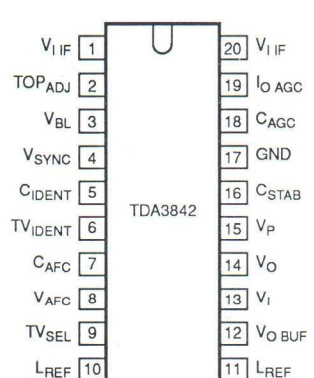


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I\,IF}$	1	IF input (balanced)
TOP_{ADJ}	2	tuner AGC take-over point adjustment
V_{BL}	3	black level voltage
V_{SYNC}	4	sync pulse amplitude voltage
C_{IDENT}	5	identification capacitor
TV_{IDENT}	6	video identification output
C_{AFC}	7	AFC capacitor
V_{AFC}	8	AFC output signal
TV_{SEL}	9	video standard selection switch
L_{REF}	10	LC reference tuned circuit
L_{REF}	11	LC reference tuned circuit
$V_{O\,BUF}$	12	buffered video output signal
V_I	13	video input signal for buffer
V_O	14	video output signal with intercarrier signal
V_P	15	supply voltage
C_{STAB}	16	supply voltage stabilization
GND	17	ground
C_{AGC}	18	AGC capacitor
$I_{O\,AGC}$	19	tuner AGC output signal
$V_{I\,IF}$	20	IF input (balanced)

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video identification
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer
15. Standard switch

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal polarity is switched according to the TV standard selected. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth. The DC level is shifted according to the TV standard to provide the same sync level for positive and negative IF modulation.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

With negative modulation (B/G) a peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion

Positive modulation (L) uses a peak white AGC detector.

To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector. The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video identification output. The bandwidth is limited to reduce the noise and increase the ident sensitivity.

11. Video identification

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier and the IF signal are fed to the AFC demodulator. The demodulated signal is fed to the AFC gating stage.

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector sink/source output). At positive modulation the AFC operates continuously.

AFC function can be externally switched off for test purposes. For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

15. Standard switch

The operating mode of the AGC detector and video IF demodulator for positive and negative IF modulation is selected by the logic level on pin 9.

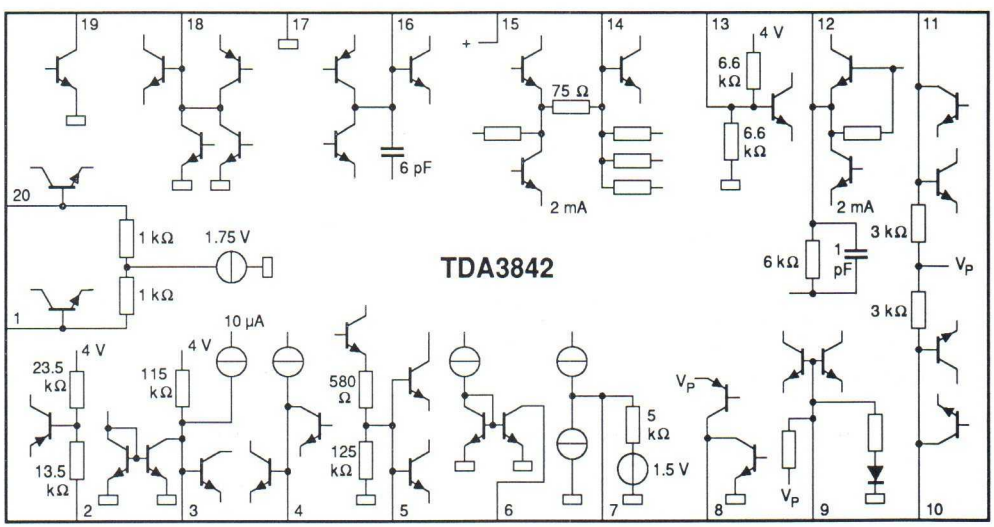


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage at pin 15: SOT146	–	8.8	V
	SOT163A	–	6.0	V
V_{19}	tuner AGC voltage	–	13.2	V
V_8	permissible voltage at AFC output	–	V_P	V
I_{15}	supply current	–	55	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD sensitivity	–	± 300	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C; f_{VC} = 38.9 MHz; all voltages are measured to GND (pin 17); measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R_I	input resistance (pins 1 and 20)		–	2	–	kΩ
C_I	input capacitance (pins 1 and 20)		–	1.5	–	pF
$V_{1\text{-}20(rms)}$	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G_v ; note 1	100	–	–	mV
G_v	gain control range		63	66	–	dB
IF AGC: negative modulation						
I_{18}	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video identification	–	13	–	μA
	charging current AGC capacitor	without video identification	–	35	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_1	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AGC: standard L (note 2)						
I_{18}	leakage current AGC capacitor		–	–	20	nA
	charging current AGC capacitor	with video identification	–	280	–	nA
		without video identification	–	22	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_2	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	300	–	ms
Tuner AGC (note 3)						
$V_{1\text{-}20(rms)}$	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I_{19}	tuner AGC output current	V_{19} = 0.5 V	1	2	–	mA
Sync demodulator and video amplifier (note 4)						
V_{14}	composite video output signal		0.9	1.0	1.1	V
	sync level voltage	standard B/G	–	1.5	–	V
	zero carrier level voltage	negative modulation	–	2.6	–	V
		positive modulation	–	1.47	–	V
I_{14}	output current	DC and AC	–	–	± 1.0	mA
R_{14}	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	$C_{load} \leq 20$ pF	7	8	–	MHz
V_{14}	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V_{12}	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I_{12}	output current	DC and AC	–	–	± 1.0	mA
R_{12}	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	$C_{load} \leq 20$ pF	–	10	–	MHz
R_I	input resistance (pin 13)		–	3.3	–	kΩ
C_I	input capacitance (pin 13)		–	2	–	pF

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall video performance (see Fig.6)						
V_o	video output signal (pin 12)	negative modulation	–	2	–	V
		positive modulation; note 4	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	$C_{load} \leq 20$ pF	7	8	–	MHz
S/N	signal to noise ratio (see Fig.7)	$V_{1-20} = 10$ mV; note 5	55	60	–	dB
α_1	intermodulation for blue (note 6)	f = 1.1 MHz f = 3.3 MHz	56 62	58 –	– –	dB dB
α_2	intermodulation for yellow (note 6)	f = 1.1 MHz f = 3.3 MHz	53 60	56 –	– –	dB dB
α_3	signal harmonic suppression		–	26	–	dB
V_5	video switch off voltage	note 7	–	–	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	–	dB
ΔG	differential gain	EBU test line 330	–	2	–	%
$\Delta\Phi$	differential phase	EBU test line 330	–	2	–	deg
$\Delta V/V$	variation of video output signal (pin 14)	gain control 50 dB; $V_{1-20(rms)} = 0.3$ to 100 mV	–	–	0.5	dB
V_{res1}	residual vision carrier (pin 12)		–	1	–	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		–	1	–	mV
Video identification						
$V_{1-20(rms)}$	minimum IF input signal for TV identification at pin 14 (RMS value)	maximum G_v	–	20	40	μV
V_6	video identification voltage (signal unidentified)	$V_{1-20(rms)} = < 40$ μV $I_6 = 0.5$ mA	–	–	0.4	V
	video identification voltage (signal identified)	$V_{1-20(rms)} = \geq 40$ μV $I_6 = -1$ μA	4.5	–	–	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	$\times 10^{-3}$
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 8	–	8	–	dB
I_5	allowed leakage current		–	–	3	μA
α_5	sync pulse suppression for correct TV signal identification		–	–	70	%
t_d	delay time of mute output signal		–	100	150	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC (see Fig.9 and Fig.10); note 9						
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	–	4.7	V
	lower output voltage		0.3	–	0.7	V
S	control steepness	QB = 40; $V_{1\text{-}20(rms)}$ = 10 mV	–	2	–	μA/kHz
I_7	leakage current at AFC gating		–	–	± 1	μA
Standard switch						
V_9	voltage for negative modulation	standard switch open	2.5	n.c.	V_P	V
	voltage for positive modulation (L)	standard switch closed	0	–	0.8	V

Notes to the characteristics

1. The video signal is still gain-controlled, $V_{14(p\text{-}p)}$ = 1 V, but intermodulation figures are degraded.
2. In multi-standard applications the capacitor at pin 18 must be a low-leakage (foil) type.
3. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
4. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.4). The IF input signal is fed from 50 Ω via a 1:1 transformer, DSB, to pins 1 and 20. With a 10 mV_{RMS} IF input signal, the residual vision carrier is:
   = 10 % for white (standard B/G),
   = 3 % for sync (standard L).
5. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

$$S/N = \frac{V_{14\ (black\ to\ white)}}{V_{14\ noise}\ (RMS,\ black)}$$

6. Intermodulation figures are defined as follows:

$$\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

and

$$\alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

7. When $V_5 < 1$ V (short-circuited identification capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to "zero carrier level ("ultra white" (2.6V) for negative modulation or "top sync" (1.5 V) for positive modulation). During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3$ μA).
8. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
9. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz. The AFC function can be switched off for test purposes when pin 7 is connected to ground (V_7 = 0 V).

Multistandard TV IF amplifier and demodulator with TV signal identification

TDA3842

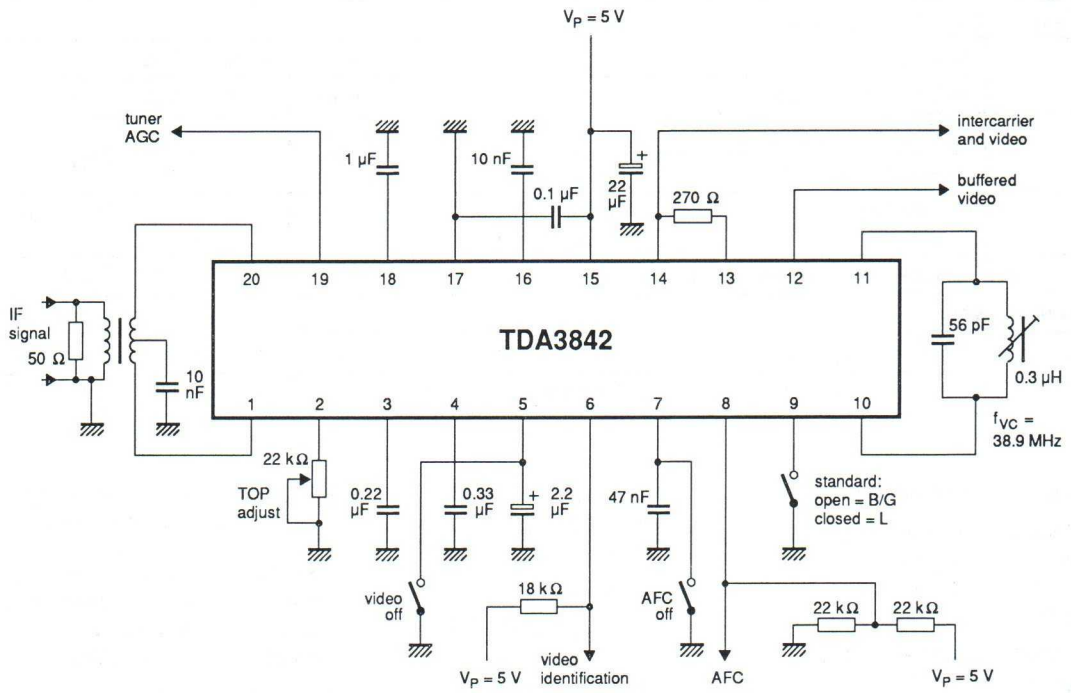


Fig.4 Test circuit.

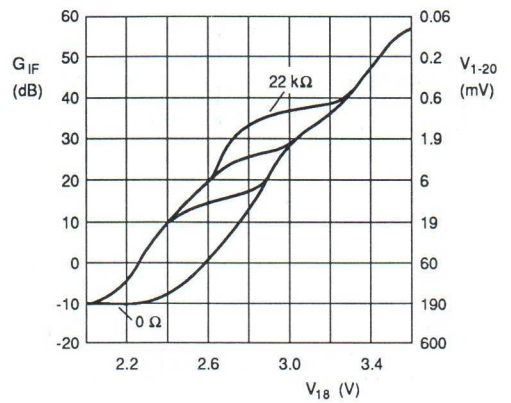


Fig.5 AGC characteristics with different values of R2.

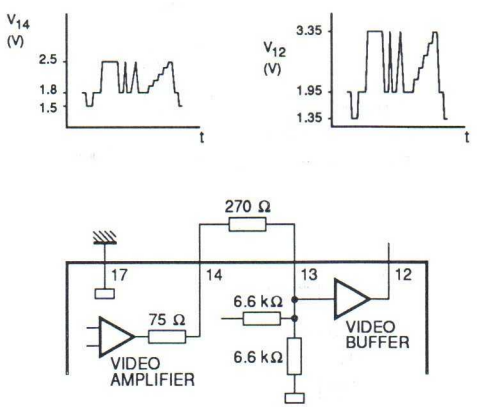


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

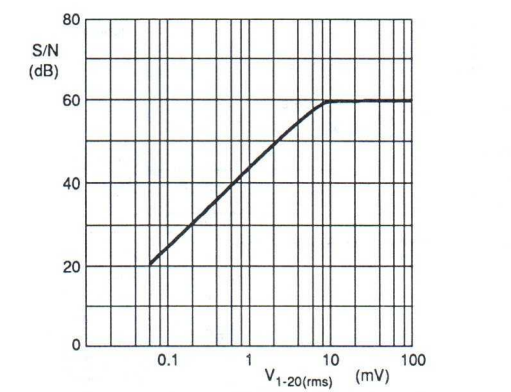


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.

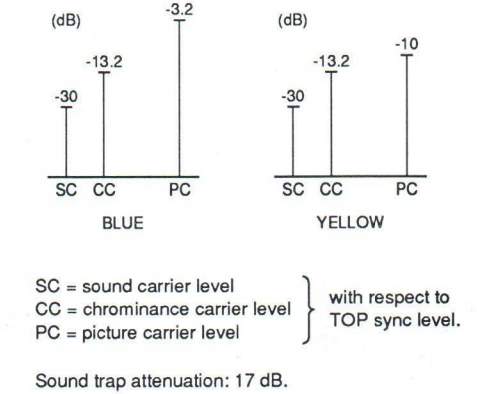


Fig.8 Input conditions for intermodulation measurements.

APPLICATION INFORMATION

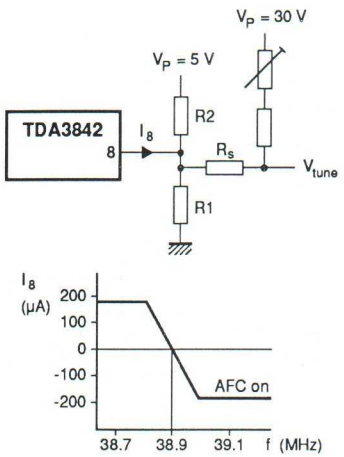


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

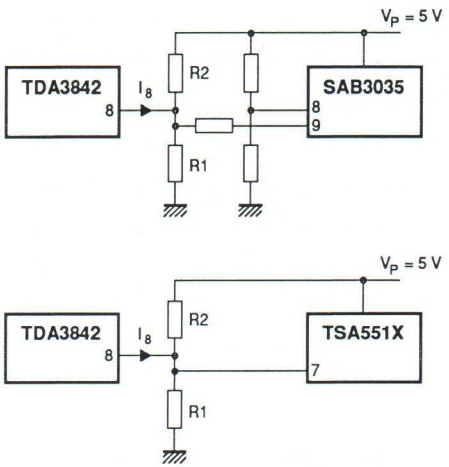


Fig.10 AFC interfacing for μP controlled systems.

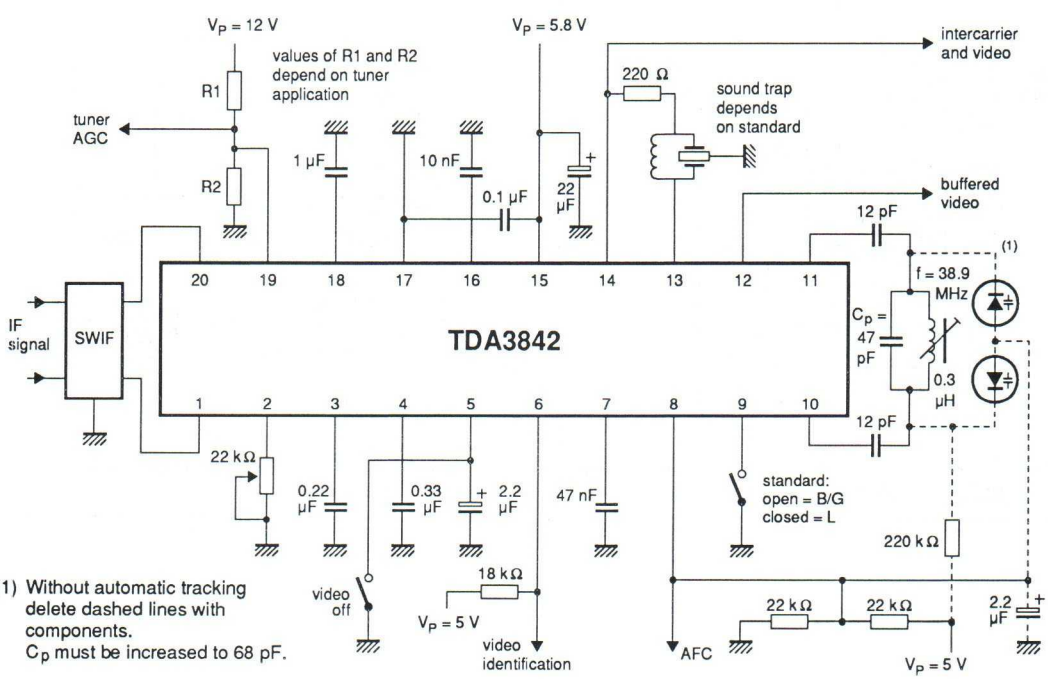


Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

APPLICATION INFORMATION (continued)

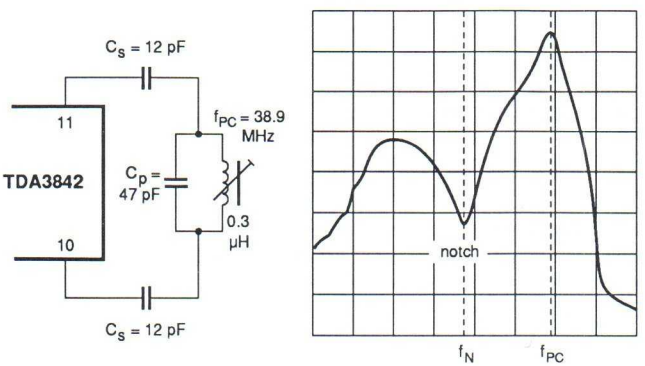


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

Note to Fig.12

Recommended for reception of data signals e.g. in Teletext and D2-MAC. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_s and C_p are calculated as follows:

$$C_s = 2\,C_p\left\{\frac{f_{PC}^2}{f_N^2} - 1\right\}$$

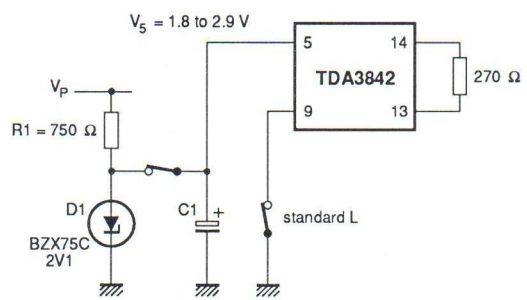


Fig.13 Modification of Fig.11 for MAC/D2-MAC application.

Note to Fig.13

When the TDA3842 is used in a MAC/D2-MAC receiver the voltage at pin 5 must be stabilized between 1.8 and 2.9 V by zener diode D1 and resistor R1. Standard switch at pin 9 must be in position 'standard L' to activate the peak-related slow AGC mode.

SOUND-IF CIRCUIT FOR TV AM-SOUND STANDARD L AND L'

GENERAL DESCRIPTION

The TDA3843 performs the AM-sound demodulation for the L- and L'- standard.

Features

- 5 to 8 V power supply and an alternative 12 V power supply
- Low power consumption (200 mW) at 5 V supply voltage
- New AC-coupled wideband IF-amplifier (high dynamic ranges, less intermodulation)
- In-phase wideband AM demodulator without external reference circuit
- Reduced THD figures even for low AF frequencies (typical 1%)
- Stabilizer circuit for ripple rejection and constant output signals
- All pins are ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	12	13.2	V
Supply current	$I_{11, 14\text{-}13}$	–	40	48	mA
Minimum IF input (RMS value)	$V_{1\text{-}16}$	–	70	100	μV
IF control range	ΔG_V	60	63	–	dB
AF output signal (RMS value)	$V_{6\text{-}13}$	–	550	–	mV
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	S+W/W	50	56	–	dB

PACKAGE OUTLINE

16-lead DIL; plastic (opposite bent leads) (SOT38WBE)

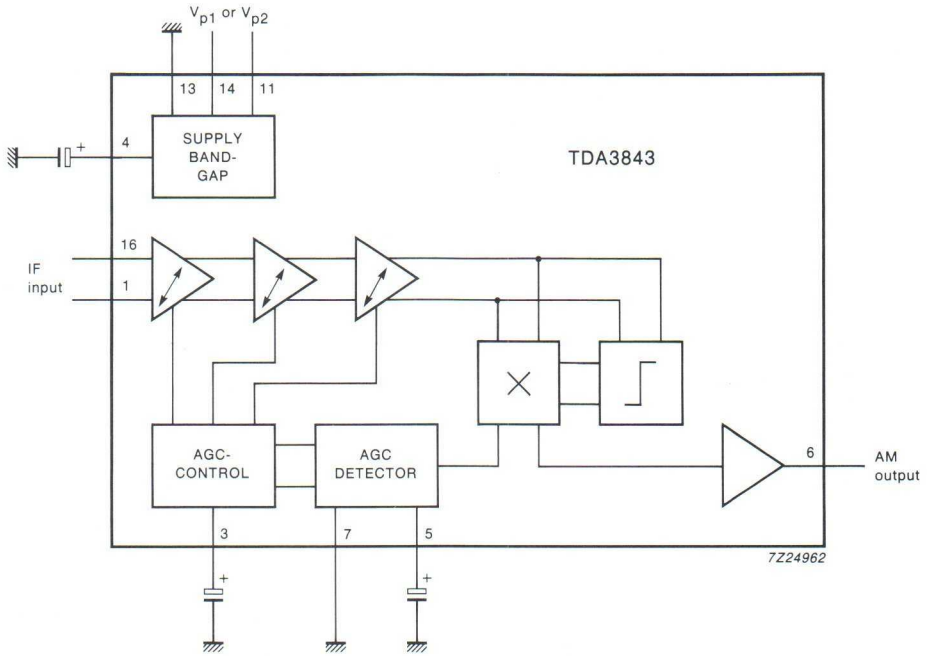


Fig.1 Block diagram.

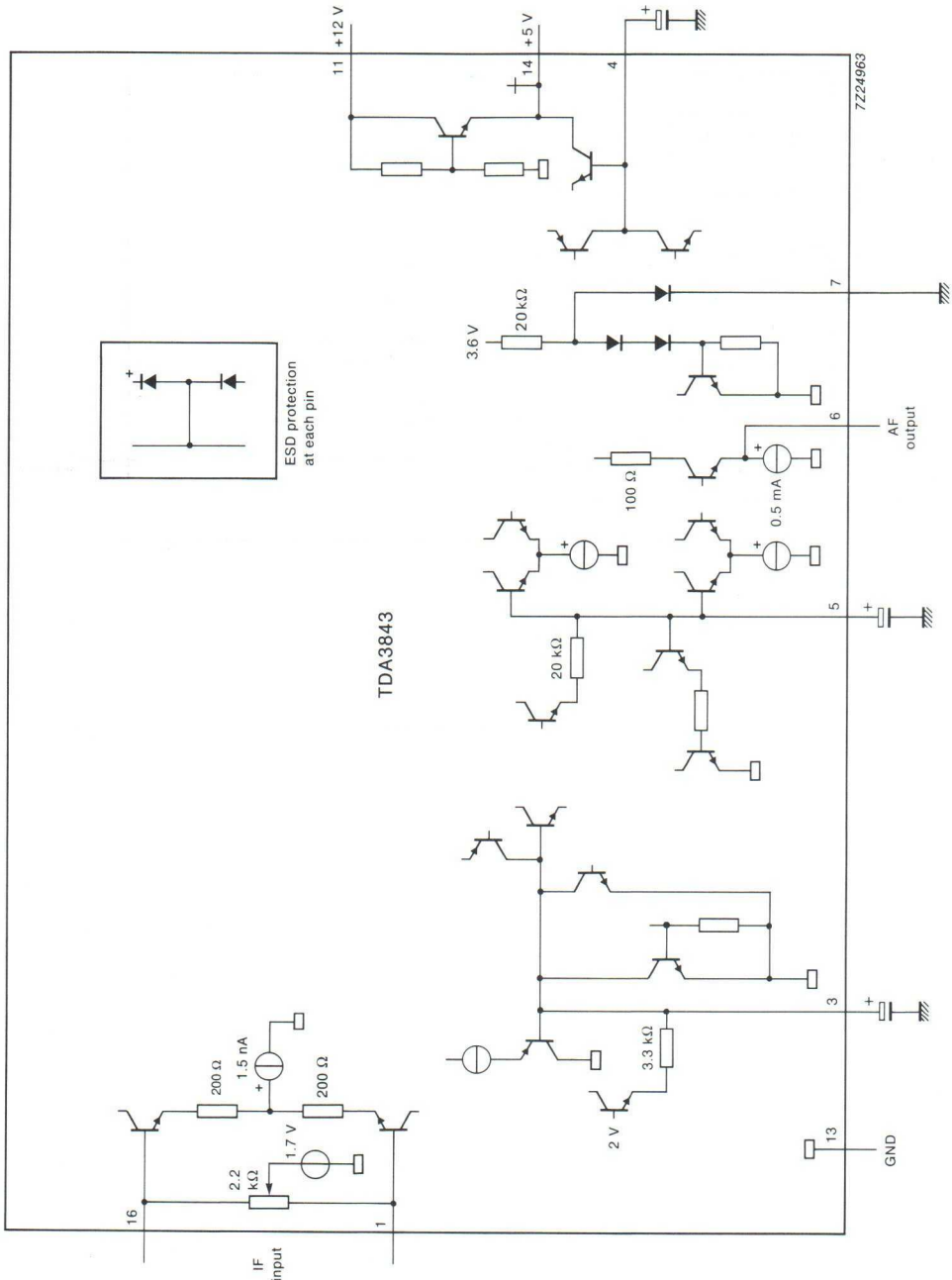


Fig.2 Input/output loading diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	13.2	V
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−25	+ 125	°C
Total power dissipation at V_{P2}	P_{tot}	−	635	mW

CHARACTERISTICS

V_{P1} = 5 V (see note 1); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current consumption		I_{11}	−	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	−	2	−	kΩ
Input capacitance		$C_{1\text{-}16}$	−	2.5	−	pF
Minimum IF input signal (RMS value)	note 2	$V_{1\text{-}16}$	−	70	100	μV
Maximum IF input signal (RMS value)	note 3	$V_{1\text{-}16}$	70	100	−	mV
Gain control range			60	63	−	dB
IF bandwidth	−3 dB		50	70	−	MHz
DC potential		$V_{1/16\text{-}3}$	−	1.7	−	V
AM demodulator	note 4					
AF output signal (RMS value)		$V_{6\text{-}13}$	440	550	660	mV
AF bandwidth	−3 dB, note 5	$V_{6\text{-}13}$	0.02	−	> 100	kHz
Total harmonic distortion		THD	−	1	2	%
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	note 6	S+W/W	50	56	−	dB
DC potential		$V_{6\text{-}13}$	−	1.8	−	V
Output resistance	emitter follower with 0.5 mA bias current	R_6	−	200	−	Ω
Allowable AC output current (peak-to-peak value)	note 7	$\pm I_6$	−	−	0.3	mA
Allowable DC output current		$-I_6$	−	−	1	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection	$V_{ripple} < 200$ mV (peak-to-peak), 50 to 100 Hz, measured at 70 Hz					
AF signal output	$\alpha RR = V_{ripple}$ on V_P/V_{ripple} on V_O	αRR	30	40	–	dB
IF filter						
Proposal for sound carrier filter for L-standard	Fig.5					

Notes to the characteristics

1. Using the power supply voltage range V_{P1} = 5 to 8 V, the performance will not essentially change. Using the power supply voltage range, V_{P2} = 12 V, the performance will be comparable with the performance at V_{P1} = 5 to 8 V. The unused power supply pin must not be connected.
2. Start of gain control (low IF input signal) at –3 dB AF signal reduction at pin 6.
3. End of gain control (high IF input signal) at +1 dB AF signal expansion at pin 6.
4. Sound carrier = 32.4 MHz modulated with f = 1 kHz and a modulation depth m = 80%. IF input signal $V_{1\text{-}16}$ = 10 mV (RMS value).
5. A maximum value of 100 kHz is guaranteed, but, typically a maximum value of 700 kHz is found.
6. The capacitor at pin 4 may be omitted, but then the S+W/W figure will be degraded by up to 8 dB in the IF voltage range 1 mV up to 100 mV.
7. If a higher AC output current is required, an external resistor must be connected from the output to ground. This is to increase the bias current of the emitter follower (note, the maximum allowable DC output current).

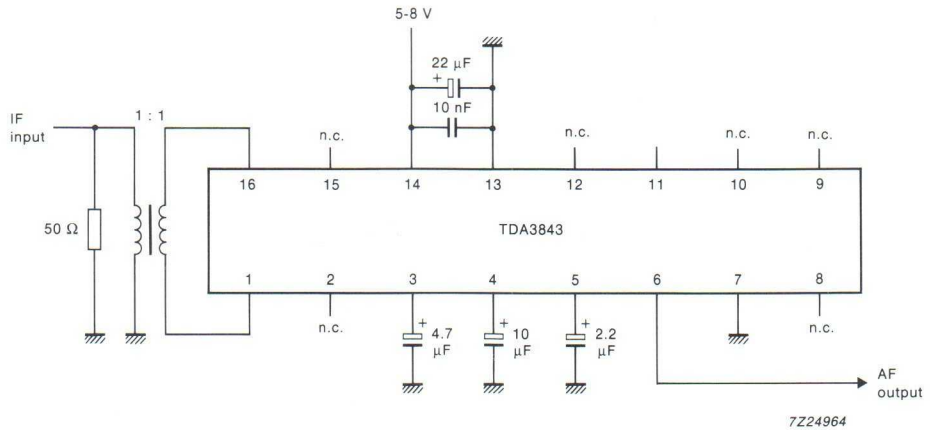


Fig.3 Test circuit, 5 V supply.

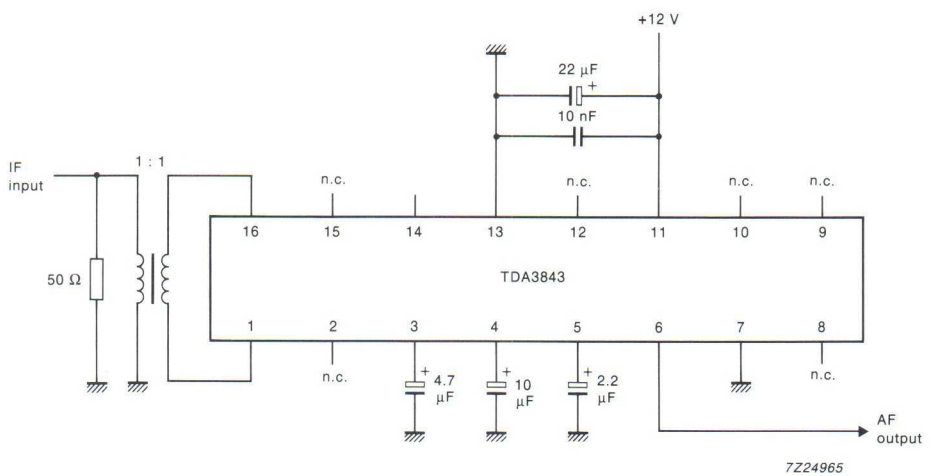
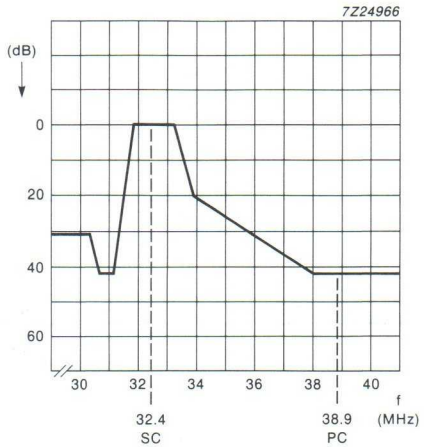


Fig.4 Test circuit, 12 V supply.



Where SC = sound carrier and PC = picture carrier.

Fig.5 AM IF filter for standard L.

Quasi split-sound circuit and AM demodulator

TDA3845; TDA3845T

FEATURES

- Power supply from 5 V (200 mW) to 8 V source also an alternative 12 V source (12 V not for TDA3845T)
- Gain controlled wideband IF amplifier (AC coupled with three stages)
- High precision internal 90° phase shifter for quadrature demodulator
- Amplitude detector for gain control which operates as a peak detector for FM sound and as a mean level detector for AM sound (switchable)
- In-phase wideband synchronous demodulator for AM detection
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection for all pins
- Suitable for all FM standards and L as well as L-accent standard
- NICAM compatible.

GENERAL DESCRIPTION

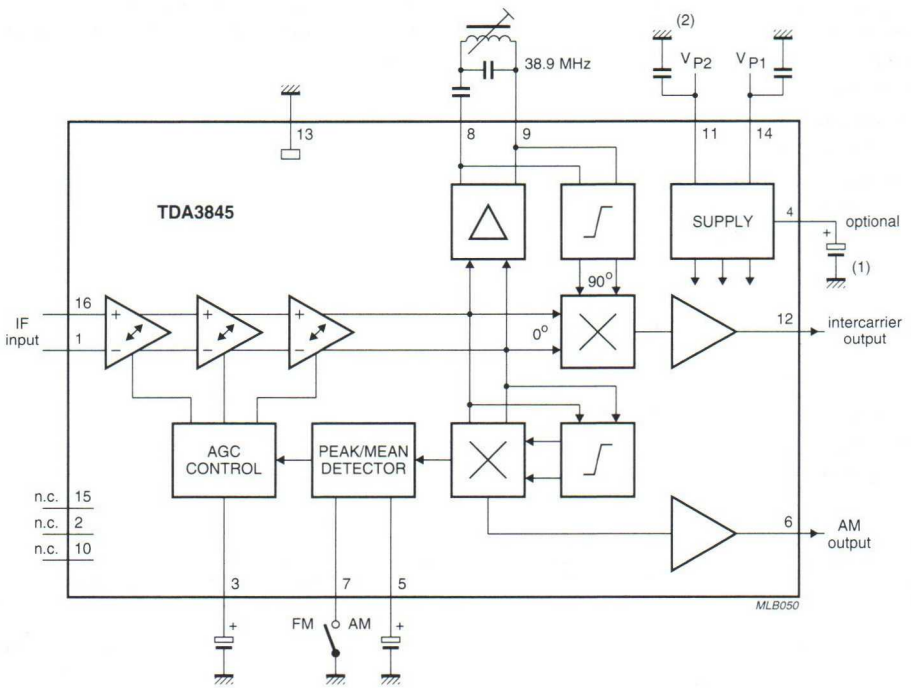
The TDA3845 is a quasi split-sound IF circuit which is designed to provide high performance television FM/AM sound.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
	positive supply voltage				
V_{P1}	pin 14	4.5	5.0	8.8	V
V_{P2}	pin 11 (not for TDA3845T)	10.8	12.0	13.2	V
I_P	supply current	–	40	–	mA
$V_{1\text{-}16(RMS)}$	minimum IF input voltage (RMS value)	–	70	100	μV
	IF control range	60	63	–	dB
$V_{12\text{-}13(RMS)}$	intercarrier output voltage 5.5 MHz (RMS value)	70	100	–	mV
(S + W)/W	signal-to-weighted-noise ratio (relative to 1 kHz; 50 kHz deviation)				
	at 5.5 MHz for 2T/20T	–	60	–	dB
	at 5.742 MHz for 2T/20T	–	58	–	dB
$V_{6\text{-}13(RMS)}$	AF output votage AM (RMS value)	440	550	660	mV
(S + W)/W	signal-to-weighted-noise ratio; AM mode	–	56	–	dB
THD	total harmonic distortion; AM mode	–	1	2	%
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3845	16	DIL	plastic	SOT38
TDA3845T	16	SO16	plastic	SOT109A

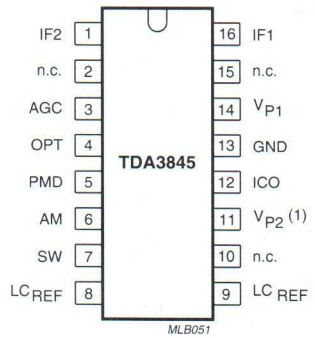


(1) See note 10 to the characteristics.
(2) Not for TDA3845T, pin 11 not connected.

Fig.1 Block diagram.

Quasi split-sound circuit and AM demodulator

TDA3845; TDA3845T



(1) Not for TDA3845T, pin 11 not connected.

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
IF2	1	IF amplifier input 2
n.c.	2	not connected
AGC	3	AGC control capacitor
OPT	4	optional capacitor (see note 10 to the characteristics
PMD	5	peak/mean detector capacitor
AM	6	AM output
SW	7	FM/AM switch
LC_{REF}	8	LC reference circuit for the picture carrier
LC_{REF}	9	LC reference circuit for the picture carrier
n.c.	10	not connected
V_{P2}	11	positive supply voltage 2 (+12 V); note 1
ICO	12	intercarrier output
GND	13	ground (0 V)
V_{P1}	14	positive supply voltage 1 (+5 V)
n.c.	15	not connected
IF1	16	IF amplifier input 1

Note to Pinning

1. Not for TDA3845T, pin 11 not connected.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
	supply voltage			
V_{P1}	pin 14	4.5	8.8	V
V_{P2}	pin 11 (not for TDA3845T)	10.8	13.2	V
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	storage temperature	−25	+125	°C

CHARACTERISTICS

V_{P1} = 5 V (note 11); T_{amb} = 25 °C; all measurements are referenced to ground (pin 13); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
	supply voltage					
V_{P1}	pin 14		4.5	5.0	8.8	V
V_{P2}	pin 11 (not for TDA3845T)		10.8	12.0	13.2	V
I_{tot}	total supply current		–	40	48	mA
IF amplifier						
R_{1-16}	input resistance		–	2	–	kΩ
C_{1-16}	input capacitance		–	2.5	–	pF
$V_{1-16(RMS)}$	minimum IF input voltage (RMS value)	note 1	–	70	100	μV
$V_{1-16(RMS)}$	maximum IF input voltage (RMS value)	note 2	70	100	–	mV
ΔG	gain control range		60	63	–	dB
G_{v3-16}	gain control voltage range		1.5	–	3.0	V
B_{IF}	IF bandwidth	–3 dB	50	70	–	MHz
V_{1-16}	DC potential		–	1.7	–	V
Intercarrier mode (FM mode; standard B/G) notes 3, 4 and 5						
Reference amplifier						
$V_{8-9(p-p)}$	picture carrier amplitude (peak-to-peak value)		–	270	–	mV
R_{8-9}	operating resistance		–	4	–	kΩ
V_{8-9}	DC potential		–	3.9	–	V
Intercarrier mixer and output stage						
$V_{12(RMS)}$	output signal (RMS value)					
	at 5.5 MHz		70	100	–	mV
	at 5.74 MHz		32	45	–	mV
B_{12}	intercarrier bandwidth					
	at –1 dB		–	8	–	MHz
	at –3 dB		–	9	–	MHz
	residual video AM on intercarrier signal	note 6	–	3	10	%
R_{12}	output resistance		–	30	–	Ω
V_{12}	DC potential		–	1.8	–	V
$I_{12(peak)}$	permissable AC output current (peak value)	note 7	–	–	±0.7	mA
I_{12}	permissable DC output current		–	–	–2	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF signal performance (note 8)						
(S + W)/W	black picture		60/58	68/64	–	dB
(S + W)/W	2T/20T pulses with white bars		57/55	60/58	–	dB
(S + W)/W	6 kHz sinewave (black-to-white modulation)		53/51	57/55	–	dB
(S + W)/W	250 kHz square wave (black-to-white modulation)		50/44	56/50	–	dB
AM mode (standard L) note 9						
S/N weighted in accordance with CCIR 468-3						
$V_{6(RMS)}$	AF output signal (RMS value)		440	550	660	mV
B_{AF}	AF bandwith	–3 dB; note 12	0.02	–	120	kHz
THD	total harmonic distortion		–	1	2	%
(S + W)/W	signal-to-weighted-noise ratio	note 10	50	56	–	dB
R_6	output resistance		–	200	–	Ω
V_6	DC potential		–	1.8	–	V
$I_{6(peak)}$	permissable AC output current (peak value)	note 7	–	–	±0.3	mA
I_6	permissable DC output current		–	–	–1	mA
Standard switch (note 4)						
V_7	peak signal AGC (FM mode)	V_{P1} used	1.8	–	V_{P1}	V
V_7	or switch open-circuit	V_{P2} used	1.8	–	5.5	V
V_7	mean signal AGC (AM mode)		–	–	0.8	V
I_7	switch current					
	at 0 V		–	–	–200	μA
	at V_{P1}		–	–	10	μA
	at V_{P2}	via a 2.2 kΩ series resistor	–	–	2.5	mA
Ripple rejection (note 13)						
AM/AF signal						
αRR	voltage ripple on V_P/ voltage ripple on output signal		30	40	–	dB
FM phase noise						
Δf(RMS)	intercarrier signal		–	10	20	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode (standard L) note 9						
S/N weighted in accordance with CCIR 468-3						
$V_{6(RMS)}$	AF output signal (RMS value)		440	550	660	mV
B_{AF}	AF bandwith	−3 dB; note 12	0.02	–	120	kHz
THD	total harmonic distortion		–	1	2	%
(S + W)/W	signal-to-weighted-noise ratio	note 10	50	56	–	dB
R_6	output resistance		–	200	–	Ω
V_6	DC potential		–	1.8	–	V
$I_{6(peak)}$	permissable AC output current (peak value)	note 7	–	–	±0.3	mA
I_6	permissable DC output current		–	–	−1	mA
Standard switch (note 4)						
V_7	peak signal AGC (FM mode)	V_{P1} used	1.8	–	V_{P1}	V
V_7	or switch open-circuit	V_{P2} used	1.8	–	5.5	V
V_7	mean signal AGC (AM mode)		–	–	0.8	V
I_7	switch current					
	at 0 V		–	–	−200	μA
	at V_{P1}		–	–	10	μA
	at V_{P2}	via a 2.2 kΩ series resistor	–	–	2.5	mA
Ripple rejection (note 13)						
AM/AF signal						
αRR	voltage ripple on V_P/ voltage ripple on output signal		30	40	–	dB
FM phase noise						
Δf(RMS)	intercarrier signal		–	10	20	Hz

Notes to the characteristics

1. Start of gain control (LOW IF input signal) at –3 dB intercarrier signal reduction at pin 12, AGC mode set to FM or –3 dB AF signal reduction at pin 6, AGC mode set to AM.
2. End of gain control (HIGH IF input signal) at +1 dB intercarrier signal expansion at pin 12, AGC mode set to FM or +1 dB AF signal expansion at pin 6, AGC mode set to AM.
3. Picture carrier (38.9 MHz) to sound carriers (33.4 MHz/33.158 MHz) ratio: 13/20 dB.

   IF input signal (picture carrier at sync pulse); $V_{1\text{-}16}$ = 10 mV (RMS). Transmitter mode: DSB.

   Reference for the (S + W)/W ratio (0 dB) corresponds to the sound modulation where f = 1 kHz and frequency deviation $\Delta f = \pm 50$ kHz.

   With reduced frequency deviation $\Delta f = \pm 27$ kHz and the (S + W)/W figures will decrease by 5.4 dB.
4. If the device is used only for the B/G standard (no AM), the capacitor at pin 5 can be omitted (pin 5 has to be disconnected). In this event the AGC will always operate as a peak signal AGC and is independent of the voltage at pin 7.

   The AM mode can also be used for the B/G standard, consequently standard switching is not required. However, the intercarrier level depends on the video modulation and the AF performance may decrease.

   When the IC is operated from a 12 V power supply pin 7 can be connected to a 12 V logic level via a 2.2 kΩ resistor.
5. LC reference circuit for the picture carrier (pins 8 and 9); 68 pF/0.247 µH; in series with 27 pF:

   Q loaded = 40 (Qo = 90); tuned to 38.9 MHz yields quadrature demodulation for the picture carrier which provides optimum video suppression at the intercarrier output (e.g. black-to-white jump of the video modulation.

   The series capacitor provides a notch at the sound carrier frequency in order to produce more attenuation for the sound carrier in the PC reference channel. The ratio of parallel to series capacitance depends on the ratio of picture to sound carrier frequency which has to be adapted to other TV transmission standards, if required, in accordance with the formula:

   $C_S = C_P(f_{PC}/f_{SC})^2 - C_P$

   Where:

   C_S = series capacitor

   C_P = parallel capacitor

   f_{PC} = picture carrier frequency

   f_{SC} = sound carrier frequency

   The result is an improved 'intercarrier buzz' in the stereo system B/G, particularly with 250 kHz video modulation (up to 10 dB improvement in sound Channel 2), or to suppress 350 kHz video modulated beat in the digitally modulated NICAM subcarrier.

   In order to optimize the AF signal performance, fine tuning to the optimum S/W at the sound Channel 2 may be achieved by a 250 kHz video modulated square wave.
6. Residual video AM is defined as:

   m = (A-B)/A

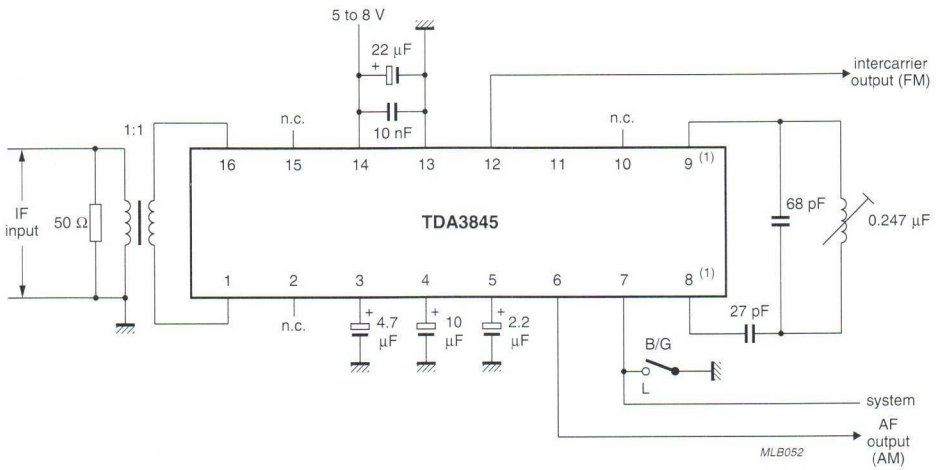
   A = intercarrier level at sync pulse

   B = intercarrier level at 100% white video modulation
7. If higher AC output current is required an external resistor must be be connected between the output pin and ground in order to increase the bias current of the emitter follower. The permissable maximum DC output current must not be exceeded.

8. For all S/N measurements the used vision IF modulator must conform to the following:

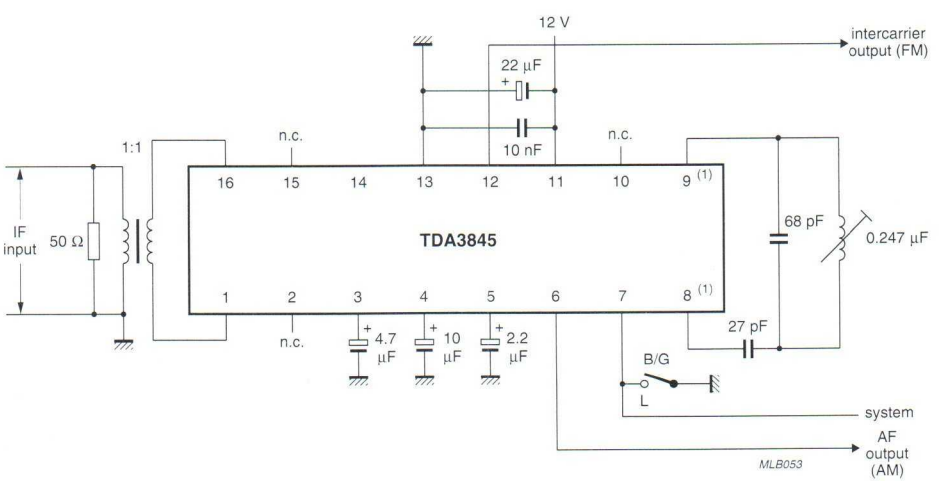
   Incidental phase modulation for black-to-white jump should be less than 0.5 degrees. Intercarrier performance, measured with the television demodulator AMF2 (intercarrier mode weighted S/N ratio) better than 60 dB for 6 kHz sinewave black-to-white video modulation. Weighted S/N ratio of the demodulated intercarrier signals in accordance with CCIR 468-3, measured with de-emphasis of 50 μs.

   The indicated (S + W)/W ratio X/Y concerns the sound channels 1 and 2 that means demodulated intercarrier signals of 5.5 and 5.74 MHz respectively.
9. Sound carrier frequency in the range of 30 to 40 MHz modulated with f = 1 kHz and a modulation depth of 80%. IF input signal (sound carrier) $V_{1\text{-}16}$ = 10 mV (RMS).
10. The capacitor at pin 4 can be omitted, however, the (S + W)/W figure for the AM sound (standard L) will be up to 8 dB worse in the IF voltage range 1 mV to 100 mV.
11. When the supply at V_{P2} = 12 V the performance will be comparable with the performance when V_{P1} = 5 to 8 V. The power supply pin that is not in use should be disconnected.
12. The maximum value given as minimum 120 kHz and typical 700 kHz.
13. Voltage ripple < 200 mV (p-p) at 70 Hz.



(1) See note 5 to the characteristics.

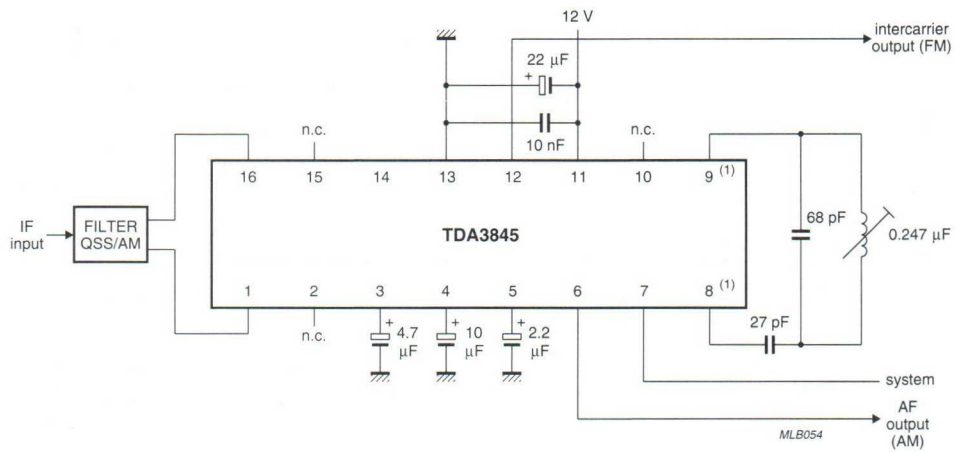
Fig.3 Test circuit for the +5 V supply.



(1) See note 5 to the characteristics.

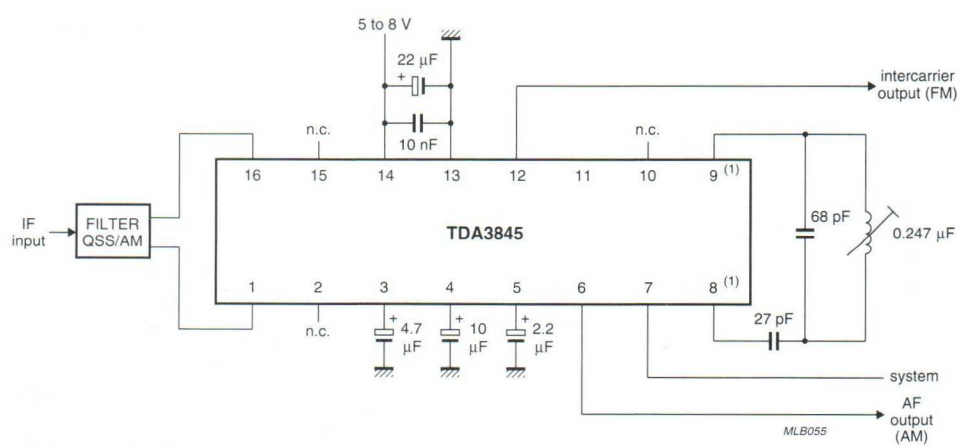
Fig.4 Test circuit for the +12 V supply; not for TDA3845T.

APPLICATION INFORMATION



(1) See note 5 to the characteristics.

Fig.5 Application diagram for the +12 V supply; not for TDA3845T.



(1) See note 5 to the characteristics.

Fig.6 Application diagram for the +5 V supply.

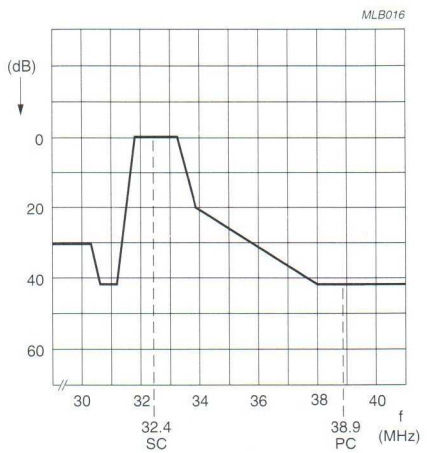


Fig.7 AM IF filter for standard L.

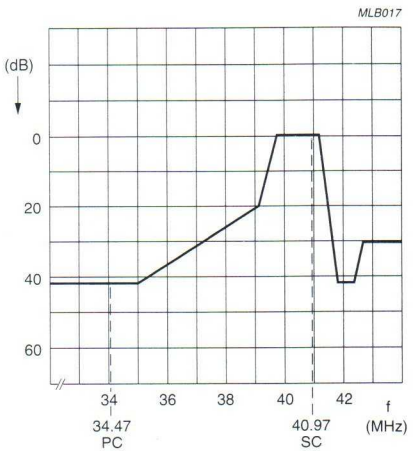


Fig.8 AM IF filter for standard L-accent.

IF filter proposal for AM sound (see Figs 7 and 8)

With an IF filter in accordance with this proposal, the video buzz suppression on the audio output is better than 50 dB (in accordance with CCIR 468-3, m = 54%) for the worst case video modulation with 6 kHz sinewave black-to-white.

Note to figures 7 and 8.

Where SC = sound carrier and PC = picture carrier.

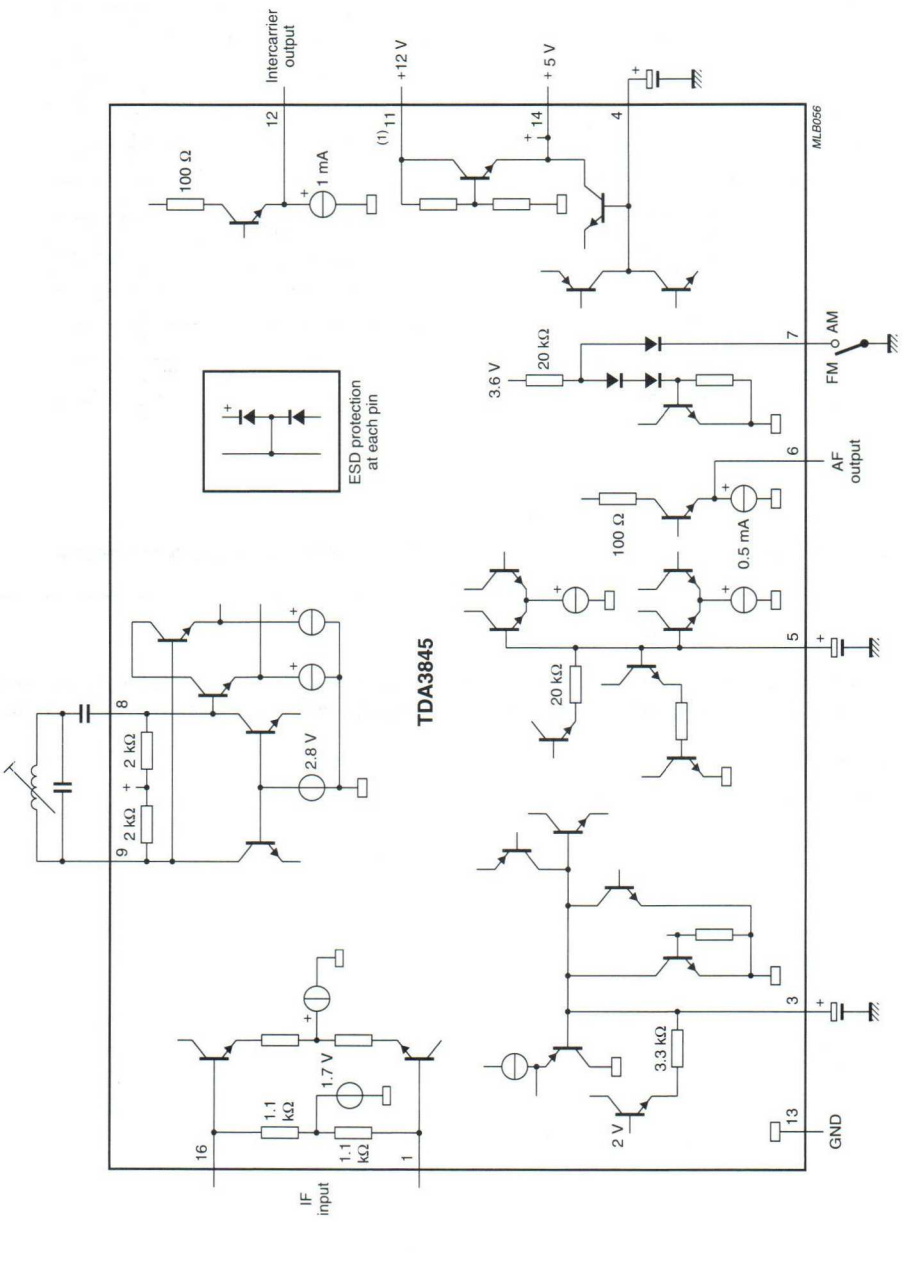
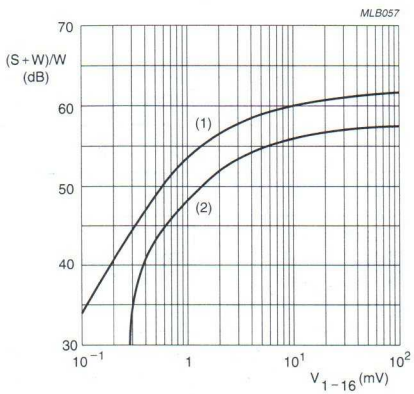


Fig.9 Internal pin circuitry.



Picture modulation; 6 kHz sinewave.
Intercarrier signal; sound Channel 1 = 5.5 MHz, sound Channel 2 = 5.74 MHz.

Fig.10 Response curve of the signal-to-weighted noise ratio of the demodulated intercarrier signal.

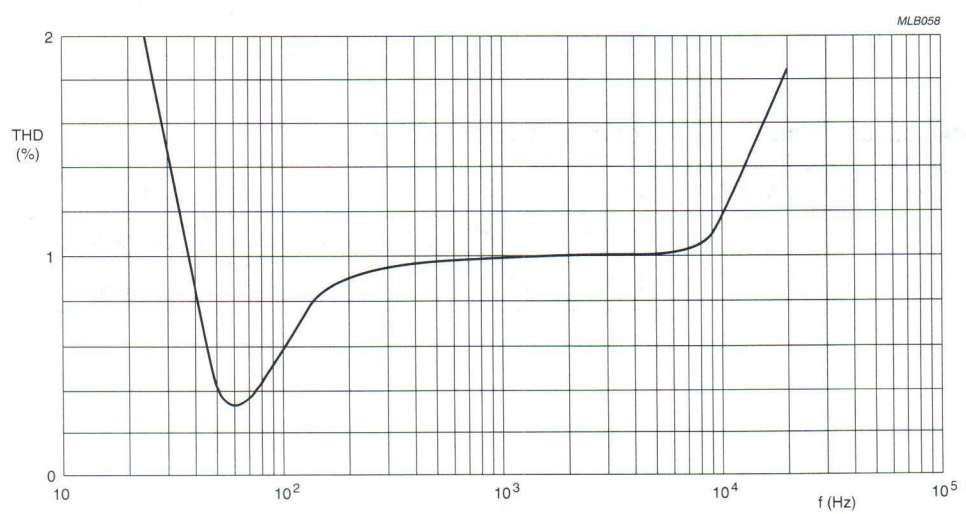


Fig.11 Response curve for the total harmonic distortion of the AM signal.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3853T

TV IF amplifier and demodulator with TV-identification

FEATURES

- Suitable for standards B/G (I, M, N, DK), see Table 1
- Gain controlled 3-stage IF amplifier with typically 80 MHz bandwidth
- High performance synchronous demodulator for negative and positive video modulation; passive regeneration of the reference signal
- Peak-sync-related AGC
- AGC output voltage take over point adjustable
- High sensitive TV identification based on vertical pulse duty cycle recognition; IDENT output
- Video off switch
- Sound trap buffer amplifier
- Tracking generator (AFT output) with Q-demodulator and internal 90 degree phase shifter for tracking the reference circuit
- Low supply voltage 5 V, low power consumption

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.75	5	6	V
I_P	supply current	-	46	-	mA
V_i	vision IF input signal sensitivity (RMS value, pins 1-20)	-	70	100	µV
	maximum vision IF input signal (RMS value, pins 1-20)	100	-	-	mV
G_v	IF gain control range	63	66	-	dB
$V_{o\ CVBS}$	buffered CVBS output signal on pin 12 (peak-to-peak value)	1.7	2	2.3	V
B	–3 dB video bandwidth (pin 12)	-	14	-	MHz
S/N	signal-to-noise ratio for video	55	60	-	dB
$\alpha_{1.1}$	intermodulation attenuation at yellow	53	56	-	dB
$\alpha_{3.3}$		60	-	-	dB
α_{spur}	suppression of spurious harmonics of video signal	22	26	-	dB
T_{amb}	operating ambient temperature	0	-	70	°C

GENERAL DESCRIPTION

Monolithic integrated circuit for vision IF signal processing in TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3853T	20	mini-pack	plastic	SOT163A

TV IF amplifier and demodulator with TV-identification

TDA3853T

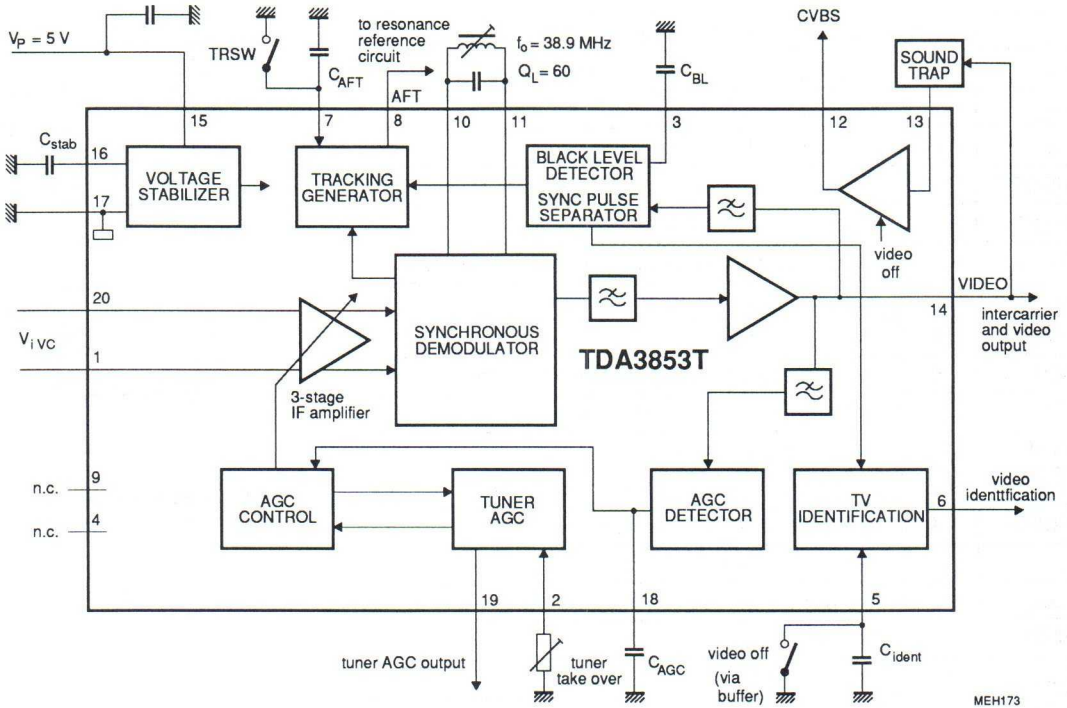


Fig.1 Block diagram.

TV IF amplifier and demodulator with TV-identification

TDA3853T

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,a}$	1	balanced vision IF input a
TOP	2	tuner AGC take over adjustment point (TOP)
C_{BL}	3	capacitor for black level
n.c.	4	not connected
VIDOFF	5	video off input, identification capacitor
IDENT	6	TV identification output
TRSW	7	set input for tracking switch, tracking hold capacitor
AFT	8	automatic frequency tracking output
n.c.	9	not connected
RES1	10	resonance reference circuit for vision carrier
RES2	11	resonance reference circuit for vision carrier
CVBS	12	CVBS output (positive)
TRAP	13	video buffer amplifier input from sound trap
VIDEO	14	video and sound intercarrier output
V_P	15	+5 V supply voltage
C_{stab}	16	decoupling capacitor for voltage stabilizer
GND	17	ground (0 V)
C_{AGC}	18	capacitor for AGC
AGC	19	AGC output to tuner
$V_{i\,b}$	20	balanced vision IF input b

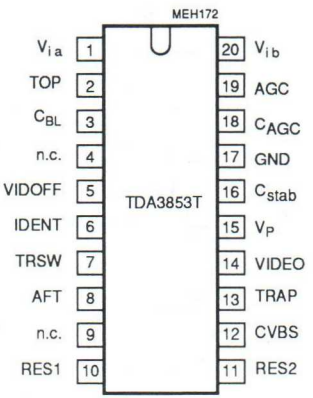


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3853T is a TV IF amplifier/demodulator for negative modulation.

The IF input signal is amplified, gain-controlled and demodulated (Fig.1).

Vision IF amplifier and demodulator

The vision IF amplifier consists of three AC-coupled differential amplifiers. Gain control is achieved by current divider stages. Emitter feedback resistors in the differential amplifiers are optimized with respect to noise and signal capability.

Synchronous demodulator

The demodulator has a reference amplifier consisting of a differential amplifier with resistive load to provide passive vision carrier regeneration. This allows capacitive coupling of the resonance circuit to obtain a notch filter characteristic and tracking of the resonance circuit.
A cascaded limiter amplifier follows the reference amplifier to eliminate amplitude modulation. The limited IF reference signal is fed to the demodulator. The unlimited IF signal is fed via a phase correction network to the demodulator. The video amplifier is an operational amplifier with a wide bandwidth and internal feedback . The video and sound intercarrier signal is output on pin 14.

TV IF amplifier and demodulator with TV-identification

TDA3853T

Video buffer amplifier

This operational amplifier has a wide bandwidth with internal feedback and frequency compensation. Gain and input impedance are adapted to operate with a ceramic sound trap. The switching functions are described in Table 1.

AGC detector and IF gain control

The video signal is fed through low-pass filters to attenuate the sound carriers and then is fed to the AGC detector.

Peak-sync AGC detection.
A special network provides current pulses to fast charge the AGC capacitor on pin 18 (gain reduction). This achieves a minimum of video distortion.
The AGC control converts the AGC capacitor voltage to three separate voltages to control the IF stages.

Sync pulse separator

The sync pulse separator separates the composite sync signal to gate the AFT. The vertical sync is used for identification. The input is band-limited to obtain a higher ident sensitivity.

Table 1 Switching functions of TDA3853T.

	VIDOFF pin 5	TRSW pin 7	video signal	IDENT pin 6
pin setting	L 2.2 µF	L* L*	video OFF video ON	0.5 mA sink H or 0.5 mA sink

* capacitor on pin 7 means tracking active; LOW means tracking inactive

Tuner AGC

The tuner AGC output current is fed to the open-collector output on pin 19. The take-over point is adjusted externally at pin 2 to adapt the tuner and SAW filter to an optimum IF input level. The IF gain variation over the full tuner gain range (slip) is minimized to ensure a constant tuner output signal.

Identification

An analog integrating network followed by a window comparator identifies the video signal by detection of the duty cycle of the vertical sync pulses. The pulses charge the identification capacitor on pin 5.

Tracking generator (AFT)

A limited 90 degree phase-shifted vision carrier signal is fed to the AFT quadrature demodulator, internal RC networks provide active phase shifting. The linear IF signal is applied to the other AFT quadrature demodulator input. The AFT output signal is applied to a gating stage. Gating with the composite sync pulses activates the AFT demodulator. Therefore the AFT output is free from video modulation. The AFT capacitor (pin 7) is charged by the gated AFT current. The capacitor voltage is converted to an DC output current on pin 9 (open-collector sink/source currents).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	6.0	V
I_P	supply current on pin 15	-	55	mA
V_n	voltage on pins 6, 8 and 12	−0.3	V_P	V
$V_{5,7}$	voltage on pins 5 and 7	−0.3	5.5	V
V_{13}	voltage on pin 13	−0.3	5.0	V
V_{14}	voltage on pin 14	−0.3	4.2	V
V_{19}	voltage on pin 19	−0.3	13.2	V
$I_{2,16}$	current on pins 2 and 16	-	−200	μA
$I_{5,6}$	current on pins 5 and 6	-	−60	μA
I_7	current on pin 7	-	−100	μA
I_8	current on pin 8	-	−50	μA
I_{12}	current on pin 12	-	−10	mA
I_{14}	current on pin 14	-	−3	mA
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins**	-	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Pins 1, 10, 11 and 20 have special protection, the other pins have standard protection by diodes to V_P and GND (this excludes pins 15 (V_P) and 19 (tuner AGC output) which have standard protection to GND only).

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C, f_{VC} = 38.9 MHz; V_{iIF} = 10 mV rms; DSB video modulation; sync level for B/G.
Measurements taken in Fig.3 without notch components and video signal according to Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5	6	V
I_P	supply current		-	46	55	mA
Standard set inputs (Table 1)						
V_{IL}	input voltage LOW, pins 5 and 7		0	-	0.8	V
Vision IF input (pins 1-20)						
V_i	input signal sensivity (RMS value)	–1 dB video	-	70	100	µV
	maximum input signal (RMS value)	+1 dB video; note 1	100	-	-	mV
G_v	IF gain control range	Fig.6	63	66	-	dB
B	IF bandwidth	–3 dB	-	80	-	MHz
R_i	input resistance		-	2	-	kΩ
C_i	input capacitance		-	1.5	-	pF
V_I	DC voltage on pins 1 and 20		-	2.50	-	V
Synchronous demodulator (pins 10 and 11)						
$V_{o\ ref}$	picture carrier amplitude, pins 10-11 (peak-to-peak value)		-	1.6	-	V
R_{10-11}	integrated operating resistance		-	12	-	kΩ
$R_{L\ 10-11}$	load resistance		tbn	-	-	kΩ
Q_L	load Q-factor of resonance circuit; note 2	no notch components	55	60	-	
$V_{10,\ 11}$	DC voltage		-	2.8	-	V
Composite video output (pin 14)						
V_o	output signal (peak-to-peak value)		0.9	1.0	1.1	V
V_{14}	sync level		-	1.5	-	V
	ultra-white level		-	2.63	-	V
	upper video clipping level		-	4.3	-	V
	lower video clipping level		-	0.3	-	V
R_{14}	output resistance		-	-	10	Ω
I_{14}	output current	DC and AC	-	-	±1	mA
B	–1 dB video bandwidth	C_{14} < 20 pF	tbn	10	-	MHz
	–3 dB video bandwidth	C_{14} < 20 pF	tbn	14	-	MHz
RR	ripple rejection on pin 14	f_{ripple} = 70 Hz; note 3	tbn	30	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS buffer amplifier (pins 12 and 13)						
R_{13}	input resistance		-	3.3	-	kΩ
C_{13}	input capacitance		-	2	-	pF
$V_{o\ CVBS}$	typical CVBS output signal on pin 14 (peak-to-peak value)	note 4	-	2	-	V
	CVBS output level	upper video clipping	-	4.25	-	V
		lower video clipping	-	0.3	-	V
		sync level	-	1.35	-	V
I_{12}	output current	DC and AC	-	-	±1	mA
R_{12}	output resistance		-	-	10	Ω
G_v	voltage gain	note 4	6.5	7	7.5	dB
B	–3 dB video bandwidth	C_{14} < 20 pF	tbn	14	-	MHz
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	35	-	dB
Measurements from IF input to CVBS output (pin 12)						
$V_{o\ CVBS}$	typical CVBS output signal on pin 12 (peak-to-peak value)	Fig.10	1.7	2	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	-	-	0.5	dB
		30 dB gain control	-	0.1	-	dB
ΔG	differential gain	10 to 90% modulation	-	2	5	%
Δφ	differential phase	10 to 90% modulation	-	2	5	°
$tilt_H$	horizontal tilt		-	0.7	1.5	%
B	–2 dB video bandwidth	C_L < 20 pF	tbn	12	-	MHz
S/N	signal-to-noise ratio	note 5; Fig.5	-	58	-	dB
$\alpha_{1.1}$	intermodulation at "blue", note 6	f = 1.1 MHz; Fig.8	56	58	-	dB
	intermodulation at "yellow"	f = 1.1 MHz	53	56	-	dB
$\alpha_{3.3}$	intermodulation at "blue"	f = 3.3 MHz	62	-	-	dB
	intermodulation at "yellow"	f = 3.3 MHz	60	-	-	dB
α_{1H}	residual vision carrier (RMS value)	fundamental wave	-	1	10	mV
α_{2H}		second harmonic	-	1	10	mV
α_{spur}	suppression of spurious video signal harmonics	transformer; Fig.4	22	26	-	dB
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	30	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector (pin 18)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal		-	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		-	150	300	ms
V_{18}	gain control voltage on capacitor	full gain range	1.5	-	4	V
I_{18}	peak charging current (peak value)		-	–2	-	mA
	charging current		-	–0.5	-	mA
	discharging current		-	11	-	μA
Tuner AGC (pin 19)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1-20	-	-	1	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1-20	50	-	-	mV
ΔG_{IF}	IF gain variation	maximum ΔI_{AGC} = 1 mA	-	3	6	dB
V_{19}	permitted output voltage	from external	-	-	13.2	V
	saturation voltage	I_{19} = 1 mA	-	0.2	0.5	V
ΔV_{19}	variation of take over point by temperature	ΔT = 60 °C	-	2	3	dB
I_{19}	sink current	no tuner gain reduction; Fig.7	-	0	0.1	μA
		maximum tuner gain reduction	1.5	1.8	2.0	mA
RR	ripple rejection on pin 19	f_{ripple} = 70 Hz; note 3	tbn	20	-	dB
TV identification and black level detector (pins 5, 6 and 3)						
V_i	IF input signal on pins 1-20 (RMS value)	TV identified	-	50	-	μV
C/N	carrier-to-noise ratio at IF input	TV identified; note 7	-	10	-	dB
V_{14}	minimum sync amplitude in relation to typical sync	identification on	-	30	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_6	output voltage for TV identified		4.5	4.95	V_P	V
	output voltage for TV not identified	I_7 = 500 µA	-	0.1	0.4	V
I_6	output current (sink)	no ident	-	500	-	µA
	allowed leakage current (source)	ident	-	-	−1	µA
V_5	voltage for "identification on"	2.2 µF capacitor on pin 5	-	2.6	-	V
I_{leak}	permitted leakage current (capacitor pin 5)		-	-	3	µA
$t_{p\ V}$	vertical pulse duty cycle for TV identified	$t_{sync}/t_{vertical}$	4	8	25	10^{-3}
Tracking generator, AFT (pins 7 and 8)		note 8				
V_8	maximum output voltage	note 9; Fig.9	4.3	-	4.7	V
	minimum output voltage		0.3	-	0.7	V
	permitted output voltage		-	-	V_P	V
I_8	sink output current		160	180	220	µA
	source output current		−160	−180	−220	µA
	offset output current		-	-	±20	µA
S	control steepness	$\Delta I_9/\Delta f$; note 9	-	2	-	µA/kHz
$\Delta\varphi$	phase offset spread for 38.9 MHz	note 10	-	-	±4	°
V_7	input voltage for TRSW	tracking off; Table 1	0	-	0.8	V
	(independent of other mode switches)	tracking on	open-circuit			V

Notes to the characteristics

1. Video signal is still gain controlled with 2 V (p-p) on output ; but intermodulation figures are lowered.
2. AFT characteristic depends on Q-factor.
3. Ripple rejection for f = 50 to 100 Hz.
4. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). When no sound trap is applied, a 330 Ω resistor must be connected from output to input (from pin 14 to pin 13).
5. S/N is the ratio of the black-to-white amplitude (pin 12) and the RMS value of noise (black, pin 12). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.

6. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal.
   $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
7. The carrier-to-noise ratio at IF input for "TV identified" is defined as the ratio of carrier (top sync, RMS value) and noise (RMS value). Conditions: 5 MHz bandwidth; V_{iIF} = 10 mV RMS (top sync) and a video signal of 2T + 20T + white bar.
8. A current source output is provided to match the AFT output signal to the different tuning systems. The internal 90 degrees phase shifter is matched for f_o = 38.9 MHz.
9. The AFT characteristic depends on Q_L of the resonance circuit (Q_L = 60, without notch components).
10. ±4 ° corresponds to ±23 kHz for Q_L as in Fig.1 (refer to note 9).

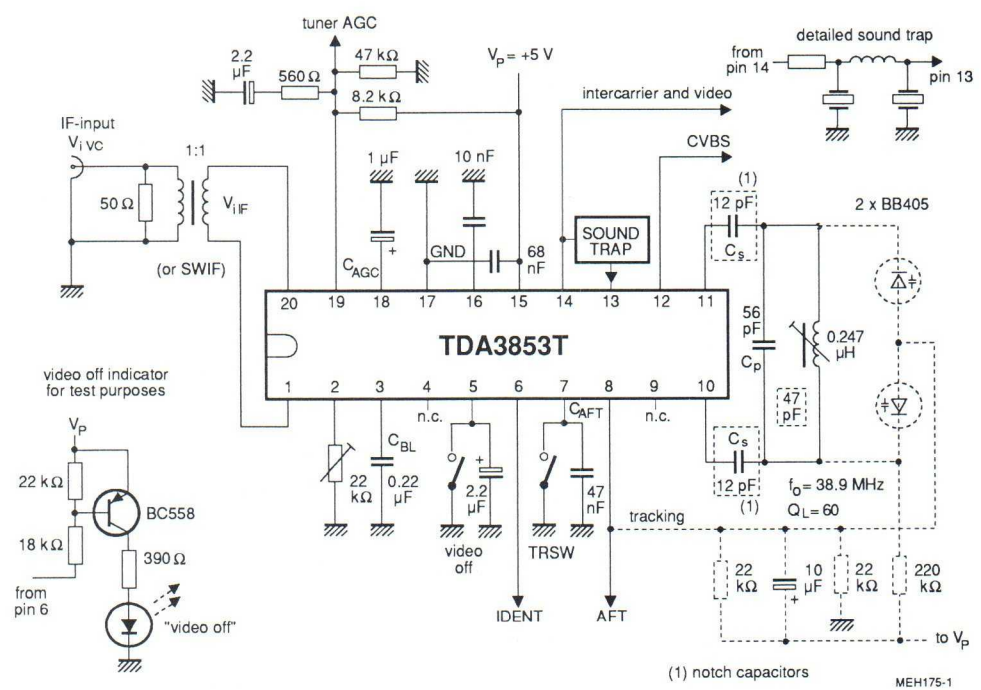


Fig.3 Test and application circuit. Test circuit without notch capacitors and with sound trap replaced by a 330 Ω resistor. Dashed components for tracking application only; application circuit with SWIF.

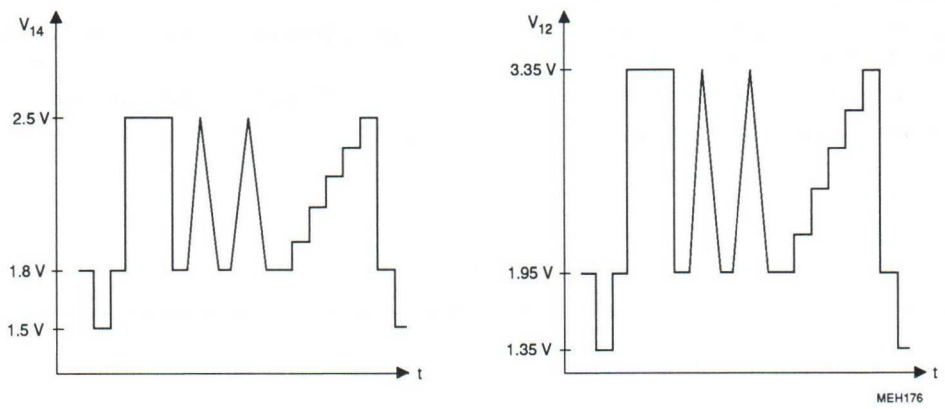


Fig.4 Video test signals.

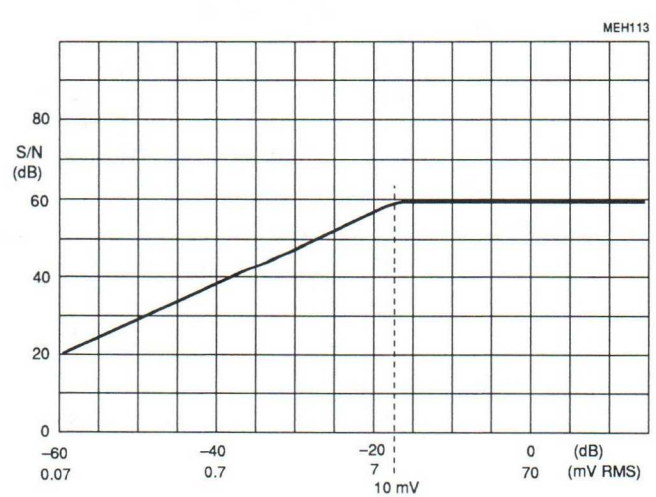


Fig.5 Signal-to-noise ratio (typical) as a function of IF input signal.

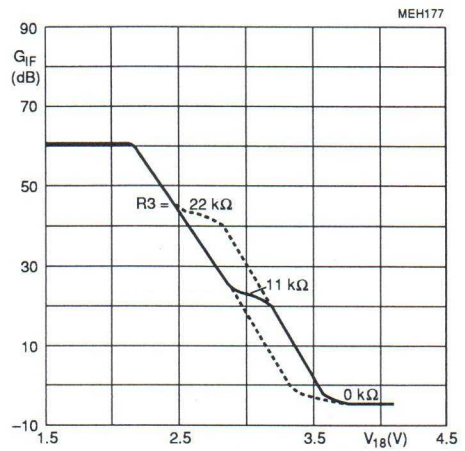


Fig.6 IF gain as a function of adjustment at pin 2.

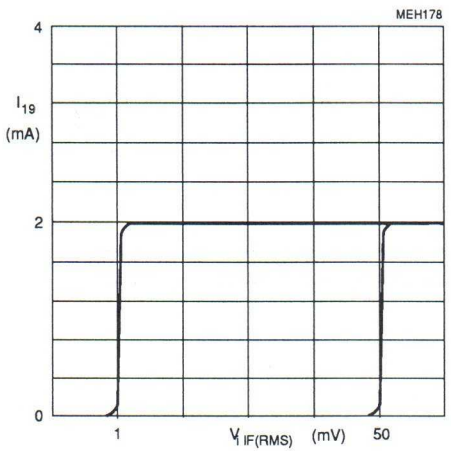
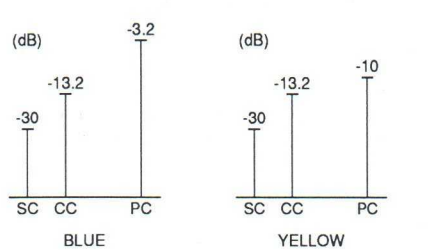


Fig.7 Tuner AGC characteristic.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound trap attenuation: 17 dB.

MEH114

Fig.8 Input conditions for intermodulation measurements.

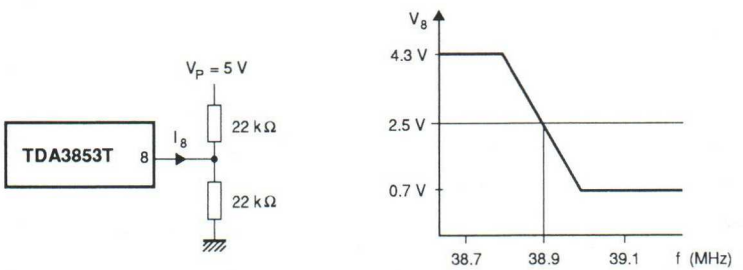


Fig.9 AFT characteristic.

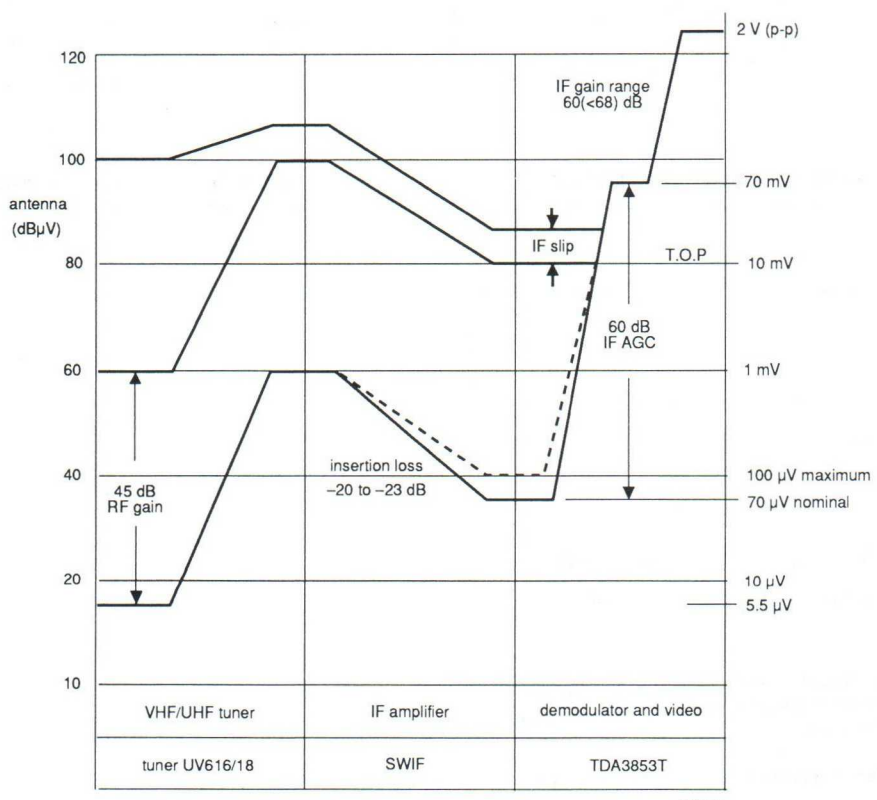


Fig.10 Front end level diagram.

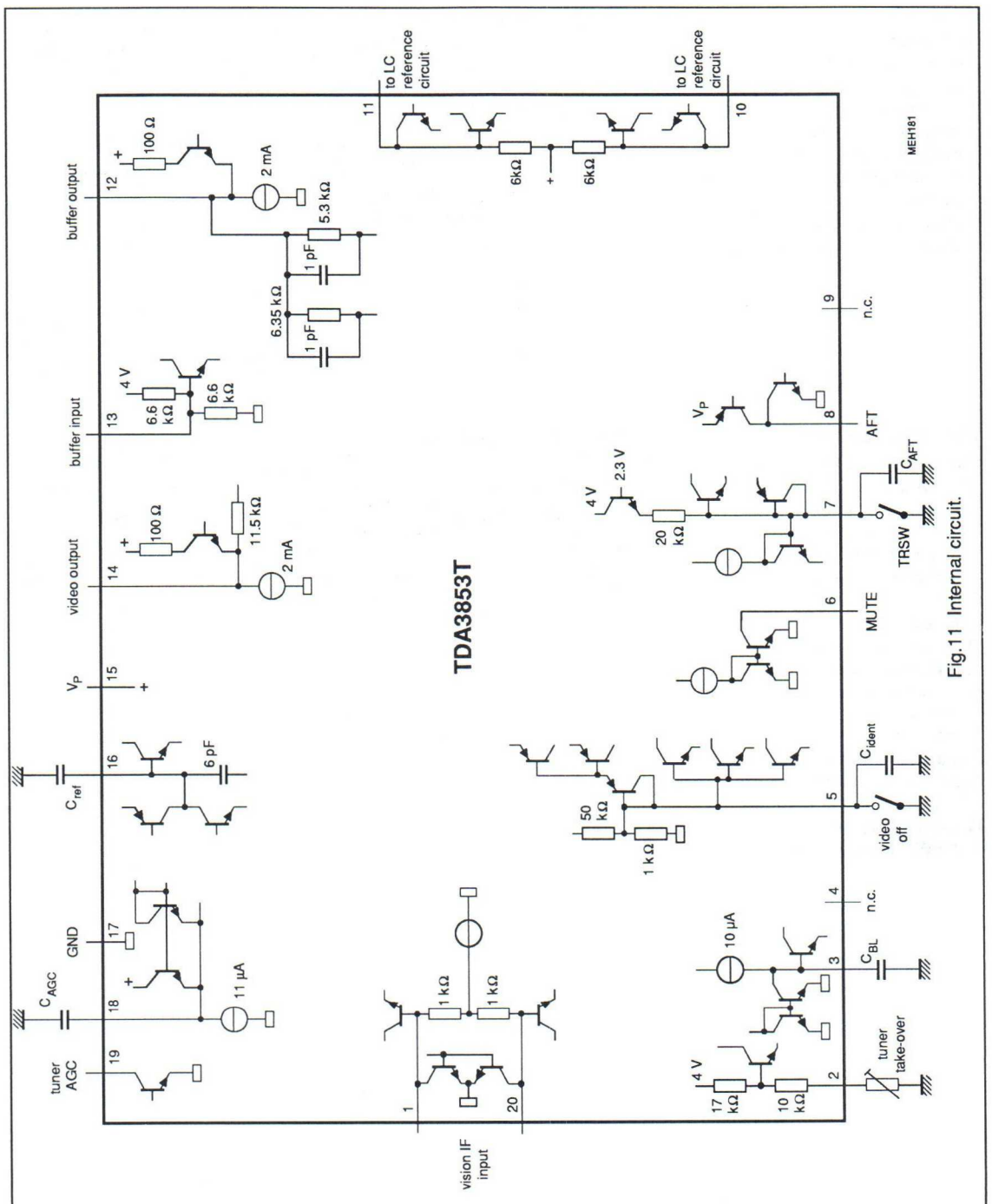


Fig.11 Internal circuit.

Quasi-split sound processor for all standards TDA3856

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	–	60	72	mA
$V_{i\,IF}$	IF input sensitivity (–3 dB)	–	70	100	μV
$V_{o\,(RMS)}$	audio output signal for FM (B/G)	–	1	–	V
$V_{o\,(RMS)}$	audio output signal for AM (L)	–	0.6	–	V
THD	total harmonic distortion				
	for FM	–	0.5	–	%
	for AM	–	1	–	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	–	68	–	dB
	for AM	–	56	–	dB

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.
Gain controlled wideband IF amplifier, input select switch.
AGC generation due to peak sync for FM or mean signal level for AM.
Reference amplifier for the regeneration of the vision carrier.
Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.
Intercarrier mixer for FM sound, output with low-pass filter.
Separate signal processing for 5.5 and 5.74 MHz intercarriers.
Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3856	24	shrink DIL	plastic	SOT234
TDA3856T	24	SO	plastic	SOT137

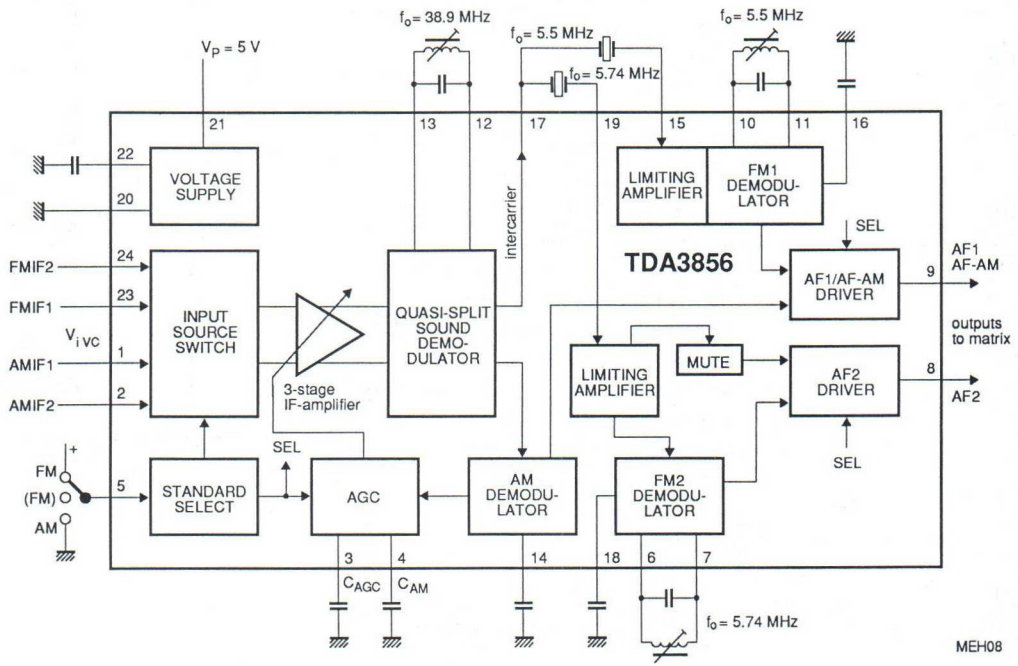


Fig.1 Block diagram (B/G and L).

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard (32.4 MHz)
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5.74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 to +8 V supply voltage
C_{REF}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

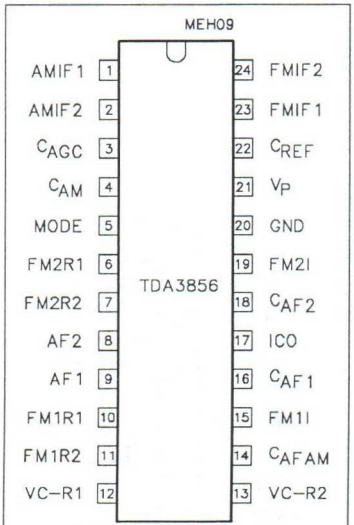


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all standards. Dependent on the voltage at pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode)

Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2.

Muting

With no sound carrier SC2 at pin 19, AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV at pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise at pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise at pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder, when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode)

Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

Sound carrier notch filter for an improved intercarrier buzz

The series capacitor C_S in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$C_S = C_P (fvc/fsc)^2 - C_P$.

The result is an improved intercarrier buzz (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.

Intercarrier buzz fine tuning with 250 kHz square wave video modulation

The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators

For all signal-to-noise measurements the generator must meet the following specifications: phase modulation errors < 0.5° for B/W-jumps

intercarrier signal-to-noise ratio as measured with 'TV-demodulator AMF2' (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 21)	–	8.8	V
V_I	voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	650	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling (note 1)			
	all pins except pins 1, 2, 23 and 24	±500	–	V
	pins 1, 2, 23 and 24	+400	–	V
		–500	–	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = +25 °C; measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals, modulation depth 100% (proportional to 10% residual carrier).
Vision carrier amplitude (RMS value) $V_{i\,VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards B/G (FM) with automatic muting	pin 5 connected	2.8	–	V_P	V
		pin 5 open-circuit	–	2.8	–	V
	B/G (FM) without muting	pin 5 connected or alternative measure: 22 kΩ to GND	1.3	–	2.3	V
	L (AM sound)	pin 5 connected	0	–	0.8	V
I_5	input current	$V_5 = V_P$	–	–	100	μA
		V_5 = 0 V	–	–	–300	μA
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		–	–	100	Ω
V_I	DC input voltage (pins 1, 2 or 23, 24)	LOW set internally	–	–	0.1	V
$\alpha_{12\text{-}13}$	crosstalk attenuation of IF input switch	note 1	50	56	–	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		1.8	2.2	–	kΩ
C_I	input capacitance		–	2.0	2.6	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		–	1.75	–	V
$V_{i\,IF\,(RMS)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	–	mV
	input signal sensitivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction at pin 17	–	70	100	μV
	input signal sensitivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction at pin 9	–	70	100	μV
V_3	voltage for gain control (pin 3)		1.7	–	2.6	V
ΔG_v	IF gain control		60	63	–	dB
B	IF bandwidth	–3 dB	50	70	–	MHz
Resonance amplifier (pins 12-13)						
$V_{o\,(p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	–	270	–	mV
$R_{12\text{-}13}$	operating resistance		–	4	–	kΩ
L	inductance	Figs 3 and 5	–	0.247	–	μH
C	capacitance		–	68	–	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	–	40	–	
$V_{12,\,13}$	DC voltage (pins 12 and 13)		–	V_P – 1	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 17)						
$V_{o\,(RMS)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	6	8.5	–	MHz
		–3 dB	7	10	–	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	–	3	10	%
$V_{VC\,(RMS)}$	residual vision carrier (RMS value)	1st/2nd harmonic (38.9/77.8 MHz)	–	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	–	30	–	Ω
I_o	allowable AC output current (pin 17)		–	–	±0.7	mA
I_{17}	allowable DC output current		–	–	–2	mA
V_{17}	DC voltage	LC-circuit at pin 12, 13 adjusted to minimum video content at pin 17	1.5	1.75	2.0	V
Limiting amplifiers (pins 15 and 19)						
$V_{i\,(RMS)}$	minimum input signal (RMS value)	–3 dB AF signal	–	300	450	μV
	maximum input signal (RMS value)		200	–	–	mV
$R_{15,\,19}$	input resistance		450	560	700	Ω
$V_{15,\,19}$	DC voltage		–	0	–	V
$V_{i\,(RMS)}$	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	0.8	1.2	1.7	mV
ΔV_i	hysteresis of level detector		4	7	12	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\,IF\,(RMS)}$ = 10 mV (f_{mod} = 1 kHz, deviation Δf = ±50 kHz) at pins 15 and 19 without ceramic filters, R_S = 50 Ω. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11 (including IC).						
$V_{IC\,(RMS)}$	intercarrier signals (RMS values, pins 6-7 and 10-11)		–	100	–	mV
V	DC voltage (pins 6, 7, 10 and 11)		–	1.8	–	V
$V_{o\,(RMS)}$	AF output signals (RMS values, pins 8 and 9)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		–	–	1	dB
$R_{8,\,9}$	output resistance		75	100	130	Ω
$V_{8,\,9}$	DC voltage		1.8	2.1	2.4	V
$I_{8,\,9\,(M)}$	allowed AC current of emitter output (peak value)	note 3	–	–	±1.5	mA
$I_{8,\,9}$	maximum allowed DC output current		–	–	–2	mA
THD	total harmonic distortion		–	0.5	1.0	%
$V_{o\,(RMS)}$	AF output signal (RMS value)	THD = 1.5%	1.25	–	–	V
α_{AM}	AM suppression	1 kHz; m = 0.3	48	54	–	dB
S/N(W)	weighted signal-to-noise ratio	CCIR468-3	64	68	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	AF bandwidth (–3 dB)					
	lower limit		–	–	20	Hz
	upper limit		100	–	–	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	–	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		–	1.8	–	V
AM demodulator V_5 = 0 V (AM mode) input signals at pins 1-2: SC = 32.4 MHz; f_{mod} = 1 kHz; m = 0.8; $V_{i\,AM\,(RMS)}$ = 10 mV						
$V_{o\,(RMS)}$	AF output signal at pin 9 (RMS value)		530	600	675	mV
R_9	output resistance (pin 9)		75	100	130	Ω
$I_{o\,(M)}$	maximum AC output current (peak value)	note 3	–	–	±1.5	mA
I_9	maximum DC output current		–	–	–2	mA
V_9	DC voltage		1.8	2.1	2.4	V
THD	total harmonic distortion	Fig.4	–	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR468-3	50	56	–	dB
B	AF bandwidth (–3 dB)					
	lower limit		–	–	20	Hz
	upper limit		100	–	–	kHz
V_{14}	DC voltage (pin 14)		–	2	–	V
AF signal switches input signals: AM carrier into pin 1, 2 — see part AM demodulator; FM intercarrier into pin 15 — see part FM demodulator; no signal in pin 19 (AF2) the output signals are related to the signals described in the demodulator parts.						
V_o/V_{omute}	AF2 mute attenuation (pin 8)	B/G mode; $V_5 = V_P$	70	–	–	dB
V_{oAM}/V_{oFM}	AF1 AM signal (pin 9) attenuation of unwanted FM signal	L mode; V_5 = 0; FM: modulated; AM: unmodulated	70	–	–	dB
V_{oFM}/V_{oAM}	AF1 FM signal (pin 9) attenuation of unwanted AM signal	B/G mode; $V_5 = V_P$; FM: unmodulated; AM: modulated	70	–	–	dB
$dV_{8, 9}$	DC jump at the AF outputs	switching to FM or AM sound or Mute	–	5	25	mV
AF performance for FM operation (standard B/G) input signals: B/G IF input signal (pin 23, 24); unmodulated sound carriers; different video modulation (100%) the output signals are related to the signals described in the demodulator parts.						
(S+N)/N(W)	weighted signal-to-noise ratio	CCIR468-3; de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	–	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.5 MHz	50	54	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	black picture	f_i = 5.742 MHz	57	61	–	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.742 MHz	48	52	–	dB
Ripple rejection of the AF outputs (B/G and L standard)						
RR	ripple rejection V_{ripple} on V_P / V_{ripple} on V_{out}	$V_{R(p-p)}$ = 200 mV; f_R = 70 Hz	30	40	–	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at R_{12-13} = 470 Ω (instead of LC circuit); input signal $V_{i\,(RMS)}$ = 20 mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\,(RMS)}$ = 20 mV (pins 12-13). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A – B)/A (A = signal at sync; B = signal with 100% picture modulation).
3. For larger current: R_L > 2.2 kΩ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

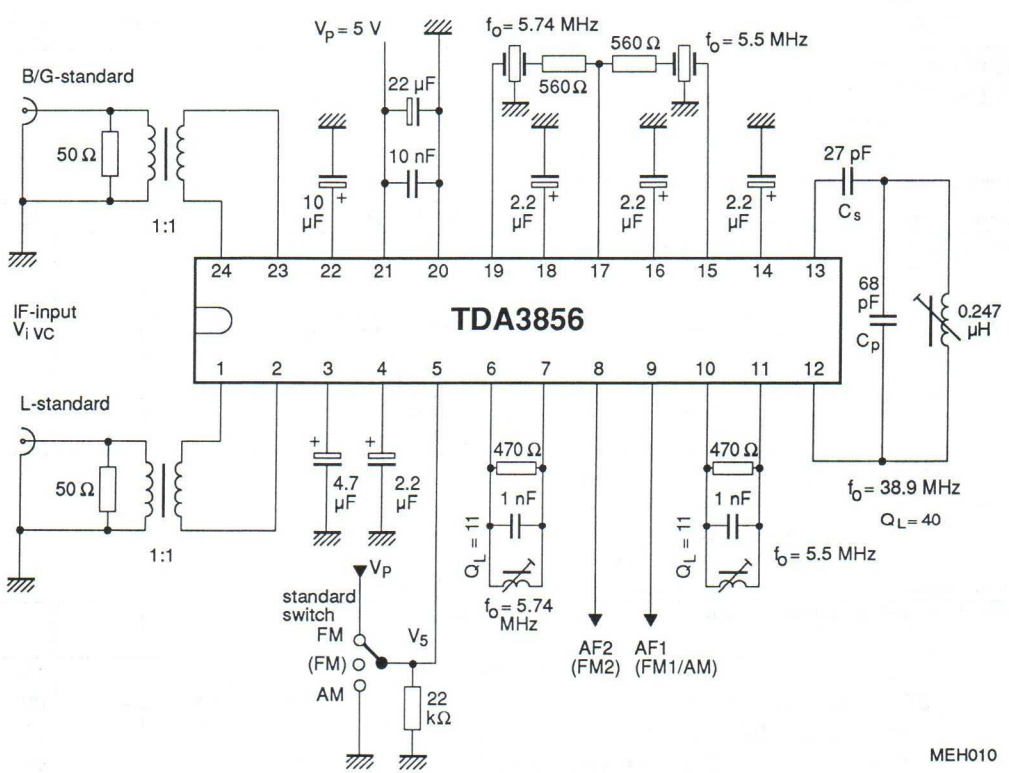


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

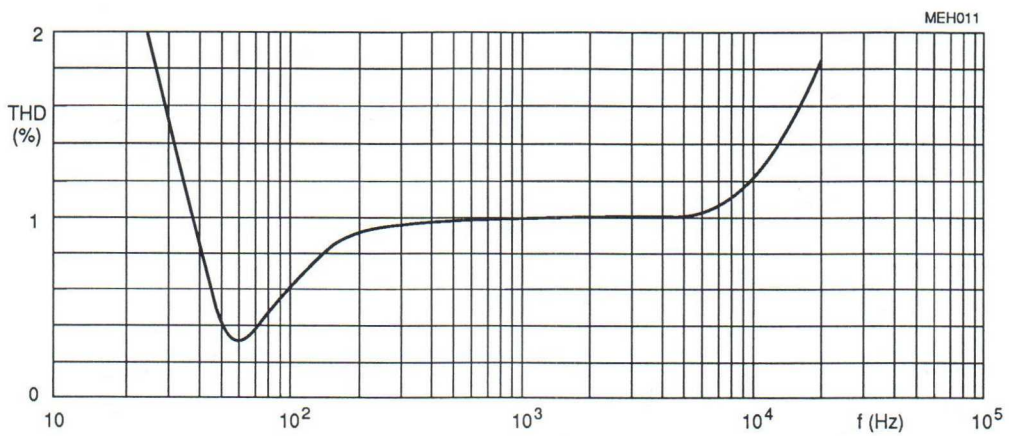
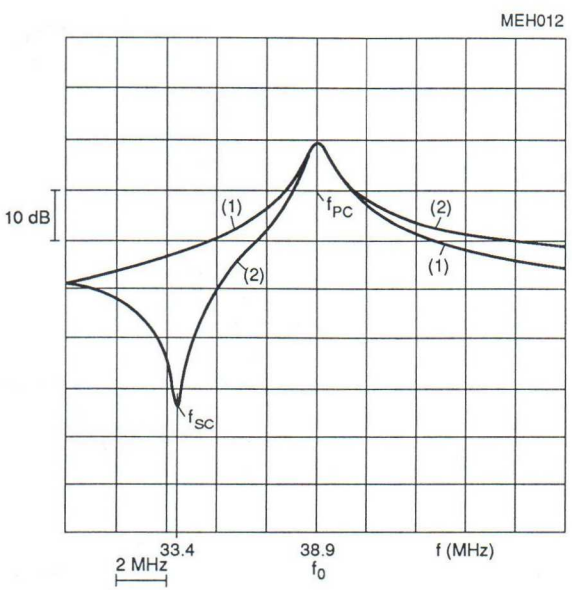


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (see Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

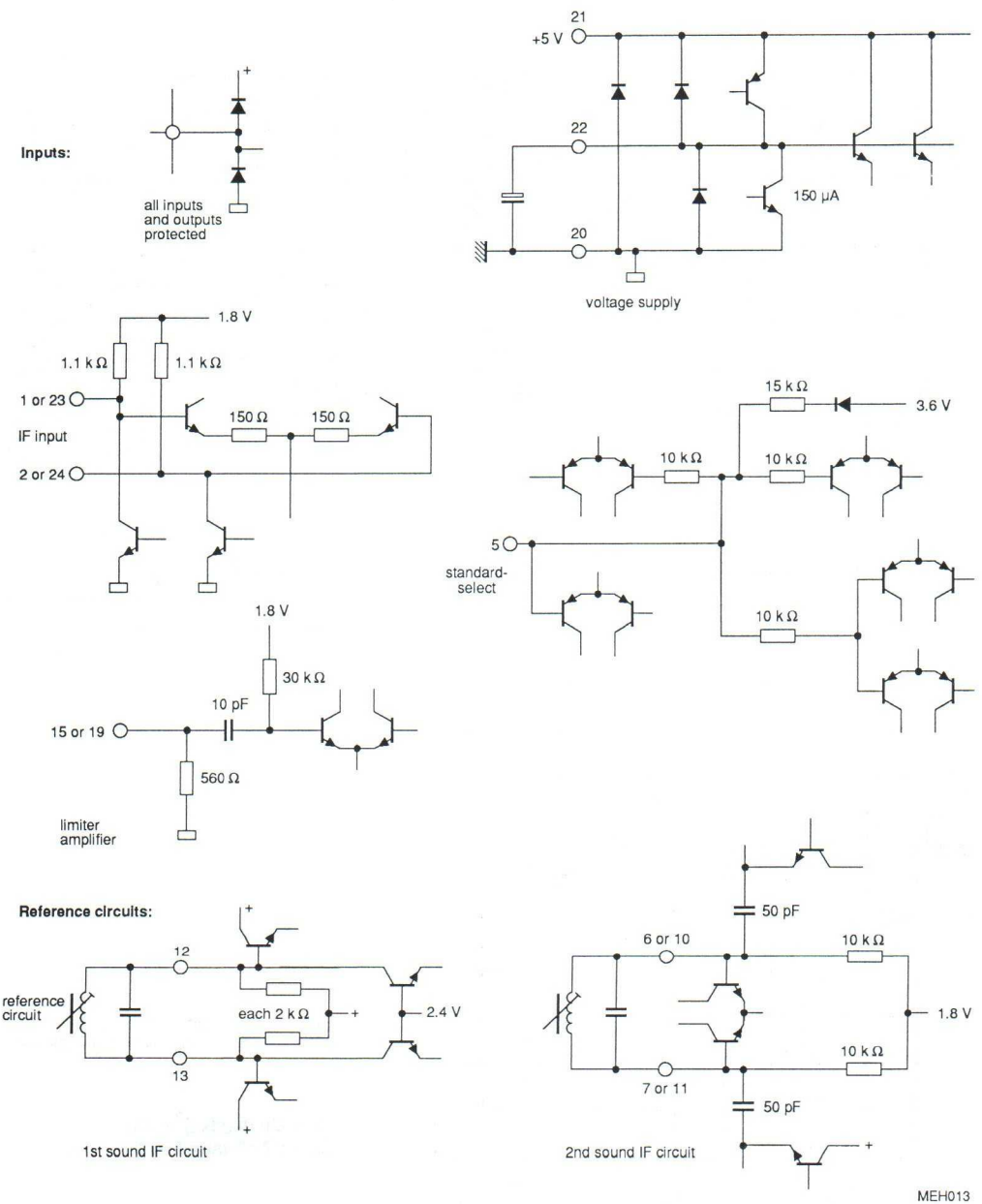


Fig.6 Internal circuits (continued in Fig.7).

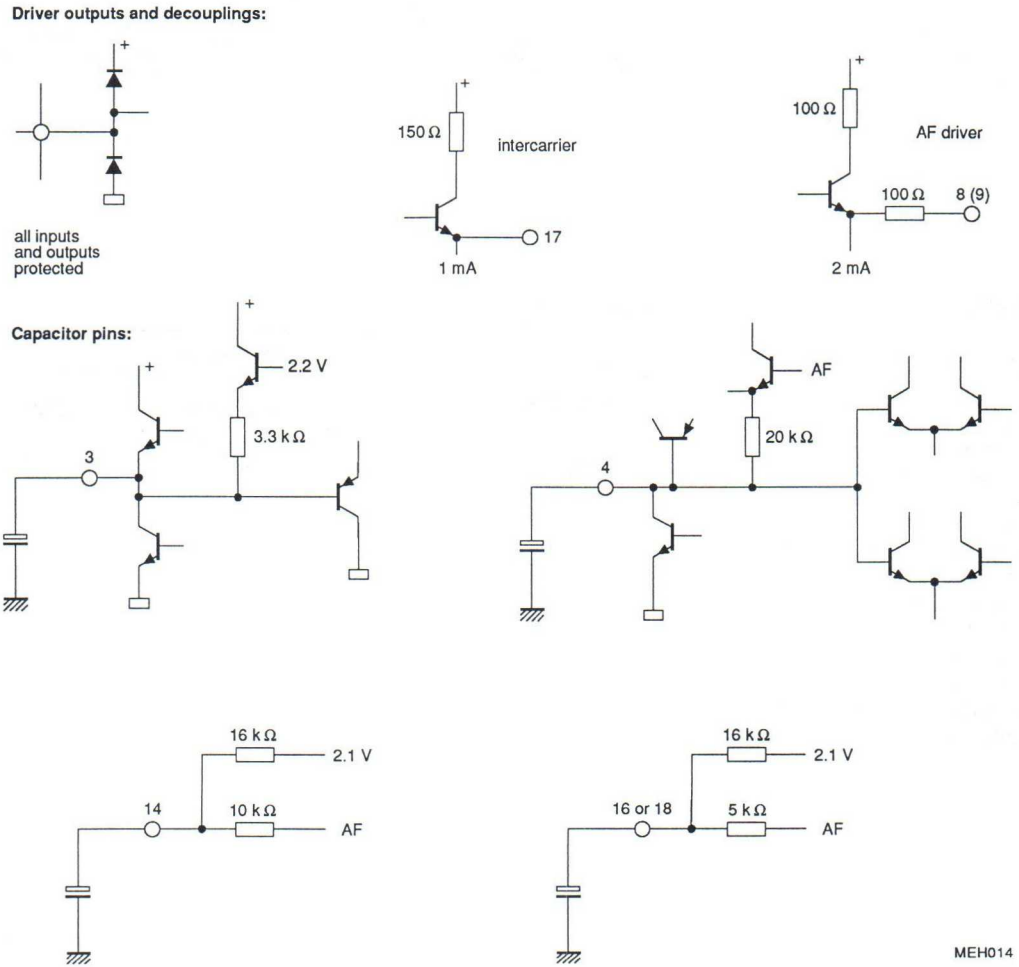


Fig.7 Internal circuits (continued from Fig.6).

Quasi-split sound processor with two FM demodulators TDA3857

FEATURES

- Quasi-split sound processor for all FM standards e. g. B/G
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (recommendable for NICAM)
- Automatic muting of the AF2 signal by the input level
- Stereo matrix correction
- Layout-compatible with TDA3856 (24 pins) and TDA3858 (32 pins).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 19)	4.5	5	8.8	V
I_P	supply current	–	60	72	mA
$V_{i\,IF}$	IF input sensitivity (–3 dB)	–	70	100	μV
$V_{o\,AF}$	audio output signal (RMS value)	–	1	–	V
THD	total harmonic distortion	–	0.5	–	%
S/N (W)	weighted signal-to-noise ratio	–	68	–	dB

GENERAL DESCRIPTION

Symmetrical IF inputs.
Gain controlled wideband IF amplifier.
AGC generation due to peak sync.
Reference amplifier for the regeneration of the vision carrier.
Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.
Intercarrier mixer for FM sound, output with low-pass filter.
Separate signal processing for 5.5 and 5.74 MHz intercarriers.
Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3857	20	DIL	plastic	SOT146

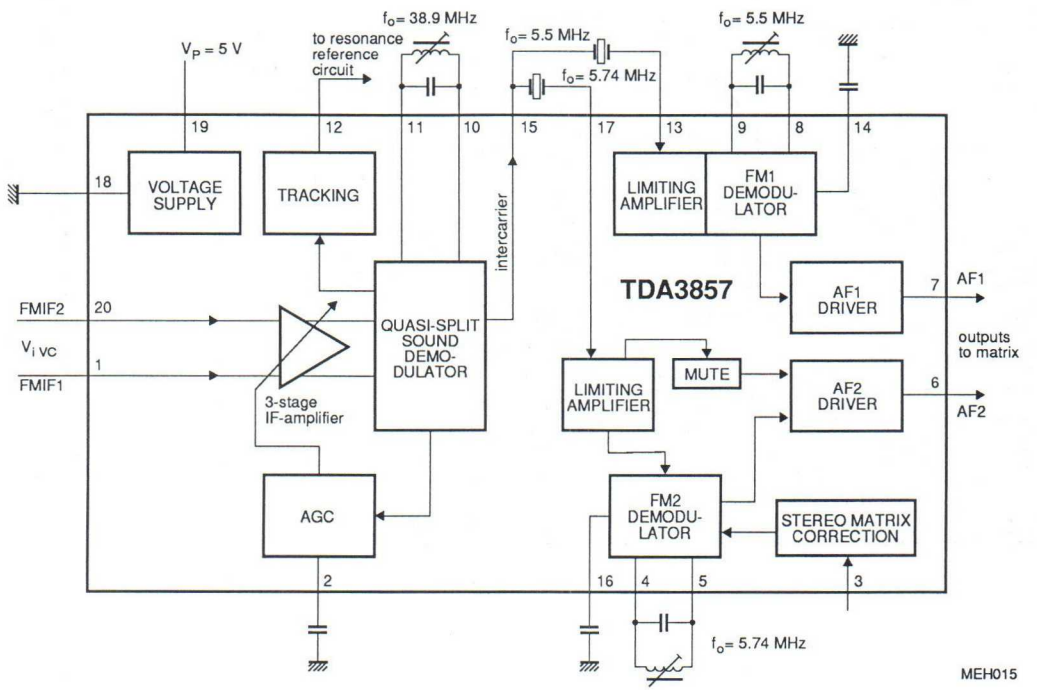


Fig.1 Block diagram (standard B/G).

PINNING

SYMBOL	PIN	DESCRIPTION
FMIF1	1	IF difference input 1 for B/G standard (38.9 MHz)
C_{AGC}	2	charge capacitor for AGC
MATR	3	input for stereo matrix correction
FM2R1	4	reference circuit for FM2 (5.74 MHz)
FM2R2	5	reference circuit for FM2 (5.74 MHz)
AF2	6	AF2 output (AF out of 5.74 MHz)
AF1	7	AF1 output (AF out of 5.5 MHz)
FM1R1	8	reference circuit for FM1 (5.5 MHz)
FM1R2	9	reference circuit for FM1 (5.5 MHz)
VC-R1	10	reference circuit for the vision carrier (38.9 MHz)
VC-R2	11	reference circuit for the vision carrier (38.9 MHz)
TRACK	12	DC output level for tracking
FM1I	13	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	14	DC decoupling capacitor for FM1 demodulator (AF1)
ICO	15	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	16	DC decoupling capacitor for FM2 demodulator (AF2)
FM2I	17	intercarrier input for FM2 (5.74 MHz)
GND	18	ground (0 V)
V_P	19	+5 to +8 V supply voltage
FMIF2	20	IF difference input 2 for B/G standard (38.9 MHz)

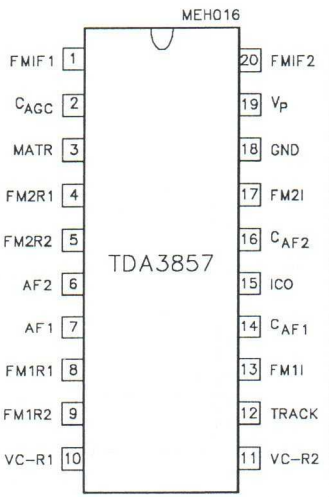


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all FM standards (e. g. B/G).

B/G standard

AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2.

Muting

With no sound carrier SC2 at pin 17, AF2 output is muted.
The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV at pin 17, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 1 and 20 generate noise at pin 17, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise at pin 17 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder, when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

Sound carrier notch filter for an improved intercarrier buzz

The series capacitor C_S in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula
$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$.
The result is an improved intercarrier buzz (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.

Intercarrier buzz fine tuning with 250 kHz square wave video modulation

The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators

For all signal-to-noise measurements the generator must meet the following specifications:
phase modulation errors < 0.5° for B/W-jumps
intercarrier signal-to-noise ratio as measured with 'TV-demodulator AMF2' (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal.
Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 19)	–	8.8	V
V_I	voltage (pins 1, 6, 7, 13, 15, 17 and 20)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling (note 1)			
	all pins except pins 1 and 20	±500	–	V
	pins 1 and 20	+400	–	V
		–500	–	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = +25 °C; measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals, modulation depth 100% (proportional to 10% residual carrier).
Vision carrier amplitude (RMS value) $V_{i\,VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 19)		4.5	5	8.8	V
I_P	supply current (pin 19)		48	60	72	mA
IF amplifier (pins 1 and 20)						
R_I	input resistance		1.8	2.2	–	kΩ
C_I	input capacitance		–	2.0	2.6	pF
V_I	DC input voltage		–	1.75	–	V
$V_{i\,IF\,(RMS)}$	maximum input signal (RMS value, pins 1-20)	V_o = +1 dB	70	100	–	mV
	input signal sensitivity (RMS value)	–3 dB intercarrier signal reduction at pin 15	–	70	100	μV
ΔG_v	IF gain control		60	63	–	dB
V_2	voltage for gain control (pin 2)		1.7	–	2.6	V
B	IF bandwidth	–3 dB	50	70	–	MHz
Resonance amplifier (pins 10-11)						
$V_{o\,(p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	–	270	–	mV
$R_{10\text{-}11}$	operating resistance		–	4	–	kΩ
L	inductance	Figs 3 and 4	–	0.247	–	μH
C	capacitance		–	68	–	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	–	40	–	
$V_{10,\,11}$	DC voltage (pins 10 and 11)		–	V_P – 1	–	V
Intercarrier mixer output (pin 15)						
$V_{o\,(RMS)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	6	8.5	–	MHz
		–3 dB	7	10	–	MHz
V_{VID}/V_{15}	residual video AM on intercarrier	note 1	–	3	10	%
$V_{VC\,(RMS)}$	residual vision carrier (RMS value)	1st/2nd harmonic (38.9/77.8 MHz)	–	0.5	1	mV
R_{15}	output resistance (emitter follower)	1 mA emitter current	–	30	–	Ω
I_o	allowable AC output current (pin 15)		–	–	±0.7	mA
I_{15}	allowable DC output current		–	–	–2	mA
V_{15}	DC voltage	LC-circuit at pin 10, 11 adjusted to minimum video content at pin 15	1.5	1.75	2.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 13 and 17)						
$V_{i\,(RMS)}$	minimum input signal (RMS value)	–3 dB AF signal	–	300	450	μV
	maximum input signal (RMS value)		200	–	–	mV
$R_{13,\,17}$	input resistance		450	560	700	Ω
$V_{13,\,17}$	DC voltage		–	0	–	V
$V_{i\,(RMS)}$	level detector threshold for no muting (RMS value, pin 17)	only 5.74 MHz channel	0.8	1.2	1.7	mV
ΔV_i	hysteresis of level detector		4	7	12	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\,IF\,(RMS)}$ = 10 mV (f_{mod} = 1 kHz, deviation Δf = ±50 kHz) at pins 13 and 17 without ceramic filters, R_S = 50 Ω. De-emphasis 50 μs. Q_L-factor = 11 for resonant circuits at pins 4-5 and 8-9 (including IC).						
$V_{IC\,(RMS)}$	intercarrier signals (RMS values, pins 4-5 and 8-9)		–	100	–	mV
V	DC voltage (pins 4, 5, 8 and 9)		–	1.8	–	V
$V_{o\,(RMS)}$	AF output signals (RMS values, pins 6 and 7)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 6 and 7)	note 2	–	–	1	dB
$R_{6,\,7}$	output resistance		75	100	130	Ω
$V_{6,\,7}$	DC voltage		1.8	2.1	2.4	V
$I_{6,\,7\,(M)}$	allowed AC current of emitter output (peak value)	note 3	–	–	±1.5	mA
$I_{6,\,7}$	maximum allowed DC output current		–	–	–2	mA
THD	total harmonic distortion		–	0.5	1.0	%
$V_{o\,(RMS)}$	AF output signal (RMS value)	THD = 1.5%	1.25	–	–	V
α_{AM}	AM suppression	1 kHz; m = 0.3	48	54	–	dB
S/N(W)	weighted signal-to-noise ratio	CCIR468-3	64	68	–	dB
B	AF bandwidth (–3 dB) lower limit upper limit		 – 100	 – –	 20 –	 Hz kHz
α_{CR}	crosstalk attenuation (pins 6-7)		60	70	–	dB
V_3	adjustment voltage for AF2	note 4 minimum output signal maximum output signal	 – –	 0 5	 – –	 V V
ΔG_{AF2min}	gain for minimum V_{out}	V_3 = 0 V	–1.5	–2.5	–	dB
ΔG_{AF2max}	gain for maximum V_{out}	V_3 = 5 V	1.0	1.5	–	dB
$V_{14,\,16}$	DC voltage (pins 14 and 16)		–	1.8	–	V
Tracking Automatic Frequency Control (AFC) of the vision carrier reference circuit						
$V_{o\,12}$	tracking output voltage (pin 12)	note 5	V_P – 3.3	–	V_P – 1	V
F_{TR}	tracking reducing factor for black picture white test picture 50% grey picture		 – – –	 9 4 6	 – – –	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S	AFC steepness (open loop) for					
	black picture		–	–8	–	mV/kHz
	white test picture		–	–3	–	mV/kHz
	50% grey picture		–	–5.5	–	mV/kHz
AF signal switches						
input signals: FM intercarrier into pin 13		see part FM demodulator				
	no signal in pin 17 (AF2)					
the output signals are related to the signals described in the demodulator part.						
V_o/V_{omute}	AF2 mute attenuation (pin 6)		70	–	–	dB
dV_6	DC jump at the AF2 output	switching to Mute	–	5	25	mV
AF performance for FM operation (standard B/G)						
input signals: B/G IF input signal (pin 1, 20)						
	unmodulated sound carriers					
	different video modulation (100%)					
the output signals are related to the signals described in the demodulator part.						
(S+N)/N(W)	weighted signal-to-noise ratio	CCIR468-3; de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	–	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.5 MHz	50	54	–	dB
	black picture	f_i = 5.742 MHz	57	61	–	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.742 MHz	48	52	–	dB
Ripple rejection of the AF outputs						
RR	ripple rejection V_{ripple} on V_P / V_{ripple} on V_{out}	$V_{R(p-p)}$ = 200 mV; f_R = 70 Hz	30	40	–	dB

Notes to the characteristics

1. Spurious intercarrier AM: m = (A – B)/A (A = signal at sync; B = signal with 100% picture modulation).
2. AF signal can be adjusted by V_3.
3. For larger current: $R_L > 2.2$ kΩ (pin 6 or 7 to GND) in order to increase the bias current of the output emitter follower.
4. If not used, pin 3 should not be connected.
5. Automatic Frequency Control (AFC) of the vision carrier reference circuit (pins 10 and 11) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.

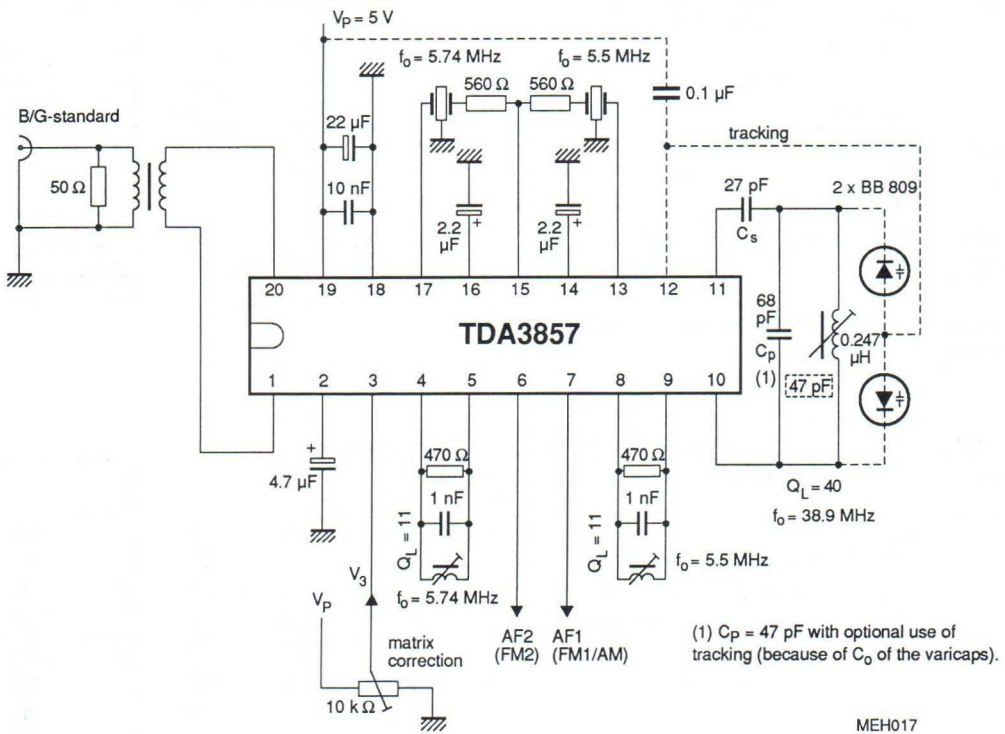
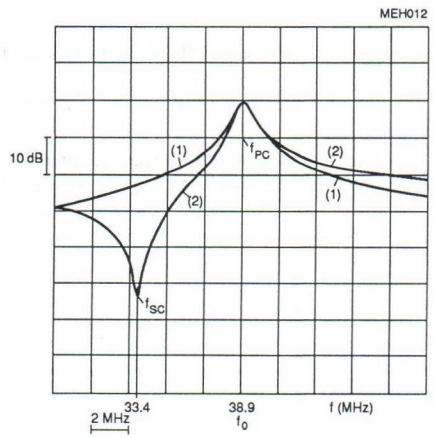


Fig.3 Test and application circuit for standard B/G (for application SAW-filters must be used).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (see Fig.3)

Fig.4 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

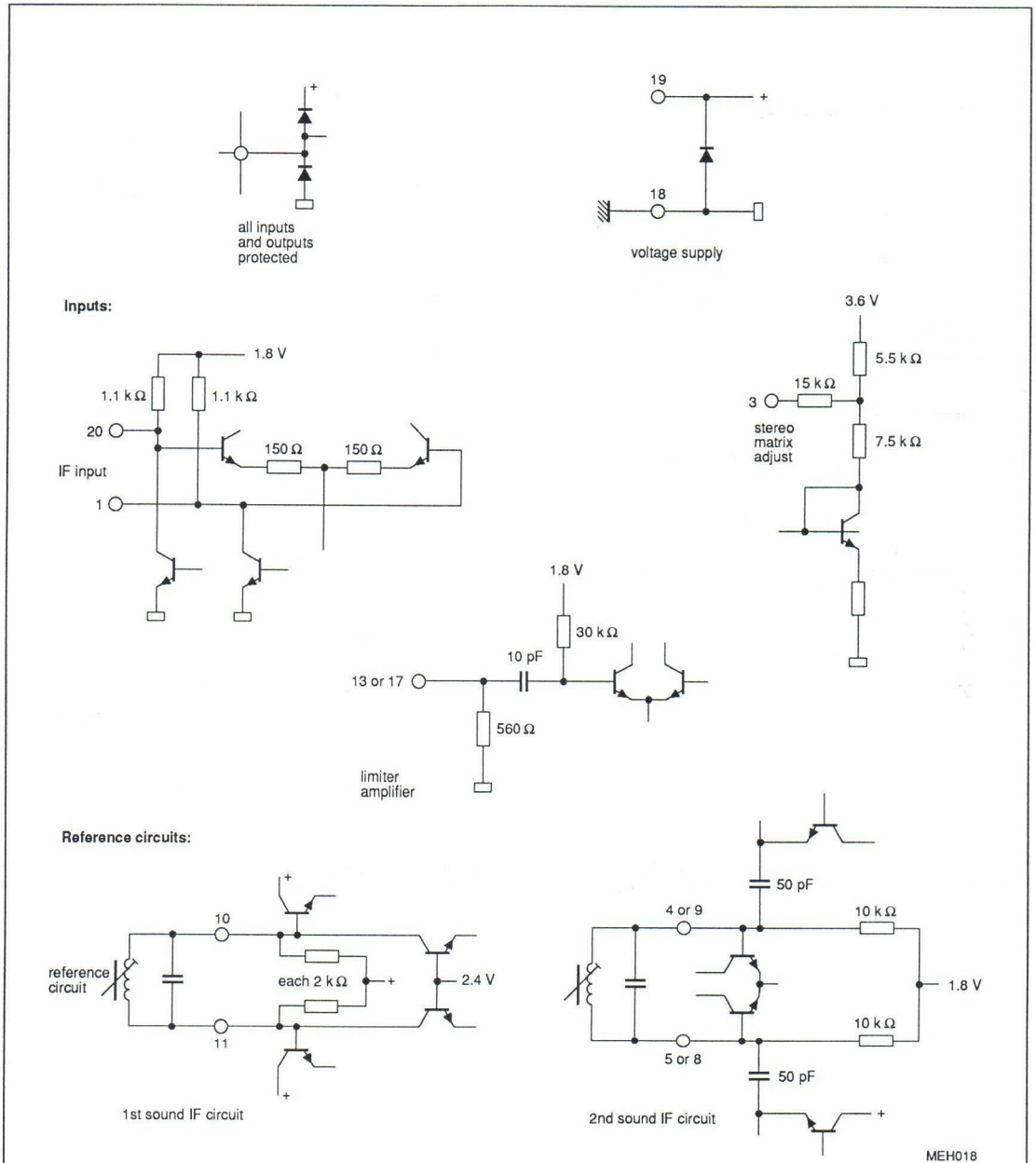


Fig.5 Internal circuits (continued in Fig.6).

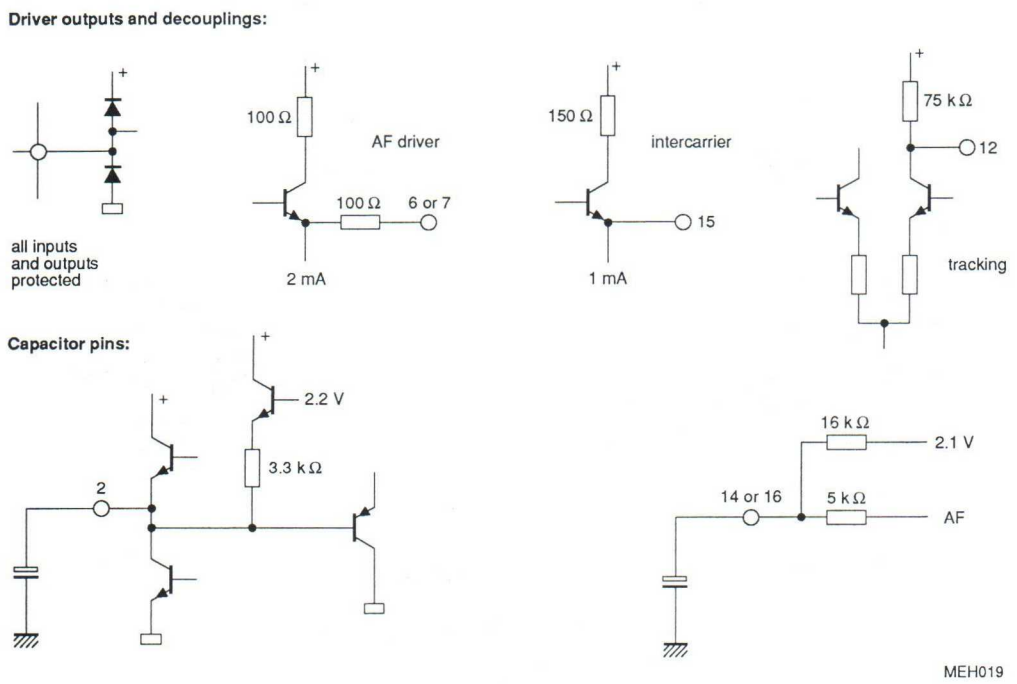


Fig.6 Internal circuits (continued from Fig.5).

Quasi-split sound processor for all standards TDA3858

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (recommendable for NICAM)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo matrix correction
- Layout-compatible with TDA3856 (24 pins) and TDA3857 (20 pins).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 27)	4.5	5	8.8	V
V_{P2}	alternative supply voltage (pin 28)	10.8	12	13.2	V
Data at V_{P1} = 5 V					
I_P	supply current (pin 27)	–	60	72	mA
$V_{i\,IF}$	IF input sensitivity (–3 dB)	–	70	100	μV
$V_{o\,(RMS)}$	audio output signal for FM (B/G)	–	1	–	V
$V_{o\,(RMS)}$	audio output signal for AM (L)	–	0.6	–	V
THD	total harmonic distortion				
	for FM	–	0.5	–	%
	for AM	–	1	–	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	–	68	–	dB
	for AM	–	56	–	dB

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.
Gain controlled wideband IF amplifier, input select switch.
AGC generation due to peak sync for FM or mean signal level for AM.
Reference amplifier for the regeneration of the vision carrier.
Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.
Intercarrier mixer for FM sound, output with low-pass filter.
Separate signal processing for 5.5 and 5.74 MHz intercarriers.
Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3858	32	shrink DIL	plastic	SOT232

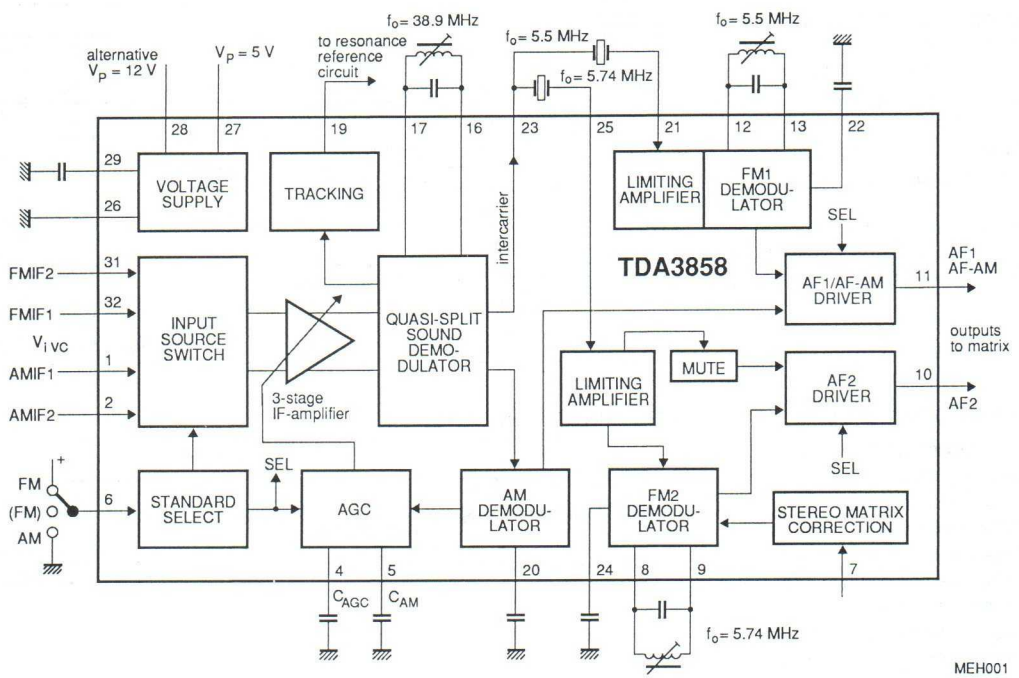


Fig.1 Block diagram (B/G and L).

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard (32.4 MHz)
n.c.	3	not connected
C_{AGC}	4	charge capacitor for AGC (FM and AM)
C_{AM}	5	charge capacitor for AM AGC
MODE	6	3-state input for standard select
MATR	7	input for stereo matrix correction
FM2R1	8	reference circuit for FM2 (5.74 MHz)
FM2R2	9	reference circuit for FM2 (5.74 MHz)
AF2	10	AF2 output (AF out of 5.74 MHz)
AF1	11	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	12	reference circuit for FM1 (5.5 MHz)
FM1R2	13	reference circuit for FM1 (5.5 MHz)
n.c.	14	not connected
n.c.	15	not connected
VC-R1	16	reference circuit for the vision carrier (38.9 MHz)
VC-R2	17	reference circuit for the vision carrier (38.9 MHz)
n.c.	18	not connected
TRACK	19	DC output level for tracking
C_{AFAM}	20	DC decoupling capacitor for AM demodulator (AF-AM)
FM1I	21	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	22	DC decoupling capacitor for FM1 demodulator (AF1)
ICO	23	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	24	DC decoupling capacitor for FM2 demodulator (AF2)
FM2I	25	intercarrier input for FM2 (5.74 MHz)
GND	26	ground (0 V)
V_{P1}	27	+5 to +8 V supply voltage (pin 28 not connected)
V_{P2}	28	+12 V supply voltage (pin 27 not connected)
C_{REF}	29	charge capacitor for reference voltage
n.c.	30	not connected
FMIF1	31	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	32	IF difference input 2 for B/G standard (38.9 MHz)

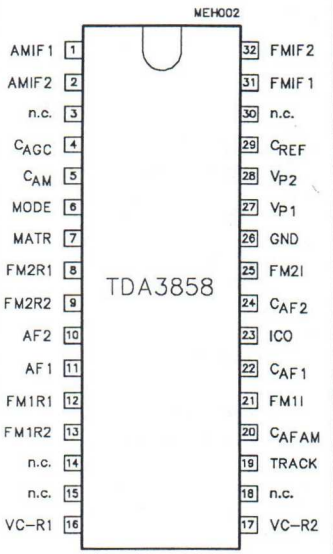


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all standards. Dependent on the voltage at pin 6 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode)

Pins 31 and 32 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2.

Muting

With no sound carrier SC2 at pin 25, AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).
The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV at pin 25, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 31 and 32 generate noise at pin 25, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise at pin 25 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder, when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode)

Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

Sound carrier notch filter for an improved intercarrier buzz

The series capacitor C_S in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula
$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$.
The result is an improved intercarrier buzz (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.

Intercarrier buzz fine tuning with 250 kHz square wave video modulation

The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators

For all signal-to-noise measurements the generator must meet the following specifications:
phase modulation errors < 0.5° for B/W-jumps
intercarrier signal-to-noise ratio as measured with 'TV-demodulator AMF2' (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal.
Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 27)	–	8.8	V
V_{P2}	supply voltage (pin 28)	–	13.2	V
V_I	voltage (pins 1, 2, 6, 10, 11, 21, 23, 25, 31 and 32)	0	V_P	V
$V_{I(12\ V)}$	voltage at 12 V supply (pin 6)	0	5.5	V
P_{tot}	total power dissipation	0	950	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling (note 1)			
	all pins except pins 1, 2, 31 and 32	±500	–	V
	pins 1, 2, 31 and 32	+400	–	V
		–500	–	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V (pin 27) and T_{amb} = +25 °C; measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals, modulation depth 100% (proportional to 10% residual carrier).
Vision carrier amplitude (RMS value) $V_{i\,VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 27)	pin 28 not connected	4.5	5	8.8	V
V_{P2}	supply voltage (pin 28)	pin 27 not connected	10.8	12	13.2	V
I_{P1}	supply current (pin 27)	V_{P1} = 5 V	48	60	72	mA
IF source control (pin 6)						
V_6	input voltage in order to obtain standards B/G (FM) with automatic muting	pin 6 connected	2.8	–	V_{P1}	V
		pin 6 open-circuit	–	2.8	–	V
	B/G (FM) without muting	pin 6 connected or alternative measure: 22 kΩ to GND	1.3	–	2.3	V
	L (AM sound)	pin 6 connected	0	–	0.8	V
I_6	input current	$V_6 = V_{P1}$	–	–	100	μA
		V_6 = 0 V	–	–	–300	μA
$V_{6\,(12\,V)}$	maximum input voltage (pin 6)	supply at pin 28	–	–	5.5	V
IF input not activated (pins 1-2 or 31-32)						
R_I	input resistance		–	–	100	Ω
V_I	DC input voltage (pins 1, 2 or 31, 32)	LOW set internally	–	–	0.1	V
$\alpha_{16\text{-}17}$	crosstalk attenuation of IF input switch	note 1	50	56	–	dB
IF amplifier (pins 1-2 or 31-32)						
R_I	input resistance		1.8	2.2	–	kΩ
C_I	input capacitance		–	2.0	2.6	pF
V_I	DC potential, voltage (pins 1, 2, 31, 32)		–	1.75	–	V
$V_{i\,IF\,(RMS)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	–	mV
	input signal sensitivity B/G standard (RMS value, pins 31-32)	–3 dB intercarrier signal reduction at pin 23	–	70	100	μV
	input signal sensitivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction at pin 11	–	70	100	μV
V_4	voltage for gain control (pin 4)		1.7	–	2.6	V
ΔG_v	IF gain control		60	63	–	dB
B	IF bandwidth	–3 dB	50	70	–	MHz
Resonance amplifier (pins 16-17)						
$V_{o\,(p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	–	270	–	mV
$R_{16\text{-}17}$	operating resistance		–	4	–	kΩ
L	inductance	Figs 3 and 5	–	0.247	–	μH
C	capacitance		–	68	–	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	–	40	–	
$V_{16,\,17}$	DC voltage (pins 16 and 17)		–	V_{P1} – 1	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 23)						
$V_{o\,(RMS)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	6	8.5	–	MHz
		–3 dB	7	10	–	MHz
V_{VID}/V_{23}	residual video AM on intercarrier	note 2	–	3	10	%
$V_{VC\,(RMS)}$	residual vision carrier (RMS value)	1st/2nd harmonic (38.9/77.8 MHz)	–	0.5	1	mV
R_{23}	output resistance (emitter follower)	1 mA emitter current	–	30	–	Ω
I_o	allowable AC output current (pin 23)		–	–	±0.7	mA
I_{23}	allowable DC output current		–	–	–2	mA
V_{23}	DC voltage	LC-circuit at pin 16, 17 adjusted to minimum video content at pin 23	1.5	1.75	2.0	V
Limiting amplifiers (pins 21 and 25)						
$V_{i\,(RMS)}$	minimum input signal (RMS value)	–3 dB AF signal	–	300	450	μV
	maximum input signal (RMS value)		200	–	–	mV
$R_{21,\,25}$	input resistance		450	560	700	Ω
$V_{21,\,25}$	DC voltage		–	0	–	V
$V_{i\,(RMS)}$	level detector threshold for no muting (RMS value, pin 25)	only 5.74 MHz channel	0.8	1.2	1.7	mV
ΔV_i	hysteresis of level detector		4	7	12	dB
Tracking Automatic Frequency Control (AFC) of the vision carrier reference circuit						
$V_{o\,19}$	tracking output voltage (pin 19)	note 3	$V_{P1} - 3.3$	–	$V_{P1} - 1$	V
F_{TR}	tracking reducing factor for					
	black picture		–	9	–	
	white test picture		–	4	–	
	50% grey picture		–	6	–	
S	AFC steepness (open loop) for					
	black picture		–	–8	–	mV/kHz
	white test picture		–	–3	–	mV/kHz
	50% grey picture		–	–5.5	–	mV/kHz
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\,IF\,(RMS)}$ = 10 mV (f_{mod} = 1 kHz, deviation Δf = ±50 kHz) at pins 21 and 25 without ceramic filters, R_S = 50 Ω. De-emphasis 50 μs and $V_6 = V_{P1}$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 8-9 and 12-13 (including IC).						
$V_{IC\,(RMS)}$	intercarrier signals (RMS values, pins 8-9 and 12-13)		–	100	–	mV
V	DC voltage (pins 8, 9, 12 and 13)		–	1.8	–	V
$V_{o\,(RMS)}$	AF output signals (RMS values, pins 10 and 11)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 10 and 11)	note 4	–	–	1	dB
$R_{10,\,11}$	output resistance		75	100	130	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{10, 11}$	DC voltage		1.8	2.1	2.4	V
$I_{10, 11 (M)}$	allowed AC current of emitter output (peak value)	note 5	–	–	±1.5	mA
$I_{10, 11}$	maximum allowed DC output current		–	–	–2	mA
THD	total harmonic distortion		–	0.5	1.0	%
$V_{o (RMS)}$	AF output signal (RMS value)	THD = 1.5%	1.25	–	–	V
α_{AM}	AM suppression	1 kHz; m = 0.3	48	54	–	dB
S/N(W)	weighted signal-to-noise ratio	CCIR468-3	64	68	–	dB
B	AF bandwidth (–3 dB) lower limit upper limit		 – 100	 – –	 20 –	 Hz kHz
α_{CR}	crosstalk attenuation (pins 10-11)		60	70	–	dB
V_7	adjustment voltage for AF2	note 6 minimum output signal maximum output signal	 – –	 0 5	 – –	 V V
ΔG_{AF2min}	gain for minimum V_{out}	V_7 = 0 V	–1.5	–2.5	–	dB
ΔG_{AF2max}	gain for maximum V_{out}	V_7 = 5 V	1.0	1.5	–	dB
$V_{22, 24}$	DC voltage (pins 22 and 24)		–	1.8	–	V
AM demodulator V_6 = 0 V (AM mode) input signal at pins 1-2: SC = 32.4 MHz; f_{mod} = 1 kHz; m = 0.8; $V_{i\,AM\,(RMS)}$ = 10 mV						
$V_{o (RMS)}$	AF output signal at pin 11 (RMS value)		530	600	675	mV
R_{11}	output resistance (pin 11)		75	100	130	Ω
$I_{o (M)}$	maximum AC output current (peak value)	note 5	–	–	±1.5	mA
I_{11}	maximum DC output current		–	–	–2	mA
V_{11}	DC voltage		1.8	2.1	2.4	V
THD	total harmonic distortion	Fig.4	–	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR468-3	50	56	–	dB
B	AF bandwidth (–3 dB) lower limit upper limit		 – 100	 – –	 20 –	 Hz kHz
V_{20}	DC voltage (pin 20)		–	2	–	V
AF signal switches input signals: AM carrier into pin 1, 2 FM intercarrier into pin 21 no signal in pin 25 (AF2) the output signals are related to the signals described in the demodulator parts.		see part AM demodulator see part FM demodulator				
V_o/V_{omute}	AF2 mute attenuation (pin 10)	B/G mode; $V_6 = V_P$	70	–	–	dB
V_{oAM}/V_{oFM}	AF1 AM signal (pin 11) attenuation of unwanted FM signal	L mode; V_6 = 0; FM: modulated; AM: unmodulated	70	–	–	dB
V_{oFM}/V_{oAM}	AF1 FM signal (pin 11) attenuation of unwanted AM signal	B/G mode; $V_6 = V_P$; FM: unmodulated; AM: modulated	70	–	–	dB
$dV_{10, 11}$	DC jump at the AF outputs	switching to FM or AM sound or Mute	–	5	25	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF performance for FM operation (standard B/G)						
input signals: B/G IF input signal (pin 31, 32) unmodulated sound carriers different video modulation (100%) the output signals are related to the signals described in the demodulator parts.						
(S+N)/N(W)	weighted signal-to-noise ratio	CCIR468-3; de-emphasis 50 μs				
	black picture	f_i = 5.5 MHz	59	63	–	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.5 MHz	50	54	–	dB
	black picture	f_i = 5.742 MHz	57	61	–	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	–	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	–	dB
	250 kHz square wave, B/W-modulated	f_i = 5.742 MHz	48	52	–	dB
Ripple rejection of the AF outputs (B/G and L standard)						
RR	ripple rejection V_{ripple} on V_P / V_{ripple} on V_{out}	$V_{R(p-p)}$ = 200 mV; f_R = 70 Hz	30	40	–	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at R_{16-17} = 470 Ω (instead of LC circuit); input signal $V_{i\,(RMS)}$ = 20 mV (pins 31-32). AGC voltage V_4 set to a value to achive $V_{o\,(RMS)}$ = 20 mV (pins 16-17). After switching (V_6 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A – B)/A (A = signal at sync; B = signal with 100% picture modulation).
3. Automatic Frequency Control (AFC) of the vision carrier reference circuit (pins 16 and 17) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.
4. AF signal can be adjusted by V_7.
5. For larger current: R_L > 2.2 kΩ (pin 10 or 11 to GND) in order to increase the bias current of the output emitter follower.
6. If not used, pin 7 should not be connected.

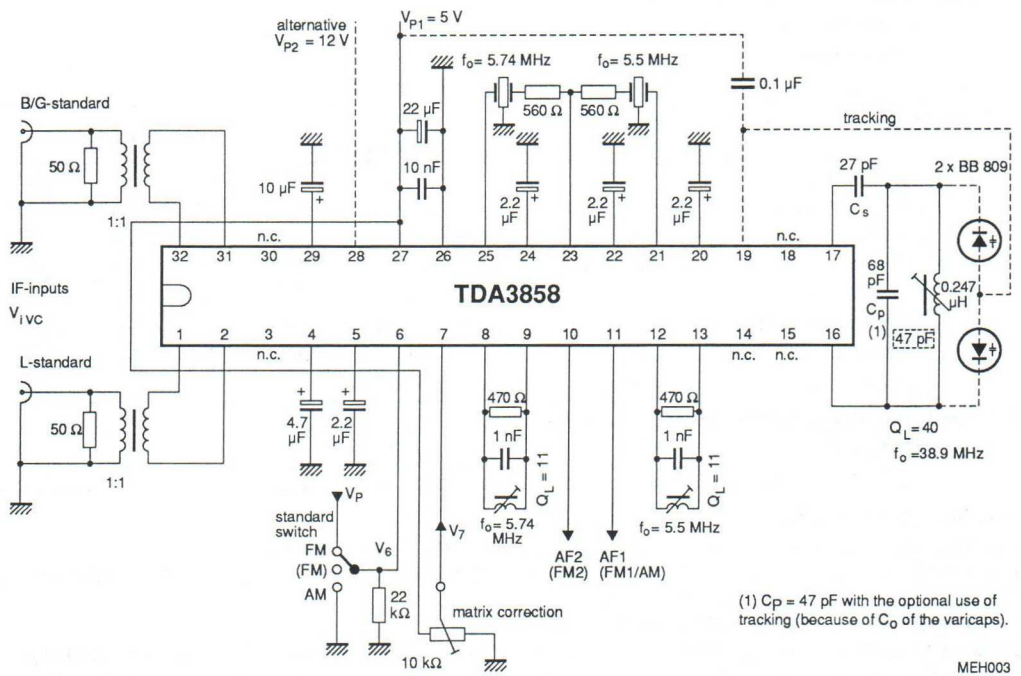


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used). For 12 V supply at pin 28, the capacitors shown at pin 27 must be connected to pin 28.

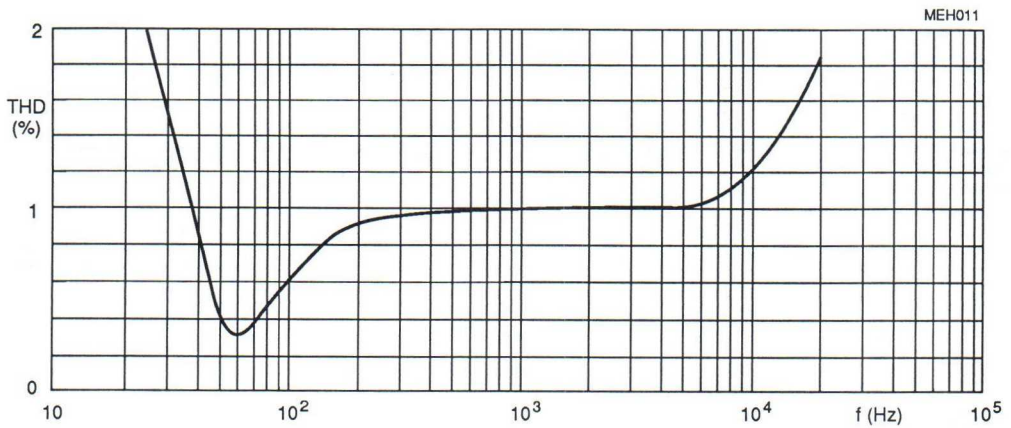
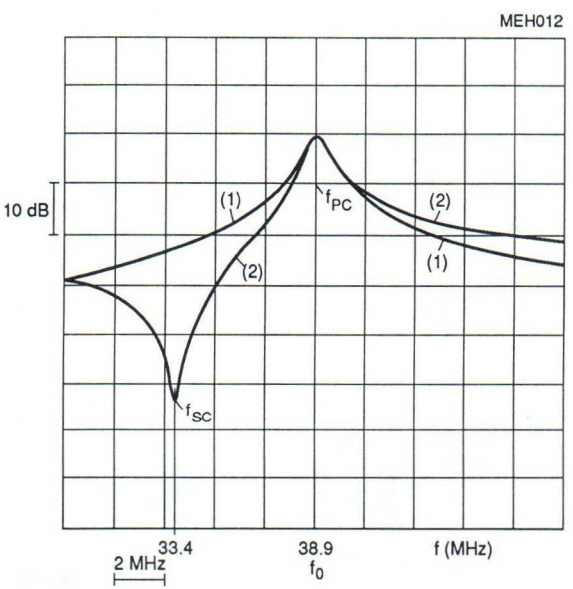


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard (V_6 = 0).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (see Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

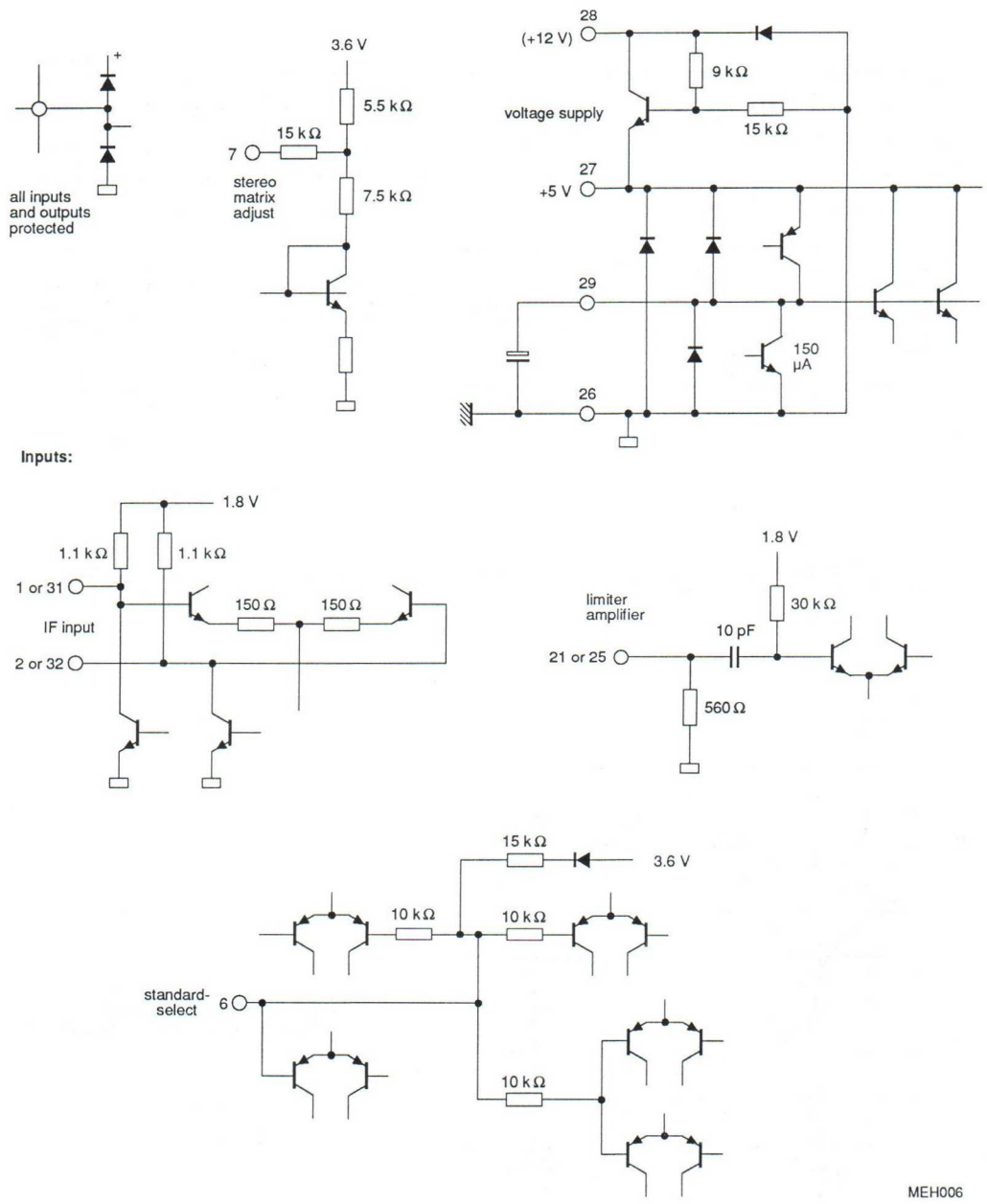


Fig.6 Internal circuits (continued in Fig.7).

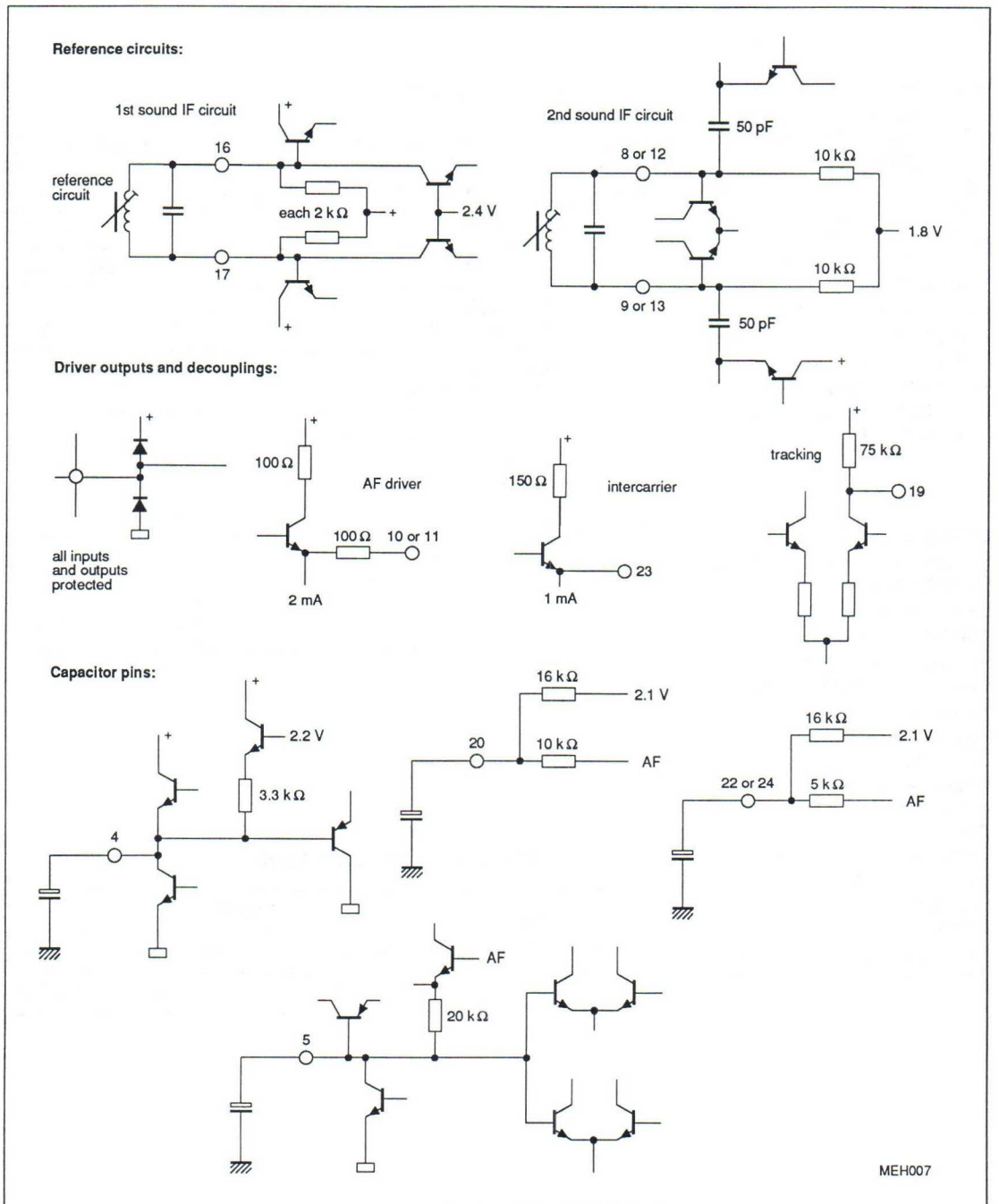


Fig.7 Internal circuits (continued from Fig.6).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3866

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- AF2 signal automatically muted (at B/G) by the input signal level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins)
- AM output level typically 500 mV at m = 0.54 (+2.5 dB in comparison to TDA 3856)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
V_o	audio output signal for FM standard B/G (RMS value)	-	1	-	V
	audio output signal for AM standard L (RMS value)	-	0.5	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3866	24	shrink DIL	plastic	SOT234

Quasi-split sound processor for all standards

TDA3866

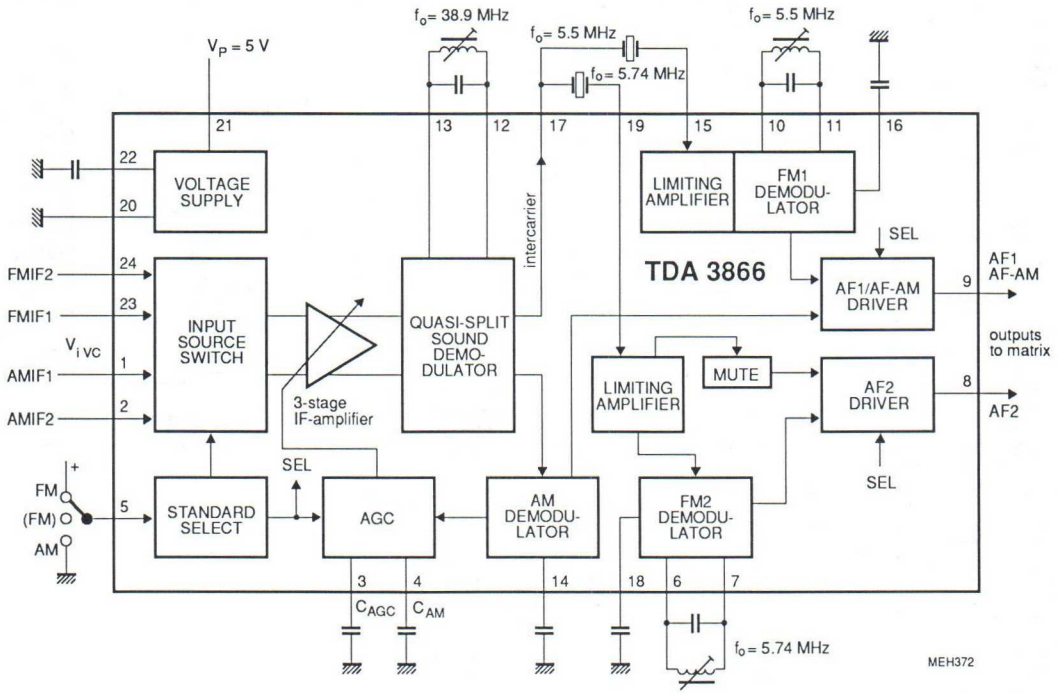


Fig.1 Block diagram (B/G and L).

Quasi-split sound processor for all standards

TDA3866

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5,74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC-decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 ... +8 V supply voltage
C_{ref}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

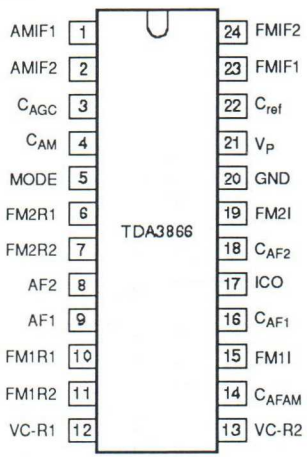


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 19 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV on pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise on pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.
The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ± 27 kHz the S/N ratio is deteriorated by 5.3 dB.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 21)	-	8.8	V
V_n	input and output voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 1, 2, 23 and 24	±500	-	V
	pins 1, 2, 23 and 24	+400	-	V
	pins 1, 2, 23 and 24	–500	-	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_P	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected	1.3	-	2.3	V
		22 kΩ to GND (alternative measure)	-	1.8	-	V
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_P$	-	-	100	μA
		V_5 = 0	-	-	–300	μA

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		-	-	100	Ω
V_{DC}	DC input voltage (pins 1, 2, 23 and 24)	internally set LOW	-	-	0.1	V
$\alpha_{1,2\text{-}23,24}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		1.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction on pin 17	-	70	100	μV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction on pin 9	-	70	100	μV
ΔG_V	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V
Resonance amplifier (pins 12-13)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{12\text{-}13}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{12,\ 13}$	DC voltage (pins 12 and 13)		-	V_P–1	-	V
Intercarrier mixer output (pin 17)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 17)		-	-	±0.7	mA
I_{17}	allowable DC output current		-	-	–2	mA
V_{17}	DC voltage		-	1.75	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 15 and 19)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{15, 19}$	input resistance		-	560	-	Ω
$V_{15, 19}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 15 and 19 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11.						
V_{IC}	intercarrier signals (RMS values, pins 6-7 and 10-11)		-	100	-	mV
V_{DC}	DC voltage (pins 6, 7, 10, and 11)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 8 and 9)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		-	-	1	dB
$R_{8, 9}$	output resistance		-	100	-	Ω
$V_{8, 9}$	DC voltage		-	2.1	-	V
$I_{8, 9}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{8, 9}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	-	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		-	1.7	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.54; $V_{i\,AM}$ = 10 mV rms				
V_o	AF output signal on pin 9 (RMS value)		400	500	600	mV
R_9	output resistance (pin 9)		-	100	-	Ω
I_o	maximum AC output current (peak value)	note 3	-	-	±1.5	mA
I_9	maximum DC output current		-	-	–2	mA
V_9	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{14}	DC voltage (pin 14)		-	2	-	V
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$) unless otherwise specified.						
Measurements on AF outputs (pins 8 and 9)						
V_o	signals attenuation of AF signal switches					
	mute: AF2 on pin 8	V_5 = 0	70	-	-	dB
	AM mode: not required signal AF1 on pin 9 (from FM)	5.5 MHz on pin 18; V_5 = 0; V_i = 10 mV	70	-	-	dB
	FM mode: not required signal AF1 on pin 9 (from AM)	signal for L standard (pins 1-2); $V_5 = V_P$	70	-	-	dB
$dV_{8,9}$	DC level deviation (pins 8 and 9)	when switching to FM or AM sound or Mute	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 9	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 8					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{12\text{-}13}$ = 470 Ω (instead of LC circuit); input signal $V_{i\ (rms)}$ = 20 mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\ (rms)}$ = 20 mV (pins 12-13). After switching (V_5 = 0 V) measure attenuation.
   IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100% picture modulation.)
3. For larger current: R_L > 2.2 kΩ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

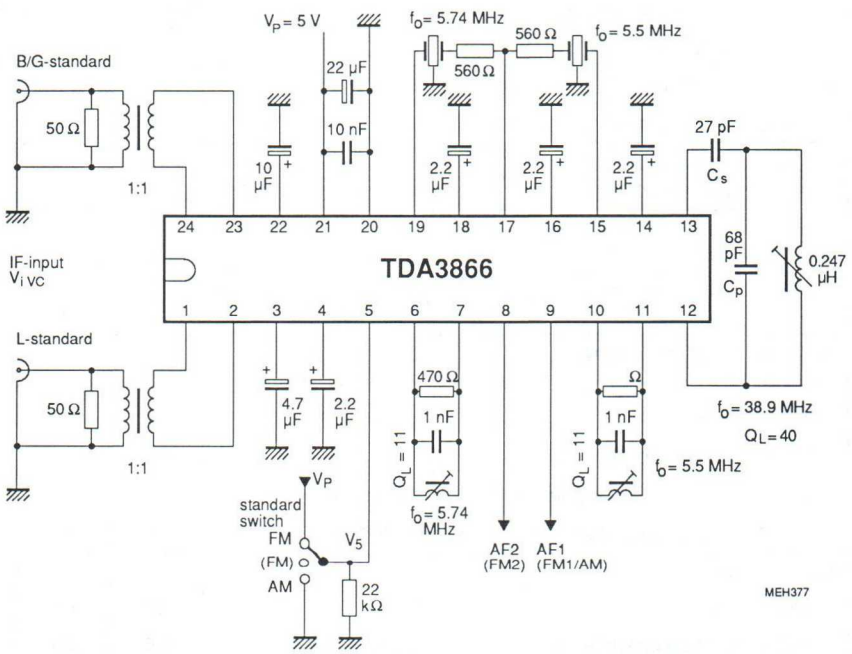


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

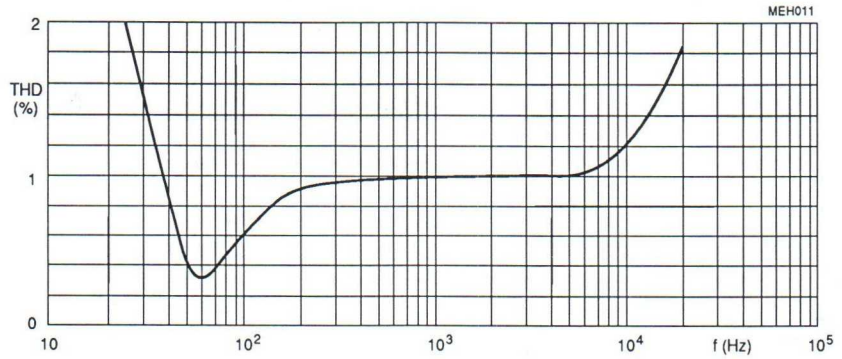
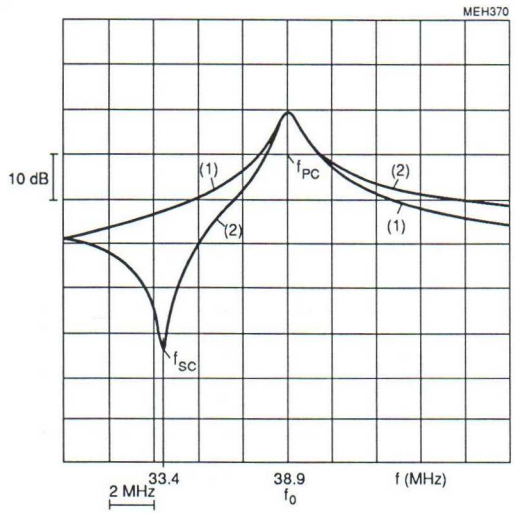


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonace circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

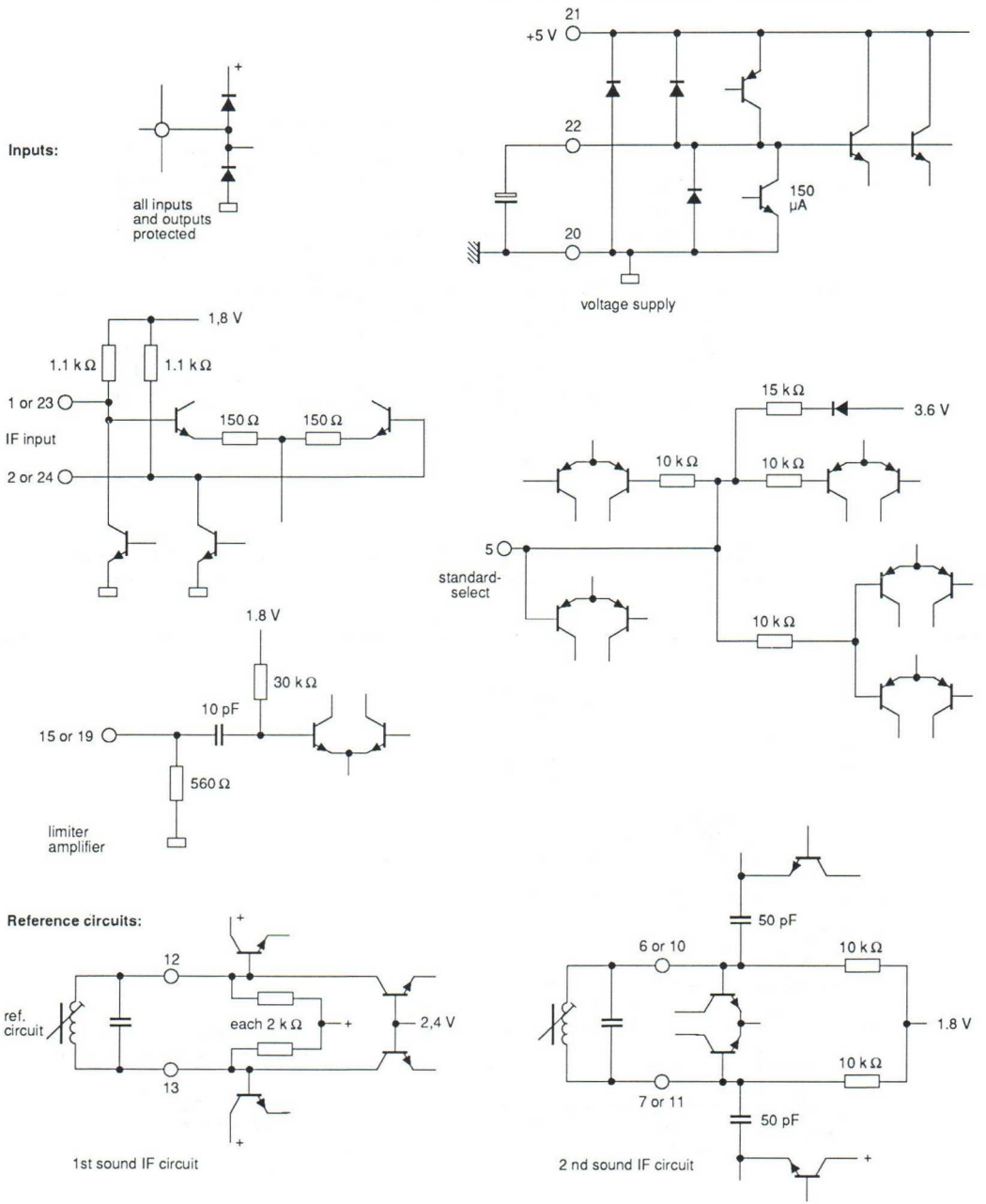


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

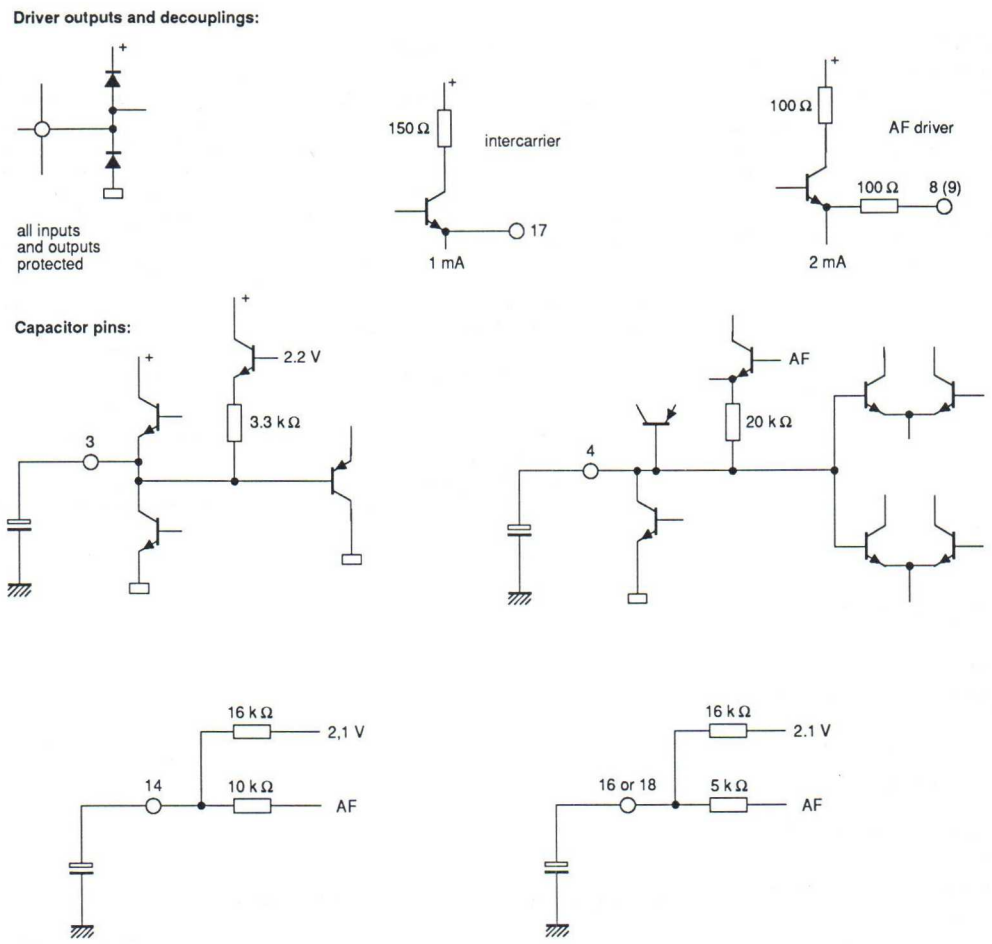


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3867T

Quasi-split sound processor with two FM demodulators

FEATURES

- Quasi-split sound processor for all FM standards e. g. B/G
- Reduction of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- AF2 signal automatically muted (at B/G) by the input signal level

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 24)	4.5	5	8.8	V
I_P	supply current (pin 24)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	µV
V_o	audio output signal (RMS value)	-	1	-	V
THD	total harmonic distortion	-	0.5	-	%
S/N (W)	weighted signal-to-noise ratio for FM	-	68	-	dB
	for FM with 6 kHz sinus vision modulation	-	56	-	dB

GENERAL DESCRIPTION

Symmetrical IF input and gain controlled wideband IF amplifier.

AGC generation due to peak sync Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3867T	28	mini-pack	plastic	SOT136A

Quasi-split sound processor with two FM demodulators

TDA3867T

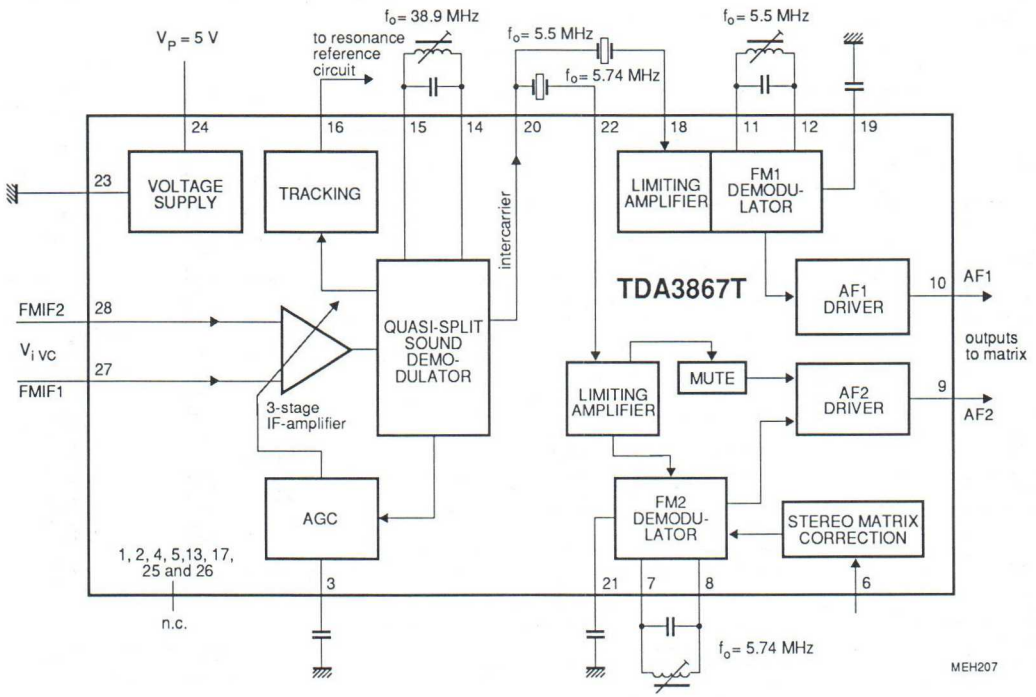


Fig.1 Block diagram.

Quasi-split sound processor with two FM demodulators

TDA3867T

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
C_{AGC}	3	charge capacitor for AGC
n.c.	4	not connected
n.c.	5	not connected
MATR	6	input for stereo matrix correction
FM2R1	7	reference circuit for FM2 (5.74 MHz)
FM2R2	8	reference circuit for FM2 (5,74 MHz)
AF2	9	AF2 output (AF out of 5.74 MHz)
AF1	10	AF1 output (AF out of 5.5 MHz)
FM1R1	11	reference circuit for FM1 (5.5 MHz)
FM1R2	12	reference circuit for FM1 (5.5 MHz)
n.c.	13	not connected
VC-R1	14	reference circuit for the vision carrier (38.9 MHz)
VC-R2	15	reference circuit for the vision carrier (38.9 MHz)
TRACK	16	DC output level for tracking
n.c.	17	not connected
FM1I	18	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	19	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	20	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	21	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	22	intercarrier input for FM2 (5.74 MHz)
GND	23	ground (0 V)
V_P	24	+5 to +8 V supply voltage
n.c.	25	not connected
n.c.	26	not connected
FMIF1	27	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	28	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

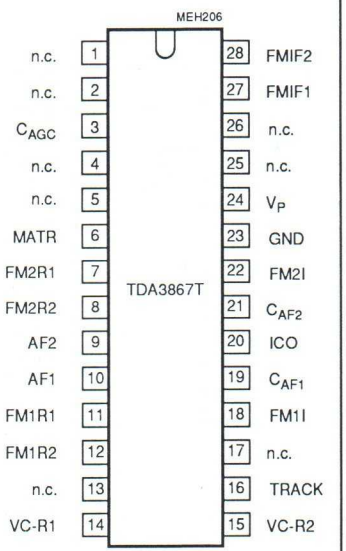


Fig.2 Pin configuration.

Quasi-split sound processor with two FM demodulators

TDA3867T

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all FM standards (e. g. B/G).
The AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 22 , AF2 output is muted. The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 22, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 27 and 28 generate noise on pin 22, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 22 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_S in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators: For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±27 kHz the S/N ratio is deteriorated by 5.3 dB.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 24)	-	8.8	V
V_n	input and output voltage (pins 9, 10, 18, 20, 22, 27 and 28)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 27 and 28	±500	-	V
	pins 27 and 28	+400 –500	- -	V V

CHARACTERISTICS

V_{P1} = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = ±50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 24)		4.5	5	8.8	V
I_P	supply current (pin 24)	V_P = 5 V	48	60	72	mA
IF amplifier (pins 27-28)						
R_I	input resistance		1.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 27 and 28)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity (RMS value)	–3 dB intercarrier signal reduction on pin 20	-	70	100	μV
ΔG_V	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resonance amplifier (pins 14-15)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
R_{14-15}	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 4	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{14, 15}$	DC voltage (pins 14 and 15)		-	V_P–1	-	V
Intercarrier mixer output (pin 20)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{20}	residual video AM on intercarrier	note 1	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{20}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 20)		-	-	±0.7	mA
I_{20}	allowable DC output current		-	-	–2	mA
V_{20}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 18 and 22)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{18, 22}$	input resistance		-	560	-	Ω
$V_{18, 22}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 22)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 16)	note 5	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) on pins 18 and 22 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis of 50 µs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 7-8 and 11-12.						
V_{IC}	intercarrier signals (RMS values, pins 7-8 and 11-12)		-	100	-	mV
V_{DC}	DC voltage (pins 7, 8,11 and 12)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 9 and 10)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 9 and 10)	pin 6 open-circuit; note 2	-	-	1	dB
$R_{9, 10}$	output resistance		-	100	-	Ω
$V_{9, 10}$	DC voltage		-	2.1	-	V
$I_{9, 10}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-10)		60	70	-	dB
V_6	adjusting voltage for AF2 signal (pin 6)	note 4	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_6	due to V_6	–1.5	-	1.0	dB
	typical gain range	due to V_6	–2.5	-	1.5	dB
$V_{19, 21}$	DC voltage (pins 19 and 21)		-	1.7	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance in B/G standard unless otherwise specified.						
Measurements on AF outputs (pins 9 and 10)						
V_o	AF signal attenuation	V_i = 400 μV;				
	mute: AF2 on pin 9	5.74 MHz on pin 22	70	-	-	dB
dV_9	DC level deviation	after mute switching	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 10	CCIR 468-3 de-emphasis 50 μs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 9					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
2. AF2 signal can be adjusted by V_6
3. For larger current: R_L > 2.2 kΩ (pin 9 or 10 to GND) in order to increase the bias current of the output emitter follower.
4. If not used, pin 6 should not be connected.
5. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 14 and 15) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.

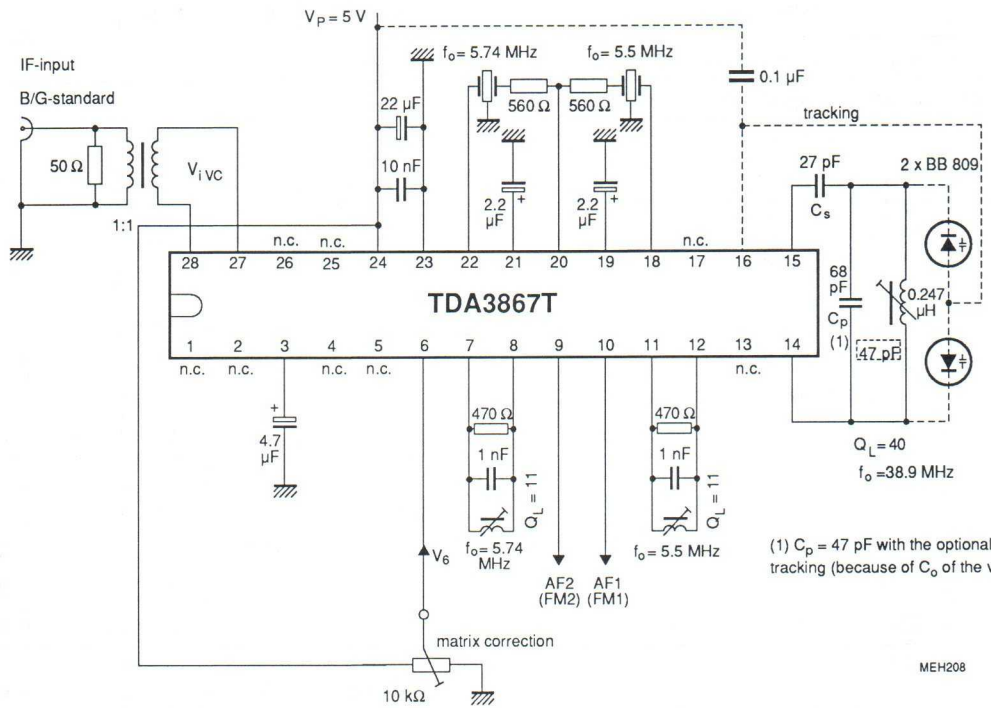
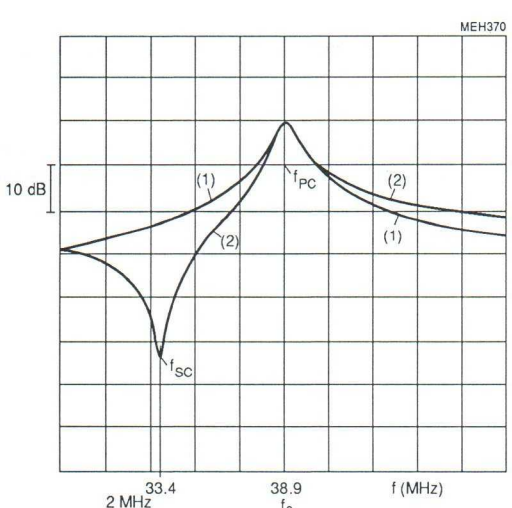


Fig.3 Test and application circuit (for application SAW-filters must be used).



(1) simple resonance circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.4 Frequency response of the 38.9 MHz reference circuit.

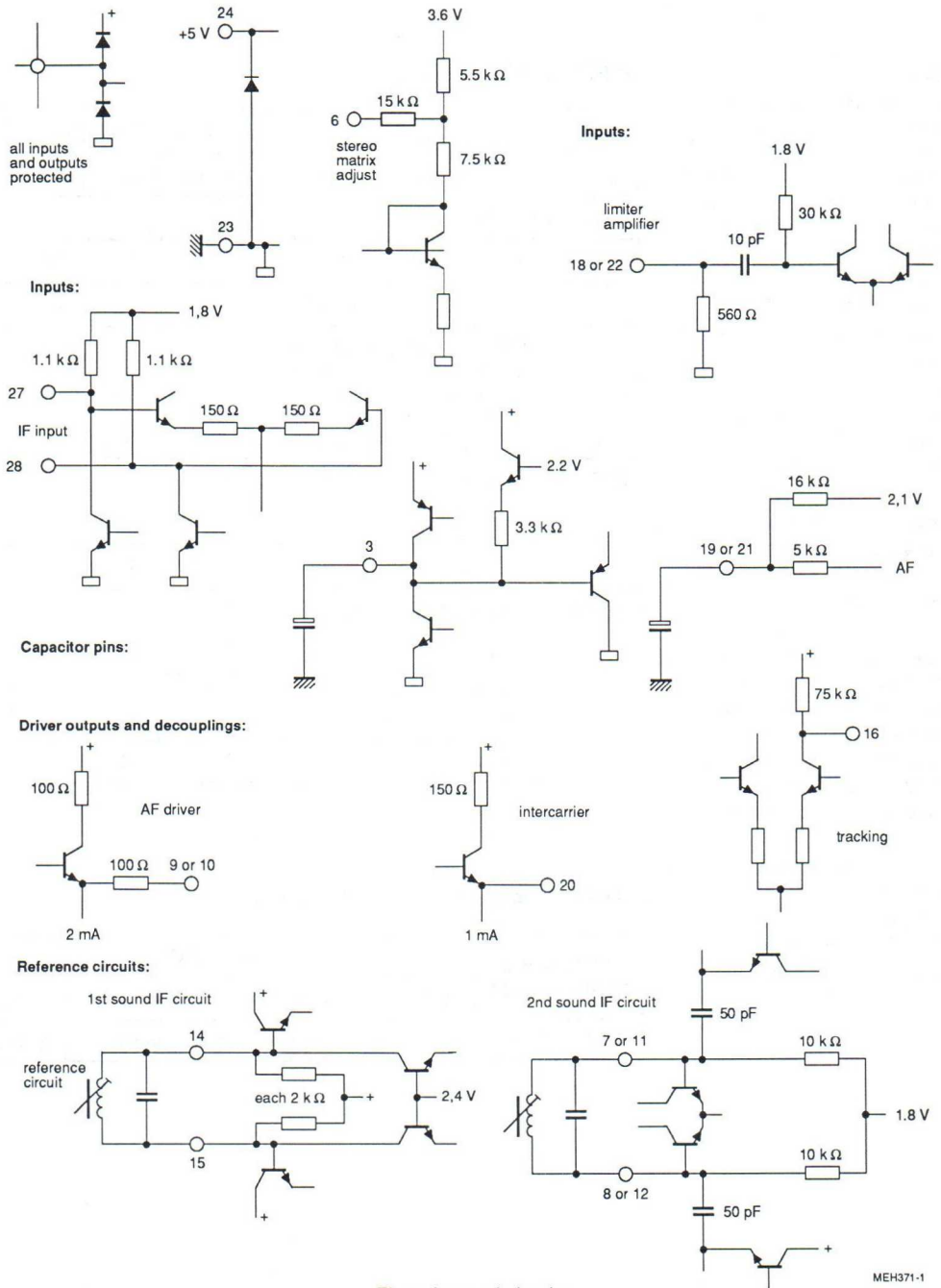


Fig.5 Internal circuits.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3868T

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Reduction of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- AF2 signal automatically muted (at B/G) by input signal level
- AM signal processing for L standard and audio switching over
- Stereo-matrix correction
- AM output level typically 500 mV at m = 0.54 (+2.5 dB in comparison to TDA3858)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM and AM sound.

Gain controlled wideband IF amplifier and input select switch.

AGC generation due to peak-sync for FM or mean signal level for AM.

Reference amplifier to regenerate the vision carrier.

Limiting amplifier optimized for AM suppression of the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 24)	4.5	5	8.8	V
Data at V_P = 5 V					
I_P	supply current (pin 24)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
V_o	audio output signal for FM standard B/G (RMS value)	-	1	-	V
	audio output signal for AM standard L (RMS value)	-	0.5	-	V
THD	total harmonic distortion for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio for FM	-	68	-	dB
	for FM with 6 kHz sinus vision modulation	-	56	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3868T	28	mini-pack	plastic	SOT136A

Quasi-split sound processor for all standards

TDA3868T

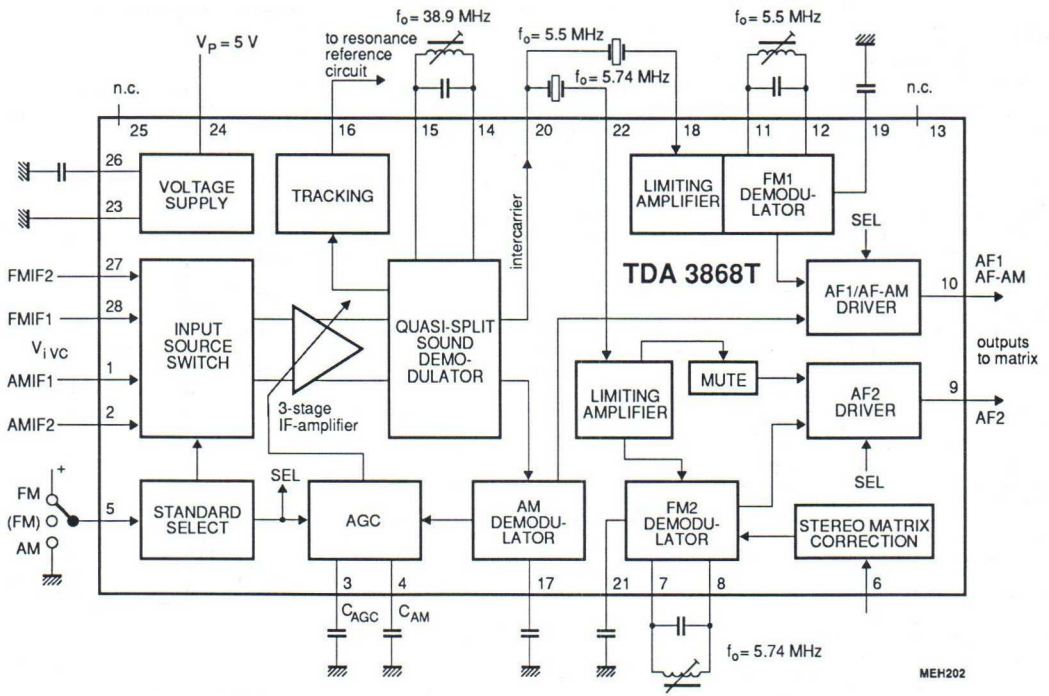


Fig.1 Block diagram (B/G and L standards).

Quasi-split sound processor for all standards

TDA3868T

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard (32.4 MHz)
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
MATR	6	input for stereo matrix correction
FM2R1	7	reference circuit for FM2 (5.74 MHz)
FM2R2	8	reference circuit for FM2 (5,74 MHz)
AF2	9	AF2 output (AF out of 5.74 MHz)
AF1	10	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	11	reference circuit for FM1 (5.5 MHz)
FM1R2	12	reference circuit for FM1 (5.5 MHz)
n.c.	13	not connected
VC-R1	14	reference circuit for the vision carrier (38.9 MHz)
VC-R2	15	reference circuit for the vision carrier (38.9 MHz)
TRACK	16	DC output level for tracking
C_{AFAM}	17	DC-decoupling capacitor for AM demodulator (AF AM)
FM1I	18	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	19	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	20	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	21	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	22	intercarrier input for FM2 (5.74 MHz)
GND	23	ground (0 V)
V_P	24	+5 to +8 V supply voltage
n.c.	25	not connected
C_{ref}	26	charge capacitor for reference voltage
FMIF1	27	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	28	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

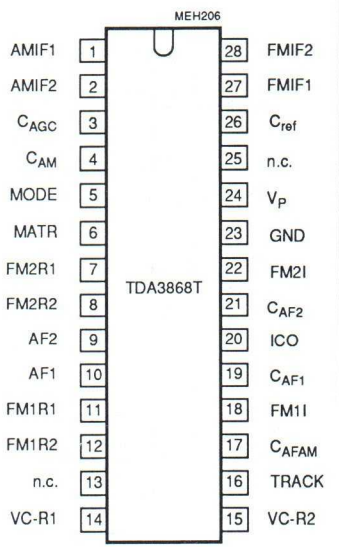


Fig.2 Pin configuration.

Quasi-split sound processor for all standards

TDA3868T

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 27 and 28 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 22 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected). The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 22, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals on pins 27 and 28 generate noise on pin 22, which is present in the intercarrier signal and passes through the 5,74 MHz filter. Noise on pin 22 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_s in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators: For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±27 kHz the S/N ratio is deteriorated by 5.3 dB.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level.The audio signal from the AM demodulator is output on AF1 with AF2 output muted.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 24)	-	8.8	V
V_I	voltage (pins 1, 2, 5, 9, 10, 18, 20, 22, 27 and 28)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 1, 2, 27 and 28	±500	-	V
	pins 1, 2, 27 and 28	+400	-	V
	pins 1, 2, 27 and 28	–500	-	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals, modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = ±50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 24)		4.5	5	8.8	V
I_P	supply current (pin 24)	V_P = 5 V	48	60	72	mA
IF input not activated (pins 1-2 or 27-28)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1-2 or 31-32)	LOW internal set	-	-	0.1	V
$\alpha_{1,2\text{-}27.28}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_{P1}	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected or alternative measure: 22 kΩ to GND	1.3	-	2.3	V
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_P$	-	-	100	µA
		$V_5 = 0$	-	-	–300	µA
IF amplifier (pins 27-28 or 1-2)						
R_I	input resistance		2.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 1, 2, 27, 28)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 27-28)	–3 dB intercarrier signal reduction on pin 20	-	70	100	µV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction on pin 10	-	70	100	µV
ΔG_V	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V
Resonance amplifier (pins 14-15)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
R_{14-15}	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{14, 15}$	DC voltage (pins 14 and 15)		-	V_P–1	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 20)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{20}	residual video AM on intercarrier	note 2	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{20}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 20)		-	-	±0.7	mA
I_{20}	allowable DC output current		-	-	–2	mA
V_{20}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 18 and 22)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{18, 22}$	input resistance		-	560	-	Ω
$V_{18, 22}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 22)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 16)	note 3	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 18 and 22 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 7-8 and 11-12.						
V_{IC}	intercarrier signals (RMS values, pins 7-8 and 11-12)		-	100	-	mV
V_{DC}	DC voltage (pins 7, 8, 11 and 12)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 9 and 10)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 9 and 10)	pin 6 open-circuit; note 4	-	-	1	dB
$R_{9,\ 10}$	output resistance		-	100	-	Ω
$V_{9,\ 10}$	DC voltage		-	2.1	-	V
$I_{9,\ 10}$	allowed AC current of emitter output (peak value)	note 5	-	-	±1.5	mA
$I_{9,\ 10}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-10)		60	70	-	dB
V_6	adjusting voltage for AF2 signal (pin 6)	note 6	0	-	5	V
ΔG_{AF2}	minimum gain range	due to V_6	–1.5	-	1.0	dB
	typical gain range	due to V_6	–2.5	-	1.5	dB
$V_{19,\ 21}$	DC voltage (pins 19 and 21)		-	1.7	-	V
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.54; $V_{i\ AM}$ = 10 mV rms				
V_o	AF output signal on pin 10 (RMS value)		400	500	600	mV
R_{10}	output resistance (pin 10)		-	100	-	Ω
I_o	maximum AC output current (peak value)	note 5	-	-	±1.5	mA
I_{10}	maximum DC output current		-	-	–2	mA
V_{10}	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{17}	DC voltage (pin 17)		-	2	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$) unless otherwise specified.						
Measurements on AF outputs (pins 9 and 10)						
V_o	signal attenuation of AF signal switches					
	mute: AF2 on pin 9	V_5 = 0	70	-	-	dB
	AM mode: not required signal AF1 on pin 10 (from FM)	5.5 MHz on pin 18; V_5 = 0; V_i = 10 mV	70	-	-	dB
	FM mode: not required signal AF1 on pin 10 (from AM)	signal for L standard (pins 1-2); $V_5 = V_P$	70	-	-	dB
$dV_{9, 10}$	DC level deviation (pins 9 and 10)	when switching to FM or AM sound or Mute	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 10	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 9					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{14\text{-}15}$ = 470 Ω (instead of LC circuit); input signal V_i = 20 mV rms (pins 27-28). AGC voltage V_3 set to a value to achive V_o = 20 mV rms (pins 14-15). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
3. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 14 and 15) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.
4. AF2 signal can be adjusted by V_6
5. For larger current: R_L > 2.2 kΩ (pin 9 or 10 to GND) in order to increase the bias current of the output emitter follower.
6. If not used, pin 6 should not be connected.

Quasi-split sound processor for all standards

TDA3868T

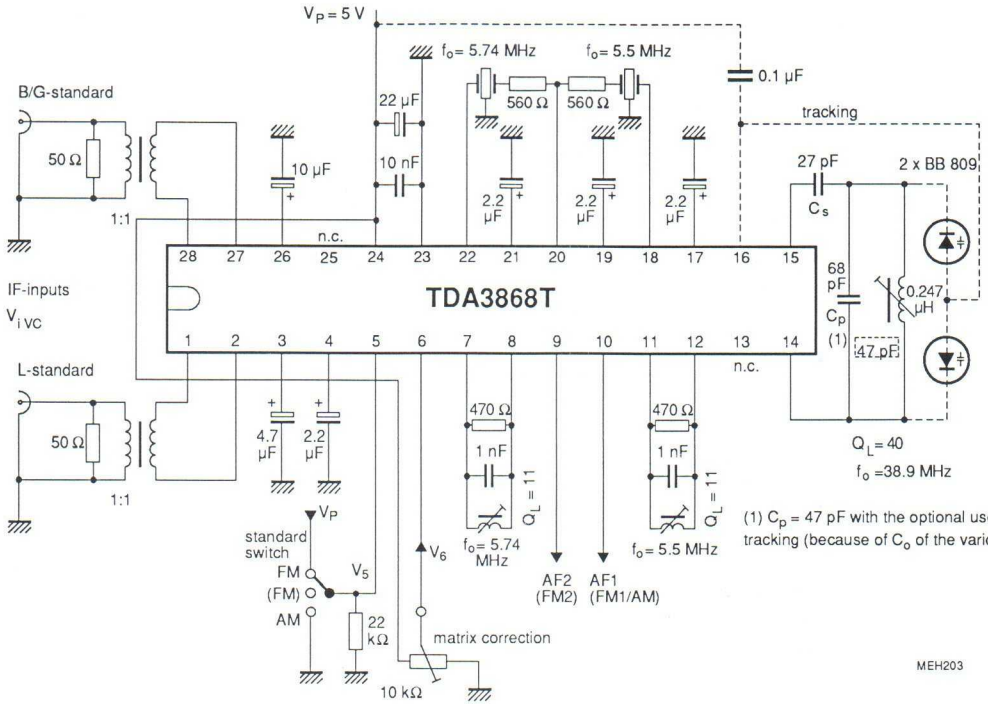


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

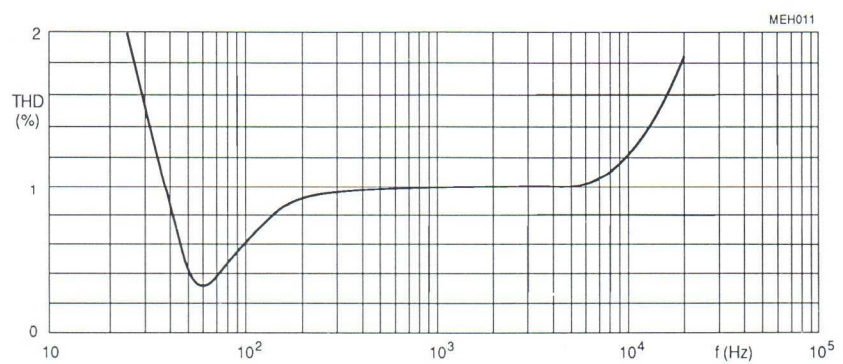
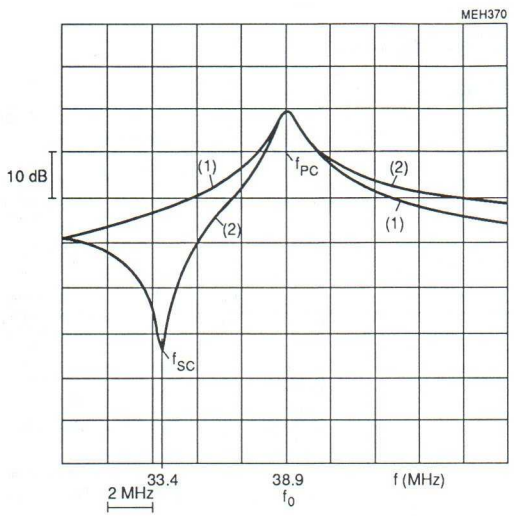


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard (V_5 = 0).

APPLICATION INFORMATION



(1) simple resonance circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

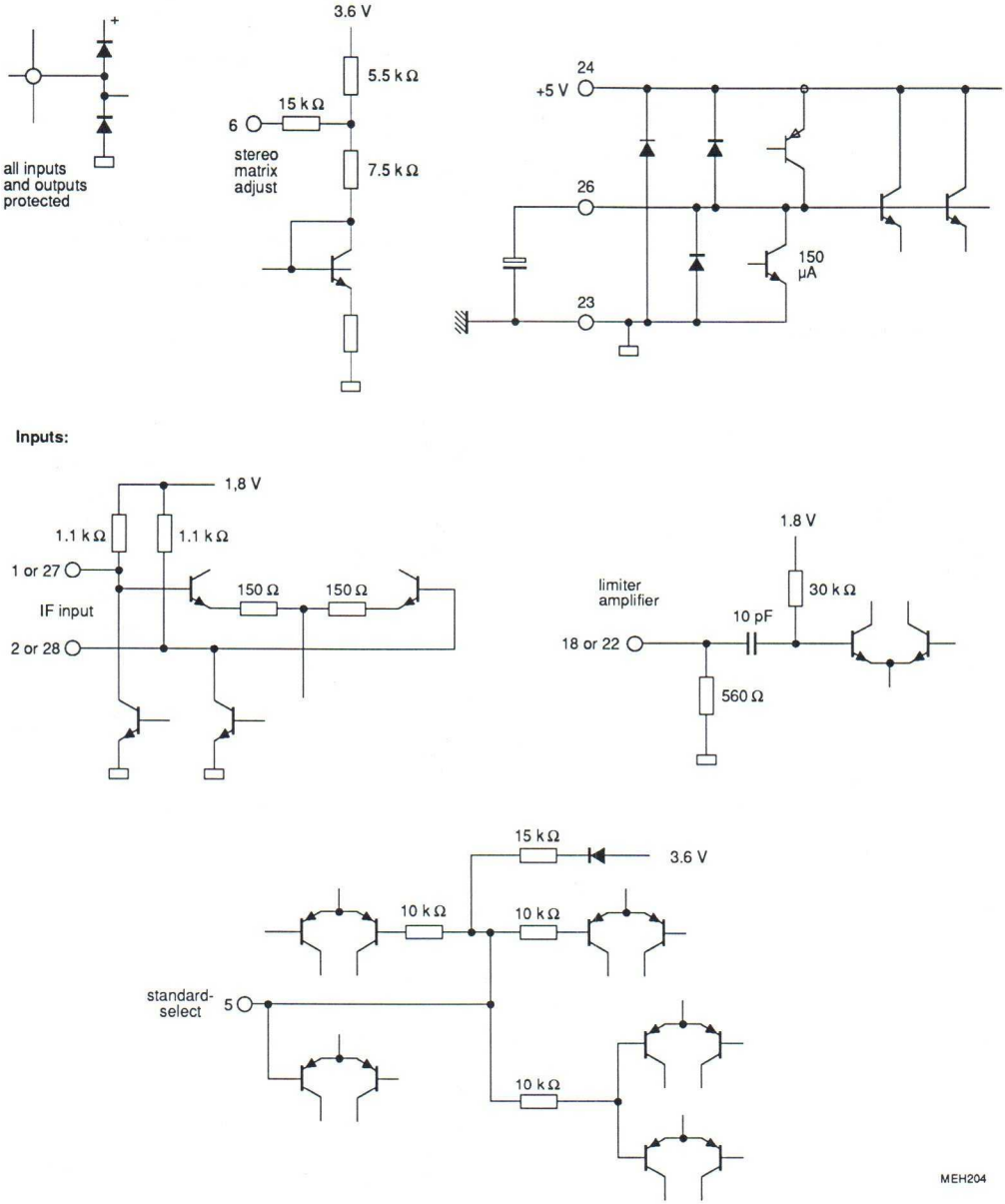


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

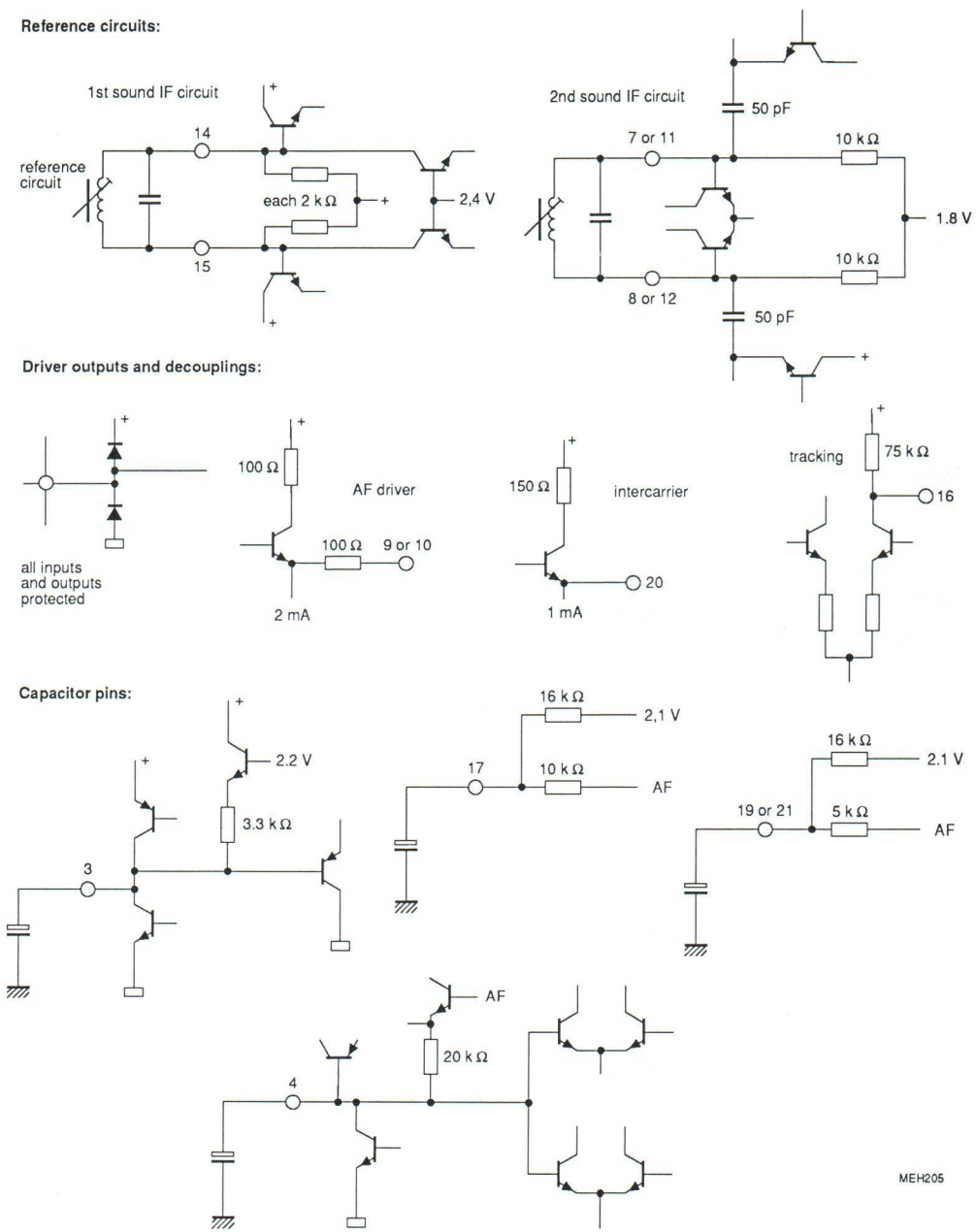


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		$V_{13\text{-}16}$	4.5	5.0	5.5	V
pin 1		$V_{1\text{-}16}$	11.0	11.25	11.5	V
Supply current	$V_{13\text{-}16} = 5$ V	I_{13}	–	14	–	mA
Operating current	$V_{1\text{-}16} = 11.25$ V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

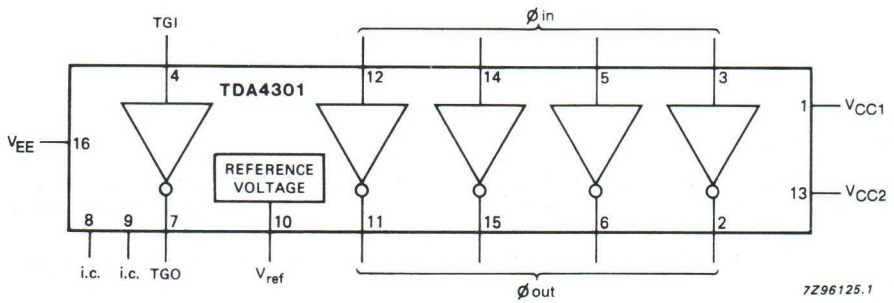


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

AC CHARACTERISTICS

$V_{CC1} = V_{1-16} = 11.25$ V; $V_{CC2} = V_{13-16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

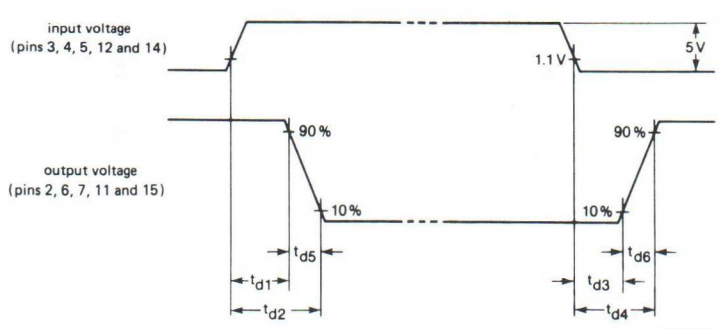


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

APPLICATION INFORMATION

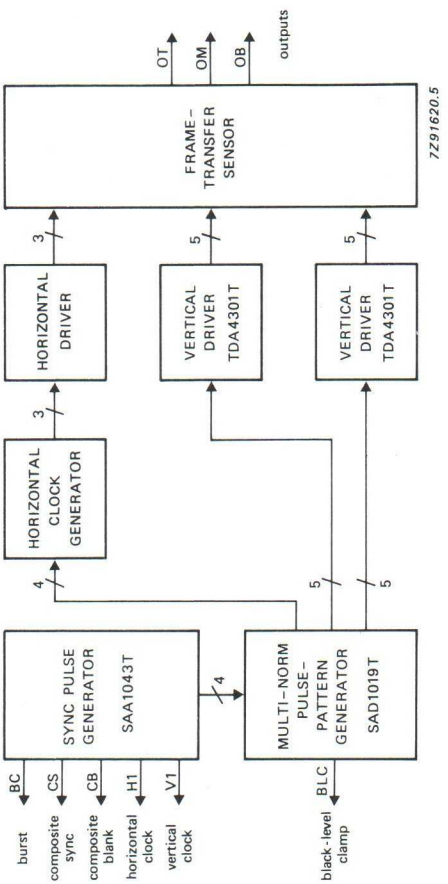


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301T is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 11		$V_{11\text{-}14}$	4.5	5.0	5.5	V
pin 1		$V_{1\text{-}14}$	11.0	11.25	11.5	V
Supply current	$V_{11\text{-}14}$ = 5 V	I_{11}	–	14	–	mA
Operating current	$V_{1\text{-}14}$ = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

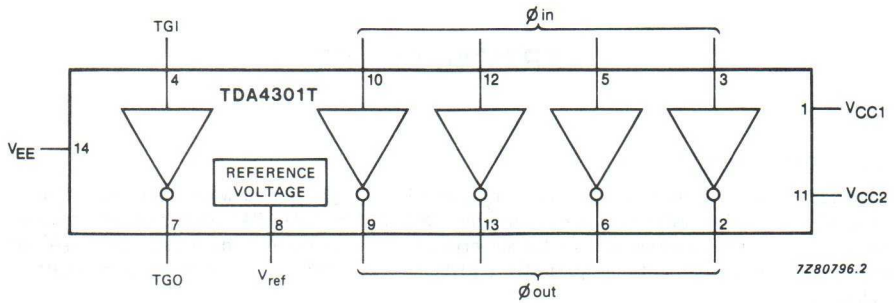


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 11		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 9 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 8)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 11)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

AC CHARACTERISTICS

$V_{CC1} = V_{1-14} = 11.25$ V; $V_{CC2} = V_{11-14} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 10 and 12)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 9 and 13)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

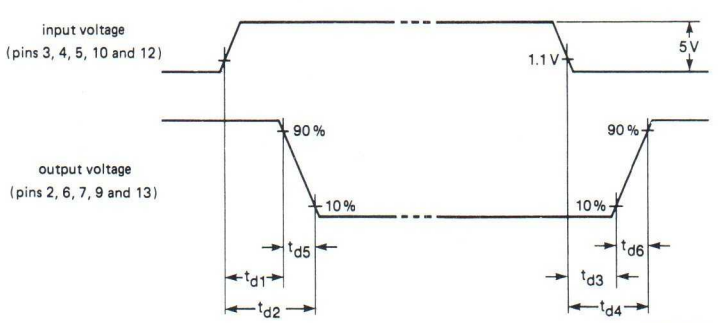


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load switching only one may be done at a time.

APPLICATION INFORMATION

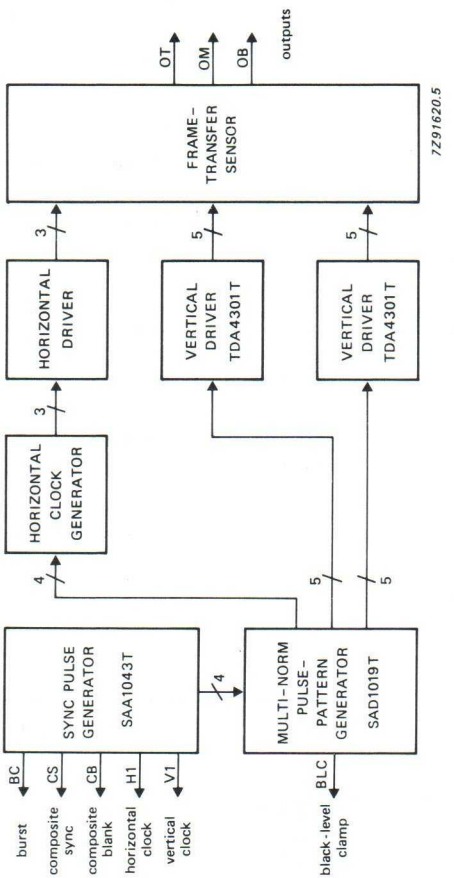


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

MASTER GAIN

GENERAL DESCRIPTION

The TDA4306 is an integrated circuit which controls the amplification of the four output signals (White, Yellow, Green and Cyan) from the frame transfer sensors (NXA1021 to NXA1041). The matching of the four channels is excellent over the whole control and temperature range. An on-chip white clipping circuit protects the white processor (TDA4303) from output signals that are too large. If white clipping occurs, a pulse is available to kill the colour information. Highlights will always be white, not coloured.

Features

- Four variable gain amplifiers
- White clipping circuit
- Blanking switch
- 2.1 V reference voltage

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 20)	$V_P = V_{20\text{-}10}$	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Total power dissipation	P_{tot}	90	140	200	mW
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4306 : 20-lead DIL; plastic (SOT146).
TDA4306T: 20-lead mini-pack; plastic (SO20; SOT163A).

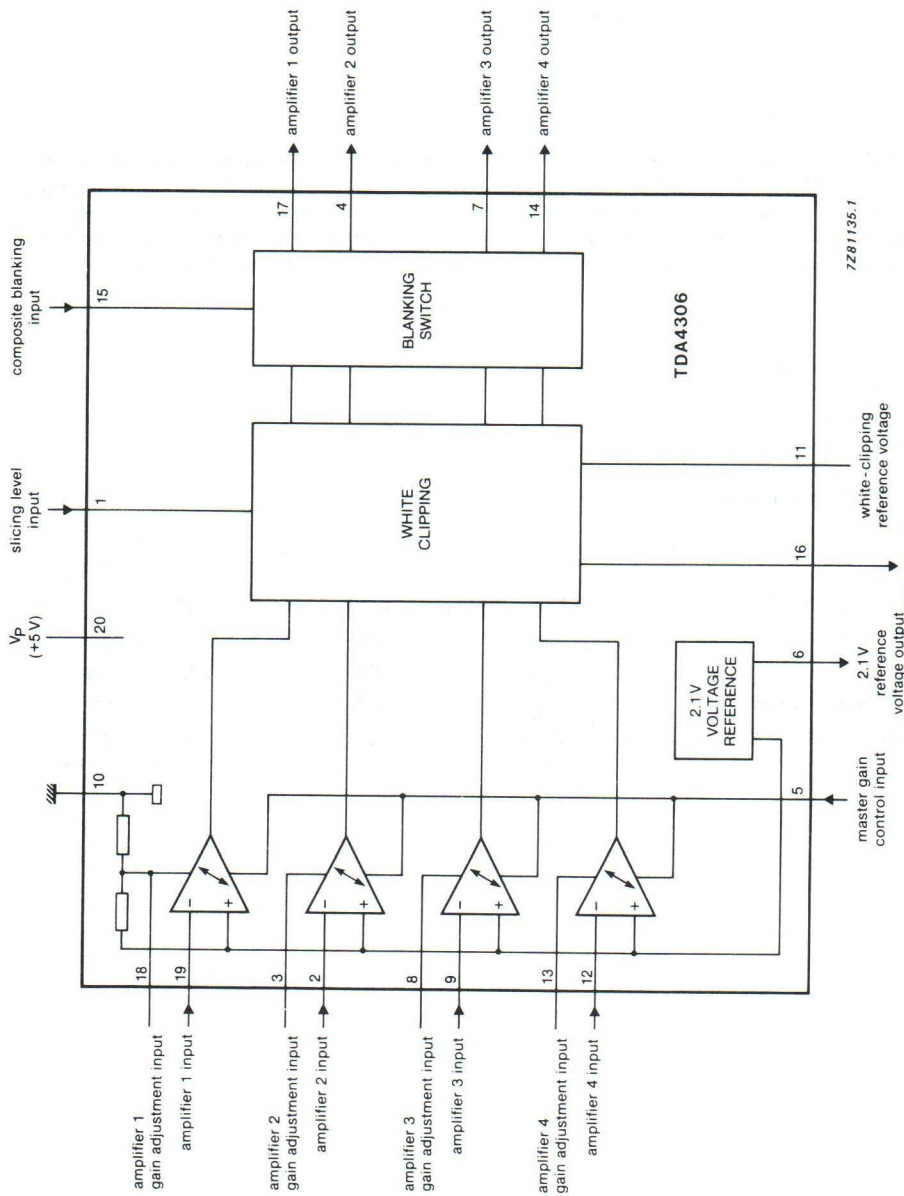


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 20)	V_P	–	12	V
Input voltage (pins 1, 2, 3, 5, 8, 9 12, 13, 15, 18 and 19)	V_I	–	5	V
Output current (pins 17, 4, 7 and 14) $t < 1$ s	I_O	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	370	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{20-10} = 5$ V; $T_{amb} = 25\,^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 20)	V_P	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Temperature drift of V_{ref}	ΔV_{ref}	–	0.18	–	mV/°C
External load current	$I_{L(ext.)}$	–	–	10	mA
Total power dissipation	P_{tot}	90	140	200	mW
Variable gain amplifiers					
Inputs (pins 2, 9, 12 and 19; note 1)					
Input voltage (peak-to-peak value)					
negative video	$V_{n-10(p-p)}$	–	–	−1100	mV
positive video (gain = 1)	$V_{n-10(p-p)}$	–	–	400	mV
Input bias current at $V_I = 2.6$ V	$I_{n(bias)}$	–	2.2	5	μA
Input resistance	$R_{2, 9, 12, 19}$	–	300	–	kΩ
Outputs (pins 17, 4, 7 and 14)					
DC offset voltage of input to output (output = V_{ref})		–	–	−220	mV
DC offset voltage of input to output (output = V_{ref})		–	–	100	mV
Offset voltage between blanked output and V_{ref}		–	–	2	mV
Drift of blanked output voltages	ΔV_O	10	–	–	μV/°C
Output sink current	I_{OS}	–	–	100	μA
Resistive load of output to ground	R_L	1.5	–	–	kΩ
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}−500 mV	–	
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}+ 1200 mV	–	
Output impedance	$\|Z_O\|$	–	100	–	Ω
Power supply rejection ratio (1 kHz)	RR	–	30	–	dB
Bandwidth	B	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Master gain control input (pin 5)					
Gain control range			see Fig. 2		
Input current at V_{5-10} = 0 V	I_5	–	–	30	μA
Matching of gain (note 2) between the 4 channels ($f_{temp.\ range}$ and as $f_{gain\ range\ 2\ to\ x\ 8}$)		–	–	1	%
Gain stability = $f_{temp.range}$ $-20 < t < 60$ °C		–	3	–	%
Differential gain	dG	–	–	1	%
Differential phase	dϕ	–	–	2	deg.
Gain adjustment inputs (pins 18, 3, 8, 13)					
Input voltage range	V_{adj}	0.9	–	1.9	V
Overall gain (MG = 2) at V_{adj} = 0.9 V	G	–	–	2.2	
at V_{adj} = 1.9 V	G	1.5	–	–	
Input current (pins 3, 8 and 13) at V_I = 1,6 V	I_I	–	–	2	μA
Input resistance (pin 18)	R_{18}	–	3.25	–	kΩ
Input voltage (pin 18; open-circuit)	V_I	–	1.2	–	V
White clipping circuit					
Slicing level (pin 1) input voltage range	V_{1-10}	0.5	–	1.8	V
input current at V_{1-10} = 1 V	I_1	–	–	2	μA
White clipping reference voltage (pin 11)	V_{11-10}	–	V_{1-10} x 2.5 V	–	V
Output pulse (pin 16) (peak-to-peak value)	$V_{16-10(p-p)}$	3.0	–	–	V
Output voltage (pin 16) LOW	V_{OL}	–	–	1	V
HIGH	V_{OH}	4	–	–	V
Output sink current (pin 16)	I_{OS}	–	–	0.1	mA
Delay of a variable gain amplifier input to white clipping output	t_d	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Blanking switch (pin 15)					
Composite blanking input voltage					
active HIGH	$V_{15\text{-}10}$	2.4	–	V_P	V
active LOW	$V_{15\text{-}10}$	–	–	1.4	V
Input current at $V_{15\text{-}10}$ = 5 V	I_{15}	–	–	2	μA
Input capacitance	C_I	–	–	5	pF
Delay between blanking input and one of the 4 amplifier outputs	t_d	–	40	100	ns

Notes to the characteristics

1. The maximum input voltage is permitted only if the input voltage minus the DC offset voltage = 2.1 V. If the input voltage minus the DC offset voltage = 1.6 V, the maximum input voltage is 1 V(p-p).
2. Over the range 2 to x 8, after that each channel is adjusted to 0. This is possible only if the blanking pulse is switched off and the DC input voltage is equal to V_{ref}.

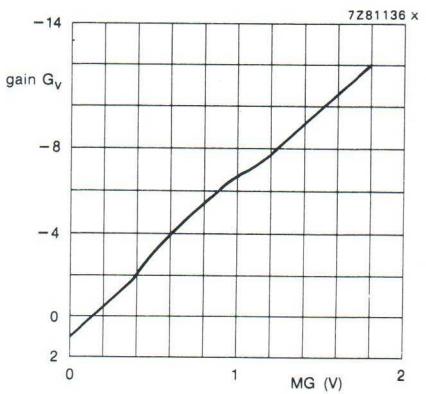


Fig.2 Gain as a function of V_{MG}.

Small signal combination for multistandard colour TV

TDA4504B

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on peak white level for positive demodulation
- Tuner AGC
- AFC circuit with two control polarities and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch
- Start-up circuit
- Vertical guard

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4504B	32	DIL	plastic	SOT201

GENERAL DESCRIPTION

Having the capability to demodulate IF signals with either positive or negative-going video information, the TDA4504B (Fig.1) is contained within a 32 pin encapsulation. It includes a three-stage vision IF amplifier, mute circuit, AFC and AGC circuitry, fully synchronised horizontal and vertical timebases with drive circuits and integral three-level sandcastle pulse generator. A functional colour tv receiver can thus be realized with the addition of a tuner, audio demodulator and amplifier, chroma decoder and respective line and field deflection circuitry.

Small signal combination for multistandard colour TV

TDA4504B

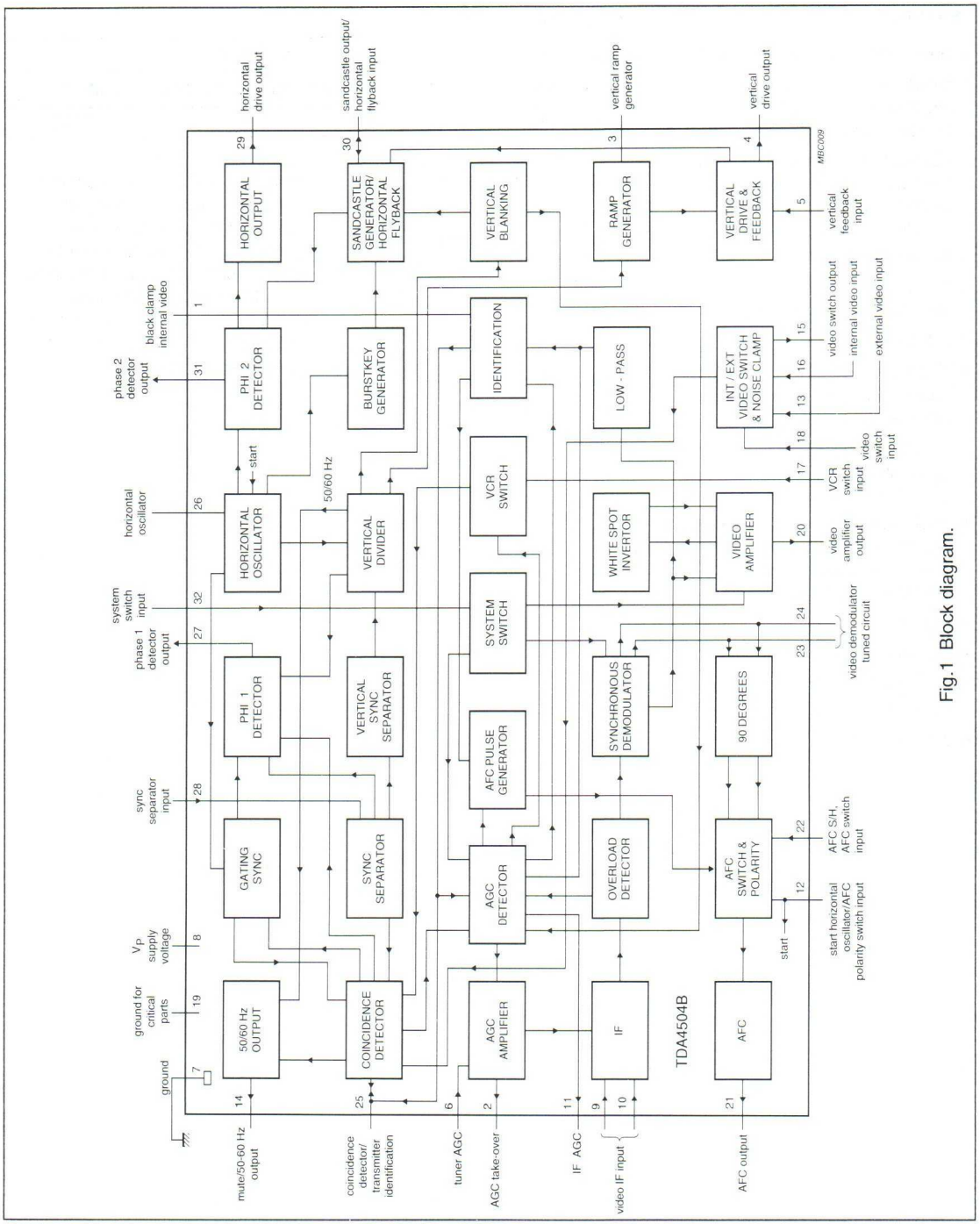


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_8	positive supply voltage pin 8		10	12	13.2	V
I_8	supply current pin 8		90	115	140	mA
I_{12}	start current pin 12		–	6.5	9	mA
Video						
$V_{9\text{-}10}$	IF sensitivity (RMS value)		25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal to noise ratio	V_i input signal = 10 mV	-	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
	video output amplitude		-	2	-	V
Video switch						
$16_{(p\text{-}p)}$	internal video input		-	2	-	V
$V_{13(p\text{-}p)}$	external video input		-	1	-	V
$V_{15(p\text{-}p)}$	video output		-	2.5	-	V
Sync						
V_{28}	sync pulse input amplitude (p-p)		200	-	-	mV
I_{30}	flyback input current		0.1	-	2	mA
V_{30}	sandcastle output during burst key		8	-	-	V
	- during hor. blanking		4	4.4	5	V
	- during vert. blanking		2.1	3.3	3.7	
V_{14}	video transmitter identification					
	- no signal condition		-	0.3	-	V
	- 50 Hz signal		-	12	-	V
	- 60 Hz signal		-	9	-	V
V_5	vert. feedback					
	- DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	- AC voltage		-	1	-	V

PINNING

PIN	DESCRIPTION
1	black level internal video
2	AGC take over (output)
3	vertical ramp generator (output)
4	vertical drive (output)
5	vertical feedback (input)
6	tuner AGC (input)
7	ground
8	supply voltage
9	vision IF (input)
10	vision IF (input)
11	IF AGC (output)
12	start horizontal oscillator (output)/AFC polarity switch (input)
13	external video (input)
14	mute/50 / 60 Hz (output)
15	video switch (output)
16	internal video (input)
17	VCR switch (input)
18	video switch (input)
19	ground for some critical parts
20	video amplifier (output)
21	AFC (output)
22	AFC S/H, AFC switch (input)
23	vision demodulator tuned circuit
24	vision demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector (output)
28	sync separator (input)
29	horizontal drive (output)
30	sandcastle output/horizontal flyback (input)
31	phase 2 detector (output)
32	AGC system switch (input)

FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permit the omission of DC feedback and possess a control range in excess of 20 dB.

The IF amplifier, which is completely symmetrical, is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator.

A noise clamp circuit is provided at the video input (pin 16) to limit interference pulses below the sync tip level and is more efficient than a noise inverter in providing improved picture stability during the presence of interference.

The video amplifier has good linearity and bandwidth figures.

AFC-circuit

Obtaining the AFC reference signal from the demodulator tuned circuit presents the advantage of utilizing a single tuned circuit and one adjustment. However, since the frequency spectrum of the signal applied to the demodulator is determind by the characteristic of the SAW filter, the resultant asymmetrical spectrum with respect to the vision carrier causes the AFC output voltage to be dependent upon the video signal. The TDA4504B thus contains a sample-and-hold circuit.

With negative-going vision signals the AFC is active only during the sync pulse period. When positive-going signals are applied to the device, however, the AFC is continuously active but filtered to ensure only a small by-pass current is present in the sample-and-hold circuit.

With weak input signals the drive signal will contain considerable noise which also possesses an asymmetrical frequency spectrum and could create an offset in the AFC output voltage. The inclusion of a notch in the demodulator tuned circuit minimises this effect.

The sample-and-hold circuit is followed by a high impedance output amplifier. Thus the AFC control gradient depends upon the load impedance.

The AFC polarity switch is combined with the start circuit (pin 12). It has a negative slope when pin 12 is open or connected to the main supply and a positive slope when pin 12 is grounded. The AFC is disabled when the sample connection (pin 22) is grounded.

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level but upon peak white content with those having positive modulation. Selection is facilitated by the system switch (pin 32):

pin 32	HIGH/open:	positive modulation
pin 32	LOW:	negative modulation

The AGC detector currents are:

	positive modulation	negative modulation
charge	1 µA	55 µA
discharge	3 mA	1.5 mA

With a 6.8 µF AGC capacitor, the video tilt will be < 10% for positively modulated signals and < 2% for negative modulation.

To obtain a rapid AGC action when executing a search tuning operation with the circuit set for peak white AGC, the charge current is held at 55 µA until the detection of a transmitted signal.

The transmitter identification

A mute signal is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. When the video switch is in the internal mode, the identification of a transmitted signal is derived from the coincidence detector.
In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync. pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

The connection of a 1 MΩ resistor between pin 25 and V_{CC} results in the mute information being overruled by the 50/60 Hz information derived from the internal vertical divider section (see 50/60 Hz truth table).

MUTE Truth Table:

Input signal Pins 9 and 10	50 Hz	60 Hz	none	50/60 Hz	50/60 Hz	50/60 Hz	none
pin 25	9.5 V	9.5 V	0.3 V	9.5	9.5	9.5	0.3
pin 28	50 Hz	60 Hz	none	50 Hz	60 Hz	none	50/60 Hz
pin 18	LOW	LOW	LOW/ HIGH	HIGH	HIGH	HIGH	HIGH
pin 14	12 V	9 V	0.3 V	12 V	9 V	12 V	0.3 V

50/60 Hz Information

In the external video mode and with a resistor of 1 MΩ from pin 25 to V_{CC} the mute is overruled by the 50/60 Hz information from the divider system.

50/60 Hz Truth Table:

Input Signal / Pin 9/10	50 Hz	60 Hz	None	Don't care	Don't care	Don't care
Pin 25	9.5	9.5	0.3	9.5	9.5	9.5
Pin 28	**50 Hz**	**60 Hz**	**None**	**50 Hz**	**60 Hz**	**None**
Pin 18	LOW	LOW	LOW	HIGH	HIGH	HIGH
Pin 14	12	9	0.3	12	9	12

VCR switch

Flywheel horizontal synchronization is desirable when receiving weak signals marred by noise but is usually unnecessary when receiving stronger off-air signals unless certain types of interference or multipath reception are apparent. Due to the inherent instability of VCR signals, however, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The connection of a switch to pin 17 provides for this to be accomplished manually and may take the form of an auxiliary switching function associated with a designated program selector button.

Video-switch

Video output from the demodulator is filtered to remove the audio carrier and DC-coupled to pin 16. If AC-coupling is employed the internal noise clamp will operate on sync. tips.

The TDA4504B provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18.

Video switch:

pin 18	LOW:	internal video
pin 18	HIGH:	external video

Gain reduction

To prevent crosstalk between the IF stages and the horizontal oscillator when the device is operated in its external video mode with no RF input, the TDA4504B incorporates an option to reduce iF gain by 20 dB. This is accomplished by connecting a 39 kΩ resistor between pin 17 and ground. Omission of this component results in the IF amplifier remaining at full gain.

In the internal video mode the resistor must be disconnected to achieve the auto-VCR mode.

The TDA4504B has a separate pin (pin 17) for the VCR switch:

pin 17	HIGH:	VCR mode	fast time constant; ungated
pin 17	n.c.:	auto VCR mode	
pin 17	LOW:	TV mode	slow time constant; gated

Horizontal synchronization

The horizontal synchronization circuit of the TDA4504B has been designed as follows:

- The retrace of the horizontal oscillator occurs during the horizontal retrace and not during the scan period. This has the advantage that no interference will be visible on the screen when receiving weak input signals. Video crosstalk will not disturb the phase of the horizontal locking.
- Reduced frequency shift of the horizontal oscillator due to noise since the horizontal phase detector reference signal is more symmetrical and independent of the supply voltage and temperature.
- The phase detector current ratio for strong and weak signals is increased to obtain a better performance during both VCR playback and weak signal reception. The switching level is also independent of temperature and supply voltage.

Vertical synchronization

Generation of the vertical sawtooth (pin 3) is accomplished by a divider that permits the production of a vertical frequency of either 50 Hz or 60 Hz with freedom from adjustment, amplitude correction and maximum interference/disturbance protection.

A discriminator window checks the vertical trigger pulse. When the trigger pulse occurs before count 576, the divider system operates in the 60 Hz mode otherwise the 50 Hz mode is selected. (2 clock pulses equal one horizontal line).

The divider section operates with different reset windows. These windows are activated via an up/down counter. This increases its count by 1 for each occasion the separated vertical sync pulse is within the selected window. On each occasion the vertical sync. pulse is not within the selected window, the count is reduced by 1.

LARGE (SEARCH) WINDOW; DIVIDER RATIO BETWEEN 488 - 722

This mode is valid for the following conditions:

1 divider locking to another transmitter
2 divider ratio found, not within the narrow window limits
3 up/down counter value of the divider system operating in narrow window mode, count falls below 10.

NARROW WINDOW; DIVIDER RATIO BETWEEN 522 - 528 (60 Hz) OR 622 - 628 (50 Hz)

The divider switches to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the count lowered by 1. At a counter value below 10, the divider switches to the large window mode.

An anti-top flutter pulse is also generated by the divider system. This inhibits the horizontal phase-1 detector during the vertical sync pulse. The width of this pulse depends upon the divider mode. For the large window mode the start is generated at the divider reset. In the narrow window mode the anti-top flutter pulse starts at the beginning of the first equalizing pulse. The anti-top flutter pulse ends at count 10 for 50 Hz and count 12 for 60 Hz.

When out-of-sync is detected by the coincidence detector, the divider is switched to count 625. This results in a stable vertical amplitude when no input signal is available.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{stg}	storage temperature range	– 55	+ 150	°C
T_{amb}	operating ambient temperature range	– 25	+ 65	°C
V_P	positive supply voltage (pin 8)	–	13.2	V
P_{tot}	total power dissipation	–	2.3	W

ESD

All pins meet:

2000 V, 100 pF, 1500 Ω

200 V, 200 pF, 0 Ω

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30 K/W

CHARACTERISTICS

T_{amb} = 25 °C; supply 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	–	6.5	9	mA
V_{12}	start protection level (pin 12)	I_{12} = 12 mA	–	–	16.5	V
IF Amplifier						
$V_{9\text{-}10(RMS)}$	input sensitivity (RMS–value)	note 2	25	40	65	μV
$R_{9\text{-}10}$	differential input resistance	note 3	–	1300	–	Ω
$C_{9\text{-}10}$	differential input capacitance	note 3	–	5	–	pF
$G_{9\text{-}10}$	gain control range		–	74	–	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	–	1	–	dB
$V_{9\text{-}10}$	maximum input signal		100	170	–	mV
$V_{9\text{-}10}$	input sensitivity at gain reduction	note 2	250	400	650	μV_{RMS}
Video Amplifier (note 5)						
	Zero signal output level	note 6				
V_{20}	negative modulation		4.7	4.9	5.1	V
V_{20}	positive modulation		2.5	2.7	2.9	V
V_{20}	sync tip (negative modulation)	note 7	2.5	2.7	2.9	V
V_{20}	white level (positive modulation)	note 7	4.5	4.7	4.9	V
V_{20}	white spot threshold level		–	5.5	–	V
V_{20}	white spot insertion level		–	4	–	V
Z_{20}	video output impedance		–	25	–	Ω
$I_{20(int)}$	internal bias current of NPN emitter follower output transistor		1.4	1.8	–	mA
I_{source}	maximum source current		10	–	–	mA
B	bandwidth of demodulated output signal		5	6	–	MHz
G_d	differential gain	note 8	–	2	5	%
φd	differential phase	note 8	–	2	5	°
NL	video non linearity	note 9	–	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	–	dB
	1.1 MHz; yellow		50	60	–	dB
	3.3 MHz; blue		55	65	–	dB
	3.3 MHz; yellow		55	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	note 11 see Fig.5				
	V_i = 10 mV input signal		52	57	–	dB
	end of gain control range		57	62	–	dB
V_{20}	residual carrier signal		–	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		–	2	10	mV
AGC						
I_{C11}	allowed leakage of the AGC capacitor		-	-	700	nA
System switch (note 13)						
	AGC on sync tip level for negative modulation signals					
V_{32}	control voltage		0	–	0.8	V
I_{32}	input current		–100	–	–500	µA
	AGC on white level for positive modulation signals					
V_{32}	control voltage		2	–	12	V
I_{32}	input current		0	–	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current		22	27	32	µA
V_1	clamp level		–	3.3	–	V
Tuner AGC						
$V_{9\text{-}10\ (RMS)}$	minimum starting point for tuner take-over (RMS value)		–	–	0.2	mV
$V_{9\text{-}10(RMS)}$	maximum starting point for tuner take-over (RMS value)		100	150	–	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	–	–	mA
V_6	output saturation voltage	I_6 = 2 mA	–	–	300	mV
I_6	leakage current		–	–	1	µA
Δ	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		–	–	1	V
Video Switching Circuit (note 14)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	$V_O = 2.5\ V_{(p\text{-}p)}$	–	1	–	V
I_{13}	input current		–	1.5	5	µA
V_{13}	sync tip clamping at 1 mA level		1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
16(p-p)	Internal video input signal (peak-to-peak value)	V_O = 2.5 V (p-p)	–	2	–	V
I_{16}	input current		–	1.5	5	µA
V_{16}	noise clampling at 1 mA level		2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	positive video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	sync tip signal		–	3	–	V
I_{bias}	internal bias current		1	1.5	–	mA
I_O	maximum output current		5	–	–	mA
α	crosstalk external to internal	notes 12 and 15	–	55	–	dB
α	crosstalk internal to external	notes 12 and 15	–	55	–	dB
Video switch						
V_{18}	input voltage for internal video		–	–	0.8	V
V_{18}	input voltage for external video		2	–	V_P	V
I_{18}	maximum current	pin 18 = 0 V pin 18 = 12 V	– –	0.05 0.25	0.2 1	mA mA
AFC-circuit (note 16)						
I_{22}	AFC sample and hold switch-off current		0.1	–	–	mA
I_O	output current	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current		–	–	1	µA
V_{21}	AFC output voltage swing		10.5	–	11.5	V
I_{21}	available output current		±0.2	–	–	mA
	control slope		–	100	–	mV/kHz
V_{21}	output voltage	AFC off	5.5	6	6.5	V
R_O	AFC output resistance	measured at an input signal amplitude of 150 µV(RMS)	–	40	–	kΩ
$V_{21(p-p)}$	output voltage swing	note 12	–	11	–	V
	control slope	note 12	–	80	–	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 $mV_{(RMS)}$	note 12	–	–2	–	V
AFC polarity switch						
I_{12}	sink current for negative slope		–	–	1	µA
I_{12}	sink current for positive slope		0.1	–	–	mA
I_{12}	maximum current	V_{12} = 0 V	–	–	1	mA
V_{12}	switching level		5	–	7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	–	mV
I_{28}	input current	V_{28} = 5 V V_{28} = 0 V	– –	8 −10	– –	µA mA
First control loop						
Δf_{RX}	PLL holding range		–	±1500	±2000	Hz
Δf_{XL}	PLL catching range		±600	±1500	–	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
Second control loop (positive edge)						
Δtd/Δto	control sensitivity	note 19	–	100	–	
td	control range		–	25	–	µs
Phase adjustment (via second control loop)						
	control sensitivity		–	25	–	µA/µs
α	maximum allowed phase shift		–	±2	–	µs
Horizontal oscillator (note 19)						
f_{ft}	free running frequency	R = 34.3 kΩ C = 2.7 nF	–	15625	–	Hz
Δf_{osc}	spread with fixed external components		–	–	4	%
Δf_{osc}	frequency variations with supply voltage from 10 to 13.2 V		–	–	2	%
ΔfT	frequency variation with temperature	note 12	–	−1.6	–	Hz/K
Δf_{fr}	maximum frequency deviation at start of Horizontal output		–	–	10	%
Δf_{osc}	frequency variation when only noise is received	note 12	–	–	500	Hz
Horizontal output (open collector)						
V_{29}	output limiting voltage		–	–	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	–	0.3	0.5	V
I_{sink}	maximum sink current		10	–	–	mA
S	output signal duty factor		–	46	–	%
t_r	rise time output pulse		–	260	–	ns
t_f	fall times output pulse		–	100	–	ns
Flyback input and sandcastle output (note 22, Fig. 6)						
I_{30}	required input current during flyback pulse		0.1	–	2	mA
V_{30}	output voltage during burstkey horizontal blanking during vertical blanking		 8 4 2.1	 – 4.4 2.5	 – 5 2.9	 V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input and sandcastle output (note 22, Fig. 6)						
t_W	pulse width burst key at: 60 Hz 50 Hz	 60 Hz 50 Hz	 2.9 3.2	 3.3 3.6	 3.7 4	 µs µs
	horizontal blanking		flyback pulse			
	vertical blanking					
T_1	divider in search window	50 Hz 60 Hz	– –	21 17	– –	lines lines
T_2	divider in narrow window	50 Hz 60 Hz	– –	25 21	– –	lines lines
	delay between the start of the sync pulse at the video output and the burst key pulse					
t_{Bkt}	trailing edge	60 Hz	–	–	9.4	µs
t_{Bkr}	rising edge		4.7	5.4	6.1	µs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		–	–	5	kΩ
I_{17}	output current	pin 17 = 0 V	–	–	0.5	mA
VCR switch (auto-VCR mode)						
I_{17}	source current		–	–	30	µA
I_{17}	sink current		–	–	30	µA
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		–	–	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	–	–	1	mA
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)		–	2.2	–	mV
Vertical ramp generator (note 21)						
I_3	input current during scan		–	–	2	µA
I_3	discharge current during retrace		–	0.8	–	mA
$V_{3(p\text{-}p)}$	sawtooth amplitude (peak-to-peak value)		–	1.9	–	V
t	interlace timing of the internal pulses	note 12	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	–	–	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		–	1	–	V
I_5	input current		–	–	12	μA
Δ_{tp}	internal pre-correction to sawtooth		–	3	–	%
	deviation amplitude	50/60 Hz	–	–	2	%
	temperature dependency of the amplitude	note 12 ΔT = 45 °C	–	–	2	%
Vertical guard ($V_{pin\ 30}$ = 2.5 V)						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 22				
	guard level LOW		–	1.5	–	V
	guard level HIGH		–	2	–	V
Coincidence detector/transmitter identification (note 23)						
V_{25}	voltage for in-sync condition		–	9.8	–	V
V_{25}	voltage for no-sync condition	no signal	–	0.3	–	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		–	0.6	–	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		–	2.5	–	V
Video transmitter identification output						
V_{14}	output voltage active	no sync; I = 1 mA	–	0.3	0.5	V
I_{14}	sink current active		–	–	5	mA
I_{14}	output current inactive (transmitter present)		–	–	1	μA
50/60 Hz identification (note 24)						
V_{14}	output voltage at 50 Hz		–	V_s	–	V
V_{14}	output voltage at 60 Hz		–	9	–	V

Notes to the Characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_P) is obtained from the horizontal output stage. The load current of the driver must be added to the value given above.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS) 100% input signal.
6. Projected zero point; i.e. with switched demodulator.

7. The output signal amplitude is determined by the AGC detector. For negative modulation the sync tip level is used as reference. With positive modulation the white level is stabilized.
8. Measured according to the test line given in Fig.3.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
   - The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum devatiation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV (RMS).
11. Measure with a source impedance of 75 Ω.

    $$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \ \textit{black-to-white}}{V_{n(RMS)} \ \textit{at } B = 5 \ \textit{MHz}}$$

12. These figures are based on sample tests.
13. By means of the system switch, two conditions can be obtained. Negative modulation with sync tip level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.
14. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
15. Defined as $20 \log \frac{V_O \ \textit{unwanted video black-to-white}}{V_O \ \textit{wanted video-black-to-white}}$; measured at 4.4 MHz.
16. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70.

    With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_P$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
19. This figure is valid for an external load impedance of 82 Ω from pin 31 to the shift adjustment potentiometer.
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.

22. To avoid CRT screen burn due to a collapse of the vertical deflection a continuous blanking level is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
23. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin.

    The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 / µs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
24. When the mute is active no 50/60 Hz information is available.

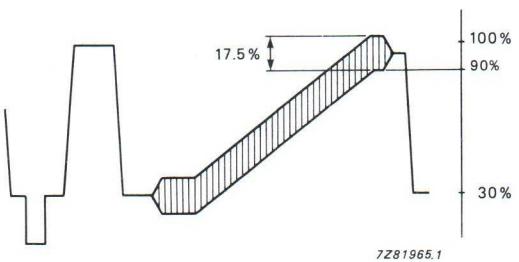


Fig.2 Video output signal.

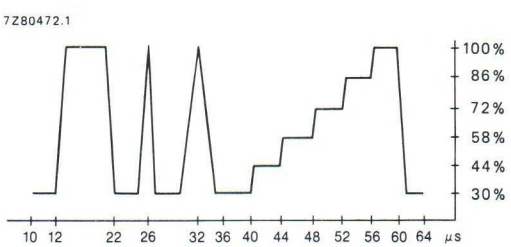
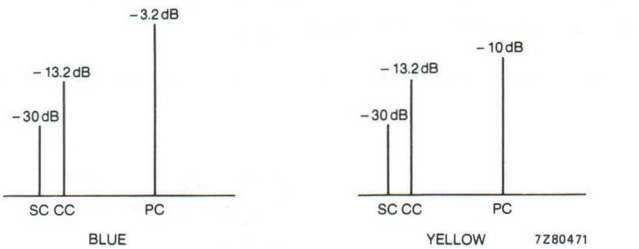
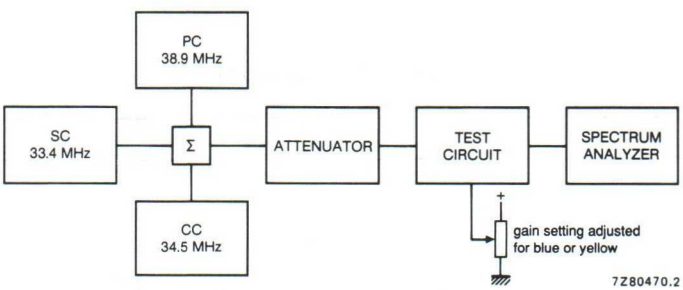


Fig.3 EBU test signal waveform (line 17).





Input signal conditons

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to top sync level

$$Value\ at\ 1.1MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 1.1MHz} + 3.6dB$$

$$Value\ at\ 3.3MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 3.3MHz}$$

Fig.4 Test set-up intermodulation.

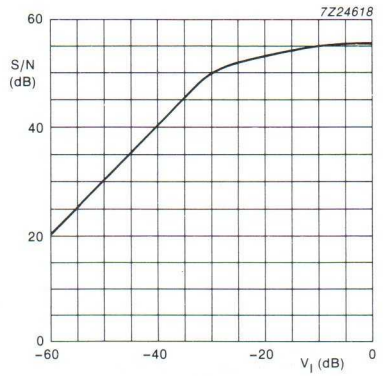
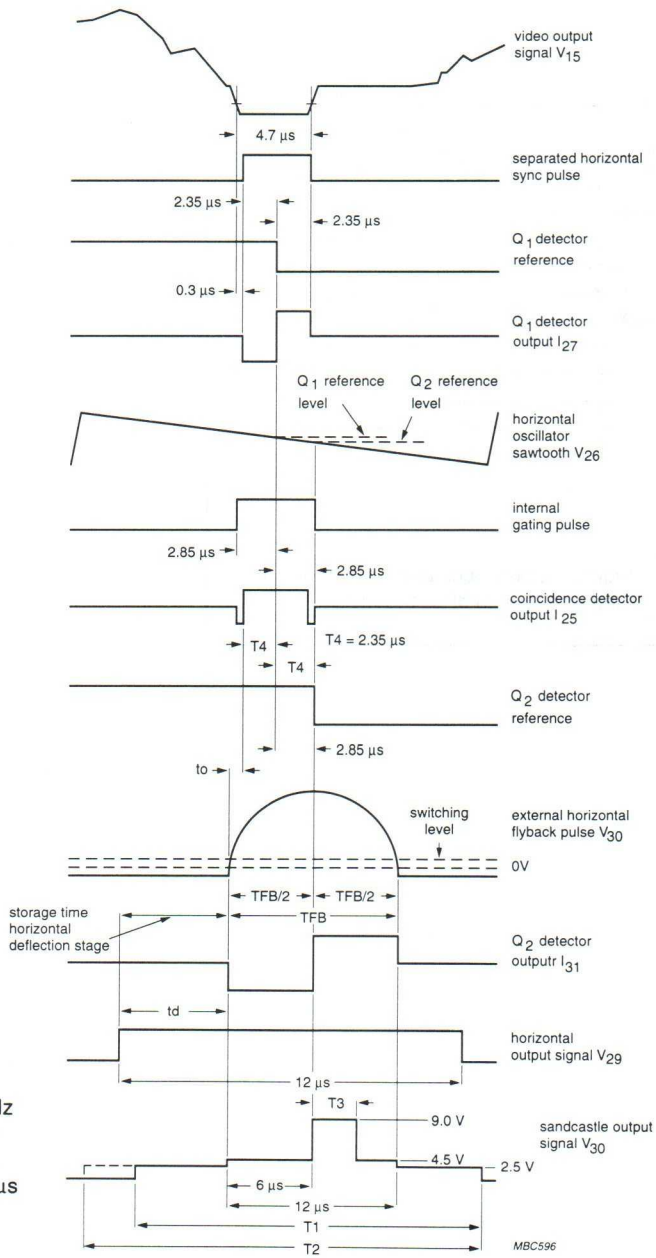


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



	50 Hz	60 Hz
T_1 - search window -	42 p	34 p
T_2 - narrow window -	50 p	42 p
T_3 - burst key pulse -	3.6 µs	3.3 µs

$(p = \frac{1}{2f_H})$

Fig.6 Timing diagram.

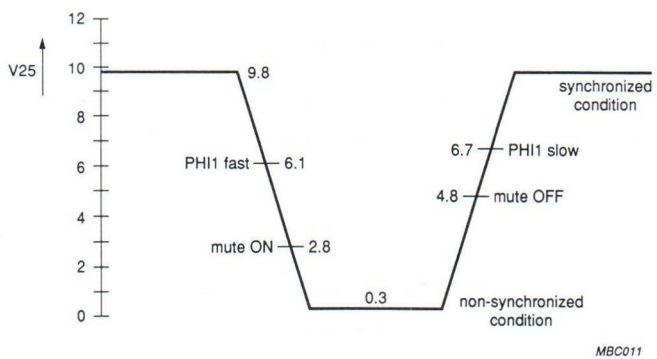


Fig.7 Switching levels coincidence detector.

COINCIDENCE DETECTOR SWITCHING LEVELS

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
			T2 – T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} > 6.7 V and		
		strong signal	11.3	7.6
		weak signal	1.3	1.3
		V_{25} < 6.1 V and		
		strong signal	11.3	7.6
		weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V	1.3	1.3
		V_{25} < 6.1 V	11.3	7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

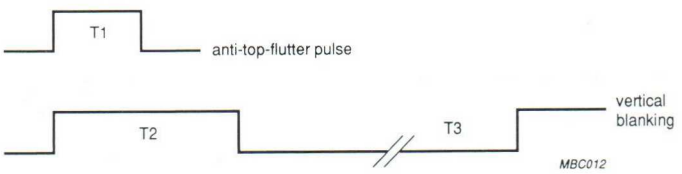


Fig.8 Horizontal oscillator control sensitivity.

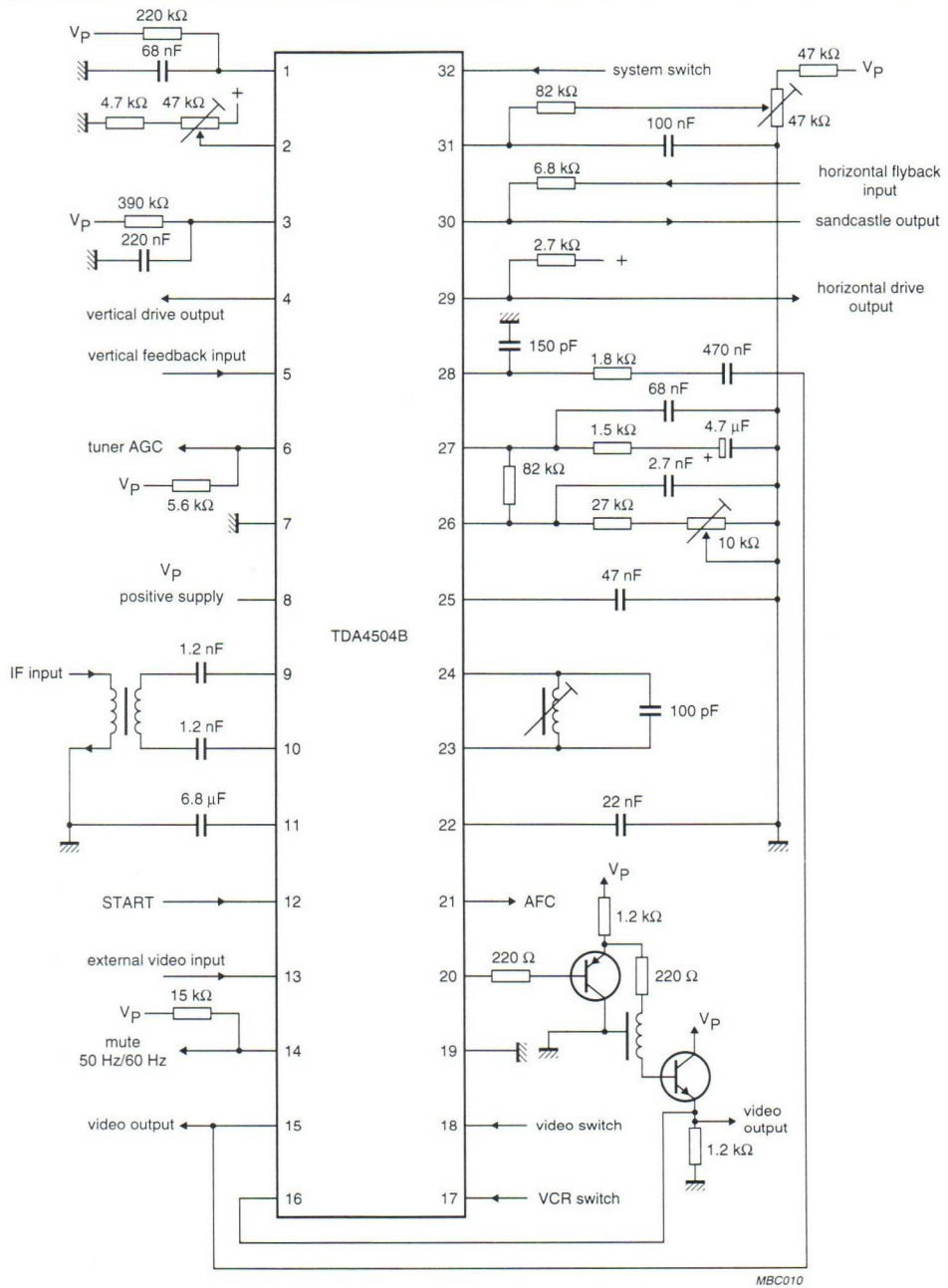


Fig.9 Application diagram.

PAL DECODER

The TDA4510 is a colour decoder for the PAL standard, which is pin sequent compatible with multi-standard decoder TDA4555 and also pin compatible with NTSC decoder TDA4570. It incorporates the following functions:

Chrominance part

- Gain controlled chrominance amplifier with operating point control stage
- Chrominance output stage for driving the 64 μs delay line
- Blanking circuit for the colour burst signal
- Automatic chrominance control (ACC) with sampled rectifier during burst-key

Oscillator and control voltage part

- Reference oscillator for double subcarrier frequency
- Gated phase comparison
- Identification demodulator and automatic colour killer
- Sandcastle pulse detector
- Service switch

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Colour switching stages
- Separate colour switching output
- (B-Y) and (R-Y) signal output stages
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7-3}$	typ.	12 V
Supply current	$I_P = I_7$	typ.	50 mA
Chrominance input signal (peak-to-peak)	$V_{9-3(p-p)}$		10 to 400 mV
Chrominance output signal (peak-to-peak)	$V_{6-3(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
—(R-Y) signal	$V_{1-3(p-p)}$	typ.	1,05 V ± 2 dB
—(B-Y) signal	$V_{2-3(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse, required amplitude for			
burst gating level	V_{15-3}	typ.	7,7 V
horizontal pulse separation	V_{15-3}	typ.	4,5 V
vertical and horizontal pulse separation	V_{15-3}	typ.	2,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

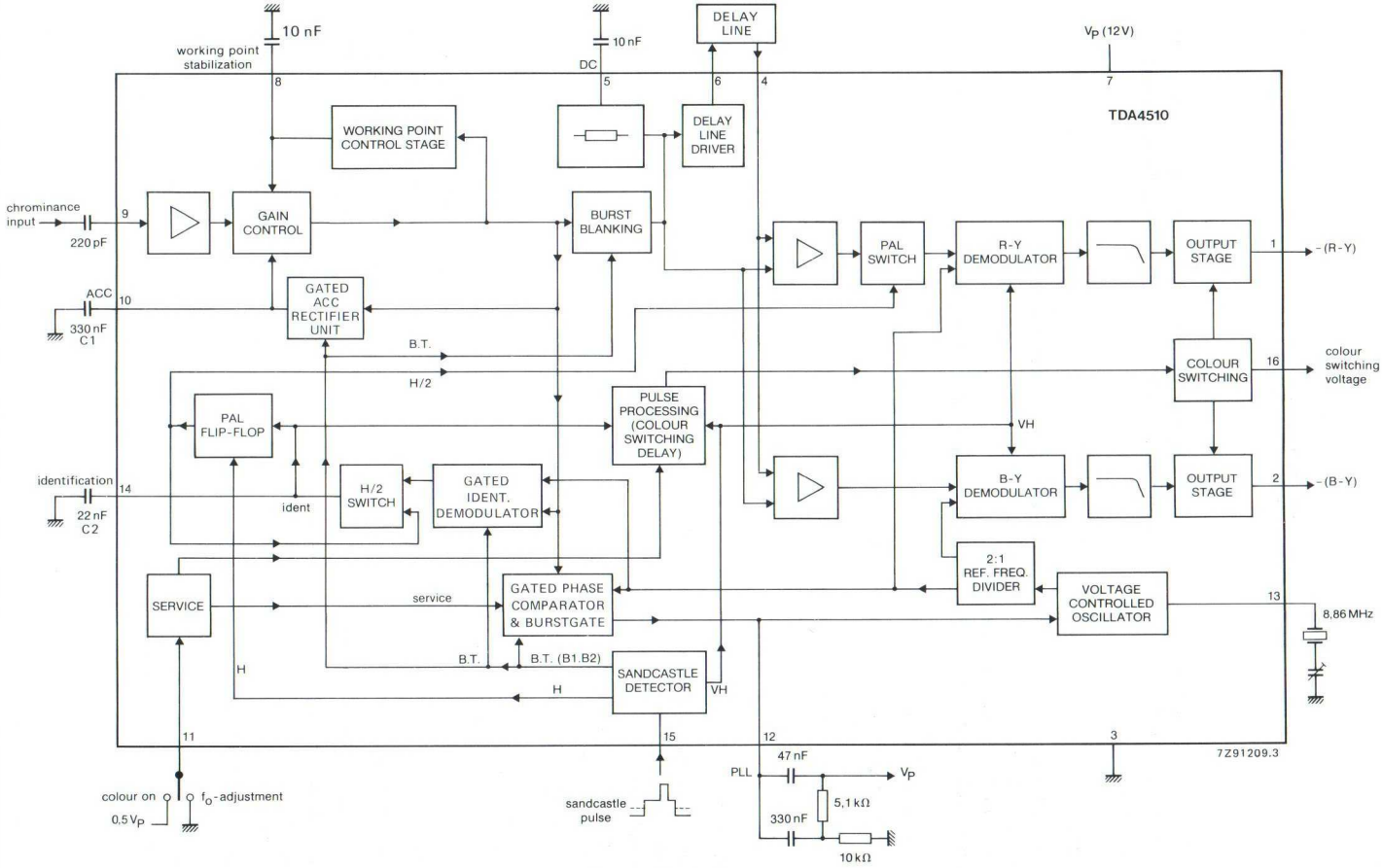


Fig. 1 Block diagram.

External capacitors in Fig. 1

C1 filter capacitor for control voltage (pin 10)
C2 filter capacitor for identification signal (pin 14)

FUNCTIONAL DESCRIPTION

DIVIDER STAGES

The divider stages provide −(R-Y) and −(B-Y) reference signals with the correct 90 degrees relation for the demodulators.

PHASE COMPARATOR

The phase comparator compares the −(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator.

IDENTIFICATION DEMODULATOR

The identification demodulator delivers a positive going identification signal for PAL-signals at pin 14, also used for the automatic colour-killer.

SERVICE SWITCH

The service switch has two functions. The first position ($V_{14-3} < 1$ V) allows the adjustment of the reference oscillator. Therefore the colour is switched on and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5$ V) switches the colour on and the output signals can be observed.

SANDCASTLE PULSE DETECTOR

Sandcastle pulse detector for burst-gate, line and blanking (horizontal and vertical) pulse detection. The vertical part of the sandcastle pulse is needed for the internal colour-on and colour-off delay.

PULSE PROCESSING PART

Pulse processing part which shall prevent a premature switching on of the colour. The colour-on delay, two or three field periods after identification of the PAL signal, is achieved by a counter. The colour is switched off immediately or at the latest one field period after disappearance of the identification voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2	V
Currents			
at pins 1 and 2	$-I_{1,2}$	max. 5	mA
at pin 6	$-I_6$	max. 15	mA
at pin 16	$-I_{16}$	max. 5	mA
Total power dissipation	P_{tot}	max. 800	mW
Storage temperature	T_{stg}	−25 to + 150	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	I_7	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9\text{-}3(p\text{-}p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9\text{-}3(p\text{-}p)}$	–	100	–	mV
Input impedance	$Z_{9\text{-}3}$	–	3,3	–	kΩ
Input capacitance	$C_{9\text{-}3}$	–	4	–	pF
Colour ON					
Chrominance output voltage (peak-to-peak) with 75% colour bar signal	$V_{6\text{-}3(p\text{-}p)}$	–	1,6	–	V
d.c. voltage at chrominance output	$V_{6\text{-}3}$	–	8,2	–	V
Oscillator and control voltage part					
Oscillator frequency	f_o	–	8,8	–	MHz
Input resistance	$R_{13\text{-}3}$	–	350	–	Ω
Catching range (depending on RC-network at pin 12)	f	± 400	–	–	Hz
Control voltage					
without burst signal	$V_{14\text{-}3}$	–	6,0	–	V
colour on switching threshold	$V_{14\text{-}3}$	–	6,6	–	V
hysteresis of colour switching	$V_{14\text{-}3}$	–	150	–	mV
flip-flop correction (FFC) voltage	$V_{14\text{-}3}$	–	5,5	–	V
hysteresis of FFC	$V_{14\text{-}3}$	–	170	–	mV
Colour-on delay		2	–	3	f.p.*
Colour-off delay		0	–	1	f.p.*
First service position (PLL is inactive for oscillator adjustment, colour on)	$V_{11\text{-}3}$	0	–	1	V
second service position (colour on)	$V_{11\text{-}3}$	5	–	–	V
Colour switching output (open npn emitter)					
output current	$-I_{16}$	–	–	5	mA
colour-on voltage	$V_{16\text{-}3}$	–	6	–	V
colour-off voltage	$V_{16\text{-}3}$	–	0	–	V
Demodulator part					
Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	–	200	–	mV
Colour difference output signals (peak-to-peak value)					
–(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	1,06	1,33	1,67	V

parameter	symbol	min.	typ.	max.	unit
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1\text{-}3}/V_{2\text{-}3}$	0,71	0,79	0,87	V
D.C. voltage at colour difference outputs	$V_{1;\,2\text{-}3}$	–	7,7	–	V
Residual carrier voltage at colour difference outputs					
1 x subcarrier frequency (4,4 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
2 x subcarrier frequency (8,8 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
Sandcastle pulse detector					
Thresholds:					
Field- and line-pulse separation pulse ON	$V_{15\text{-}3}$	1,3	1,6	1,9	V
Required pulse amplitude	$V_{15\text{-}3}$	2,0	2,5	3,0	V
Line pulse separation; pulse ON	$V_{15\text{-}3}$	3,3	3,6	3,9	V
Required pulse amplitude	$V_{15\text{-}3}$	4,1	4,5	4,9	V
Burst pulse separation; pulse ON	$V_{15\text{-}3}$	6,6	7,1	7,6	V
Required pulse amplitude	$V_{15\text{-}3}$	7,7	–	–	V
Input voltage during horizontal scanning	$V_{15\text{-}3}$	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

* f.p. is shortening for field periods in this case.

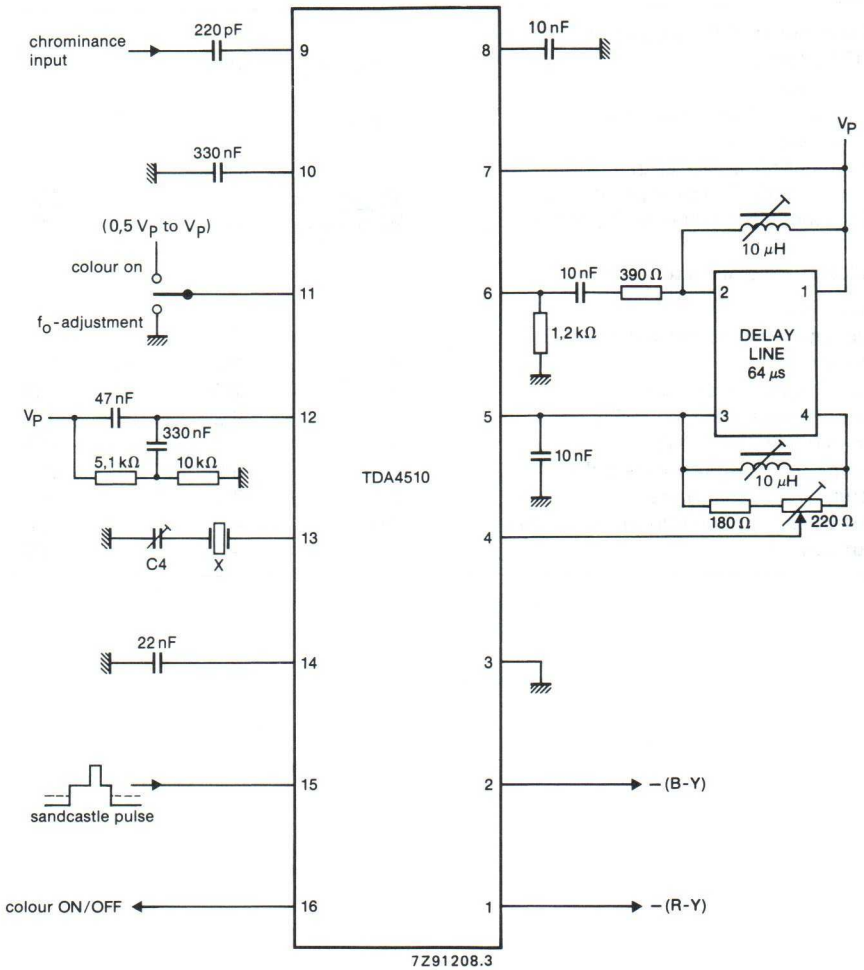


Fig. 2 Application information and test circuit.

C4 = 5 to 27 pF, X = 8,8 MHz; nominal frequency 8,867 238 MHz; resonance resistance 60 Ω, load capacitance 20 pF, dynamic capacitance 22 fF and static capacitance 5,5 pF.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4555 and TDA4556 are monolithic integrated multistandard colour decoders for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the colour difference output signals (B-Y) and (R-Y).

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	65 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 200 mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
TDA4555: –(R-Y); **TDA4556:** + (R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V ± 2 dB
TDA4555: –(B-Y); **TDA4556:** + (B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	typ.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

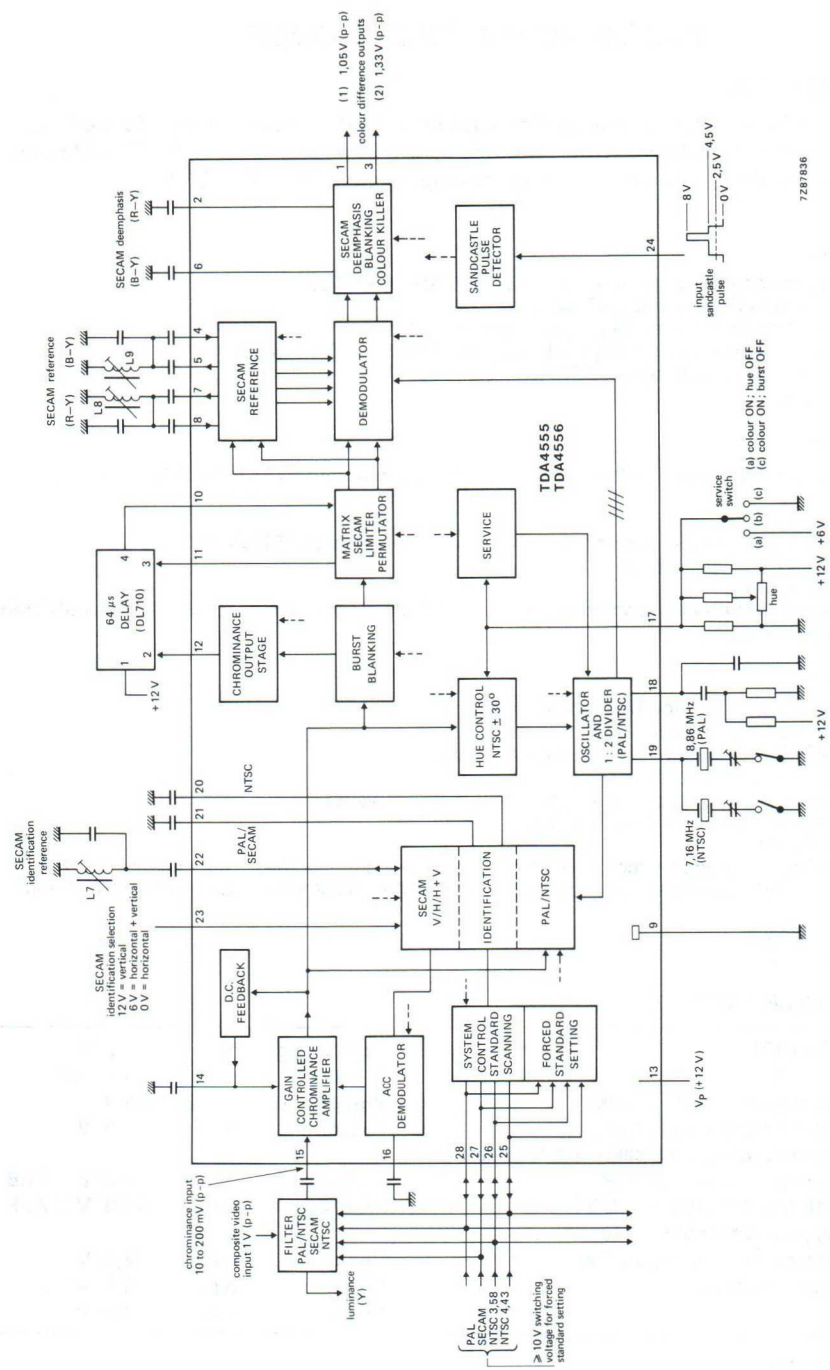


Fig. 1 Block diagram.

(1) TDA4555: −(R-Y); TDA4556: + (R-Y)
(2) TDA4555: −(B-Y); TDA4556: + (B-Y)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	8	mA
Peak value	I_{12M}	max.	15	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	65	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	200	mV
input impedance	$\lvert Z_{15-9}\rvert$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12-9}\rvert$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
TDA4555					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1-9(p-p)}$	–	–	10	mV
D.C. output voltage					
n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3-9}$	–	7,7	–	V
output impedance	$\lvert Z_{1,3-9}\rvert$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555					
–(R-Y) signal (pin 1	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
TDA4556					
+(R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
+(B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T$(R-Y)	–	–0,55	–	mV/K
	$\Delta V/\Delta T$(B-Y)	–	+0,25	–	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	–	30**	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	–	30**	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

** Relative to phase at V_{17-9} = 3 V.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3,58 MHz) at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0,5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28-9}$	–	2,45	–	V
colour ON	$V_{25,26,27,28-9}$	–	5,8	–	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	V_{28-9}	9	–	–	V
SECAM	V_{27-9}	9	–	–	V
NTSC 3,58 MHz	V_{26-9}	9	–	–	V
NTSC 4,43 MHz	V_{25-9}	9	–	–	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1,2	–	2,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3,2	–	4,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	4,0	–	5,0	V
to separate burst gating pulse	$V_{24\text{-}9}$	6,5	–	7,7	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

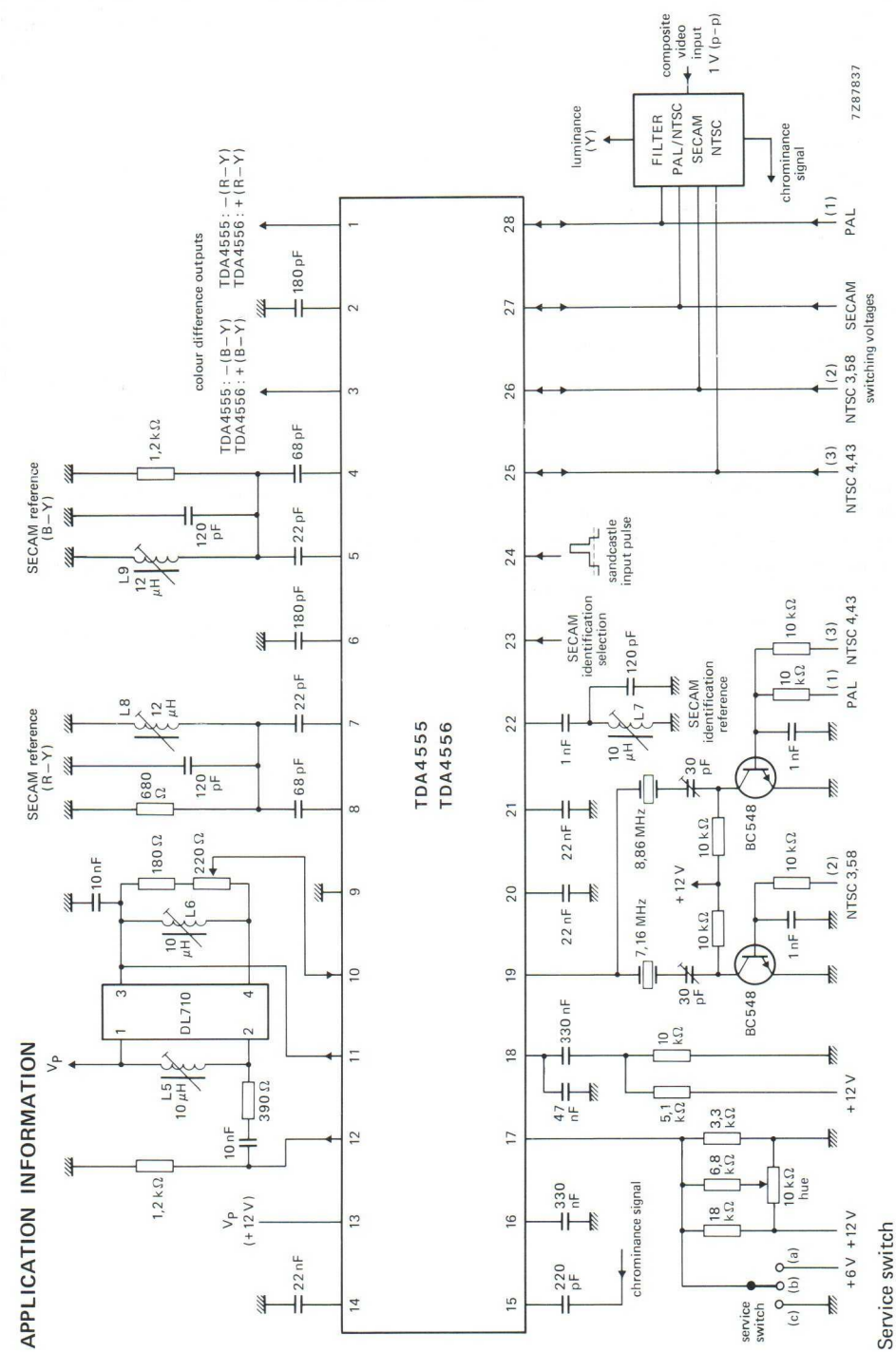


Fig. 2 Application diagram.

Service switch
(a) colour ON; hue OFF
(c) colour ON; burst OFF

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4557 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz standards.

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the demodulators (PAL, NTSC, SECAM)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit and 50/60 Hz recognition
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	10.8	12.0	13.2	V
Supply current (pin 13)	I_P	–	65	–	mA
Chrominance input voltage (peak-to-peak value)	$V_{15(p\text{-}p)}$	20	100	400	mV
Chrominance output voltage (peak-to-peak value)	$V_{12(p\text{-}p)}$	–	1.6	–	V
Colour difference output voltages (peak-to-peak values)					
–(R-Y)	$V_{1(p\text{-}p)}$	–	1.05 V ± 2 dB	–	V
–(B-Y)	$V_{3(p\text{-}p)}$	–	1.33 V ± 2 dB	–	V
Sandcastle pulse (pin 24)					
Required amplitude to separate					
vertical and horizontal pulse	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
horizontal pulse	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
burst gating pulse	$V_{24(p\text{-}p)}$	7.7	–	V_P	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

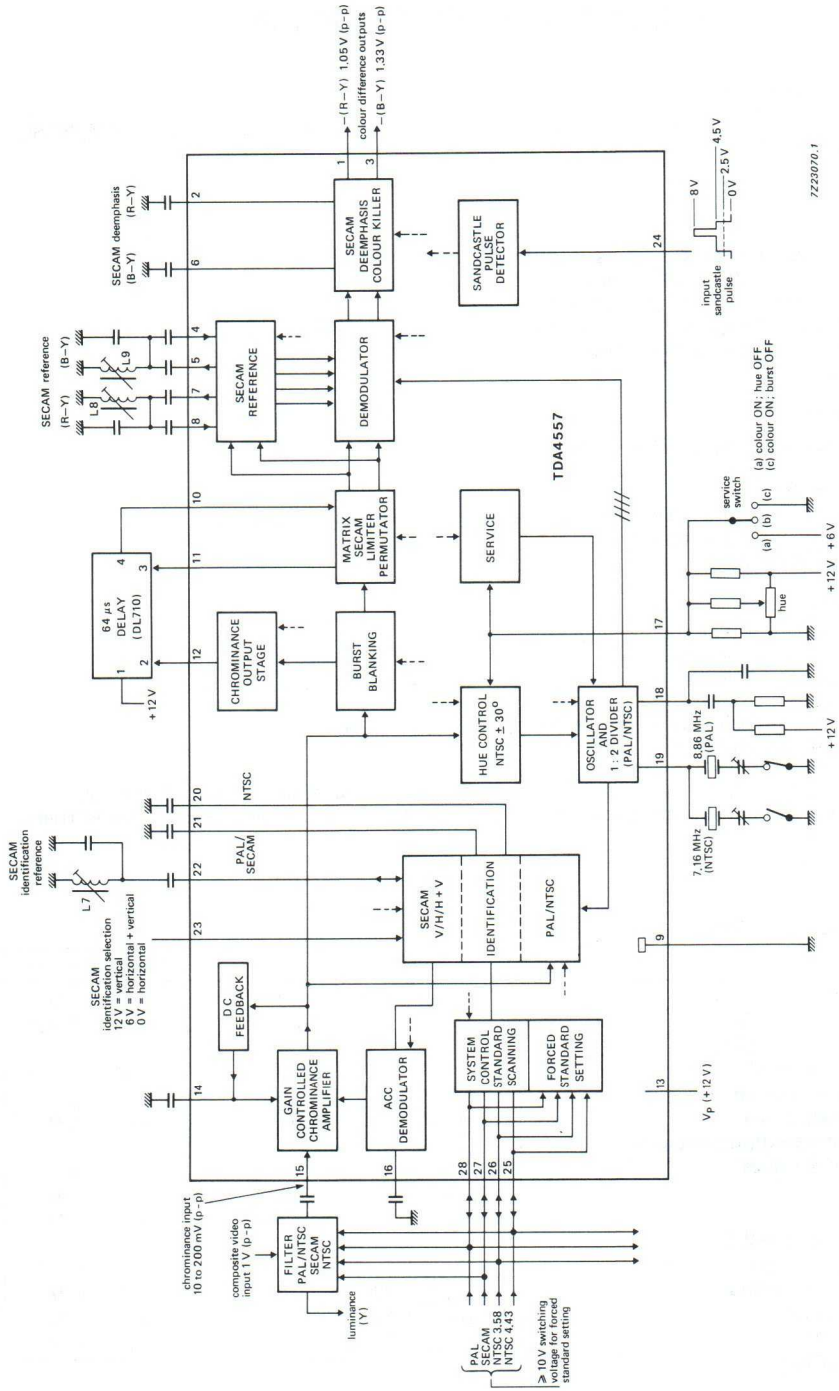


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	V_P	–	13.2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	$V_{n\text{-}9}$	0	V_P	V
Current at pin 12	I_{12}	–	8	mA
Peak value	I_{12M}	–	15	mA
Total power dissipation	P_{tot}	–	1.4	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	V_P	10.8	12	13.2	V
Supply current	I_P	50	65	80	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
input impedance	$\|Z_{15-9}\|$	7	10	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12(p-p)}$	1.1	1.6	1.75	V
output impedance (npn emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
DC output voltage	V_{12-9}	7.3	8.2	9.0	V
Input for delayed signal (pin 10)					
DC input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1(p-p)}$	–	–	10	mV
DC output voltage					
npn emitter follower with internal current source of 0.3 mA	$V_{1,3-9}$	7.0	7.7	8.4	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
–(R-Y) signal (pin 1	$V_{1(p-p)}$	–	1.05	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3(p-p)}$	–	–	30	mV
DC output voltage	$V_{1,3-9}$	7.0	7.7	8.4	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$ $\Delta V/\Delta V_P$	– –	0.5 8	0.6 –	mV/K mV/V
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	30	40	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	30	40	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	0	–	0.5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	V_P	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3.58 MHz) at pin 25 (NTSC 4.43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0.5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28-9}$	2.1	2.45	2.7	V
colour ON	$V_{25,26,27,28-9}$	5.5	5.8	6.2	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	V_{28-9}	9	–	V_P	V
SECAM	V_{27-9}	9	–	V_P	V
NTSC 3.58 MHz	V_{26-9}	9	–	V_P	V
NTSC 4.43 MHz	V_{25-9}	9	–	V_P	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	0	–	2	V
vertical identification (V)	V_{23-9}	10	–	V_P	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3.58 MHz-NTSC 4.43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

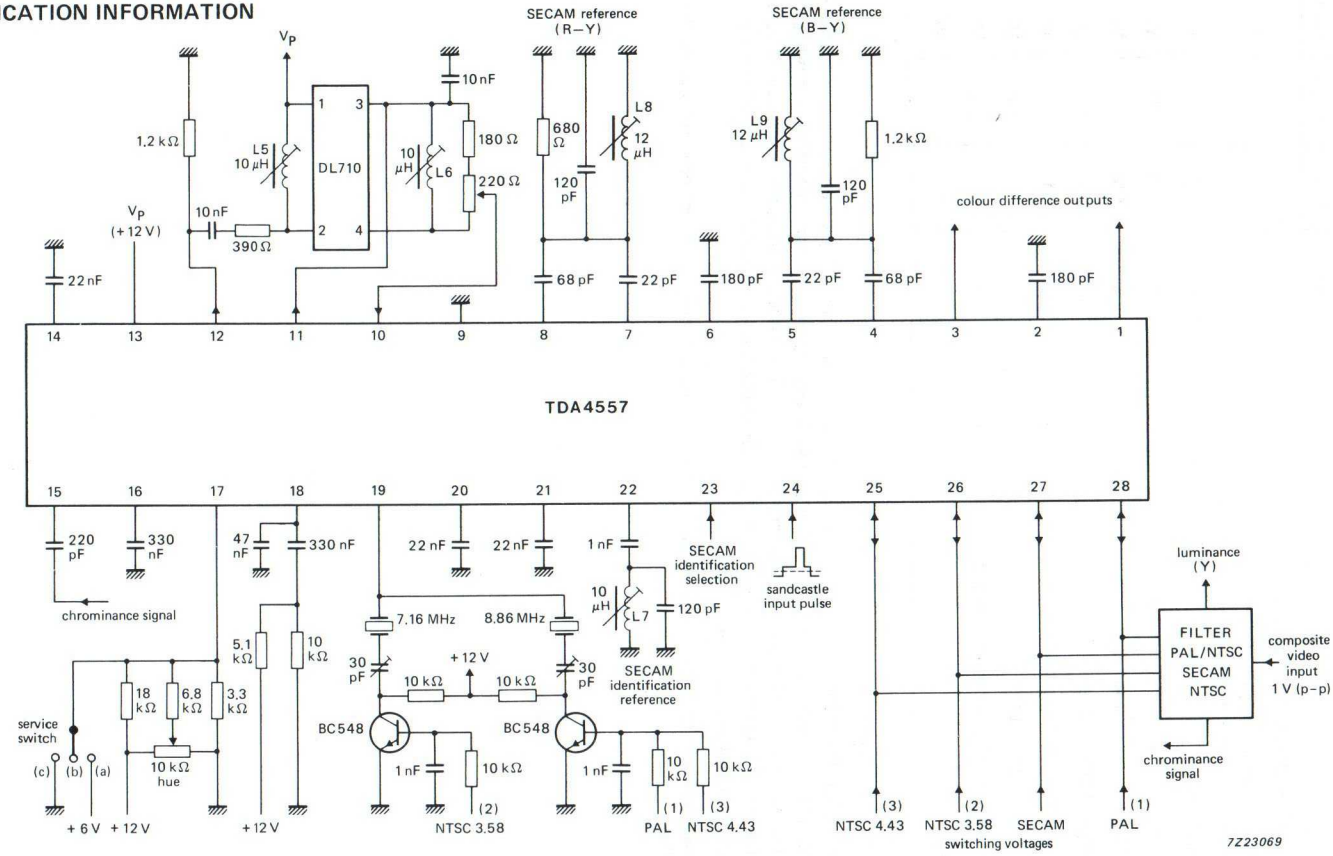
* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1.3	1.6	1.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3.3	3.6	3.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
to separate burst gating pulse	$V_{24\text{-}9}$	6.6	7.1	7.6	V
required pulse amplitude	$V_{24(p\text{-}p)}$	7.7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1.0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION



Service switch

(a) colour ON; hue OFF
(c) colour ON; burst OFF

Fig. 2 Application diagram.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d	720 to	1035	ns
Y-attenuation	α_y	typ.	7	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

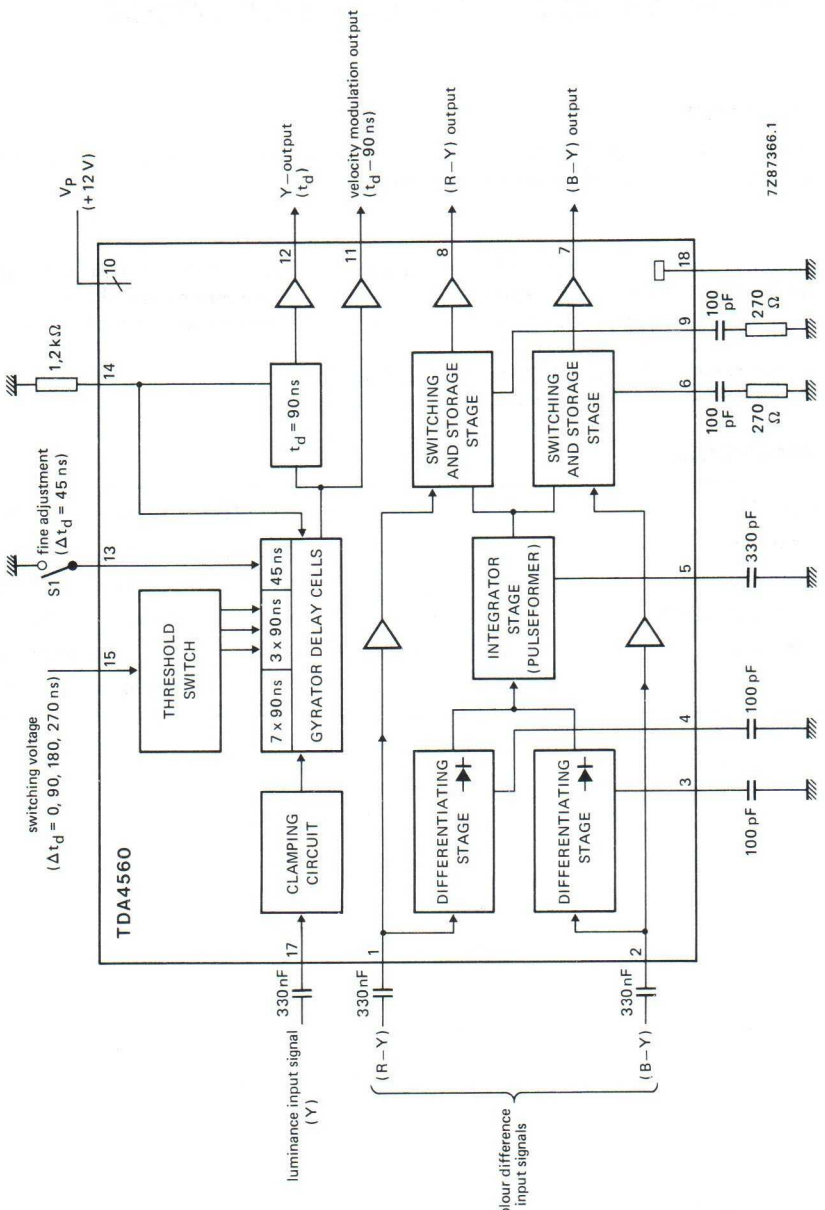


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC)

Supply voltage (pin 10)	$V_P = V_{10-18}$	max. 13,2	V
Voltage ranges to pin 18 (ground)			
at pins 1,2,12,15	V_{n-18}	0 to V_P	V
at pin 11	V_{11-18}	0 to (V_P–3V)	V
at pin 17	V_{17-18}	0 to 7	V
Voltage ranges			
at pin 7 to pin 6	V_{7-6}	0 to 5	V
at pin 8 to pin 9	V_{8-9}	0 to 5	V
Currents			
at pins 6,9	$\pm I_{6,9}$	max. 15	mA
at I_7, I_8, I_{11}, I_{12}		internally limited	
Total power dissipation	P_{tot}	max. 1,1	W
Storage temperature range	T_{stg}	–25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	50	mA
Colour difference channels (pins 1 and 2);					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1,33	–	V
Input resistance	$R_{1,\,2-18}$	–	12	–	kΩ
Internal bias (input)	$V_{1,\,2-18}$	–	4,3	–	V
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output voltage (d.c.)	$V_{7,\,8-18}$	–	4,4	–	V
Output current (emitter follower with constant current source 0,65 mA)	$-I_{7,8}$	–	1,2	–	mA
(R-Y) and B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Internal bias voltage (during clamping)	V_{17-18}	–	1,5	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}$	α_Y	–	8	–	dB
Y-signal attenuation $\frac{V_{12}}{V_{17}}$	α_Y	–	7	–	dB
Output voltage (d.c.)	V_{11-18}	–	2,3	–	V
Output voltage (d.c.)	V_{12-18}	–	10,3	–	V
Output current (emitter follower with constant current source 0,45 mA)	$-I_{11,12}$	–	1,2	–	mA
Frequency response (note 1) $R_{14-18} = 1{,}2$ kΩ; $V_{15-18} = 12$ V	f_{12-17}	–	5	–	MHz

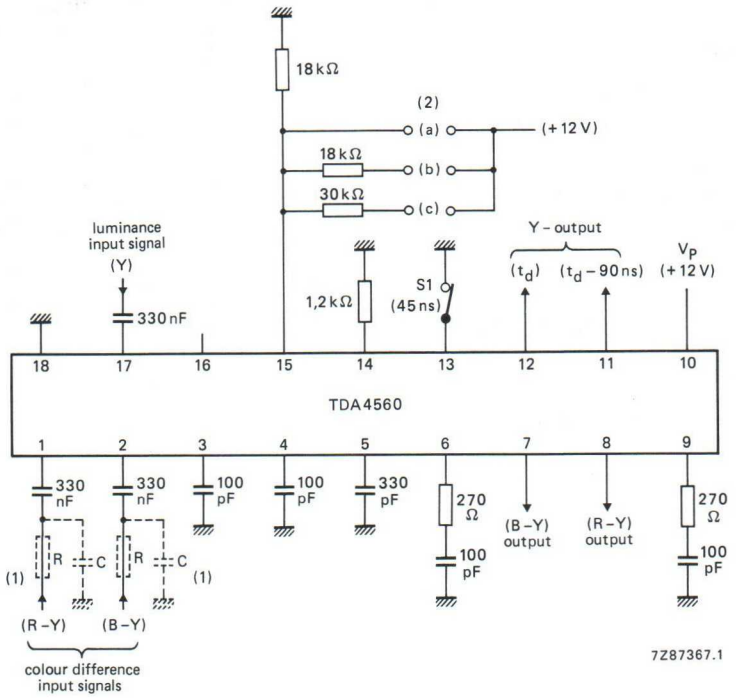
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17)					
Adjustable delay (note 2) (switch open)					
at $V_{15\text{-}18}$ = 0 to 2,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3,5 to 5,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	810	–	ns
at $V_{15\text{-}18}$ = 6,5 to 8,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	900	–	ns
at $V_{15\text{-}18}$ = 9,5 to 12 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed) at $V_{13\text{-}18}$ = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	–	–	70	K/W

NOTES TO THE CHARACTERISTICS

1. $R_{14\text{-}18}$ influences the bandwidth.
2. Delay time is proportional to resistor $R_{14\text{-}18}$.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
O	O	O	0 to 2,5 V	720
O	O	X	3,5 to 5,5 V	810
O	X	X	6,5 to 8,5 V	900
X	X	X	9,5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4565 is a monolithic integrated circuit for coulour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 730 ns to 1000 ns in steps of 90 ns and additional fine adjustment of 50 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	760	820	880	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	850	910	970	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	940	1000	1060	ns
Y-signal attenuation	0.5 MHz	α_Y	0	6.5	8.0	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

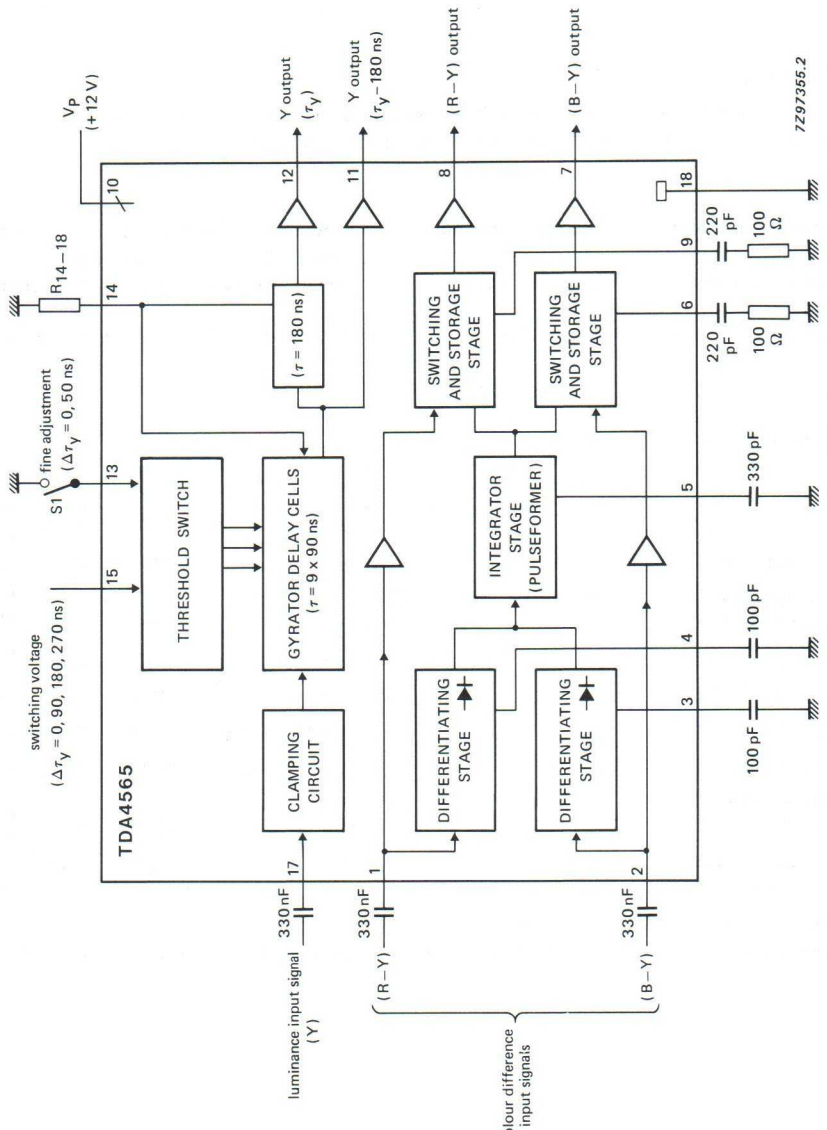


Fig.1 Block diagram.

DEVELOPMENT DATA

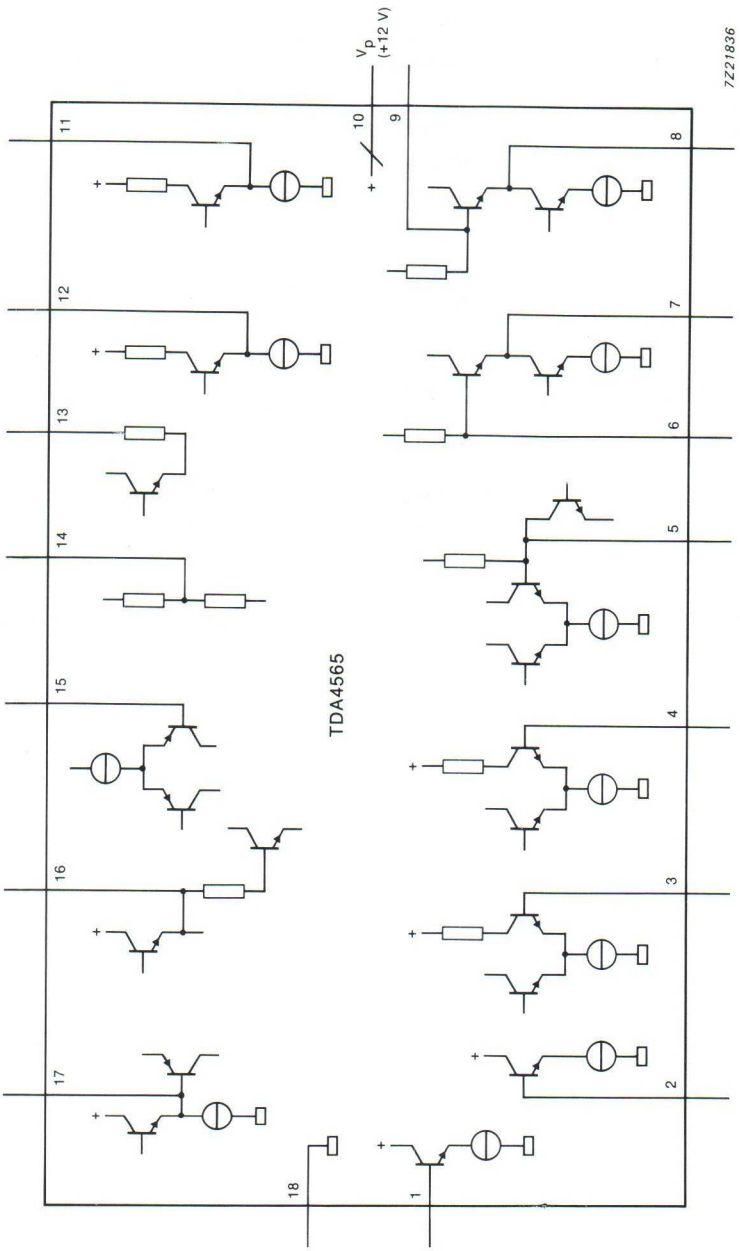


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10\text{-}18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	$V_{n\text{-}18}$	0	V_p	V
at pin 11	$V_{11\text{-}18}$	0	(V_p −3 V)	V
at pin 17	$V_{17\text{-}18}$	0	7	V
Voltage ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0	5	V
Currents				
at pins 6, 9	$I_{6, 9}$	−10	+10	mA
at pins 7, 8, 11 and 12	$I_{7, 8, 11, 12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	1.05	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	1.33	1.9	V
Input resistance (R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage (R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation (R-Y)		V_8/V_1	−1	0	+1	dB
(B-Y)		V_7/V_2	−1	0	+1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance (B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage (B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	1	1.4	V
Internal bias voltage	during clamping	V_{17-18}	1.3	1.5	1.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4)					
at V_{15-18} = 0 to 2.5 V		t_{17-18}	670	730	790	ns
at V_{15-18} = 3.5 to 5.5 V		t_{17-18}	760	820	880	ns
at V_{15-18} = 6.5 to 8.5 V		t_{17-18}	850	910	970	ns
at V_{15-18} = 9.5 to 12 V		t_{17-18}	940	1000	1060	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	30	50	70	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12}.\Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12}.\Delta V_p}$	–	−0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	5.0	6.5	8.0	dB
pin 12 from pin 17		V_{12}/V_{17}	5.0	6.5	8.0	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB

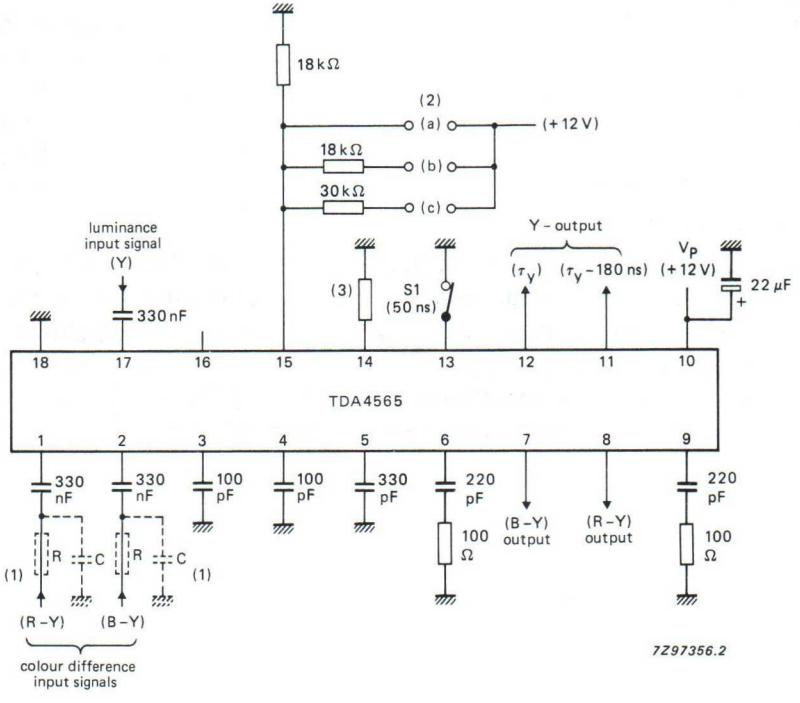
parameter	conditions	symbol	min.	typ.	max.	unit
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\,12}$	–	–	0.4	mA
sink		$-I_{11,\,12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4565
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4565A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	730
0	0	X	3.5 to 5.5 V	820
0	X	X	6.5 to 8.5 V	910
X	X	X	9.5 to 12 V	1000

Where: X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 50 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+ 1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

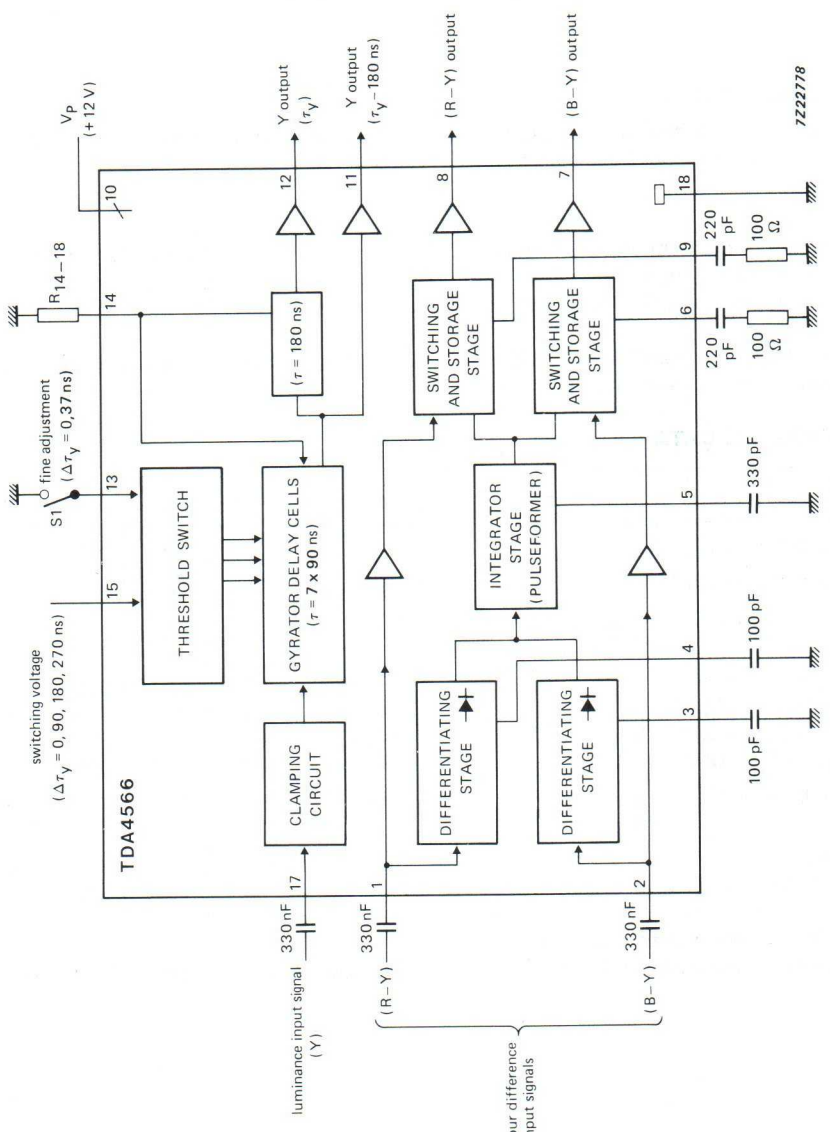


Fig.1 Block diagram.

DEVELOPMENT DATA

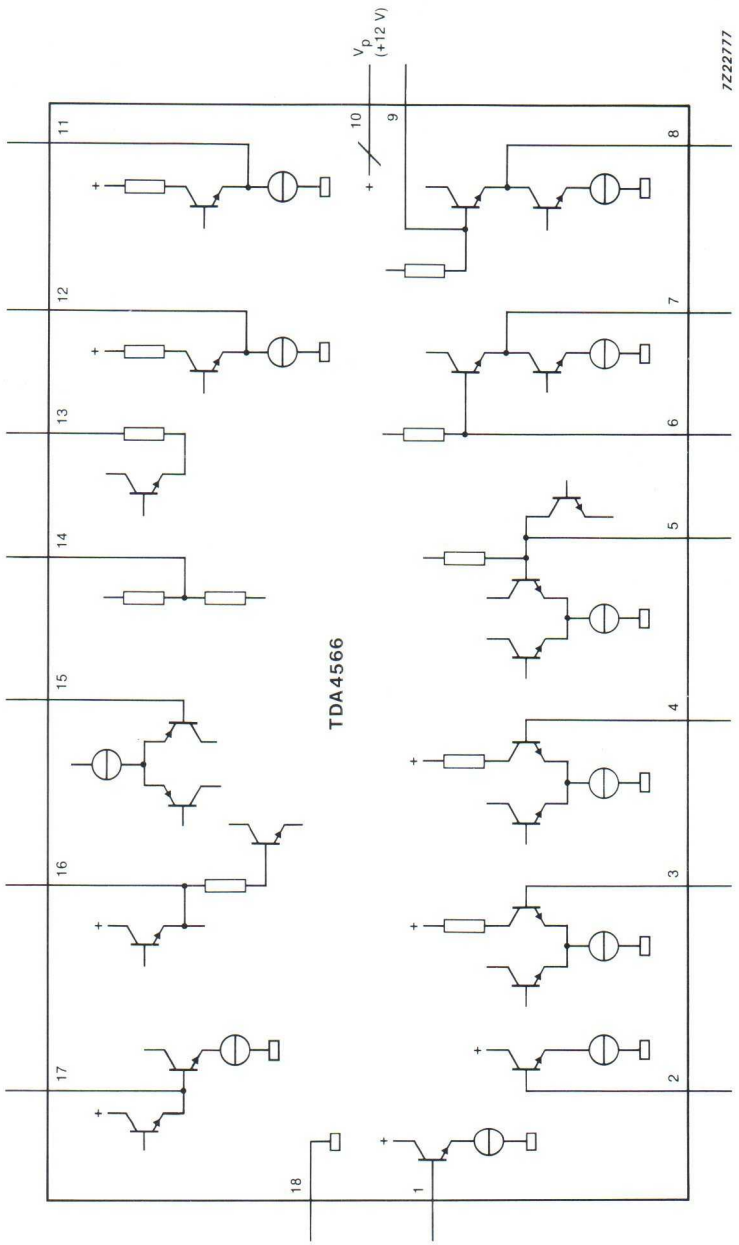


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10\text{-}18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	$V_{n\text{-}18}$	0	V_P	V
at pin 11	$V_{11\text{-}18}$	0	(V_P–3 V)	V
at pin 17	$V_{17\text{-}18}$	0	7	V
Voltage ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0	5	V
Currents				
at pins 6, 9	$I_{6,9}$	–10	+ 10	mA
at pins 7, 8, 11 and 12	$I_{7,8,11,12}$		internally limited	
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	0.63	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+ 1	dB
(B-Y)		V_7/V_2	−1	0	+ 1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	V_{17-18}	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4					
at V_{15-18} = 0 to 2.5 V		t_{17-18}	490	550	610	ns
at V_{15-18} = 3.5 to 5.5 V		t_{17-18}	580	640	700	ns
at V_{15-18} = 6.5 to 8.5 V		t_{17-18}	670	730	790	ns
at V_{15-18} = 9.5 to 12 V		t_{17-18}	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

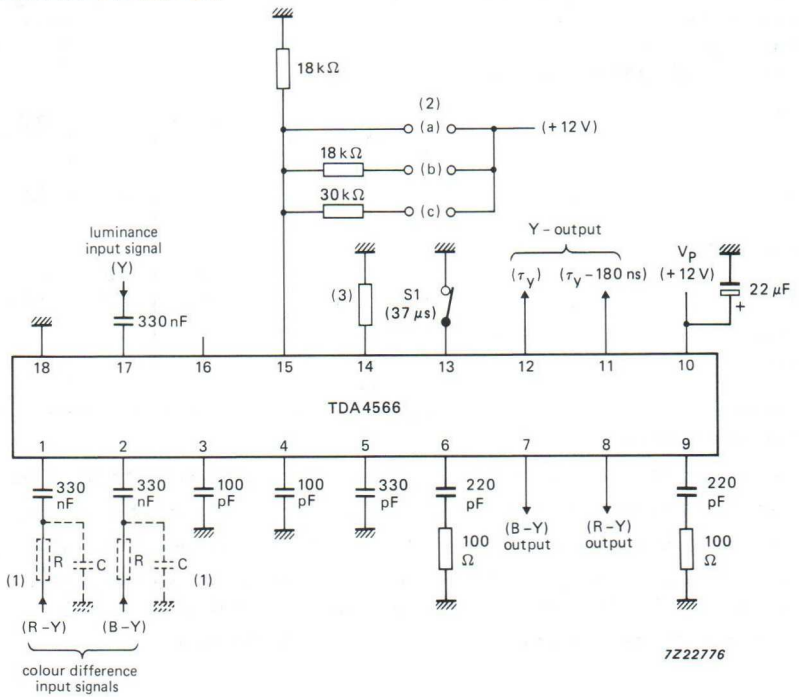
parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4566.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4566A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

LUMINANCE SIGNAL DELAY CIRCUIT

GENERAL DESCRIPTION

The TDA4568 is an integrated circuit that provides the luminance signal delay in colour television receivers.

Features

- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	22	–	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

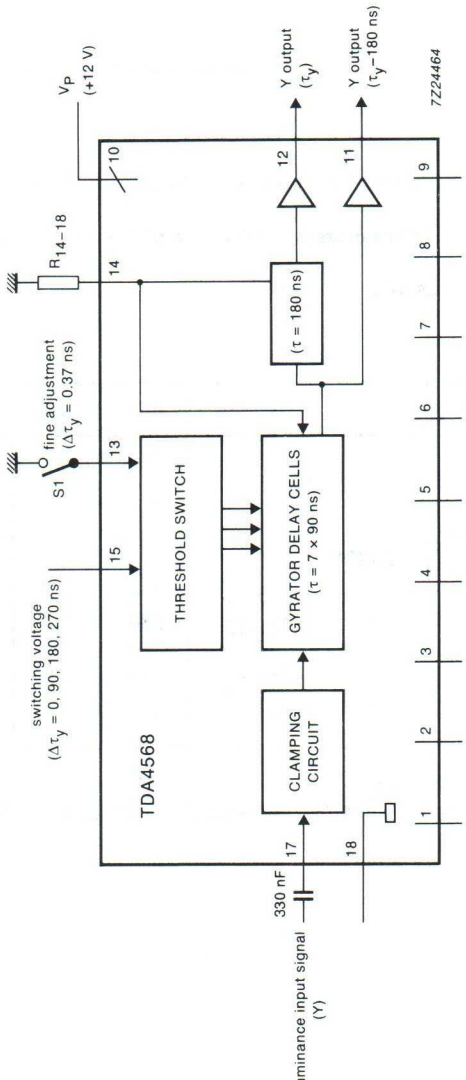


Fig.1 Block diagram.

DEVELOPMENT DATA

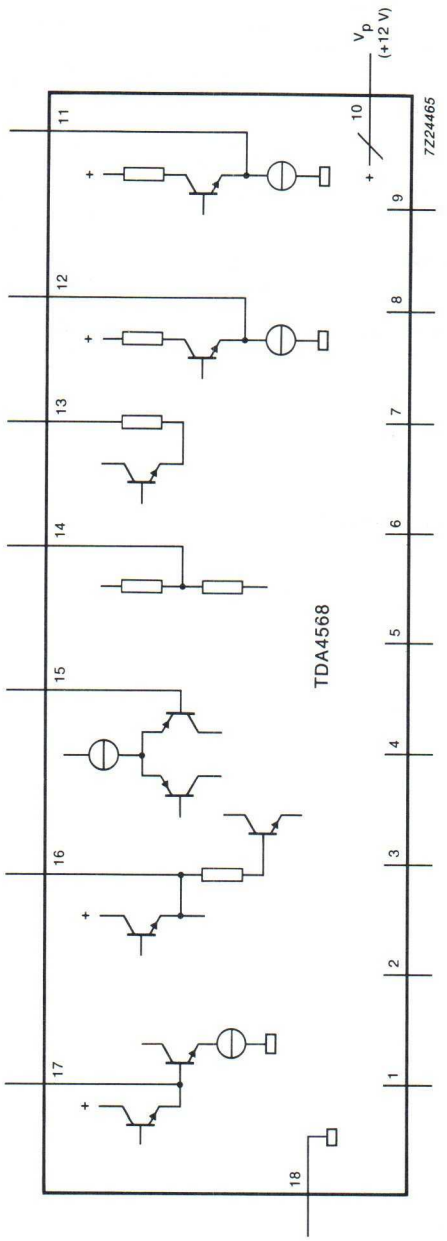


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10\text{-}18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pin 15	$V_{15\text{-}18}$	0	V_P	V
at pin 17	$V_{17\text{-}18}$	0	7	V
Current range at pins 11 and 12	$I_{11, 12}$		internally limited	
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a} = 70$ K/W

Note

Pins 13 and 14, DC potential not published.

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	22	–	mA
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	V_{17-18}	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; $R_{14} = 1.2$ kΩ; notes 1 and 2					
at $V_{15-18} = 0$ to 2.5 V		t_{17-18}	490	550	610	ns
at $V_{15-18} = 3.5$ to 5.5 V		t_{17-18}	580	640	700	ns
at $V_{15-18} = 6.5$ to 8.5 V		t_{17-18}	670	730	790	ns
at $V_{15-18} = 9.5$ to 12 V		t_{17-18}	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

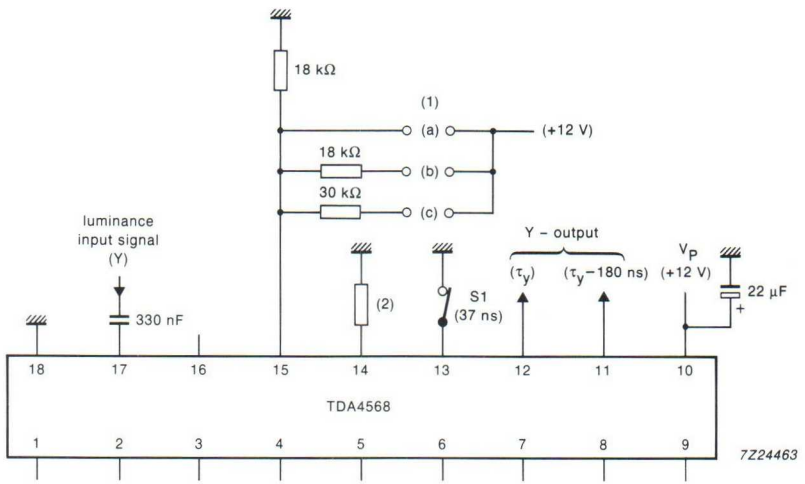
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 4					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
2. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18}$ = 1.2 kΩ.
3. Frequency response measured with $V_{15\text{-}18}$ = 9.5 V and switch S1 open.
4. Output current measured with emitter follower with constant current source of 0.6 mA.

APPLICATION INFORMATION



DEVELOPMENT DATA

(1) Switching sequence for delay times shown in Table 1.
(2) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4568.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4568A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

NTSC DECODER

GENERAL DESCRIPTION

The TDA4570 is an integrated 3,58 MHz or 4,43 MHz NTSC decoder. It is pin sequence compatible with multi-standard decoder TDA4555 and pin compatible with the PAL decoder TDA4510.

Features:

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with sampled rectification during burst-key signal
- Blanking circuit for the colour burst signal

Oscillator and control voltage part

- Voltage controlled reference oscillator for double subcarrier frequency
- Divider stages which provide the correct 90° phase between −(R-Y) and −(B-Y) reference signals for the demodulators
- Phase comparator which controls the frequency and phase of the reference oscillator and compares the (R-Y) reference with the burst pulse
- HUE control stage provides phase shifting via the combined service and hue control input (pin 11)
- Identification demodulator provides a positive-going identification signal at pin 14 for NTSC signals and acts as the automatic colour killer
- Two-function service switch:

  position one ($V_{14\text{-}3} < 1$ V): switches the colour-ON and switches the hue control and burst for the PLL oscillator-OFF, allowing the adjustment of the reference oscillator

  position two ($V_{14\text{-}3} > 5$ V): switches the colour-ON, the hue control OFF and allows the output signal to be observed
- Sandcastle pulse detector for burst-gate, horizontal and horizontal/vertical blanking pulse detection. The vertical part of the sandcastle pulse is used for the internal colour-ON and colour-OFF delay
- Pulse processing part for the prevention of premature switching ON of the colour. The colour-ON delay, two or three field periods after identification of the NTSC signal, is achieved by a counter. When there is no identification voltage present the colour is switched OFF immediately or, at the most, one field period later.

Demodulator part

- Two synchronous demodulators for the (R-Y) and (B-Y) signals, which incorporate stages for the blanking during line and field flyback
- Internal filtering of the residual carrier in the demodulated colour difference signals
- Colour switching stages controlled by the pulse processing part in front of the output stages
- The output stages for (R-Y) and (B-Y) signals are low resistance n-p-n emitter followers
- Separate colour switching output

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

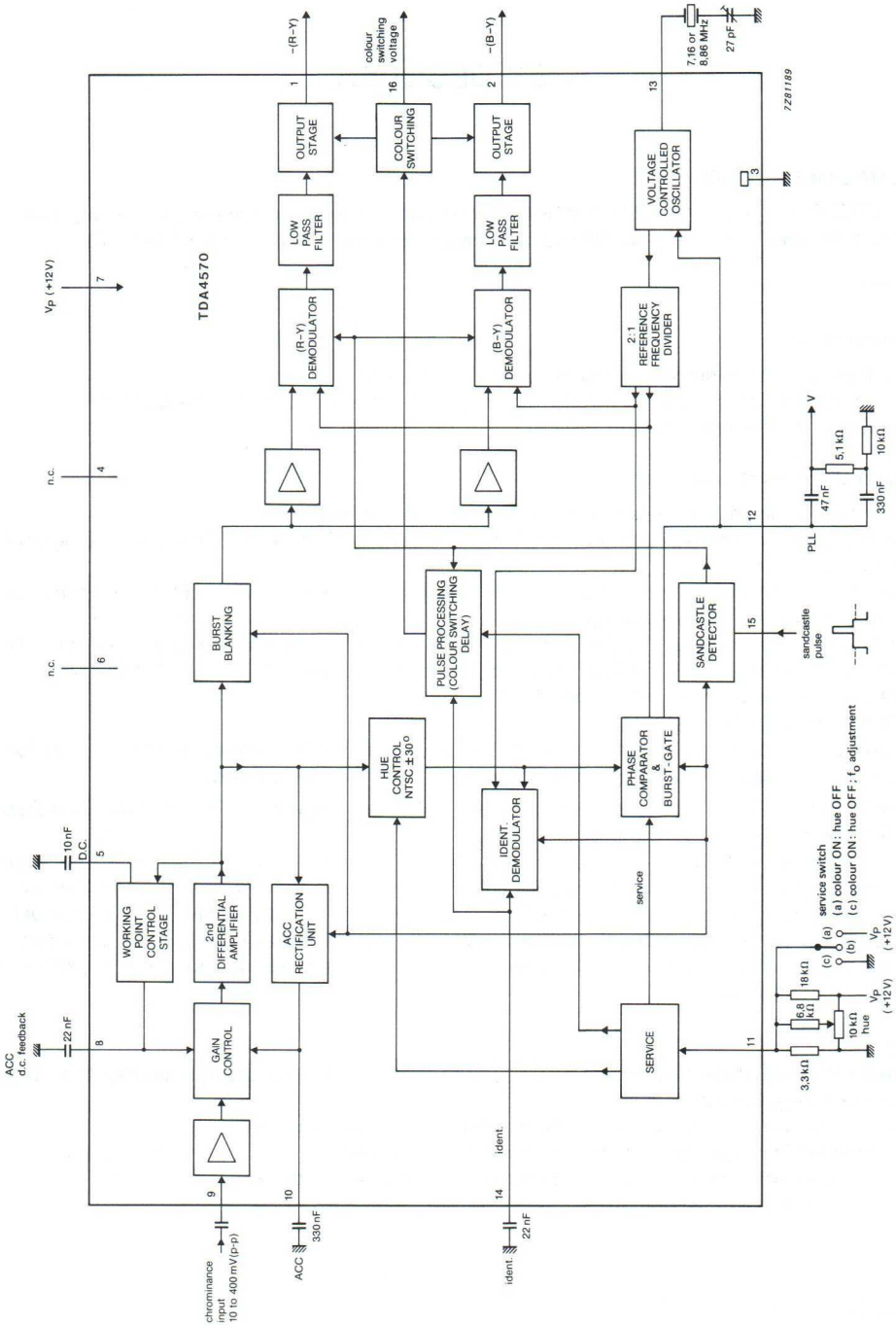


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents at:				
pins 1 and 2	$-I_{1,2}$	max.	5	mA
pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to + 150		°C
Operating ambient temperature range	T_{amb}	0 to + 70		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	max.	80	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	$I_P = I_7$	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9-3(p-p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9-3(p-p)}$	–	100	–	mV
Input impedance	$\lvert Z_{9-3}\rvert$	–	3,3	–	kΩ
Input capacitance	C_{9-3}	–	4,0	–	pF
Oscillator and control voltage part					
Oscillator frequency for subcarrier frequency					
3,58 MHz	f_{osc}	–	7,16	–	MHz
4,43 MHz	f_{osc}	–	8,86	–	MHz
Input resistance	R_{13-3}	–	350	–	Ω
Catching range (depending on RC network between pins 12 and 3)	Δf	± 300	–	–	Hz
Control voltage					
without burst signal	V_{14-3}	–	6,0	–	V
colour switching threshold	V_{14-3}	–	6,6	–	V
hysteresis of colour switching	V_{14-3}	–	150	–	mV
Colour-ON delay	$t_{d\ on}$	–	–	3	*
Colour-OFF delay	$t_{d\ off}$	–	–	1	*

* Expressed as field periods.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Colour switching output (open n-p-n emitter)					
output current	$-I_{16}$	–	–	5,0	mA
colour-ON voltage	V_{16-3}	–	6,0	–	V
colour-OFF voltage	V_{16-3}	–	0	–	V
HUE control and service switches					
Phase shift of reference carrier relative to the input signal $V_{11-3} = 3$ V	ϕ	–5	0	+ 5	deg
Phase shift of reference carrier relative to phase at $V_{11-3} = 3$ V					
$V_{11-3} = 2$ V	$-\phi$	30	–	–	deg
$V_{11-3} = 4$ V	$+\phi$	30	–	–	deg
Internal source (open pin)		–	3	–	V
First service position (PLL is inactive for oscillator adjustment, colour ON, HUE OFF)	V_{11-3}	0	–	1	V
Second service position (colour ON, HUE OFF)	V_{11-3}	5	–	V_P	V
Demodulator part					
Colour difference signals output voltage (peak-to-peak value)					
–(R-Y) signal	$V_{1-3(p-p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2-3(p-p)}$	1,06	1,33	1,67	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{1-3}}{V_{2-3}}$	0,71	0,79	0,87	
D.C. voltage at colour difference outputs	$V_{1,\,2-3}$	–	7,7	–	V
Residual carrier at colour difference outputs (peak-to-peak value)					
(1 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	20	mV
(2 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	30	mV

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (note 1)					
Input voltage level (pin 15)					
to separate vertical and horizontal blanking pulses	V_{15-3}	1,3	1,6	1,9	V
required pulse amplitude	V_{15-3}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{15-3}	3,3	3,6	3,9	V
required pulse amplitude	V_{15-3}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{15-3}	6,6	7,1	7,6	V
required pulse amplitude	V_{15-3}	7,7	–	–	V
Input voltage during horizontal scanning	V_{15-3}	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

Note

1. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION

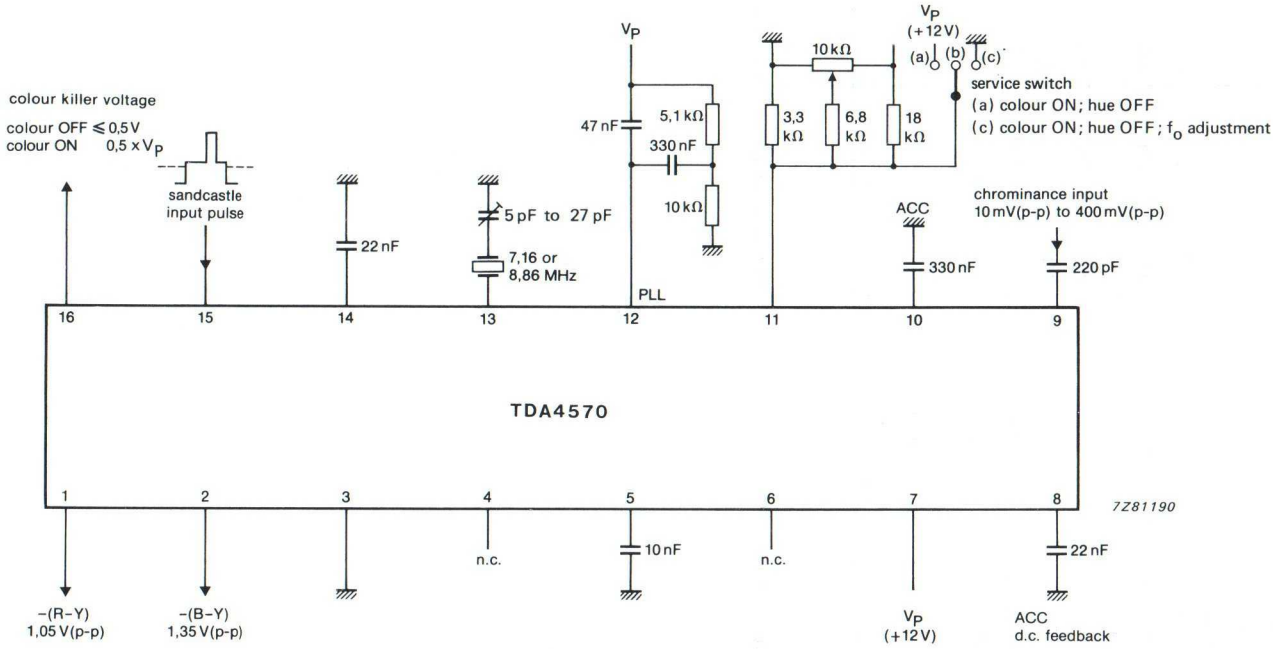


Fig. 2 Application diagram.

Crystal frequency 7, 16 or 8,86 MHz; resonance resistance 60 Ω; load capacitance 20 pF; dynamic capacitance 22 fF and static capacitance 5,5 pF.

VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

GENERAL DESCRIPTION

The TDA4580 is a monolithic integrated circuit which performs video control functions in television receivers with a colour difference interface. For example it operates in conjunction the multistandard colour decoder TDA4555. The required input signals are: luminance and negative colour difference −(R-Y) and −(B-Y), and a 3-level sandcastle pulse for control purposes. Analogue RGB signals can be inserted from two sources. One with full performance adjustment possibilities. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference, luminance and RGB input signals with black level clamping
- Two sets of analogue RGB inputs via fast switch 1 and fast switch 2
- First RGB inputs and fast switch 1 in accordance with peritelevision connector specification
- Saturation, contrast and brightness control acting on first RGB inputs
- Brightness control acting on second RGB inputs
- Equal black levels for television and inserted signals
- Clamping, horizontal and vertical blanking, and timing of automatic cut-off, controlled by a 3-level sandcastle pulse
- Automatic cut-off control with compensation for leakage current of the picture tube
- Measuring pulses of cut-off control start immediately after end of vertical part of sandcastle pulse
- Three selectable blanking intervals for PAL, SECAM and NTSC/PAL-M
- Two switch-on delays for run-in without discolouration
- Adjustable peak drive limiter
- Average beam current limiter
- G-Y and RGB matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- Bandwidth 10 MHz (typ.)
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

Supply voltage (pin 6)	$V_P = V_{6-24}$	typ.	12 V
Supply current (pin 6)	$I_P = I_6$	typ.	110 mA
Luminance input (pin 15)			
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (black to white values)	$V_{14, 13, 12-24}$	typ.	0,7 V
Inserted RGB signals for teletext use (black to white values)	$V_{23, 22, 21-24}$	typ.	1 V
Three-level sandcastle pulse (required input voltage)	V_{10-24}	typ.	2,5/4,5/8,0 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

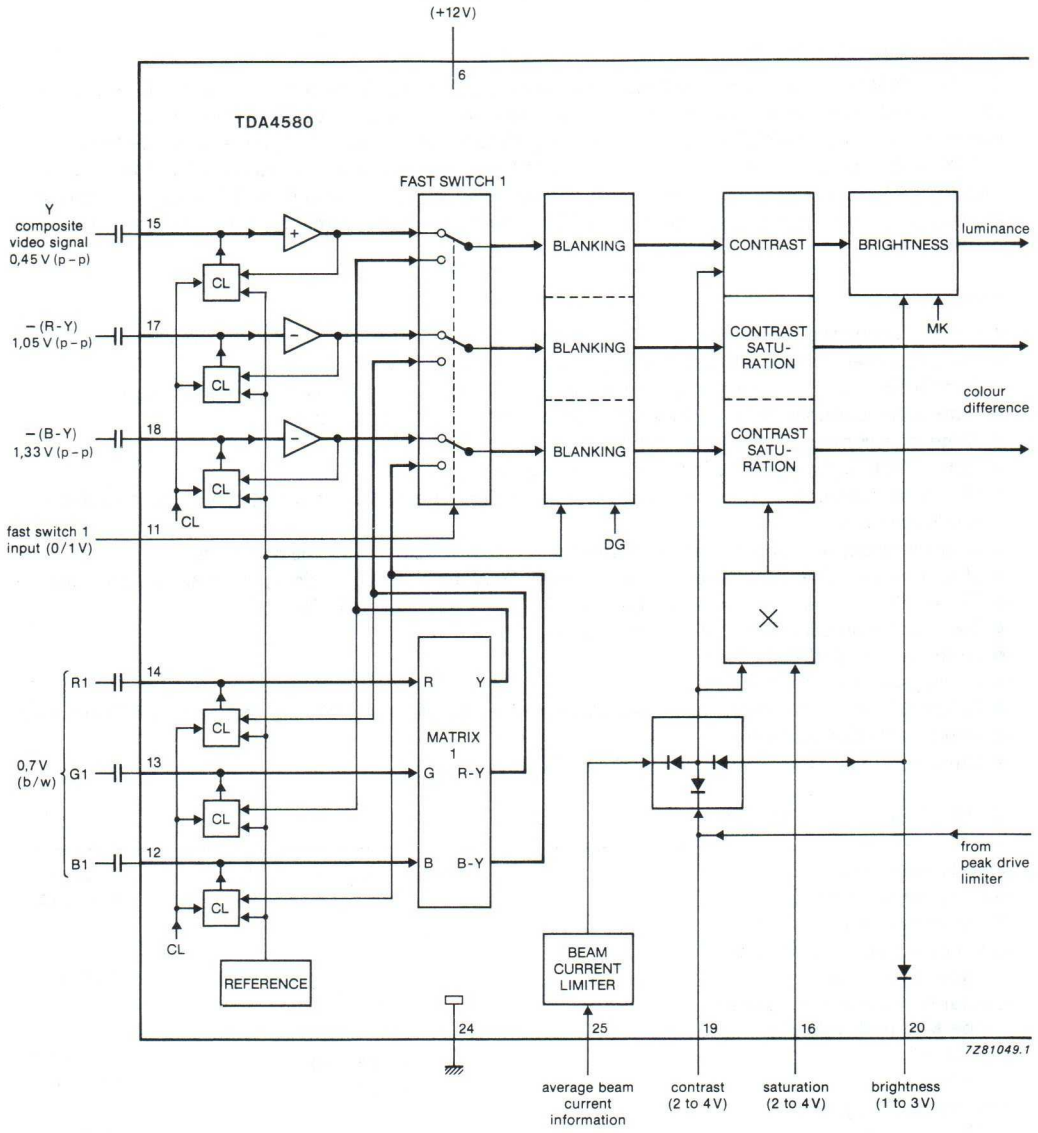


Fig. 1a Part of block diagram; continued in Fig. 1b.

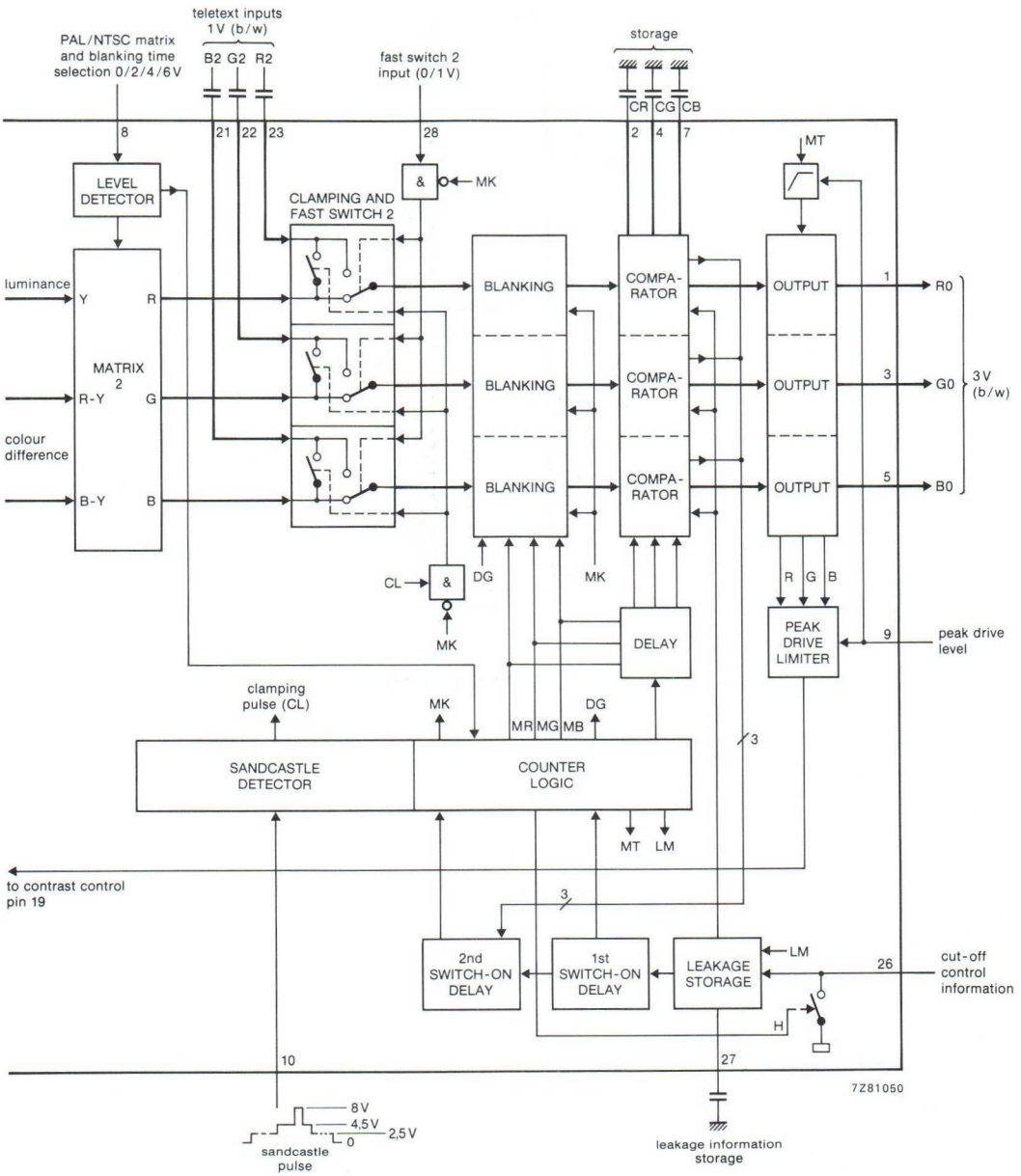


Fig. 1b Part of block diagram; continued from Fig. 1a.

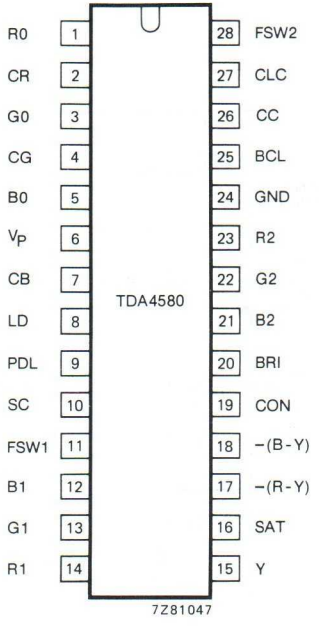


Fig. 2 Pinning diagram.

PINNING

pin no.	mnemonic	description
1	R0	Red output
2	CR	Red storage capacitor for cut-off control
3	G0	Green output
4	CG	Green storage capacitor for cut-off control
5	B0	Blue output
6	V_P	Positive supply voltage (+ 12 V)
7	CB	Blue storage capacitor for cut-off control
8	LD	PAL/NTSC matrix and blanking time level detector input
9	PDL	Peak drive limiting input
10	SC	Sandcastle pulse input
11	FSW1	Fast switch 1 for Y, CD and RGB inputs
12	B1	Blue input (external signal)
13	G1	Green input (external signal)
14	R1	Red input (external signal)
15	Y	Luminance input
16	SAT	Saturation control input
17	−(R-Y)	Colour difference input −(R-Y)
18	−(B-Y)	Colour difference input −(B-Y)
19	CON	Contrast control input
20	BRI	Brightness control input
21	B2	Teletext blue input
22	G2	Teletext green input
23	R2	Teletext red input
24	GND	Ground
25	BCL	Average beam current limiting input
26	CC	Automatic cut-off control input
27	CLC	Storage capacitor for leakage current
28	FSW2	Fast switch 2 for teletext inputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 6)	$V_P = V_{6-24}$	0 to 13,2	V
Voltage range at pins 2, 4, 7, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 25, 27 to pin 24 (ground)	V_{n-24}	0 to V_P	V
Voltages ranges			
at pins 8, 11, 28	$V_{8, 11, 28-24}$	−0,5 to V_P	V
at pin 10	V_{10-24}	0 to V_P + 0,7	V
at pin 26	V_{26-24}	−0,7 to V_P + 0,7	V
Currents			
at pins 1, 3, 5 (average)	$-I_{1, 3, 5(AV)}$	max. 3	mA
at pins 1, 3, 5 (peak)	$-I_{1, 3, 5(M)}$	max. 10	mA
at pin 19 (average)	$I_{19(AV)}$	max. 5	mA
at pin 26	I_{26}	max. 1	mA
Total power dissipation	P_{tot}	max. 2	W
Storage temperature range	T_{stg}	−20 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	= 37	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in a circuit similar to Fig. 4 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to pin 24 (ground) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage range	$V_P = V_{6-24}$	10,8	–	13,2	V
Supply current	$I_P = I_6$	–	110	–	mA
Colour difference inputs (pins 17 and 18)					
–(R-Y) input signal at pin 17 (notes 1 and 2) (peak-to-peak value)	$V_{17-24(p-p)}$	–	1,05	–	V
–(B-Y) input signal at pin 18 (notes 1 and 2) (peak-to-peak value)	$V_{18-24(p-p)}$	–	1,33	–	V
Input current during scanning	$\|I_{17, 18}\|$	–	–	0,3	μA
Input resistance	$R_{17, 18}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{17, 18-24}$	–	7,5	–	V
Luminance input (pin 15; note 2)					
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	–	0,45	–	V
Input current during scanning	$\|I_{15}\|$	–	–	0,3	μA
Input resistance	R_{15}	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	V_{15-24}	–	7,4	–	V
Signal switch 1 input (pin 11)					
Input voltage level for insertion of Y and CD signals	V_{11-24}	–	–	0,4	V
RGB1 signals	V_{11-24}	0,9	–	3,0	V
Internal resistor to ground	R_{11}	–	10	–	kΩ
RGB1 inputs (R1 pin 14, G1 pin 13, B1 pin 12; note 2) (signals controlled by saturation, contrast and brightness)					
Input signal (black to white value)	$V_{12, 13, 14-24}$	–	0,7	–	V
Input current during scanning	$\|I_{12, 13, 14}\|$	–	–	0,3	μA
Input resistance	$R_{12, 13, 14}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{12, 13, 14-24}$	–	8,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB/Y, (R-Y), (B-Y) – Matrix					
Matrixed according to the equations $V_{(R-Y)} = 0{,}7\ V_R - 0{,}59\ V_G - 0{,}11\ V_B$ $V_{(B-Y)} = -0{,}3\ V_R - 0{,}59\ V_G + 0{,}89\ V_B$ $V_{(Y)} = 0{,}3\ V_R + 0{,}59\ V_G + 0{,}11\ V_B$					
Contrast control input (pin 19; note 3) (contrast control acts on Y and CD signals or RGB1 signals respectively)					
Maximum contrast	V_{19-24}	–	4	–	V
Nominal contrast (6 dB below max.)	V_{19-24}	–	3	–	V
Attenuation of contrast at V_{19-24} = 2 V (related to max.)		–	22	–	dB
Input current at V_{19-24} = 2 to 4 V	$-I_{19}$	–	–	3	μA
Peak drive limiting input (pin 9; note 4)					
Internal d.c. bias voltage	V_{9-24}	–	9	–	V
Input resistance at $V_{9-24} > 9$ V	R_9	–	10	–	kΩ
Control current into contrast input (pin 19) during peak drive $V_{1,\ 2\ or\ 3-24} > V_{9-24}$	I_{19}	–	20	–	mA
Average beam current limiting input (pin 25; note 5)					
Start of contrast reduction at maximum contrast setting	V_{25-24}	–	8,5	–	V
Input range for full contrast reduction	ΔV_{25-24}	–	1,0	–	V
Input resistance at $V_{25-24} < 6$ V	R_{25}	–	2,2	–	kΩ
Saturation control input (pin 16) (saturation control acts on CD signals or RGB1 signals respectively)					
Maximum saturation	V_{16-24}	–	4	–	V
Nominal saturation (6 dB below max.)	V_{16-24}	–	3	–	V
Attenuation of saturation at V_{16-24} = 1,8 V (related to max. at 100 kHz)		50	–	–	dB
Input current at V_{16-24} = 1,8 to 4 V	I_{16}	–	–	10	μA

parameter	symbol	min.	typ.	max.	unit
Brightness control input (pin 20; note 6 and 7)					
Control voltage range	V_{20-24}	1	–	3	V
Input current at V_{20-24} = 1 to 3 V	$-I_{20}$	–	–	10	μA
Control voltage for nominal brightness	V_{20-24}	–	2,2	–	V
Change of black level in the control range related to the nominal output signal (black/white) for ΔV_{20-24} = 1 V		–	33	–	%
Signal switched off and black level equal to cut-off measuring level at	V_{20-24}	11,5	–	–	V
Y, (R-Y), (B-Y)/RGB – Matrix (note 8)					
PAL matrix (V_{8-24} = < 4,5 V)					
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$					
NTSC matrix (V_{8-24} = > 5,5 V)					
(Adaption for NTSC-FCC primaries, nominal hue control set on –5°)					
Matrixed according to the equation $V_{(G-Y)}^* = -0{,}43\ V_{(R-Y)} - 0{,}11\ V_{(B-Y)}$					
$V_{(R-Y)}^* = 1{,}57\ V_{(R-Y)} - 0{,}41\ V_{(B-Y)}$					
$V_{(B-Y)}^* = V_{(B-Y)}$					
RGB2 inputs (Teletext) (R2 pin 23, G2 pin 22, B2 pin 21; note 2)					
(RGB signals controlled by brightness control)					
Input signal for 100% output signals (black to white value)	$V_{21, 22, 23-24}$	–	1	–	V
Input current during scanning	$I_{21, 22, 23}$	–	–	0,3	μA
Input resistance	$R_{21, 22, 23}$	5	–	–	MΩ
Signal switch 2 input (pin 28)					
Input voltage level for insertion of Y, CD signals or RGB1 signals respectively RGB signals from matrix (note 9)	V_{28-24}	–	–	0,4	V
RGB2 signals (note 9)	V_{28-24}	0,9	–	3,0	V
Internal resistor to ground	R_{28-24}	–	10	–	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Automatic cut-off control input (pin 26; note 10) (leakage current measuring time and insertion of RGB cut-off measuring lines see Fig. 5; types of ultra-black level see Fig. 3)					
Allowed maximum external D.C. bias voltage	$V_{26\text{-}24}$	5,5	–	–	V
Voltage difference between cut-off current measurement and leakage current measurement	$\Delta V_{26\text{-}24}$	–	0,5	–	V
Warm-up test pulse	$V_{1,\ 3,\ 5\text{-}24}$	–	$V_{9\text{-}24}$*	–	V
Threshold for warm-up detector	$V_{26\text{-}24}$	–	8	–	V
Storage input for leakage current (pin 27)					
Internal resistance during leakage current measuring time (current limiting at I_{27} = 0,2 mA)	R_{27}	–	400	–	Ω
Input current except during cut-off control cycle	$\lvert I_{27}\rvert$	–	–	0,5	μA
Storage inputs for automatic cut-off control (pins 2, 4, 7)					
Charge and discharge currents	$\lvert I_{2,\ 4,\ 7}\rvert$	–	0,3	–	mA
Input currents of storage inputs out of control time	$\lvert I_{2,\ 4,\ 7}\rvert$	–	–	0,1	μA
Switch input for PAL/NTSC matrix and vertical blanking time (pin 8; note 11)					
Switching voltage input for					
PAL matrix and vertical blanking period of					
25 lines	$V_{8\text{-}24}$	–	0	0,5	V
22 lines	$V_{8\text{-}24}$	1,5	2	2,5	V
18 lines	$V_{8\text{-}24}$	3,5	4	4,5	V
NTSC matrix and vertical blanking period of					
18 lines	$V_{8\text{-}24}$	5,5	6	12	V
Input current	I_8	–	–	50	μA

* Maximum 8 V.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10; note 12)					
The following amplitudes are required for separating the various pulses:					
horizontal and vertical blanking pulses	V_{10-24}	2,0	2,5	3,0	V
horizontal pulses for counter logic	V_{10-24}	4,0	4,5	5,0	V
clamping pulses	V_{10-24}	7,5	–	–	V
delay of leading edge of clamping pulse	t_d	–	1	–	µs
Input current at V_{10-24} = 0 V	$-I_{10}$	–	–	100	µA
Outputs for positive RGB signals (R0 pin 1, G0 pin 3, B0 pin 5; note 13)					
Nominal signal amplitude (black/white)	$V_{1, 3, 5-24}$	–	3	–	V
Spreads between channels		–	–	10	%
Maximum signal amplitude (black/white)	$V_{1, 3, 5-24}$	4	–	–	V
Internal current source	$I_{1, 3, 5}$	–	3	–	mA
Output resistance	$R_{1, 3, 5}$	–	160	220	Ω
Minimum output voltage	$V_{1, 3, 5-24}$	–	1	–	V
Maximum output voltage	$V_{1, 3, 5-24}$	–	10	–	V
Horizontal and vertical blanking to ultra-black level 2 related to nominal signal black level in percentage of nominal signal amplitude		45	55	–	%
Vertical blanking to ultra-black level 1 related to cut-off measuring level in percentage of nominal signal amplitude		25	35	–	%
Recommendation:					
Range for cut-off measuring level 1,5 to 5,0 V; nominal value at 3 V (note 14)					
Gain data (note 15)					
Frequency response of Y path (0 to 8 MHz) pins 1, 3 and 5 to pin 15	d	–	–	3	dB
Frequency response of CD path (0 to 8 MHz) pin 1 to pin 17 = pin 5 to pin 18	d	–	–	3	dB
Frequency response of RGB1 path (0 to 8 MHz) pin 1 to pin 14 = pin 3 to pin 13 = pin 5 to pin 12	d	–	–	3	dB
Frequency response of RGB2 path (0 to 10 MHz) pin 1 to pin 23 = pin 3 to pin 22 = pin 5 to pin 21	d	–	–	3	dB

Notes to the characteristics

1. The value of the colour difference input signals, $-(B\text{-}Y)$ and $-(R\text{-}Y)$, is given for saturated colour bar with 75% of maximum amplitude.
2. Capacitive coupled to a low ohmic source; recommended value 600 Ω (max.).
3. At pin 19 for $V_{19\text{-}24} \leqslant 2{,}0$ V, no further decrease of contrast is possible.
4. The peak drive limiting of output signals is achieved by contrast reduction. The limiting level of the output signals is equal to the voltage $V_{9\text{-}24}$, adjustable in the range 5 to 11 V. After exceeding the adjusted limiting level at peak drive limiter will not be active during the first line.
5. The average beam current limiting acts on contrast and at minimum contrast on brightness (the external contrast voltage at pin 19 is not affected).
6. At nominal brightness the black level at the output is 0,3 V ($\hat{=}$ −10% of nominal signal amplitude) below the measuring level.
7. The internal control voltage can never be more positive than 0,7 V above the internal contrast voltage.
8. Matrix equation

   $V_{(R\text{-}Y)}$, $V_{(B\text{-}Y)}$: output of NTSC decoder of PAL type demodulating axis and amplitudes

   $V_{(G\text{-}Y)}{}^*$, $V_{(R\text{-}Y)}{}^*$, $V_{(B\text{-}Y)}{}^*$: for NTSC modified CD signals; equivalent to demodulation with the following axes and amplification factors:—

$(B\text{-}Y)^*$ demodulator axis	0^o	
$(R\text{-}Y)^*$ demodulator axis	115^o	(PAL 90^o)
$(R\text{-}Y)^*$ amplification factor	1,97	(PAL 1,14)
$(B\text{-}Y)^*$ amplification factor	2,03	(PAL 2,03)

   $V_{(G\text{-}Y)}{}^* = -0{,}27\ V_{(R\text{-}Y)}{}^* - 0{,}22\ V_{(B\text{-}Y)}{}^*$.
9. During clamping time, in each channel the black level of the inserted signal is clamped on the black level of the internal signal behind the matrix (dependent on brightness control).
10. During warm-up time of the picture tube, the RGB outputs (pins 1, 3 and 5) are blanked to minimum output voltage. An inserted white pulse during the vertical flyback is used for beam current detection. If the beam current exceeds the threshold of the warm-up detector at pin 26, the cut-off current control starts operating, but the video signal is still blanked. After run-in of the cut-off current control loop, the video signal will be released.
    The first measuring pulse occurs in the first complete line after the end of the vertical part of the sandcastle pulse. The absolute minimum vertical part must contain 9 line-pulses. The cycle time of the counter is 63 lines. When the vertical pulse is longer than 61 lines, the IC is reset to the switch-on condition. In this event the video signal is blanked and the RGB-outputs are blanked to minimum output voltage as during warm-up time.
    During leakage current measurement, all three channels are blanked to ultra-black level 1. With the measuring level only in the controlled channel, the other two channels are blanked to ultra-black level 1.
    The brightness control shifts both the signal black level and the ultra-black level 2. The brightness control is disabled from line 4 to the end of the last measuring line (see Fig. 3).
    With the most adverse conditions (maximum brightness and minimum black level 2) the blanking level is located 30% of nominal signal amplitude below the cut-off measuring level.

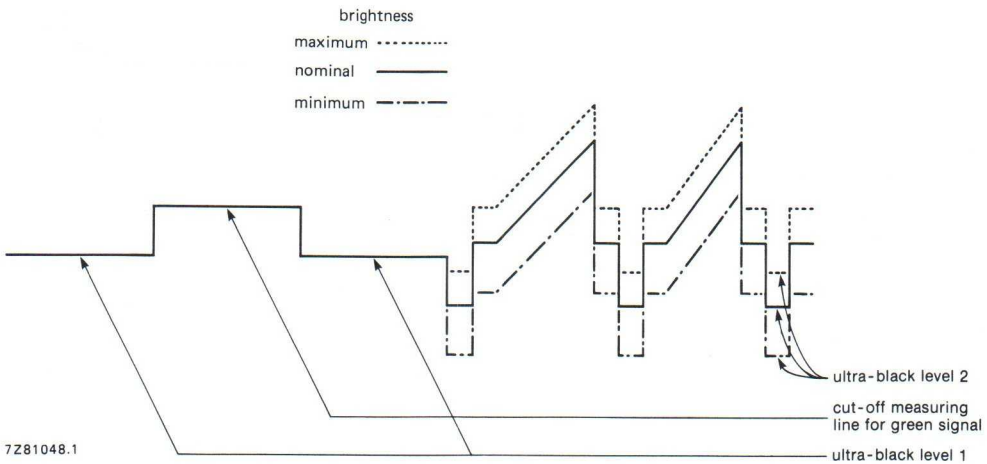
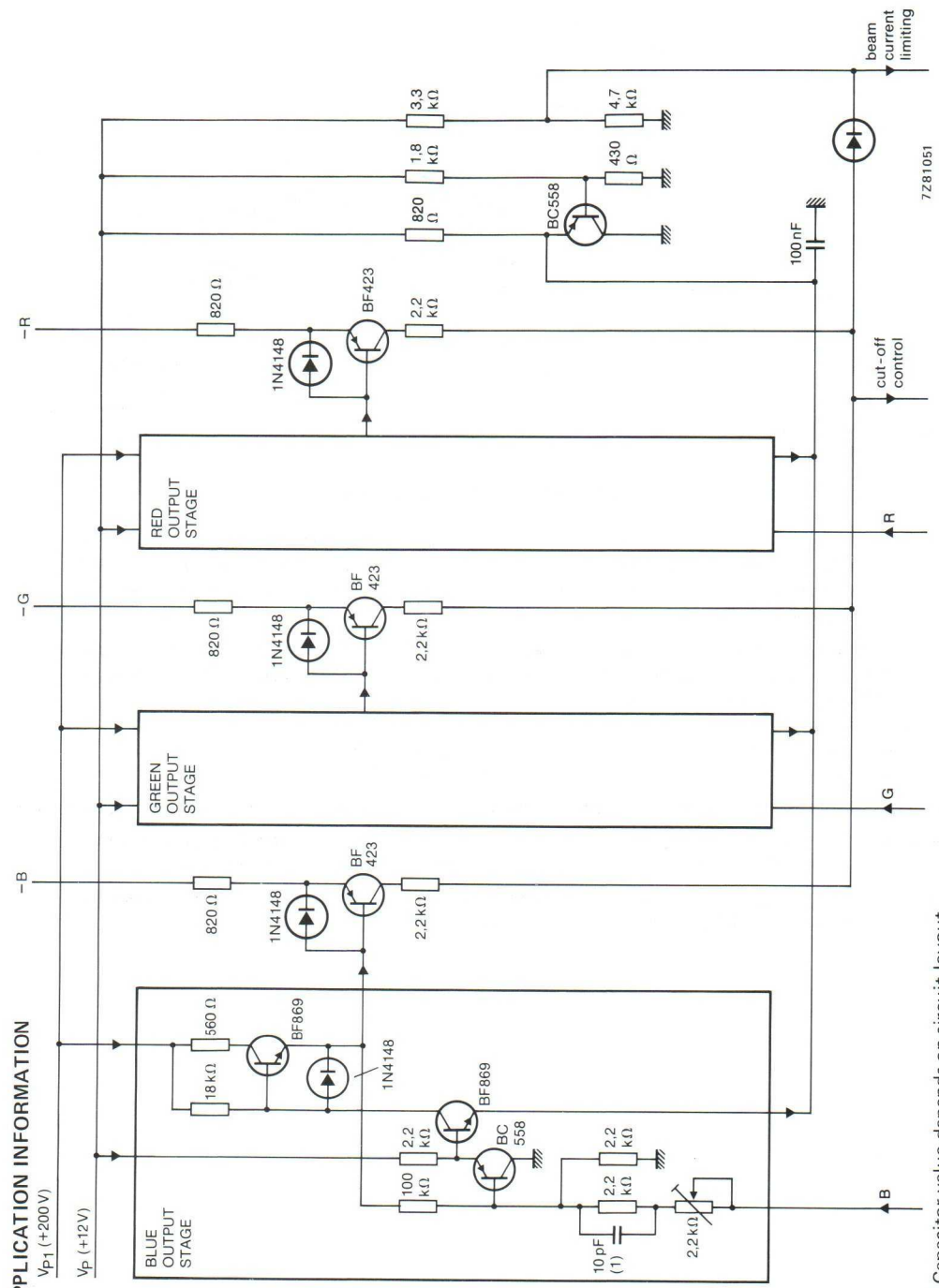


Fig. 3 Types of ultra-black levels.

11. The given blanking times are valid for the vertical part of the sandcastle pulse of 9 to 15 lines. If the vertical part is longer and the cut-off lines are outside the vertical blanking period of 18, 22 or 25 lines respectively, the blanking of the signal ends with the end of last of the three cut-off measuring pulses as shown in Fig. 5.
12. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) to separate the various pulses. The internal pulses are generated when the input pulse at pin 10 exceeds the thresholds. The thresholds are for:
    - Horizontal and vertical blanking $V_{10\text{-}24} = 1{,}5$ V
    - Horizontal pulse $V_{10\text{-}24} = 3{,}5$ V
    - Clamping pulse $V_{10\text{-}24} = 7{,}0$ V
13. The outputs at pins 1, 3 and 5 are emitter followers with current sources and emitter protection resistors.
14. The value of the cut-off control range for the positive RGB output signals is given for a nominal output signal. If the signal amplitude is reduced, the cut-off range can be increased.
15. The gain data is given for a nominal setting of the contrast and saturation controls, measured without load at the RGB outputs (pins 1, 3 and 5).



(1) Capacitor value depends on circuit layout.

Fig. 4a Part of typical application circuit diagram using the TDA4580; continued in Fig. 4b.

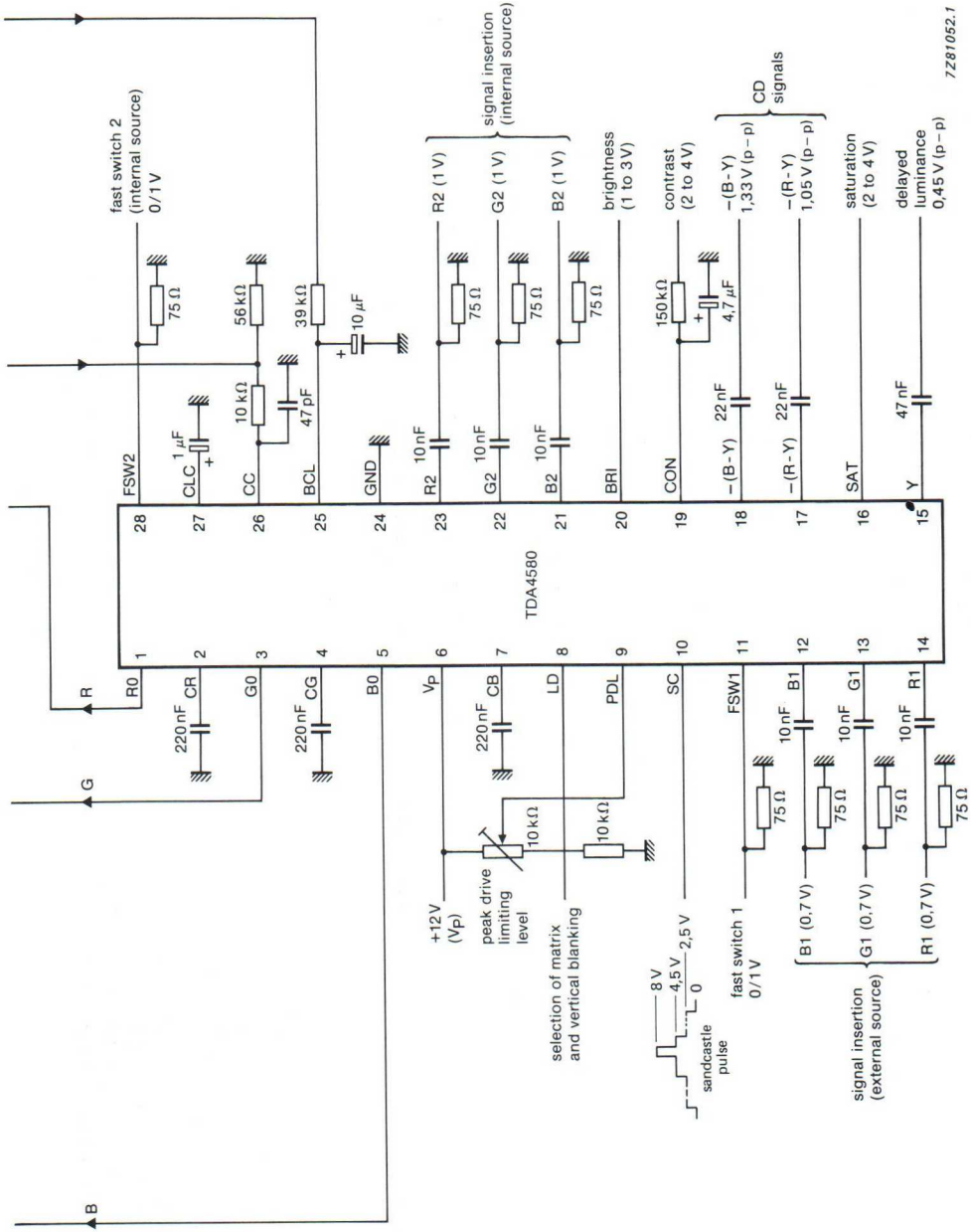
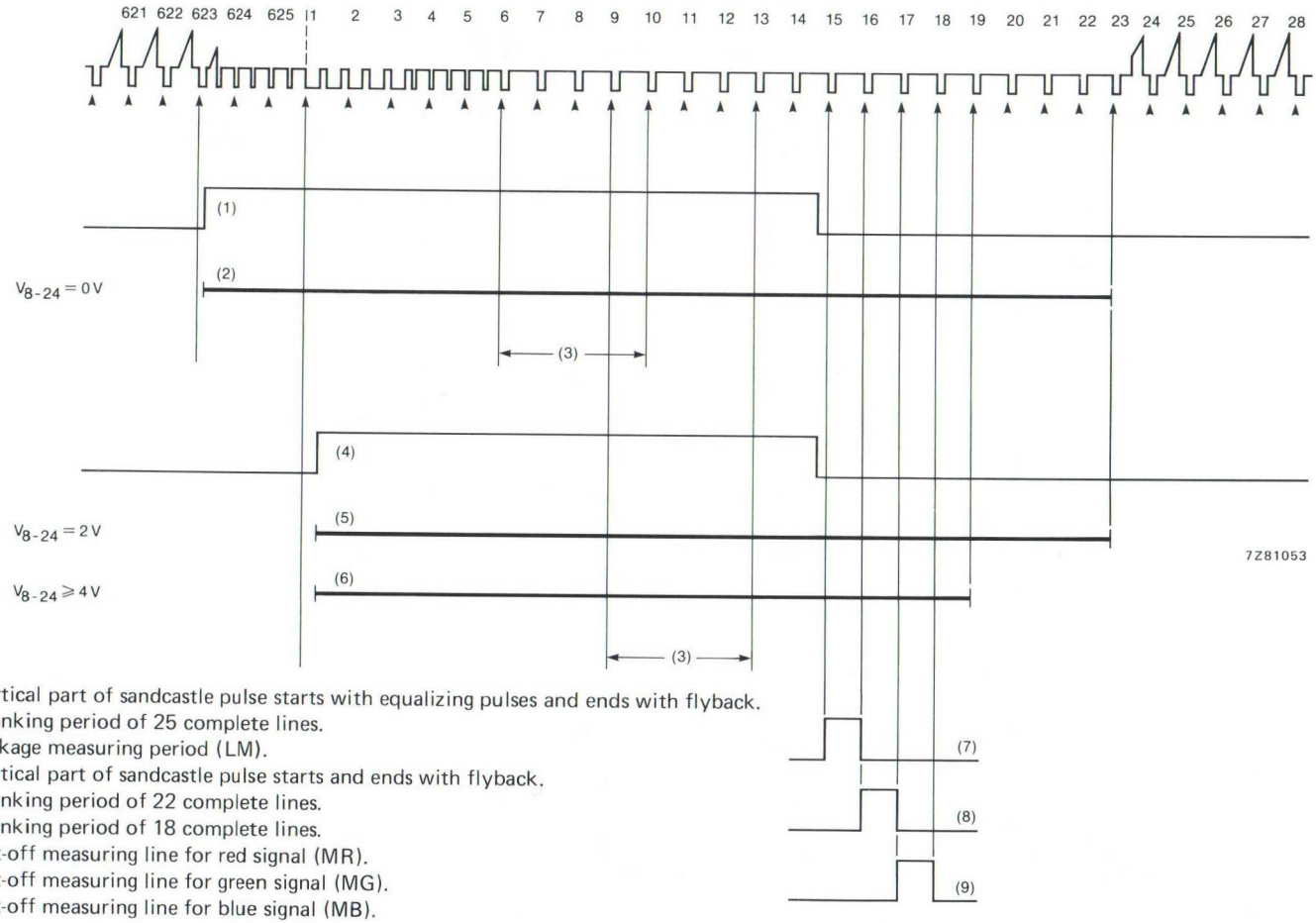


Fig. 4b Part of typical application circuit diagram using the TDA4580; continued from Fig. 4a.

APPLICATION INFORMATION (continued)



(1) vertical part of sandcastle pulse starts with equalizing pulses and ends with flyback.
(2) blanking period of 25 complete lines.
(3) leakage measuring period (LM).
(4) vertical part of sandcastle pulse starts and ends with flyback.
(5) blanking period of 22 complete lines.
(6) blanking period of 18 complete lines.
(7) cut-off measuring line for red signal (MR).
(8) cut-off measuring line for green signal (MG).
(9) cut-off measuring line for blue signal (MB).

Fig. 5 Blanking and measuring lines.

SECAM colour decoder with negative colour difference output signals

TDA4632

FEATURES

- Gain controlled chrominance amplifier
- Internal colour-difference signal output filters
- SECAM demodulation
  - Limiter-amplifier
  - Quadrature-demodulator with a single external reference tuned circuit
  - Alternate line blanking, H and V blanking
  - External de-emphasis
- Identification
  - Secure SECAM identification at 50 Hz only
  - External service switch

GENERAL DESCRIPTION

The TDA4632 is a bipolar integrated colour decoder for SECAM with negative colour difference output signals. The colour difference output signals are fed to the TDA4660/TDA4661, switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 13)	10.8	12	13.2	V
I_P	supply current (pin 13)	–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)	20	100	400	mV
$V_{o(p-p)}$	colour difference output voltage (pin 1) (peak-to-peak value)	0.83	1.05	1.32	V
	colour difference output voltage (pin 3) (peak-to-peak value)	1.06	1.33	1.67	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4632	28	DIL	plastic	SOT117

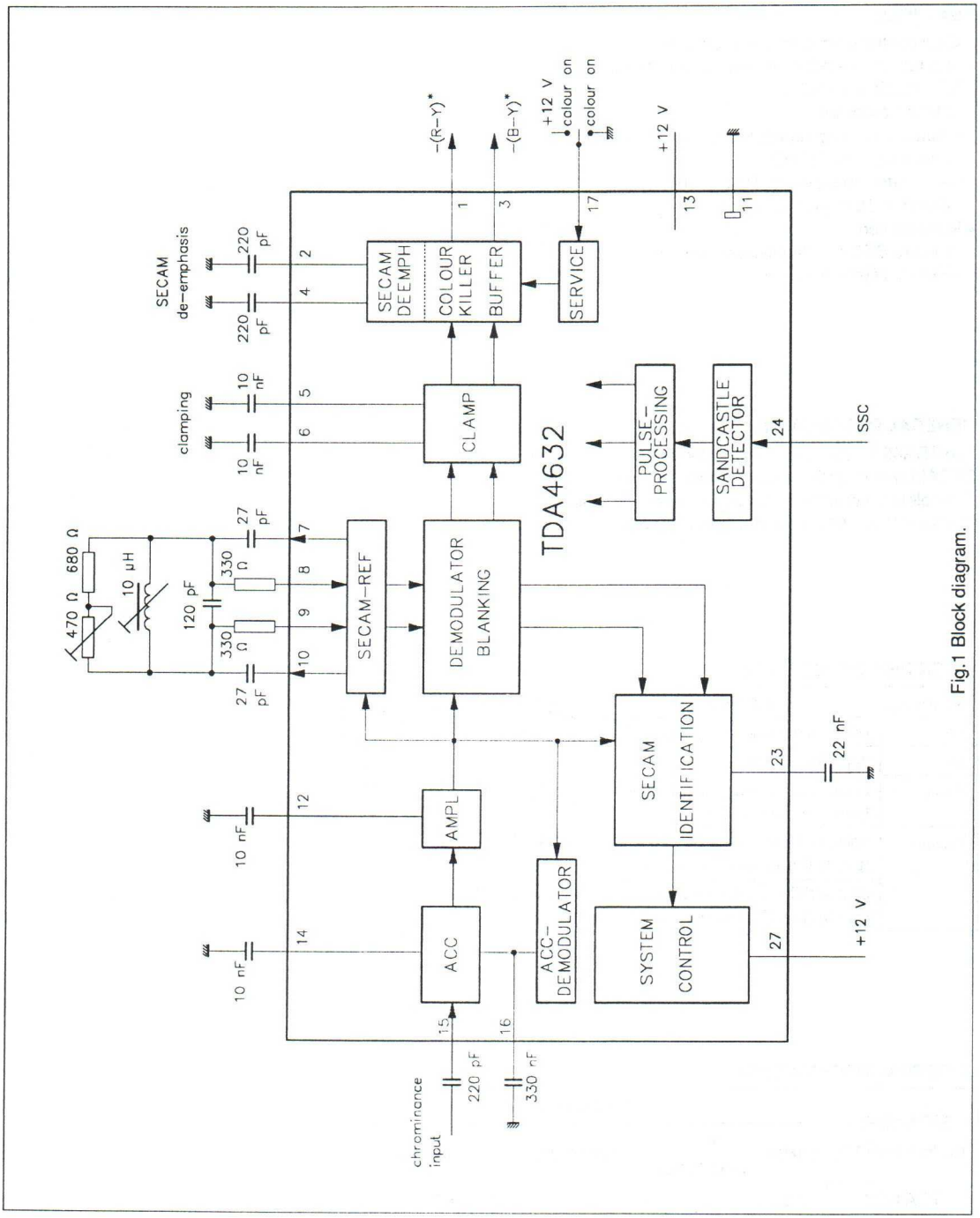


Fig.1 Block diagram.

SECAM colour decoder with negative colour difference output signals

TDA4632

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	–(R–Y) output
$-(R-Y)_{DE}$	2	(R–Y) de-emphasis
$-(B-Y)_O$	3	–(B–Y) output
$-(B-Y)_{DE}$	4	(B–Y) de-emphasis
$-(B-Y)_{CL}$	5	(B–Y) clamping
$-(R-Y)_{CL}$	6	(R–Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
	8	
	9	
	10	
GND	11	ground
C_D	12	DC for demodulators
V_P	13	supply voltage
C_{DC}	14	DC feedback
CHR_I	15	chrominance input
C_{ACC}	16	automatic colour control
SERVICE	17	service
n.c.	18	not connected
	19	
	20	
	21	
	22	
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
n.c.	25	not connected
	26	
SEC_O	27	SECAM identification
n.c.	28	not connected

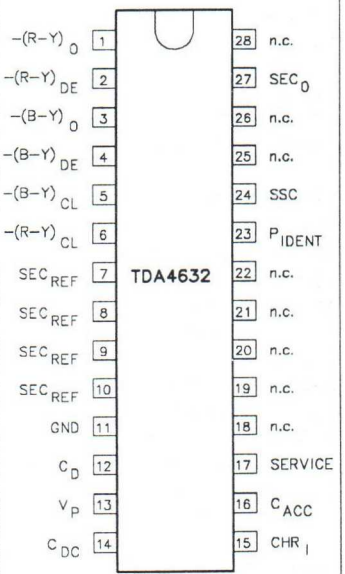


Fig.2 Pin configuration.

SECAM colour decoder with negative colour difference output signals

TDA4632

FUNCTIONAL DESCRIPTION

The IC (see block diagram Fig.1) contains all functions required for the identification and demodulation of SECAM signals. When a SECAM signal is fed into the input, the circuit is demodulating the signal and, after having identified the signal, it switches on the colour. At the outputs the two colour difference signals –(R–Y) and –(B–Y) are available.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal has to be AC coupled (pin 15). The differential amplifier stage at the input is followed by the gain control stage and a differential amplifier with lateral pnp-transistors having the function of a level-shifter. The gain control stage consists of an ACC-rectifier circuit. The rectifier circuit is switched on during part of the burst-gate-pulse and it is disabled during the prolonged frame flyback.
The DC-potential of the symmetrical signal-connections to the demodulators is kept at the same level by means of a working point control stage.

Demodulators

The demodulation of the SECAM colour-signal needs a demodulator for frequency modulated signals.
The SECAM demodulator is a combined demodulator for –(B–Y) and –(R–Y) with artificial black level being inserted alternately every second line and during line- and field-flyback. The load resistors of the demodulator are connected to two differential amplifiers, one for –(B–Y) and one for –(R–Y). The not wanted signals occuring every second line ((R–Y) in the –(B–Y)-channel and (B-Y) in the –(R–Y)-channel), have to be blanked.

Clamp

Behind the demodulators the signals are being filtered and the black level is clamped to a constant DC-level during the burst-gate-pulse. For the SECAM signals this happens every second line, when the appropriate artificial black level is present.

De-emphasis and output-buffer

Behind the clamping stages is the de-emphasis for the SECAM signals and just in front of the stages are the colour-killer and blanking-stages. The blanking level is the same as the clamping level and the black level.

Identification

The identification part contains a separate identification-demodulator for SECAM.
The identification-demodulator is active during part of the burst clamping time. It uses the same signals as the SECAM-demodulator that is not active during field-flyback. The identification-demodulator is followed by a H/2-switch 'rectifying' the demodulated signal. The result is an identification signal (P_{IDENT}) that is positive for a SECAM signal. In the event of a field frequency of 60 Hz the signal cannot be identified as a SECAM signal, even if the P_{IDENT} is positive. If the H/2 signal is of the wrong polarity, the identification signal is negative and the H/2-flip flop is set to the correct phase.
If a signal has been identified, after a delay time the colour is switched on.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13)	–	13.2	V
V_I	voltage range at pins 1, 3, 17, 24 and 27	0	V_P	V
I_o	output current (pins 1 and 3)	–	−5	mA
$I_{i/o}$	input/output current (pin 25 to 28)	–	−5	μA
T_{amb}	operating ambient temperature range	0	+70	°C
T_{stg}	storage temperature range	−25	+150	°C
P_{tot}	total power dissipation	–	1.4	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	37 K/W

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15\,(p\text{-}p)}$ = 100 mV (with 75% colour bar signal); 4.3 µs burst-blanking pulse and vertical blanking superimposed on super sandcastle pulse; T_{amb} = +25 °C; measured in test circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 13)		10.8	12	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i\,(p\text{-}p)}$	input signal (pin 15) (peak-to-peak value)	see note 1	20	100	400	mV
R_i	input resistance (pin 15)		7	10	13	kΩ
C_i	input capacitance (pin 15)		–	4	5	pF
Demodulator part (SECAM) (see note 2)						
$V_{1\,(p\text{-}p)}$	colour difference –(R–Y) output signals (peak-to-peak value)	every second line blanked	0.83	1.05	1.32	V
$V_{3\,(p\text{-}p)}$	colour difference –(B–Y) output signals (peak-to-peak value)	every second line blanked	1.06	1.33	1.67	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripples outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3\,(p\text{-}p)}$	residual carrier at CD outputs	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV
$\Delta V_{1,3} / \Delta V_P$	shift of blanking level relative to demodulated f_o levels		–	–	3	mV/V
$\Delta V_1 / \Delta T$			–	0.16	–	mV/K
$\Delta V_3 / \Delta T$			–	–0.25	–	mV/K
Service switch						
V_{17}	internal bias voltage		–	3	–	V
	switching voltage for forced colour ON	colour ON	0	–	0.5	V
	switching voltage for forced colour ON	colour ON	5.5	–	V_P	V
R_{17}	input resistance		3.8	5.0	6.2	kΩ
Identification part						
t_d	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
Super sandcastle pulse detector (see note 3)						
V_{24}	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	voltage pulse amplitude		7.7	–	V_P	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	µA

Notes to the characteristics

1. With 20 mV, 3 dB decrease of the output signal is allowed. The level shift of demodulated f_0 relative to blanking level is less than 5 mV.
2. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R–Y) and (B–Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_0 voltage level is zero in the –(B–Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_0 voltage level is zero in the –(R–Y) output channel at pin 1. If necessary, the f_0 voltage level in the –(B–Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at pins 2 and 4 (220 pF each) are matched to the internal resistance of the de-emphasis network such that every alternate scanned line is blanked.
3. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

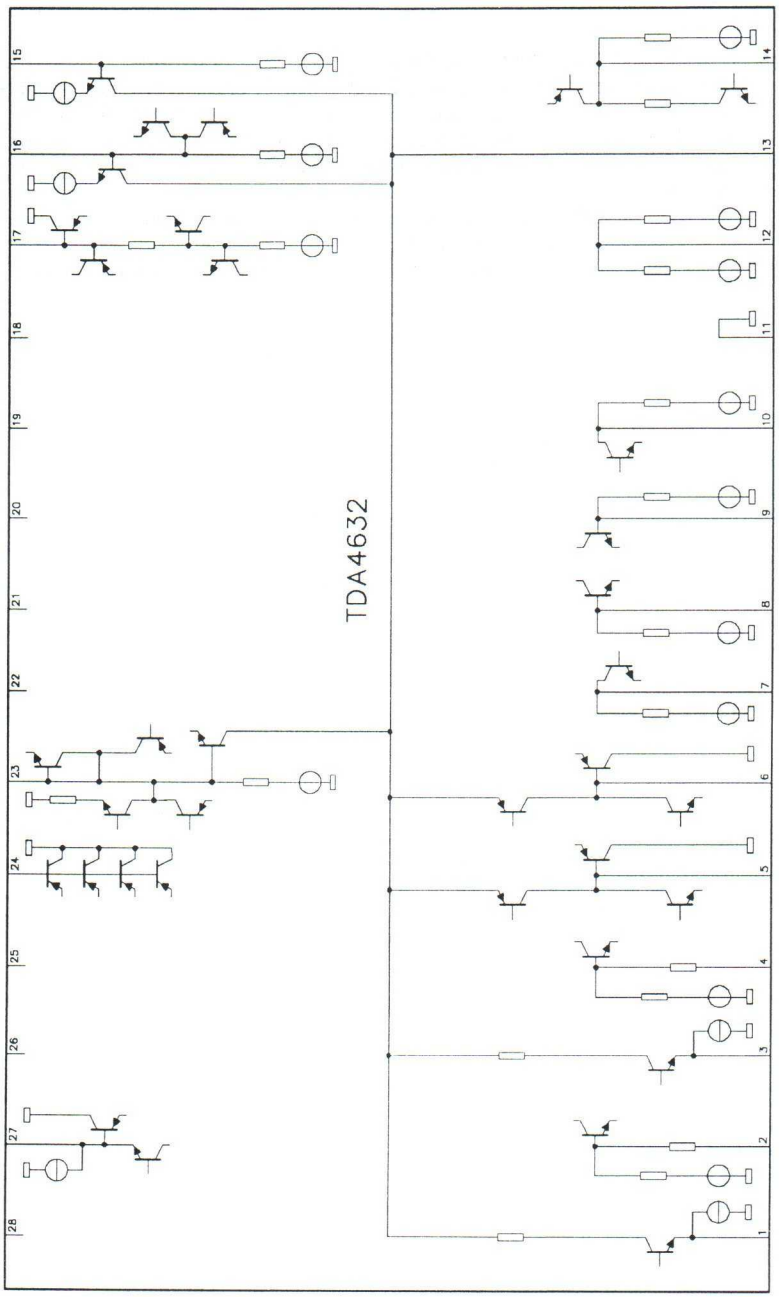


Fig.3 Internal circuits.

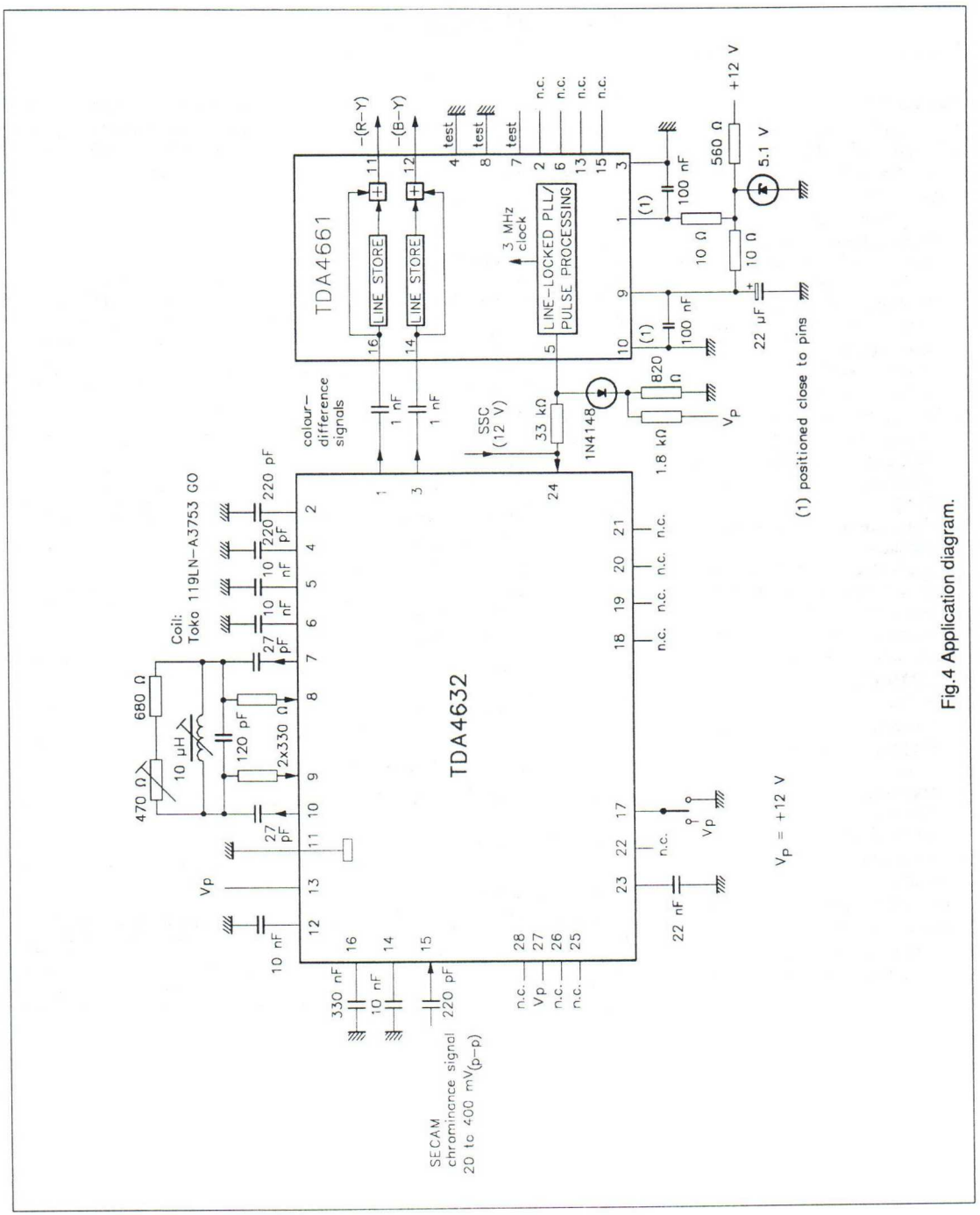


Fig.4 Application diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4650

Multistandard colour decoder, with negative colour difference output signals

FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter-amplifier
  - quadrature-demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour-difference signal output filters to remove the residual subcarrier

GENERAL DESCRIPTION

The TDA4650 is a monolitic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour-difference output signals are fed to the TDA4660/TDA4661, Switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 13)		10.8	12.0	13.2	V
I_P	supply current (pin 13)		–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)		20	100	400	mV
$V_{o(p-p)}$	colour-difference output voltage (pin 1) (peak-to-peak value)	PAL/NTSC	0.42	0.525	0.66	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	PAL/NTSC	0.53	0.665	0.84	V
	colour-difference output voltage (pin 1) (peak-to-peak value)	SECAM	0.83	1.05	1.32	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	SECAM	1.06	1.33	1.67	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4650	28	DIL	plastic	SOT117
TDA4650WP	28	PLCC	plastic	SOT261

Multistandard colour decoder, with negative colour difference output signals

TDA4650

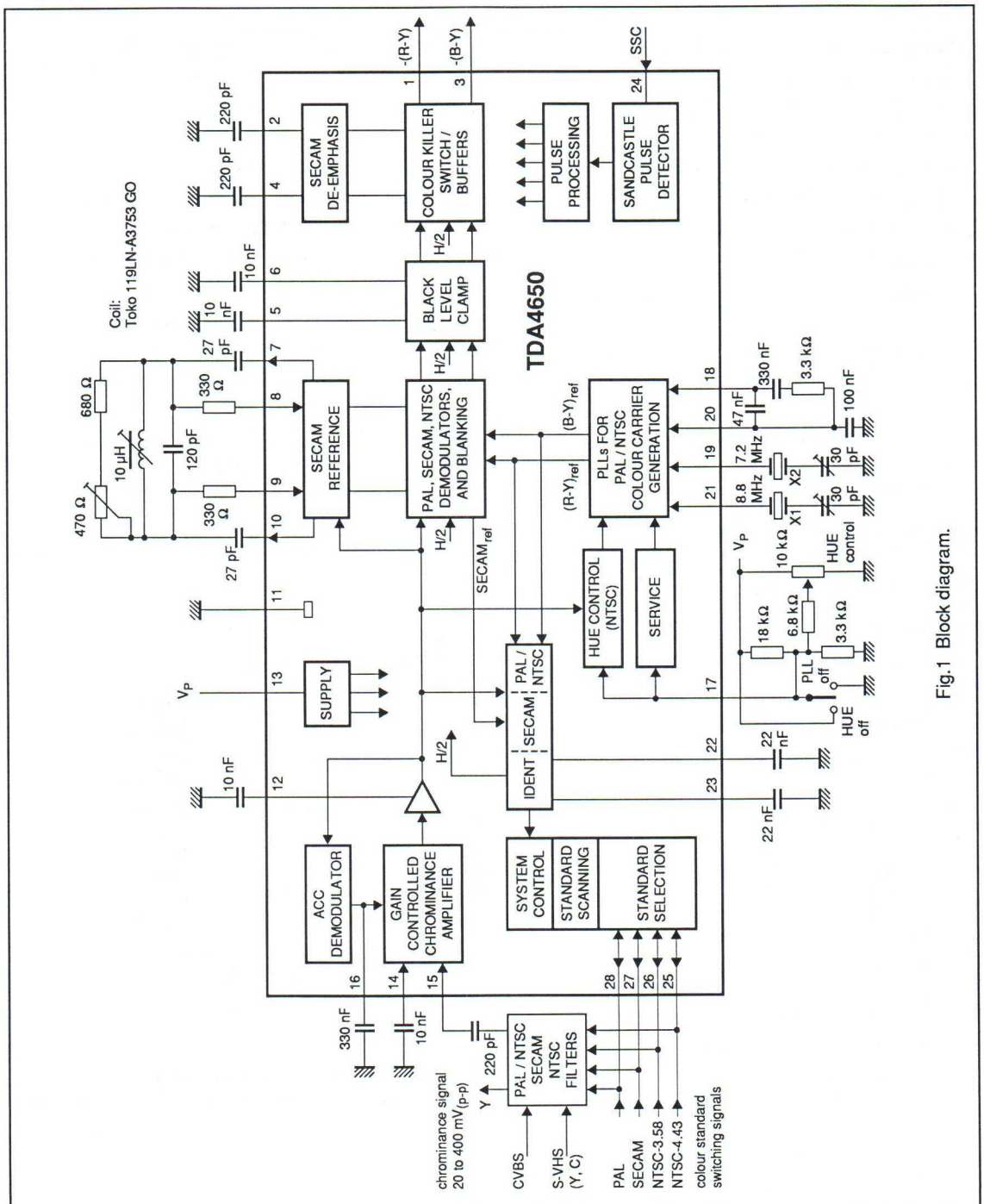


Fig.1 Block diagram.

Multistandard colour decoder, with negative colour difference output signals

TDA4650

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	-(R-Y) output
$-(R-Y)_{DE}$	2	(R-Y) de-emphasis
$-(B-Y)_O$	3	-(B-Y) output
$-(B-Y)_{DE}$	4	(B-Y) de-emphasis
$-(B-Y)_{CL}$	5	(B-Y) clamping
$-(R-Y)_{CL}$	6	(R-Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
SEC_{REF}	8	
SEC_{REF}	9	
SEC_{REF}	10	
GND	11	ground
C_D	12	DC for demodulators
V_P	13	supply voltage
C_{DC}	14	DC feedback

SYMBOL	PIN	DESCRIPTION
CHR_I	15	chrominance input
C_{ACC}	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C_{PLL}	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N_{IDENT}	22	NTSC identification
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N_{O1}	25	NTSC (4.43 MHz) identification
N_{O2}	26	NTSC (3.58 MHz) identification
SEC_O	27	SECAM identification
PAL_O	28	PAL identification

PIN CONFIGURATIONS

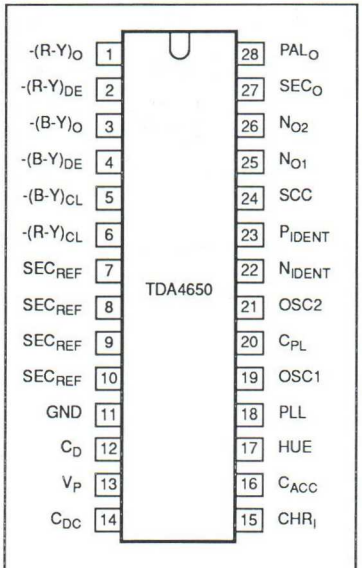


Fig.2(a) Pin configuration for DIL package.

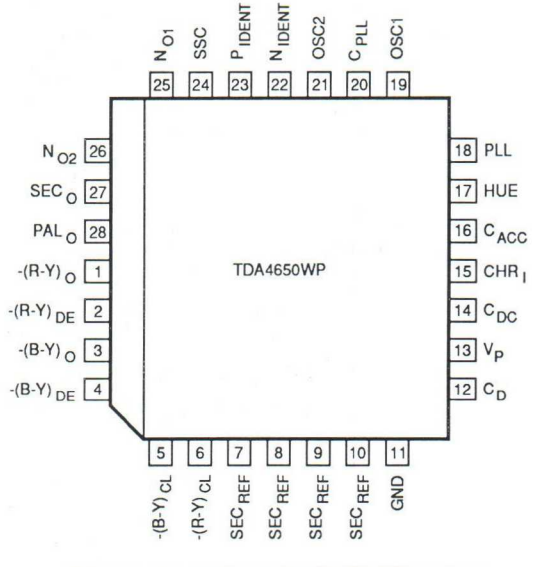


Fig.2(b) Pin configuration for PLCC package.

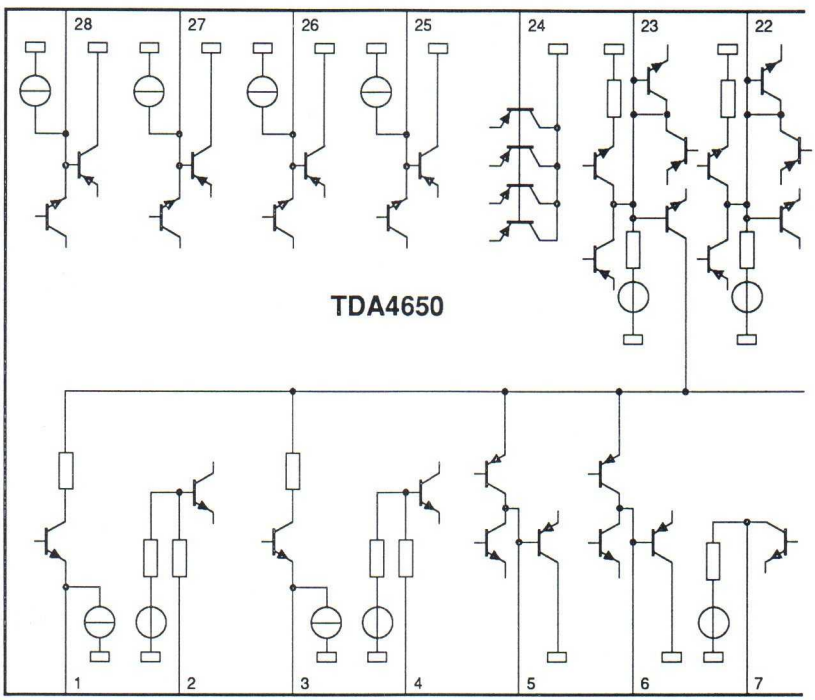


Fig.3a Internal circuits (continued in Fig.3b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13) –	13.2	V	
V_I	voltage range at pins 1, 3, 17 and 24 to 28	0	V_P	V
I_o	output current (pins 1 and 3)	–	–5	mA
$I_{i/o}$	input/output current (pins 25 to 28)	–	–5	µA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
$R_{th\ j\text{-}a}$	from junction to ambient in free air: SOT117	–	37	K/W
	SOT261	–	70	K/W
P_{tot}	total power dissipation (SOT117)	–	1.4	W
	total power dissipation (SOT261)	–	1.1	W

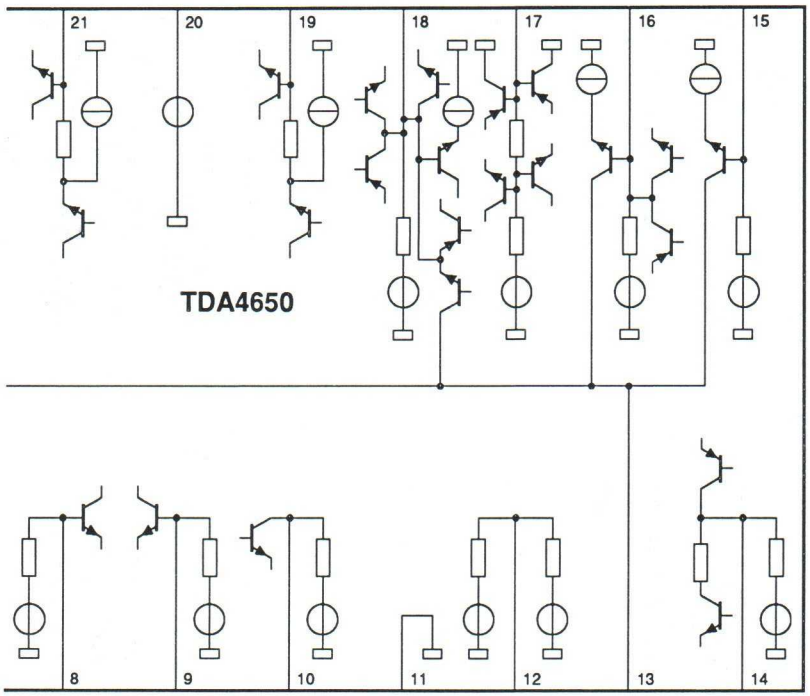


Fig.3b Internal circuits (continued from Fig.3a).

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15(p\text{-}p)}$ = 100 mV (with 75 % colour bar signal); 4 µs burst-blanking pulse and vertical blanking superimposed on super sandcastle pulse; T_{amb} = 25 °C; measured in test circuit of Fig. 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		10.8	12.0	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i(p\text{-}p)}$	input signal (pin 15) (peak-to-peak value)		20	100	400	mV
R_i	input resistance (pin 15)		7	10	13	kΩ
C_i	input capacitance (pin 15)		–	4	5	pF
Demodulator part (PAL/NTSC)						
$V_{1(p\text{-}p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.42	0.525	0.66	V
$V_{3(p\text{-}p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.53	0.665	0.84	V
V_1/V_3	ratio of colour difference signals (R-Y)/(B-Y) for NTSC	at nominal phase of hue control	0.75	0.79	0.83	
V_1/V_1	ratio of PAL/NTSC signals $(R\text{-}Y)_{PAL}/(R\text{-}Y)_{NTSC}$	at nominal phase of hue control	–	–	1	dB
m	signal linearity	$V_{1(p\text{-}p)}$ = 0.8 V – (R-Y)	0.8	–	–	
		$V_{3(p\text{-}p)}$ = 1.0 V – (B-Y)	0.8	–	–	
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3(p\text{-}p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	Ω
Demodulator part (SECAM); note 1						
$V_{1(p\text{-}p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	every second line blanked	0.83	1.05	1.32	V
$V_{3(p\text{-}p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	every second line blanked	1.06	1.33	1.67	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3(p\text{-}p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator part (SECAM) (continued); note 1						
$\Delta V_{1,3}/\Delta V_P$	shift of blanking levels relative to demodulated f_o levels		–	–	3	mV/V
$\Delta V_1/\Delta T$			–	0.16	–	mV/K
$\Delta V_3/\Delta T$			–	–0.25	–	mV/K
Hue control part						
ϕ	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 2 V	–30	–40	–	deg
	phase shift of reference carrier	V_{17} = 3 V	–	0	±5	deg
	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 4 V	30	40	–	deg
V_{17}	internal bias voltage		–	3	–	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	–	0.5	V
	switching voltage for forced colour ON	burst ON; colour ON	5.5	–	V_P	V
R_{17}	input resistance		3.8	5.0	6.2	kΩ
Reference oscillator (PLL); note 2						
$R_{19,21}$	input resistance		–	350	–	Ω
$C_{19,21}$	input resistance		–	–	10	pF
f_c	catching range	at 4.43 MHz	±400	–	–	Hz
		at 3.57 MHz	±330	–	–	Hz
Identification part switching voltages for chrominance filters and crystals: at pin 28 for PAL at pin 27 for SECAM at pin 26 for NTSC (3.58 MHz) at pin 25 for NTSC (4.43 MHz)						
$V_{28\ to\ 25}$	switching voltages	control voltage OFF state	–	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	–	V_P	V
$I_{28\ to\ 25}$	output currents		–	–	–3	mA
t_d	delay time for system hold		2	–	3	cycles
	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
t_s	scanning time for each standard	note 3	–	4	–	cycles

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Super sandcastle pulse detector (note 4)						
V_{24}	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	voltage pulse amplitude		7.7	–	V_P	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	μA

Notes to the characteristics

1. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R-Y) and (B-Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_0 voltage level is zero in the -(B-Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_0 voltage level is zero in the -(R-Y) output channel at pin 1. If necessary, the f_0 voltage level in the -(B-Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at the pins 2 and 4 (220 pF each) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
2. The f_0 frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
3. The inquiry sequence for the standard is:
   PAL – SECAM – NTSC (3.58 MHz) – NTSC (4.43 MHz).
   PAL has priority with respect to SECAM, etc.
4. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

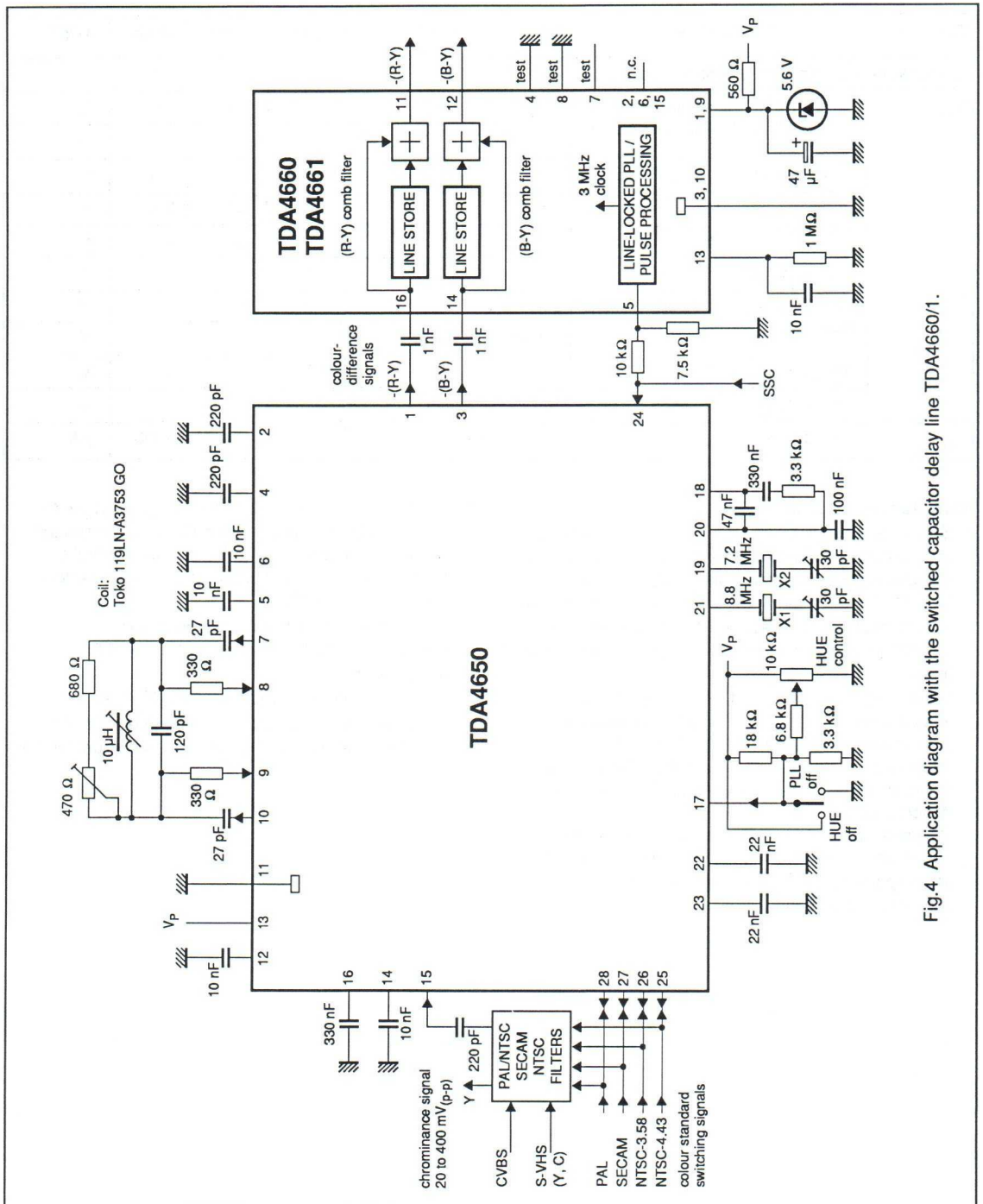


Fig.4 Application diagram with the switched capacitor delay line TDA4660/1.

Multistandard colour decoder with negative colour difference output signals

TDA4651

FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour difference signal output filters to remove the residual subcarrier
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter amplifier
  - quadrature demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment

GENERAL DESCRIPTION

The TDA4651 is a monolithic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour difference output signals are fed to the TDA4661, switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 13)		10.8	12	13.2	V
I_P	supply current (pin 13)		–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)	see note 1	20	200	400	mV
Colour difference output signals (see note 2)						
$V_{1(p-p)}$	–(R–Y) output (peak-to-peak value)	PAL	442	525	624	mV
		NTSC	370	440	523	mV
		SECAM	883	1050	1248	mV
$V_{3(p-p)}$	–(B–Y) output (peak-to-peak value)	PAL	559	665	791	mV
		NTSC	468	557	662	mV
		SECAM	1119	1330	1581	mV

Notes to the quick reference data

1. Within 3 dB output voltage deviation.
2. Burst key width for PAL 4.3 µs, for NTSC 3.6 µs
   Burst width for PAL and NTSC 2.25 µs, ratio burst-chrominance-amplitude 1/2.2.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4651	28	DIL	plastic	SOT117
TDA4651WP	28	PLCC	plastic	SOT261CG

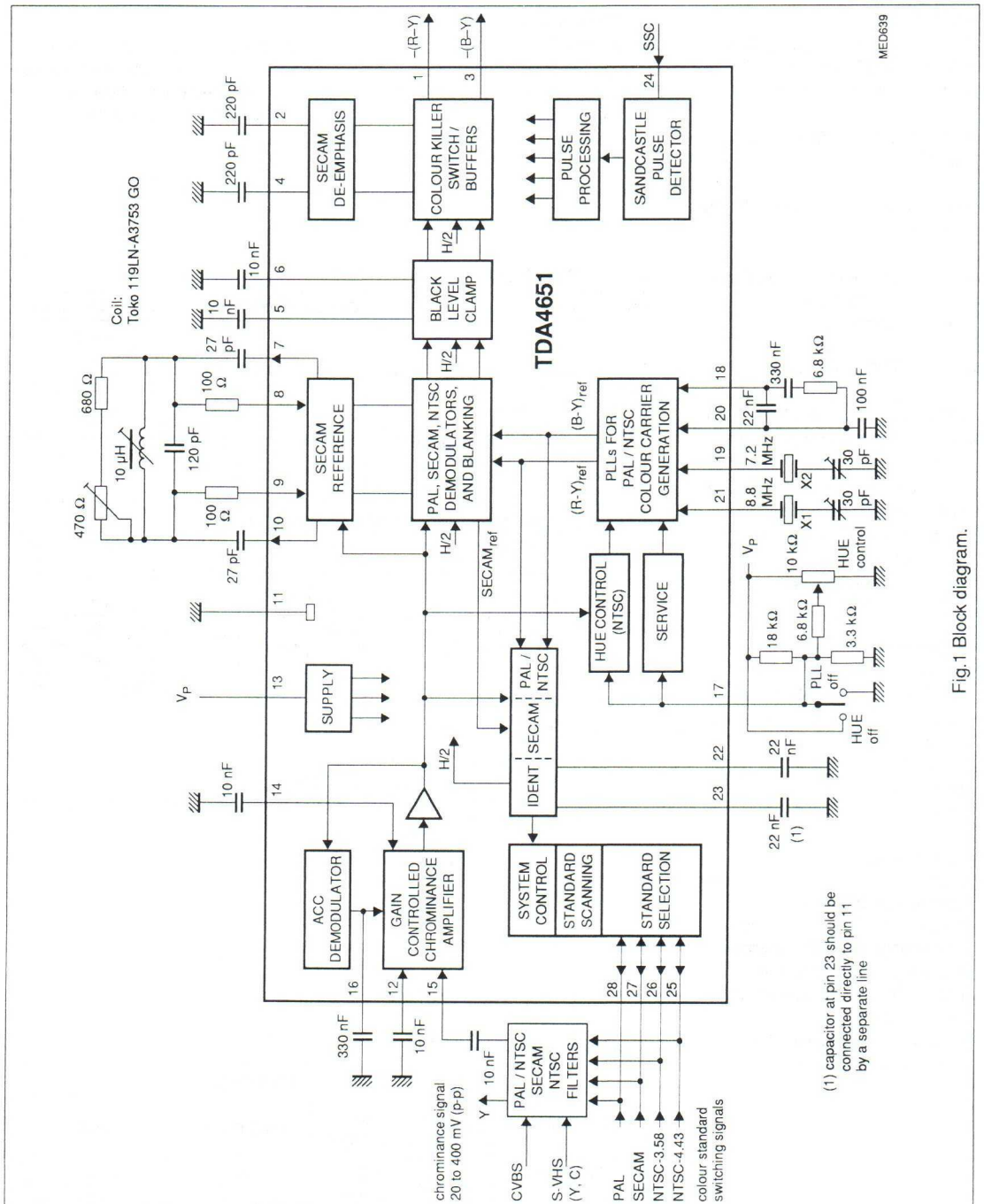


Fig.1 Block diagram.

Multistandard colour decoder with negative colour difference output signals

TDA4651

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	−(R−Y) output
$-(R-Y)_{DE}$	2	(R−Y) de-emphasis
$-(B-Y)_O$	3	−(B−Y) output
$-(B-Y)_{DE}$	4	(B−Y) de-emphasis
$-(B-Y)_{CL}$	5	(B−Y) clamping
$-(R-Y)_{CL}$	6	(R−Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
	8	
	9	
	10	
GND	11	ground
CHR_2	12	DC for ACC
V_P	13	supply voltage
C_{DC}	14	DC feedback

SYMBOL	PIN	DESCRIPTION
CHR_1	15	chrominance input
C_{ACC}	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C_{PLL}	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N_{IDENT}	22	NTSC identification
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N_{O1}	25	NTSC (4.43 MHz) identification
N_{O2}	26	NTSC (3.58 MHz) identification
SEC_O	27	SECAM identification
PAL_O	28	PAL identification

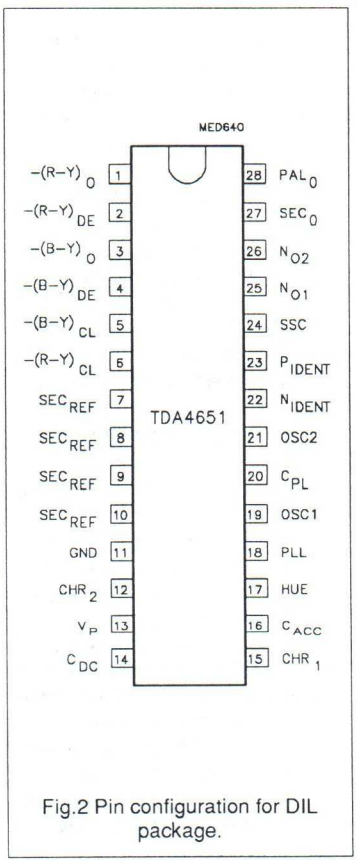


Fig.2 Pin configuration for DIL package.

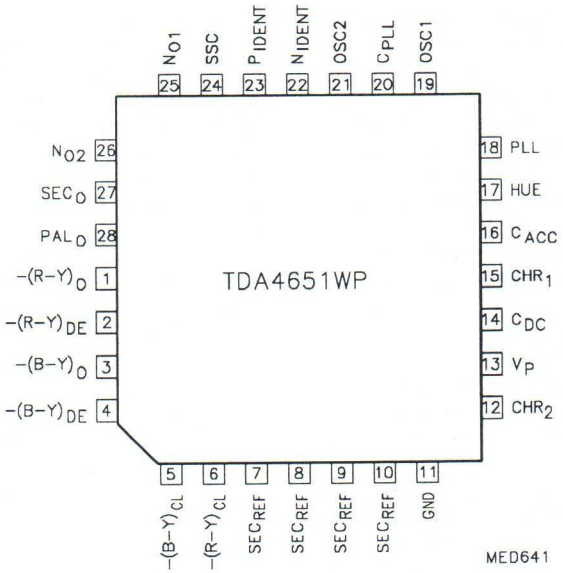


Fig.3 Pin configuration for PLCC package.

FUNCTIONAL DESCRIPTION

The IC (see block diagram Fig.1) contains all functions required for the identification and demodulation of PAL, SECAM, NTSC 4.43 MHz and NTSC 3.58 MHz signals. When an unknown signal is fed into the input, the circuit has to identify the standard of the signal; to achieve this it has to switch on successively the appropriate input filter, crystal (8.8 or 7.2 MHz) and demodulator and finally, after having identified the signal, it has to switch on the colour and, in the event of NTSC reception, the hue control. The two colour difference signals –(R–Y) and –(B–Y) are available at the outputs. The identification circuit is able to discriminate between NTSC signals with colour carrier frequencies of 3.58 MHz or 4.43 MHz.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal has to be AC coupled (pin 15). The differential amplifier stage at the input is followed by the gain control stage and a differential amplifier with lateral PNP transistors having the function of a level shifter.
The gain control stage consists of two ACC-rectifier circuits. One rectifier circuit is switched on during SECAM reception respectively during the SECAM part of the system-control-scanning (it is switched on during part of the burst gate pulse and it is disabled during the prolonged frame flyback); the other rectifier is switched on during the burst, when PAL or NTSC signals are received respectively during the PAL and NTSC parts of the system control scanning.
The DC-potential of the symmetrical signal connections to the demodulators is kept at the same level by means of a working point control stage.

Reference oscillator

The reference oscillator for PAL and NTSC operates at twice the colour carrier frequency. It is followed by a divider stage, providing the (R–Y) and (B–Y) reference signal with the correct phase relation to the PAL/NTSC demodulator and the identification part.

Demodulators

The demodulation of the colour signal requires three demodulators. Two are common for PAL and NTSC and one for the SECAM signals. In the event of NTSC reception, the symmetrical signal is fed into two differential amplifier stages with the correct gain and from there the signal is fed into two demodulators each consisting of four transistors. During NTSC reception the PAL switch between the differential amplifier of the (R–Y) channel and the corresponding demodulator is disabled. These transistors are switched on and off by the appropriate reference signals. In the event of PAL reception, the symmetrical signal is fed into the same differential amplifiers and the PAL switch is active.
The SECAM demodulator is a combined demodulator for –(B–Y) and –(R–Y) with artificial black level being inserted alternately every second line and during line and field flyback. The load resistors of the demodulator are connected to two differential amplifiers, one for –(B–Y) and one for –(R–Y). The unwanted signals occuring every second line ((R–Y) in the –(B–Y) channel and (B–Y) in the –(R–Y) channel) are blanked.

Clamp

Behind the demodulators the signals are being filtered and the black level is clamped to a constant DC-level during the burst gate pulse. For the SECAM signals this happens every second line, when the appropriate artificial black level is present.

De-emphasis and output-buffer

Behind the clamping stages is the de-emphasis for the SECAM signals and just in front of the output stages are the colour killer and blanking stages. The blanking level is the same as the clamping level and the black level.

Identification

The identification part contains three demodulators.
The first is demodulating during PAL and NTSC identification or reception. It is active during the burst clamping only. The reference signal has the (R–Y)-phase.
The second demodulator is demodulating during the SECAM identification or reception and is active during part of the burst clamping time. It uses the same signals as the SECAM demodulator that is not active during field flyback.
These two demodulators are followed by a H/2 switch 'rectifying' the demodulated signal. The result is an identification signal (P_{IDENT}) that is positive for a PAL signal during the PAL part of the scanning, for a SECAM signal during the SECAM part of the scanning and for a PAL signal during the NTSC 4.43 part of the scanning. If the P_{IDENT} is positive during the SECAM part of the scanning, the scanner switches back to the PAL part of the scanning in order to prevent that a PAL signal is erroneously identified as a SECAM signal (PAL priority). If then the P_{IDENT} is not positive, the scanner returns to SECAM part and remains there until the P_{IDENT} is

positive again. In the event of a field frequency of 60 Hz the signal cannot be identified as a SECAM signal, even if the P_{IDENT} is positive. If the H/2 signal is of the wrong polarity, the identification signal is negative and the H/2 flip-flop is set to the correct phase.

The third demodulator is demodulating during NTSC identification or reception only. It is active during the burst clamping time. The resulting identification signal (N_{IDENT}) is positive for PAL and NTSC 4.43 MHz signal during the NTSC 4.43 part of the scanning and for NTSC 3.58 MHz signal during the NTSC 3.58 part of the scanning. The reference signal has the (B–Y) phase.

The two identification signals allow an unequivocal identification of the received signal. If a signal has been identified, the scanning is stopped and after a delay time the colour is switched on.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13)	–	13.2	V
V_I	input voltage range at pins 1, 3, 17 and 24 to 28	0	V_P	V
I_O	output current (pins 1 and 3)	–	–5	mA
$I_{I/O}$	input/output current (pin 25 to 28)	–	–5	µA
T_{amb}	operating ambient temperature range	0	+70	°C
T_{stg}	storage temperature range	–25	+150	°C
P_{tot}	total power dissipation			
	SOT117	–	1.4	W
	SOT261CG	–	1.1	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT117	37 K/W
	SOT261CG	70 K/W

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15\ (p\text{-}p)}$ = 200 mV (with 75% colour bar signal); T_{amb} = +25 °C; measured in test circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		10.8	12	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i\ (p\text{-}p)}$	input signal range (pin 15) (peak-to-peak value)	see note 1	20	200	400	mV
R_I	input resistance (pin 15)		8.5	10	11.5	kΩ
C_I	input capacitance (pin 15)		–	4	5	pF
Demodulator part (PAL/NTSC)						
$V_{1\ (p\text{-}p)}$	colour difference –(R–Y) output signal (peak-to-peak value)	see note 2				
		PAL	442	525	624	mV
		NTSC	370	440	523	mV
$V_{3\ (p\text{-}p)}$	colour difference –(B–Y) output signal (peak-to-peak value)	see note 2				
		PAL	559	665	791	mV
		NTSC	468	557	662	mV
V_1/V_3	spread of ratio of colour difference signals (R–Y)/(B–Y)	at nominal phase of hue control	–	–	±5	%
V_1/V_1	spread of signal ratio PAL/NTSC	at nominal phase of hue control	–	–	±1	dB
m	signal linearity	$V_{1\ (p\text{-}p)}$ = 0.8 V – (R–Y)	0.8	–	–	
		$V_{3\ (p\text{-}p)}$ = 1.0 V – (B–Y)	0.8	–	–	
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3\ (p\text{-}p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	Ω
Demodulator part (SECAM) (see note 3)						
$V_{1\ (p\text{-}p)}$	colour difference –(R–Y) output signal (peak-to-peak value)	every second line blanked	0.88	1.05	1.25	V
$V_{3\ (p\text{-}p)}$	colour difference –(B–Y) output signal (peak-to-peak value)	every second line blanked	1.12	1.33	1.58	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3\ (p\text{-}p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV
$\Delta V_{1,3} / \Delta V_P$	shift of demodulated f_o levels relative to blanking level	with supply voltage	–	–	3	mV/V
$\Delta V_1 / \Delta T$		with temperature	–	0.16	–	mV/K
$\Delta V_3 / \Delta T$			–	–0.25	–	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hue control part						
ϕ	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 2 V	–30	–40	–	deg
	phase shift of reference carrier	V_{17} = 3 V	–	0	±5	deg
	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 4 V	30	40	–	deg
V_{17}	internal bias voltage	see note 4	–	3	–	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	–	0.5	V
	switching voltage for forced colour ON	HUE OFF; colour ON	5.5	–	V_P	V
R_{17}	input resistance		4.25	5.0	5.75	kΩ
Reference oscillator (PLL) (see note 5)						
$R_{19,21}$	input resistance		–	350	–	Ω
$C_{19,21}$	input capacitance		–	–	10	pF
f_c	catching range	at 4.43 MHz	±400	–	–	Hz
		at 3.57 MHz	±330	–	–	Hz
Identification part (see note 6)						
$V_{25 \text{ to } 28}$	switching voltages	control voltage OFF state	–	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	–	V_P	V
$I_{25 \text{ to } 28}$	output currents		–	–	–3	mA
t_d	delay time for system hold		2	–	3	cycles
	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
t_s	scanning time for each standard	see note 7	–	4	–	cycles
Super sandcastle pulse detector (see note 8)						
V_{24}	input pulse amplitude		7.7	–	V_P	V
	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	µA

Notes to the characteristics

1. With 20 mV, 3 dB decrease of the output signal is allowed. The level shift at demodulated f_0 relative to blanking level is less than 5 mV.
2. Burst-key width for PAL 4.3 µs, for NTSC 3.6 µs
   Burst width for PAL and NTSC 2.25 µs, ratio burst chrominance amplitude 1/2.2.
3. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R–Y) and (B–Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_0 voltage level is zero in the –(B–Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_0 voltage level is zero in the –(R–Y) output channel at pin 1. If necessary, the f_0 voltage level in the –(B–Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at pins 2 and 4 (each 220 pF) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
4. Pin 17 open-circuit; proportional to supply voltage.
5. The f_0 frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
6. Switching voltages for chrominance filters and crystals:
   at pin 28 for PAL
   at pin 27 for SECAM
   at pin 26 for NTSC (3.58 MHz)
   at pin 25 for NTSC (4.43 MHz).
7. The inquiry sequence for the standard is: PAL - SECAM - NTSC (3.58 MHz) - NTSC (4.43 MHz). PAL has priority with respect to SECAM, etc.
8. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

Table 1 Specification of quartz crystals in HC-49/U13 holder; standard application.

SYMBOL	PARAMETER	VALUE		UNIT
		43221430405	**43221430418**	
f_n	nominal frequency	8.867238	7.159090	MHz
C_L	load capacitance	20		pF
Δf_n	adjustment tolerance of f_n at +25 °C	±40		ppm
$R_{dld\ max}$	in the drive level range between 10^{-12} W and 1.0×10^{-3} W, the resonance resistance may not exceed (at +25 °C) the value of $R_{dld\ max}$	100	50	Ω
R_n	resonance resistance of unwanted response	$2R_{r\ (+25\ °C)}$		Ω
C_1	motional capacitance (±20%)	22	19.5	fF
C_0	parallel capacitance (±20%)	5.5	4.4	pF
T	operating temperature range	–10 to +60		°C
Δf_n	frequency tolerance over temperature range	±25		ppm
R_r	maximum resonance resistance over temperature range	60		Ω

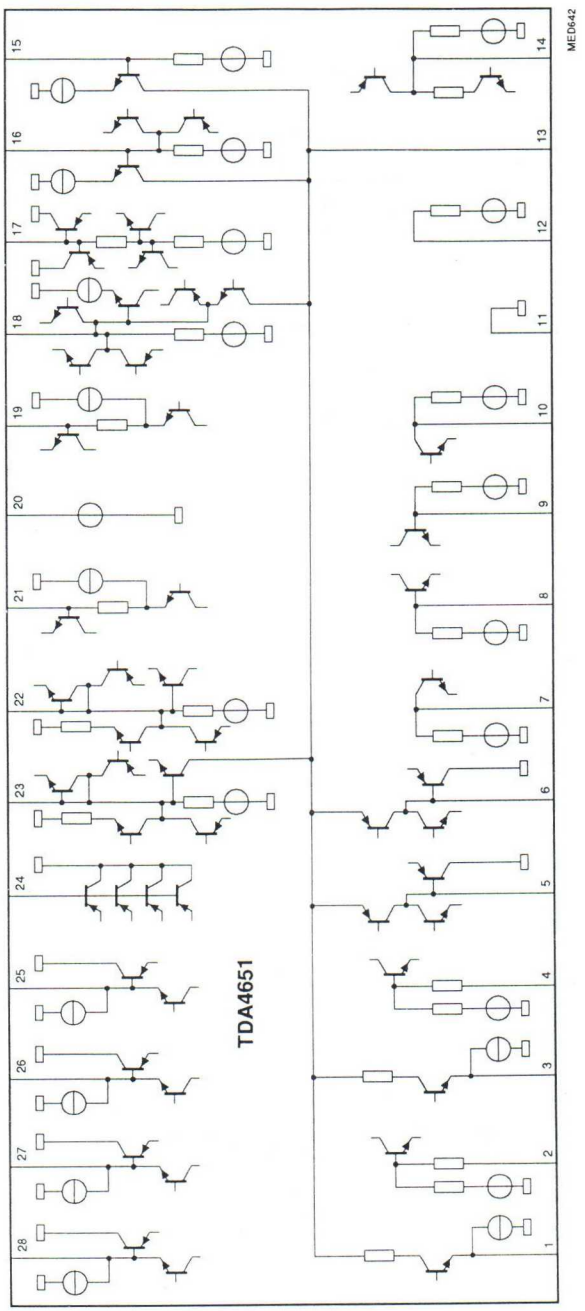


Fig.4 Internal circuits.

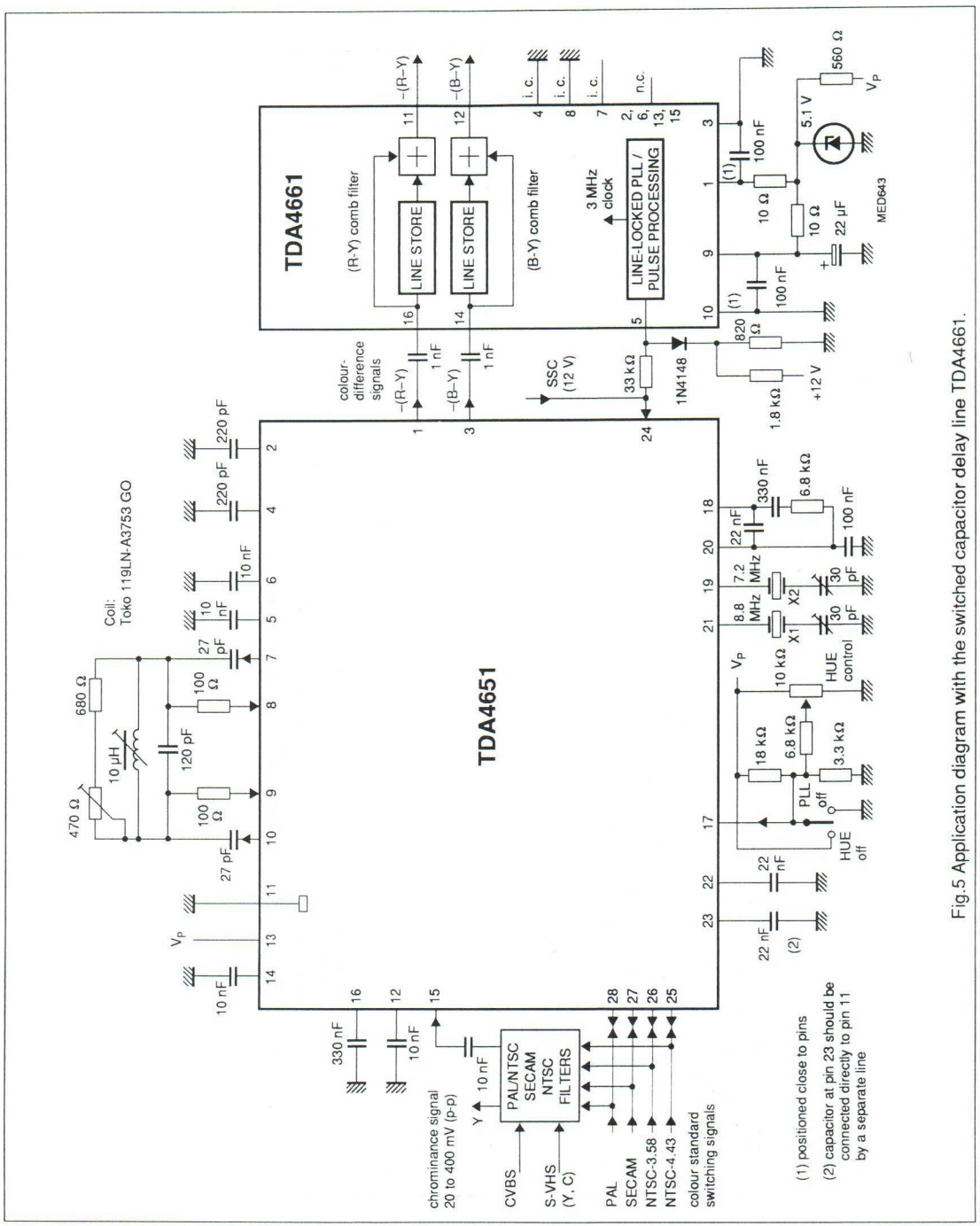


Fig.5 Application diagram with the switched capacitor delay line TDA4661.

Generic multi-standard decoder — TDA4655

FEATURES

- Low voltage (8 V)
- Low power dissipation (250 mW)
- Automatic standard recognition
- No adjustments required
- Reduced external components
- Not all time constants integrated (ACC, SECAM de-emphasis).

GENERAL DESCRIPTION

The TDA4655 is a monolithic integrated multi-standard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. It is adapted to the integrated baseband delay line TDA4660/61.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current	V_P = 8.0 V; without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V; without load	–	248	296	mW
Inputs						
V_{11}	chrominance input voltage (peak-to-peak value)	note 1	20	200	400	mV
V_{24}	sandcastle input voltage		–	–	13.2	V
Outputs						
V_1	colour difference output signals (peak-to-peak value)	independent of supply voltage; note 2				
	–(R–Y) output PAL and NTSC 4.43 MHz		442	525	624	mV
	NTSC 3.58 MHz		370	440	523	mV
	SECAM		950	1050	1150	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz		559	665	791	mV
	NTSC 3.58 MHz		468	557	662	mV
	SECAM		1200	1330	1460	mV

Notes to quick reference data

1. Within 2 dB output voltage deviation.
2. Burstkey width for PAL 4.3 µs, for NTSC 3.6 µs.
   Burst width for PAL and NTSC 2.25 µs,
   ratio burst chrominance amplitude 1/2.2.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4655	24	SDIL	plastic	SOT234
TDA4655T	24	SO	plastic	SOT137A

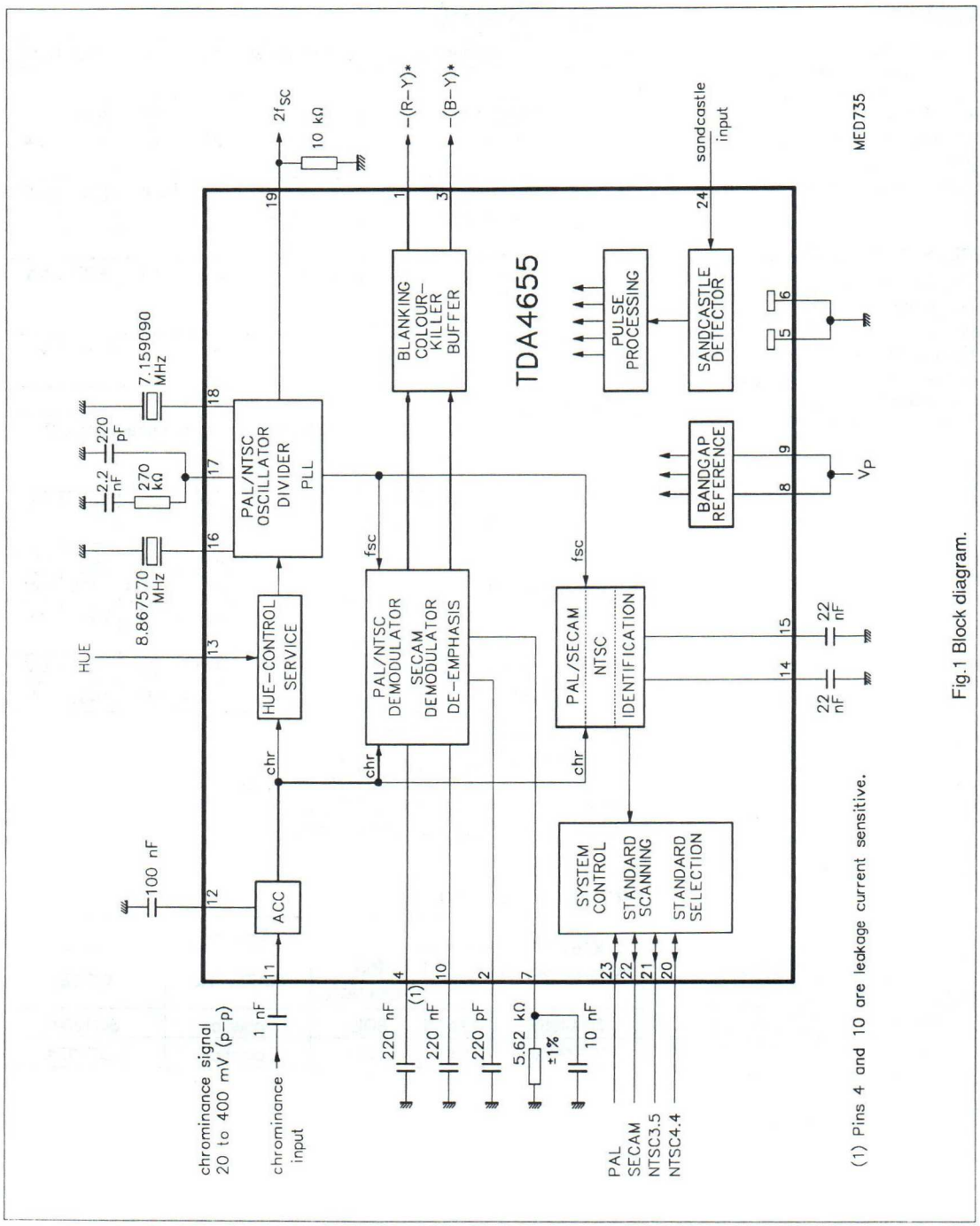


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	colour difference signal output –(R–Y)* for baseband delay line
DEEM	2	external capacitor for SECAM de-emphasis
$-(B-Y)_O$	3	colour difference signal output –(B–Y)* for baseband delay line
CFOB	4	external capacitor SECAM demodulator control (B–Y) Channel
GND_1	5	ground
GND_2	6	ground
I_{REF}	7	external resistor for SECAM oscillator
V_{P1}	8	supply 8 V
V_{P2}	9	supply 8 V
CFOR	10	external capacitor SECAM demodulator control (R–Y) Channel
CHR_I	11	chrominance signal input
C_{ACC}	12	external capacitor for ACC control
HUE	13	input for HUE control and service switch
N_{IDT}	14	external capacitor for identification circuit (NTSC)
P_{IDT}	15	external capacitor for identification circuit (PAL and SECAM)
OSC_1	16	PAL crystal
PLL	17	external loop filter
OSC_2	18	NTSC crystal
2FSC	19	2 x f_{SC} output
N_{O1}	20	standard setting input/output for NTSC4.43
N_{O2}	21	standard setting input/output for NTSC3.58
SEC_O	22	standard setting input/output for SECAM
PAL_O	23	standard setting input/output for PAL
SC	24	sandcastle input

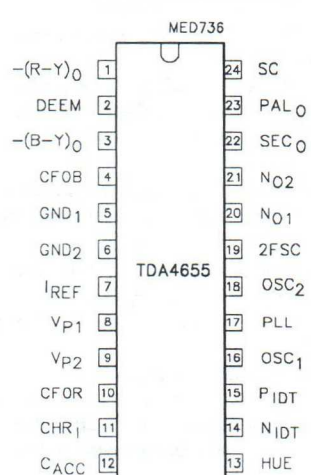


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The IC contains all functions required for the identification and demodulation of signals with the standards PAL, SECAM, NTSC3.5 with 3.58 MHz colour-carrier frequency and NTSC4.3 with 4.43 MHz colour-carrier frequency. When an unknown signal is fed into the input, the circuit has to detect the standard of the signal, and has to switch on successively the appropriate input filter, crystal (8.8 or 7.2 MHz) and demodulator and finally, after having identified the signal, it has to switch on the colour and, in event of NTSC reception, the hue control. At the outputs the two colour difference signals –(R–Y)* and –(B–Y)* are available. The identification circuit is able to discriminate between NTSC signals with colour-carrier frequencies of 3.58 MHz or 4.43 MHz.

ACC-stage

The chrominance signal is fed into the asymmetrical input (pin 11) of the ACC-stage (Automatic Colour Control). The input has to be AC coupled and has an input impedance of 20 kΩ in parallel with 10 pF.

To control the chrominance amplitude the modulation independent burst amplitude is measured during the burstkey pulse which is derived from the sandcastle pulse present at pin 24. The generated error current is fed into an external storage capacitor at pin 12. The integrated error voltage controls the gain of the ACC stage so that its output is independent of input signal variations.

The measurement is disabled during the vertical blanking to avoid failures because of missing burst signals.

Reference signal generation

The reference signal generation is achieved by a PLL system. The reference oscillator operates at twice the colour-carrier frequency and is locked on the burst of the chrominance signal (chr). A divider provides reference signals (f_{SC}) with the correct phase relationship for the PAL/NTSC demodulator and the identification part. In the SECAM mode the two f_0 frequencies are derived from the PAL crystal frequency by special dividers. In this mode the oscillator is not locked to the input signal. In the NTSC mode the hue control circuit is switched between ACC stage and PLL. The phase shift of the signal can be controlled by a DC voltage at pin 13. The hue control circuit is switched off during scanning.

The reference frequency ($2 \times f_{SC}$) is available at pin 19 to drive a PAL comb filter for example.

Demodulation

The demodulation of the colour signal requires two demodulators. One is common for PAL and NTSC signals, the other is for SECAM signals.

The PAL/NTSC demodulator consists of two synchronized demodulators, one for the (B–Y) Channel and the other for the (R–Y) Channel. The required reference signals (f_{SC}) are input from the reference oscillator. In NTSC mode the PAL switch is disabled.

The SECAM demodulator consists of a PLL system. During vertical blanking the PLL oscillator is tuned to the f_0 frequencies to provide a fixed black level at the demodulator output. During demodulation the control voltages are stored in the external capacitors at pins 4 and 10.

The oscillator requires an external resistor at pin 7. Behind the PLL demodulator the signal is fed into the de-emphasis network which consists of two internal resistors (2.8 kΩ and 5.6 kΩ) and an external capacitor connected at pin 2 (220 pF).

After demodulation the signal is filtered and then fed into the next stage.

Blanking, colour-killer, buffers

As a result of using only one demodulator in SECAM mode the demodulated signal has to be split up in the (B–Y) Channel and the (R–Y) Channel. The unwanted signals occuring every second line, (R–Y) in the (B–Y) Channel and (B–Y) in the (R–Y) Channel, have to be blanked. This happens in the blanking stage by an artificial black level being inserted alternately every second line.

To avoid disturbances during line and field flyback these parts of the colour differential signals are blanked in all modes.

When no signal has been identified, the colour is switched off (signals are blanked) by the colour killer.

At the end of the colour channels are low-ohmic buffers (emitter followers). The CD output signals –(B–Y)* and –(R–Y)* are available at pins 1 and 3.

Identification and system control

The identification part contains three identification demodulators.

The first demodulates in PAL mode. It is only active during the burstkey pulse. The reference signal (f_{SC}) has the (R–Y) phase.

The second demodulator (PLL system) operates in SECAM mode and is active also during the burstkey pulse, but delayed by 2 µs.

The PLL demodulator discriminates the frequency difference between the unmodulated f_0 frequencies of the incoming signal (chr) and the reference frequency input from the crystal oscillator.
These two demodulators are followed by an H/2 switch 'rectifying' the demodulated signal. The result is an identification signal (P_{IDT}, pin 15) that is positive for a PAL signal in PAL mode, for a SECAM signal in SECAM mode and for a PAL signal in NTSC4.4 mode. If P_{IDT} is positive in SECAM mode, the scanner switches back to the PAL mode in order to prevent a PAL signal being erroneously identified as a SECAM signal (PAL priority). If then P_{IDT} is not positive, the scanner returns to SECAM mode and remains there until P_{IDT} is positive again. In the event of a field frequency of 60 Hz the signal can not be identified as a SECAM signal, even if P_{IDT} is positive. In this event the scanner switches forward in the NTSC3.5 mode. If the H/2 signal has the wrong polarity, the identification signal is negative and the H/2 flip-flop is set to the correct phase.
The third demodulator operates in NTSC mode and is active during the burstkey pulse. The resulting identification signal (N_{IDT}, pin 14) is positive for PAL and NTSC4.4 signals in NTSC4.4 mode and for NTSC3.5 signals in the NTSC3.5 mode. The reference signal has the (B–Y) phase.
The two identification signals allow an unequivocal identification of the received signal. In the event of a signal being identified, the scanning is stopped and after a delay time the colour is switched on.
The standard outputs (active HIGH) are available at the pins 20, 21, 22 and 23. During scanning the HIGH level is 2.5 V and when a signal has been identified the HIGH level is switched to 6 V. The standard pins can also be used as inputs in order to force the IC into a desired mode (Forced Standard Setting).

Sandcastle detector and pulse processing
In the sandcastle detector the super sandcastle pulse (SC) present at pin 24 is compared with three internal threshold levels by means of three differential amplifiers. The derived signals are the burstkey pulse, the horizontal blanking pulse and the combined horizontal and vertical blanking pulse. These signals are processed into various control pulses required for the timing of the IC.

Bandgap reference
In order to ensure that the CD output signals and the threshold levels of the sandcastle detector are independent of supply voltage variations a bandgap reference voltage has been integrated.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_P	supply voltage		–	8.8	V
P_{tot}	power dissipation	without load	–	330	mW
V_{24}	voltage at pin 24	I_{max} = 10 μA	–	15	V
	voltage at all other pins	I_{max} = 100 μA	–	V_P + V_{be}	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance on printed-circuit board from junction to ambient in free air (without heat spreader)	
	SO 24	90 K/W
	SDIL 24	70 K/W

CHARACTERISTICS

Measured with application circuit (Fig.4) at T_{amb} = +25 °C, 8 V supply, 75% colour bar chrominance input signal of 200 mV (peak-to-peak value) and nominal phase for NTSC unless otherwise specified. All voltages measured referenced to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
I	supply current	V_P = 8.0 V without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V without load	–	248	296	mW
CD signal outputs (pins 1 and 3)						
PAL or NTSC						
V_1	colour difference output signals	independent of supply voltage; note 1				
	–(R–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		442	525	624	mV
	NTSC 3.58 MHz (peak-to-peak value)		370	440	523	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		559	665	791	mV
	NTSC 3.58 MHz (peak-to-peak value)		468	557	662	mV
V_{PAL}/V_{NTSC}	signal ratio PAL/NTSC 3.58 MHz	note 2	0.5	1.5	2.5	dB
V_1/V_3	ratio of CD signal amplitudes V(R–Y)/V(B–Y)	note 2	0.75	0.79	0.83	–
m	signal linearity –(R–Y) output	V_1 = 0.8 V (p-p)	0.8	–	–	–
	signal linearity –(B–Y) output	V_3 = 1.0 V (p-p)	0.8	–	–	–
f_g	cut-off frequency (both outputs)	–3 dB	–	1	–	MHz
t_d	chrominance delay time		220	270	320	ns
S/N	signal to noise ratio for nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs: 1 x subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 x subcarrier frequency (peak-to-peak value)	note 4	–	–	30	mV
	H/2 content at R–Y output at nominal input signal (peak-to-peak value)		–	–	10	mV
A	crosstalk between CD Channels		–40	–	–	dB
R_1, R_3	output resistance (npn emitter follower)		–	–	200	Ω
I_1, I_3	output current		–	–	–3	mA
SECAM						
V_1	colour difference output signals	independent of supply voltage; note 5				
	–(R–Y) output (peak-to-peak value)		0.95	1.05	1.15	V
V_3	–(B–Y) output (peak-to-peak value)		1.20	1.33	1.46	V
V_1/V_3	ratio of CD signal amplitudes V(R–Y)/V(B–Y)		0.75	0.79	0.83	–
m	signal linearity at nominal output voltage		0.8	–	–	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_g	cut-off frequency	–3 dB	–	730	–	kHz
t_d	chrominance delay time		400	500	600	ns
S/N	signal to noise ratio for 100 mV (p-p) input signal and nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs: 1 x subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 x subcarrier frequency (peak-to-peak value)		–	–	20	mV
ΔV_3	shift of demodulated f_0 level relative to blanking level –(B–Y) output	note 9	–	0	±13	mV
ΔV_1	–(R–Y) output		–	0	±10	mV
Impedance and currents see PAL or NTSC specification						
Capacitor for SECAM de-emphasis (pin 2)						
C_2	value of external capacitor		–	220	–	pF
R_A	value of internal de-emphasis resistors	T_{amb} = +35 °C	2.4	2.8	3.2	kΩ
R_B			4.8	5.6	6.4	kΩ
$\Delta(R_A/R_B)$	relative tolerance of de-emphasis resistors		–	–	±5	%
Capacitors for SECAM demodulator control (pins 4 and 10; note 6)						
$\Delta V_{1,3}$	shift of demodulated f_0 level due to external leakage current	C_{ext} = 220 nF	–	–	0.3	mV/nA
Resistor for SECAM oscillator (pin 7)						
V_7	DC voltage		2.4	2.81	3.2	V
R_7	value of external resistor (±1%)		–	5.62	–	kΩ
C_7	value of external capacitor (±20%)		–	10	–	nF
Chrominance input (pin 11)						
V_{11}	input signal (peak-to-peak value)	note 7	20	200	400	mV
R_{11}	input resistance		16	20	24	kΩ
C_{11}	input capacitance		–	–	10	pF
Capacitor for ACC (pin 12; note 8)						
$\Delta V_{1,3}$	change of CD output signals during field blanking due to external leakage current	C_{ext} = 100 nF	–	0.2	–	%/nA
Hue control (NTSC) and service switch (pin 13)						
ϕ	phase shift of reference carrier relative to phase at open-circuit pin 13	V_{13} = 3 V	–30	–	–	°
		V_{13} = open-circuit	–5	0	+5	°
		V_{13} = 5 V	+30	–	–	°
V_{13}	internal bias voltage (proportional to supply voltage)	pin 13 open-circuit	3.8	4.0	4.2	V
R_{13}	input resistance		25	30	35	kΩ
Capacitor for identification (pins 14 and 15)						
V_{14}, V_{15}	DC voltage for an identified signal		2.8	3.2	3.5	V
	DC voltage for an unidentified signal		1.5	2.0	2.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL oscillator measured with nominal crystal (pins 16 and 18; see Table 1)						
R_{16}, R_{17}	initial oscillator amplifier input resistance		−500	–	–	Ω
C_{16}, C_{17}	oscillator amplifier input capacitance		–	–	10	pF
Δf_L	lock-in-range referenced to	note 10				
	4.43361875 MHz		±400	–	±1300	Hz
	3.579545 MHz		±330	–	±1300	Hz
ϕ	phase difference for ±400 Hz respectively 330 Hz deviation of colour carrier frequency		–	–	1	degree
2 x f_{SC} output (pin 19; if the output is not used, the pin should be connected to supply)						
V_{19}	DC output level	I_{19} = 0 A	6.1	6.3	6.5	V
R_{19}	output resistance	I_{19} = 0 A	–	–	350	Ω
I_{19}	output current		–	–	−1.0	mA
V_{19}	output signal (peak-to-peak value)		–	250	–	mV
Standard setting inputs/outputs (pins 20 to 23; note 11)						
used as output: npn emitter follower output with 0.1 mA source to ground						
V_O	on-state, during scanning, colour OFF		2.4	2.5	2.7	V
	on-state, colour ON		5.8	6.0	6.2	V
R_O	output resistance	I_O = 0	–	–	300	Ω
I_O	output current		–	–	−3	mA
used as input: forced system switching						
V_O	threshold for system ON		6.8	7.0	7.2	V
I_O	input current		100	150	180	µA
Sandcastle pulse detector (pin 24; note 12)						
C_{24}	input capacitance		–	–	10	pF
V_{24}	thresholds for field and line pulse separation	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	line pulse separation	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	burst pulse separation	pulse ON	5.3	5.6	5.9	V
		pulse OFF	5.1	5.4	5.7	V
System control processing (note 13)						
t_d	system hold delay	in event of a signal disappearing for a short time	2	–	3	field periods
	colour killer; colour ON delay	switching occurs during field blanking	2	–	3	field periods
	colour OFF delay		0	–	1	field periods
t_s	scanning time for each system		–	4	–	field periods

QUALITY SPECIFICATION

URV-4-2-59/601

Notes to the characteristics

1. Burstkey width for PAL 4.3 µs, for NTSC 3.6 µs.
   Burst width for PAL and NTSC 2.25 µs, ratio burst chrominance amplitude 1/2.2.
2. At nominal phase of hue control.
3. V (p-p) of signal divided by 6 times effective noise voltage.
4. At NTSC 3.58 35 mV (p-p).
5. H/2 blanking alternately every second line.
6. These pins are leakage current sensitive. Pin 4 for (B–Y) Channel, pin 10 for (R–Y) Channel.
7. Within 2 dB output voltage deviation.
8. This pin is leakage current sensitive.
9. IC only.
10. Depends also on network on pin 17.
11. Pin 23 for PAL, pin 22 for SECAM, pin 21 for NTSC 3.58 MHz, pin 20 for NTSC 4.43 MHz.
    Threshold levels are dependent on supply.
12. The field interval of the sandcastle has to be adapted to the ICs TDA2579B and TDA4690.
    The thresholds are independent of supply voltage.
13. System scanning sequence: PAL, SECAM, NTSC3.5, NTSC4.4.

Table 1 Specification of quartz crystals in HC-49/U13 holder; standard application.

SYMBOL	PARAMETER	VALUE		UNIT
		9922 520 00385	**9922 520 00387**	
f_n	nominal frequency	8.867570	7.159090	MHz
C_L	load capacitance	series resonance		
Δf_n	adjustment tolerance of f_n at +25 °C	±20		ppm
R_r	resonance resistance over temperature range	≤ 60		Ω
$R_{dld\ max}$	in the drive level range between 10^{-12} W and 1.0×10^{-3} W, the resonance resistance may not exceed (at +25 °C) the value of $R_{dld\ max}$	tbn	tbn	Ω
R_n	resonance resistance of unwanted response	$2R_{r\ (+25\ °C)}$		Ω
C_1	motional capacitance (±20%)	14.0	19.5	fF
C_0	parallel capacitance (±20%)	3.6	4.4	pF
T_{amb}	operating ambient temperature	−10 to +60		°C
Δf_n	frequency tolerance over temperature	±20		ppm

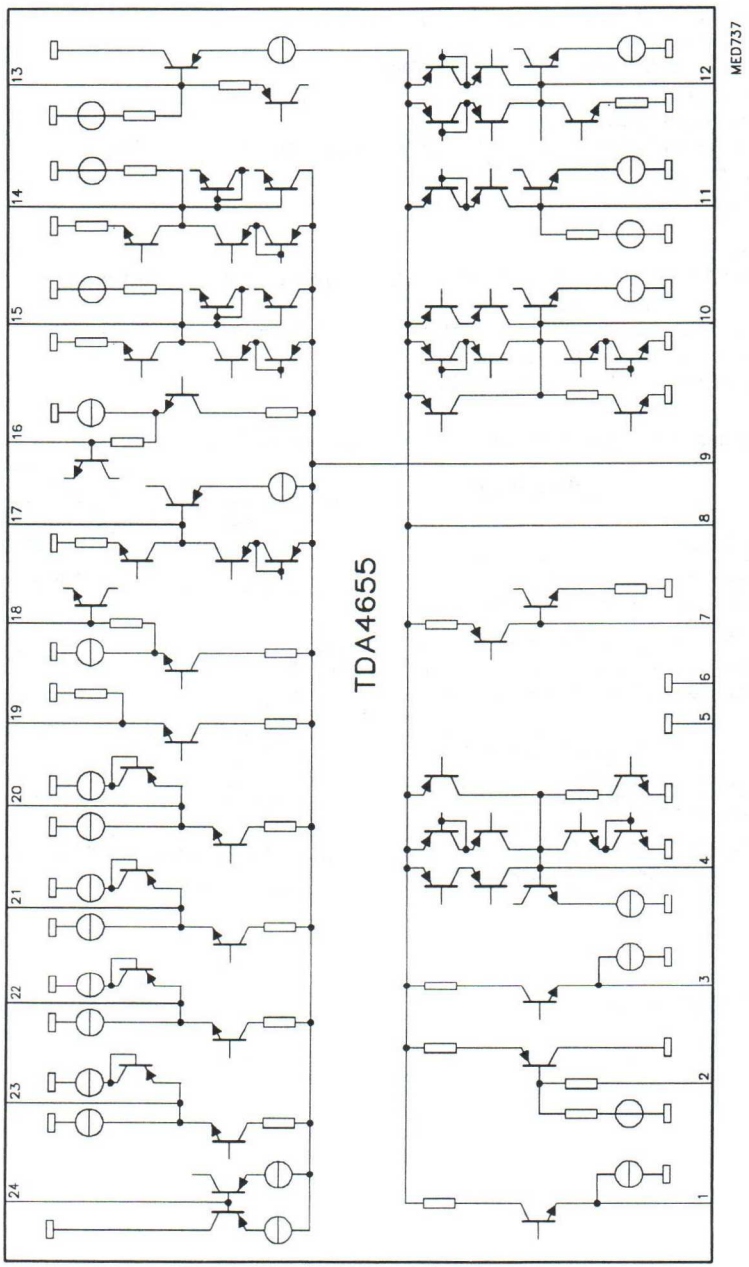
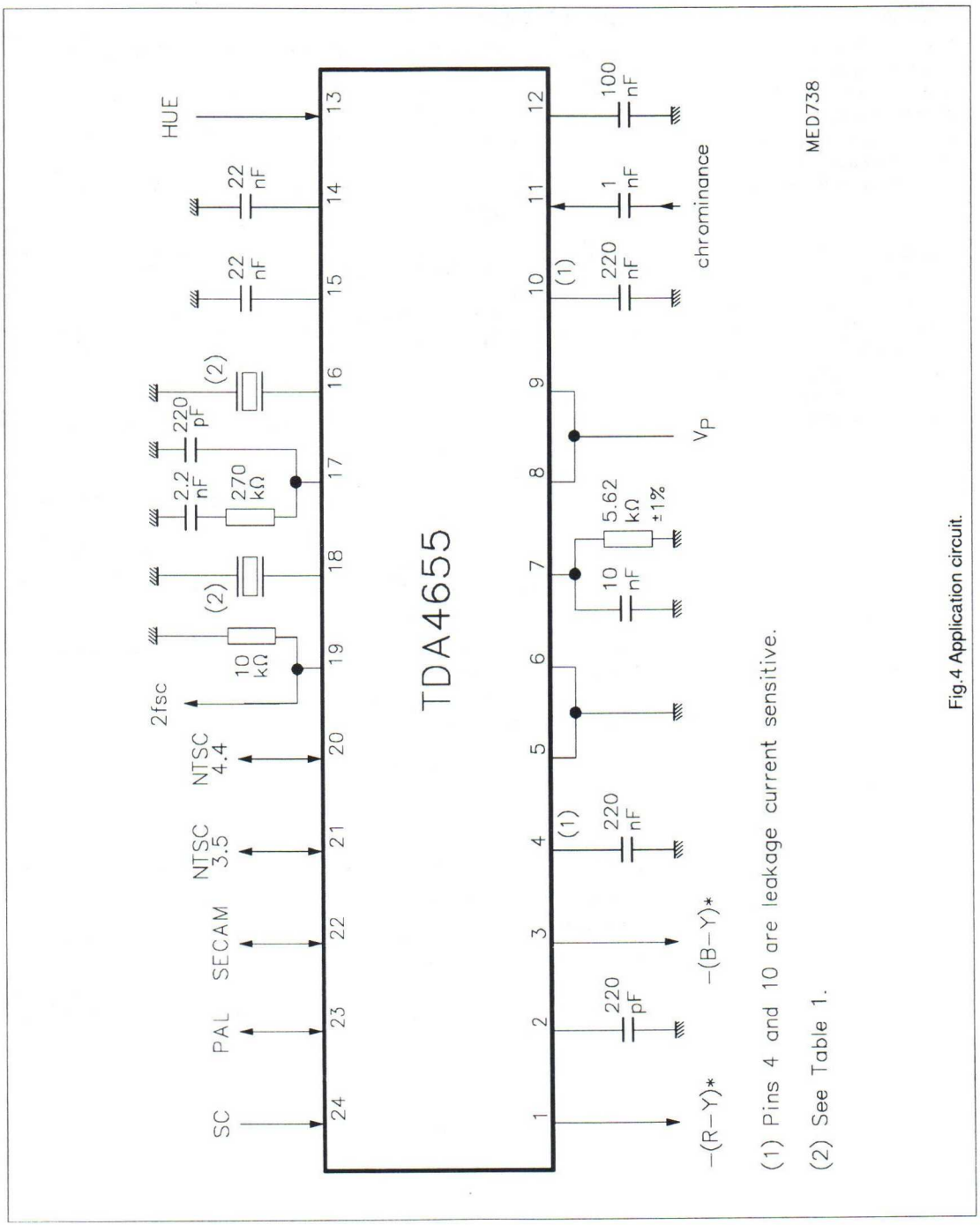


Fig.3 Internal circuits.



(1) Pins 4 and 10 are leakage current sensitive.

(2) See Table 1.

Fig.4 Application circuit.

Generic multi-standard decoder — TDA4657

FEATURES

- Low voltage (8 V)
- Low power dissipation (250 mW)
- Automatic standard recognition
- No adjustments required
- Reduced external components
- Not all time constants integrated (ACC, SECAM de-emphasis).

GENERAL DESCRIPTION

The TDA4657 is a monolithic integrated multi-standard colour decoder for PAL, SECAM and NTSC 4.43 MHz with negative colour difference output signals. It is adapted to the integrated baseband delay line TDA4660/61.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current	V_P = 8.0 V; without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V; without load	–	248	296	mW
Inputs						
V_9	chrominance input voltage (peak-to-peak value)	note 1	20	200	400	mV
V_{20}	sandcastle input voltage		–	–	13.2	V
Outputs						
V_1	colour difference output signals (peak-to-peak value)	independent of supply voltage; note 2				
	–(R–Y) output PAL and NTSC 4.43 MHz		442	525	624	mV
	SECAM		950	1050	1150	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz		559	665	791	mV
	SECAM		1200	1330	1460	mV

Notes to quick reference data

1. Within 2 dB output voltage deviation.
2. Burstkey width 4.3 µs
   Burst width 2.25 µs,
   ratio burst chrominance amplitude 1/2.2.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4657	20	DIL	plastic	SOT146
TDA4657T	20	SO	plastic	SOT163A

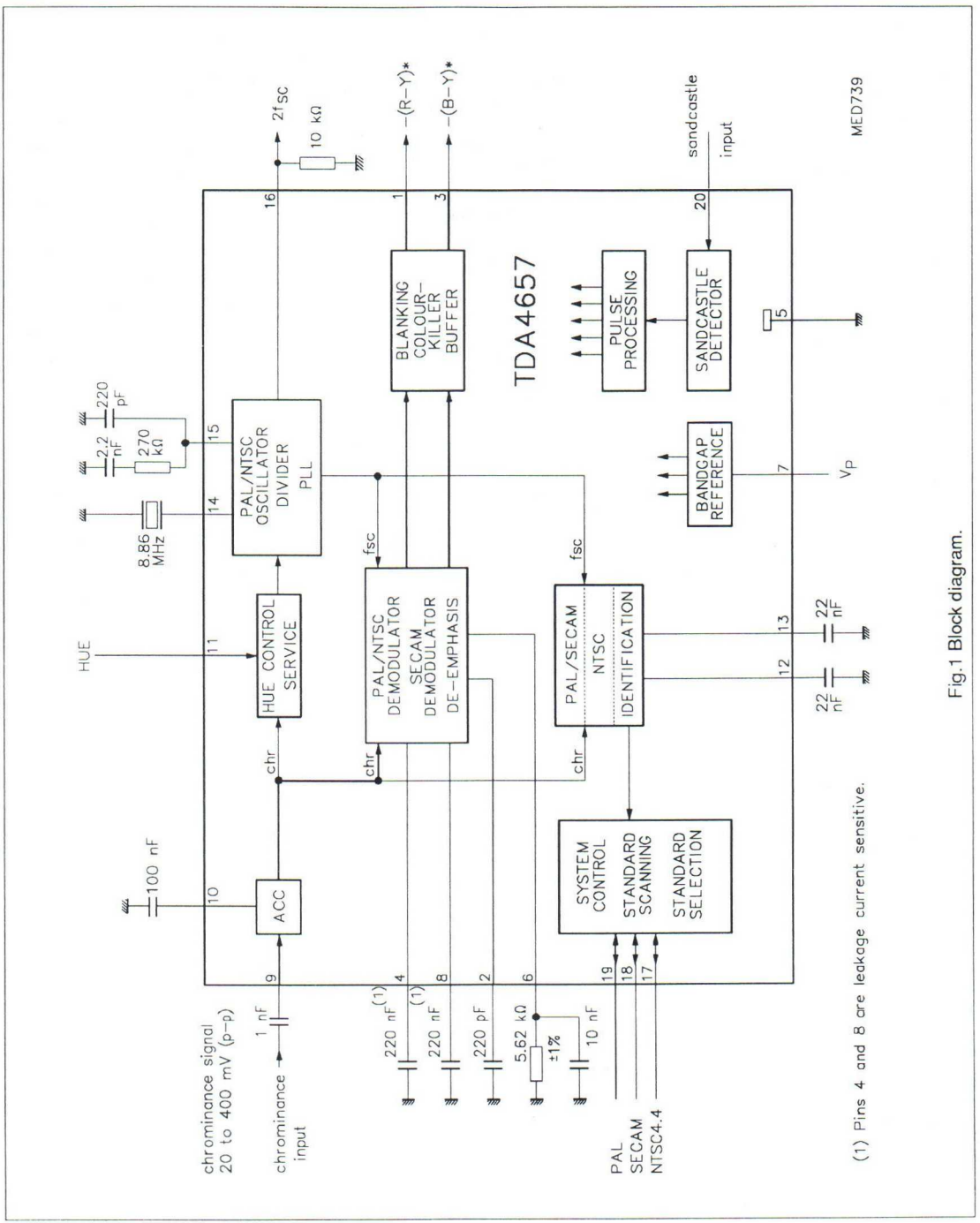


Fig.1 Block diagram.

(1) Pins 4 and 8 are leakage current sensitive.

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	colour difference signal output –(R–Y)* for baseband delay line
DEEM	2	external capacitor for SECAM de-emphasis
$-(B-Y)_O$	3	colour difference signal output –(B–Y)* for baseband delay line
CFOB	4	external capacitor SECAM demodulator control (B–Y) Channel
GND	5	ground
I_{REF}	6	external resistor for SECAM oscillator
V_P	7	supply 8 V
CFOR	8	external capacitor SECAM demodulator control (R–Y) Channel
CHR_I	9	chrominance signal input
C_{ACC}	10	external capacitor for ACC control
HUE	11	input for HUE control and service switch
N_{IDT}	12	external capacitor for identification circuit (NTSC)
P_{IDT}	13	external capacitor for identification circuit (PAL and SECAM)
OSC	14	PAL crystal
PLL	15	external loop filter
2FSC	16	2 x f_{SC} output
N_O	17	standard setting input/output for NTSC4.43
SEC_O	18	standard setting input/output for SECAM
PAL_O	19	standard setting input/output for PAL
SC	20	sandcastle input

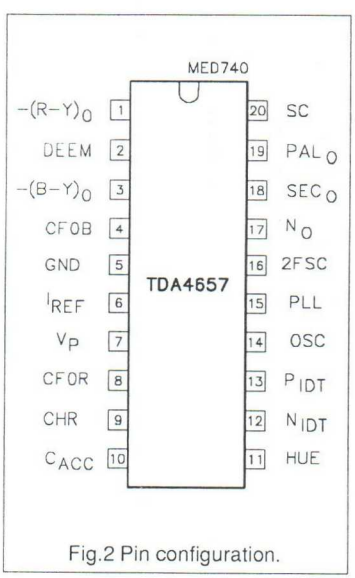


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The IC contains all functions required for the identification and demodulation of signals with the standards PAL, SECAM and NTSC4.3 with 4.43 MHz colour-carrier frequency. When an unknown signal is fed into the input, the circuit has to detect the standard of the signal, and has to switch on successively the appropriate input filter and demodulator and finally, after having identified the signal, it has to switch on the colour and, in event of NTSC reception, the hue control. At the outputs the two colour difference signals –(R–Y)* and –(B–Y)* are available.

ACC stage

The chrominance signal is fed into the asymmetrical input (pin 9) of the ACC stage (Automatic Colour Control). The input has to be AC coupled and has an input impedance of 20 kΩ in parallel with 10 pF.

To control the chrominance amplitude the modulation independent burst amplitude is measured during the burstkey pulse which is derived from the sandcastle pulse present at pin 20. The generated error current is fed into an external storage capacitor at pin 10. The integrated error voltage controls the gain of the ACC stage so that its output is independent of input signal variations.

The measurement is disabled during the vertical blanking to avoid failures because of missing burst signals.

Reference signal generation

The reference signal generation is achieved by a PLL system. The reference oscillator operates at twice the colour-carrier frequency and is locked on the burst of the chrominance signal (chr). A divider provides reference signals (f_{SC}) with the correct phase relationship for the PAL/NTSC demodulator and the identification part. In the SECAM mode the two f_0 frequencies are derived from the PAL crystal frequency by special dividers. In this mode the oscillator is not locked to the input signal. In the NTSC mode the hue control circuit is switched between ACC stage and PLL. The phase shift of the signal can be controlled by a DC voltage at pin 11. The hue control circuit is switched off during scanning.

The reference frequency (2 x f_{SC}) is available at pin 16 to drive a PAL comb filter for example.

Demodulation

The demodulation of the colour signal requires two demodulators. One is common for PAL and NTSC signals, the other is for SECAM signals.

The PAL/NTSC demodulator consists of two synchronized demodulators, one for the (B–Y) Channel and the other for the (R–Y) Channel. The required reference signals (f_{SC}) are input from the reference oscillator. In NTSC mode the PAL switch is disabled.

The SECAM demodulator consists of a PLL system. During vertical blanking the PLL oscillator is tuned to the f_0 frequencies to provide a fixed black level at the demodulator output. During demodulation the control voltages are stored in the external capacitors at pins 4 and 8.

The oscillator requires an external resistor at pin 6. Behind the PLL demodulator the signal is fed into the de-emphasis network which consists of two internal resistors (2.8 kΩ and 5.6 kΩ) and an external capacitor connected at pin 2 (220 pF).

After demodulation the signal is filtered and then fed into the next stage.

Blanking, colour killer, buffers

As a result of using only one demodulator in SECAM mode the demodulated signal has to be split up in the (B–Y) Channel and the (R–Y) Channel. The unwanted signals occuring every second line, (R–Y) in the (B–Y) Channel and (B–Y) in the (R–Y) Channel, have to be blanked. This happens in the blanking stage by an artificial black level being inserted alternately every second line.

To avoid disturbances during line and field flyback these parts of the colour differential signals are blanked in all modes.

When no signal has been identified, the colour is switched off (signals are blanked) by the colour killer.

At the end of the colour channels are low-ohmic buffers (emitter followers). The CD output signals –(B–Y)* and –(R–Y)* are available at pins 1 and 3.

Identification and system control

The identification part contains three identification demodulators.

The first demodulates in PAL mode. It is only active during the burstkey pulse. The reference signal (f_{SC}) has the (R–Y) phase.

The second demodulator (PLL system) operates in SECAM mode and is active also during the burstkey pulse, but delayed by 2 µs.

The PLL demodulator discriminates the frequency difference between the unmodulated f_0 frequencies of the incoming signal (chr) and the reference frequency input from the crystal oscillator.
These two demodulators are followed by an H/2 switch 'rectifying' the demodulated signal. The result is an identification signal (P_{IDT}, pin 13) that is positive for a PAL signal in PAL mode, for a SECAM signal in SECAM mode and for a PAL signal in NTSC4.4 mode. If P_{IDT} is positive in SECAM mode, the scanner switches back to the PAL mode in order to prevent a PAL signal being erroneously identified as a SECAM signal (PAL priority). If then P_{IDT} is not positive, the scanner returns to SECAM mode and remains there if P_{IDT} is positive again. In the event of a field frequency of 60 Hz the signal can not be identified as a SECAM signal, even if P_{IDT} is positive. In this event the scanner switches forward in the NTSC4.4 mode. If the H/2 signal has the wrong polarity, the identification signal is negative and the H/2 flip-flop is set to the correct phase.
The third demodulator operates in NTSC mode and is active during the burstkey pulse. The resulting identification signal (N_{IDT}, pin 12) is positive for PAL and NTSC4.4 signals in NTSC4.4 mode. The reference signal has the (B–Y) phase.
The two identification signals allow an unequivocal identification of the received signal. In the event of a signal being identified, the scanning is stopped and after a delay time the colour is switched on.
The standard outputs (active HIGH) are available at the pins 17, 18 and 19. During scanning the HIGH level is 2.5 V and when a signal has been identified the HIGH level is switched to 6 V. The standard pins can also be used as inputs in order to force the IC into a desired mode (Forced Standard Setting).

Sandcastle detector and pulse processing
In the sandcastle detector the super sandcastle pulse (SC) present at pin 20 is compared with three internal threshold levels by means of three differential amplifiers. The derived signals are the burstkey pulse, the horizontal blanking pulse and the combined horizontal and vertical blanking pulse. These signals are processed into various control pulses required for the timing of the IC.

Bandgap reference
In order to ensure that the CD output signals and the threshold levels of the sandcastle detector are independent of supply voltage variations a bandgap reference voltage has been integrated.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_P	supply voltage		–	8.8	V
P_{tot}	power dissipation	without load	–	330	mW
V_{20}	voltage at pin 20	I_{max} = 10 μA	–	15	V
	voltage at all other pins	I_{max} = 100 μA	–	V_P + V_{be}	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance on printed-circuit board from junction to ambient in free air (without heat spreader)	
	SO 20	90 K/W
	DIL 20	70 K/W

CHARACTERISTICS

Measured with application circuit (Fig.4) at T_{amb} = +25 °C, 8 V supply, 75% colour bar chrominance input signal of 200 mV (peak-to-peak value) and nominal phase for NTSC unless otherwise specified. All voltages measured referenced to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
I	supply current	V_P = 8.0 V without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V without load	–	248	296	mW
CD signal outputs (pins 1 and 3)						
PAL or NTSC						
V_1	colour difference output signals	independent of supply voltage; note 1				
	–(R–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		442	525	624	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		559	665	791	mV
V_1/V_3	ratio of CD signal amplitudes V(R–Y)/V(B–Y)	note 2	0.75	0.79	0.83	–
m	signal linearity –(R–Y) output	V_1 = 0.8 V (p-p)	0.8	–	–	–
	signal linearity –(B–Y) output	V_3 = 1.0 V (p-p)	0.8	–	–	–
f_g	cut-off frequency (both outputs)	–3 dB	–	1	–	MHz
t_d	chrominance delay time		220	270	320	ns
S/N	signal to noise ratio for nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs 1 x subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 x subcarrier frequency (peak-to-peak value)		–	–	30	mV
	H/2 content at R–Y output at nominal input signal (peak-to-peak value)		–	–	10	mV
A	crosstalk between CD Channels		–40	–	–	dB
R_1, R_3	output resistance (npn emitter follower)		–	–	200	Ω
I_1, I_3	output current		–	–	–3	mA
SECAM						
V_1	colour difference output signals	independent of supply voltage; note 4				
	–(R–Y) output (peak-to-peak value)		0.95	1.05	1.15	V
V_3	–(B–Y) output (peak-to-peak value)		1.20	1.33	1.46	V
V_1/V_3	ratio of CD signal amplitudes V(R–Y)/V(B–Y)		0.75	0.79	0.83	–
m	signal linearity at nominal output voltage		0.8	–	–	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_g	cut-off frequency	–3 dB	–	730	–	kHz
t_d	chrominance delay time		400	500	600	ns
S/N	signal to noise ratio for 100 mV (p-p) input signal and nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs: 1 x subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 x subcarrier frequency (peak-to-peak value)		–	–	20	mV
ΔV_3	shift of demodulated f_0 level relative to blanking level –(B–Y) output	note 8	–	0	±13	mV
ΔV_1	–(R–Y) output		–	0	±10	mV
Impedance and currents see PAL or NTSC specification						
Capacitor for SECAM de-emphasis (pin 2)						
C_2	value of external capacitor		–	220	–	pF
R_A	value of internal de-emphasis resistors	T_{amb} = 35 °C	2.4	2.8	3.2	kΩ
R_B			4.8	5.6	6.4	kΩ
$\Delta(R_A/R_B)$	relative tolerance of de-emphasis resistors		–	–	±5	%
Capacitors for SECAM demodulator control (pins 4 and 8; note 5)						
$\Delta V_{1,3}$	shift of demodulated f_0 level due to external leakage current	C_{ext} = 220 nF	–	–	0.3	mV/nA
Resistor for SECAM oscillator (pin 6)						
V_6	DC voltage		2.4	2.81	3.2	V
R_6	value of external resistor (±1%)		–	5.62	–	kΩ
C_6	value of external capacitor (±20%)		–	10	–	nF
Chrominance input (pin 9)						
V_9	input signal (peak-to-peak value)	note 6	20	200	400	mV
R_9	input resistance		16	20	24	kΩ
C_9	input capacitance		–	–	10	pF
Capacitor for ACC (pin 10; note 7)						
$\Delta V_{1,3}$	change of CD output signals during field blanking due to external leakage current	C_{ext} = 100 nF	–	0.2	–	%/nA
Hue control (NTSC) and service switch (pin 11)						
ϕ	phase shift of reference carrier relative to phase at open-circuit pin 11	V_{11} = 3 V	–30	–	–	degree
		V_{11} = open-circuit	–5	0	+5	degree
		V_{11} = 5 V	+30	–	–	degree
V_{11}	internal bias voltage (proportional to supply voltage)	pin 11 open-circuit	3.8	4.0	4.2	V
R_{11}	input resistance		25	30	35	kΩ
Capacitor for identification (pins 12 and 13)						
V_{12}, V_{13}	DC voltage for an identified signal		2.8	3.2	3.5	V
	DC voltage for an unidentified signal		1.5	2.0	2.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL oscillator measured with nominal crystal (pin 14; see Table 1)						
R_{14}	initial oscillator amplifier input resistance		−500	–	–	Ω
C_{14}	oscillator amplifier input capacitance		–	–	10	pF
Δf_L	lock-in-range referenced to 4.43361875 MHz	note 9	±400	–	±1300	Hz
ϕ	phase difference for ±400 Hz deviation of colour carrier frequency		–	–	1	degree
2 x fsc output (pin 16; if the output is not used, the pin should be connected to supply)						
V_{16}	DC output level	I_{16} = 0 A	6.1	6.3	6.5	V
R_{16}	output resistance	I_{16} = 0 A	–	–	350	Ω
I_{16}	output current		–	–	−1.0	mA
V_{16}	output signal (peak-to-peak value)		–	250	–	mV
Standard setting inputs/outputs (pins 17 to 19; note 10)						
used as output: npn emitter follower output with 0.1 mA source to ground						
V_O	on-state, during scanning, colour OFF		2.3	2.5	2.7	V
	on-state, colour ON		5.8	6.0	6.2	V
R_O	output resistance	I_O = 0	–	–	300	Ω
I_O	output current		–	–	−3	mA
used as input: forced system switching						
V_O	threshold for system ON		6.8	7.0	7.2	V
I_O	input current		100	150	180	μA
Sandcastle pulse detector (pin 20; note 11)						
C_{20}	input capacitance		–	–	10	pF
V_{20}	thresholds for field and line pulse separation	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	line pulse separation	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	burst pulse separation	pulse ON	5.3	5.6	5.9	V
		pulse OFF	5.1	5.4	5.7	V
System control processing (note 12)						
t_d	system hold delay	in event of a signal disappearing for a short time	2	–	3	field periods
	colour killer; colour ON delay	switching occurs during field blanking	2	–	3	field periods
	colour OFF delay		0	–	1	field periods
t_s	scanning time for each system		–	4	–	field periods

QUALITY SPECIFICATION

URV-4-2-59/601

Notes to the characteristics

1. Burstkey width 4.3 µs.
   Burst width 2.25 µs, ratio burst chrominance amplitude 1/2.2.
2. At nominal phase of hue control.
3. V (p-p) of signal divided by 6 times effective noise voltage.
4. H/2 blanking alternately every second line.
5. These pins are leakage current sensitive. Pin 4 for (B–Y) Channel, pin 8 for (R–Y) Channel.
6. Within 2 dB output voltage deviation.
7. This pin is leakage current sensitive.
8. IC only.
9. Depends also on network on pin 15.
10. Pin 19 for PAL, pin 18 for SECAM, pin 17 for NTSC 4.43 MHz.
    Threshold levels are dependent of supply.
11. The field interval of the sandcastle has to be adapted to the ICs TDA2579B and TDA4690.
    The thresholds are independent of supply voltage.
12. System scanning sequence: PAL, SECAM, NTSC4.4.

Table 1 Specification of quartz crystals in HC-49/U13 holder; standard application.

SYMBOL	PARAMETER	VALUE	UNIT
		9922 520 00385	
f_n	nominal frequency	8.867570	MHz
C_L	load capacitance	series resonance	
Δf_n	adjustment tolerance of f_n at +25 °C	±20	ppm
R_r	resonance resistance over temperature range	≤ 60	Ω
$R_{dld\ max}$	in the drive level range between 10^{-12} W and 1.0 x 10^{-3} W, the resonance resistance may not exceed (at +25 °C) the value of $R_{dld\ max}$	tbn	Ω
R_n	resonance resistance of unwanted response	$2R_{r\ (+25\ °C)}$	Ω
C_1	motional capacitance (±20%)	14.0	fF
C_0	parallel capacitance (±20%)	3.6	pF
T_{amb}	operating ambient temperature	–10 to +60	°C
Δf_n	frequency tolerance over temperature	±20	ppm

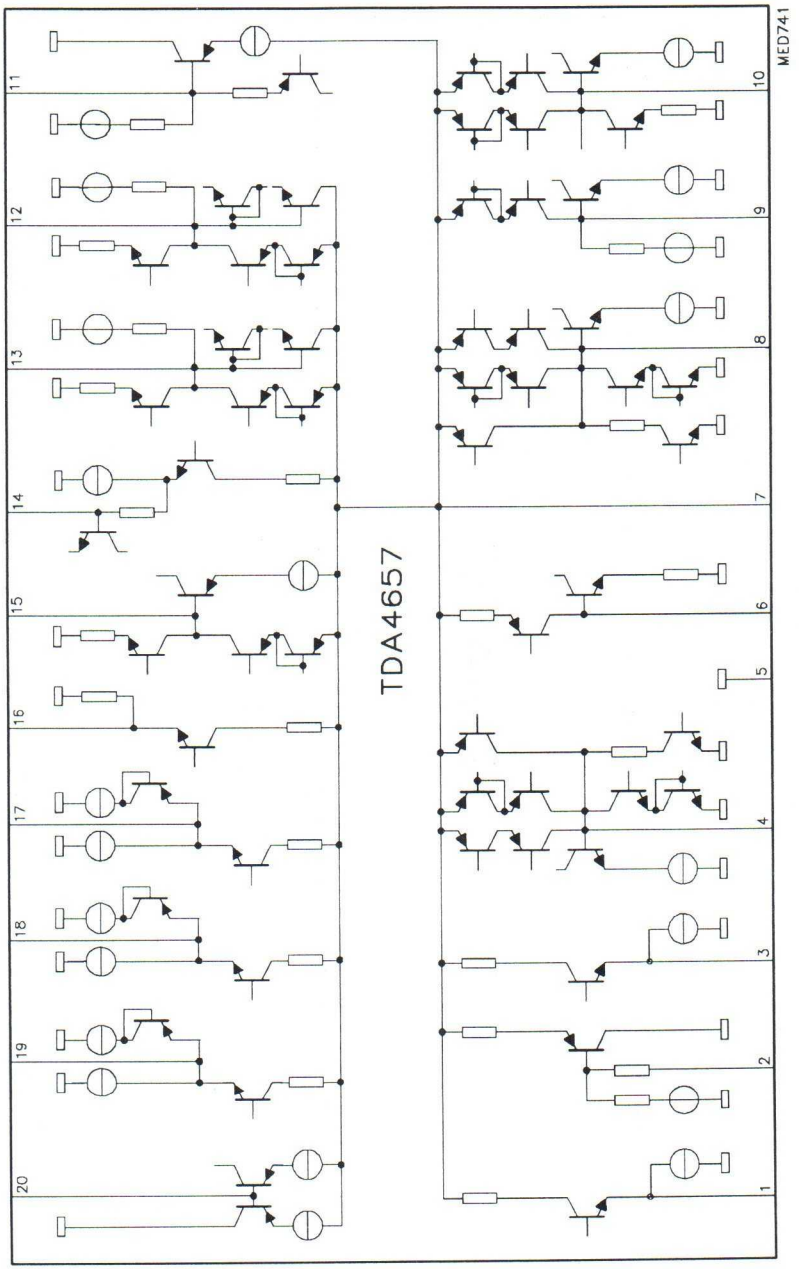


Fig.3 Internal circuits.

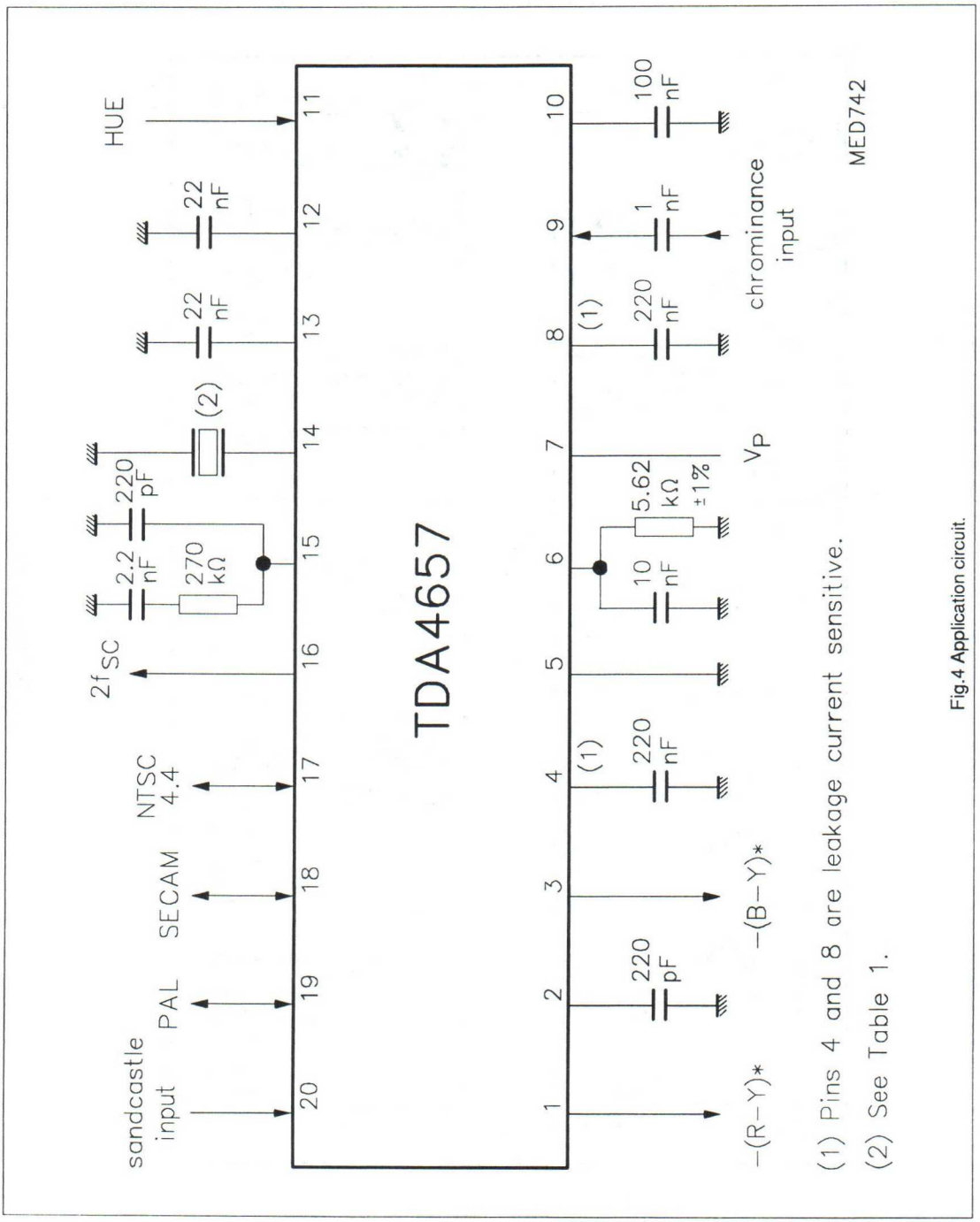


Fig.4 Application circuit.

Baseband delay line TDA4661

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 μs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 μs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour.

GENERAL DESCRIPTION

The TDA4661 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	6	V
$I_{P(tot)}$	total supply current	–	4.9	7.0	mA
V_I	±(R–Y) input signal PAL/NTSC (peak-to-peak value; pin 16)	–	525	–	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value; pin 14)	–	665	–	mV
	±(R–Y) input signal SECAM (peak-to-peak value; pin 16)	–	1.05	–	V
	±(B–Y) input signal SECAM (peak-to-peak value; pin 14)	–	1.33	–	V
G_v	gain V_O / V_I of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{11} / V_{16} for SECAM	–0.6	–0.1	+0.4	dB
	V_{12} / V_{14} for SECAM	–0.6	–0.1	+0.4	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4661	DIP16	plastic dual in-line package; 16 leads (300 mil) long body	SOT38-4
TDA4661T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

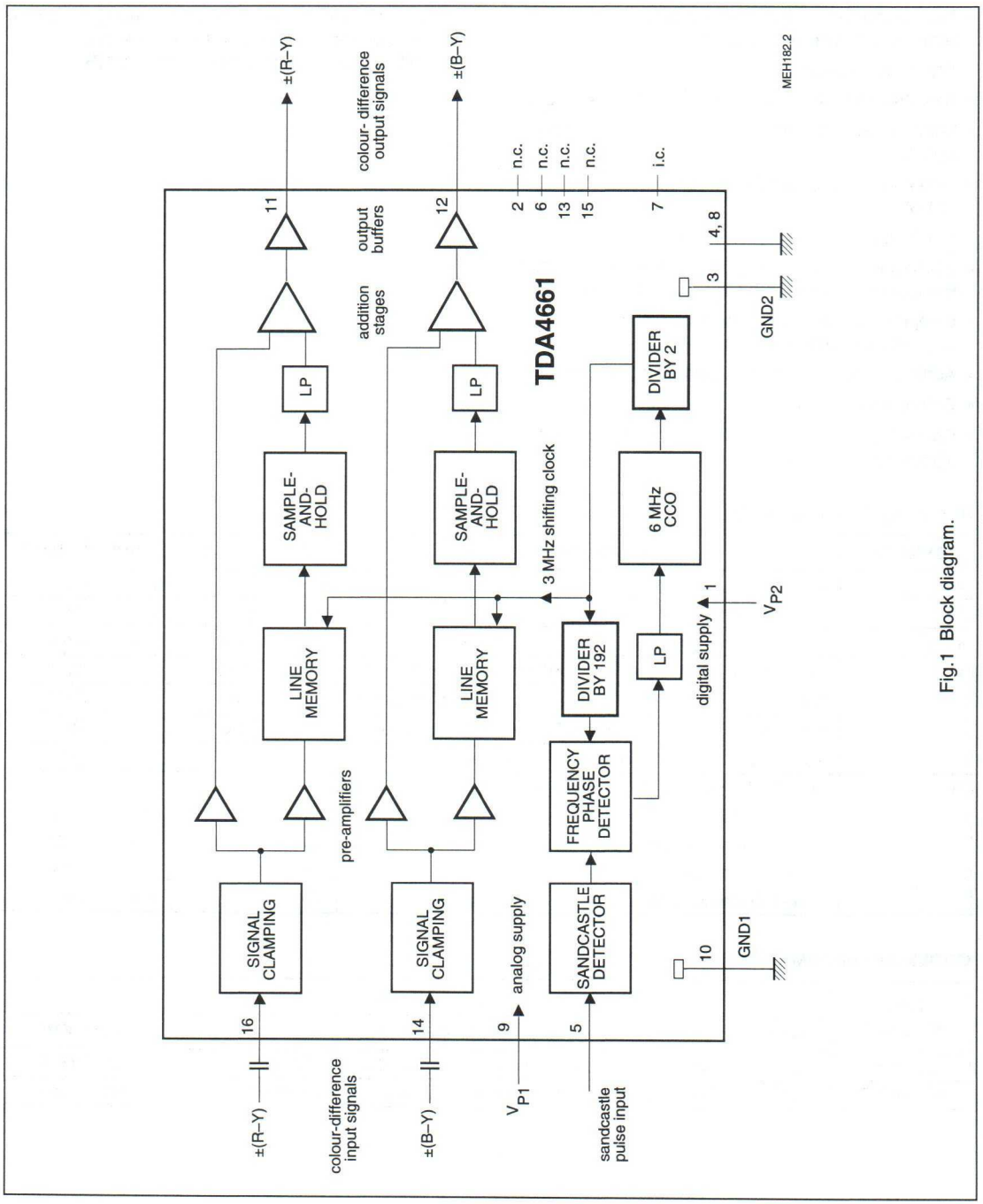


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{O(R-Y)}$	11	±(R–Y) output signal
$V_{O(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{I(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{I(R-Y)}$	16	±(R–Y) input signal

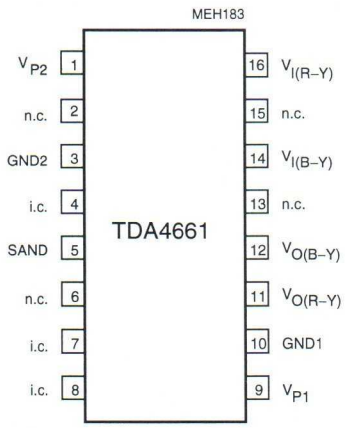


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	−0.5	+7	V
V_{P2}	supply voltage (pin 1)	−0.5	+7	V
V_5	voltage on pin 5	−0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	−0.5	V_P	V
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−	±500	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R_{thj-a}	thermal resistance from junction to ambient in free air		
	SOT38-4	75	K/W
	SOT109-1	220	K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = +25 °C; measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part; pin 9)		4.5	5	6	V
V_{P2}	supply voltage (digital part; pin 1)		4.5	5	6	V
I_{P1}	supply current		–	4.2	6.0	mA
I_{P2}	supply current		–	0.7	1.0	mA
Colour-difference input signals						
V_I	input signal (peak-to-peak value)					
	±(R–Y) PAL and NTSC (pin 16)		–	525	–	mV
	±(B–Y) PAL and NTSC (pin 14)		–	665	–	mV
	±(R–Y) SECAM (pin 16)	note 1	–	1.05	–	V
	±(B–Y) SECAM (pin 14)	note 1	–	1.33	–	V
$V_{I(max)}$	maximum symmetrical input signal (peak-to-peak value)					
	±(R–Y) or ±(B–Y) for PAL and NTSC	before clipping	1	–	–	V
	±(R–Y) or ±(B–Y) for SECAM	before clipping	2	–	–	V
$R_{14, 16}$	input resistance		–	–	40	kΩ
$C_{14, 16}$	input capacitance		–	–	10	pF
$V_{14, 16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
V_O	output signal (peak-to-peak value)					
	±(R–Y) on pin 11	all standards	–	1.05	–	V
	±(B–Y) on pin 12	all standards	–	1.33	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{I14, 16}$ = 1.33 V (p-p)	–0.4	0	+0.4	dB
$V_{11, 12}$	DC output voltage	proportional to V_P	2.5	2.9	3.3	V
$R_{11, 12}$	output resistance		–	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_O/V_I	5.3	5.8	6.3	dB
	gain for SECAM	ratio V_O/V_I	–0.6	–0.1	+0.4	dB
V_n/V_{n+1}	ratio of output signals on pins 11 and 12 for adjacent time samples at constant input signals	$V_{I14, 16}$ = 1.33 V (p-p); SECAM signals	–0.1	0	+0.1	dB
V_n	noise voltage (RMS value; pins 11 and 12)	$V_{I14, 16}$ = 0 V; note 2	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_O = 1 V (p-p); note 2	–	54	–	dB
t_d	delay of delayed signals		63.94	64.0	64.06	µs
	delay of non-delayed signals		40	60	80	ns
t_{tr}	transient time of delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	350	–	ns
	transient time of non-delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	320	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency		14.2	15.625	17.0	kHz
f_{SAND}	sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 3	4.0	–	$V_P + 1.0$	V
V_{slice}	internal slicing level		$V_5 - 1.0$	–	$V_5 - 0.5$	V
I_5	input current		–	–	10	μA
C_5	input capacitance		–	–	10	pF

Notes

1. The signal must be blanked line-sequentially. The blanking level must be equal to the non-colour signal.
2. Noise voltage at f = 10 kHz to 1 MHz; $V_{I14, 16} = 0$ ($R_S < 300\ \Omega$).
3. The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

APPLICATION INFORMATION

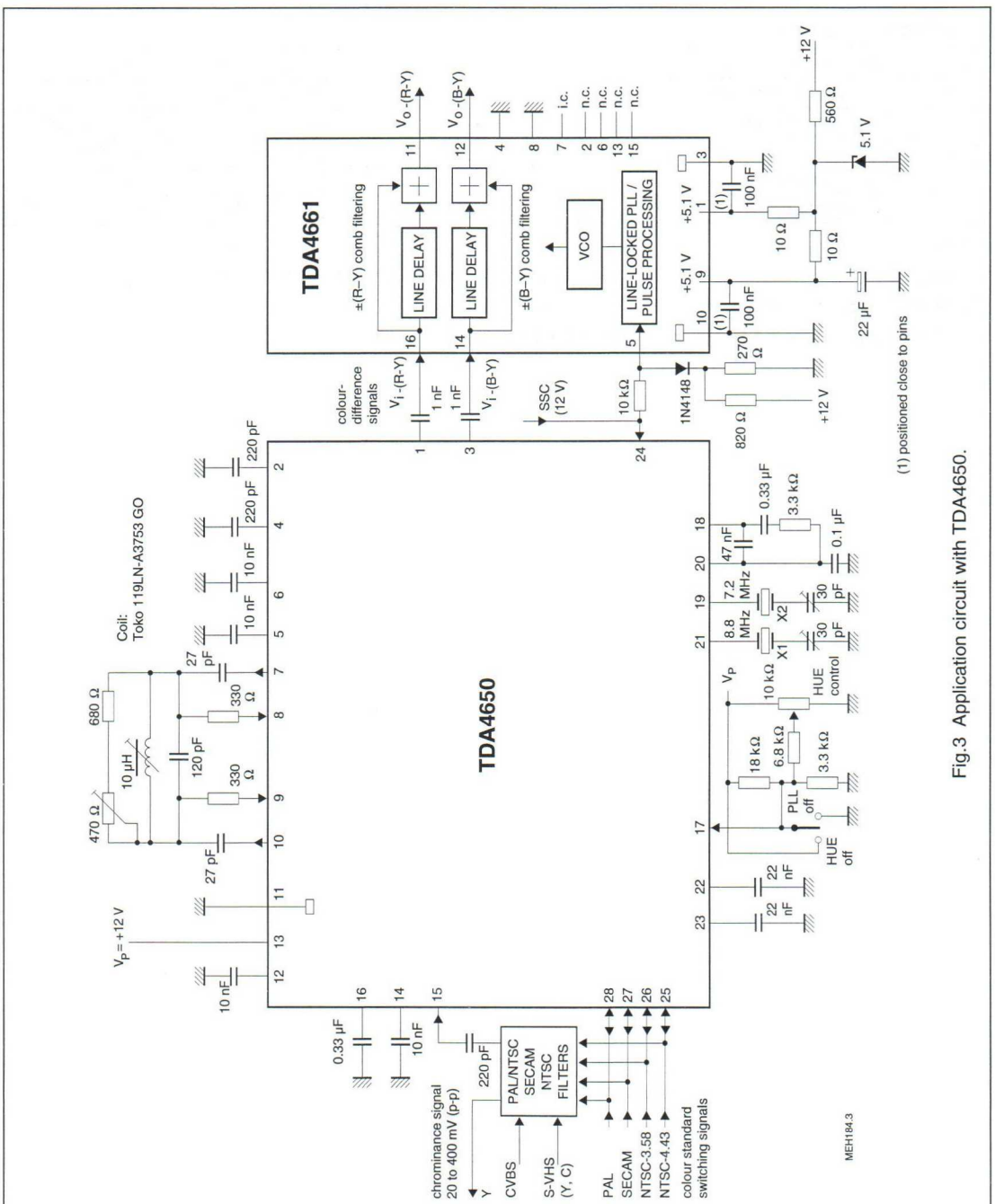


Fig.3 Application circuit with TDA4650.

Baseband delay line TDA4662

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 µs)
- For PAL and NTSC
- Adjustment-free application
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 µs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross colour.

GENERAL DESCRIPTION

The TDA4662 is an integrated baseband delay line circuit with one line delay. It is suitable for PAL and NTSC decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	5.6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	5.6	V
$I_{P\,tot}$	total supply current	–	5.9	7.0	mA
V_i	±(R–Y) input signal PAL/NTSC (peak-to-peak value, pin 16)	–	525	–	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value, pin 14)	–	665	–	mV
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4662	16	DIL	plastic	SOT38-4
TDA4662T	16	mini-pack	plastic	SOT109A

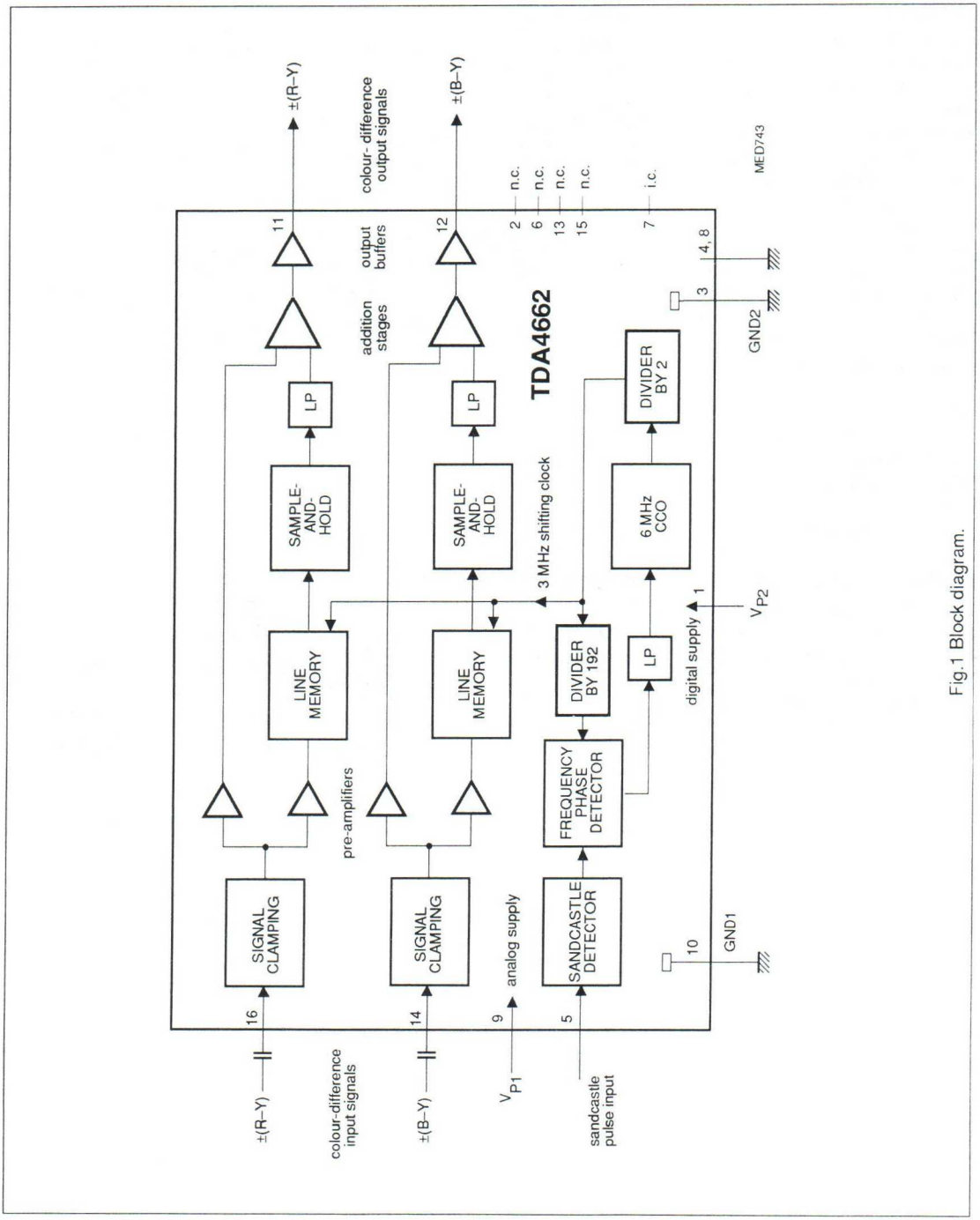


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o\,(R-Y)}$	11	±(R–Y) output signal
$V_{o\,(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i\,(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i\,(R-Y)}$	16	±(R–Y) input signal

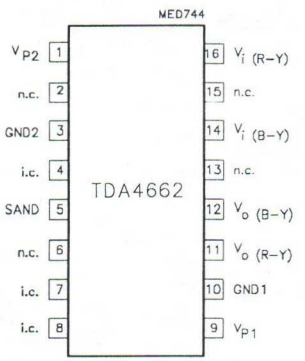


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	–0.5	+7	V
V_{P2}	supply voltage (pin 1)	–0.5	+7	V
V_5	voltage on pin 5	–0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	–0.5	V_P	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j-a}$	from junction to ambient in free air	
	SOT38-4	75 K/W
	SOT109A	220 K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = +25 °C, measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part, pin 9)		4.5	5	5.6	V
V_{P2}	supply voltage (digital part, pin 1)		4.5	5	5.6	V
I_{P1}	supply current		–	5.4	6.2	mA
I_{P2}	supply current		–	0.8	1.1	mA
Colour-difference input signals						
V_i	input signal (peak-to-peak value)					
	±(R–Y) PAL and NTSC (pin 16)		–	525	–	mV
	±(B–Y) PAL and NTSC (pin 14)		–	665	–	mV
$V_{i\,max}$	maximum symmetrical input signal (peak-to-peak value)					
	±R–Y for PAL and NTSC	before clipping	660	–	–	mV
	±B–Y for PAL and NTSC	before clipping	840	–	–	mV
$R_{14,16}$	input resistance		–	–	40	kΩ
$C_{14,16}$	input capacitance		–	–	10	pF
$V_{14,16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
V_o	output signal (peak-to-peak value)					
	±(R–Y) on pin 11		–	1.05	–	V
	±(B–Y) on pin 12		–	1.33	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i\,14,16}$ = 665 mV (p-p)	–0.4	0	+0.4	dB
$V_{11,12}$	DC output voltage	proportional to V_P	2.90	3.10	3.30	V
$R_{11,12}$	output resistance		–	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_o/V_i	5.3	5.8	6.3	dB
V_n	noise voltage (RMS value, pins 11 and 12)	$V_{i\,14,16}$ = 0 V; note 1	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_o = 840 mV (p-p); note 1	–	52	–	dB
t_d	line delay		63.94	64.0	64.06	ns
	additional processing delay for delayed and non-delayed signals		40	60	80	ns
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency / sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 2	4.0	–	V_P + 1.0	V
V_{slice}	internal slicing level		V_5 – 1.0	–	V_5 – 0.5	V
I_5	input current		–	–	10	µA
C_5	input capacitance		–	–	10	pF

Notes to the characteristics

1. Noise voltage at f = 10 kHz to 1 MHz; $V_{i\,14,16}$ = 0 (R_S < 300 Ω).
2. The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

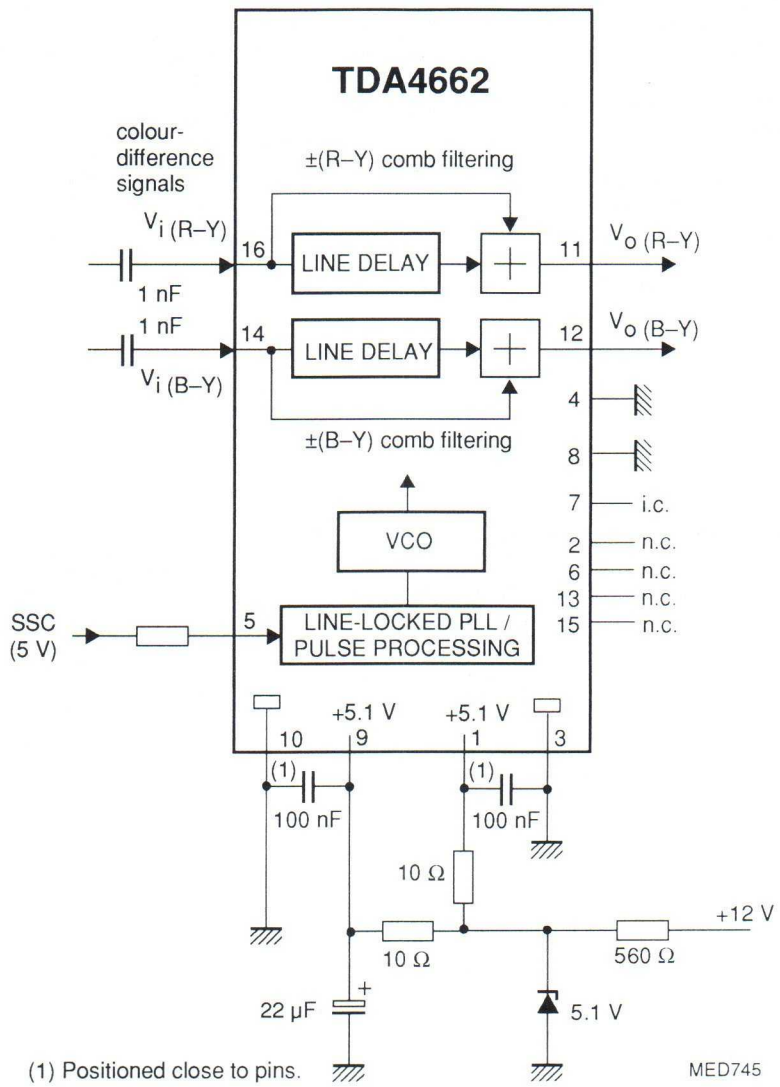


Fig.3 Application circuit.

Baseband delay line TDA4663

FEATURES

- Two delay lines, using the switched-capacitor technique, for a delay time of 1H –55 ns
- Adjustment-free application
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (mostly colour-difference signals ±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 µs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Output buffer amplifiers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.75	5	5.25	V
V_{P2}	digital supply voltage (pin 1)	4.75	5	5.25	V
$I_{P\ tot}$	total supply current	–	5.9	7.0	mA
V_i	±(R–Y) input signal PAL/NTSC (peak-to-peak value, pin 16)	–	1.3	–	V
	±(B–Y) input signal PAL/NTSC (peak-to-peak value, pin 14)	–	1.3	–	V
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	–1	0	+1	dB
	V_{12} / V_{14} for PAL and NTSC	–1	0	+1	dB

GENERAL DESCRIPTION

The TDA4663 is an integrated baseband delay line circuit with a delay time of 1H –55 ns.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4663T	16	SO16	plastic	SOT109A

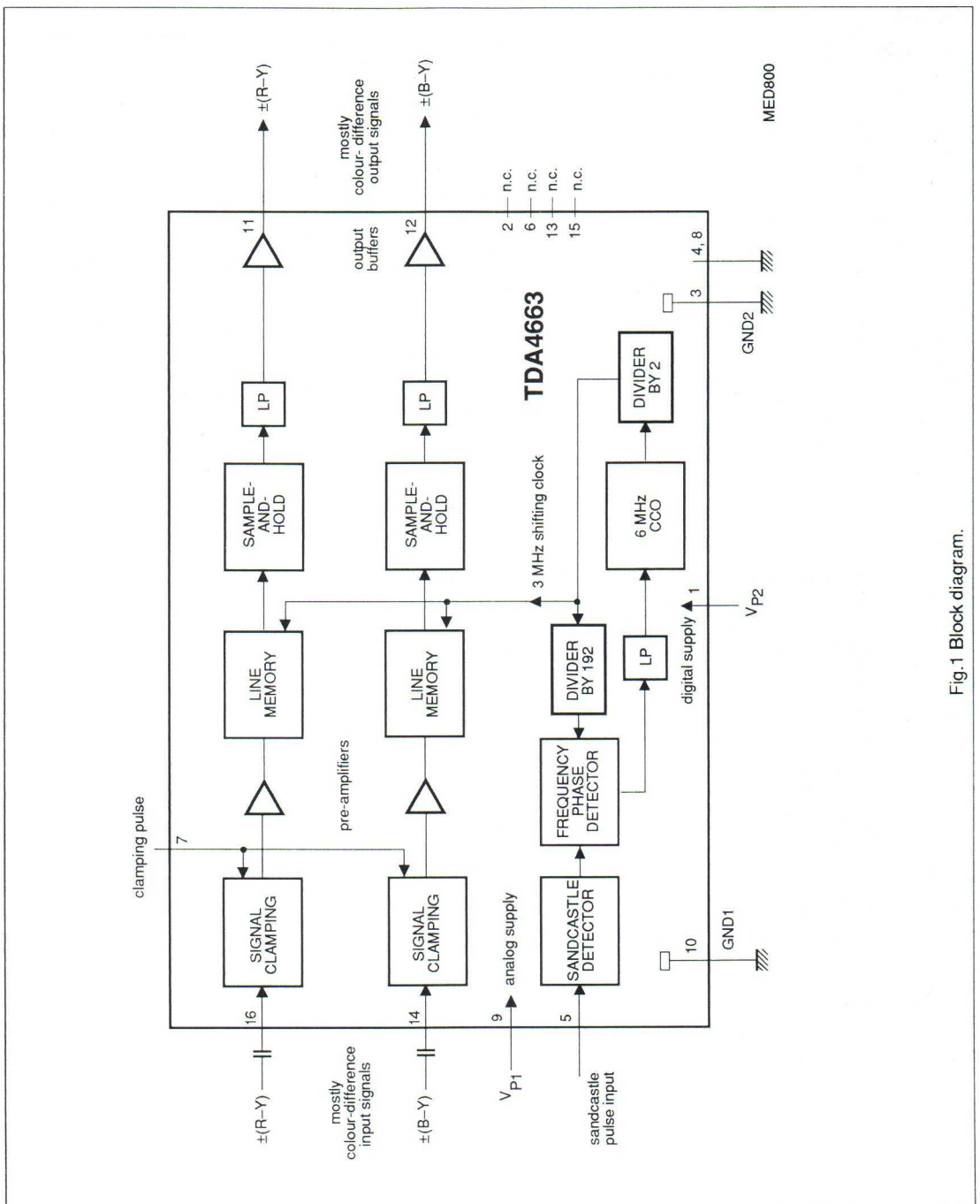


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
V_{CL}	7	clamping pulse input
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o\,(R-Y)}$	11	±(R–Y) output signal
$V_{o\,(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i\,(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i\,(R-Y)}$	16	±(R–Y) input signal

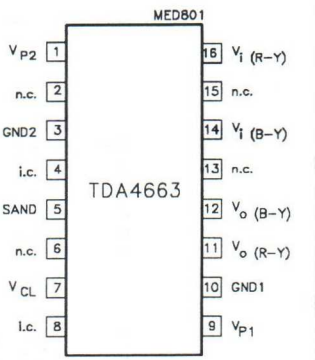


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	–0.5	+7	V
V_{P2}	supply voltage (pin 1)	–0.5	+7	V
V_5	voltage at pin 5	–0.5	V_P + 1.0	V
V_n	voltage at pins 7, 11, 12, 14 and 16	–0.5	V_P	V
I_n	current at pins 7, 11 and 12	–	20	mA
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
P_{tot}	total power dissipation	–	100	mW
V_{ESD}	electrostatic handling for all pins (note 1)	–	±500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j-a}$	from junction to ambient in free air	220 K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = +25 °C, measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part, pin 9)		4.75	5	5.25	V
V_{P2}	supply voltage (digital part, pin 1)		4.75	5	5.25	V
I_{P1}	supply current		–	5.1	5.9	mA
I_{P2}	supply current		–	0.8	1.1	mA
Colour-difference input signals						
V_i	input signal (peak-to-peak value)					
	pin 16		–	1.3	–	V
	pin 14		–	1.3	–	V
$V_{i\,max}$	maximum symmetrical input signal (peak-to-peak value)					
	pin 16	before clipping	1.6	–	–	V
	pin 14	before clipping	1.6	–	–	V
$I_{14,16}$	input leakage current (during picture content)		0.06	0.085	0.1	µA
$R_{14,16}$	input resistance		–	–	40	kΩ
$C_{14,16}$	input capacitance		–	–	10	pF
$V_{14,16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
V_o	output signal (peak-to-peak value)					
	pin 11		–	1.3	–	V
	pin 12		–	1.3	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i\,14,16}$ = 665 mV (p-p)	–0.4	0	+0.4	dB
$V_{11,12}$	DC output voltage	proportional to V_P	2.90	3.10	3.30	V
$R_{11,12}$	output resistance		–	300	400	Ω
G_v	gain	ratio V_o/V_i	–1	0	+1	dB
V_n	noise voltage (RMS value, pins 11 and 12)	$V_{i\,14,16}$ = 0 V; note 1	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_o = 840 mV (p-p); note 1	–	52	–	dB
t_j	jitter of output signal to external sandcastle reference V_5		–	–	20	ns
V_{11}/V_{12}	crosstalk between channels	V_{14} = 0 V; R_s = 300 Ω; V_{11} = 1.35 V (p-p)	30	–	–	dB
V_{12}/V_{11}		V_{16} = 0 V; R_s = 300 Ω; V_{12} = 1.35 V (p-p)	30	–	–	dB
V_{14}/V_{12}	crosstalk direct from input to output signal	V_{16} = 0 V; R_s = 300 Ω; V_{14} = 1.35 V (p-p)	30	–	–	dB
V_{16}/V_{11}		V_{14} = 0 V; R_s = 300 Ω; V_{16} = 1.35 V (p-p)	30	–	–	dB
$\Delta V_{11,12}/V_R$	supply ripple rejection	V_R = 100 mV (p-p); f_R = 10 Hz to 1 kHz; $V_{11,12}$ = 1.35 V (p-p)	34	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{11, 12}$	clamping offset during H-clamp (peak-to-peak value)	$V_{14} = V_{16} = 0$ V; $R_S = 300\ \Omega$	–	–	5	mV
$V_{11, 12}$	unwanted signals (line-locked) (peak-to-peak value)	$V_{14} = V_{16} = 0$ V; active video; $R_S = 300\ \Omega$				
	residual clock (3 MHz)		–	–	6.25	mV
	meander		–	–	1.5	mV
	needles		–	–	2.5	mV
t_d	line delay	for PAL signals	64 – 0.125	64 – 0.055	64 + 0.015	µs
		for NTSC signals	63.555 – 0.125	63.555 – 0.055	63.555 + 0.015	µs
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency / sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 2	4.0	–	$V_P + 1.0$	V
t_{BK}	top pulse duration		–	2.5	–	µs
V_{slice}	internal slicing level		$V_5 - 1.0$	–	$V_5 - 0.5$	V
I_5	input current		–	–	10	µA
C_5	input capacitance		–	–	10	pF
t_{li}	lock-in time for PLL		–	–	1	ms
Clamping pulse input (pin 7)						
V_7	clamping pulse ON clamping pulse OFF		3.5 –0.5	$V_P - 0.1$ 0.1	V_P +1.5	V V
I_7	input current		–	–	10	µA
C_7	input capacitance		–	–	10	pF
t_7	clamping pulse duration		0.1	2	3	µs
t_{rf7}	rise and fall time		10	–	–	ns

Notes to the characteristics

1. Noise voltage at f = 10 kHz to 1 MHz; $V_{i\ 14, 16} = 0$ ($R_S < 300\ \Omega$).
2. The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

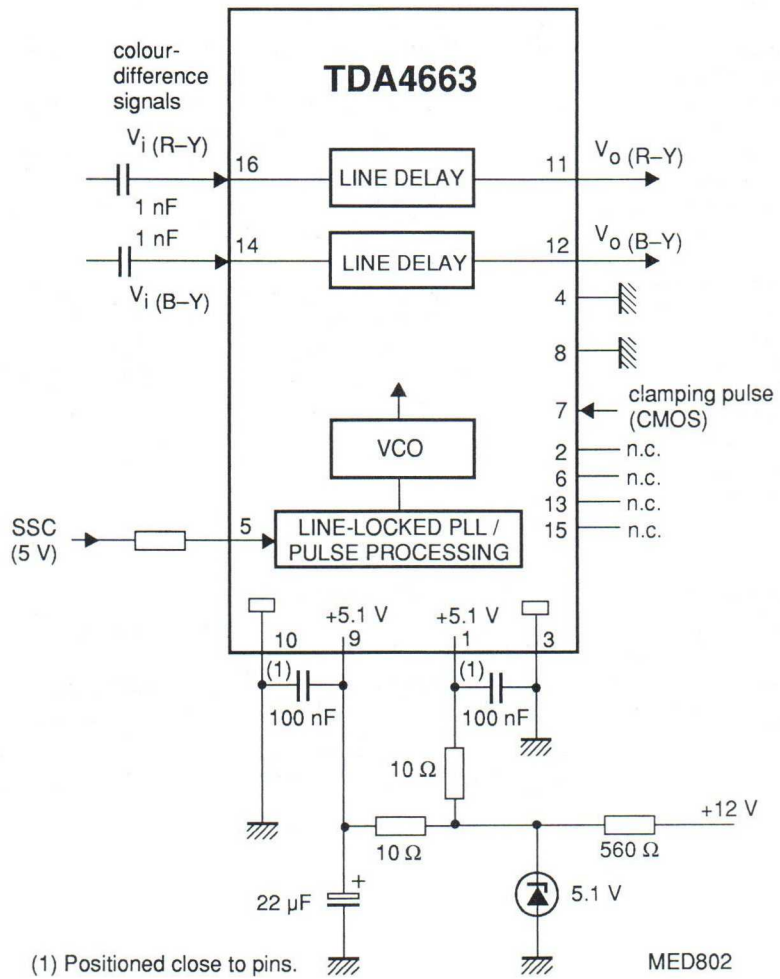


Fig.3 Application circuit.

Baseband delay line TDA4665

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 µs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 µs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	6	V
$I_{P\ tot}$	total supply current	–	5.9	7.0	mA
V_i	±(R–Y) input signal PAL/NTSC (peak-to-peak value, pin 16)	–	525	–	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value, pin 14)	–	665	–	mV
	±(R–Y) input signal SECAM (peak-to-peak value, pin 16)	–	1.05	–	V
	±(B–Y) input signal SECAM (peak-to-peak value, pin 14)	–	1.33	–	V
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{11} / V_{16} for SECAM	–0.6	–0.1	+0.4	dB
	V_{12} / V_{14} for SECAM	–0.6	–0.1	+0.4	dB

GENERAL DESCRIPTION

The TDA4665 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4665	16	DIL	plastic	SOT38-4
TDA4665T	16	mini-pack	plastic	SOT109A

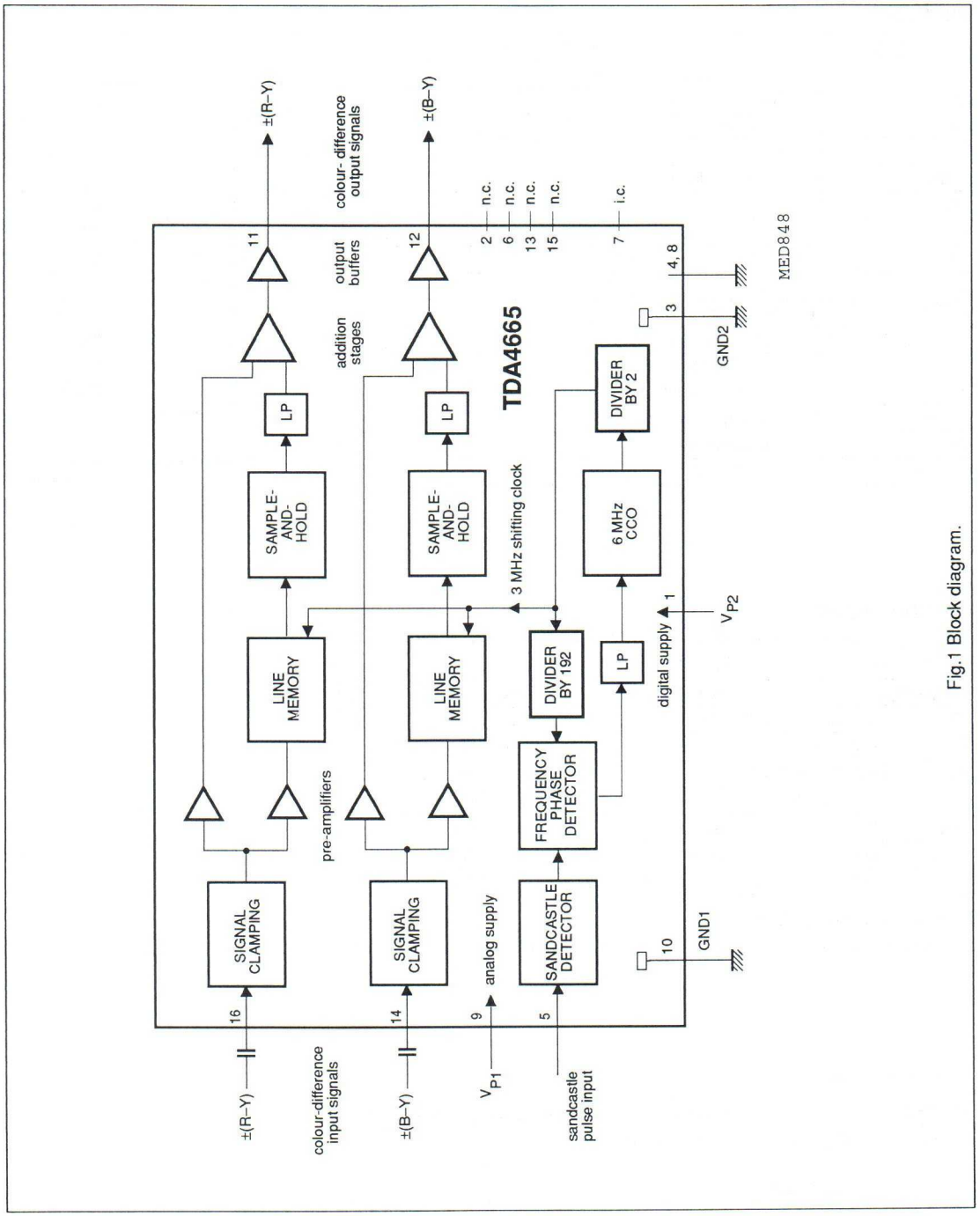


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o\,(R-Y)}$	11	±(R–Y) output signal
$V_{o\,(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i\,(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i\,(R-Y)}$	16	±(R–Y) input signal

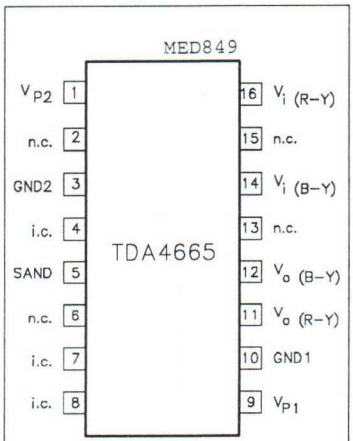


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	–0.5	+7	V
V_{P2}	supply voltage (pin 1)	–0.5	+7	V
V_5	voltage on pin 5	–0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	–0.5	V_P	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j-a}$	from junction to ambient in free air	
	SOT38-4	75 K/W
	SOT109A	220 K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = +25 °C, measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part, pin 9)		4.5	5	6	V
V_{P2}	supply voltage (digital part, pin 1)		4.5	5	6	V
I_{P1}	supply current		–	5.2	6.0	mA
I_{P2}	supply current		–	0.7	1.0	mA
Colour-difference input signals						
V_i	input signal (peak-to-peak value; note 1)					
	±(R–Y) PAL and NTSC (pin 16)		–	525	–	mV
	±(B–Y) PAL and NTSC (pin 14)		–	665	–	mV
	±(R–Y) SECAM (pin 16)		–	1.05	–	V
	±(B–Y) SECAM (pin 14)		–	1.33	–	V
$V_{i\,max}$	maximum symmetrical input signal (peak-to-peak value)					
	±(R–Y) or ±(B–Y) for PAL and NTSC	before clipping	1	–	–	V
	±(R–Y) or ±(B–Y) for SECAM	before clipping	2	–	–	V
$R_{14,16}$	input resistance		–	–	40	kΩ
$C_{14,16}$	input capacitance		–	–	10	pF
$V_{14,16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
V_o	output signal (peak-to-peak value)					
	±(R–Y) on pin 11	all standards	–	1.05	–	V
	±(B–Y) on pin 12	all standards	–	1.33	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i\,14,16}$ = 1.33 V (p-p)	–0.4	0	+0.4	dB
$V_{11,12}$	DC output voltage	proportional to V_P	2.90	3.10	3.30	V
$R_{11,12}$	output resistance		–	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_o/V_i	5.3	5.8	6.3	dB
	gain for SECAM	ratio V_o/V_i	–0.6	–0.1	+0.4	dB
V_n/V_{n+1}	ratio of output signals on pins 11 and 12 for adjacent time samples at constant input signals	$V_{i\,14,16}$ = 1.33 V (p-p); SECAM signals	–0.1	0	+0.1	dB
V_n	noise voltage (RMS value, pins 11 and 12)	$V_{i\,14,16}$ = 0 V; note 2	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_o = 1 V (p-p); f = tbn	–	54	–	dB
t_d	delay of delayed signals		63.94	64.0	64.06	µs
	delay of non-delayed signals		40	60	80	ns
t_{tr}	transient time of delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	350	–	ns
	transient time of non-delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	320	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency / sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 3	4.0	–	$V_P + 1.0$	V
V_{slice}	internal slicing level		$V_5 - 1.0$	–	$V_5 - 0.5$	V
I_5	input current		–	–	10	μA
C_5	input capacitance		–	–	10	pF

Notes to the characteristics

1. For SECAM the signal must be blanked line-sequentially. The blanking level must be equal to the non-colour signal. For SECAM, PAL and NTSC the input signal must be equal to the non-colour signal during the internal clamping of TDA4665 (3 μs to 1 μs before the leading edge of the top pulse of V_5.
2. Noise voltage at f = 10 kHz to 1 MHz; $V_{i\,14,\,16} = 0$ ($R_S < 300\ \Omega$).
3. The leading edge of the burst-key pulse or top pulse is used for timing.

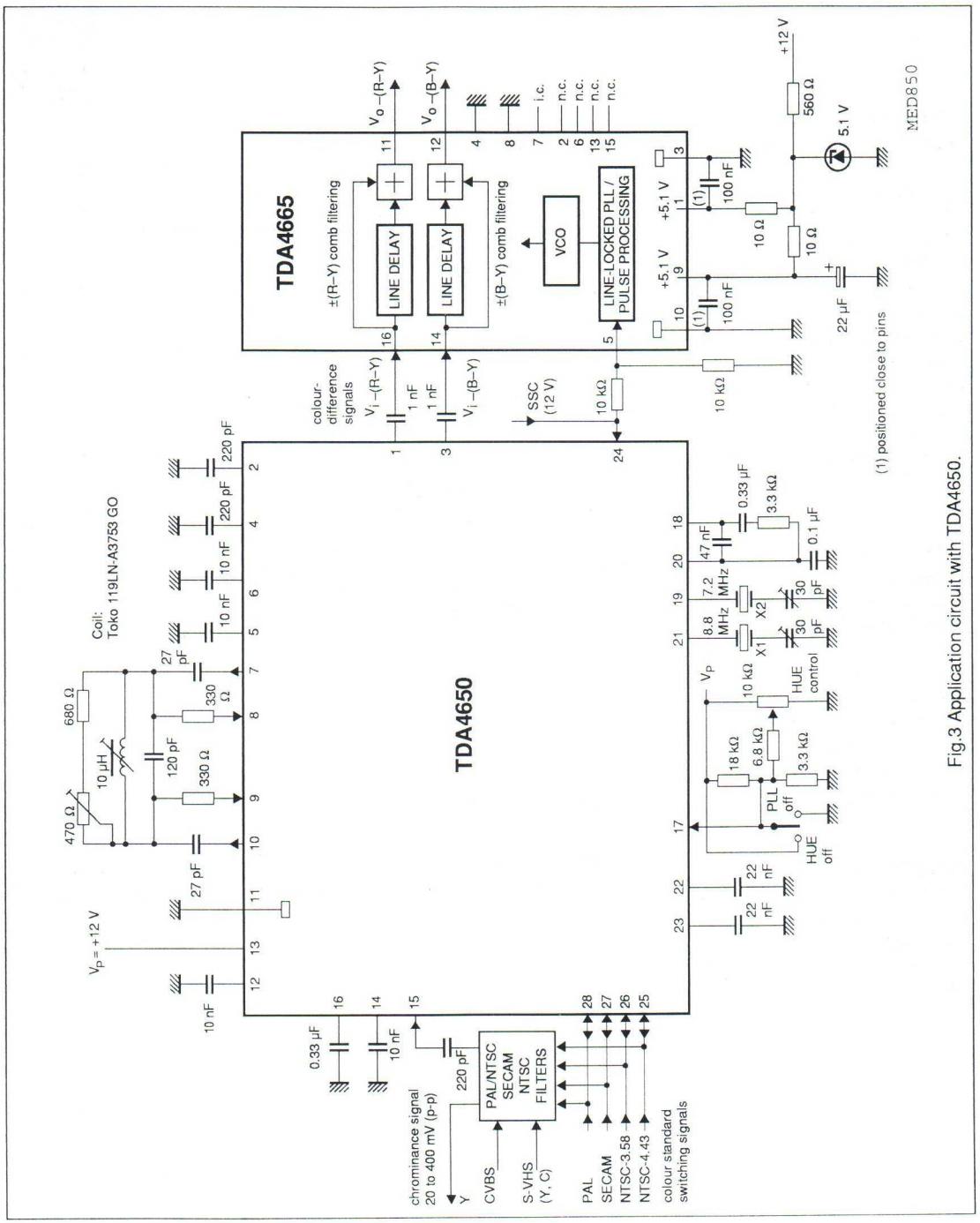


Fig.3 Application circuit with TDA4650.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991
supersedes data of August 1990	

TDA4670

Picture signal improvement (PSI) circuit

FEATURES

- Luminance signal delay from 20 ns up to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with symmetrical overshoots selectable
- 2.6 or 5 MHz peaking centre frequency and degree of peaking selectable (–3, 0, +3 and +6 dB)
- Noise reduction by coring selectable
- Handles negative as well as positive colour-difference signals
- Colour transient improvement (CTI) selectable to decrease the colour-difference signal transient times to those of the high frequency luminance signals
- 5 or 12 V sandcastle input voltage selectable
- All controls selected via the I²C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance and colour-difference input signal clamping with coupling-capacitor
- +4.5 to 8.8 V supply voltage range
- Minimum of external components

GENERAL DESCRIPTION

The TDA4670 delays the luminance signal and improves colour-difference signal transients. Additional, the luminance signal can be improved by peaking and noise reduction (coring).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 1 and 5)	4.5	5	8.8	V
I_P	total supply current	31	41	52	mA
$t_{d\,Y}$	Y signal delay time	20	-	1130	ns
$V_{i\,VBS}$	composite Y input signal (peak-to-peak value, pin 16)	-	450	640	mV
$V_{i\,CD}$	colour-difference input signal (peak-to-peak value)				
	±(R–Y) on pin 3	-	1.05	1.48	V
	±(B–Y) on pin 7	-	1.33	1.88	V
G_Y	gain of Y channel	-	–1	-	dB
G_{CD}	gain of colour-difference channel	-	0	-	dB
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4670	18	DIL	plastic	SOT102

Picture signal improvement (PSI) circuit

TDA4670

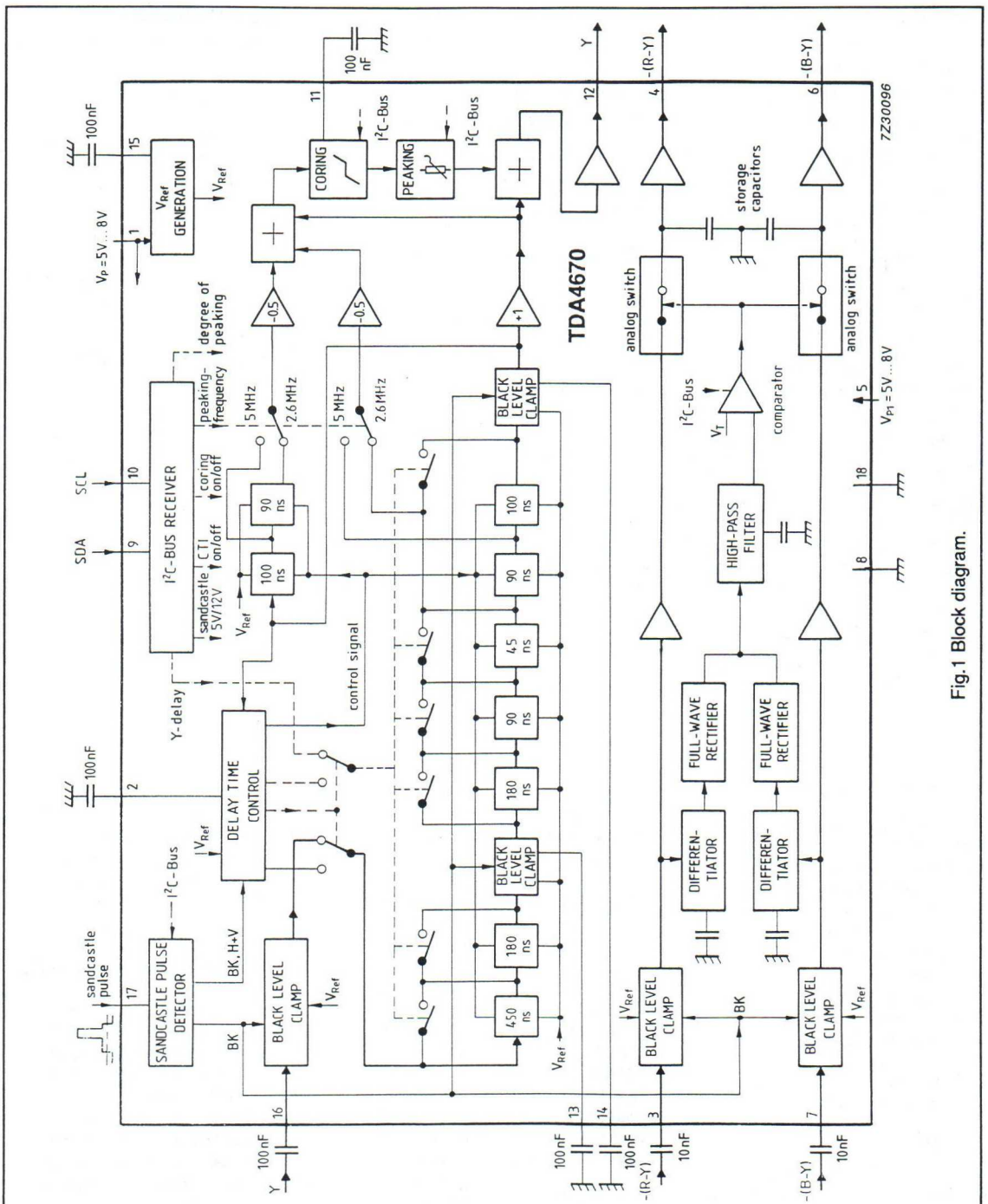


Fig.1 Block diagram.

Picture signal improvement (PSI) circuit

TDA4670

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
C_{DL}	2	capacitor of delay time control
$V_{i\,(R-Y)}$	3	±(R–Y) colour-difference input signal
$V_{o\,(R-Y)}$	4	±(R–Y) colour-difference output signal
V_{P2}	5	positive supply voltage 2
$V_{o\,(B-Y)}$	6	±(B–Y) colour-difference output signal
$V_{i\,(B-Y)}$	7	±(B–Y) colour-difference input signal
GND2	8	ground 2 (0 V)
SDA	9	I²C-bus data line
SCL	10	I²C-bus clock line
C_{COR}	11	coring capacitor
$V_{o\,Y}$	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{ref}	15	capacitor of reference voltage
$V_{i\,Y}$	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

PIN CONFIGURATION

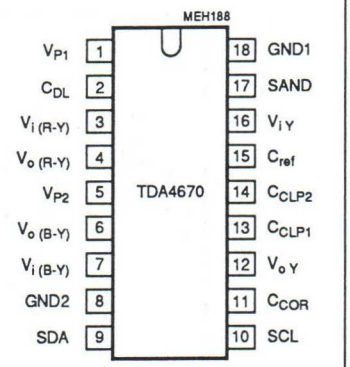


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4670 contains luminance signal processing and colour-difference signal processing.The luminance signal section comprises a variable, integrated luminance delay line with luminance signal peaking and a noise reduction by coring.
The colour-difference section consists of a transient improvement circuit to decreases the rise and fall times of the colour-difference signal transients.
All functions and parameters are controlled via the I²C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input pin 16. Its black porch is clamped to a DC reference voltage to ensure fitting to the operating range of the luminance delay stage.
The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (Fig.1). The luminance signal delay is controlled via the I²C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.
An automatic luminance delay time adjustment in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst-key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} at pin 2.
The peaking section is using a transversal filter circuit with selectable centre frequencies of 2.6 and 5.0 MHz.
It provides selectable degrees of peaking of –3, 0, +3 and +6 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.
The output buffer stage ensures a low-ohmic VBS output signal on pin 12 (< 160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.

An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal during the vertical blanking interval in lines 16 (330) to 18 (332). Therefore, this output signal should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are clamped to a reference voltage.

Each colour-difference signal is fed to a transient detector and to an analog signal switch with an attached voltage storage stage.
The transient detectors consist of differentiators and full-wave rectifiers. The output voltages of both transient detectors are added and then compared in a comparator. This comparator controls both following analog signal switches simultaneously. The analog signal switches are in open position at a certain value of transient time; then the held value (held by storage capacitors) is applied to the outputs. The switches close to accept rapidly the actual signal levels at the end of these transients. The improved transient time is approximately 100 ns long independent of the input signal transient time.

Colour-difference paths are independent of the input signal polarity and have a gain of unity .

The CTI functions are switched on and off via the I^2C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). V_{P1} and V_{P2} as well as GND1 and GND 2 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)	0	8.8	V
V_{P2}	supply voltage (pin 5)	0	8.8	V
P_{tot}	total power dissipation	0	0.97	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for pins 9 and 10	- -	+300 –500	V V
	for other pins	-	±500	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	-	82	K/W

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; nominal video amplitude $V_{VB} = 315$ mV; $t_H = 64$ µs; $t_{BK} = 4$ µs (burst key); $T_{amb} = 25$ °C and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 1)		4.5	5	8.8	V
V_{P2}	supply voltage range (pin 5)		4.5	5	8.8	V
I_P	total supply current		31	41	52	mA
Y-signal path						
$V_{i\,Y}$	VBS input signal on pin 16 (peak-to-peak value)		-	450	640	mV
V_{16}	black level clamping voltage		-	3.1	-	V
I_{16}	input current	during clamping	±95	-	±190	µA
		outside clamping	-	-	±0.1	µA
R_{16}	input resistance	outside clamping	5	-	-	MΩ
C_{16}	input capacitance		-	3	10	pF
$t_{d\,Y}$	maximum Y delay time	set via I²C-bus	1070	1100	1130	ns
	minimum Y delay time		-	20	-	ns
$\Delta t_{d\,Y}$	minimum delay step	set via I²C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz maximum delay	-	0	±25	ns
	delay time difference between Y and colour-difference signals	Y delay; CTI and peaking off	70	100	130	ns
$t_{d\,peak}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_o / V_i; f = 500 kHz; maximum delay	–2	–1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	–1	-	-	mA
		sink current	0.4	-	-	mA
R_{12}	output resistance		-	-	160	Ω
f	frequency response for	maximum delay				
	f = 0.5 to 3 MHz		–2	–1	0	dB
	f = 0.5 to 5 MHz		–4	–3	–1	dB
LIN	signal linearity for	a_{min} / a_{max}				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	-	-	-
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	-	-	-

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance peaking, selected via I²C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (f_C amplitude over 0.5 MHz amplitude)					
	selectable values		-	–3	-	dB
			-	0	-	dB
			-	+3	-	dB
			-	+6	-	dB
	limitation of peaking (positive amplitude of correction signal referred to 315 mV)		-	20	-	%
V_n	noise voltage on pin 12 (RMS value)	without peaking f = 0 to 5 MHz	-	-	1	mV
COR	coring of peaking (coring part referred to 315 mV)	COR-bit = 1	-	20	-	%
Colour-difference paths measured with transient times $t_r = t_f = 1$ µs; $t_{pH} \geq 1$ µs; $V_i = 1.33$ V (p-p) on pins 3 and 7 and with burst key pulse $t_{BK} = 4$ µs.						
$V_{i\,CD}$	±(R–Y) input signal (peak-to-peak values, pin 3)	75% colour bar;	-	1.05	1.48	V
	±(B–Y) input signal (peak-to-peak values, pin 7)	75% colour bar	-	1.33	1.88	V
	input transient sensitivity	$V_{3,7}$/dt	0.15	-	-	V/µs
$V_{3,7}$	internal clamping voltage level		-	2.45	-	V
$I_{3,7}$	input current	outside clamping during clamping	- ±100	- -	±1 ±190	µA µA
$C_{3,7}$	input capacitance		-	6	12	pF
$V_{4,6}$	DC output voltage		-	2	-	V
$\Delta V_{4,6}$	output offset voltage	$R_S \leq 300\ \Omega$; note 1	-	-	±5	mV
		during and after storage time	-	-	±18	mV
V_{spike}	spurious spike signals on pins 4 and 6	$R_S \leq 300\ \Omega$; note 1	-	-	±30	mV
$I_{4,6}$	output current (emitter-follower with constant current source)	source current sink current	–1 0.4	- -	- -	mA mA
$R_{4,6}$	output resistance		-	-	100	Ω
G_v	signal gain in each path	V_o / V_i	–1	0	+1	dB
ΔG_v	gain difference –(R–Y) / –(B–Y)		-	0	±0.3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN	signal linearity	a_{min} / a_{max}				
	for nominal signal	V_i = 1.33 V (p-p)	0.90	-	-	
	for +3 dB signal	V_i = 1.88 V (p-p)	0.65	-	-	
ΔV_o	signal reduction at higher frequency (output signal ratio V_i / V_o)	signal with t_{pH} = 50 ns; $t_r = t_f$ = 1 µs	−1.5	-	-	dB
Sandcastle pulse, input voltage selectable via I²C-bus						
V_{17}	input voltage threshold for H and V sync	SC5-bit = 0 (12 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 0 (12 V)	5.5	6.5	7.5	V
	input voltage threshold for H and V sync	SC5-bit = 1 (5 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 1 (5 V)	3.0	3.5	4.0	V
R_{17}	input resistance	12 V input level	30	40	50	kΩ
		5 V input level	15	20	25	kΩ
C_{17}	input capacitance		-	4	8	pF
t_{BK}	burst-key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referred to t_{BK}	-	1	-	µs
n_p	number of required burst-key pulses vertical blanking interval	note 2	4	-	31	
I²C-bus control, SDA and SCL						
V_{IH}	input voltage HIGH on pins 9 and 10		3	-	5	V
V_{IL}	input voltage LOW		0	-	1.5	V
$I_{9,10}$	input current		-	-	±10	µA
V_9	output voltage at acknowledge on pin 9	I_9 = 3 mA	-	-	0.4	V
I_{ACK}	output current at acknowledge on pin 9	sink current	3	-	-	mA

Notes to the characteristics

1. Crosstalk on output, measured in the unused channel when the other channel is provided with a nominal input signal (CTI active).
2. A number of more than 31 burst-key pulses repeats the counter cycle of delay time control.

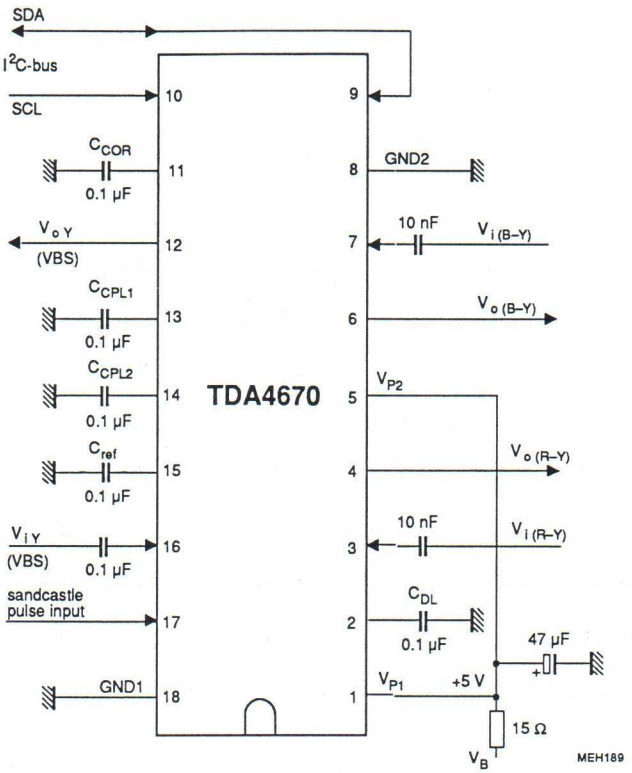


Fig.3 Test and application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**1000 100X**
A	=	acknowledge, generated by the slave
SUBADDRESS	=	subadress byte, Table 1
DATA	=	data byte, Table 1
P	=	stop condition
X	=	read/write control bit X = 0, to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus transmission

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
Y delay / CTI / SC	0 0 0 1 0 0 0 0	0	SC5	CTI	DL4	DL3	DL2	DL1	DL0
peaking and coring	0 0 0 1 0 0 0 1	COR	PEAK	LCF	0	0	0	PCON1	PCON0

Function of the bits:

DL0	set delay in luminance channel:	1 = 45 ns;	0 = 0 ns
DL1		1 = 90 ns;	0 = 0 ns
DL2		1 = 180 ns;	0 = 0 ns
DL3		1 = 180 ns;	0 = 0 ns
DL4		1 = 450 ns;	0 = 0 ns
CTI	set colour transient improvement:	1 = active	0 = inactive
SC5	select sandcastle pulse voltage:	1 = 5 V	0 = 12 V
LCF	set peaking frequency response:	1 = 2.6 MHz	0 = 5.0 MHz
PEAK	set peaking delay:	1 = active	0 = inactive
COR	set coring control:	1 = active	0 = inactive

PCON — set peaking amplification:

PCON1	PCON0	grade of peaking
0	0	–3 dB
0	1	0 dB
1	0	+3 dB
1	1	+6 dB

Remarks to the subaddress bytes

Hex subaddresses 00 to 0F are reserved for colour decoders and RGB processors.
Subaddresses 10 and 11 only are acknowledged .
General call address is not acknowledged.
Power-on reset: D7 to D1 bits of data bytes are set to 0 , D0 bit is set to 1.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

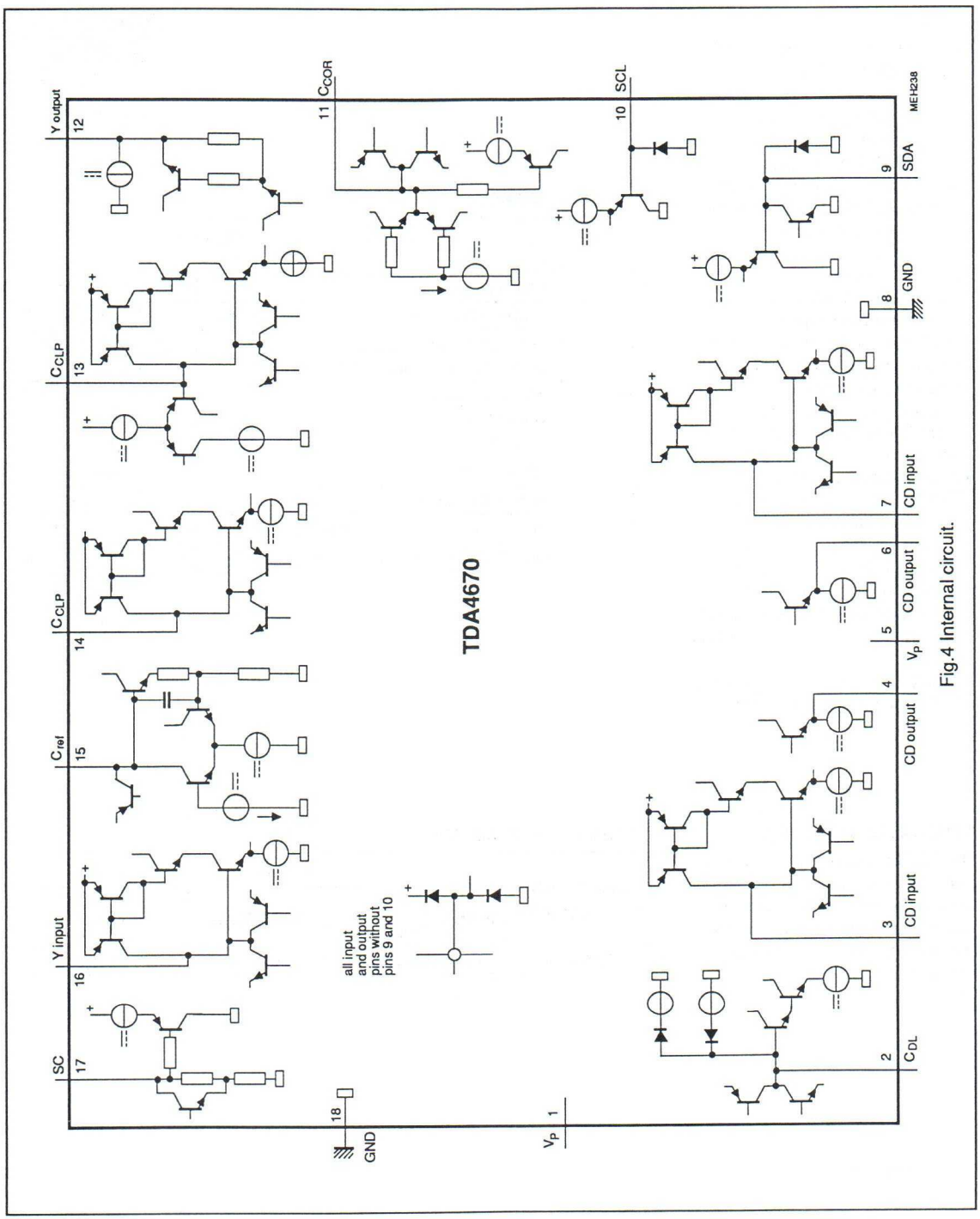


Fig.4 Internal circuit.

Picture signal improvement (PSI) circuit — TDA4671

FEATURES

- Luminance signal delay from 20 ns up to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with symmetrical overshoots selectable
- 2.6 or 5 MHz peaking centre frequency and degree of peaking selectable (–3, 0, +3 and +6 dB)
- Noise reduction by coring selectable
- Handles negative and positive colour-difference signals
- Colour transient improvement (CTI) selectable to decrease the colour-difference signal transient times to those of the high frequency luminance signals
- 5 or 12 V sandcastle input voltage selectable
- All controls selected via the I^2C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance and colour-difference input signal clamping with coupling capacitor
- +4.5 to 8.8 V supply voltage range
- Minimum of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 1 and 5)	4.5	5	8.8	V
I_P	total supply current	31	41	52	mA
$t_{d\,Y}$	Y signal delay time	20	–	1130	ns
$V_{i\,VBS}$	composite Y input signal (peak-to-peak value, pin 16)	–	450	640	mV
$V_{i\,CD}$	colour-difference input signal (peak-to-peak value)				
	±(R–Y) on pin 3	–	1.05	1.48	V
	±(B–Y) on pin 7	–	1.33	1.88	V
G_Y	gain of Y channel	–	–1	–	dB
G_{CD}	gain of colour-difference channel	–	0	–	dB
T_{amb}	operating ambient temperature	0	–	+70	°C

GENERAL DESCRIPTION

The TDA4671 delays the luminance signal and improves colour-difference signal transients. The luminance signal can also be improved by peaking and noise reduction (coring).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4671	18	DIL	plastic	SOT102

Picture signal improvement (PSI) circuit TDA4671

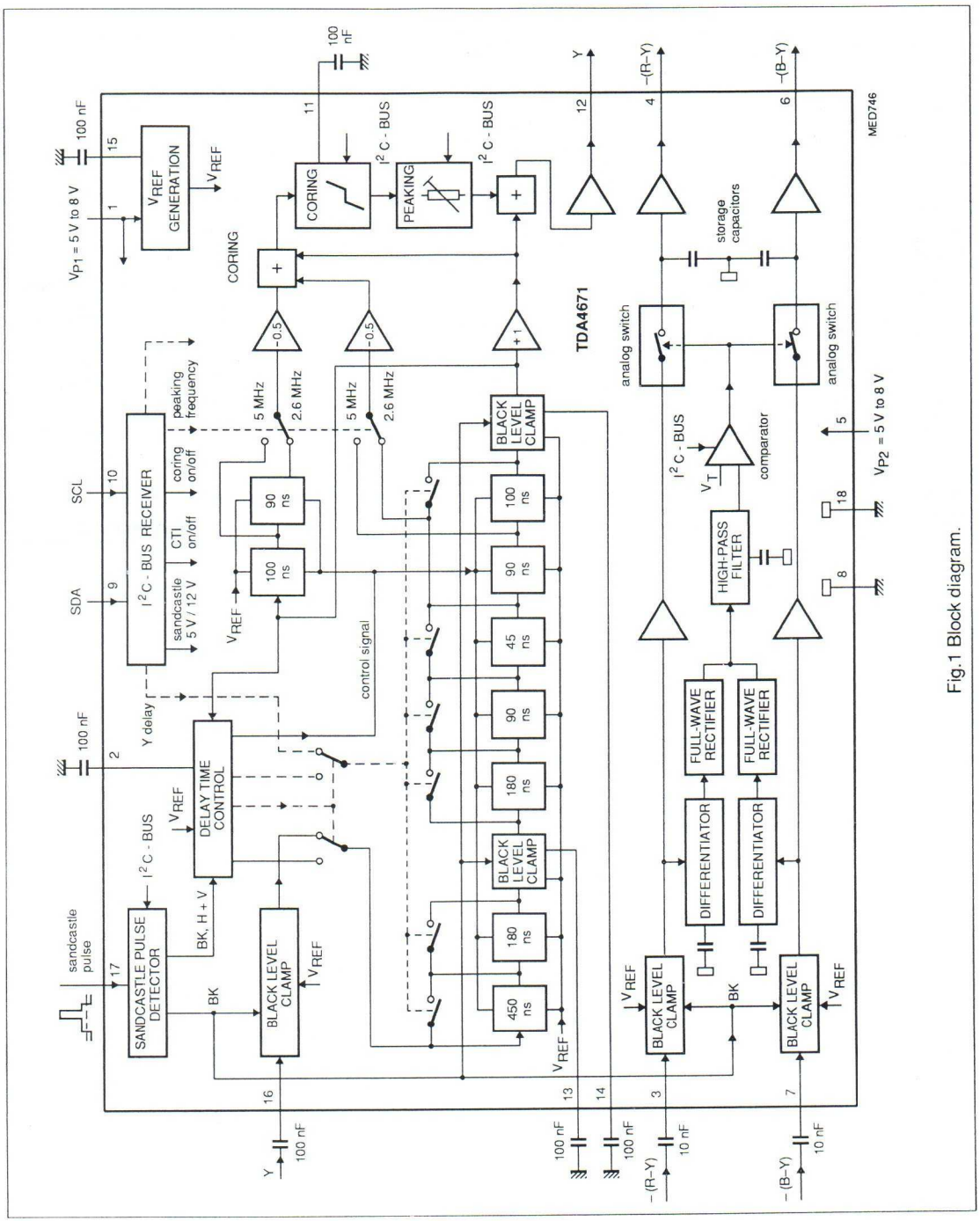


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
C_{DL}	2	capacitor of delay time control
$V_{i\,(R-Y)}$	3	±(R–Y) colour-difference input signal
$V_{o\,(R-Y)}$	4	±(R–Y) colour-difference output signal
V_{P2}	5	positive supply voltage 2
$V_{o\,(B-Y)}$	6	±(B–Y) colour-difference output signal
$V_{i\,(B-Y)}$	7	±(B–Y) colour-difference input signal
GND2	8	ground 2 (0 V)
SDA	9	I^2C-bus data line
SCL	10	I^2C-bus clock line
C_{COR}	11	coring capacitor
$V_{o\,Y}$	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{REF}	15	capacitor of reference voltage
$V_{i\,Y}$	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

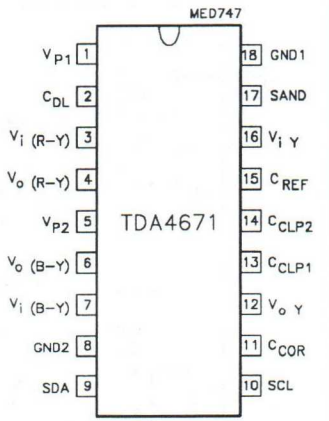


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4671 contains luminance signal processing and colour-difference signal processing. The luminance signal section comprises a variable, integrated luminance delay line with luminance signal peaking and a noise reduction by coring.
The colour-difference section consists of a transient improvement circuit to decrease the rise and fall times of the colour-difference signal transients. All functions and parameters are controlled via the I^2C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input pin 16. Its black porch is clamped to a DC reference voltage to ensure fitting to the operating range of the luminance delay stage.
The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (Fig.1). The luminance signal delay is controlled via the I^2C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.

An automatic luminance delay time adjustment in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst-key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} at pin 2.
The peaking section is using a transversal filter circuit with selectable centre frequencies of 2.6 and 5.0 MHz.
It provides selectable degrees of peaking of –3, 0, +3 and +6 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.
The output buffer stage ensures a low-ohmic VBS output signal on pin 12 (< 160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.
An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal. It is present during the vertical blanking interval of the burst-key pulses in lines 16 (330) to 18 (332). This sync should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are clamped to a reference voltage.
Each colour-difference signal is fed to a transient detector and to an analog signal switch with an attached voltage storage stage.
The transient detectors consist of differentiators and full-wave rectifiers. The output voltages of both transient detectors are added and then compared. The comparator controls both following analog signal switches simultaneously.
The analog signal switches are in open position at a certain value of transient time; then the held value (held by capacitors) is applied to the outputs. The switches close to rapidly accept the actual signal levels at the end of these transients. The improved transient time is approximately 100 ns long independent of the input transient time.
Colour-difference paths are independent of the input signal polarity and have a nominal unity gain.
The CTI functions are switched on and off via the I^2C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). V_{P1} and V_{P2} as well as GND1 and GND2 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)	0	8.8	V
V_{P2}	supply voltage (pin 5)	0	8.8	V
P_{tot}	total power dissipation	0	0.97	W
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling (note 1)			
	for pins 9 and 10	–	+300	V
		–	−500	V
	for other pins	–	±500	V

Note to the limiting values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	82 K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; nominal video amplitude $V_{VB} = 315$ mV; $t_H = 64$ µs; $t_{BK} = 4$ µs (burst key); $T_{amb} = +25$ °C and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)		4.5	5	8.8	V
V_{P2}	supply voltage (pin 5)		4.5	5	8.8	V
I_P	total supply current		31	41	52	mA
Y-signal path						
$V_{i\,Y}$	VBS input signal on pin 16 (peak-to-peak value)		–	450	640	mV
V_{16}	black level clamping voltage		–	3.1	–	V
I_{16}	input current	during clamping	±95	–	±190	µA
		outside clamping	–	–	±0.1	µA
R_{16}	input resistance	outside clamping	5	–	–	MΩ
C_{16}	input capacitance		–	3	10	pF
$t_{d\,Y}$	maximum Y delay time	set via I^2C-bus	1070	1100	1130	ns
	minimum Y delay time		–	20	–	ns
$\Delta t_{d\,Y}$	minimum delay step	set via I^2C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz maximum delay	–	0	±25	ns
	delay time difference between Y and colour-difference signals	Y delay; CTI and peaking off	70	100	130	ns
$t_{d\,peak}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_o / V_i; f = 500 kHz; maximum delay	–2	–1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	–1	–	–	mA
		sink current	0.4	–	–	mA
R_{12}	output resistance		–	–	160	Ω
f	frequency response for	maximum delay				
	f = 0.5 to 3 MHz		–2	–1	0	dB
	f = 0.5 to 5 MHz		–4	–3	–1	dB
LIN	signal linearity for	a_{min} / a_{max}				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	–	–	–
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	–	–	–
Luminance peaking, selected via I^2C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (f_C amplitude over 0.5 MHz amplitude) selectable values					
			–	–3	–	dB
			–	0	–	dB
			–	+3	–	dB
			–	+6	–	dB
	limitation of peaking (positive amplitude of correction signal referred to 315 mV)		–	20	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_n	noise voltage on pin 12 (RMS value)	without peaking f = 0 to 5 MHz	–	–	1	mV
COR	coring of peaking (coring part referred to 315 mV)	COR-bit = 1	–	20	–	%
Colour-difference paths measured with transient times $t_r = t_f = 1$ µs; $t_{pH} \geq 1$ µs; $V_i = 1.33$ V (p-p) on pins 3 and 7 and with burst key pulse $t_{BK} = 4$ µs						
$V_{i\,CD}$	±(R–Y) input signal (peak-to-peak value, pin 3)	75% colour bar	–	1.05	1.48	V
	±(B–Y) input signal (peak-to-peak value, pin 7)	75% colour bar	–	1.33	1.88	V
	input transient sensitivity	$V_{3,7}/dt$	0.22	–	–	V/µs
$V_{3,7}$	internal clamping voltage level		–	2.45	–	V
$I_{3,7}$	input current	outside clamping during clamping	– ±100	– –	±1 ±190	µA µA
$C_{3,7}$	input capacitance		–	6	12	pF
$V_{4,6}$	DC output voltage		–	2	–	V
$\Delta V_{4,6}$	output offset voltage	$R_S \leq 300\ \Omega$; note 1 during and after storage time	– –	– –	±5 ±18	mV mV
V_{spike}	spurious spike signals on pins 4 and 6	$R_S \leq 300\ \Omega$; note 1	–	–	±30	mV
$I_{4,6}$	output current (emitter-follower with constant current source)	source current sink current	–1 0.4	– –	– –	mA mA
$R_{4,6}$	output resistance		–	–	100	Ω
G_v	signal gain in each path	V_o / V_i	–1	0	+1	dB
ΔG_v	gain difference –(R–Y) / –(B–Y)		–	0	±0.3	dB
LIN	signal linearity for nominal signal for +3 dB signal	a_{min} / a_{max} $V_i = 1.86$ V (p-p) $V_i = 1.33$ V (p-p)	 0.90 0.65	 – –	 – –	
ΔV_o	signal reduction at higher frequency (output signal ratio for $f_{50\,ns} / f_{1\,\mu s}$)	signal with $t_{pH} = 50$ ns; $t_r = t_f = 1$ µs	–1.5	–	–	dB
Sandcastle pulse, input voltage selectable via I^2C-bus						
V_{17}	input voltage threshold for H and V sync input voltage threshold for burst	SC5-bit = 0 (12 V) SC5-bit = 0 (12 V)	1.1 5.5	1.5 6.5	1.9 7.5	V V
	input voltage threshold for H and V sync input voltage threshold for burst	SC5-bit = 1 (5 V) SC5-bit = 1 (5 V)	1.1 3.0	1.5 3.5	1.9 4.0	V V
R_{17}	input resistance	12 V input level 5 V input level	30 15	40 20	50 25	kΩ kΩ
C_{17}	input capacitance		–	4	8	pF
t_{BK}	burst-key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referred to t_{BK}	–	1	–	µs
n_p	number of required burst-key pulses vertical blanking interval	note 2	4	–	31	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus control, SDA and SCL						
V_{IH}	HIGH level input voltage on pins 9 and 10		3	–	5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
$I_{9,10}$	input current		–	–	±10	µA
V_9	output voltage at acknowledge on pin 9	I_9 = 3 mA	–	–	0.4	V
I_{ACK}	output current at acknowledge on pin 9	sink current	3	–	–	mA

Notes to the characteristics

1. Crosstalk on output, measured in the unused channel when the other channel is provided with a nominal input signal (CTI active).
2. A number of more than 31 burst-key pulses repeats the counter cycle of delay time control.

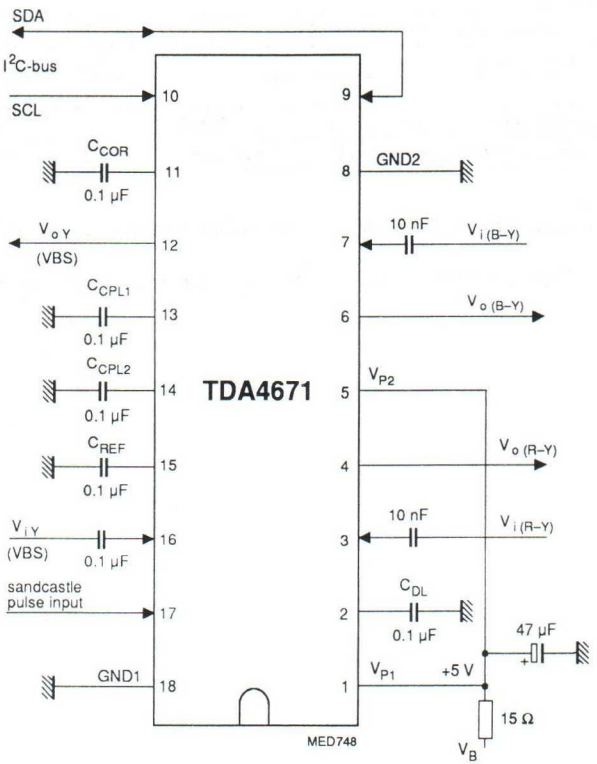


Fig.3 Test and application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = 1000 100X
A = acknowledge, generated by the slave
SUBADDRESS = subaddress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; SUBADDRESS/DATA

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Y delay / CTI / SC	00010000	0	SC5	CTI	DL4	DL3	DL2	DL1	DL0
peaking and coring	00010001	COR	PEAK	LCF	0	0	0	PCON1	PCON0

Function of the bits:

DL0	set delay in luminance channel:	1 = 45 ns;		0 = 0 ns
DL1		1 = 90 ns;		0 = 0 ns
DL2		1 = 180 ns;		0 = 0 ns
DL3		1 = 180 ns;		0 = 0 ns
DL4		1 = 450 ns;		0 = 0 ns
CTI	set colour transient improvement:	1 = active		0 = inactive
SC5	select sandcastle pulse voltage:	1 = 5 V		0 = 12 V
LCF	set peaking frequency response:	1 = 2.6 MHz		0 = 5.0 MHz
PEAK	set peaking delay:	1 = active		0 = inactive
COR	set coring control:	1 = active		0 = inactive
PCON	set peaking amplification:	PCON1	PCON0	grade of peaking
		0	0	–3 dB
		0	1	0 dB
		1	0	+3 dB
		1	1	+6 dB

Remarks to the subaddress bytes

Hex subaddresses 00 to 0F are reserved for colour decoders and RGB processors.
Subaddresses 10 and 11 only are acknowledged.
General call address is not acknowledged.
Power-on reset: D7 to D1 bits of data bytes are set to 0, D0 bit is set to 1.

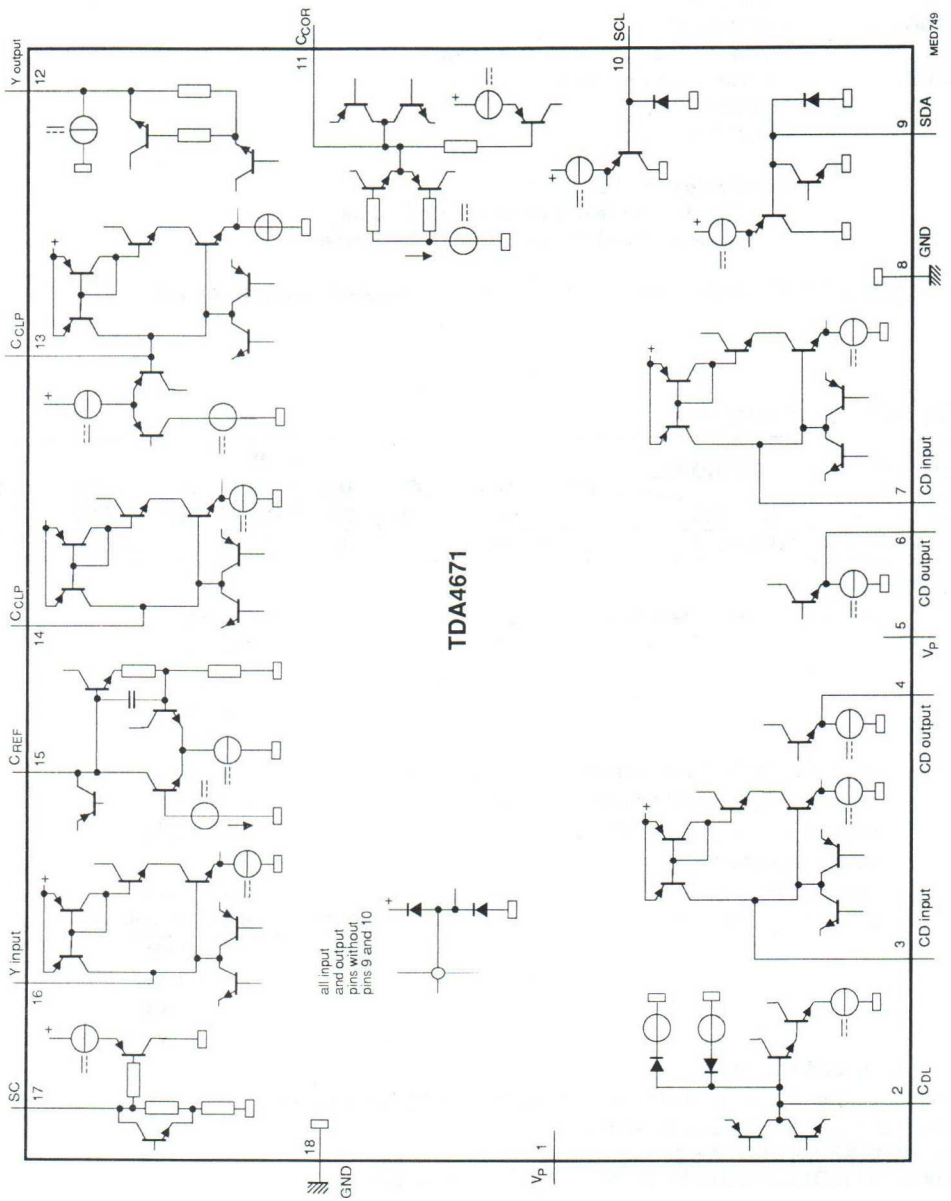


Fig.4 Internal circuit.

Picture signal improvement (PSI) circuit with enhanced peaking function

TDA4672

FEATURES

- Luminance signal delay from 20 ns up to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with symmetrical overshoots selectable
- 2.6 or 5 MHz peaking centre frequency and degree of peaking selectable from −6 dB to +9 dB in 16 steps of 1 dB each
- Noise reduction by coring selectable
- 5 or 12 V sandcastle input voltage selectable
- All controls selected via the I^2C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance input signal clamping with coupling capacitor
- +4.5 to +8.8 V supply voltage
- Minimum of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	4.5	5	8.8	V
I_P	total supply current	26	37	46	mA
t_d	Y signal delay time	20	–	1130	ns
$V_{i\,(p\text{-}p)}$	composite Y input signal (peak-to-peak value, pin 16)	–	450	640	mV
G_Y	voltage gain of Y channel	–	−1	–	dB
T_{amb}	operating ambient temperature	0	–	+70	°C

GENERAL DESCRIPTION

The TDA4672 delays the luminance signal. The luminance signal can also be improved by peaking and noise reduction (coring).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4672	18	DIL	plastic	SOT102

Picture signal improvement (PSI) circuit with enhanced peaking function

TDA4672

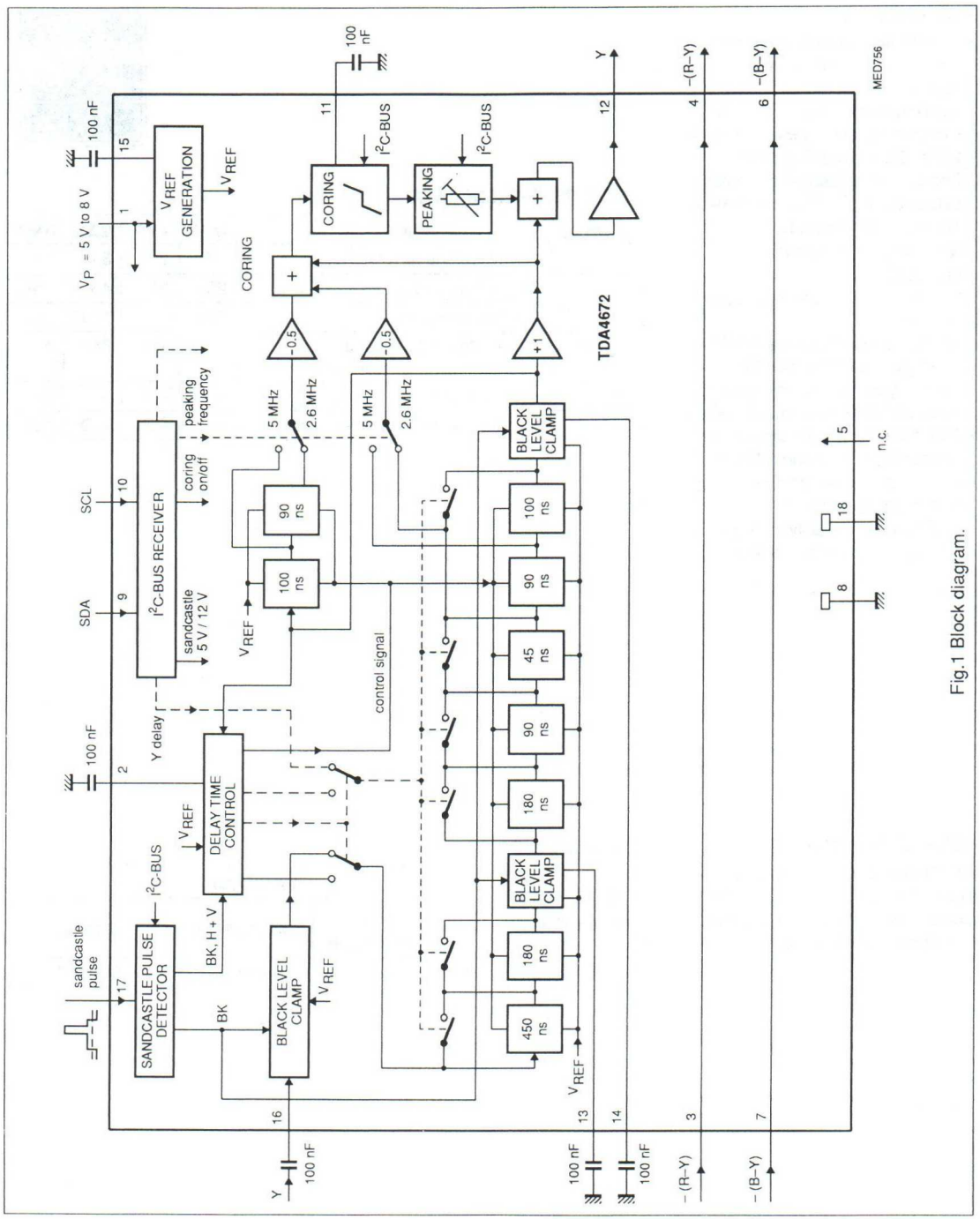


Fig.1 Block diagram.

Picture signal improvement (PSI) circuit with enhanced peaking function

TDA4672

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{DL}	2	capacitor of delay time control
$V_{i(R-Y)}$	3	±(R–Y) colour-difference input signal; note 1
$V_{o(R-Y)}$	4	±(R–Y) colour-difference output signal; note 1
n.c.	5	not connected
$V_{o(B-Y)}$	6	±(B–Y) colour-difference output signal; note 2
$V_{i(B-Y)}$	7	±(B–Y) colour-difference input signal; note 2
GND2	8	ground 2 (0 V)
SDA	9	I^2C-bus data line
SCL	10	I^2C-bus clock line
C_{COR}	11	coring capacitor
$V_{o(Y)}$	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{REF}	15	capacitor of reference voltage
$V_{i(Y)}$	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

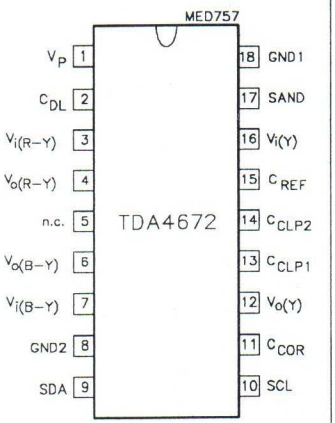


Fig.2 Pin configuration.

Notes to the pinning

1. Pin 3 is connected directly to pin 4.
2. Pin 7 is connected directly to pin 6.

FUNCTIONAL DESCRIPTION

The TDA4672 contains luminance signal processing.
The luminance signal section comprises a variable, integrated luminance delay line with luminance signal peaking and a noise reduction by coring.
All functions and parameters are controlled via the I^2C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input pin 16. Its black porch is clamped to a DC reference voltage to ensure fitting to the operating range of the luminance delay stage.
The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (Fig.1). The luminance signal delay is controlled via the I^2C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.

An automatic luminance delay time adjustment in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst-key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} at pin 2.
The peaking section is using a transversal filter circuit with selectable centre frequencies of 2.6 and 5.0 MHz.
It provides selectable degrees of peaking from –6 to +9 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.
The output buffer stage ensures a low-ohmic VBS (Video Blanking Synchronization) output signal on pin 12 (< 160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.
An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal. It is present during the vertical blanking interval of the burst-key pulses in lines 16 (330) to 18 (332). This sync should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are connected directly to the output pins.
This is for compatibility with other Philips Semiconductors PSI-circuits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
GND1 and GND2 are connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	8.8	V
V_I	input voltage (pins 2 to 7 and pins 11 to 16)	−0.1	V_P	V
$V_{9, 10}$	input voltage at pins 9 and 10	−0.1	8.8	V
V_{17}	input voltage at pin 17	−0.1	12	V
I_{8-18}	current between pins 8 and 18	–	±20	mA
I_{3-4}	current between pins 3 and 4	–	±4	mA
I_{6-7}	current between pins 6 and 7	–	±4	mA
P_{tot}	total power dissipation	0	0.97	W
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling (note 1)			
	for pin 17	–	+250	V
		–	−500	V
	for other pins	–	±500	V

Note to the limiting values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	82 K/W

CHARACTERISTICS

V_P = 5 V; nominal video amplitude V_{VB} = 315 mV; t_H = 64 µs; t_{BK} = 4 µs (burst key); T_{amb} = +25 °C and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)		4.5	5	8.8	V
I_P	total supply current		26	37	46	mA
Y-signal path						
$V_{i(Y)}$	VBS input signal on pin 16 (peak-to-peak value)		–	450	640	mV
V_{16}	black level clamping voltage		–	3.1	–	V
I_{16}	input current	during clamping	±95	–	±190	µA
		outside clamping	–	–	±0.1	µA
R_{16}	input resistance	outside clamping	5	–	–	MΩ
C_{16}	input capacitance		–	3	10	pF
$t_{d(Y)}$	maximum Y delay time	set via I^2C-bus	1070	1100	1130	ns
	minimum Y delay time		–	20	–	ns
$\Delta t_{d(Y)}$	minimum delay step	set via I^2C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz maximum delay	–	0	±25	ns
$t_{d\ peak}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_{12} / V_{16}; f = 500 kHz; maximum delay	–2	–1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	–1	–	–	mA
		sink current	0.4	–	–	mA
R_{12}	output resistance		–	–	160	Ω
f	frequency response for	maximum delay				
	f = 0.5 to 3 MHz		–2	–1	0	dB
	f = 0.5 to 5 MHz		–4	–3	–1	dB
LIN	signal linearity for	a_{min} / a_{max}; note 1				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	–	–	–
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	–	–	–
Luminance peaking, selected via I^2C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (fc amplitude over 0.5 MHz amplitude)	Y delay = 215 ns; peaking delay only				
	selectable values					
	from		–	–6	–	dB
	to		–	+9	–	dB
	each step		–	1	–	dB
	no limitation of peaking		–	–	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_n	noise voltage on pin 12 (RMS value)	without peaking; f = 0 to 5 MHz	–	–	1	mV
COR	coring of peaking (coring part referenced to 315 mV)	COR-bit = 1	–	20	–	%
Sandcastle pulse, input voltage selectable via I^2C-bus						
V_{17}	input voltage threshold for H and V	SC5-bit = 0 (12 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 0 (12 V)	5.5	6.5	7.5	V
	input voltage threshold for H and V	SC5-bit = 1 (5 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 1 (5 V)	3.0	3.5	4.0	V
R_{17}	input resistance	12 V input level	30	40	50	kΩ
		5 V input level	15	20	25	kΩ
C_{17}	input capacitance		–	4	8	pF
t_{BK}	burst-key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referenced to t_{BK}	–	1	–	µs
n_p	number of required burst-key pulses vertical blanking interval	note 2	4	–	31	
I^2C-bus control, SDA and SCL						
V_{IH}	HIGH level input voltage on pins 9 and 10		3	–	5	V
V_{IL}	LOW level input voltage on pins 9 and 10		0	–	1.5	V
$I_{9,10}$	input current on pins 9 and 10		–	–	±10	µA
V_{ACK}	output voltage at acknowledge on pin 9	I_9 = 3 mA	–	–	0.4	V
I_{ACK}	output current at acknowledge on pin 9	sink current	3	–	–	mA

Note to the characteristics

1. a_{min}: minimum differential voltage gain of the luminance video signal;
   a_{max}: maximum differential voltage gain of the luminance video signal.
2. A number of more than 31 burst-key pulses repeats the counter cycle of delay time control.

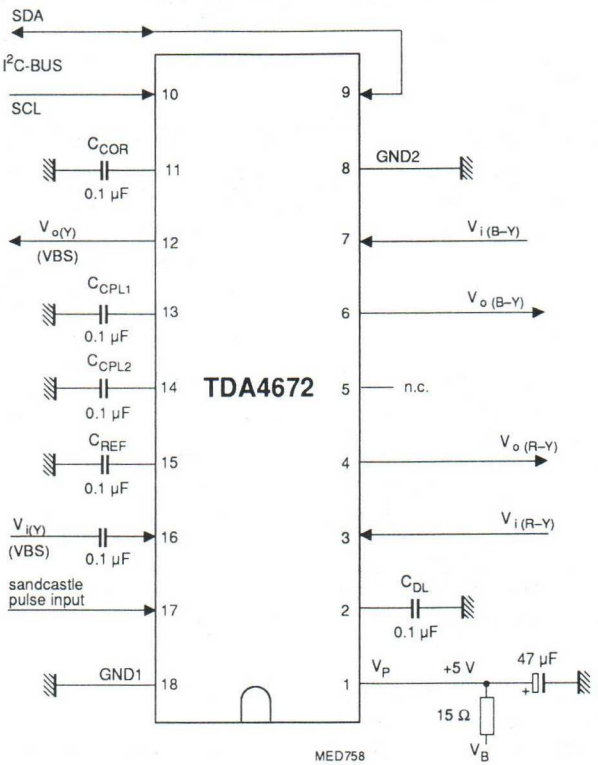


Fig.3 Test and application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = 1000 100X
A = acknowledge, generated by the slave
SUBADDRESS = subaddress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; SUBADDRESS/DATA.

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Y delay / SC	00010000	0	SC5	0	DL4	DL3	DL2	DL1	DL0
peaking and coring	00010001	COR	PEAK	LCF	0	PCON3	PCON2	PCON1	PCON0

Explanation of data bits in Table 1:

DL0	set delay in luminance channel:	1 = 45 ns;			0 = 0 ns	
DL1	set delay in luminance channel:	1 = 90 ns;			0 = 0 ns	
DL2	set delay in luminance channel:	1 = 180 ns;			0 = 0 ns	
DL3	set delay in luminance channel:	1 = 180 ns;			0 = 0 ns	
DL4	set delay in luminance channel:	1 = 450 ns;			0 = 0 ns	
SC5	select sandcastle pulse voltage:	1 = 5 V			0 = 12 V	
LCF	set peaking frequency response:	1 = 2.6 MHz			0 = 5.0 MHz	
PEAK	set peaking delay:	1 = active (190 ns)			0 = inactive	
COR	set coring control:	1 = active			0 = inactive	
PCON	set peaking amplification:	PCON3	PCON2	PCON1	PCON0	grade of peaking
	inverse 4-bit-value:	1	1	1	1	–6 dB
	each step 1 dB	1	1	1	0	–5 dB
		.	.	.	.	.
		.	.	.	.	.
		.	.	.	.	.
		1	0	0	1	0 dB
		.	.	.	.	.
		.	.	.	.	.
		.	.	.	.	.
		0	0	0	0	+9 dB

Remarks to the subaddress bytes

Hex subaddresses 00 to 0F are reserved for colour decoders and RGB processors.
Subaddresses 10 and 11 only are acknowledged.
General call address is not acknowledged.
Power-on reset: D7 to D1 bits of data bytes are set to 0, D0 bit is set to 1.

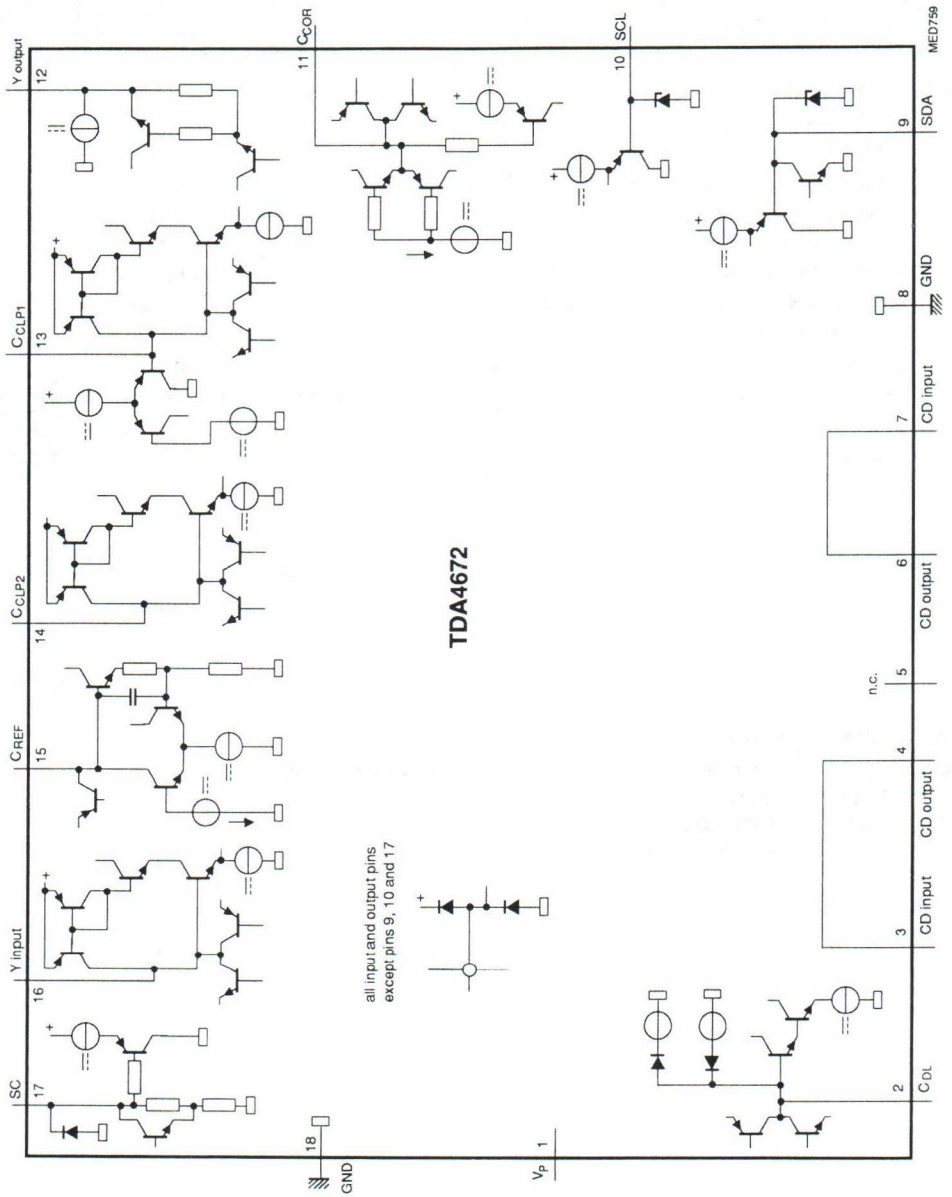


Fig.4 Internal circuit.

Video processor with automatic cut-off and white level control

TDA4680

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two fully-controlled, analog RGB inputs, selected either by fast switch signals or via I²C-bus
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, horizontal and vertical synchronization, cut-off and white level timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Software-based automatic white level control or fixed white levels via I²C-bus
- Cut-off and white level measurement pulses in the last 4 lines of the vertical blanking interval (I²C-bus selection for PAL, SECAM, or NTSC, PAL-M)
- Increased RGB signal bandwidths for progressive scan and 100 Hz operation (selected via I²C-bus)
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Three adjustable reference voltage levels (via I²C-bus) for automatic cut-off and white level control
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555, TDA4650/T, TDA4655/T or TDA4657.

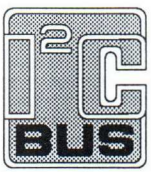
There is a very similar IC TDA4681 available. The only differences are in the NTSC matrix.

GENERAL DESCRIPTION

The TDA4680 is a monolithic integrated circuit with a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from multistandard colour decoders, TDA4555, TDA4650/T, TDA4655/T or TDA4657, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals for microprocessor control.



Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator; both inputs are fully-controlled internally. The TDA4680 includes full I²C-bus control of all parameters and functions with automatic cut-off and white level control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	85	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4680	28	DIL	plastic	SOT117
TDA4680WP	28	PLCC	plastic	SOT261CG

Video processor with automatic cut-off and white level control

TDA4680

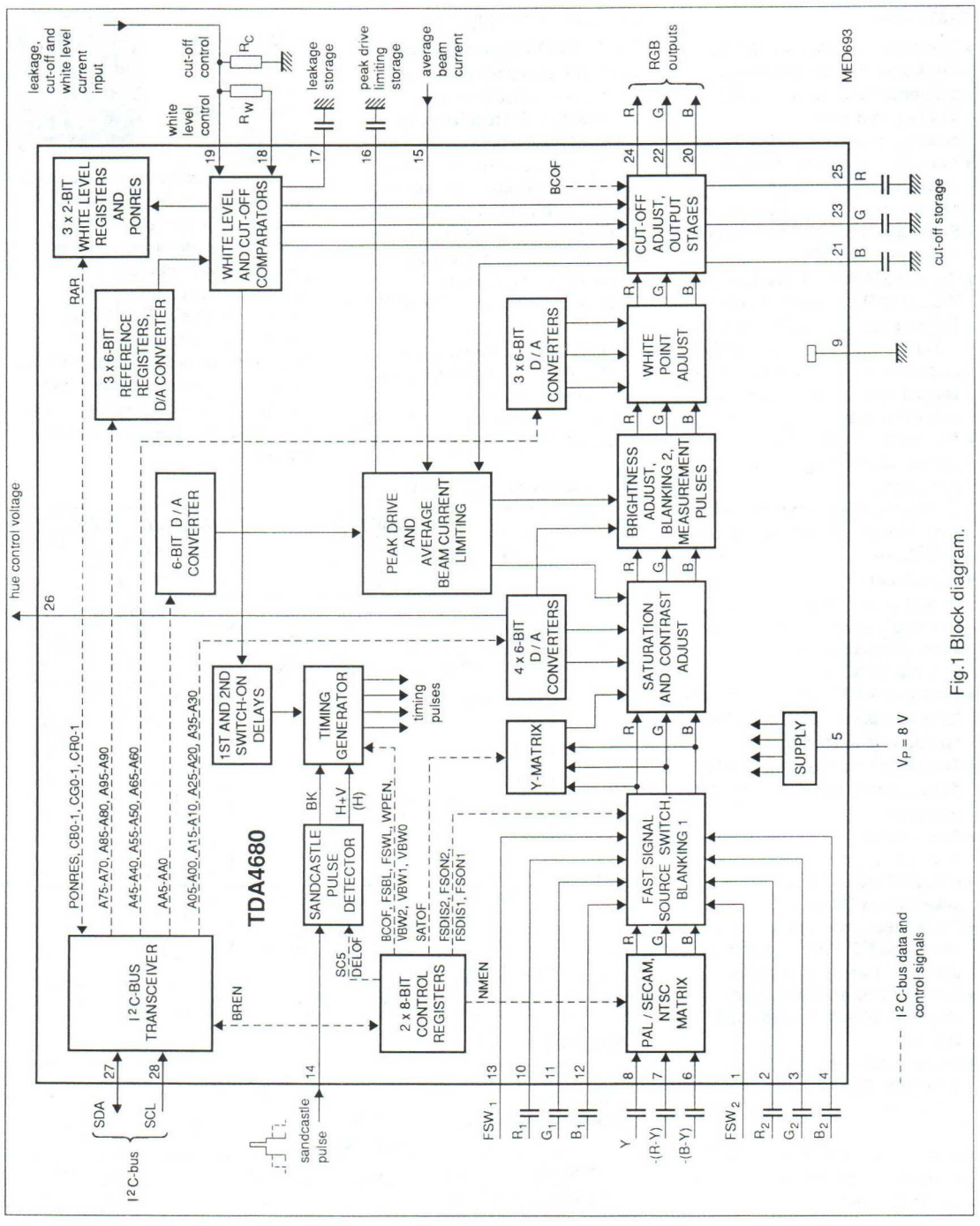


Fig.1 Block diagram.

Video processor with automatic cut-off and white level control

TDA4680

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
WI	18	white level measurement input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

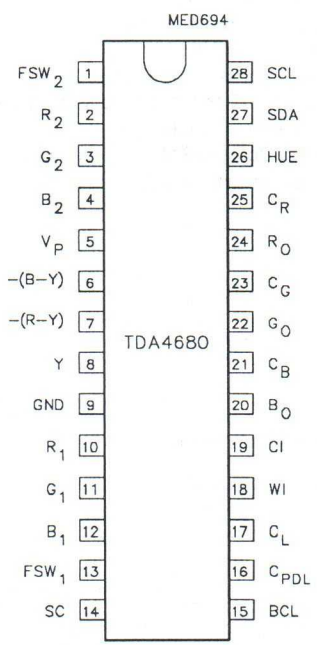


Fig.2 Pin configuration for DIL package.

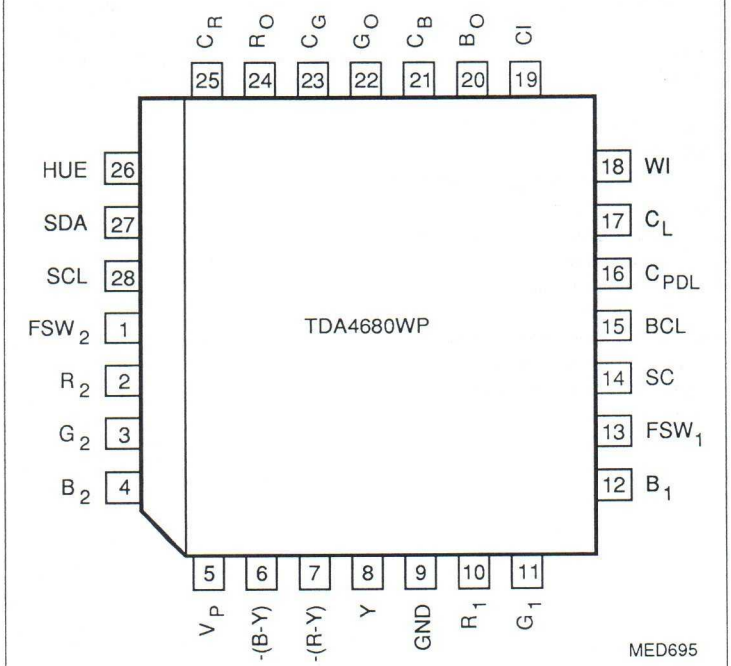


Fig.3 Pin configuration for PLCC package.

I²C-BUS CONTROL

The I²C-bus transmitter/receiver provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting
- selection of the vertical blanking interval and measurement lines for cut-off and white level control according to transmission standard
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables/disables input clamping pulse delay
- enables/disables white level control
- enables cut-off control / enables output clamping
- enables/disables full screen white level
- enables/disables full screen black level
- selects either PAL/SECAM or NTSC matrix
- enables saturation adjust / enables nominal saturation
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- reads the result of the comparison of the nominal and actual RGB signal levels for automatic white level control.

I²C-BUS TRANSMITTER / RECEIVER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits/receives data from the I²C-bus transceiver in the TDA4680 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This consists of the module address, 1000100_2 for the TDA4680, plus the $R/\overline{W}$ bit (see Fig.4). When the TDA4680 is a slave receiver ($R/\overline{W} = 0$) the module address byte is 10001000_2 (88 Hex). When the TDA4680 is a slave transmitter ($R/\overline{W} = 1$) the module address byte is 10001001_2 (89 Hex).

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.5 and Fig.6. Without auto-increment (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.5).

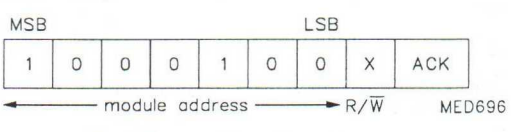


Fig.4 The module address byte.

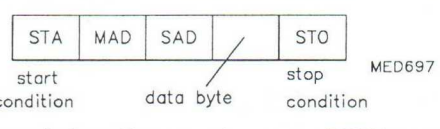


Fig.5 Data transmission without auto-increment (BREN = 0 or 1).

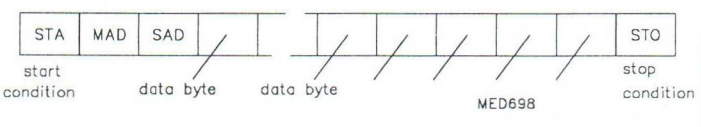


Fig.6 Data transmission with auto-increment (BREN = 0).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.
If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.6).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device and neither auto-increment nor any other internal operation takes place (For versions V1 to V5 sub-addresses outside the range 00 and 0F are acknowledged but neither auto-increment nor any other internal operation takes place).
Sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:
- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

VBWx (Vertical Blanking Window):
x = 0, 1 or 2. VBWx selects the vertical blanking interval and positions the measurement lines for cut-off and white level control.
The actual lines in the vertical blanking interval after the start of the V pulses selected as measurement lines for cut-off and white level control are shown in Table 2.
The standards marked with (*) are for progressive line scan at double line frequency ($2F_L$), i.e. approximately 31 kHz.
NMEN (NTSC - Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.
WPEN (White Pulse ENable):
0 = white measuring pulse disabled
1 = white measuring pulse enabled.
BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.
The I^2C-bus transceiver does not accept any new data until this data is transferred into the data registers.
DELOF (DELay OFf) delays the leading edge of clamping pulses:
0 = delay enabled
1 = delay disabled.
SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 3).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.
FSBL - Full Screen Black Level:
0 = normal mode
1 = full screen black level (cut-off measurement level during full field).
FSWL - Full Screen White Level:
0 = normal mode
1 = full screen white level (white measurement level during full field).
SATOF - SATuration control OFf:
0 = saturation control enabled
1 = saturation control disabled, nominal saturation enabled.

I^2C-bus transmitter

(microcontroller read mode)
As an I^2C-bus transmitter, $R/\overline{W} = 1$, the TDA4680 sends a data byte from the status register to the microcontroller. The data byte consists of following bits:
PONRES, CB1, CB0, CG1, CG0, CR1, CR0 and 0, where PONRES is the most significant bit.
PONRES (Power ON RESet) monitors the state of TDA4680's supply voltage:
0 = normal operation
1 = supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage was interrupted).
When PONRES changes state from a logic LOW to a logic HIGH all data and function bits are set to logic LOW.

2-bit white level error signal

(see Table 4).
CB1, CB0 = 2-bit white level of the blue channel.
CG1, CG0 = 2-bit white level of the green channel.
CR1, CR0 = 2-bit white level of the red channel.

Table 1 Sub-address (SAD) and data bytes.

FUNCTION	SAD (HEX)	MSB DATA BYTE							LSB
		7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	DELOF	BREN	WPEN	NMEN	VBW2	VBW1	VBW0
Control register 2	0D	SATOF	FSWL	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Table 2 Cut-off and white level measurement lines.

VBW2	VBW1	VBW0	R	G	B	WHITE	STANDARD
0	0	0	19	20	21	22	PAL/SECAM
0	0	1	16	17	18	19	NTSC/PAL M
0	1	0	22	23	24	25	PAL/SECAM (EB)
1	0	0	38, 39	40, 41	42, 43	44, 45	PAL*/SECAM*
1	0	1	32, 33	34, 35	36, 37	38, 39	NTSC*/PAL M*
1	1	0	44, 45	46, 47	48, 49	50, 51	PAL*/SECAM* (EB)

Notes to Table 2

1. The line numbers given are those of the horizontal pulse counts after the start of the vertical component of the sandcastle pulse.
2. * line frequency of approximately 31 kHz.
3. (EB) is extended blanking.

Table 3 Signal input selection by the fast source switches.

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 3

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is 'don't care', and ON is the selected input signal.

Table 4 2-bit white level error signals, CX1 and CX0.

CX1	CX0	INTERPRETATION
0	0	RAR (Reset-After-Read): no new measurements since last read
1	0	actual (measured) white level less than the tolerance range
1	1	actual (measured) white level within the tolerance range
0	1	actual (measured) white level greater than the tolerance range

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	−0.1	V_P	V
	input voltage (pins 14, 15, 18 and 19)	−0.7	V_P + 0.7	V
	input voltage (pins 27 and 28)	−0.1	8.8	V
I_{AV}	average current (pins 20, 22 and 24)	4	−10	mA
I_M	peak current (pins 20, 22 and 24)	4	−20	mA
I_{18}	input current	0	2	mA
I_{26}	output current	0.5	−8	mA
T_{stg}	storage temperature	−20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation			
	SOT117	–	1.2	W
	SOT261CG	–	1.0	W

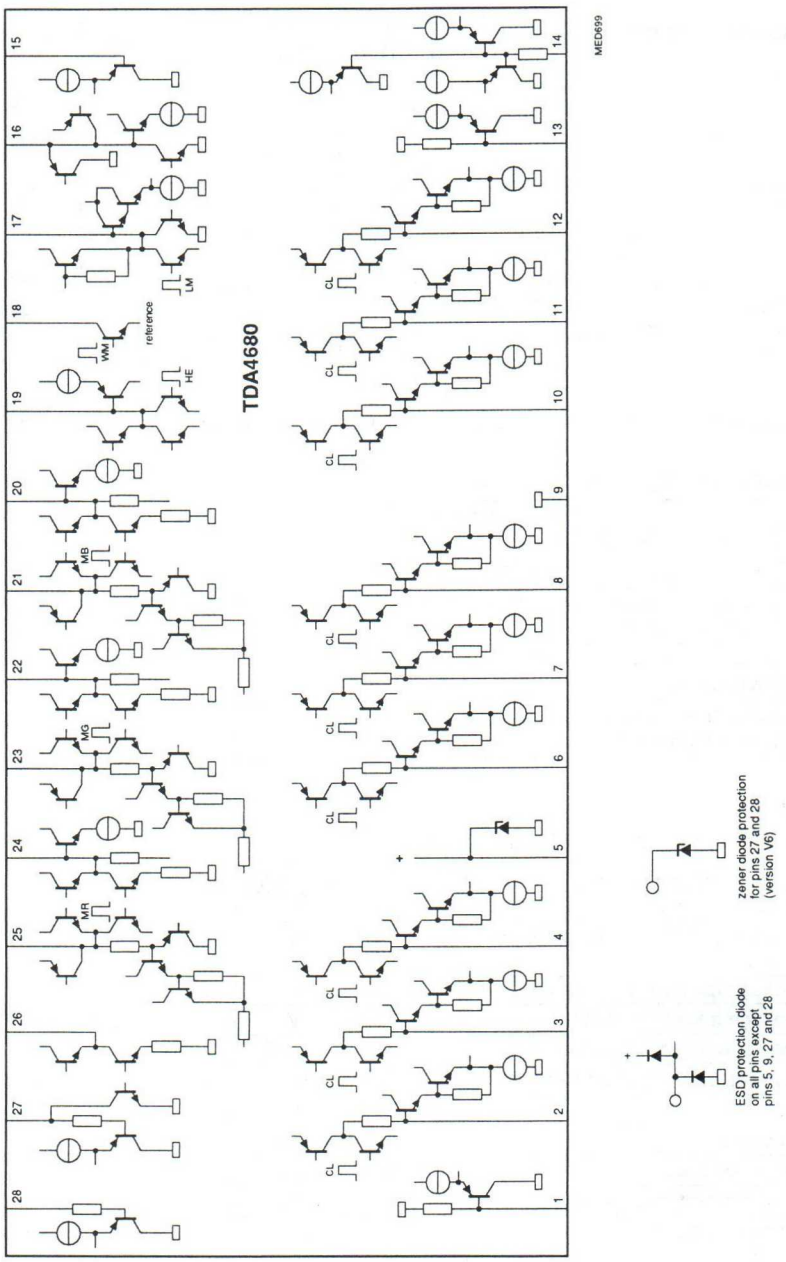


Fig.7 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.8 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = +25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	85	110	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	3.1	–	V
I_8	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.3	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.3	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (notes 3 and 4)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs (control bits: see Table 3)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs (control bits: see Table 3)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust acts on internal RGB signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation data byte 23_{Hex} for nominal saturation data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast data byte $2C_{Hex}$ for nominal contrast data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at $2C_{Hex}$	–	3	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of brightness range); data byte $3F_{Hex}$ for maximum brightness data byte 27_{Hex} for nominal brightness data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 5. data byte $3F_{Hex}$ for maximum gain data byte 22_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain:					
	increase of gain	at $3F_{Hex}$	–	60	–	%
	decrease of gain	at 00_{Hex}	–	60	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs pins 24, 22 and 20 (positive going output signals and no peak drive limitation; sub-address $0A_{Hex} = 3F_{Hex}$); see note 6.						
$V_{o(b-w)}$	nominal output signals (black-to-white value)		–	2	–	V
	maximum output signals (black-to-white value)		3.2	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	output clamping (BCOF = 1)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	65	110	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 7 and 8						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses		6.3	–	$V_P + 0.7$	V
Sandcastle pulse detector (control bit SC5 = 1) two level; note 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 0.7$	V
Sandcastle pulse detector						
I_{14}	input current	V_{14} = 0 V	–	–	100	µA
t_d	leading edge delay of the clamping pulse	control bit DELOF = 0	–	1.5	–	µs
		control bit DELOF = 1	–	0	–	µs
t_{BK}	required burst key pulse time	control bit DELOF = 0; normally used with f_L	3	–	–	µs
		control bit DELOF = 1; normally used with $2f_L$	1.5	–	–	µs
n_{pulse}	required horizontal or burst key pulses during vertical blanking interval	e.g. at interlace scan (VBW2 = 0)	4	–	29	
		e.g. at progressive line scan (VBW2 = 1)	8	–	57	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	6.5	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Automatic cut-off and white level control (notes 11, 12 and 13) see Fig.10						
V_{19}	permissible voltage (also during scanning period)		–	–	$V_P - 1.4$	V
I_{19}	output current		–	–	–140	µA
	input current		150	–	–	µA
	additional input current	during monitor pulse	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1	–	$V_{pdl} - 0.7$	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	5.0	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	3.0	–	V
data byte 07_{Hex} for red reference level data byte 08_{Hex} for green reference level data byte 09_{Hex} for blue reference level						
ΔV_{19}	difference between V_{MEAS} (cut-off or white level measurement voltage) and V_{REF}	$3F_{Hex}$ (maximum V_{MEAS})	1.5	–	–	V
		20_{Hex} (nominal V_{MEAS})	–	1.0	–	V
		00_{Hex} (minimum V_{MEAS})	–	–	0.5	V
I_{18}	input current	white level measurement	–	–	800	µA
R_{18}	internal resistance	to V_{REF}; $I_{18} \leq 800$ µA	–	100	–	Ω
ΔV_{19}	white level register (measured value within tolerance range)	white level measurement	–	250	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	µA
V_{17}	voltage for reset to switch-on below		–	< 3.0	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.0	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA
I^2C-bus transceiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_d	pulse delay time LOW		4.7	–	–	µs
	pulse delay time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I^2C-bus transceiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B–Y) and –(R–Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):
   $V_{R-Y}^* = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y}^* = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B–Y)* demodulator axis	0°	0°
(R–Y)* demodulator axis	115°	90°
(R–Y)* amplification factor	1.97	1.14
(B–Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27V_{R-Y}^* - 0.22V_{B-Y}^*$.
4. The vertical blanking interval is selected via the I^2C-bus (see Table 2 and Fig.10). Vertical blanking is determined by the vertical component of the sandcastle pulse; this vertical component has priority when it is longer than the vertical blanking interval of the transmission standard.
5. The white potentiometers affect the amplitudes of the RGB output signals including the white measurement pulses.
6. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
7. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.0 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
8. A sandcastle pulse with a maximum voltage equal to (V_P + 0.7 V) is obtained by limiting a 12 V sandcastle pulse.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. The vertical blanking interval is defined by a V pulse which contains 4 (8) or more H pulses; it begins with the start of the V pulse and ends with the end of the white measuring line. If the V pulse is longer than the selected vertical blanking window the blanking period ends with the end of the complete line after the end of the V pulse. The counter cycle time is 31 (63) H pulses. If the V pulse contains more than 29 (57) H pulses, the black level storage capacitors will be discharged while all signals are blanked. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Figs 9 and 10).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 5.0 V, the monitor pulse is switched off and cut-off and white level control are activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

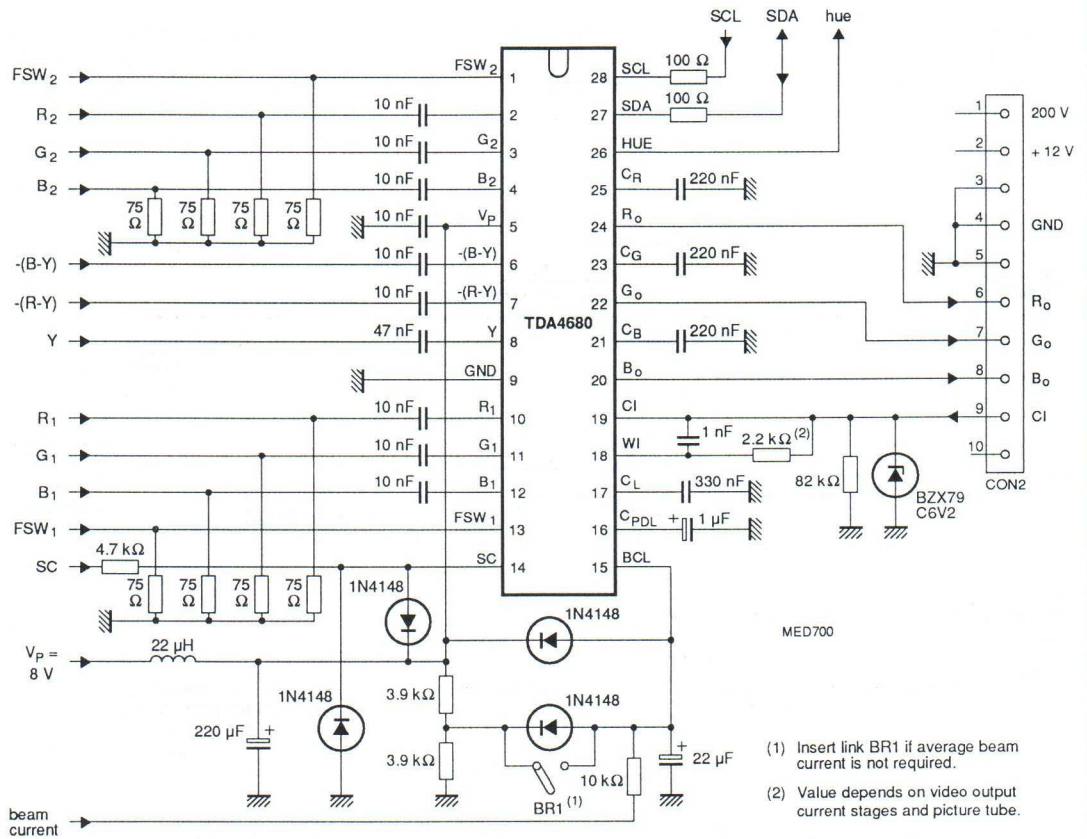


Fig.8 Test and application circuit.

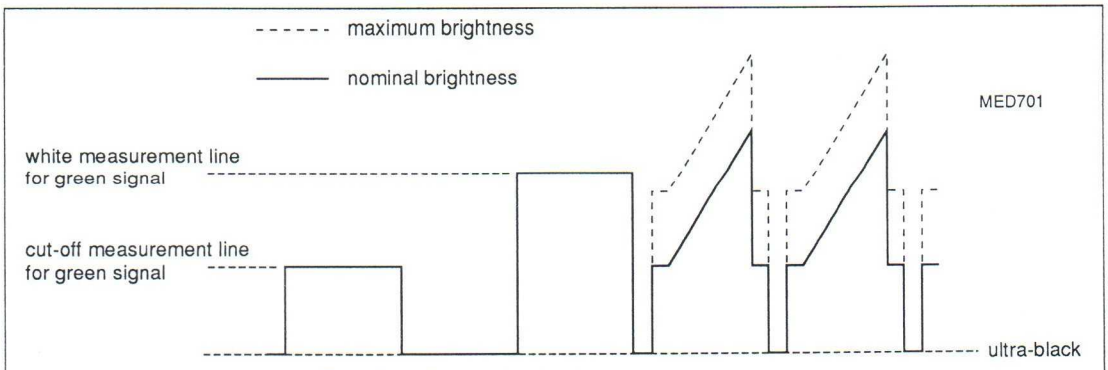


Fig.9 Cut-off and white level measurement pulses.

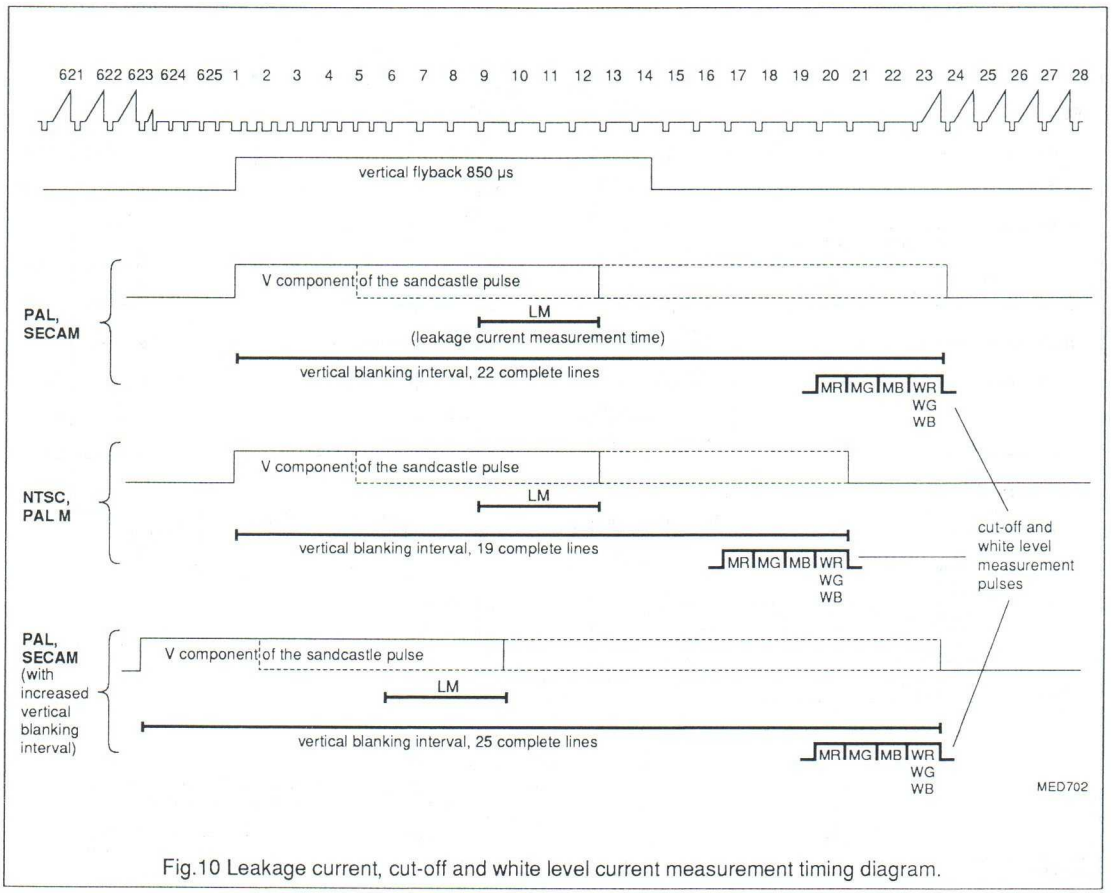


Fig.10 Leakage current, cut-off and white level current measurement timing diagram.

Video processor with automatic cut-off control TDA4685

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I^2C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast, brightness and white adjustment via I^2C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control or clamped output selectable via I^2C-bus
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I^2C-bus
- Emitter-follower RGB output stages to drive the video output stages
- I^2C-bus controlled DC output e. g. for hue-adjust of NTSC (multistandard) decoders

GENERAL DESCRIPTION

The TDA4685 is a monolithic, integrated circuit with a luminance and a colour difference interface for video processing in TV receivers.

(*continued*)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4685	28	DIL	plastic	SOT117

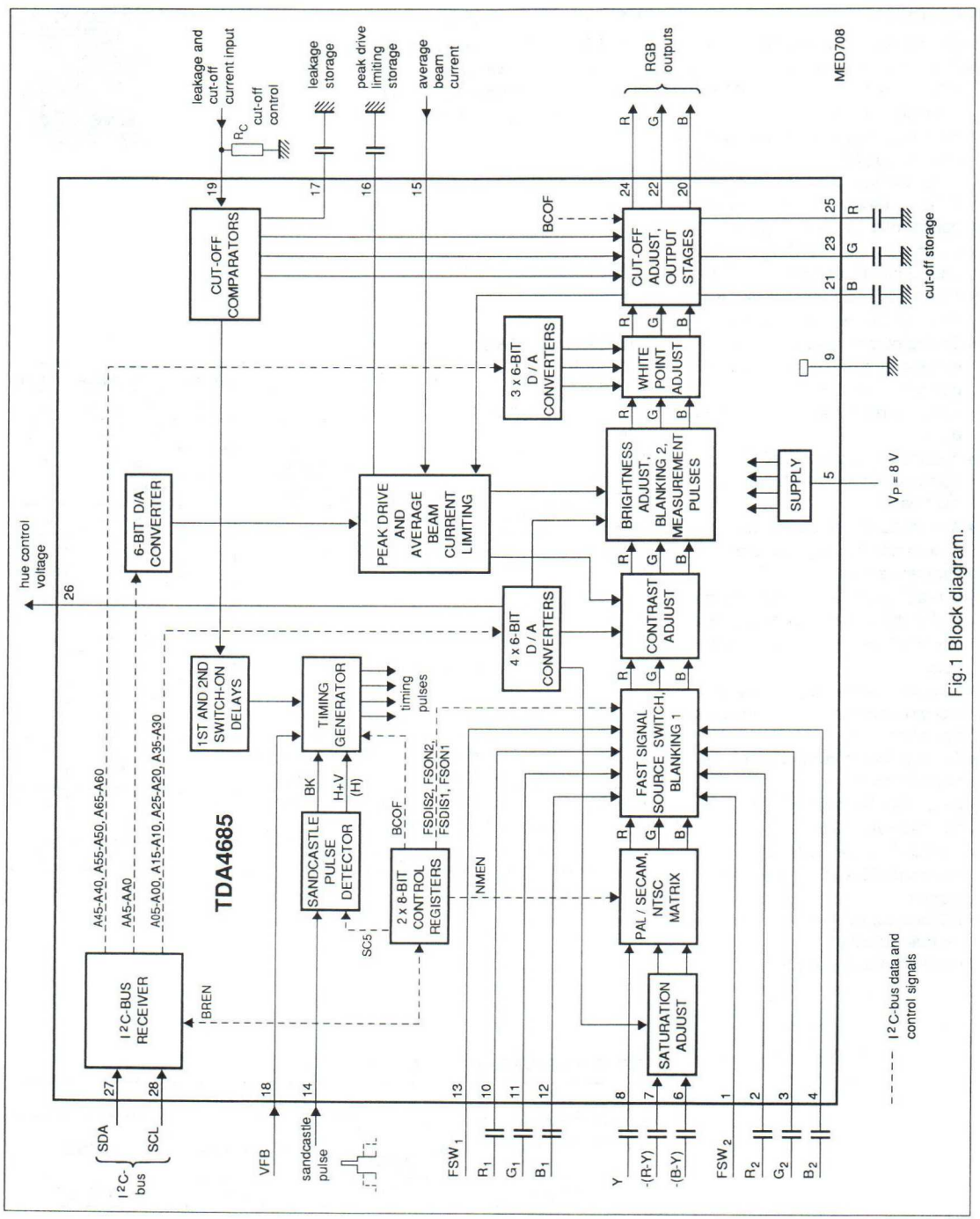


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input / acknowledge output
SCL	28	I^2C-bus serial clock input

GENERAL DESCRIPTION

(continued)

Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e. g. with the multistandard decoder TDA4655 or TDA9160 plus delayline TDA4661 and the Picture Signal Improvement (PSI) IC TDA467X or from a Feature Module. The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4685 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4685 then the I^2C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not adjustable via I^2C-bus
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The TDA4686 is like TDA4685 but intended for double line frequency application.

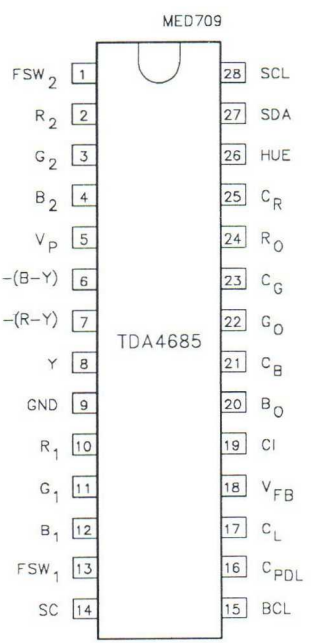


Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- DC output e. g. for hue control
- RGB gain adjust
- peak drive limiting level adjust
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control / enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- enables Y-CD, RGB1 or RGB2 input.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA4685 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit.

A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to the I²C-bus receiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4685 is a slave receiver ($R/\overline{W} = 0$), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. Without auto-increment (BREN = 0 or 1) the Module ADdress (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

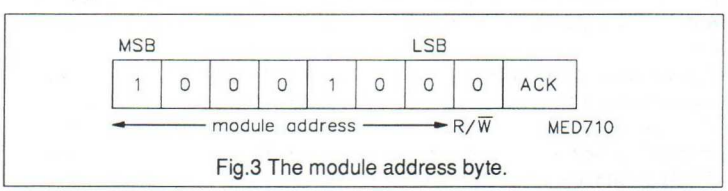


Fig.3 The module address byte.

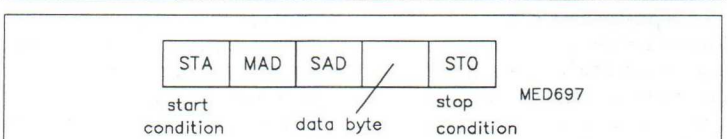


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

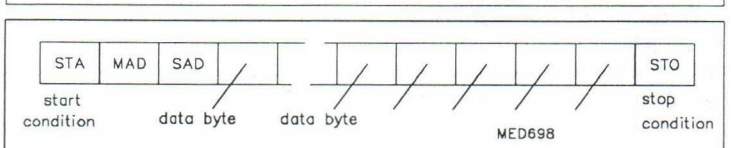


Fig.5 Data transmission with auto-increment (BREN = 0).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.
If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.5).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device.
The sub-addresses are stored in the TDA4685 to address the following parameters and functions, see Table 1:
- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

NMEN (**N**TSC-Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.
BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.
The I^2C-bus receiver does not accept any new data until this data is transferred into the data registers.
SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

Table 1 Sub-address (SAD) and data bytes.

FUNCTION	SAD (HEX)	MSB			DATA BYTE				LSB
		7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Note to Table 1

X is 'don't care', but for software compatibility with other or future video ICs it is recommended to set all 'X' to '0'.

Table 2 Signal input selection by the fast source switches.

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is 'don't care', and ON is the selected input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	−0.1	V_P	V
	input voltage (pins 15, 18 and 19)	−0.7	$V_P + 0.7$	V
	input voltage (pins 27 and 28)	−0.1	8.8	V
V_{14}	sandcastle pulse voltage	−0.7	$V_P + 5.8$	V
I_{AV}	average current (pins 20, 22 and 24)	−10	4	mA
I_M	peak current (pins 20, 22 and 24)	−20	4	mA
I_{26}	output current	−8	0.6	mA
T_{stg}	storage temperature	−20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation	–	1.2	W

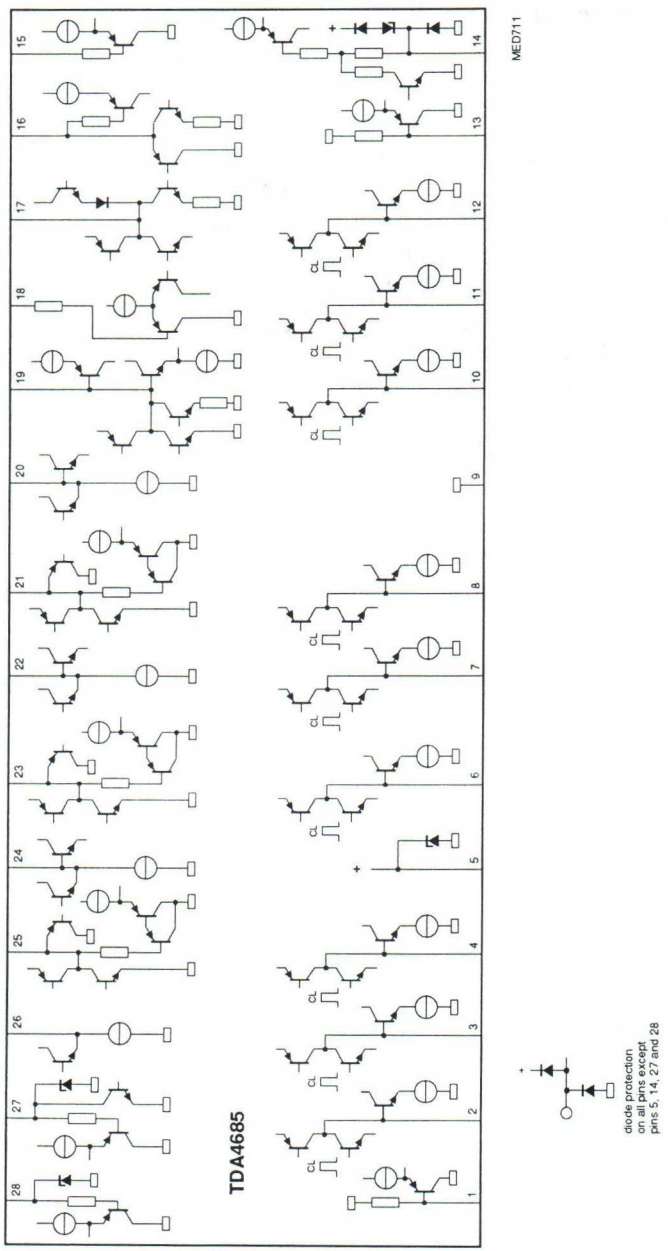


Fig.6 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = +25 °C:
– at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
– at nominal settings of brightness, contrast, saturation and white level control,
– without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				
Fast signal switch FSW$_1$ to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see Table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see Table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust acts on –(R–Y) and –(B–Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation data byte 23_{Hex} for nominal saturation data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast data byte 22_{Hex} for nominal contrast data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of maximum brightness); data byte $3F_{Hex}$ for maximum brightness data byte 26_{Hex} for nominal brightness data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs pins 24, 22 and 20 (positive going output signals; peak drive limiter set = $3F_{Hex}$); note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line ≡ voltage during ultra-black	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	$V_P + 5.8$	V
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 5.8$	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	1.5	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open-circuit; note 8	–	5.0	–	V
I_{18}	input current		–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	external voltage		–	–	$V_P - 1.4$	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1; note 12	–	$V_{pdl} - 1.0$	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} (cut-off measurement voltage) and V_{REF}		–	1.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	µA
V_{17}	threshold voltage for reset to switch-on state		–	2.5	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA
I^2C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_d	pulse delay time LOW		4.7	–	–	µs
	pulse delay time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I^2C-bus receiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B–Y) and –(R–Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):
   $V_{R-Y}^* = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y}^* = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B–Y)* demodulator axis	0°	0°
(R–Y)* demodulator axis	115°	90°
(R–Y)* amplification factor	1.97	1.14
(B–Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27V_{R-Y}^* - 0.22V_{B-Y}^*$.
4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9(b). In this case, the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open-circuit or connected to V_P. If pin 18 is always LOW neither automatic cut-off control nor output clamping can happen.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

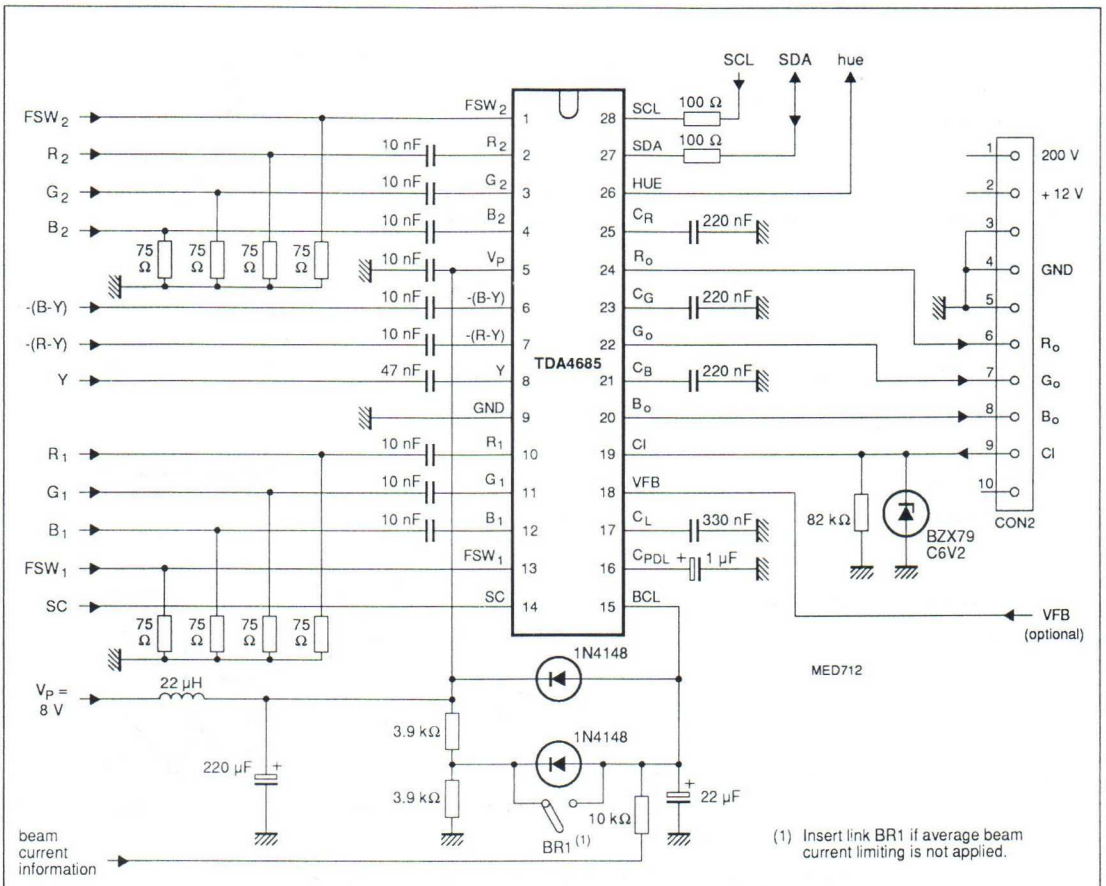


Fig.7 Test and application circuit.

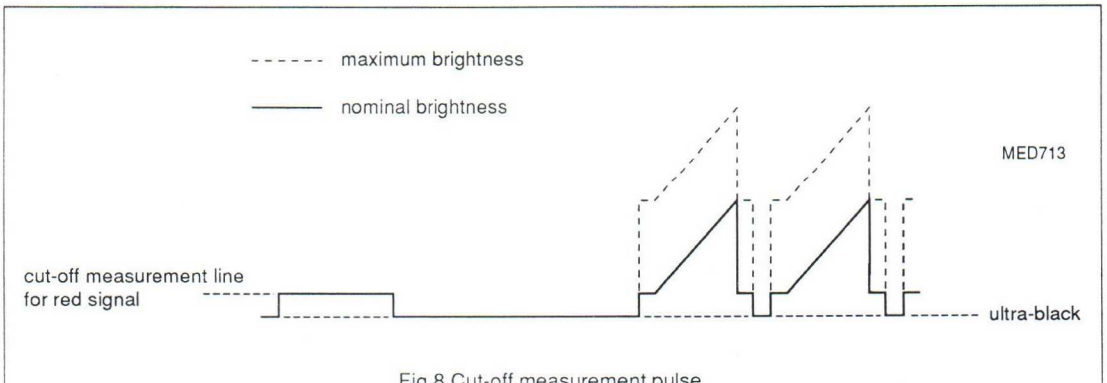


Fig.8 Cut-off measurement pulse.

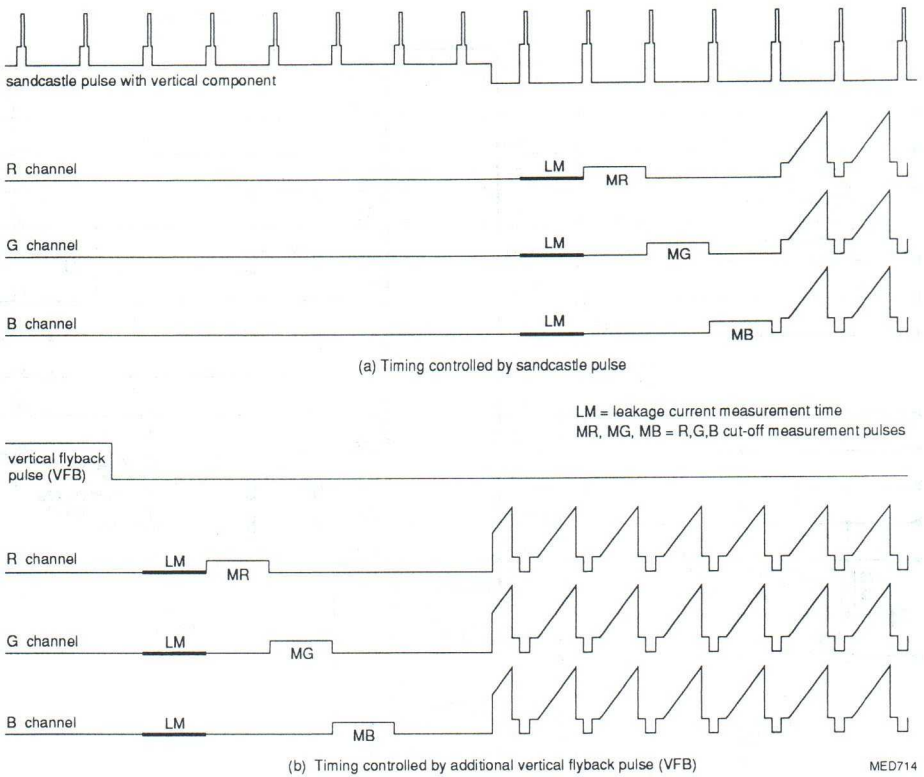


Fig.9 Leakage and cut-off current measurement timing diagram.

Video processor with automatic cut-off control TDA4686

FEATURES

- Intended for double line frequency application (100/120 Hz)
- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast, brightness and white adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control or clamped output selectable via I²C-bus
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Increased RGB signal bandwidths
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- I²C-bus controlled DC output e. g. for hue-adjust of NTSC (multistandard) decoders
- No delay of clamping pulse
- Large luminance, colour difference and RGB bandwidth

GENERAL DESCRIPTION

The TDA4686 is a monolithic, integrated circuit with a luminance and a colour difference interface for video processing in TV receivers.

(*continued*)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4686	28	DIL	plastic	SOT117
TDA4686WP	28	PLCC	plastic	SOT261CG

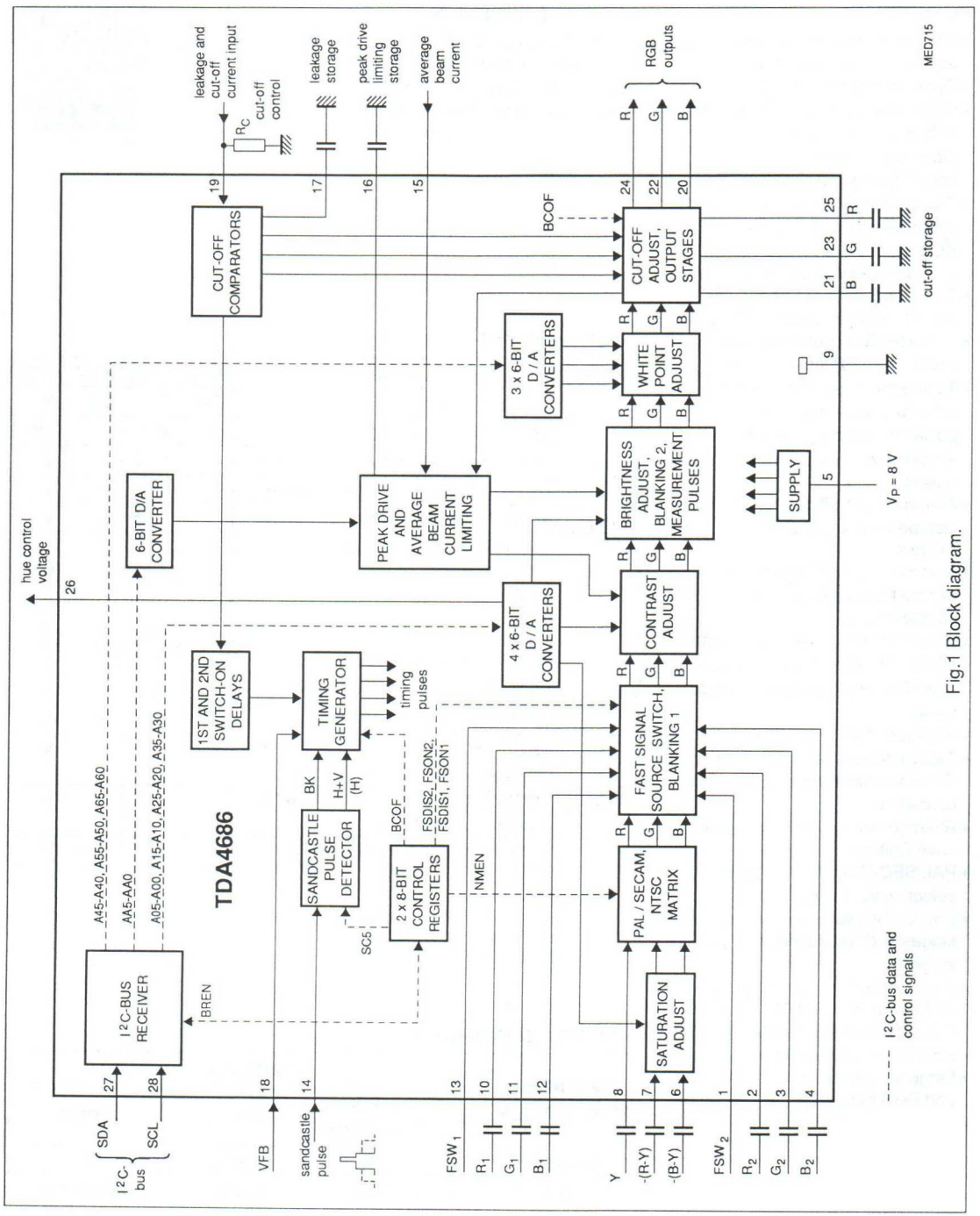


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B–Y)	6	colour difference input -(B–Y)
-(R–Y)	7	colour difference input -(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input / acknowledge output
SCL	28	I^2C-bus serial clock input

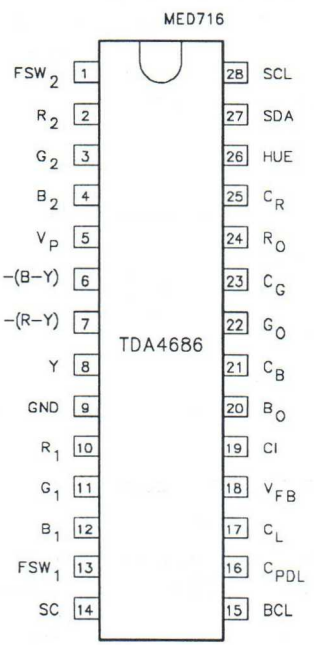


Fig.2 Pin configuration for DIL package.

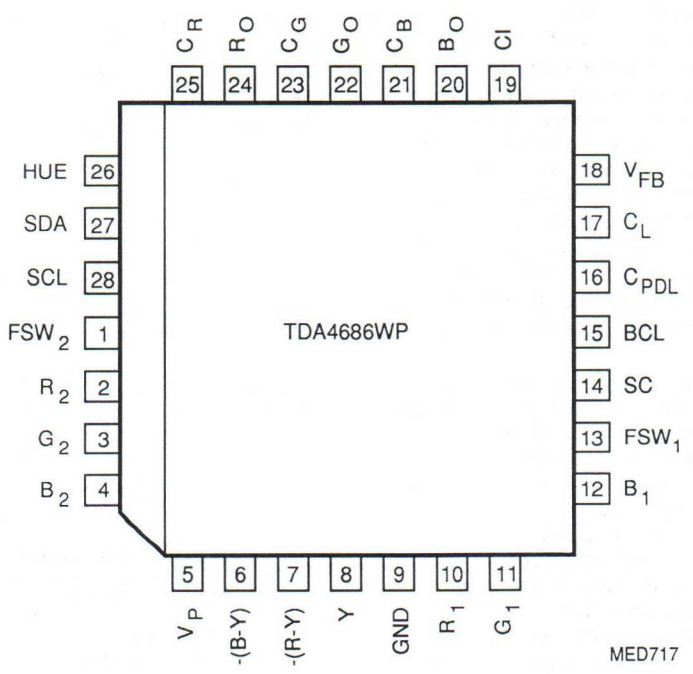


Fig.3 Pin configuration for PLCC package.

GENERAL DESCRIPTION

(continued)

Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e. g. with the multistandard decoder TDA4655 or TDA9160 plus delayline tda4661 and the Picture Signal Improvement (PSI) IC TDA467X or from a Feature Module. The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4686 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages. The TDA4686 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4686 then the I^2C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not adjustable via I^2C-bus
- no clamping delay
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The TDA4685 is like TDA4686 but intended for normal line frequency application.

I^2C-BUS CONTROL

The I^2C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- DC output e. g. for hue control
- RGB gain adjust
- peak drive limiting level adjust
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control / enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of I^2C-bus commands with the vertical blanking interval
- enables Y-CD, RGB1 or RGB2 input.

I^2C-BUS TRANSMITTER AND DATA TRANSFER

I^2C-bus specification

The I^2C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I^2C-bus receiver in the TDA4686 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit.

A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

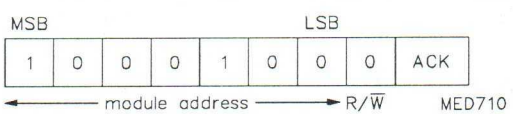


Fig.4 The module address byte.

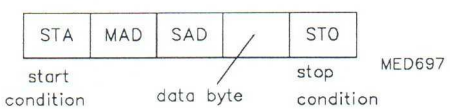


Fig.5 Data transmission without auto-increment (BREN = 0 or 1).

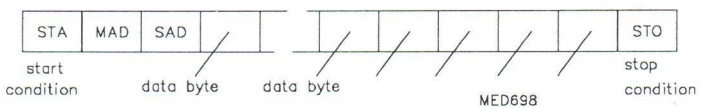


Fig.6 Data transmission with auto-increment (BREN = 0).

I²C-bus receiver

(microcontroller write mode)
Each transmission to the I²C-bus receiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4686. The TDA4686 is a slave receiver ($R/\overline{W}$ = 0), therefore the module address byte is 10001000_2 (88 Hex), see Fig.4.
The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.5 and Fig.6. Without auto-increment (BREN = 0 or 1) the Module ADdress (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.5).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I²C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.
If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.6).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device.
The sub-addresses are stored in the TDA4686 to address the following parameters and functions, see Table 1:
- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

NMEN (NTSC-Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.
BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.
The I²C-bus receiver does not accept any new data until this data is transferred into the data registers.
SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

Table 1 Sub-address (SAD) and data bytes.

FUNCTION	SAD (HEX)	MSB DATA BYTE							LSB
		7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Note to Table 1

X is 'don't care', but for software compatibility with other or future video ICs it is recommended to set all 'X' to '0'.

Table 2 Signal input selection by the fast source switches.

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is 'don't care', and ON is the selected input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	–0.1	V_P	V
	input voltage (pins 15, 18 and 19)	–0.7	V_P + 0.7	V
	input voltage (pins 27 and 28)	–0.1	8.8	V
V_{14}	sandcastle pulse voltage	–0.7	V_P + 5.8	V
I_{AV}	average current (pins 20, 22 and 24)	–10	4	mA
I_M	peak current (pins 20, 22 and 24)	–20	4	mA
I_{26}	output current	–8	0.6	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation			
	SOT117	–	1.2	W
	SOT261CG	–	1.0	W

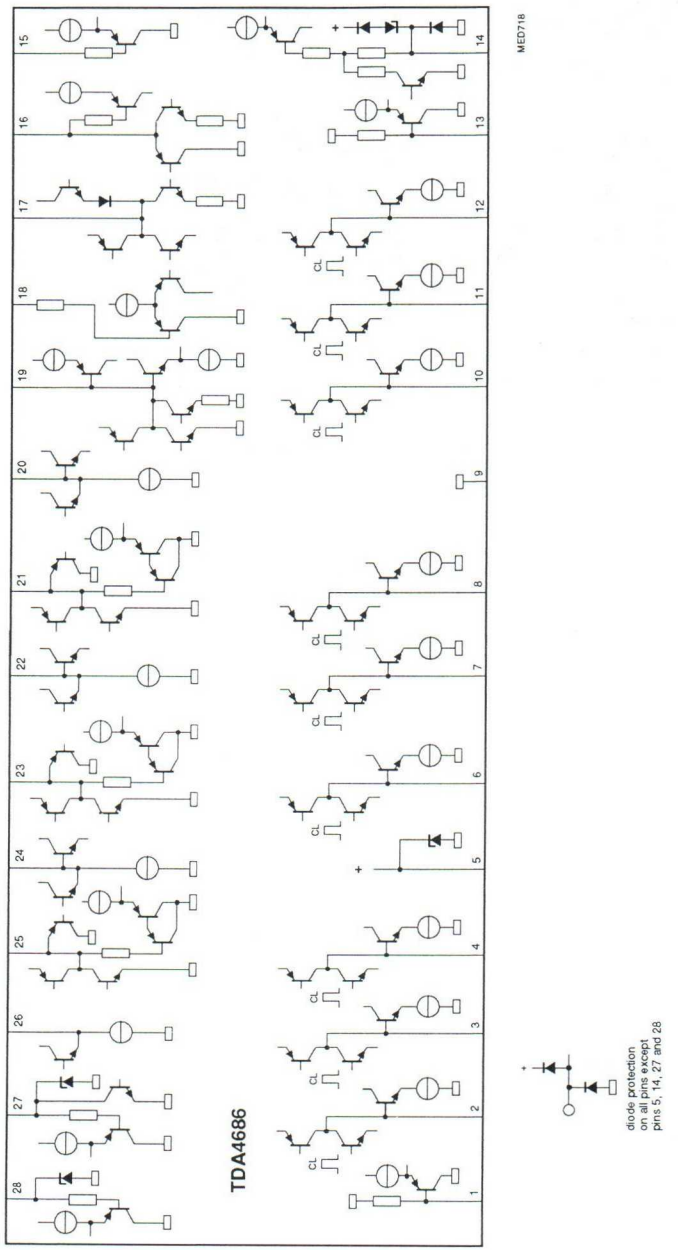


Fig.7 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.8 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = +25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				
Fast signal switch FSW$_1$ to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see Table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see Table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust acts on –(R–Y) and –(B–Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation data byte 23_{Hex} for nominal saturation data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast data byte 22_{Hex} for nominal contrast data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of maximum brightness); data byte $3F_{Hex}$ for maximum brightness data byte 26_{Hex} for nominal brightness data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain:					
	increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs pins 24, 22 and 20 (positive going output signals; peak drive limiter set = $3F_{Hex}$); note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response (measured with 10 MΩ, 30 pF external load)						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 14 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 12 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 22 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 22 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	$V_P + 5.8$	V
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 5.8$	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	0	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open-circuit; note 8	–	5.0	–	V
I_{18}	input current		–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.10						
V_{19}	external voltage		–	–	$V_P - 1.4$	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1; note 12	–	$V_{pdl} - 1.0$	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} (cut-off measurement voltage) and V_{REF}		–	1.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	µA
V_{17}	threshold voltage for reset to switch-on state		–	2.5	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA
I^2C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_d	pulse delay time LOW		4.7	–	–	µs
	pulse delay time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I^2C-bus receiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B–Y) and –(R–Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):
   $V_{R-Y}^* = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y}^* = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B–Y)* demodulator axis	0°	0°
(R–Y)* demodulator axis	115°	90°
(R–Y)* amplification factor	1.97	1.14
(B–Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27V_{R-Y}^* - 0.22V_{B-Y}^*$.
4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.10(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.10(b). In this case, the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 should be connected to V_P. If pin 18 is always LOW neither automatic cut-off control nor output clamping can happen.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.9 and Fig.10).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

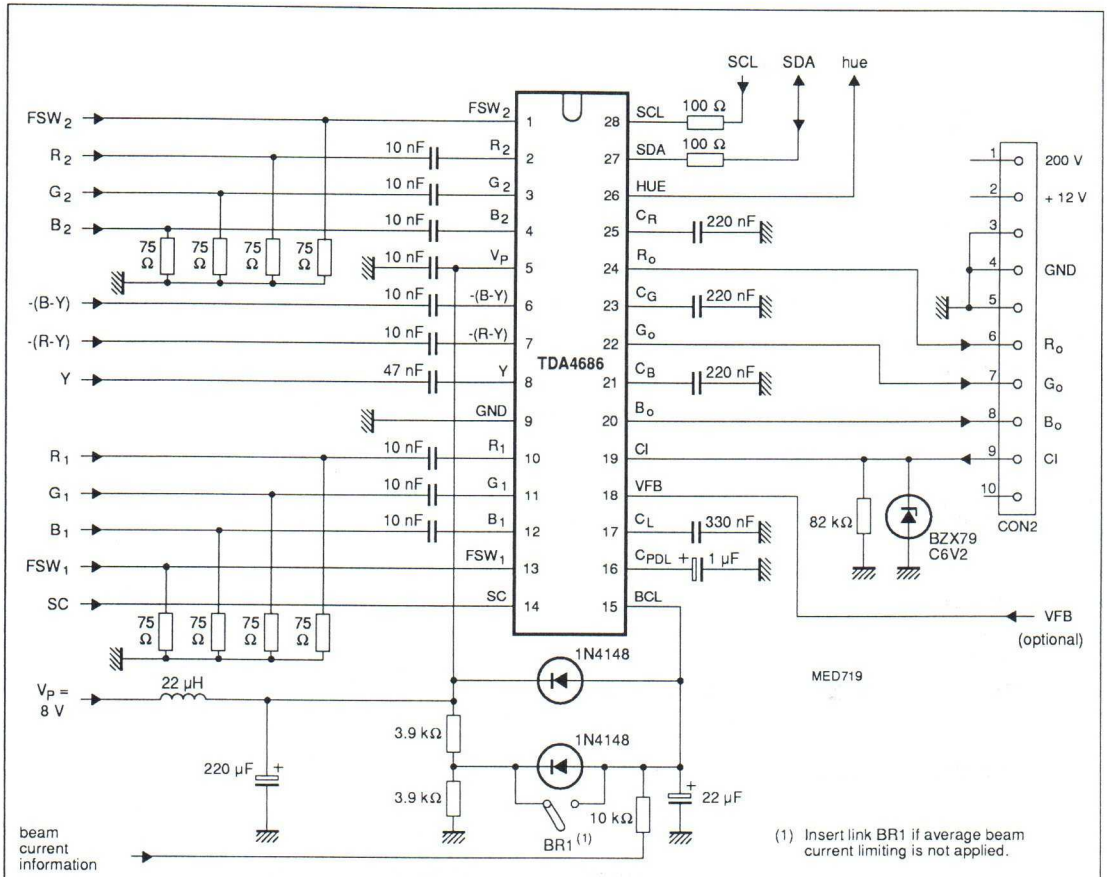


Fig.8 Test and application circuit.

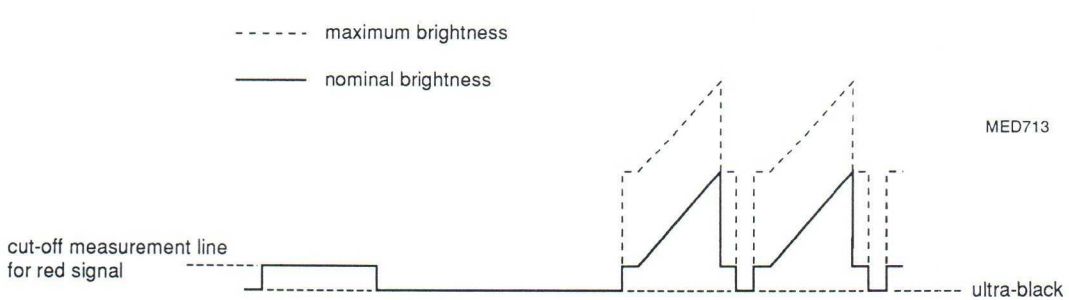


Fig.9 Cut-off measurement pulse.

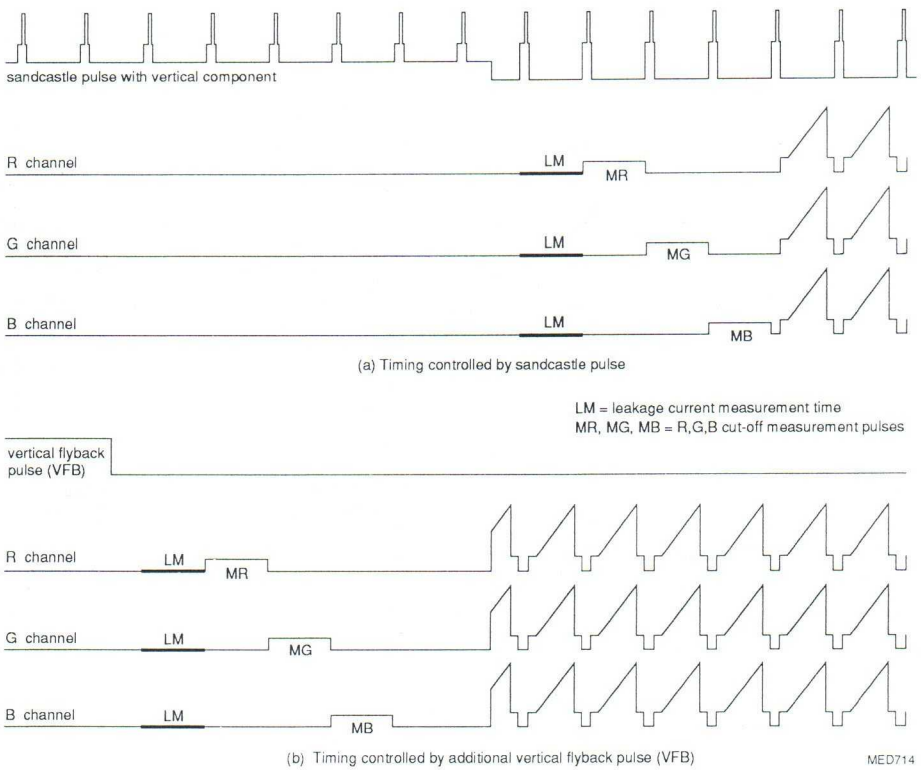


Fig.10 Leakage and cut-off current measurement timing diagram.

Video processor with automatic cut-off control TDA4688

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast, brightness and white adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control or clamped output selectable via I²C-bus
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Ultra black or nominal black blanking selectable via I²C-bus in clamped output mode
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC (Japan) matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- I²C-bus controlled DC output e. g. for hue-adjust of NTSC (multistandard) decoders
- Positive amplification factor of cut-off control voltage.

GENERAL DESCRIPTION

The TDA4688 is a monolithic, integrated circuit with a luminance and a colour difference interface for video processing in TV receivers.

(*continued*)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4688	28	DIL	plastic	SOT117

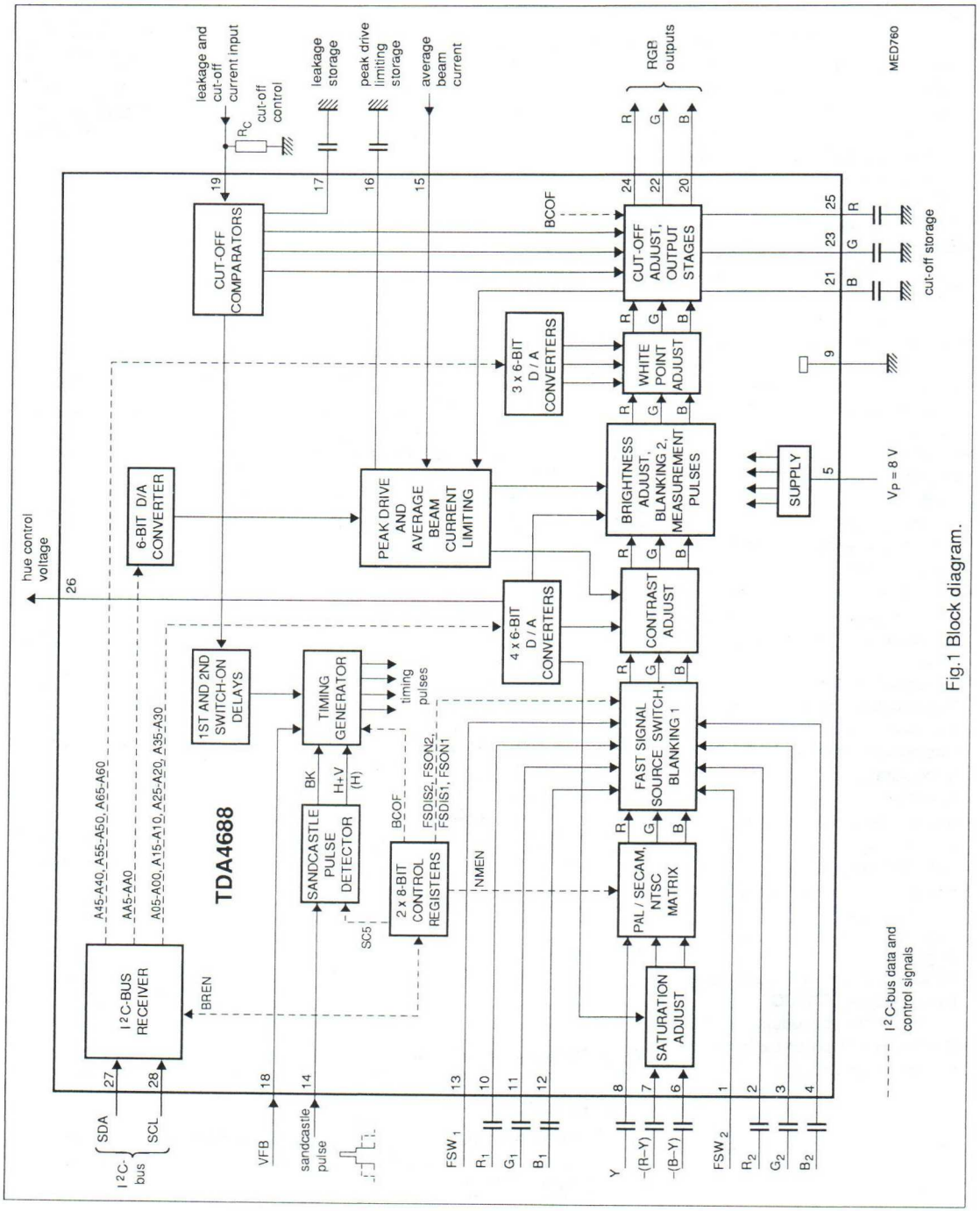


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input / acknowledge output
SCL	28	I^2C-bus serial clock input

GENERAL DESCRIPTION

(continued)

Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e. g. with the multistandard decoder TDA4655 or TDA9160 plus delay line TDA4661 and the Picture Signal Improvement (PSI) IC TDA467X or from a Feature Module. The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4688 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4688 is a simplified, pin compatible (except pin 18) version of the TDA4681. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4688 then the I^2C-bus command is not executed. The differences with the TDA4681 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not adjustable via I^2C-bus
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The difference compared to TDA4687 is the japanese type NTSC matrix.

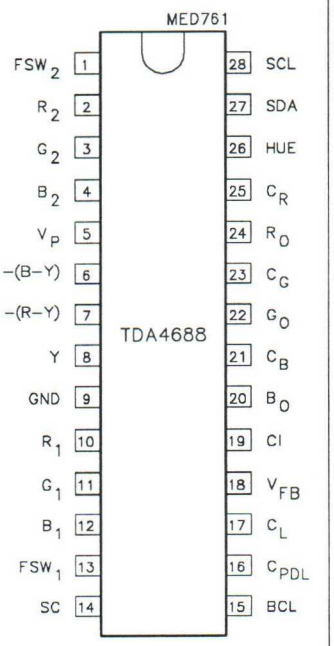


Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- DC output e. g. for hue control
- RGB gain adjust
- peak drive limiting level adjust
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control / enables output clamping (2 different modes)
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- enables Y-CD, RGB1 or RGB2 input.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA4688 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit.

A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to the I²C-bus receiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4688. The TDA4688 is a slave receiver ($R/\overline{W} = 0$), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. Without auto-increment (BREN = 0 or 1) the Module ADdress (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

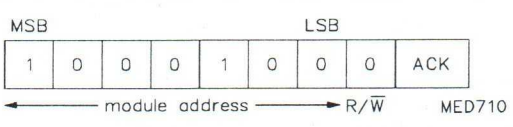


Fig.3 The module address byte.

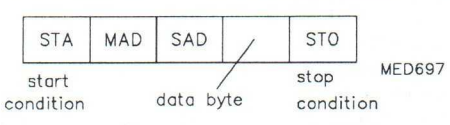


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

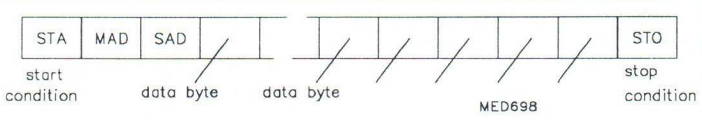


Fig.5 Data transmission with auto-increment (BREN = 0).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.
If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.5).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device.
The sub-addresses are stored in the TDA4688 to address the following parameters and functions, see Table 1:
- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

NMEN (**N**TSC-Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.
BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I^2C-bus receiver does not accept any new data until this data is transferred into the data registers.
SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

Control register 3

MOD2 (output clamp MODe2):
0 = inactive
1 = output clamping, but brightness inactive
When MOD2 = 1 and BCOF = 1 output clamp is enabled and brightness adjust is disabled (for clamping purpose of following RGB receivers).
(BCOF = 0) AND (MOD2 = 1) is senseless

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

Table 1 Sub-address (SAD) and data bytes.

FUNCTION	SAD (HEX)	MSB			DATA BYTE				LSB
		7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Control register 3	0E	x	x	MOD2	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Note to Table 1

x is 'don't care', but for software compatibility with other or future video ICs it is recommended to set all 'x' to '0'.

Table 2 Signal input selection by the fast source switches.

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is 'don't care', and ON is the selected input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	−0.1	V_P	V
	input voltage (pins 15, 18 and 19)	−0.7	V_P + 0.7	V
	input voltage (pins 27 and 28)	−0.1	8.8	V
V_{14}	sandcastle pulse voltage	−0.7	V_P + 5.8	V
I_{AV}	average current (pins 20, 22 and 24)	−10	4	mA
I_M	peak current (pins 20, 22 and 24)	−20	4	mA
I_{26}	output current	−8	0.6	mA
T_{stg}	storage temperature	−20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation	–	1.2	W

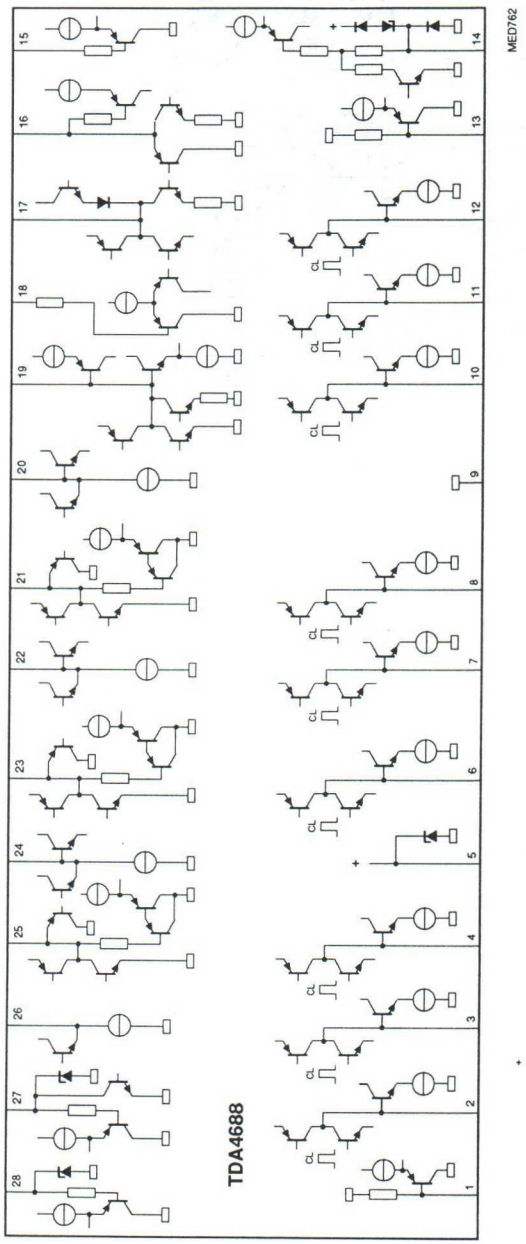


Fig.6 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = +25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				
Fast signal switch FSW$_1$ to select Y, CD or R_1, G_1, B_1 inputs Control bits FSDIS1, FSON1 (see Table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs Control bits FSDIS2, FSON2 (see Table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust Acts on –(R–Y) and –(B–Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation data byte 23_{Hex} for nominal saturation data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust Acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast data byte 22_{Hex} for nominal contrast data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust Acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of maximum brightness); data byte $3F_{Hex}$ for maximum brightness data byte 26_{Hex} for nominal brightness data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs pins 24, 22 and 20 (positive going output signals; peak drive limiter set = $3F_{Hex}$); note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line equivalent to voltage during ultra-black	BCOF = 1; output clamping	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) Three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	$V_P + 5.8$	V
Sandcastle pulse detector (control bit SC5 = 1) Two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 5.8$	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	1.5	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open-circuit; note 8	–	5.0	–	V
I_{18}	input current		–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) Internal peak drive limiting level (V_{pdl}) acts on RGB outputs I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Automatic cut-off control (notes 7, 11, 12 and 13) See Fig.9						
V_{19}	external voltage		–	–	$V_P - 1.4$	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1; note 12	–	$V_{pdl} - 1.0$	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} (cut-off measurement voltage) and V_{REF}		–	1.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	µA
V_{17}	threshold voltage for reset to switch-on state		–	2.5	–	V
Hue control (note 14) Under I^2C-bus control, sub-address 03_{Hex} Data byte $3F_{Hex}$ for maximum voltage Data byte 20_{Hex} for nominal voltage Data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA
I^2C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_d	pulse delay time LOW		4.7	–	–	µs
	pulse delay time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I^2C-bus receiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B–Y) and –(R–Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –2 degrees):
   $V_{R-Y}^* = 1.39V_{R-Y} - 0.07V_{B-Y}$; $V_{G-Y}^* = -0.46V_{R-Y} - 0.15V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B–Y)* demodulator axis	0°	0°
(R–Y)* demodulator axis	95°	90°
(G–Y)* demodulator axis	240°	236°
(R–Y)* amplification factor	1.59	1.14
(B–Y)* amplification factor	2.03	2.03
(G–Y)* amplification factor	0.606	0.698

4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9b. In this case, the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open-circuit or connected to V_P. If pin 18 is always LOW neither automatic cut-off control nor output clamping can happen.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

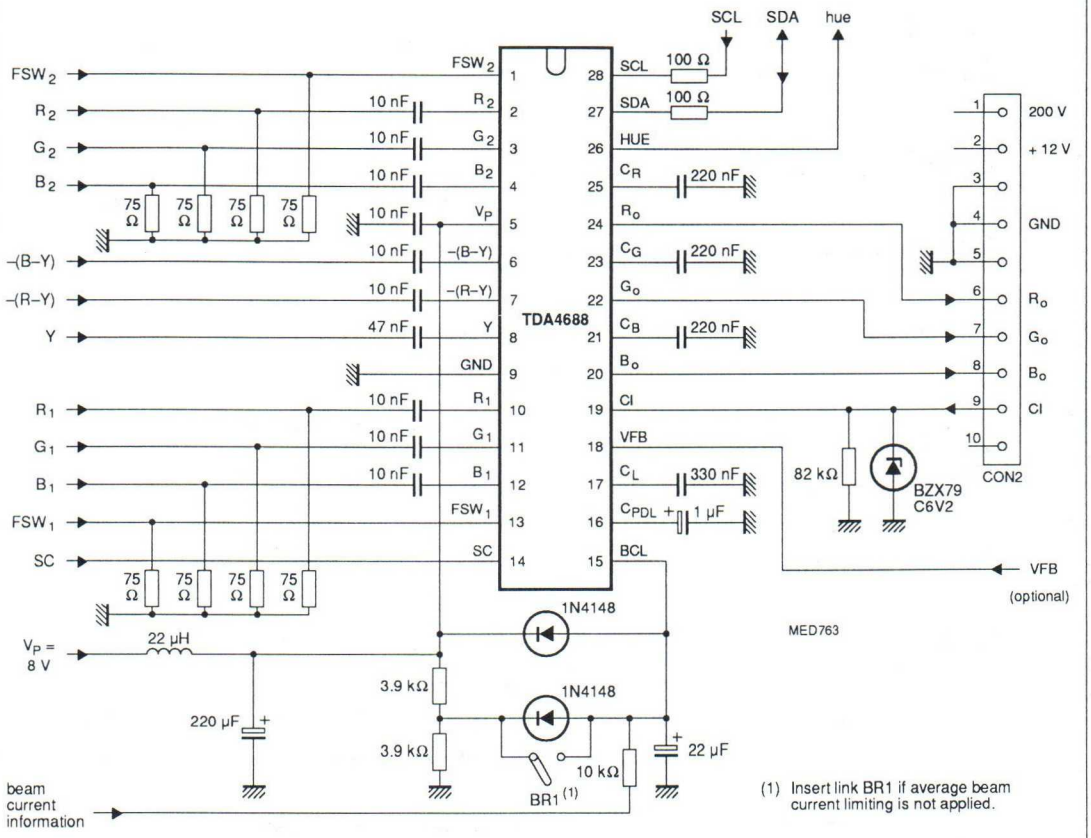


Fig.7 Test and application circuit.

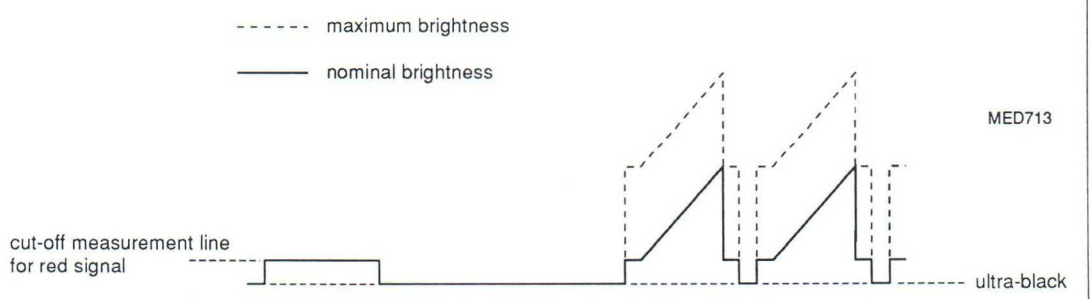


Fig.8 Cut-off measurement pulse.

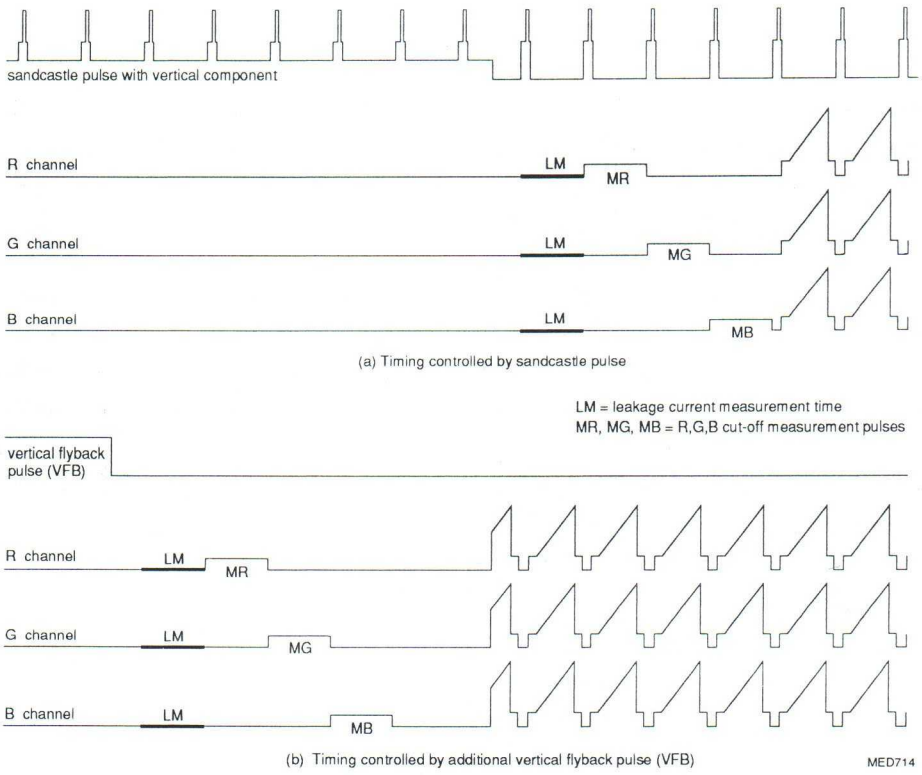


Fig.9 Leakage and cut-off current measurement timing diagram.

Sync Processor with Clock (SPC) — TDA4691

FEATURES

- Sync processor for horizontal (H) and vertical (V) sync pulses generated by internal 13.5 MHz oscillator
- Stable 'On Screen Display (OSD)', if no input signal is present with free running internal oscillator; automatic turn over to locked oscillator, if input signal is available
- External clock oscillator can be used
- Standard 50/60 Hz signals are identified automatically
- Additional outputs for 13.5 MHz, composite sync, 50/60 Hz identification, signal identification (mute), super-sandcastle 12 V
- TTL compatible outputs (H, V, composite sync and 13.5 MHz)
- 3 different time constants for the PHI1 PLL: fast, normal and slow (T_1, T_2 and T_3). Fast and normal time constant are set independent from each other
- Start of H-pulse definable by application
- Digital interference reduction for H and V signals
- Digital noise detector
- Time correction of non-standard H-pulses and equalizing pulses for optimum PLL control.

GENERAL DESCRIPTION

The TDA4691 is a bipolar integrated circuit for sync processing in 50/100 and 60/120 Hz TV sets, preferably in conjunction with the programmable deflection controller TDA9150. A line locked 13.5 MHz clock with several dividers and logic circuitry is available generating the horizontal and vertical sync outputs. The device can be assembled in a DIL20 or SO20 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P2}	supply voltage		4.5	5.0	5.5	V
I_{P2}	supply current		–	–	30	mA
V_{P1}	supply voltage		7.2	8.0	8.8	V
I_{P1}	supply current		–	–	30	mA
P_{tot}	total power dissipation		–	260	430	mW
Inputs						
V_{20}	input voltage	R_G = 1 kΩ	–	1	2	V
Outputs						
V_4	signal identification voltage	no signal; 1 mA	–	–	0.3	V
		signal	open collector	–	V_{P1}	V
V_7	50/60 Hz voltage	50 Hz; 1 mA	–	–	0.3	V
		60 Hz	open collector	–	V_{P1}	V
V_{10}	vertical output voltage	HIGH; –1 to 0 mA	2.7	–	V_{P2}	V
		LOW; 2 mA	–	–	0.8	V
V_{11}	horizontal output voltage	HIGH; –1 to 0 mA	2.7	–	V_{P2}	V
		LOW; 2 mA	–	–	0.8	V
V_{13}	clock output voltage	HIGH; –1 to 0 mA	2.7	–	V_{P2}	V
		LOW; 2 mA	–	–	0.8	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4691	20	DIL	plastic	SOT146
TDA4691T	20	SO	plastic	SOT163

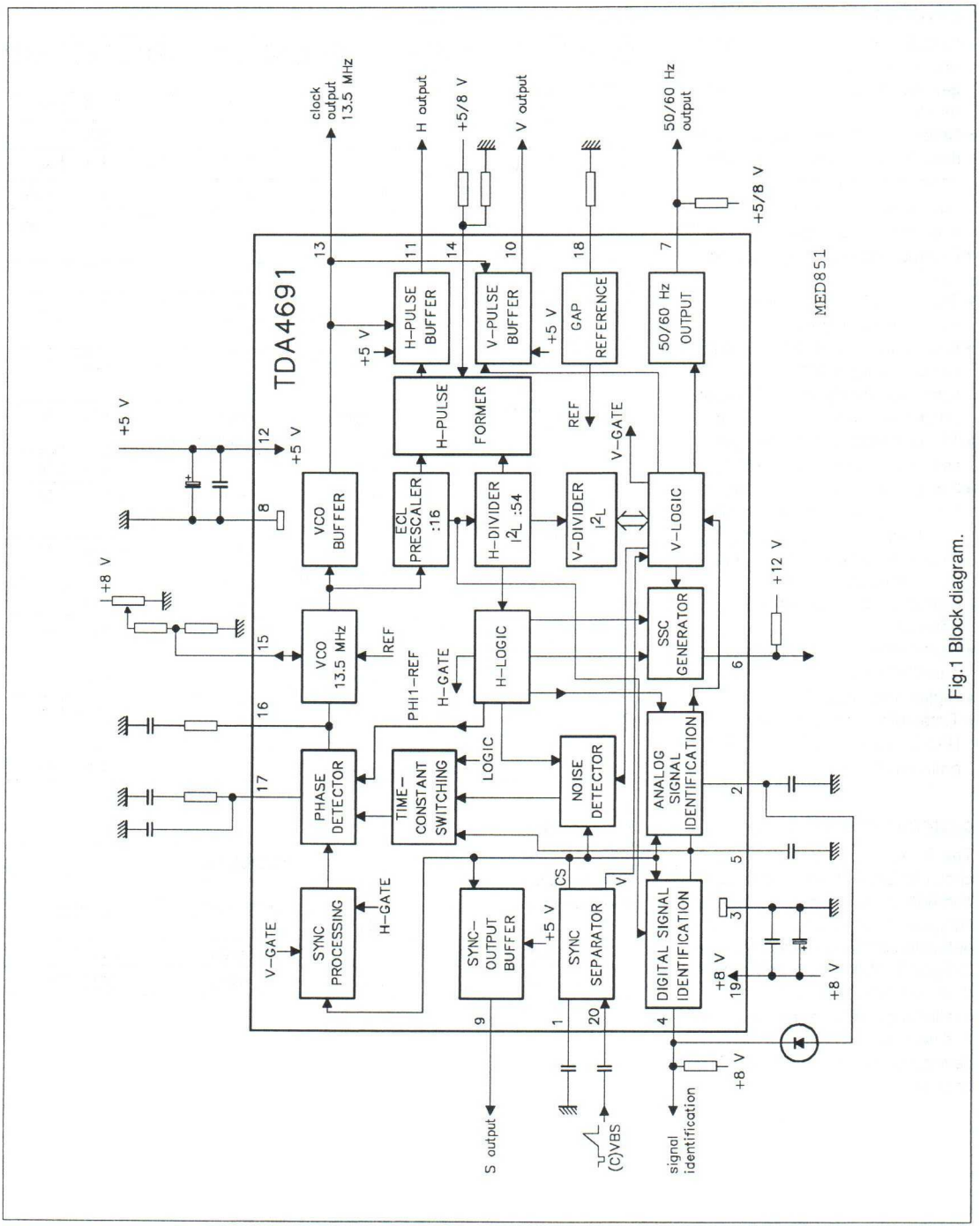


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BL	1	black level storage of sync separator
INT1	2	integration for time constant switching
GND1	3	ground for 8 V supply
SI	4	signal identification output
INT2	5	integration for signal identification
SSC	6	sandcastle output
50/60 Hz	7	50/60 Hz output
GND2	8	ground for 5 V supply
CS	9	sync output
V_{out}	10	V-output buffer
H_{out}	11	H-output buffer
V_{P2}	12	supply 5 V
CL_{out}	13	clock-output buffer
SH	14	start of H-pulse
VCOF	15	current defining VCO frequency
Fi_1	16	phase detector filtering
Fi_2	17	phase detector filtering
V_{REF}	18	reference voltage
V_{P1}	19	supply 8 V
(C)VBS	20	input sync separator

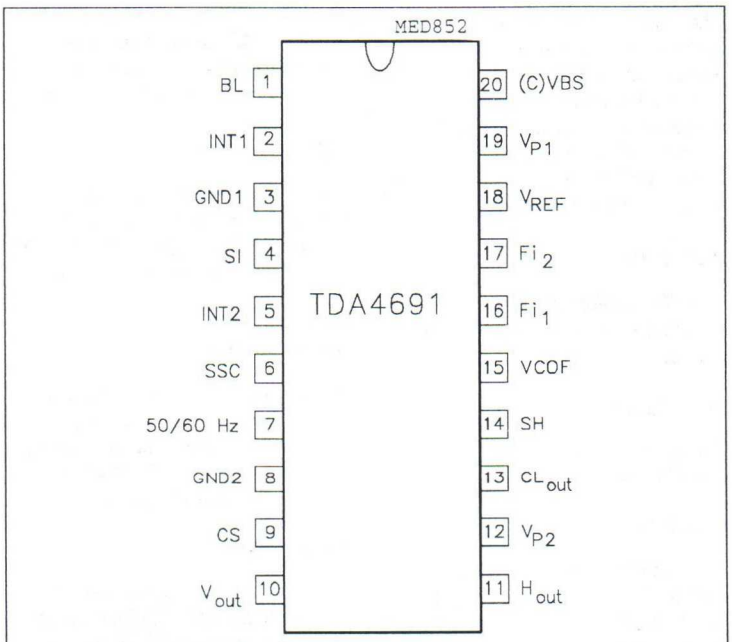


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

(See block diagram Fig.1 and timing Figs 12 to 16)

Sync separator

Top-sync and blacklevel are stored and H and V sync pulses are sliced in the middle of both levels (50%).

Sync-output buffer

This circuit turns the current pulse from the sync separator into a TTL signal.

Sync processing

This circuit assures that phase comparison can operate correctly during V-pulses. Phase jumps initiated by alternating headpulses of VCR recorders are quickly recovered. The sync processing contains the functions H/2 suppression, sync extension and sync interruption. These three functions are only active if successive pulses have a minimum distance of 1.6 µs.
The H/2 suppression operates with a gate –15 µs up to +14 µs around the PHI1-reference and is necessary for suppression of the equalizing pulses.
For sync interruption this gate is closed earlier if the detected sync is longer than 4.8 µs.
Only during V-pulses will the duration of the applied pulses be tested. If they are longer than 1.6 µs they will be recognized as sync pulses and enlarged up to 4.6 µs.

Phase detector (PHI1)

The phase detector has separate filters for the fast time constant T_1 (pin 17) and normal time constant T_2 (pins 17 and 16). The slow time constant T_3 uses the normal time constant T_2 with reduced control current. For reduction of H-pulse modulation the filter at pin 16 is switched off during sync time if normal time constant T_2 is on. Thus no frequency shifting of the oscillator is possible during sync.

Time-constant switching

This block contains a switch and an impedance converter (buffer). The switch connects the filters at pin 16 and 17 in parallel (normal time constant T_2 or slow time constant T_3). The buffer transfers the control voltage at pin 17 to pin 16 (fast time constant T_1). Which of the 2 functions is active is determined by the blocks noise detector, V-logic or signal identification.

VCO 13.5 MHz

The adjustment of the nominal frequency (13.5 MHz) is achieved at pin 15. The VCO control voltage is applied (from the phase detector) at pin 16.
The control range can be adjusted by the current at pin 18.
Pin 15 can be used to feed in an external frequency. Under these circumstances the internal VCO is switched off by application.
The control voltage at pin 16 can be used to control the external VCO.

VCO-buffer

The VCO-buffer delivers a TTL compatible signal of 13.5 MHz to pin 13.

ECL-prescaler

This block consists of a :16 asynchronous prescaler.

H-divider

This is a divider by 54. It is split into a prescaler :2 and a divider by 27. Out of this block several signals are taken for generation of H-frequently pulses in the H-logic block. These signals must have good timing. This is achieved by special synchronization.

H-logic

This block creates all pulses necessary for the SSC generator, the signal identification, the phase detector, the sync preparation and the V-divider.

V-divider

The V-divider consists of an asynchronous 10-bit divider and a decoder logic. The divider is clocked with twice the line frequency. The decoder circuit delivers the pulses necessary for the V-logic.

V-logic

In the V-logic the V-syncs from the sync separator are evaluated and noise reduced. Also certain operation states are switched ON and OFF. Additionally the reset pulse for the V-divider and the 50/60 Hz information is generated.

H-pulse former

The H-pulse starting point can be shifted in this stage, also the gate pulse of ~2.4 µs is generated for use in the digital noise identification block.

H-pulse buffer

In this circuit the line signal will be pre-synchronized by output signal of the :16 divider and synchronized by the 13.5 MHz clock. The buffer delivers TTL output signals.

V-pulse buffer

The signal out of the V-divider is synchronized with 13.5 MHz clock and converted to a TTL output level.

Gap reference

This circuit operates with the gap-principle and is stable with regard to temperature and supply voltage changes.

50/60 Hz output

This is an open-collector output, which is LOW if more than 287 lines/field are detected.

SSC generator

The SSC generator generates a 3 stage super-sandcastle pulse on an open-collector output, which is able to operate up to 12 volts. The blanking thresholds 2.5 V and 4.5 V are derived from the gap reference (point 16).

Signal identification with Digital PLL (DPLL)

The analog signal identification with output signal at pin 4 is completed with a DPLL. This PLL is able to lock on the seperated sync although the 13.5 MHz VCO is not locked on the input signal. The ratio of the lock condition to the unlock condition influences the voltage at pin 5. The detector circuit of the analog signal identification block evaluates the voltages at pins 2 and 5. If the voltage at pin 5 reaches 4 V (most of the time the PLL is locked) pin 4 will be HIGH. The voltages at pins 2 and 5 together with the state of the V-logic set the operation state of the TDA4691. The TDA4691 is able to accomodate to different input conditions automatically.

Some operation conditions can be set externally by influencing the voltages at pins 2 and 5:

1. Time constant T_1 (fast) on:
   voltage at pin 2 is limited to 5 V (0 to 5 V).
2. Time constant T_3 (slow) on:
   voltage at pin 5 is limited to 6.2 V (0 to 6.2 V).
3. Time constant T_3 (slow) inoperative:
   voltage at pin 2 is limited between 4 V and 6.5 V.
4. Time constant T_3 (slow) inoperative with input signal:
   voltage at pin 2 is limited to 6.5 V (0 to 6.5 V).
5. VCO frequency fixed to f_0:
   pin 2 is set to ground ($V_2 < 1$ V).

Noise detector

This block switches the time constant to 'slow' if on standard signal a certain noise level is reached. This noise level is measured in a small window inside the sync pulse.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage	0	9.0	V
I_{P1}	supply current	–	40	mA
V_{P2}	supply voltage	0	5.7	V
I_{P2}	supply current	–	50	mA
P_{tot}	total power dissipation	–	650	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	ESD-protection on all pins; note 1	300	–	V
$I_{I/O}$	currents on all pins except supply pins 3, 8, 12 and 19	–10	+10	mA
V_I	voltage applied to pins 1, 2, 4, 5, 7, 14 and 20	0	V_{P1}	V
V_I	voltage applied to pins 9, 10, 11 and 13	0	V_{P2}	V
V_6	voltage applied to pin 6	0	13.2	V
V_{15}	voltage applied to pin 15	0	5	V
V_{16}	voltage applied to pin 16	0	5	V
V_{17}	voltage applied to pin 17	0	5	V
V_{18}	voltage applied to pin 18	0	5	V

Note to the limiting values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146 (without heat spreader)	65 K/W
	SOT163	85 K/W

CHARACTERISTICS

V_{P1} = 8 V; V_{P2} = 5 V; measured at T_{amb} = +25 °C; unless otherwise specified; application see Figs 10 and 11; video input signal referenced to CCIR standard.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins 19 and 12; all voltages are measured with regard to ground (pins 3 and 8))						
V_{19}	supply voltage		7.2	8.0	8.8	V
I_{P1}	supply current		–	20	30	mA
V_{12}	supply voltage	same rise time as V_{19}	4.5	5.0	5.5	V
I_{P2}	supply current		–	15	30	mA
P_{tot}	total power dissipation		–	260	430	mW
Sync separator (pin 20)						
$V_{20(p-p)}$	input voltage (peak-to-peak value)	AC coupled	–	1	2	V
$V_{20(p-p)}$	sync amplitude (peak-to-peak value)		0.1	–	0.6	V
R_G	source resistor of generator		–	–	1	kΩ
I_{20}	current during sync		–	–30	–	μA
I_{20}	current during remaining time		–	1	–	μA
Black level (pin 1)						
SLH	slicing level H		–	50	–	%
SLV	slicing level V		–	50	–	%
Sync output (pin 9)						
V_9	no sync	I_9 = +1 mA	–	0.3	–	V
V_9	positive sync	I_9 = –1 mA	2.7	–	V_{12}	V
C_L	load capacitance		–	–	40	pF
t_1	time delay between pin 20 and pin 9	see Fig.3	100	200	500	ns
t_2	time delay between pin 20 and pin 9	see Fig.3	100	300	500	ns
Phase detector (pins 16 and 17)						
f_0	nominal sync frequency		–	15.625	–	kHz
f_0'	f_{osc} : 864 = phiref		–	15.625	–	kHz
I_{17}	current at sync time (fast and normal time constant)		–	±240	–	μA
I_{17}	current at sync time (slow time constant)		–	±80	–	μA
I_{16}	current at sync time	time constant T_1	–	±2	–	mA
V_{17}	filter 2 voltage		1.5	3	4.5	V
V_{16}	filter 1 voltage		1.5	3	4.5	V
$\Delta f_0/\Delta V_{16}$	VCO sensitivity	see VCO	–	360	–	kHz/V
13.5 MHz VCO (pin 15)						
R_{15}	f_0 defining resistor	see Fig.4(a)	–	3.75	–	kΩ
V_{15}	pin voltage (V_{19} dependent)	see Fig.4(a)	2.9	3	3.1	V
I_{15}	current for 13.5 MHz		–720	–800	–880	μA
g_{VCO}	transconductance at f_0		15.2	–	18.6	kHz/μA
$\Delta f_0/\Delta V_{16}$	VCO sensitivity	4% control range; depending on current at pin 18	–	360	–	kHz/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input of external oscillator (pin 15)						
V_{15}	pin voltage AC	see Fig.4(b)	1	–	3	V
V_{15}	pin voltage DC	dependent on V_{19}	–	5	–	V
R_{int}	internal resistance	see Fig.4(b)	–	7	–	kΩ
C_{int}	internal capacitance	see Fig.4(b)	–	4	–	pF
13.5 MHz buffer (pin 13)						
V_{13}	clock HIGH level output voltage	I_{13} = –1 mA; V_{12} = 4.5 V	2.7	–	V_{12}	V
V_{13}	clock HIGH level output voltage	I_{13} = 0 mA	2.7	–	V_{12}	V
V_{13}	clock LOW level output voltage	I_{13} = 2 mA; V_{12} = 5.5 V	0	–	0.8	V
t_r	rise time	see Fig.5	–	20	–	ns
t_f	fall time	see Fig.5	–	20	–	ns
D_{13}	mark-to-space ratio	V_{13} = 1.5 V	45/55	–	55/45	%
C_L	load capacitance		–	–	40	pF
ΔT_{13}	jitter on clock output (peak-to-peak value)	normal time constant T_2; measured between lines 25 and 305	–	–	2	ns
H-output buffer (pin 11)						
V_{11}	H HIGH level output voltage	I_{11} = –1 mA; V_{12} = 4.5 V	2.7	–	V_{12}	V
V_{11}	H HIGH level output voltage	I_{11} = 0 mA	2.7	–	V_{12}	V
V_{11}	H LOW level output voltage	I_{11} = 2 mA; V_{12} = 5.5 V	0	–	0.8	V
t_r	rise time	see Fig.6	–	25	–	ns
t_f	fall time	see Fig.6	–	25	–	ns
t_3	time relation pin 13 to 11	see Fig.6	–	25	55	ns
t_4	time relation pin 13 to 11	see Fig.6	3	–	–	ns
t_5	H-pulse width	see Fig.6	3.0	3.6	4.2	µs
C_L	load capacitance	see Fig.6	–	–	40	pF
Start of H-pulse (pin 14)						
I_{14}	current pin 14		–	–	±100	µA
t_{61}	time delay pulse between pin 20 and 11	see Fig.6	–1.1	–1.3	–1.5	µs
t_{62}	time delay pulse between pin 20 and 11	see Fig.6	–0.6	–0.8	–1.0	µs
t_{63}	time delay pulse between pin 20 and 11	see Fig.6	3.8	4.0	4.2	µs
t_{64}	time delay pulse between pin 20 and 11	see Fig.6	5.0	5.2	5.4	µs
V_{14} (t_{61})	voltage pin 14 (proportional to V_{19})		0	–	1	V
V_{14} (t_{62})	voltage pin 14 (proportional to V_{19})		2	2.4	2.8	V
V_{14} (t_{63})	voltage pin 14 (proportional to V_{19})		3.5	4	4.5	V
V_{14} (t_{64})	voltage pin 14 (proportional to V_{19})		5	5.5	6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V-output buffer (pin 10)						
V_{10}	V HIGH level output voltage	$I_{10} = -1$ mA; $V_{12} = 4.5$ V	2.7	–	V_{12}	V
V_{10}	V HIGH level output voltage	$I_{10} = 0$ mA	2.7	–	V_{12}	V
V_{10}	V LOW level output voltage	$I_{10} = 2$ mA; $V_{12} = 5.5$ V	0	–	0.8	V
t_r	rise time	see Fig.6	–	25	–	ns
t_f	fall time	see Fig.6	–	25	–	ns
t_3	time relation pin 13 to 10	see Fig.6	–	25	55	ns
t_4	time relation pin 13 to 10	see Fig.6	3	–	–	ns
t_5	V-pulse width	see Fig.7	280	320	350	µs
t_6	time delay between pin 20 and pin 10	see Fig.7	12	16	20	µs
C_L	load capacitance	see Fig.7	–	–	40	pF
Reference (pin 18)						
V_{REF}	reference voltage		1.1	1.2	1.3	V
R_{18}	control current defining resistor		8	–	30	kΩ
Δf	control range VCO		–	±4	–	%
$I_{18/1}$	current pin 18 (±4%)		–	105	–	µA
Δf_a	adjustable control range		±3	–	±5	%
$I_{18/3}$	current pin 18 (±3%)		–	80	–	µA
$I_{18/3}$	current pin 18 (±5%)		–	120	–	µA
50/60 Hz output (pin 7; open collector; see Fig.8)						
V_7	output voltage pin 7; 50 Hz ≥ 287.5 lines/field = LOW	$I_7 = 1$ mA	0	–	0.3	V
		$I_7 = 2$ mA	0	0.3	0.8	V
V_7	output voltage pin 7; 60 Hz ≤ 287 lines/field = HIGH		2.7	–	V_{19}	V
I_7	output leakage current		–	–	50	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle output (pin 6)						
V_6	burstkey pulse	see Fig.9	9.5	10	12	V
V_6	H-blanking pulse independent from V_{supply}		4.3	4.5	4.7	V
V_6	V-blanking pulse independent from V_{supply}		2.3	2.5	2.7	V
V_6	voltage pin 6 LOW		0	0.2	0.8	V
t_w	pulse width burstkey; 50 Hz	at 6.5 V; see Fig.9	4.0	4.3	4.7	µs
t_w	pulse width burstkey; 60 Hz	at 6.5 V; see Fig.9	3.3	3.8	4.1	µs
t_2	time relation between pin 20 and burstkey	see Fig.9	2.2	2.5	2.8	µs
t_3	time relation between pin 20 and blanking	see Fig.9	3.5	4.0	4.5	µs
t_4	H-blanking time	see Fig.9	–	11.8	–	µs
t_5	start time H-pulse pin 20 to stop time burstkey pin 6; 50 Hz	H-sync = 4.7 µs; see Fig.9	8.0	9.0	9.7	µs
t_5	start time H-pulse pin 20 to stop time burstkey pin 6; 60 Hz	see Fig.9	7.5	8.6	9.2	µs
t_6	V-blanking pulse; 50 Hz		–	–2.5 to +22.5	–	lines
t_6	V-blanking pulse; 60 Hz		–	–3.0 to +17	–	lines
Integration (pin 5)						
V_5	no TV signal	see Fig.16	0	–	2	V
	TV signal	see Fig.16	4	–	–	V
V_5	slow time constant on		5	–	6.2	V
Signal identification (pin 4; open collector via R_4 to V_{19} or V_{12})						
V_4	voltage pin 4, if no signal is identified	I_4 = 1 mA	0	–	0.3	V
		I_4 = 5 mA	0	0.2	0.8	V
V_4	voltage pin 4, if signal is identified		–	–	V_{19}	V
I_4	leakage current		–	–	50	µA
Integration (pin 2; see Fig.15)						
V_2	no signal at pin 20		–	1.5	–	V
V_2	noise at input pin 20		–	3	–	V
V_2	switching T_3 to T_1 (delay 7 fields)		–	2.5	–	V
V_2	switching T_3 to T_1 (noise and signal at input pin 20)		–	2.5	–	V
V_2	release V-divider		–	4	–	V
	hysteresis		–	–0.2	–	V
V_2	release time constant normal (T_2) signal identification at pin 4		–	5	–	V
	hysteresis		–	–0.2	–	V
V_2	release noise detector		–	6.5	–	V

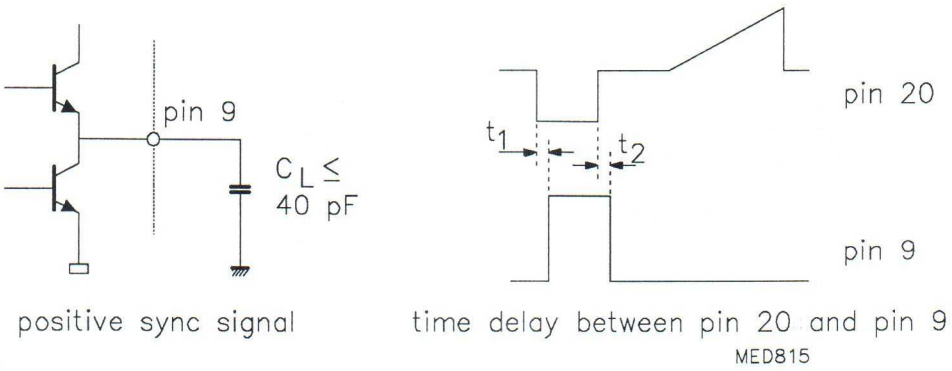


Fig.3 Sync output.

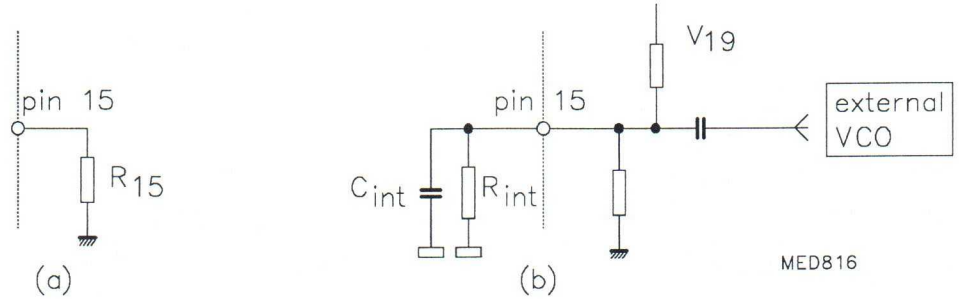


Fig.4 Pin 15 circuit for (a) internal VCO; (b) external VCO.

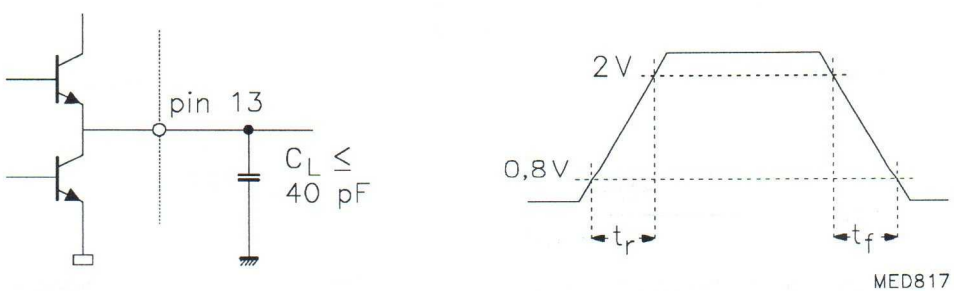
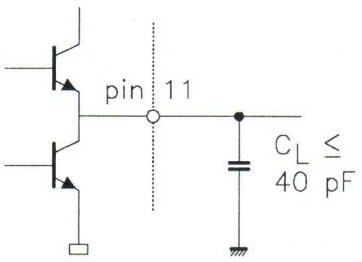
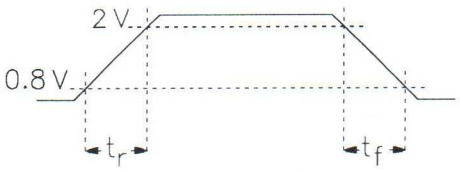


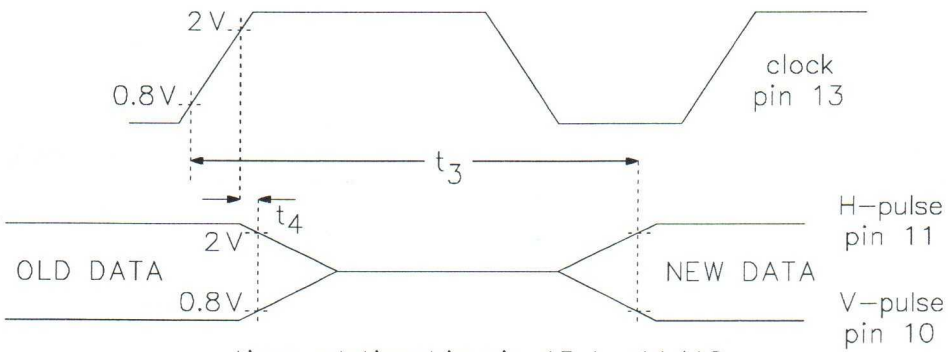
Fig.5 Clock output.



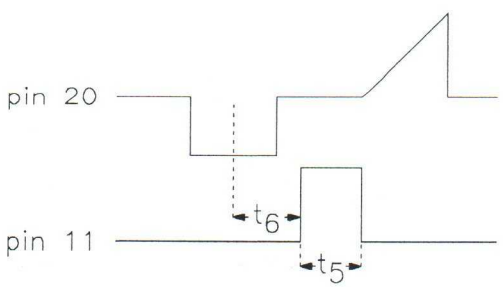
horizontal output pin 11



rise and fall time pin 10, 11



time relationship pin 13 to 11/10



timing relationship adjustable in steps with pin 14

time delay between pin 20 and pin 11

MED818

Fig.6 Time relationship of pin 10/11 to pin 13/20.

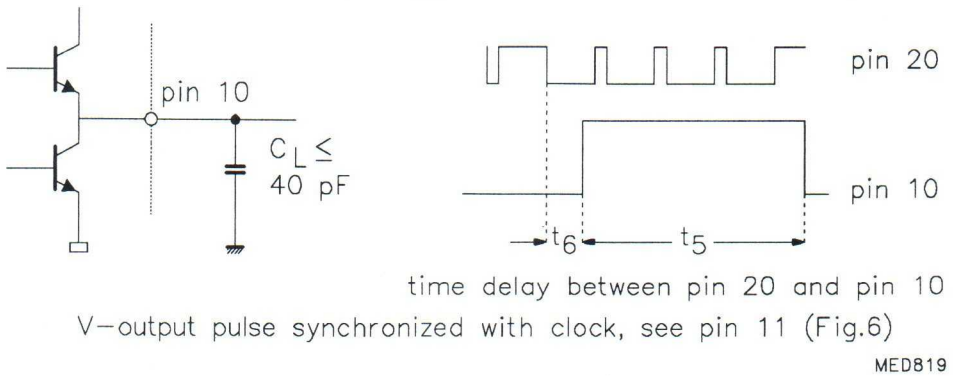


Fig.7 Time relationship pin 10 to pin 20.

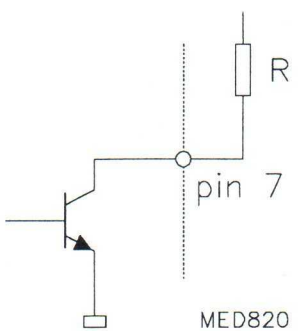


Fig.8 50/60 Hz output.

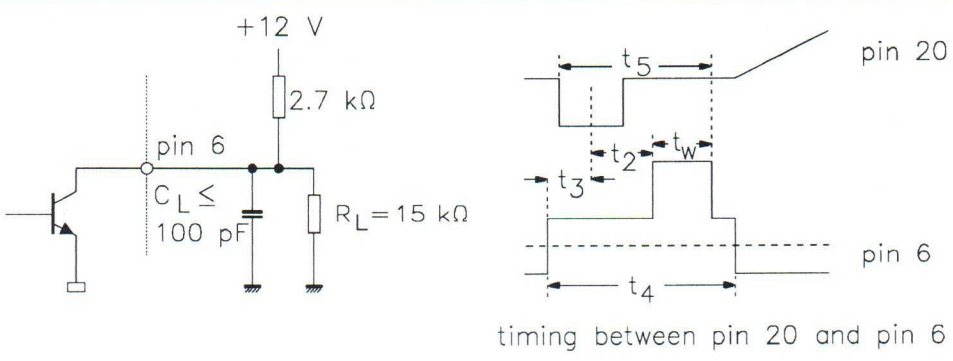


Fig.9 Sandcastle output.

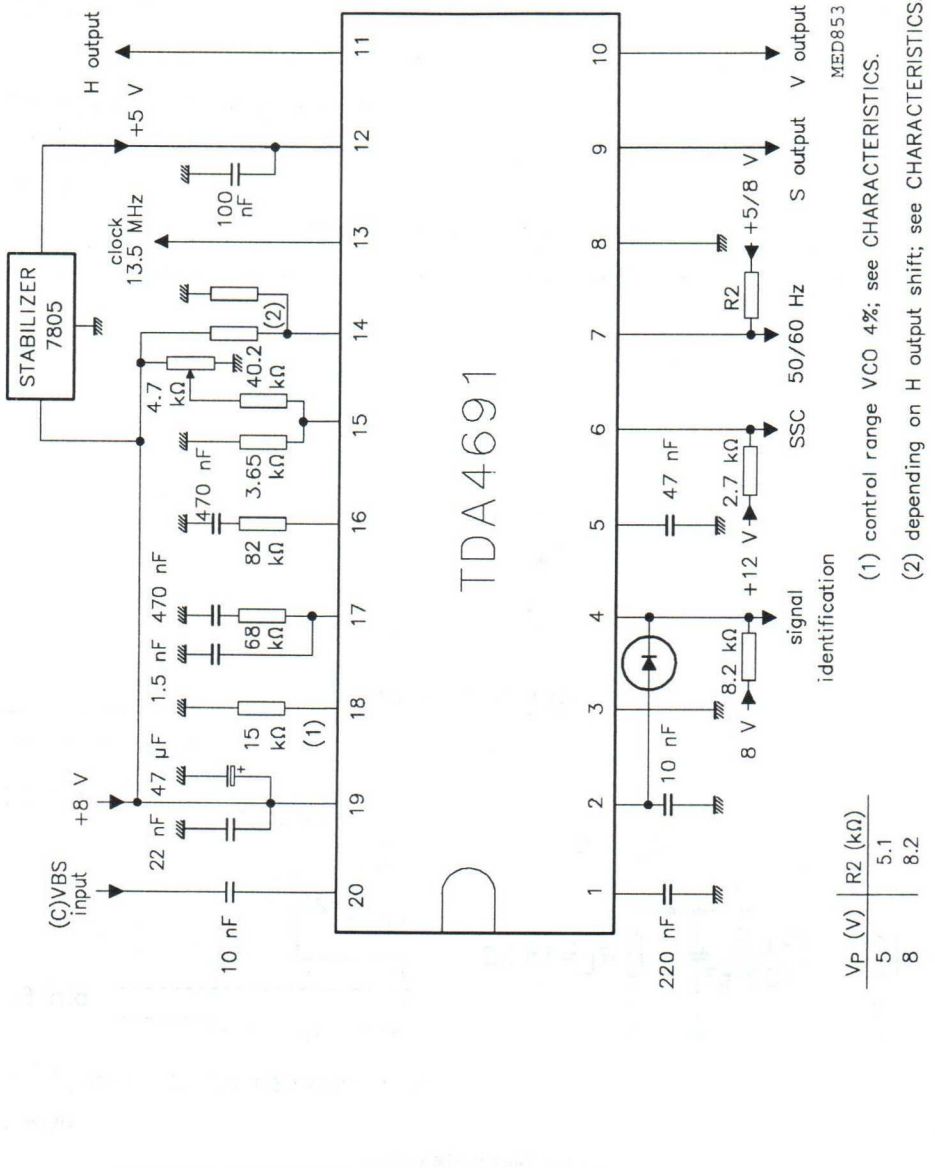


Fig.10 Application diagram.

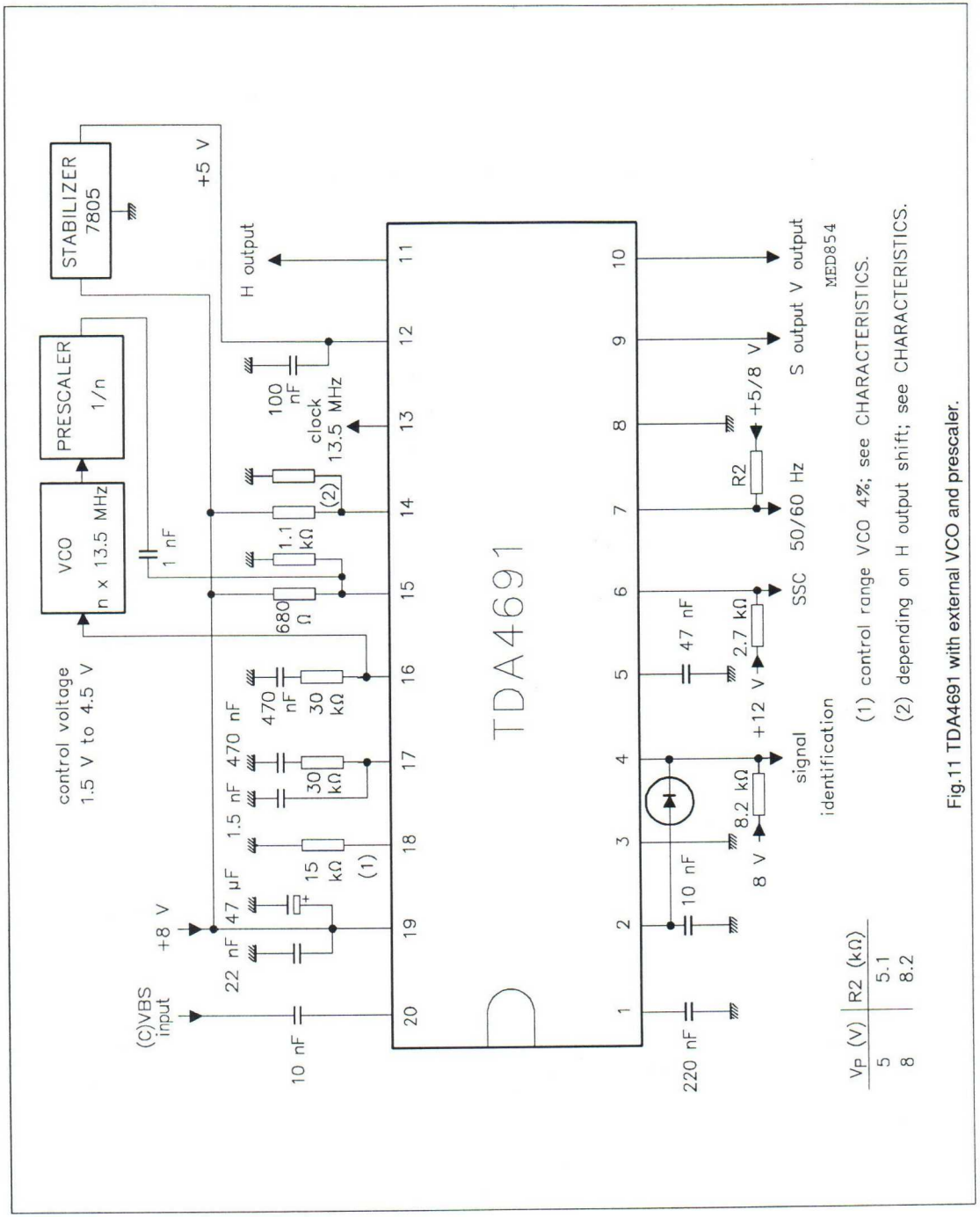


Fig.11 TDA4691 with external VCO and prescaler.

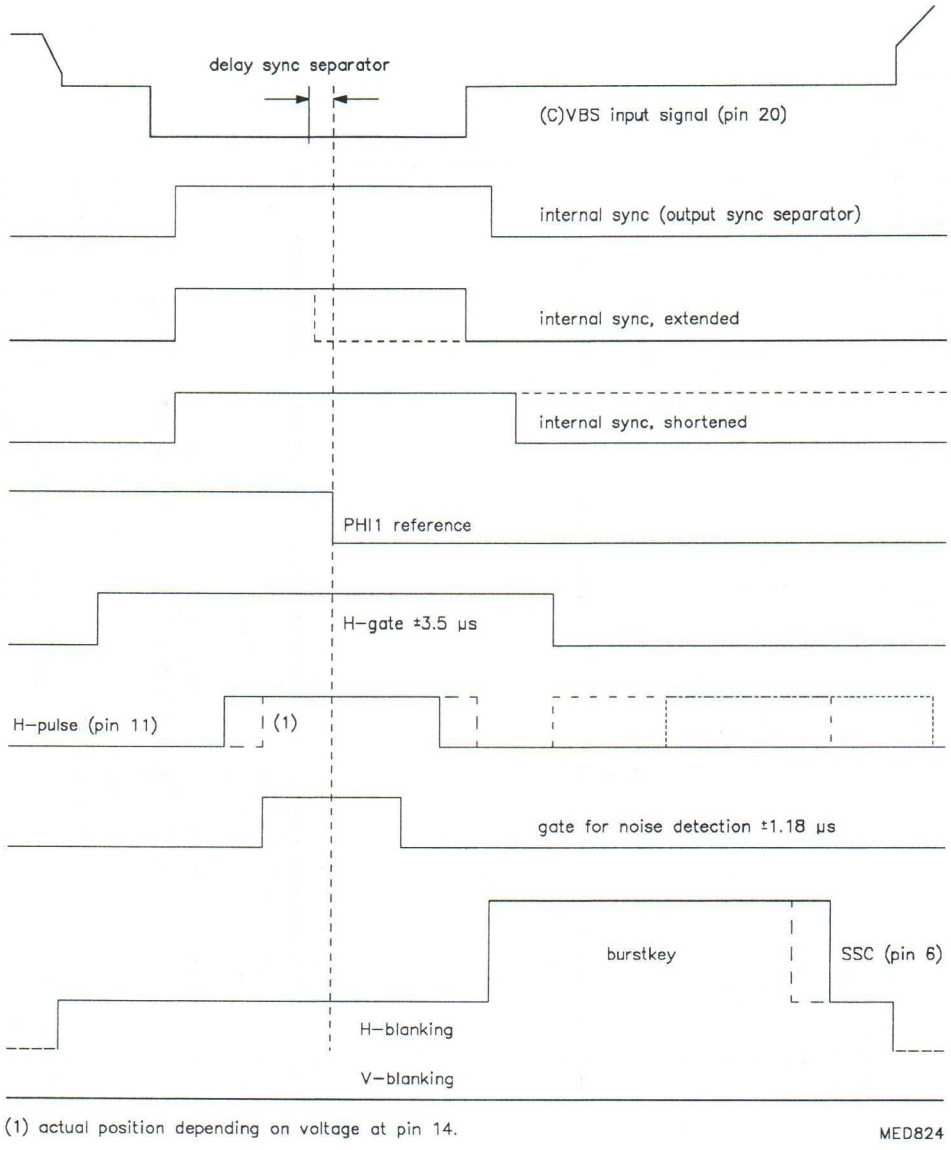


Fig.12 H-timing overview.

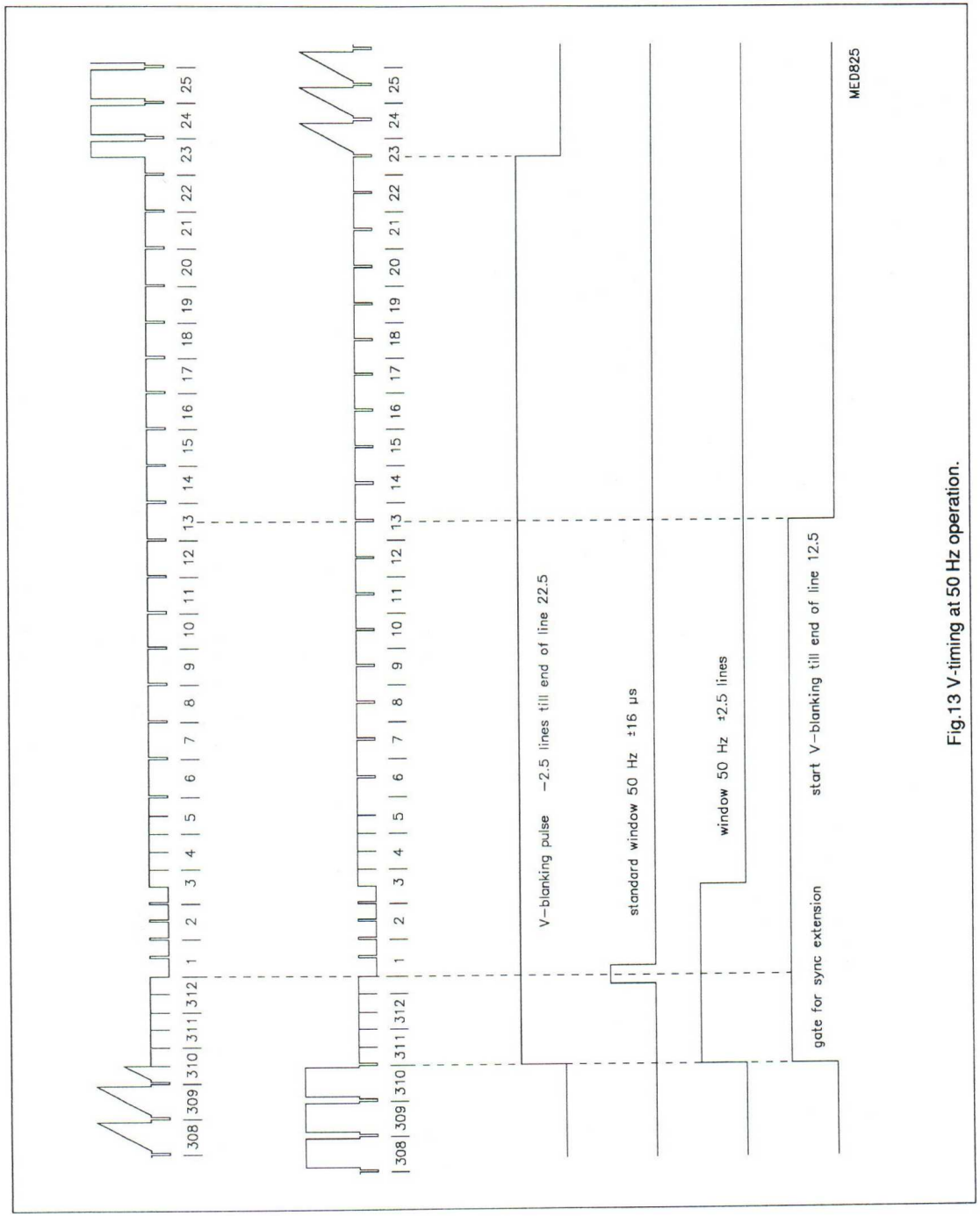


Fig.13 V-timing at 50 Hz operation.

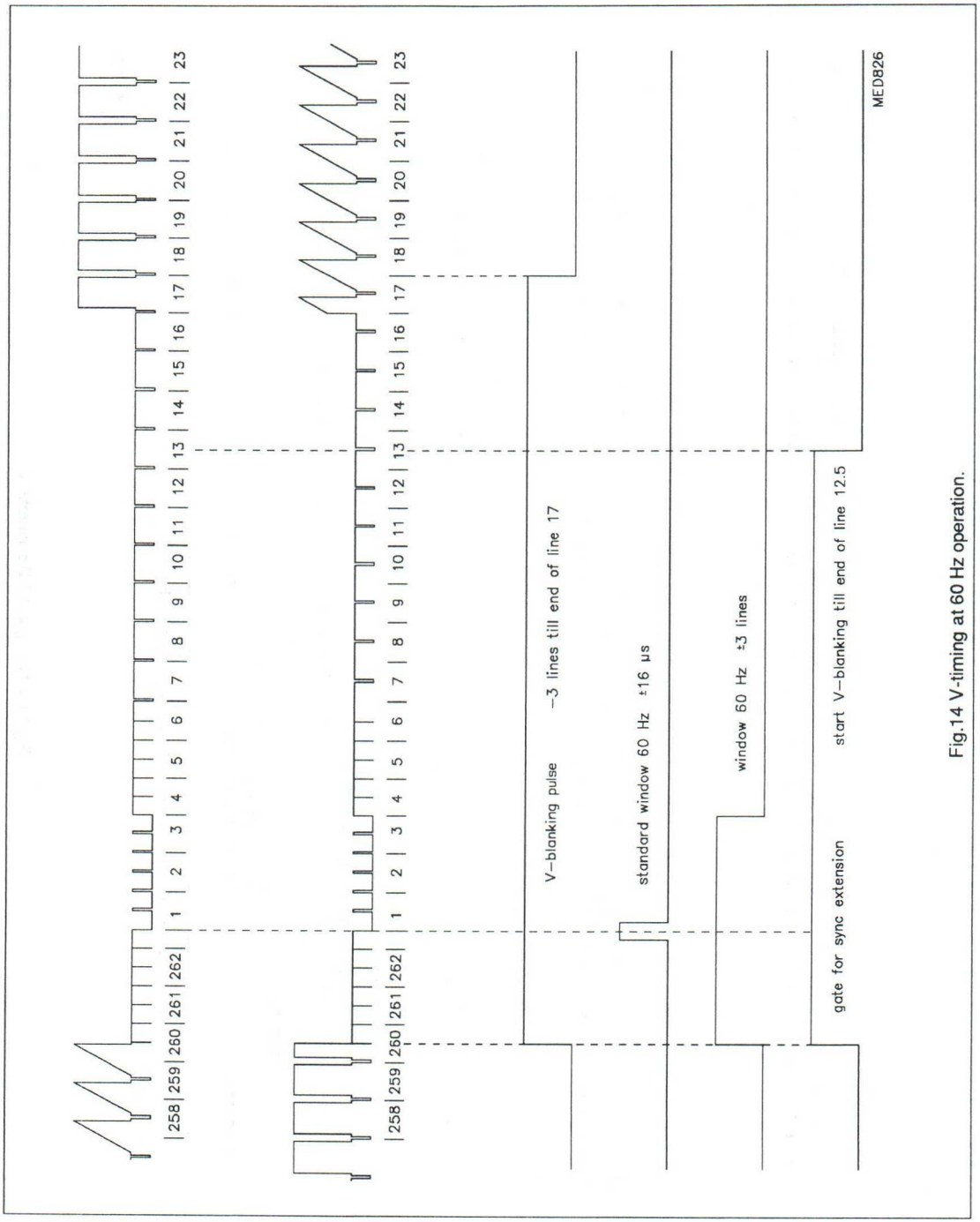


Fig.14 V-timing at 60 Hz operation.

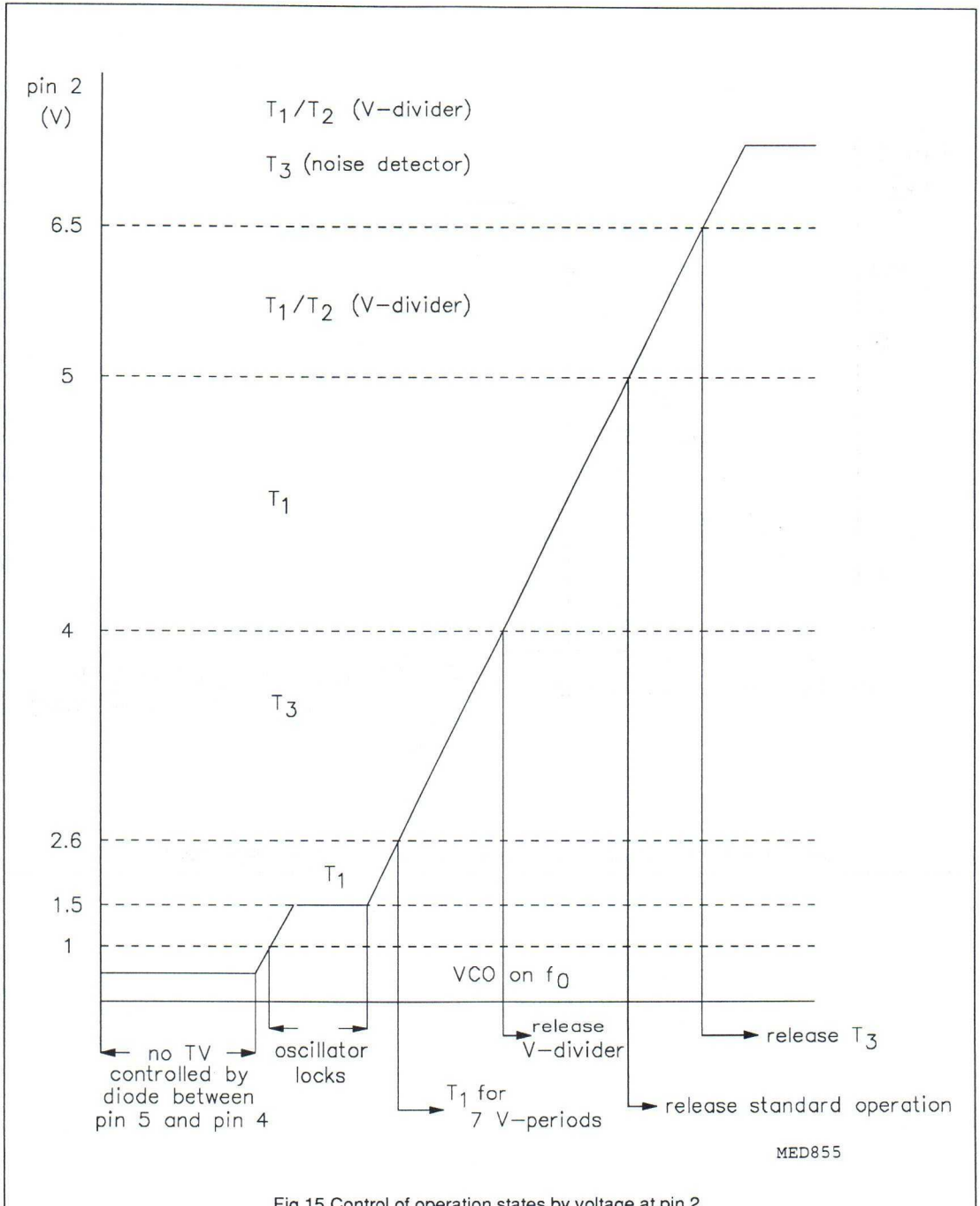


Fig.15 Control of operation states by voltage at pin 2.

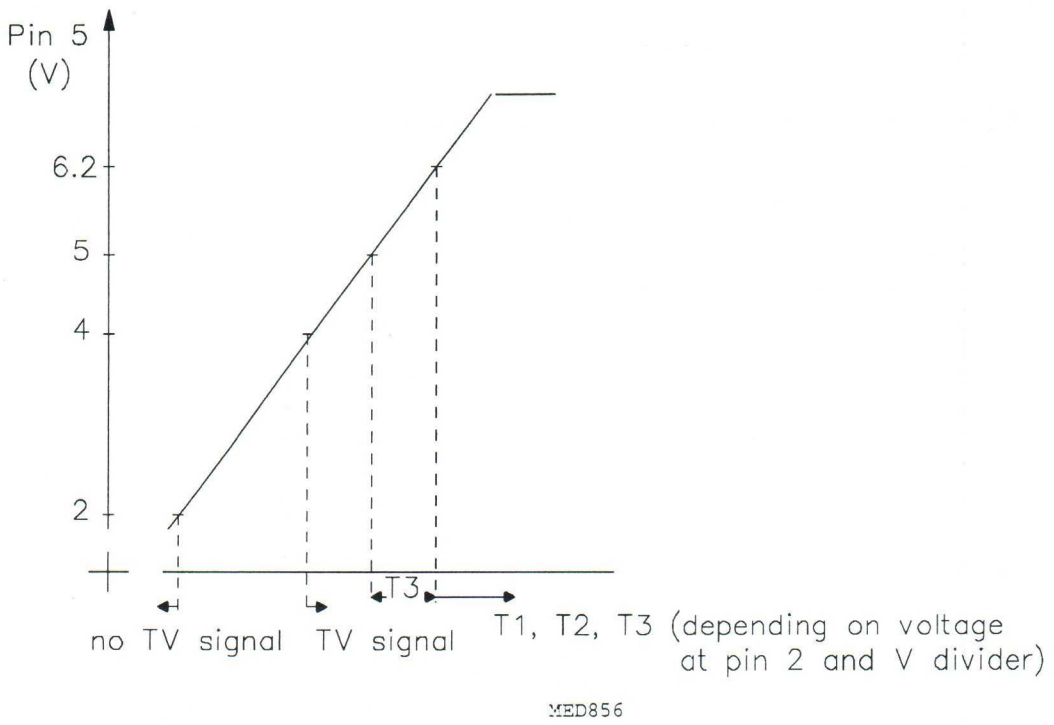


Fig.16 Control of signal identification (pin 4) and time constants by voltage at pin 5.

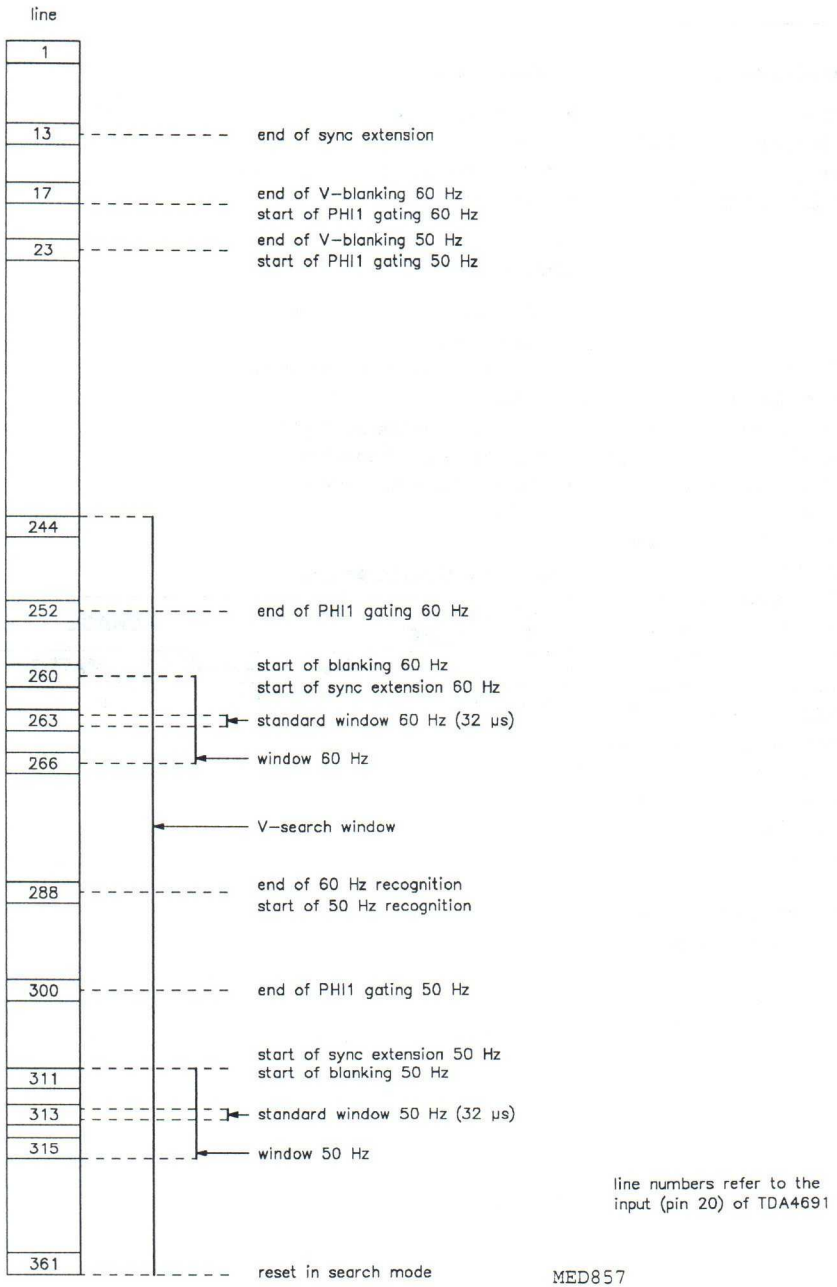


Fig.17 V-timing.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4710H

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

GENERAL DESCRIPTION

The TDA4710 is an integrated circuit for VHS PAL, SECAM ME or NTSC chrominance and synchronization processing in (S) VHS cassette recorders.

FEATURES

Chrominance

- 4.43/3.58 MHz chrominance output with colour-killer for record, electronic-to-electronic (e.g. direct to a SCART connector) and playback modes
- 627/629 kHz chrominance output with colour-killer
- 8.86/7.16 MHz crystal oscillator (voltage controlled oscillator in record mode and fixed frequency oscillator during playback mode)
- Separate automatic gain control (AGC) for record and playback (two channel hold capacity)
- Burst pre-emphasis/de-emphasis selection input (for NTSC)
- Subcarrier phase rotion and head-pulse input
- PAL error detector and correction circuit for longplay multispeed (LP MS)
- Test picture generator

Synchronization

- Phase-locked loop (PLL) with coincidence detector and mute output stage for the line frequency
- Sandcastle output signal

Additional features

- Standard/longplay multispeed mode selection
- 32 µs SKEW detector and output stage
- Selectable burst pulse insert for longplay feature mode (PAL)
- NTS to PAL-M transcoder at playback

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4710H	48	QFP48	plastic	SOT196A

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
V_{17-19}	digital part		-	5	-	V
V_{41-43}	analog part		-	5	-	V
$I_{17}+I_{41}$	supply current		-	45	-	mA
V_{20-19}	sync input signal slicing level		-	1.5	-	V
V_{23-19}	sandcastle output signal		-	4	-	V
V_{16-19}	test picture output signal		-	1	-	V
$V_{31(p-p)}$	4.43/3.58MHz subcarrier output (peak-to-peak value)		-	400	-	mV
Record (PAL) note 1						
$V_{48(p-p)}$	composite video input signal (peak-to-peak value)		-	450	-	mV
$V_{44(p-p)}$	AGC chrominance input signal (peak-to-peak value)		10	-	210	mV
$V_{37(p-p)}$	627 kHz subcarrier mixer output signal (peak-to-peak value)		-	1.06	-	V
Playback (PAL) note 1						
$V_{42(p-p)}$	627kHz chrominance input signal (peak-to-peak value)		-	24	-	mV
$V_{8(p-p)}$	4.43MHz chrominance output signal (peak-to-peak value)		-	420	-	mV
Playback (SECAM) note 2						
$V_{8(p-p)}$	chrominance output signal (peak-to-peak value)		-	200	-	mV

Notes to the quick reference data

1. PAL signal (red) with 75% saturation, –9 dB bandpath (pins 44 to 46), 6 dB trap pins 2 to 4 and chrominance-to-burst ratio of 2.2:1.
2. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the signal frequency.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

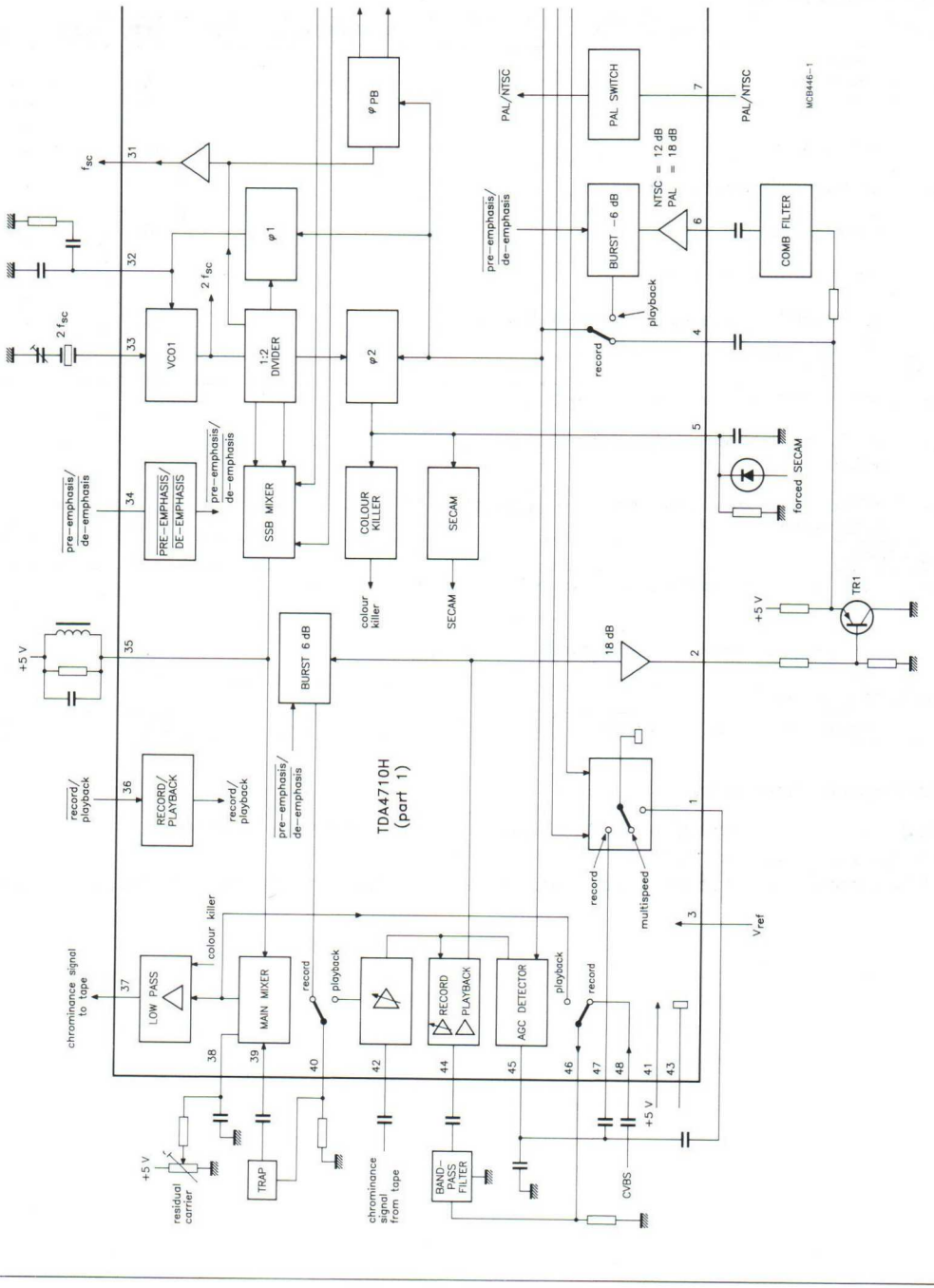


Fig.1(a) Block diagram (continued in Fig.1(b).

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

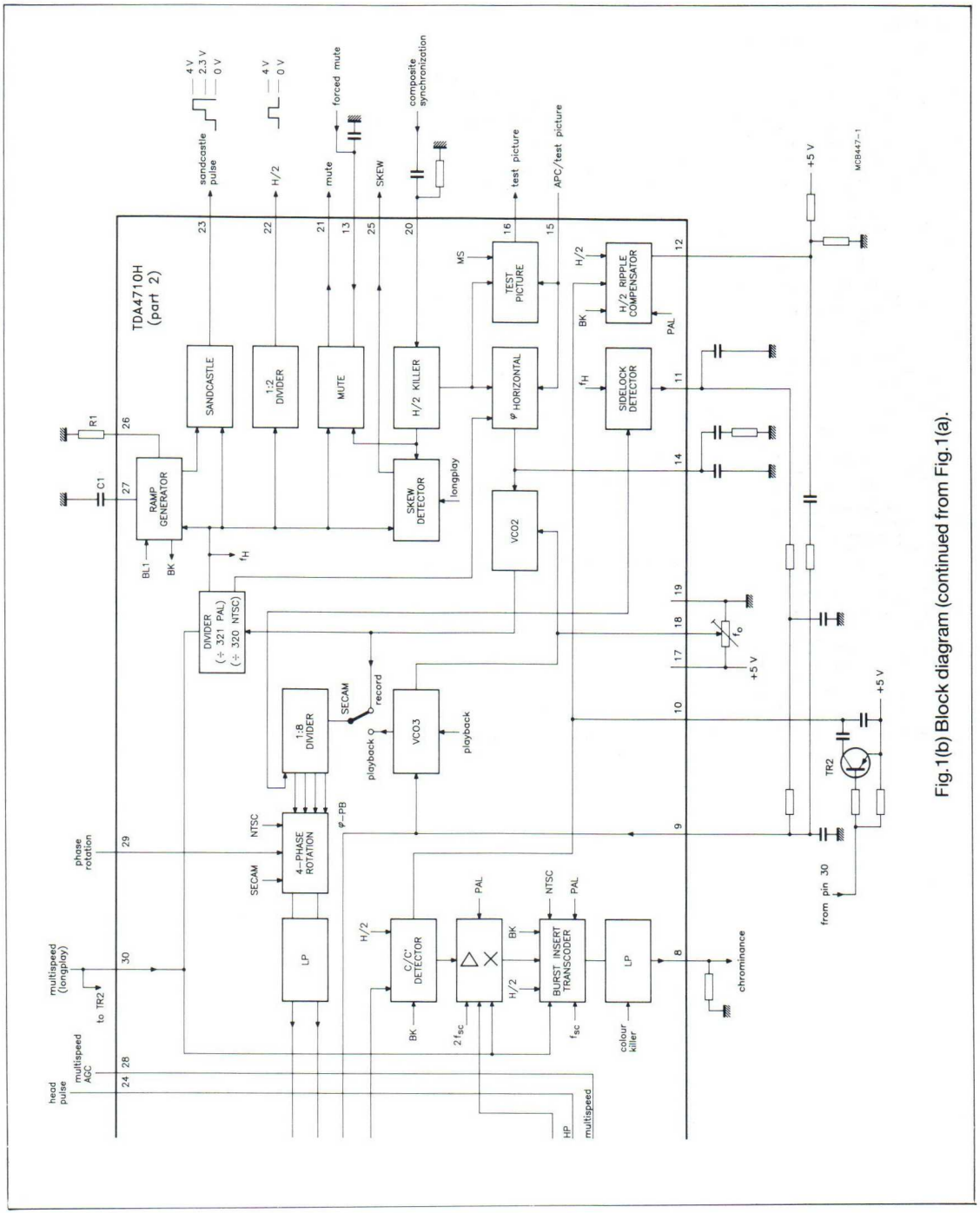


Fig.1(b) Block diagram (continued from Fig.1(a).

PINNING

PIN	DESCRIPTION
1	connection for an external capacitor, required for the AGC channel 2
2	chrominance/AGC output (record/playback)
3	reference voltage input
4	chrominance input (record)
5	colour-killer input/output, select colour ON, OFF or SECAM-BG mode
6	chrominance de-emphasis input (playback)
7	PAL/NTSC switch
8	chrominance output (to TV)
9	voltage controlled oscillator 3 (playback)
10	PAL sequence error detector output
11	sidelock detector output (playback)
12	H/2 ripple compensation output (playback)
13	connection for an external capacitor, required for the mute timing constant
14	voltage controlled oscillator 2
15	automatic phase correction (APC)/test picture input switch
16	test picture output
17	supply voltage, digital part
18	frequency adjustment for voltage controlled oscillator 2 and 3
19	ground, digital part
20	synchronization input
21	mute detector output
22	H/2 output
23	sandcastle pulse output
24	head-pulse input

PINNING (continued)

PIN	DESCRIPTION
25	SKEW detector output
26	sawtooth generator timing resistor
27	sawtooth generator timing capacitor
28	multispeed input switch (AGC)
29	phase rotation control input
30	multispeed input switch (longplay)
31	4.43/3.58 MHz subcarrier output
32	voltage controlled oscillator 1
33	crystal oscillator (8.86/7.16 MHz)
34	burst de-emphasis/pre-emphasis input switch
35	subcarrier resonance input (5.06 MHz, PAL; 4.21 MHz, NTSC)
36	record/playback input switch
37	627/629 kHz chrominance output signal to tape
38	main mixer balance capacitor
39	main mixer input
40	chrominance output signal
41	supply voltage, analog part
42	chrominance input signal from tape
43	ground, analog part
44	chrominance/AGC input (playback/record)
45	connection for an external capacitor, required for the AGC timing constant
46	chrominance selector output
47	connection for an external capacitor, required for the AGC channel 1
48	composite video blanking signal (CVBS) input

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	supply voltage				
V_{17-19}	digital part		-	6	V
V_{41-43}	analog part		-	6	V
	input voltage				
V_{13-19}			1	V_P	V
V_{18-19}			0	4	V
V_n	other voltages		0	V_P	V
	output currents				
$-I_{2,8,37,40,46}$			-	2	mA
$-I_{21,22,31}$			-	1	mA
$-I_{23}$			-	1	mA
$I_{1,25,47}$	other currents		-	3	mA
T_{amb}	operating ambient temperature range		0	70	°C
T_{stg}	storage temperature range		−25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$R_{th\ j-a}$	junction-to-ambient		-	92	K/W

Table 1 Abbreviations used in the characteristics tables

ABBREVIATION	DESCRIPTION
f_{sc}	chrominance sub-carrier frequency: PAL, 4.433619 MHz; NTSC, 3.579545 MHz
f_H	line frequency: PAL, 15.625 kHz; NTSC, 15.73426 kHz
LP	longplay mode: PAL, 1.17 cm/s; NTSC, 1.667 cm/s
N x f_H	PAL: 40.125 x f_H = 626.953 kHz NTSC: 40 x f_H = 629.370 kHz
MS	multispeed mode
V_T	temperature voltage (26 mV at 25 °C) generated at the emitter follower
I_C	collector current
C	PAL chrominance signal
C' (conjugate)	Complex PAL chrominance signal

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder — TDA4710H

CHARACTERISTICS

V_p = 5 V; V_{ref} = 1.4 V; burstkey duration = 4.0 µs; VCO 1 frequency = 4.433619/3.579545 MHz (PAL/NTSC) at pin 31 during playback mode; VCO 2 frequency = 15.625/1573426 kHz (PAL/NTSC) at pin 16 during test picture mode; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
	supply voltage range					
$V_P = V_{17-19}$	digital		4.5	5.0	5.5	V
$V_P = V_{41-43}$	analog		4.5	5.0	5.5	V
$V_{ref} = V_{3-43}$	reference input voltage		1.3	1.4	1.5	V
	input current without load					
I_{17}	digital		-	31	38	mA
I_{41}	analog		-	14	17	mA
PAL/NTSC SWITCH						
	input voltage					
V_{7-43}	PAL		3	-	V_P	V
V_{7-43}	NTSC		0	-	1.5	V
$\pm I_7$	input current		-	-	50	µA
RECORD/PLAYBACK SWITCH						
	input voltage					
V_{36-43}	record mode		0	-	3	V
V_{36-43}	playback mode		3.5	-	V_P	V
$\pm I_{7,36}$	input current		-	-	50	µA
COLOUR-KILLER (see note 1)						
	input voltage					
V_{5-43}	colour OFF		0	-	1	V
V_{5-43}	colour ON	no SECAM	2.5	-	3	V
V_{5-43}	SECAM ON (colour ON)		3.5	-	4.5	V
Record mode (see note 2)						
CONTROLLED CHROMINANCE AMPLIFIER SIGNAL						
$V_{48(P-p)}$	composite video signal input (peak-to-peak value)		-	450	-	mV
R_{48-43}	input resistance		14	20	26	kΩ
V_{48-43}	DC input voltage		-	2	-	V
$V_{40(p-p)}$	controlled output signal (peak-to-peak value)		-	335	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{40-43}	DC output voltage		-	3.1	-	V
BURST PRE-EMPHASIS						
	input voltage pre-/de-emphasis					
V_{34-43}	ON		0	-	0.8	V
V_{34-43}	OFF		1.5	-	V_P	V
$\pm I_{34}$	input current		-	-	50	µA
ΔV_{37-43}	burst pre-emphasis		5	6	7	dB

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE SELECTOR OUTPUT						
$V_{46(p-p)}$	output signal (peak-to-peak value)		-	450	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
CHROMINANCE INPUT SIGNAL						
$V_{44(p-p)}$	input signal (peak-to-peak value)		10	106	200	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V
AGC OUTPUT						
	chrominance output	note 4				
$V_{2(p-p)}$	PAL, NTSC		-	840	-	mV
$V_{2(p-p)}$	SECAM		-	290	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
PHASE SYNC						
	chrominance input signal (peak-to-peak value)					
$V_{4(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{4(p-p)}$	SECAM	note 4	-	145	-	mV
R_{4-43}	input resistance		14	20	26	kΩ
V_{4-43}	DC input voltage		-	2	-	V
627/629 kHz MIXER						
$V_{39(p-p)}$	input signal (peak-to-peak value)		-	335	-	mV
R_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC level		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{37(p-p)}$	PAL, NTSC		-	1.06	-	V
$V_{37(p-p)}$	SECAM	note 4	-	365	-	mV
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
	signal suppression					
α_{37}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{37}		f_{sc}	40	-	-	dB
α_{37}		$2 \times N \times f_H$	30	-	-	dB
α_{37}		$3 \times N \times f_H$	35	-	-	dB
α_{37}		colour OFF	40	-	-	dB
CHROMINANCE OUTPUT						
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM	note 2	-	150	-	mV
V_{8-43}	DC output voltage		-	1.8	-	V
α_{CK}	signal suppression	colour OFF	35	-	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sc} PLL AND VC01						
V_{32-43}	DC voltage		-	2.7	-	V
V_{33-43}	DC voltage		-	1.8	-	V
R_{33-43}	input resistance		300	-	-	Ω
R_{VCO1}	crystal resistance	series	-	70	-	Ω
C_{33-43}	input capacitance		-	10	-	pF
Δf	oscillator lock-in frequency range	note 5	-	500	-	Hz
$\pm\Delta\varphi$	static phase error between reference and burst signal	Δf = 400 Hz	-	5	-	deg
TC	oscillator temperature coefficient		-	-	3	Hz/K
Playback mode (see notes 2 and 6)						
CHROMINANCE AGC						
$V42_{(p-p)}$	input signal (peak-to-peak value)		4.8	24	48	mV
R_{42-43}	input resistance		7	10	13	kΩ
V_{42-43}	DC input voltage		-	2.4	-	V
$V_{40(p-p)}$	output signal (peak-to-peak value)		-	237	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	kΩ
V_{40-43}	DC output voltage		-	2.3	-	V
4.43/3.58 MHz MIXER						
V_{39-43}	input signal		-	237	-	mV
V_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC input voltage		-	1.6	-	V
$V_{46(p-p)}$	output signal (peak-to-peak value)	note 7	-	150	-	mV
R_{46-43}	output resistance	note 3	-	V_T/I_C	-	Ω
	signal suppression	note 8				
α_{46}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - (2 \times N \times f_H)$	30	-	-	dB
CHROMINANCE AMPLIFIER						
$V_{44(p-p)}$	input signal (peak-to-peak value)		-	53	-	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE DE-EMPHASIS						
	input signal (peak-to-peak value)					
$V_{6(p-p)}$	PAL		-	53	-	mV
$V_{6(p-p)}$	NTSC		-	106	-	mV
R_{6-43}	input resistance		3.5	5.0	6.5	kΩ
V_{6-43}	DC input voltage		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM		-	150	-	mV
ΔV_{8-43}	burst de-emphasis	$V_{34-43} \leq 0.8$ V	–4.5	–5.5	–6.5	dB
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{8-43}	DC output voltage		-	1.8	-	V
AGC CAPACITOR SWITCH $V_{28-43} \leq 1.5$ V; see note 9						
$I_{1,47-43}$	saturation voltage	$I_{1,47} = 1$ mA	-	-	500	mV
	headpulse input voltage	conductive				
V_{24-43}		pin 47	-	-	1.5	V
V_{24-43}		pin 1	3	-	-	V
V_{24-23}	input threshold voltage for blanking and burstkey suppression	note 10	1.5	2.5	3.0	V
$\pm I_{24}$	input current		-	-	50	μA
MULTI-SPEED AGC INPUT						
V_{28-43}	input voltage	normal mode; note 9	0	-	1.5	V
	input voltage for picture search					
V_{28-43}	normal sync		2	-	3	V
V_{28-43}	super sync		3.5	-	V_P	V
$\pm I_{28}$	input current		-	-	50	μA
PLAYBACK PHASE CONTROL - VCO3						
V_{9-43}	PLL DC voltage	locked	-	2.5	-	V
R_9	source resistance during burstkey suppression		-	40	-	kΩ
G	loop gain		-	800[3]	-	s
Δf	oscillator deviation with respect to f_{sc}		-	76	-	kHz/V
Δf	pull-in range with respect to f_{sc}		38	-	-	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL SEQUENCE ERROR DETECTION						
	output voltage	see note 11				
V_{10-43}	HIGH		3.2	-	-	V
V_{10-43}	LOW		-	-	1.0	V
I_{10}	output current during burstkey		-	100	-	µA
$-\Delta I_{10}$	demodulated burst	polarity equal to H/2 signal	-	100	-	µA
$-\Delta I_{10}$	demodulated burst	polarity unequal to H/2 signal	-	100	-	µA
SIDELOCK DETECTOR						
$\pm I_{11}$	output current	sidelock detection	-	300	-	µA
t_p	pulse duration		-	64	-	µs
H/2 RIPPLE COMPENSATION						
$\pm I_{12}$	output current during burstkey		-	150	-	µA
V_{12-43}	DC range for linear operation		1.8	-	3.2	V
VC02 AND VCO3 f_O FREQUENCY CONTROL						
V_{18-43}	DC voltage		-	2	-	V
	nominal frequency					
f_{PAL}	PAL		-	5.016	-	MHz
f_{NTSC}	NTSC		-	4.208	-	MHz
$-I_{18}$	input current		-	100	-	µA
APC/TEST PICTURE (see note 12)						
	input voltage					
V_{15-43}	APC ON		0	-	1.4	V
V_{15-43}	APC OFF	test picture with white signal	2.7	-	3.4	V
V_{15-43}	APC OFF	test picture with white signal	4.3	-	V_P	V
$\pm I_{15}$	input current		-	-	50	µA
N x f_H PLL (VC02)						
V_{14-43}	PLL DC voltage	locked	-	1	-	V
R_{14-43}	source resistance during sync pulse		-	40	-	kΩ
G	loop gain		-	380	-	10^3/s
Δf	oscillator deviation related to f_H		-	900	-	Hz/V
Δf	pull-in range related to f_H		800	-	-	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part						
TEST PICTURE OUTPUT (see note 13)						
	output voltage					
V_{16-19}	white level		-	2.1	-	V
V_{16-19}	black level		-	1.4	-	V
V_{16-19}	sync level		-	1.1	-	V
V_{16-19}	super sync level		-	-	0.25	V
R_{16-19}	source resistance		-	10	-	kΩ
SYNC INPUT SIGNAL						
V_{20-19}	sync input voltage		2.2	4.0	V_P	V
H/2 OUTPUT						
	output voltage					
V_{22-19}	HIGH	$-I_{22}$ = 0.5 mA	2.5	-	-	V
V_{22-19}	LOW	$-I_{22}$ = 0.5 mA	-	-	0.8	V
SANDCASTLE OUTPUT (see note 10)						
	output voltage					
V_{23-19}	LOW	I_{23} = 1 mA	-	-	0.5	V
V_{23-19}	MEDIUM	$-I_{23}$ = 0.5 mA	2.0	2.3	2.7	V
V_{23-19}	HIGH	$-I_{23}$ = 1 mA	3.75	4.0	-	V
BURSTKEY STAGE (see note 14)						
R_{26-19}	resistor R1		-	47	-	kΩ
t_p	burstkey pulse duration		-	4	-	µs
HEAD-PULSE INPUT FOR 4 PHASE ROTATION (see note 15)						
	input voltage					
V_{29-19}	channel 1		0	-	1.5	V
V_{29-19}	channel 2		3	-	V_P	V
$\pm I_{29}$	input current		-	-	50	µA
LP MS INPUT (see note 16)						
	input voltage					
V_{30-19}	normal mode		0	-	1.5	V
V_{30-19}	LPS MG		2	-	3	V
V_{30-19}	LPS MS	auto-burst				
V_{30-19}	NTSC, PAL-M	insertion	3.5	-	V_P	V
		transcoding	3.5	-	V_P	V
SEARCH CONTROL (SKEW) (see note 17)						
	output voltage					
V_{25-19}	LOW	I_{25} = 0.5 mA	-	-	0.8	V
V_{25-19}	HIGH	$-I_{25}$ = 20 µA	4	-	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part (continued)						
MUTE FUNCTION						
	detector output voltage					
V_{21-19}	LOW	N x f_H; PLL locked, I_{21} = 0.5 mA	-	-	0.8	V
V_{21-19}	HIGH	N x f_H; PLL unlocked, I_{21} = 0.5 mA	2.5	-	-	V
	mute voltage					
V_{13-19}	LOW		3.5	-	-	V
V_{13-19}	HIGH	active	-	-	1.5	V
V_{13-19}	forced mute		1	-	1.5	V
f_{sc} SUB-CARRIER OUTPUT						
V_{31-19}	output signal		-	400	-	mV
R_{31-19}	output resistance		-	V_T/I_C	-	Ω
V_{31-19}	DC output voltage		-	1.2	-	V

Notes to the characteristics

1. SECAM-ON switching voltage is provided by the TDA4720(T).
2. PAL signal (red) with 75% saturation, 9 dB bandpath (pins 44 to 46), 6 dB trap (pin 2 to 4) and chrominance-to-burst ratio of 2.2:1.
3. NPN open emitter output.
4. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the frequency signal.
5. VCO1 operates as a fixed frequency oscillator during SECAM-mode.
6. Comb filter attenuations: PAL = 18 dB and NTSC = 12 dB.
7. Selective measurement of the f_{sc} component.
8. Measured at $V_{42-43(p-p)}$ = 12 mV.
   The signal suppression can be balanced at pin 38 (see Fig.1(a)).
9. During playback mode, the open collector output is conductive at the upper threshold and non-conductive at the lower threshold of the head pulse. The open collector output of pin 47 is conductive at the lower threshold and non-conductive at the upper threshold of the head pulse. During LP MS mode, pins 1 and 47 are simultaneously conductive independent of the head pulse.

Notes to the Characteristics (continued)

10. When the threshold of pin 24 is passed the upper part of the sandcastle pulse (pin 23) is suppressed 11 times and the chrominance output signals (pins 8 and 37) are colour killed for 13 lines.

11. Only active in PAL mode:
    - Output is HIGH, if the polarity of the demodulated burst is equal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' mixer is active.
    - Output voltage is LOW, if the polarity of the demodulated burst is unequal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' amplifier is active.

12. If APC = OFF, the mute output (pin 21) is switched to forced HIGH (used for automatic test picture insertion).

13. Test picture output signals depend on the control voltages at pins 15 and 28 as shown in Table 2. V_{ref} at pin 3 is loaded by the output current I_{16}.

Table 2 Control of test picture output signals

CONDITION	PIN 15 (V)	PIN 28 (V)	SEE FIG.2
APC OFF, test picture without white signal	2.7 to 3.4	<3	2(b)
APC OFF, test picture with white signal	>4.3	<3	2(a)
APC ON	<1.4	<3	2(b)
APC ON, super sync ON	<1.4	>3.5	2(c)

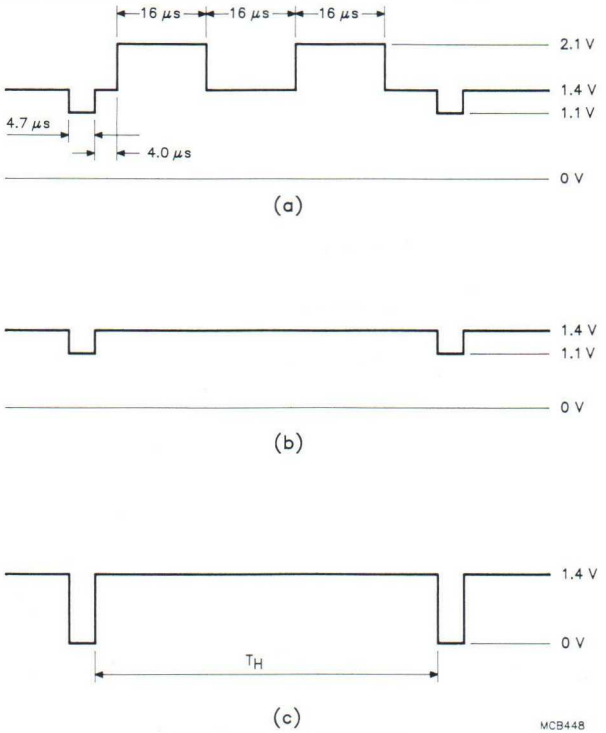


Fig.2 Test picture output.

Notes to the characteristics

14. Values refer to Fig.3 (R1 is the resistor from pin 26 to ground, C1 is the capacitor from pin 27 to ground):

- t_1 = 0.305 ms; R1C1
- t_2 = < 0.210 ms; R1C1
- t_3 = 0.1 ms; R1C1
- $t_4 1$ = 0.367 ms;

15. Phase rotation:

MODE	CHANNEL 1($V_{29\text{-}19}$ = LOW)	CHANNEL 2 (V29-19 = HIGH)
PAL	0°	–90°
NTSC	+90°	–90°
SECAM	0°	0°

16. Switching to LP MS mode activates the $2f_H$ mode of the VCO2 PLL, automatic SKEW detection and automatic PAL sequence error correction.

17 If the video head changes from one track to another during LP MS mode, the 32 µs time shifted sync pulse occurs. This shift is recognized by the SKEW detector.

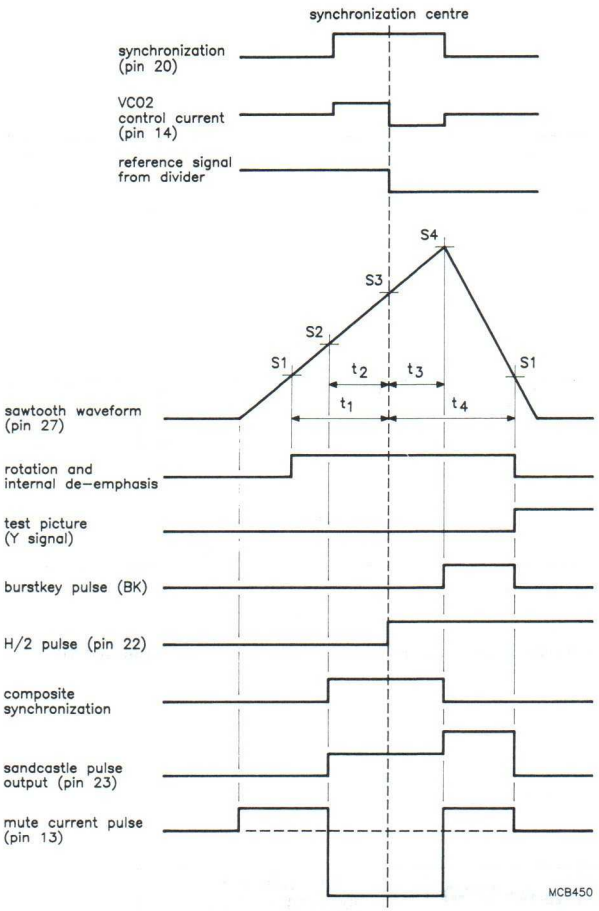


Fig.3 Timing diagram.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

APPLICATION INFORMATION

(Figs 4 to 39 show equivalent internal circuit configurations. All circuits are ESD protected).

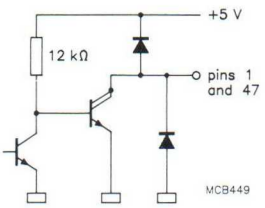


Fig.4 AGC switch output.

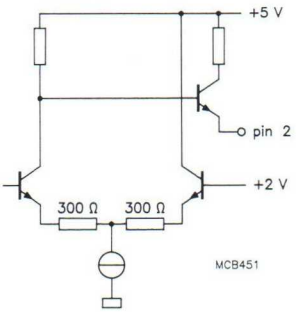


Fig.5 Chrominance output.

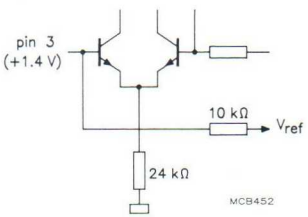


Fig.6 Voltage reference input.

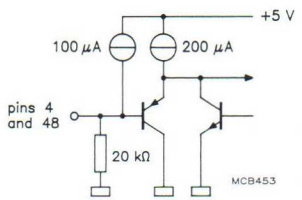
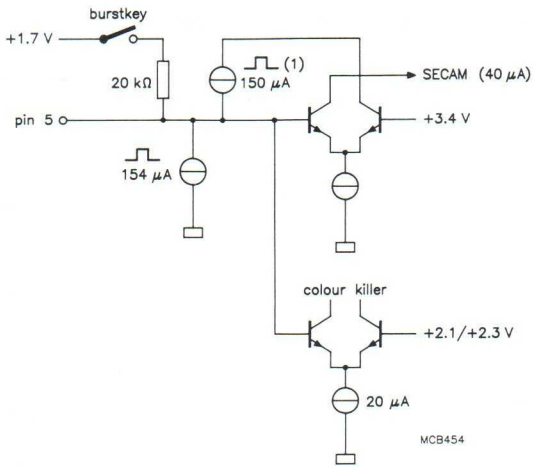


Fig.7 Chrominance/CVBS input.



(1) with an applied burst of 166 μA.

Fig.8 Colour-killer and SECAM switch input.

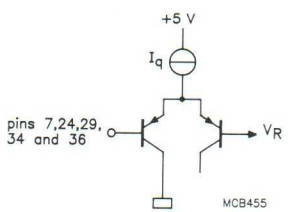


Fig.9 PAL/NTSC switch input (see Table 4).

Table 4 Switch characteristics

PIN	SIGNAL	QUIESCENT CURRENT (μA)	V(R) VOLTAGE (V)
7	PAL/NTSC switch input	20	2.5
24	HP input	30	2.5
29	phase rotation switch input	30	2.5
34	de/pre-emphasis switch input	30	1.1
36	record/playback switch input	20	3.3

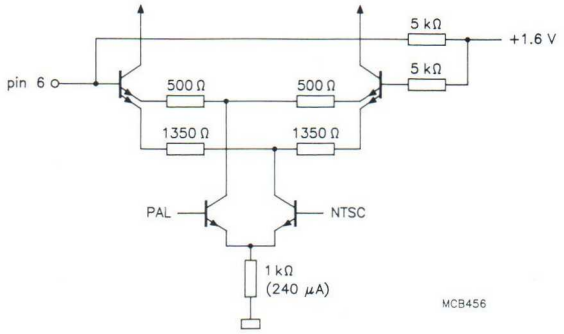


Fig.10 De-emphasis input.

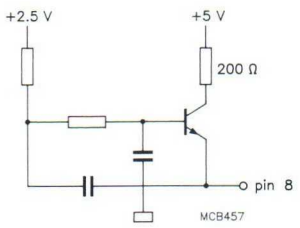


Fig.11 Chrominance output (pin 8).

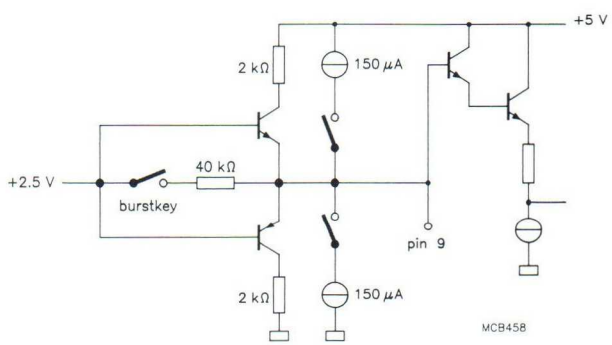


Fig.12 VCO3 control input.

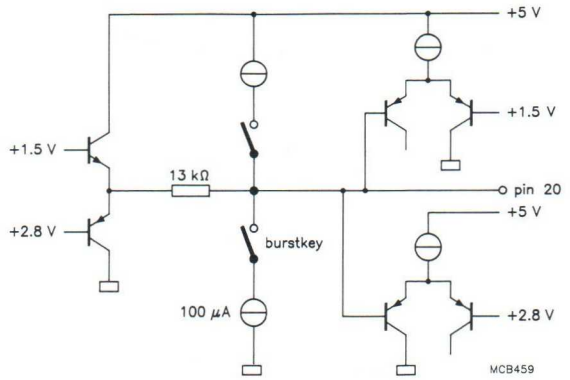


Fig.13 Sequence error detector.

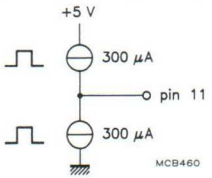


Fig.14 Sidelock detector output.

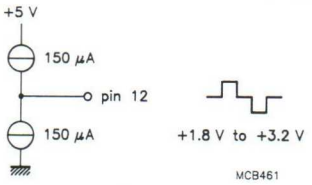


Fig.15 H/2 ripple coupling output.

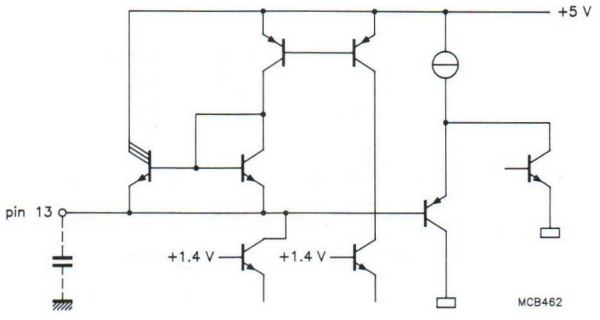


Fig.16 Mute timing input.

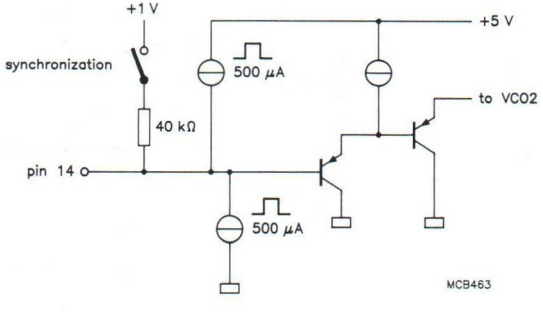


Fig.17 VCO2 control input.

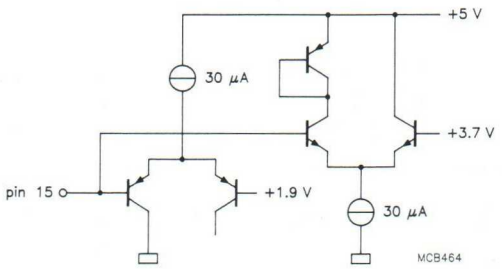


Fig.18 APC/test picture switch input.

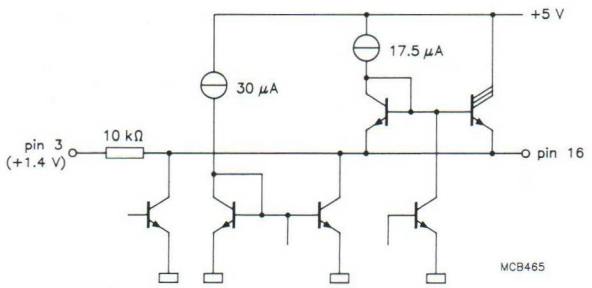


Fig.19 Test picture output.

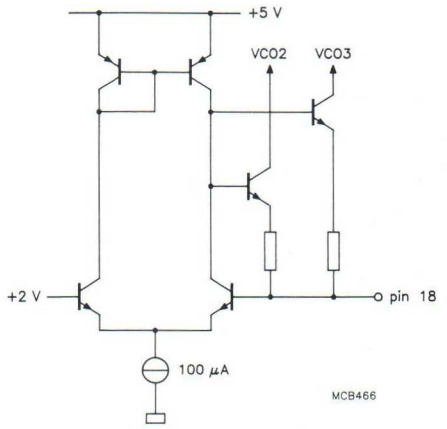


Fig.20 VCO2/VCO3 adjustment input.

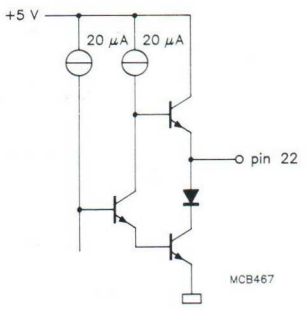


Fig.21 H/2 output.

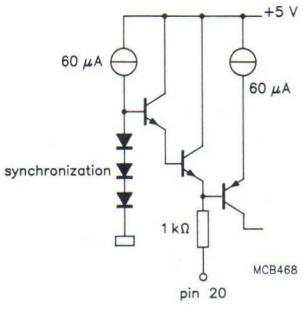


Fig.22 Synchronization input.

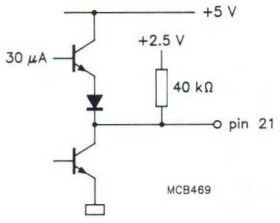


Fig.23 Mute detector output.

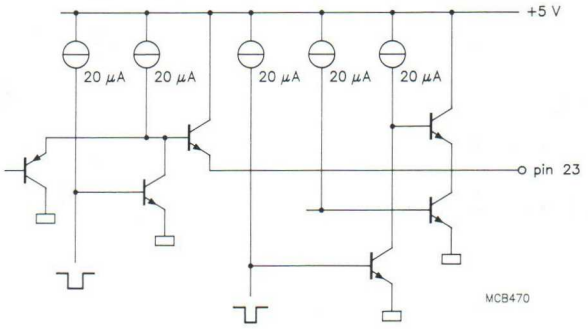


Fig.24 Sandcastle pulse output.

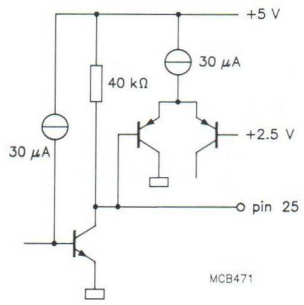


Fig.25 Skew detector output.

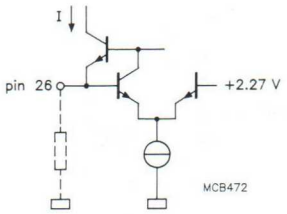


Fig.26 Reference current input for the sawtooth generator.

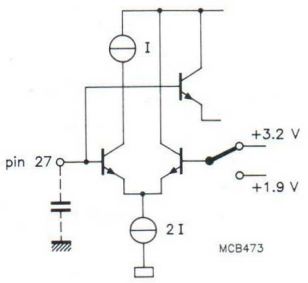


Fig.27 Sawtooth generator.

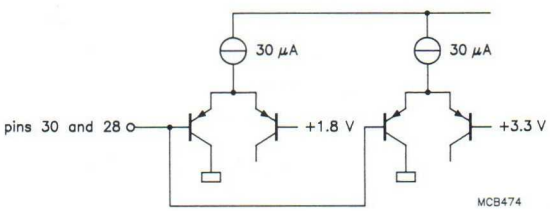


Fig.28 Multispeed AGC/LP input.

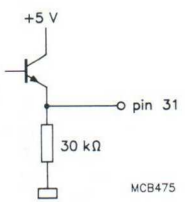


Fig.29 Subcarrier signal output.

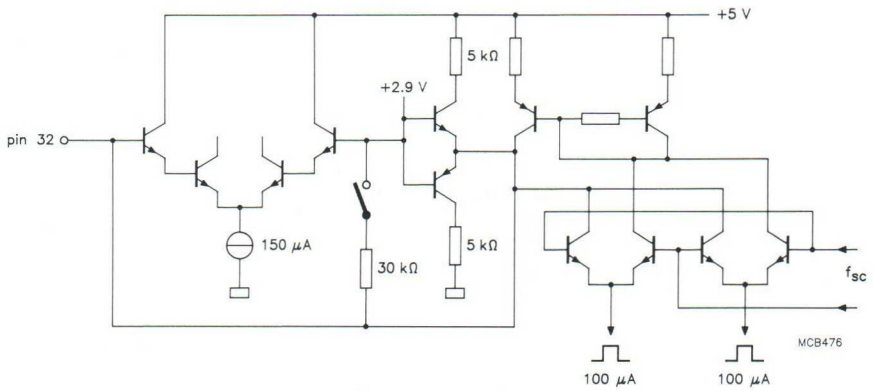


Fig.30 VCO1 control input.

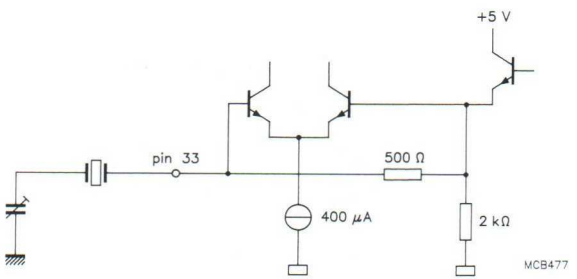


Fig.31 Oscillator input.

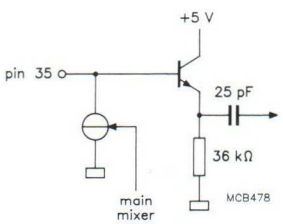


Fig.32 Subcarrier resonance output.

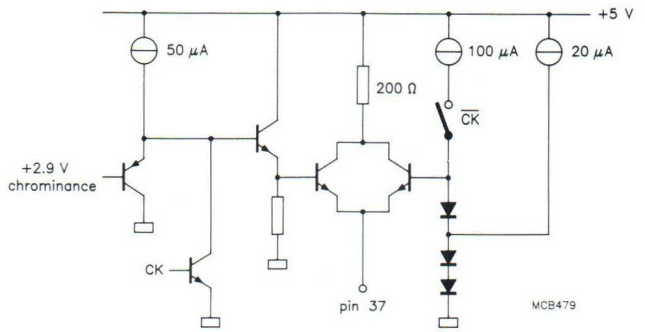


Fig.33 Chrominance signal output.

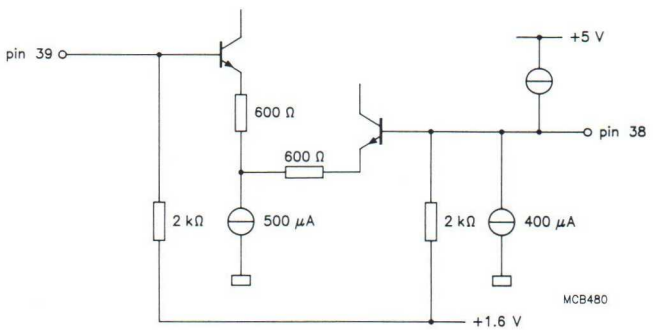


Fig.34 Main mixer input/balance circuit.

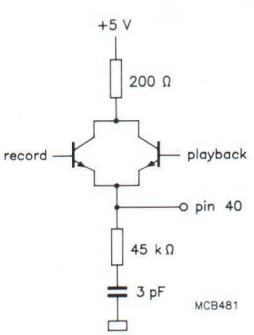


Fig.35 Chrominance output.

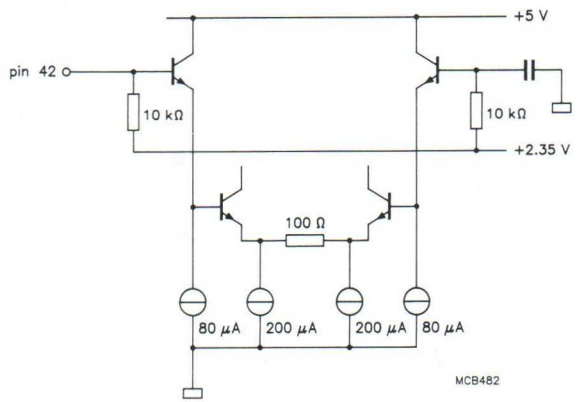


Fig.36 Chrominance input.

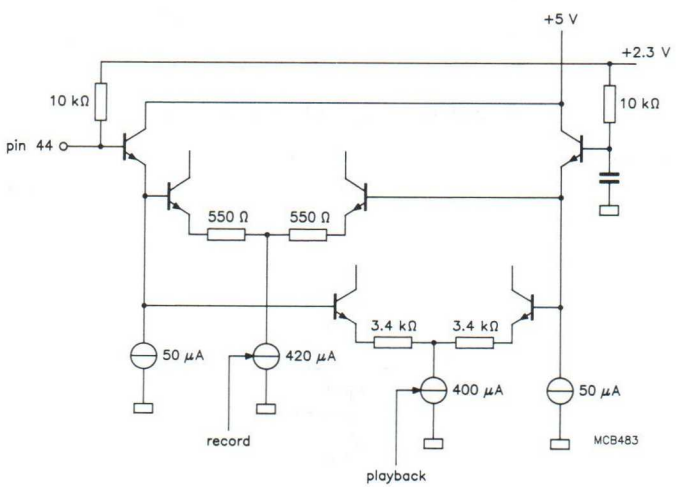


Fig.37 Chrominance AGC input.

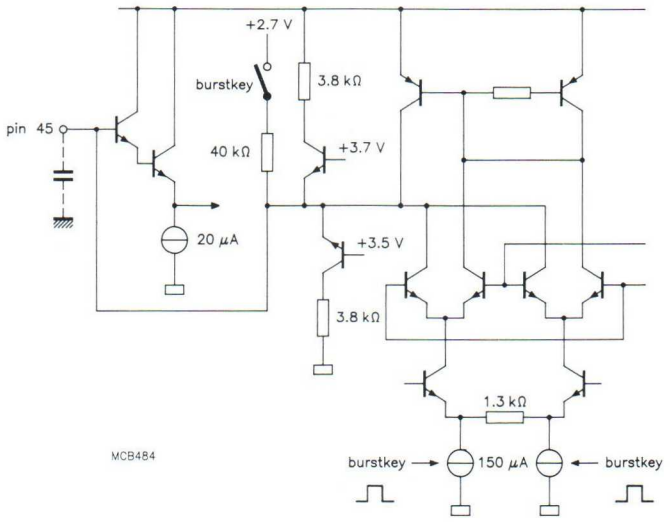


Fig.38 AGC control input.

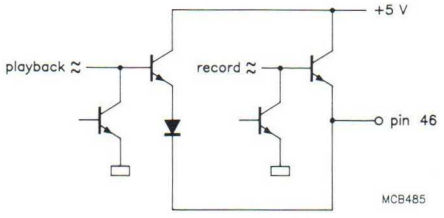


Fig.39 Chrominance output.

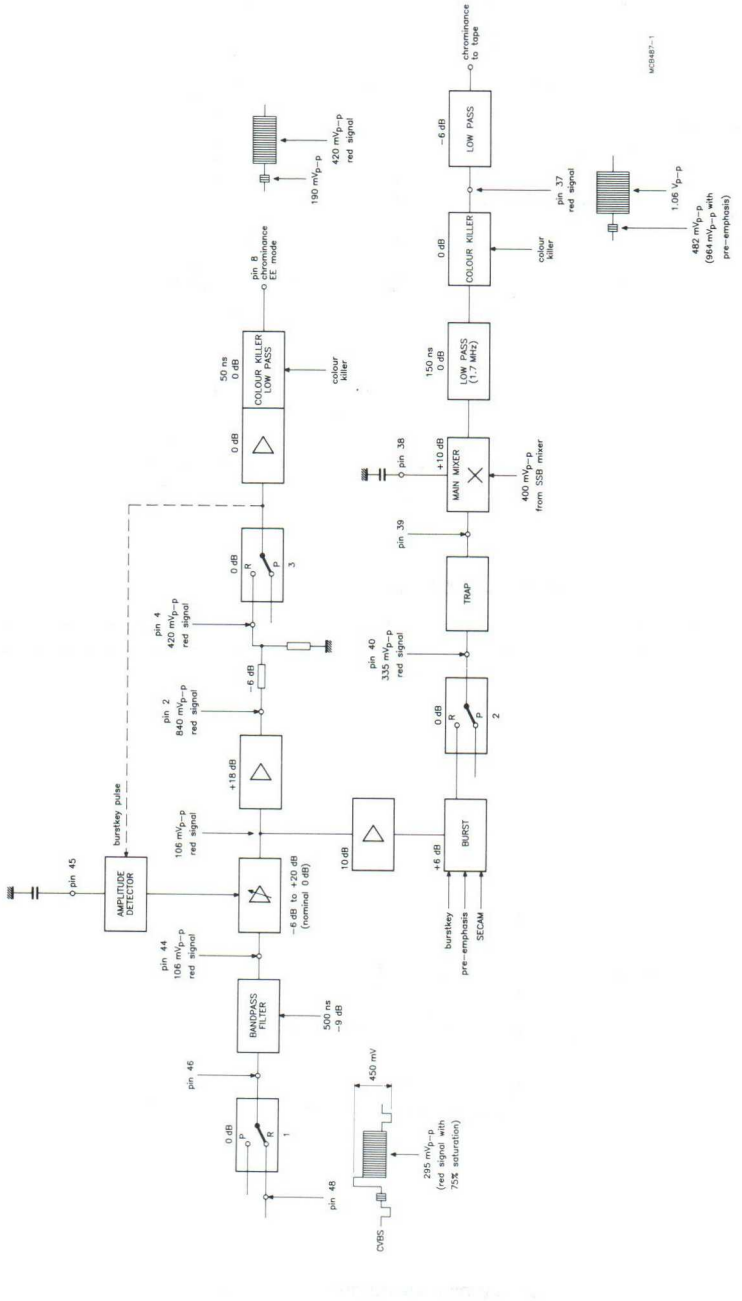


Fig.40 Signal path; record mode.

Where:

P = playback
R = record

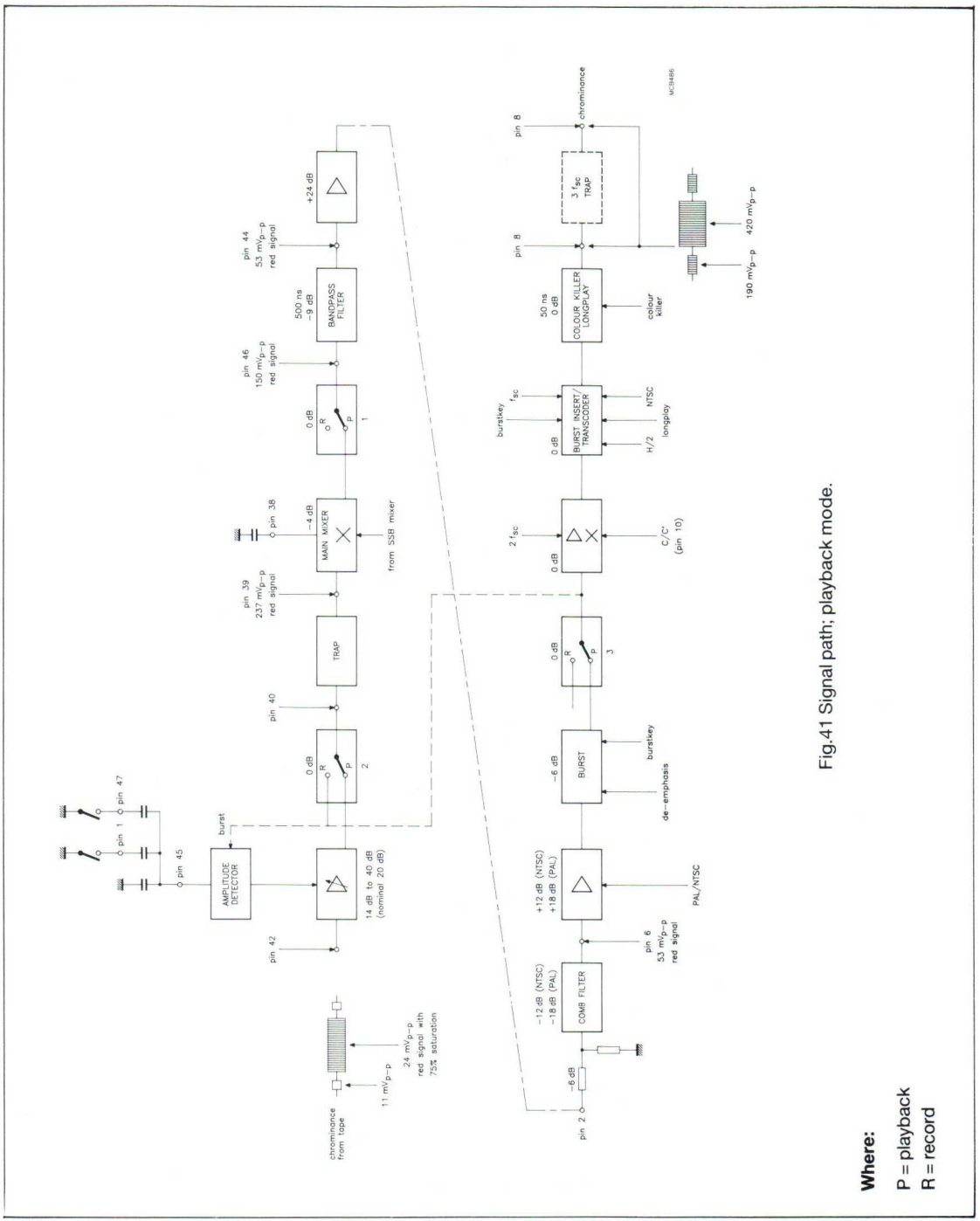


Fig.41 Signal path; playback mode.

Where:

P = playback
R = record

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

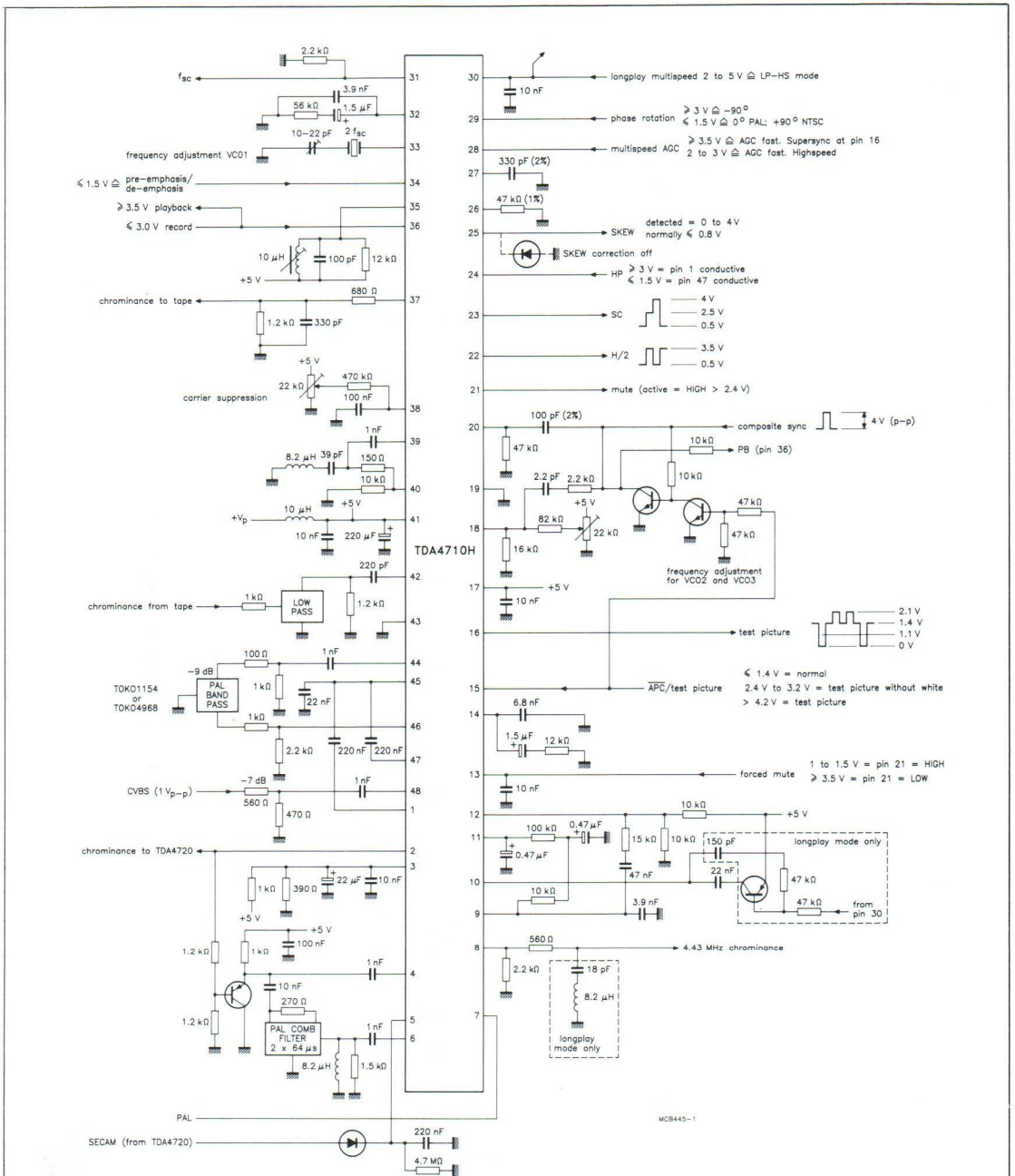


Fig.42 Application diagram (PAL).

Note to Fig.42

If not otherwise stated, the tolerance for external components is:
resistors ±5%
capacitors ±20%
inductors ±10%

SECAM IDENTIFICATION AND CHROMINANCE CORRECTION CIRCUIT

The TDA4720T is a monolithic integrated circuit for SECAM identification and chrominance signal correction in VHS video cassette recorders (VCR). It can be applied as a stand-alone SECAM identification circuit and, when used in conjunction with TDA4710, together they provide all the functions necessary for PAL/SECAM B, G chrominance processing in VHS VCRs.

Features

- Very reliable SECAM identification by means of chrominance burst amplitude, presence of both SECAM colour carriers and line alternation of both carriers
- Two identification outputs: SECAM YES/NO
- Internal phase correction of the demodulated burst
- Internal detection and switching for SECAM long-play VCR (for 'trick' modes)
- Internal buffers and switches for correction of the line-alternating colour carriers

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	4,5	5,0	5,5	V
Supply current	I_P	–	16	17	mA
Chrominance input signal to phase detector (peak-to-peak value)	$V_{14,15-4(p-p)}$	60	–	300	mV
Chrominance input signal to line correction circuit (peak-to-peak value)	$V_{5,12-4(p-p)}$	–	–	1	V
Chrominance output signal from line correction circuit (peak-to-peak value)	$V_{7-4(p-p)}$	–	–	1	V

PACKAGE OUTLINES

TDA4720: 16-lead DIL; plastic (SOT38).
TDA4720T: 16-lead mini-pack; plastic (SO16; SOT109A).

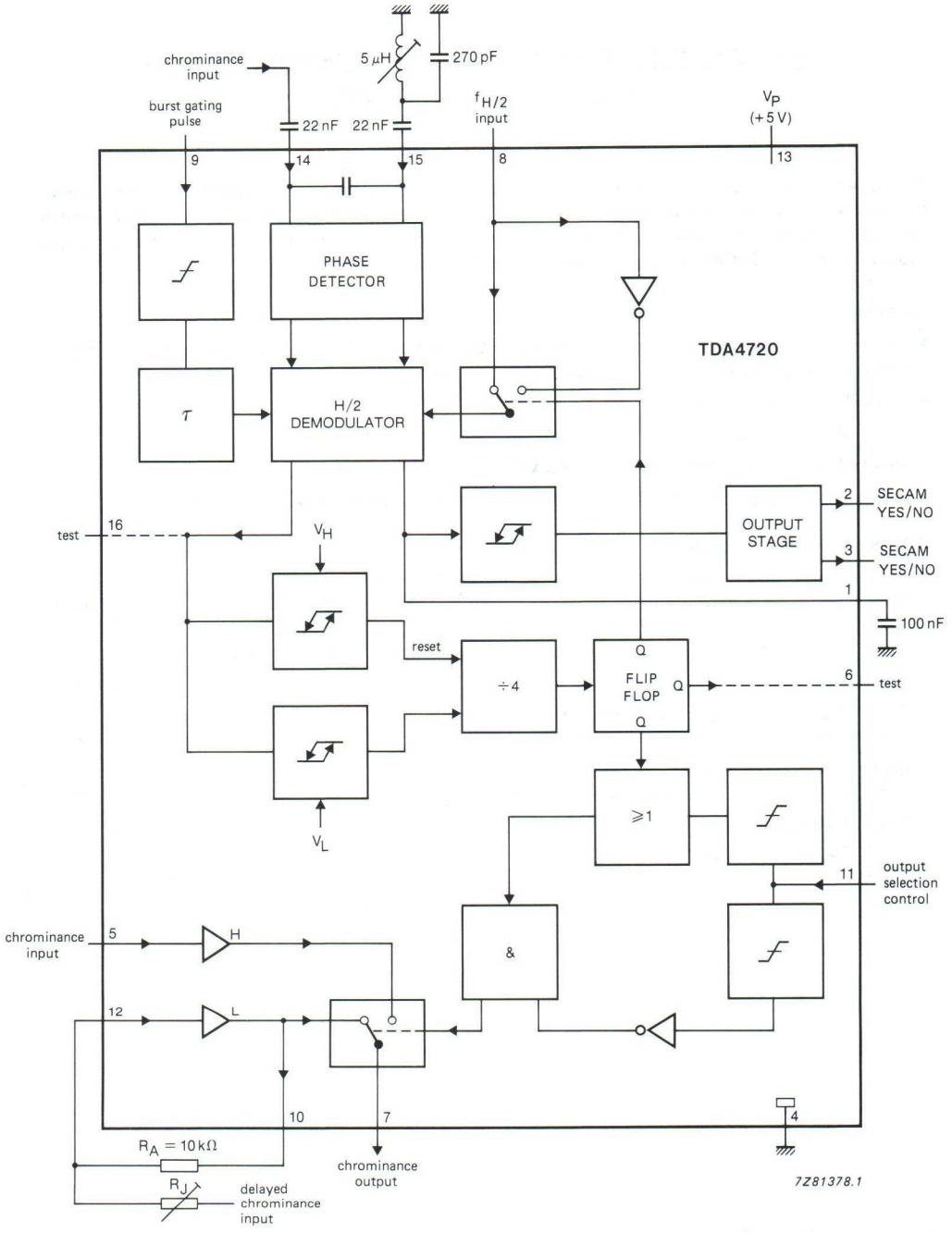


Fig. 1 Block diagram and test circuit.

PINNING

pin. no.	function
1	Integration of demodulated bursts.
2	Buffered output; SECAM YES/NO.
3	Buffered output; SECAM YES/NO.
4	Ground.
5	Chrominance input (only if line correction of SECAM carrier is used).
6	Test pin (internal connection).
7	Chrominance output (of line-corrected SECAM; only if line correction of SECAM carrier is used).
8	$f_{H/2}$ frequency input for chrominance burst demodulation.
9	Burst gating pulse input.
10	Feedback resistor for pin 12 signal path (only if line correction of SECAM carrier is used).
11	Output selection control (selects signal path to pin 7).
12	Delayed chrominance input (delayed by 1H; only if line correction of SECAM carrier is used).
13	Positive supply voltage (V_P = + 5 V).
14,15	The LC circuit at pin 15 has to be tuned to the centre frequency between the two chrominance carriers (at pin 14). The phase detector then provides a positive or negative output voltage depending on the first or second chrominance carrier.
16	Test pin (internal connection).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_P = V_{13-4}$	–	6,0	V
Voltage range on pins 6, 8, 9, 11, 12, 14 and 15	V_{n-4}	0	V_P	V
Maximum current at pins 1, 2, 3, 7, 15, 16 and 18	I_n	–	2	mA
Total power dissipation	P_{tot}	–	120	mW
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-4} = 5$ V; $T_{amb} = 25$ °C; test circuit as per Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_P	4,5	5,0	5,5	V
Supply current		I_{13}	–	16	17	mA
Identification						
AC input voltage (peak-to-peak value)		$V_{14,15-4}$	60	125	300	mV
Input resistance		$R_{14,15-4}$	14	18	22	kΩ
Charge capacitor		C_{1-4}	–	100	–	nF
Forced SECAM-ON voltage		V_{1-4}	3,8	–	–	V
Forced SECAM-OFF voltage		V_{1-4}	–	–	2	V
Sensitivity of phase detector	$V_{14,15-4(p-p)}$ = 125 mV	α	–	1,6	–	V/rad.
Output voltage						
in SECAM mode		$V_{2,3-4}$	4,3	–	–	V
in non-SECAM mode		$V_{2,3-4}$	–	–	0,8	V
Output current						
in SECAM mode		$I_{2,3}$	1	–	–	mA
in non-SECAM mode		$I_{2,3}$	–	–	0,3	μA
Burst gating						
Input resistance		R_{9-4}	20	25	–	kΩ
Threshold voltage HIGH (phase detector active)		V_{9-4}	3,0	3,25	3,5	V
H/2 demodulator						
Input resistance		R_{8-4}	20	25	–	kΩ
Threshold voltage for changing conditions of H/2 demodulator		V_{8-4}	3,0	3,25	3,5	V
Chrominance correction						
Chrominance input signal (peak-to-peak value)		$V_{5-4(p-p)}$	–	–	1	V
Input resistance		R_{5-4}	10	13	16	kΩ
Input capacitance		C_{5-4}	–	–	10	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Delayed chrominance input signal (peak-to-peak value)		$V_{12\text{-}4(p\text{-}p)}$	–	–	1	V
Input resistance		$R_{12\text{-}4}$	–	50	–	kΩ
Input capacitance		$C_{12\text{-}4}$	–	–	10	pF
Voltage gain		$\frac{V_{7\text{-}4}}{V_{12\text{-}4}}$	–	$\frac{R_A}{R_J}$	–	
Gain adjustment range		ΔG	19	–	–	dB
Gain bandwidth product		f_G	30	–	–	MHz
Output signal (peak-to-peak value)		$V_{7\text{-}4(p\text{-}p)}$	–	–	1	V
Output resistance		$R_{7\text{-}4}$	$\frac{V_T}{I_C}$	–	–	Ω
DC output voltage		$V_{7\text{-}4}$	–	–	2,5	V
Difference in DC output levels at pin 7 with pin 5/pin 12 switching		$\Delta V_{7\text{-}4}$	–	–	20	mV
Output selection control						
Input resistance		$R_{11\text{-}4}$	20	25	30	kΩ
Input voltage to select pin 5 signal for output		$V_{11\text{-}4}$	0	–	1,5	V
Input voltage to select pin 12 signal for output		$V_{11\text{-}4}$	2,75	–	5,0	V
Input voltage for automatic output switching*		$V_{11\text{-}4}$	2,0	–	2,6	V

* This voltage is generated internally if pin 11 is not connected.

SECAM-L chrominance processor for VHS video recorders

TDA4722/TDA4724

FEATURES

- Forced recording or playback mode input
- One circuit for Bell and anti-Bell filter (1.07 MHz)
- Fully ESD protected
- Low power consumption (170 mW)
- 5 V supply.

GENERAL DESCRIPTION

The TDA4722/24 is a bipolar integrated circuit for chrominance processing of SECAM-L signals in SECAM-L or multistandard VHS video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{18\text{-}24,26}$	supply voltage		4.5	5.0	5.5	V
I_{18}	supply current		–	34	–	mA
$V_{25\text{-}24(p\text{-}p)}$	chrominance input (peak-to-peak value)	record mode	–	–	645	mV
$V_{21\text{-}24(p\text{-}p)}$		playback mode	–	300	600	mV
$V_{15\text{-}24(p\text{-}p)}$	chrominance output (peak-to-peak value)	record mode	560	630	700	mV
$V_{1\text{-}24(p\text{-}p)}$		playback mode	–	–	1000	mV
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		–25	–	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4722	32	ShrDIL	plastic	SOT232AH
TDA4724	28	DIL	plastic	SOT117

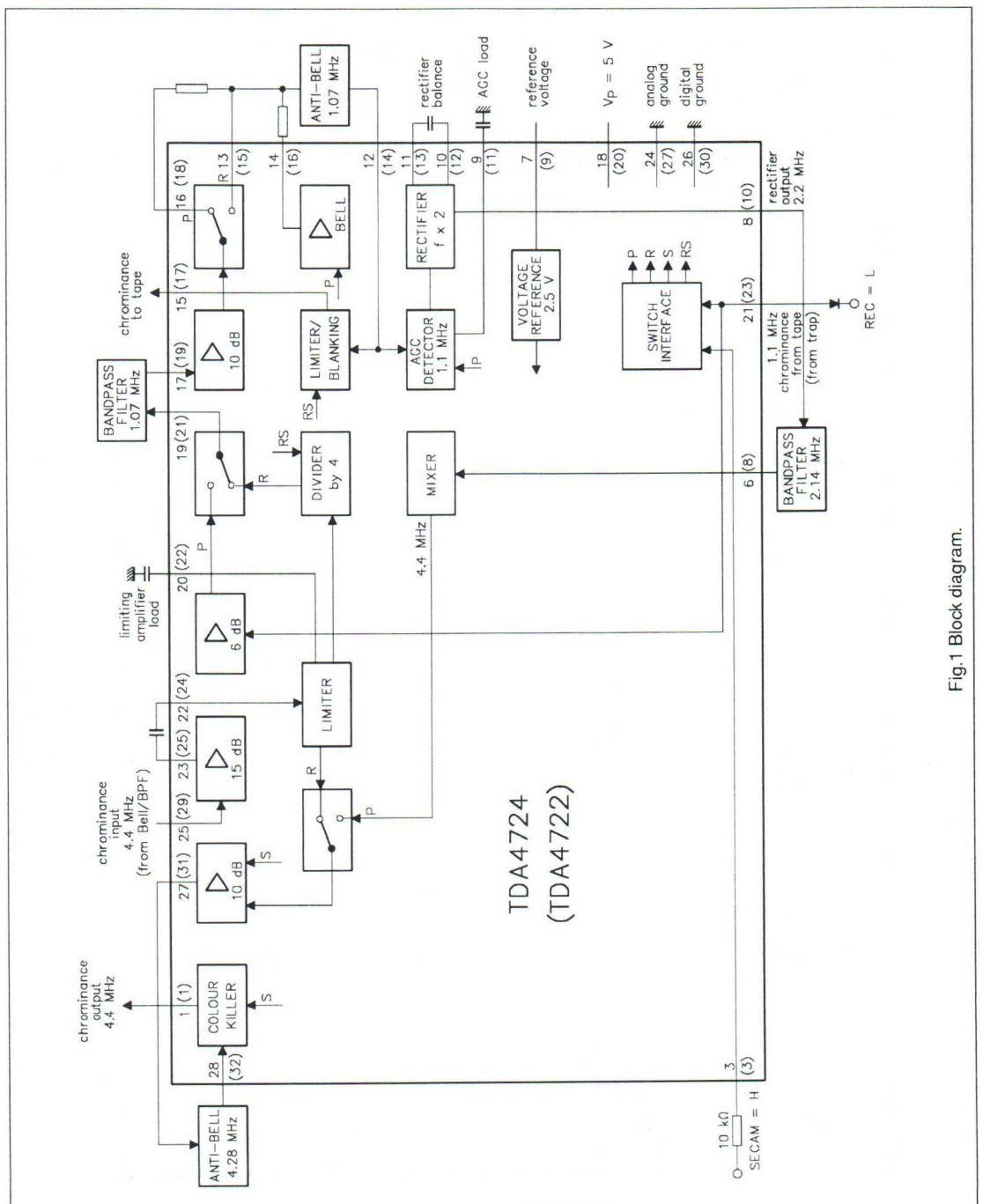


Fig.1 Block diagram.

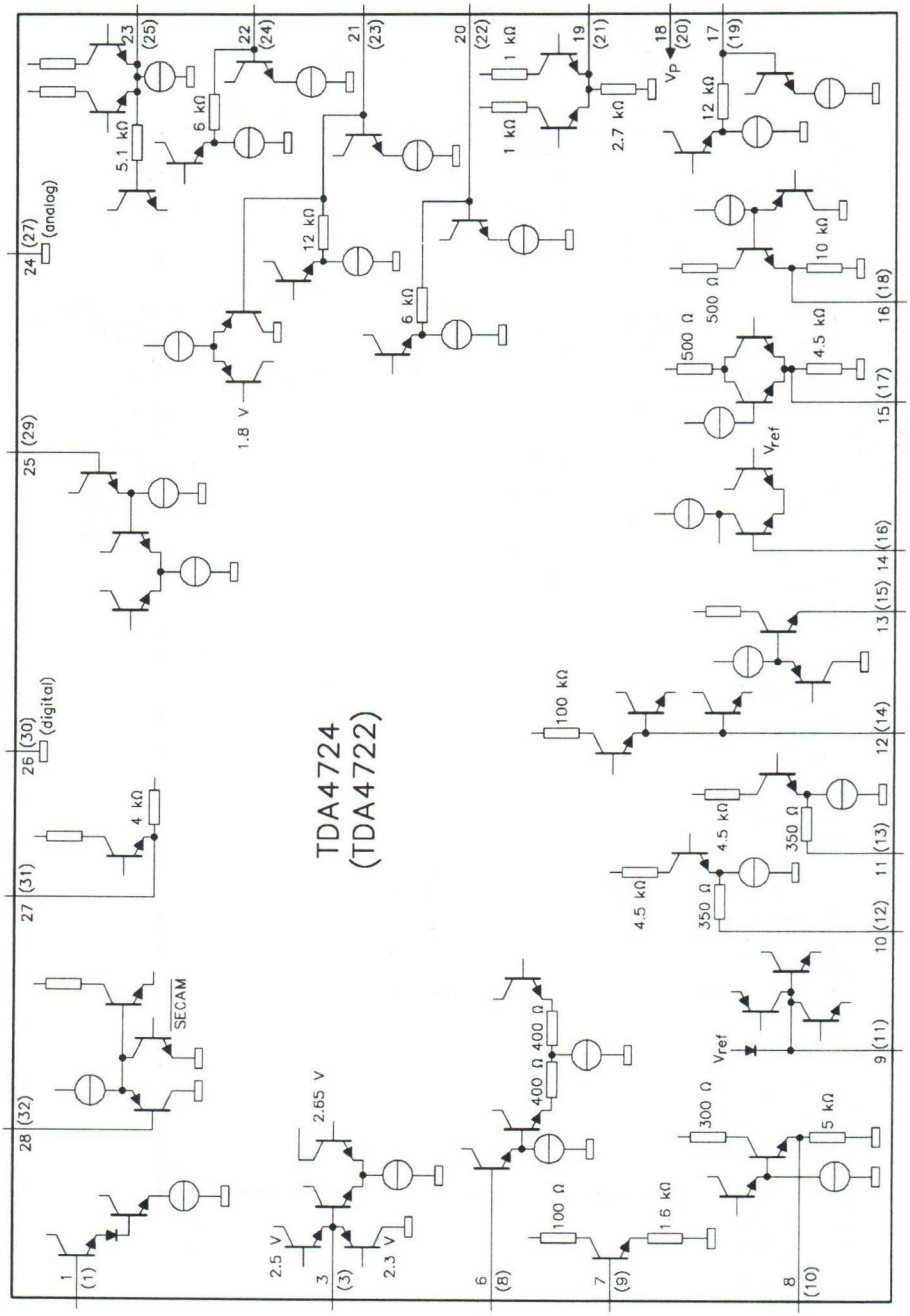


Fig.2 Internal pin configuration diagram.

PINNING

TDA4722	TDA4724	DESCRIPTION
1	1	chrominance output (4.4 MHz)
2	2	not connected
3	3	SECAM switch
4	4	not connected
5	5	not connected
6	–	not connected
7	–	not connected
8	6	mixer input
9	7	reference voltage
10	8	rectifier circuit output (2.2 MHz)
11	9	connection for external load capacitor for the AGC
12	10	connection for external balancing capacitor for the rectifier circuit
13	11	connection for external balancing capacitor for the rectifier circuit
14	12	output to passive anti-Bell circuit and limiter circuit (record mode) or output to Bell circuit and AGC circuit (playback mode)
15	13	10 dB amplifier output to anti-Bell circuit (record mode only)
16	14	virtual ground
17	15	chrominance signal output to tape (1.1 MHz)
18	16	output 10 dB amplifier and input active Bell filter (playback mode only)
19	17	input to 10 dB amplifier
20	18	power supply
21	19	divider output (record mode) or 6 dB amplifier output (playback mode)
22	20	external capacitor for limiting amplifier
23	21	chrominance signal input from tape (1.1 MHz) and record/playback switch
24	22	limiting amplifier input
25	23	15 dB amplifier output
26	–	not connected
27	24	analog ground
28	–	not connected
29	25	15 dB amplifier input (4.4 MHz)
30	26	digital ground
31	27	10 dB amplifier output
32	28	input for colour killer circuit

FUNCTIONAL DESCRIPTION

(see Fig.1 and pinning of TDA4724)

Recording mode

The chrominance signal is separated from the CVBS signal using an external bandpass filter and an external Bell circuit. The signal is applied to a divider (+4) via a 15 dB amplifier (pin 25) and limiter (pin 22). Once divided the 1.1 MHz signal is fed via an external bandpass filter (pins 17 and 19), an internal 10 dB amplifier (via pin 17), an external anti-Bell filter (pins 12 and 13) and a limiter stage.

E to E mode

The 4.4 MHz signal is obtained from a tap in the limiter circuit and is applied to the chrominance output (pin 1) via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

Playback mode

The 1.1 MHz signal from the tape is applied, via a trap, to an internal 6 dB amplifier (via pin 21). Once amplified the signal is applied via an external bandpass filter and 10 dB amplifier to an operational amplifier (pins 12 and 14). The operational amplifier has an external anti-Bell circuit connected in its feedback path and, consequently, performs as a Bell circuit. From the operational amplifier the signal is applied to the AGC stage. The output signal from the AGC stage is applied to a rectifier where the frequency is doubled. Unwanted harmonics are removed by an external bandpass filter (pins 6 and 8) and the frequency is again doubled by the mixer at pin 6. The resultant 4.4 MHz signal is applied to the output stage at pin 1 via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

NOTE: The 1.07 MHz bandpass filter (pins 17 and 19) and the anti-Bell circuit (pins 12 and 13) are used in both the record and playback mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–	6	V
P_{tot}	total power dissipation	–	250	mW
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C

CHARACTERISTICS (TDA4722 pinning in parenthesis)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin 1 (Pin 1)						
$V_{1-24(p-p)}$	chrominance output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	–	–	1	V
V_{1-24}	DC level	SECAM signal	–	V_{28-24}	–	V
		non-SECAM signal	–	–	0.1	V
R_{1-24}	output resistance		–	V_t/I_e	–	Ω
α_1	non-SECAM signal suppression		40	–	–	dB
Pin 3 (Pin 3)						
V_{3-24}	SECAM mode active voltage		3.0	–	–	V
V_{3-24}	SECAM mode inactive voltage		–	–	2.2	V
R_{3-24}	input resistance 1	V_3 = 1.8 to 3.0 V	22	25	28	kΩ
R_{3-24}	input resistance 2		–	V_t/I_e	–	Ω
Pin 6 (Pin 8)						
V_{6-24}	input signal	2.2 MHz sinusoidal signal	–	300	–	mV
V_{6-24}	DC level		–	V_{7-24}	–	V
R_{6-7}	input resistance		–	560	1200	Ω
C_{6-24}	input capacitance		–	–	5	pF
Pin 7 (Pin 9)						
V_{7-24}	DC level		2.4	2.5	2.6	V
I_7	output current		–	–	–5	mA
I_7	input current		1	–	–	mA
R_{7-24}	output resistance		–	–	1	Ω
Pin 8 (Pin 10)						
$V_{8-24(p-p)}$	output signal voltage (peak-to-peak value)	2.2 MHz	–	600	–	mV
V_{8-24}	DC level		–	2.45	–	V
R_{8-24}	output resistance		–	V_t/I_e	–	Ω
α_8	1.1 MHz suppression		30	–	–	dB
α_8	3.3 MHz suppression		30	–	–	dB
α_8	4.4 MHz suppression		10	–	–	dB
Pin 12 (Pin 14)						
$V_{12-24(p-p)}$	input signal (peak-to-peak value)	playback mode	24	–	320	mV
V_{12-24}	DC level	record mode	–	V_{13-24}	–	V
		playback mode (closed loop)	–	V_{7-24}	–	V
B	gain bandwidth (operational amplifier)	playback mode	40	–	–	MHz
R_{12-24}	input resistance	record mode	100	–	–	kΩ
R_{12}	open-loop output resistance		–	V_t/I_e	–	Ω
Pin 13 (Pin 15)						
V_{13-24}	DC level	record mode	–	V_{7-24} – 85 mV	–	V
G_{13-24}	signal gain	record mode	–	10	–	dB
R_{13-24}	output resistance	record mode	–	V_t/I_e	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin 14 (Pin 16)						
V_{14-24}	DC level	playback mode	–	V_{7-24}	–	V
Pin 15 (Pin 17)						
$V_{15-24(p-p)}$	chrominance output (peak-to-peak value)		560	630	700	mV
V_{15-24}	DC level		–	V_{7-24} – 80 mV	–	V
R_{15-24}	output resistance		–	–	10	Ω
α_{15}	playback suppression		30	–	–	dB
α_{15}	non-SECAM suppression		40	–	–	dB
Pin 16 (Pin 18)						
V_{16-24}	DC level	playback mode	–	V_{7-24} – 54 mV	–	V
G_{16-17}	signal gain	playback mode	–	10	–	dB
R_{16-24}	input resistance	record mode	–	10	–	kΩ
R_{16-24}	output resistance	playback mode	–	V_t/I_e	–	Ω
Pin 17 (Pin 19)						
$V_{17-24(p-p)}$	input signal (peak-to-peak value)		–	400	–	mV
V_{17-24}	DC level		–	V_{7-24} – 30 mV	–	V
R_{17-24}	input resistance		8	12	16	kΩ
C_{17-24}	input capacitance		–	–	5	pF
Pin 19 (Pin 21)						
V_{19-24}	DC level	record mode	–	1.82	–	V
		playback mode	–	1.7	–	V
$V_{19-24(p-p)}$	AC level (peak-to-peak value)	sinusoidal	–	800	–	mV
		block	–	621	–	mV
G_{19-24}	signal gain	playback mode	–	6	–	dB
R_{19-24}	output resistance		–	V_t/I_e	–	Ω
Pin 21 (Pin 23)						
$V_{21-24(p-p)}$	input signal (peak-to-peak value)	playback mode	–	300	600	mV
V_{21-24}	DC level		–	3.25	–	V
V_{21-24}	record mode active voltage level		–	–	1.5	V
V_{21-24}	playback mode active voltage level		2.2	–	–	V
R_{21-24}	input resistance		8	12	16	kΩ
C_{21-24}	input capacitance		–	–	5	pF
Pin 25 (Pin 29)						
$V_{25-24(p-p)}$	input signal (peak-to-peak value)		–	–	645	mV
V_{25-24}	DC level		–	V_{7-24}	–	V
R_{25-24}	input resistance		100	–	–	kΩ
C_{25-24}	input capacitance		–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin 27 (Pin 31)						
R_{27-24}	output resistance		–	–	10	Ω
RECORD MODE						
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 600 $mV_{(p-p)}$	–	1175	–	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 300 $mV_{(p-p)}$	–	1110	–	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 30 $mV_{(p-p)}$	–	272	–	mV
V_{27-24}	DC level		–	1.65	–	V
PLAYBACK MODE						
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	–	1175	–	mV
V_{27-24}	DC level		–	3	–	V
G_{27-6}	signal gain		–	12	–	dB
α_{27}	2.2 MHz suppression		23	–	–	dB
α_{27}	6.6 MHz suppression		30	–	–	dB
α_{27}	8.8 MHz suppression		10	–	–	dB
Pin 28 (Pin 32)						
$V_{28-24(p-p)}$	input signal (peak-to-peak value)		–	–	1000	mV
V_{28-24}	DC level		–	V_{27-24}	–	V
R_{28-24}	input resistance		100	–	–	kΩ
C_{28-24}	input capacitance		–	–	5	pF

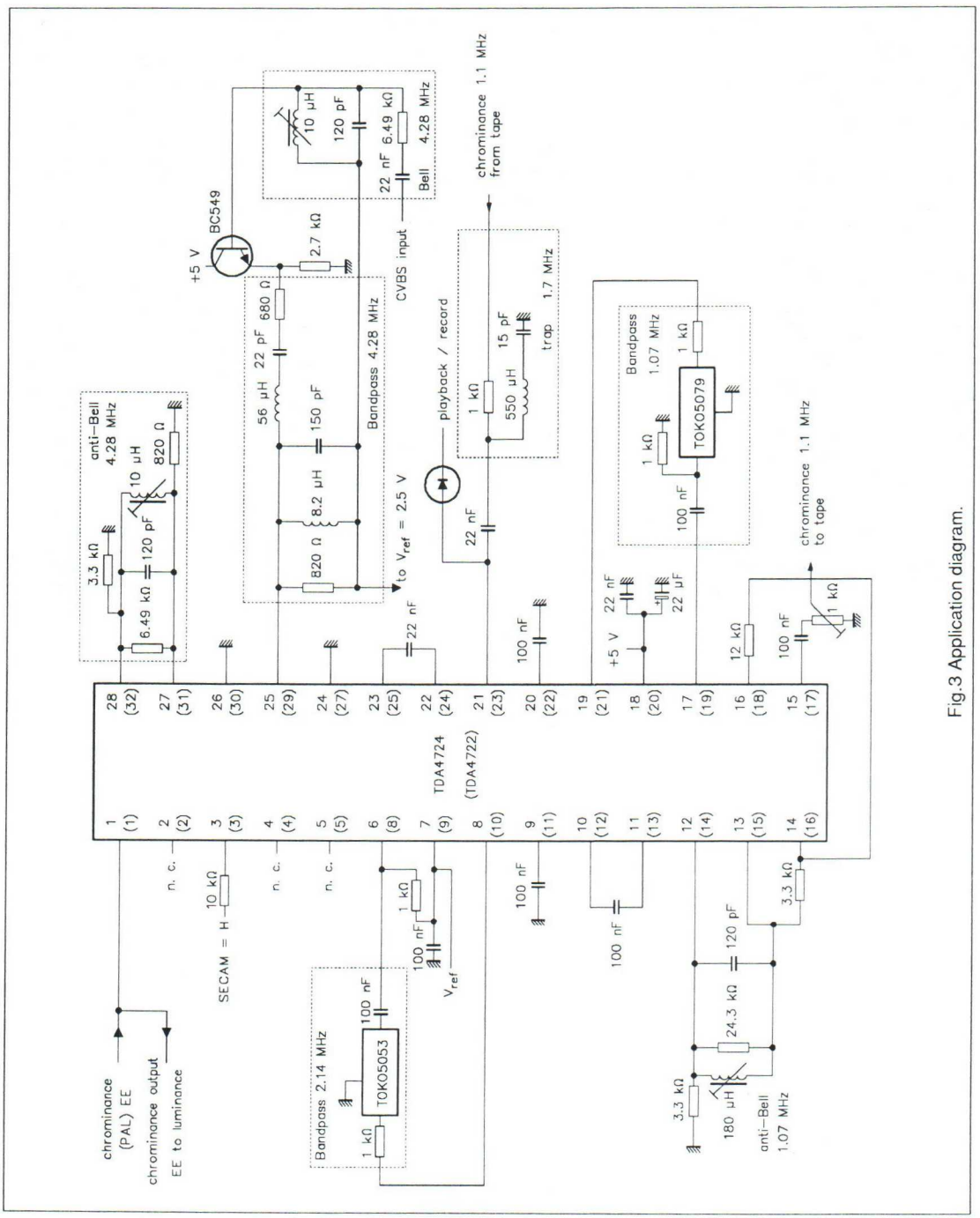


Fig.3 Application diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4725T

SECAM-L chrominance processor for VHS video recorders

FEATURES

- Forced recording or playback mode input
- SECAM identification circuit
- One circuit for Bell and anti-Bell filter (1.07 MHz)
- Fully ESD protected
- Low power consumption (170 mW)
- 5 V supply.

GENERAL DESCRIPTION

The TDA4725 is a bipolar integrated circuit for chrominance processing of SECAM-L signals in SECAM-L or Multistandard VHS video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{18\text{-}24,26}$	supply voltage		4.5	5.0	5.5	V
I_{18}	supply current		-	34	-	mA
$V_{25\text{-}24(p\text{-}p)}$ $V_{21\text{-}24(p\text{-}p)}$	chrominance input (peak-to-peak value)	record mode playback mode	- -	- 300	645 600	mV mV
$V_{15\text{-}24(p\text{-}p)}$ $V_{1\text{-}24(p\text{-}p)}$	chrominance output (peak-to-peak value)	record mode playback mode	560 -	630 -	700 1000	mV mV
T_{amb}	operating ambient temperature range		0	-	70	°C
T_{stg}	storage temperature range		–25	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4725	28	DIL28	plastic	SOT117
TDA4725T	28	SO28	plastic	SOT136A

SECAM-L chrominance processor for VHS video recorders

TDA4725T

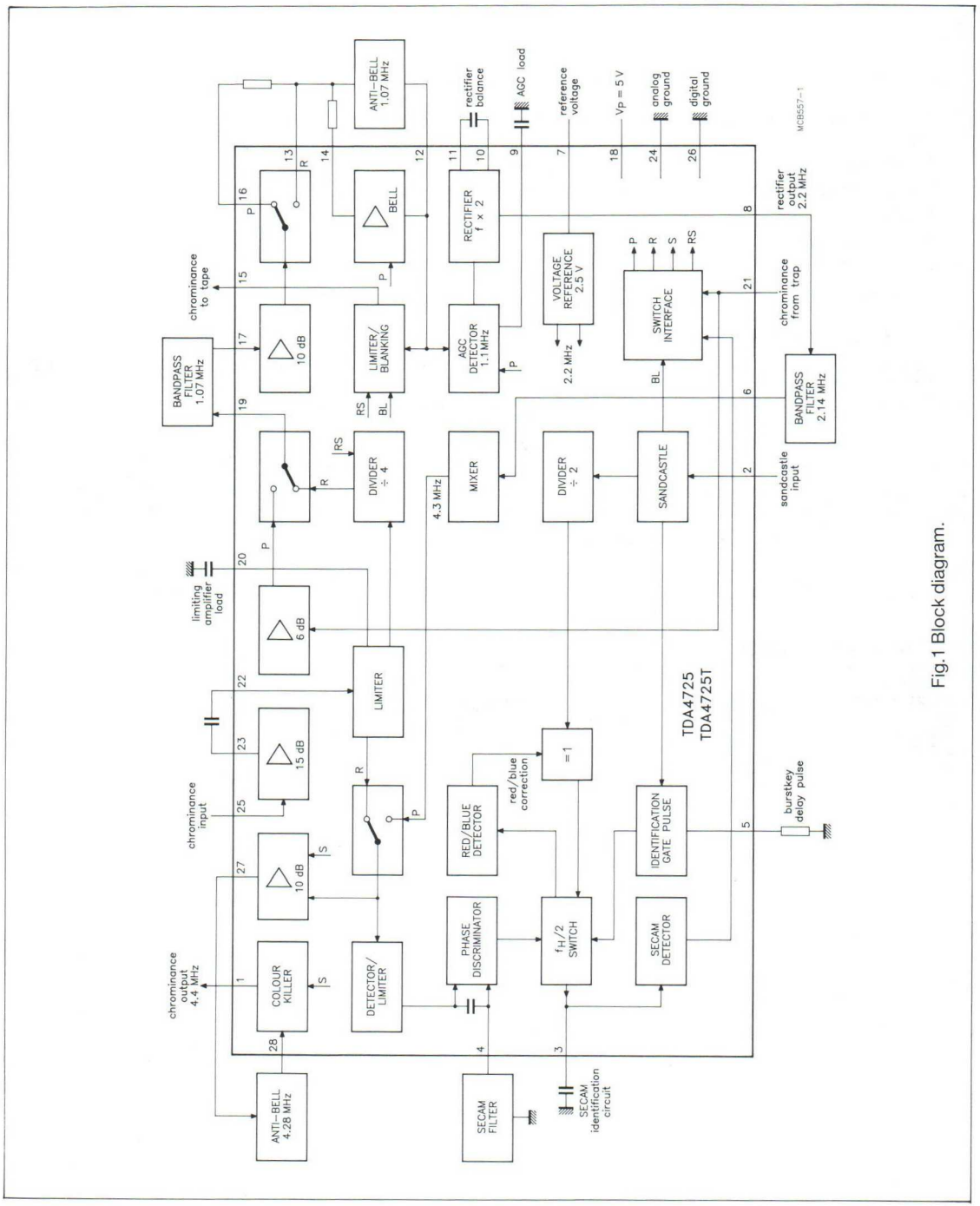


Fig.1 Block diagram.

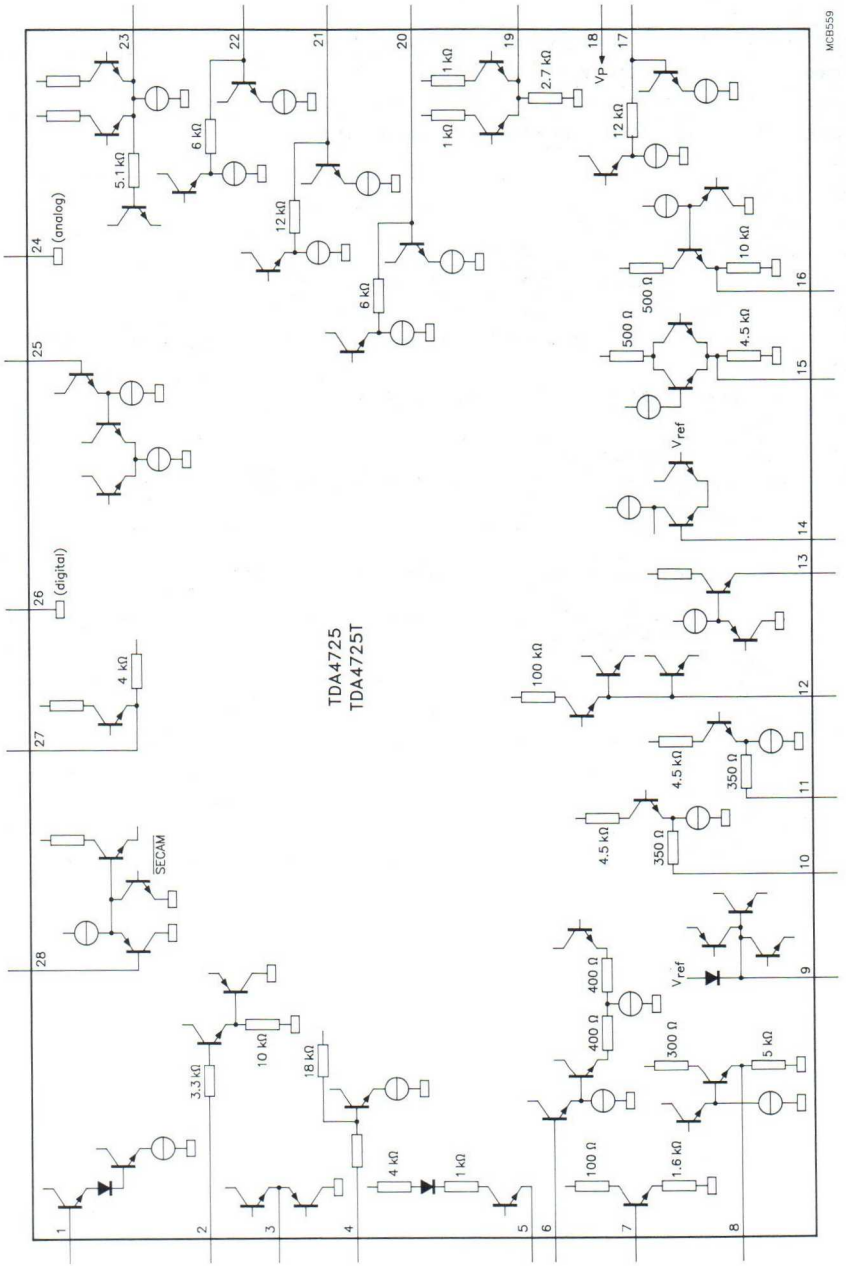


Fig.2 Internal pin configuration diagram.

PINNING

PIN	DESCRIPTION
1	chrominance output (4.4 MHz)
2	sandcastle pulse or composite synchronization pulse input
3	connection for external load capacitor for the SECAM identification circuit
4	connection for external resonance circuit for the phase discriminator circuit
5	connection for resistor required for internal delay of burstkey pulse
6	mixer input
7	reference voltage
8	rectifier circuit output (2.2 MHz)
9	connection for external load capacitor for the AGC
10	connection for external balancing capacitor for the rectifier circuit
11	connection for external balancing capacitor for the rectifier circuit
12	output to passive anti-Bell circuit and limiter circuit (record mode) or output to Bell circuit and AGC circuit (playback mode)
13	10 dB amplifier output to anti-Bell circuit (record mode only)
14	virtual ground
15	chrominance signal output to tape (1.1 MHz)
16	output 10 dB amplifier and input active Bell filter (playback mode only)
17	input to 10 dB amplifier
18	power supply
19	divider output (record mode) or 6 dB amplifier output (playback mode)
20	external capacitor for limiting amplifier
21	chrominance signal input from tape
22	limiting amplifier input
23	15 dB amplifier output
24	analog ground
25	15 dB amplifier input
26	digital ground
27	10 dB amplifier output
28	input for colour killer circuit

SECAM-L chrominance processor for VHS video recorders

TDA4725T

FUNCTIONAL DESCRIPTION (see Fig.1)

Recording mode

The chrominance signal is separated from the CVBS signal using an external bandpass filter and an external Bell circuit. The signal is applied to a divider (÷ 4) via a 15 dB amplifier (pin 25) and limiter (pin 22). Once divided the 1.1 MHz signal is fed via an external bandpass filter (pins 17 and 19), an internal 10 dB amplifier (via pin 17), an external anti-Bell filter (pins 12 and 13) and a limiter/blanking stage. The blanking stage is active during the sandcastle pulses.

E to E mode

The 4.4 MHz signal is obtained from a tap in the limiter circuit and is applied to the chrominance output (pin 1) via the 10 dB amplifier, the external anti-Bell circuit and the colour-killer stage

Playback mode

The 1.1 MHz signal from the tape is applied, via a trap, to an internal 6 dB amplifier (via pin 21). Once amplified the signal is applied via an external bandpass filter and 10 dB amplifier to an operational amplifier (pins 12 and 14). The operational amplifier has an external anti-Bell circuit connected in its feedback path and, consequently, performs as a Bell circuit. From the operational amplifier the signal is applied to the AGC stage. The output signal from the AGC stage is applied to a rectifier where the frequency is doubled. Unwanted harmonics are removed by an external bandpass filter (pins 6 and 8) and the frequency is again doubled by the mixer at pin 6. The resultant 4.4 MHz signal is applied to the output stage at pin 1 via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

NOTE: The 1.07 MHz bandpass filter (pins 17 and 19) and the anti-Bell circuit (pins 12 and 13) are used in both the record and playback mode.

SECAM identification

For SECAM identification the input signal is phase shifted by an external resonent circuit [$f_O = (f_b + f_r)/2$] and fed to the phase discriminator at pin 4. If the signal is a SECAM signal the positive- and negative-going pulses (with reference to the clamping voltage) are generated and rectified via the H/2 demodulator. The signal now consists of positive-going pulses only which are integrated via an external capacitor and applied to the SECAM detector at pin 3.

A non-SECAM signal (i.e. PAL) is removed from the phase discriminator having only positive-going pulses. After the H/2 demodulator, the signal has line-alternate positive- and negative-going pulses which compensate after integration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Ratings System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	-	6	V
P_{tot}	total power dissipation	-	250	mW
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 1						
$V_{1-24(p-p)}$	chrominance output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	-	1	V
V_{1-24}	DC level	SECAM signal non-SECAM signal	- -	V_{28-24} -	- 0.1	V V
R_{1-24}	output resistance		-	V_t/I_e	-	Ω
α_1	non-SECAM signal suppression		40	-	-	dB
Pin 2						
V_{2-24}	phase discriminator active voltage level		3.6	-	V_P	V
V_{2-24}	blanking active voltage level		2.0	2.5	3.0	V
V_{2-24}	blanking and phase discriminator inactive voltage level		-	-	1.5	V
R_{2-24}	input resistance		20	-	-	kΩ
Pin 4						
R_{4-24}	input resistance		14	18	22	kΩ
Pin 5						
R_{5-24}	required resistance to ground	for 1 μs	-	26	-	kΩ
Pin 6						
V_{6-24}	input signal	2.2 MHz sinusoidal signal	-	300	-	mV
V_{6-24}	DC level		-	V_{7-24}	-	V
R_{6-7}	input resistance		-	560	1200	Ω
C_{6-24}	input capacitance		-	-	5	pF
Pin 7						
V_{7-24}	DC level		2.4	2.5	2.6	V
$-I_7$	output current		-	-	5	mA
I_7	input current		1	-	-	mA
R_{7-24}	output resistance		-	-	1	Ω
Pin 8						
$V_{8-24(p-p)}$	output signal voltage (peak-to-peak)	2.2 MHz	-	600	-	mV
V_{8-24}	DC level		-	2.45	-	V
R_{8-24}	output resistance		-	V_t/I_e	-	Ω
α_8	1.1 MHz suppression		30	-	-	dB
α_8	3.3 MHz suppression		30	-	-	dB
α_8	4.4 MHz suppression		10	-	-	dB
Pin 12						
$V_{12-24(p-p)}$	input signal (peak-to-peak value)	playback mode	24	-	320	mV
V_{12-24}	DC level	record mode playback mode (closed loop)	- -	V_{13-24} V_{7-24}	- -	V V
B	gain bandwidth (operational amplifier)	playback mode	40	-	-	MHz
R_{12-24}	input resistance	record mode	100	-	-	kΩ
R_{12}	open-loop output resistance		-	V_t/I_e	-	Ω

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 13 V_{13-24}	DC level	record mode	-	V_{7-24} – 85 mV	-	V
G_{13-24}	signal gain	record mode	-	10	-	dB
R_{13-24}	output resistance	record mode	-	V_t/I_e	-	Ω
Pin 14 V_{14-24}	DC level	playback mode	-	V_{7-24}	-	V
Pin 15 $V_{15-24(p-p)}$	chrominance output (peak-to-peak value)		560	630	700	mV
V_{15-24}	DC level		-	V_{7-24} – 80 mV	-	V
R_{15-24}	output resistance		-	-	10	Ω
α_{15}	playback suppression		30	-	-	dB
α_{15}	non-SECAM suppression		40	-	-	dB
α_{15}	blanking suppression		30	-	-	dB
Pin 16 V_{16-24}	DC level	playback mode	-	V_{7-24} – 54 mV	-	V
G_{16-17}	signal gain	playback mode	-	10	-	dB
R_{16-24}	input resistance	record mode	-	10	-	kΩ
R_{16-24}	output resistance	playback mode	-	V_t/I_e	-	Ω
Pin 17 $V_{17-24(p-p)}$	input signal (peak-to-peak value)		-	400	-	mV
V_{17-24}	DC level		-	V_{7-24} – 30 mV	-	V
R_{17-24}	input resistance		8	12	16	kΩ
C_{17-24}	input capacitance		-	-	5	pF
Pin 19 V_{19-24}	DC level	record mode playback mode	- -	1.82 1.7	- -	V V
$V_{19-24(p-p)}$	AC level (peak-to-peak value)	sinusoidal	-	800	-	mV
		block	-	621	-	mV
G_{19-24}	signal gain	playback mode	-	6	-	dB
R_{19-24}	output resistance		-	V_t/I_e	-	Ω
Pin 21 $V_{21-24(p-p)}$	input signal (peak-to-peak)	playback mode	-	300	600	mV
V_{21-24}	DC level		-	3.25	-	V
V_{21-24}	record mode active voltage level		-	-	1.5	V
V_{21-24}	playback mode active voltage level		2.2	-	-	V
R_{21-24}	input resistance		8	12	16	kΩ
C_{21-24}	input capacitance		-	-	5	pF
Pin 25 $V_{25-24(p-p)}$	input signal (peak-to-peak value)		-	-	645	mV
V_{25-24}	DC level		-	V_{7-24}	-	V
R_{25-24}	input resistance		100	-	-	kΩ
C_{25-24}	input capacitance		-	-	5	pF

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 27 R_{27-24}	output resistance		-	-	10	Ω
RECORD MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 600 mV (p-p)	-	1175	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 300 mV (p-p)	-	1110	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 30 mV(p-p)	-	272	-	mV
V_{27-24}	DC level		-	1.65	-	V
PLAYBACK MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	1175	-	mV
V_{27-24}	DC level		-	3	-	V
G_{27-6}	signal gain		-	12	-	dB
α_{27}	2.2 MHz suppression		23	-	-	dB
α_{27}	6.6 MHz suppression		30	-	-	dB
α_{27}	8.8 MHz suppression		10	-	-	dB
Pin 28 $V_{28-24(p-p)}$	input signal (peak-to-peak)		-	-	1000	mV
V_{28-24}	DC level		-	V_{27-24}	-	V
R_{28-24}	input resistance		100	-	-	kΩ
C_{28-24}	input capacitance		-	-	5	pF

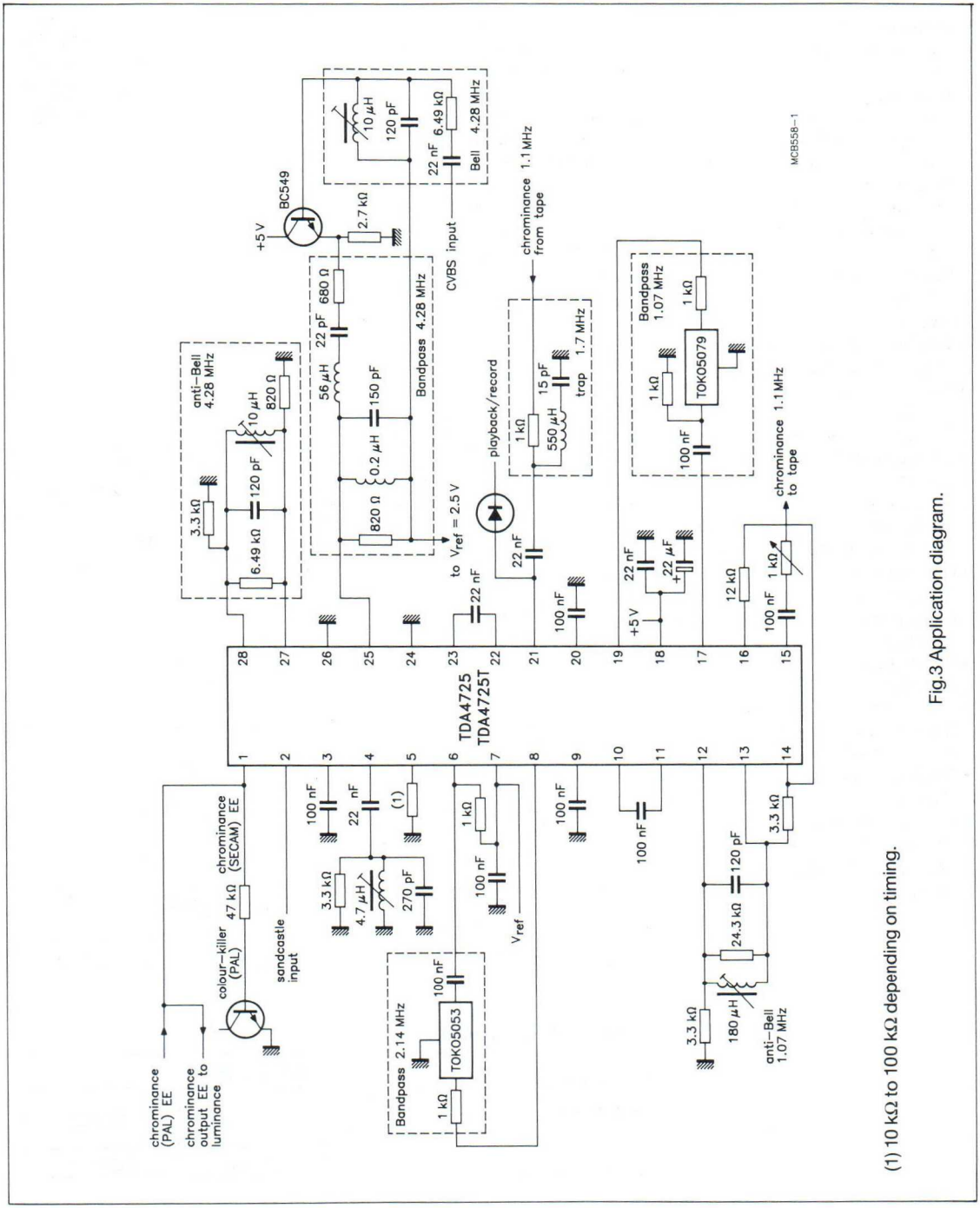


Fig.3 Application diagram.

(1) 10 kΩ to 100 kΩ depending on timing.

RGB video processor with automatic cut-off control and gamma adjust

TDA4780

FEATURES

- Gamma adjust
- Dynamic black control (adaptive black)
- All input signals clamped on black-levels
- Automatic cut-off control, alternative: output clamping on fixed levels
- Three adjustable reference voltage levels via I^2C-bus for automatic cut-off control
- Luminance/colour difference interface
- Two luminance input levels allowed
- Two RGB interfaces controlled by either fast switches or by I^2C-bus
- Two peak drive limiters, selection via I^2C-bus
- Blue stretch, selection via I^2C-bus
- Luminance output for scan velocity modulation (SCAVEM)
- Extra luminance output; same pin can be used as hue control output e.g. for the TDA4650 and TDA4655
- Non standard operations like 50 Hz/32 kHz are also possible
- Either 2 or 3 level sandcastle pulse applicable
- High bandwidth for 32 kHz application
- White point adjusts via I^2C-bus
- Average beam current and improved peak drive limiting
- Two switch-on delays to prevent discolouration during start-up
- All functions and features programmable via I^2C-bus
- PAL/SECAM or NTSC matrix selection.

GENERAL DESCRIPTION

The TDA4780 is a monolithic integrated circuit with a luminance and a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e.g. with the multistandard decoder TDA4655 or TDA9160 plus delay line TDA4661 or TDA4665 and the Picture Signal Improvement (PSI) IC TDA467x or from a Feature Module.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	80	100	120	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value) (C)VBS	–	0.45 / 1.43	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{O(p-p)}$	RGB output at pins 24, 22 and 20 (black-to-white value)	–	2.0	–	V
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4780	28	DIL	plastic	SOT117

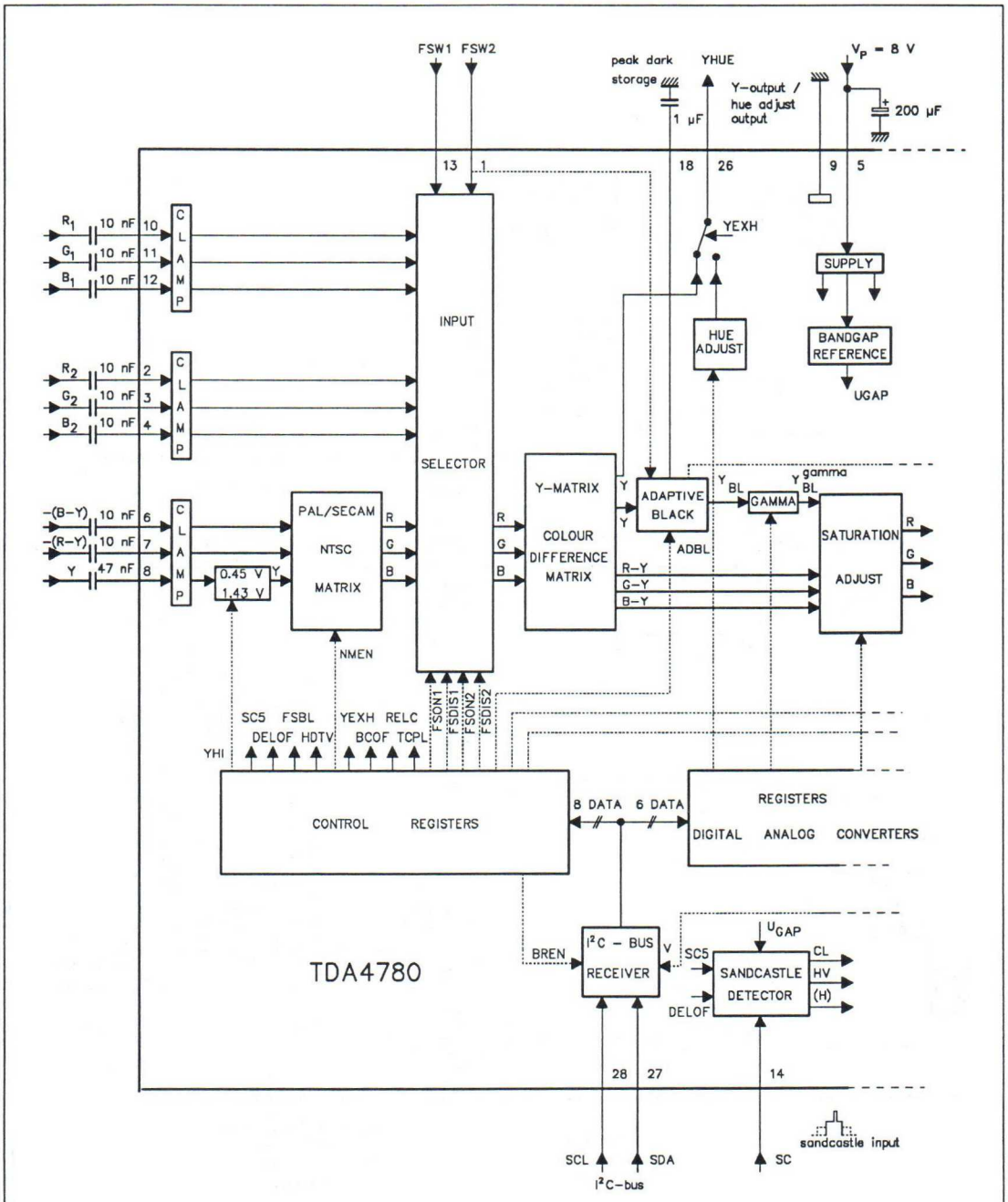


Fig.1 Block diagram (continued in Fig.2).

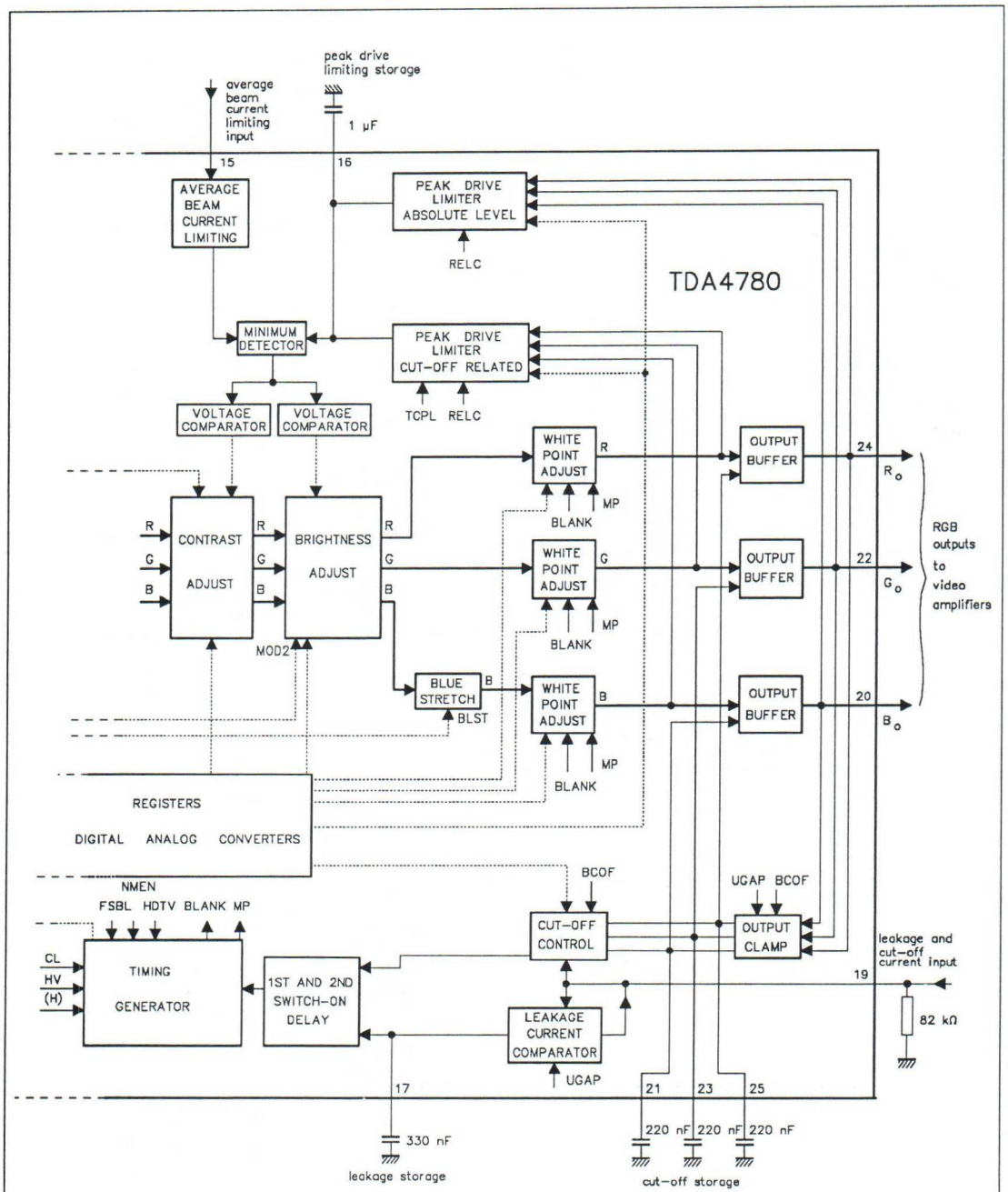


Fig.2 Block diagram (continued from Fig.1).

RGB video processor with automatic cut-off control and gamma adjust

TDA4780

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak limiting
C_L	17	storage capacitor for leakage current compensation
C_{PDST}	18	storage capacitor for peak dark
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
YHUE	26	Y-output/hue adjust output
SDA	27	I^2C-bus serial data input/acknowledge output
SCL	28	I^2C-bus serial clock input

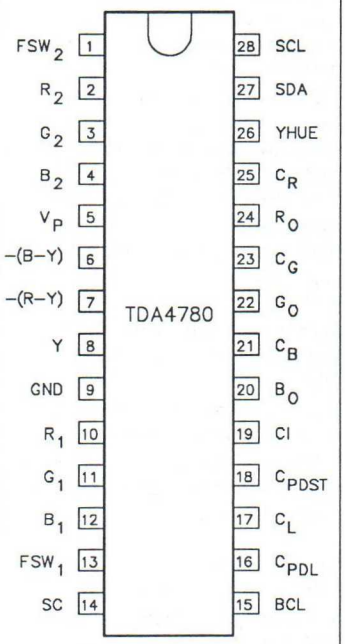


Fig.3 Pin configuration.

GENERAL DESCRIPTION

(continued)

The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector (SCART plug) and the other one from an on-screen display (OSD) generator. The TDA4780 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages. In clamped output mode it can also be used as an RGB source.

The main differences to the sister type TDA4680 are:

- additional features, namely gamma adjust, adaptive black, blue stretch and two different peak drive limiters.
- the measurement lines are triggered by the trailing edge of the vertical component of the sandcastle pulse.
- I^2C-bus receiver only. Automatic white level control is not provided; the white levels are determined directly by the I^2C-bus data.
- the TDA4780 is pin compatible (except pin 18) to the TDA4680. The slave address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4680 then the I^2C-bus command is not executed. Special commands (except control bit FSWL) for the TDA4680 will be ignored by the TDA4780.

FUNCTIONAL DESCRIPTION

Signal input stages

The TDA4780 contains 3 sets of input signal stages for:
a) Luminance/colour-difference signals: (Y: 0.45 V(p-p) VBS or 1.43 V(p-p) VBS, selectable via I^2C-bus, –(R–Y): 1.05 V(p-p); –(B–Y): 1.33 V(p-p)). The capacitively coupled signals are matrixed to RGB signals by either a PAL/SECAM or NTSC matrix (selected via I^2C-bus).
b) $(RGB)_1$ signals (0.7 V(p-p) VB), capacitively coupled (e.g. from external source).
c) $(RGB)_2$ signals (0.7 V(p-p) VB), capacitively coupled (e.g. videotext, OSD).
All input signals are clamped in order to have the same black levels at the signal switch input. Displayed signals must be synchronous with the sandcastle pulse.

Signal switches

Both fast signal switches can be operated by switching pins (e.g. SCART facilities) or set via the I^2C-bus. By switch 1 the Y-CD signals or the $(RGB)_1$ signals can be selected, by switch 2 the above selected signals or the $(RGB)_2$ signals are enabled. During the vertical and horizontal blanking time an artificial black level equal to the clamped black level is inserted in order to clip off the sync pulse of the luminance signal and to suppress hum during the cut-off measurement time and eliminate noise during these intervals.

Saturation, gamma, contrast and brightness adjust

Saturation, contrast and brightness adjusts are adjusted via the I^2C-bus and act on Y, CD as well as on RGB input signals. Gamma acts on the luminance content of the input signals.

Gamma adjust

The gamma adjust stage has a non-linear transmission characteristic according to the formula $y = x^{gamma}$, where x represents the input and y the output signal. If gamma is smaller than unity, the lower parts of the signal are amplified with higher gain.

Adaptive black (ADBL)

The adaptive black stage detects the lowest voltage of the luminance component of the internal RGB signals during the scanning time and shifts it to the nominal black level. In order to keep the nominal white level the contrast is increased simultaneously.

Blue stretch (BLST)

The blue stretch channel gets additional amplification if the blue signal is greater than 80% of the nominal signal amplitude. In that case the white point is shifted towards higher colour temperature so that white parts of a picture seem to be brighter.

Measurement pulse and blanking stage

During the vertical and horizontal blanking time and the measurement period the signals are blanked to an ultra black level, so the leakage current of the picture tube can be measured and automatically compensated for.
During the cut-off measurement lines (one line period for each R, G or B) the output signal levels are at cut-off measurement level.
The vertical blanking period is timed by the sandcastle pulse. The measurement pulses (leakage, R, G and B) are triggered by the negative going edge of the vertical pulse of the sandcastle pulse and start after the following horizontal pulse.
The IC is prepared for $2f_H$ (32 kHz) application.

Output amplifier and white adjust potentiometer

The RGB signals are amplified to nominal 2 V(p-p), the DC-levels are shifted according to cut-off control. The nominal signal amplitude can be varied by ±50% by the white point adjustment via the I^2C-bus (individually for RGB respect).

Automatic cut-off control

During leakage measurement time the leakage current is compensated in order to get a reference voltage at the cut-off measurement info pin. This compensation value is stored in an external capacitor. During cut-off current measurement times for the R, G and B channels, the voltage at this pin is compared with the reference voltage, which is individually adjustable via I^2C-bus for each colour channel. The so derived control voltages are stored in the external feedback capacitors. Shift stages add these voltages to the corresponding output signals. The automatic cut-off control may be disabled via the I^2C-bus. In this mode the output voltage is clamped to 2.5 V. Clamping periods are the same as the cut-off measurement periods.

Signal limiting

The TDA4780 provides two kinds of signal limiting. First, an average beam limiting, that reduces signal level if a certain average is exceeded. Second, a peak drive limiting, that is activated if one of the RGB signals even shortly exceeds a via I^2C-bus adjusted threshold. The latter can be either referred to the cut-off measurement level of the outputs or to ground.
When signal limiting occurs, contrast is reduced, and at minimum contrast brightness is reduced additionally.

Sandcastle decoder and timer
A 3-level detector separates the sandcastle pulse into combined line and field pulses, line pulses, and clamping pulses. The timer contains a line counter and controls the cut-off control measurement. Application with a 2-level 5 V sandcastle pulse is possible.

Switch on delay circuit
After switch on all signals are blanked and a warm up test pulse is fed to the outputs during the cut-off measurement lines. If the voltage at the cut-off measurement input exceeds an internal level the cut-off control is enabled but the signal remains still blanked. The signal blanking is finished when the cut-off control has stabilized. In case of output clamping, the cut-off control is disabled and the switch on procedure will be skipped.

Y output and hue adjust
The TDA4780 contains a D/A converter for hue adjust. The analog information can be fed, e.g. to the multistandard decoder TDA4650 or TDA4655. This output pin may be switched to a Y output signal, which can be used for scan velocity modulation (SCAVEM). The Y output is the Y input signal or the matrixed (RGB) input signal according to the switch position of fast switch.

I^2C-bus
The TDA4780 contains an I^2C-bus receiver for control function.

ESD protection
Pins are provided with protection diodes against ground and supply voltage (see pin description). I^2C-bus input pins do not shunt the I^2C-bus signals in case of missing supply voltage.

EMC
Pins are protected against electromagnetic radiation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
P_{tot}	total power dissipation	–	1200	mW
$V_{5-9} = V_P$	supply voltage	–0.1	+9.0	V
$V_{10,11,12-9}$	$(RGB)_1$ inputs	–0.1	V_P	V
$V_{2,3,4-9}$	$(RGB)_2$ inputs	–0.1	V_P	V
$V_{8,7,6-9}$	Y, CD-inputs	–0.1	V_P	V
$V_{13,1-9}$	switch I, II	–0.1	V_P	V
$V_{25,23,21,17-9}$	black level, leakage storage	–0.1	V_P	V
V_{14-9}	sandcastle	–0.7	$V_P + 5.8$	V
V_{15-9}	average current inf.	–0.7	$V_P + 0.7$	V
V_{16-9}	peak drive storage	–0.1	V_P	V
$V_{27,28-9}$	I^2C-bus	–0.1	V_P	V
I_{26}	Y output / hue adjust	–8	–	mA
V_{18-9}	peak dark storage	–0.1	V_P	V
V_{19-9}	cut-off control input	–0.7	$V_P + 0.7$	V
$I_{24,22,20}$	output peak	–20	–	mA
$I_{24,22,20}$	output average	–10	–	mA
ESD	electrostatic handling (note 1) for all pins	–500	+500	V

Note to the Limiting Values

1. Charge device model class A: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	47 K/W

QUALITY SPECIFICATION

URV-4-2-59/601

CHARACTERISTICS

T_{amb} = +25 °C; V_P = 8 V; V_{nom}: nominal signal amplitude (black-white) 2000 mV (peak-to-peak value) at output pins; gamma = 1; adaptive black inactive; brightness, contrast, saturation and white balance at nominal settings; no beam current or peak drive limiting; all voltages are related to ground (pin 9) and measured in Figs 1 and 2; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8	8.8	V
I_P	supply current (pin 5)		–	100	120	mA
Colour-difference inputs (–(B–Y): pin 6, –(R–Y): pin 7; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω)						
V_6	–(B–Y) signal (peak-to-peak value)	75% colour bar signal	–	1.33	–	V
$V_{6,7}$	internal bias during clamping		–	4.0	–	V
$I_{6,7}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{6,7}$	maximum input current during clamping		100	180	260	µA
V_7	–(R–Y) signal (peak-to-peak value)	75% colour bar signal	–	1.05	–	V
$R_{6,7}$	AC input resistance		10.0	–	–	MΩ
Y input (pin 8; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω)						
V_8	input signal (composite signal; VBS; peak-to-peak value)	adaption to two different signal levels via control bit YHI				
		YHI = 0	–	0.45	–	V
		YHI = 1	–	1.43	–	V
R_8	AC input resistance		10.0	–	–	MΩ
V_8	internal bias during clamping	YHI = 0	–	3.7	–	V
		YHI = 1	–	4.6	–	V
I_8	DC input current between clamping pulses		–	–	0.1	µA
I_8	maximum input current during clamping		100	180	260	µA
RGB input 1 (R_1: pin 10, G_1: pin 11, B_1: pin 12; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω; note 1)						
$V_{10,11,12}$	input signal (peak-to-peak value)		–	0.7	–	V
$R_{10,11,12}$	AC input resistance		10.0	–	–	MΩ
$V_{10,11,12}$	internal bias during clamping		–	5.1	–	V
$I_{10,11,12}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{10,11,12}$	maximum input current during clamping		100	180	260	µA
RGB input 2 (R_2: pin 2, G_2: pin 3, B_2: pin 4; capacitively coupled to a low ohmic source; recommendation: maximum 600 Ω; note 1)						
$V_{2,3,4}$	input signal (peak-to-peak value)		–	0.7	–	V
$R_{2,3,4}$	AC input resistance		10.0	–	–	MΩ
$V_{2,3,4}$	internal bias during clamping		–	5.1	–	V
$I_{2,3,4}$	DC input current between clamping pulses		–	–	0.1	µA
$I_{2,3,4}$	maximum input current during clamping		100	180	260	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/SECAM and NTSC matrix (note 2; for demodulation axis see appendix)						
PAL/SECAM matrix		control bit NMEN = 0				
NTSC matrix		control bit NMEN = 1; hue position set on (–2) degrees				
Fast signal switches and blanking (fast signal switch 1 (pin 13); Y, CD / R_1, G_1, B_1; control bits FSDIS1, FSON1)						
V_{13}	voltage to select Y and CD		–	0	0.4	V
V_{13}	voltage range to select R_1, G_1 and B_1		0.9	1.0	5.5	V
R_{13}	internal resistor to ground		3.3	3.8	4.8	kΩ
Crosstalk (see Table 2)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns
Fast signal switch 2 (pin 1; Y, CD or R_1, G_1, B_1 / R_2, G_2, B_2; control bits FSDIS2, FSON2)						
V_1	voltage to select Y and CD / R_1, G_1 and B_1		–	0	0.4	V
V_1	voltage range to select R_2, G_2 and B_2		0.9	1.0	5.5	V
V_1	required minimal voltage to switch off the ADBL measurement		–	0.87	1.0	V
R_1	internal resistor to ground	$R_1 > R_{13}$	2.8	4.2	6.0	kΩ
Crosstalk (see Table 2)						
$t_s - t_i$	difference between transit times for signal switching and signal insertion		–	–	10	ns
Adjust stages (adaptive black, gamma, contrast, saturation, brightness and white point adjust, blue stretch)						
Adaptive black (detectors inactive status due to action of fast switch 2 (pin 1); see Table 1, Fig.9 and note 3)						
I_{18}	discharge current of peak dark storage capacitor	outside active measurement window	0.1	0.5	1.0	µA
		inside active measurement window	1.5	2.5	3.5	µA
I_{18}	charge current of peak dark storage capacitor		–360	–300	–250	µA
	maximum level shift: Δ black level in percent of nominal signal amplitude		10	13	16	%
	difference between nominal black and adaptive black in percent of nominal signal amplitude		–3	0	+3	%
	detectors inactive time before blanking		2.3	3.1	4.0	µs
	detectors inactive time after blanking		2.3	2.5	3.4	µs
Gamma adjust Acts on internal Y signal; Y matrix see Y output; I^2C-bus controlled potentiometer (subaddress 0B) Resolution 6 bit						
	range of gamma minimum ($3F_{HEX}$) maximum (00_{HEX})		 – –	 0.7 1.0	 – –	 – –
	maximum gain at minimum gamma	near nominal black	5	6	7	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Saturation adjust Acts on RGB signals; Y matrix see Y output; I^2C-bus controlled potentiometers (subaddress 01) Resolution 1.5% of maximum saturation						
	I^2C-bus data for nominal saturation		1F	20	21	HEX
	maximum saturation	I^2C-bus data $3F_{HEX}$; measured at 100 kHz; relative to nominal saturation	4.9	5.5	6.1	dB
	minimum saturation	I^2C-bus data 00_{HEX}; measured at 100 kHz; relative to typical value of maximum saturation	–	–	–50	dB
Contrast adjust Acts on RGB signals; I^2C-bus controlled potentiometers (subaddress 02) Resolution 1.5% of maximum contrast						
	I^2C-bus data for nominal contrast		20	22	24	HEX
	maximum contrast	I^2C-bus data $3F_{HEX}$; limiters inactive; relative to nominal contrast	–	4.5	5.5	dB
	minimum contrast	I^2C-bus data 00_{HEX}; relative to maximum	–28	–22	–16	dB
Brightness adjust Acts on RGB signals; I^2C-bus controlled potentiometers (subaddress 00) Resolution 1.5% of range; Δ black level in percent of nominal signal amplitude referred to cut-off measuring level						
	maximum brightness: Δ black level	$3F_{HEX}$	23	30	37	%
	nominal brightness: Δ black level	29_{HEX}	–7	0	+7	%
	minimum brightness: Δ black level	00_{HEX}	–58	–50	–42	%
	maximum brightness: Δ black level	$3F_{HEX}$; control bits BCOF = 1 and MOD2 = 0	23	30	37	%
	minimum brightness: Δ black level	00_{HEX}; control bits BCOF = 1 and MOD2 = 0	–58	–50	–42	%
Blue stretch Blue stretch is activated by I^2C-bus control bit BLST = 1 (see Fig.10)						
	increase of small signal gain	100% of nominal signal amplitude and at 1 MHz	15	20	25	%
Differences of black level steps Differences from channel to channel of the ratio of the difference (black level cut-off measurement level) to actual nominal signal amplitude (V_{nom24}, V_{nom22}, V_{nom20}) over the whole contrast, brightness and saturation range, switching matrix or switching fast switches, gamma = 1, BLST = 0, ADBL = 0						
dV/V_{nom}	static deviation	$dV/V_{nom} = dV_{24}/V_{nom24} - dV_{22}/V_{nom22} = dV_{24}/V_{nom24} - dV_{20}/V_{nom20} = dV_{22}/V_{nom22} - dV_{20}/V_{nom20}$; ripple on pin 5 during clamping ≤ 1 mV; note 8	–1.0	–	+1.0	%
		at nominal saturation	–0.5	–	+0.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs (output for positive RGB signals (R: pin 24, G: pin 22, B: pin 20); following data without external load)						
$R_{24,22,20}$	differential output resistance		–	25	30	Ω
$I_{24,22,20}$	maximum output current		4.0	5.0	–	mA
$V_{24,22,20}$	minimum output voltage	note 9	–	–	0.8	V
$V_{24,22,20}$	maximum output voltage	$R_L \geq 2$ kΩ	6.3	7.0	–	V
$V_{24,22,20}$	maximum signal amplitude (black-white) due to internal limits (peak-to-peak value)		3.3	–	–	V
$V_{24,22,20}$	nominal signal amplitude (black-white; peak-to-peak value)	at nominal white adjust; contrast and saturation setting; gamma = 1; nominal input signals	1.7	2.0	2.3	V
$V_{24,22,20}$	range of cut-off measurement level	note 9	1.0	–	5.0	V
$V_{24,22,20}$	recommended cut-off measurement level		–	3.0	–	V
Output clamp (RGB)						
$V_{20,22,24}$	clamp voltage black level	control bit BCOF = 1	2.3	2.5	2.7	V
White potentiometers						
	I^2C-bus data for nominal settings		21	22	23	HEX
	maximum increase of AC gain	$3F_{HEX}$	40	50	60	%
	maximum decrease of AC gain	00_{HEX}	40	50	60	%
Overall white point deviation						
dV/V_{nom}	$dV/V_{nom} = dV_{24}/V_{nom24} - dV_{22}/V_{nom22} = dV_{24}/V_{nom24} - dV_{20}/V_{nom20} = dV_{22}/V_{nom22} - dV_{20}/V_{nom20}$ meaning of actual nominal signal see 'differences of black level step'; over whole contrast range see 'contrast adjust'	input: $(RGB)_{1,2}$ differences from channel to channel of the ratio of the difference (signal white level cut-off measurement level) to actual nominal signal amplitude ($V_{nom\ 24}$, $V_{nom\ 22}$, $V_{nom\ 20}$) over the whole saturation range at nominal contrast, brightness and nominal input signals; ripple on pin 5 during clamping ≤ 1 mV; note 8	–2.0	–	+2.0	%
Frequency behaviour, crosstalk						
Between the Y input (pin 8) and the RGB outputs (pins 24, 22 and 20)						
	decrease in gain	1 MΩ and 20 pF load at 13 MHz	–	–	3	dB
Between the colour-difference inputs (pins 7 and 6) and the corresponding R and B outputs (pins 24 and 20)						
	decrease in gain	at 13 MHz	–	–	3	dB
Between the $(RGB)_{1,2}$ inputs (pins 10, 11 and 12 or 2, 3 and 4) and the RGB outputs (pins 24, 22 and 20)						
	decrease in gain	at 22 MHz	–	–	3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle input (pin 14; control bit SC5; note 4)						
I_{14}	input current	$V_{14} < 0.5$ V	–	–	–100	µA
C_{14-9}	input capacitance		–	–	10	pF
V_{14}	required voltage range for horizontal and vertical blanking pulses	SC5 = 0 or SC5 = 1	2.0	2.5	3.0	V
	for horizontal pulses (line count)	SC5 = 0	4.0	4.5	4.9	V
	for burst key pulses	SC5 = 0	6.1	–	V_P + 5.8	V
	for burst key pulses and line count	SC5 = 1	4.0	–	V_P + 5.8	V
Clamp pulse delay						
	delay of leading edge of clamping pulse	nominal sandcastle pulse				
		DELOF = 0	1.2	1.5	1.8	µs
		DELOF = 1	–	0	–	µs
Required minimal burst gate pulse width						
	DELOF = 0	line frequency = 16 kHz	3	–	–	µs
	DELOF = 1	line frequency = 32 kHz	1.5	–	–	µs
Generation of measurement lines and blanking						
Blanking to ultra black level occurs during time DG except MR in R-channel, MG in G-channel, MB in B-channel (see pulse diagram Fig.11) Difference between ultra black level (VUB) and measurement level (VCL) in percent of nominal signal amplitude (independent of white point adjust)						
dV/V_{nom}	dV = VCL – VUB	no clipping	25	35	45	%
Leakage current measuring time: LM will start after the end of vertical sandcastle (see pulse diagram)						
Vertical blanking period and cut-off measurement lines (see pulse diagram) The vertical component will be identified if it contains 2 or more burst key pulses in case of SC5 = 1 or two or more line pulses (H) in case of SC5 = 0 The line counter is triggered by the leading edge The blanking time is valid for a vertical pulse detected by the sandcastle decoder The internal blank pulse is OR gated with the sandcastle vertical pulse and the end of the measurement pulses						
Insertion time: full line period Measurement time: line period minus horizontal period (50/60 Hz)						
Line sequence of measuring lines: First line after end of horizontal pulse which followed the end of vertical pulse: leakage measurement LM First line after leakage pulse: red measurement MR Second line after leakage pulse: green measurement MG Third line after leakage pulse: blue measurement MB (see pulse diagram)						
Warm up test pulse during MT (see pulse diagram)						
V_{WU}	warm up level	$V_{WU} = V_{PL} - 1$ V; V_{PL} = peak drive level (see also signal limiting); given by I^2C-bus; subaddress OA; no warm up test pulse in case of output clamping (BCOF = 1)	–	–	–	–
	maximum warm up level	$3F_{HEX}$	5.6	6.0	6.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Threshold for Power On Reset (POR) during time DG (see pulse diagram)						
$V_{20,22,24POR}$	output voltage to cause POR	RELC = 0 RELC = 1	– –	V_{PL} V_{PL} + 1	– –	V V
Y output (pin 26; note 5)						
V_{26}	nominal signal amplitude (black-white; independent of gamma, adaptive black and contrast; peak-to-peak value)	control bit YEXH = 1; hue DAC (register 03) set > 28_{HEX}	0.85	1.0	1.15	V
V_{26}	black level	YEXH = 1 $3F_{HEX}$ 20_{HEX}	 – –	 4.0 2.0	 – –	 V V
	Y matrix coefficients a_r a_g a_b	$Y = a_r R + a_g G + a_b B$	 0.27 0.53 0.10	 0.30 0.59 0.11	 0.33 0.65 0.12	 – – –
R_{26}	differential output resistance		–	190	230	Ω
$\Delta\tau_{26}$	group delay time	between RGB outputs and Y output	20	25	30	ns
f_g	3 dB bandwidth		11	15	–	MHz
Automatic cut-off control (pin 19; measurement periods see beam info on pin 19)						
V_{19}	permissible voltage (also during scanning period)		–	–	$V_P - 1.4$	V
V_{REF0}	internally controlled voltage on pin 19	during leakage measurement time LM	2.4	2.7	3.0	V
I_{19}	maximum output current		–350	–	–250	µA
I_{19}	maximum input current		250	–	350	µA
R_{19}	input resistance for measurement input		1	–	–	MΩ
I_{19}	additional input current	only during warm up	–	0.5	–	mA
V_{19}	threshold of warm up detector (active in line MG)		4.3	4.5	4.7	V
V_{MEAS}	difference between input voltage for cut-off and V_{REF0}; adjustable via I^2C-bus (subaddress for reference: R: 07, G: 08 and B: 09)		–	–	–	–
	maximum V_{MEAS}	$3F_{HEX}$	1.5	1.6	1.7	V
	nominal V_{MEAS}	20_{HEX}	0.9	1.0	1.1	V
	minimum V_{MEAS}	00_{HEX}	0.4	0.45	0.5	V
Storage of cut-off control voltage / output clamping voltage (pins 25, 23 and 21)						
$I_{25,23,21}$	input currents of storage inputs outside of the measurement time		–	–	0.1	µA
$\|I_{25,23,21}\|$	maximum charge / discharge current during measurement time		0.2	0.3	0.4	mA
	amplification from storage pins 25, 23 and 21 to outputs		–	1.7	–	–

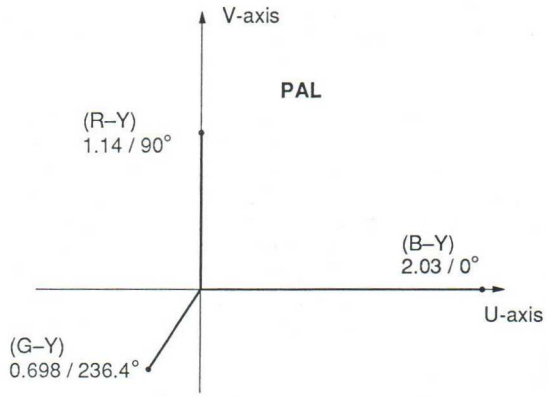
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Storage of leakage information (pin 17)						
I_{17}	maximum charge / discharge current at time LM		300	400	–	µA
I_{17}	discharge current	peak limiting during time MK active	–	4	–	mA
I_{17}	leakage current	outside time LM	–	–	0.1	µA
V_{17}	voltage to reset IC to switch on conditions	V_{17} is below	2.3	2.5	3.0	V
Signal limiting (The limitation acts on contrast and at low contrast on brightness)						
Average beam current limiting (pin 15)						
V_{15}	start of contrast reduction		–	4	–	V
dV_{15}	input range for full contrast reduction		–	–2	–	V
V_{15}	start of brightness reduction		–	2.5	–	V
dV_{15}	input range for full brightness reduction		–	–1.6	–	V
I_{15}	input current		–	–	–0.5	µA
Peak signal limiting of output signals (pin 16) The limitation acts 1 H delayed Limiting level adjustable by I^2C-bus (subaddress OA; control bit RELC = 0)						
$V_{24,22,20}$	maximum limiting level	extrapolated from 2F	6.8	–	7.2	V
$V_{24,22,20}$	minimum limiting level	00_{HEX}	–	2.3	3	V
I_{16}	maximum discharge current at peak drive	RELC = 0	4	–	6	mA
Peak signal limiting (pin 16) Control bit RELC = 1; Limiting Level (V_{LiL}) adjustable by I^2C-bus (subaddress OA)						
V_{LiL}		equal gain in white point adjust; signal only in one output channel				
	maximum limiting level	$3F_{HEX}$	3.3	3.5	3.9	V
	minimum limiting level	00_{HEX}	1.3	1.5	1.7	V
Peak drive limiting starts, if the maximum of the RGB signals after white point adjustment exceeds a threshold Cut-off measurement level MX = MR or MB or MG						
Discharge currents						
The total discharge current is a summation of $I_{16(1)} + I_{16(2)} + I_{16(3)}$						
Threshold 1 (TH1)						
$I_{16(1)}$	maximum discharge current	TH1 = MX + V_{LiL}; 1 line delayed and low-pass filtered	4.5	6	7.5	mA
	steepness		–	1.5	–	mA / 0.1 V
Low-pass filter, control bit TCPL						
t_{DPDL}	time constant low-pass filter	TCPL = 1 (at $1f_H$); RELC = 1	0.9	1.2	1.5	µs
t_{DPDL}	time constant low-pass filter	TCPL = 0 (at $2f_H$); RELC = 1	0.4	0.6	0.8	µs

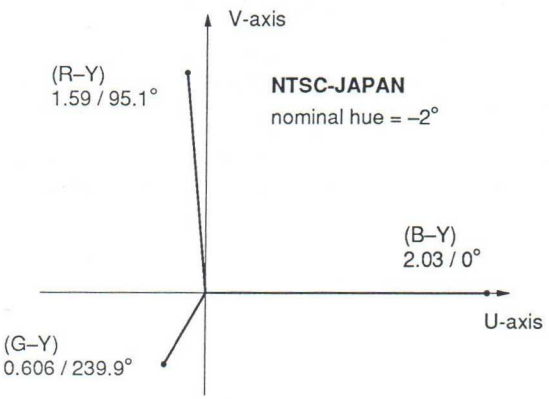
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Threshold 2 (TH2)						
$I_{16(2)}$	maximum discharge current	TH2 = MX + V_{LiL} x 1.10; 1 line delayed	4.5	6	7.5	mA
	steepness		–	1.5	–	mA / 0.1 V
Threshold 3 (TH3)						
$I_{16(3)}$	maximum discharge current	TH3 = MX + V_{LiL}; undelayed	0.45	0.6	0.75	mA
	steepness		–	0.15	–	mA / 0.1 V
Charge current						
I_{16}	charge current		–0.5	–1	–2	µA
V_{16}	start of contrast reduction		–	4	–	V
dV_{16}	input range for full contrast reduction		–	–2	–	V
V_{16}	start of brightness reduction		–	2.5	–	V
dV_{16}	input range for full brightness reduction		–	–1.6	–	V
V_{16}	maximum voltage by internal limitation		4.5	–	–	V
Hue adjust output (pin 26; note 6)						
V_{26}	minimum output voltage	YEXH = 0; 00_{HEX}	0.5	–	1.0	V
V_{26}	nominal output voltage	YEXH = 0; 20_{HEX}	3.0	3.2	3.4	V
V_{26}	maximum output voltage	YEXH = 0; $3F_{HEX}$	4.8	–	5.5	V
I_{26}	current of internal emitter follower		500	700	–	µA
I^2C-bus inputs						
f_{28}	clock frequency range		0	–	100	kHz
$t_{SU;DAT}$	data set-up		250	–	–	ns
t_H	clock pulse HIGH		4	–	–	µs
t_L	clock pulse LOW		4.7	–	–	µs
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
Input levels						
V_{27}	LOW level input voltage		–	–	1.5	V
V_{28}			–	–	1.5	V
V_{27}	HIGH level input voltage		3.0	–	5.5	V
V_{28}			3.0	–	5.5	V
I_{27}	input current	V_{27} = 0.4 V	–10	–	–	µA
I_{28}		V_{28} = 0.4 V	–10	–	–	µA
I_{27}	input current	V_{27} = 0.9 V	–	–	10	µA
I_{28}		V_{28} = 0.9 V	–	–	10	µA
V_{27}	LOW level output voltage		–	–	0.4	V
I_{27}	output current	V_{27} = 0.4 V	3.0	–	–	mA

Notes to the characteristics

1. RGB signals controlled by saturation, adaptive black, contrast and brightness, gamma affects the Y component of the internal RGB signals.
2. Matrix coefficients should be tested by comparing RGB output signals with a reference RGB colour bar, which is fed in at $(RGB)_1$ or $(RGB)_2$ inputs. In case of NMEN = 1 (NTSC) at minimum saturation the Y output and RGB output signals are not identical to the Y input signal. PAL/SECAM signals are matrixed by the equation:
   $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –2 degrees):
   $V_{R-Y}^* = 1.39V_{R-Y} - 0.07V_{B-Y}$; $V_{G-Y}^* = -0.46V_{R-Y} - 0.15V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the demodulator. V_{R-Y}^*, V_{G-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals.
3. Adaptive black control acts on Y signal, which is either Y input or Y output from RGB matrix. Negative set-up is not affected. The level shift value is determined by the peak dark detector, operation selected by control bit ADBL. The peak dark detector is inactive during blanking. Peak dark detector activated by internal line counter, which starts after the end of the vertical blank of the sandcastle. Active from line 16 (after end of vertical sandcastle) to line 224 (NTSC mode, NMEN = 1) or line 272 (PAL mode, NMEN = 0). It is recommended to increase the contrast value (subaddress 02) by 15% if ADBL = 1. The line numbers are doubled if control bit HDTV = 1.
4. Sandcastle pulse detector (pin 14)
   The sandcastle pulse is compared with 3 (control bit SC5 = 0) or 2 (SC5 = 1) internal threshold levels to separate the various pulses; the internal pulses are generated while the input pulse is higher than the thresholds. The thresholds are independent of supply voltage and temperature.
5. Y output can be switched to hue adjust output via I^2C-bus control bit YEXH. Output without sync pulse. Recommendation: Hue adjust DAC set to $3F_{HEX}$. Black level adjustable via hue adjust DAC.
6. Output can be switched to Y output via I^2C-bus control bit YEXH (via I^2C-bus, resolution 6 bit, bus subaddress 03).
7. At minimum gamma ($3F_{HEX}$) any differences in black level steps are amplified by 6 dB.
8. Series resistor in supply voltage should be less than 0.3 Ω.
9. At 1.0 V cut-off measurement level the function of the cut-off control loop is not guaranteed because the blanking level is limited to the minimum output voltage. For proper working a guide number for the minimum cut-off measurement level is 1.3 V.

APPENDIX Demodulation axes.





I²C-BUS RECEIVER (pins 27 and 28)

S: start condition
P: stop condition
W: write
A: acknowledge

slave address:

A6	A5	A4	A3	A2	A1	A0	$\overline{W}$
1	0	0	0	1	0	0	0

receiver (write mode)
slave receiver format is (BREN = 0)

S	SLAVE ADDRESS A	SUBADDRESS A	DATA BYTE A ... DATA BYTE A n data bytes with auto-increment of subaddresses	P

All subaddresses within the range 00 to 0F are automatically incremented. The subaddress counter wraps around from 0F to 00. Only in this case 0F will be acknowledged too.
Subaddresses outside the range 00 to 0E are not acknowledged by the device and neither auto-increment nor any other internal operation takes place.
All eight bits of the subaddress have to be decoded by the device.
If BREN = 1 (control register 1) auto-increment is not possible, the slave receiver format is:
S, SLAVE ADDRESS A, SUB ADDRESS A, DATA BYTE A, P

Table 1 Signal input selection and effect on adaptive black measurements by fast source switches and I²C-bus.

I²C-BUS CONTROLLED BITS				ANALOG SWITCH		SELECTED SIGNALS			
FSON2	FSDIS2	FSON1	FSDIS1	FSW2 (pin 1)	FSW1 (pin 13)	RGB_2 (pins 2, 3 and 4)	ADBL	RGB_1 (pins 10, 11 and 12)	TV (pins 6, 7 and 8)
L	L	L	L	L	L		active		ON
				L	H		active	ON	
				H	*	ON	off		
L	L	L	H	L	*		active		ON
				H	*	ON	off		
L	L	H	*	L	*		active	ON	
				H	*	ON	off		
L	H	L	L	*	L		active		ON
				*	H		active	ON	
L	H	L	H	*	*		active		ON
L	H	H	*	*	*		active	ON	
H	L	*	*	L	*	ON	active		
				H		ON	off		
H	H	*	*	*	*	ON	active		

Where:

H: logical HIGH or analog switch (pins 1 and 13) to > 0.9 V
L: logical LOW or analog switch (pins 1 and 13) to < 0.4 V
*: H or L, no influence
ON: is the selected signal input

Table 2 Crosstalk.

FSW1	FSW2	CROSSTALK	at 4 MHz maximum value (dB)	at 8 MHz maximum value (dB)	at 13 MHz maximum value (dB)
L	L	$RGB_1 \rightarrow Y, CD$	–58	–55	–50
		$RGB_2 \rightarrow Y, CD$	–58	–55	–50
L	H	$Y, CD \rightarrow RGB_1$	–51	–50	–47
		$RGB_2 \rightarrow RGB_1$	–58	–55	–50
L	H	$Y, CD \rightarrow RGB_2$	–51	–50	–47
		$RGB_1 \rightarrow RGB_2$	–58	–55	–50
H	H	$Y, CD \rightarrow RGB_2$	–51	–50	–47
		$RGB_1 \rightarrow RGB_2$	–58	–55	–50

Table 3 Subaddress byte and data byte format.

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
brightness	00	0	0	A05	A04	A03	A02	A01	A00
saturation	01	0	0	A15	A14	A13	A12	A11	A10
contrast	02	0	0	A25	A24	A23	A22	A21	A20
hue	03	0	0	A35	A34	A33	A32	A31	A30
red gain	04	0	0	A45	A44	A43	A42	A41	A40
green gain	05	0	0	A55	A54	A53	A52	A51	A50
blue gain	06	0	0	A65	A64	A63	A62	A61	A60
red level reference	07	0	0	A75	A74	A73	A72	A71	A70
green level reference	08	0	0	A85	A84	A83	A82	A81	A80
blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
gamma	0B	0	0	AB5	AB4	AB3	AB2	AB1	AB0
control register 1	0C	SC5	DELOF	BREN	X	NMEN	X	X	X
control register 2	0D	X	HDTV	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
control register 3	0E	ADBL	YHI	MOD2	BLST	YEXH	RELC	TCPL	0

The least significant bit of an analog control alignment register is defined as AX0 (D0).
After power on reset (PONRES) all alignment registers are set to 01.
X means don't care but for software compability with further video ICs with the same slave address, it is recommended to set all X to 0.

Table 4 RGB processor mode bits control register.

SYMBOL	PARAMETER	CONDITIONS
Control register 1		
SC5	sandcastle 5 V	0 = 3-level sandcastle pulse
		1 = 2-level sandcastle pulse
DELOF	delay of leading edge of clamping pulse switched off	0 = delay
		1 = no delay
BREN	buffer register enable	0 = new data are executed just after reception
		1 = data are hold in a latch (buffer register) and will be transferred to their destination register within the next vertical blanking interval; the device does not acknowledge any new data transfer until the internal transfer to the destination register has been completed
NMEN	NTSC - matrix enable	0 = PAL matrix
		1 = NTSC matrix
Control register 2		
HDTV	HDTV / progressive scan for ADBL line counter	0 = 272 (PAL), 224 (NTSC) lines
		1 = 544 (PAL), 448 (NTSC) lines
FSBL	full screen black level, e.g. for optical measurement	0 = normal mode
		1 = cut-off measurement level during full field brightness, inactive
BCOF	internal black level control off	0 = automatic cut-off control active
		1 = RGB outputs clamped to fixed DC levels
FSON2	fast switch 2 on	see Table 1
FSDIS1	fast switch 1 disable	
FSDIS2	fast switch 2 disable	
FSON1	fast switch 1 on	
Control register 3		
ADBL	adaptive black	0 = off
		1 = on
YHI	Y high level	0 = input = 0.315 V(p-p) (black-white)
		1 = input = 1.0 V(p-p) (black-white)
MOD2	modus 2	0 = inactive (BCOF = 0) AND (MOD2 = 1) is senseless; no output stabilization
		1 = output clamp without brightness adjust, brightness remains active e.g. for blue stretch
BLST	blue stretch	0 = off
		1 = on
YEXH	Y exclusive hue	0 = pin 26 is switched to hue adjust output
		1 = pin 26 is switched to Y output
RELC	relative to cut-off	0 = peak drive limit to absolute output
		1 = peak drive limit relative to cut-off
TCPL	time constant peak drive limiter	0 = 2 f_H
		1 = 1 f_H

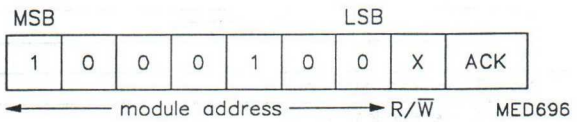


Fig.4 The module address byte.

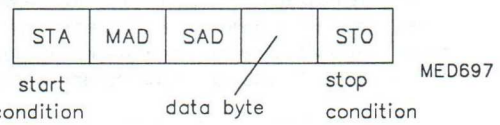


Fig.5 Data transmission without auto-increment (BREN = 0 or 1).

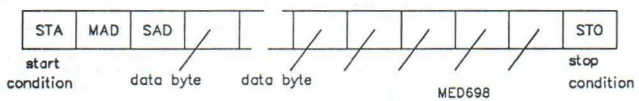


Fig.6 Data transmission with auto-increment (BREN = 0).

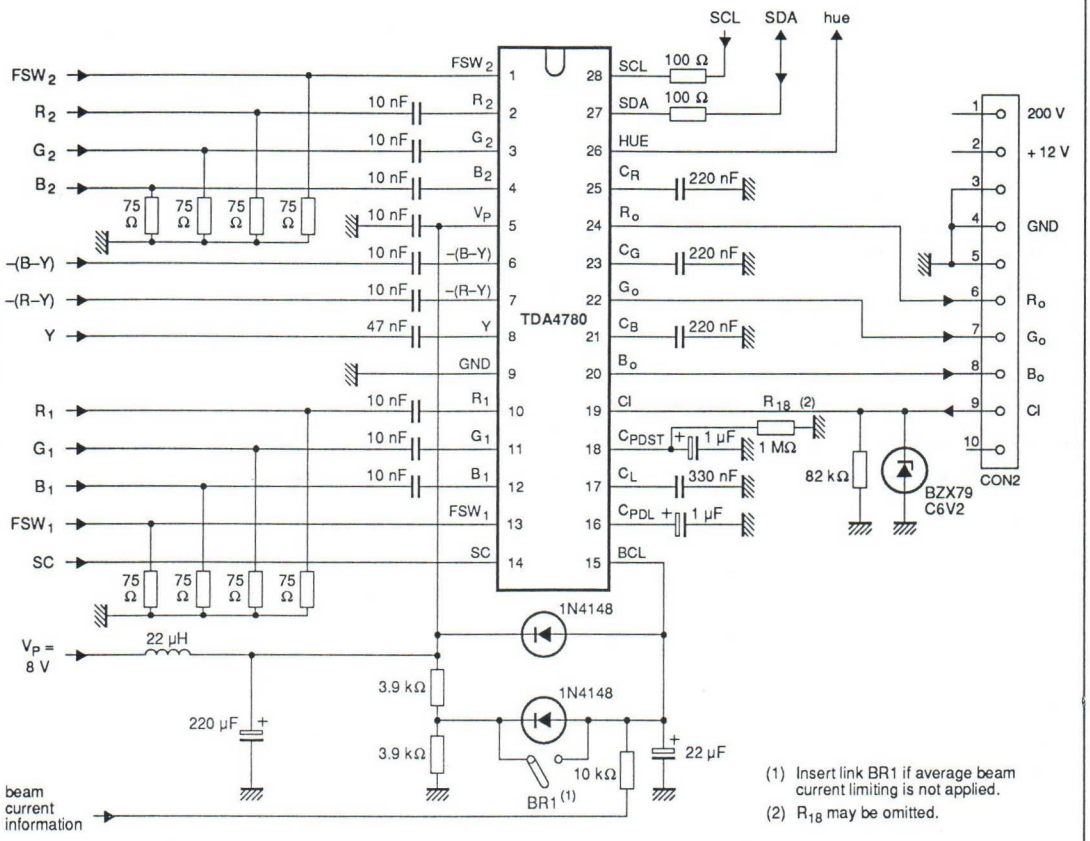


Fig.7 Test and application circuit.

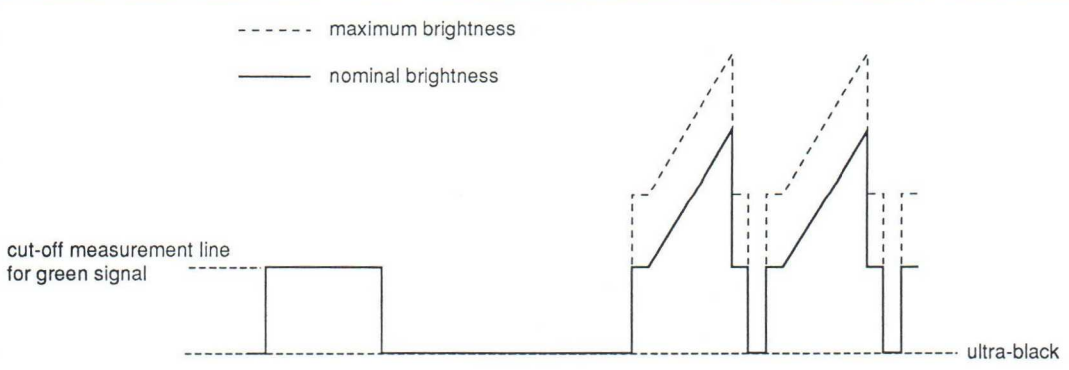


Fig.8 Cut-off measurement pulses.

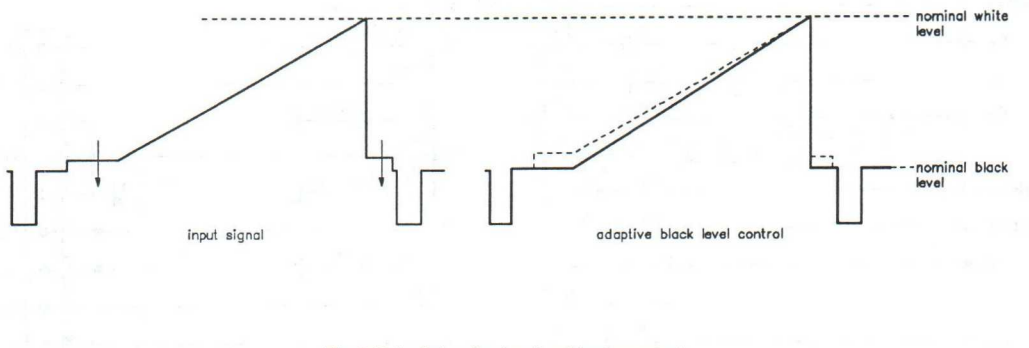


Fig.9 Principle of adaptive black control.

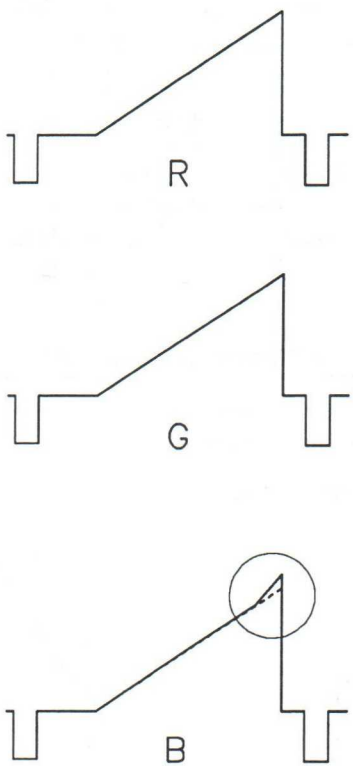


Fig.10 Principle of blue stretch.

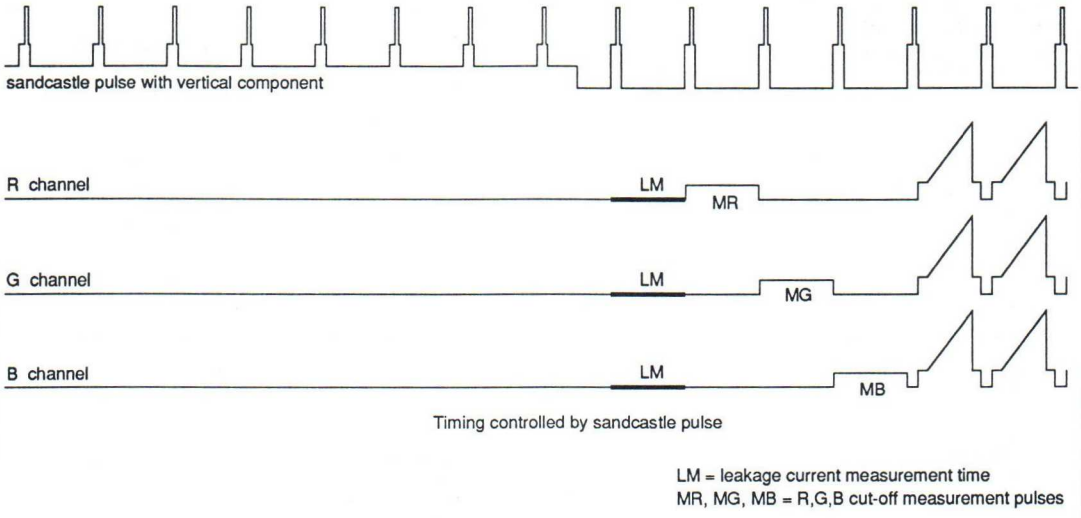
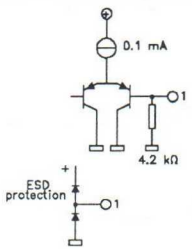
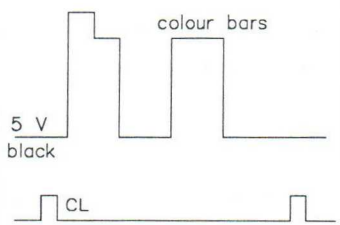
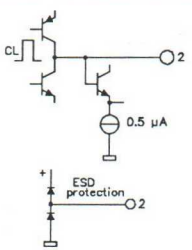
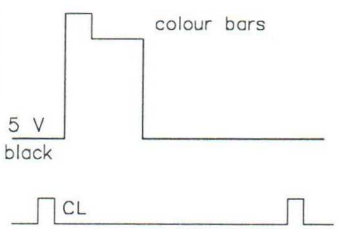
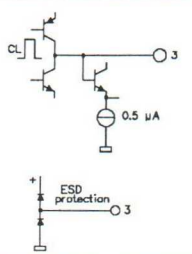
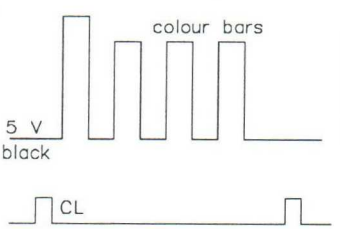
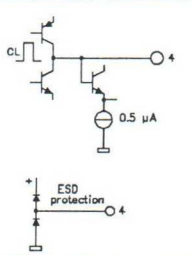
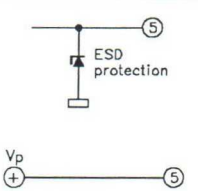
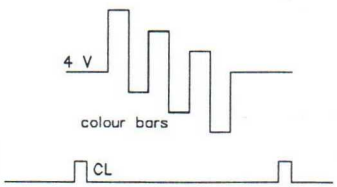
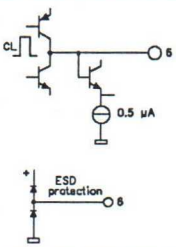
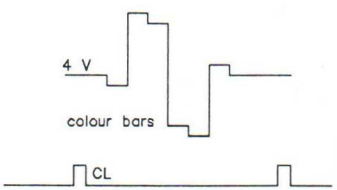
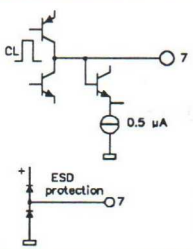
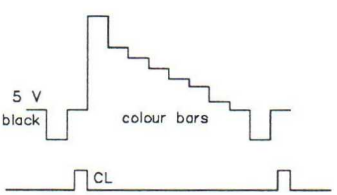
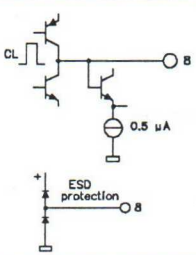
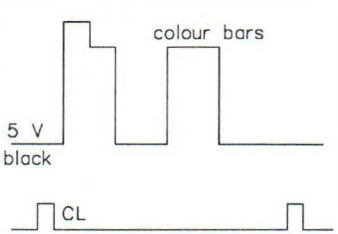
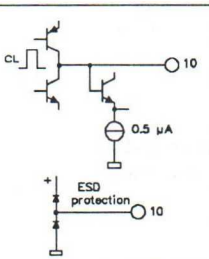
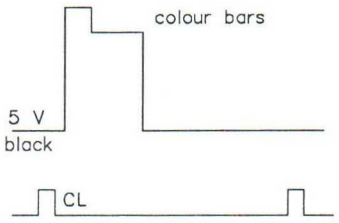
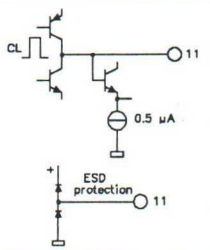
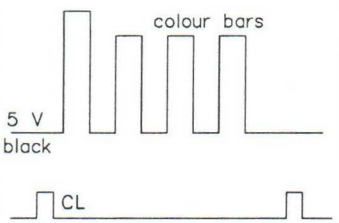
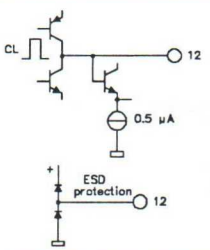
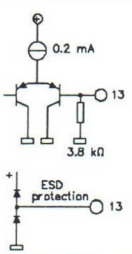
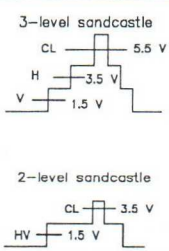
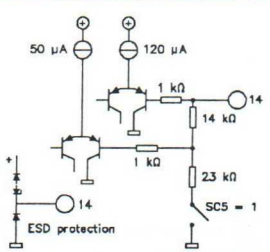
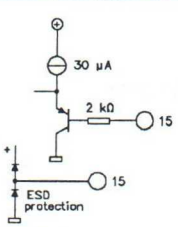


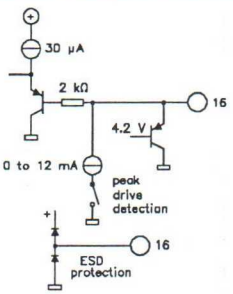
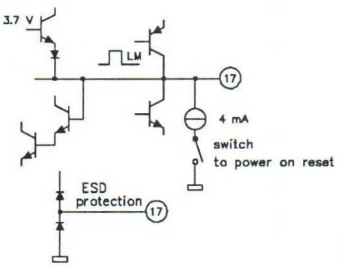
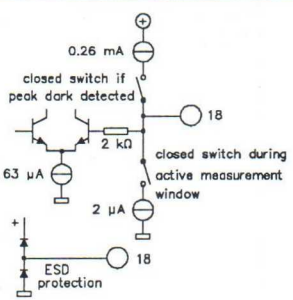
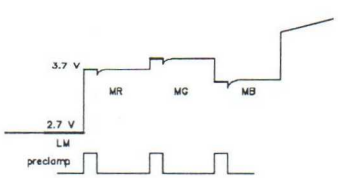
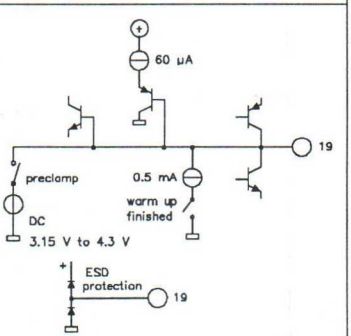
Fig.11 Leakage and cut-off current measurement timing diagram.

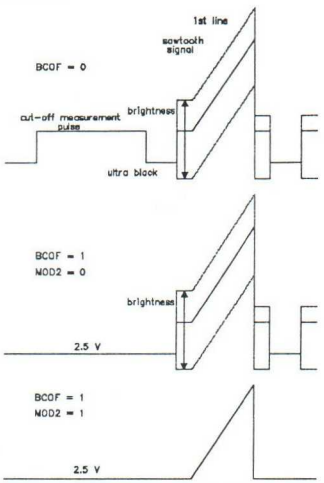
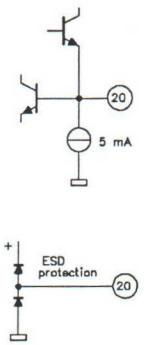
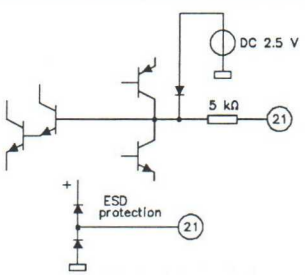
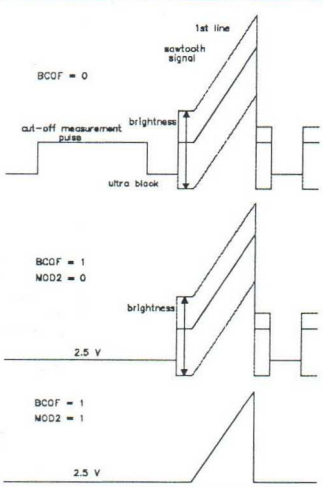
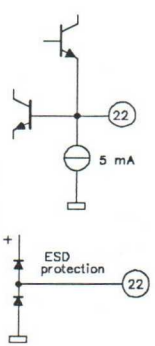
Table 5 Internal circuitry (Abbreviations: OB: open base and CL: clamp pulse).

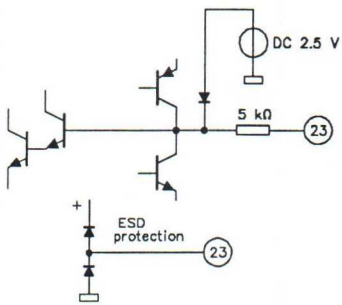
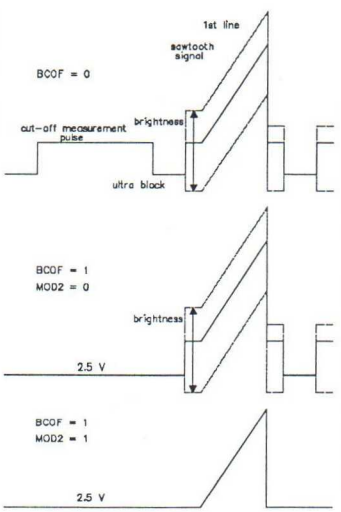
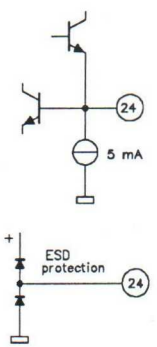
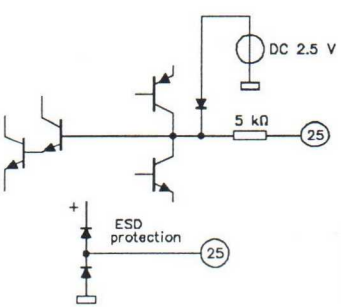
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
1	fast switch 2			
2	R_2 input clamp		100 µA / OB	
3	G_2 input clamp		100 µA / OB	
4	B_2 input clamp		100 µA / OB	
5	supply voltage			

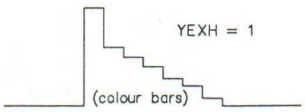
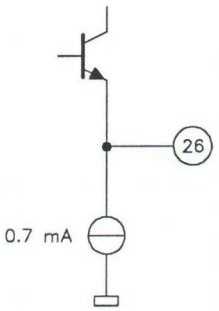
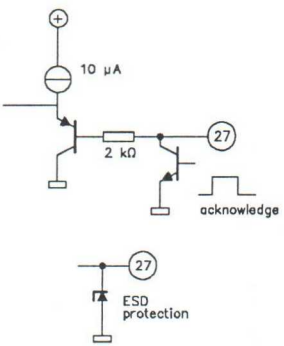
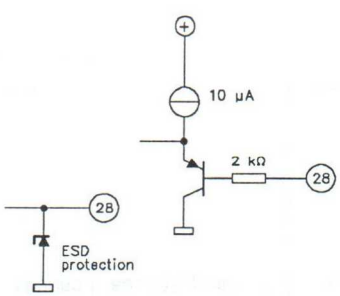
PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
6	–(B–Y) input clamp		100 µA / OB	
7	–(R–Y) input clamp		100 µA / OB	
8	Y input clamp		100 µA / OB	
9	ground			 no ESD protection circuit for ground pin
10	R_1 input clamp		100 µA / OB	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
11	G_1 input clamp		100 µA / OB	
12	B_1 input clamp		100 µA / OB	
13	fast switch 1			
14	sandcastle input		37 kΩ (SC5 = 0) OB (SC5 = 1)	
15	average beam current limiting input		OB	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
16	storage capacitor for peak limiting input	outside peak drive during peak drive (RELC = 1) during peak drive (RELC = 0)	OB 0 to 12 mA 5 mA	
17	storage capacitor for leakage current	outside leakage current measurement during leakage current measurement automatic switch to power on reset	OB –400 µA to +400 µA 4 mA	
18	peak dark storage		OB / 0.26 mA	
19	cut-off measurement input (beam current information input)		–180 µA to +180 µA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
20	blue output		5 mA 5 mA 5 mA	
21	blue cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	
22	green output		5 mA 5 mA 5 mA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
23	green cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	
24	red output		5 mA 5 mA 5 mA	
25	red cut-off storage capacitor	during cut-off control or during output clamping	OB –300 µA to +300 µA	

PIN NO.	PIN NAME (DESCRIPTION)	WAVE FORM	Z	INTERNAL CIRCUIT
26	Y output		0.7 mA	
	hue adjust output	YEXH = 0 DC 0.8 V to 5.0 V	0.7 mA	
27	I^2C-bus data input	outside acknowledge	OB	
	acknowledge output	during acknowledge	less than 0.1 V up to 4 mA due to external pull-up resistor	
28	I^2C-bus serial clock input		OB	

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	February 1992

TDA4800
Vertical deflection circuit for monitor applications

FEATURES

- Fully integrated, few external components
- RC oscillator with wide sync range of 1:3 (e.g. 50 Hz to 150 Hz)
- Synchronization by positive or negative going sync pulse
- Blanking pulse duration is determined externally
- Dual frequency criterion for automatic amplitude switch-over (e.g. 50 Hz to 60 Hz)
- Guard circuit for screen protection
- Sawtooth generator with buffer stage supplied by external voltage
- Preamplifier
- Power output stage with thermal and SOAR protection
- Flyback generator
- Internal voltage stabilizer

GENERAL DESCRIPTION

The TDA4800 is a monolithic integrated circuit for vertical deflection primarily in monitors (and TV receivers). The complete circuit consists of 11 main functional blocks as shown in Fig.1.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_P	supply current (pins 6 and 10)	note 1	–	215	–	mA
I_7	output current (peak-to-peak value)		–	–	2.6	A
f_{sync}	picture frequency	note 1, 3	–	–	135	Hz
V_3	positive sync input pulse		1.0	–	6.0	V
V_3	negative sync input pulse		–0.5	–	–0.7	V
T_{amb}	operating ambient temperature range	note 2	–20	–	+ 70	°C

Notes to the quick reference data

1. Measured in circuit Fig.4
2. $P_{tot} = 3.6$ W for $R_{th\ j\text{-}a} = 20$ K/W
3. $f_o = 45$ Hz ($f_{sync\ max} = 3f_o$)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4800	13	DBS	plastic	SOT141

Vertical deflection circuit for monitor applications

TDA4800

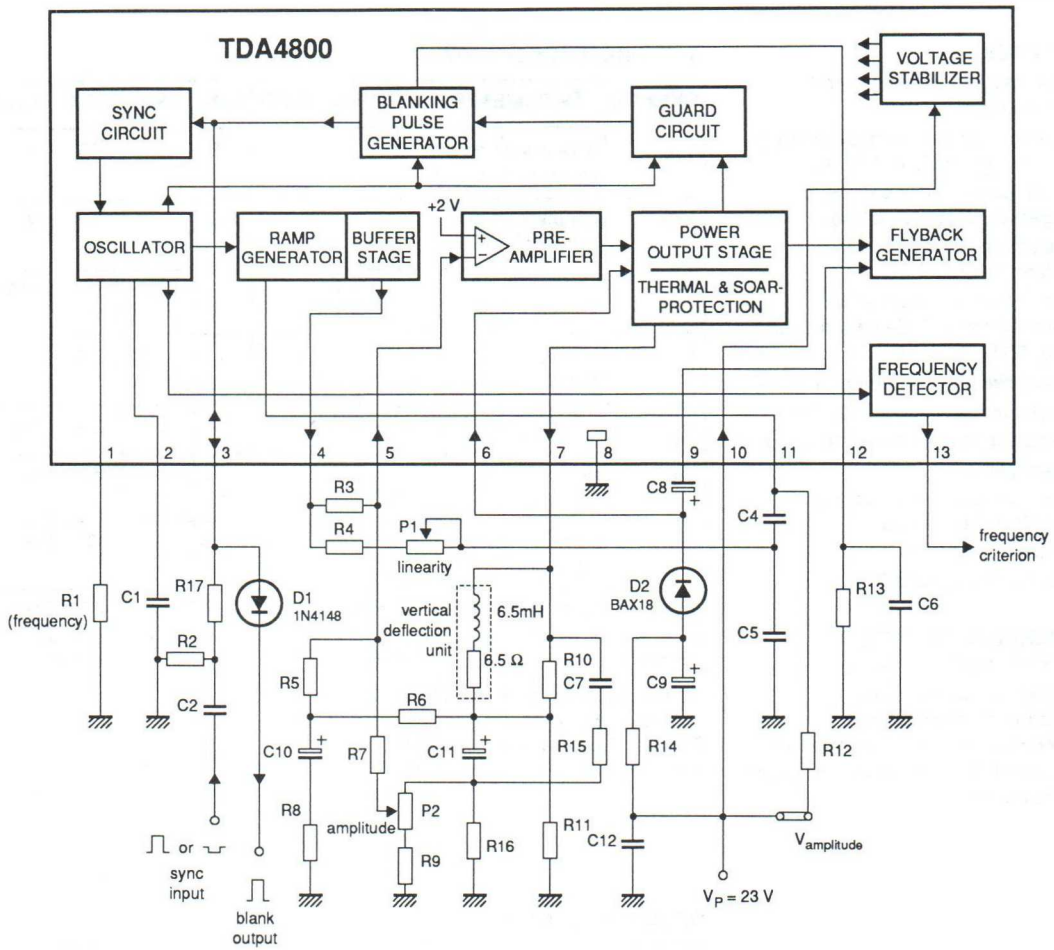


Fig.1 Block diagram.

Vertical deflection circuit for monitor applications

TDA4800

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. Oscillator
2. Synchronization circuit
3. Blanking pulse generator
4. Frequency detector and storage
5. Ramp generator
6. Buffer stage
7. Preamplifier
8. Power output stage
9. Flyback generator
10. Guard circuit
11. Voltage stabilizer

1. Oscillator (pins 1, 2)

The oscillator is an RC-oscillator with a threshold value switch, which ensures very good frequency stability.

The upper and lower threshold voltages are defined by an internal voltage divider.

An external capacitor C1 at pin 2 is charged by a constant current source. When the scan voltage of C1 reaches the upper threshold voltage, oscillator flyback starts. Capacitor C1 discharges via an internal resistor and transistor until the lower threshold is reached.

The constant charge current and free-running frequency f_o are adjusted by an external resistor R1 at pin 1:

$$f_o = \frac{1}{K \times R1 \times C1} \quad \text{with } K = 0.68$$

2. Synchronization circuit (pin 3)

A positive- or negative-going pulse fed to pin 3 synchronizes the oscillator by lowering the upper threshold voltage. The synchronizing range is f_o to 3 f_o. For example:

$f_o = 50$ Hz $\longrightarrow$ $f_{sync\ max} = 150$ Hz.

3. Blanking pulse generator (pin 3)

Also at pin 3 a blanking pulse is available. Diode D1 separates the synchronization pulse from the blanking pulse. During scanning, the external capacitor C6 at pin 12 is charged to an internal stabilized voltage V. The blanking pulse starts with the beginning of oscillator flyback; then capacitor C6 discharges via the external resistor R13 at pin 12. The blanking pulse stops when the capacitor voltage is V/2.

The blanking pulse duration is determined by the values of external components R13 and C6 at pin 12:

$$t_{bl} = R13 \times C6 \times Ln2$$

4. Frequency detector with storage (pin 13)

At the end of the scanning period a frequency detector detects the oscillator frequency (see *Note*). When this frequency is above the threshold a flip-flop is set to store this information. The output is an open collector output.

Note:

Frequency detector change-over at pin 13 from low (= low frequency) to high (= high frequency) is determined by f_o:

$$f_{threshold} = 1.23 \times f_o$$

5. Ramp generator (pin 11)

The ramp generator consists of two external series capacitors C4 and C5, external charge resistor R12 (connected to pin 11), and an internal differential amplifier which is synchronously-switched by the oscillator.

External capacitors C4 and C5 at pin 11 are charged by the charging current via the external charge resistor R12 until oscillator flyback starts. C4 and C5 are then discharged via pin 11 by an internal resistor and transistor. This generates a positive-going ramp voltage.

6. Buffer stage (pin 4)

The buffer stage consists of two emitter followers. The ramp voltage is fed via the buffer stage and is available at pin 4 with a low ohmic output impedance. With R4 and P1 it generates a ramp function, which, together with the feedback network of the deflection yoke, gives a high degree of linearity at the picture tube. The linearity can be adjusted by P1.

7. Preamplifier (pin 5)

The preamplifier is a differential amplifier. The non-inverting input is fixed at about 2 V by an internal voltage divider. The inverting input at pin 5 is connected to the ramp voltage via R3 and feedback network P2, R5 - R11, R15, R16, C7, C10 and C11.

8. Power output stage (pin 7)

The power output stage is an amplifier with a quasi-complementary class-B output. The output is connected to pin 7.

The power stage includes SOAR and thermal protection.

9. Flyback generator (pin 9)

The flyback generator has an external capacitor C8 at pin 9. During scanning, the internal circuit switches pin 9 almost to ground; thereby C8 is charged by the supply voltage via external components R14 and D2.

During the flyback time pin 9 is switched almost to the supply voltage, so that the supply voltage for the power output stage (pin 6) is nearly doubled. This high flyback voltage ensures a very short flyback time.

10. Guard circuit (pin 3)

When the vertical deflection current is absent (e.g. short-circuit, or open-circuit of the yoke) the guard circuit changes the blanking pulse at pin 3 into a DC signal which blanks the beam current to protect the screen.

Also an oscillator defect (C1 short-circuited or R1 disconnected from pin 1) switches on the guard circuit.

11. Voltage stabilizer

The voltage stabilizer circuit provides a stable operating voltage of about 7.5 V for several circuits of the TDA4800.

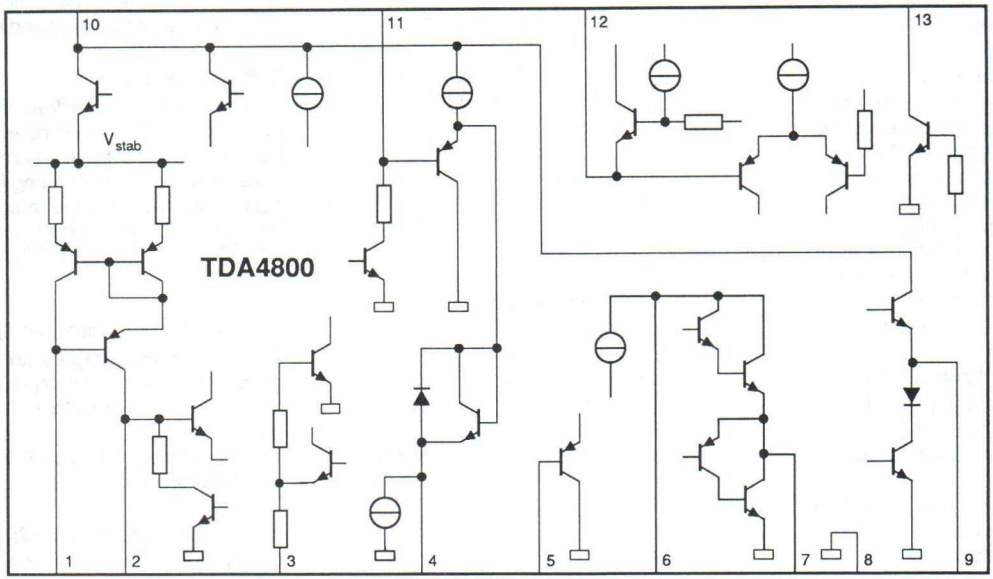


Fig.2 Internal circuits.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC_R	1	oscillator resistor
OSC_C	2	oscillator capacitor
SYB_O	3	sync. input, blanking pulse output
S_{OUT}	4	sawtooth output
PRE_I	5	preamplifier input
P_{SUP}	6	power supply
OUTP	7	deflection output
GND	8	ground
C_{FLY}	9	pin for the flyback generator capacitor
V_P	10	supply voltage
S_{GEN}	11	sawtooth generator
BP_{DU}	12	blanking pulse duration
FRQ_C	13	frequency criterion

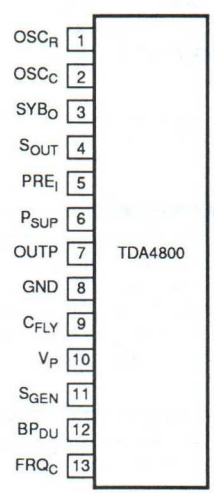


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_2	voltages		0	6	V
V_{11}			0	24	V
V_{12}			0	6	V
V_{13}			0	50	V
V_{10}	supply voltages (V_P)		0	50	V
V_9			0	50	V
V_7			0	60	V
V_6			0	60	V
V_5			0	6	V
V_4			0	24	V
V_3			−0.7	6	V
I_1	currents		0	−1	mA
I_3			+3	−10	mA
I_4			0	−5	mA
I_6, I_7, I_8		see note 1			
I_9			−1.5	+1.5	A
I_{11}			−0.1	+30	mA
T_{stg}	storage temperature range		−25	+150	°C
T_{amb}	operating ambient temperature range	see note 2	−20	+70	°C
$T_{j\ max}$	maximum junction temperature	see note 3	−	150	°C
P_{tot}	total power dissipation	see note 2	−	−	W
V_{ESD}	ESD sensitivity	see note 4	−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	20 K/W
$R_{th\ j\text{-}mb}$	from junction to mounting base	5 K/W

Notes to the limiting values

1. I_6, I_7 and I_8 are limited by SOAR protection circuit that ensures that a short-circuit between the output pin 7 and supply voltage or ground does not destroy the output stage. A short-circuit may be soldered into the printed-circuit board or may sometimes (non-periodically) occur in the applied circuit.
2. The maximum value for the operating ambient temperature range and the power dissipation depends on the heatsink.
3. Internally limited by thermal protection: switching temperature point at T_j = 150 °C ± 8 °C.
4. Human body model: 1.5 kΩ, 100 pF, 5 pulses.

CHARACTERISTICS

All voltages are measured to V_{GND} (pin 8); T_{amb} = 25 °C; V_P = 23 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_{10}	supply current	V_{10} = 25 V; V_5 = 3 V without load	–	12	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 1 V without load	–	20	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 3 V without load	–	5	–	mA
V_7	minimum output voltage	I_7 = 1 A	–	1.4	1.65	V
V_7	maximum output voltage	I_7 = –1 A	V_6 –2.3	V_6 –2.0	–	V
V_9	output voltage during flyback	I_9 = –1 A	–	V_{10} –2.2	–	V
I_7	output current		–	–	± 1.3	A
I_9	output current		–	–	± 1.3	A
I_5	preamplifier input current		–	–0.1	–	µA
V_1	stabilized voltage		6.1	6.8	7.3	V
V_3	blanking pulse output voltage		–	5.7	–	V
R_3	blanking pulse output resistance		–	300	–	Ω
I_3	blanking pulse output current		0	–	–3	mA
t_{bl}	blanking pulse duration	R = 100 kΩ; C = 10 nF (pin 12)	640	680	730	µs
V_{11}	output voltage ramp generator		0.3	–	20	V
I_{11}	output current ramp generator		–2	–	15×10^3	µA
V_{13}	output voltage frequency detector	lower frequency I_{13} = 1mA	–	–	1.0	V
I_{13}	leakage current frequency detector	higher frequency V_{13} = 50 V	–	–	1.0	µA
V_4	output voltage buffer stage		0	–	20	V
I_4	output current buffer stage		–	–	–4.0	mA
V_3	synchronizing input voltage	positive sync	1.0	–	6.0	V
V_3	synchronizing input voltage	negative sync	–0.5	–	–0.7	V
	tolerance of free running oscillator	without sync	–3.0	–	+ 3.0	%
$\Delta f/f / \Delta T_C$	oscillator temperature dependency	T_{case} = 20 °C to 100 °C	–	10^{-4}	–	K^{-1}
$\Delta f/f / \Delta V_P$	oscillator voltage dependency	V_P = 10 V to 30 V	–	4×10^{-4}	–	K^{-1}
f_0 / f_{sync}	synchronizing ratio		1:2.9	1:3	–	–

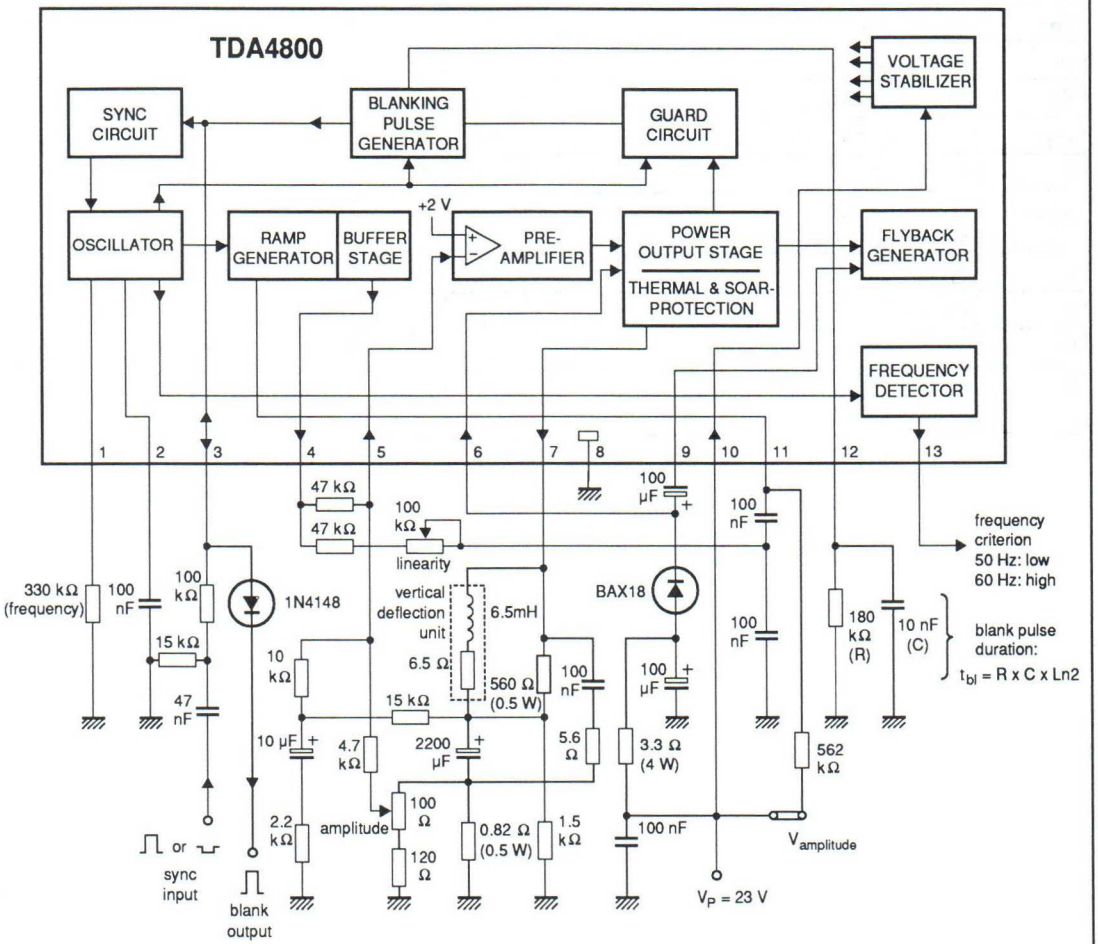


Fig.4 Test and application circuit.

TDA4800 IN THE TEST AND APPLICATION CIRCUIT (see Fig.4)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
V_P	supply voltage		23	V
I_P	supply current		215	mA
V_7	DC output voltage		11.8	V
V_{7M}	peak output voltage		45	V
I_7	output current		0.8	A
$I_{Y(p-p)}$	vertical deflection current (peak to peak)		1.5	A
t_{fb}	flyback time		0.3	ms
t_{bl}	blanking pulse duration		1.25	ms
P_{tot}	total power dissipation		3.3	W
f_o	free running oscillator frequency	without sync	45	Hz

Data sheet	
status	Preliminary specification
date of issue	May 1991

TDA4810

Sync processor and horizontal driver for monitors

FEATURES

- Sync separator with AC-coupled and DC-coupled inputs for signals of nearly all existing sync sources (e.g. TTL / video)
- Amplitude dependent sync slicing
- Automatic sync polarity correction
- Wide horizontal frequency range
- Artificial sync generator for sync pulse-width-independent operation
- Short vertical integration time
- Vertical/composite sync output signal selectable
- Super sandcastle pulse generator
- Two phase loops (PLL1, PLL2) to achieve excellent sync-locking and horizontal picture shift
- Horizontal output stage optimized for bipolar and Darlington deflection transistors
- Protection circuits against too low supply voltage and excessive EHT (X-ray protection)
- Voltage stabilizer with excellent ripple rejection
- Number of external components depend on the requirements and realized features

GENERAL DESCRIPTION

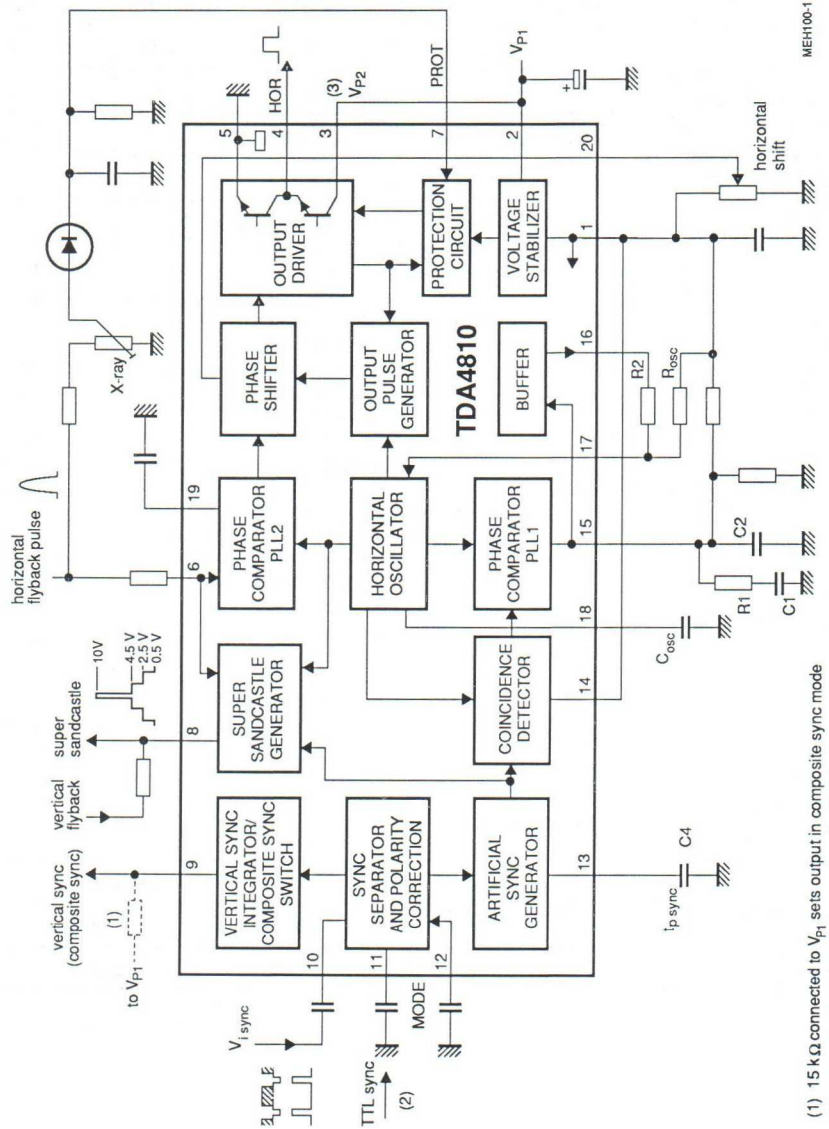
Monolithic integrated circuit for sync processing in monochrome and colour monitors, applicable for all commonly used graphic cards (e.g. EGA, Super VGA and IBM8514/A). The flexible sync separator handles different sync signals of either polarity over a wide amplitude range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	8.5	12	16	V
V_{P2}	supply voltage (pin 3)	8.5	12	16	V
V_{stab}	stabilized output voltage (pin 1)	6.18	6.3	6.5	V
I_{P1}	supply current (pin 2)	-	35	-	mA
$V_{i\ sync}$	mode 1: AC-coupled negative-going input signal on pin 10 (peak-to-peak value)	-	1	1.5	V
	mode 2: AC-coupled positive- or negative-going sync pulse on pin 10 (peak-to-peak value)	2	-	5.5	V
	mode 3: DC-coupled positive- or negative-going sync pulse on pin 11 (peak value)	3.2	-	5.5	V
V_9	vertical/composite sync output voltage HIGH ($I_9 = -1$ mA)	-	10	-	V
I_4	maximum horizontal output current for Darlington deflection transistor ($-I_4 = I_3$)	-	-	−900	mA
	maximum horizontal output sink current for bipolar deflection transistor	-	-	100	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4810	20	DIL	plastic	SOT146



(1) 15 kΩ connected to V_{P1} sets output in composite sync mode
(2) connection for other modes as described in Fig.3
(3) connection for Darlington deflection transistor as described in Fig.4

Fig.1 Block diagram for full facility (mode 2); horizontal output signal suitable for bipolar deflection transistor .

Sync processor and horizontal driver for monitors

TDA4810

PINNING

SYMBOL	PIN	DESCRIPTION
V_{stab}	1	stabilizer voltage output (6.3 V)
V_{P1}	2	supply voltage
V_{P2}	3	supply voltage for horizontal output
HOR	4	horizontal pulse output
GND	5	ground (0 V)
FLB	6	horizontal flyback pulse input
PROT	7	protection input (for over-current /EHT protection)
SSC	8	super sandcastle generator output
VS	9	vertical sync / composite sync output
$V_{i\ sync}$	10	sync input signal , AC-coupled
TTL	11	alternative sync input DC-coupled, e.g. TTL
APC	12	automatic sync polarity correction
C_{SY}	13	capacitor of artificial sync generator
COIN	14	coincidence detector
PLL1	15	time constant of PLL1
BUF	16	buffered PLL1 output
R_{osc}	17	reference current of horizontal oscillator
C_{osc}	18	capacitor of horizontal oscillator
PLL2	19	time constant of PLL2
SHIFT	20	horizontal phase shift

PIN CONFIGURATION

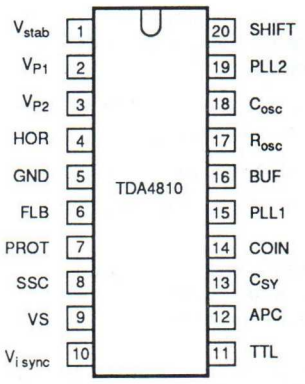


Fig.2 Pin configuration.

Sync processor and horizontal driver for monitors

TDA4810

FUNCTIONAL DESCRIPTION

Sync separator and polarity correction (Fig.1)

The circuit handles sync signals of nearly all existing standards . Features of the sync separator:

- inputs for DC-coupled signal or AC-coupled signal
- automatic sync polarity correction
- amplitude dependent sync slicer

The type of coupling and the necessary external components are shown in Figure 3.

Mode 1: A negative going sync signal (V_i sync < 1.5 V (p-p)) is fed via a coupling capacitor to pin 10. The sync separator clamps the bottom of the input signal on 1.28 V. Sync is sliced 120 mV above. Since the automatic polarity correction does not work below 2 V (p-p), pins 11 and 12 are connected to ground.

Mode 2: Positive or negative going sync pulses >2 V(p-p) (e.g. TTL) are AC-coupled to pin 10. The upper level is peak-rectified referred to the external capacitor on pin 11 at $V_{11} = 1.28V + 0.5 \times V_{i\ sync}$. This means, the slicing level tracks with typical 50% of $V_{i\ sync}$. The polarity switch corrects the polarity automatically by means of the external capacitor on pin 12. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Then pin 12 can be connected to ground or V_{stab} (pin 1) to force the polarity.

Mode 3: Positive or negative going sync signals >3.2 V(p) (e.g. TTL) are DC-coupled to pin 11. They are sliced at 1.4 V according to TTL standard. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Pin 12 can be connected to ground or V_{stab} (pin 1) to select the polarity from external.

Vertical/composite sync output

If a video signal or composite sync signal is applied to pin 10 the vertical sync separator generates a vertical sync trigger pulse. The separated vertical and composite sync pulses are fed to the vertical or composite sync switch and to the output stage (pin 9).
The external load current at pin 9 determines which of the two signals is fed out of pin 9. If there is an additional current from V_{P1} via the 15 kΩ resistor, composite sync signal is achieved (without additional current the vertical sync pulse is output.

Artificial sync generator

The sync signal from the sync separator is directly fed to the phase comparator (with unchanged leading and trailing edges), if the internal monoflop at pin 13 is connected to ground. This operation is possible.

Sync signals with leading edge as only sync reference (because the trailing edge could occur at an undefined time) is achieved by connecting a time-determining capacitor from pin 13 to ground. The internal monoflop generates an artificial sync signal triggered by the leading edge of the incoming sync signal.
Furthermore, the artificial sync generator reduces disturbances of the PLL1 during vertical sync.

Coincidence detector

Coincidence is detected between the input sync pulse and the gating pulse of the oscillator. The centring current for PLL1 is switched off at coincidence (V_{14} > 3 V).

Phase comparator PLL1

This stage compares the PLL1 (timing reference of the oscillator) with the centre of the horizontal input sync pulse (respectively with the artificial sync pulse, Fig.6). The time difference is converted into a proportional current on pin 15 to tune the oscillator via the buffer amplifier. This ensures that the phase relationship in the TDA4810 is stable independent of changes in frequency.

Horizontal oscillator (Fig.6)

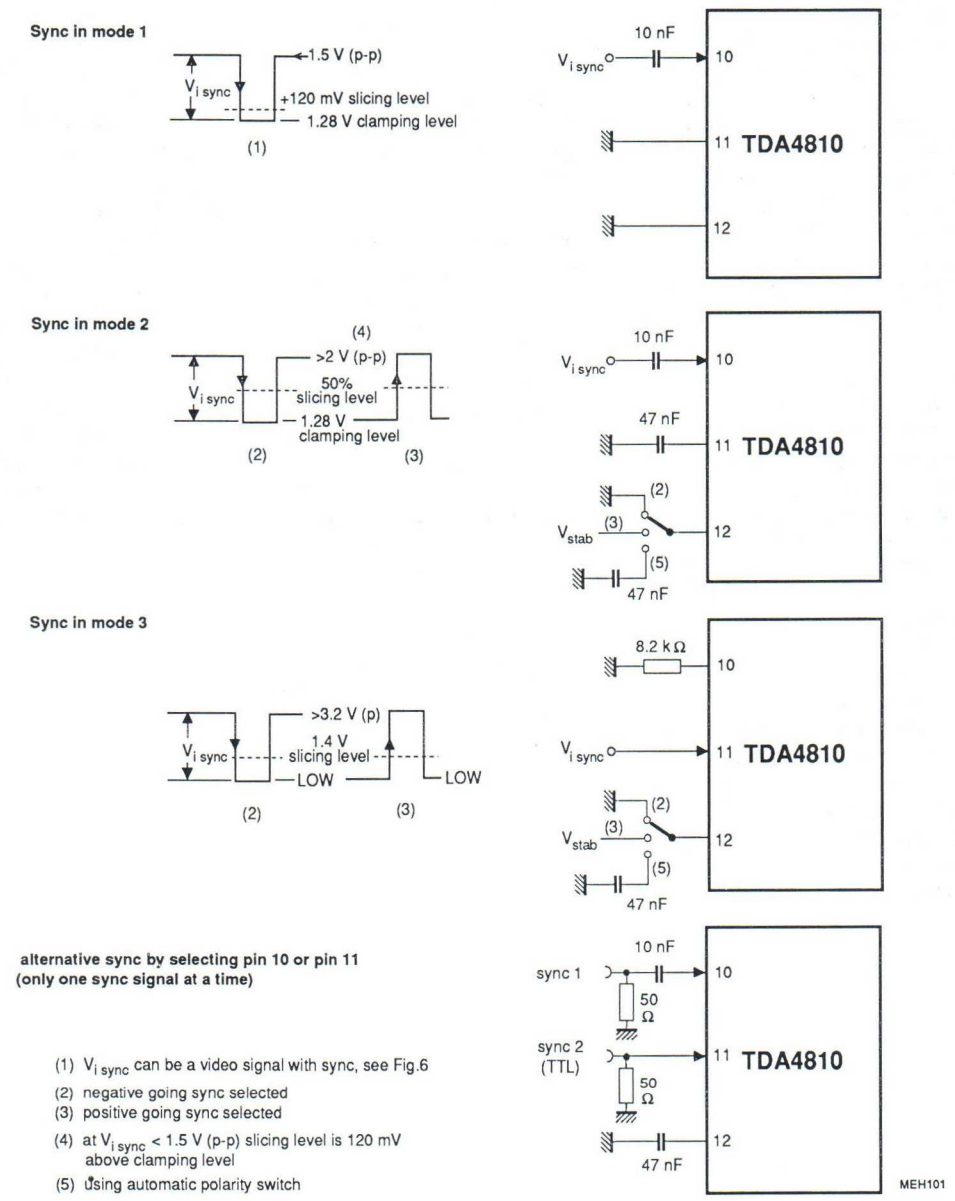
The frequency of the free-running oscillator is determined by the capacitor on pin 18 and the reference current via pin 17. The reference current is fed from the voltage stabilizer via R_{osc}, and also from the PLL1 buffer amplifier via R2 to define the catching range. In order to cover a wide frequency range (one octave) R_{osc} can be modified as described in notes to the characteristics.

Phase comparator PLL 2 (Fig.6)

This stage compares the centre of the positive-going flyback pulse (on pin 6, internal threshold voltage 3 V) with the PLL2 timing reference generated by the horizontal oscillator. A time difference is converted into a proportional current on pin 19. The line flyback pulse and the oscillator pulse are compared to eliminate the delay time in the horizontal deflection stage.

Horizontal phase shifter

An external stabilized voltage on pin 20 sets the phase relationship between sync pulse and horizontal flyback pulse. The horizontal output pulse can be adjusted over a wide range (±20% referred to the horizontal period time) by means of the external potentiometer (Fig.1).



(1) $V_{i\,sync}$ can be a video signal with sync, see Fig.6
(2) negative going sync selected
(3) positive going sync selected
(4) at $V_{i\,sync}$ < 1.5 V (p-p) slicing level is 120 mV above clamping level
(5) using automatic polarity switch

Fig.3 Sync modes of TDA4810.

Output pulse generator and horizontal output (Fig.4)

The output pulse generator generates a pulse of constant width within the control range of the PLL 2. The horizontal output driver generates two different pulse widths (Fig.6) depending on the voltage between pins 2 and 3

- 45% relative pulse width for standard bipolar deflection transistor ($V_3 = V_2$)
- 30% relative pulse width for Darlington deflection transistor. ($V_3 < V_2$)

NON-INVERTED POLARITY.

The push-pull output stage of the horizontal driver is connected between the supply voltage (pin 3) and ground (pin 5). The output signal (pin 4) is usually fed to a transformer-coupled driver. The upper transistor (collector on pin 3) is designed for a maximum current of 900 mA, the lower one for 100 mA.

INVERTED POLARITY

The horizontal output signal is now available on pin 3 by means of the 220 Ω pull-up resistor. Pin 4 is connected to ground. The open-collector output can directly drive a Darlington deflection transistor.

Voltage stabilizer

A stabilized voltage of 6.3 V, based on a bandgap reference, is provided on pin 1. This avoids phase jitter in deflection, caused by an insufficient filtered supply voltage. The excellent performance of the voltage stabilizer allows the TDA4810 to be driven directly by a switch mode power supply.

Super sandcastle pulse generator

Three levels are generated (Fig.6):

a) The 2.5 V level is generated by a external vertical blanking current which is fed into pin 8.

b) The 4.5 V level is derived from the line flyback pulse referred to a threshold of 0.3 V for horizontal blanking. When horizontal flyback pulses are absent, the 4.5 V level is inserted by the protection circuit to blank the screen continuously .

c) The 10 V level starts with the trailing edge of the sync pulse (respectively with artificial sync) and ends with a pulse, derived from the horizontal oscillator saw-tooth signal.

Protection circuit

The protection circuit is activated and the horizontal output is switched off when the voltage on pin 7 exceeds V_{stab} = 6.3 V or decreases below –0.2 V . One of these both thresholds can be used for X-ray protection or for over-current protection (Fig.1).

There is an additional protection against too low supply voltage (V_{P1}< 5.8 V).

Operations:

- output pin 4 goes to ground when $V_2 = V_3$ (e.g. in a bipolar deflection transistor application)
- output pin 3 goes to ground when $V_3 < V_2$ (e.g. in a Darlington deflection transistor application)
- the error indication is latched; therefore all the supply voltages must be switched off and on again, to enable the circuit.

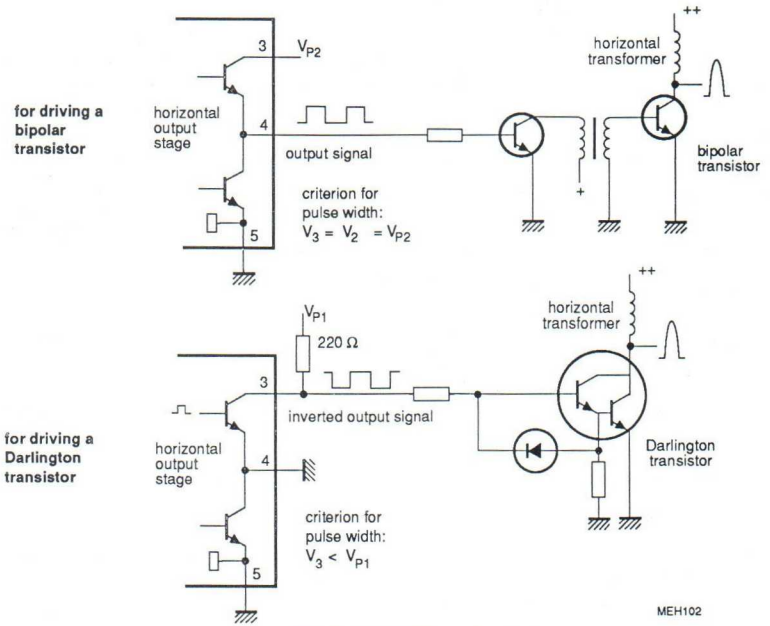


Fig.4 Horizontal output stage.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	0	16	V
V_{P2}	supply voltage (pin 3)	0	16	V
$V_{10, 11}$	input voltage	–0.5	8	V
I_3	supply current for horizontal output	-	1.0	A
I_4	horizontal output current	-	+200	mA
		-	–1.0	A
I_6	flyback input current	-	±10	mA
I_9	vertical sync output current	-	–10	mA
I_{16}	buffer output current	-	±10	mA
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 2)		8.5	12	16	V
V_{P2}	supply voltage range (pin 3)		8.5	12	16	V
I_{P1}	supply current		-	35	-	mA
V_{stab}	stabilized voltage (pin 1)		6.18	6.3	6.5	V
RR	ripple rejection for V_{stab}	f_R = 1 kHz (sinewave) on supply voltage	60	70	-	dB
Sync input signal modes 1 and 2, AC-coupled to pin 10						
$V_{i\ sync}$	negative-going sync input signal (peak-to-peak value, pin 10)	mode 1; Fig.3; R_S = 50 to 500 Ω	-	1	1.5	V
	sync amplitude in video signal		180	300	400	mV
	clamping voltage		-	1.28	-	V
	slicing level above clamping level	$t_{p\ sync}/t_H$ = 0.1	-	120	-	mV
	voltage for automatic polarity correction inactive	mode 1	-	-	1.5	V
	positive or negative-going sync input signal (peak-to-peak value, pin 10)	mode 2; Fig.3; R_S = 50 to 500 Ω	2	-	5.5	V
	voltage for automatic polarity correction active	mode 2	2	-	-	V
	slicing level	mode 2	25	50	75	%
I_{10p}	input current	during video signal	1	2	3.5	μA
R_{10}	input resistance	V_{10} < 1.28 V	-	50	-	Ω
		V_{10} > 1.28 V	-	high-ohmic	-	Ω
V_{11}	charging current (peak value)	mode 2	-	–6	-	mA
	discharging current	V_{11} > 1.4 V	-	10	-	μA
V_{12}	threshold voltage for automatic polarity correction	mode 2	2.6	3.0	3.4	V
	voltage to select positive-going sync		3.5	V_{stab}	-	V
	voltage to select negative-going sync		0	-	2.5	V
I_{12}	charging current at positive-going sync	mode 2	-	–50	-	μA
	discharging current at negative-going sync		-	50	-	μA
Sync input signal mode 3 DC-coupled to pin 11 (8.2 kΩ from pin 10 to ground)						
V_{11}	positive or negative-going sync input signal (peak value, pin 11)	mode 3; Fig.3	3.2	-	5.5	V
	slicing level of sync pulses		1.25	1.4	1.55	V
	voltage for automatic polarity switch active		3.2	-	-	V
V_{12}	input voltage to select polarity correction	positive-going sync	3.5	V_{stab}	-	V
		negative-going sync	0	-	2.5	V
$t_{p\ sync}$ / t_H	duty cycle for automatic correction in polarity		-	-	25	%

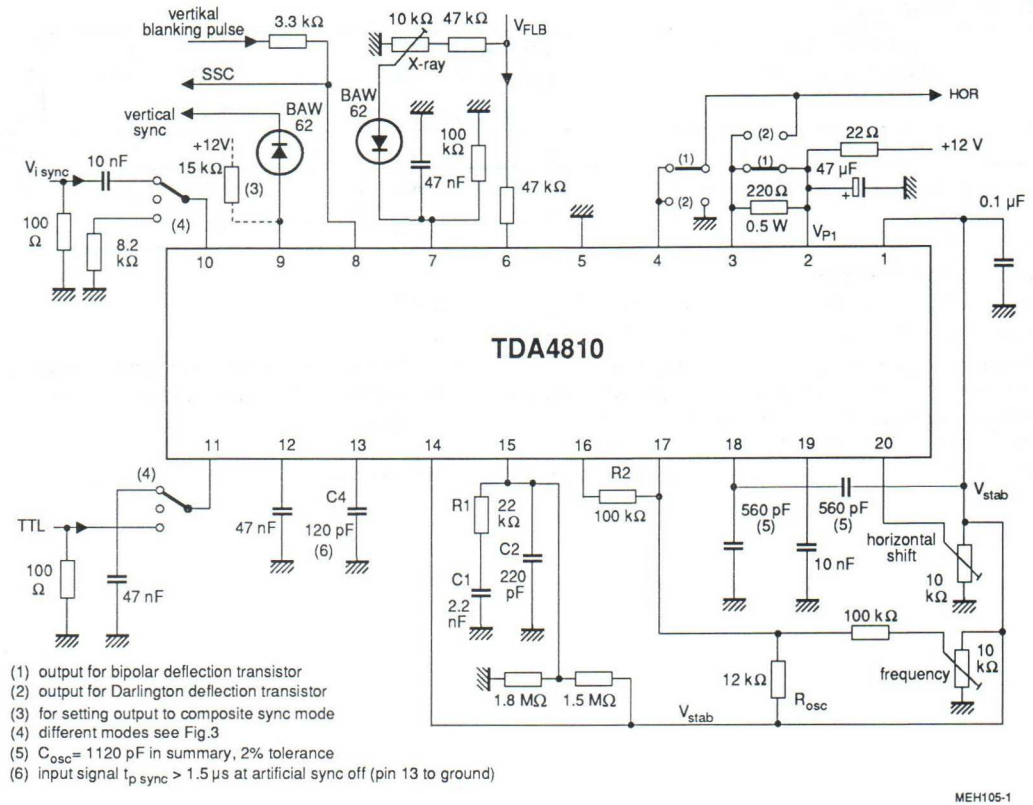
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical/composite sync output						
$V_{9\,H}$	sync output voltage HIGH	I_9 = –1 mA	9.3	10	11	V
$V_{9\,L}$	sync output voltage LOW	I_9 = 0.3 mA	-	0.7	1.1	V
R_9	resistor from V_{P1} to pin 9 to achieve composite sync mode	Fig.1	-	15	-	kΩ
t_d	delay time between leading edge of vertical sync and vertical trigger pulse	pin 9	7.5	15	20	µs
Artificial sync generator						
V_{13}	threshold voltage	lower threshold; Fig.6	-	1.6	-	V
		upper threshold	-	4.8	-	V
	input voltage for generator off	direct sync	ground-connected			V
I_{13}	output current	generator active	-	$\pm I_{17}$	-	µA
$t_{p\,sync}$	internal sync pulse width	C4 = 120 pF; note 5 f_{osc} = 64 kHz	-	1.5	-	µs
Coincidence detector		with 47 nF from pin 14 to ground				
V_{14}	capacitor voltage	during coincidence	-	5	-	V
		during catching	-	-	1.5	V
I_{14}	charging current	during sync pulse	-	–150	-	µA
	discharging current	during gating pulse	-	25	-	µA
Phase comparator PLL1						
V_{15}	control voltage	lower limit	-	1.6	-	V
		upper limit	-	4.6	-	V
I_{15}	control current	during sync pulse	-	$\pm 0.8 I_{17}$	-	µA
I_{16}	buffer output current		-	±2	-	mA
R_{16}	buffer output resistance		-	10	-	Ω
Horizontal oscillator						
f_{osc}	free-running frequency	R_{osc} = 12 kΩ; C_{osc} = 1.1 nF; note 1	-	65	-	kHz
$\Delta f / f_o$	frequency deviation with fixed external components		-	-	±3	%
TC	temperature coefficient	$(\Delta f/f_o)/\Delta T$	-	-	±15	10^{-5}/K
$\Delta f/\Delta V_{P1}$	frequency dependent on supply voltage	8.5 V < V_{P1} < 16 V	-	±5	±20	Hz/V
φ_H / t_H	relative holding/catching range	R2 = 100 kΩ; note 2	±4.5	±5	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase comparator PLL2 and phase shifter						
V_{19}	control voltage	upper limit	-	4.6	-	V
		lower limit	-	1.6	-	V
I_{19}	control current during flyback	$V_6 > 3.4$ V	-	$\pm 0.8 I_{17}$	-	µA
V_{20}	input voltage range		-	1.6 to 4.6	-	V
$\Delta t_s/t_H$	phase shifting range, Fig.6	leading edge of sync to middle of flyback	-	±20	-	%
$t_{d\ FLB}$	relative delay time between middle of sync pulse and middle of flyback pulse	Fig.6	3.6	4.4	5.3	%
Horizontal flyback input						
V_6	maximum input voltage		internal limited			V
	slicing level for PLL2	Fig.6	-	3	3.4	V
	slicing level for horizontal blanking		-	0.3	0.45	V
Horizontal pulse generator and output for bipolar deflection transistor						
V_4	output voltage LOW	$I_4 = 100$ mA	-	0.8	1.2	V
I_4	output current (sink)	Fig.4	-	-	100	mA
t_p/t_H	relative pulse width	$V_3 = V_2 = V_{P1}$	-	45	-	%
Horizontal pulse generator and output for Darlington deflection transistor						
V_{3-4}	saturation voltage	$I_3 = -I_4 = 900$ mA	-	1.4	2	V
		$I_4 = -100$ mA	-	0.25	0.4	V
I_3	output current (sink)		-	-	900	mA
t_p/t_H	relative pulse width	$V_3 < V_{P1}$	-	30	-	%
Super sandcastle pulse generator (SSC)						
V_8	output voltage during horizontal scan	$I_8 = 0$	-	-	0.5	V
	output voltage during vertical blanking	$I_8 = 2.8$ mA	2.15	2.5	3.0	V
	output voltage during horizontal blanking		4.2	4.5	4.9	V
	output voltage during clamping pulse	note 3	-	11	-	V
I_8	sink current during trailing edge	$V_8 = 1.5$ V	-	2	-	mA
	vertical blanking current	$V_8 > 2.15$ V	2.3	-	-	mA
		$V_8 < 3$ V	-	-	3.3	mA
$t_{p\ SC}$	gating pulse width	Figures 5 and 6; note 6	-	0.8	-	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Protection circuit input						
V_7	threshold input voltage for horizontal output off	note 4 V_7 positive-going V_7 negative-going	 6.18 -	 6.3 –0.2	 6.5 -	 V V
t_d	switching off delay time		-	17	-	µs
V_{P1}	too low supply voltage threshold	horizontal output off horizontal output on	5.4 6.0	5.8 6.4	6.2 6.8	V V

Notes to the characteristics

1. $T_{osc} = 1.16 \times R_{osc} \times C_{osc}$ (approximate value); R_{osc}: 9 kΩ to 18 kΩ
2. $R2 = 48 / p \times R_{osc}$ (approximate value); p ≤10% (catching range)
3. The leading edge of the clamping pulse starts after the trailing edge of the sync pulse respectively with artificial sync.
4. The effect of the protection circuit is to switch off the horizontal output and to latch the error indication. Therefore, the supply voltage must be switched off and on to enable the circuit again
5. Approximate sync pulse width $t_{p\ sync} = C4 \times R_{osc}$
6. Gating pulse width $t_{p\ SC} = 0.1t_H - t_{p\ sync} / 2$ (approximate value at $V_8 = 7$ V)



(1) output for bipolar deflection transistor
(2) output for Darlington deflection transistor
(3) for setting output to composite sync mode
(4) different modes see Fig.3
(5) C_{osc}= 1120 pF in summary, 2% tolerance
(6) input signal $t_{p\ sync}$ > 1.5 µs at artificial sync off (pin 13 to ground)

MEH105-1

Fig.5 Test and application circuit for 64 kHz deflection.

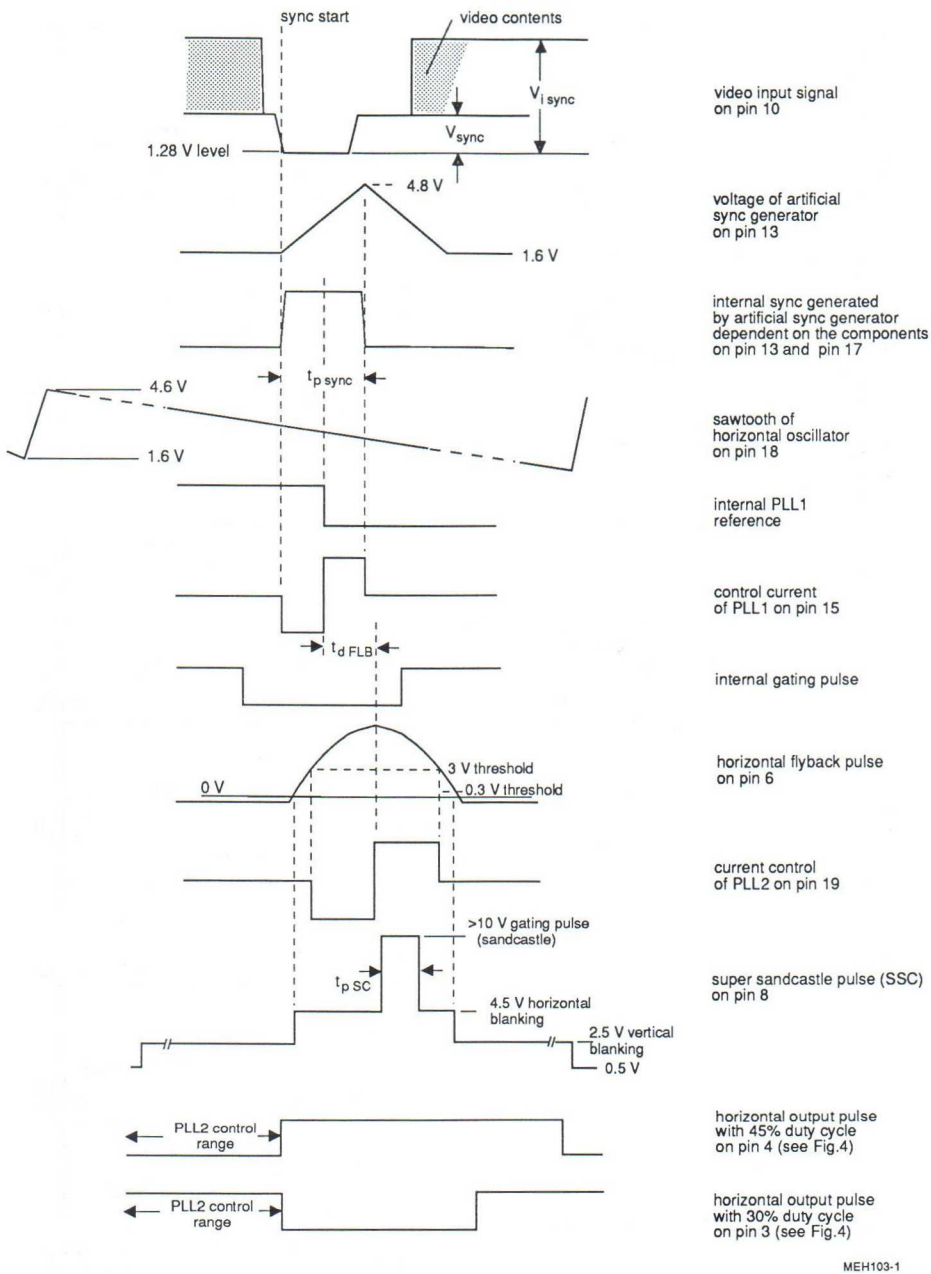


Fig.6 Timing diagram using the artificial sync generator.

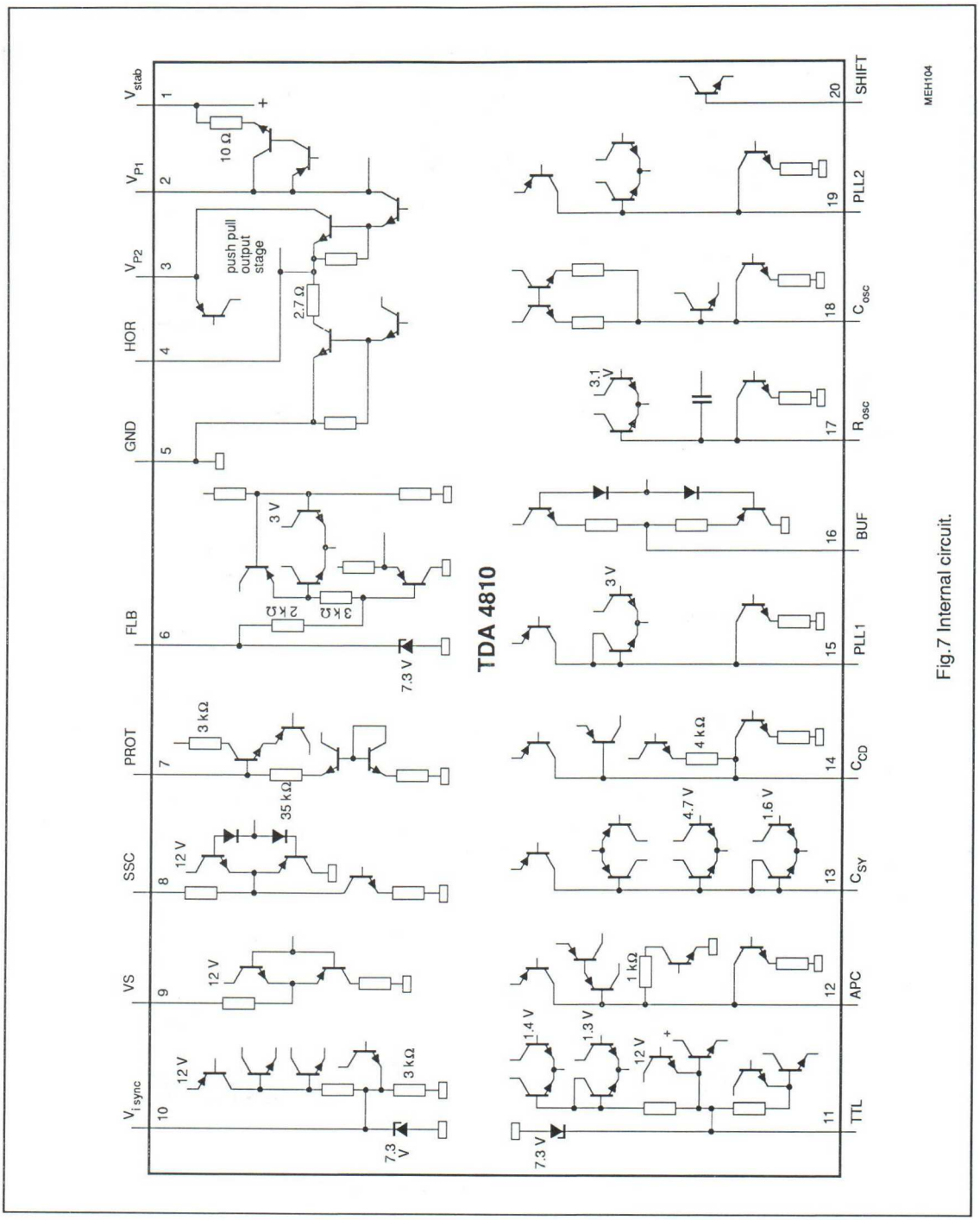


Fig.7 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	June 1990

TDA4820T
Sync separation circuit for video applications

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7} = 1$ mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A

Sync separation circuit for video applications

TDA4820T

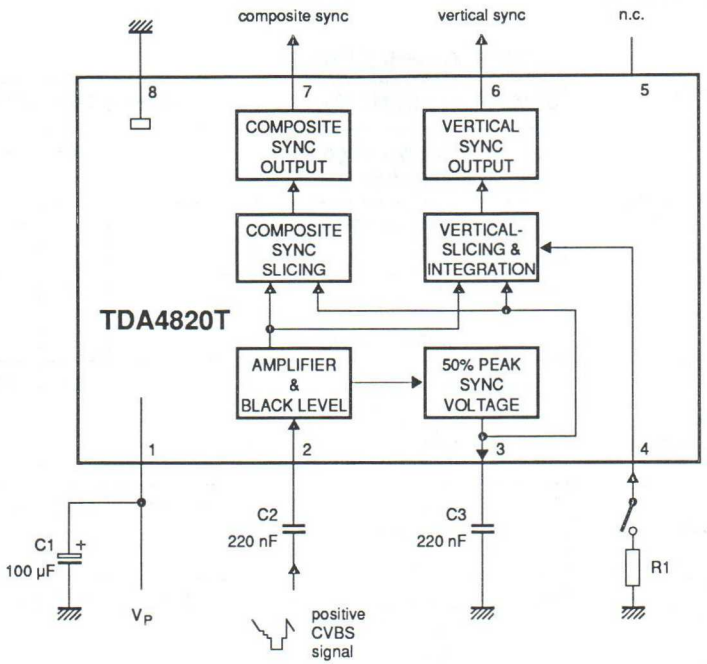


Fig. 1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

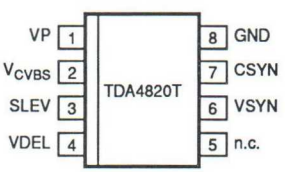


Fig. 2 Pin configuration.

Sync separation circuit for video applications

TDA4820T

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.

The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3.

A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.

With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.

The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded). Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be $\geq$ 3.3 kΩ. In this case t_{dV} is typically $\geq$ 23 µs.

Vertical sync output
Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

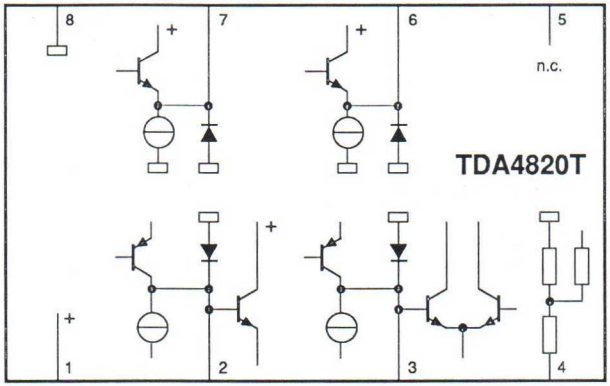


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	–0.5	6	V
I_o	output current (pin 6 and pin 7)	3	–10	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	–	150	°C
P_{tot}	total power dissipation	–	500	mW

Sync separation circuit for video applications

TDA4820T

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for $0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	50	300	500	mV
Z_s	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	µA
	charge currents of C2	sync below slicing level	–	–40	–	µA
		sync above slicing level	–	–25	–	µA
		during black level	–	–20	–	µA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	µA
	maximum charge current of C3		–	–345	–	µA
	reduced charge current of C3	during vertical sync	–	–255	–	µA
	charge current of C3	during sync pulse	–	–160	–	µA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: $C_L \leq 5\ pF$; $R_L \geq 100\ k\Omega$	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	µs
		pin 4 grounded	11	18	25	µs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1\ mA$	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3\ mA$	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7} = 1\ mA$	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	µs

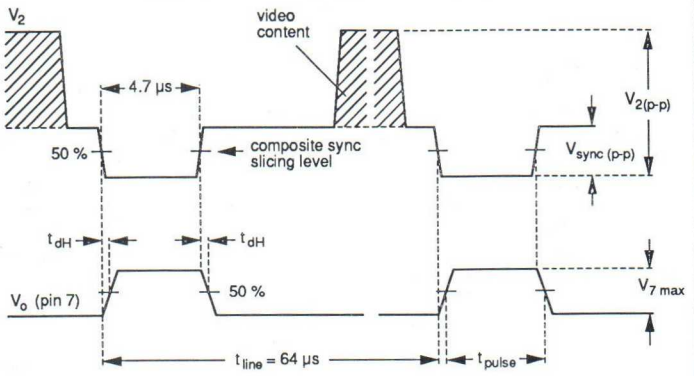
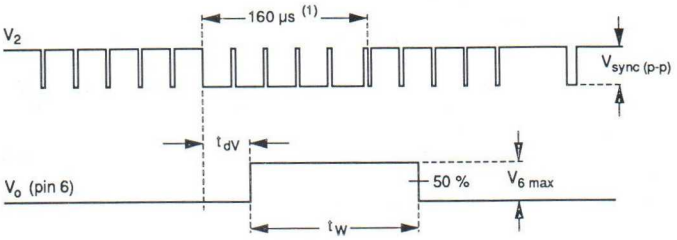


Fig.4 Typical horizontal sync signal.



(1) due to 625 line standard

Fig.5 Typical vertical sync signal.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	September 1991

TDA4850

Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

FEATURES

- VGA operation fully implemented including alignment-free vertical and E/W amplitude presettings
- 4th VGA mode easy applicable (XGA, Super VGA)
- Multi-frequency operation externally selectable
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in multi-frequency operation
- DC-coupling to vertical power amplifier (TDA4860, TDA8351)
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments

GENERAL DESCRIPTION

The TDA4850 is a monolithic integrated circuit for economical solutions in VGA/XGA and multi-frequency monitors. The IC incorporates the complete horizontal and vertical small signal processing. VGA-dependent mode detection and settings are performed on chip. In conjunction with TDA4860 or TDA8351 (vertical output circuits) both ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	9.2	12	16	V
I_P	supply current	-	40	-	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value, pin 9)	-	1	-	V
	sync slicing level	-	120	-	mV
	DC-coupled TTL-compatible horizontal sync signal (peak value, pin 9)	1.7	-	-	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak value, pin 10)	1.7	-	-	V
	slicing level	1.2	1.4	1.6	V
$I_{o\ V}$	vertical differential output current (peak-to-peak value, pins 5 and 6)	-	1	-	mA
$I_{o\ H}$	horizontal sink output current on pin 3	-	-	60	mA
T_{amb}	operating ambient temperature	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4850	20	DIL	plastic	SOT146

Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

TDA4850

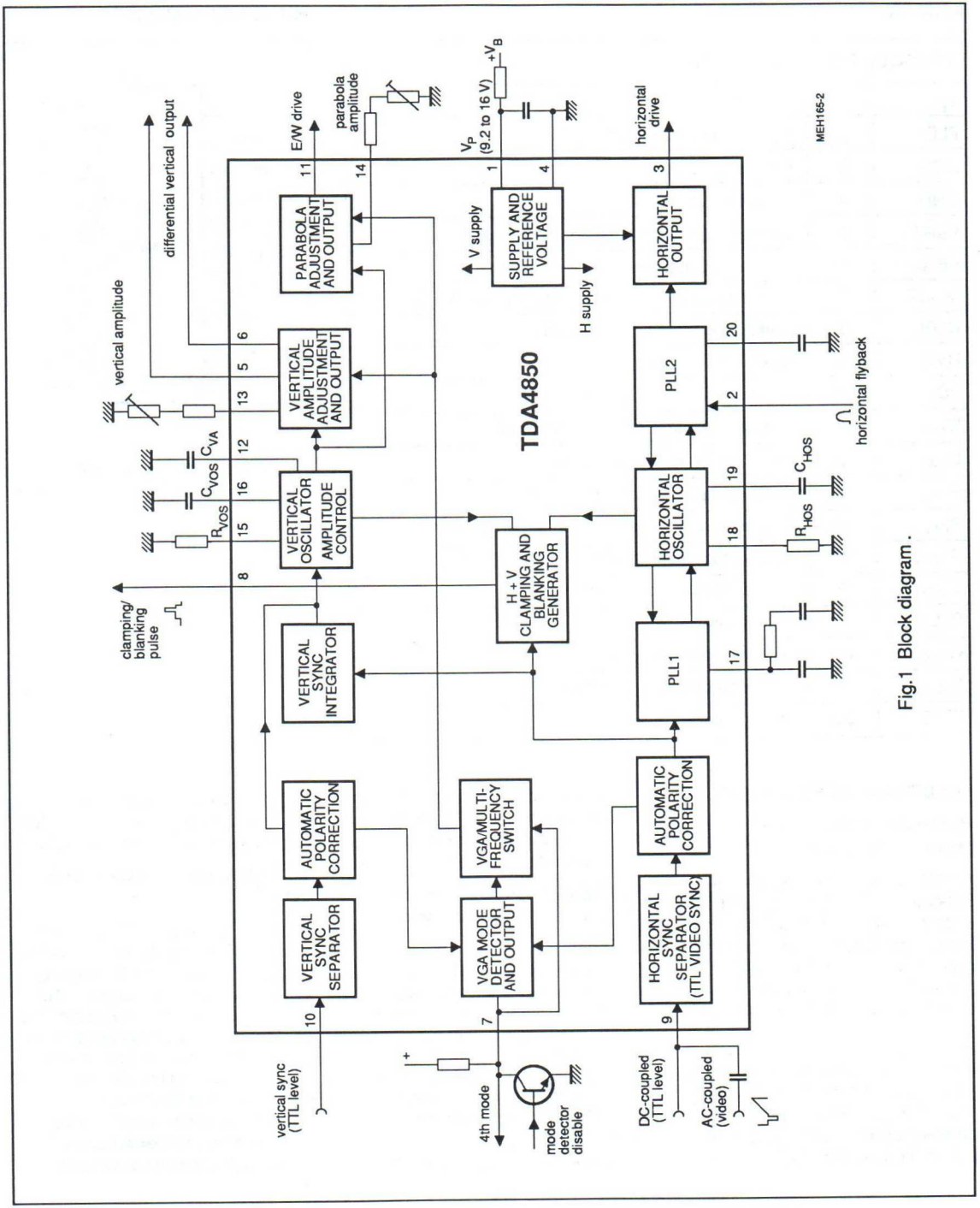


Fig.1 Block diagram.

Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

TDA4850

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
MODE	7	4th mode output and mode detector disable input
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync /video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C_{VA}	12	capacitor for amplitude control
R_{VA}	13	vertical amplitude adjustment input
R_{EW}	14	E/W amplitude adjustment input (parabola)
R_{VOS}	15	vertical oscillator resistor
C_{VOS}	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R_{HOS}	18	horizontal oscillator resistor
C_{HOS}	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase

PIN CONFIGURATION

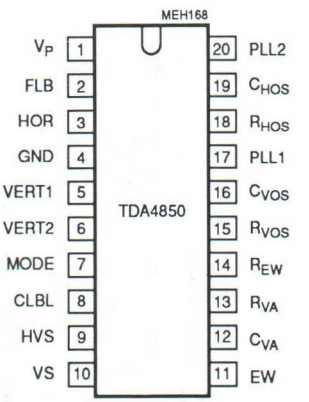


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.
DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected. The polarity information is fed to the VGA mode detector. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then polarity is corrected. The polarity information is fed to the VGA mode detector. If pin 10 is not used, it must be connected to ground.
The separated $V_{i\ sync}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

VGA mode detector and mode output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V_P to pin 7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by HIGH on pin 7. This signal can be used externally to switch any horizontal or vertical parameters.

VGA mode detector input

For multi-frequency operation the voltage on pin 7 must be externally forced to a level of <50 mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 µs to 300 µs (575 µs is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 Hz up to 110 Hz.

Clamping and blanking generator

A combined clamping and blanking pulse is available on pin 8 (suitable for the video pre-amplifier TDA 4880). The lower level of 2.1 V can be the blanking signal derived from line flyback, or the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals to the delay between vertical sync and start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA as well as for multi-frequency operation (selectable via pin 7).

The upper level of 3.9 V is the horizontal clamping pulse with internally fixed pulse width of 1 µs. A monoflop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse.

PLL1 phase detector

The phase detector is a standard one using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17.

Horizontal oscillator

This oscillator is a relaxation type oscillator. Its frequency is determined mainly by the capacitor on pin 19. A frequency range of one octave is achieved by the current on pin 18. The φ1 control voltage from pin 17 is fed via a buffer amplifier and an attenuator to the current reference pin 18 to achieve a high DC loop gain. Therefore, changes in frequency will not affect the phase relationship between horizontal sync pulses and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.
A certain amount of phase adjustment is possible by injecting a DC current from an external source into the PLL2 filter capacitor on pin 20.

Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is 300 mV at 20 mA.
To protect the line deflection transistor, the horizontal output stage does not conduct at $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions.The free-running frequency f_o is determined by the values of R_{VOS} and C_{VOS}. The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS}. Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_o = 1 / (10.8 \times R_{VOS} \times C_{VOS})$$

To achieve a stabilized amplitude the free-running frequency f_o (without adjustment) must be lower than the lowest occuring sync frequency. The following contributions can be assumed:

- minimum frequency offset between f_o and the lowest trigger frequency	10% ±3% ±1%
- spread of IC	±5%
- spread of R (22 kΩ)	19%
- spread of C (0.1 µF)	

Result: f_o = 50 Hz/1.19 = 42 Hz
(for 50 to 110 Hz application)

Table 1 VGA modes

mode	H/V sync polarity	frequency H	frequency V	number of active lines	mode output pin 7
1	+ / –	31.45 kHz	70 Hz	350	LOW
2	– / +	31.45 kHz	70 Hz	400	LOW
3	– / –	31.45 kHz	60 Hz	480	LOW
4	+ / +	fixed by external circuitry	-	-	HIGH

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.5	16	V
$V_{3,7}$	voltage on pins 3 and 7	–0.5	16	V
V_8	voltage on pin 8	–0.5	7	V
V_n	voltage on pins 5, 6, 9, 10, 13, 14 and 18	–0.5	6.5	V
I_2	current on pin 2	-	±10	mA
I_3	current on pin 3	-	100	mA
I_7	current on pin 7	-	20	mA
I_8	current on pin 8	-	–10	mA
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
T_j	maximum junction temperature	0	150	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	-	65	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		9.2	12	16	V
I_P	supply current		-	40	-	mA
Internal reference voltage						
V_{ref}	internal reference voltage		6.0	6.25	6.5	V
TC	temperature coefficient	T_{amb} = 20 to 100 °C	-	-	±90	10^{-6}/K
PSRR	power supply ripple rejection	f = 1 kHz sinewave	60	75	-	dB
		f = 1 MHz sinewave	25	35	-	dB
V_P	supply voltage (pin 1) to ensure all internal reference voltages		9.2	-	16	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite sync input (AC-coupled)		V_{10} = 5 V				
$V_{i\ sync}$	sync amplitude of video input signal (pin 9)	sync on green	-	300	-	mV
	top sync clamping level		1.1	1.28	1.5	V
	slicing level above top sync level	R_S = 50 Ω	90	120	150	mV
R_S	allowed source resistance for 7% duty-cycle	$V_{i\ sync}$ > 200 mV	-	-	1.5	kΩ
r_9	differential input resistance	during sync	-	80	-	Ω
I_9	charging current of coupling capacitor	V_9 > 1.5 V	1.3	2	3	μA
t_{int}	vertical sync integration time to generate sync pulse		7	10	13	μs
Horizontal sync input (DC-coupled, TTL-compatible)						
$V_{i\ sync}$	sync input signal (peak value, pin 9)		1.7	-	-	V
	slicing level		1.2	1.4	1.6	V
t_p	minimum pulse width		700	-	-	ns
t_r, t_f	rise time and fall time		10	-	500	ns
I_9	input current	V_9 = 0.8 V	-	-	–200	μA
		V_9 = 5.5 V	-	-	10	μA
Automatic horizontal polarity switch		H-sync on pin 9				
$t_{p\ H}/t_H$	horizontal sync pulse width related to t_H (duty cycle for automatic polarity correction)		-	-	30	%
t_p	delay time for changing sync polarity		0.3	-	1.8	ms
Vertical sync input (DC-coupled, TTL-compatible)		V-sync on pin 10				
$V_{i\ sync}$	sync input signal (peak value, pin 10)		1.7	-	-	V
	slicing level		1.2	1.4	1.6	V
I_{10}	input current	0 < V_{10} < 5.5 V	-	-	±10	μA
$t_{p\ V}$	maximum vertical sync pulse width for automatic vertical polarity switch		-	-	300	μs
Horizontal mode detector output		VGA mode				
V_7	output saturation voltage LOW (for modes 1, 2 and 3)	I_7 = 6 mA	-	0.275	0.33	V
	output voltage HIGH	mode 4	-	-	V_P	V
I_7	load current range to force VGA mode-dependent vertical and parabola amplitudes	modes 1, 2 and 3	2	-	6	mA
	output current	mode 4	-	0	-	mA
VGA / multi-frequency mode switch						
V_7	input voltage LOW to force multi-frequency mode		0	-	50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal comparator PLL1						
V_{17}	upper control voltage limitation		-	5.0	-	V
	lower control voltage limitation		-	1.2	-	V
I_{17}	control current	Fig.4	-	±300	-	µA
Horizontal oscillator						
f_{osc}	centre frequency	R_{18} = 12 kΩ (pin 18); C_{19} = 2.2 nF (pin 19)	-	31.45	-	kHz
	deviation of centre frequency		-	-	±3	%
	temperature coefficient		-	-	±150	10^{-6}/K
φ_H/t_H	relative holding/catching range		±6	±6.5	±7.3	%
R_{18}	external oscillator resistor		9	-	18	kΩ
V_{18}	voltage at reference current input (pin 18)	PLL1 and PLL2 locked; V_{ref} = 6.25 V	-	3.125	-	V
ΔV_{18}	control voltage range		-	±205	-	mV
Horizontal PLL2		Fig.4				
V_2	upper clamping level of flyback input	I_2 = 6 mA	-	5.5	-	V
	lower clamping level of flyback input	I_2 = −1 mA	-	−0.75	-	V
	H-flyback slicing level		-	3.0	-	V
I_2	input current	H-scan ; V_8 < 0.9 V	−0.5	-	-	mA
		H-flyback ; V_8 >1.8 V	-	-	−0.2	mA
t_d/t_H	delay between middle of sync and middle of H-flyback related to t_H		-	3.0	-	%
V_{20}	upper control voltage limitation		-	4.6	-	V
	lower control voltage limitation		-	1.6	-	V
I_{20}	control current		-	±200	-	µA
$\Delta t/t_H$	PLL2 control range related to t_H		30%	-	-	%
Horizontal output (open-collector)		Fig.4				
V_3	output voltage LOW	I_3 = 20 mA	-	-	0.3	V
		I_3 = 60 mA	-	-	0.8	V
t_p/t_H	t_H duty cycle		42	45	48	%
V_P	threshold to activate too low supply voltage protection	horizontal output off	-	5.8	-	V
		horizontal output on	-	6.4	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal clamping/blanking generator output		Fig.4				
V_8	output voltage LOW	H and V scanning	-	-	0.9	V
	blanking output voltage	internal V blanking	1.8	2.1	2.4	V
		external H blanking	1.8	2.1	2.4	V
	clamping output voltage	H-sync on pin 9	3.5	3.9	4.3	V
I_8	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
t_8	clamping pulse start		with end of H-sync			
t_{clp}	clamping pulse width		0.8	1.0	1.2	µs
S	steepness of rise and fall times		-	40	-	ns/V
Vertical oscillator		V_{ref} = 6.25 V				
f_o	vertical free-running frequency	R_{15} = 22 kΩ; C_{16} = 0.1 µF		42	-	Hz
f_V	nominal vertical sync range	no f_o adjustment	50	-	110	Hz
V_{15}	voltage on pin 15	R_{15} = 22 kΩ	2.8	3.0	3.2	V
t_d	delay between sync pulse and start of vertical scan	measured on pin 8				
	in VGA/XGA mode, activated by an external resistor on pin 7		500	575	650	µs
	in multi-frequency mode	V_7 < 50 mV	240	300	360	µs
I_{12}	control current for amplitude control		-	±200	-	µA
C_{12}	capacitor for amplitude control		-	-	0.33	µF
Vertical differential output		Fig.5				
I_o	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; I_{13} > −135 µA; R_{15} = 22 kΩ	0.9	1.0	1.1	mA
	maximum offset-current error	I_o = 1 mA	-	-	±2.5	%
	maximum linearity error		-	-	±1.5	%
Vertical amplitude adjustment (in percents of output signal)						
V_{13}	input voltage		-	5.0	-	V
I_{13}	adjustment current	$I_{o\,max}$ (100%)	−110	−120	−135	µA
		$I_{o\,min}$ (typically 58%)	-	0	-	µA
$\Delta I_o/\Delta t$	VGA mode-dependent pre-settings activated by an external resistor on pin 7	Table 1; note 1				
	in mode 1		116.1	116.8	117.5	%
	in mode 2		102.0	102.2	102.5	%
	in mode 3		-	100	-	%
	in mode 4		-	100	-	%
	in multi-frequency operation (VGA operation disabled)	V_7 < 50 mV	-	100	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W output		note 2				
V_{11}	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.2	4.5	4.8	V
	temperature coefficient of output signal		-	-	250	10^{-6}/K
E/W amplitude adjustment (parabola)		Fig.5				
V_{14}	input voltage (pin 14)		-	5.0	-	V
I_{14}	adjustment current	100% parabola	−110	−120	−135	μA
		typically 28% parabola	-	0	-	μA

Notes to the characteristics

1. $\Delta I_o/\Delta t$ relative to value of mode 3.
2. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potmeter to pin 14.

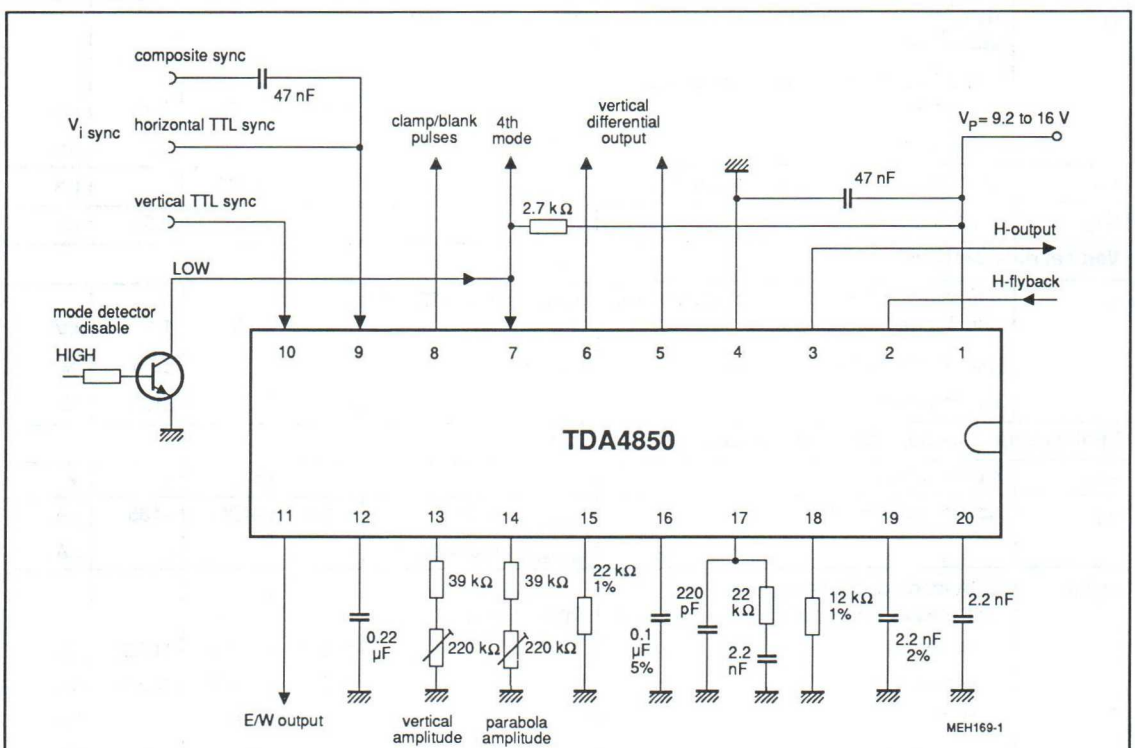


Fig.3 Test and application circuit (measurements taken at V_P = 12 V).

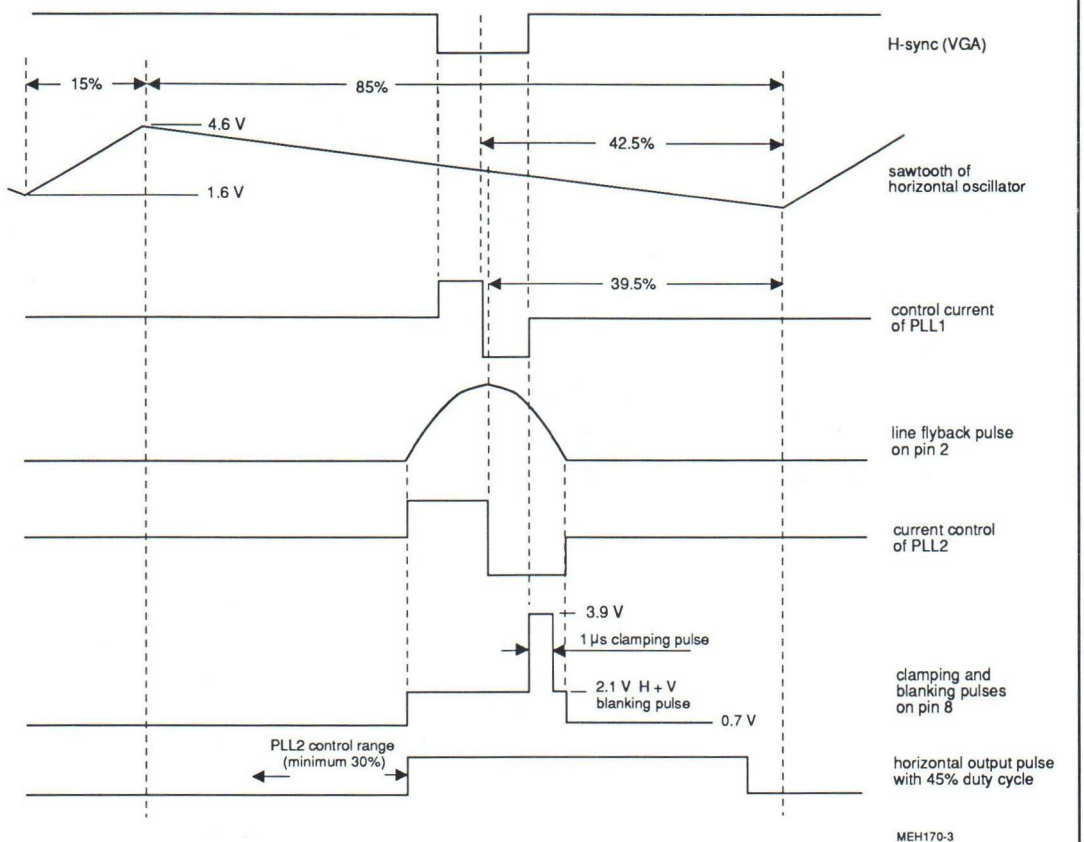


Fig.4 Horizontal timing diagram.

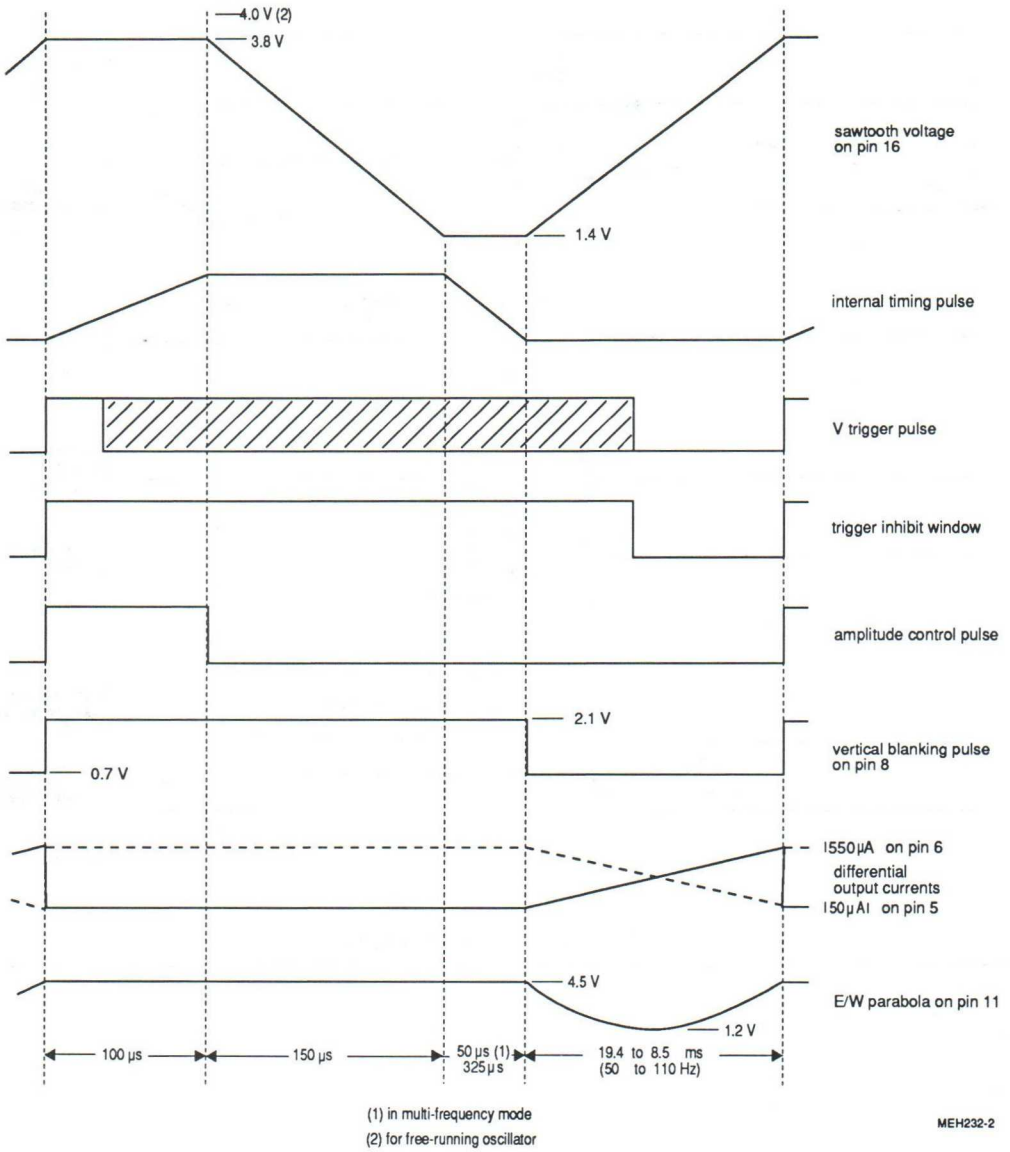


Fig.5 Vertical and E/W timing diagram.

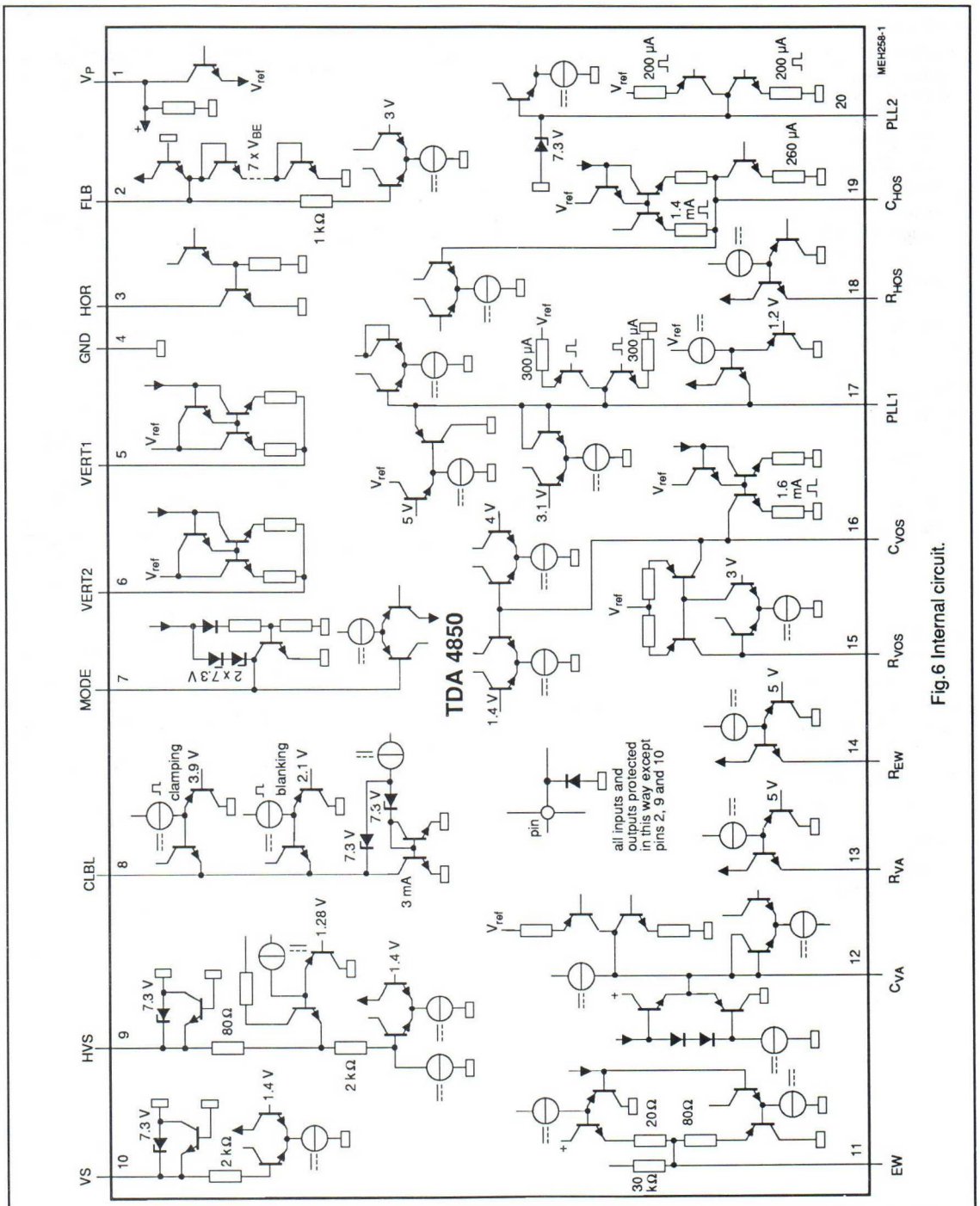


Fig.6 Internal circuit.

Horizontal and vertical deflection controller for VGA/XGA and autosync monitors

TDA4851

FEATURES

- VGA operation fully implemented including alignment-free vertical and E/W amplitude presettings
- 4th VGA mode easy applicable (XGA, Super VGA)
- Autosync operation externally selectable
- Low jitter
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in autosync operation
- DC-coupling to vertical power amplifier
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	9.2	12	16	V
I_P	supply current	–	40	–	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value, pin 9)	–	1	–	V
	sync slicing level	–	120	–	mV
	DC-coupled TTL-compatible horizontal sync signal (peak-to-peak value, pin 9)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak-to-peak value, pin 10)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
$I_{o\ V}$	vertical differential output current (peak-to-peak value, pins 5 and 6)	–	1	–	mA
$I_{o\ H}$	horizontal sink output current on pin 3	–	–	60	mA
T_{amb}	operating ambient temperature range	0	–	+70	°C

GENERAL DESCRIPTION

The TDA4851 is a monolithic integrated circuit for economical solutions in VGA/XGA and autosync monitors. The IC incorporates the complete horizontal and vertical small signal processing.
VGA-dependent mode detection and settings are performed on chip. In conjunction with TDA4860/61/65, or TDA8351 (vertical output circuits) the ICs offer an extremely advanced system solution.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4851	20	DIL	plastic	SOT146

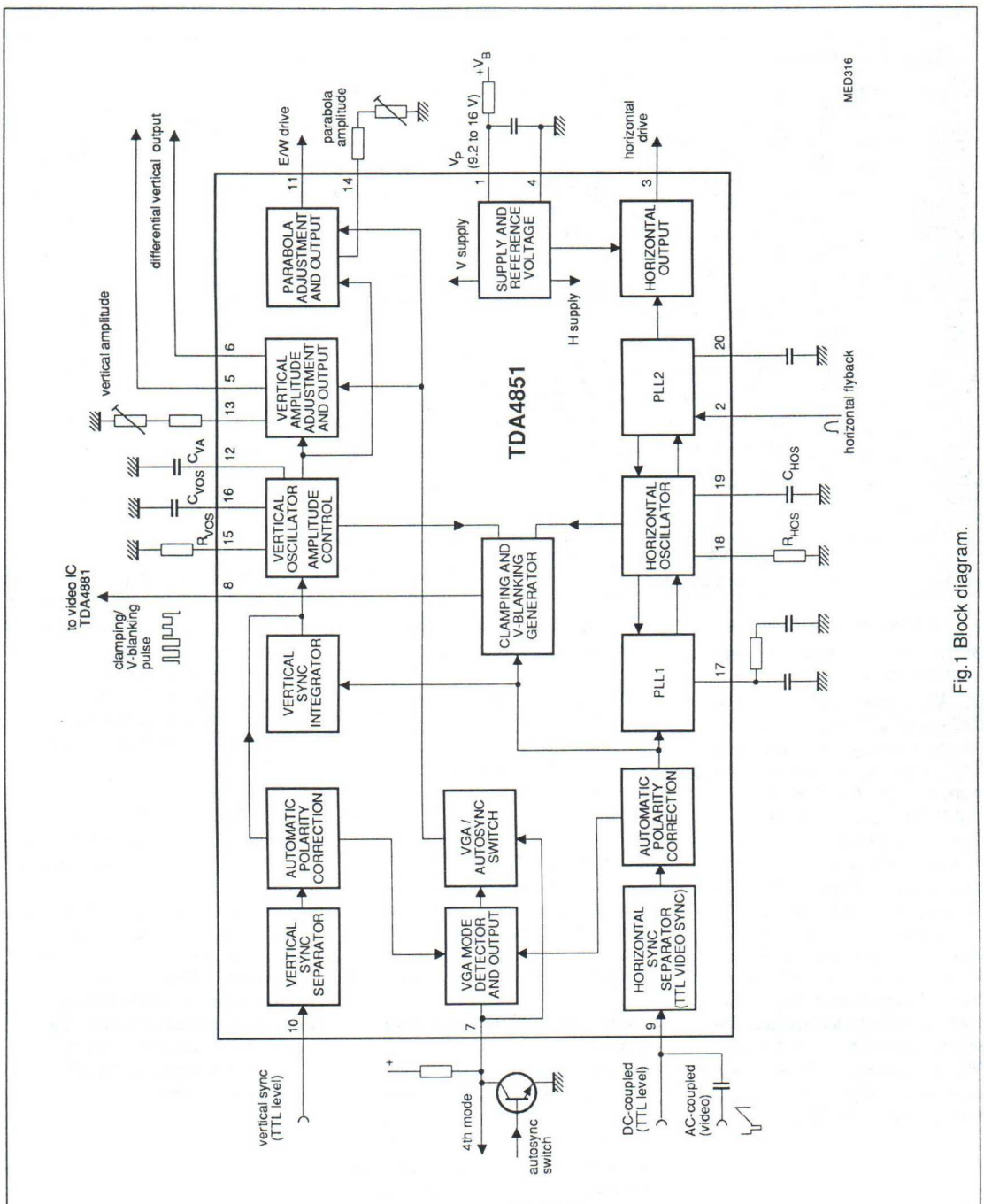


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
MODE	7	4th mode output and autosync input
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync/video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C_{VA}	12	capacitor for amplitude control
R_{VA}	13	vertical amplitude adjustment input
R_{EW}	14	E/W amplitude adjustment input (parabola)
R_{VOS}	15	vertical oscillator resistor
C_{VOS}	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R_{HOS}	18	horizontal oscillator resistor
C_{HOS}	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase

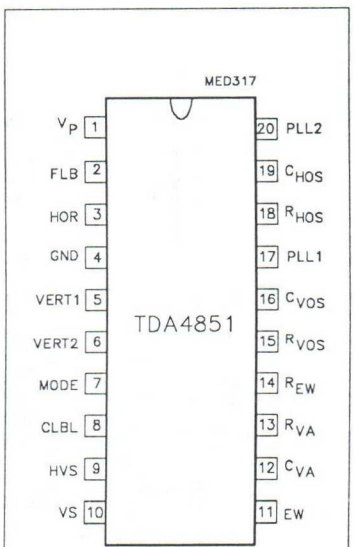


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.

DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected. The polarity information is fed to the VGA mode detector. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then the polarity is corrected. The polarity information is fed to the VGA mode detector. If pin 10 is not used, it must be connected to ground.

The separated $V_{i\ sync}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

VGA mode detector and mode output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V_P to pin 7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by a HIGH on pin 7. This signal can be used externally to switch any horizontal or vertical parameters.

VGA mode detector input

For autosync operation the voltage on pin 7 must be externally forced to a level of < 50 mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 µs to 300 µs (575 µs is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 Hz up to 110 Hz.

Clamping and V-blanking generator

A combined clamping and V-blanking pulse is available on pin 8 (suitable for the video pre-amplifier TDA4881). The lower level of 1.9 V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals the delay between vertical sync and start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA and autosync operation (selectable via pin 7).

The upper level of 5.4 V is the horizontal clamping pulse with an internally fixed pulse width of 0.8 µs. A monoflop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse.

If composite sync is applied, one clamping pulse per H-period is generated during V-sync. The phase of the clamping pulse may change during V-sync (see Fig.8).

PLL1 phase detector

The phase detector is a standard type using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17. If composite sync is applied, the disturbed control voltage is corrected during V-sync (see Fig.8).

Horizontal oscillator

This oscillator is of the relaxation type and requires a fixed capacitor of 10 nF at pin 19. By changing the current into pin 18 the whole frequency range from 13 to 100 kHz can be covered.

The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary.

The PLL1 control voltage at pin 17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustment is possible by injecting a DC current from an external source into the PLL2 filter capacitor at pin 20.

Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is less than 300 mV at 20 mA.

To protect the line deflection transistor, the horizontal output stage does not conduct for $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions. The free-running frequency f_0 is determined by the values of R_{VOS} and C_{VOS}. The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS}. Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_0 = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_0 (without adjustment) must be lower than the lowest occuring sync frequency. The following contributions can be assumed:

minimum frequency offset between f_0 and the lowest trigger frequency	10%
spread of IC	±3%
spread of R (22 kΩ)	±1%
spread of C (0.1 µF)	±5%
	19%

Result: $f_0 = \frac{50}{1.19}$ Hz = 42 Hz

(for 50 to 110 Hz application)

Table 1 VGA modes

MODE	H / V SYNC POLARITY	FREQUENCY H (kHz)	FREQUENCY V (Hz)	NUMBER OF ACTIVE LINES	MODE OUTPUT PIN 7
1	+ / −	31.45	70	350	LOW
2	− / +	31.45	70	400	LOW
3	− / −	31.45	60	480	LOW
4	+ / +	fixed by external circuitry	−	−	HIGH
autosync	*/*	fixed by external circuitry	−	−	forced to GND

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	−0.5	16	V
$V_{3,7}$	voltage on pins 3 and 7	−0.5	16	V
V_8	voltage on pin 8	−0.5	7	V
V_n	voltage on pins 5, 6, 9, 10, 13, 14 and 18	−0.5	6.5	V
I_2	current on pin 2	−	±10	mA
I_3	current on pin 3	−	100	mA
I_7	current on pin 7	−	20	mA
I_8	current on pin 8	−	−10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	70	°C
T_j	maximum junction temperature	0	+150	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−	±400	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = +25 °C; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		9.2	12	16	V
I_P	supply current	I_{18} = −1.05 mA	−	36	44	mA
		I_{18} = −3.388 mA	−	40	49	mA
Internal reference voltage						
V_{ref}	internal reference voltage		6.0	6.25	6.5	V
TC	temperature coefficient	T_{amb} = +20 to +100 °C	−	−	±90	10^{-6}/K
PSRR	power supply ripple rejection	f = 1 kHz sinewave	60	75	−	dB
		f = 1 MHz sinewave	25	35	−	dB
V_P	supply voltage (pin 1) to ensure all internal reference voltages		9.2	−	16	V
Composite sync input (AC-coupled)		V_{10} = 5 V				
$V_{i\ sync}$	sync amplitude of video input signal (pin 9)	sync on green	−	300	−	mV
	top sync clamping level		1.1	1.28	1.5	V
	slicing level above top sync level	R_S = 50 Ω	90	120	150	mV
R_S	allowed source resistance for 7% duty factor	$V_{i\ sync}$ > 200 mV	−	−	1.5	kΩ
r_9	differential input resistance	during sync	−	80	−	Ω
I_9	charging current of coupling capacitor	V_9 > 1.5 V	1.3	2	3	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{int}	vertical sync integration time to generate vertical trigger pulse	f_H = 31 kHz; I_{18} = −1.050 mA	7	10	13	µs
		f_H = 64 kHz; I_{18} = −2.169 mA	3.5	5	6.5	µs
		f_H = 100 kHz; I_{18} = −3.388 mA	2.5	3.4	4.5	µs
Horizontal sync input (DC-coupled, TTL-compatible)						
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 9)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
t_p	minimum pulse width		700	–	–	ns
t_r, t_f	rise time and fall time		10	–	500	ns
I_9	input current	V_9 = 0.8 V	–	–	−200	µA
		V_9 = 5.5 V	–	–	10	µA
Automatic horizontal polarity switch		H-sync on pin 9				
$t_{p\ H}/t_H$	horizontal sync pulse width related to t_H (duty factor for automatic polarity correction)		–	–	30	%
t_p	delay time for changing sync polarity		0.3	–	1.8	ms
Vertical sync input (DC-coupled, TTL-compatible)		V-sync on pin 10				
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 10)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
I_{10}	input current	$0 < V_{10} < 5.5$ V	–	–	±10	µA
$t_{p\ V}$	maximum vertical sync pulse width for automatic vertical polarity switch		–	–	300	µs
Horizontal mode detector output		VGA mode				
V_7	output saturation voltage LOW (for Modes 1, 2 and 3)	I_7 = 6 mA	–	0.275	0.33	V
	output voltage HIGH	mode 4	–	–	V_P	V
I_7	load current range to force VGA mode-dependent vertical and parabola amplitudes	modes 1, 2 and 3	2	–	6	mA
	output current	mode 4	–	0	–	mA
VGA / autosync mode switch						
V_7	input voltage LOW to force autosync mode		0	–	50	mV
Horizontal clamping / blanking generator output		Fig.6				
V_8	output voltage LOW		–	–	0.9	V
	blanking output voltage	internal V blanking	1.6	1.9	2.2	V
	clamping output voltage	H-sync on pin 9	5.15	5.4	5.65	V
I_8	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
	external load current		–	–	−3.0	mA
t_8	clamping pulse start		with end of H-sync			
t_{clp}	clamping pulse width	V_8 = 3 V	0.6	0.8	1.0	µs
S	steepness of rise and fall times		–	60	75	ns/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical oscillator		V_{ref} = 6.25 V				
f_0	vertical free-running frequency	R_{15} = 22 kΩ; C_{16} = 0.1 µF	–	42	–	Hz
f_v	nominal vertical sync range	no f_0 adjustment	50	–	110	Hz
V_{15}	voltage on pin 15	R_{15} = 22 kΩ	2.8	3.0	3.2	V
t_d	delay between sync pulse and start of vertical scan	measured on pin 8				
	in VGA/XGA mode, activated by an external resistor on pin 7		500	575	650	µs
	in autosync mode	V_7 < 50 mV	240	300	360	µs
I_{12}	control current for amplitude control		–	±200	–	µA
C_{12}	capacitor for amplitude control		–	–	0.18	µF
Vertical differential output		Fig.7				
I_o	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; I_{13} > −135 µA; R_{15} = 22 kΩ	0.9	1.0	1.1	mA
	maximum offset-current error	I_o = 1 mA	–	–	±2.5	%
	maximum linearity error		–	–	±1.5	%
Vertical amplitude adjustment (in percentage of output signal)						
V_{13}	input voltage		–	5.0	–	V
I_{13}	adjustment current	$I_{o\,max}$ (100%)	−110	−120	−135	µA
		$I_{o\,min}$ (typically 58%)	–	0	–	µA
$\Delta I_o/\Delta t$	VGA mode-dependent pre-settings activated by an external resistor on pin 7	Table 1; note 1				
	Mode 1		116.2	116.8	117.4	%
	Mode 2		101.6	102.2	102.8	%
	Mode 3		–	100	–	%
	Mode 4		–	100	–	%
	autosync operation (VGA operation disabled)	V_7 < 50 mV	–	100	–	%
Horizontal comparator PLL1						
V_{17}	upper control voltage limitation		–	5.9	–	V
	lower control voltage limitation		–	5.1	–	V
I_{17}	control current	Fig.6	–	±0.083I_{18}	–	mA
Horizontal oscillator						
f_{osc}	centre frequency	R_{18} = 2.4 kΩ (pin 18); C_{19} = 10 nF (pin 19)	–	31.45	–	kHz
	deviation of centre frequency		–	–	±3	%
	temperature coefficient		0	+200	+300	10^{-6}/K
φ_H/t_H	relative holding/catching range		±6	±6.5	±7.3	%
I_{18}	external oscillator current		−0.5	–	−4.3	mA
V_{18}	voltage at reference current input (pin 18)		2.35	2.5	2.65	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal PLL2		Fig.6				
V_2	upper clamping level of flyback input	I_2 = 6 mA	–	5.5	–	V
	lower clamping level of flyback input	I_2 = −1 mA	–	−0.75	–	V
	H-flyback slicing level		–	3.0	–	V
t_d/t_H	delay between middle of sync and middle of H-flyback related to t_H		–	3.0	–	%
V_{20}	upper control voltage limitation		–	6.2	–	V
	lower control voltage limitation		–	4.8	–	V
I_{20}	control current		–	$\pm 0.083 I_{18}$	–	µA
$\Delta t/t_H$	PLL2 control range related to t_H		30	–	–	%
Horizontal output (open-collector)		Fig.6				
V_3	output voltage LOW	I_3 = 20 mA	–	–	0.3	V
		I_3 = 60 mA	–	–	0.8	V
t_p/t_H	t_H duty factor		42	45	48	%
V_P	threshold to activate under voltage protection	horizontal output off	–	5.6	–	V
		horizontal output on	–	5.8	–	V
Δt_H	jitter of horizontal output	f = 31 kHz	–	–	3.5	ns
		f = 64 kHz	–	–	1.9	ns
		f = 100 kHz	–	–	1.2	ns
E/W output		note 2				
V_{11}	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.2	4.5	4.8	V
	temperature coefficient of output signal		–	–	250	10^{-6}/K
E/W amplitude adjustment (parabola)		Fig.7				
V_{14}	input voltage (pin 14)		–	5.0	–	V
I_{14}	adjustment current	100% parabola	−110	−120	−135	µA
		typically 28% parabola	–	0	–	µA

Notes to the characteristics

1. $\Delta I_o/\Delta t$ relative to value of Mode 3.
2. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.

APPLICATION INFORMATION

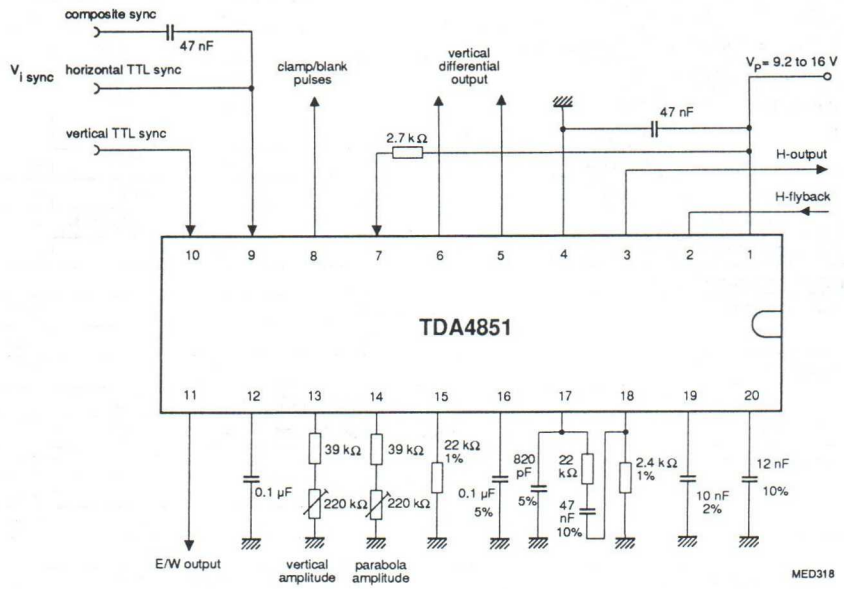


Fig.3 Application circuit for 3-mode VGA (31.45 kHz).

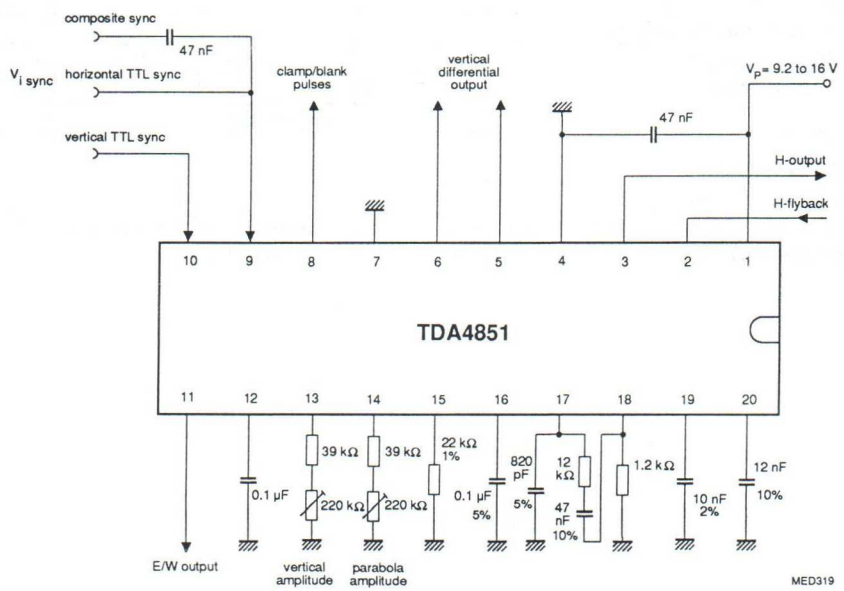


Fig.4 64 kHz application circuit.

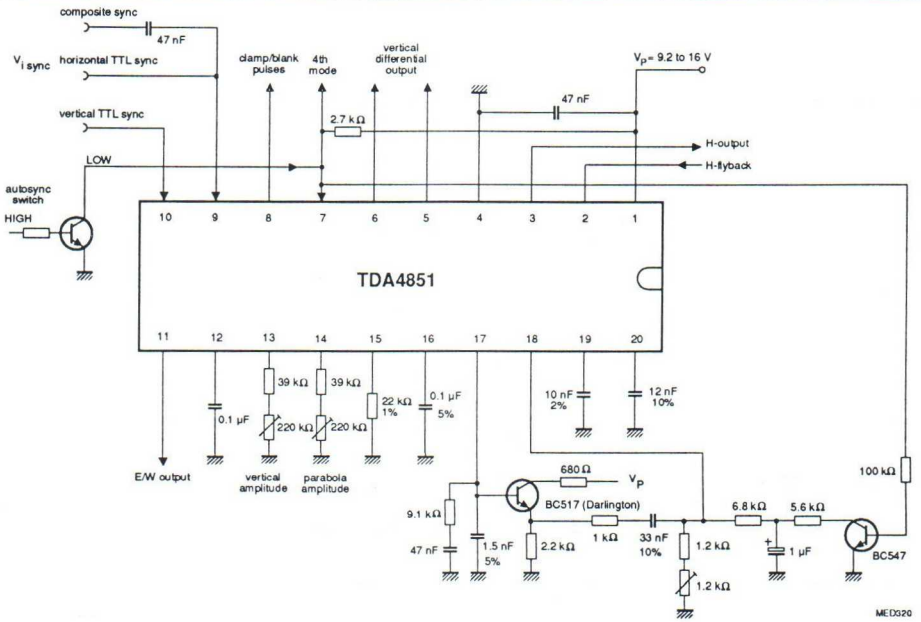


Fig.5 31 to 64 kHz application including 4-mode VGA.

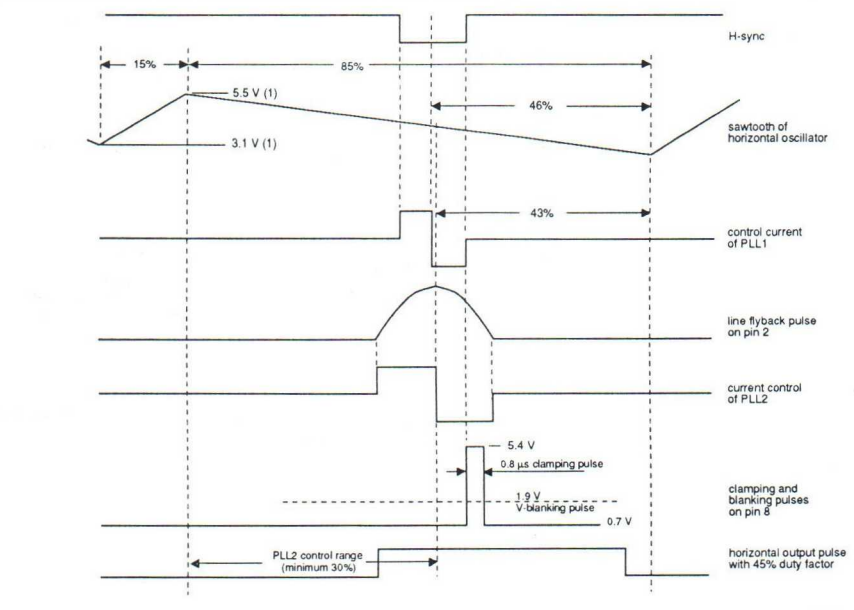


Fig.6 Horizontal timing diagram.

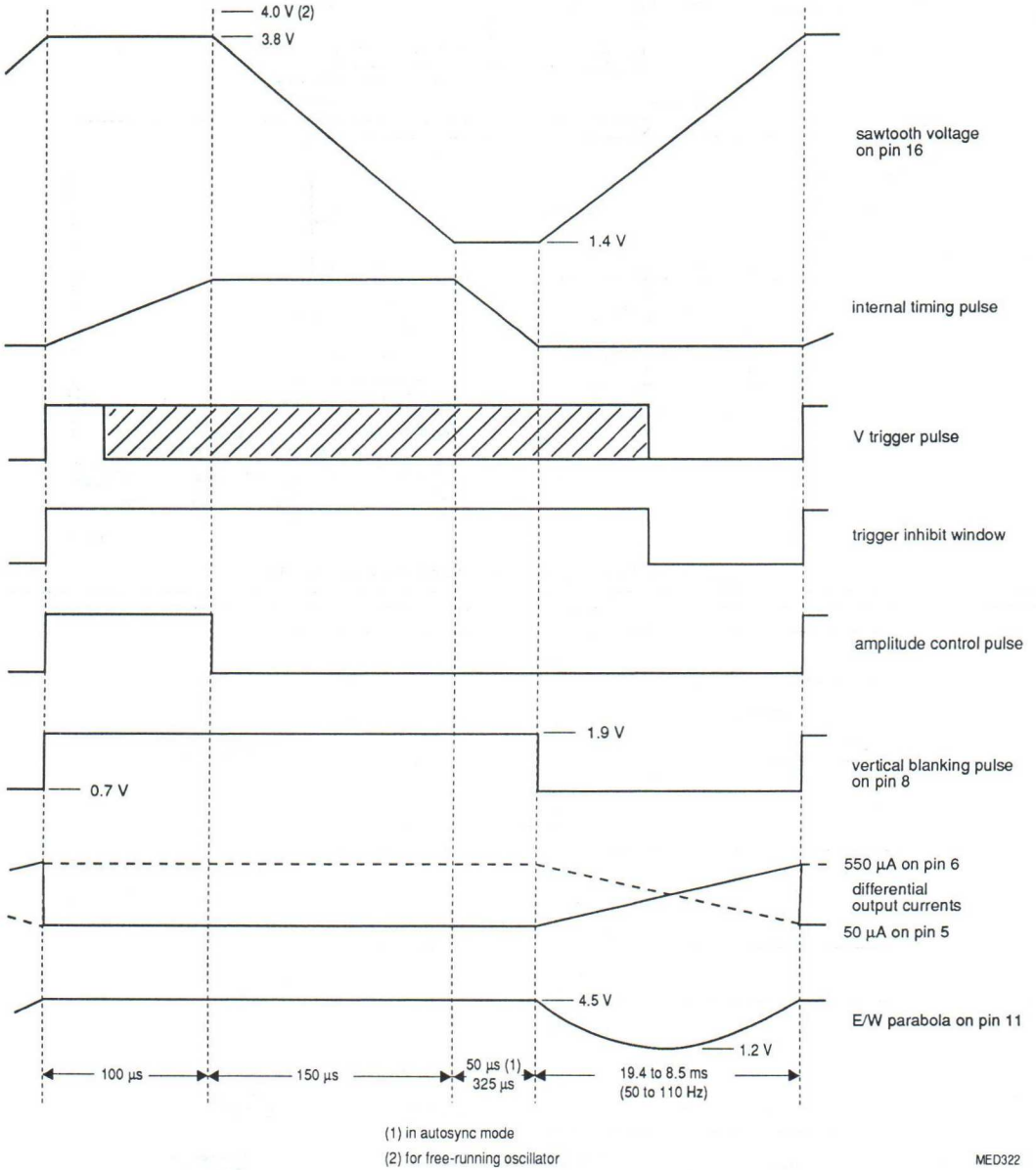
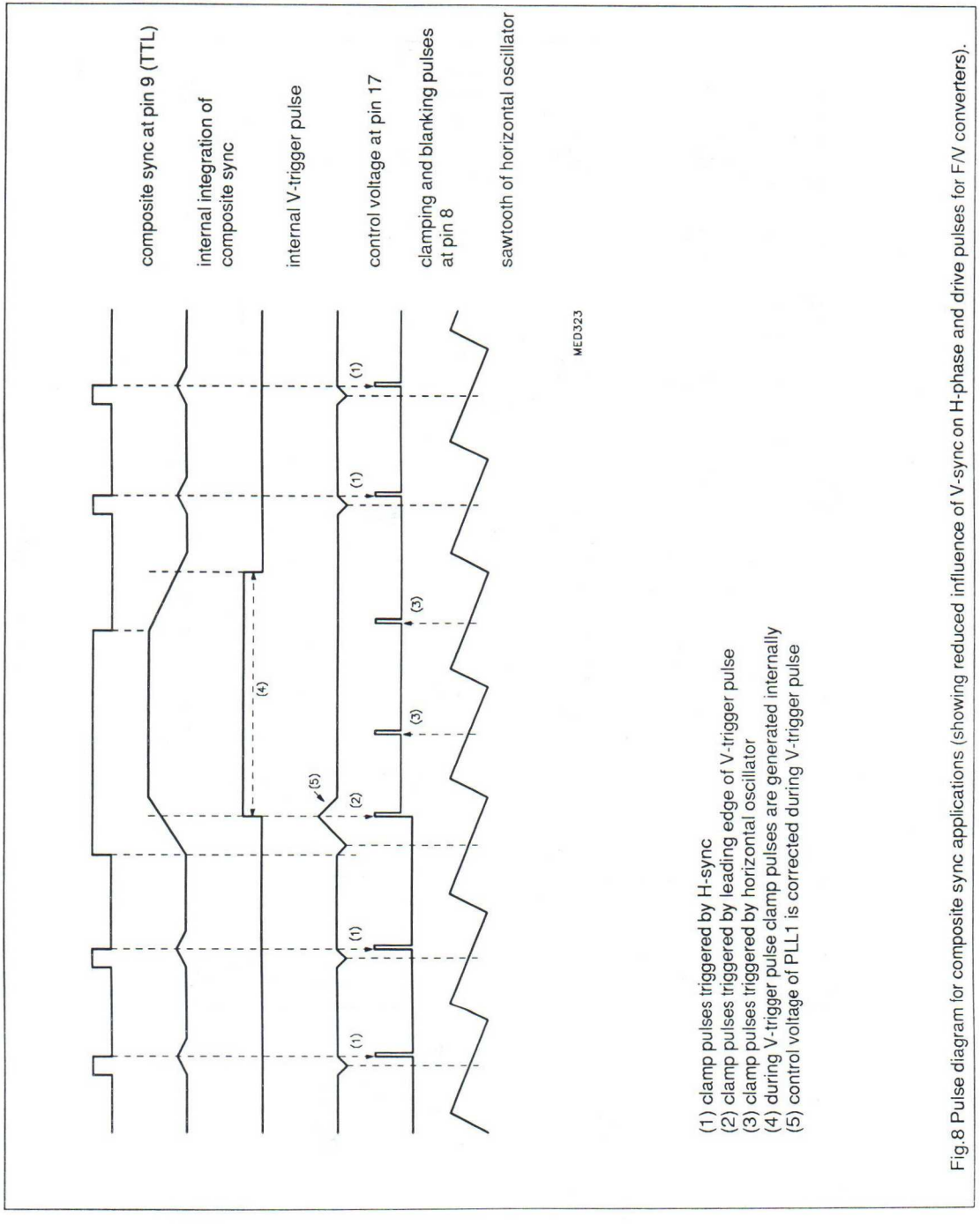


Fig.7 Vertical and E/W timing diagram.



(1) clamp pulses triggered by H-sync
(2) clamp pulses triggered by leading edge of V-trigger pulse
(3) clamp pulses triggered by horizontal oscillator
(4) during V-trigger pulse clamp pulses are generated internally
(5) control voltage of PLL1 is corrected during V-trigger pulse

Fig.8 Pulse diagram for composite sync applications (showing reduced influence of V-sync on H-phase and drive pulses for F/V converters).

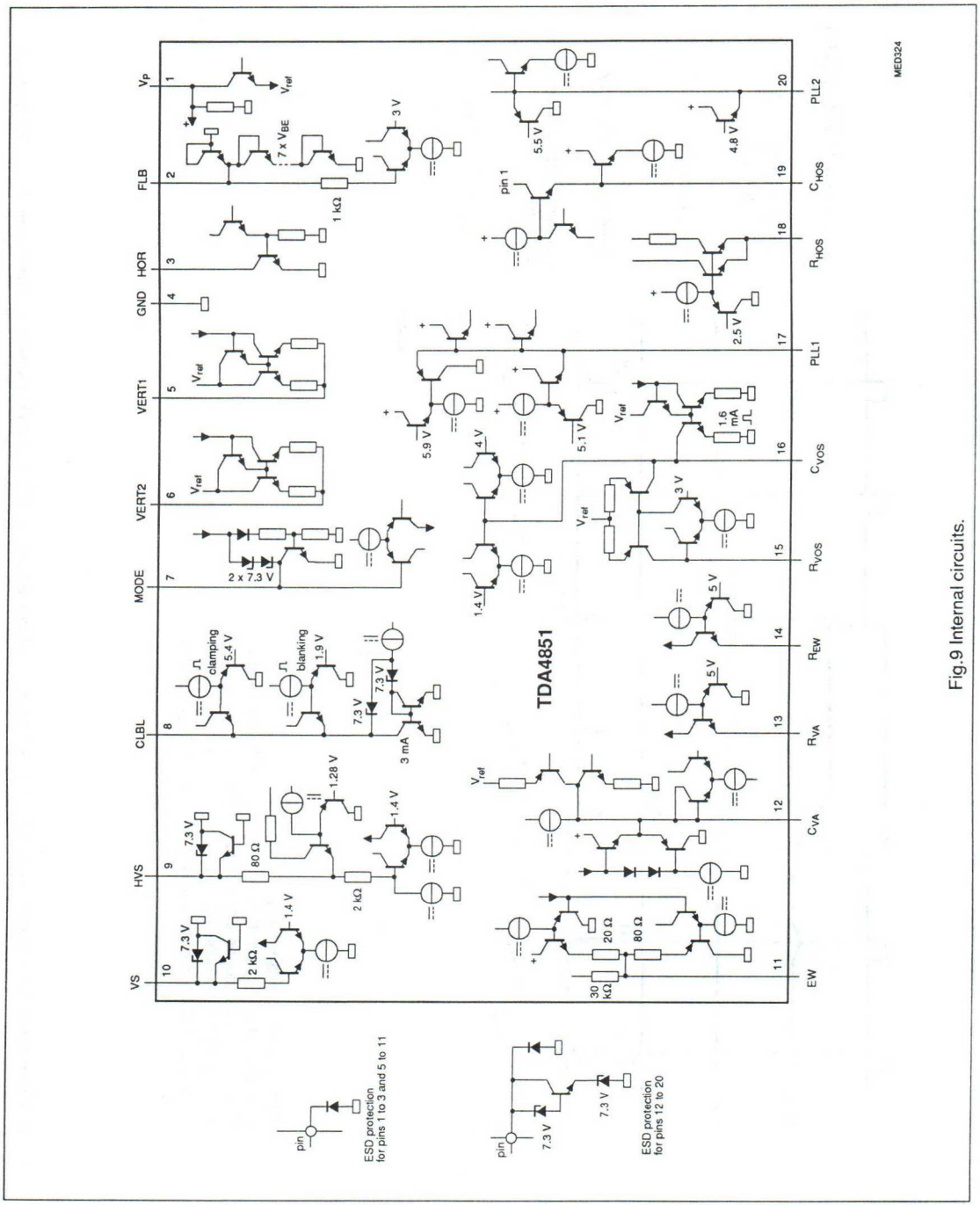


Fig.9 Internal circuits.

Horizontal and vertical deflection controller for autosync monitors

TDA4852

FEATURES

- Low jitter
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in autosync operation
- DC-coupling to vertical power amplifier
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	9.2	12	16	V
I_P	supply current	–	40	–	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value, pin 9)	–	1	–	V
	sync slicing level	–	120	–	mV
	DC-coupled TTL-compatible horizontal sync signal (peak-to-peak value, pin 9)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak-to-peak value, pin 10)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
$I_{o\ V}$	vertical differential output current (peak-to-peak value, pins 5 and 6)	–	1	–	mA
$I_{o\ H}$	horizontal sink output current on pin 3	–	–	60	mA
T_{amb}	operating ambient temperature range	0	–	+70	°C

GENERAL DESCRIPTION

The TDA4852 is a monolithic integrated circuit for economical solutions in autosync monitors. The IC incorporates the complete horizontal and vertical small signal processing. In conjunction with TDA4860/61/65, or TDA8351 (vertical output circuits) the ICs offer an extremely advanced system solution.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4852	20	DIL	plastic	SOT146

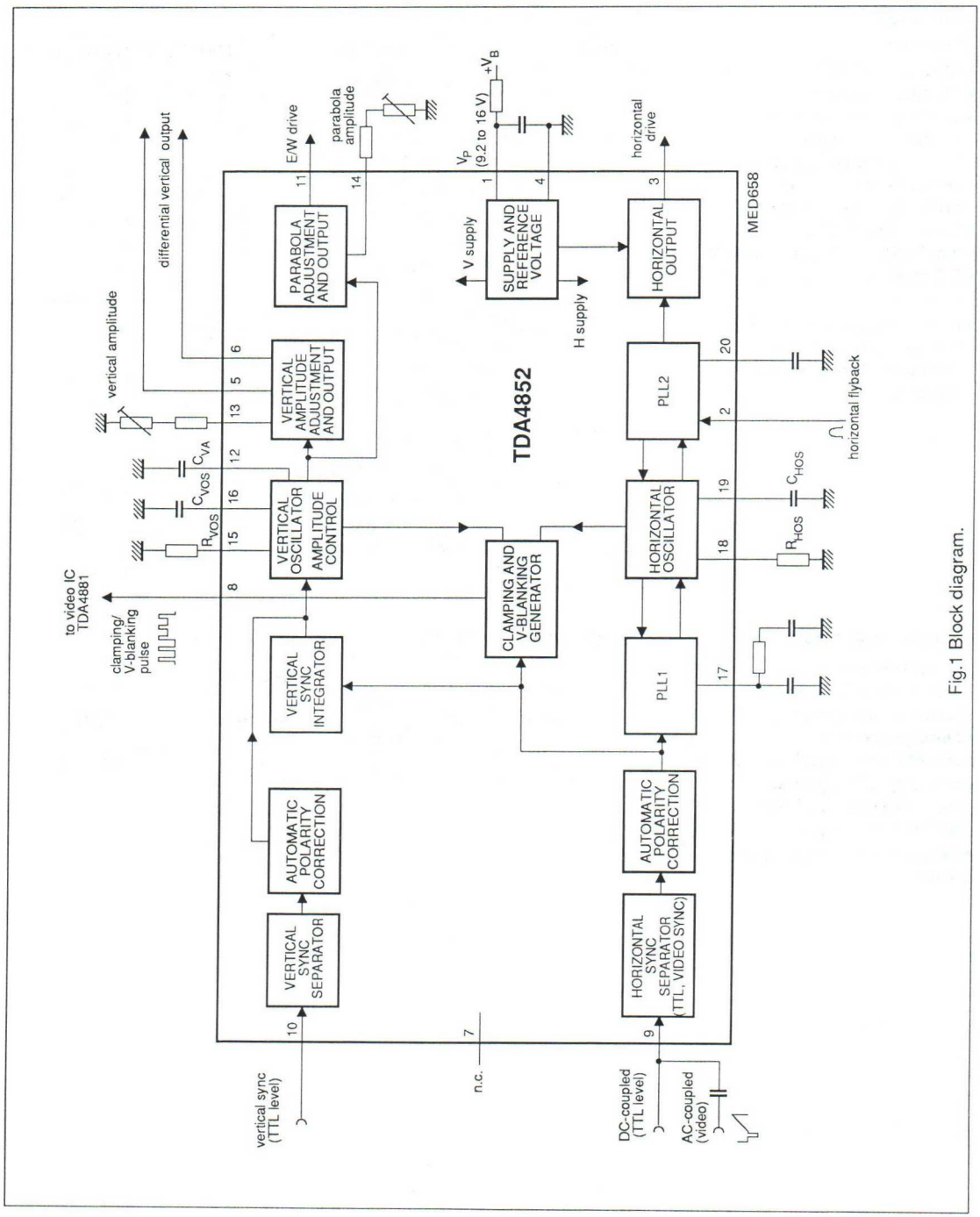


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
n.c.	7	not connected
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync/video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C_{VA}	12	capacitor for amplitude control
R_{VA}	13	vertical amplitude adjustment input
R_{EW}	14	E/W amplitude adjustment input (parabola)
R_{VOS}	15	vertical oscillator resistor
C_{VOS}	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R_{HOS}	18	horizontal oscillator resistor
C_{HOS}	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase

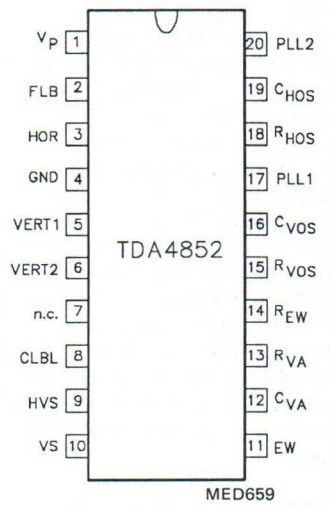


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.
DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then the polarity is corrected. If pin 10 is not used, it must be connected to ground.
The separated $V_{i\ sync}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

Clamping and V-blanking generator

A combined clamping and V-blanking pulse is available on pin 8 (suitable for the video pre-amplifier TDA4881). The lower level of 1.9 V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator.
Vertical blanking starts with vertical sync and stops at the begin of vertical scan. By this, an optimum blanking is achieved.

The upper level of 5.4 V is the horizontal clamping pulse with an internally fixed pulse width of 0.8 µs. A monoflop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse.
If composite sync is applied, one clamping pulse per H-period is generated during V-sync. The phase of the clamping pulse may change during V-sync (see Fig.8).

PLL1 phase detector

The phase detector is a standard type using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17. If composite sync is applied, the disturbed control voltage is corrected during V-sync (see Fig.8).

Horizontal oscillator

This oscillator is of the relaxation type and requires a fixed capacitor of 10 nF at pin 19. By changing the current into pin 18 the whole frequency range from 13 to 100 kHz can be covered.
The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary.
The PLL1 control voltage at pin 17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustment is possible by injecting a DC current from an external source into the PLL2 filter capacitor at pin 20.

Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is less than 300 mV at 20 mA.
To protect the line deflection transistor, the horizontal output stage does not conduct for $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions. The free-running frequency f_0 is determined by the values of R_{VOS} and C_{VOS}. The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS}. Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_0 = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_0 (without adjustment) must be lower than the lowest occuring sync frequency. The following contributions can be assumed:

minimum frequency offset between f_0 and the lowest trigger frequency	10%
spread of IC	±3%
spread of R (22 kΩ)	±1%
spread of C (0.1 µF)	±5%
	19%

Result: $f_0 = \frac{50}{1.19}$ Hz = 42 Hz

(for 50 to 110 Hz application)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.5	16	V
V_3	voltage on pin 3	–0.5	16	V
V_8	voltage on pin 8	–0.5	7	V
V_n	voltage on pins 5, 6, 9, 10, 13, 14 and 18	–0.5	6.5	V
I_2	current on pin 2	–	±10	mA
I_3	current on pin 3	–	100	mA
I_8	current on pin 8	–	–10	mA
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	70	°C
T_j	maximum junction temperature	0	+150	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±400	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = +25 °C; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		9.2	12	16	V
I_P	supply current	I_{18} = –1.05 mA	–	36	44	mA
		I_{18} = –3.388 mA	–	40	49	mA
Internal reference voltage						
V_{ref}	internal reference voltage		6.0	6.25	6.5	V
TC	temperature coefficient	T_{amb} = +20 to +100 °C	–	–	±90	10^{-6}/K
PSRR	power supply ripple rejection	f = 1 kHz sinewave	60	75	–	dB
		f = 1 MHz sinewave	25	35	–	dB
V_P	supply voltage (pin 1) to ensure all internal reference voltages		9.2	–	16	V
Composite sync input (AC-coupled)		V_{10} = 5 V				
$V_{i\ sync}$	sync amplitude of video input signal (pin 9)	sync on green	–	300	–	mV
	top sync clamping level		1.1	1.28	1.5	V
	slicing level above top sync level	R_S = 50 Ω	90	120	150	mV
R_S	allowed source resistance for 7% duty factor	$V_{i\ sync}$ > 200 mV	–	–	1.5	kΩ
r_9	differential input resistance	during sync	–	80	–	Ω
I_9	charging current of coupling capacitor	V_9 > 1.5 V	1.3	2	3	µA
t_{int}	vertical sync integration time to generate vertical trigger pulse	f_H = 31 kHz; I_{18} = –1.050 mA	7	10	13	µs
		f_H = 64 kHz; I_{18} = –2.169 mA	3.5	5	6.5	µs
		f_H = 100 kHz; I_{18} = –3.388 mA	2.5	3.4	4.5	µs
Horizontal sync input (DC-coupled, TTL-compatible)						
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 9)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
t_p	minimum pulse width		700	–	–	ns
t_r, t_f	rise time and fall time		10	–	500	ns
I_9	input current	V_9 = 0.8 V	–	–	–200	µA
		V_9 = 5.5 V	–	–	10	µA
Automatic horizontal polarity switch		H-sync on pin 9				
$t_{p\ H}/t_H$	horizontal sync pulse width related to t_H (duty factor for automatic polarity correction)		–	–	30	%
t_p	delay time for changing sync polarity		0.3	–	1.8	ms

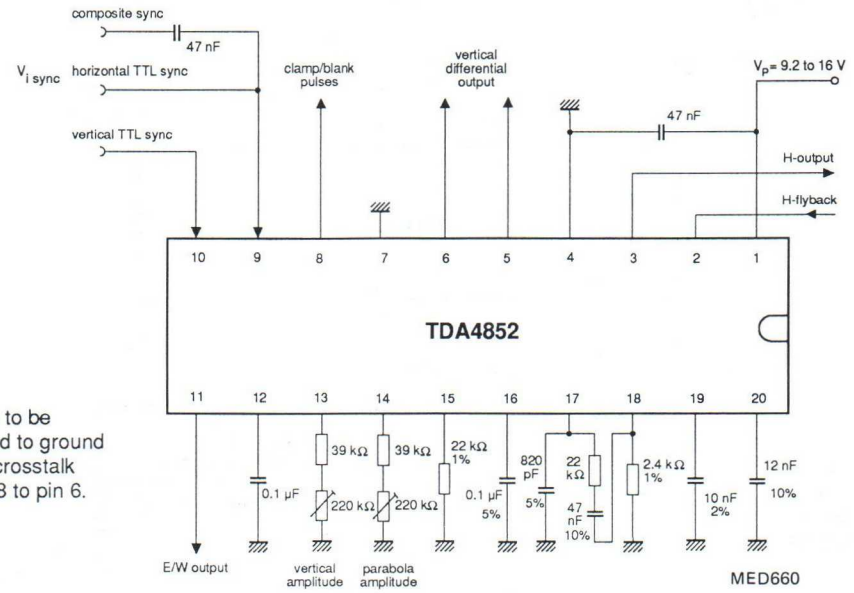
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sync input (DC-coupled, TTL-compatible)		V-sync on pin 10				
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 10)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
I_{10}	input current	$0 < V_{10} < 5.5$ V	–	–	±10	µA
$t_{p\ V}$	maximum vertical sync pulse width for automatic vertical polarity switch		–	–	300	µs
Horizontal clamping / blanking generator output		Fig.6				
V_8	output voltage LOW		–	–	0.9	V
	blanking output voltage	internal V blanking	1.6	1.9	2.2	V
	clamping output voltage	H-sync on pin 9	5.15	5.4	5.65	V
I_8	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
	external load current		–	–	–3.0	mA
t_8	clamping pulse start		with end of H-sync			
t_{clp}	clamping pulse width	$V_8 = 3$ V	0.6	0.8	1.0	µs
S	steepness of rise and fall times		–	60	75	ns/V
Vertical oscillator		$V_{ref} = 6.25$ V				
f_0	vertical free-running frequency	$R_{15} = 22$ kΩ; $C_{16} = 0.1$ µF	–	42	–	Hz
f_V	nominal vertical sync range	no f_0 adjustment	50	–	110	Hz
V_{15}	voltage on pin 15	$R_{15} = 22$ kΩ	2.8	3.0	3.2	V
t_d	delay between sync pulse and start of vertical scan	measured on pin 8	240	300	360	µs
I_{12}	control current for amplitude control		–	±200	–	µA
C_{12}	capacitor for amplitude control		–	–	0.18	µF
Vertical differential output		Fig.7				
I_o	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; $I_{13} > -135$ µA; $R_{15} = 22$ kΩ	0.9	1.0	1.1	mA
	maximum offset-current error	$I_o = 1$ mA	–	–	±2.5	%
	maximum linearity error		–	–	±1.5	%
Vertical amplitude adjustment (in percentage of output signal)						
V_{13}	input voltage		–	5.0	–	V
I_{13}	adjustment current	$I_{o\ max}$ (100%)	–110	–120	–135	µA
		$I_{o\ min}$ (typically 58%)	–	0	–	µA
Horizontal comparator PLL1						
V_{17}	upper control voltage limitation		–	5.9	–	V
	lower control voltage limitation		–	5.1	–	V
I_{17}	control current	Fig.6	–	$\pm 0.083 I_{18}$	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal oscillator						
f_{osc}	centre frequency	R_{18} = 2.4 kΩ (pin 18); C_{19} = 10 nF (pin 19)	–	31.45	–	kHz
	deviation of centre frequency		–	–	±3	%
	temperature coefficient		0	+200	+300	10^{-6}/K
φ_H/t_H	relative holding/catching range		±6	±6.5	±7.3	%
I_{18}	external oscillator current		–0.5	–	–4.3	mA
V_{18}	voltage at reference current input (pin 18)		2.35	2.5	2.65	V
Horizontal PLL2		Fig.6				
V_2	upper clamping level of flyback input	I_2 = 6 mA	–	5.5	–	V
	lower clamping level of flyback input	I_2 = –1 mA	–	–0.75	–	V
	H-flyback slicing level		–	3.0	–	V
t_d/t_H	delay between middle of sync and middle of H-flyback related to t_H		–	3.0	–	%
V_{20}	upper control voltage limitation		–	6.2	–	V
	lower control voltage limitation		–	4.8	–	V
I_{20}	control current		–	$\pm 0.083 I_{18}$	–	µA
$\Delta t/t_H$	PLL2 control range related to t_H		30	–	–	%
Horizontal output (open-collector)		Fig.6				
V_3	output voltage LOW	I_3 = 20 mA	–	–	0.3	V
		I_3 = 60 mA	–	–	0.8	V
t_p/t_H	t_H duty factor		42	45	48	%
V_P	threshold to activate under voltage protection	horizontal output off	–	5.6	–	V
		horizontal output on	–	5.8	–	V
Δt_H	jitter of horizontal output	f = 31 kHz	–	–	3.5	ns
		f = 64 kHz	–	–	1.9	ns
		f = 100 kHz	–	–	1.2	ns
E/W output		note 1				
V_{11}	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.2	4.5	4.8	V
	temperature coefficient of output signal		–	–	250	10^{-6}/K
E/W amplitude adjustment (parabola)		Fig.7				
V_{14}	input voltage (pin 14)		–	5.0	–	V
I_{14}	adjustment current	100% parabola	–110	–120	–135	µA
		typically 28% parabola	–	0	–	µA

Note to the characteristics

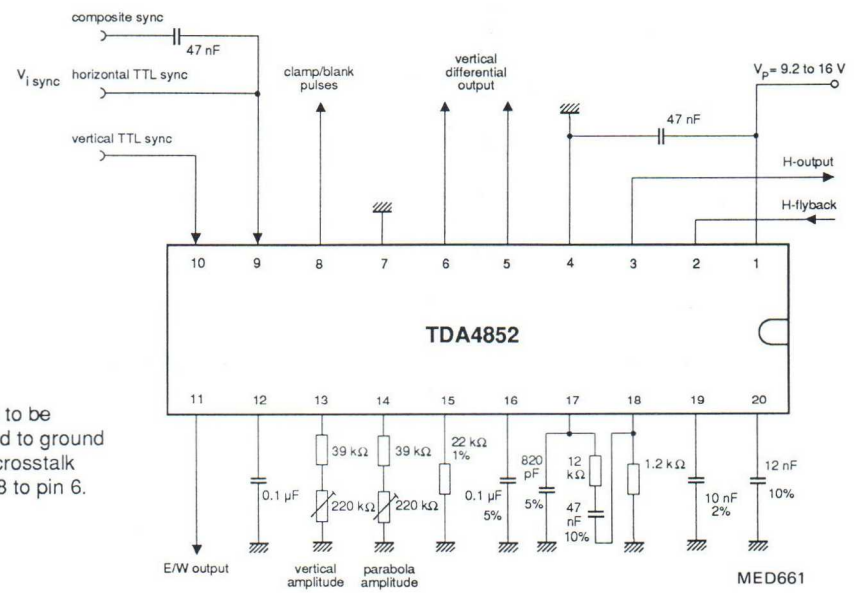
1. Parabola amplitude does not track with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.

APPLICATION INFORMATION



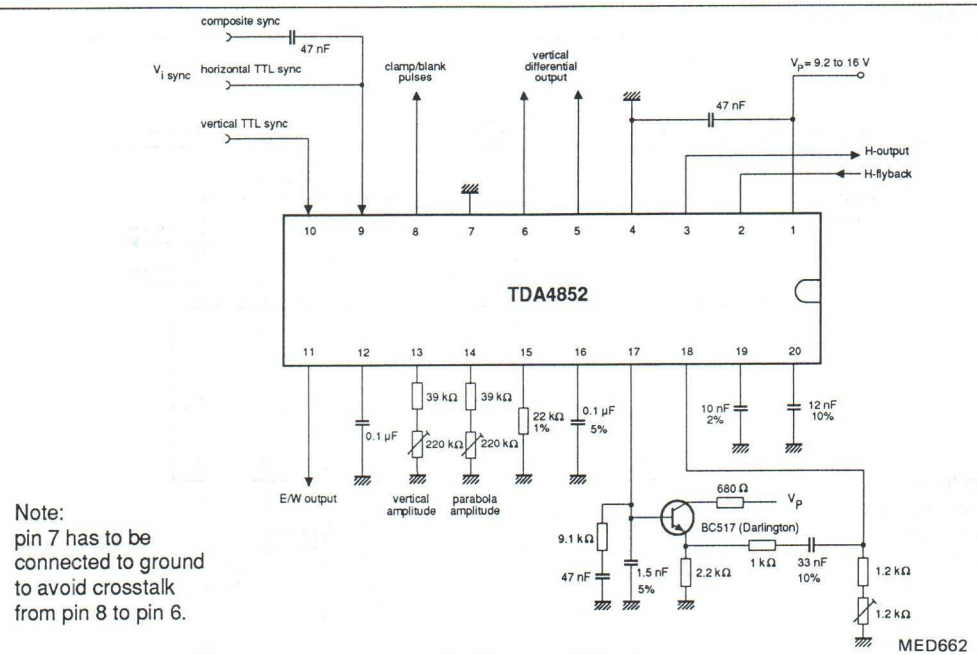
Note:
pin 7 has to be connected to ground to avoid crosstalk from pin 8 to pin 6.

Fig.3 Application circuit for 31.45 kHz.



Note:
pin 7 has to be connected to ground to avoid crosstalk from pin 8 to pin 6.

Fig.4 Application circuit for 64 kHz.



Note:
pin 7 has to be connected to ground to avoid crosstalk from pin 8 to pin 6.

Fig.5 Application circuit for 31 to 64 kHz.

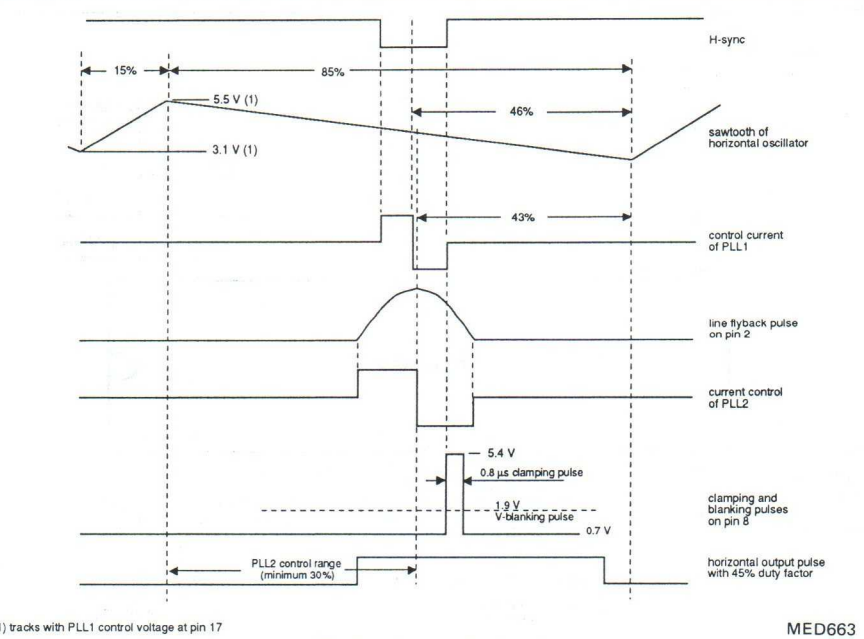


Fig.6 Horizontal timing diagram.

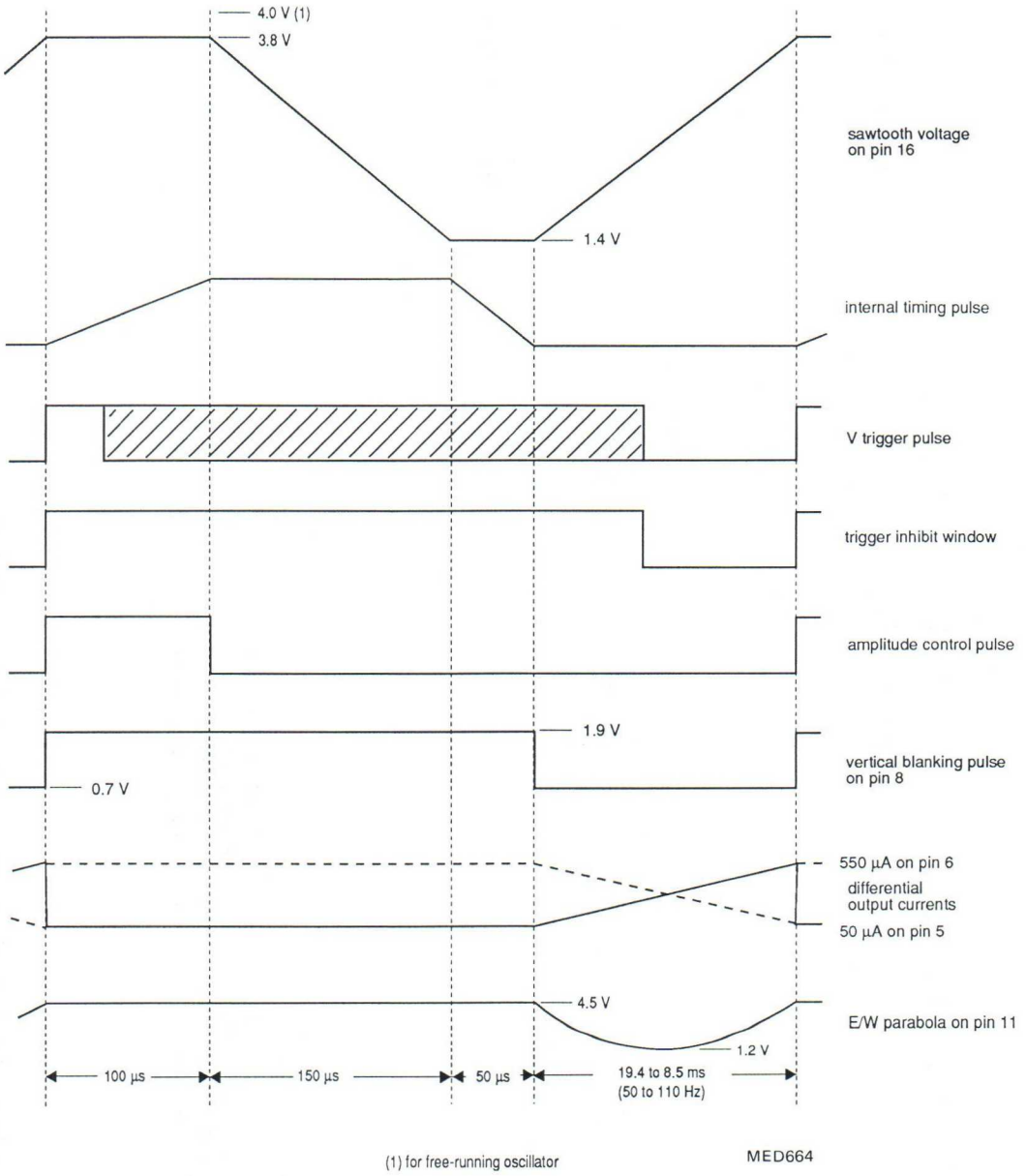
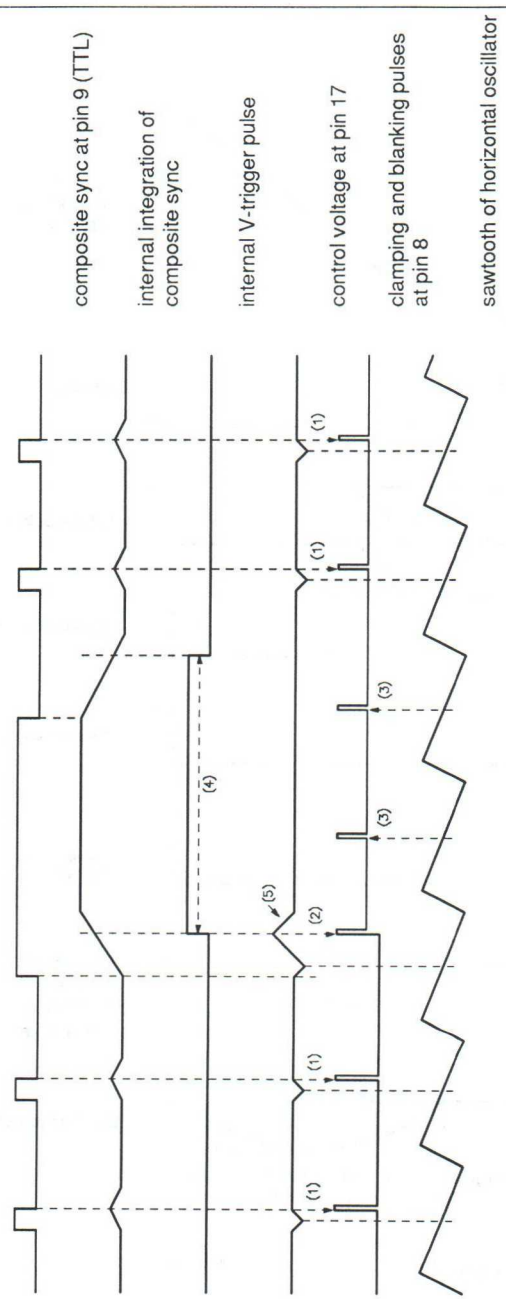


Fig.7 Vertical and E/W timing diagram.



(1) clamp pulses triggered by H-sync
(2) clamp pulses triggered by leading edge of V-trigger pulse
(3) clamp pulses triggered by horizontal oscillator
(4) during V-trigger pulse clamp pulses are generated internally
(5) control voltage of PLL1 is corrected during V-trigger pulse

Fig.8 Pulse diagram for composite sync applications (showing reduced influence of V-sync on H-phase and drive pulses for F/V converters).

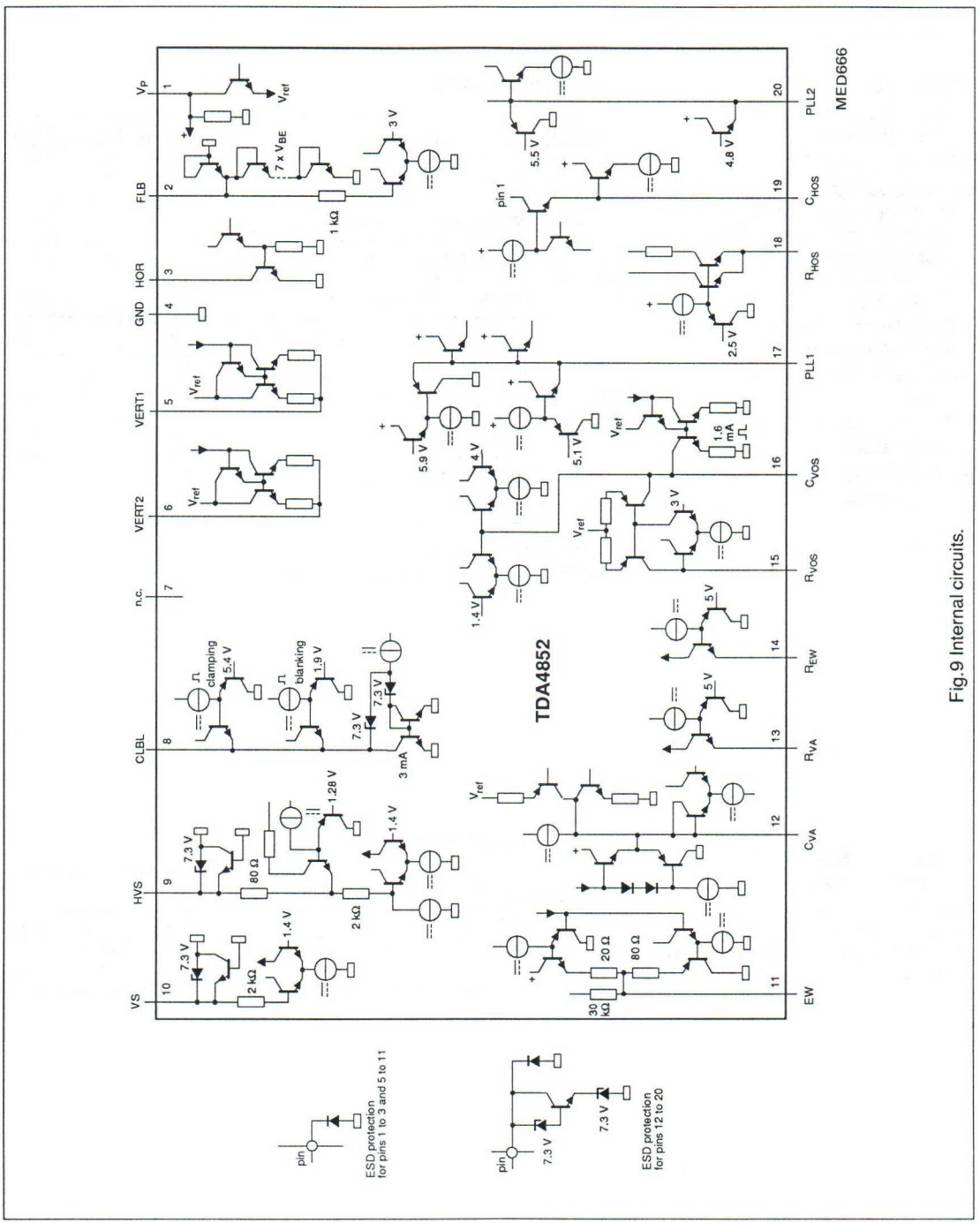


Fig.9 Internal circuits.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	September 1991

TDA4860

Vertical deflection power amplifier for monitors

FEATURES

- Vertical pre-amplifier with differential inputs
- Powerless vertical shift
- Flyback voltage generation suitable for two operating modes (doubling the supply voltage or external supply for the short flyback time, this achieves a minimum of power dissipation)
- Vertical output stage with thermal and SOAR protection
- High deflection frequency up to 140 Hz
- High linear sawtooth signal amplification
- Possibility of guarding the deflection
- Voltage stabilizer

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{P1} = V_1$	positive supply voltage (pin 1)	9	-	30	V
$V_{P2} = V_4$	positive supply voltage (pin 4)	9	-	60	V
$V_{P3} = V_8$	flyback supply voltage (pin 8)	9	-	60	V
I_{P1}	supply current (pin 1)	-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	-	9	-	mA
V_I	input voltage range (pins 2 and 3)	1.6		V_{P1}-0.5	V
$\pm I_{5\,M}$	deflection output current (maximum value, pin 5)	-	-	±1	A
T_{amb}	operating ambient temperature range	–20	-	+75	°C

Note to quick reference data
Measurements referenced to substrate (pin 6).

GENERAL DESCRIPTION

The TDA4860 is a vertical power amplifier for differential input signals suitable for colour monitor/TV systems with deflection frequency up to 140 Hz.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4860	9	SIL	plastic	SOT110

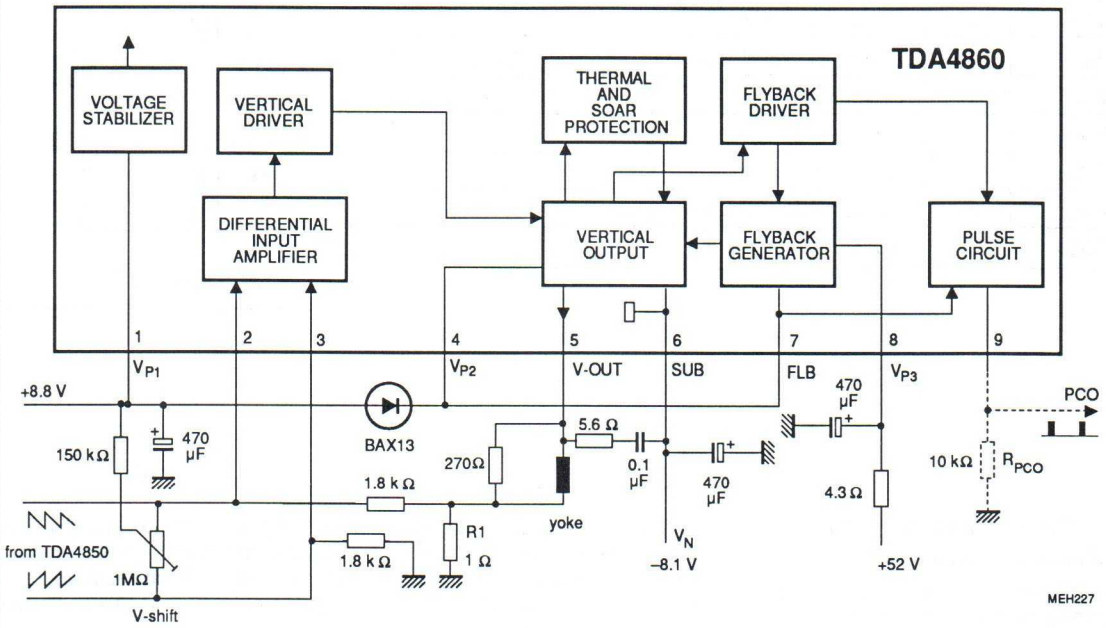


Fig.1 Block diagram and application circuit with flyback supply voltage V_{P3} from an external source. Deflection frequency range from 50 Hz up to 100 Hz.

Notes to Fig.1

Assumed values

I_{yoke}	=	1.42 A
R_{yoke}	=	4.17 Ω + 7% + ΔR(T) = 6.12 Ω
L_{yoke}	=	5.25 mH
R_1	=	1.0 Ω ±1%
T_{amb}	=	65 °C
$T_{j\,max}$	=	105 °C
T_{yoke}	=	75 °C
P_{yoke}	=	1.2 W
P_{IC}	=	1.8 W
P_{tot}	=	3.0 W
$t_{p\,FLB}$	=	typically 250 µs

Attention: the heatsink of the IC must be isolated against ground; the cooling fin is connected to pin 6.

Vertical deflection power amplifier for monitors

TDA4860

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
INP1	2	input 1 of differential input amplifier
INP2	3	input 2 of differential input amplifier
V_{P2}	4	positive supply voltage 2 for vertical output stage
V-OUT	5	vertical output
SUB	6	substrate
FLB	7	flyback generator output
V_{P3}	8	positive flyback supply voltage 3
PCO	9	pulse circuit output

PIN CONFIGURATION

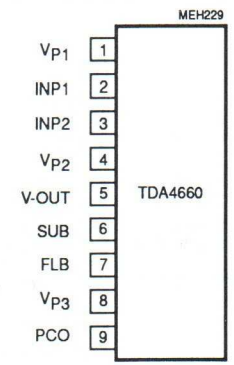


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Differential input amplifier

The differential sawtooth input signal (coming from ramp output of the TDA 4850 for example) is fed to the input pins 2 and 3. The non-inverted signal is attached to pin 3. The vertical feedback signal is superimposed to the inverted input signal on pin 2.

Vertical shift is applied at the inputs in a power-less way (Fig.1).

Flyback generator

Signals for the flyback generator and the pulse circuit are composed in the flyback driver stage.The flyback output consists of a Darlington transistor and a flyback diode. The flyback generator can operate in two modes:

- a supply voltage from external is applied for the short flyback time, thus the power dissipation is a minimum (Fig.1).
- the flyback voltage is generated by doubling the supply voltage (Fig.5). The 100 µF capacitor C2 between pins 4 and 7 is charged up to V_{P1} during scan, using the external diode and the resistor R2. The cathode of the capacitor C2 is connected to the positive rail during flyback. Thus, the flyback voltage is double the supply voltage.

Vertical output

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity. The output contains SOAR (short-circuit protection) and thermal protection. The output current on pin 5 is reduced for a short time (to let the temperature decrease to T_j <150 °C), when the junction temperature T_j exceeds 160 °C.

Deflection guard

Pin 9 goes to HIGH in case of too high junction temperature (Fig.3).

A pulse signal with 50% duty cycle is output on pin 9, if the deflection coil is open-circuit . A flyback pulse signal is output at normal condition.

Further watching can be achieved by means of an external guard circuit as shown in Fig.4. The 22 µF capacitor is charged during flyback time ($V_5 > V_8$) at normal condition.

In case of failures, the capacitor is discharged – the guard output becomes HIGH.

Guard output level (Fig.4):

- LOW for normal condition
- HIGH for deflection coil short-circuit respectively open-circuit
- HIGH when there are neither input nor output signals.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134);
voltages referenced to substrate (pin 6).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	-	40	V
V_{P2}	positive supply voltage (pin 4)	-	60	V
V_{P3}	positive supply voltage (pin 8)	-	60	V
$V_{2,3,9}$	voltage on pins 2, 3, and 9	-	V_{P1}	V
$V_{5,7}$	voltage on pins 5 and 7	-	60	V
I_4	current on pin 4	-	1	A
$I_{5\,(M)}$	output current* on pin 5 (peak value)	-	±1.3	A
$I_{7(M)}$	flyback current on pin 7 (peak value)	-	±1.3	A
I_9	current on pin 9	-	–8	mA
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	–20	+75	°C
T_j	junction temperature*	-	+168	°C
V_{ESD}	electrostatic handling** for all pins	-	±300	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction-to-case	-	10	K/W

The heatsink can be estimated according to application circuit Fig.1.

$R_{th\ j\text{-}a} = R_{th\ j\text{-}c} + R_{th\ c\text{-}h} + R_{th\ h\text{-}a} = (T_{j\ max} - T_{amb}) / P_{IC\ max} = (105 - 65)\ °C / 1.8\ W = 22.2\ K/W.$

A heatsink is needed at $R_{th\ j\text{-}c} < 10$ K/W and $R_{th\ c\text{-}h} = 0.5$ K/W (using silicon grease) with

$R_{th\ h\text{-}a} = 22.2\ K/W - (10 + 0.5)\ K/W = \underline{11.7\ K/W}$

* Internally limited by thermal protection; switching temperature point at 160 ±8 °C.

** Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor

CHARACTERISTICS

$V_{P1} = V_{P2} = 25$ V; $V_N = V_6 = 0$ V; $T_{amb} = 25$ °C and voltages referenced to substrate (pin 6) unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage 1 range (pin 1)		9	25	30	V
V_{P2}	positive supply voltage 2 range (pin 4)		9	25	60	V
V_{P3}	positive supply voltage 3 range (pin 8)		9	-	60	V
I_{P1}	supply current (pin 1)		-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	without input signal	-	9	-	mA
Pre-amplifier						
$V_{2,3}$	input voltage range (pins 2 and 3)		1.6	-	V_{P1}-0.5	V
$I_{2,3}$	input quiescent current	without input signal	-	100	-	nA
Flyback generator						
V_7	output voltage	upper value; $I_7 = -1$ A	-	V_{P3}-2.2	-	V
$I_{7\,(M)}$	flyback output current (maximum value, pin 7)	-		-	±1	A
V_{1-5}	threshold voltage to switch flyback	on/off threshold	-	1.4	-	V
$t_{p\,FLB}$	flyback pulse time	Fig.1; Fig.3	-	250	-	µs
Vertical output		Fig.3				
V_5	output voltage	upper value; $I_5 = -1$ A	V_{P2}-2.3	V_{P2}-2	-	V
		lower value; $I_5 = 1$ A	-	1.5	1.7	V
$I_{5\,(M)}$	vertical output current (maximum value, pin 5)		-	±1	A	
LIN	non-linearity of output signal		-	-	1	%
Pulse circuit output		Fig.3				
V_9	output voltage range	$R_{PCO} = 10$ kΩ; Fig.1	0.4	-	V_{P1}-0.4	V
	output voltage for thermal protection active		V_{P1}-0.4	-	-	V
V_{1-5}	voltage to insert flyback pulse on pin 9	normal condition	-	-	1.4	V
$t_{p\,9}$	pulse width	deflection open-circuit	-	50	-	%
		normal condition	$t_{p\,FLB}$	-	-	µs

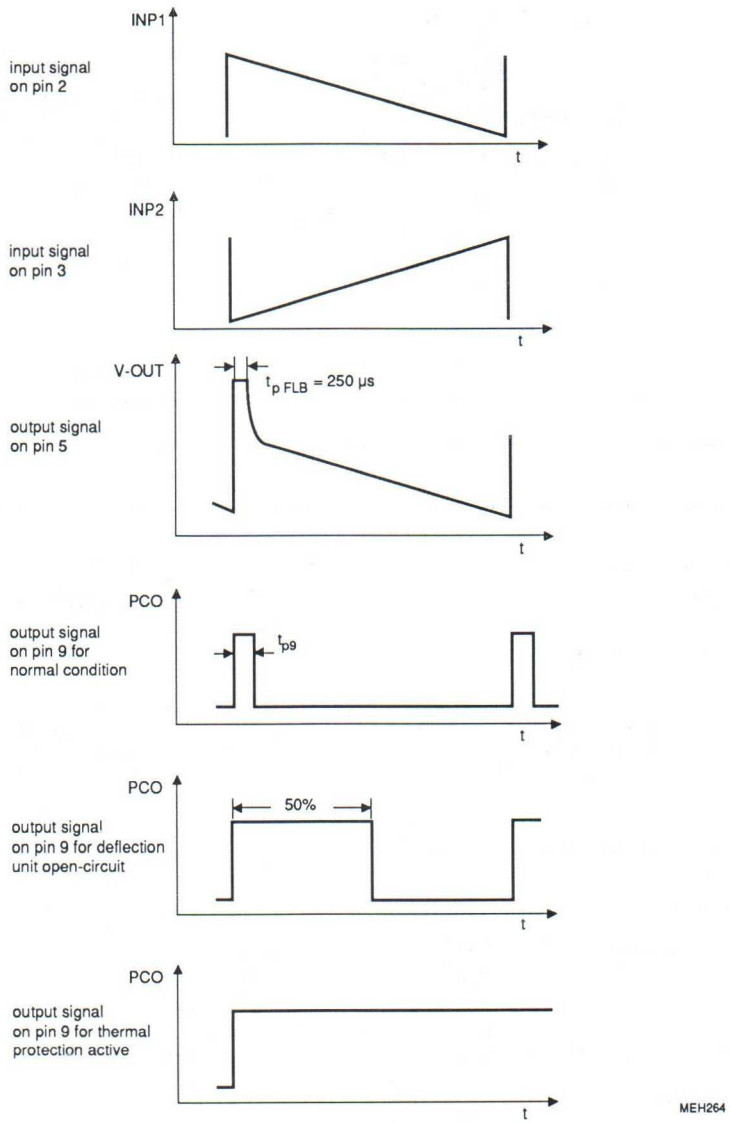


Fig.3 Vertical timing.

APPLICATION INFORMATION

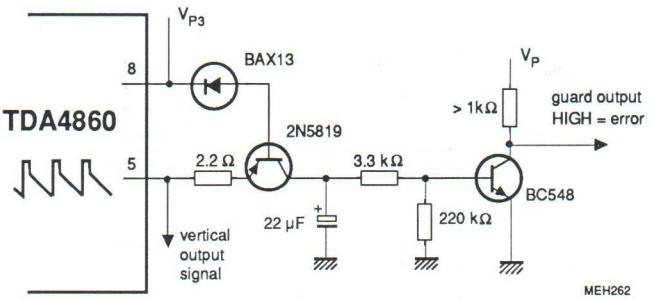


Fig.4 Guard circuit application on vertical output.

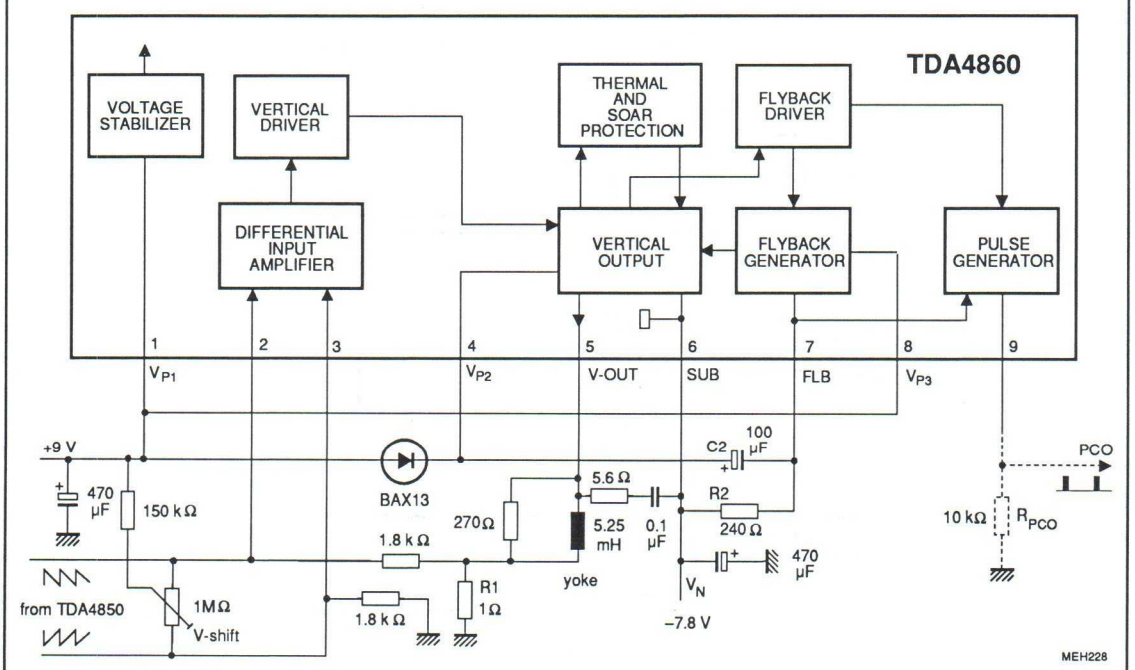


Fig.5 Application for flyback voltage generation by doubling the supply voltage.

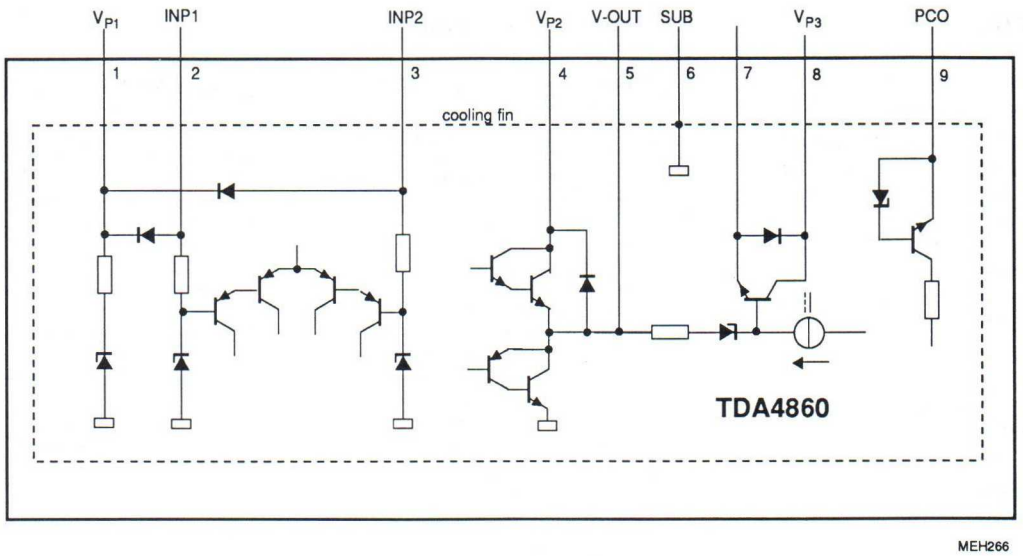


Fig.6 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1992

TDA4861

Vertical deflection power amplifier for monitors

FEATURES

- Vertical pre-amplifier with differential inputs
- Powerless vertical shift
- Flyback voltage generation suitable for two operating modes (doubling the supply voltage or external supply for the short flyback time, this achieves a minimum of power dissipation)
- Vertical output stage with thermal and SOAR protection
- High deflection frequency up to 140 Hz
- High linear sawtooth signal amplification
- Possibility of guarding the deflection
- Voltage stabilizer

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	9	-	30	V
V_{P2}	positive supply voltage (pin 4)	9	-	60	V
V_{P3}	flyback supply voltage (pin 8)	9	-	60	V
I_{P1}	supply current (pin 1)	-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	-	9	-	mA
V_I	input voltage range (pins 2 and 3)	1.6		V_{P1}-0.5	V
I_5	deflection output current (peak-to-peak value, pin 5)	-	-	2.8	A
T_{amb}	operating ambient temperature range	–20	-	75	°C

Note to quick reference data

Measurements referenced to substrate (pin 6).

GENERAL DESCRIPTION

The TDA4861 is a vertical power amplifier for differential input signals suitable for colour monitor/TV systems with deflection frequency up to 140 Hz.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4861	9	SIL	plastic	SOT131

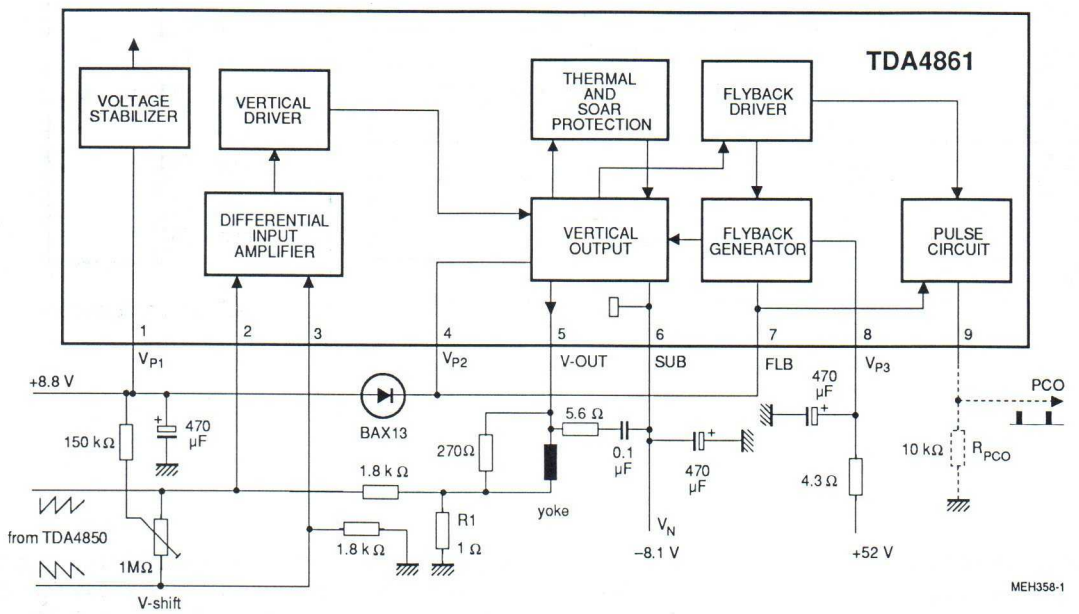


Fig.1 Block diagram and application circuit with flyback supply voltage V_{P3} from an external source. Deflection frequency range from 50 Hz up to 100 Hz.

Notes to Fig.1

Assumed values

I_{yoke}	=	1.42 A	P_{yoke}	=	1.2 W
R_{yoke}	=	4.17 Ω + 7% + ΔR(T) = 6.12 Ω	P_{IC}	=	1.8 W
L_{yoke}	=	5.25 mH	P_{tot}	=	3.0 W
R_1	=	1.0 Ω ±1%	$t_{p\ FLB}$	=	typically 250 µs
T_{amb}	=	65 °C			
$T_{j\ max}$	=	105 °C			
T_{yoke}	=	75 °C			

Attention: the heatsink of the IC must be isolated against ground (it is connected to pin 6).

Vertical deflection power amplifier for monitors

TDA4861

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
INP1	2	input 1 of differential input amplifier
INP2	3	input 2 of differential input amplifier
V_{P2}	4	positive supply voltage 2 for vertical output stage
V-OUT	5	vertical output
SUB	6	substrate
FLB	7	flyback generator output
V_{P3}	8	positive flyback supply voltage 3
PCO	9	pulse circuit output

PIN CONFIGURATION

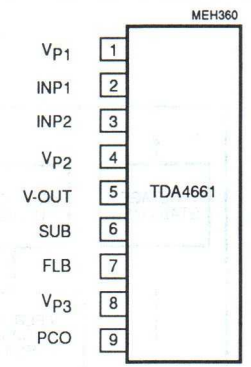


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Differential input amplifier

The differential sawtooth input signal (coming from ramp output of the TDA 4850 for example) is fed to the input pins 2 and 3. The non-inverted signal is attached to pin 3. The vertical feedback signal is superimposed to the inverted input signal on pin 2.

Vertical shift is applied at the inputs in a power-less way (Fig.1).

Flyback generator

Signals for the flyback generator and the pulse circuit are composed in the flyback driver stage.The flyback output consists of a Darlington transistor and a flyback diode. The flyback generator can operate in two modes:

- a supply voltage from external is applied for the short flyback time, thus the power dissipation is a minimum (Fig.1).
- the flyback voltage is generated by doubling the supply voltage (Fig.5). The 100 µF capacitor C2 between pins 4 and 7 is charged up to V_{P1} during scan, using the external diode and the resistor R2. The cathode of the capacitor C2 is connected to the positive rail during flyback. Thus, the flyback voltage is double the supply voltage.

Vertical output

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity. The output contains SOAR (short-circuit protection) and thermal protection. The output current on pin 5 is reduced for a short time (to let the temperature decrease to T_j <150 °C), when the junction temperature T_j exceeds 160 °C.

Deflection guard

Pin 9 goes to HIGH in case of too high junction temperature (Fig.3).

A pulse signal with 50% duty cycle is output on pin 9, if the deflection coil is open-circuit . A flyback pulse signal is output at normal condition.

Further watching can be achieved by means of an external guard circuit as shown in Fig.4. The 22 µF capacitor is charged during flyback time ($V_5 > V_8$) at normal condition.

In case of failures, the capacitor is discharged – the guard output becomes HIGH.

Guard output level (Fig.4):

- LOW for normal condition
- HIGH for deflection coil short-circuit respectively open-circuit
- HIGH when there are neither input nor output signals.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134);
voltages refering to substrate pin 6.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	-	40	V
V_{P2}	positive supply voltage (pin 4)	-	60	V
V_{P3}	positive supply voltage (pin 8)	-	60	V
$V_{2,3,9}$	voltage on pins 2, 3, and 9	-	V_{P1}	V
$V_{5,7}$	voltage on pins 5 and 7	-	60	V
I_4	current on pin 4	-	1	A
$I_{5\,(M)}$	output current* on pin 5 (peak value)	-	±1.5	A
$I_{7(M)}$	flyback current on pin 7 (peak value)	-	±1.5	A
I_9	current on pin 9	-	–8	mA
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	–20	75	°C
T_j	junction temperature*	-	168	°C
V_{ESD}	electrostatic handling** for all pins	-	±300	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction-to-case	-	5	K/W

The heatsink can be estimated according to application circuit Fig.1.

$R_{th\ j\text{-}a} = R_{th\ j\text{-}c} + R_{th\ c\text{-}h} + R_{th\ h\text{-}a} = (T_{j\ max} - T_{amb}) / P_{IC\ max} = (105 - 65)\ °C / 1.8\ W = 22.2\ K/W.$

A heatsink is needed at $R_{th\ j\text{-}c} < 5$ K/W and $R_{th\ c\text{-}h} = 0.5$ K/W (using silicon grease) with

$R_{th\ h\text{-}a} = 22.2\ K/W - (5 + 0.5)\ K/W = \underline{16.7\ K/W}$

* Internally limited by thermal protection; switching temperature point at 160 ±8 °C.

** Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor

CHARACTERISTICS

$V_{P1} = V_{P2} = 25$ V; $V_N = V_6 = 0$ V; $T_{amb} = 25$ °C and voltages referenced to substrate (pin 6) unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage 1 range (pin 1)		9	25	30	V
V_{P2}	positive supply voltage 2 range (pin 4)		9	25	60	V
V_{P3}	positive supply voltage 3 range (pin 8)		9	-	60	V
I_{P1}	supply current (pin 1)		-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	without input signal	-	9	-	mA
Pre-amplifier						
$V_{2,3}$	input voltage range (pins 2 and 3)		1.6	-	V_{P1}-0.5	V
$I_{2,3}$	input quiescent current	without input signal	-	100	-	nA
Flyback generator						
V_7	output voltage	upper value; $I_7 = -1$ A	-	V_{P3}-2.2	-	V
$I_{7\,(M)}$	flyback output current (maximum value, pin 7)	-		-	±1.3	A
V_{1-5}	threshold voltage to switch flyback	on/off threshold	-	1.4	-	V
$t_{p\,FLB}$	flyback pulse time	Fig.1; Fig.3	-	250	-	µs
Vertical output		Fig.3				
V_5	output voltage	upper value; $I_5 = -1$ A	V_{P2}-2.3	V_{P2}-2	-	V
		lower value; $I_5 = 1$A	-	1.5	1.7	V
		upper value; $I_5 = -1.4$ A	-	V_{P2}-2.3	-	V
		lower value; $I_5 = 1.4$ A	-	1.7	-	V
I_5	vertical output current (peak-to-peak value, pin 5)		-	-	2.8	A
LIN	non-linearity of output signal		-	-	1	%
Pulse circuit output		Fig.3				
V_9	output voltage range	$R_{PCO} = 10$ kΩ; Fig.1	0.4	-	V_{P1}-0.4	V
	output voltage for thermal protection active		V_{P1}-0.4	-	-	V
V_{1-5}	voltage to insert flyback pulse on pin 9	normal condition	-	-	1.4	V
$t_{p\,9}$	pulse width	deflection open-circuit	-	50	-	%
		normal condition	$t_{p\,FLB}$	-	-	µs

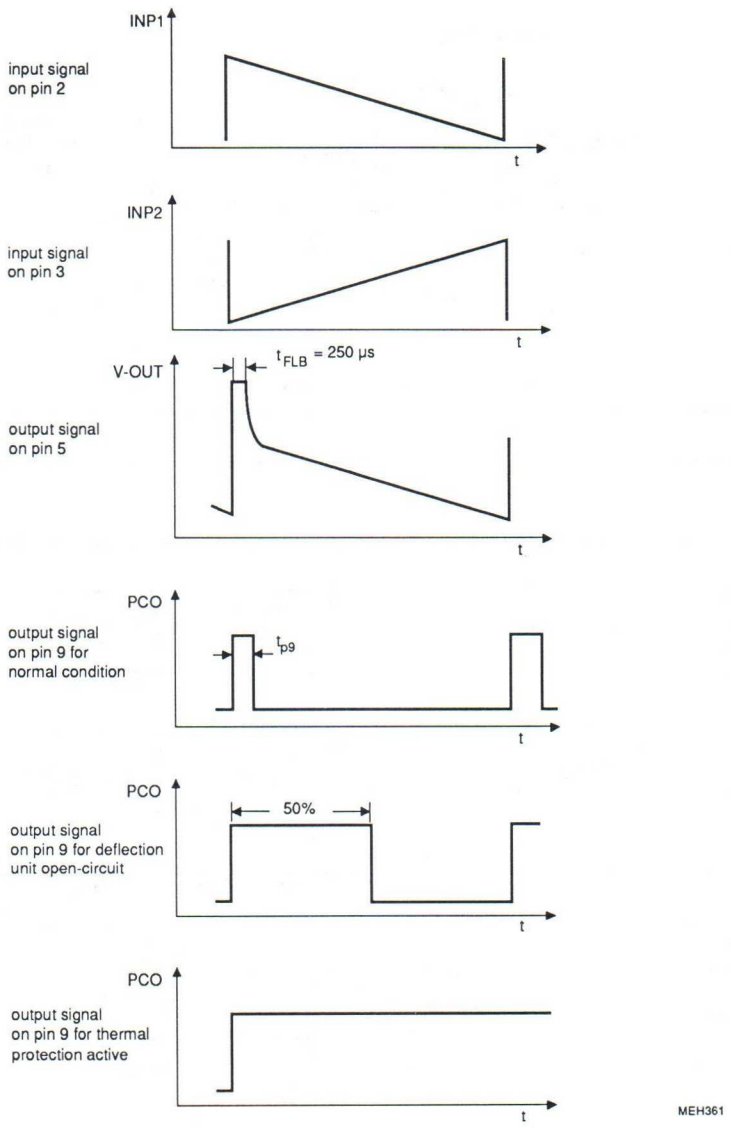


Fig.3 Vertical timing.

APPLICATION INFORMATION

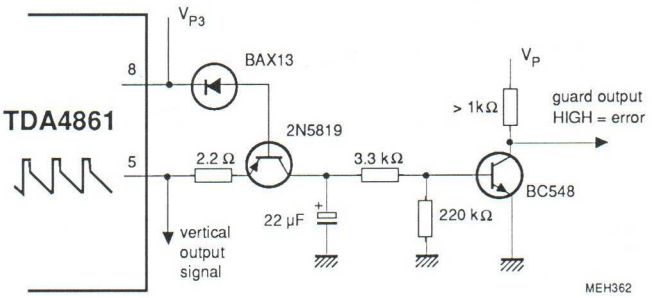


Fig.4 Guard circuit application on vertical output.

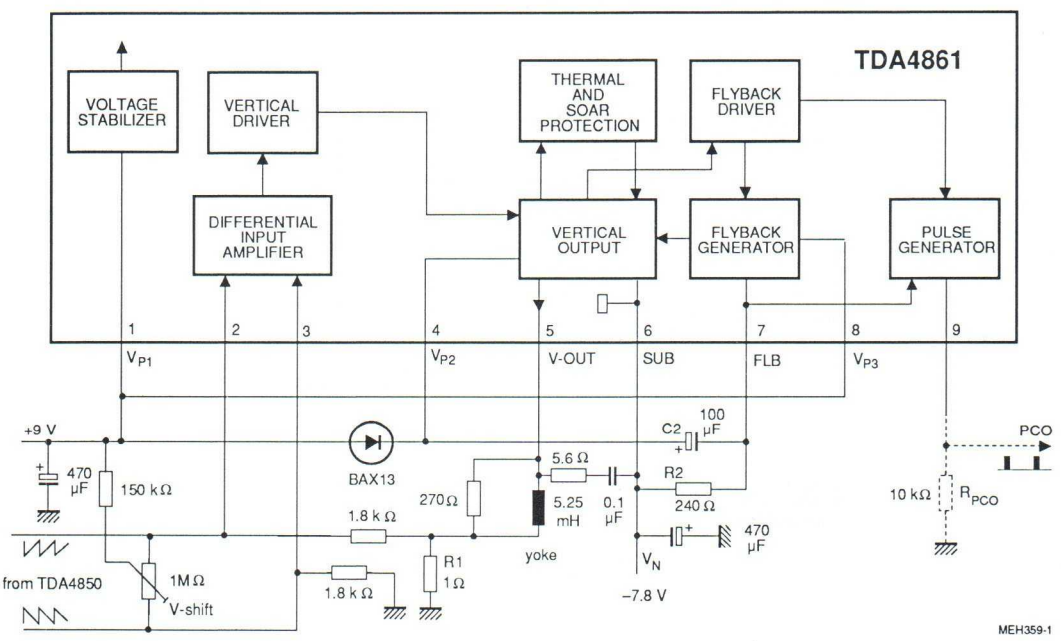


Fig.5 Application for flyback voltage generation by doubling the supply voltage.

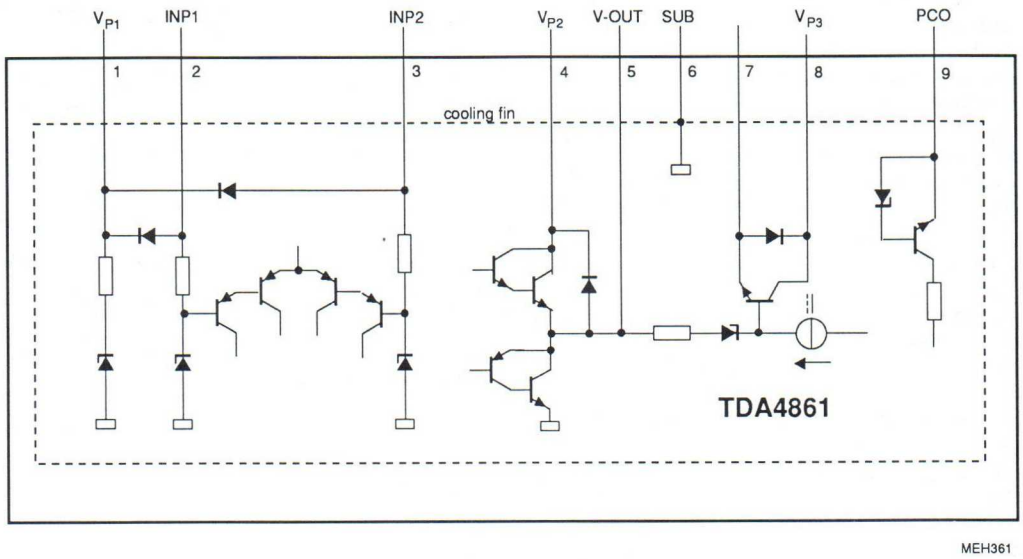


Fig.6 Internal circuit.

Full bridge current driven vertical deflection booster TDA4865

FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA4850/51
- Pre-amplifier with differential high CMRR current mode inputs
- High electro-magnetic immunity
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 140 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage range (pin 3)	8	–	25	V
V_{FB}	flyback supply voltage (pin 7; note 2)	–	–	60	V
I_{FB}	quiescent current (pin 7)	–	12	18	mA
Vertical circuit					
I_{defl}	deflection current (peak-to-peak value; pins 4 and 6)	0.6	–	2	A
I_{id}	differential input current (peak-to-peak value; note 3)	–	±500	±600	μA
Flyback generator					
I_{FB}	maximum current during flyback (peak-to-peak value; pin 7)	–	–	±1	A
Guard circuit					
V_8	guard voltage (guard on)	–	–	12.5	V
I_8	guard current (guard on)	5	–	–	mA

Notes to the quick reference data

1. Voltages refer to pin 5 (GND).
2. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 μF (between pin 7 and pin 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
3. Differential input current $I_{id} = I_1 - I_2$.

GENERAL DESCRIPTION

The TDA4865 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 Hz to 140 Hz. The circuit provides a high CMRR current driven differential input with high electro-magnetic immunity. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA4850/51 the ICs offer an extremely advanced system solution.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4865	9	SIL	plastic	SOT110

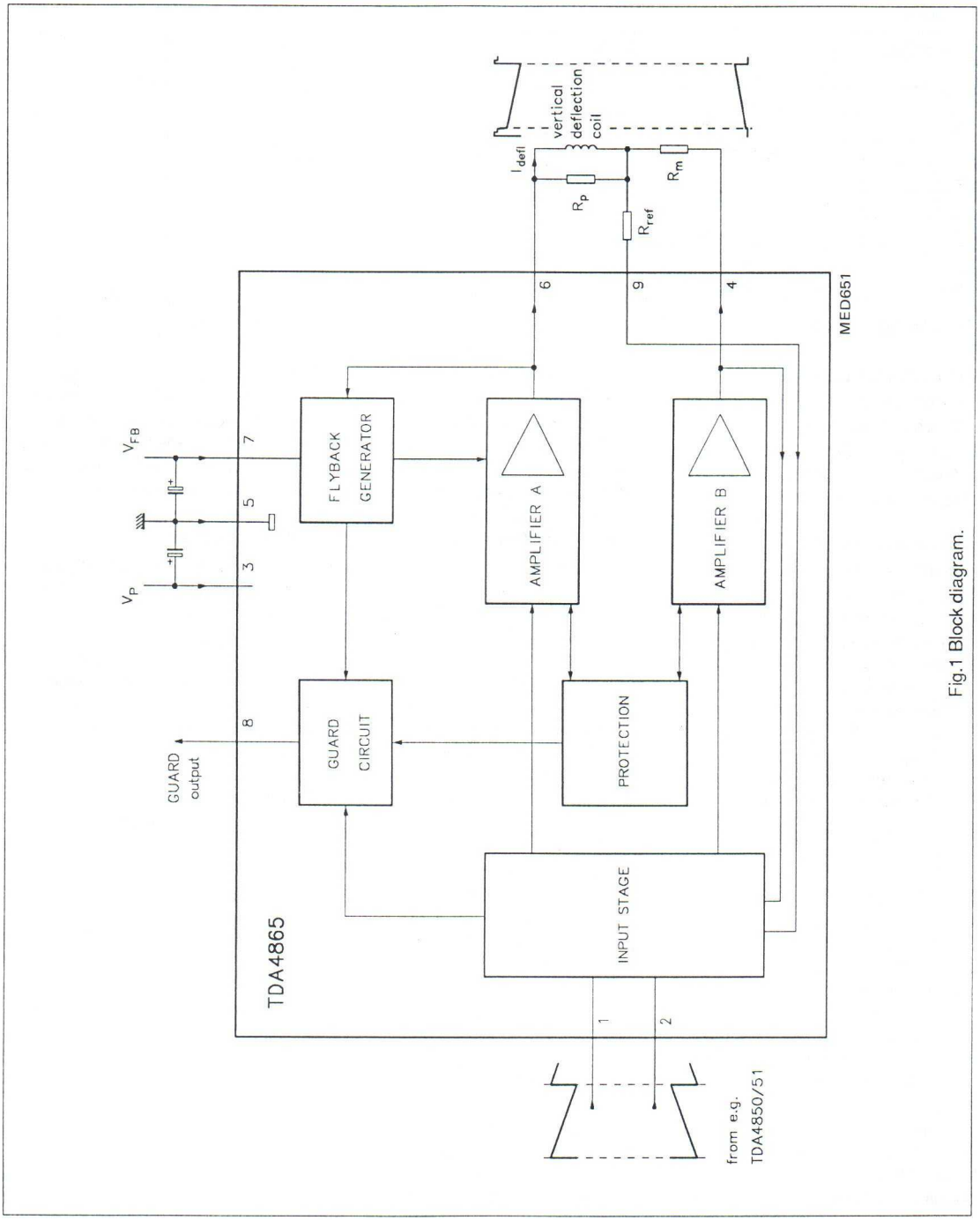


Fig.1 Block diagram.

Full bridge current driven vertical deflection booster TDA4865

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V_P	3	supply voltage
OUTB	4	output B
GND	5	ground
OUTA	6	output A
V_{FB}	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

The cooling fin is connected to pin 5 (GND)

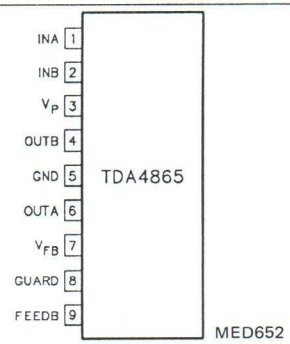


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4865 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA4850/51) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required). The differential input stage delivers the driver signals for the output stages.

Output stages

The two output stages are current driven in opposite phase and work in combination with the deflection coil in a full bridge configuration. Therefore the TDA4865 needs no external coupling capacitor (e.g. 2200 µF) and works with one supply voltage V_P and a separate adjustable flyback supply voltage V_{FB}. The deflection current through the coil (I_{defl}) is measured with the resistor R_m which produces a voltage drop (U_{rm}) of:

U_{rm} = (approx.) = $R_m \times I_{defl}$

At the feedback input (pin 9) a part of I_{defl} is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current (I_9) through R_{ref} is:

$$I_9 = (\text{approx.}) = \frac{R_m}{R_{ref}} \times I_{defl}$$

The input stage directly compares the driver currents into pin 1 and 2 with the feedback current I_9. Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current (I_{id}) is:

$$I_{id} = I_9 = (\text{approx.}) = \frac{R_m}{R_{ref}} \times I_{defl}$$

Due to the feedback loop gain ($V_{U\,loop}$) and internal bondwire resistance (R_{bo}) correction factors are needed to determine the accurate value of I_{defl}:

$$I_{defl} = I_{id} \times \frac{R_{ref}}{R_m + R_{bo}} \times \left(1 - \frac{1}{V_{U\,loop}}\right)$$

with R_{bo} = (approx.) = 70 mΩ

and $\left(1 - \frac{1}{V_{U\,loop}}\right) = 0.98$

for I_{defl} = 1 A

The deflection current can be adjusted from ±1 A to ±0.3 A by varying R_{ref} when R_m is fixed to 1 Ω. Because of its current mode the feedback input (pin 9) has high immunity against electro-magnetic interferences too. High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle this circuit works with.

Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage V_P) and flyback time (flyback voltage V_{FB}). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

Protection

The output stages are fully protected against:

- Thermal overshoot
- Short circuit of the coil (pins 4 and 6)

Guard circuit

The internal guard circuit gives information of any irregular values of the deflection current. The guard signal is active high:
- at thermal overshoot
- when feedback loop is out of range
- during flyback

The guard signal can be used to blank the CRT. The internal guard circuit will not be activated, if the input signals on pin 1 and 2 delivered from the driver circuit are out of range.
For this reason an external guard circuit can be applied to detect failures of the input signal too (see Fig.6; application proposal). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referring to pin 5 (GND) unless otherwise specified

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 3)	0	30	V
V_{FB}	flyback supply voltage (pin 7)	0	62	V
I_{FB}	flyback supply current	0	±1.8	A
$V_{1,2}$	input voltage	0	V_P	V
$I_{1,2}$	input current	0	±5	mA
$V_{4,6}$	output voltage	0	V_P	V
$I_{4,6}$	output current (note 1)	0	±1.8	A
V_9	feedback voltage	0	V_P	V
I_9	feedback current	0	±5	mA
V_8	guard voltage (note 2)	0	V_P + 0.4	V
I_8	guard current	0	±5	mA
T_{stg}	storage temperature range	–20	+150	°C
T_{amb}	operating ambient temperature range	–20	+75	°C
T_j	junction temperature (note 3)	–20	+150	°C
V_{ESD}	electrostatic handling (note 4)	–	±300	V

Notes to the limiting values

1. Maximum output currents I_4 and I_6 are limited by current protection.
2. For V_P > 13 V the guard voltage V_8 is limited to 13 V.
3. Internally limited by thermal protection; switching point > 150 °C.
4. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	8 K/W

CHARACTERISTICS

T_{amb} = +25 °C; V_P = 15 V; V_{FB} = 40 V; voltages refer to pin 5 (GND) unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 3)		8	–	25	V
V_{FB}	flyback supply voltage (pin 7)	see note 1	V_P	–	60	V
I_{FB}	quiescent current (pin 7)	no load; no signal	–	12	18	mA
Input stage						
I_{id}	differential input current ($I_{id} = I_1 - I_2$) (peak-to-peak value)		–	±500	±600	μA
$I_{1,2}$	single ended input current (peak-to-peak value)	see note 2	0	±300	±600	μA
D_i	common mode rejection ratio	see note 3	–	–54	–	dB
V_1	input clamp voltage	I_1 = 300 μA	2.7	3.0	3.3	V
V_2	input clamp voltage	I_2 = 300 μA	2.7	3.0	3.3	V
TC_1	TC input clamp voltage on pin 1		0	–	±800	μV/K
TC_2	TC input clamp voltage on pin 2		0	–	±800	μV/K
V_{1-2}	differential input voltage	I_{id} = 0	0	–	±10	mV
I_9	feedback current		–	±500	±600	μA
V_9	feedback voltage		1	–	V_P – 1.5	V
I_{idoff}	differential input offset current ($I_{idoff} = I_1 - I_2$)	I_{defl} = 0; R_{ref} = 1.5 kΩ; R_m = 1 Ω	0	–	±30	μA
TC_{off}	TC differential input offset shift		0	–	±50	nA/K
C_{INA}	input capacity pin 1 referring to GND		–	–	5	pF
C_{INB}	input capacity pin 2 referring to GND		–	–	5	pF
Output stages A and B						
I_4	output current		–	–	±1	A
I_6	output current		–	–	±1	A
V_{6-5}	output A saturation voltage to GND	I_6 = 0.7 A	–	1.5	1.8	V
V_{6-3}	output A saturation voltage to V_P	I_6 = 0.7 A; see note 4	–	3	3.4	V
V_{4-5}	output B saturation voltage to GND	I_4 = 0.7 A	–	1.5	1.8	V
V_{4-3}	output B saturation voltage to V_P	I_4 = 0.7 A; see note 4	–	1.9	2.3	V
Lin	linearity error	I_{defl} = ±0.7 A; see note 5	–	–	2	%
V_4	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
V_6	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
G_{oi}	open loop current gain ($I_{4,6}/I_{id}$)	$I_{4,6}$ < 100 mA; see note 6	–	100	–	dB
G_{of}	open loop current gain ($I_{4,6}/I_9$)	$I_{4,6}$ < 100 mA; see note 6	–	100	–	dB
G_{if}	current ratio (I_{id}/I_9)	closed loop	–	–0.2	–	dB
$I_{deflrip}$	output ripple current versus supply ripple	V_{Prip} = ±0.5 V; I_{id} = 0; closed loop	–	±1	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback generator						
V_{7-6}	voltage drop during flyback					
	reverse	I_{defl} = 0.7 A;	–	–2	–3.0	V
	forward	during flyback	–	4	5.2	V
V_7	switching on threshold voltage		$V_P - 1$	–	$V_P - 0.2$	V
V_7	switching off threshold voltage		$V_P - 2.6$	–	$V_P - 0.9$	V
I_7	flyback current during flyback		–	–	±1	A
Guard circuit						
V_8	output voltage	guard on	7.7	–	12.5	V
V_8	output voltage	guard on; V_P = 8 V	6.9	–	$V_P - 0.4$	V
I_8	output current	guard on	5	–	–	mA
V_8	output voltage	guard off; I_9 = 0.3 mA	–	–	0.4	V
I_8	output current	guard off; V_9 = 5 V	0.5	1	1.5	mA
$V_{8\,(ext.)}$	allowable external voltage on pin 8	see note 7	0	–	$V_P + 0.3$	V

Notes to the characteristics

1. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 µF (between pin 7 and pin 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
2. Saturation voltages of output stages A and B can be increased in case of negative input currents $-I_{1,2} > 500$ µA.
3. $D_i = \frac{I_{deflc}}{I_{idc}} \times \frac{I_{id}}{I_{defl}}$ with I_{deflc} = common mode deflection current and I_{idc} = common mode input current.
4. For $V_{FB} < (V_P + 7\ V)$ increasing of saturation voltages V_{6-3} and V_{4-3} is possible (reduced limiting level of the input stage).
5. Deviation of the output signal with respect to the input signal.
6. Frequency behaviour of G_{oi} and G_{of}:
   –3 dB open loop bandwidth (–45 °) at 15 kHz; second pole (–135 °) at 1.3 MHz;
   open loop gain at second pole (–135 °) 55 dB.
7. For $V_P < 12.6$ V is $V_{8\,(ext.)} = V_P + 0.3$ V.

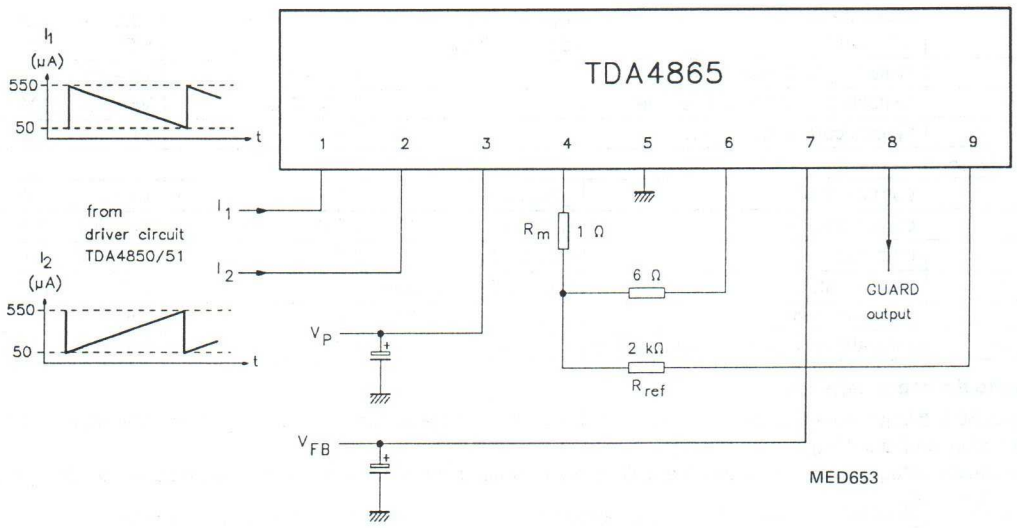


Fig.3 Test diagram.

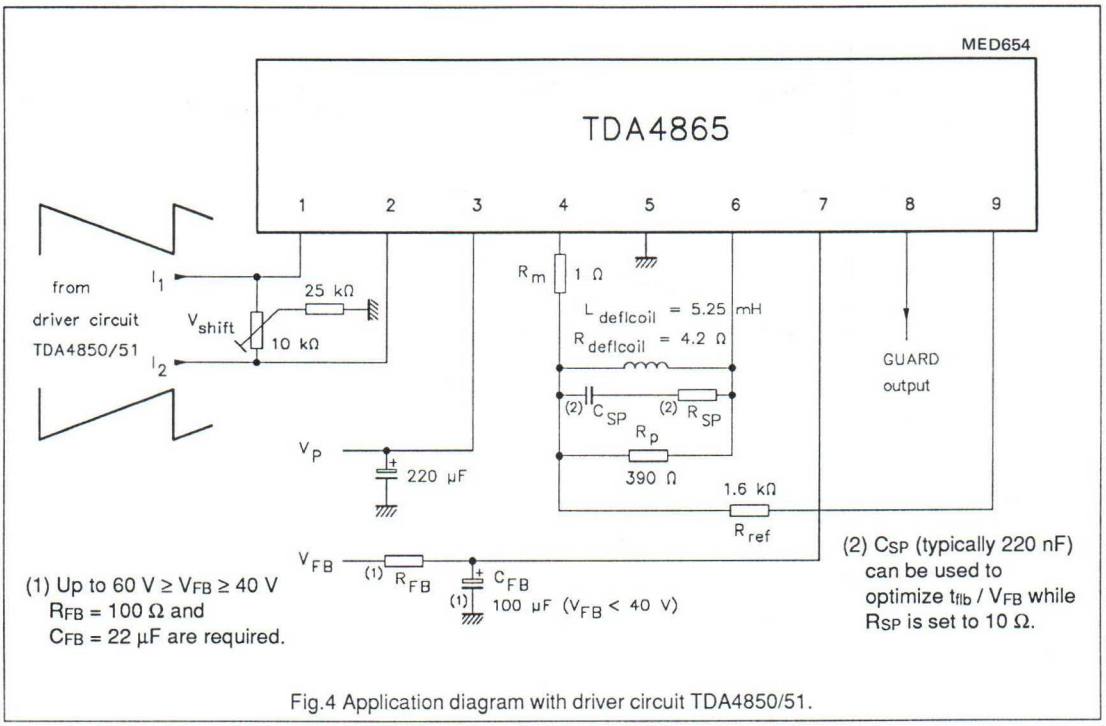


Fig.4 Application diagram with driver circuit TDA4850/51.

Example

Values given from application

$I_{deflmax}$	=	0.71 A
$L_{deflcoil}$	=	5.25 mH
$R_{deflcoil}$	=	4.17 Ω + 7% + ΔR(ϑ)
	=	6.12 Ω
R_m	=	1 Ω + 1%
R_p	=	390 Ω
R_{ref}	=	1.6 kΩ
V_{FB}	=	40 V
T_{amb}	=	+50 °C
T_{jmax}	=	+110 °C
$T_{deflcoil}$	=	+75 °C

Calculated values

V_P	=	10 V
t_{flb}	=	250 µs
P_{tot}	=	4.5 W
P_{defl}	=	1.2 W
P_{IC}	=	3.3 W
R_{thtot}	=	60 K / 3.3 W ≈ 18 K/W
$R_{th\ j\text{-}c}$	=	8 K/W

Therefore a heatsink with $R_{th\ c\text{-}a}$ < 10 K/W is needed.

Calculation formula for supply voltage and power consumption

$V_{b1} = V_{6-3} + R_{deflcoil} \times I_{deflmax} - U'_L + R_m \times I_{deflmax} + V_{4-5}$

$V_{b2} = V_{6-5} + R_{deflcoil} \times I_{deflmax} + U'_L + R_m \times I_{deflmax} + V_{4-3}$

for $V_{b1} > V_{b2}$ $V_P = V_{b1}$

for $V_{b2} > V_{b1}$ $V_P = V_{b2}$

with $U'_L = L_{deflcoil} \times 2\ I_{deflmax} \times f_v$

f_v = vertical deflection frequency

$$P_{tot} = V_P \times \frac{I_{deflmax}}{\sqrt{3}} + V_P \times 0.003\ A + 0.05\ W + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3}\left(R_{deflcoil} + R_m\right) I^2_{deflmax}$$

$P_{IC} = P_{tot} - P_{defl}$

with P_{IC} = power dissipation of the IC

P_{defl} = power dissipation of the deflection coil

P_{tot} = total power dissipation

Calculation formula for flyback time (t_{flb})

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \ln\left(\frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} + V_{flbdr}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} - V_{flbdf}}}\right) + t_{flboff}$$

with t_{flboff} = flyback switch off time = 50 µs for this application (t_{flboff} depends on V_{FB}, $I_{deflmax}$, $L_{deflcoil}$ and C_{SP}).

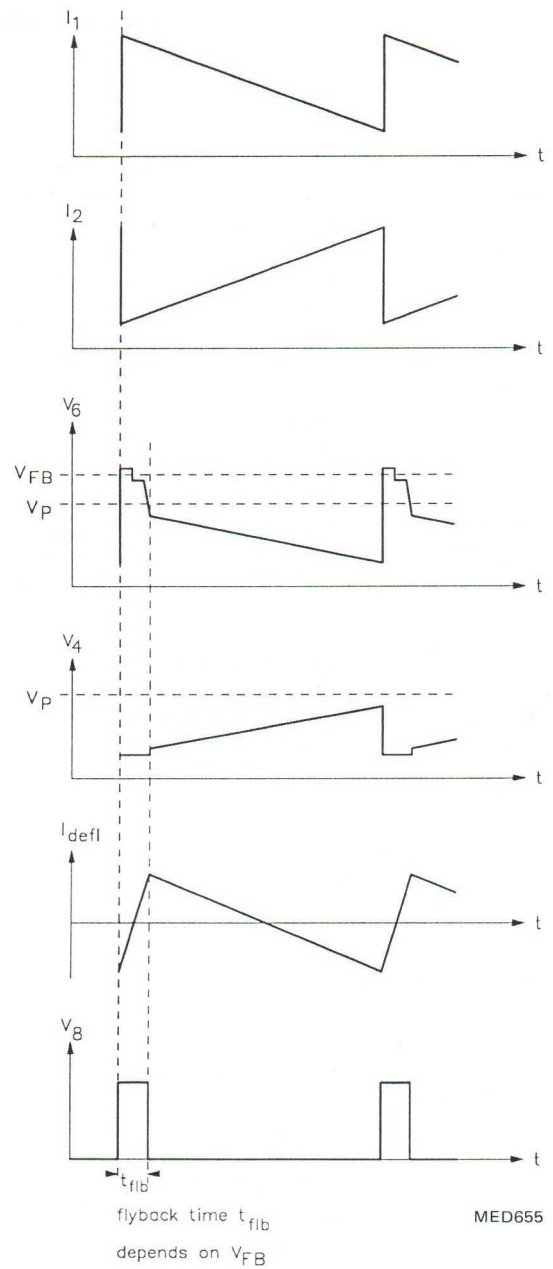


Fig.5 Timing diagram.

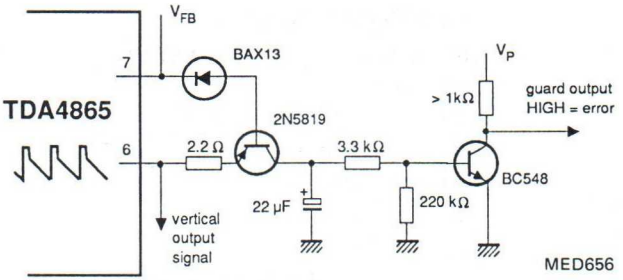


Fig.6 Application circuit for external guard signal generation.

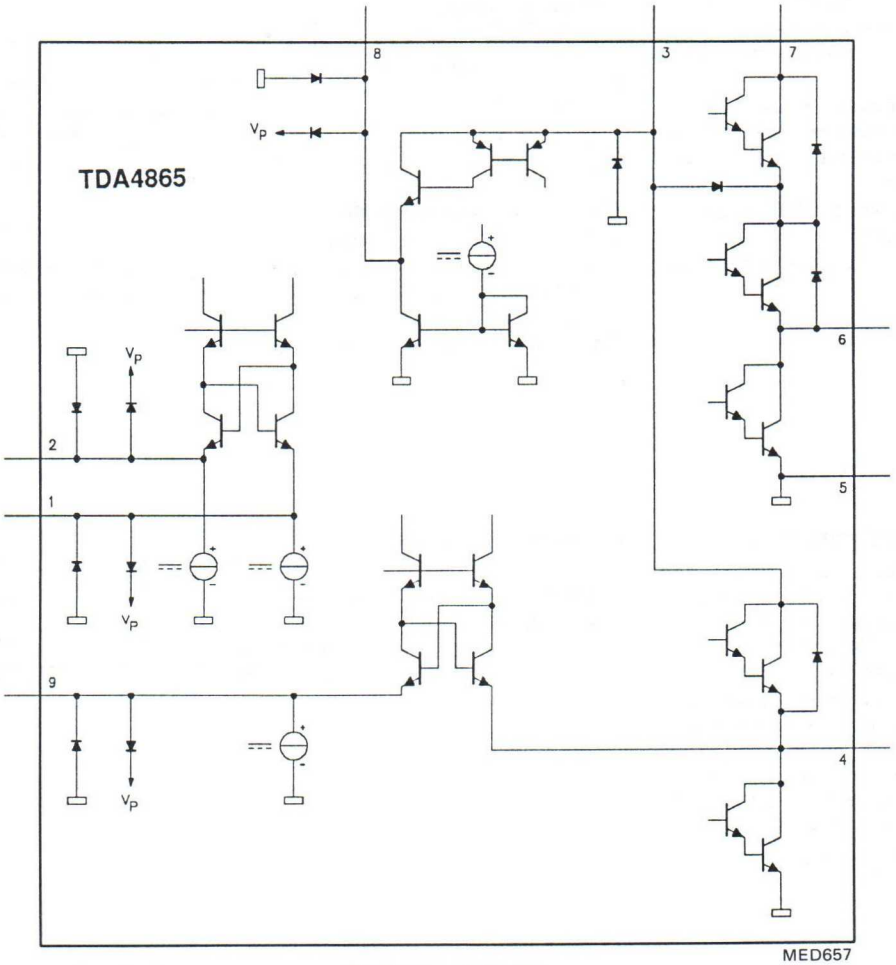


Fig.7 Internal circuits.

Full bridge current driven vertical deflection booster TDA4866

FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA4850/51
- Pre-amplifier with differential high CMRR current mode inputs
- High electro-magnetic immunity
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 140 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage (pin 3)	8	–	25	V
V_{FB}	flyback supply voltage (pin 7; note 2)	–	–	60	V
I_{FB}	quiescent current (pin 7)	–	12	18	mA
Vertical circuit					
I_{defl}	deflection current (peak-to-peak value; pins 4 and 6)	0.6	–	2	A
I_{id}	differential input current (peak-to-peak value; note 3)	–	±500	±600	μA
Flyback generator					
I_{FB}	maximum current during flyback (peak-to-peak value; pin 7)	–	–	2	A
Guard circuit					
V_8	guard voltage (guard on)	–	8.5	12.5	V
I_8	guard current (guard on)	5	–	–	mA

Notes to the quick reference data

1. Voltages refer to pin 5 (GND).
2. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 μF (between pin 7 and pin 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
3. Differential input current $I_{id} = I_1 - I_2$.

GENERAL DESCRIPTION

The TDA4866 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 Hz to 140 Hz. The circuit provides a high CMRR current driven differential input with high electro-magnetic immunity. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA4850/51 the ICs offer an extremely advanced system solution.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4866	9	SIL	plastic	SOT131

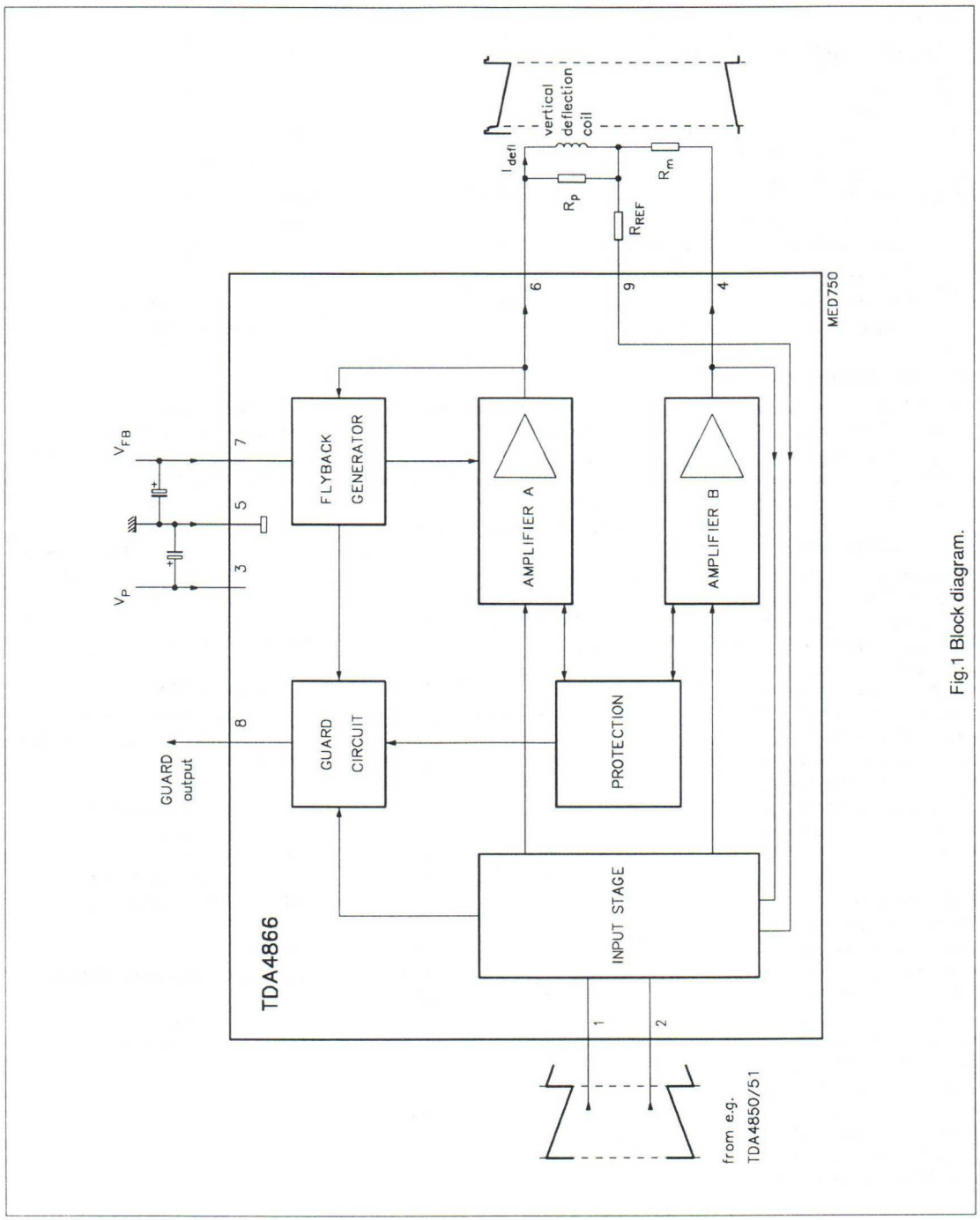


Fig.1 Block diagram.

Full bridge current driven vertical deflection booster TDA4866

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V_P	3	supply voltage
OUTB	4	output B
GND	5	ground
OUTA	6	output A
V_{FB}	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

The cooling fin is connected to pin 5 (GND)

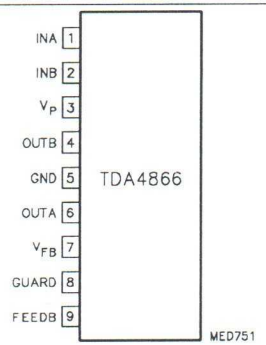


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4866 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA4850/51) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required). The differential input stage delivers the driver signals for the output stages.

Output stages

The two output stages are current driven in opposite phase and operate in combination with the deflection coil in a full bridge configuration. Therefore the TDA4866 requires no external coupling capacitor (e.g. 2200 µF) and operates with one supply voltage V_P and a separate adjustable flyback supply voltage V_{FB} only. The deflection current through the coil (I_{defl}) is measured with the resistor R_m which produces a voltage drop (U_{rm}) of:

$U_{rm} = (approx.) = R_m \times I_{defl}$

At the feedback input (pin 9) a part of I_{defl} is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current (I_9) through R_{REF} is:

$$I_9 = (approx.) = \frac{R_m}{R_{REF}} \times I_{defl}$$

The input stage directly compares the driver currents into pin 1 and 2 with the feedback current I_9. Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current (I_{id}) is:

$$I_{id} = I_9 = (approx.) = \frac{R_m}{R_{REF}} \times I_{defl}$$

Due to the feedback loop gain ($V_{U\ loop}$) and internal bondwire resistance (R_{bo}) correction factors are required to determine the accurate value of I_{defl}:

$$I_{defl} = I_{id} \times \frac{R_{REF}}{R_m + R_{bo}} \times \left(1 - \frac{1}{V_{U\ loop}}\right)$$

with $R_{bo} = (approx.) = 70\ m\Omega$

and $\left(1 - \frac{1}{V_{U\ loop}}\right) = 0.98$

for $I_{defl} = 1$ A

The deflection current can be adjusted from ±1 A to ±0.3 A by varying R_{REF} when R_m is fixed to 1 Ω. Because of its current mode the feedback input (pin 9) also has high immunity against electro-magnetic interferences. High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle with which this circuit operates.

Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage V_P) and flyback time (flyback voltage V_{FB}). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

Protection

The output stages are protected against:

- thermal overshoot
- short-circuit of the coil (pins 4 and 6)

Guard circuit

The internal guard circuit provides information of any irregular values of the deflection current. The guard signal is active HIGH:
- at thermal overshoot
- when feedback loop is out of range
- during flyback

The guard signal can be used to blank the CRT. The internal guard circuit will not be activated, if the input signals on pin 1 and 2 delivered from the driver circuit are out of range.
For this reason an external guard circuit can be applied to also detect failures of the input signal (see Fig.6; application proposal). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to pin 5 (GND) unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 3)	0	30	V
V_{FB}	flyback supply voltage (pin 7)	0	62	V
I_{FB}	flyback supply current	0	±1.8	A
$V_{1,2}$	input voltage	0	V_P	V
$I_{1,2}$	input current	0	±5	mA
$V_{4,6}$	output voltage	0	V_P	V
$I_{4,6}$	output current (note 1)	0	±1.8	A
V_9	feedback voltage	0	V_P	V
I_9	feedback current	0	±5	mA
V_8	guard voltage (note 2)	0	V_P + 0.4	V
I_8	guard current	0	±5	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	–20	+75	°C
T_j	junction temperature (note 3)	–20	+150	°C
V_{ESD}	electrostatic handling (note 4)	–	±300	V

Notes to the limiting values

1. Maximum output currents I_4 and I_6 are limited by current protection.
2. For $V_P > 13$ V the guard voltage V_8 is limited to 13 V.
3. Internally limited by thermal protection; switching point ≥ 150 °C.
4. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}c}$	from junction to case	4 K/W

CHARACTERISTICS

V_P = 15 V; T_{amb} = +25 °C; V_{FB} = 40 V; voltages referenced to pin 5 (GND); parameters are measured in test circuit Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 3)		8	–	25	V
V_{FB}	flyback supply voltage (pin 7)	note 1	V_P	–	60	V
I_{FB}	quiescent feedback current (pin 7)	no load; no signal	–	12	18	mA
Input stage						
I_{id}	differential input current ($I_{id} = I_1 - I_2$) (peak-to-peak value)		–	±500	±600	µA
$I_{1,2}$	single ended input current (peak-to-peak value)	note 2	0	±300	±600	µA
D_i	common mode rejection ratio	note 3	–	–54	–	dB
V_1	input clamp voltage	I_1 = 300 µA	2.7	3.0	3.3	V
V_2	input clamp voltage	I_2 = 300 µA	2.7	3.0	3.3	V
TC_1	TC input clamp voltage on pin 1		0	–	±800	µV/K
TC_2	TC input clamp voltage on pin 2		0	–	±800	µV/K
V_{1-2}	differential input voltage	I_{id} = 0	0	–	±10	mV
I_9	feedback current		–	±500	±600	µA
V_9	feedback voltage		1	–	V_P – 1.5	V
I_{idoff}	differential input offset current ($I_{idoff} = I_1 - I_2$)	I_{defl} = 0; R_{REF} = 1.5 kΩ; R_m = 1 Ω	0	–	±30	µA
TC_{off}	TC differential input offset shift		0	–	±50	nA/K
C_{INA}	input capacity pin 1 referenced to GND		–	–	5	pF
C_{INB}	input capacity pin 2 referenced to GND		–	–	5	pF
Output stages A and B						
I_4	output current		–	–	±1	A
I_6	output current		–	–	±1	A
V_{6-5}	output A saturation voltage to GND	I_6 = 0.7 A	–	1.5	1.8	V
		I_6 = 1.0 A	–	1.8	2.1	V
V_{6-3}	output A saturation voltage to V_P	I_6 = 0.7 A; note 4	–	3	3.5	V
		I_6 = 1.0 A; note 4	–	3.4	3.9	V
V_{4-5}	output B saturation voltage to GND	I_4 = 0.7 A	–	1.5	1.8	V
		I_4 = 1.0 A	–	1.8	2.1	V
V_{4-3}	output B saturation voltage to V_P	I_4 = 0.7 A; note 4	–	1.9	2.3	V
		I_4 = 1.0 A; note 4	–	2.2	2.6	V
Lin	linearity error	I_{defl} = ±0.7 A; note 5	–	–	2	%
V_4	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
V_6	DC output voltage	I_{id} = 0 A; closed loop	6.6	7.2	7.8	V
G_{oi}	open loop current gain ($I_{4,6}/I_{id}$)	$I_{4,6}$ < 100 mA; note 6	–	100	–	dB
G_{of}	open loop current gain ($I_{4,6}/I_9$)	$I_{4,6}$ < 100 mA; note 6	–	100	–	dB
G_{if}	current ratio (I_{id}/I_9)	closed loop	–	–0.2	–	dB
$I_{deflrip}$	output ripple current as a function of supply ripple	V_{Prip} = ±0.5 V; I_{id} = 0; closed loop	–	±1	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback generator						
V_{7-6}	voltage drop during flyback					
	reverse	I_{defl} = 0.7 A	–	–2.0	–3.0	V
		I_{defl} = 1.0 A	–	–2.3	–3.5	V
	forward	I_{defl} = 0.7 A	–	4.0	5.3	V
		I_{defl} = 1.0 A	–	4.5	5.8	V
V_7	switching on threshold voltage		V_P – 1	–	V_P – 0.2	V
V_7	switching off threshold voltage		V_P – 2.6	–	V_P – 0.9	V
I_7	flyback current during flyback		–	–	±1	A
Guard circuit						
V_8	output voltage	guard on	7.7	–	12.5	V
V_8	output voltage	guard on; V_P = 8 V	6.9	–	V_P – 0.4	V
I_8	output current	guard on	5	–	–	mA
V_8	output voltage	guard off; I_9 = 0.3 mA	–	–	0.4	V
I_8	output current	guard off; V_9 = 5 V	0.5	1	1.5	mA
$V_{8\,(ext.)}$	allowable external voltage on pin 8	note 7	0	–	V_P + 0.3	V

Notes to the characteristics

1. Up to 60 V ≥ V_{FB} ≥ 40 V a decoupling capacitor C_{FB} = 22 µF (between pins 7 and 5) and a resistor R_{FB} = 100 Ω (between pin 7 and V_{FB}) are required (see Fig.4).
2. Saturation voltages of output stages A and B can be increased in the event of negative input currents $-I_{1,2} > 500$ µA.
3. $D_i = \frac{I_{deflc}}{I_{idc}} \times \frac{I_{id}}{I_{defl}}$ with I_{deflc} = common mode deflection current and I_{idc} = common mode input current.
4. For $V_{FB} < (V_P + 7\ V)$ increasing of saturation voltages V_{6-3} and V_{4-3} is possible (reduced limiting level of the input stage).
5. Deviation of the output slope at a constant input slope.
6. Frequency behaviour of G_{oi} and G_{of}:
   –3 dB open-loop bandwidth (–45°) at 15 kHz; second pole (–135°) at 1.3 MHz;
   open-loop gain at second pole (–135°) 55 dB.
7. For $V_P < 12.6$ V is $V_{8\,(ext.)} = V_P + 0.3$ V.

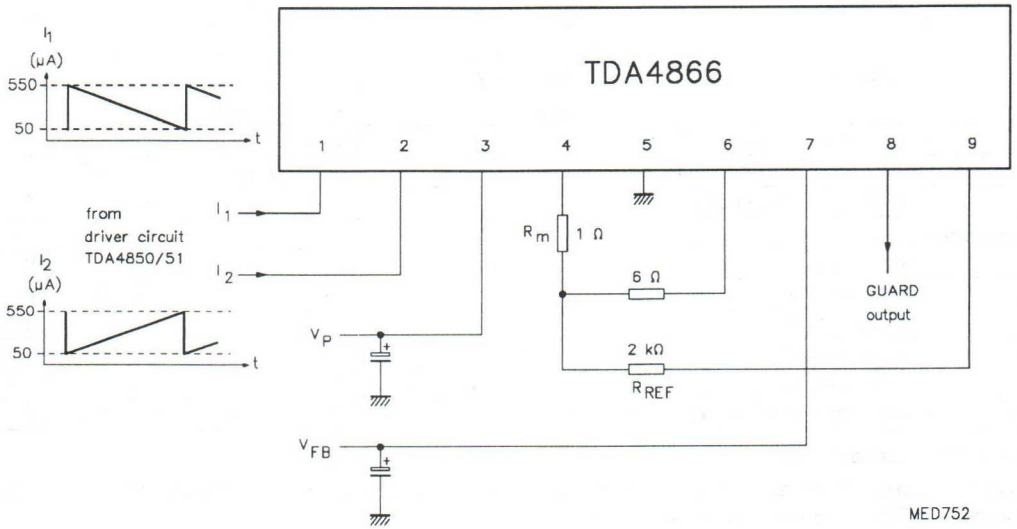


Fig.3 Test diagram.

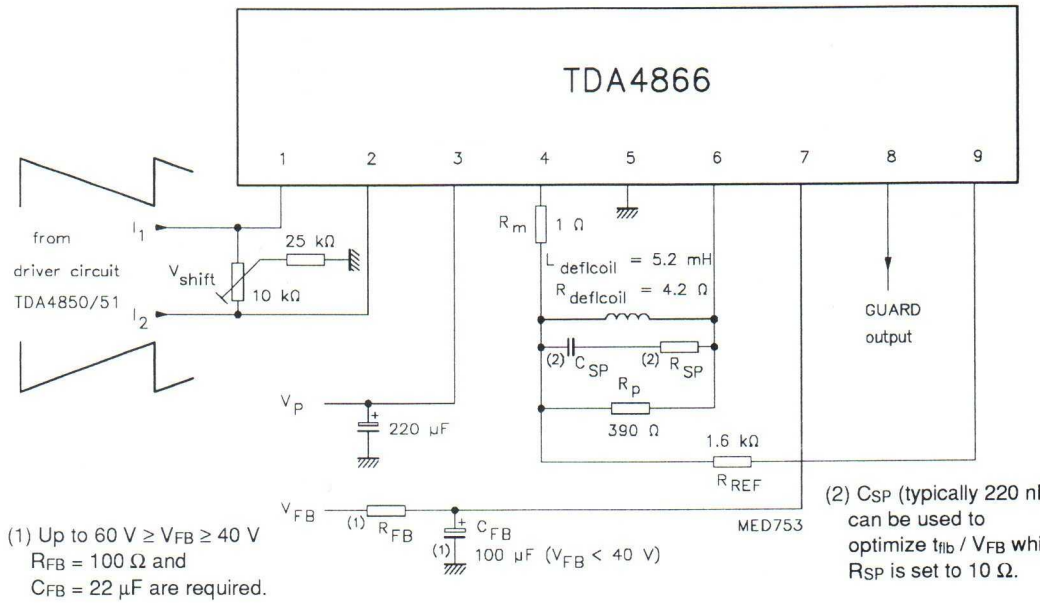


Fig.4 Application diagram with driver circuit TDA4850/51.

Example

Values given from application

$I_{deflmax}$	=	0.71 A
$L_{deflcoil}$	=	5.2 mH
$R_{deflcoil}$	=	4.2 Ω + 7% + ΔR(ϑ)
	=	5.4 Ω
R_m	=	1 Ω + 1%
R_p	=	390 Ω
R_{REF}	=	1.6 kΩ
V_{FB}	=	35 V
T_{amb}	=	+50 °C
$T_{deflcoil}$	=	+75 °C
$R_{th\ j\text{-}c}$	=	4 K/W
$R_{th\ c\text{-}a}$	=	8 K/W

Calculated values

V_P	=	10 V
t_{flb}	=	270 µs
P_{tot}	=	4.4 W
P_{defl}	=	0.9 W
P_{IC}	=	3.5 W
R_{thtot}	=	12 K/W
T_{jmax}	=	+92 °C

Under normal operating conditions T_{jmax} should not exceed 110 °C.

Calculation formula for supply voltage and power consumption

$V_{b1} = V_{6-3} + R_{deflcoil} \times I_{deflmax} - U'_L + R_m \times I_{deflmax} + V_{4-5}$

$V_{b2} = V_{6-5} + R_{deflcoil} \times I_{deflmax} + U'_L + R_m \times I_{deflmax} + V_{4-3}$

for $V_{b1} > V_{b2}$ $V_P = V_{b1}$

for $V_{b2} > V_{b1}$ $V_P = V_{b2}$

with $U'_L = L_{deflcoil} \times 2\ I_{deflmax} \times f_v$

f_v = vertical deflection frequency; V_P is calculated with 0.5 V tolerance

$$P_{tot} = V_P \times \frac{I_{deflmax}}{2} + V_P \times 0.03\ A + 0.1\ W + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3}\left(R_{deflcoil} + R_m\right) I^2_{deflmax}$$

$P_{IC} = P_{tot} - P_{defl}$

with P_{IC} = power dissipation of the IC

P_{defl} = power dissipation of the deflection coil

P_{tot} = total power dissipation

Calculation formula for flyback time (t_{flb})

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \ln\left(\frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} + V_{7-6r}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} - V_{7-6f}}}\right) + t_{flboff}$$

with t_{flboff} = flyback switch off time = 50 µs for this application (t_{flboff} depends on V_{FB}, $I_{deflmax}$, $L_{deflcoil}$ and C_{SP}).

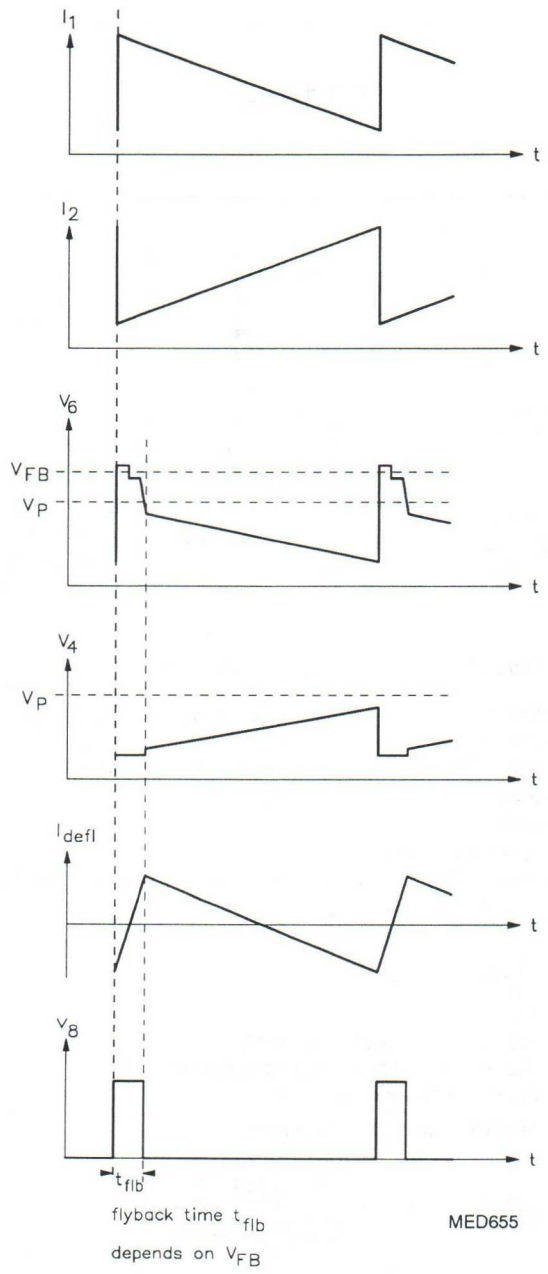


Fig.5 Timing diagram.

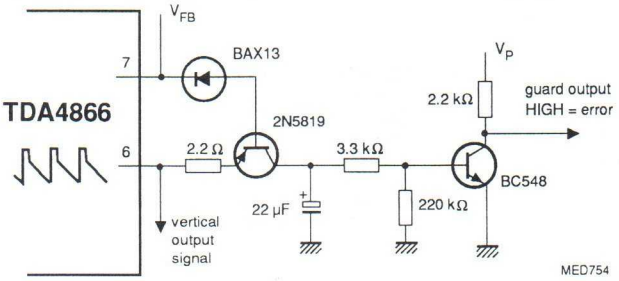


Fig.6 Application circuit for external guard signal generation.

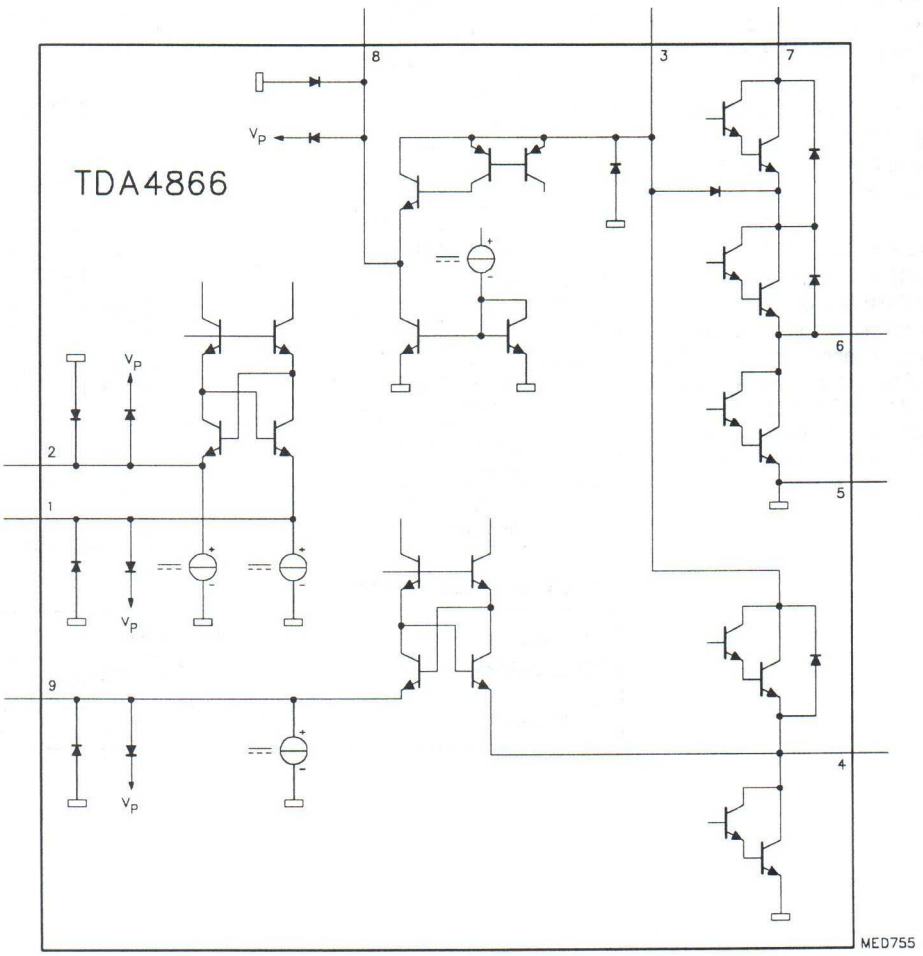


Fig.7 Internal circuits.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	August 1991

TDA4880

Advanced monitor video controller

FEATURES

- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- Individual gain control for white level adjustment
- Brightness control with correct grey scale tracking
- Contrast control for the 3 channels simultaneously
- Cathode feedback to internal reference for black level control
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch off input for screen protection

GENERAL DESCRIPTION

The TDA4880 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA4850.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	40	–	mA
$V_{I(b\text{-}w)}$	input voltage (pins 2, 5 and 8) (black-to-white)		–	0.7	–	V
$V_{O(b\text{-}w)}$	output voltage (pins 19, 16 and 13) (black-to-white)		–	1.0	–	V
$I_{O(b\text{-}w)}$	output current (pins 20, 17 and 14) (black-to-white)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	100	–	mA
B	bandwidth	–3 dB	70	–	–	MHz
G_{nom}	nominal gain		–	3		dB
G_v	gain control range (relative to G_{nom})		–6	–	0	dB
C_v	contrast control range (relative to G_{nom})		–20	–	3	dB
ΔV_{bl}	brightnesss control range		–0.1	–	0.3	V
T_{amb}	operating ambient temperature range		0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4880	20	DIL	plastic	SOT146

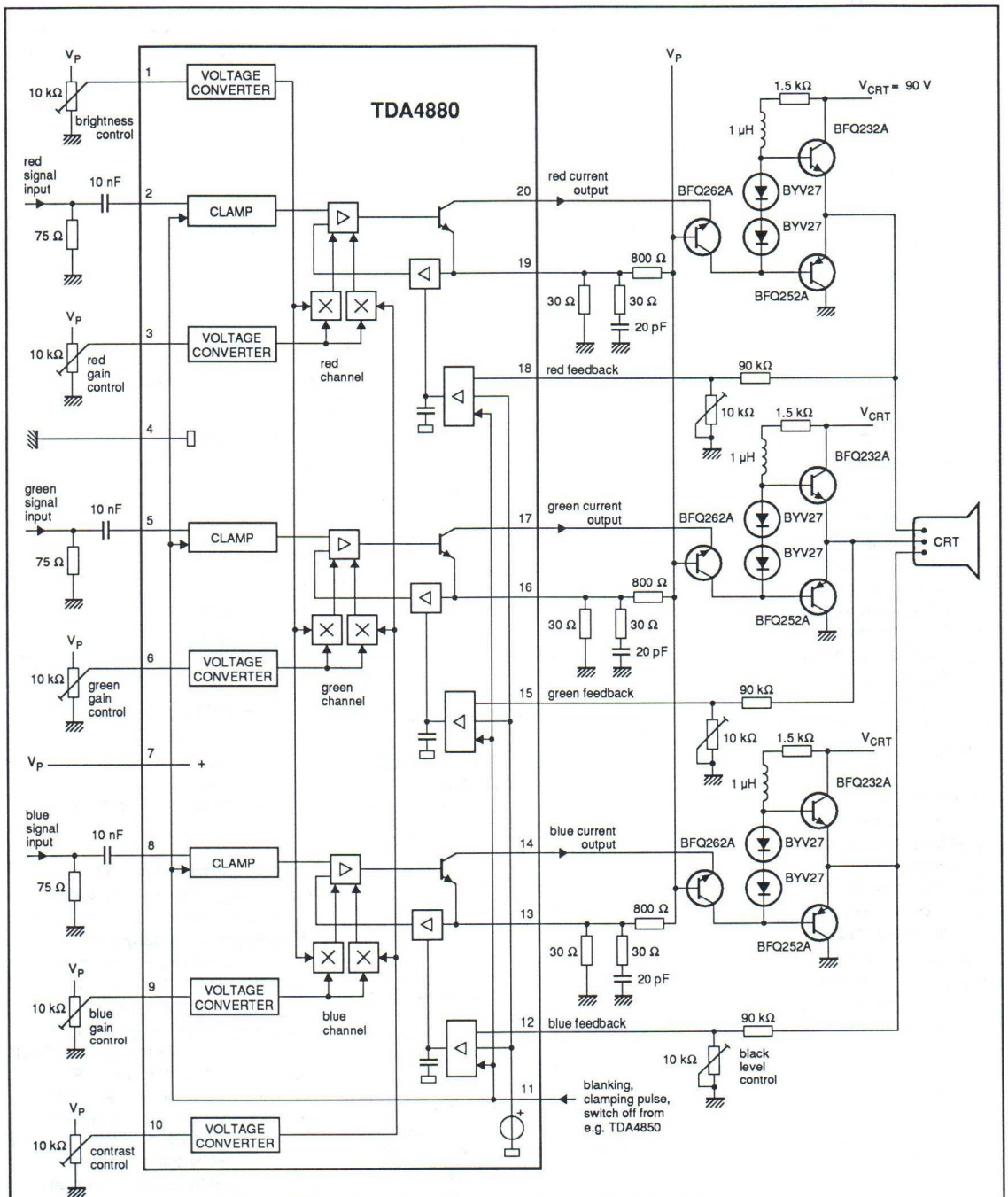


Fig. 1 Block diagram and basic application circuit for DC coupling.

PIN CONFIGURATION

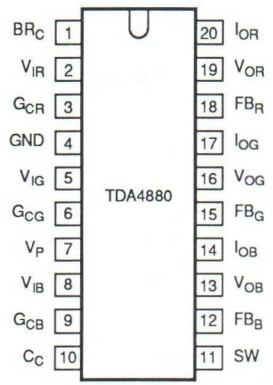


Fig. 2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
BR_C	1	brightness control
V_{IR}	2	red signal input
G_{CR}	3	red gain control
GND	4	ground
V_{IG}	5	green signal input
G_{CG}	6	green gain control
V_P	7	supply voltage
V_{IB}	8	blue signal input
G_{CB}	9	blue gain control
C_C	10	contrast control
SW	11	blanking / clamping pulse, switch off
FB_B	12	blue feedback
V_{OB}	13	blue voltage output
I_{OB}	14	blue current output
FB_G	15	green feedback
V_{OG}	16	green voltage output
I_{OG}	17	green current output
FB_R	18	red feedback
V_{OR}	19	red voltage output
I_{OR}	20	red current output

FUNCTIONAL DESCRIPTION

RGB input signals are capacitively coupled into the TDA4880 from a low ohmic source and are clamped to an internal DC voltage. Sync-on-green will not disturb normal operation. Each channel has a maximum voltage gain of 6 dB. With the nominal gain of 3 dB the nominal black-to-white output voltage is 1 V(p-p).

DC voltages are used for brightness, contrast and gain control.

For **brightness control** (pin 1) the signal black levels are shifted relative to a reference black level voltage. The brightness is set internally to the nominal brightness level during blanking and clamping pulses.

Contrast control is adjusted simultaneously for the three colour signals by a voltage at pin 10.

The **RGB gain controls** (pins 3, 6 and 9) adjust the RGB signal levels of each channel separately to provide the correct white point. Variable RGB gain affects contrast as well as brightness to achieve correct grey scale tracking.

Each **RGB output stage** provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13).

External cascode transistors reduce power consumption and prevent breakdown of the output transistors.

RGB signal output currents and peaking characteristics are determined by resistors and capacitors (pins 19, 16 and 13) and inductors connected to the 90 V supply.

The RGB colour channels have separate internal feedback loops. This ensures high signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The **sandcastle pulse** (e.g. from the TDA4850) is used for input clamping, black level clamping and blanking during flyback. During the clamping pulse the input signals are clamped to an internal black level. During blanking and clamping the brightness is set internally to a nominal value.

For **black level stabilization** the signals at the colour feedback inputs (pins 18, 15 and 12) are compared with an internal reference voltage. Input voltages higher than the reference voltage will increase (lower voltages will decrease) the black level voltage during the clamping pulse. The actual CRT cathode voltage is used for feedback. Therefore, variations of the 90 V supply voltage only marginally affect the black level stabilization. A voltage proportional to the black level is stored on internal capacitors. An integrated colour switch-off facility allows the RGB outputs to be switched to ultra-black for screen protection.

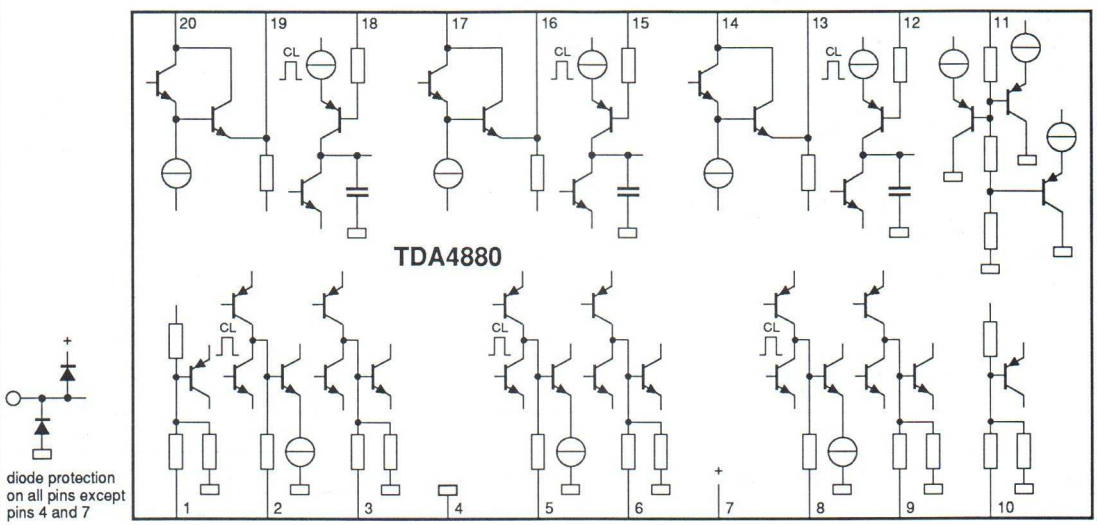


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_i	input voltage range (pins 2, 5 and 8)	–0.1	V_P	V
V_{ext}	external DC voltage ranges pins 20, 17 and 14	–0.1	V_P	V
	pins 19,16 and 13	–	–	V
	pins 1, 3, 6, 9 and 10	–0.1	V_P	V
	pin 11	–0.7	$V_P + 0.7$	V
I_M	peak output current (pins 20, 17 and 14)	–	150	mA
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
T_j	maximum junction temperature	–	150	°C
P_{tot}	total power dissipation	–	1200	mW

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = 25 °C; all voltages measured to GND (pin 4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	40	–	mA
Video signal inputs						
$V_{I(b-w)}$	input amplitude (pins 2, 5 and 8) (black-to-white)		–	0.7	1.0	V
$I_{2,5,8}$	DC current	no clamping	–0.1	–	0.1	µA
		during clamping	± 50	–	–	µA
Brightness control						
V_1	input voltage range		1.0	–	6.0	V
I_1	current		–	–	± 100	µA
ΔV_{bl1}	black level voltage change at nominal gain (pins 19, 16 and 13)	V_1 = 1.0 V; $V_{3,6,9}$ = 6 V	–	–0.1	–	V
		V_1 = 2.25 V; $V_{3,6,9}$ = 6 V	–	0	–	V
		V_1 = 6.0 V; $V_{3,6,9}$ = 6 V	–	0.3	–	V
Contrast control						
V_{10}	input voltage range		1.0	–	6.0	V
I_{10}	current		–	–	± 100	µA
C_v	contrast relative to nominal contrast	V_{10} = 6.0 V; $V_{3,6,9}$ = 6 V	–	3	–	dB
		V_{10} = 4.5 V; $V_{3,6,9}$ = 6 V	–	0	–	dB
		V_{10} = 1.0 V; $V_{3,6,9}$ = 6 V	–	–20	–	dB
Tr	tracking of RGB signals		–	0	0.5	dB
Gain control						
$V_{3,6,9}$	input voltage range		1.0	–	6.0	V
$I_{3,6,9}$	current		–	–	± 100	µA
G_v	gain relative to nominal gain	V_{10} = 4.5 V; $V_{3,6,9}$ = 6 V	–	0	–	dB
		V_{10} = 4.5 V; $V_{3,6,9}$ = 1 V	–	–6	–	dB
Frequency response						
G_{vf}	gain decrease by frequency response at pins 20, 17 and 14	70 MHz	–	–	–3	dB
t_{rO}	rise time at voltage output (pins 19,16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	5	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage outputs (pins 19, 16, 13)						
$V_{O(b-w)}$	signal output voltage (black-to-white value)	at nominal contrast, gain and nominal input signals	–	1.0	–	V
V_{bl}	black level voltage	during clamping	0.5	–	0.7	V
		during switch-off	–	–	0.3	V
S/N	signal to noise ratio	note 1	–	–	44	dB
Current outputs (pins 20, 17 and 14)						
$I_{O(b-w)}$	signal current (black-to-white)		–	50	–	mA
		with peaking (note 2)	–	100	–	mA
THD	total harmonic distortion	output swing = 1 V	–	–	1	%
Feedback input						
V_{int}	internal reference voltage		–	5.8	–	V
$I_{18,15,12}$	output current		–	–	–1	µA
Threshold voltages (note 3)						
V_{11}	threshold voltage for blanking		1.0	1.4	1.7	V
	threshold voltage for clamping		2.6	3.0	3.3	V
	threshold voltage for switch off		4.5	5.0	5.2	V
I_{11}	current		–	–	± 100	µA
t_{w11}	width of clamping pulse		1	–	–	µs

Notes to the characteristics

1. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):

$$\frac{\text{peak-to peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$$

2. The external RC combinations at pins 19, 16 and 13 enables peak currents during transients.
3. The internal threshold voltages are derived from an internally stabilized voltage.

Advanced monitor video controller TDA4881

FEATURES

- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 2 channels only
- Brightness control with correct grey scale tracking
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible

GENERAL DESCRIPTION

The TDA4881 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA4851.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	46	56	mA
$V_{I(b-w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b-w)}$	output voltage (black-to-white, pins 19, 16 and 13)	nominal contrast and nominal gain	–	0.8	–	V
$I_{O(b-w)}$	output current (black-to-white, pins 20, 17 and 14)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	–	–	MHz
G_{nom}	nominal gain		–	1	–	dB
G_v	gain control range for 2 channels (relative to G_{nom})		–4	–	+2	dB
C_v	contrast control range (relative to G_{nom})		–20	–	+3	dB
ΔV_{bl}	brightness control range	nominal gain	–80	–	+240	mV
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4881	20	DIL	plastic	SOT146

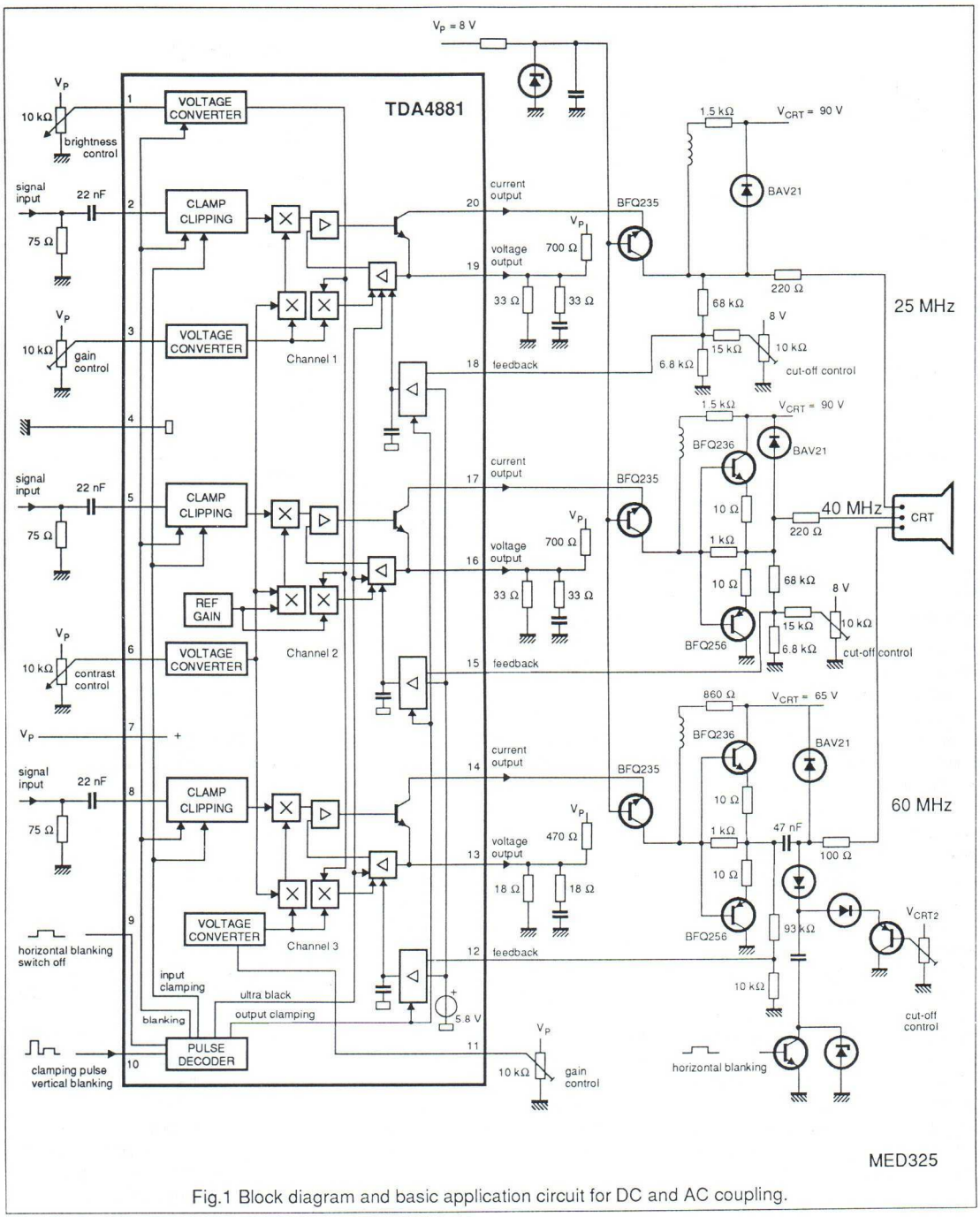


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

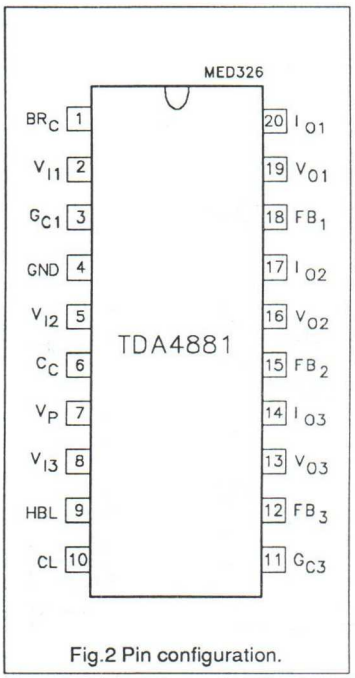


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
BR_C	1	brightness control
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch off
CL	10	input clamping, vertical blanking
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

FUNCTIONAL DESCRIPTION

RGB input signals (0.7 $V_{(p-p)}$) are capacitively coupled into the TDA4881 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Channels 1 and 3 have a maximum total voltage gain of 6 dB (maximum contrast and maximum individual channel gain), Channel 2 of 4 dB (maximum contrast and nominal channel gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.8 $V_{(p-p)}$.

DC voltages are used for brightness, contrast and gain control.

Brightness control yields a simultaneous signal black level shift of the three channels relative to a reference black level. For nominal brightness (pin 1 open-circuit) the signal black level is equal to the reference black level.

Contrast control is achieved by a voltage at pin 6 and affects the three channels simultaneously.

To provide the correct white point, an individual *gain control* (pins 3 and 11) adjusts the signals of Channels 1 and 3 compared to the reference Channel 2. Gain setting effects contrast and brightness to achieve correct grey scale tracking.

Each *output stage* provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply.

The three channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

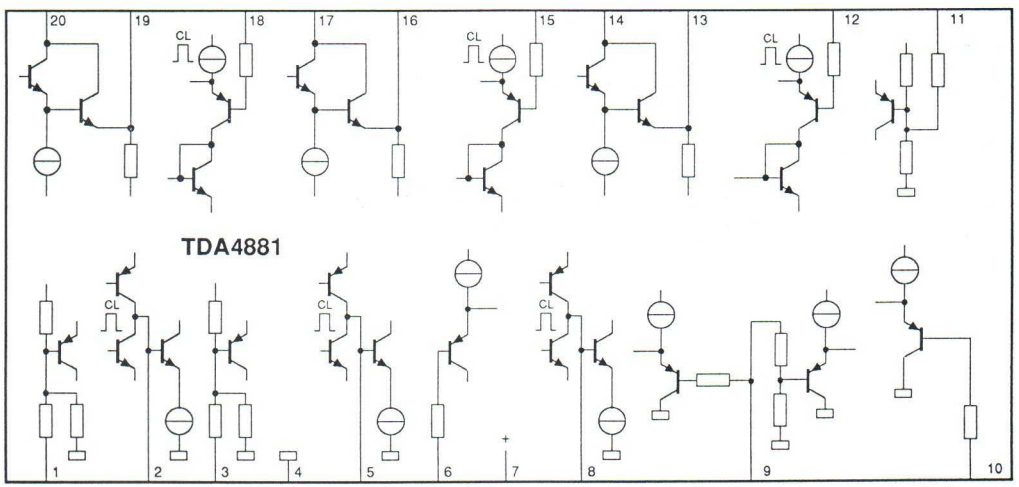
The *clamping pulse* (pin 10) is used for *input clamping* only. The input signals have to be at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V (1 V to 3.5 V).

The *vertical blanking pulse* will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 300 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled to

avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted instead. Additionally the brightness is internally set to its nominal value, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization.

During *horizontal blanking* (pin 9) the output signal is set to reference black level as previously described and *output clamping* is activated. If the voltage at pin 9 exceeds the *switch off* threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during V-flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For *cut-off stabilization* (DC coupling to the CRT) respectively *black level stabilization* (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.



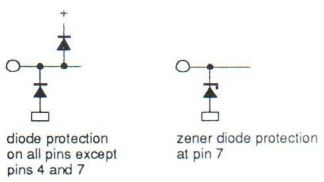


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_i	input voltage range (pins 2, 5 and 8)	−0.1	V_P	V
V_{ext}	external DC voltage ranges			
	pins 20, 17 and 14	−0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	−0.1	V_P	V
	pin 9	−0.1	$V_P + 0.7$	V
	pin 10	−0.7	$V_P + 0.7$	V
I_o	average output current (pins 20, 17 and 14)	0	50	mA
I_M	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−500	+500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 8.0 V, T_{amb} = +25 °C; all voltages measured to GND (pin 4); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	46	56	mA
Video signal inputs						
$V_{I(b-w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$I_{2, 5, 8}$	DC current	no clamping	–0.1	–	0.1	µA
		during clamping	±50	–	–	µA
Brightness control						
V_1	input voltage range	see note 1	1.0	–	6.0	V
R_1	input resistance to V_{N1}		–	50	–	kΩ
ΔV_{bl1}	black level voltage change at nominal gain (pins 19, 16 and 13)	V_1 = 1.0 V; $V_{3, 11}$ open-circuit	–	–80	–	mV
		V_1 = 6.0 V; $V_{3, 11}$ open-circuit	–	240	–	mV
V_{N1}	input voltage for nominal brightness	pin 1 open-circuit	–	2.25	–	V
Contrast control (see note 2)						
V_6	input voltage range	see note 1	1.0	–	6.0	V
I_6	current		–5	–1	–	µA
C_v	contrast relative to nominal contrast	V_6 = 6.0 V; $V_{3, 11}$ open-circuit	–	3	–	dB
		V_6 = 4.5 V; $V_{3, 11}$ open-circuit	–	0	–	dB
		V_6 = 1.0 V; $V_{3, 11}$ open-circuit	–	–20	–	dB
Tr	tracking of RGB signals	2.5 V < V_6 < 6 V; $V_{3, 11}$ open-circuit	–	0	0.5	dB
Gain control						
$V_{3, 11}$	input voltage range	see note 1	1.0	–	6.0	V
$R_{3, 11}$	input resistance against $V_{N3, N11}$		–	43	–	kΩ
G_v	gain relative to nominal gain	V_6 = 4.5 V; $V_{3, 11}$ = 6 V	–	2	–	dB
		V_6 = 4.5 V; $V_{3, 11}$ = 1 V	–	–4	–	dB
$V_{N3, N11}$	input voltage for nominal gain	pin 3, 11 open-circuit	–	4.6	–	V
Feedback input						
V_{int}	internal reference voltage	see note 3	tbn	5.8	tbn	V
$I_{18, 15, 12}$	output current	during output clamping	–1.5	–1.0	–0.1	µA
Voltage outputs (pins 19, 16 and 13)						
$V_{O(b-w)}$	signal output voltage (black-to-white value)	$V_{3, 11}$ open; V_6 = 4.5 V; $V_{I(b-w)}$ = 0.7 V	–	0.8	–	V
V_{bl}	black level voltage	during output clamping; depending on black level adjustment; see note 4	0.3	–	1.0	V
		during switch-off	–	0.1	0.3	V
S/N	signal-to-noise ratio	see note 5	–	–	44	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at voltage outputs						
G_{vf}	gain decrease by frequency response at pins 19, 16 and 13	70 MHz	–	–	–3	dB
t_{rO}	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.5	5.0	ns
Current outputs (pins 20, 17 and 14)						
$I_{O(b-w)}$	signal current (black-to-white)		–	50	–	mA
		with peaking; see note 6	–	–	100	mA
$V_{20-19,\ 17-16,\ 14-13}$	HF saturation of output transistors	I_O = 50 mA	–	–	2.0	V
		I_O = 100 mA	–	–	2.2	V
Threshold voltages (see note 7)						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance referenced to ground		50	80	110	kΩ
t_{d9}	delay between horizontal blanking input and output signal blanking		–	35	60	ns
V_{10}	threshold for vertical blanking (blanking, no input clamping)	see Fig.4	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	see Fig.4	2.6	3.0	3.5	V
I_{10}	input current		–3	–1	–	μA
$t_{r,f10}$	rise and fall time for clamping pulse	transition 1 to 3.5 V; see Fig.4	–	–	75	ns/V
t_{w10}	clamping pulse width	V_{10} = 3 V	0.6	–	–	μs
t_{d10}	delay between vertical blanking input and output signal blanking	see Fig.4	–	300	–	ns

Notes to the characteristics

1. Typical range is 1 to 6 V, the range can be increased (e.g. 0 to 7 V) to slightly increase the control range.
2. Open contrast control pin leads to undefined contrast setting.
3. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping in closed feedback loop.
4. Minimum guaranteed control range, the typical minimum black level voltage is 0.1 V.
5. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):
   $\frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$
6. The external RC combinations at pins 19, 16 and 13 enables peak currents during transients.
7. The internal threshold voltages are derived from an internally stabilized voltage. The internal pulses are generated if the input pulses are higher than the thresholds.

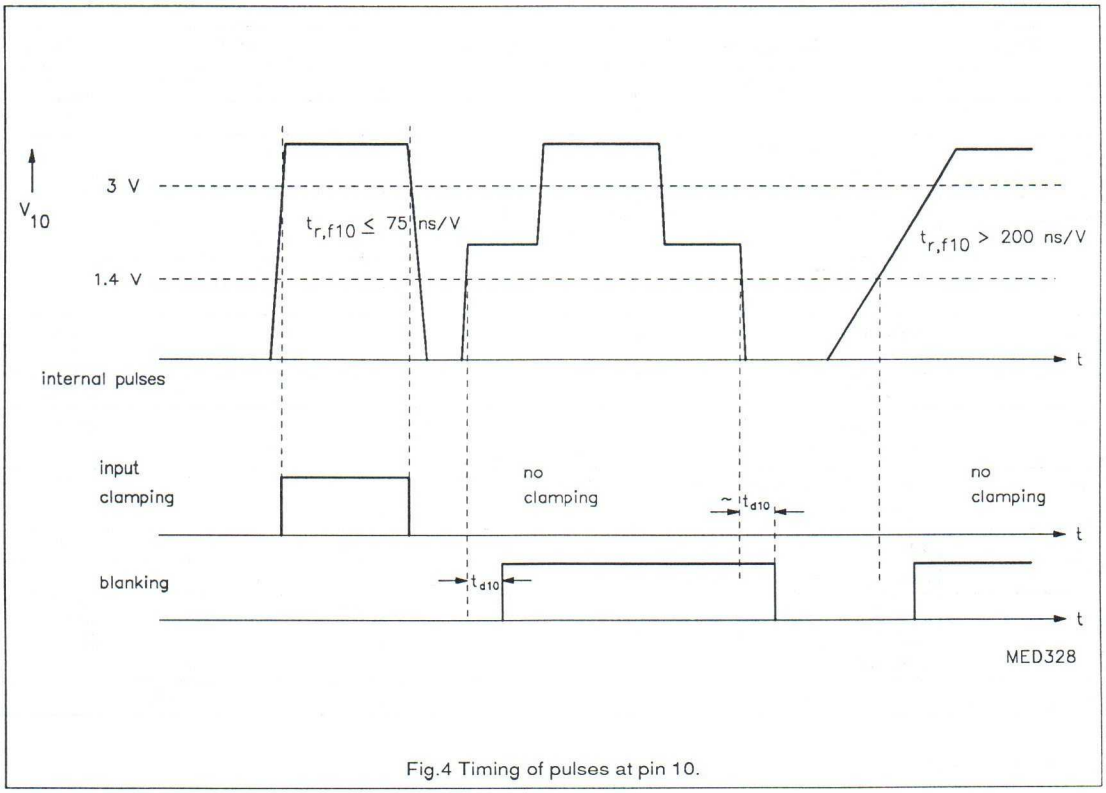


Fig.4 Timing of pulses at pin 10.

Advanced monitor video controller for OSD TDA4882

FEATURES

- 85 MHz video controller
- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 2 channels only
- Brightness control with correct grey scale tracking
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible
- OSD application very easily.

GENERAL DESCRIPTION

The TDA4882 is an RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT.

With special advantages the circuit can be used in conjunction with the TDA485X monitor deflection IC family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	48	–	mA
$V_{I(b-w)}$	input voltage (black-to-white; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b-w)}$	output voltage (black-to-white; pins 19, 16 and 13)	nominal contrast; pins 3 and 11 open-circuit	–	0.79	–	V
$I_{O(b-w)}$	output current (black-to-white; pins 20, 17 and 14)		–	50	–	mA
I_{OM}	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	85	–	MHz
G_{nom}	nominal gain (pins 2, 5 and 8 to pins 19, 16 and 13)	nominal contrast; pins 3 and 11 open-circuit	–	1	–	dB
ΔG	gain control difference for 2 channels	relative to G_{nom}	–5	–	+2.6	dB
C_c	contrast control	V_6 = 1 to 6 V	–22	–	+3.4	dB
C_{OSD}	minimum contrast for OSD	V_6 = 0.7 V	–	–40	–	dB
ΔV_{bl}	brightness control related to nominal output signal amplitude		–11	–	+34	%
T_{amb}	operating ambient temperature		–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4882	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

BLOCK DIAGRAM

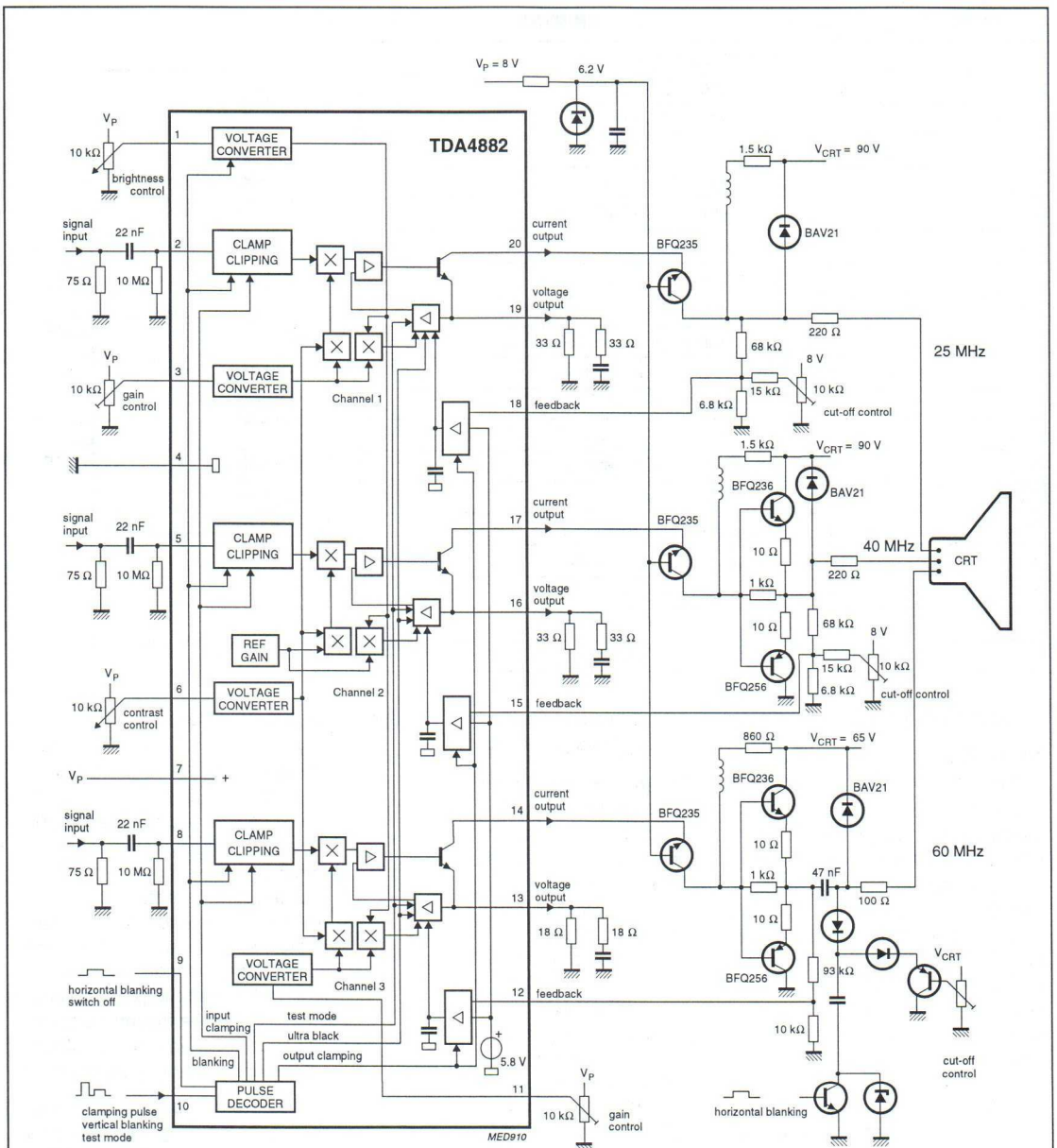


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

PINNING

SYMBOL	PIN	DESCRIPTION
BR_C	1	brightness control
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control, OSD switch
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch-off
CL	10	input clamping, vertical blanking, test mode
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

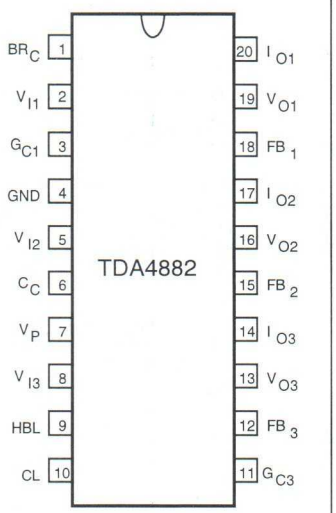


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The RGB input signals 0.7 V (p-p) are capacitively coupled into the TDA4882 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Channels 1 and 3 have a maximum total voltage gain of 7 dB (maximum contrast and maximum individual channel gain), Channel 2 of 4.4 dB (maximum contrast and nominal gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.79 V (p-p).

DC voltages are used for brightness, contrast and gain control.

Brightness control yields a simultaneous signal black level shift of the three channels relative to a reference black level. For nominal brightness (pin 1 open-circuit) the signal black level is equal to the reference black level. **Contrast control** is achieved by a voltage at pin 6 and affects the three channels simultaneously. To provide the correct white point, an individual **gain control** (pins 3 and 11) adjusts the signals of Channels 1 and 3 compared to the reference Channel 2. Gain setting changes contrast as well as brightness to achieve correct grey scale tracking.

Each **output stage** provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply. The channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The **clamping pulse** (pin 10) is used for **input clamping** only. The input signals have to be at black level during the clamping pulse and are

clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V during transition from 1 V to 3.5 V.

The **vertical blanking pulse** will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 320 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled in order to avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted instead. Additionally the brightness is internally set to its nominal value, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization (see below).

During **horizontal blanking** (pin 9) the output signal is set to reference black level as previously described and **output clamping** is activated. If the voltage at pin 9 exceeds the **switch-off** threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during V-flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For **cut-off stabilization** (DC coupling to the CRT) respectively **black level stabilization** (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.

For OSD fast switching of control pin 6 to less than 1 V (e.g. 0.7 V) blanks the input signals. The OSD signals can easily be inserted to the external cascode transistor (see Fig.3).

During **test mode** (pins 9 and 10 connected to V_P) the black levels at the voltage outputs (pins 19, 16 and 13) are internally set to typical 0.5 V nominal brightness, 3 V DC at signal inputs (pins 2, 5 and 8).

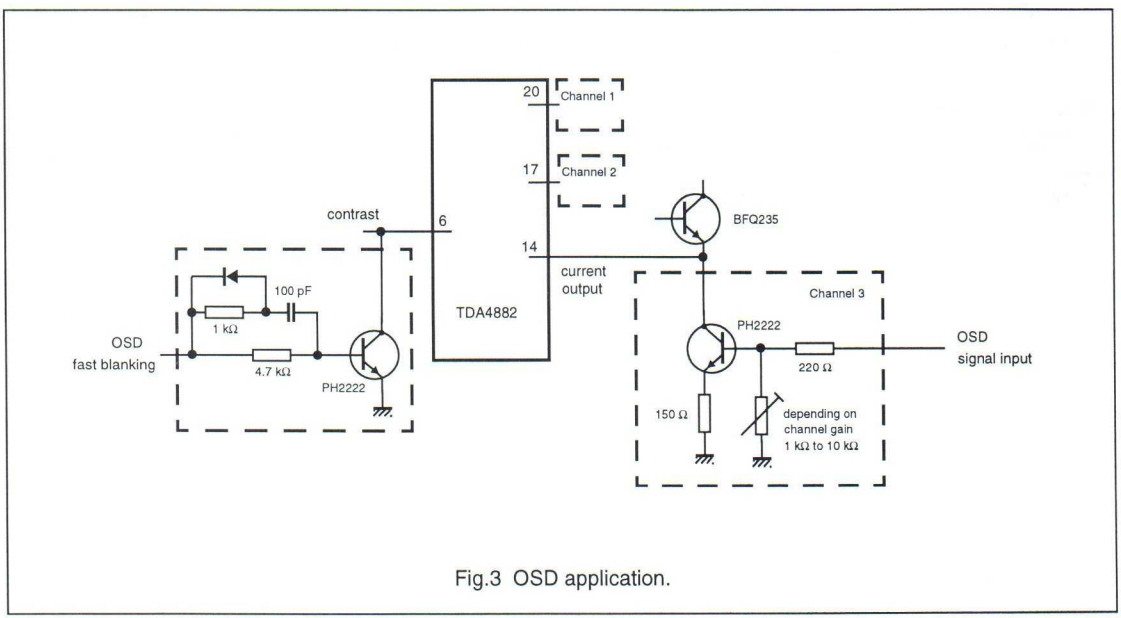


Fig.3 OSD application.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_I	input voltage (pins 2, 5 and 8)	−0.1	V_P	V
V_{ext}	external DC voltage			
	pins 20, 17 and 14	−0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	−0.1	V_P	V
	pin 9	−0.1	V_P + 0.7	V
	pin 10	−0.1	V_P + 0.7	V
$I_{O(AV)}$	average output current (pins 20, 17 and 14; note 1)	0	50	mA
I_{OM}	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C
T_j	junction temperature	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	−500	+500	V

Notes

1. Signal amplitude of 50 mA black-to-white is possible if the average current (including blanking times and signal variation against time) does not exceed 50 mA. The maximum power dissipation of 1200 mW has to be considered.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R_{thj-a}	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = +25 °C; all voltages measured to GND (pin 4); note 1; see also Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		36	48	60	mA
Video signal inputs (Channel 1: pin 2, Channel 2: pin 5 and Channel 3: pin 8)						
$V_{I(b\text{-}w)}$	input voltage (black-to-white value; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{I(cl)2, 5, 8}$	DC voltage during input clamping (artificial black + V_{BE})		2.8	3.1	3.4	V
$I_{I2, 5, 8}$	DC input current	no clamping; $V_{I2, 5, 8} = V_{I(cl)2, 5, 8}$; T_{amb} = –20 to +70 °C	–0.05	+0.05	+0.250	µA
		during clamping; $V_{I2, 5, 8} = V_{I(cl)2, 5, 8} \pm 0.7$ V	±50	±75	±120	µA
Brightness control (pin 1); note 2; see Fig.5						
V_1	input voltage		1.0	–	6.0	V
R_1	input resistance		40	50	60	kΩ
$V_{1(nom)}$	input voltage for nominal brightness	pin 1 open-circuit	2.0	2.25	2.5	V
ΔV_{bl}	black level voltage change at voltage outputs referred to reference black level during output clamping (V_9 > 1.6 V) related to output signal amplitude with nominal 0.7 V (p-p) input signal and nominal contrast (V_6 = 4.3 V) for any gain setting	V_1 = 1.0 V	–13	–11	–9.5	%
		V_1 = 6.0 V	30	34	37	%
		pin 1 open-circuit	–	–	0.8	%
ΔV_{BT}	difference of ΔV_{bl} between any two channels		–	0	±1.2	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Contrast control (pin 6); note 3; see Fig.6						
V_6	input voltage		1.0	–	6.0	V
$V_{6(max)}$	maximum input voltage		–	–	$V_P - 1$	V
$V_{6(nom)}$	input voltage for nominal contrast	note 4	–	4.3	–	V
I_6	input current	$V_6 = 4.3$ V	–5	–1	–0.1	µA
C_c	contrast relative to nominal contrast	$V_6 = 6.0$ V; pins 3 and 11 open-circuit	2.4	3.4	–	dB
		$V_6 = 1.0$ V; pins 3 and 11 open-circuit	–26	–22	–19	dB
$V_{6(min)}$	input voltage for minimum contrast	pins 3 and 11 open-circuit	–	0.7	–	V
TR_O	tracking of output signals of Channels 1, 2 and 3	$1 V < V_6 < 6$ V; note 5	–	0	0.5	dB
t_{dfC}	delay between leading edges (falling) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	$V_6 = 4.3$ V to 0.7 V; input fall time at pin 6: $t_{fCC} = 2$ ns; Fig.7; note 6	–	7	20	ns
t_{drC}	delay between trailing edges (rising) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	$V_6 = 0.7$ V to 4.3 V; input rise time at pin 6: $t_{rCC} = 2$ ns; Fig.7; note 6	–	15	25	ns
t_{fC}	fall time of output signals at voltage outputs (pins 19, 16 and 13)	90% to 10% amplitude; input fall time at pin 6: $t_{fCC} = 2$ ns; Fig.7; note 6	–	6	15	ns
t_{rC}	rise time of output signals at voltage outputs (pins 19, 16 and 13)	10% to 90% amplitude; input rise time at pin 6: $t_{rCC} = 2$ ns; Fig.7; note 6	–	6	15	ns
Gain control (pin 3 for Channel 1 and pin 11 for Channel 3); Fig.8; note 7						
$V_{3, 11}$	input voltage		1.0	–	6.0	V
$V_{3, 11(nom)}$	input voltage for nominal gain	pins 3 and 11 open-circuit	3.6	3.75	3.95	V
$R_{3, 11}$	input resistance		44	55	66	kΩ
ΔG	gain control difference relative to nominal gain (Channels 1 and 3 only)	$V_6 = 4.3$ V; $V_{3, 11} = 6$ V	2	2.6	3.3	dB
		$V_6 = 4.3$ V; $V_{3, 11} = 1$ V	–5.5	–5	–4.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Feedback input (Channel 1: pin 18, Channel 2: pin 15 and Channel 3: pin 12); Fig.9; note 8						
V_{ref}	internal reference voltage		5.6	5.8	6.1	V
$I_{O18, 15, 12(max)}$	maximum output current	during output clamping; $V_{18, 15, 12} = 3$ V	−500	−100	−60	nA
$\Delta V_{bl(CRT)}$	black level variation at CRT	note 9	0	40	200	mV
$\Delta V_{ref(T)}$	variation of V_{ref} in the temperature range	$T_{amb} = -20$ to +70 °C	0	20	50	mV
$\Delta V_{ref(VP)}$	variation of V_{ref} with supply voltage	7.2 V ≤ V_P ≤ 8.8 V	0	60	100	mV
Voltage outputs (Channel 1: pin 19, Channel 2: pin 16 and Channel 3: pin 13)						
$V_{O(b-w)}$	nominal signal output voltage (black-to-white value)	pins 3 and 11 open-circuit; $V_6 = 4.3$ V; $V_{I(b-w)} = 0.7$ V	0.69	0.79	0.89	V
$V_{blx(max)}$	maximum adjustable black level voltage	during output clamping; $T_{amb} = -20$ to +70 °C	1	1.2	1.4	V
$V_{bl(SO)}$	black level voltage during switch-off, equal to minimum adjustable black level voltage	$V_9 = V_P$; $R_O = 33\ \Omega$; $T_{amb} = -20$ to +70 °C	30	45	100	mV
$V_{bl(TST)}$	black level voltage during test mode	$V_9 = V_P$; $V_{10} = V_P$; pin 1 open-circuit; $V_{I2, 5, 8} = V_{I(cl)2, 5, 8}$; note 10	0.3	0.7	1.2	V
S/N	signal-to-noise ratio	note 11	–	50	44	dB
$d_{O(th)}$	output thermal distortion	$I_{O(b-w)} = 50$ mA; note 12	–	0.6	1	%
$\Delta V_{bl(fl)}$	black level variation between clamping pulses	line frequency 30 kHz	–	0.5	4.5	mV
V_{off}	maximum offset during sync clipping	$V_{I2, 5, 8} < V_{I(cl)2, 5, 8}$; Fig.10; note 13	0	7	15	mV
$\Delta V_{O(b-w)(T)}$	variation of nominal output signal (black-to-white value) with temperature	pins 3 and 11 open-circuit; $V_6 = 4.3$ V; $V_{I(b-w)} = 0.7$ V; $T_{amb} = -20$ to +70 °C	0	2.5	10	%
Current outputs (Channel 1: pin 20, Channel 2: pin 17 and Channel 3: pin 14); note 14						
$I_{O(b-w)}$	output current (black-to-white value)		–	50	–	mA
		with peaking	–	–	100	mA
V_{20-19}; V_{17-16}; V_{14-13}	start of HF-saturation voltage of output transistors	$I_O = 50$ mA	–	–	2.0	V
		$I_O = 100$ mA	–	–	2.2	V
$I_{bl(SO)}$	output current during switch-off	$V_9 = V_P$; $R_O = 33\ \Omega$	0	20	900	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at voltage outputs (Figs 11, 12 and 13; note 15)						
$\Delta G_{(f)}$	gain decrease by frequency response at pins 19, 16 and 13	70 MHz; single channel	–	1.3	3	dB
$t_{r(O)}$	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.1	5.0	ns
dV_O	overshoot of output signal pulse related to actual output pulse amplitude	single channel; input rise time = 2.5 ns; $V_{I(b\text{-}w)}$ = 0.7 V; pins 3 and 11 open-circuit; V_6 = 4.3 V	–	4	8	%
Crosstalk at voltage outputs with speed up circuit (Figs 14, 15 and 16; note 16)						
$\alpha_{cr(tr)}$	transient crosstalk		–	–	0.1	–
Threshold voltages for clamping, blanking and switch-off (pins 9 and 10); note 17						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance	against ground	50	80	110	kΩ
t_{d9}	delay between horizontal blanking input and output signal blanking	input rise time at pin 9 > 100 ns; Fig.17; note 18	–	40	60	ns
V_{10}	threshold for vertical blanking (blanking, no input clamping)	Fig.18; note 19	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	Fig.18; note 19	2.6	3.0	3.5	V
	threshold for test mode (no clamping, no blanking, for $V_{bl(TST)}$ see above)	for test mode also V_9 > 6.8 V (switch-off)	$V_P - 1$	–	V_P	V
I_{10}	current	$V_{10} < V_P - 1$ V	–3	–1	–	µA
		$V_{10} \geq V_P - 1$ V	–	100	–	µA
$t_{r, f10}$	rise and fall time for clamping pulse	Fig.18; note 19	–	–	75	ns/V
t_{w10}	width of clamping pulse		0.6	–	–	µs
t_{d10}	delay between vertical blanking input and internal blanking	Fig.18; note 19	260	320	380	ns

Notes to the characteristics

1. Definition of levels:
   a) **Artificial black level**: internal signal level behind input emitter follower during input clamping and signal clipping. This level is inserted instead of the input signal during blanking.
   b) **Reference black level**: DC voltage during output clamping at voltage outputs, not influenced by brightness, contrast or gain setting, adjustable by cut-off stabilization.
   c) **Cut-off level**: corresponding DC voltage at CRT cathode in closed feedback loop.
   d) **Black level**: actual signal black level at either voltage outputs or cathode, can be adjusted by (brightness × gain), refers to reference black level or cut-off level respectively.
   e) **Ultra black level, switch-off level**: lowest adjustable reference black level, lowest signal level at voltage outputs.
   f) The minimum guaranteed control range for reference black level is 0.1 to 1 V.
   The ultra black level is depending on the external resistor R_O at voltage outputs (pins 13, 16 and 19) to ground.
   g) $V_{bl(SO)} \approx \frac{R_O}{3.5\ k\Omega + R_O} \times 4.65\ V$
2. Linear control range is 1 to 6 V for V_1, independent from supply voltage.
3. Linear control range is 1 to 6 V for V_6, independent from supply voltage. Open pin 6 leads to absolute maximum contrast setting. It is recommended to not exceed $V_6 = V_P - 1$ V in order to avoid saturation of internal circuitry. For $V_6 < V_{6(min)} \approx 0.7$ V a small negative signal (≈ -40 dB) will appear. For frequency dependency of contrast control see note 15.
4. Definition for nominal output signals: input $V_{I(b\text{-}w)} = 0.7$ V, gain pins 3 and 11 open-circuit, contrast control $V_6 = V_{6(nom)}$.
5. $Tr = 20 \times \text{maximum of } \left\{ \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2} \right) \right| ; \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3} \right) \right| ; \left| \log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3} \right) \right| \right\}$ [dB]
   A_x: signal output amplitude in Channel x at any contrast setting between 1 and 6 V.
   A_{x0}: signal output amplitude in Channel x at nominal contrast and same gain setting.
6. Typical step in contrast voltage and response at signal outputs for nominal input signal $V_{I(b\text{-}w)} = 0.7$ V (OSD fast blanking input/output).
7. Linear control range is 1 to 6 V for V_3 and V_{11}, independent from supply voltage.
8. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping ($V_9 = 2$ V) in closed feedback loop.
9. Slow variations of video supply voltage V_{CRT} (see Fig.1) will be suppressed at CRT cathode by cut-off stabilization. Change of V_{CRT} by 5 V leads to specified change of cut-off voltage.
10. The test mode allows testing without input and output clamping pulses. The signal inputs (pins 2, 5 and 8) have to be biased via resistors to the previously measured clamp voltages of approximately 3 V (artificial black level + V_{BE}). Signal and brightness blanking is not possible during test mode. The output currents (pins 10, 17 and 14) should be adjusted by resistors >> R_0 from voltage outputs to a positive voltage (e.g. V_P).
11. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):
    $\frac{S}{N} = 20 \log \frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$ [dB]
12. Large output swing e.g. $I_{O(b\text{-}w)} = 50$ mA leeds to signal depending power dissipation in output transistors. Thermal V_{BE} variation is compensated.
13. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level.

14. The output current approximately follows the equation $I_O = V_O\left(\frac{1}{R_O} + \frac{1}{2.2\ k\Omega}\right) - 500\ \mu A$ for $V_O > V_{bl(SO)}$ and with

    R_O = external resistor at voltage output to ground.

    The external RC combination at pins 19, 16 and 13 (see Fig.1) enables peak currents during transients.

15. Frequency response, crosstalk and pulse response have been measured at voltage outputs in a special printed-circuit board with 50 Ω line in/out connections and without peaking (see Chapter "Application information / test").

16. Crosstalk between any two output pins.

    a) **Input conditions**: one channel (Channel A) with nominal input signal and minimum rise time. The inputs of the other channels capacitively coupled to ground (Channel B). Gain pins 3 and 11 open-circuit.

    b) **Output conditions**: output signal of Channel A controlled by contrast setting (pin 6) to $V_{O(b\text{-}w)} = V_A = 0.7$ V, the rise time should be 5 ns. Output signal of Channel B then is $V_{O(b\text{-}w)} = V_B$.

    c) **Transient crosstalk**: $\alpha_{cr\,(tr)} = \frac{V_B}{V_A}$

    d) Crosstalk as a function of frequency has been measured without peaking circuit, with nominal input signal and nominal settings.

17. The internal threshold voltages are derived from a stabilized voltage. The internal pulses are generated while the input pulses are higher than the thresholds. Voltages of less than –0.1 V at pins 9 and 10 can influence black level control and should be avoided.

18. The delay between horizontal blanking input at pin 9 (HBL pulse) and output signal blanking as well as brightness blanking (ΔV_{bl}) at pins 19, 16 and 13 depends on the input rise time of the HBL pulse. The specified values for t_{d9} are valid for HBL rise times greater than 100 ns only.

19. For 75 ns/V < t_{rf10} < 240 ns/V generation of internal input clamping and blanking pulse is not defined. Any pulses not exceeding the threshold of input clamping (typical 3 V) will be detected as blanking pulse.

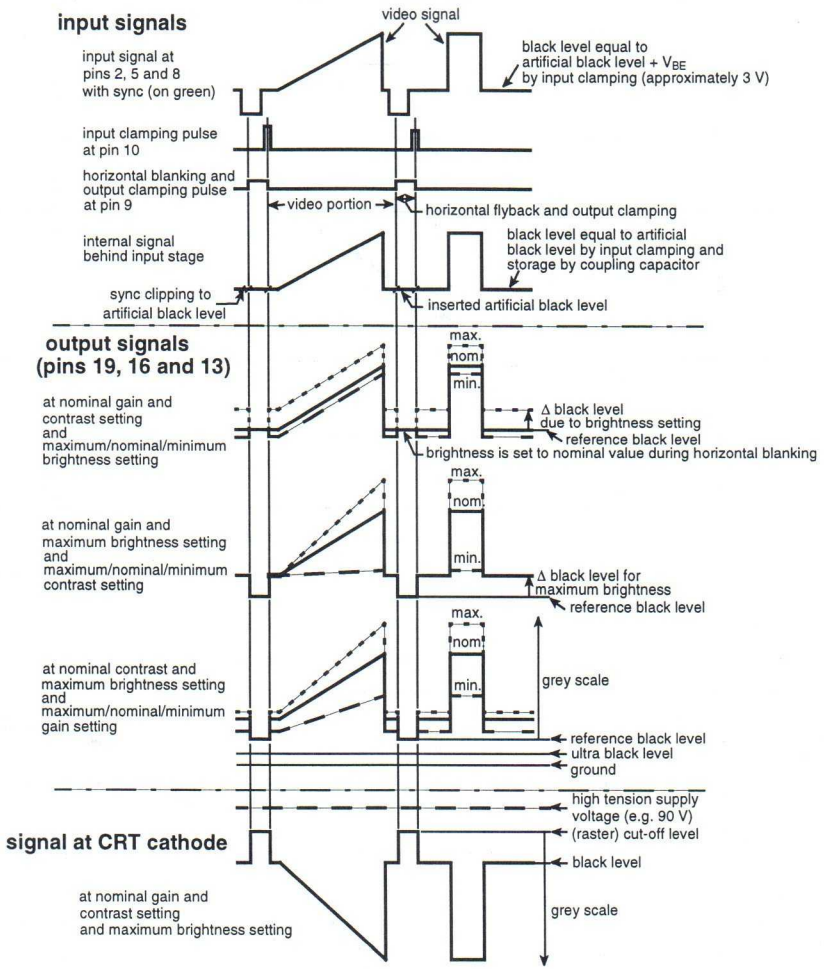


Fig.4 Signal processing.

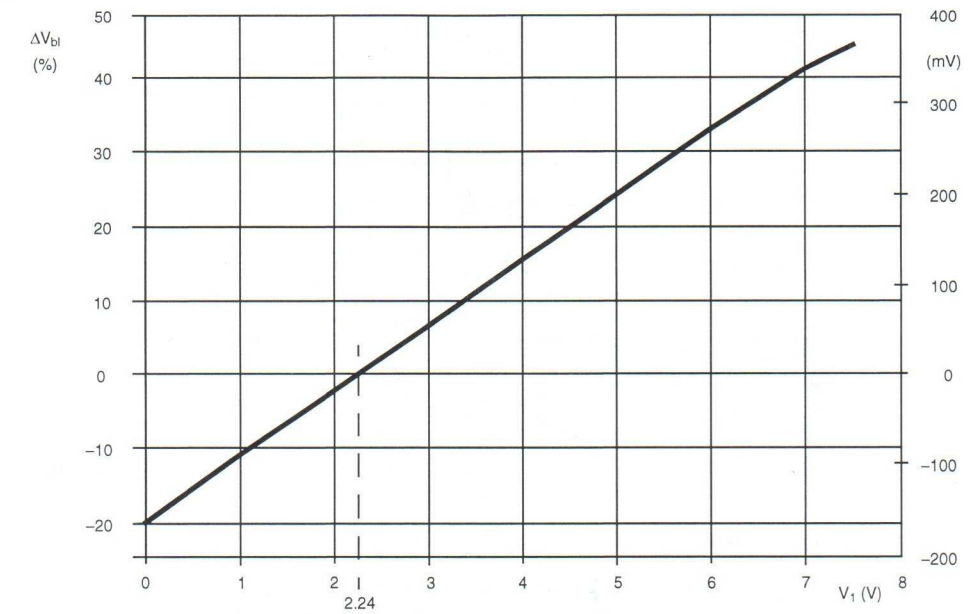


Fig.5 Typical brightness characteristic.

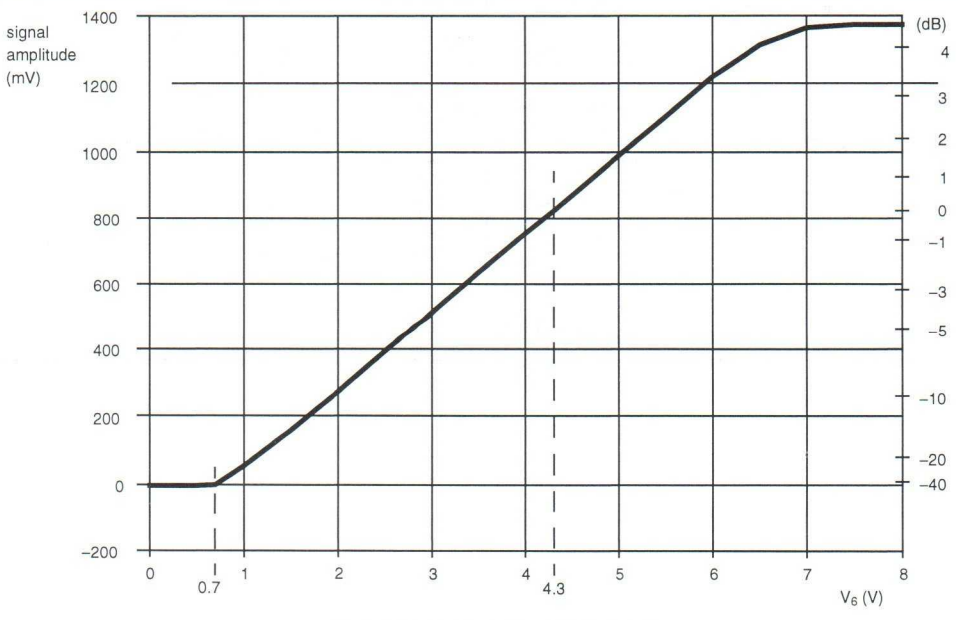


Fig.6 Typical contrast characteristic.

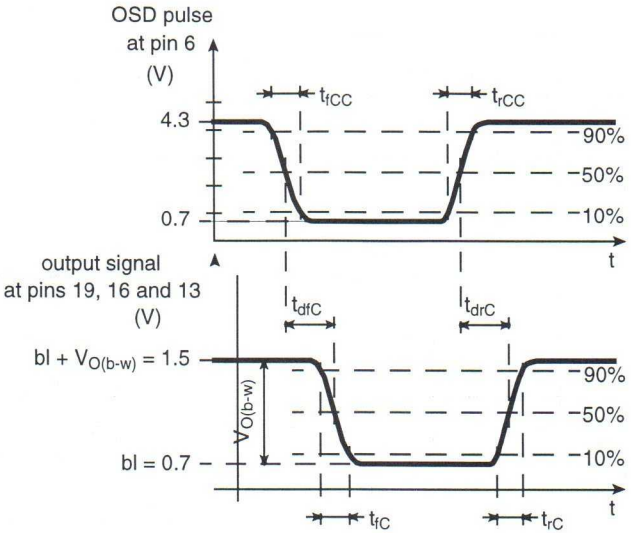


Fig.7 Typical OSD fast blanking input/output waveforms.

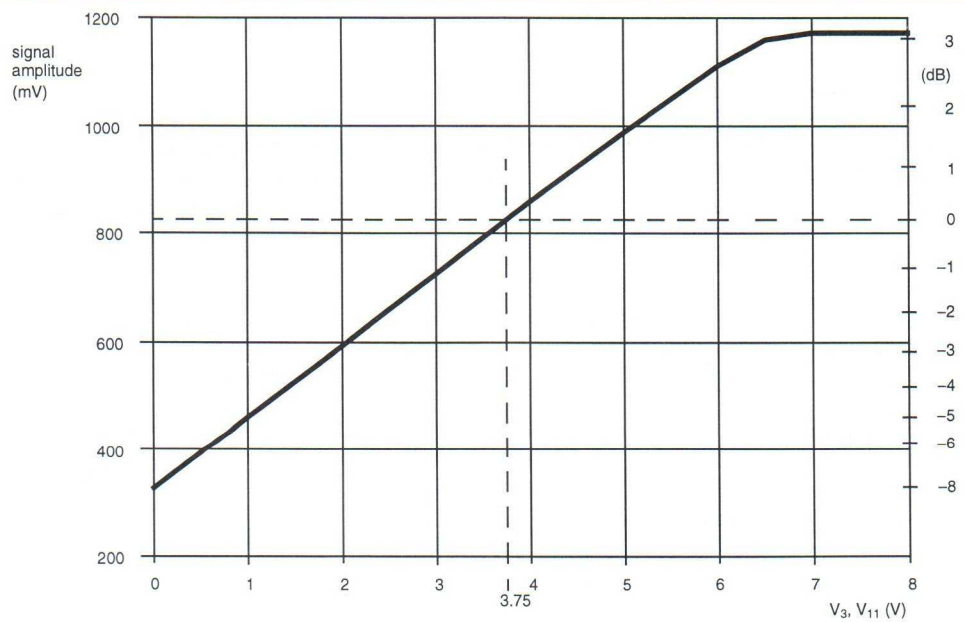
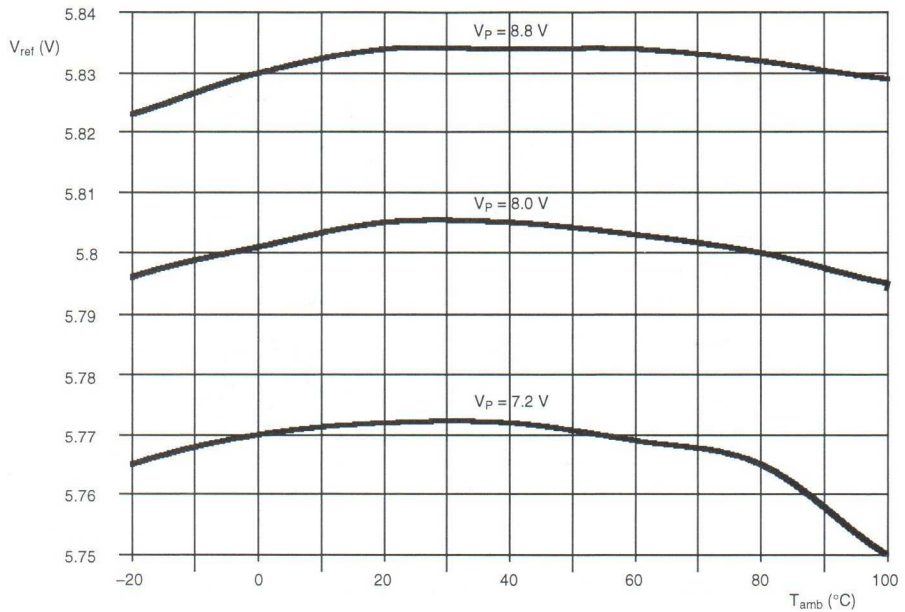
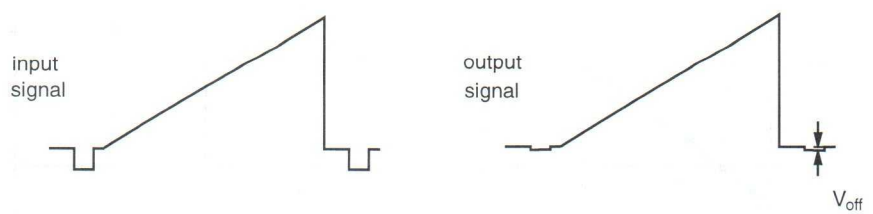


Fig.8 Typical gain characteristic.



Conditions: 0.5 V reference black level, no signal.

Fig.9 Typical variation of V_{ref} with temperature and power supply voltage.



e.g. with sync on green

Fig.10 Typical sync clipping.

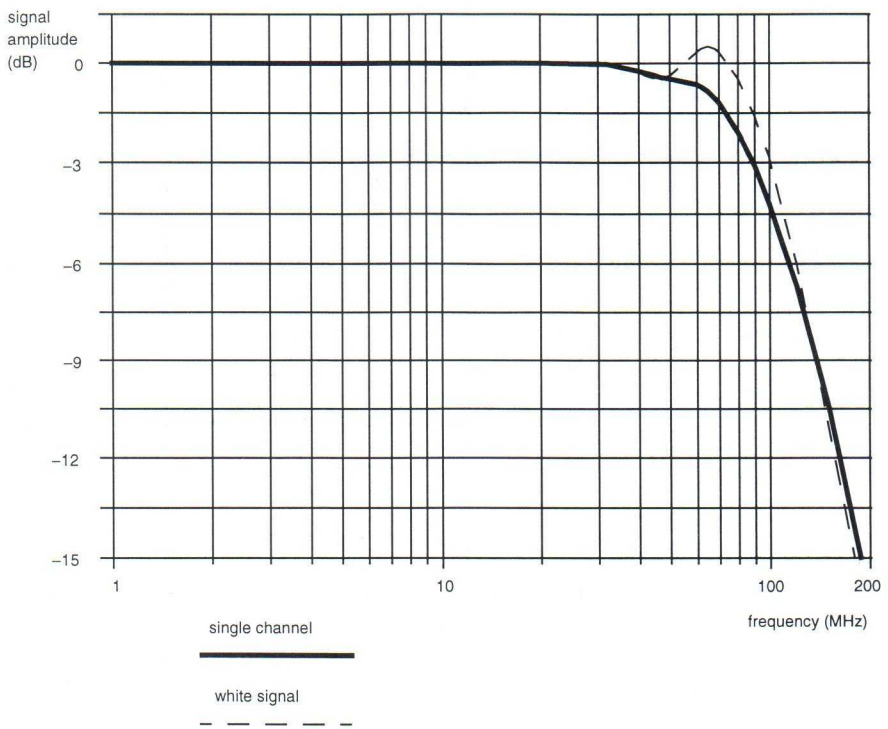


Fig.11 Typical frequency response.

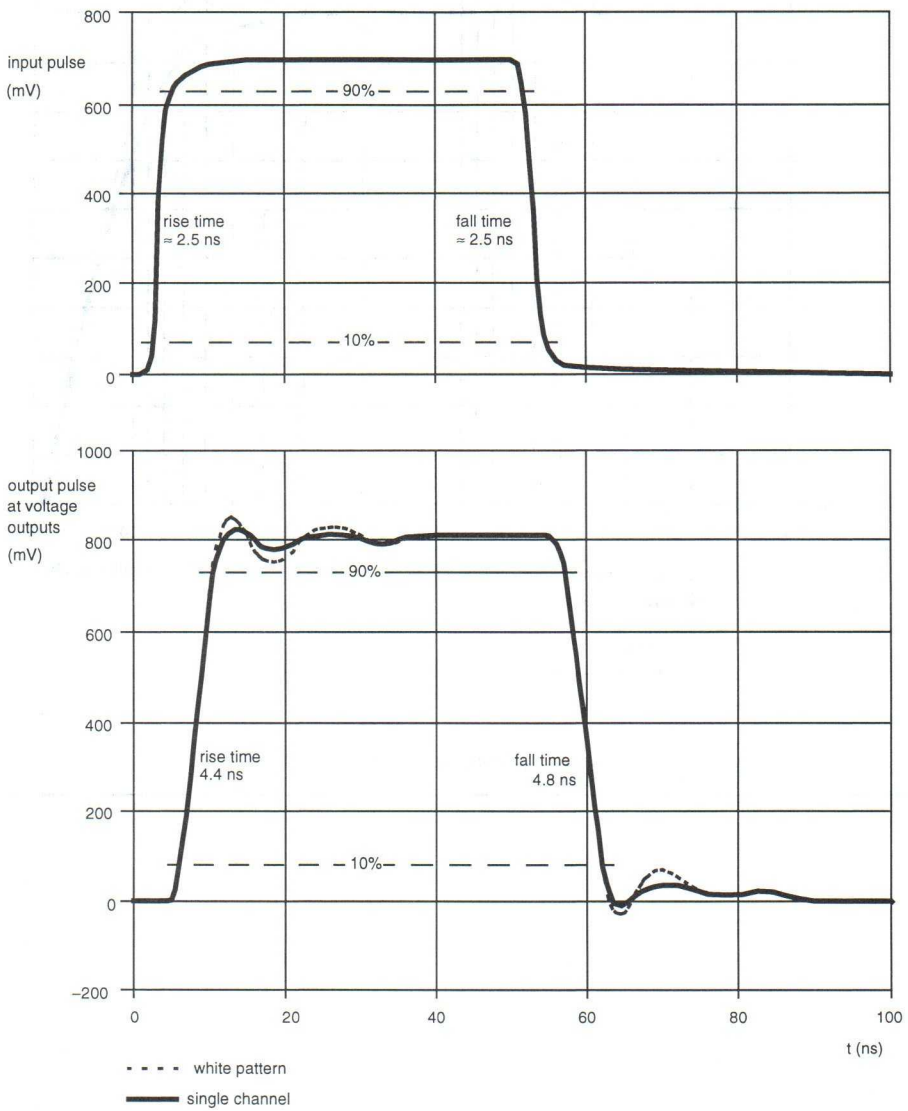


Fig.12 Typical pulse responses.

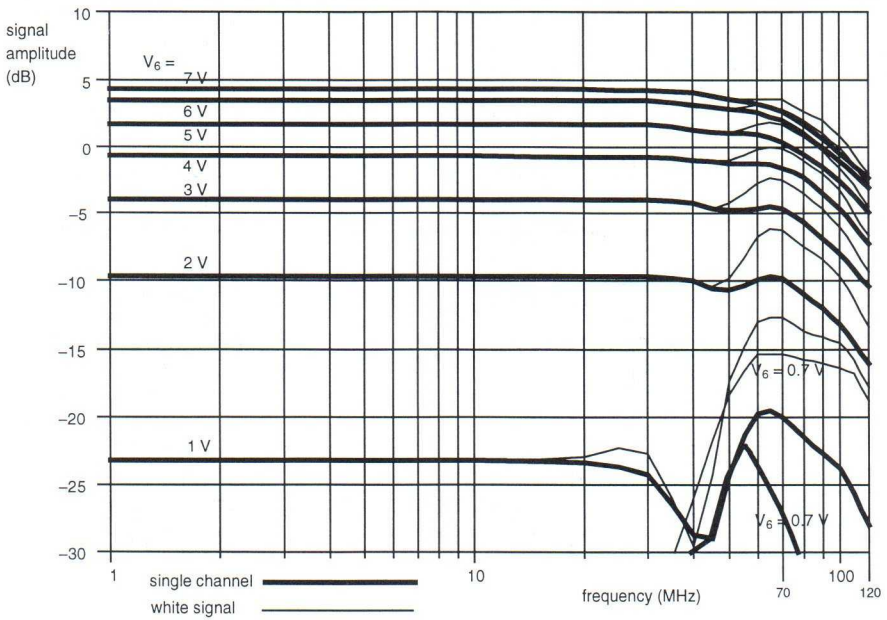


Fig.13 Typical characteristic of contrast control as a function of frequency.

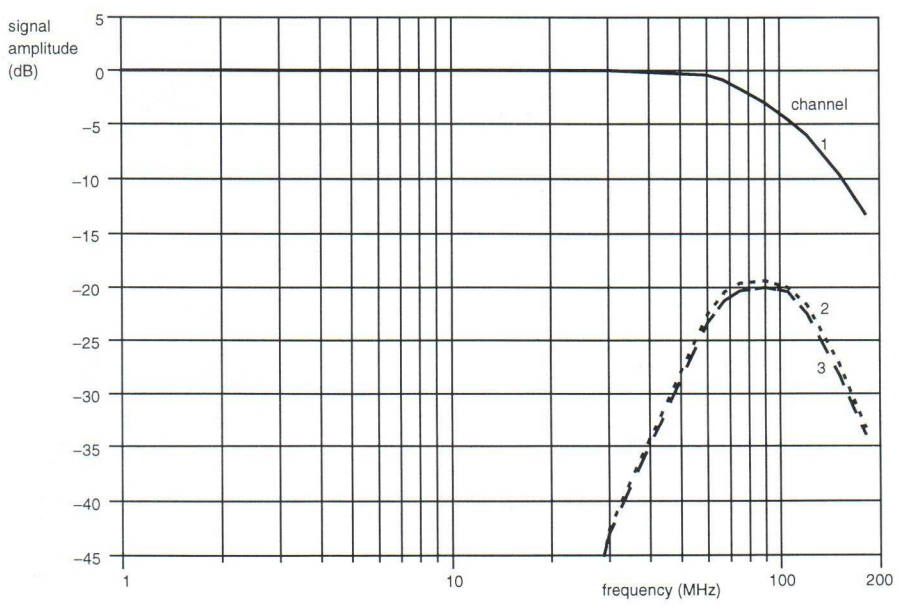


Fig.14 Typical crosstalk: Channel 1→ 2 and 3.

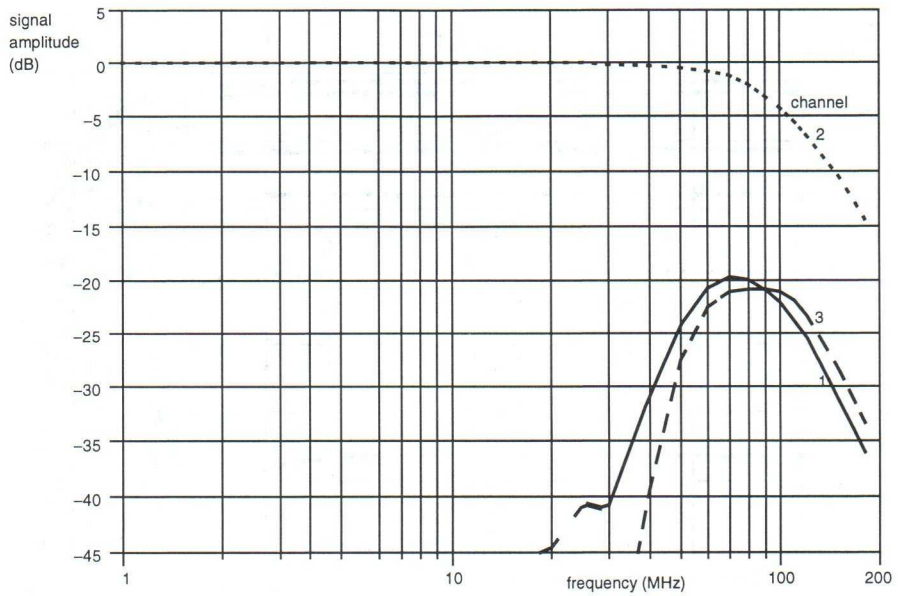


Fig.15 Typical crosstalk: Channel 2 → 1 and 3.

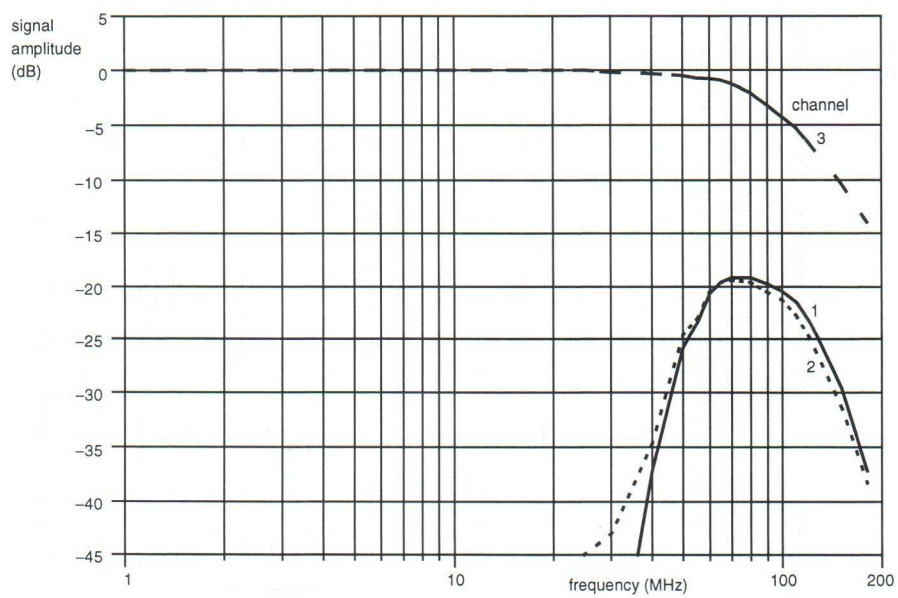


Fig.16 Typical crosstalk: Channel 3 → 1 and 2.

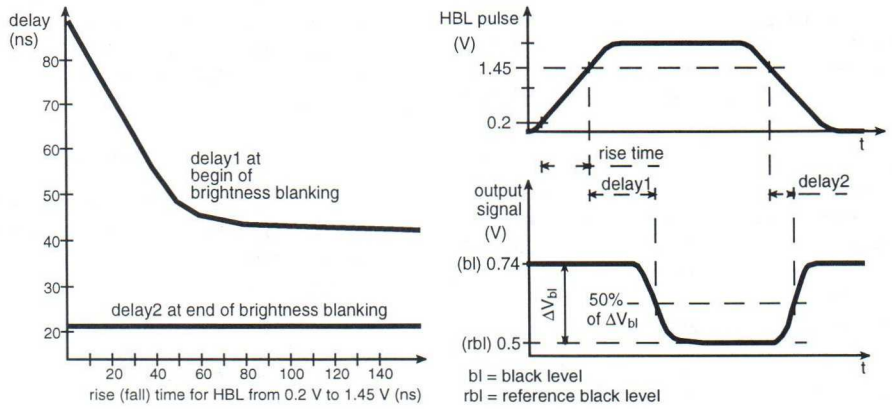


Fig.17 Typical delay between HBL pulse and brightness blanking at voltage outputs.

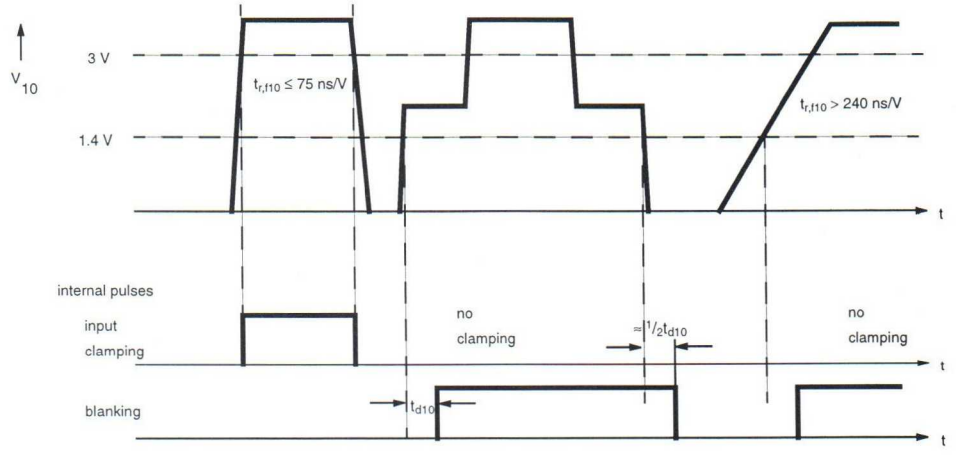


Fig.18 Timing of pulses at pin 10.

APPLICATION INFORMATION / TEST

For high frequency measurements a special application and printed-circuit board with only a few external components is built. Figure 19 shows the application circuit and Fig.20 the layout of the double sided printed board. All components on the rear (below) are of SMD type as well as R13, R14 and R15 on the front. Short HF loops and minimum crosstalk between the channels as well as input and output are achieved by properly shaped ground areas star connected to the IC ground pin.

The HF input signal can be fed to the subclick connectors X1, X2 and X3 by a 50 Ω line. The line is then terminated by a 51 Ω resistor on the board. With choice of jumper connections (JA1, JA2 and JA3) it is possible to connect channel inputs to its input connector, to connect all channels to one input connector (white pattern) and to ground each input via the coupling capacitor.

For operation without input clamping (e.g. test mode) the DC bias can be provided by VIDC (connector X21) if a short-circuit at JA4, JA5 and JA6 is made (solder short or small SMD resistor).

The output signal can be monitored via 50 Ω terminated lines at the voltage outputs (subclick connectors X4, X5 and X6). With 100 Ω in parallel to the 50 Ω terminated line the effective load resistance at the voltage outputs is 33 Ω.

The mismatch seen from the line towards the IC has no significant effect if the line is match terminated. A peaking circuit (C15, R16 Channel 1) can be added for realistic loading of the voltage outputs.

Black level adjustment is done by VIOS, UFBX (connector X21) and resistors R19, R22 and R25 (Channel 1). If R19 is equal to the effective load resistor at the voltage output the reference black level is approximately:

$$U_{REF} = VIOS - V(IO1) \text{ and}$$

$$V(IO1) = V_{int} + (V_{int} - UFBX) \times \frac{R22}{R25}$$

V_{int} is the internal reference voltage at the feedback input (typical 5.8 V). By this it is possible to adjust the reference black level and the voltage at the current outputs independently.

DC control for brightness, contrast and gain is prepared at connectors X21 and X22. Contrast control can also be set by the potentiometer P1 (jumper JA11). The series resistor R11 is necessary if fast OSD switching is activated via 50 Ω line (X10), a line termination can be done at the connector X9. Clamping and blanking pulses are fed to the IC via connectors X7 and X8. Connector X23 is used for power supply. The capacitors C7 and C8 should be located as near as possible to the IC pins.

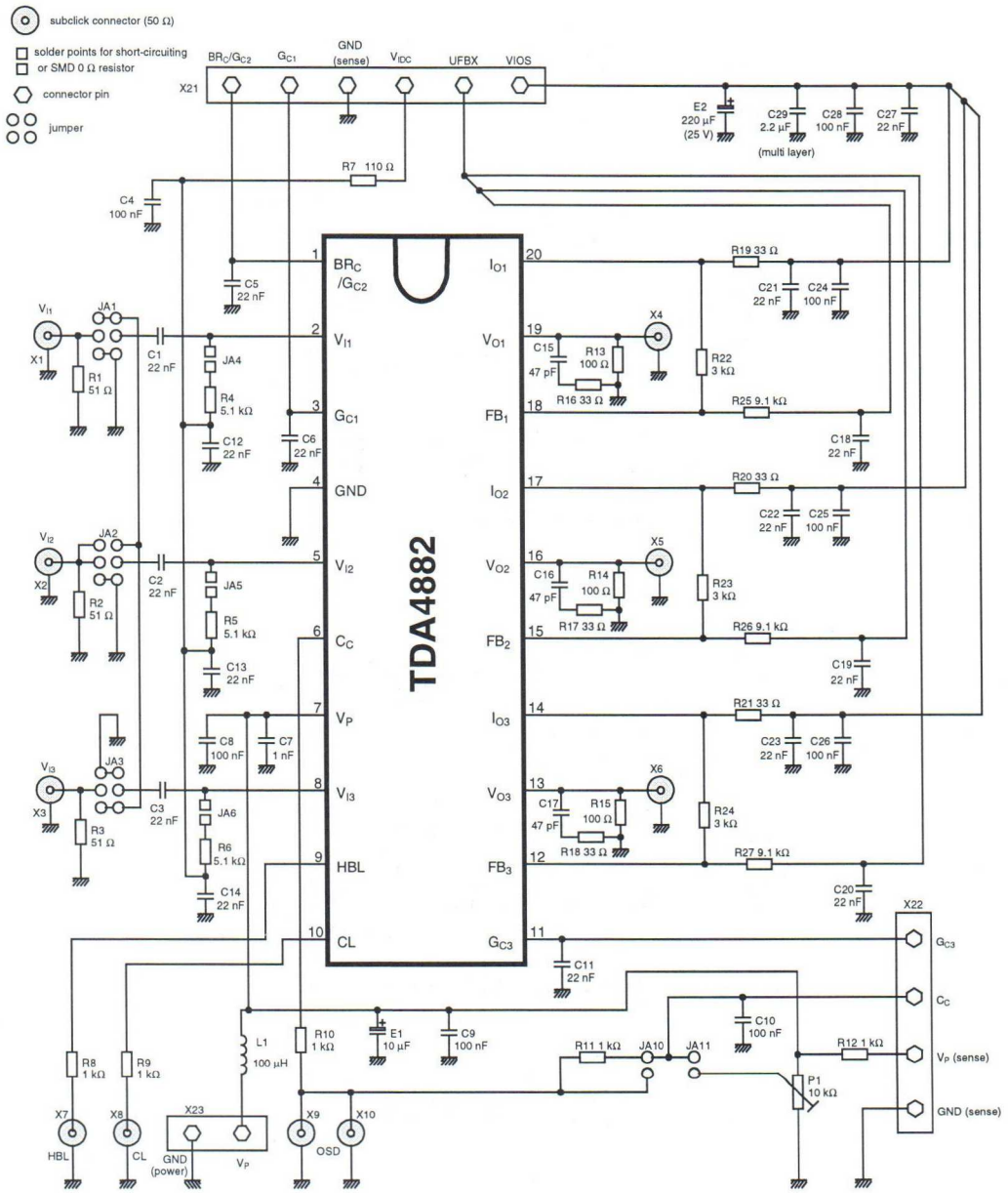


Fig.19 Application circuit for test PCB.

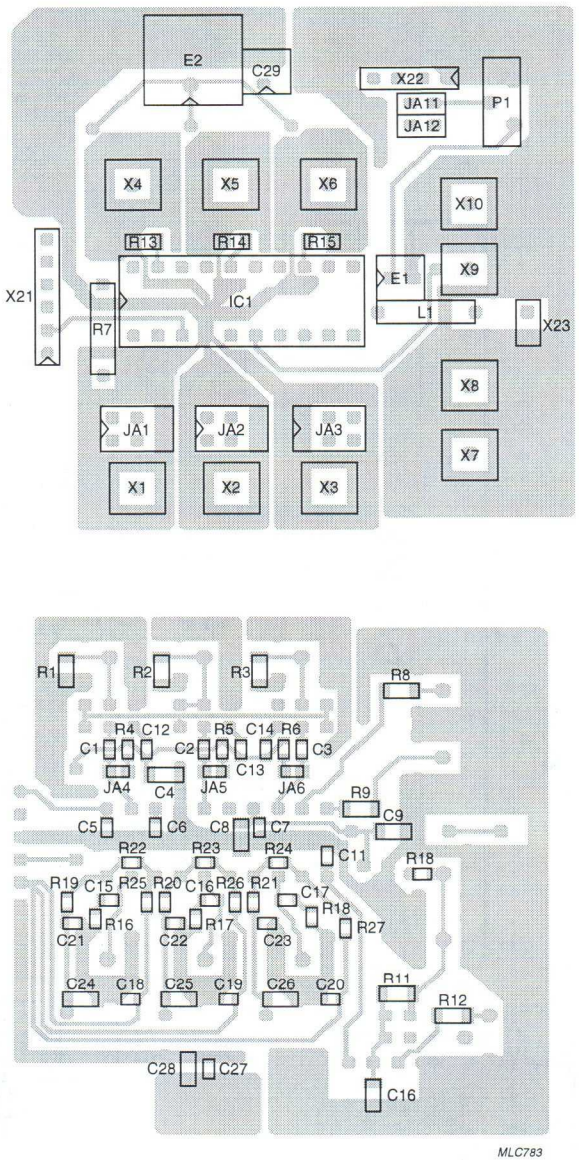


Fig.20 Double sided test PCB layout.

RECOMMENDATIONS FOR BUILDING THE APPLICATION BOARD

General

- Double-sided board
- Short HF loops by large ground plane on the rear.

Voltage outputs

- Capacitive loads as small as possible
- Short interconnection via resistor to ground.

Supply voltage

- Capacitors as near as possible to the pins
- Use of high-frequency capacitors (low self inductance, e.g. SMD).

Current outputs, emitter of cascode transistors

- The external interconnection inductivity can build a resonance together with the internal substrate capacity, a damping resistor of 10 to 30 Ω near to the IC pin can suppress such oscillations.

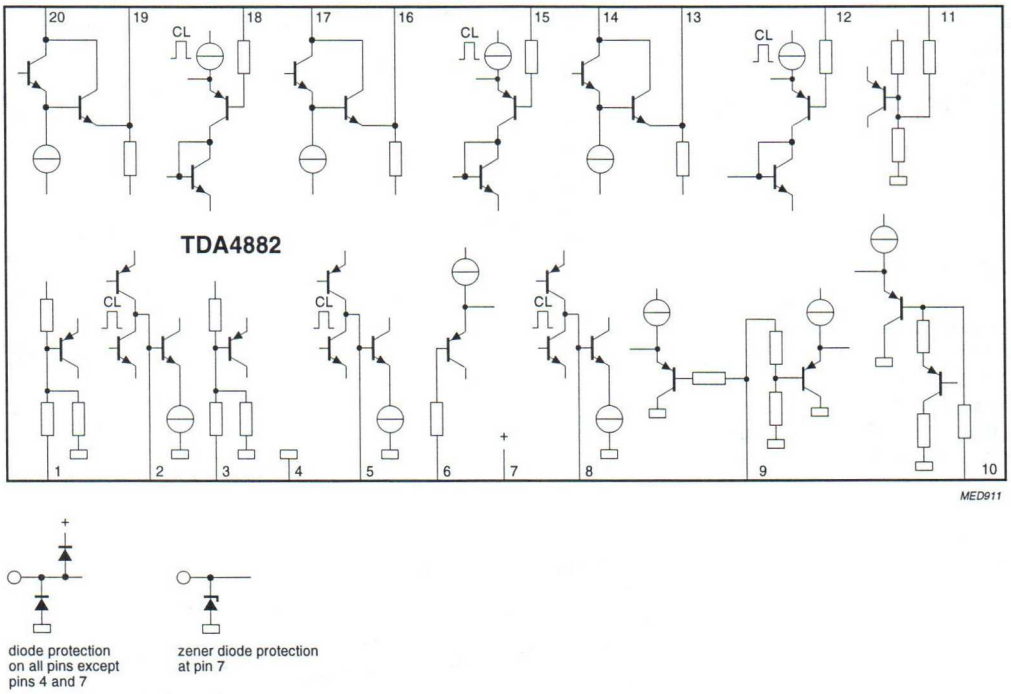


Fig.21 Internal circuits.

Three gain control video pre-amplifier TDA4883

FEATURES

- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 3 channels
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible.

GENERAL DESCRIPTION

The TDA4883 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA4851.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	46	56	mA
$V_{I(b\text{-}w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b\text{-}w)}$	output voltage (black-to-white, pins 19, 16 and 13)	nominal contrast and nominal gain	–	0.8	–	V
$I_{O(b\text{-}w)}$	output current (black-to-white, pins 20, 17 and 14)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	–	–	MHz
G_{nom}	nominal gain		–	1	–	dB
G_v	gain control for all channels (relative to G_{nom})		–4	–	+2	dB
C_v	contrast control (relative to G_{nom})		–20	–	+3	dB
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4883	20	DIL	plastic	SOT146

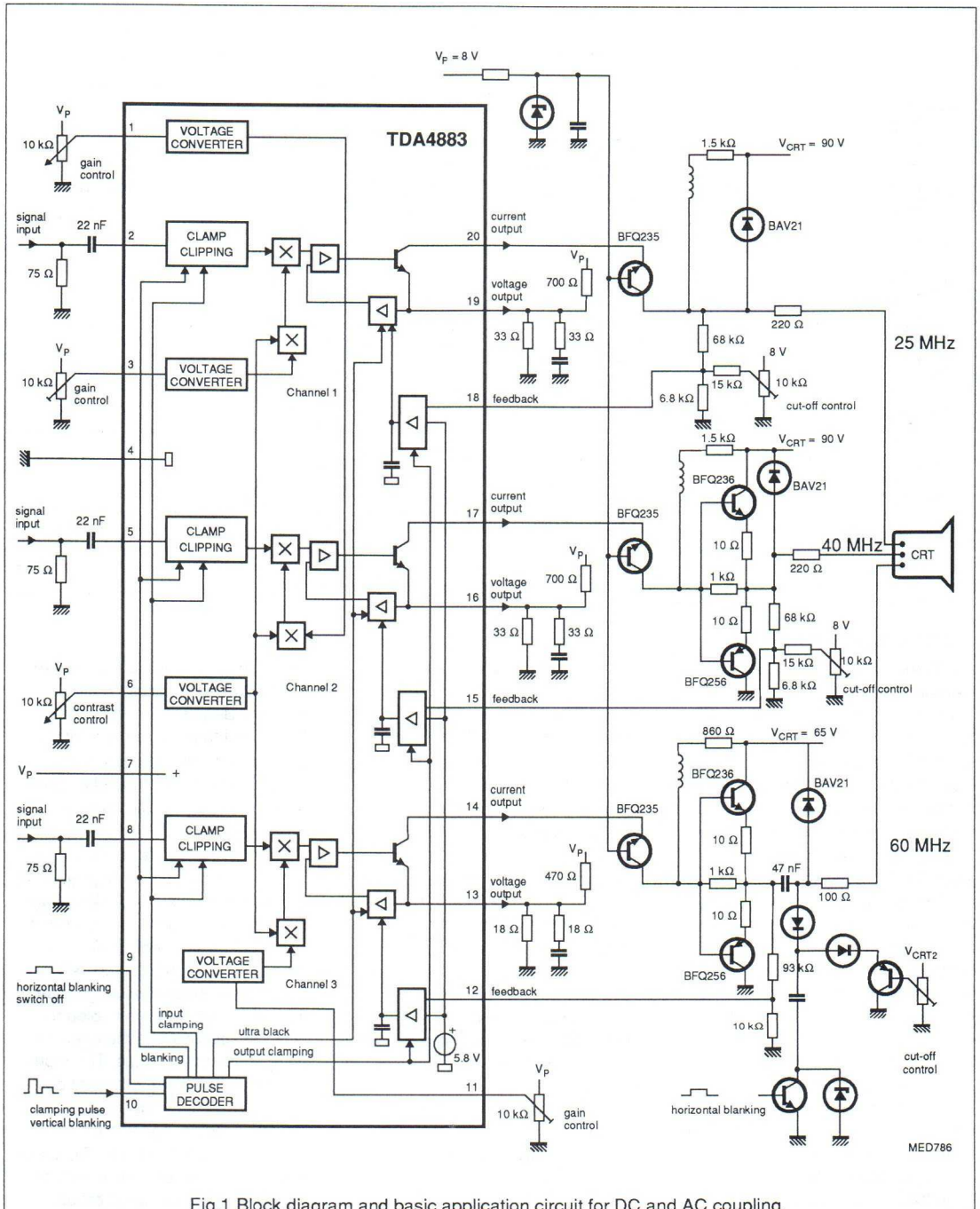


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

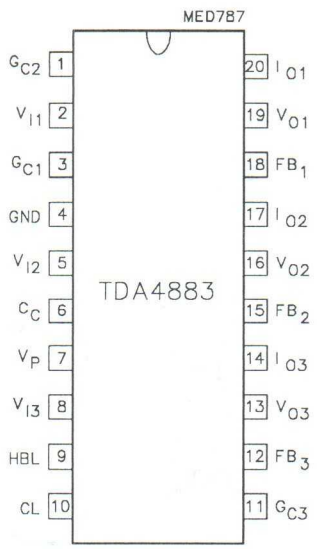


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
G_{C2}	1	gain control Channel 2
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch off
CL	10	input clamping, vertical blanking
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

FUNCTIONAL DESCRIPTION

RGB input signals (0.7 V(p-p)) are capacitively coupled into the TDA4883 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. All channels have a maximum total voltage gain of 6 dB (maximum contrast and maximum individual channel gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.8 V(p-p).

DC voltages are used for contrast and gain control.

Contrast control is achieved by a voltage at pin 6 and affects the three channels simultaneously.

To provide the correct white point, an individual *gain control* (pins 1, 3 and 11) adjusts the signals of Channels 1, 2 and 3.

Each *output stage* provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply.

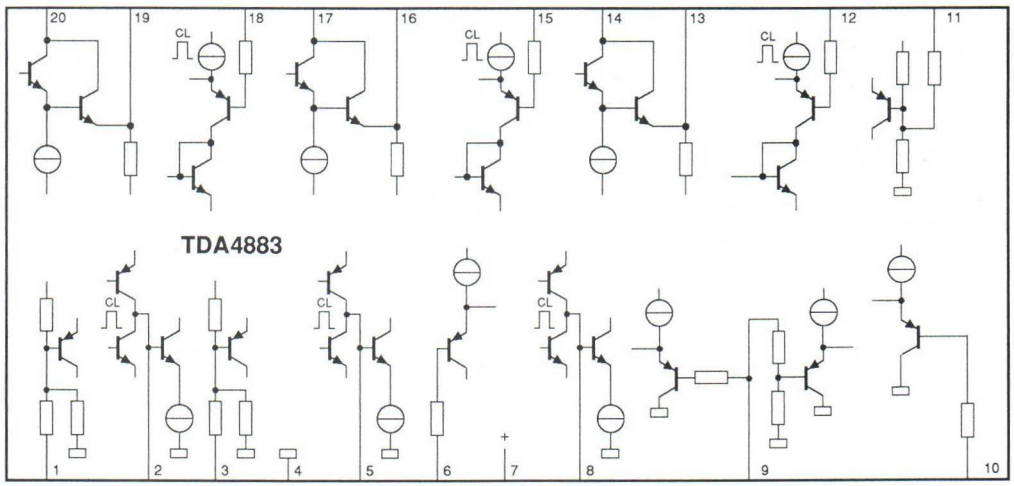
The three channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The *clamping pulse* (pin 10) is used for *input clamping* only. The input signals have to be at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V (1 V to 3.5 V).

The *vertical blanking pulse* will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 300 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled to avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted instead. Thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization.

During *horizontal blanking* (pin 9) the output signal is set to reference black level as previously described and *output clamping* is activated. If the voltage at pin 9 exceeds the *switch off* threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during vertical flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For *cut-off stabilization* (DC coupling to the CRT) respectively *black level stabilization* (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.



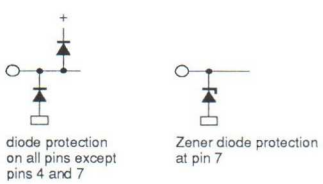


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_i	input voltage (pins 2, 5 and 8)	−0.1	V_P	V
V_{ext}	external DC voltage			
	pins 20, 17 and 14	−0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	−0.1	V_P	V
	pin 9	−0.1	$V_P + 0.7$	V
	pin 10	−0.7	$V_P + 0.7$	V
I_o	average output current (pins 20, 17 and 14)	0	50	mA
I_M	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−500	+500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 8.0 V, T_{amb} = +25 °C; all voltages measured to GND (pin 4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	46	56	mA
Video signal inputs						
$V_{I(b-w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$I_{2, 5, 8}$	DC current	no clamping	–0.1	–	0.1	µA
		during clamping	±50	–	–	µA
Contrast control (note 2)						
V_6	input voltage range	note 1	1.0	–	6.0	V
I_6	current		–5	–1	–	µA
C_V	contrast relative to nominal contrast	V_6 = 6.0 V; $V_{1, 3, 11}$ open-circuit	–	3	–	dB
		V_6 = 4.5 V; $V_{1, 3, 11}$ open-circuit	–	0	–	dB
		V_6 = 1.0 V; $V_{1, 3, 11}$ open-circuit	–	–20	–	dB
Tr	tracking of RGB signals	2.5 V < V_6 < 6 V; $V_{1, 3, 11}$ open-circuit	–	0	0.5	dB
Gain control						
$V_{1, 3, 11}$	input voltage	note 1	1.0	–	6.0	V
$R_{1, 3, 11}$	input resistance against $V_{N1, N3, N11}$		–	43	–	kΩ
G_V	gain relative to nominal gain	V_6 = 4.5 V; $V_{1, 3, 11}$ = 6 V	–	2	–	dB
		V_6 = 4.5 V; $V_{1, 3, 11}$ = 1 V	–	–4	–	dB
$V_{N1, N3, N11}$	input voltage for nominal gain	pin 1, 3, 11 open-circuit	–	4.6	–	V
Feedback input						
V_{int}	internal reference voltage	note 3	tbn	5.8	tbn	V
$I_{18, 15, 12}$	output current	during output clamping	–1.5	–1.0	–0.1	µA
Voltage outputs (pins 19, 16 and 13)						
$V_{O(b-w)}$	signal output voltage (black-to-white value)	$V_{1, 3, 11}$ open-circuit; V_6 = 4.5 V; $V_{I(b-w)}$ = 0.7 V	–	0.8	–	V
V_{bl}	black level voltage	during output clamping; depending on black level adjustment; note 4	0.3	–	1.0	V
		during switch-off	–	0.1	0.3	V
S/N	signal-to-noise ratio	note 5	–	–	44	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at voltage outputs						
G_{vf}	gain decrease by frequency response at pins 19, 16 and 13	70 MHz	–	–	–3	dB
t_{rO}	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.5	5.0	ns
Current outputs (pins 20, 17 and 14)						
$I_{O(b-w)}$	signal current (black-to-white)		–	50	–	mA
		with peaking; note 6	–	–	100	mA
$V_{20-19,\ 17-16,\ 14-13}$	HF saturation of output transistors	I_O = 50 mA	–	–	2.0	V
		I_O = 100 mA	–	–	2.2	V
Threshold voltages (see note 7)						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance referenced to ground		50	80	110	kΩ
t_{d9}	delay between horizontal blanking input and output signal blanking		–	35	60	ns
V_{10}	threshold for vertical blanking (blanking, no input clamping)	see Fig.4	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	see Fig.4	2.6	3.0	3.5	V
I_{10}	input current		–3	–1	–	µA
$t_{r,f10}$	rise and fall time for clamping pulse	transition 1 to 3.5 V; see Fig.4	–	–	75	ns/V
t_{w10}	clamping pulse width	V_{10} = 3 V	0.6	–	–	µs
t_{d10}	delay between vertical blanking input and output signal blanking	see Fig.4	–	300	–	ns

Notes to the characteristics

1. Typical range is 1 to 6 V, the range can be increased (e.g. 0 to 7 V) to slightly increase the control range.
2. Open contrast control pin leads to undefined contrast setting.
3. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping in closed feedback loop.
4. Minimum guaranteed control range, the typical minimum black level voltage is 0.1 V.
5. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):
   $$\frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$$
6. The external RC combinations at pins 19, 16 and 13 enables peak currents during transients.
7. The internal threshold voltages are derived from an internally stabilized voltage. The internal pulses are generated if the input pulses are higher than the thresholds.

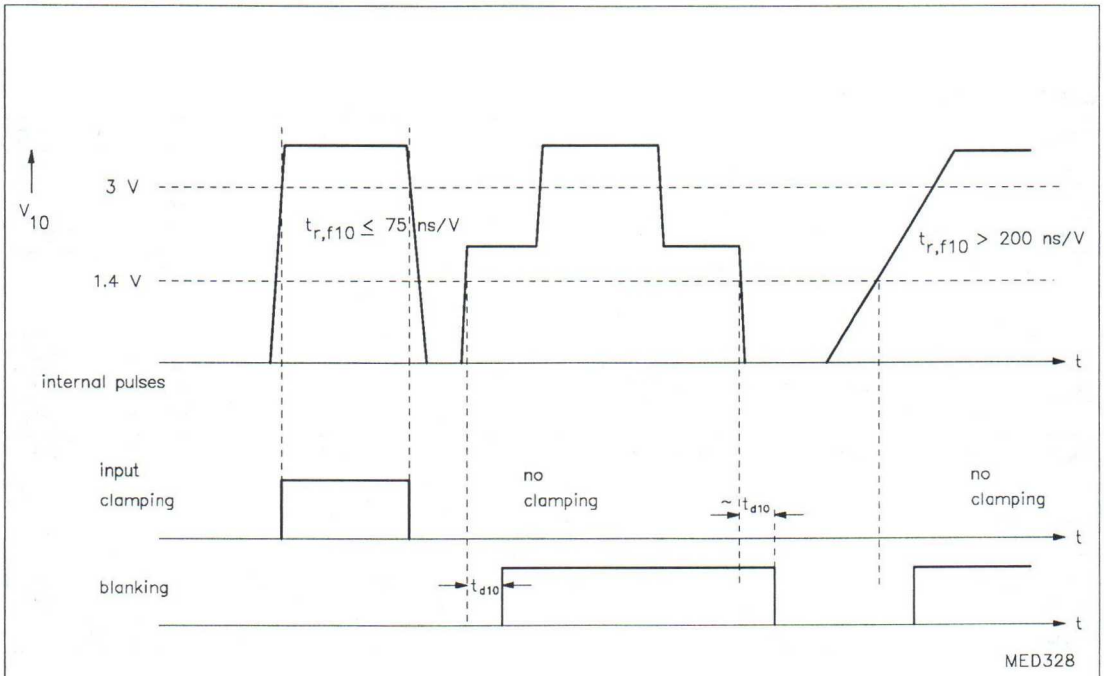


Fig.4 Timing of pulses at pin 10.

Three gain control video pre-amplifier for OSD TDA4884

FEATURES

- 85 MHz video controller
- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 3 channels
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible
- OSD application very easily.

GENERAL DESCRIPTION

The TDA4884 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA485x monitor deflection IC family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	48	–	mA
$V_{I(b-w)}$	input voltage (black-to-white; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b-w)}$	output voltage (black-to-white; pins 19, 16 and 13)	nominal contrast; pins 3, 1 and 11 open-circuit	–	0.79	–	V
$I_{O(b-w)}$	output current (black-to-white; pins 20, 17 and 14)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	85	–	MHz
G_{nom}	nominal gain (pins 2, 5 and 8 to pins 19, 16 and 13)	nominal contrast; pins 3, 1 and 11 open-circuit	–	1	–	dB
G_v	gain control for all channels (relative to G_{nom})		–5	–	+2.6	dB
C_v	contrast control	V_6 = 1 to 6 V	–22	–	+3.4	dB
C_{OSD}	minimum contrast for OSD	V_6 = 0.7 V	–	–40	–	dB
T_{amb}	operating ambient temperature		–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4884	20	DIL	plastic	SOT146

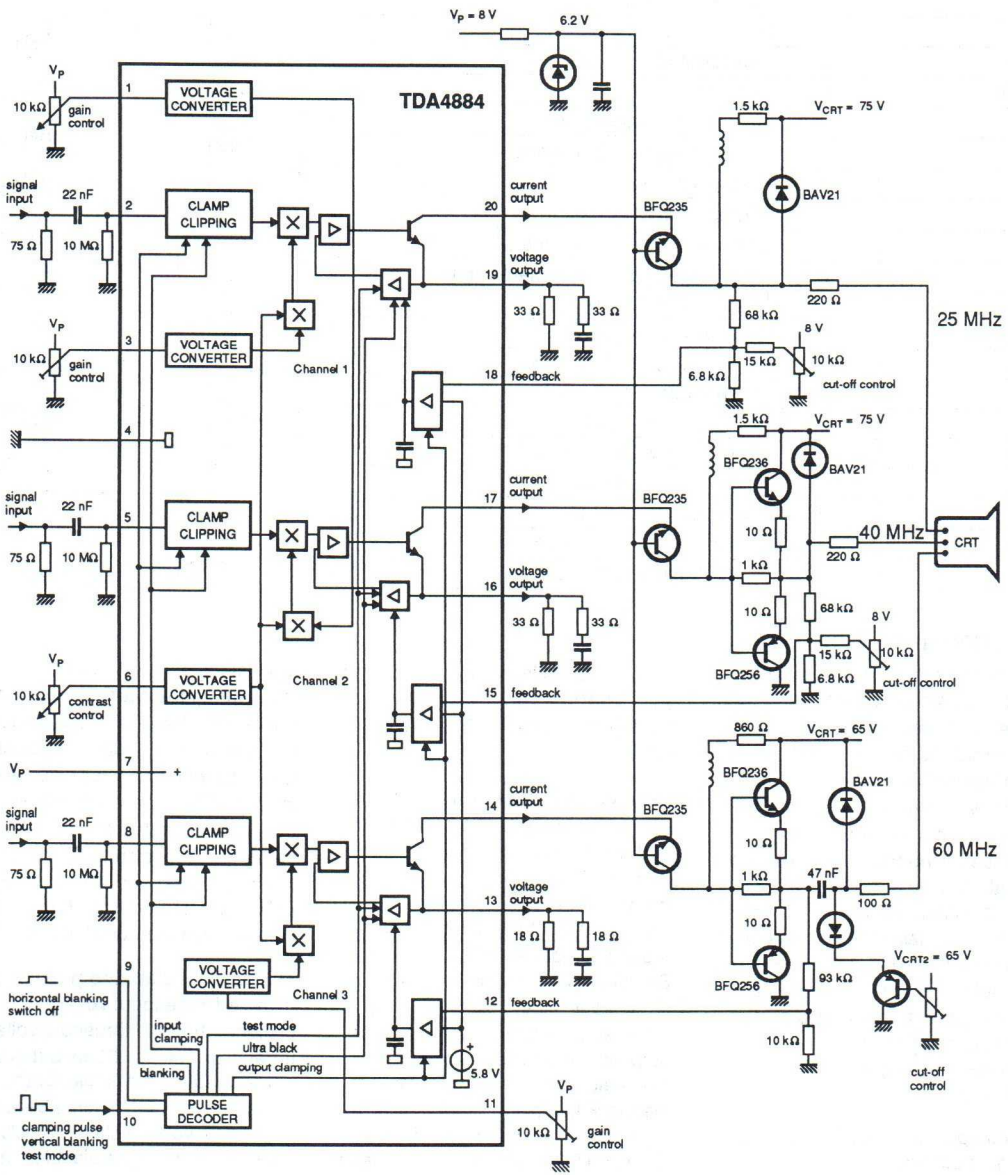


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

PINNING

SYMBOL	PIN	DESCRIPTION
G_{C2}	1	gain control Channel 2
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control, OSD switch
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch-off
CL	10	input clamping, vertical blanking, test mode
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

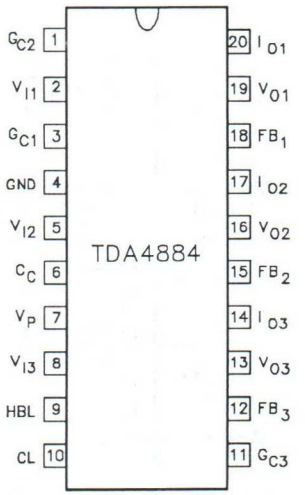


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The RGB input signals (0.7 $V_{(p\text{-}p)}$) are capacitively coupled into the TDA4884 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. All channels have a maximum total voltage gain of 7 dB (maximum contrast and maximum individual channel gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.79 $V_{(p\text{-}p)}$.

DC voltages are used for contrast and gain control.

Contrast control is achieved by a voltage at pin 6 and affects the three channels simultaneously. To provide the correct white point, an individual **gain control** (pins 3, 1 and 11) adjusts the signals of Channels 1, 2 and 3.

Each **output stage** provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply. The channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The **clamping pulse** (pin 10) is used for **input clamping** only. The input signals have to be at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V during transition from 1 V to 3.5 V.

The **vertical blanking pulse** will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 320 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled in order to avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted

instead, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization (see below).

During **horizontal blanking** (pin 9) the output signal is set to reference black level as previously described and **output clamping** is activated. If the voltage at pin 9 exceeds the **switch-off** threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during V-flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For **cut-off stabilization** (DC coupling to the CRT) respectively **black level stabilization** (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During the horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.

For OSD fast switching of control pin 6 to less than 1 V (e.g. 0.7 V) blankes the input signals. The OSD signals can easily be inserted to the external cascode transistor (see Fig.3).

During **test mode** (pins 9 and 10 connected to V_P) the black levels at the voltage outputs (pins 12, 16 and 13) are internally set to typical 0.5 V (3 V DC at signal inputs (pins 2, 5 and 8)).

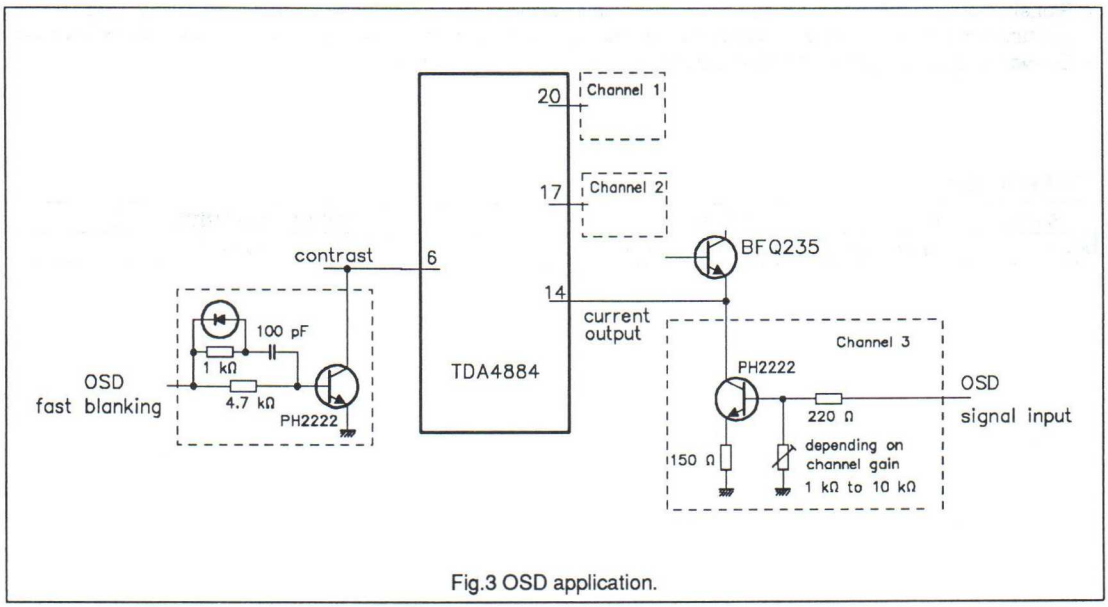


Fig.3 OSD application.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_I	input voltage (pins 2, 5 and 8)	−0.1	V_P	V
V_{ext}	external DC voltage			
	pins 20, 17 and 14	−0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	−0.1	V_P	V
	pin 9	−0.1	V_P + 0.7	V
	pin 10	−0.1	V_P + 0.7	V
I_O	average output current (pins 20, 17 and 14; note 1)	0	50	mA
I_M	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C
T_j	junction temperature	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	−500	+500	V

Notes to the limiting values

1. Signal amplitude of 50 mA black-to-white is possible if the average current (including blanking times and signal variation against time) does not exceed 50 mA. The maximum power dissipation of 1200 mW has to be considered.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = +25 °C; all voltages measured to GND (pin 4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		36	48	60	mA
Video signal inputs (Channel 1: pin 2, Channel 2: pin 5 and Channel 3: pin 8)						
$V_{I(b-w)}$	input voltage (black-to-white value; pins 2, 5 and 8)		–	0.7	1.0	V
$V_{IC2,5,8}$	DC voltage during input clamping (artificial black + V_{BE})	note 1	2.8	3.1	3.4	V
$I_{2,5,8}$	DC current	no clamping; $V_{2,5,8} = V_{IC2,5,8}$; T_{amb} = –20 to +70 °C	–0.05	+0.05	+0.250	µA
		during clamping; $V_{2,5,8} = V_{IC2,5,8} \pm 0.7$ V	±50	±75	±120	µA
Contrast control (pin 6; note 2)						
V_6	input voltage		1.0	–	6.0	V
	maximum input voltage		–	–	$V_P - 1$	V
V_{N6}	input voltage for nominal contrast	note 3	–	4.3	–	V
I_6	input current	V_6 = 4.3 V	–5	–1	–0.1	µA
C_v	contrast relative to nominal contrast	V_6 = 6.0 V; pins 3, 1 and 11 open-circuit	2.4	3.4	–	dB
		V_6 = 1.0 V; pins 3, 1 and 11 open-circuit	–26	–22	–19	dB
V_{M6}	input voltage for minimum contrast	pins 3, 1 and 11 open-circuit	–	0.7	–	V
Tr	tracking of output signals of Channels 1, 2 and 3	1 V < V_6 < 6 V; note 4	–	0	0.5	dB
t_{dfC}	delay between leading edges (falling) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	V_6 = 4.3 V to 0.7 V; input fall time at pin 6: t_{fCC} = 2 ns; note 5	–	7	20	ns
t_{drC}	delay between trailing edges (rising) of step in contrast voltage and output signals at voltage outputs (pins 19, 16 and 13)	V_6 = 0.7 V to 4.3 V; input rise time at pin 6: t_{rCC} = 2 ns; note 5	–	15	25	ns
t_{fC}	fall time of output signals at voltage outputs (pins 19, 16 and 13)	90% to 10% amplitude; input fall time at pin 6: t_{fCC} = 2 ns; note 5	–	6	15	ns
t_{rC}	rise time of output signals at voltage outputs (pins 19, 16 and 13)	10% to 90% amplitude; input rise time at pin 6: t_{rCC} = 2 ns; note 5	–	6	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain control (pin 3 for Channel 1, pin 1 for Channel 2 and pin 11 for Channel 3; note 6)						
$V_{3,1,11}$	input voltage		1.0	–	6.0	V
$V_{N3,1,11}$	input voltage for nominal gain	pins 3, 1 and 11 open-circuit	3.6	3.75	3.95	V
$R_{3,1,11}$	input resistance		44	55	66	kΩ
G_v	gain relative to nominal gain	V_6 = 4.3 V; $V_{3,1,11}$ = 6 V	2	2.6	3.3	dB
		V_6 = 4.3 V; $V_{3,1,11}$ = 1 V	–5.5	–5	–4.5	dB
Feedback input (Channel 1: pin 18, Channel 2: pin 15 and Channel 3: pin 12; note 7)						
V_{int}	internal reference voltage		5.6	5.8	6.1	V
$I_{18,15,12}$	maximum output current	during output clamping; $V_{18,15,12}$ = 3 V	–500	–100	–60	nA
ΔV_{CRT}	Δ black level at CRT	note 8	0	40	200	mV
$\Delta_T V_{int}$	variation of V_{int} in the temperature range	T_{amb} = –20 to +70 °C	0	20	50	mV
$\Delta_V V_{int}$	variation of V_{int} with supply voltage	7.2 V ≤ V_P ≤ 8.8 V	0	60	100	mV
Voltage outputs (Channel 1: pin 19, Channel 2: pin 16 and Channel 3: pin 13; note 1)						
$V_{O(b-w)}$	nominal signal output voltage (black-to-white value)	V_6 = 4.3 V; $V_{I(b-w)}$ = 0.7 V; pins 3, 1 and 11 open-circuit	0.69	0.79	0.89	V
V_{blx}	maximum adjustable black level voltage	during output clamping; T_{amb} = –20 to +70 °C	1	1.2	1.4	V
V_{blSO}	black level voltage during switch-off, equal to minimum adjustable black level voltage	V_9 = V_P; R_O = 33 Ω; T_{amb} = –20 to +70 °C	30	45	100	mV
V_{blT}	black level voltage during test mode	V_9 = V_P; V_{10} = V_P; pin 1 open-circuit; $V_{2,5,8}$ = $V_{IC2,5,8}$; note 9	0.3	0.7	1.2	V
S/N	signal-to-noise ratio	note 10	–	50	44	dB
D_{Th}	output thermal distortion	$I_{O(b-w)}$ = 50 mA; note 11	–	0.6	1	%
$\Delta_{LF} V_{bl}$	Δ black level between clamping pulses	line frequency 30 kHz	–	0.5	4.5	mV
V_{off}	maximum offset during sync clipping	$V_{2,5,8}$ < $V_{IC2,5,8}$; note 12	0	7	15	mV
$\Delta_T V_{O(b-w)}$	variation of nominal output signal (black-to-white value) with temperature	V_6 = 4.3 V; $V_{I(b-w)}$ = 0.7 V; T_{amb} = –20 to +70 °C; pins 3, 1 and 11 open-circuit	0	2.5	10	%
Current outputs (Channel 1: pin 20, Channel 2: pin 17 and Channel 3: pin 14; note 13)						
$I_{O(b-w)}$	signal current (black-to-white value)		–	50	–	mA
		with peaking	–	–	100	mA
V_{20-19}; V_{17-16}; V_{14-13}	start of HF-saturation of output transistors	I_O = 50 mA	–	–	2.0	V
		I_O = 100 mA	–	–	2.2	V
I_{blSO}	output current during switch-off	V_9 = V_P; R_O = 33 Ω	0	20	900	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at voltage outputs (note 14)						
G_{vf}	gain decrease by frequency response at pins 19, 16 and 13	70 MHz; single channel	–	1.3	3	dB
t_{rO}	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.1	5.0	ns
dV_O	overshoot of output signal pulse related to actual output pulse amplitude	single channel; input rise time = 2.5 ns; $V_{I(b-w)}$ = 0.7 V; V_6 = 4.3 V; pins 3, 1 and 11 open-circuit	–	4	8	%
Crosstalk at outputs with speed up circuit (note 15)						
C_{tr}	transient crosstalk		–	–	0.1	–
Threshold voltages for clamping, blanking and switch-off (pins 9 and 10; note 16)						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance	against ground	50	80	110	kΩ
V_{10}	threshold for vertical blanking (blanking, no input clamping)	note 17	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	note 17	2.6	3.0	3.5	V
	threshold for test mode (no clamping, no blanking, for V_{blT} see above)	for test mode also $V_9 > 6.8$ V (switch-off)	$V_P - 1$	–	V_P	V
I_{10}	current	$V_{10} < V_P - 1$ V	–3	–1	–	µA
		$V_{10} \geq V_P - 1$ V	–	100	–	µA
$t_{r,f10}$	rise and fall time for clamping pulse	note 17	–	–	75	ns/V
t_{w10}	width of clamping pulse		0.6	–	–	µs

Notes to the characteristics

1. Definition of levels:

Artificial black level: internal signal level behing input emitter follower during input clamping and signal clipping. This level is inserted instead of the input signal during blanking.

Reference black level: DC voltage during output clamping at voltage outputs, not influenced by contrast or gain setting, adjustable by cut-off stabilization.

Cut-off level: corresponding DC voltage at CRT cathode in closed feedback loop.

Black level: actual signal black level at either voltage outputs or cathode. At voltage outputs the black level is equal to reference black level because there is no brightness control via TDA4884. At cathode the black level is equal to cut-off level. Brightness can be adjusted via grid 1.

Ultra black level, switch-off level: lowest adjustable reference black level, lowest signal level at voltage outputs. The minimum guaranteed control range for reference black level is 0.1 to 1 V.

The ultra black level is depending on the external resistor R_O at voltage outputs (pins 13, 16 and 19) to ground.

$$V_{blSO} \approx \frac{R_O}{3.5\ k\Omega + R_O} \times 4.65\ V.$$

Signal processing see Fig.4.

2. Linear control range is 1 to 6 V for V_6, independent from supply voltage. Open pin 6 leads to absolute maximum contrast setting. It is recommended to not exceed $V_6 = V_P - 1$ V in order to avoid saturation of internal circuitry. For $V_6 < V_{M6} \sim 0.7$ V a small negative signal (~ -40 dB) will appear. For frequency dependence of contrast control see note 14. Typical contrast characteristic see Fig.5.
3. Definition for nominal output signals: input $V_{I(b\text{-}w)} = 0.7$ V, gain pins 3, 1 and 11 open-circuit, contrast control $V_6 = V_{N6}$.
4. $$Tr = 20 \times \text{maximum of } \left|\log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2}\right)\right|; \left|\log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3}\right)\right|; \left|\log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3}\right)\right| \text{ [dB]}$$

   A_x: signal output amplitude in Channel x at any contrast between 1 and 6 V.
   A_{x0}: signal output amplitude in Channel x at nominal contrast and same gain setting.
5. Typical step in contrast voltage and response at signal outputs for nominal input signal $V_{I(b\text{-}w)} = 0.7$ V. Typical OSD fast blanking input/output see Fig.6.
6. Linear control range is 1 to 6 V for V_3, V_1 and V_{11}, independent from supply voltage. Typical gain characteristic see Fig.7.
7. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping ($V_9 = 2$ V) in closed feedback loop. Typical variation of V_{int} with temperature and power supply voltage see Fig.8.
8. Slow variations of video supply voltage V_{CRT} (see Fig.1) will be suppressed at CRT cathode by cut-off stabilization. Change of V_{CRT} by 5 V leads to specified change of cut-off voltage.
9. The test mode allows testing without input and output clamping pulses. The signal inputs (pins 2, 5 and 8) have to be biased via resistors to the previously measured clamp voltages of approximately 3 V (artificial black level + V_{BE}). Signal blanking is not possible during test mode.
10. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):
    $$\frac{S}{N} = 20\log \frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}} \text{ [dB]}$$
11. Large output swing e.g. $I_{O(b\text{-}w)} = 50$ mA leeds to signal depending power dissipation in output transistors. Thermal V_{BE} variation is compensated.
12. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Typical sync clipping see Fig.9.
13. The output current approximately follows the equation $I_O = V_O\left(\frac{1}{R_O} + \frac{1}{2.2\ k\Omega}\right) - 500\ \mu A$ for $V_O > V_{bISO}$ and with

    R_O = external resistor at voltage output to ground.
    The external RC combination at pins 19, 16 and 13 (see Fig.1) enables peak currents during transients.
14. Frequency response, crosstalk and pulse response have been measured at voltage outputs in a special printed-circuit board with 50 Ω line in/out connections and without peaking (see TEST PCB). Typical frequency response see Fig.10, typical pulse response see Fig.11 and typical characteristic of contrast control versus frequency see Fig.12.
15. Crosstalk between any two output pins.
    Input conditions: One channel (Channel A) with nominal input signal and minimum rise time. The inputs of the other channels capacitively coupled to ground (Channel B). Gain pins 3, 1 and 11 open-circuit.
    Output conditions: Output signal of Channel A controlled by contrast setting (pin 6) to $V_{O(b\text{-}w)} = V_A = 0.7$ V, the rise time should be 5 ns. Output signal of Channel B then is $V_{O(b\text{-}w)} = V_B$.

    Transient crosstalk: $C_{tr} = \frac{V_B}{V_A}$.

    Crosstalk versus frequency has been measured without peaking circuit, with nominal input signa and nominal settings. Typical frequency dependent crosstalk between channels see Figs 13, 14 and 15.
16. The internal threshold voltages are derived from a stabilized voltage. The internal pulses are generated while the input pulses are higher than the thresholds. Voltages of less than –0.1 V at pins 9 and 10 can influence black level control and should be avoided.
17. For 75 ns/V < t_{rf10} < 240 ns/V generation of internal input clamping and blanking pulse is not defined. Any pulses not exceeding the threshold of input clamping (typical 3 V) will be detected as blanking pulse. Timing of pulses at pin 10 see Fig.16.

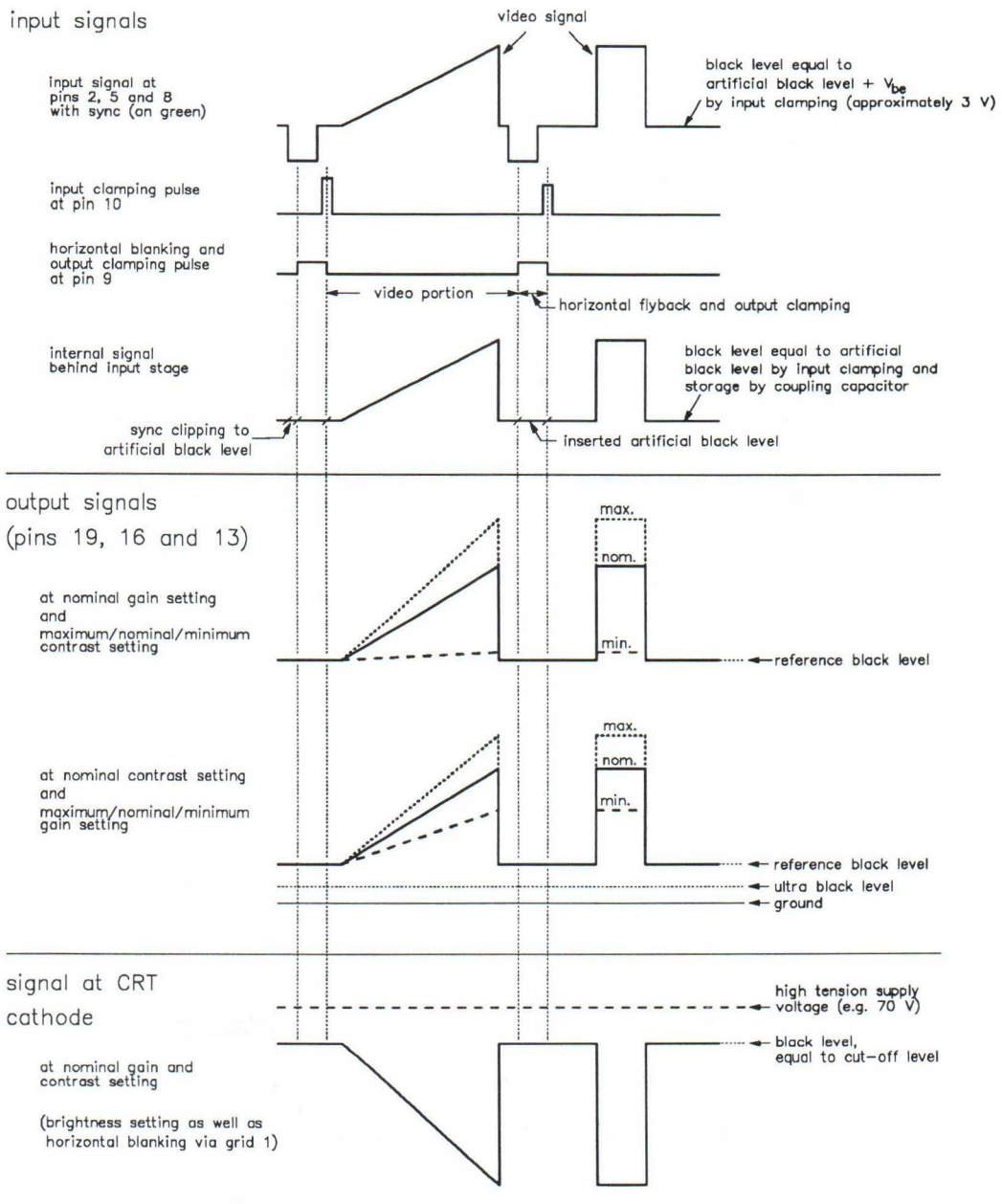


Fig.4 Signal processing.

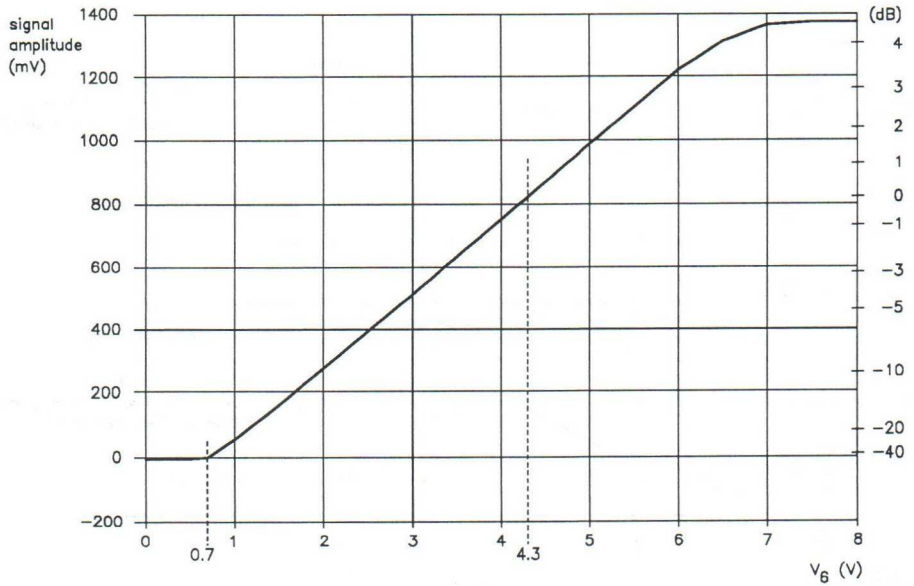


Fig.5 Typical contrast characteristic.

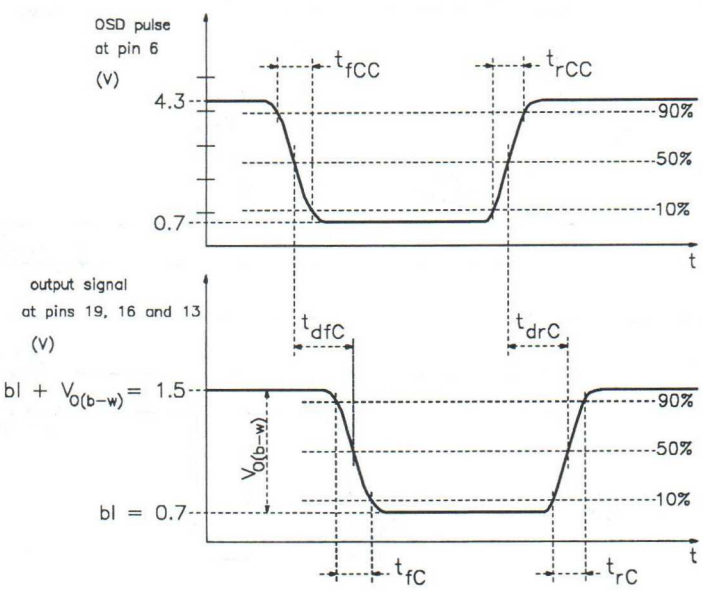


Fig.6 Typical OSD fast blanking input/output.

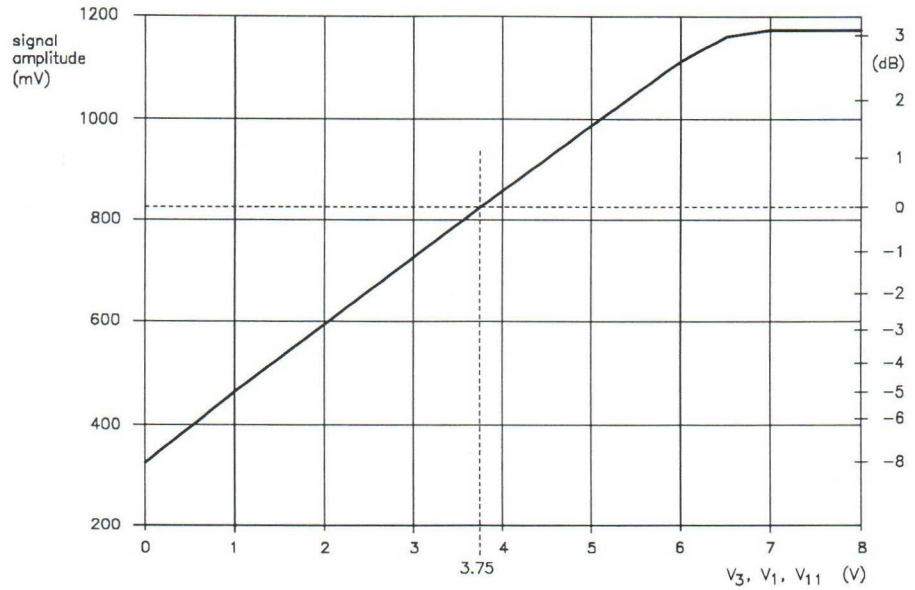


Fig.7 Typical gain characteristic.

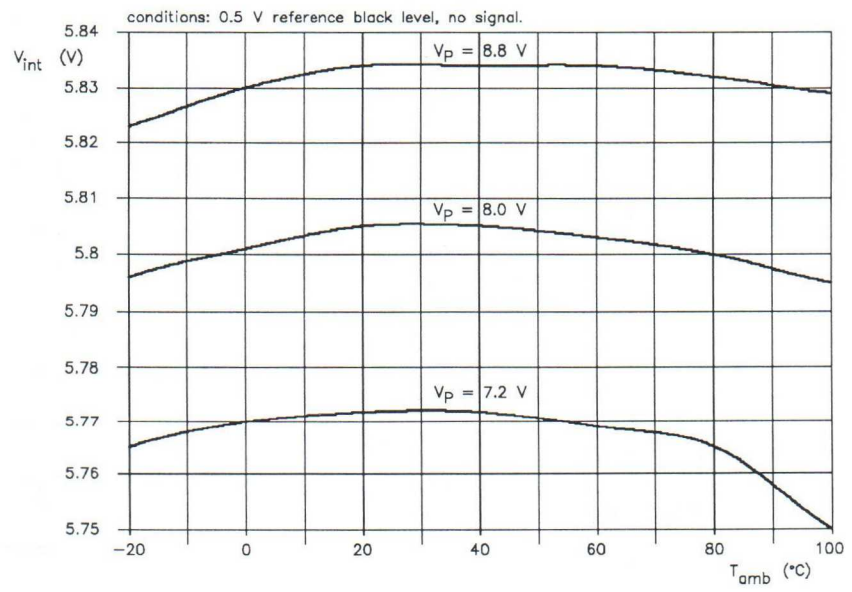


Fig.8 Typical variation of V_{int} with temperature and power supply voltage.

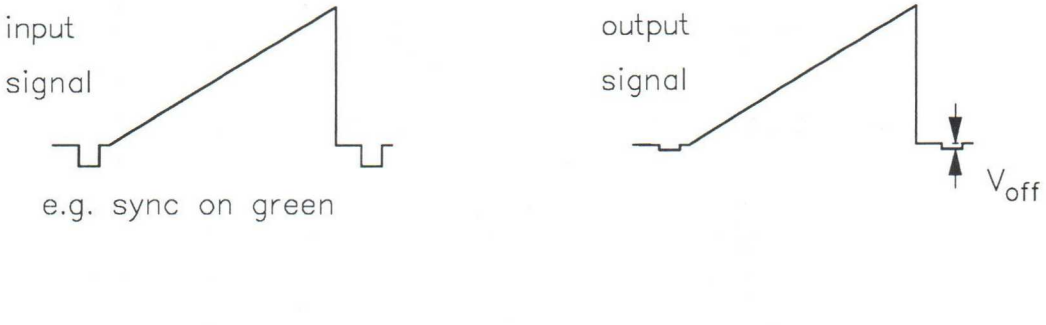


Fig.9 Typical sync clipping.

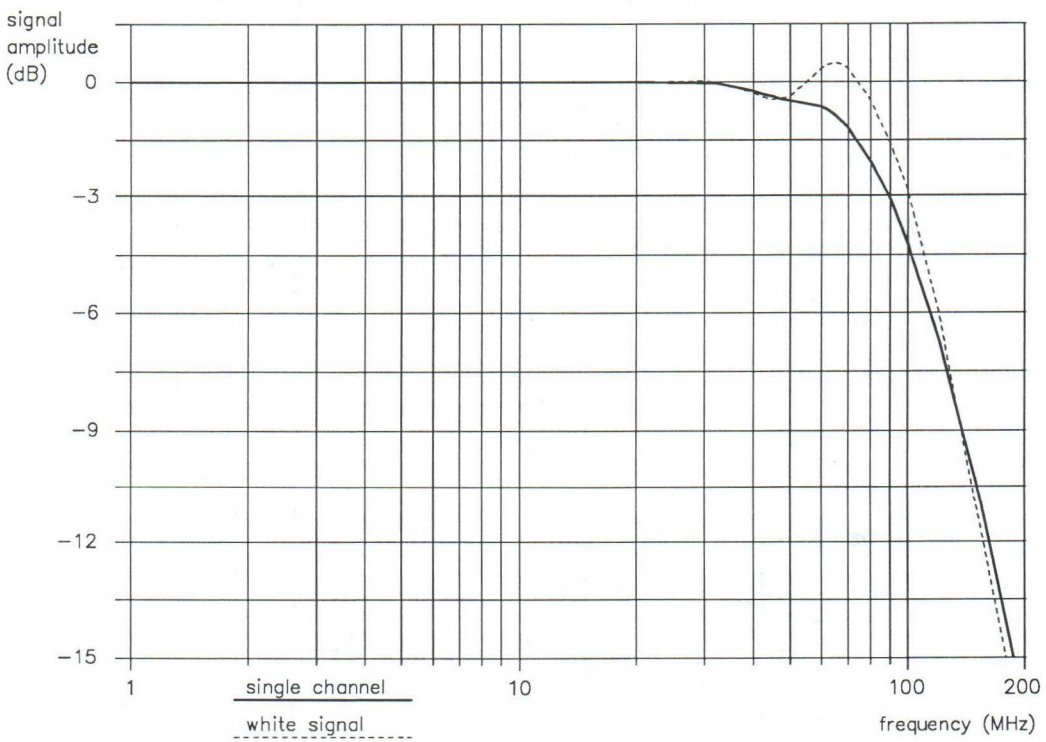


Fig.10 Typical frequency response.

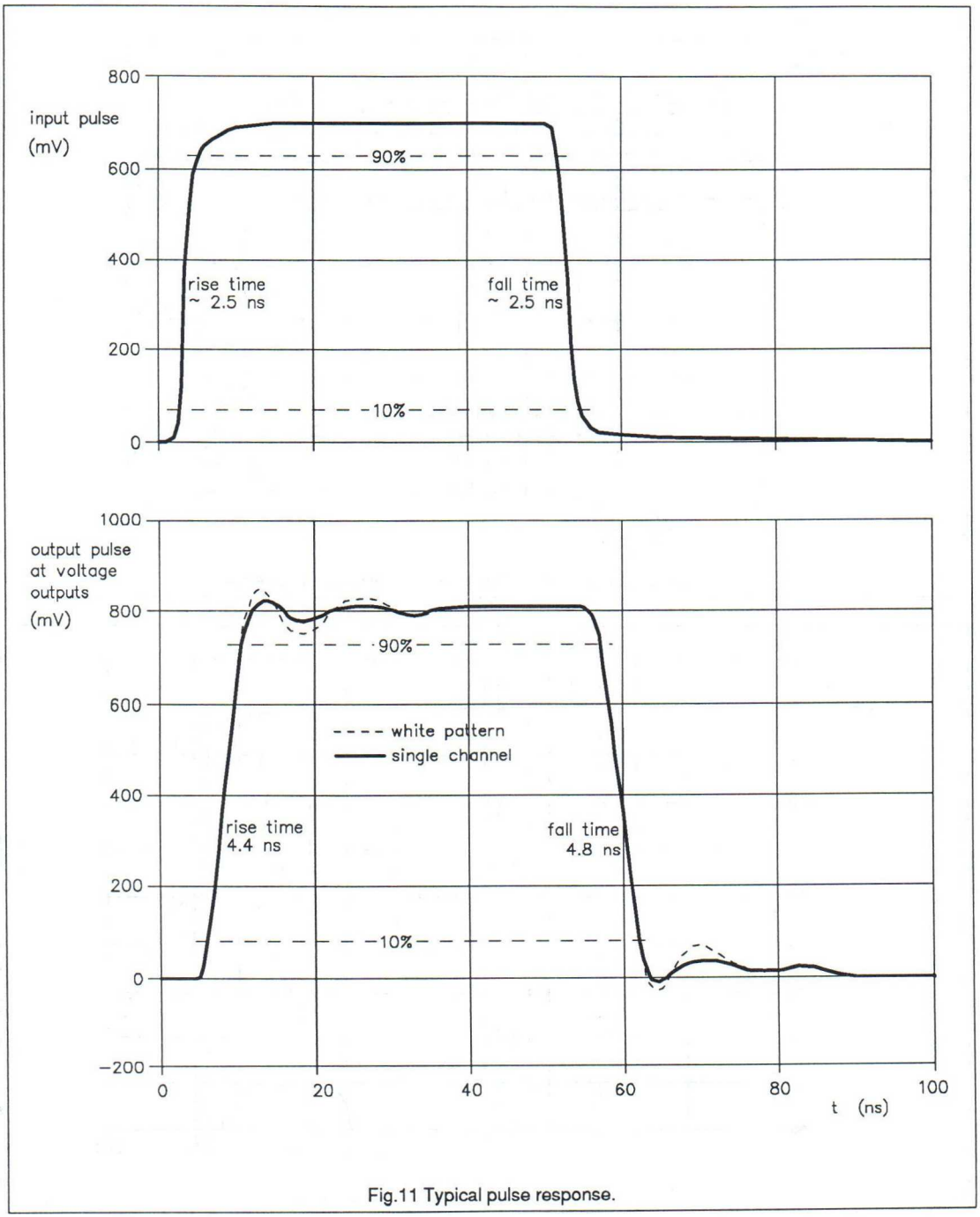


Fig.11 Typical pulse response.

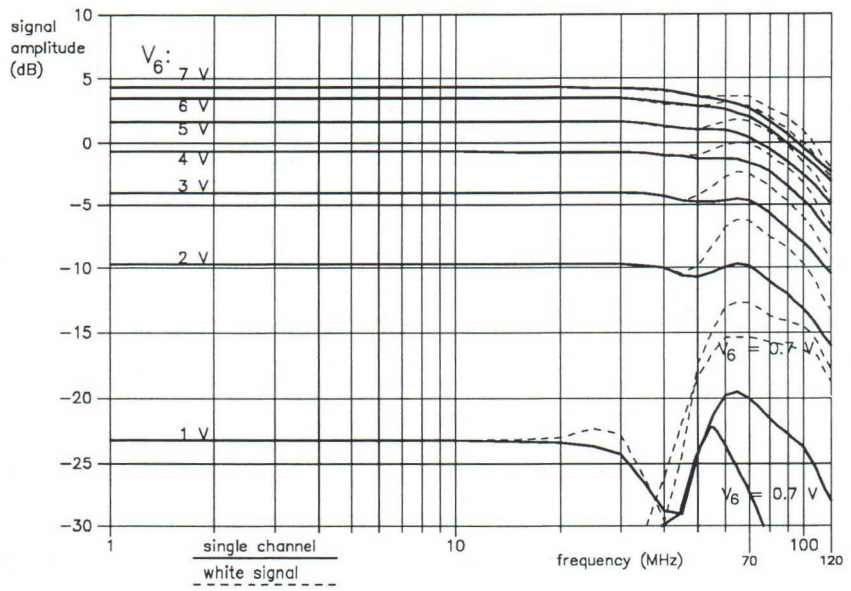


Fig.12 Typical characteristic of contrast control versus frequency.

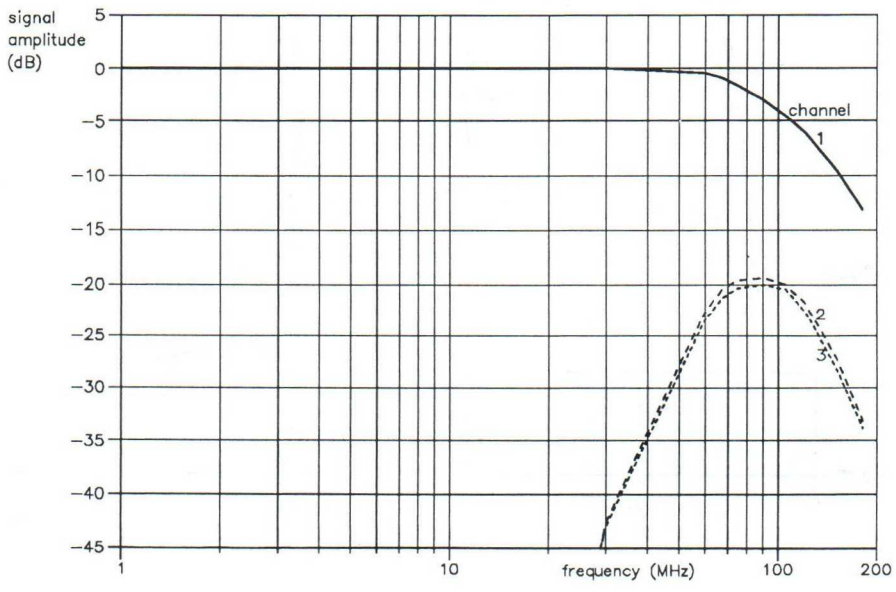


Fig.13 Typical crosstalk: Channel 1 → 2 and 3.

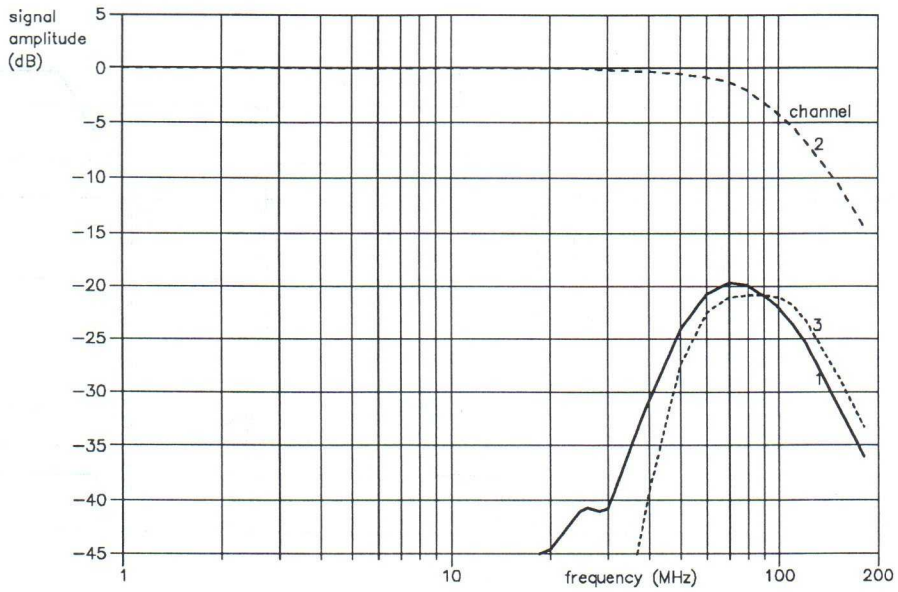


Fig.14 Typical crosstalk: Channel 2 → 1 and 3.

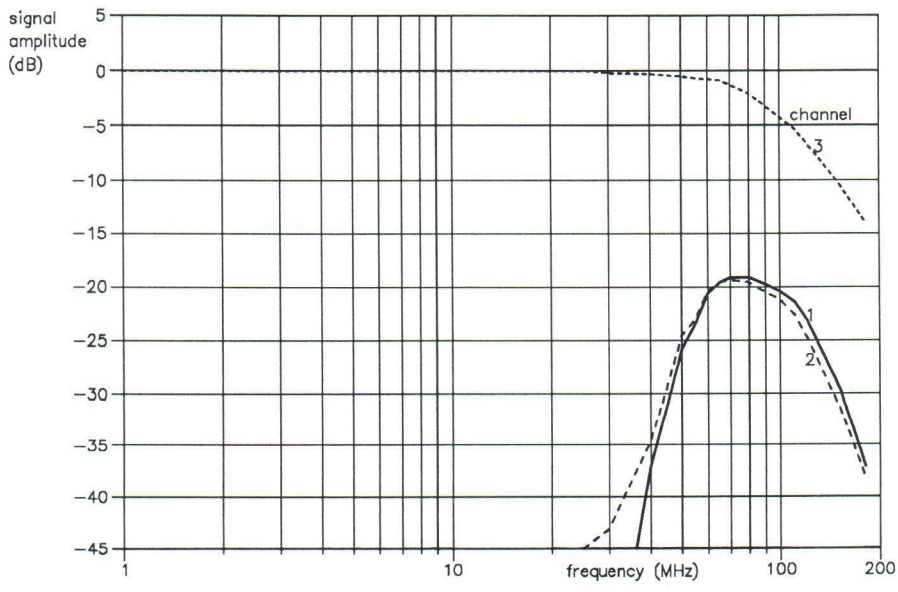


Fig.15 Typical crosstalk: Channel 3 → 1 and 2.

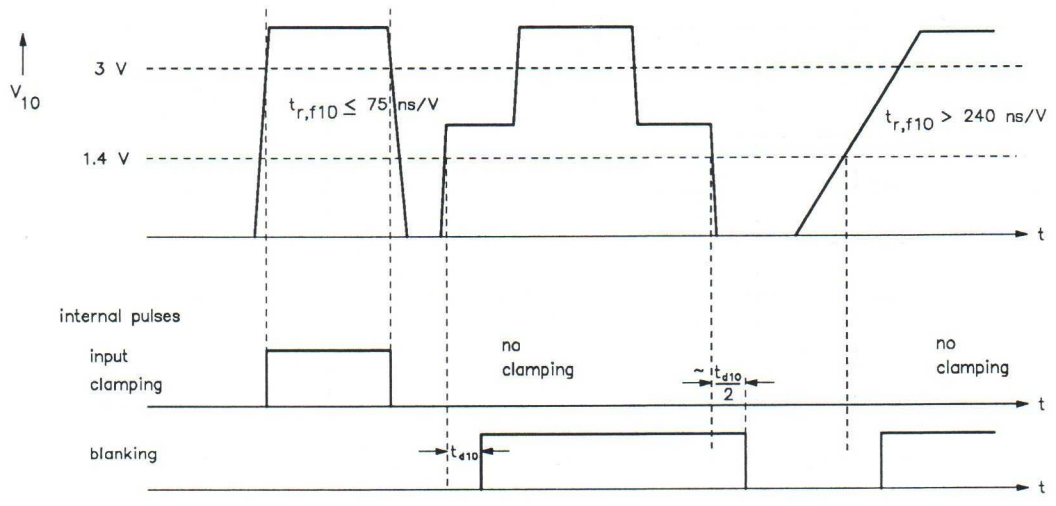


Fig.16 Timing of pulses at pin 10.

TEST PCB

For high frequency measurements a special application and printed-circuit board with only a few external components is built. Fig.17 shows the application circuit and Fig.18 the layout of the double sided printed board. All components on the rear (below) are of SMD type as well as R13, R14 and R15 on the front. Short HF loops and minimum crosstalk between the channels as well as input and output are achieved by properly shaped ground areas star connected to the IC ground pin.

The HF input signals can be fed to the subclick connectors X1, X2 and X3 by a 50 Ω line. The line is then terminated by a 51 Ω resistor on the board. With choice of jumper connections (JA1, JA2 and JA3) it is possible to connect channel inputs to its input connector, to connect all channels to one input connector (white pattern) and to ground each input via the coupling capacitor.

For operation without input clamping (e.g. test mode) the DC bias can be provided by VIDC (connector X21) if a short at JA4, JA5 and JA6 is made (solder short or small SMD resistor).

The output signal can be monitored via 50 Ω terminated lines at the voltage outputs (subclick connectors X4, X5 and X6). With 100 Ω in parallel to the 50 Ω terminated line the effective load resistance at the voltage outputs is 33 Ω. The mismatch seen from the line towards the IC has no significant effect if the line is match terminated. A peaking circuit (C15, R16 Channel 1) can be added for realistic loading of the voltage outputs.

Black level adjustment is done by VIOS, UFBX (connector X21) and resistors R19, R22 and R25 (Channel 1). If R19 is equal to the effective load resistor at the voltage output the reference black level is approximately
$U_{REF} = VIOS - V(IO1)$ and

$$V(IO1) = V_{int} + (V_{int} - UFBX) \times \frac{R22}{R25}.$$

V_{int} is the internal reference voltage at the feedback input (typical 5.8 V). By this it is possible to adjust the reference black level and the voltage at the current outputs independently.

DC control for contrast and gain is prepared at connectors X21 and X22. Contrast control can also be set by the potentiometer P1 (jumper JA11). The series resistor R11 is necessary if fast OSD switching is activated via 50 Ω line (X10), a line termination can be done at the connector X9. Clamping and blanking pulses are fed to the IC via connectors X7 and X8. Connector X23 is used for power supply. The capacitors C7 and C8 should be located as near as possible to the IC pins.

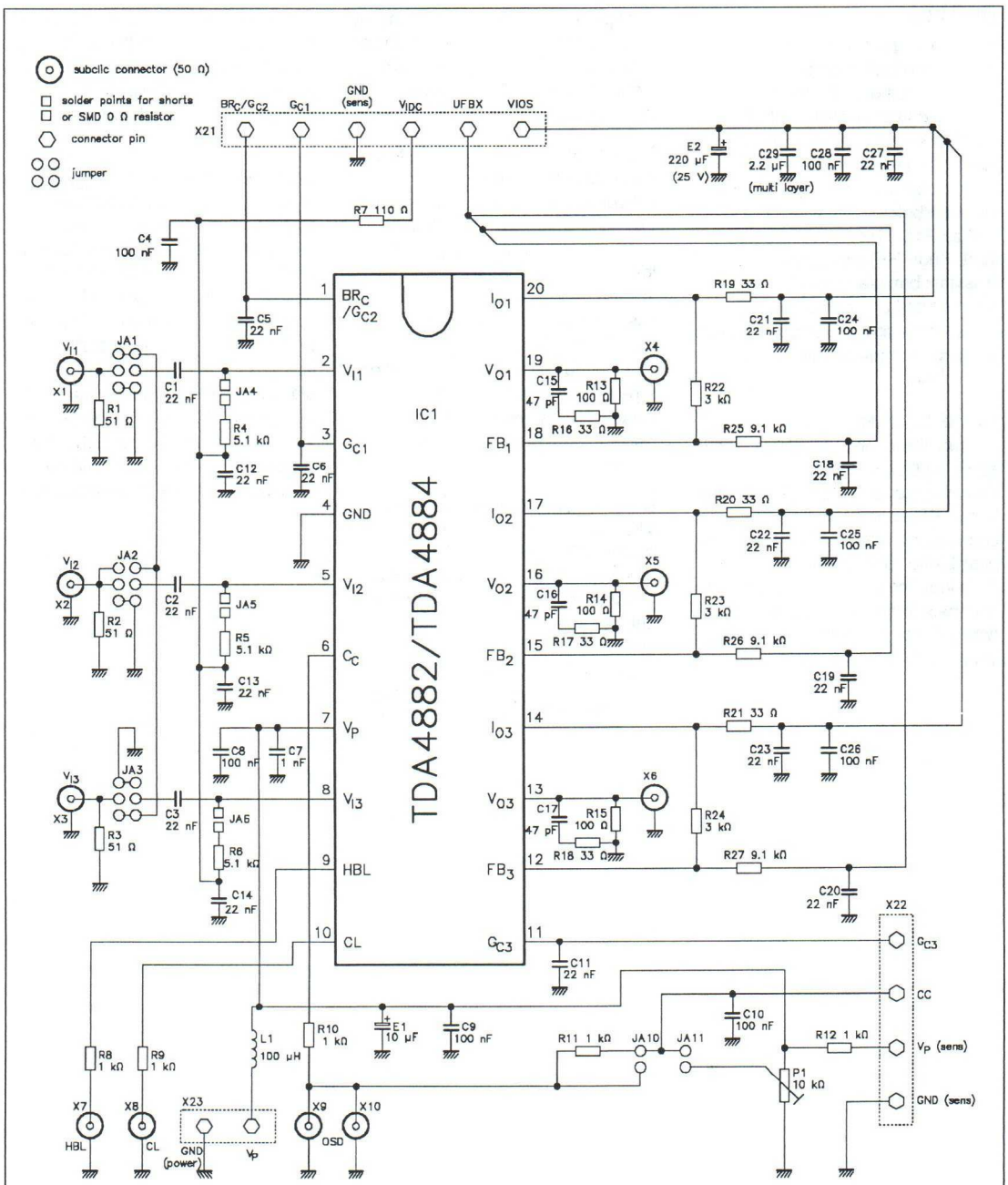


Fig.17 Application circuit for test PCB.

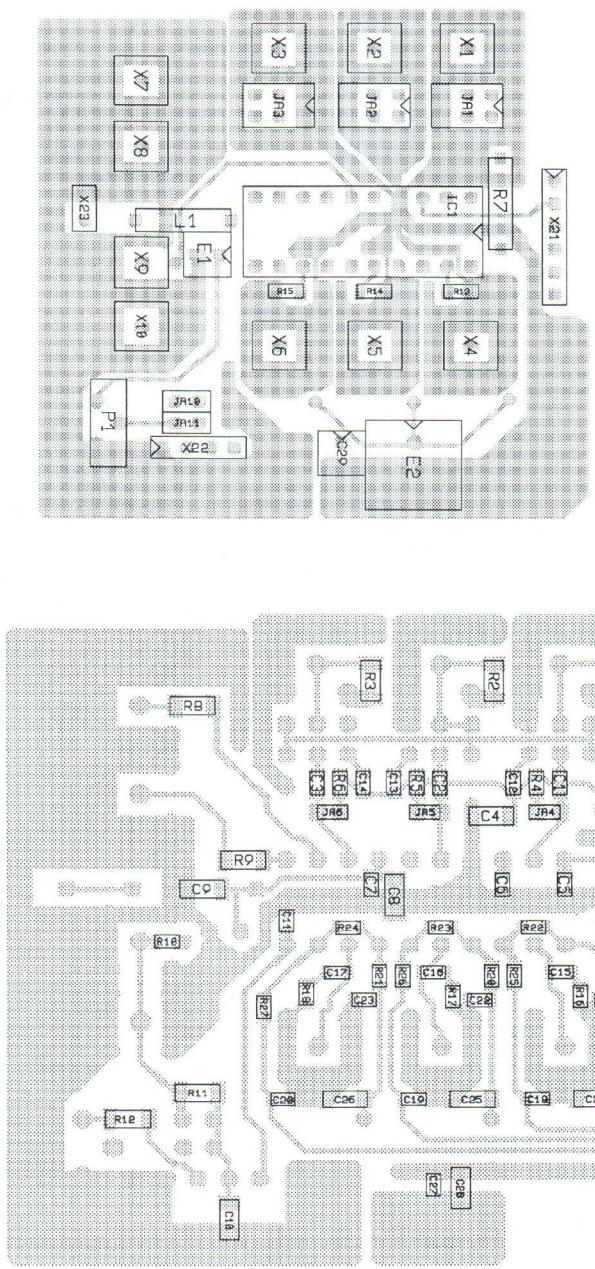


Fig.18 Double sided test PCB layout.

RECOMMENDATIONS FOR BUILDING THE APPLICATION BOARD

General

- Double sided board
- Short HF loops by large ground plane on the rear.

Voltage outputs

- Capacitive loads as small as possible
- Short interconnection via resistor to ground.

Supply voltage

- Capacitors as near as possible to the pins
- Use of high frequency capacitors (low self inductance, e.g. SMD).

Current outputs, emitter of cascode transistors

- The external interconnection inductivity can build a resonance together with the internal substrate capacity, a damping resistor of some 10 Ω near to the IC pin can suppress such oscillations.

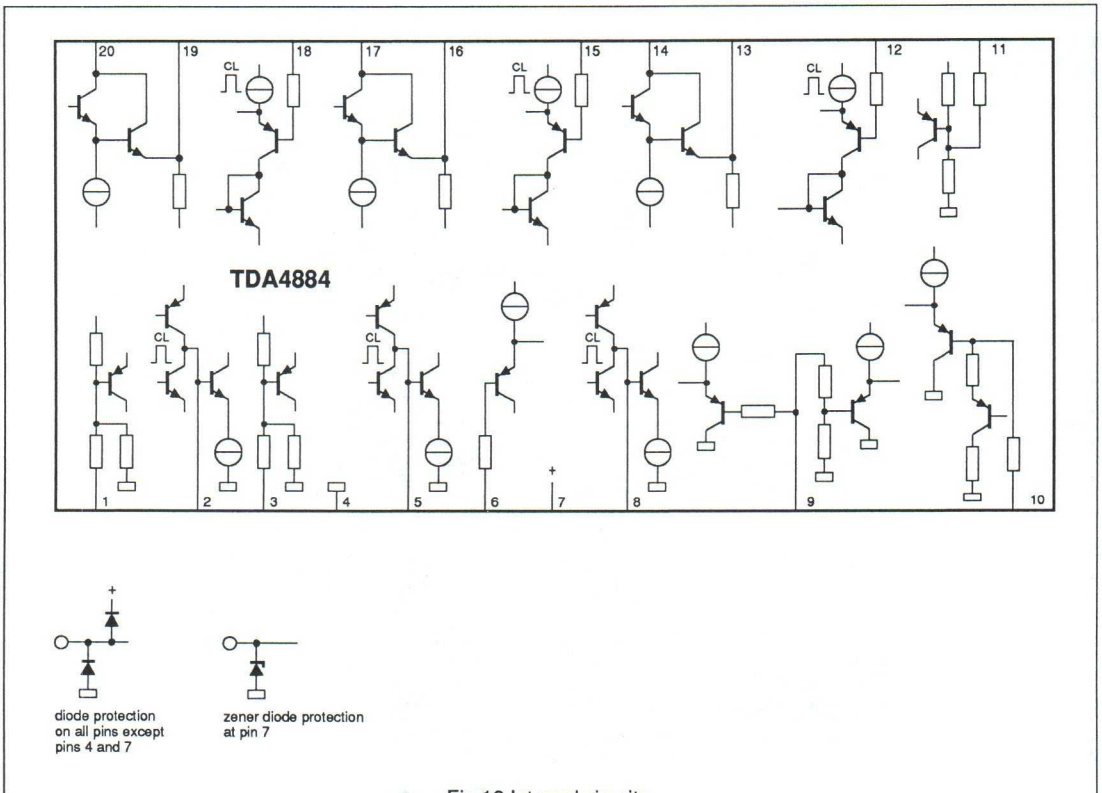


Fig.19 Internal circuits.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	–55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL, plastic (SOT102).

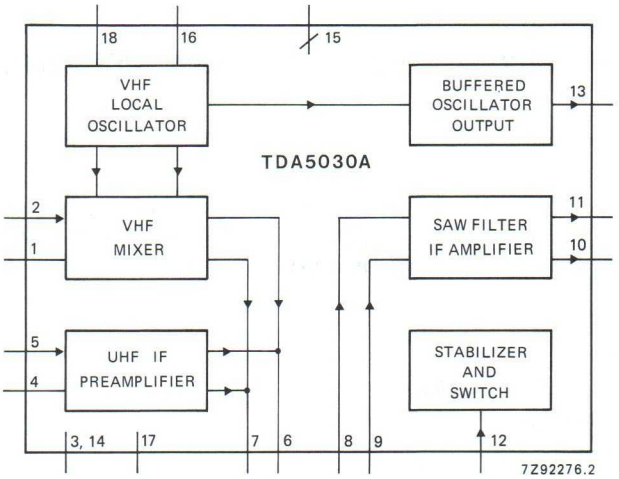


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15-3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	$V_{15}+0,3$	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 55 K/W

CHARACTERISTICS

Measured in circuit of Fig. 2, $V_P = V_{15-3} = 12$ V, $T_{amb} = 25$ °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	V_{15-3}	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	$V_{15}+0,3$	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-14}	100	–	–	dBμV
Voltage gain		A_v	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Yc_{2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω					
	f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	−14	dB

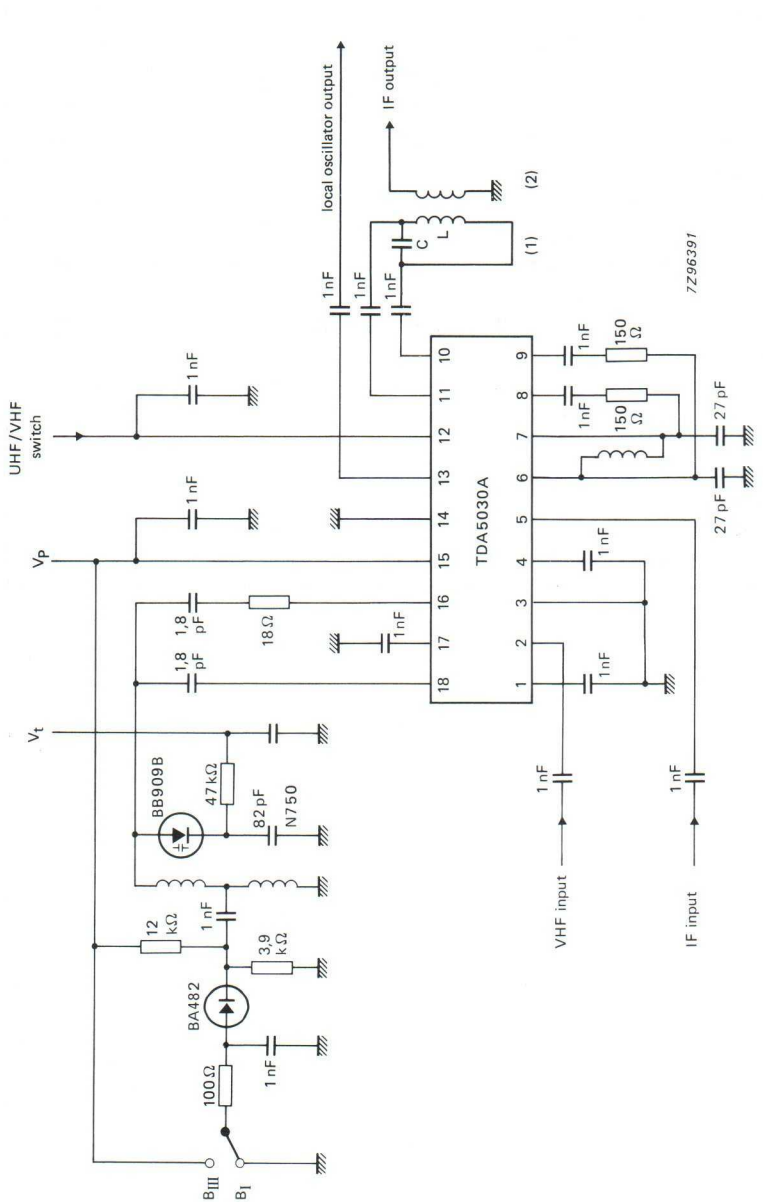


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.

(2) Turns ratio = 7 : 1, load = 50 Ω.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030AT provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 11, 12, 13 and 14

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	25	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 80	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

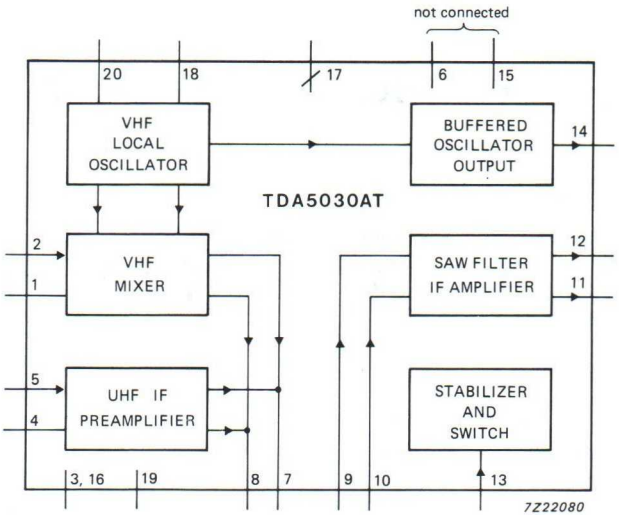


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-3}$	–	14	V
Input voltage (pins 1, 2, 4 and 5)	V_i	0	5	V
VHF switching voltage (pin 13)	V_{13}	0	V_P+0,3	V
Output current (pins 11, 12 or 14)	$-I_{11,12,14}$	–	10	mA
Short-circuit time on outputs (pins 11, 12 and 14)	t_{sc}	–	10	s
Storage temperature range	T_{stg}	–55	+125	°C
Operating ambient temperature range	T_{amb}	–25	+ 80	°C
Junction temperature range	T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

$V_P = V_{17-3} = 12$ V; $T_{amb} = 25$ °C; measured in circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 17)		V_{17-3}	10	–	13,2	V
Supply current		I_{17}	–	42	55	mA
Switch voltage level for VHF (pin 13)		V_{13}	0	–	2,5	V
Switch voltage level for UHF (pin 13)		V_{13}	9,5	–	V_P+0,3	V
Switch current	UHF selected	I_{13}	–0,05	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor (pin 2)	f = 50 MHz	NF	–	7,5	9	dB
	f = 225 MHz	NF	–	9	10	dB
	f = 300 MHz	NF	–	10	12	dB
	f = 470 MHz	NF	–	11	13	dB
Optimum source conductance (pin 2)	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
	f = 470 MHz	G	–	1,9	–	mS
Input conductance (pin 2)	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
	f = 470 MHz	G_i	–	1,45	–	mS
Input capacitance (pin 2)	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	96	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-16}	100	–	–	dBμV
Input voltage for 100 kHz pulling	f = 470 MHz	V_{2-3}	73	–	–	dBμV
Voltage gain		A_v	23	25	27	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance (pin 5)		G_i	–	0,3	–	mS
Input capacitance (pin 5)		C_i	–	3,0	–	pF
Noise factor (pin 5)		NF	–	5	6	dB
Optimum source conductance (pin 5)		G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		V_{5-16}	88	90	–	dBμV
Voltage gain		A_v	32	34	36	dB
VHF mixer						
Conversion transadmittance (pins 2 to 7, 8)		$Yc_{2-7,8}$	–	5,7	–	mS
Output impedance (pins 7 and 8)		Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{11,12}$ = 2 kΩ; f = 36 MHz	$Z_{9,10}$	–	300+ j100	–	Ω
Transimpedance		$Z_{9,10-11,12}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage (pin 14)	R_L = 75 Ω					
	f < 100 MHz	V_{14}	14	20	–	mV
	f > 100 MHz	V_{14}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{14}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

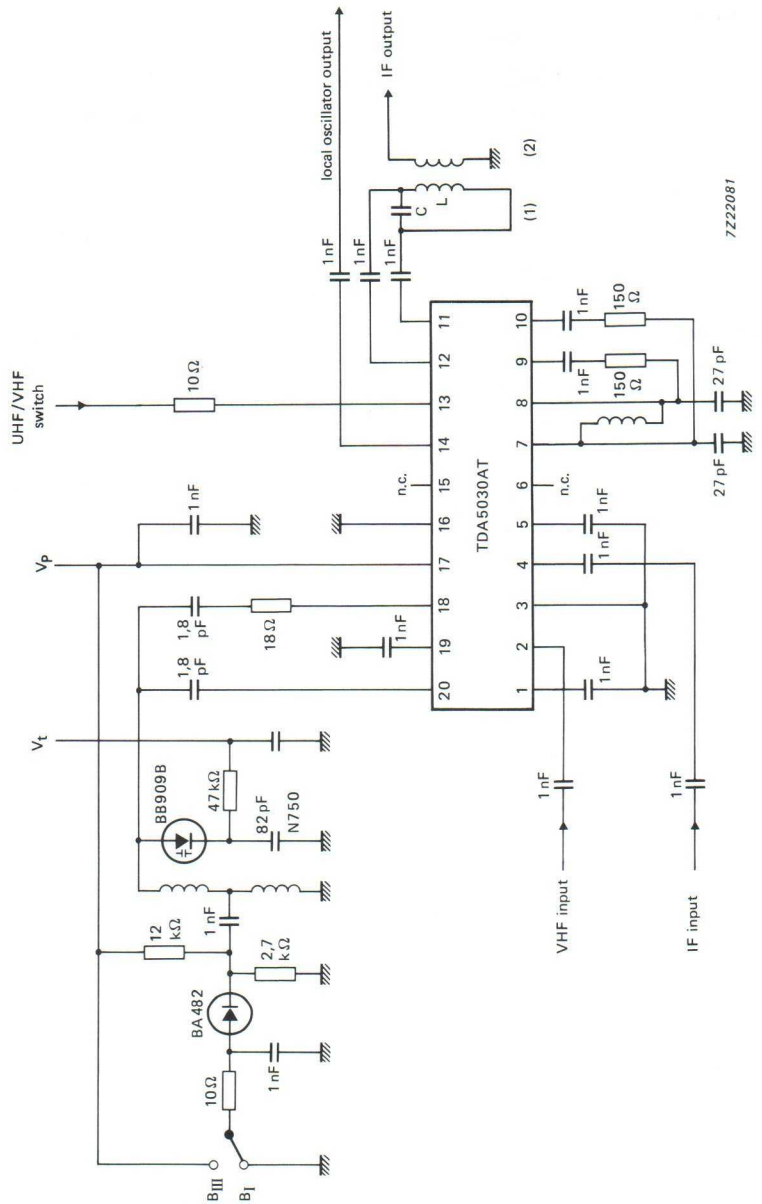


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

Brushless DC motor drive circuit TDA5140A

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.8 A output current (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- VCR
- Laser beam printer
- Fax machine
- Blower
- Automotive.

GENERAL DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 3.9 Ω	0.7	0.8	1	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5140A	18	DIL	plastic	SOT102
TDA5140AT	20	SOL	plastic	SOT163A

BLOCK DIAGRAM

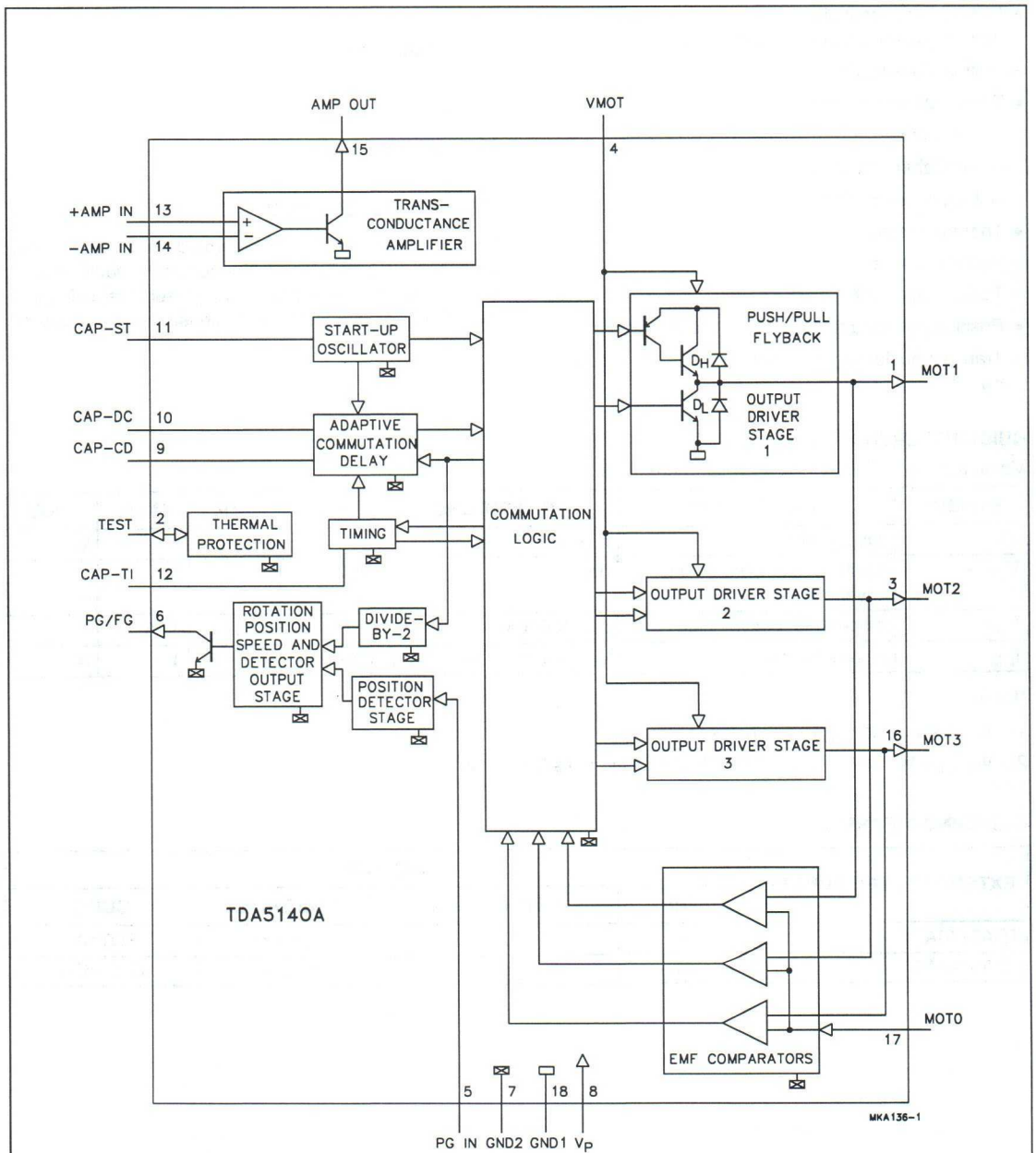


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	DESCRIPTION
MOT1	1	1	driver output 1
TEST	2	2	test input/output
n.c.		3	not connected
MOT2	3	4	driver output 2
VMOT	4	5	input voltage for the output driver stages
PG IN	5	6	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	ground supply return for control circuits
V_P	8	9	positive supply voltage
CAP-CD	9	10	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	external capacitor connection for start-up oscillator
CAP-TI	12	13	external capacitor connection for timing
+AMP IN	13	14	non-inverting input of the transconductance amplifier
–AMP IN	14	15	inverting input of the transconductance amplifier
AMP OUT	15	16	transconductance amplifier output (open collector)
MOT3	16	17	driver output 3
n.c.	–	18	not connected
MOT0	17	19	input from the star point of the motor coils
GND1	18	20	ground (0 V) motor supply return for output stages

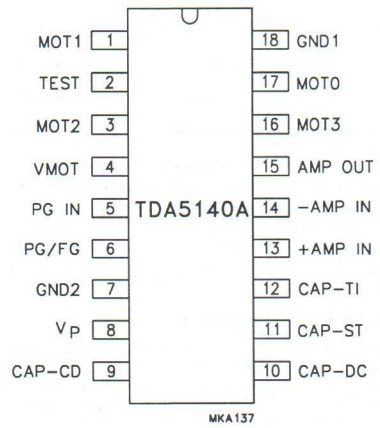


Fig.2 Pin configuration (SOT102; DIL18).

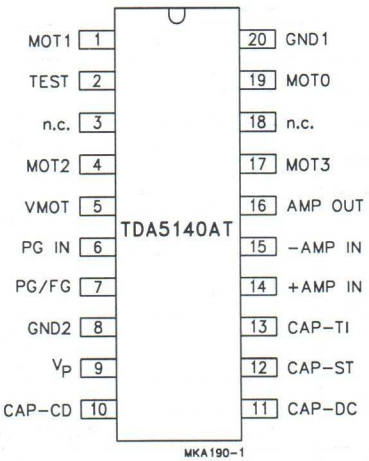


Fig.3 Pin configuration (SOT163A; SO20L).

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (0.8 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Accurate frequency generator (FG) by using the motor EMF.
- Amplifier for external position generator (PG) signal.
- Suitable for use with a wide tolerance, external PG sensor.
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

Brushless DC motor drive circuit TDA5141

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - output current 1.9 A (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- VCR
- Laser beam printer
- Fax machine.

GENERAL DESCRIPTION

The TDA5141 is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. It is ideally suited for applications requiring powerful output stages (minimum current limit of 1.9 A).

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.9	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.6	1.9	2.3	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5141	18	DIL	plastic	SOT102
TDA5141T	28	SOL	plastic	SOT136A
TDA5141AT	20	SOL	plastic	SOT163A

BLOCK DIAGRAM

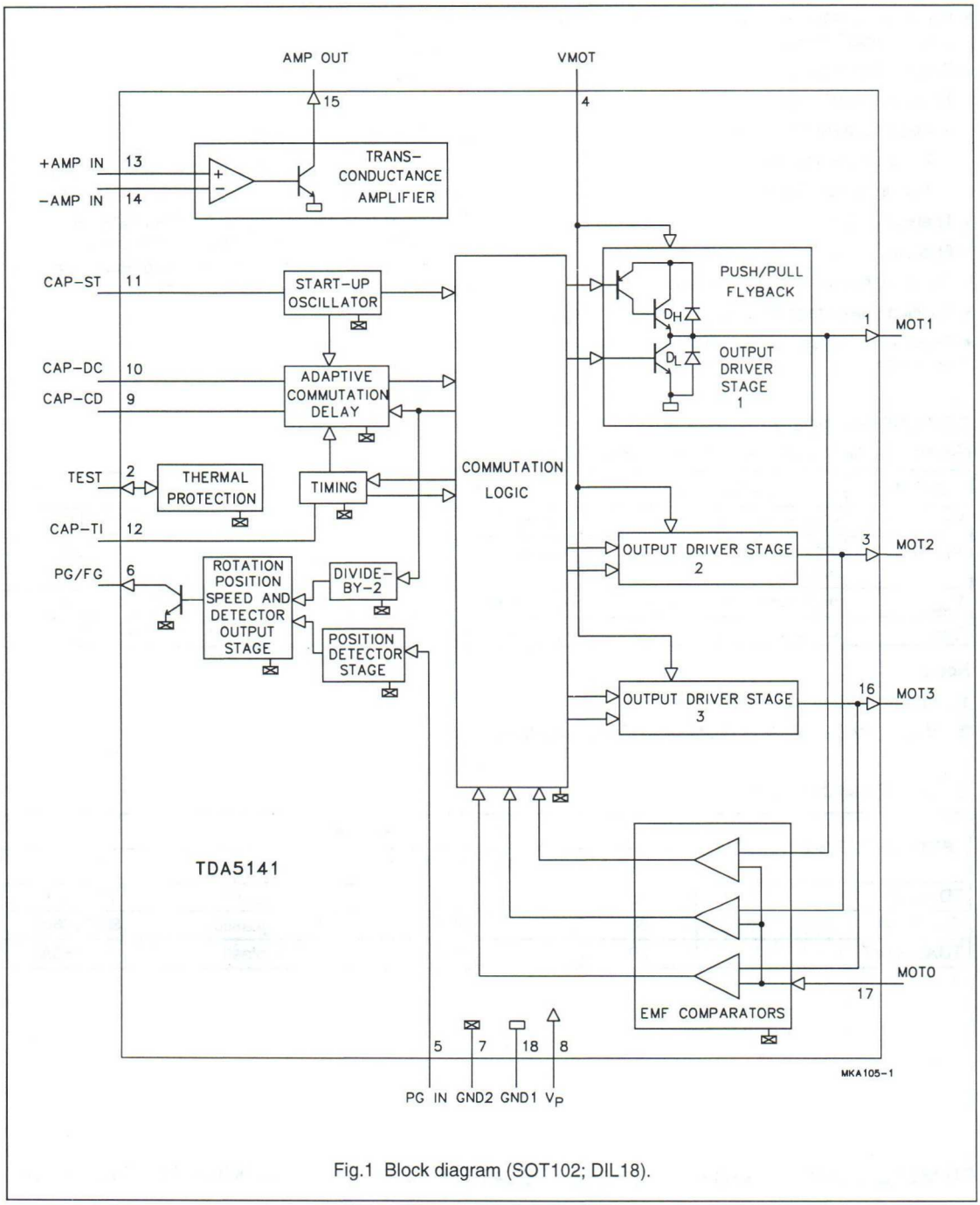


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20L	PIN SO28L	DESCRIPTION
MOT1	1	1	1 and 2	driver output 1
TEST	2	2	3	test input/output
n.c.		3	4	not connected
MOT2	3	4	5 and 6	driver output 2
n.c.	–	–	7	not connected
VMOT	4	5	8 and 9	input voltage for the output driver stages
PG IN	5	6	10	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	11	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	12	ground supply return for control circuits
V_P	8	9	13	supply voltage
CAP-CD	9	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	16	external capacitor connection for start-up oscillator
CAP-TI	12	13	17	external capacitor connection for timing
+AMP IN	13	14	18	non-inverting input of the transconductance amplifier
–AMP IN	14	15	19	inverting input of the transconductance amplifier
AMP OUT	15	16	20	transconductance amplifier output (open collector)
n.c.	–	–	21 and 22	not connected
MOT3	16	17	23 and 24	driver output 3
n.c.	–	18	25	not connected
MOT0	17	19	26	input from the star point of the motor coils
GND1	18	20	27 and 28	ground (0 V) motor supply return for output stages

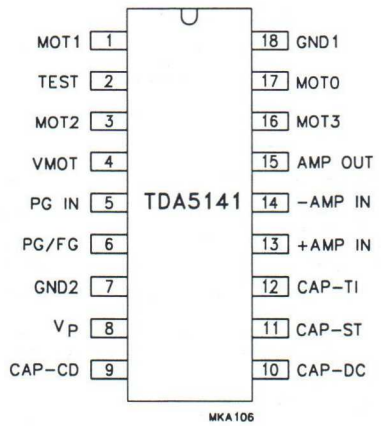


Fig.2 Pin configuration (SOT102; DIL18).

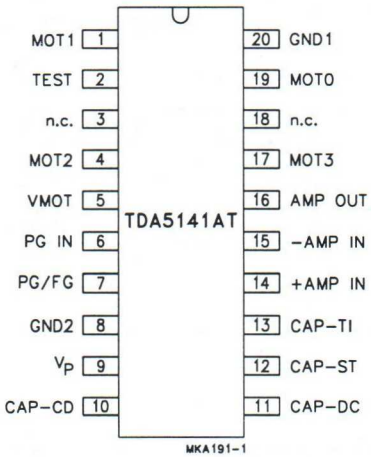


Fig.3 Pin configuration (SOT163A; SO20L).

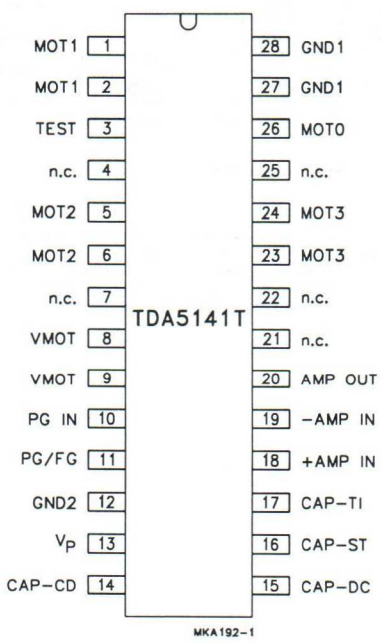


Fig.4 Pin configuration (SOT136A; SO28L).

Brushless DC motor drive circuit TDA5142T

FEATURES

- Full-wave commutation without position sensors
- Built-in start-up circuitry
- Six outputs that can drive three external transistor pairs:
  - 0.15 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor
- Motor brake facility

APPLICATIONS

- General purpose spindle driver (e.g. HDD, fan motor)

DESCRIPTION

The TDA5142T is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for power-drum motors (hard disk drives, tape drives, fan motors).

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.25	mA
V_{VMOT}	input voltage to the output driver stages	3	–	18	V
V_O	driver output voltage range;				
	I_O = 0 mA	0.2	–	–	V
	OUT-NA, NB, NC	–	–	V_{VMOT}	V
	OUT-PA, PB, PC	0.2	–	– 0.9	V
				–	

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5142T	24	SOL	plastic	SOT137A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

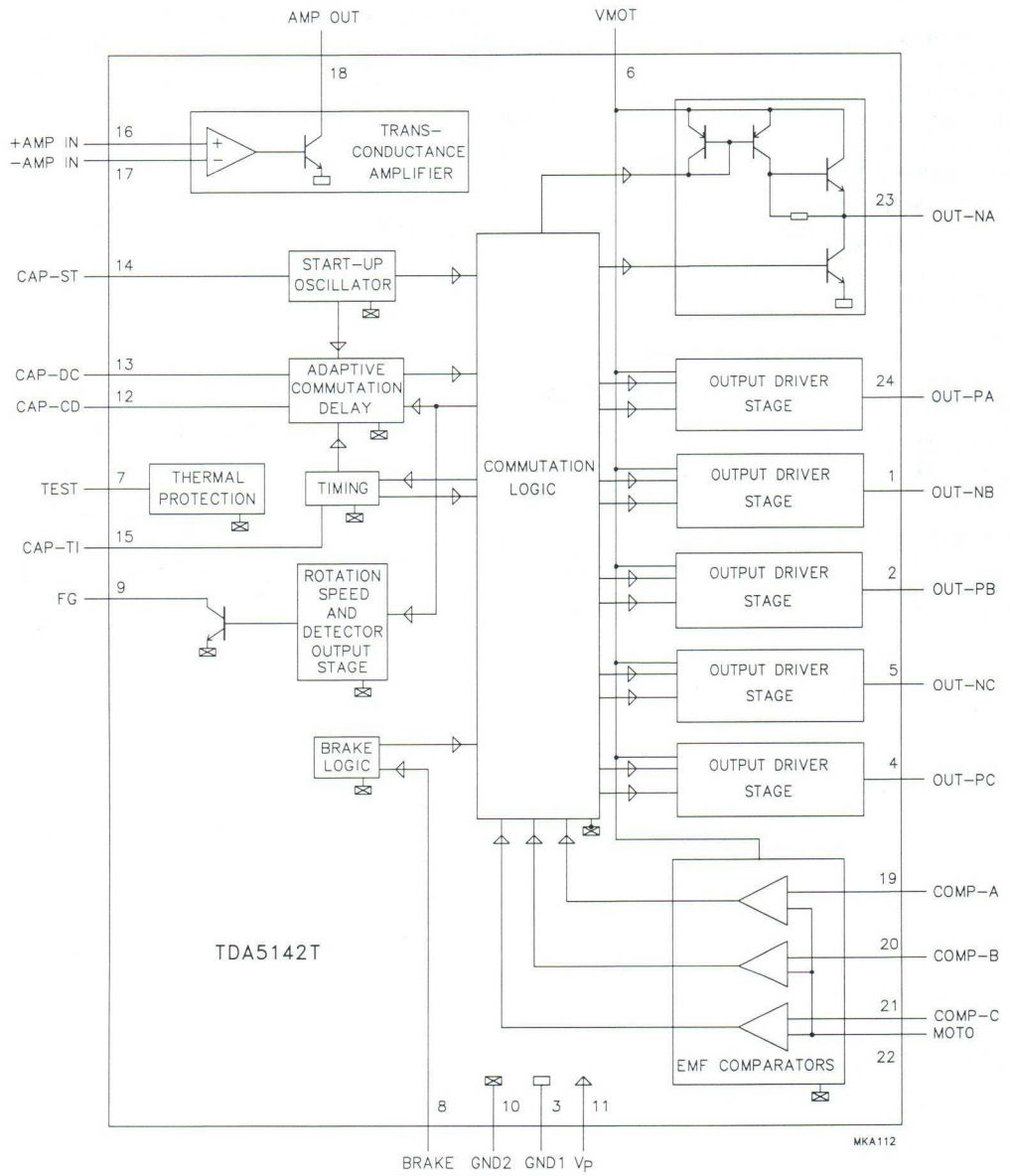


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT-NB	1	driver output for driving the n-channel power FET or power NPN
OUT-PB	2	driver output for driving the p-channel power FET or power PNP
GND1	3	ground (0 V) motor supply return for output stages
OUT-PC	4	driver output for driving the p-channel power FET or power PNP
OUT-NC	5	driver output for driving the n-channel power FET or power NPN
VMOT	6	input voltage for the output driver stages
TEST	7	test input/output
BRAKE	8	brake input command
FG	9	output of the rotation speed position detector stage
GND2	10	ground supply return for control circuits
V_P	11	positive supply voltage
CAP-CD	12	external capacitor connection for adaptive communication delay timing
CAP-DC	13	external capacitor connection for adaptive communication delay timing copy
CAP-ST	14	external capacitor connection for start-up oscillator
CAP-TI	15	external capacitor connection for timing
+AMP IN	16	non-inverting input of the transconductance amplifier
–AMP IN	17	inverting input of the transconductance amplifier
AMP OUT	18	transconductance amplifier output (open collector)
COMP-A	19	input of comparator corresponding to output A
COMP-B	20	input of comparator corresponding to output B
COMP-C	21	input of comparator corresponding to output C
MOT0	22	input from the star point of the motor coils
OUT-NA	23	driver output for driving the n-channel power FET or power NPN
OUT-PA	24	driver output for driving the p-channel power FET or power PNP

FUNCTIONAL DESCRIPTION

The TDA5142T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5142T offers protected outputs capable of driving external power FETs or bipolar power transistors. It can easily be adapted for different motors and applications. The TDA5142T offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Six output drivers
- Maximum output current (0.15 A)
- Outputs protected by current limiting and thermal protection
- Low current consumption
- Accurate frequency generator (FG) by using the motor EMF
- Brake function
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

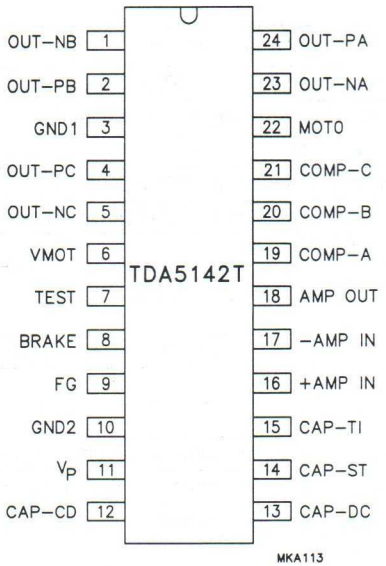


Fig.2 Pin configuration.

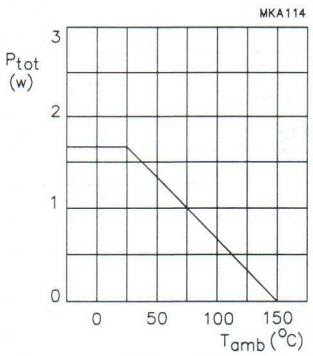


Fig.3 Power derating curve.

Brushless DC motor drive circuit TDA5143T

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.85 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. for HDD)

DESCRIPTION

The TDA5143 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	0.6	0.85	1	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5143T	20	SOL	plastic	SOT163A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

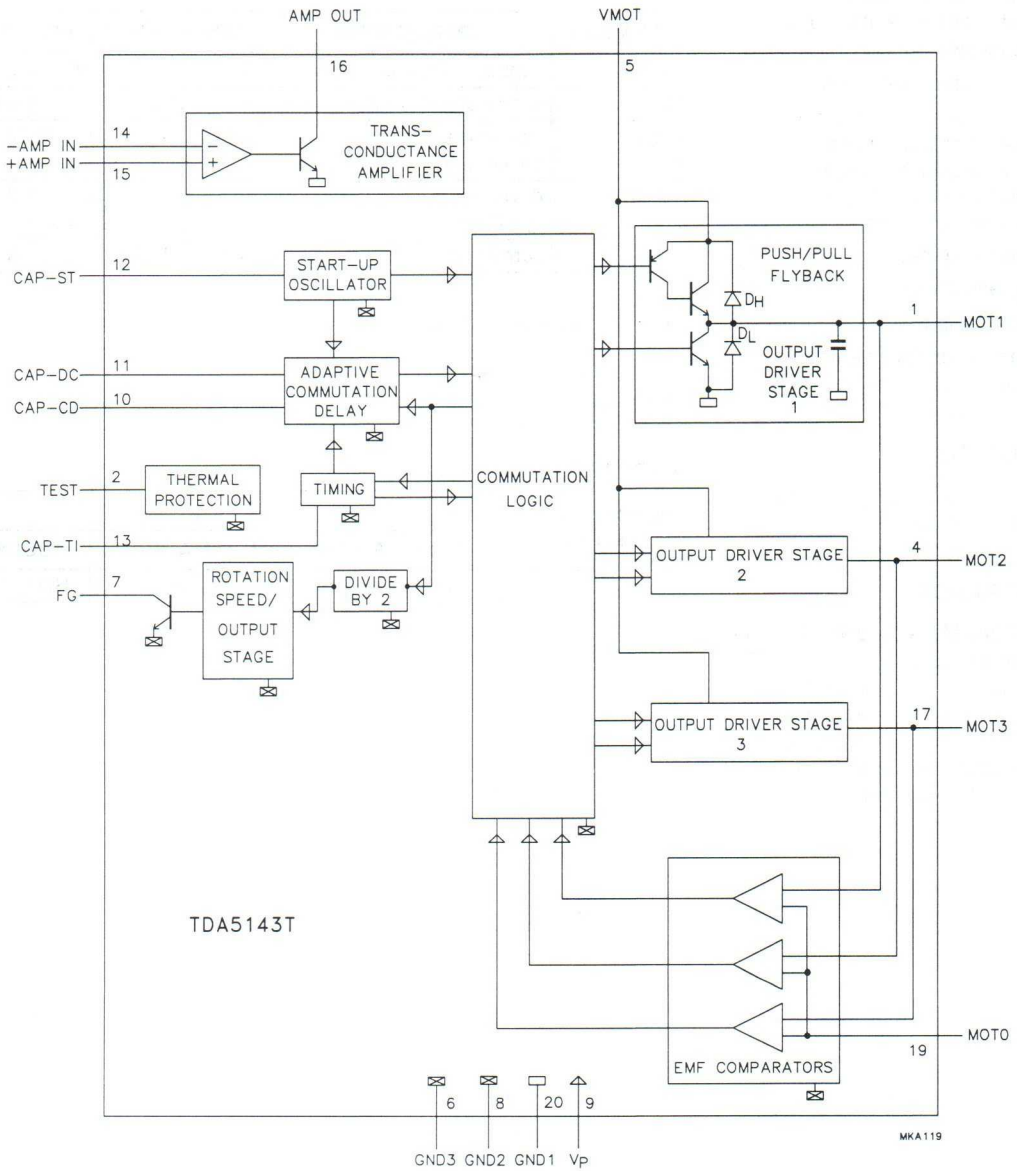


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1	driver output 1
TEST	2	test input/output
n.c.	3	not connected
MOT2	4	driver output 2
VMOT	5	input voltage for the output driver stages
GND3	6	ground supply
FG	7	frequency generator: output of the rotation speed (open collector digital output, negative-going edge is valid)
GND2	8	ground supply return for control circuits
V_P	9	positive supply voltage
CAP-CD	10	external capacitor connection for adaptive communication delay timing
CAP-DC	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	external capacitor connection for start-up oscillator
CAP-TI	13	external capacitor connection for timing
+AMP IN	14	non-inverting input of the transconductance amplifier
–AMP IN	15	inverting input of the transconductance amplifier
AMP OUT	16	transconductance amplifier output (open collector)
MOT3	17	driver output 3
n.c.	18	not connected
MOT0	19	input from the star point of the motor coils
GND1	20	ground (0 V) motor supply return for output stages

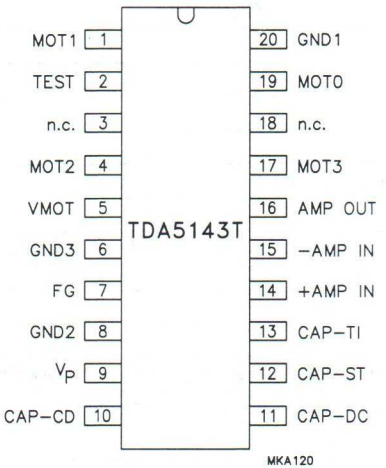


Fig.2 Pin configuration.

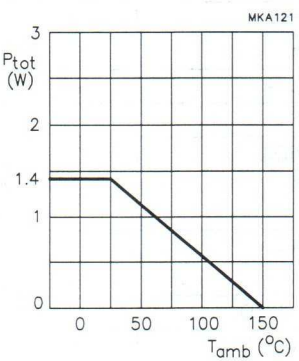


Fig.3 Power derating curve.

Brushless DC motor drive circuit TDA5144T/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. for HDD)

DESCRIPTION

The TDA5144 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.3	1.8	2.3	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5144AT	20	SOL	plastic	SOT163A
TDA5144T	28	SOL	plastic	SOT136A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

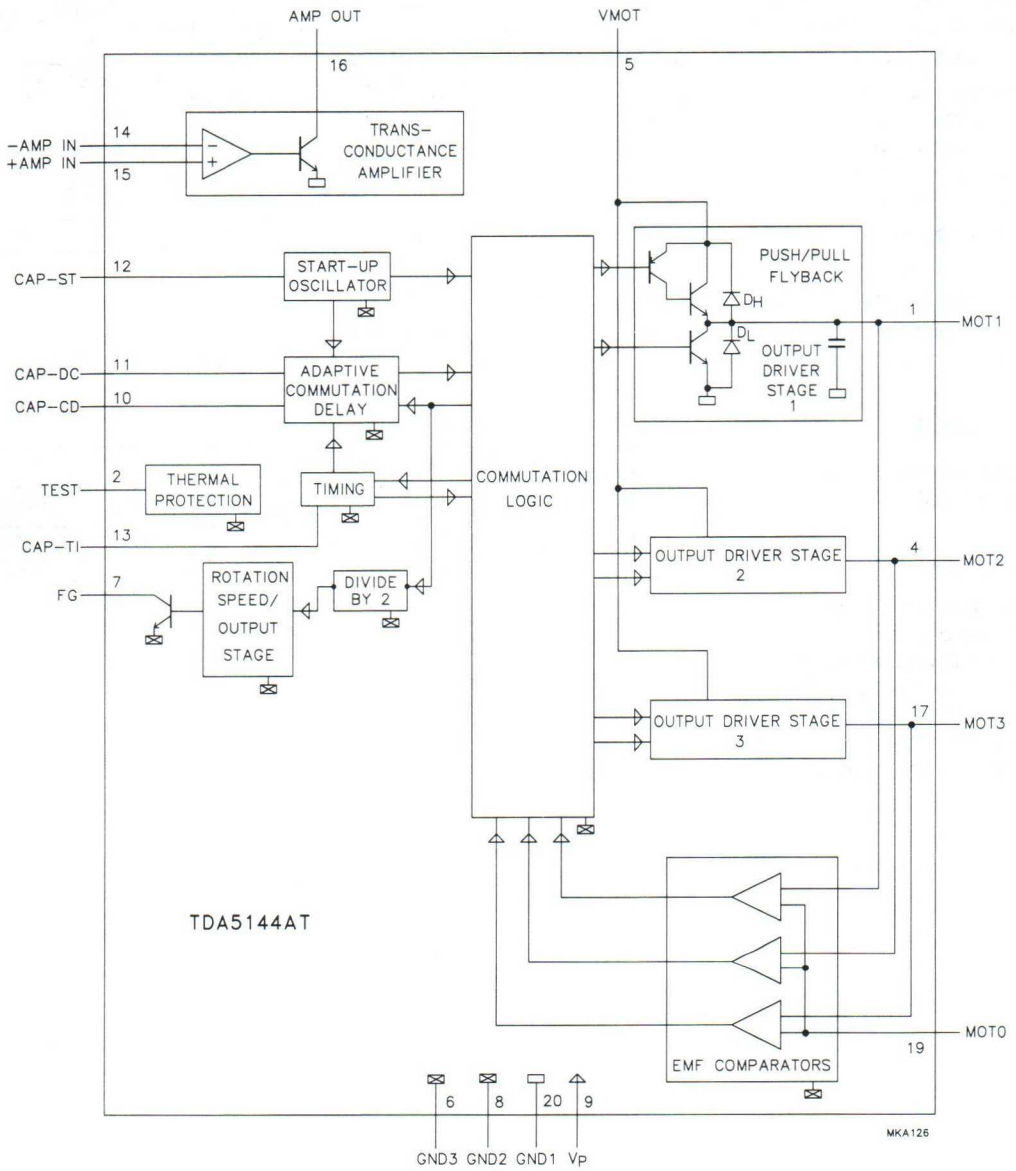


Fig.1 Block diagram (SOT163A; SO20L).

PINNING

SYMBOL	PIN SO20	PIN SO28	DESCRIPTION
MOT1	1	1, 2	driver output 1
TEST	2	3	test input/output
n.c.	3	4	not connected
MOT2	4	5, 6	driver output 2
n.c.		7	not connected
VMOT	5	8, 9	input voltage for the output driver stages
GND3	6	10	ground supply
FG	7	11	frequency generator: output of the rotation speed (open collector digital output, negative-going edge is valid)
GND2	8	12	ground supply return for control circuits
V_P	9	13	positive supply voltage
CAP-CD	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	16	external capacitor connection for start-up oscillator
CAP-TI	13	17	external capacitor connection for timing
+AMP IN	14	18	non-inverting input of the transconductance amplifier
–AMP IN	15	19	inverting input of the transconductance amplifier
AMP OUT	16	20	transconductance amplifier output (open collector)
n.c.		21, 22	not connected
MOT3	17	23, 24	driver output 3
n.c.	18	25	not connected
MOT0	19	26	input from the star point of the motor coils
GND1	20	27, 28	ground (0 V) motor supply return for output stages

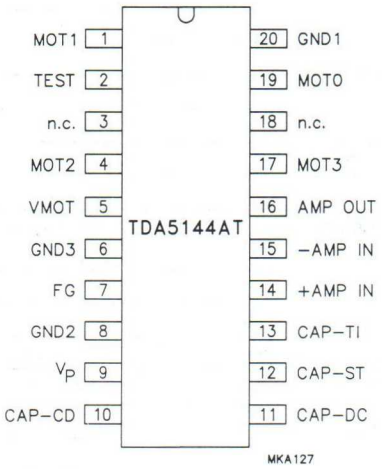


Fig.2 Pin configuration (SOT163A; SO20L).

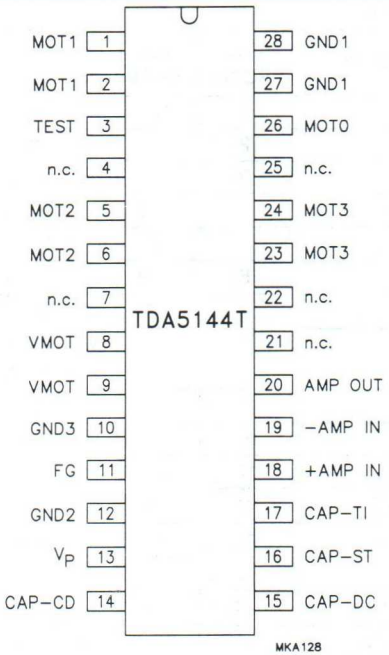


Fig.3 Pin configuration (SOT136A; SO28L).

Brushless DC motor drive circuit TDA5145

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - built-in current limiter
- Thermal protection
- Soft-switching outputs
- Flyback diodes
- Tacho output without extra sensor
- Motor brake facility
- Direction control input
- Reset function
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g.HDD, tape drives)

DESCRIPTION

The TDA5145 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor or tape driver.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.45	1.75	2	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5145	28	DIL	plastic	SOT117AG

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

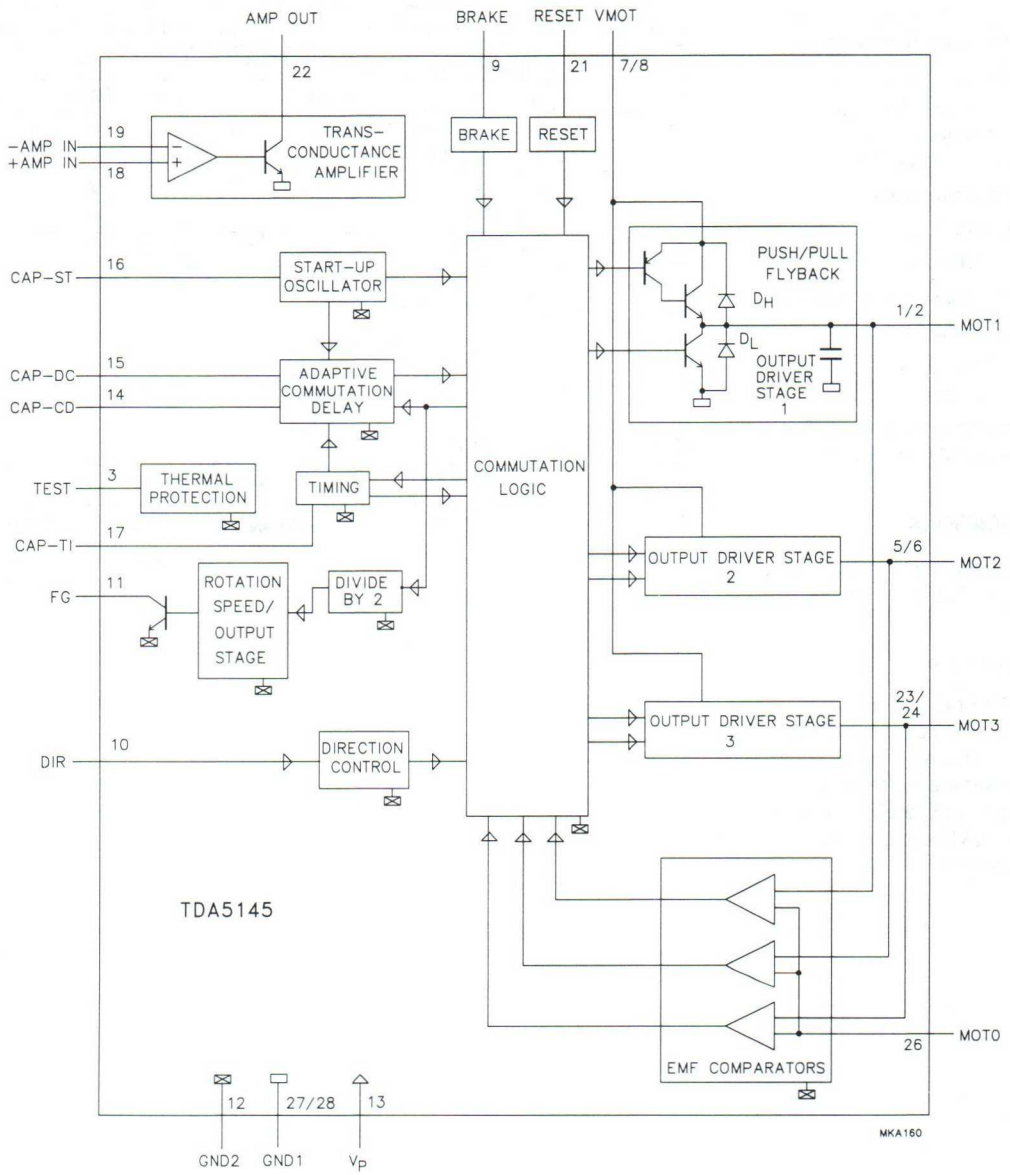


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1, 2	driver output 1
TEST	3	test input/output
n.c.	4	not connected
MOT2	5, 6	driver output 2
VMOT	7, 8	input voltage for the output driver stages
BRAKE	9	brake input
DIR	10	direction control input
FG	11	frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	12	ground supply return for control circuits
V_P	13	positive supply voltage
CAP-CD	14	external capacitor connection for adaptive communication delay timing
CAP-DC	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	16	external capacitor connection for start-up oscillator
CAP-TI	17	external capacitor connection for timing
+AMP IN	18	non-inverting input of the transconductance amplifier
–AMP IN	19	inverting input of the transconductance amplifier
n.c.	20	not connected
RESET	21	reset input
AMP OUT	22	transconductance amplifier output (open collector)
MOT3	23, 24	driver output 3
n.c.	25	not connected
MOT0	26	input from the star point of the motor coils
GND1	27, 28	ground (0 V) motor supply return for output stages

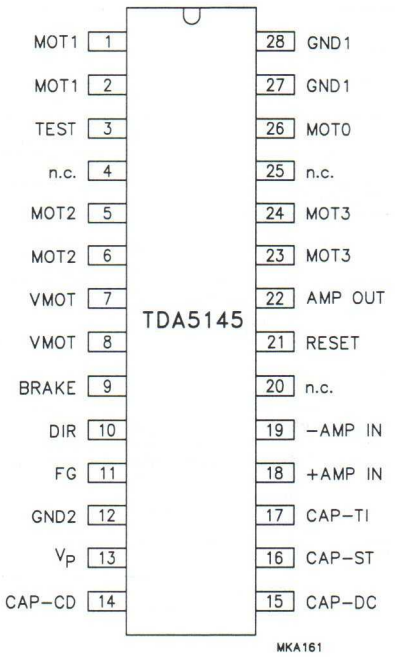


Fig.2 Pin configuration.

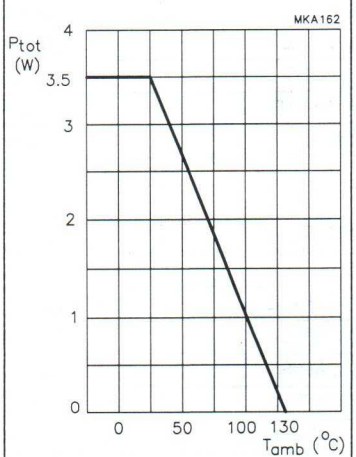


Fig.3 Power derating curve.

VHF, UHF AND HYPERBAND MIXER/OSCILLATOR FOR TV AND VCR 3-BAND TUNERS

GENERAL DESCRIPTION

The TDA5330T is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small 3-band tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B and C
- Balanced oscillator for band B and C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with an output impedance of 100 Ω
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	–	12	–	V
Band A frequency range		f_A	48	–	180	MHz
Band B frequency range		f_B	160	–	470	MHz
Band C frequency range		f_C	430	–	860	MHz
Conversion noise		F	7	–	11	dB
Band A input voltage	1% cross-modulation	$V_{24\text{-}26}$	–	100	–	dBμV
Band B and C input power	1% cross-modulation	P_I	–	–21	–	dBm
Band A voltage gain		G_v	–	24	–	dB
Band B voltage gain		G_v	–	37	–	dB
Band C voltage gain		G_v	–	36	–	dB

PACKAGE OUTLINE

28-lead mini-pack, plastic (SO20; SOT163A).

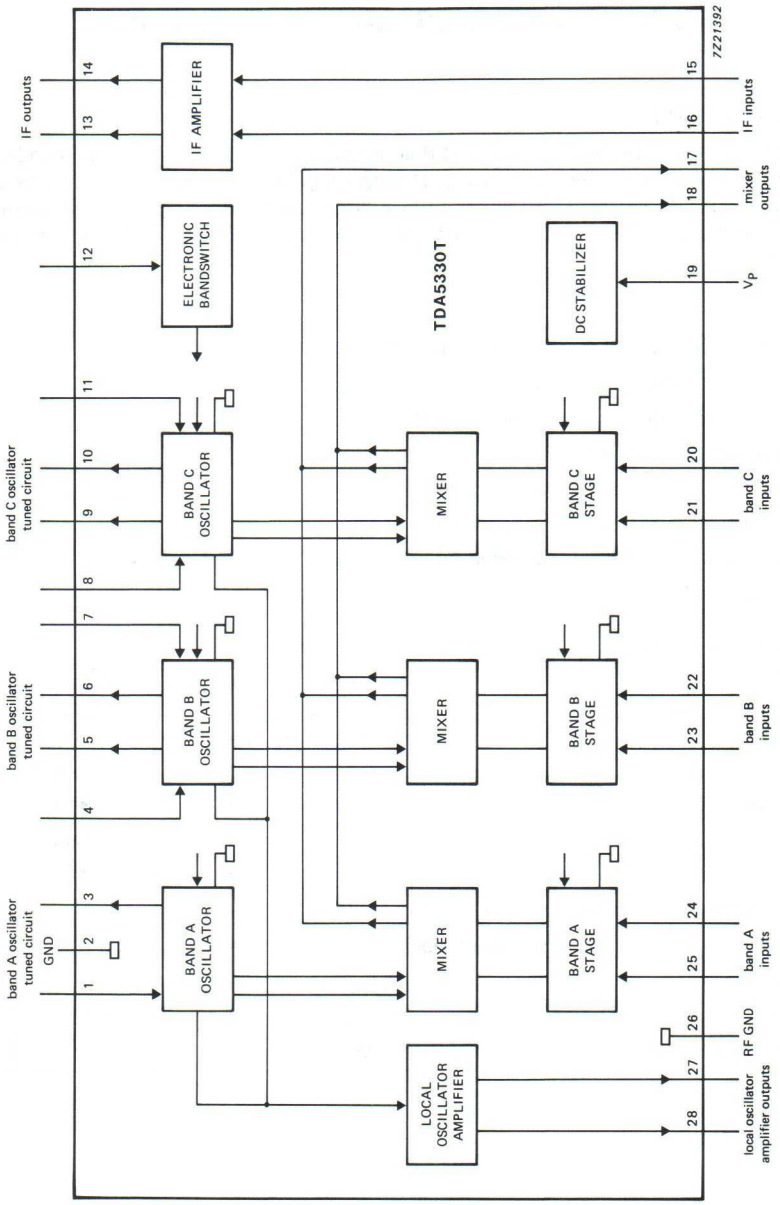


Fig. 1 Block diagram.

DEVELOPMENT DATA

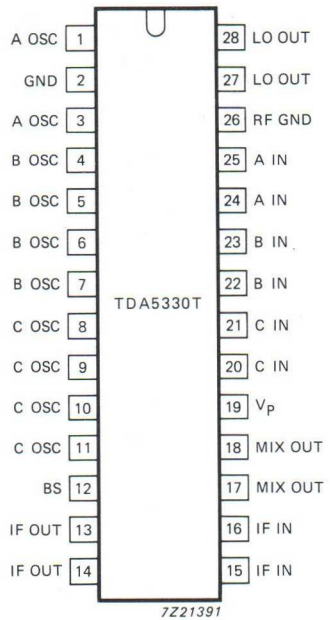


Fig. 2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	C OSC	band C oscillator input
9	C OSC	band C oscillator output
10	C OSC	band C oscillator output
11	C OSC	band C oscillator input
12	BS	electronic bandswitch
13	IF OUT	IF amplifier output
14	IF OUT	IF amplifier output
15	IF IN	IF amplifier input
16	IF IN	IF amplifier input
17	MIX OUT	mixer output
18	MIX OUT	mixer output
19	V_P	positive supply voltage
20	C IN	band C input
21	C IN	band C input
22	B IN	band B input
23	B IN	band B input
24	A IN	band A input
25	A IN	band A input
26	RF GND	ground for RF inputs
27	LO OUT	local oscillator amplifier output
28	LO OUT	local oscillator amplifier output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_{19-2, 26}$	−0.3	14	V
Switching voltage		V_{12}	0	14	V
Output current of each pin to ground		I_O	−	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	−	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 75 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	10	–	13.2	V
Supply current		I_{19}	–	42	55	mA
Switching voltage;						
band A		V_{12}	0	–	1.1	V
band B		V_{12}	1.6	–	2.4	V
band C		V_{12}	3.0	–	5.0	V
Switching current;						
band C		I_{12}	–	–	50	μA
Band A Mixer (including IF amplifier)	measured using circuit shown in Fig. 9					
Frequency range		f_A	48	–	180	MHz
Noise figure	note 1;					
	50 MHz	NF	–	7.5	9	dB
	180 MHz	NF	–	9	10	dB
Optimum source conductance	50 MHz	$G_{24\text{-}26}$	–	0.5	–	mS
	180 MHz	$G_{24\text{-}26}$	–	1.1	–	mS
Input admittance	see Fig. 9					
Input capacitance	50 - 180 MHz	$C_{24\text{-}26}$	–	2	–	pF
Input voltage	1% cross-modulation; in channel	$V_{24\text{-}26}$	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel	$V_{24\text{-}26}$	100	108	–	dBμV
Voltage gain	20 log ($V_{13\text{-}14}/V_{24}$)	G_v	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$Sc = I_{17}/V_{24}$ $= -I_{18}/V_{24}$	$Sc_{24\text{-}17,\ 18}$	–	3.5	–	mS
Mixer output admittance	pins 15 and 16		–	0.1	–	mS
Mixer output capacitance		$C_{17\text{-}18}$	–	2	–	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Band A oscillator						
Frequency range		f_A	80	–	216	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2					
Frequency range		f_B	160	–	470	MHz
Noise figure	pins 22 and 23;					
	200 MHz	NF	–	8	10	dB
	470 MHz	NF	–	8	10	dB
Input admittance	see Fig. 5					
Available input power	1% cross-modulation; in channel; pins 22 and 23;					
	200 MHz	P_{AI}	–24	–21	–	dBm
	470 MHz	P_{AI}	–24	–21	–	dBm
10 kHz pulling	pins 22 and 23; in channel;					
	470 MHz		–	–11	–	dBm
N+5 – 1 MHz pulling	note 3;					
	430 MHz		–	–11	–	dBm
Voltage gain	note 4;					
	200 MHz	G_V	33	36	39	dB
	470 MHz	G_V	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	500	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	500	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.		max.	unit
Band C mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2						
Frequency range		f_C	430	–		860	MHz
Noise figure	pins 20 and 21;						
	430 MHz	NF	–	9		11	dB
	860 MHz	NF	–	9		11	dB
Input admittance	see Fig. 6						
Available input power	1% cross-modulation in channel; pins 20 and 21;						
	430 MHz	P_{AI}	–25	–21		–	dBm
	860 MHz	P_{AI}	–25	–21		–	dBm
10 kHz pulling	pins 20 and 21; in channel;						
	860 MHz		–	–20		–	dBm
N+5 – 1 MHz pulling	note 3;						
	820 MHz		–42	–35		–	dBm
Voltage gain	note 4;						
	430 MHz	G_v	33	36		39	dB
	860 MHz	G_v	33	36		39	dB
Band C oscillator							
Frequency range		f_C	470	–		900	MHz
Frequency shift	ΔV_b = 10%	Δf	–	–		400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–		800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–		200	kHz
				mod.	phase		
IF Amplifier	note 5, differentially measured at 36 MHz; see Fig. 7						
Input reflection coefficient		S_{11}	–	–0,5	–2.0	–	dB/deg
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/deg
Forward transmission coefficient		S_{21}	–	12	160	–	dB/deg
Output reflection coefficient	see Fig. 8	S_{22}	–	–9	10	–	dB/deg

parameter	conditions	symbol	min.	typ.	max.	unit
LO output						
Output voltage into 50 Ω resistor		V_{27-28}	14	35	100	mV
Spurious signal on LO output with respect to LO output signal	note 6	SRF	–	–	−10	dB
LO signal harmonics with respect to LO signal	measured at 50 Ω	SHD	–	–	−10	dB

Notes to the characteristics

1. Measured with an input circuit for optimum noise. (See Fig. 3).

DEVELOPMENT DATA

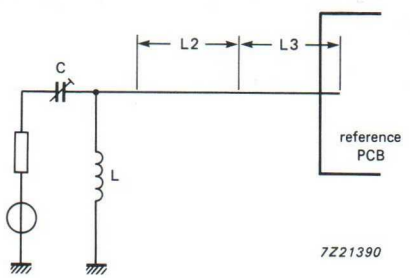


Fig. 3 Input circuit for optimum noise.

Table 1 Component values

component	f = 50 MHz	f = 180 MHz
L	13 t, ϕ 5.5 mm, wire 0.7 mm	*
L2	rigid cable, 2.9 cm	*
L3	rigid cable, 4 cm	*
C	9.6 pF	*

* Value to be fixed.

Notes to the characteristics (continued)

Table 2 Electrical parameters of the circuit (for appropriate impedance and selectivity)

parameter	f = 50 MHz	f = 180 MHz	unit
Insertion loss	0.3	*	dB
Bandwidth	8	*	MHz
Image suppression	15	*	dB
Output impedance (source for IC)	2	*	kΩ

2. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
3. The input level of a N+5 − 1 MHz signal (just visible).
4. The gain is defined as the transducer gain (measured in Fig. 9) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
5. All S parameters are referred to a 50 Ω system.
6. Measured with 50 Ω output impedance on pins 26 and 27 and a RF input signal level of:
   RF level = 1 V at $f < 180$ MHz
   RF power = 0.5 dBm at 100 MHz $< f <$ 225 MHz
   RF power = −10 dBm at 225 MHz $< f <$ 860 MHz

* Value to be fixed.

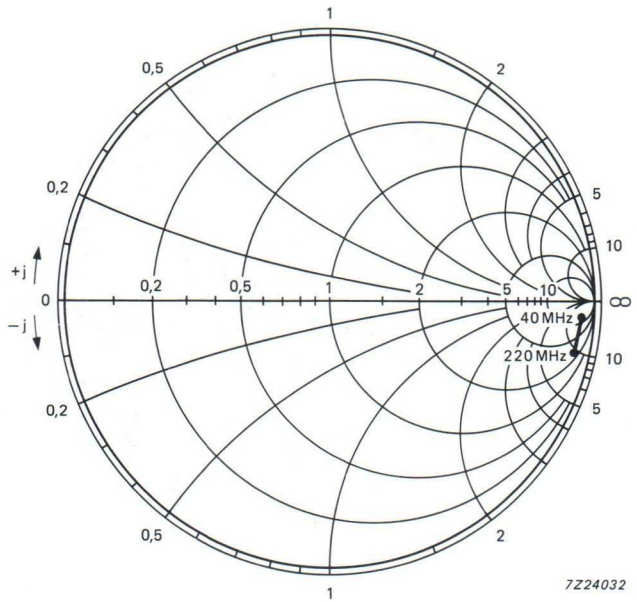


Fig. 4 S11 of the band A mixer input (40 to 220 MHz).

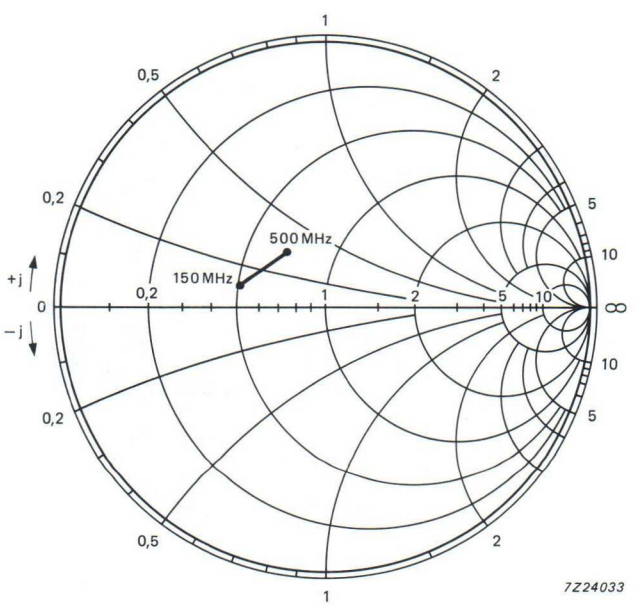


Fig. 5 S11 of the band B mixer input (150 to 500 MHz).

DEVELOPMENT DATA

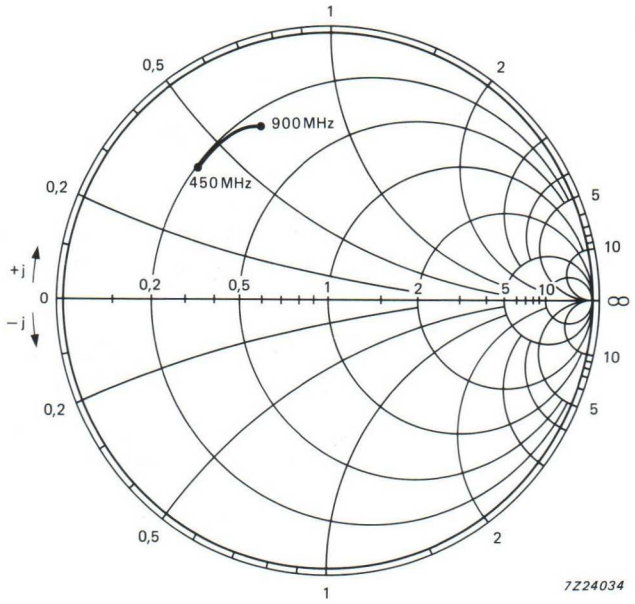


Fig. 6 S11 of the band C mixer input (450 to 900 MHz).

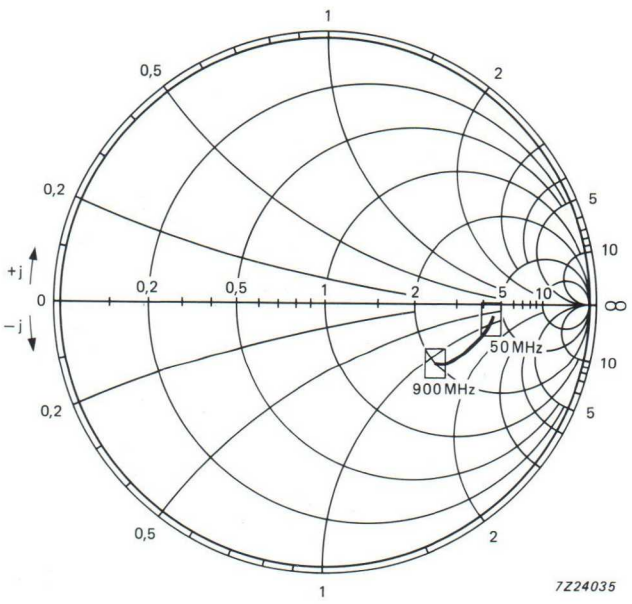


Fig. 7 S11 of the LO output (50 to 900 MHz).

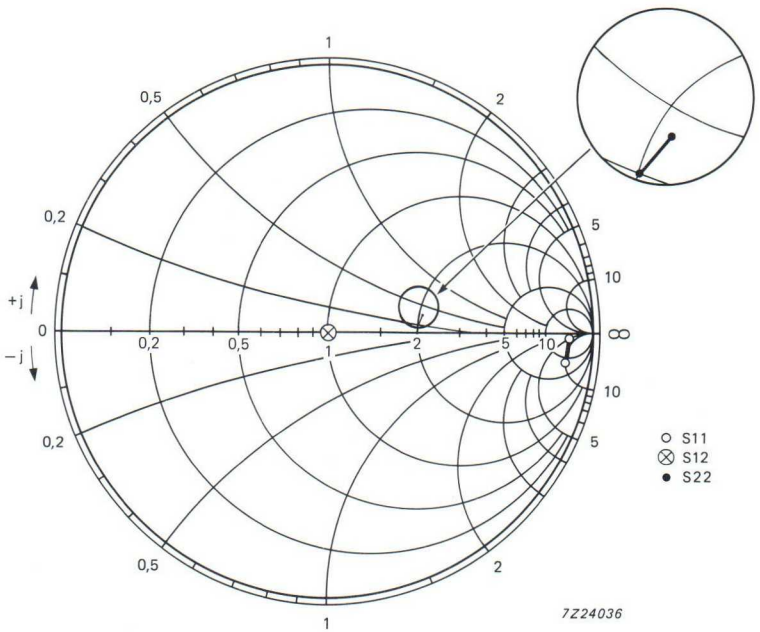


Fig. 8 S11, S12 and S22 of the IF amplifier (30 to 60 MHz).

DEVELOPMENT DATA

APPLICATION INFORMATION

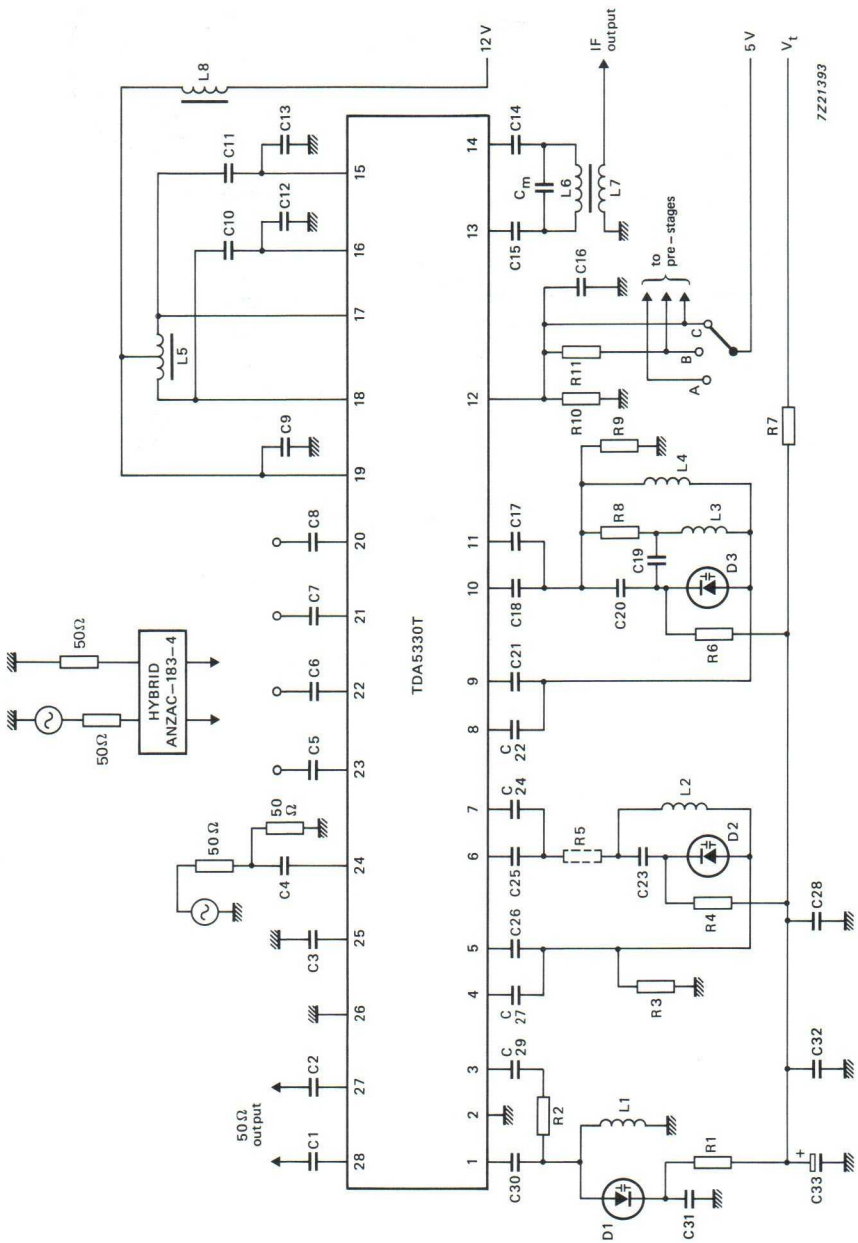


Fig. 9 Test circuit diagram.

DEVELOPMENT DATA

Component values of the test circuit

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 22 kΩ	R4 = 22 kΩ
R5 = 22 Ω (SMD)	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 22 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 1 nF
C9 = 1 nF	C10 = 1 nF	C11 = 1 nF	C12 = 15 pF (N750)
C13 = 15 pF (N750)	C14 = 1 nF	C15 = 1 nF	C16 = 1 nF
C17 = 0.68 pF (SMD)	C18 = 1 pF (SMD)	C19 = 100 pF (SMD)	C20 = 5.6 pF (SMD)
C21 = 1 pF	C22 = 0.68 pF (SMD)	C23 = 150 pF (N750)	C24 = 1.8 pF (N750)
C25 = 3.3 pF (SMD)	C26 = 3.3 pF (SMD)	C27 = 1.8 pF (SMD)	C28 = 1 nF
C29 = 1 pF (NPO)	C30 = 1 pF (NPO)	C31 = 82 pF (N750)	C32 = 1 nF
C33 = 1 μF (40 V)	Cm = 18 pF (N750)		

diodes and IC

D1 = BB911	D2 = BB909B	D3 = BB405B
IC = TDA5330T		

coils

L1 = 6.5 t (ϕ3)	L2 = 1.5 t (ϕ3)	L3 = 1.5 t (ϕ3)	L4 = 1.5 t (ϕ3)
L5 = 2 x 6 t*	L6 = 12 t*	L7 = 2 t (mounted on L6)	L8 = 5 μH (choke coil)

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

DOUBLE MIXER/OSCILLATOR FOR TV AND VCR TUNERS

GENERAL DESCRIPTION

The TDA5332T is an integrated circuit that performs the mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B
- Balanced oscillator for band B
- SAW filter preamplifier with an output impedance of 75 Ω in application
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	12	–	V
Band A frequency range	depending on application	f_A	45	–	470	MHz
Band B frequency range	depending on application	f_B	160	–	860	MHz
Band A noise factor	50 MHz	NF_A	–	7.5	–	dB
Band B noise factor	860 MHz	NF_B	–	9	–	dB
Band A input voltage	1% cross-modulation	$V_{18\text{-}20}$	–	100	–	dBμV
Band B input power	1% cross-modulation note 5	P_I	–	–21	–	dBm
Band A voltage gain		G_{VA}	–	25	–	dB
Band B voltage gain		G_{VB}	–	36	–	dB

PACKAGE OUTLINE

20-lead mini-pack, plastic (SO20L; SOT163A).

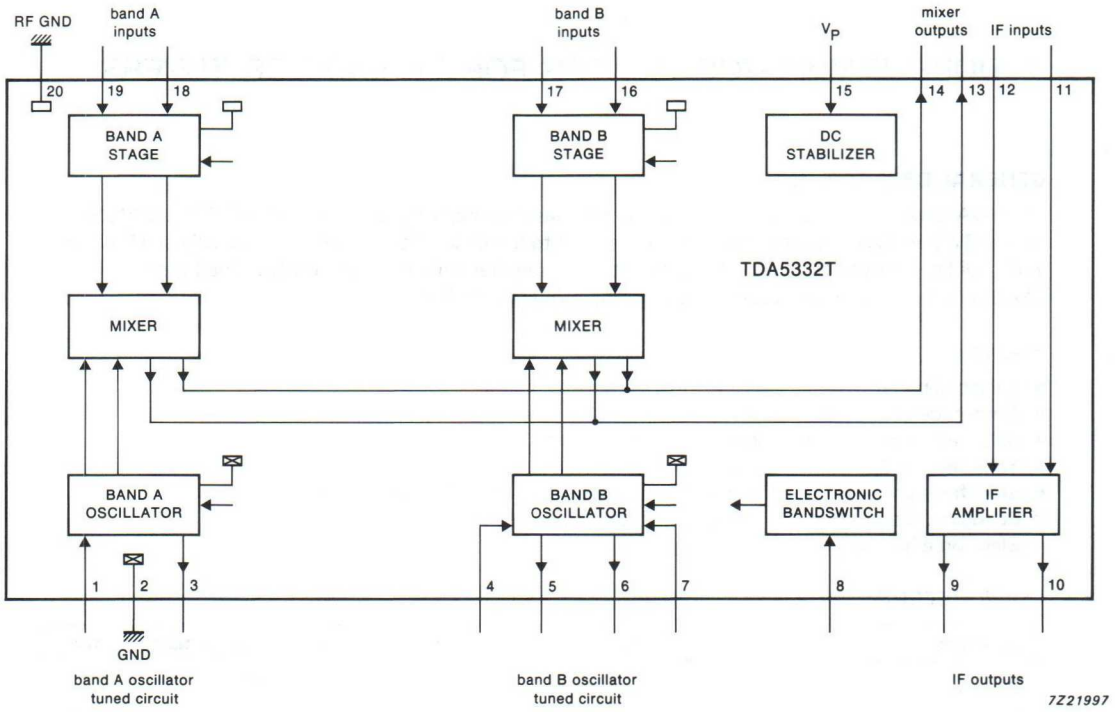


Fig.1 Block diagram.

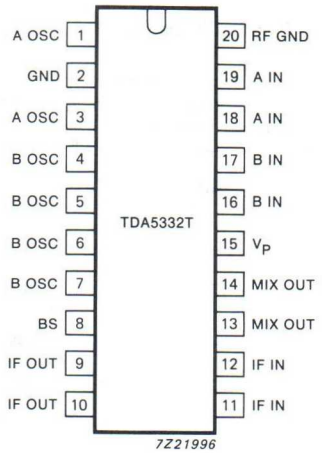


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	BS	electronic bandswitch
9	IF OUT	IF amplifier output
10	IF OUT	IF amplifier output
11	IF IN	IF amplifier input
12	IF IN	IF amplifier input
13	MIX OUT	mixer output
14	MIX OUT	mixer output
15	V_P	positive supply voltage
16	B IN	band B input
17	B IN	band B input
18	A IN	band A input
19	A IN	band A input
20	RF GND	ground for RF inputs

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	−0.3	14	V
Switching voltage		V_8	0	14	V
Output current of each pin to ground		I_O	–	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	–	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C
Junction temperature		T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	typ.	100	K/W

HANDLING

Pins 8, 9 and 10 withstand the ESD test in accordance with MIL-STD-883C category B (2000 V).

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pins 2 and 20); measured in Fig.3; unless otherwise specified.

parameter	conditions	symbol	min.	typ.		max.	unit
Supply voltage		V_{15}	10	–		13.2	V
Supply current		I_{15}	–	42		55	mA
Switching voltage;							
band A		V_{SA}	0	–		1.1	V
band B		V_{SB}	3	–		5	V
Switching current							
band A		I_{SA}	–	–		10	μA
band B		I_{SB}	–	–		50	μA
IF Amplifier	differentially measured at 36 MHz			mod.	phase		
Input reflection coefficient	note 4	S_{11}	–	–0.5	–2	–	dB/°
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/°
Forward transmission coefficient		S_{21}	–	12	160	–	dB/°
Output reflection coefficient		S_{22}	–	–9	10	–	dB/°
Input admittance in application		Y_I	–	–	1.4	–	mS
					0.9	–	pF
Output admittance in application		Z_O	–	–	55	–	Ω
					230	–	nH
Band A mixer (including IF amplifier)	measured using circuit shown in Fig.3						
Frequency range		f_A	45	–		470	MHz
Noise factor	50 MHz	NF	–	7.5		9	dB
	225 MHz	NF	–	9		11	dB
	300 MHz	NF	–	10		12	dB
	470 MHz	NF	–	11		13	dB
Optimum source conductance	50 MHz	$G_{18\text{-}20}$	–	0.5		–	mS
	225 MHz	$G_{18\text{-}20}$	–	1.1		–	mS
	300 MHz	$G_{18\text{-}20}$	–	1.2		–	mS
	470 MHz	$G_{18\text{-}20}$	–	1.9		–	mS

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	50 - 470 MHz	$C_{18\text{-}20}$	–	2.5	–	pF
Input voltage	1% cross-modulation; in channel	$V_{18\text{-}20}$	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel; f < 300 MHz	$V_{18\text{-}20}$	100	108	–	dBμV
Voltage gain	20 log ($V_{9\text{-}10}/V_{18}$)	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$I_{13}/V_{18} = -I_{14}/V_{18}$	C_t	–	3.5	–	mS
Mixer output admittance	pins 13 and 14		–	0.1	–	mS
Mixer output capacitance		$C_{13\text{-}14}$	–	2	–	pF
Band A oscillator						
Frequency range		f_A	80	–	520	MHz
Frequency shift	ΔV_P = 10% note 6; f = 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C note 7; f = 330 MHz	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on; f = 330 MHz	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig.3; measurements using hybrid; note 1					
Frequency range		f_B	160	–	860	MHz
Noise factor not corrected for image	pins 16 and 17					
	160 MHz	NF_B	–	9	11	dB
	860 MHz	NF_B	–	9	11	dB
Available input power	note 5; 1% cross-modulation; in channel; pins 16 and 17;					
	160 MHz	P_{IB}	–25	–21	–	dBm
	860 MHz	P_{IB}	–25	–21	–	dBm
10 kHz pulling	note 5; pins 16 and 17; in channel;					
	860 MHz		–	–20	–	dBm

DEVELOPMENT DATA

CHARACTERISTICS (continued)

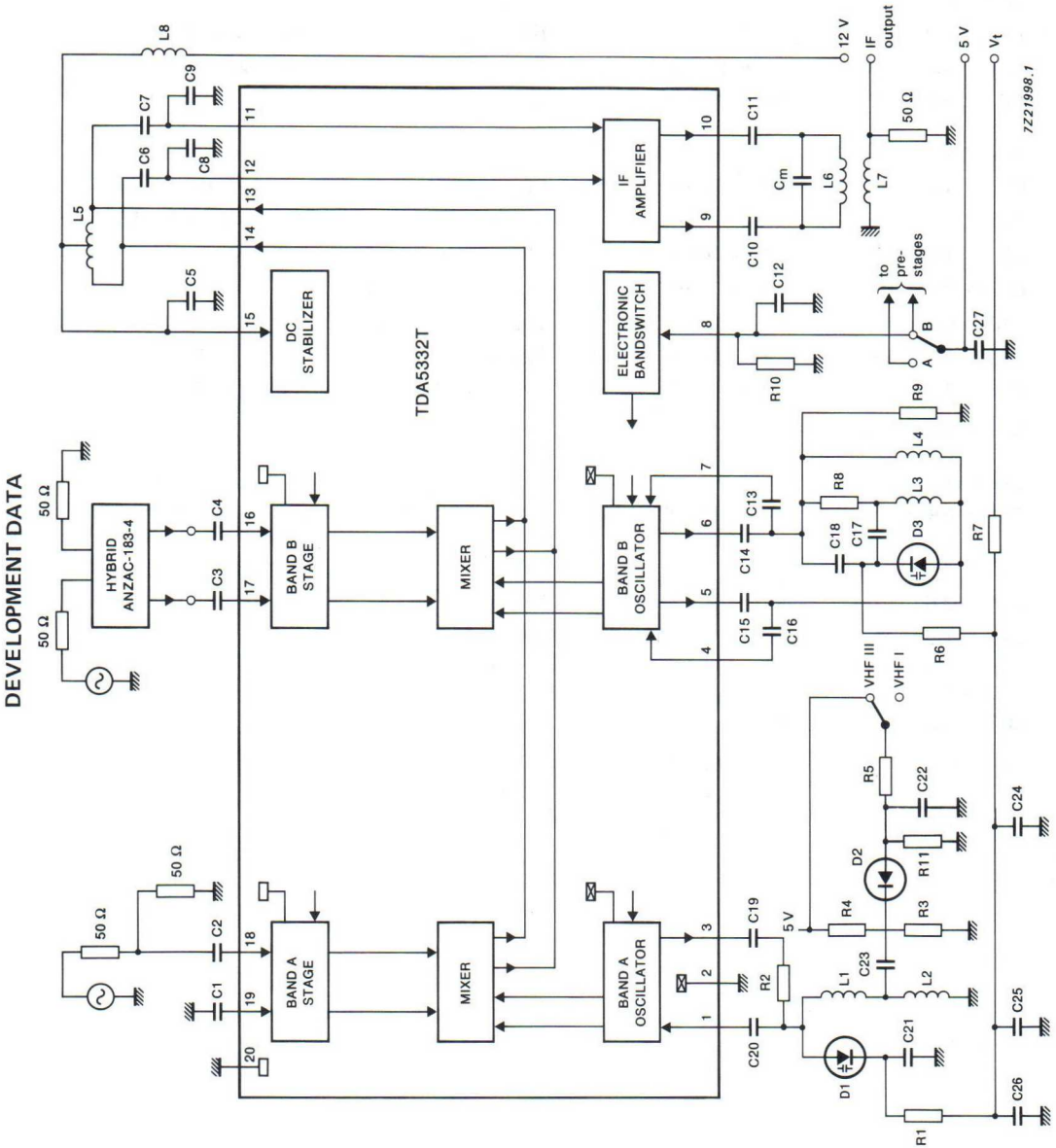
parameter	conditions	symbol	min.	typ.	max.	unit
N + 5 – 1 MHz pulling	notes 2 and 5; 820 MHz		–42	–35	–	dBm
Voltage gain	note 3;					
	160 MHz	G_{VB}	33	36	39	dB
	860 MHz	G_{VB}	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	900	MHz
Frequency shift	note 6; ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	note 7; ΔT = 25 °C	Δf	–	–	800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	400	kHz

Notes to the characteristics

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. The input level of a N + 5 – 1 MHz signal (just visible).
3. The gain is defined as the transducer gain (measured in Fig.3) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
4. All S parameters are referred to a 50 Ω system.
5. The input power is defined as the power delivered by the generator on a 50 Ω load.
6. The frequency shift is defined for a variation of power supply from;
   (a) V_P = 12 V to V_P = 10.8 V
   (b) V_P = 12 V to V_P = 13.2 V
   In both cases the frequency shift is below the specified value.
7. The frequency drift is defined for a variation of ambient temperature from;
   (a) T_{amb} = 25 °C to T_{amb} = 0 °C
   (b) T_{amb} = 25 °C to T_{amb} = 50 °C
   In both cases the frequency shift is below the specified value.

APPLICATION INFORMATION

DEVELOPMENT DATA



Proposal of VHF/UHF tuner band A = VHF I + VHF III (45 to 300 MHz)
band B = UHF (470 to 900 MHz)

Fig.3 Application diagram.

Component values of the application diagram

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 1.2 kΩ	R4 = 4.7 kΩ
R5 = 100 Ω	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 47 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 15 pF (N750)
C9 = 15 pF (N750)	C10 = 1 nF	C11 = 1 nF	C12 = 1 nF
C13 = 0.68 pF (SMD)	C14 = 1 pF (SMD)	C15 = 1 pF (SMD)	
C16 = 0.68 pF (SMD)	C17 = 100 pF (SMD)	C18 = 5.6 pF (SMD)	C19 = 1 pF (NPO)
C20 = 1 pF (NPO)	C21 = 82 pF (N750)	C22 = 1 nF	C23 = 1 nF
C24 = 1 nF	C25 = 1 nF	C26 = 1 μF (40V)	C27 = 1 nF

Cm = 18 pF (N750)

diodes and IC

D1 = BB911	D2 = BA482	D3 = BB405B	IC = TDA5332T

coils

L1 = 2.5 t (ϕ3)	L2 = 8.5 t (ϕ3)	L3 = 1.5 t (ϕ3)
L4 = 1.5 t (ϕ3)	L5 = 2 x 5 t*	L8 = 5 μH (choke coil)

transformer

L6 = 12 t*	L7 = 2 t

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5630

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

DESCRIPTION

The TDA5630 is a monolithic integrated circuit that performs the bands A, B and C mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 3-band tuner.

The tuner development time can be drastically reduced by using this device. In addition, when hyperband is not necessary, the TDA5630 may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHF I and VHF III in band A, and the tuned circuit of band C for UHF.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	35	–	mA
f_{RA}	frequency range; band A	RF input	45	–	180	MHz
f_{RB}	frequency range; band B	RF input	160	–	470	MHz
f_{RC}	frequency range; band C	RF input	430	–	860	MHz
N_{ARA}	noise figure; band A		–	7.5	–	dB
N_B	noise figure; band B		–	8	–	dB
N_C	noise figure; band C		–	9	–	dB
V_{IA}	input voltage; band A	1% cross-modulation	–	93	–	dBμV
V_{IB}	input voltage; band B	1% cross-modulation	–	82	–	dBμV
V_{IC}	input voltage; band C	1% cross-modulation	–	82	–	dBμV
G_v	voltage gain	band A	–	25	–	dB
		band B	–	36	–	dB
		band C	–	36	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5630T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5630M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

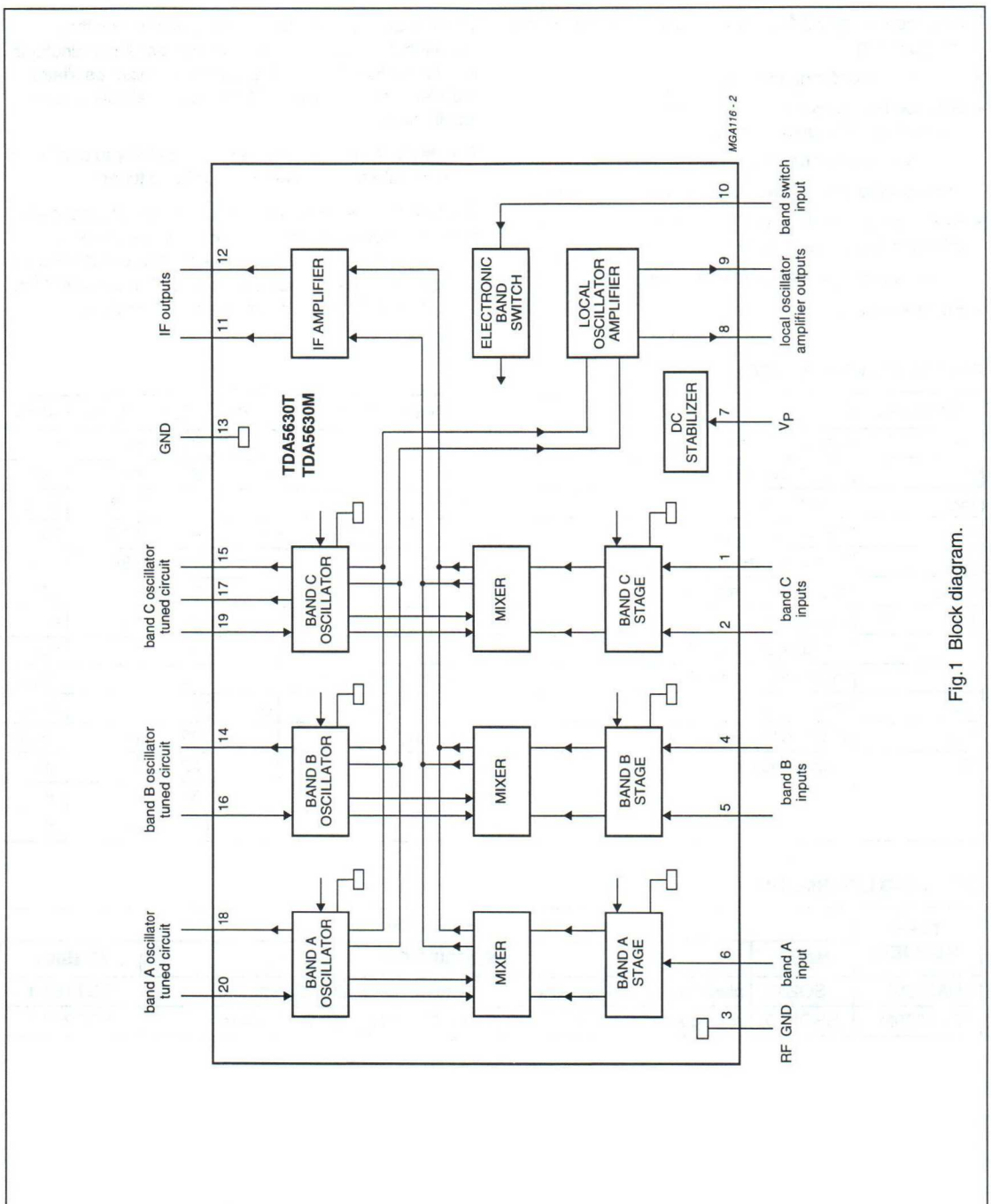


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CIN1	1	band C input 1
CIN2	2	band C input 2
RFGND	3	ground for RF inputs
BIN1	4	band B input 1
BIN2	5	band B input 2
AIN	6	band A input
V_P	7	supply voltage
LOOUT1	8	local oscillator amplifier output 1
LOOUT2	9	local oscillator amplifier output 2
BS	10	electronic bandswitch
IFOUT1	11	IF amplifier output 1
IFOUT2	12	IF amplifier output 2
GND	13	ground (0 V)
BOSCOC	14	band B oscillator output collector
COSCOC1	15	band C oscillator output collector 1
BOSCIB	16	band B oscillator input base
COSCOC2	17	band C oscillator output collector 2
AOSCOC	18	band A oscillator output collector
COSCIB	19	band C oscillator input base
AOSCIB	20	band A oscillator input base

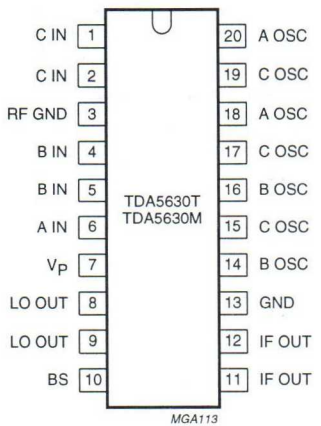


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT163-1	100	K/W
	SOT266-1	120	K/W

HANDLING

Human body model: the IC withstands 3000 V in accordance with UZW-BO-FQ-A302 (stress reference pins 3 and 13 shorted together).

Machine model: the IC withstands 200 V in accordance with UZW-BO-FQ-B302 (stress reference pins 3 and 13 shorted together).

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	see Fig.9	–	−10	9	–	dB/0
Z_o	output impedance (R_s + j$L_s\Omega$)	R_s	–	95		–	Ω
		L_s	–	45		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

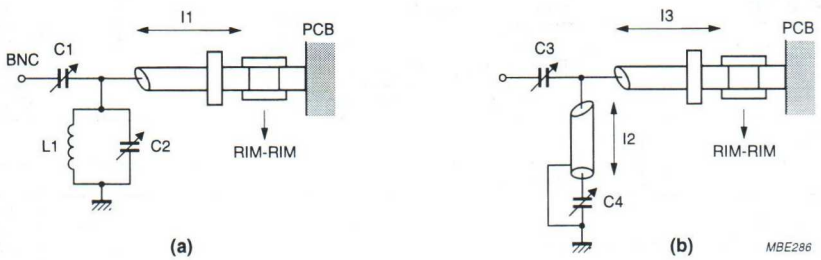
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9	9.9	V
I_P	supply current		–	35	45	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band B	1.6	–	2.4	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A	–	–	2	µA
		band B	–	–	5	µA
		band C	–	–	10	µA
Band A mixer (pin 6)						
f_R	frequency range		45	–	180	MHz
N	noise figure	50 MHz; see Fig.3	–	7.5	9	dB
		180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for noise figure	50 MHz	–	0.5	–	mS
		180 MHz	–	1.1	–	mS
g_i	input conductance	50 MHz; see Fig.5	–	0.26	–	mS
		180 MHz; see Fig.5	–	0.35	–	mS
C_I	input capacitance	50 to 180 MHz	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel f = 180 MHz	90	93	–	dBµV
		10 kHz pulling; in channel f = 180 MHz	–	100	–	dBµV
G_v	voltage gain	20 log (V12-11/V6); 50 MHz	22.5	25	27.5	dB
		20 log (V12-11/V6); 180 MHz	22.5	25	27.5	dB
Band A oscillator						
f_R	frequency range		80	–	216	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0NP0 capacitors; note 2	–	–	500	kHz
		5 s to 15 min after switch on; note 2	–	–	200	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (pins 4 and 5; including IF amplifier); measurements using hybrid; note 3						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	170 MHz	–	8	10	dB
		470 MHz	–	8	10	dB
Z_I	input impedance (R_S + j$L_S\Omega$)	R_S; see Fig.6	–	30	–	Ω
		L_S; see Fig.6		8		nH
V_i	input voltage	1% cross-modulation; in channel; 170 MHz	79	82	–	dBμV
		1% cross-modulation; in channel; 470 MHz	79	82	–	dBμV
		10 kHz pulling; in channel; 470 MHz; TDA5630T	–	91	–	dBμV
		10 kHz pulling; in channel; 470 MHz; TDA5630M	–	83	–	dBμV
		N + 5 – 1 MHz pulling; 430 MHz; TDA5630T; note 4	–	81	–	dBμV
		N + 5 – 1 MHz pulling; 430 MHz; TDA5630M; note 4	–	66	–	dBμV
G_v	voltage gain	170 MHz; note 5	33	36	39	dB
		470 MHz; note 5	33	36	39	dB
Band B oscillator						
f_R	frequency range		200	–	500	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation: NP0 capacitors; note 2	–	–	2	MHz
		5 s to 15 min after switch on; note 2	–	–	300	kHz
Band C mixer (pins 1 and 2; including IF amplifier); measurements using hybrid; note 3						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	430 MHz	–	9	11	dB
		860 MHz	–	9	11	dB
Z_I	input impedance (R_S + j$L_S\Omega$)	R_S; 430 MHz; see Fig.7	–	40	–	Ω
		R_S; 860 MHz; see Fig.7	–	53	–	Ω
		L_S; 430 to 860 MHz	–	9	–	nH
V_i	input voltage	1% cross-modulation; in channel; 430 MHz	79	82	–	dBμV
		1% cross-modulation; in channel; 860 MHz	79	82	–	dBμV
		10 kHz pulling; in channel; 860 MHz; TDA5630T	–	87	–	dBμV
		10 kHz pulling; in channel; 860 MHz; TDA5630M	–	93	–	dBμV
		N + 5 – 1 MHz pulling; 820 MHz; note 4	–	61	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_v	voltage gain	430 MHz; note 5	33	36	39	dB
		860 MHz; note 5	33	36	39	dB
Band C oscillator						
f_R	frequency range		470	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 2	–	–	2.5	MHz
		5 s to 15 min after switching on; note 2	–	–	600	kHz
LO output (pins 8 and 9; R_L = 100 Ω)						
S_{22}	output reflection coefficient	see Fig.8				
V_O	output voltage		14	35	100	mV
SRF	spurious signal on LO output w.r.t. LO output signal	note 7	–	–	–10	dB
SHD	LO signal harmonics w.r.t. LO signal		–	–	–10	dB

Notes

1. The frequency shift is defined for a variation of power supply, first from V_P = 9 to 8.1 V, then from V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
2. The frequency drift is defined for a variation of ambient temperature, first from T_{amb} = 25 °C to T_{amb} = 0 °C, then from T_{amb} = 25 °C to T_{amb} = 50 °C. In both cases, the frequency drift is below the specified value with NP0 capacitors. Capacitor types C1 to C11, as specified in Fig.4 for non-PLL applications, must be changed to series with other temperature coefficients (e.g. N330, N750 etc.).
3. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
4. The input level of a N + 5 – 1 MHz signal which gives a signal 30 dB below the oscillator carrier at the LO output.
5. The gain is defined as the transducer gain (measured in Fig.4) plus the voltage transformation ratio of L6 to L7 (6 : 1, 15.4 dB).
6. Measured at 50 Ω, with RF input voltage:
   a) RF voltage = 120 dBμV at f < 180 MHz
   b) RF voltage = 107.5 dBμV at 180 MHz < f < 225 MHz
   c) RF voltage = 97 dBμV at 225 MHz < f < 860 MHz.
7. All S-parameters are referred to a 50 Ω system.



(a) For f_R = 50 MHz:

mixer A frequency response measured = 57 MHz, loss = 0 dB

image suppression = 16 dB

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (Δ 5.5 mm, wire diam. = 0.5 mm)

l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50; 96 pF/m).

(b) For f_R = 180 MHz:

mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB

image suppression = 13 dB

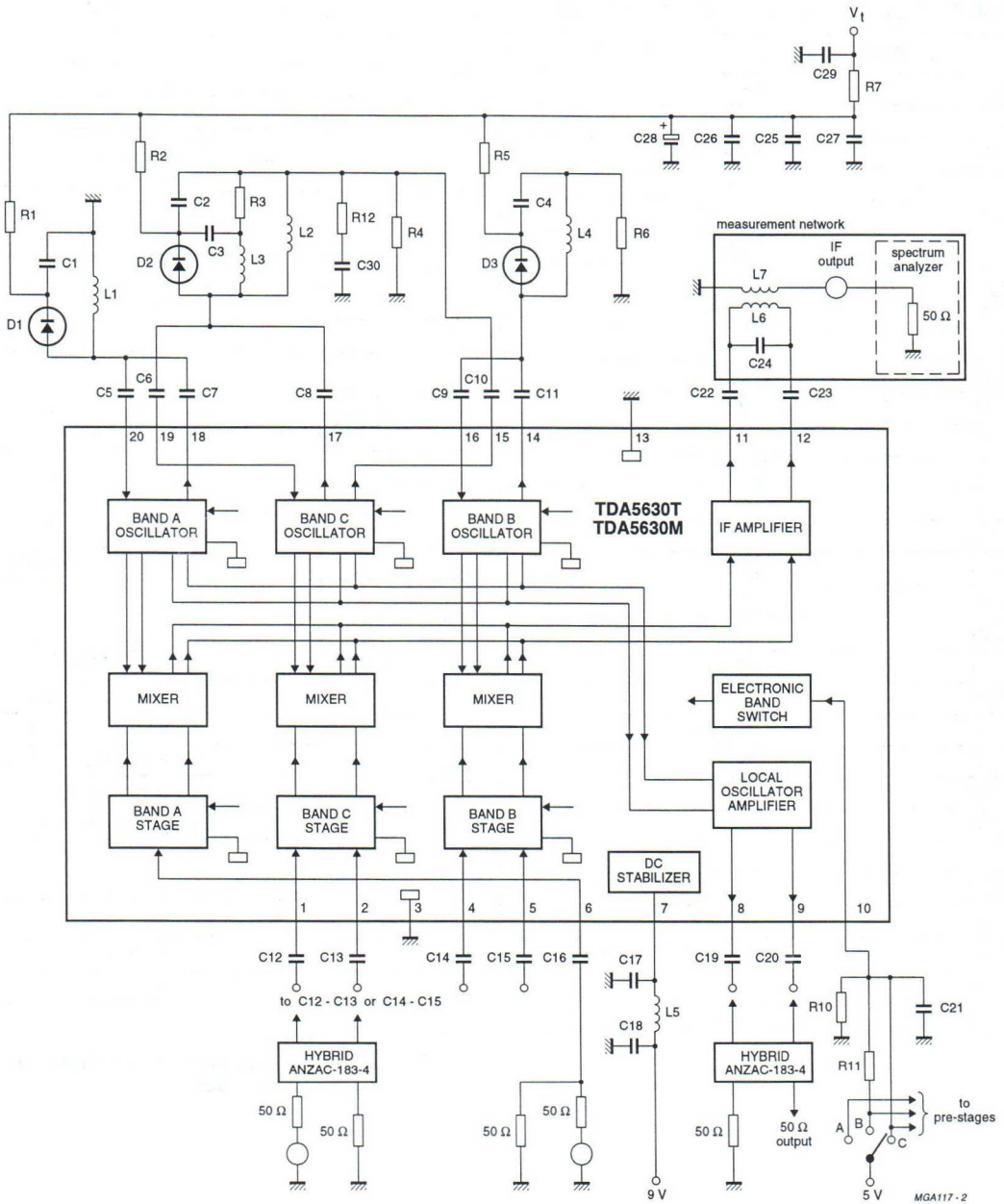
C3 = 5 pF

C4 = 25 pF

l2 = rigid cable (RIM): 30 cm long

l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.



L6, L7 and C24 are only required for measurement purposes; they are not used in a tuner.

Fig.4 Measurement circuit.

Component values for measurement circuit

Table 1 Capacitors (all SMD and NP0 except C28)

COMPONENT	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	150 pF
C5	2.2 pF
C6	1 pF
C7	2.2 pF
C8	1 pF
C9	1.8 pF
C10	2.2 pF
C11	3.9 pF
C12	1 nF
C13	1 nF
C14	1 nF
C15	1 nF
C16	1 nF
C17	1.5 nF
C18	1.5nF
C19	1 nF
C20	1 nF
C21	1.5 nF
C22	1 nF
C23	1 nF
C24	18 pF
C25	1.5 nF
C26	1.5 nF
C27	1.5 nF
C28	1 μF; 40 V electrolytic
C29	1.5 nF
C30	0.56 pF

Table 2 Resistors (all SMD)

COMPONENT	VALUE
R1	47 kΩ
R2	22 kΩ
R3	2.2 kΩ
R4	22 kΩ
R5	47 kΩ
R6	22 Ω
R7	1 kΩ
R10	15 kΩ
R11	36 kΩ
R12	470 Ω

Table 3 Diodes and IC

COMPONENT	VALUE
D1	BB911
D2	BB405/215
D3	BB909/219
IC	TDA5630T/TDA5630M

Table 4 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L1	7.5 turns; dia. 3 mm
L2	2.5 turns; dia. 3 mm
L3	1.5 turns; dia. 2.5 mm
L4	1.5 turns; dia. 4 mm
L5	4.7 μH; choke coil

Table 5 Transformers; note 1

COMPONENT	VALUE
L6	2 × 5 turns
L7	2 turns

Note

1. Coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026.

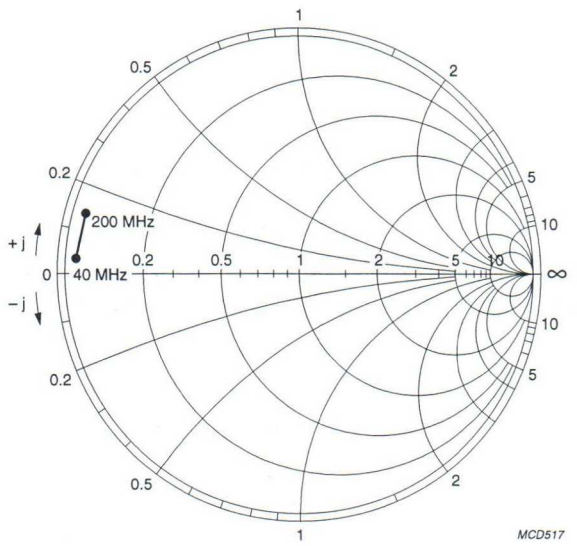


Fig.5 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

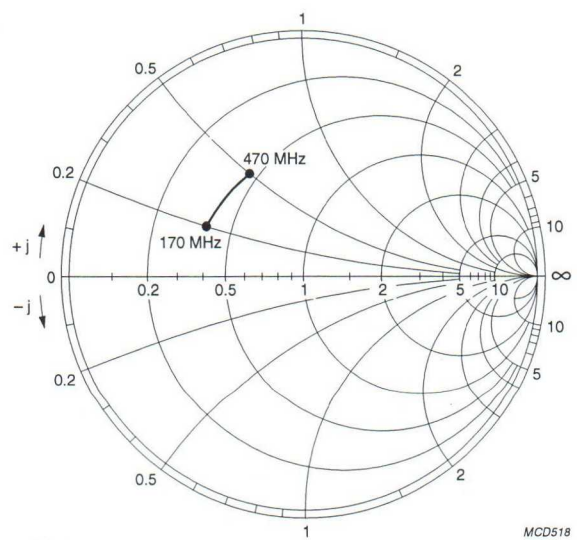


Fig.6 Input admittance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

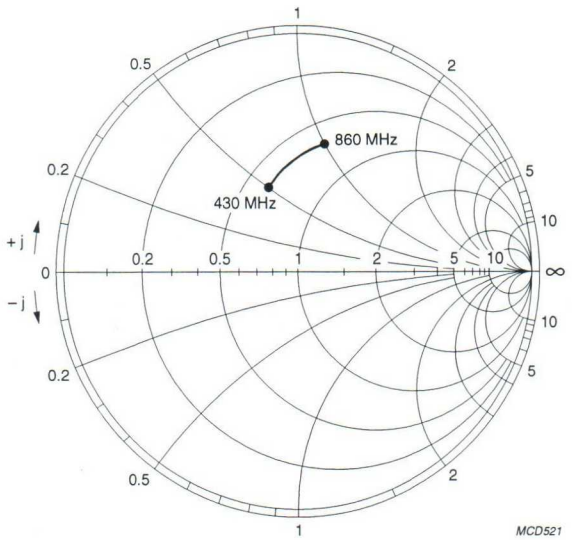


Fig.7 Input admittance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

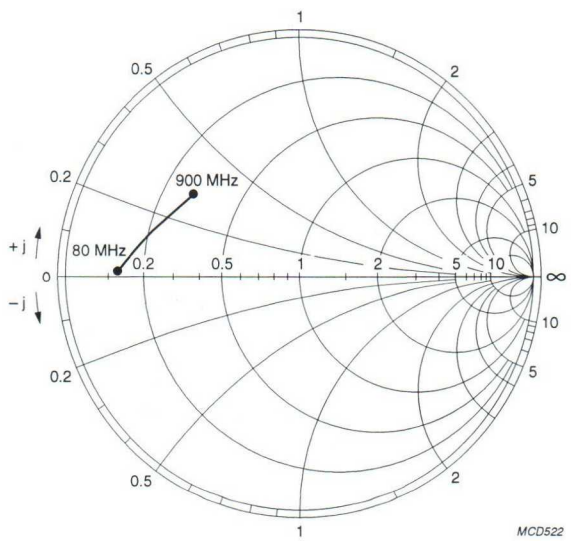


Fig.8 Output reflection coefficient (S_{22}) of the LO output (80 to 900 MHz) (Y chart).

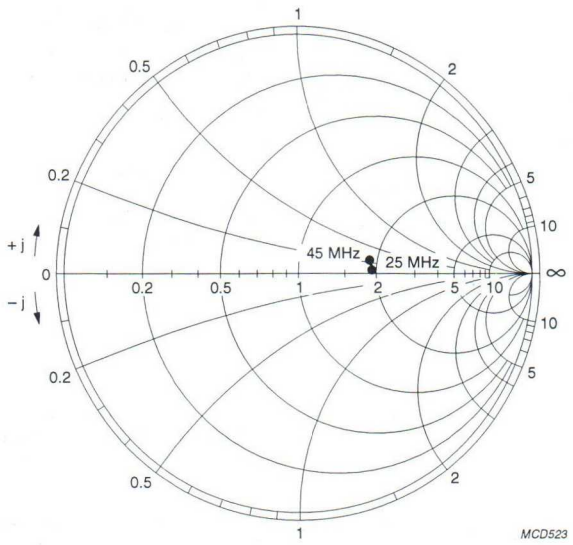


Fig.9 Output reflection coefficient (S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners

TDA5630BT

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- Balanced mixer with a common base input for bands C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

DESCRIPTION

The TDA5630BT is a monolithic integrated circuit that performs the bands A and C mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 2-band tuner.

The tuner development time can be drastically reduced by using this device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	48	–	mA
f_{RA}	frequency range; band A	RF input	45	–	470	MHz
f_{RC}	frequency range; band C	RF input	430	–	860	MHz
N_A	noise figure; band A		–	7.5	–	dB
N_C	noise figure; band C		–	9.0	–	dB
V_{IA}	input voltage; band A	1% cross-modulation	–	93	–	dBμV
V_{IC}	input voltage; band C	1% cross-modulation	–	84	–	dBμV
G_v	voltage gain	band A	–	25	–	dB
		band C	–	36	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5630BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

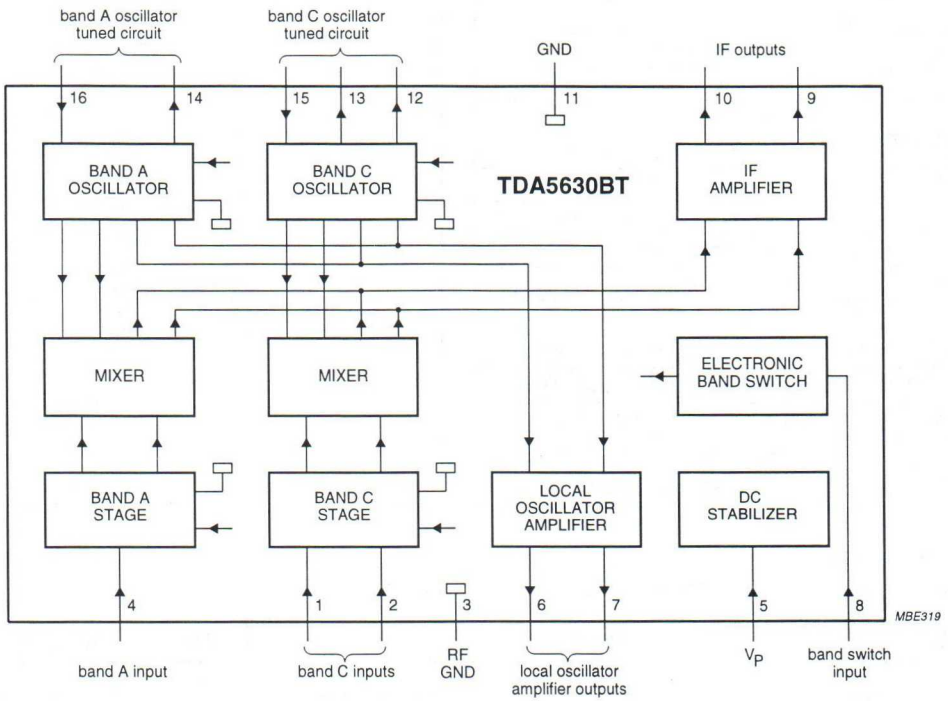


Fig.1 Block diagram.

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners

TDA5630BT

PINNING

SYMBOL	PIN	DESCRIPTION
CIN1	1	band C input 1
CIN2	2	band C input 2
RFGND	3	ground for RF inputs
AIN	4	band A input
V_P	5	supply voltage
LOOUT1	6	local oscillator amplifier output 1
LOOUT2	7	local oscillator amplifier output 2
BS	8	electronic band switch input
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
GND	11	ground (0 V)
COSCOC1	12	band C oscillator output collector 1
COSCOC2	13	band C oscillator output collector 2
AOSCOC	14	band A oscillator output collector
COSCIB	15	band C oscillator input base
AOSCIB	16	band A oscillator input base

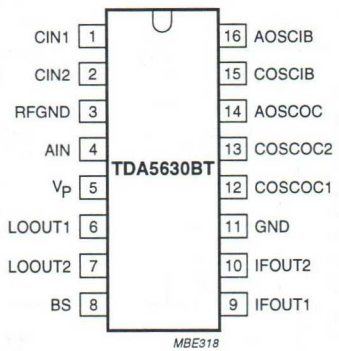


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	–0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	–10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–10	+70	°C
T_j	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	115	K/W

HANDLING

Human body model: the IC withstands 2250 V in accordance with *UZW-BO-FQ-A302* (stress reference pins 3, 11 and 5 shorted together).

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302* (stress reference pins 3, 11 and 5 shorted together).

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	see Fig.8	–	–10	9	–	dB/°
Z_o	output impedance (R_s + j$L_s\Omega$)	R_s	–	95		–	Ω
		L_s	–	45		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

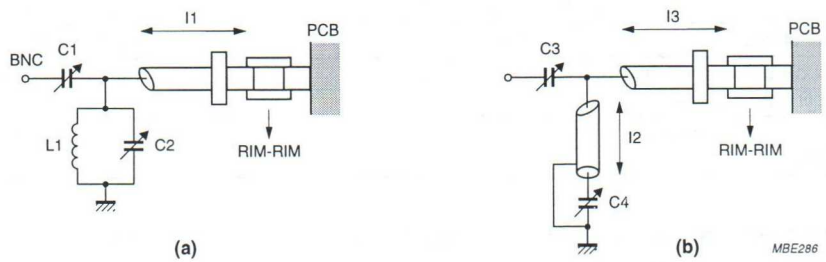
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9	9.9	V
I_P	supply current		35	48	55	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A	–	–	2	μA
		band C	–	–	10	μA
Band A mixer (including IF amplifier; pin 4)						
f_R	frequency range	V_t = 0.45 to 28 V	45	–	300	MHz
$f_{(max)}$	maximum frequency		–	470	–	MHz
N	noise figure	50 MHz; see Fig.3; note 1	–	7.5	9	dB
		180 MHz; see Fig.3; note 1	–	9	10	dB
		300 MHz; see Fig.3; note 1	–	10.5	11.5	dB
g_{os}	optimum source conductance for noise figure	50 MHz	–	0.5	–	mS
		180 MHz	–	1.1	–	mS
Y_I	input admittance (G_P//C_P)	50 MHz; see Fig.5	–	0.26	–	mS
		180 MHz; see Fig.5	–	0.35	–	mS
		50 to 180 MHz; see Fig.5	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel; f_i = 300 MHz; note 2	90	93	–	dBμV
		10 kHz pulling; in channel; f_i = 300 MHz	–	104	–	dBμV
G_v	voltage gain	20 log ($V_{10\text{-}9}/V_4$); 50 MHz	22.5	25	27.5	dB
		20 log ($V_{10\text{-}9}/V_4$); 300 MHz	22.5	25	27.5	dB
		20 log ($V_{10\text{-}9}/V_4$); 470 MHz	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band A oscillator						
f_R	frequency range		80	–	336	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 3	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 4	–	–	500	kHz
		5 s to 15 min after switch on; without compensation; note 5	–	500	950	kHz
		5 s to 15 min after switch on; with compensation; note 5	–	200	300	kHz
Band C mixer (including IF amplifier; measurements using hybrid; pins 1 and 2); notes 1 and 6						
f_R	frequency range	V_t = 0.45 to 28 V	430	–	860	MHz
N	noise figure (not corrected for image)	430 MHz	–	9	10	dB
		860 MHz	–	11	12	dB
Z_I	input impedance ($R_S + jL_S\Omega$)	R_S; 430 MHz; see Fig.6	–	40	–	Ω
		R_S; 860 MHz; see Fig.6	–	53	–	Ω
		L_S; 430 to 860 MHz; see Fig.6	–	9	–	nH
V_i	input voltage	1% cross-modulation; in channel; 430 MHz; note 2	80	84	–	dBμV
		1% cross-modulation; in channel; 860 MHz; note 2	80	84	–	dBμV
		10 kHz pulling; in channel; 860 MHz;	–	84	–	dBμV
		N + 5 – 1 MHz pulling; 820 MHz; note 6	–	63	–	dBμV
G_v	voltage gain	430 MHz; note 7	33	36	39	dB
		860 MHz; note 7	33	36	39	dB
Band C oscillator						
f_R	frequency range	V_t = 0.45 to 28 V	470	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 3	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 4	–	–	2.5	MHz
		5 s to 15 min after switching on; without compensation; note 5	–	1000	1300	kHz
		5 s to 15 min after switching on; with compensation; note 5	–	550	950	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LO output (pins 6 and 7)						
Y_o	output admittance (G_P//C_P)	80 MHz; see Fig.7	–	2.5	–	mS
		80 MHz; see Fig.7	–	0.9	–	pF
		900 MHz; see Fig.7	–	3.5	–	mS
		900 MHz; see Fig.7	–	0.7	–	pF
V_O	output voltage	R_L = 100 Ω	83	91	100	dBμV
SRF	spurious signal on LO output w.r.t. LO output signal	R_L = 100 Ω; note 8	–	–	–10	dB
SHD	LO signal harmonics w.r.t. LO signal	R_L = 100 Ω	–	–	–10	dB

Notes

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. To avoid pulling influence the local oscillators should be driven by a generator.
3. The frequency shift is defined for a variation of power supply, first from V_P = 9 to 8.1 V, then from V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
4. The frequency drift is defined for a variation of ambient temperature, first from T_{amb} = 25 °C to T_{amb} = 0 °C, then from T_{amb} = 25 °C to T_{amb} = 50 °C. In both cases, the frequency drift is below the specified value with NP0 capacitors. Capacitor types C1 to C11, as specified in Fig.4 for non-PLL applications, must be changed to series with other temperature coefficients (e.g. N330, N750 etc.)
5. Without compensation, all capacitors are NP0. With compensation C5 to C11 are N750 and C1, C2 and C4 are N470. All other capacitors are NP0.
6. The input level of a N + 5 – 1 MHz signal which gives a signal 30 dB below the oscillator carrier at the LO output.
7. The gain is defined as the transducer gain (measured in Fig.4) plus the voltage transformation ratio of L6 to L7 (6 : 1, 15.4 dB).
8. All S-parameters are referred to a 50 Ω system.



(a) For f_R = 50 MHz:

mixer A frequency response measured = 57 MHz, loss = 0 dB

image suppression = 16 dB

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)

l1 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

(b) For f_R = 180 MHz:

mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB

image suppression = 13 dB

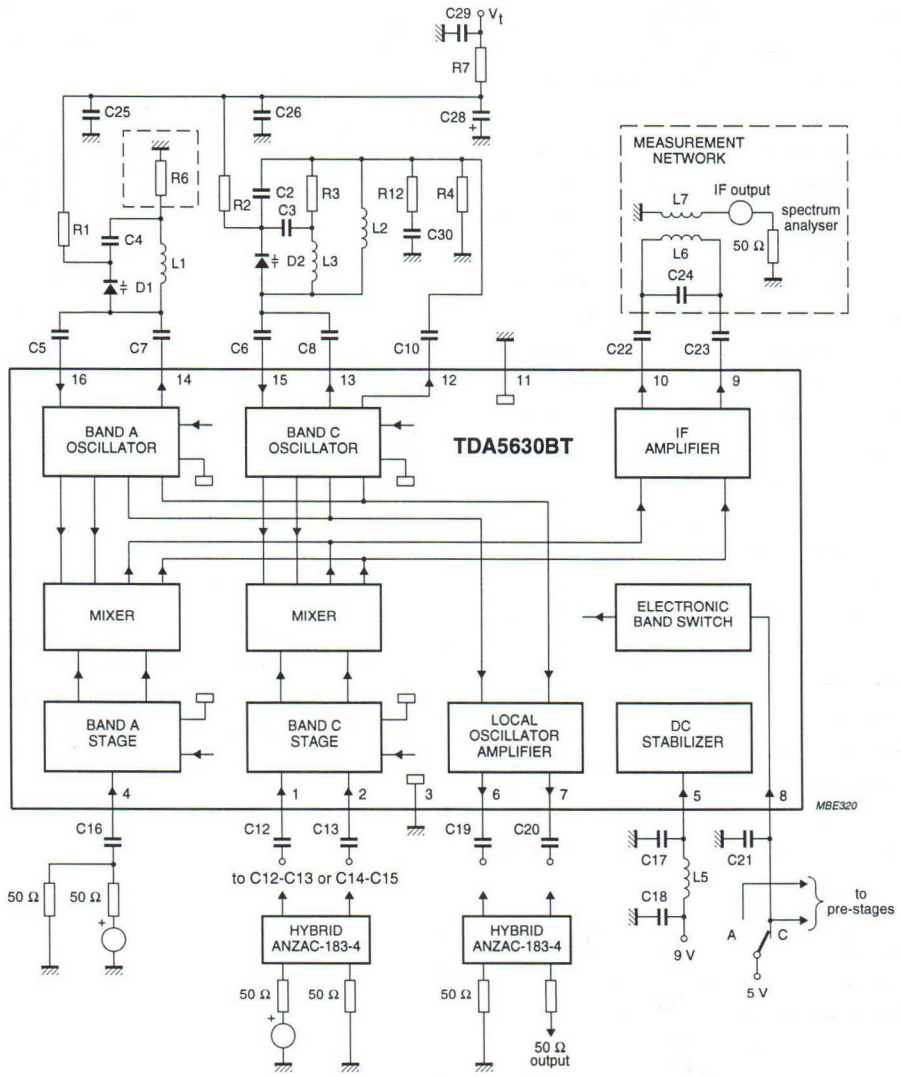
C3 = 5 pF

C4 = 25 pF

l2 = rigid cable (RIM): 30 cm long

l3 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.



L6, L7 and C24 are only required for measurement purposes; they are not used in a tuner.

Fig.4 Measurement circuit.

Component values for measurement circuit

Table 1 Capacitors (all SMD and NP0 except C28)

COMPONENT	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	150 pF
C5	2.2 pF
C6	1 pF
C7	2.2 pF
C8	1 pF
C9	1.8 pF
C10	2.2 pF
C11	3.9 pF
C12	1 nF
C13	1 nF
C16	1 nF
C17	1.5 nF
C18	1.5nF
C19	1 nF
C20	1 nF
C21	1.5 nF
C22	1 nF
C23	1 nF
C24	18 pF
C25	1.5 nF
C26	1.5 nF
C28	1 μF; 40 V electrolytic
C29	1.5 nF
C30	0.56 pF

Table 2 Resistors (all SMD)

COMPONENT	VALUE
R1	47 kΩ
R2	22 kΩ
R3	2.2 kΩ
R4	22 kΩ
R6	22 Ω
R7	1 kΩ
R12	470 Ω

Table 3 Diodes and IC

COMPONENT	VALUE
D1	BB911
D2	BB405/215
D3	BB909/219
IC	TDA5630BT

Table 4 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L1	7.5 turns; dia. 3 mm
L2	2.5 turns; dia. 3 mm
L3	1.5 turns; dia. 2.5 mm
L4	1.5 turns; dia. 4 mm
L5	4.7 μH; choke coil

Table 5 Transformers; note 1

COMPONENT	VALUE
L6	2 × 5 turns
L7	2 turns

Note

1. Coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026.

For a band A oscillator frequency range of 80 to 216 MHz, C1, C5, C7, D1 and L1 should be used.

For a band A oscillator frequency range of 180 to 506 MHz, C4, C9, C11, D3, R6 and L4 should be used.

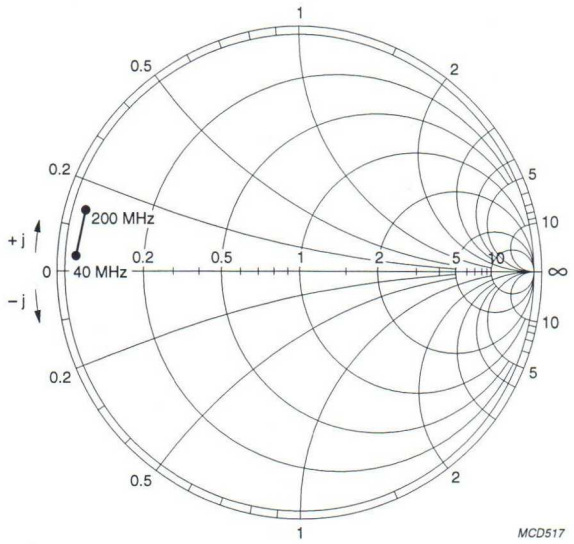


Fig.5 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

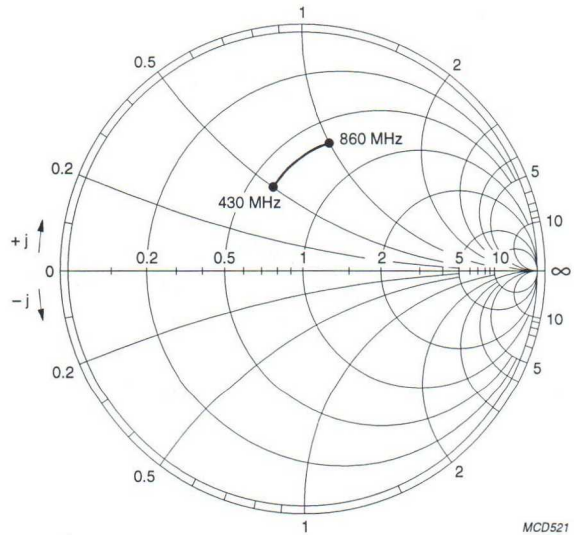


Fig.6 Input impedance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

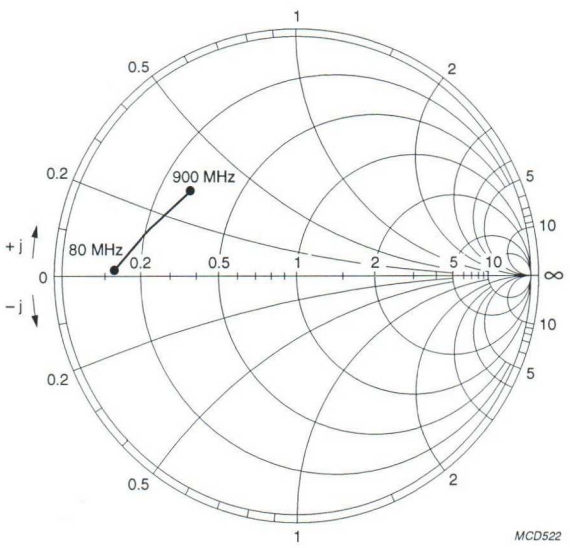


Fig.7 Output admittance (S_{11}) of the LO output (80 to 900 MHz) (Y chart).

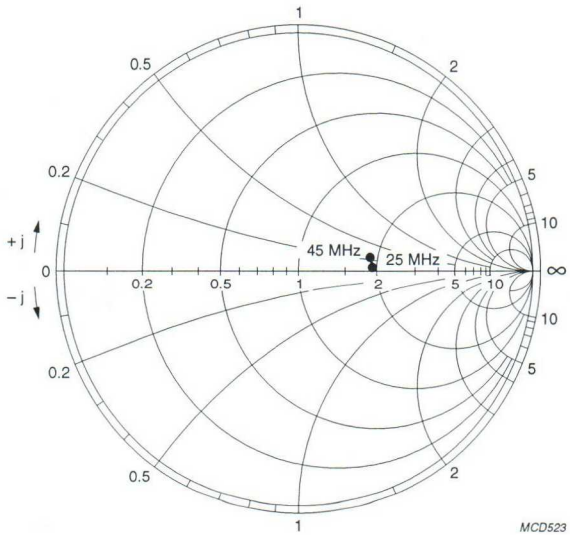


Fig.8 Output reflection coefficient (S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5630CT

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

DESCRIPTION

The TDA5630CT is a monolithic integrated circuit that performs the bands A, B and C mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 3-band tuner.

The tuner development time can be drastically reduced by using this device. In addition, when hyperband is not necessary, the TDA5630CT may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHF I and VHF III in band A, and the tuned circuit of band C for UHF.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	35	–	mA
f_{RA}	frequency range; band A	RF input	45	–	180	MHz
f_{RB}	frequency range; band B	RF input	160	–	470	MHz
f_{RC}	frequency range; band C	RF input	430	–	860	MHz
N_A	noise figure; band A		–	7.5	–	dB
N_B	noise figure; band B		–	8	–	dB
N_C	noise figure; band C		–	9	–	dB
V_{IA}	input voltage; band A	1% cross-modulation	–	93	–	dBμV
V_{IB}	input voltage; band B	1% cross-modulation	–	82	–	dBμV
V_{IC}	input voltage; band C	1% cross-modulation	–	82	–	dBμV
G_v	voltage gain	band A	–	25	–	dB
		band B	–	36	–	dB
		band C	–	36	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5630CT	SO20M	plastic small outline package; 20 leads; body width 7.5 mm	SOT336-1

BLOCK DIAGRAM

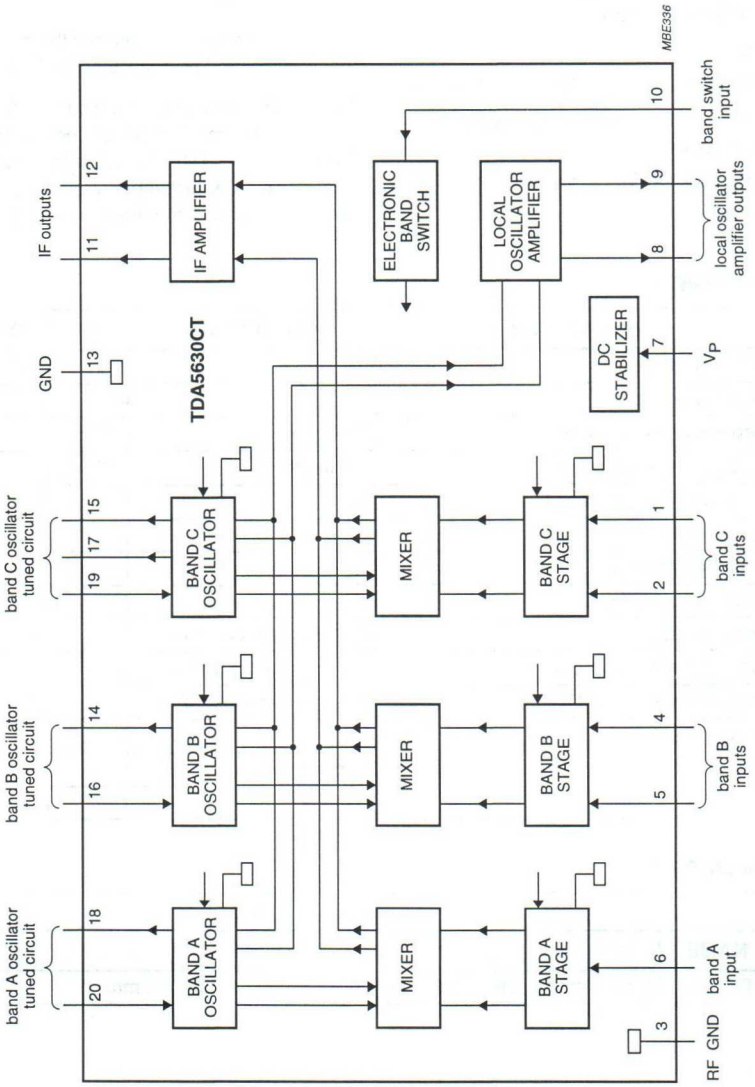


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CIN1	1	band C input 1
CIN2	2	band C input 2
RFGND	3	ground for RF inputs
BIN1	4	band B input 1
BIN2	5	band B input 2
AIN	6	band A input
V_P	7	supply voltage
LOOUT1	8	local oscillator amplifier output 1
LOOUT2	9	local oscillator amplifier output 2
BS	10	electronic band switch input
IFOUT1	11	IF amplifier output 1
IFOUT2	12	IF amplifier output 2
GND	13	ground (0 V)
BOSCOC	14	band B oscillator output collector
COSCOC1	15	band C oscillator output collector 1
BOSCIB	16	band B oscillator input base
COSCOC2	17	band C oscillator output collector 2
AOSCOC	18	band A oscillator output collector
COSCIB	19	band C oscillator input base
AOSCIB	20	band A oscillator input base

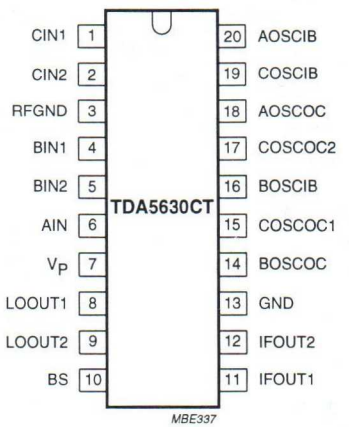


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	102	K/W

HANDLING

Human body model: the IC withstands 2250 V in accordance with *UZW-BO-FQ-A302* (stress reference pins 3, 7 and 13 shorted together).

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302* (stress reference pins 3, 7 and 13 shorted together).

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	see Fig.9	–	−10	9	–	dB/°
Z_o	output impedance ($R_s + jL_s\Omega$)	R_s	–	95		–	Ω
		L_s	–	45		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

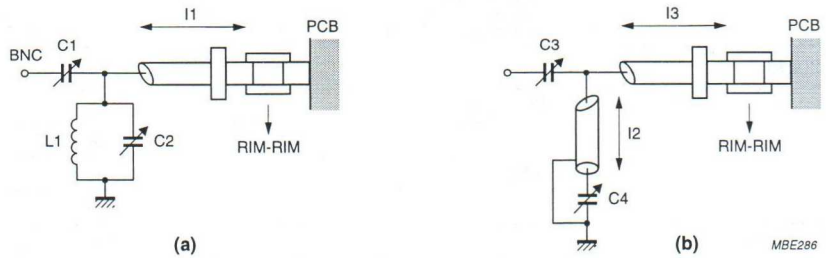
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current		–	35	45	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band B	1.6	–	2.4	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A	–	–	2	µA
		band B	–	–	5	µA
		band C	–	–	10	µA
Band A mixer (including IF amplifier; pin 6)						
f_R	frequency range		45	–	180	MHz
N	noise figure	50 MHz; see Fig.3	–	7.5	9	dB
		180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for noise figure	50 MHz	–	0.5	–	mS
		180 MHz	–	1.1	–	mS
g_i	input admittance (G_P//C_P)	50 MHz; see Fig.5	–	0.26	–	mS
		180 MHz; see Fig.5	–	0.35	–	mS
		50 to 180 MHz	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel f = 180 MHz	90	93	–	dBµV
		10 kHz pulling; in channel;180 MHz	–	100	–	dBµV
G_v	voltage gain	20 log ($V_{12\text{-}11}/V_6$); 50 MHz	22.5	25	27.5	dB
		20 log ($V_{12\text{-}11}/V_6$); 180 MHz	22.5	25	27.5	dB
Band A oscillator						
f_R	frequency range		80	–	216	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 2	–	–	500	kHz
		5 s to 15 min after switch on; note 2	–	–	200	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (pins 4 and 5; including IF amplifier) measurements using hybrid; see Fig.4; note 3						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	170 MHz	–	8	10	dB
		470 MHz	–	8	10	dB
Z_I	input impedance ($R_S + jL_S\Omega$)	R_S; see Fig.6	–	30	–	Ω
		L_S; see Fig.6		8		nH
V_i	input voltage	1% cross-modulation; in channel; 170 MHz	79	82	–	dBμV
		1% cross-modulation; in channel; 470 MHz	79	82	–	dBμV
		10 kHz pulling; in channel; 470 MHz	–	87	–	dBμV
		N + 5 – 1 MHz pulling; 430 MHz; note 4	–	81	–	dBμV
G_v	voltage gain	170 MHz; note 5	33	36	39	dB
		470 MHz; note 5	33	36	39	dB
Band B oscillator						
f_R	frequency range		200	–	500	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation: NP0 capacitors; note 2	–	–	2	MHz
		5 s to 15 min after switch on; note 2	–	–	300	kHz
Band C mixer (pins 1 and 2; including IF amplifier) measurements using hybrid; see Fig.4; note 3						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	430 MHz	–	9	11	dB
		860 MHz	–	9	11	dB
Z_I	input impedance ($R_S + jL_S\Omega$)	R_S; 430 MHz; see Fig.7	–	40	–	Ω
		R_S; 860 MHz; see Fig.7	–	53	–	Ω
		L_S; 430 to 860 MHz	–	9	–	nH
V_i	input voltage	1% cross-modulation; in channel; 430 MHz	79	82	–	dBμV
		1% cross-modulations channel; 860 MHz	79	82	–	dBμV
		10 kHz pulling; in channel; 860 MHz	–	90	–	dBμV
		N + 5 – 1 MHz pulling; 820 MHz; note 4	–	61	–	dBμV
G_v	voltage gain	430 MHz; note 5	33	36	39	dB
		860 MHz; note 5	33	36	39	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range		470	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 2	–	–	2.5	MHz
		5 s to 15 min after switching on; note 2	–	–	600	kHz
LO output (pins 8 and 9; R_L = 100 Ω)						
Y_O	output admittance (G_P//C_P)	80 MHz; see Fig.8		2.5		mS
				0.9		pF
		900 MHz; see Fig.8		3.5		mS
				0.7		pF
V_O	output voltage		83	91	100	dBμV
SRF	spurious signal on LO output w.r.t. LO output signal	note 6	–	–	–10	dB
SHD	LO signal harmonics w.r.t. LO signal		–	–	–10	dB

Notes

1. The frequency shift is defined for a variation of power supply, first from V_P = 9 to 8.1 V, then from V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
2. The frequency drift is defined for a variation of ambient temperature, first from T_{amb} = 25 °C to T_{amb} = 0 °C, then from T_{amb} = 25 °C to T_{amb} = 50 °C. In both cases, the frequency drift is below the specified value with NP0 capacitors. Capacitor types C1 to C11, as specified in Fig.4 for non-PLL applications, must be changed to series with other temperature coefficients (e.g. N330, N750 etc.).
3. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
4. The input level of a N + 5 – 1 MHz signal which gives a signal 30 dB below the oscillator carrier at the LO output.
5. The gain is defined as the transducer gain (measured in Fig.4) plus the voltage transformation ratio of L6 to L7 (6 : 1, 15.4 dB).
6. Measured at 50 Ω, with RF input voltage:
   a) RF voltage = 120 dBμV at f_i < 180 MHz
   b) RF voltage = 107.5 dBμV at f_i = 180 to 225 MHz
   c) RF voltage = 97 dBμV at f_i = 225 to 860 MHz.



(a) For f_R = 50 MHz:

mixer A frequency response measured = 57 MHz, loss = 0 dB

image suppression = 16 dB

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)

I1 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:

mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB

image suppression = 13 dB

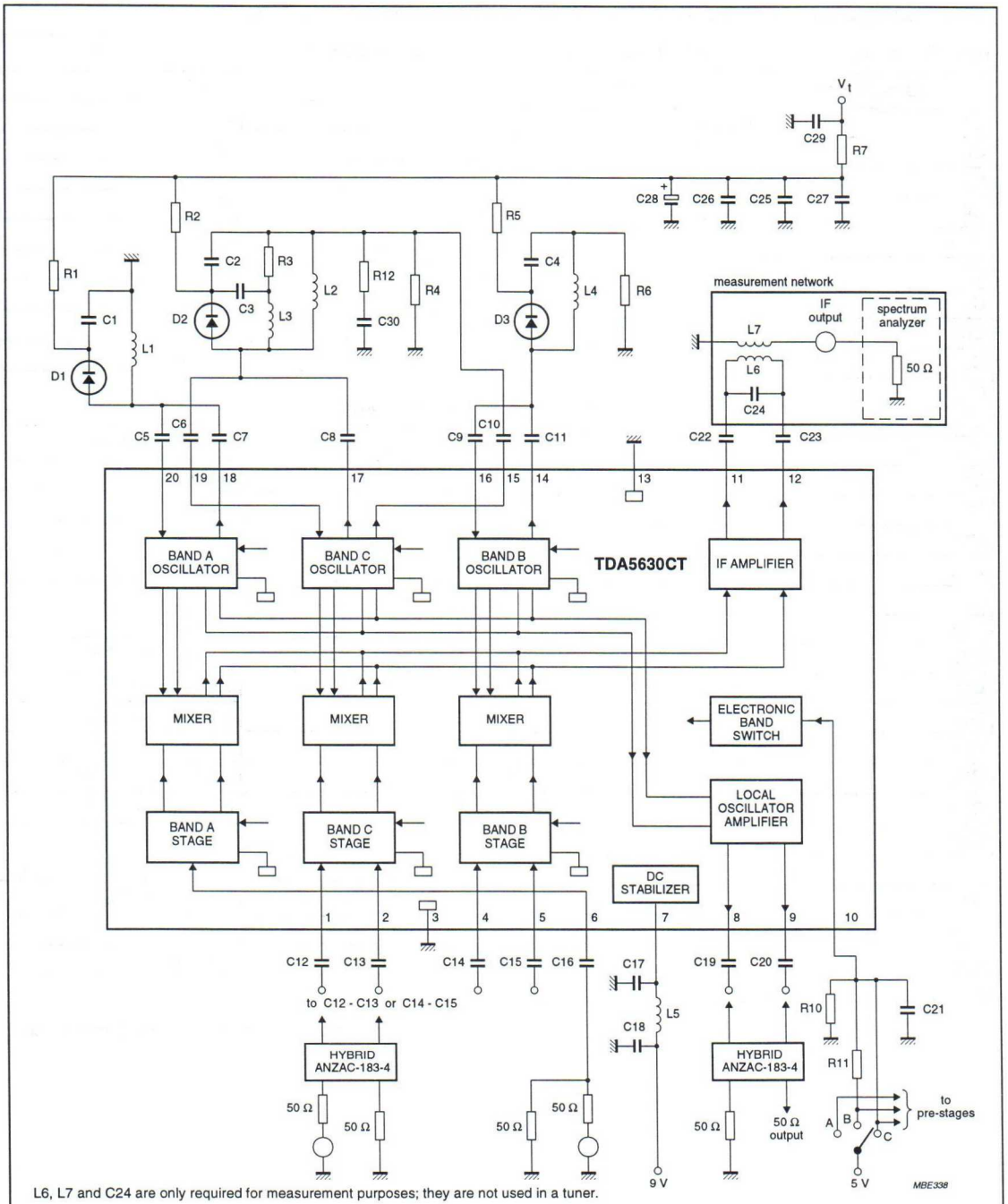
C3 = 5 pF

C4 = 25 pF

I2 = rigid cable (RIM): 30 cm long

I3 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.



L6, L7 and C24 are only required for measurement purposes; they are not used in a tuner.

Fig.4 Measurement circuit.

Component values for measurement circuit

Table 1 Capacitors (all SMD and NPO except C28)

COMPONENT	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	150 pF
C5	2.2 pF
C6	1 pF
C7	2.2 pF
C8	1 pF
C9	1.8 pF
C10	2.2 pF
C11	3.9 pF
C12	1 nF
C13	1 nF
C14	1 nF
C15	1 nF
C16	1 nF
C17	1.5 nF
C18	1.5nF
C19	1 nF
C20	1 nF
C21	1.5 nF
C22	1 nF
C23	1 nF
C24	18 pF
C25	1.5 nF
C26	1.5 nF
C27	1.5 nF
C28	1 μF; 40 V electrolytic
C29	1.5 nF
C30	0.56 pF

Table 2 Resistors (all SMD)

COMPONENT	VALUE
R1	47 kΩ
R2	22 kΩ
R3	2.2 kΩ
R4	22 kΩ
R5	47 kΩ
R6	22 Ω
R7	1 kΩ
R10	15 kΩ
R11	22 kΩ
R12	470 Ω

Table 3 Diodes and IC

COMPONENT	VALUE
D1	BB911
D2	BB405/215
D3	BB909/219
IC	TDA5630CT

Table 4 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L1	7.5 turns; dia. 3 mm
L2	2.5 turns; dia. 3 mm
L3	1.5 turns; dia. 2.5 mm
L4	1.5 turns; dia. 4 mm
L5	4.7 μH; choke coil

Table 5 Transformers; note 1

COMPONENT	VALUE
L6	2 × 5 turns
L7	2 turns

Note

1. Coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026.

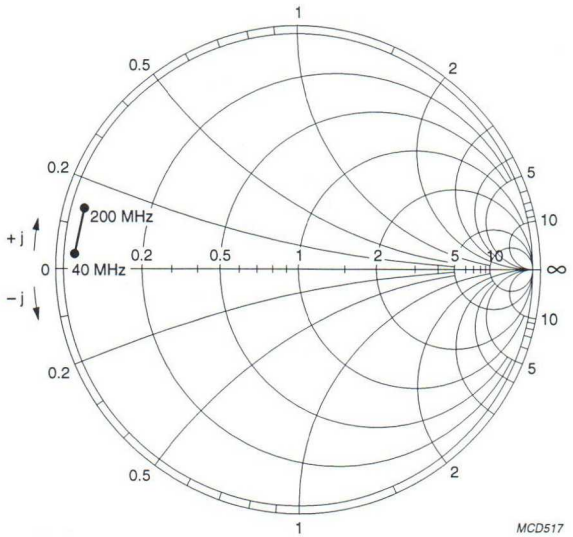


Fig.5 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

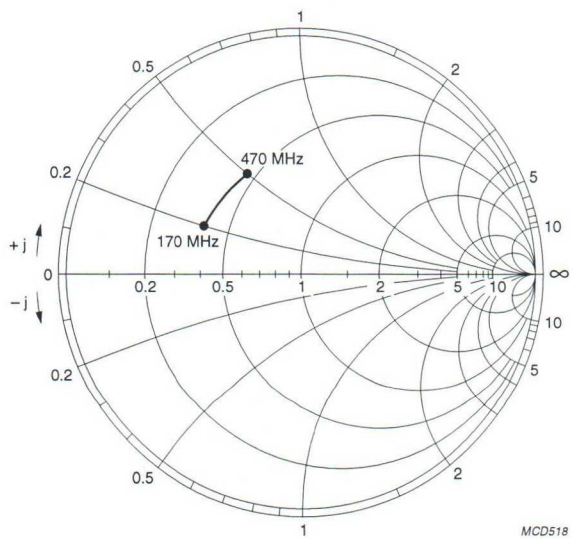


Fig.6 Input impedance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

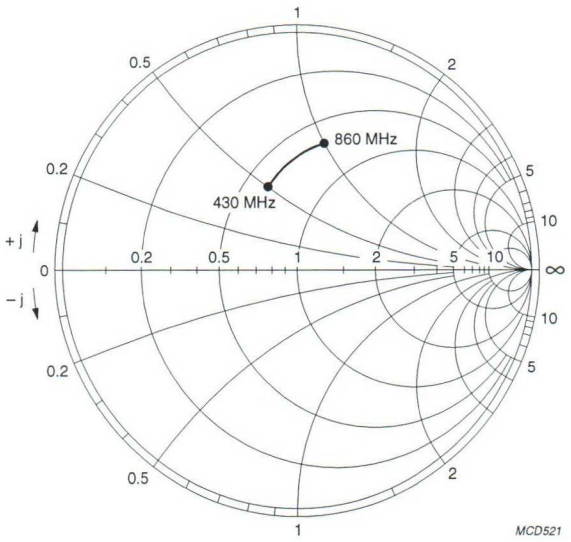


Fig.7 Input impedance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

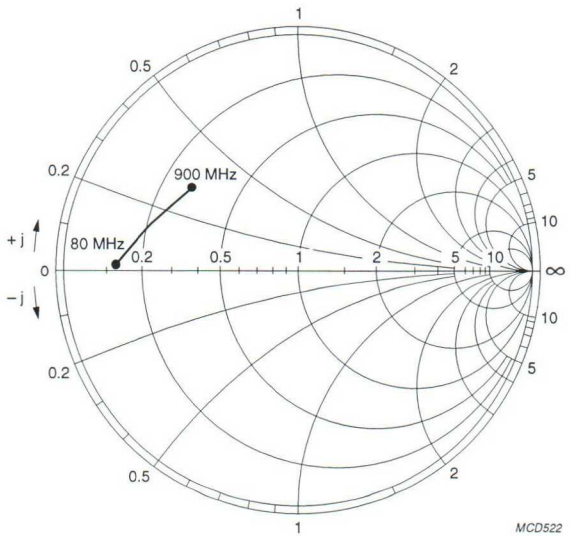


Fig.8 Output admittance (S_{11}) of the LO output (80 to 900 MHz) (Y chart).

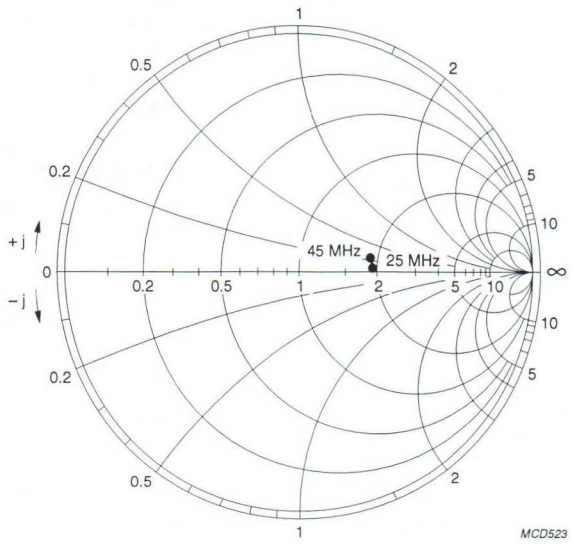


Fig.9 Output reflection coefficient (S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5631

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance of 75 Ω in the application
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch.

DESCRIPTION

The TDA5631 is a monolithic integrated circuit that performs the bands A, B and C mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 3-band tuner.

The tuner development time can be drastically reduced by using this device. In addition, when hyperband is not necessary, the TDA5631 may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHF I and VHF III in band A, and the tuned circuit of band C for UHF.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	35	–	mA
f_R	frequency range	band A	45	–	180	MHz
		band B	160	–	470	MHz
		band C	430	–	860	MHz
N	noise figure	band A	–	7.5	–	dB
		band B	–	8	–	dB
		band C	–	9	–	dB
V_i	input voltage	band A; 1% cross-modulation	–	93	–	dBμV
P_i	input power	band B; 1% cross-modulation; note 1	–	–25	–	dBm
		band C; 1% cross-modulation; note 1	–	–25	–	dBm
G_v	voltage gain	band A	–	25	–	dB
		band B	–	36	–	dB
		band C	–	36	–	dB

Note

1. The input power is defined as the power delivered by the generator into a 50 Ω load.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5631T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5631M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

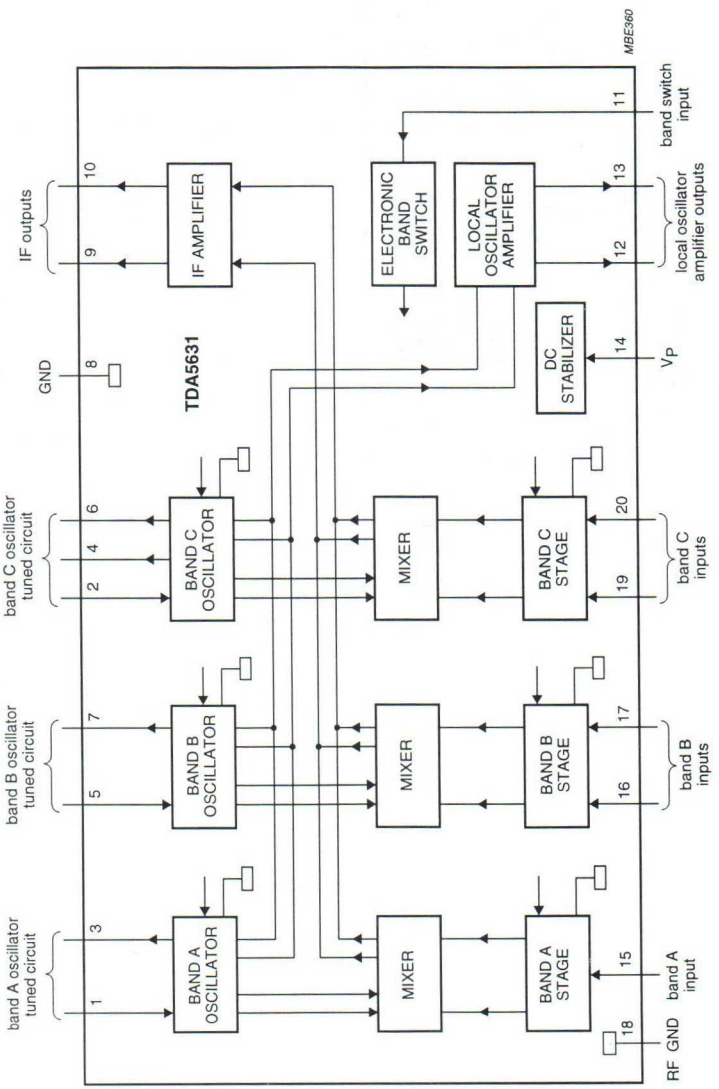


Fig.1 Block diagram.

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5631

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
COSCIB	2	band C oscillator input base
AOSCOC	3	band A oscillator output collector
COSCOC1	4	band C oscillator output collector 1
BOSCIB	5	band B oscillator input base
COSCOC2	6	band C oscillator output collector 2
BOSCOC	7	band B oscillator output collector
GND	8	ground (0 V)
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
BS	11	electronic band switch input
LOOUT1	12	local oscillator amplifier output 1
LOOUT2	13	local oscillator amplifier output 2
V_P	14	supply voltage
AIN	15	band A input
BIN1	16	band B input 1
BIN2	17	band B input 2
RFGND	18	ground for RF inputs
CIN1	19	band C input 1
CIN2	20	band C input 2

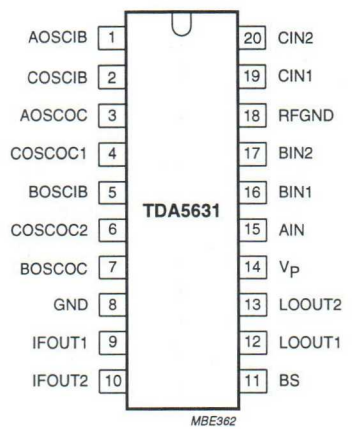


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	IC storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT163-1	100	K/W
	SOT266-1	120	K/W

HANDLING

Human body model: the IC withstands 2500 V in accordance with *UZW-BO-FQ-A302* (pins 18, 8 and 14 shorted together).

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302* (pins 18, 8 and 14 shorted together).

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	see Fig.9	–	−10	9	–	dB/°
Z_o	output impedance ($R_s + jL_s\Omega$)	R_s	–	95		–	Ω
		L_s	–	45		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

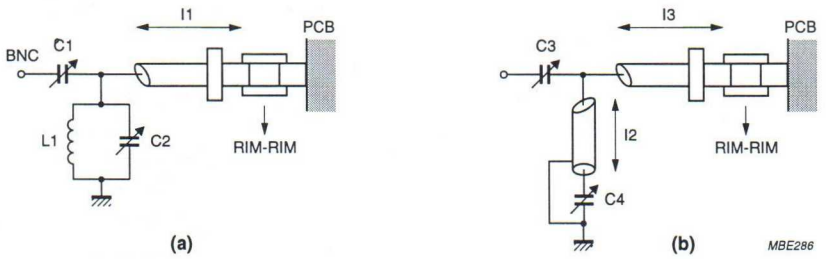
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9	9.9	V
I_P	supply current		–	35	45	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band B	1.6	–	2.4	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A	–	–	2	μA
		band B	–	–	5	μA
		band C	–	–	10	μA
Band A mixer (including IF amplifier)						
f_R	frequency range		45	–	180	MHz
N	noise figure	f_i = 50 MHz; see Fig.3	–	7.5	9	dB
		f_i = 180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for noise figure	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1.1	–	mS
Y_i	input admittance	see Fig.5	–	–	–	
C_I	input capacitance	f_i = 50 to 180 MHz	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel f_i = 180 MHz	90	93	–	dBμV
		10 kHz pulling; in channel f_i = 180 MHz	–	100	–	dBμV
G_v	voltage gain	20 log ($V_{10\text{-}9}/V_{15}$); f_i = 50 MHz	22.5	25	27.5	dB
		20 log ($V_{10\text{-}9}/V_{15}$); f_i = 180 MHz	22.5	25	27.5	dB
Band A oscillator						
f_R	frequency range		80	–	216	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 2	–	–	500	kHz
		5 s to 15 min after switch on	–	–	200	kHz
Band B mixer (including IF amplifier) pins 16 and 17; measurements using hybrid; note 3						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz	–	8	10	dB
		f_i = 470 MHz	–	8	10	dB
Z_I	input impedance	see Fig.6	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power	1% cross-modulation; in channel; f_i = 170 MHz; note 4	−28	−25	–	dBm
		1% cross-modulation; in channel; f_i = 470 MHz; note 4	−28	−25	–	dBm
		TDA5631T; 10 kHz pulling; in channel; f_i = 470 MHz; note 4	–	−16	–	dBm
		TDA5631M; 10 kHz pulling; in channel; f_i = 470 MHz; note 4	–	−24	–	dBm
		TDA5631T; N + 5 − 1 MHz pulling; f_i = 430 MHz; note 4	–	−26	–	dBm
		TDA5631M; N + 5 − 1 MHz pulling; f_i = 430 MHz; note 4	–	−41	–	dBm
G_v	voltage gain	f_i = 170 MHz; note 6	33	36	39	dB
		f_i = 470 MHz; note 6	33	36	39	dB
Band B oscillator						
f_R	frequency range		200	–	500	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation: NP0 capacitors; note 2	–	–	2	MHz
		5 s to 15 min after switch on	–	–	300	kHz
Band C mixer (including IF amplifier) pins 19 and 20; measurements using hybrid; note 3						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz	–	9	11	dB
		f_i = 860 MHz	–	9	11	dB
Z_I	input impedance	see Fig.7	–	–	–	
P_i	input power	1% cross-modulation; in channel; f_i = 430 MHz; note 4	−28	−25	–	dBm
		1% cross-modulation; in channel; f_i = 860 MHz; note 4	−28	−25	–	dBm
		TDA5631T; 10 kHz pulling; in channel; f_i = 860 MHz; note 4	–	−20	–	dBm
		TDA5631M; 10 kHz pulling; in channel; f_i = 860 MHz; note 4	–	−14	–	dBm
		N + 5 − 1 MHz pulling; 820 MHz; notes 4 and 5	–	−46	–	dB
G_v	voltage gain	f_i = 430 MHz; note 6	33	36	39	dB
		f_i = 860 MHz; note 6	33	36	39	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range		470	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 1	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors; note 2	–	–	2.5	MHz
		5 s to 15 min after switching on	–	–	600	kHz
LO output (pins 12 and 13; R_L = 100 Ω)						
S_{22}	output reflection coefficient	see Fig.8				
V_O	output voltage		14	35	100	mV
SRF	spurious signal on LO output w.r.t. LO output signal	note 7	–	–	–10	dB
SHD	LO signal harmonics w.r.t. LO signal		–	–	–10	dB

Notes

1. The frequency shift is defined for a variation of power supply, first from V_P = 9 to 8.1 V, then from V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
2. The frequency drift is defined for a variation of ambient temperature, first from T_{amb} = 25 °C to T_{amb} = 0 °C, then from T_{amb} = 25 °C to T_{amb} = 50 °C. In both cases, the frequency drift is below the specified value with NP0 capacitors. Capacitor types C1 to C11, as specified in Fig.4 for non-PLL applications, must be changed to series with other temperature coefficients (e.g. N330, N750 etc.).
3. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
4. The input power is defined as the power delivered by the generator into a 50 Ω load.
5. The input level of a N + 5 – 1 MHz signal (just visible).
6. The gain is defined as the transducer gain (measured in Fig.4) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
7. Measured at 50 Ω, with RF input voltage:
   a) RF voltage = 1 V at f_i < 180 MHz
   b) RF power = 0.5 dBm at f_i = 180 to 225 MHz
   c) RF power = –10 dBm at f_i = 225 to 860 MHz.



(a) For f_R = 50 MHz:

mixer A frequency response measured = 57 MHz, loss = 0 dB

image suppression = 16 dB

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)

l1 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:

mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB

image suppression = 13 dB

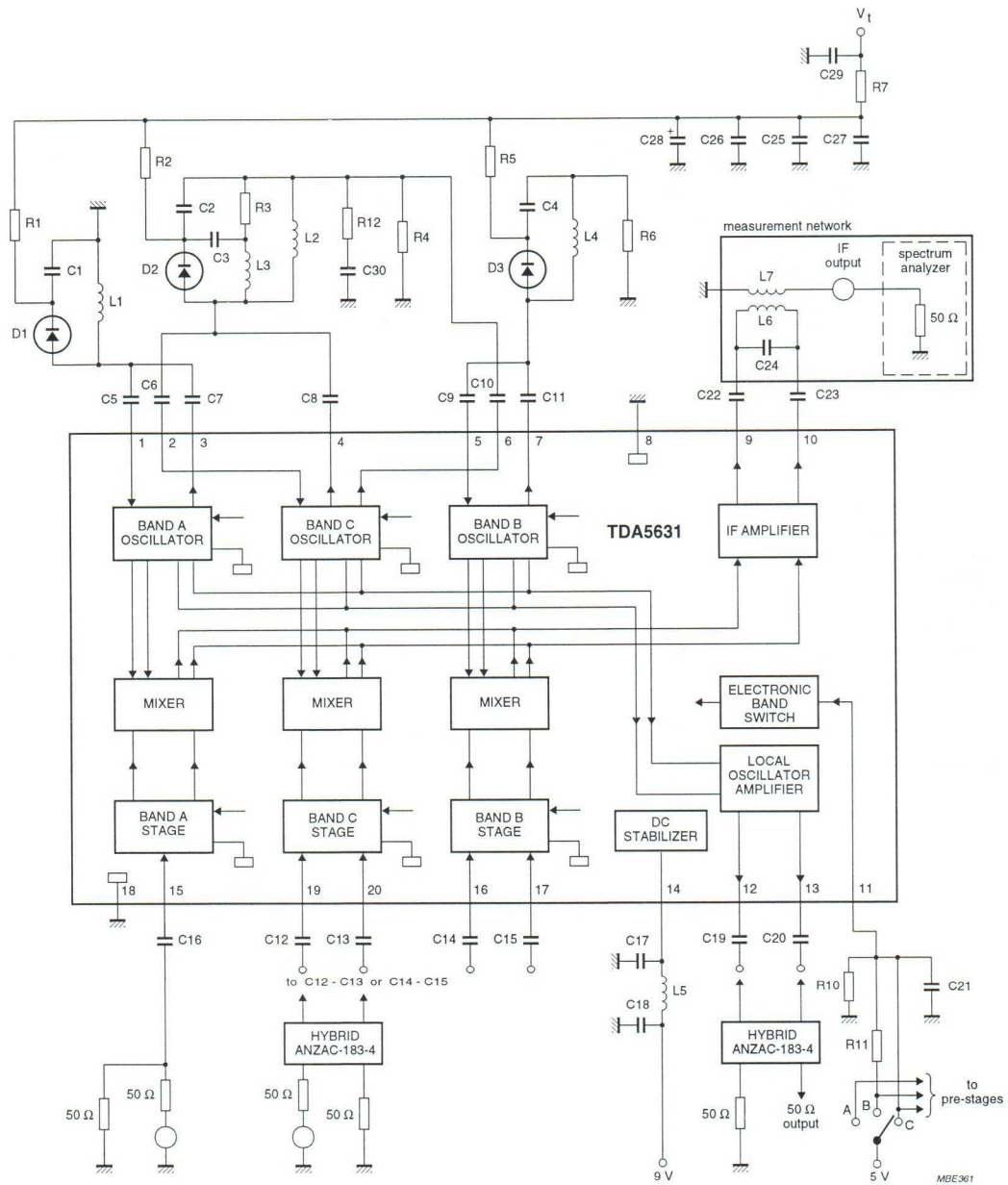
C3 = 5 pF

C4 = 25 pF

l2 = rigid cable (RIM): 30 cm long

l3 = rigid cable (RIM): 5 cm long (rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.



L6, L7 and C24 are only required for measurement purposes; they are not used in a tuner.

Fig.4 Measurement circuit.

Component values for measurement circuit

Table 1 Capacitors (all SMD and NP0 except C28)

COMPONENT	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	150 pF
C5	2.2 pF
C6	1 pF
C7	2.2 pF
C8	1 pF
C9	1.8 pF
C10	2.2 pF
C11	3.9 pF
C12	1 nF
C13	1 nF
C14	1 nF
C15	1 nF
C16	1 nF
C17	1.5 nF
C18	1.5nF
C19	1 nF
C20	1 nF
C21	1.5 nF
C22	1 nF
C23	1 nF
C24	18 pF
C25	1.5 nF
C26	1.5 nF
C27	1.5 nF
C28	1 µF; 40 V electrolytic
C29	1.5 nF
C30	0.56 pF

Table 2 Resistors (all SMD)

COMPONENT	VALUE
R1	47 kΩ
R2	22 kΩ
R3	2.2 kΩ
R4	22 kΩ
R5	47 kΩ
R6	22 Ω
R7	1 kΩ
R10	15 kΩ
R11	22 kΩ
R12	470 Ω

Table 3 Diodes and IC

COMPONENT	VALUE
D1	BB911
D2	BB405/215
D3	BB909/219
IC	TDA5631T/TDA5631M

Table 4 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L1	7.5 turns; dia. 3 mm
L2	2.5 turns; dia. 3 mm
L3	1.5 turns; dia. 2.5 mm
L4	1.5 turns; dia. 4 mm
L5	4.7 µH; choke coil

Table 5 Transformers; note 1

COMPONENT	VALUE
L6	2 × 5 turns
L7	2 turns

Note

1. Coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026.

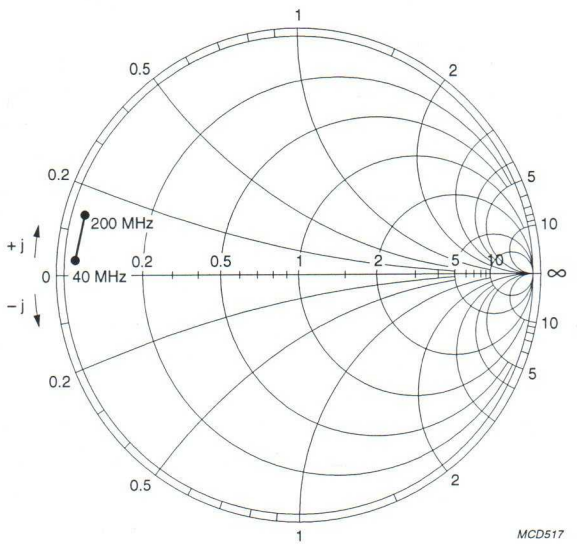


Fig.5 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

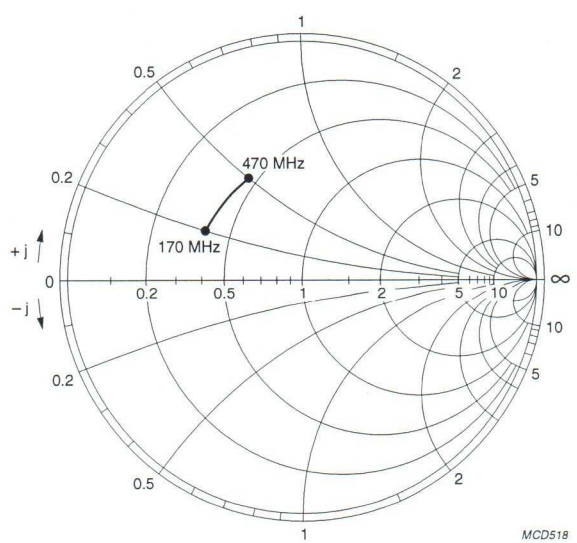


Fig.6 Input impedance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

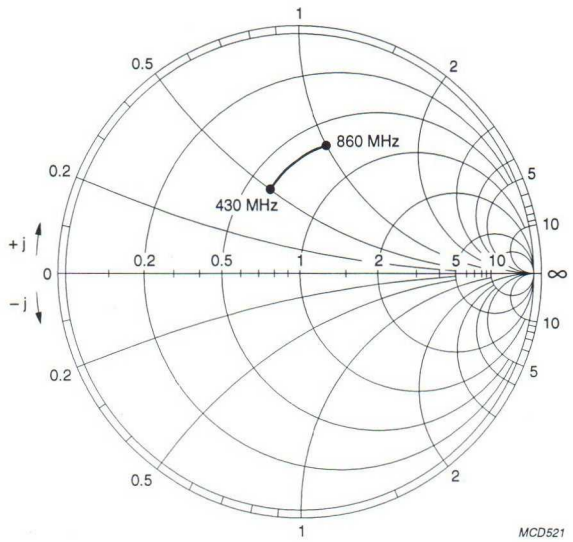


Fig.7 Input impedance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

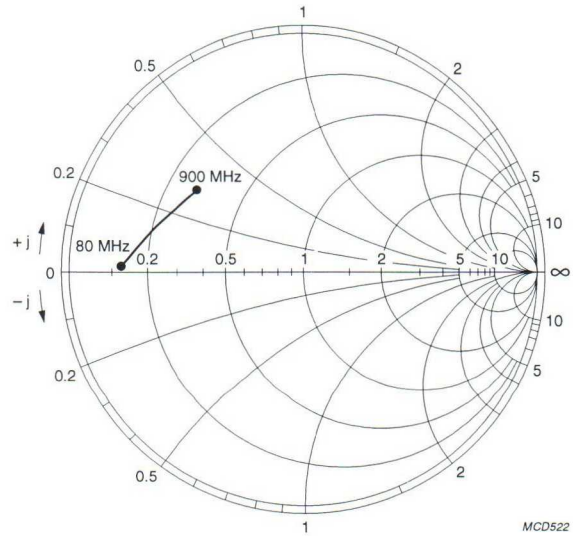


Fig.8 Output admittance (S_{22}) of the LO output (80 to 900 MHz) (Y chart).

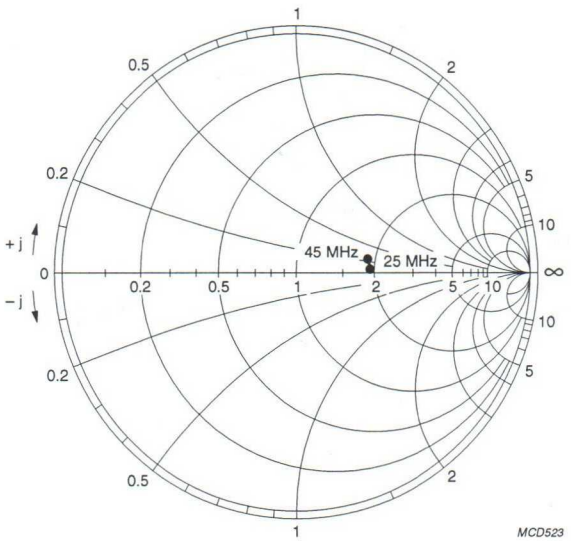


Fig.9 Output impedance (S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

Low-power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners

TDA5632

FEATURES

- Balanced mixer with a common emitter input for band A
- 2-pin oscillator for band A
- Balanced mixer with a common base input for band C
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance of 75 Ω in the application
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter connected between the mixer output and the IF amplifier input.

DESCRIPTION

The TDA5632 is a monolithic integrated circuit that performs VHF I, VHF III, hyperband and UHF mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 2-band tuner.

The tuner development time can be drastically reduced by using this device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	40	–	mA
f_R	frequency range	band A; note 1	57.5	–	357.5	MHz
		band C; note 1	469.5	–	887.5	MHz
N	noise figure	band A; R_L = 75 Ω	–	10	–	dB
		band C; R_L = 75 Ω	–	9.5	–	dB
V_i	input voltage	band A; R_L = 75 Ω; 1% cross-modulation	–	91	–	dBμV
		band C; R_L = 75 Ω; 1% cross-modulation	–	80	–	dBμV
G_v	voltage gain	band A; R_L = 75 Ω	–	19	–	dB
		band C; R_L = 75 Ω	–	30	–	dB

Note

1. A second UHF frequency range is available by modifying the tank circuit. The modification enables the following frequency range:
   a) RF frequencies from 363.5 to 803.5 MHz.
   b) Oscillator frequencies from 407 to 847 MHz. For this UHF range, L4 = 3 turns (dia. = 3.5 mm).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5632T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5632M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

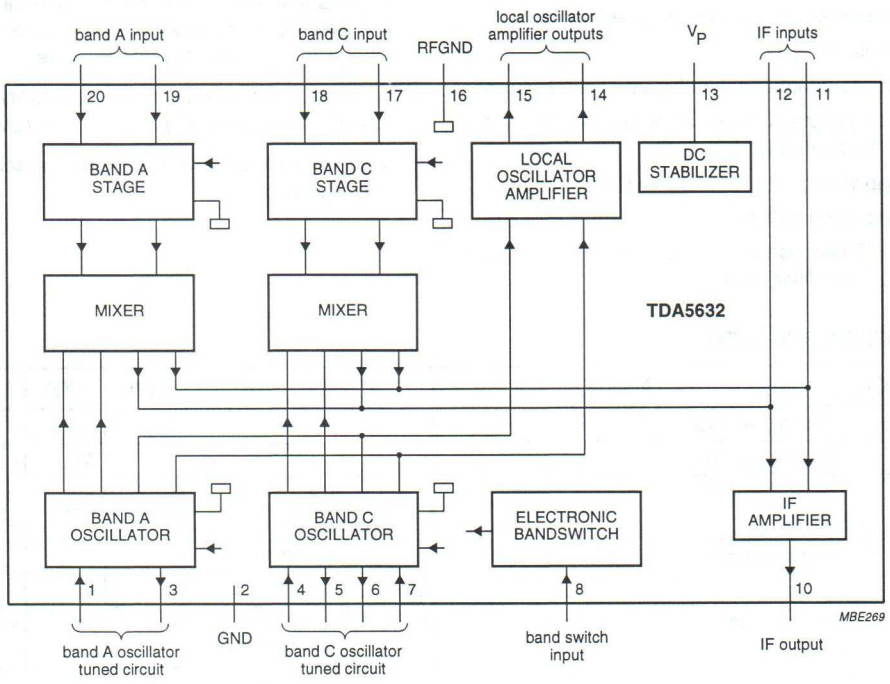


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
GND	2	ground (0 V)
AOSCOC	3	band A oscillator output collector
COSCIB1	4	band C oscillator input base 1
COSCOC1	5	band C oscillator output collector 1
COSCOC2	6	band C oscillator output collector 2
COSCIB2	7	band C oscillator input base 2
BS	8	electronic band switch
n.c.	9	not connected
IFOUT	10	IF amplifier output
IFIN1	11	IF amplifier input 1
IFIN2	12	IF amplifier input 2
V_P	13	supply voltage
LOOUT1	14	local oscillator amplifier output 1
LOOUT2	15	local oscillator amplifier output 2
RFGND	16	ground for RF inputs
CIN1	17	band C input 1
CIN2	18	band C input 2
AIN1	19	band A input 1
AIN2	20	band A input 2

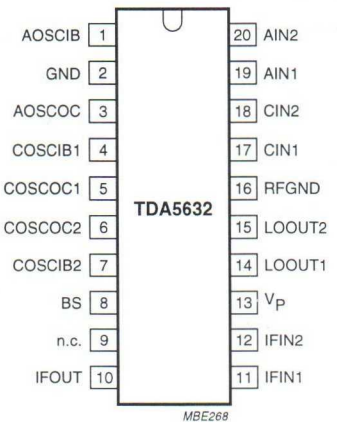


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−20	+85	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT163-1	82	K/W
	SOT266-1	120	K/W

HANDLING

Human body model: the IC withstands 2000 V in accordance with *UZW-BO-FQ-A302*; R = 1.5 kΩ; C = 100 pF.

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302*; R = 0 Ω; C = 200 pF.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 43.5 MHz; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient		–	−14	−1.9	–	dB/°
Z_o	output impedance (R_s + L_s)	R_s; through 1 nF	–	75		–	Ω
		L_s; through 1 nF	–	2.8		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current		–	40	48	mA
V_{SW}	switching voltage	band A	0	–	2.0	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A	–	–	2	µA
		band C	–	–	10	µA
Band A mixer (including IF amplifier)						
f_R	frequency range		57.5	–	357.5	MHz
N	noise figure	f_i = 50 MHz; R_L = 75 Ω	–	7.5	9.5	dB
		f_i = 150 MHz; R_L = 75 Ω	–	8.5	10.5	dB
		f_i = 300 MHz; R_L = 75 Ω	–	10	12.5	dB
g_{os}	optimum source conductance for noise figure	f_i = 50 MHz; R_L = 75 Ω	–	0.5	–	mS
		f_i = 150 MHz; R_L = 75 Ω	–	1.1	–	mS
		f_i = 300 MHz; R_L = 75 Ω	–	1.9	–	mS
g_i	input conductance	f_i = 57.5 MHz	–	0.27	–	mS
		f_i = 357.5 MHz	–	0.68	–	mS
C_I	input capacitance	f_i = 57.5 to 357.5 MHz; R_L = 75 Ω	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel; f_i = 57.5 MHz; R_L = 75 Ω; note 1	88	91	–	dBµV
		1% cross modulation; in channel; f_i = 357.5 MHz; R_L = 75 Ω; note 1	88	91	–	dBµV
		10 kHz pulling; in channel; R_L = 75 Ω; f_i = 357.5 MHz	–	91	–	dBµV
G_v	voltage gain	f_i = 57.5 MHz; R_L = 75 Ω	16.5	19	21.5	dB
		f_i = 357.5 MHz; R_L = 75 Ω	16.5	19	21.5	dB
Band A oscillator						
f_R	frequency range		101	–	401	MHz
f_{shift}	frequency shift	ΔV_P = 10%	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NP0 capacitors	–	–	1200	kHz
		5 s to 15 min after switch on	–	–	400	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C mixer (including IF amplifier)						
f_R	frequency range	note 2	469.5	–	887.5	MHz
N	noise figure (not corrected for image)	f_i = 469.50 MHz; R_L = 75 Ω	–	7.5	9.5	dB
		f_i = 887.5 MHz; R_L = 75 Ω	–	9.5	11.5	dB
Z_I	input impedance (R_s + L_s)	R_s; f_i = 469.50 MHz	–	30	–	Ω
		L_s; f_i = 887.5 MHz	–	12	–	nH
$V_{i(av)}$	available input voltage	1% cross-modulation; in channel; f_i = 887.5 MHz; R_L = 75 Ω; note 1	77	80	–	dBμV
V_i	input voltage	10 kHz pulling; in channel; R_L = 75 Ω	–	82	–	dBμV
G_v	voltage gain	f_i = 469.50 MHz; R_L = 75 Ω	27	30	33	dB
		f_i = 887.5 MHz; R_L = 75 Ω	27	30	33	dB
Band C oscillator						
f_R	frequency range		513	–	931	MHz
f_{shift}	frequency shift	ΔV_P = 10%	–	–	500	kHz
f_{drift}	frequency drift	ΔT = 25 °C with compensation	–	–	900	kHz
		5 s to 15 min after switching on	–	–	400	kHz
LO output						
V_O	output voltage	R_L = 50 Ω	83	91	100	dBμV
SRF	spurious signal on LO output w.r.t. LO output signal	R_L = 50 Ω; note 3	–	–14	–10	dB
HLO	LO signal harmonics w.r.t. LO signal	R_L = 50 Ω	–	–11	–10	dB

Notes

1. Cross-modulation measurements:
   a) Input voltage for mixer A at f_{RF} = 57.5 MHz; wanted at 55.25 MHz (80 dBμV); unwanted at 59.75 MHz, 30%, AM modulated with 100 kHz.
   b) Input voltage for mixer A at f_{RF} = 357.5 MHz; wanted at 355.25 MHz (80 dBμV); unwanted at 359.75 MHz, 30%, AM modulated with 100 kHz.
   c) Input voltage for mixer A at f_{RF} = 887.5 MHz; wanted at 885.25 MHz (69 dBμV); unwanted at 889.75 MHz, 30%, AM modulated with 50 kHz.
2. A second UHF frequency range is available by modifying the tank circuit. The modification enables the following frequency range:
   a) RF frequencies from 363.5 to 803.5 MHz.
   b) Oscillator frequencies from 407 to 847 MHz. For this UHF range, L4 = 3 turns (dia. = 3.5 mm).
3. SRF: spurious signal on LO with respect to LO output signal;
   a) RF voltage level = 1 V at f_i = 57.5 to 225 MHz.
   b) RF level = 2.5 dBm at f_i = 225 to 357.5 MHz.
   c) RF level = –10 dBm at f_i = 469.5 to 887.5 MHz.

APPLICATION INFORMATION

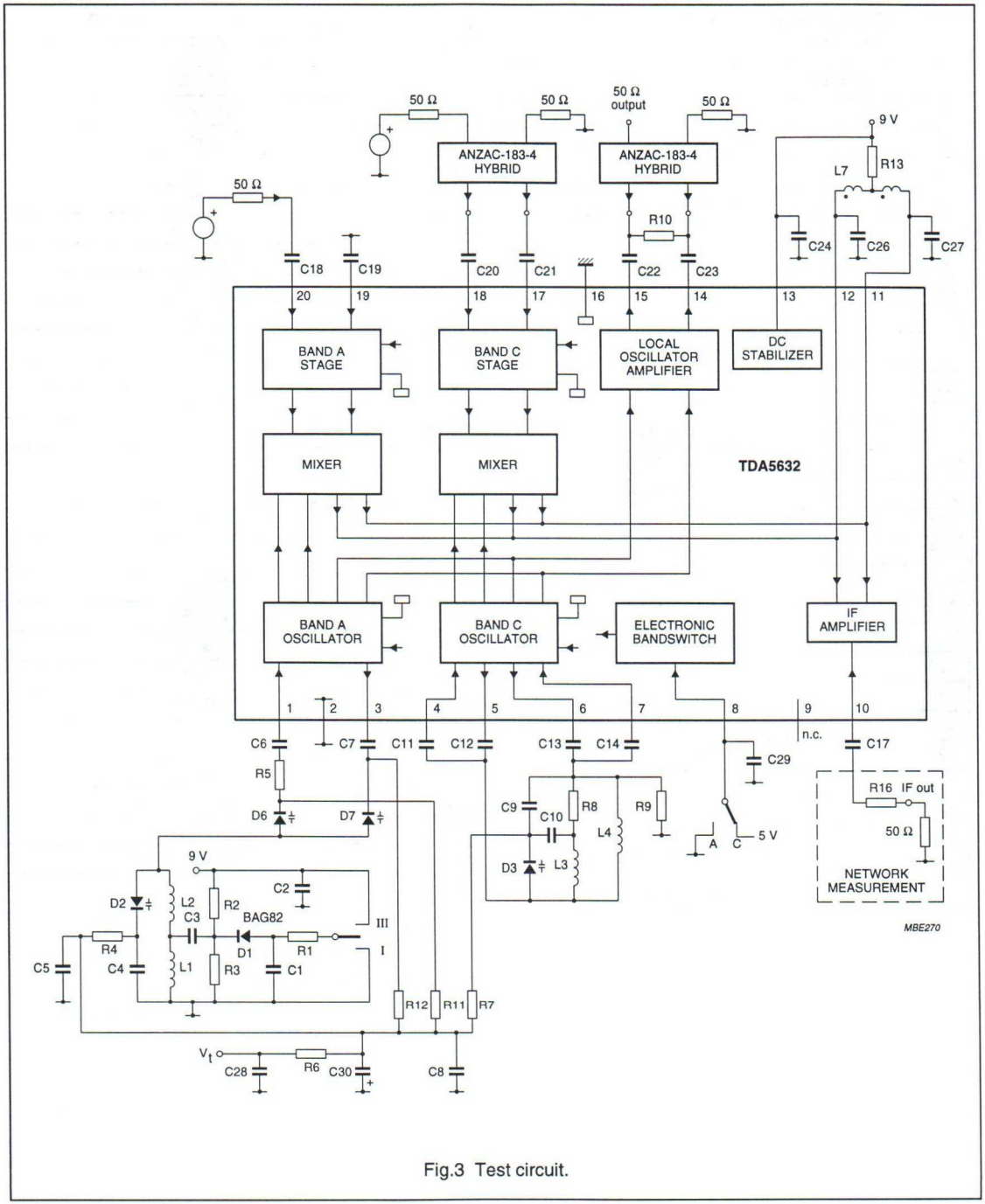


Fig.3 Test circuit.

Application diagram components values

Table 1 Capacitors (all SMD and NP0 except C9, C11 to C14 and C30)

NUMBER	VALUE
C1	1 nF
C2	1 nF
C3	1 nF
C4	56 pF
C5	2.2 nF
C6	2 pF
C7	4 pF
C8	2.2 nF
C9	6 pF (N470)
C10	100 pF
C11	1 pF (N750)
C12	1 pF (N750)
C13	1 pF (N750)
C14	1 pF (N750)
C17	1 nF
C18	1 nF
C19	1 nF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C26	15 pF
C27	15 pF
C28	2.2 nF
C29	1 nF
C30	1 μF (40 V electrolytic capacitor)

Table 2 Resistors (all SMD)

NUMBER	VALUE
R1	10 Ω
R2	12 kΩ
R3	2.7 kΩ
R4	47 kΩ
R5	56 Ω
R6	47 kΩ
R7	22 kΩ
R8	2.2 kΩ
R9	22 kΩ
R10	100 Ω
R11	47 kΩ
R12	47 kΩ
R13	150 Ω
R16	27 Ω

Table 3 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BA682
D2	BB133
D3	BB134
D6	BB131
D7	BB131
Coils[1]	
L1	6 t (4 mm)
L2	3 t (3.5 mm)
L3	2 t (2.5 mm)
L4	3 t (2.5 mm)

Note

1. Wire size for L1 to L4 is 0.4 mm.

Transformer (L7 = 2 × 5 t)

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

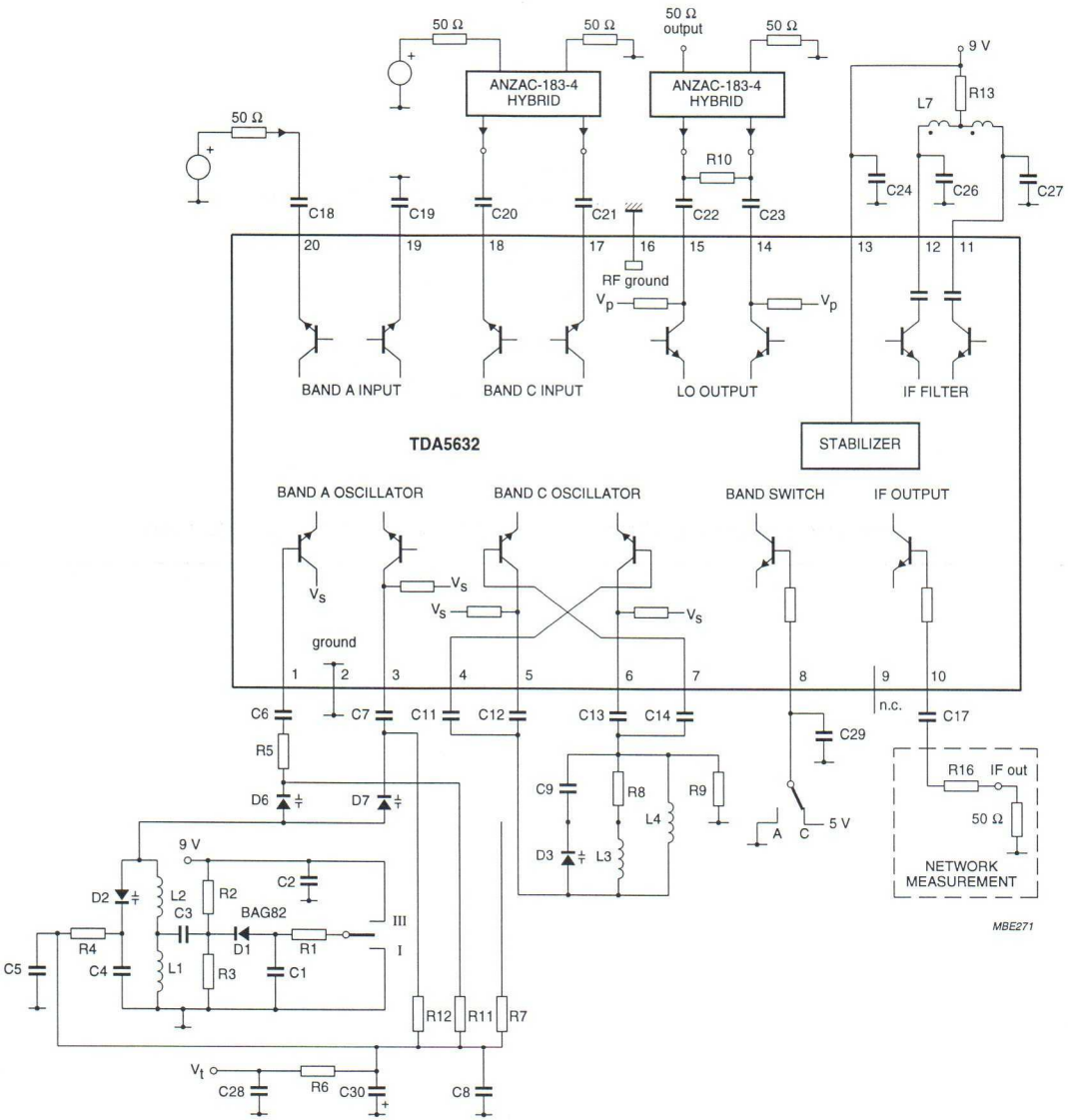


Fig.4 Electrical test circuit.

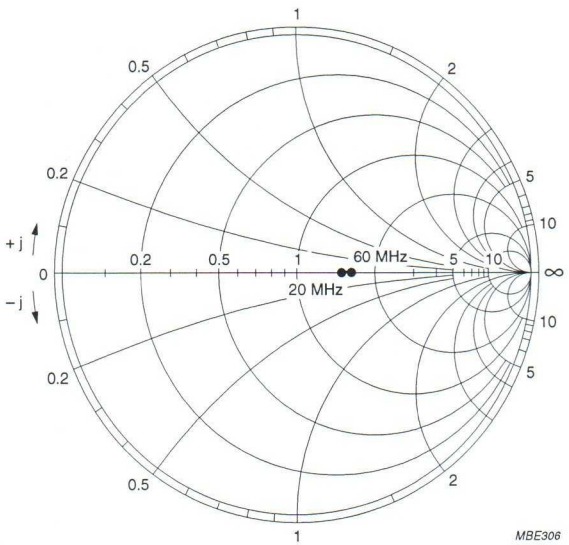


Fig.5 Output reflection coefficient (S_{22}) of the IF amplifier (20 to 60 MHz) (Z chart).

Low-power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners

TDA5633

FEATURES

- Balanced mixer with a common emitter input for band A
- 2-pin oscillator for band A
- Balanced mixer with a common base input for band C
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance of 75 Ω in the application
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter connected between the mixer output and the IF amplifier input.

DESCRIPTION

The TDA5633 is a monolithic integrated circuit that performs VHF I, VHF III, hyperband and UHF mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 2-band tuner.

The tuner development time can be drastically reduced by using this device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	40	–	mA
f_R	frequency range	band A; note 1	57.5	–	357.5	MHz
		band C; note 1	469.5	–	887.5	MHz
N	noise figure	band A; R_L = 75 Ω	–	10	–	dB
		band C; R_L = 75 Ω	–	9.5	–	dB
V_i	input voltage	band A; R_L = 75 Ω; 1% cross-modulation	–	91	–	dBμV
		band C; R_L = 75 Ω; 1% cross-modulation;	–	80	–	dBμV
G_v	voltage gain	band A; R_L = 75 Ω	–	19	–	dB
		band C; R_L = 75 Ω	–	30	–	dB

Note

1. A second UHF frequency range is available by modifying the tank circuit. The modification enables the following frequency range:
   a) RF frequencies from 363.5 to 803.5 MHz.
   b) Oscillator frequencies from 407 to 847 MHz. For this UHF range, L4 = 3 turns (dia. = 3.5 mm).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5633T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA5633M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

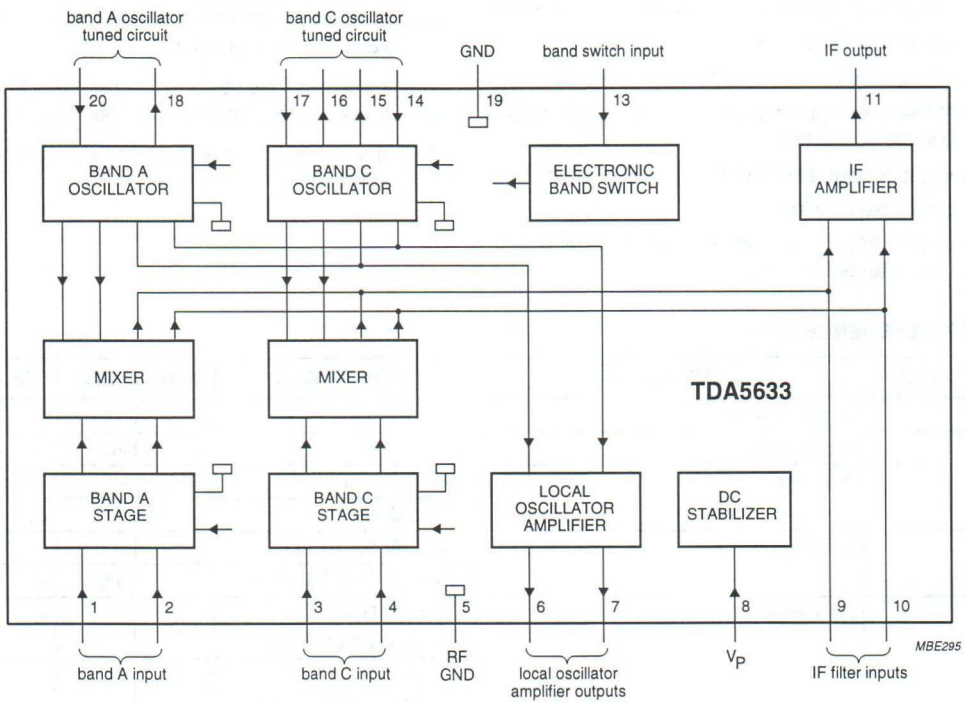


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AIN1	1	band A input 1
AIN2	2	band A input 2
CIN1	3	band C input 1
CIN2	4	band C input 2
RFGND	5	ground for RF inputs
LOOUT1	6	local oscillator amplifier output 1
LOOUT2	7	local oscillator amplifier output 2
V_P	8	supply voltage
IFIN1	9	IF amplifier input 1
IFIN2	10	IF amplifier input 2
IFOUT	11	IF amplifier output
n.c.	12	not connected
BS	13	electronic band switch input
COSCIB1	14	band C oscillator input base 1
COSCOC1	15	band C oscillator output collector 1
COSCOC2	16	band C oscillator output collector 2
COSCIB2	17	band C oscillator input base 2
AOSCOC	18	band A oscillator output collector
GND	19	ground (0 V)
AOSCIB	20	band A oscillator input base

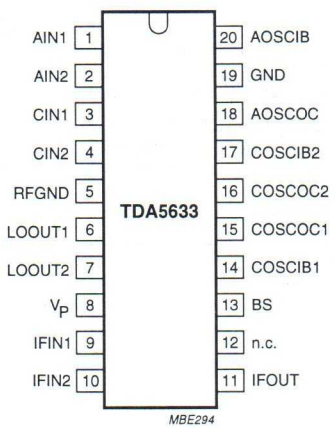


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−20	+85	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT163-1	82	K/W
	SOT266-1	120	K/W

HANDLING

Human body model: the IC withstands 2000 V in accordance with *UZW-BO-FQ-A302*; R = 1.5 kΩ; C = 100 pF.

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302*; R = 0 Ω; C = 200 pF.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 43.5 MHz; measured in circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient		–	−14	−1.9	–	dB/°
Z_o	output impedance (R_s + L_s)	R_s; through 1 nF	–	75		–	Ω
		L_s; through 1 nF	–	2.8		–	nF

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current		–	40	48	mA
V_{SW}	switching voltage	band A	0	–	2.0	V
		band C	3.0	–	5.0	V
I_{SW}	switching current	band A; V_{SW} = 0 V	–	–	2	µA
		band C; V_{SW} = 5 V	–	–	10	µA
Band A mixer (including IF amplifier)						
f_R	frequency range		57.5	–	357.5	MHz
N	noise figure	f_i = 50 MHz; R_L = 75 Ω	–	7.5	9.5	dB
		f_i = 150 MHz; R_L = 75 Ω	–	8.5	10.5	dB
		f_i = 300 MHz; R_L = 75 Ω	–	10	12.5	dB
g_{os}	optimum source conductance for noise figure	f_i = 50 MHz; R_L = 75 Ω	–	0.5	–	mS
		f_i = 150 MHz; R_L = 75 Ω	–	1.1	–	mS
		f_i = 300 MHz; R_L = 75 Ω	–	1.9	–	mS
g_i	input conductance	f_i = 57.5 MHz	–	0.27	–	mS
		f_i = 357.5 MHz	–	0.68	–	mS
C_I	input capacitance	f_i = 57.5 to 357.5 MHz; R_L = 75 Ω	–	2	–	pF
V_i	input voltage	1% cross modulation; in channel; f_i = 57.5 MHz; R_L = 75 Ω; note 1	88	91	–	dBµV
		1% cross modulation; in channel; f_i = 357.5 MHz; R_L = 75 Ω; note 1	88	91	–	dBµV
		10 kHz pulling; in channel; R_L = 75 Ω; f_i = 357.5 MHz	–	91	–	dBµV
G_v	voltage gain	f_i = 57.5 MHz; R_L = 75 Ω	16.5	19	21.5	dB
		f_i = 357.5 MHz; R_L = 75 Ω	16.5	19	21.5	dB
Band A oscillator						
f_R	frequency range		101	–	401	MHz
f_{shift}	frequency shift	ΔV_P = 10%	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C with no compensation; NPO capacitors	–	–	1200	kHz
		5 s to 15 min after switch on	–	–	400	kHz
Band C mixer (including IF amplifier)						
f_R	frequency range	note 2	469.5	–	887.5	MHz
N	noise figure (not corrected for image)	f_i = 469.50 MHz; R_L = 75 Ω	–	7.5	9.5	dB
		f_i = 887.5 MHz; R_L = 75 Ω	–	9.5	11.5	dB
Z_I	input impedance (R_s + L_s)	R_s; f_i = 469.50 MHz	–	30	–	Ω
		L_s; f_i = 887.5 MHz	–	12	–	nH

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(av)}$	available input voltage	1% cross-modulation; in channel; f_i = 887.5 MHz; R_L = 75 Ω; note 1	77	80	–	dBμV
V_i	input voltage	10 kHz pulling; in channel; R_L = 75 Ω	–	82	–	dBμV
G_v	voltage gain	f_i = 469.50 MHz; R_L = 75 Ω	27	30	33	dB
		f_i = 887.5 MHz; R_L = 75 Ω	27	30	33	dB
Band C oscillator						
f_R	frequency range		513	–	931	MHz
f_{shift}	frequency shift	ΔV_P = 10%	–	–	500	kHz
f_{drift}	frequency drift	ΔT = 25 °C with compensation	–	–	900	kHz
		5 s to 15 min after switching on	–	–	400	kHz
LO output						
V_O	output voltage	R_L = 50 Ω	83	91	100	dBμV
SRF	spurious signal on LO output w.r.t. LO output signal	R_L = 50 Ω; note 3	–	−14	−10	dB
HLO	LO signal harmonics w.r.t. LO signal	R_L = 50 Ω	–	−11	−10	dB

Notes

1. Cross-modulation measurements:
   a) Input voltage for mixer A at f_{RF} = 57.5 MHz; wanted at 55.25 MHz (80 dBμV); unwanted at 59.75 MHz, 30%, AM modulated with 100 kHz.
   b) Input voltage for mixer A at f_{RF} = 357.5 MHz; wanted at 355.25 MHz (80 dBμV); unwanted at 359.75 MHz, 30%, AM modulated with 100 kHz.
   c) Input voltage for mixer A at f_{RF} = 887.5 MHz; wanted at 885.25 MHz (69 dBμV); unwanted at 889.75 MHz, 30%, AM modulated with 50 kHz.
2. A second UHF frequency range is available by modifying the tank circuit. The modification enables the following frequency range:
   a) RF frequencies from 363.5 to 803.5 MHz.
   b) Oscillator frequencies from 407 to 847 MHz. For this UHF range, L4 = 3 turns (dia. = 3.5 mm).
3. SRF: spurious signal on LO with respect to LO output signal;
   a) RF voltage level = 1 V at f_i = 57.5 to 225 MHz.
   b) RF level = 2.5 dBm at f_i = 225 to 357.5 MHz.
   c) RF level = −10 dBm at f_i = 469.5 to 887.5 MHz.

APPLICATION INFORMATION

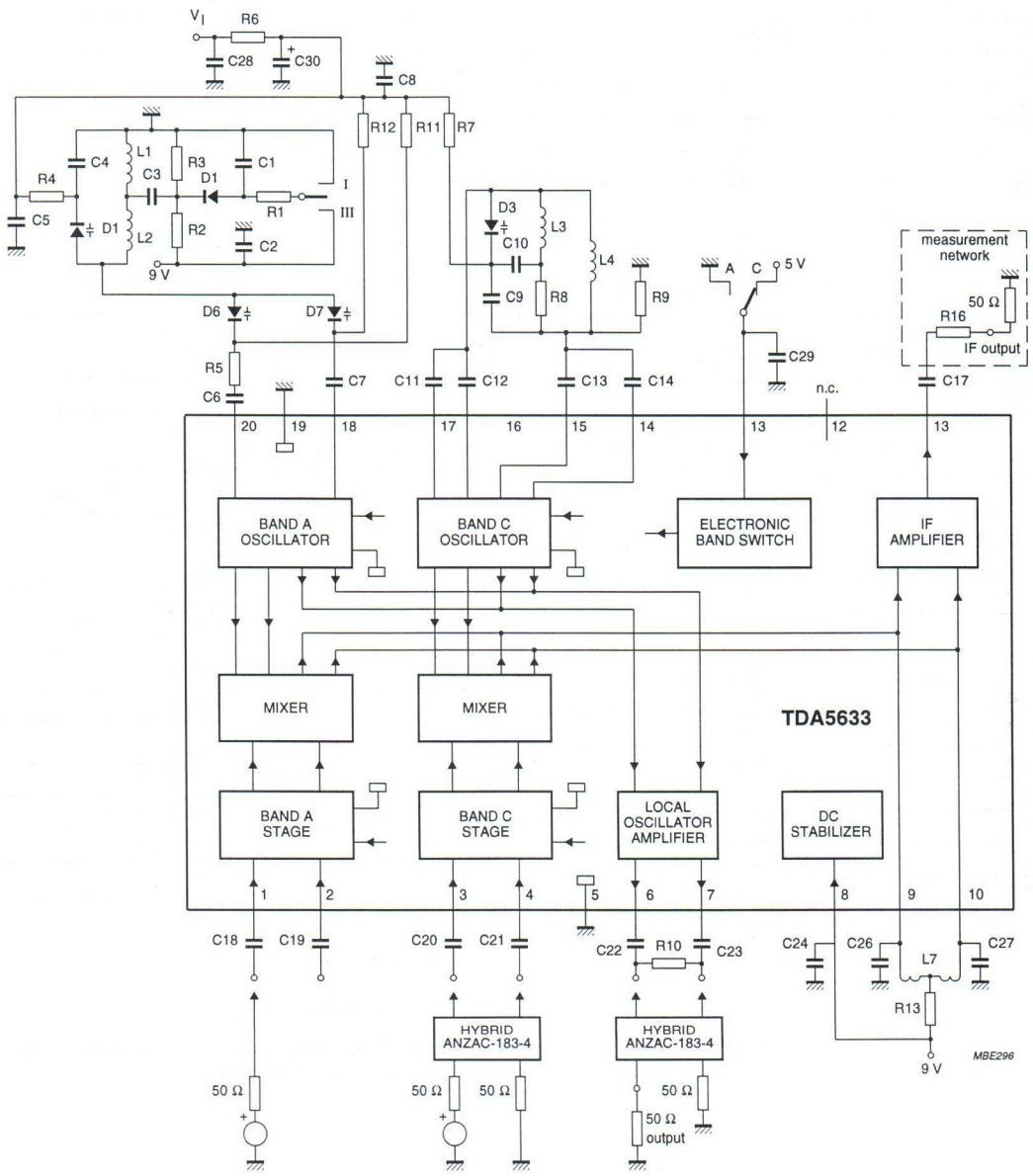


Fig.3 Test circuit.

Application diagram components values

Table 1 Capacitors (all SMD and NP0 except C5 to C9 and C29)

NUMBER	VALUE
C1	1 nF
C2	1 nF
C3	1 nF
C4	56 pF
C5	2.2 nF
C6	2 pF
C7	4 pF
C8	2.2 nF
C9	6 pF (N470)
C10	100 pF
C11	1 pF (N750)
C12	1 pF (N750)
C13	1 pF (N750)
C14	1 pF (N750)
C17	1 nF
C18	1 nF
C19	1 nF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C26	15 pF
C27	15 pF
C28	2.2 nF
C29	1 nF
C30	1 μF (40 V electrolytic capacitor)

Table 2 Resistors (all SMD)

NUMBER	VALUE
R1	10 Ω
R2	12 kΩ
R3	2.7 kΩ
R4	47 kΩ
R5	56 Ω
R6	47 kΩ
R7	22 kΩ
R8	2.2 kΩ
R9	22 kΩ
R10	100 Ω
R11	47 kΩ
R12	47 kΩ
R13	150 Ω
R16	27 Ω

Table 3 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BA682
D2	BB133
D3	BB146
D6	BB131
D7	BB131
Coils(1)	
L1	6 t (4 mm)
L2	3 t (3.5 mm)
L3	2 t (2.5 mm)
L4	3 t (2.5 mm)

Note

1. Wire size for L1 to L4 is 0.4 mm

Transformer (L7 = 2 × 5 t)

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

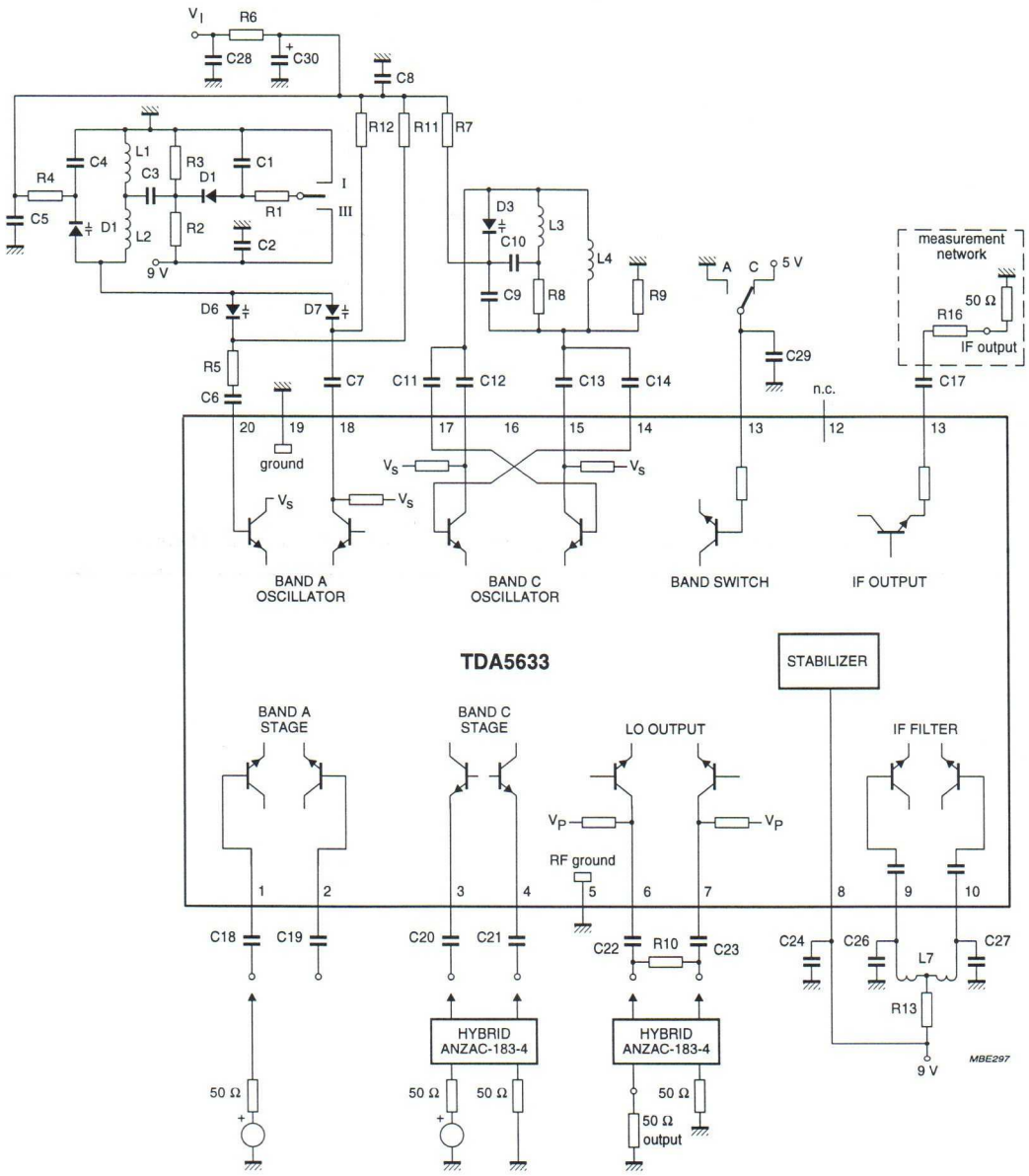


Fig.4 Electrical test circuit.

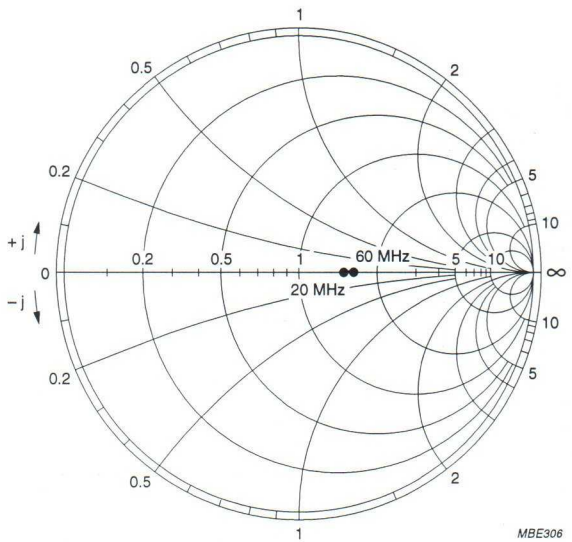


Fig.5 Output reflection coefficient (S_{22}) of the IF amplifier (20 to 60 MHz) (Z chart).

Low-power UHF mixer/oscillator for TV and VCR tuners

TDA5634T

FEATURES

- Balanced mixer with common base inputs
- 4-pin oscillator
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability.

DESCRIPTION

The TDA5634T is a monolithic integrated circuit which has been designed to cover the UHF mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package. The UHF oscillator frequency range is from 470 to 900 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9.0	–	V
I_P	supply current		–	35	–	mA
f_R	frequency range		430	–	860	MHz
N	noise figure		–	9	–	dB
V_i	input voltage	1% cross-modulation	–	85	–	dBμV
G_v	voltage gain		–	36	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5634T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

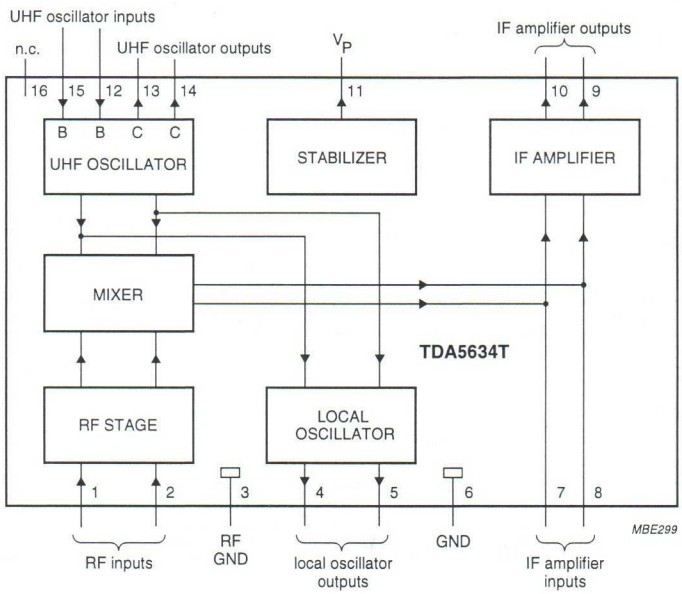


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RFIN1	1	RF input 1
RFIN2	2	RF input 2
RFGND	3	ground for RF inputs
LOOUT1	4	local oscillator amplifier output 1
LOOUT2	5	local oscillator amplifier output 2
GND	6	ground (0 V)
IFIN1	7	IF amplifier input 1
IFIN2	8	IF amplifier input 2
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
V_P	11	supply voltage
UHFOSCIB1.	12	oscillator input base 1
UHFOSCOC1	13	oscillator output collector 1
UHFOSCOC2	14	oscillator output collector 2
UHFOSCIB2	15	oscillator input base 2
n.c.	16	not connected

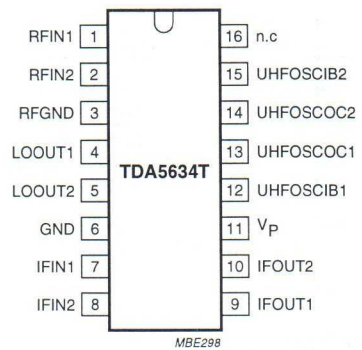


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+10.5	V
$V_{P(op)}$	operating supply voltage	8.1	9.9	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Human body model: the IC withstands 2000 V in accordance with *UZW-BO-FQ-A302*; R = 1.5 kΩ; C = 100 pF.

Machine model: the IC withstands 200 V except pin 11 (175 V) in accordance with *UZW-BO-FQ-B302*; R = 0 Ω; C = 200 pF.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; differentially measured at 36 MHz; all S parameters are referenced to a 50 Ω system: unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX	UNIT
				MOD.	PHASE		
S_{11}	input reflection coefficient	see Fig.6	–	–0.6	–2.5	–	dB/°C
S_{12}	reverse transmission coefficient	see Fig.7	–	–56	30	–	dB/°C
S_{21}	forward transmission coefficient		–	–9.5	165	–	dB/°C
S_{22}	output reflection coefficient	see Fig.7	–	–7	6	–	dB/°C
Z_o	output impedance ($R_s + jL_s$)	R_s; see Fig.3	-	100		-	Ω
		L_s; see Fig.3	-	32		-	nH
Y_i	input admittance	see Fig.3	–	0.8		–	mS
		see Fig.3	–	2.5		–	pF

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current	V_P = 8.1 to 9.9 V; T_{amb} = –10 to +80 °C	–	35	45	mA
Mixer (including IF amplifier); measurements using hybrid; note 1						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz	–	9	11	dB
		f_i = 860 MHz	–	9	11	dB
Z_I	input impedance ($R_s + L_s$)	f_i = 430; see Fig.4	–	28	–	Ω
		f_i = 430; see Fig.4	–	8	–	nH
		f_i = 860; see Fig.4	–	33	–	Ω
		f_i = 860; see Fig.4	–	8	–	nH
V_i	input voltage	1% cross modulation; in channel; f_i = 430 MHz	79	82	–	dBμV
		1% cross modulation; in channel; f_i = 860 MHz	82	85	–	dBμV
		10 kHz pulling; in channel; f_i = 860 MHz	–	87	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 820 MHz; note 2	65	72	–	dBμV
G_v	voltage gain	f_i = 430 MHz; note 3	33	36	39	dB
		f_i = 860 MHz; note 3	33	36	39	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_R	frequency range	V_{tune} = 0.45 to 28 V; V_P = 8.1 to 9.9 V; T_{amb} = −10 to +80 °C	470	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 4	–	–	400	kHz
f_{drift}	frequency drift	with no compensation; notes 5 and 6	–	–	2.5	MHz
		with compensation; notes 5 and 7	–	–	800	kHz
		5 s to 15 min after switch on; with no compensation; note 8	–	–	600	kHz
LO output						
Y_o	output admittance (G_P//C_P)	f_i = 470 MHz; see Fig.5	–	3	–	mS
		f_i = 470 MHz; see Fig.5	–	0.5	–	pF
		f_i = 900 MHz; see Fig.5	–	3.5	–	mS
		f_i = 900 MHz; see Fig.5	–	0.5	–	pF
V_O	output voltage	R_L = 50 Ω; V_P = 8.1 to 9.9 V; T_{amb} = −10 to +80 °C	83	91	100	dBμV
SRF	spurious signal on LO output w.r.t. LO output signal	R_L = 50 Ω; note 9	–	–	−10	dB
HLO	LO signal harmonics w.r.t. LO signal	R_L = 50 Ω	–	–	−10	dB

Notes

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. The input level of N + 5 − 1 MHz signal which gives a signal of 30 dB below the oscillator carrier at the LO output.
3. The gain is defined as the transducer gain (measured in Fig.3) plus the voltage transformation ratio of L3 to L2.
4. The frequency shift is defined as a change in oscillator frequency fro a variation in supply voltage. In one instance V_P = 9 to 8.1 V and in the other instance V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
5. The frequency drift is defined as a change in oscillator frequency for a variation of ambient temperature. In one instance T_{amb} = 25 °C to T_{amb} = 0 °C and in the other instance T_{amb} = 25 °C to T_{amb} = 50 °C.
6. The capacitors in the oscillator circuit in Fig.3 (C11 to C16) are NP0 types.
7. The capacitors in the oscillator circuit in Fig.3, have the following temperature coefficients; C11 to C14 = N750; C15 = N470 and C16 = NP0.
8. Switching on drift is the change of oscillator frequency between 5 seconds and 15 minutes after switch-on.
9. Measured at 50 Ω with RF input voltage = 97 dBμV.

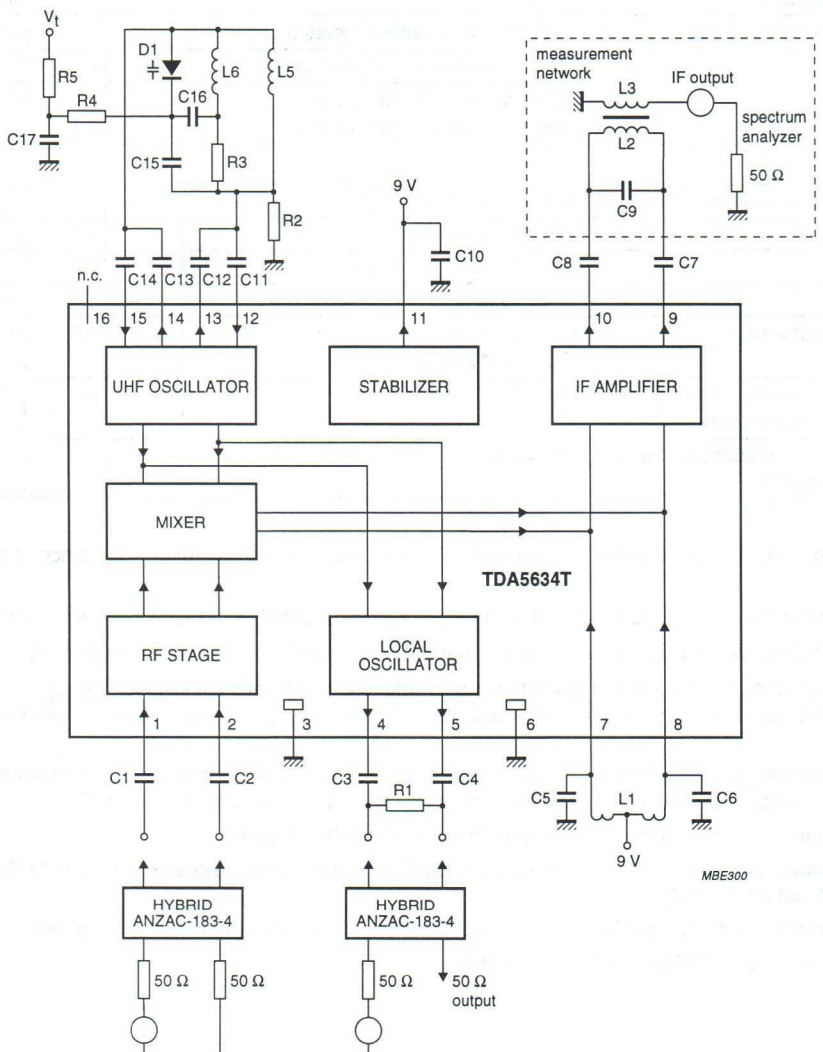


Fig.3 Reference measurement set-up.

Component values for measurement circuit

Table 1 Capacitors (all SMD and NP0 except C11 to C15)

COMPONENT	VALUE
C1	1 nF
C2	1 nF
C3	1 nF
C4	1 nF
C5	18 pF
C6	18 pF
C7	1 nF
C8	1 nF
C9	18 pF
C10	22 nF
C11	1 pF (N750)
C12	1 pF (N750)
C13	1 pF (N750)
C14	1 pF (N750)
C15	6 pF (N470)
C16	100 pF
C17	1 μF

Table 2 Resistors (all SMD))

COMPONENT	VALUE
R1	100 Ω
R2	22 kΩ
R3	2.2 kΩ
R4	22 kΩ
R5	47 kΩ

Table 3 Diodes and IC

COMPONENT	VALUE
D1	BB215
IC	TDA5634T

Table 4 Coils (wire size 0.4 mm)

COMPONENT	VALUE
L5	2.5 turns; dia. 3 mm
L6	2.5 turns; dia. 3 mm

Table 5 Transformers; note 1

COMPONENT	VALUE
L1	2 × 6 turns
L2	2 × 5 turns
L3	2 turns

Note

1. Coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026.

APPLICATION INFORMATION

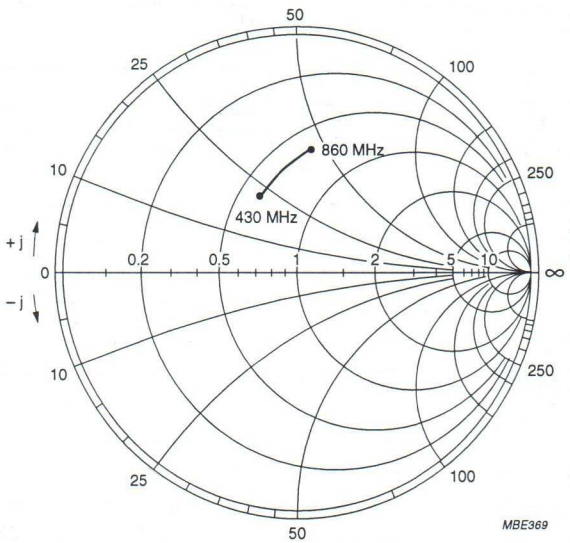


Fig.4 Input impedance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

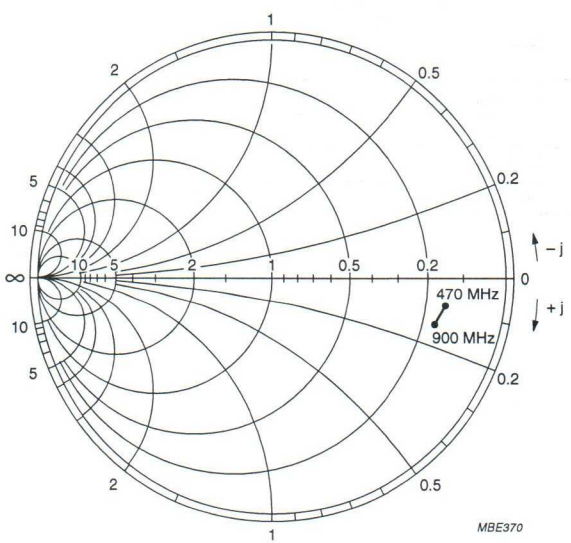


Fig.5 Output admittance (S_{22}) of the LO output (470 to 900 MHz) (Y chart).

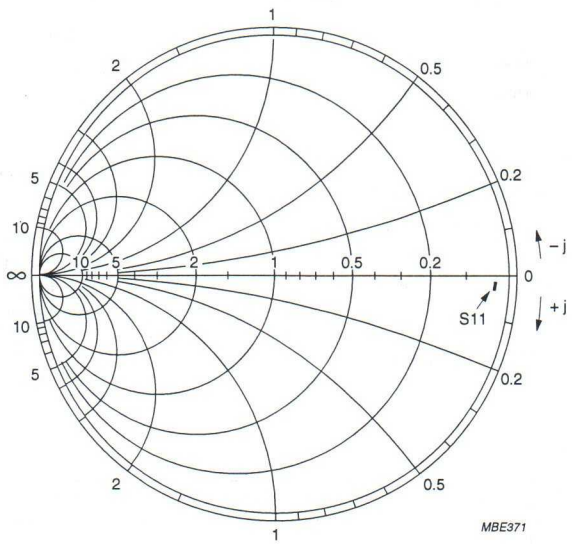


Fig.6 Input admittance (S_{11}) of the IF amplifier (25 to 45 MHz) (Y chart).

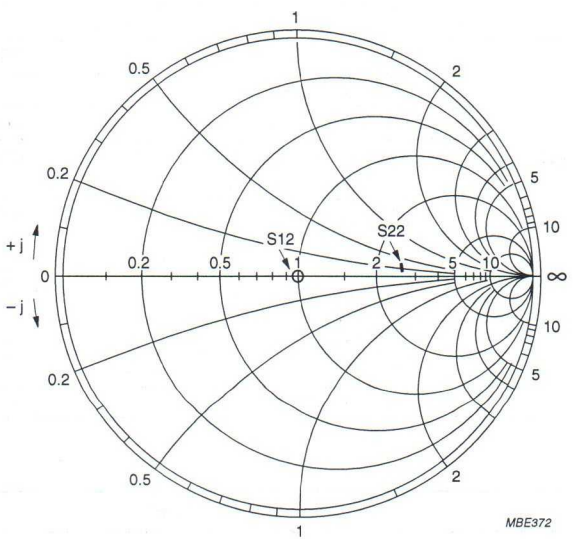


Fig.7 Reverse transmission and output reflection (S_{12} and S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5636

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A and B
- Balanced mixer with a common base input for band B and C (balanced input)
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with 75 Ω output impedance in application
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter between the mixer output and the IF amplifier input.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

GENERAL DESCRIPTION

The TDA5636 is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 9 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9	–	V
I_P	supply current	band A	–	45	–	mA
		band B	–	41	–	mA
		band C	–	44	–	mA
f_R	frequency range	band B; see Fig.13	45	–	180	MHz
		band A; see Fig.13	160	–	470	MHz
		band C; see Fig.13	430	–	860	MHz
N	noise figure	R_L = 75 Ω; band A	–	7.5	–	dB
		R_L = 75 Ω; band B	–	6.0	–	dB
		R_L = 75 Ω; band C	–	7.0	–	dB
V_O	output voltage	1% cross modulation; R_L = 75 Ω; band A	–	110	–	dBμV
		1% cross modulation; R_L = 75 Ω; band B	–	110	–	dBμV
		1% cross modulation; R_L = 75 Ω; band C	–	110	–	dBμV
G_v	voltage gain	R_L = 75 Ω; band A	–	20	–	dB
		R_L = 75 Ω; band B	–	31	–	dB
		R_L = 75 Ω; band C	–	31	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5636M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA5636T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

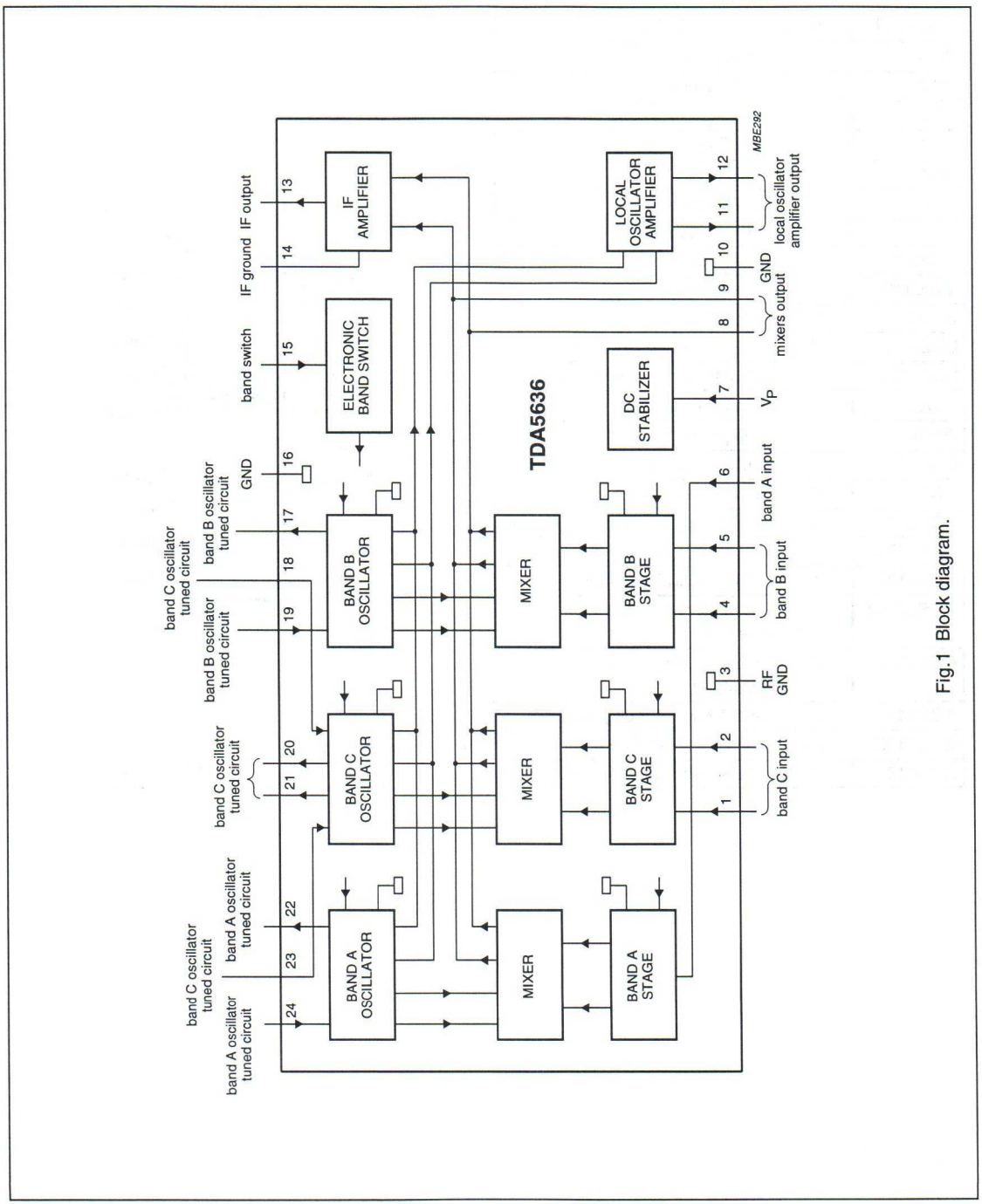


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CIN1	1	band C input 1
CIN2	2	band C input 2
RFGND	3	ground for RF inputs
BIN1	4	band B input 1
BIN2	5	band B input 2
AIN	6	band A input
V_P	7	supply voltage
MIXOUT1	8	mixers output 1
MIXOUT2	9	mixers output 2
GND1	10	ground 1 (0 V)
LOOUT1	11	local oscillator amplifier output 1
LOOUT2	12	local oscillator amplifier output 2
IFOUT	13	IF amplifier output
IFGND	14	IF amplifier ground
BS	15	electronic band switch
GND2	16	ground 2 (0 V)
BOSCOC	17	band B oscillator output collector
COSCIB1	18	band C oscillator input base 1
BOSCIB	19	band B oscillator input base
COSCOC1	20	band C oscillator output collector 1
COSCOC2	21	band C oscillator output collector 2
AOSCOC	22	band A oscillator output collector
COSCIB2	23	band C oscillator input base 2
AOSCIB	24	band A oscillator input base

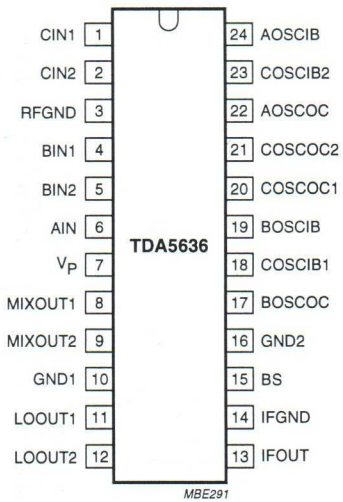


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX/	UNIT
V_P	supply voltage	−0.3	+10.5	V
$V_{SW(max)}$	maximum switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	–	10	s
T_{stg}	IC storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SSOP	119	K/W
	SO	75	K/W

HANDLING

Human Body Model: GND (10) (16), RFGND (3), IFGND (14), VP (7) separately. All pins withstand 2000 V in accordance with the *UZW-BO/FQ-A302* specification equivalent to the *MIL-STD-883C* category B (2000 V).

Machine Model: All pins withstand 200 V.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.13; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MOD.	PHASE	MAX.	UNIT
S_{22}	output reflection coefficient	through 1 nF; see Fig.10	–	−14.5	5.5	–	dB/Ↄ
Z_o	output impedance (R_s + L_s)	through 1 nF	–	73	–	–	Ω
		through 1 nF	–	12	–	–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.13; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current	band A	–	45	50.5	mA
		band B	–	41	46	mA
		band C	–	44	49	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band B	1.6	–	2.4	V
		band C	3.0	–	V_P	V
I_{SW}	switching current	band A	–	–	2	µA
		band B	–	–	5	µA
		band C; $V_{SW(C)}$ = 5 V	–	–	10	µA
Band A mixer (including IF amplifier)						
f_R	frequency range	see Fig.13	45	–	180	MHz
N	noise figure	f_i = 50 MHz; note 1	–	7.5	9.5	dB
		f_i = 180 MHz; note 1	–	7.5	9.5	dB
g_{os}	optimum source conductance	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1	–	mS
Y_I	input admittance	see Fig.7	–	–	–	mS
C_I	input capacitance	f_i = 50 to 180 MHz	–	2	–	pF
V_o	output voltage	1% cross-modulation in channel; R_L = 75 Ω; f_i = 50 MHz; see Fig.5	107	110	–	dBµV
		1% cross-modulation in channel; R_L = 75 Ω; f_i = 50 MHz; see Fig.5	107	110	–	dBµV
V_i	input voltage	R_L = 75 Ω; 10 kHz pulling in channel; f_i = 180 MHz; note 2	–	100	–	dBµV
G_v	voltage gain	R_L = 75 Ω; f_i = 50 MHz; see Fig.3	17.5	20	22.5	dB
		R_L = 75 Ω; f_i = 180 MHz; see Fig.3	17.5	20	22.5	dB
Band A oscillator						
f_R	frequency range	see Fig.13	80	–	216	MHz
f_{shift}	frequency shift	ΔV_p = 10%; note 3	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C without any compensation: NP0 capacitors; note 7	–	–	500	kHz
		5 s to 15 min after switching on; note 4	–	–	200	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (including IF amplifier)						
f_R	frequency range	see Fig.13	160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz; R_L = 75 Ω	–	6.0	8.0	dB
		f_i = 470 MHz; R_L = 75 Ω	–	7.0	9.0	dB
Z_I	input impedance (R_s + L_s)	f_i = 170 to 470 MHz; see Fig.8	–	–	–	
V_o	output voltage	1% cross-modulation in channel; R_L = 75 Ω; f_i = 170 MHz; see Fig.6	107	110	–	dBμV
		1% cross-modulation in channel; R_L = 75 Ω; f_i = 470 MHz; see Fig.6	107	110	–	dBμV
V_i	input voltage	10 kHz pulling in channel; 470 MHz; note 2	–	91	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 430 MHz; note 5	–	77	–	dBμV
G_v	voltage gain	f_i = 170 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
		f_i = 470 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
Band B oscillator						
f_R	frequency range	see Fig.13	200	–	500	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 3	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C without any compensation; NP0 capacitors; note 7	–	–	2	MHz
		5 s to 15 min after switching on; note 4	–	–	300	kHz
Band C Mixer (including IF amplifier)						
f_R	frequency range	see Fig.13	430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz; R_L = 75 Ω	–	7.0	9.0	dB
		f_i = 860 MHz; R_L = 75 Ω	–	8.0	10.0	dB
V_o	output voltage	1% cross-modulation in channel; f_i = 430 MHz; R_L = 75 Ω; see Fig.6	107	110	–	dBμV
		1% cross-modulation in channel; f_i = 860 MHz; R_L = 75 Ω; see Fig.6	107	110	–	dBμV
Z_I	input impedance (R_s + L_s)	f_i = 430 to 860 MHz; see Fig.9	–	–	–	Ω
		f_i = 430 to 860 MHz; see Fig.9	–	–	–	nH
V_i	input voltage	10 kHz pulling in channel; f_i = 860 MHz; note 2	–	93	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 820 MHz; note 6	–	79	–	dBμV
G_v	voltage gain	f_i = 430 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
		f_i = 860 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range	see Fig.13	470	–	900	MHz
f_{shiift}	frequency shift	ΔV_P = 10; note 3	–	–	500	kHz
f_{drift}	frequency drift	ΔT = 25 °C with compensation; note 7	–	–	900	kHz
		5 s to 15 min after switching on; note 4	–	–	400	kHz
LO output						
S_{22}	output reflection coefficient	see Fig.11	–	–	–	
Z_O	output impedance	see Fig.11	–	–	–	Ω
		see Fig.11	–	–	–	nH
V_o	output voltage	R_L = 50 Ω	83	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; note 8	–	–	–10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω	–	–	–10	dB

Notes

1. These measurements were made with an input circuit for optimum noise figure given in Fig.12.
2. The input level signal causing 10 kHz frequency detuning at the LO output.
3. The frequency shift is defined as a change in oscillator frequency for a variation of supply voltage. In one instance V_P = 9 to 8.1 V and in the other instance V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
4. Switching on drift is the change of oscillator frequency between 5 seconds and 15 minutes after switching on.
5. The input level of a N + 5 – 1 MHz signal which gives FM sidebands 30 dB below the oscillator carrier at the LO output;

   f_{RF} = 430 MHz: frequency of the wanted channel; this signal is not applied to the RF input for this measurement

   f_{OSC} = 468.9 MHz ($f_{RF} + f_{IF}$)

   f_{N+5-1} = 469 MHz: unwanted frequency of the N + 5 channel – 1 MHz. This signal is applied to the RF input.
6. The input level of a N + 5 – 1 MHz signal which gives FM sidebands 30 dB below the oscillator carrier at the LO output;

   f_{RF} = 820 MHz: frequency of the wanted channel; this signal is not applied to the RF input for this measurement

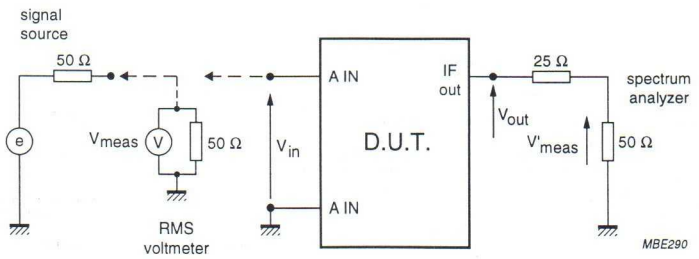
   f_{OSC} = 858.9 MHz ($f_{RF} + f_{IF}$)

   f_{N+5-1} = 859 MHz: unwanted frequency of the N + 5 channel – 1 MHz. This signal is applied to the RF input.
7. The frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from T_{amb} = 25 °C to T_{amb} = 0 °C and on the other hand from T_{amb} = 25 °C to T_{amb} = 50 °C.
8. SRF: spurious signal on LO with respect to LO output signal;

   RF level = 120 dBμV at f_i < 180 MHz

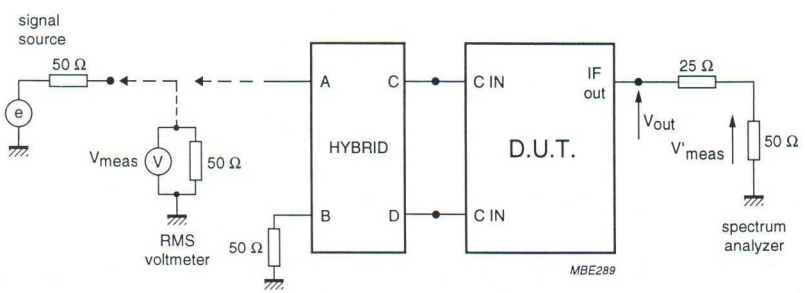
   RF level = 107 dBμV at f_i = 180 MHz to 225 MHz

   RF level = 97 dBμV at f_i = 225 MHz to 860 MHz.



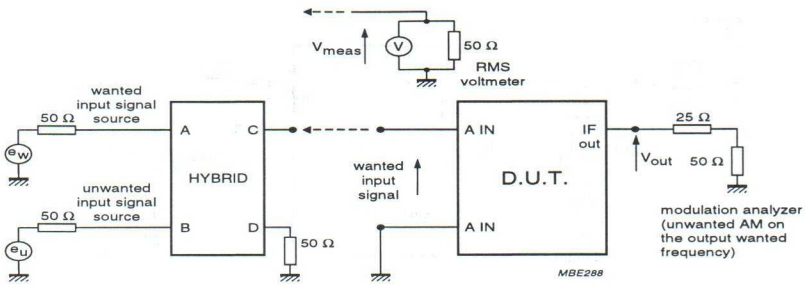
$Z_i >> 50\ \Omega \geq V_i = 2V_{meas}$; $V_o = V'_{meas} \times (50 + 25)/50$; voltage gain for band A = $20\log(V_o/V_i)$.

Fig.3 Band A gain measurement.



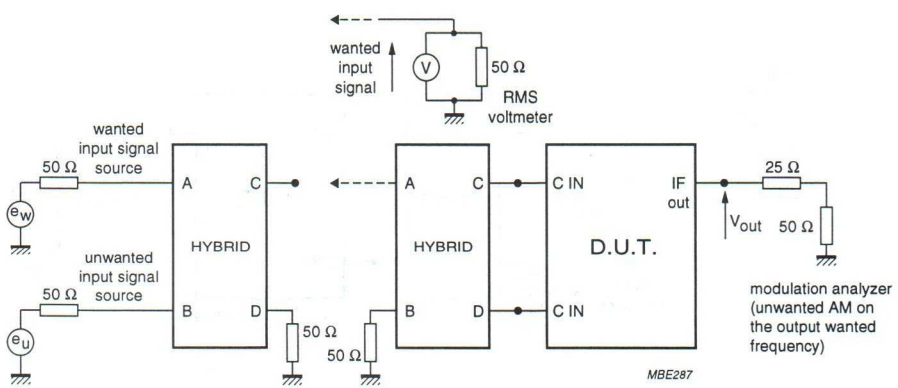
$V_i = V_{meas}$; $V_o = V_{meas} \times (50 + 25)/50$; voltage gain for band B = $20\log(V_o/V_i) + loss_{(hybrid)}$; voltage gain for band C = $20\log(V_o/V_i) + loss_{(hybrid)}$.

Fig.4 Bands B and C gain measurement.



Wanted input signal = 80 dBμV; V_o = output voltage from mixer A (including the IF amplifier) for a wanted output signal with 0.3% AM.

Fig.5 Band A 1% cross-modulation.



Wanted input signal = 70 dBμV; V_o = output voltage from mixer B (mixer C) (including the IF amplifier) for a wanted output signal with 0.3% AM.

Fig.6 Bands B and C 1% cross-modulation.

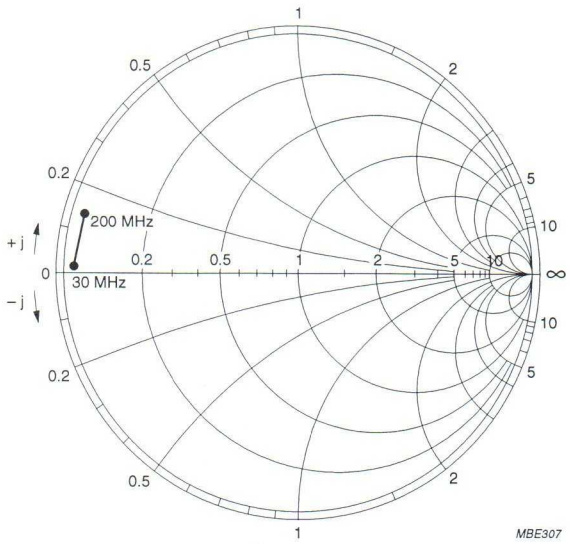


Fig.7 Input admittance (S_{11}) of the band A mixer input (30 to 200 MHz) (Y chart).

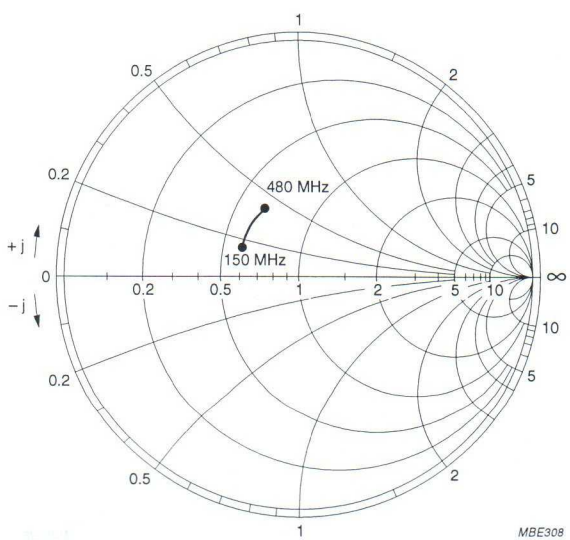


Fig.8 Input impedance (S_{11}) of the band B mixer input (150 to 480 MHz) (Z chart).

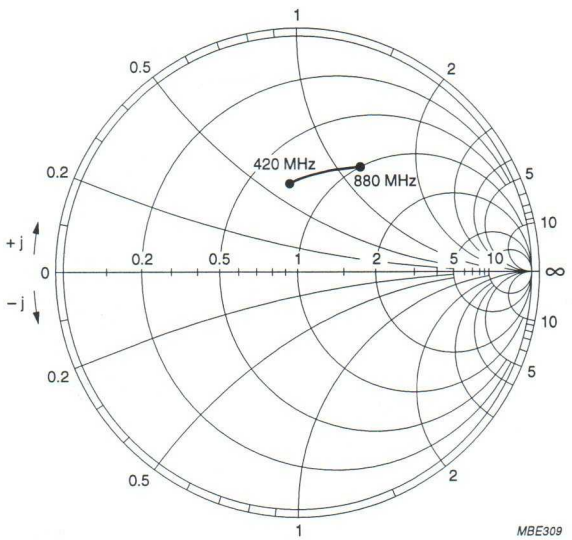


Fig.9 Input impedance (S_{11}) of the band C mixer input (430 to 880 MHz) (Z chart).

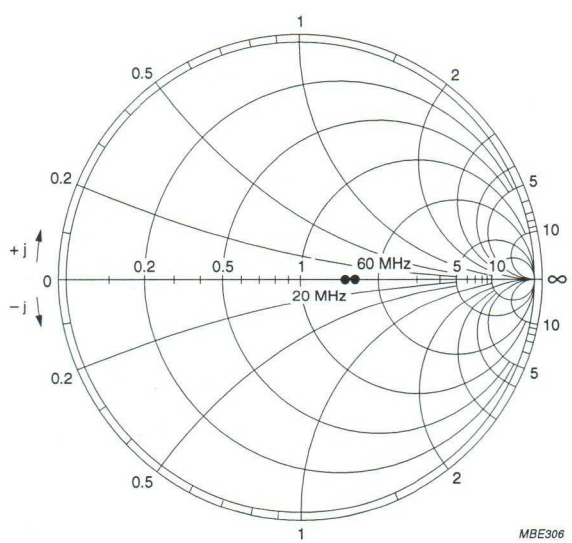


Fig.10 Output impedance (S_{22}) of the IF amplifier (20 to 60 MHz) (Z chart).

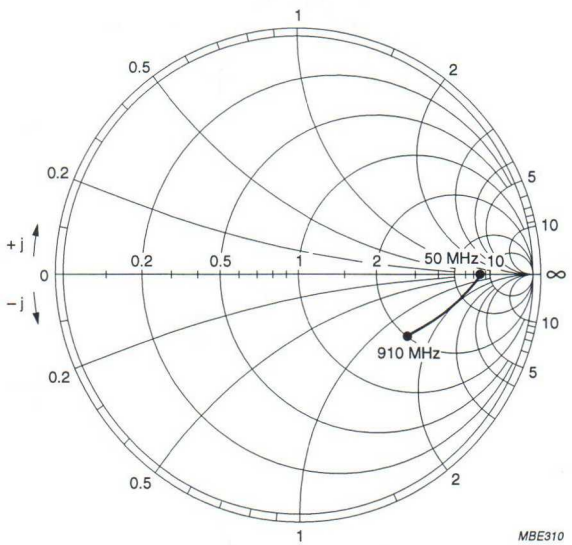
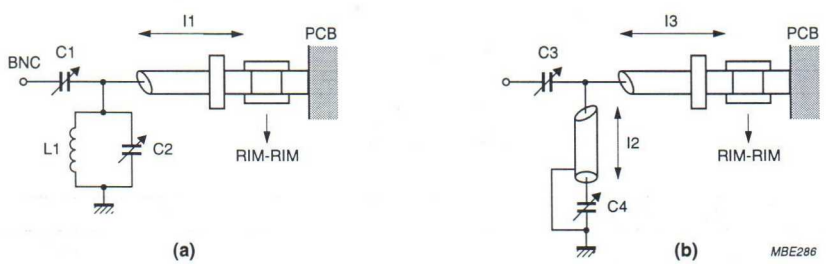


Fig.11 Output impedance (S_{22}) of the LO amplifier (50 to 910 MHz) (Z chart).

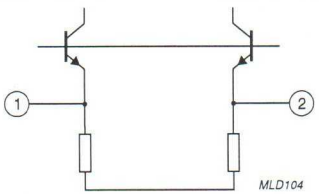
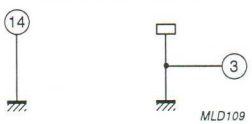
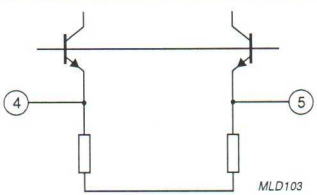
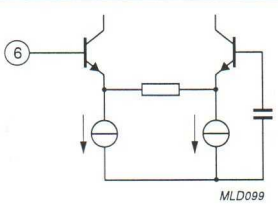


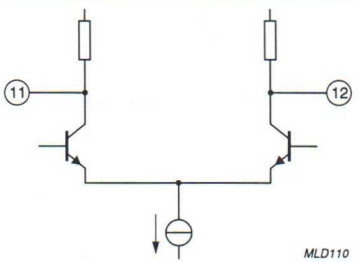
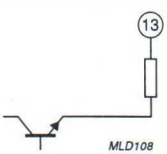
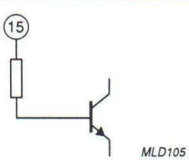
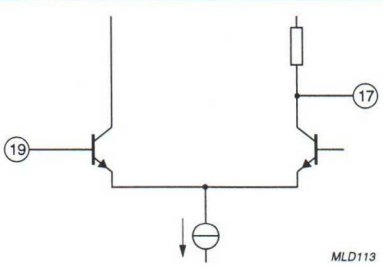
(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (5.5 mm, wire diam. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

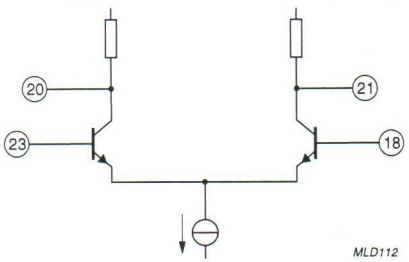
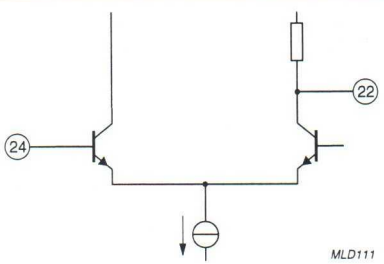
(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.12 Input circuit for minimum noise figure.

Table 1 Internal pin configuration

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
1	CIN1		0	0	2.2
2	CIN2		0	0	2.2
3	RFGND		0	0	0
14	IFGND		0	0	0
4	BIN1		0	2.2	0
5	BIN2		0	2.2	0
6	AIN		2.2	1.2	1.2
7	V_P	supply voltage	9	9	9
8	MIXOUT1		8.4	8.4	8.4
9	MIXOUT2		8.4	8.4	8.4

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
10	GND		0	0	0
16	GND		0	0	0
11	LOOUT1		5.6	5.6	5.6
12	LOOUT2		5.6	5.6	5.6
13	IFOUT		4.5	4.5	4.5
15	BS		$V_{SW(A)}$	$V_{SW(B)}$	$V_{SW(C)}$
17	BOSCOC		5.8	3.4	5.8
19	BOSCIB		1.2	2.3	1.2

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
18	COSCIB1		1.4	1.4	2.3
20	COSCOC1		5.8	5.8	4.2
21	COSCOC2		5.8	5.8	4.2
23	COSCIB2		1.4	1.4	2.3
22	AOSCOC		3.8	5.8	5.8
24	AOSCIB		2.1	1.0	1.0

APPLICATION INFORMATION

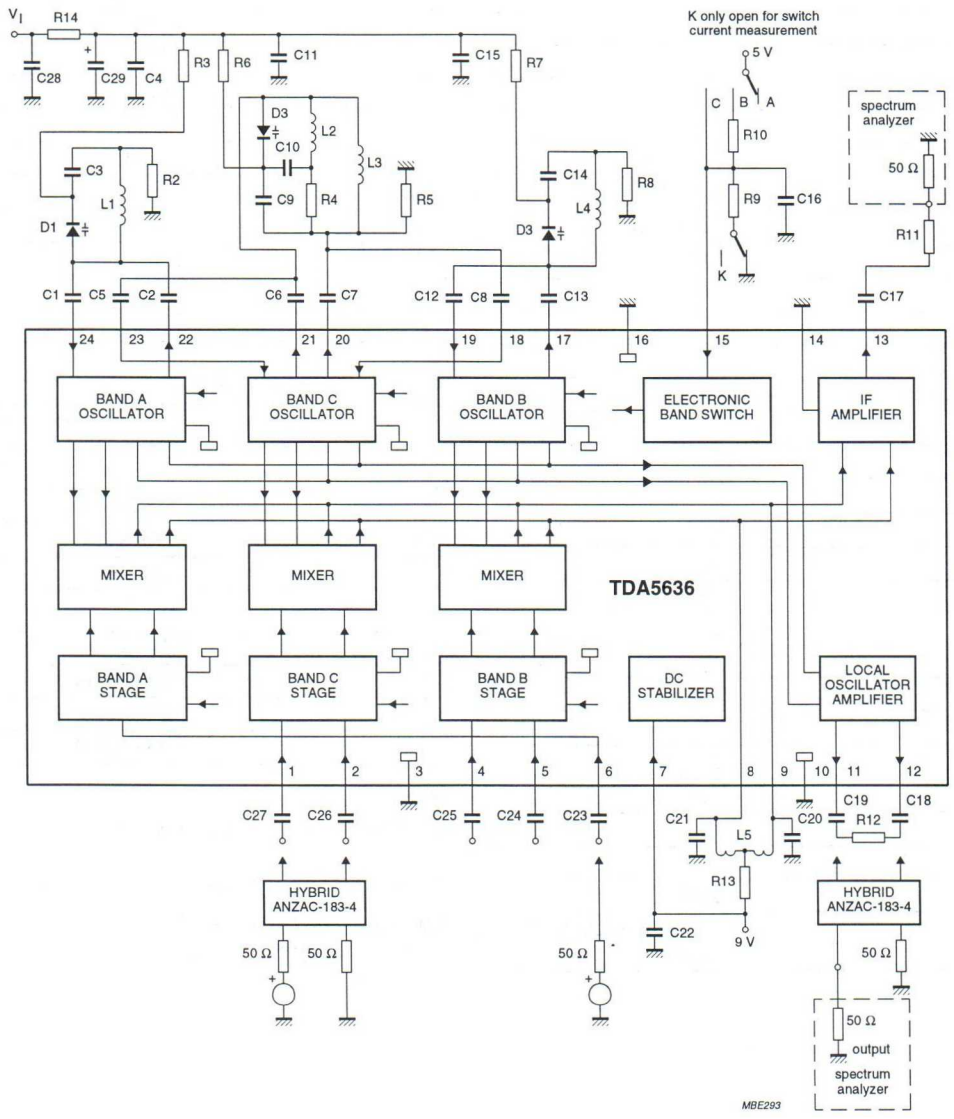


Fig.13 Application diagram.

Application diagram components values

Table 2 Capacitors (all SMD and NP0 except C5 to C9 and C29)

NUMBER	VALUE
C1	2 pF
C2	2 pF
C3	82 pF
C4	2.2 nF
C5	1 pF (N750)
C6	1 pF (N750)
C7	1 pF (N750)
C8	1 pF (N750)
C9	6 pF (N470)
C10	100 pF
C11	2.2 nF
C12	2 pF
C13	4 pF
C14	150 pF
C15	2.2 nF
C16	1.2 nF
C17	1 nF
C18	1 nF
C19	1 nF
C20	12 pF
C21	12 pF
C22	22 nF
C23	1 nF
C24	1 nF
C25	1 nF
C26	1 nF
C27	1 nF
C28	2.2 nF
C29	1 µF (40 V electrolytic capacitor)

Table 3 Resistors (all SMD)

NUMBER	VALUE
R2	22 Ω
R3	47 kΩ
R4	2.2 kΩ
R5	22 kΩ
R6	47 kΩ
R7	47 kΩ
R8	12 Ω
R9	15 kΩ
R10	33 kΩ
R11	27 Ω
R12	100 Ω
R13	150 Ω
R14	47 kΩ

Table 4 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB146
Coils(1)	
L1	8 t (3 mm)
L2	2 t (2.5 mm)
L3	3 t (2.5 mm)
L4	2 t (4 mm)

Note

1. Wire size for L1 to L4 is 0.4 mm

Transformer (L5 = 2 × 6)

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5637

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A and B
- Balanced mixer with a common base input for band B and C (balanced input)
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with 75 Ω output impedance in application
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter between the mixer output and the IF amplifier input.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

GENERAL DESCRIPTION

The TDA5637 is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 9 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	9	–	V
I_P	supply current	band A	–	45	–	mA
		band B	–	41	–	mA
		band C	–	44	–	mA
f_R	frequency range	band A; see Fig.13	45	–	180	MHz
		band B; see Fig.13	160	–	470	MHz
		band C; see Fig.13	430	–	860	MHz
N	noise figure	R_L = 75 Ω; band A	–	7.5	–	dB
		R_L = 75 Ω; band B	–	6.0	–	dB
		R_L = 75 Ω; band C	–	7.0	–	dB
V_O	output voltage	1% cross modulation; R_L = 75 Ω; band A	–	110	–	dBμV
		1% cross modulation; R_L = 75 Ω; band B	–	110	–	dBμV
		1% cross modulation; R_L = 75 Ω; band C	–	110	–	dBμV
G_v	voltage gain	R_L = 75 Ω; band A	–	20	–	dB
		R_L = 75 Ω; band B	–	31	–	dB
		R_L = 75 Ω; band C	–	31	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5637M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA5637T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

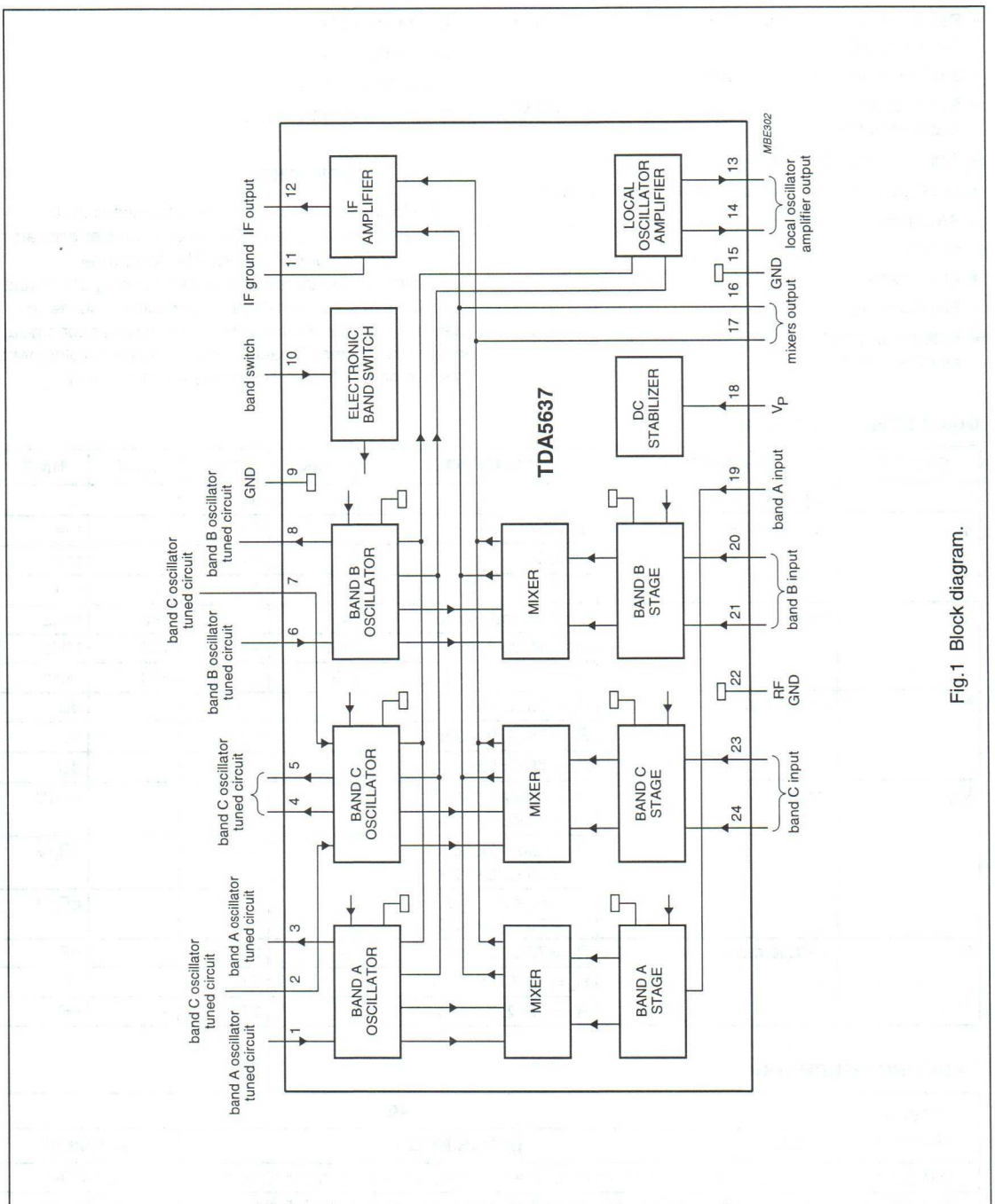


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
COSCIB1	2	band C oscillator input base 1
AOSCOC	3	band A oscillator output collector
COSCOC1	4	band C oscillator output collector 1
COSCOC2	5	band C oscillator output collector 2
BOSCIB	6	band B oscillator input base
COSCIB2	7	band C oscillator input base 2
BOSCOC	8	band B oscillator output collector
GND1	9	ground 1 (0 V)
BS	10	electronic band switch
IFGND	11	IF amplifier ground
IFOUT	12	IF amplifier output
LOOUT1	13	local oscillator amplifier output 1
LOOUT2	14	local oscillator amplifier output 2
GND2	15	ground 2 (0 V)
MIXOUT1	16	mixers output 1
MIXOUT2	17	mixers output 2
V_P	18	supply voltage
AIN	19	band A input
BIN1	20	band B input 1
BIN2	21	band B input 2
RFGND	22	ground for RF inputs
CIN1	23	band C input 1
CIN2	24	band C input 2

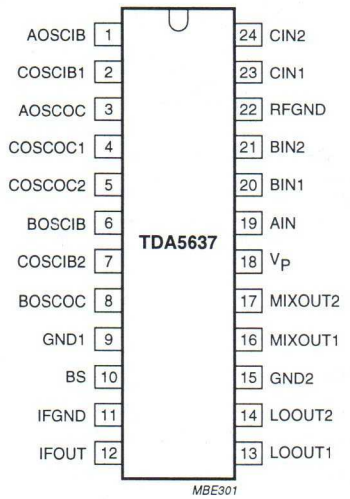


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX/	UNIT
V_P	supply voltage	−0.3	+10.5	V
$V_{SW(max)}$	maximum switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	–	10	s
T_{stg}	IC storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SSOP	119	K/W
	SO	75	K/W

HANDLING

Human Body Model: GND (9) (15), RFGND (22), IFGND (11), V_P (18) separately. All pins withstand 2000 V in accordance with the *UZW-BO/FQ-A302* specification equivalent to the *MIL-STD-883C* category B (2000 V).

Machine Model: All pins withstand 200 V.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured at 36 MHz; measured in circuit of Fig.13; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX.	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	through 1 nF; see Fig.10	–	−14.5	5.5	–	dB/°
Z_o	output impedance (R_s + L_s)	through 1 nF	–	73		–	Ω
		through 1 nF	–	12		–	nH

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; measured in circuit of Fig.13; unless otherwise specified.

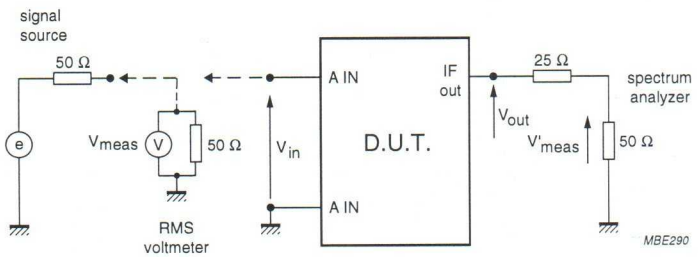
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8.1	9.0	9.9	V
I_P	supply current	band A	–	45	50.5	mA
		band B	–	41	46	mA
		band C	–	44	49	mA
V_{SW}	switching voltage	band A	0	–	1.1	V
		band B	1.6	–	2.4	V
		band C	3.0	–	V_P	V
I_{SW}	switching current	band A	–	–	2	µA
		band B	–	–	5	µA
		band C; $V_{SW(C)}$ = 5 V	–	–	10	µA
Band A mixer (including IF amplifier)						
f_R	frequency range	see Fig.13	45	–	180	MHz
N	noise figure	f_i = 50 MHz; note 1	–	7.5	9.5	dB
		f_i = 180 MHz; note 1	–	7.5	9.5	dB
g_{os}	optimum source conductance	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1	–	mS
Y_I	input admittance	see Fig.7	–	–	–	mS
C_I	input capacitance	f_i = 50 to 180 MHz	–	2	–	pF
V_o	output voltage	1% cross-modulation in channel; R_L = 75 Ω; f_i = 50 MHz; see Fig.5	107	110	–	dBµV
		1% cross-modulation in channel; R_L = 75 Ω; f_i = 180 MHz; see Fig.5	107	110	–	dBµV
V_i	input voltage	R_L = 75 Ω; 10 kHz pulling in channel; f_i = 180 MHz; note 2	–	100	–	dBµV
G_v	voltage gain	R_L = 75 Ω; f_i = 50 MHz; see Fig.3	17.5	20	22.5	dB
		R_L = 75 Ω; f_i = 180 MHz; see Fig.3	17.5	20	22.5	dB
Band A oscillator						
f_R	frequency range	see Fig.13	80	–	216	MHz
f_{shift}	frequency shift	ΔV_p = 10%; note 3	–	–	200	kHz
f_{drift}	frequency drift	ΔT = 25 °C without any compensation: NP0 capacitors; note 7	–	–	500	kHz
		5 s to 15 min after switching on; note 4	–	–	200	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (including IF amplifier)						
f_R	frequency range	see Fig.13	160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz; R_L = 75 Ω	–	6.0	8.0	dB
		f_i = 470 MHz; R_L = 75 Ω	–	7.0	9.0	dB
Z_I	input impedance (R_s + L_s)	f_i = 170 to 470 MHz; see Fig.8	–	–	–	
V_o	output voltage	1% cross-modulation in channel; R_L = 75 Ω; f_i = 170 MHz; see Fig.6	107	110	–	dBμV
		1% cross-modulation in channel; R_L = 75 Ω; f_i = 470 MHz; see Fig.6	107	110	–	dBμV
V_i	input voltage	10 kHz pulling in channel; 470 MHz; note 2	–	91	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 430 MHz; note 5	–	77	–	dBμV
G_v	voltage gain	f_i = 170 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
		f_i = 470 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
Band B oscillator						
f_R	frequency range	see Fig.13	200	–	500	MHz
f_{shift}	frequency shift	ΔV_P = 10%; note 3	–	–	400	kHz
f_{drift}	frequency drift	ΔT = 25 °C without any compensation; NP0 capacitors; note 7	–	–	2	MHz
		5 s to 15 min after switching on; note 4	–	–	300	kHz
Band C Mixer (including IF amplifiers)						
f_R	frequency range	see Fig.13	430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz; R_L = 75 Ω	–	7.0	9.0	dB
		f_i = 860 MHz; R_L = 75 Ω	–	8.0	10.0	dB
V_o	output voltage	1% cross-modulation in channel; f_i = 430 MHz; R_L = 75 Ω; see Fig.6	107	110	–	dBμV
		1% cross-modulation in channel; f_i = 860 MHz; R_L = 75 Ω; see Fig.6	107	110	–	dBμV
Z_I	input impedance (R_s + L_s)	f_i = 430 to 860 MHz; see Fig.9	–	–	–	Ω
		f_i = 430 to 860 MHz; see Fig.9	–	–	–	nH
V_i	input voltage	10 kHz pulling in channel; f_i = 860 MHz; note 2	–	93	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 820 MHz; note 6	–	79	–	dBμV
G_v	voltage gain	f_i = 430 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB
		f_i = 860 MHz; R_L = 75 Ω; see Fig.4	28	31	34	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range	see Fig.13	470	–	900	MHz
f_{shiift}	frequency shift	ΔV_P = 10; note 3	–	–	500	kHz
f_{drift}	frequency drift	ΔT = 25 °C with compensation; note 7	–	–	900	kHz
		5 s to 15 min after switching on; note 4	–	–	400	kHz
LO output						
S_{22}	output reflection coefficient	see Fig.11	–	–	–	
Z_O	output impedance	see Fig.11	–	–	–	Ω
		see Fig.11	–	–	–	nH
V_o	output voltage	R_L = 50 Ω	83	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; note 8	–	–	−10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω	–	–	−10	dB

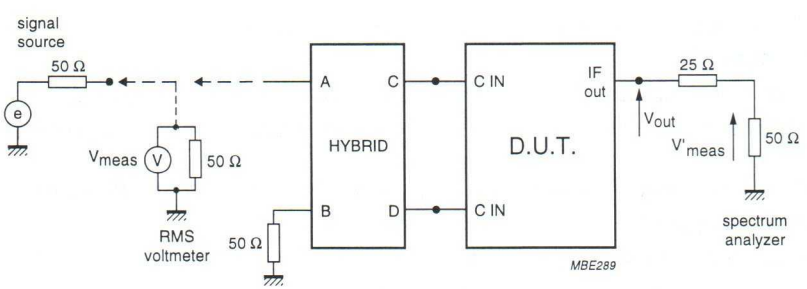
Notes

1. These measurements were made with an input circuit for optimum noise figure given in Fig.12.
2. The input level signal causing 10 kHz frequency detuning at the LO output.
3. The frequency shift is defined as a change in oscillator frequency for a variation of supply voltage. In one instance V_P = 9 to 8.1 V and in the other instance V_P = 9 to 9.9 V. In both cases, the frequency shift is below the specified value.
4. Switching on drift is the change of oscillator frequency between 5 seconds and 15 minutes after switching on.
5. The input level of a N + 5 – 1 MHz signal which gives FM sidebands 30 dB below the oscillator carrier at the LO output;
   a) f_{RF} = 430 MHz: frequency of the wanted channel; this signal is not applied to the RF input for this measurement.
   b) f_{OSC} = 468.9 MHz ($f_{RF} + f_{IF}$).
   c) f_{N+5-1} = 469 MHz: unwanted frequency of the N + 5 channel – 1 MHz. This signal is applied to the RF input.
6. The input level of a N + 5 – 1 MHz signal which gives FM sidebands 30 dB below the oscillator carrier at the LO output;
   a) f_{RF} = 820 MHz: frequency of the wanted channel; this signal is not applied to the RF input for this measurement.
   b) f_{OSC} = 858.9 MHz ($f_{RF} + f_{IF}$).
   c) f_{N+5-1} = 859 MHz: unwanted frequency of the N + 5 channel – 1 MHz. This signal is applied to the RF input.
7. The frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from T_{amb} = 25 °C to T_{amb} = 0 °C and on the other hand from T_{amb} = 25 °C to T_{amb} = 50 °C.
8. SRF: spurious signal on LO with respect to LO output signal;
   a) RF level = 120 dBμV at f_i < 180 MHz.
   b) RF level = 107 dBμV at f_i < 180 MHz to 225 MHz.
   c) RF level = 97 dBμV at f_i < 225 MHz to 860 MHz.



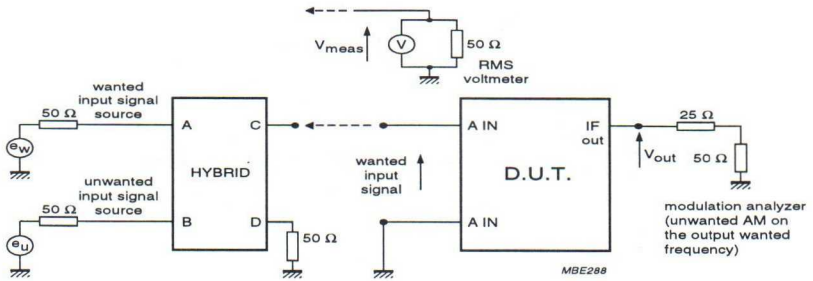
$Z_i >> 50\ \Omega \geq V_i = 2V_{meas}$; $V_o = V'_{meas} \times (50 + 25)/50$; voltage gain for band A = $20\log(V_o/V_i)$.

Fig.3 Band A gain measurement.



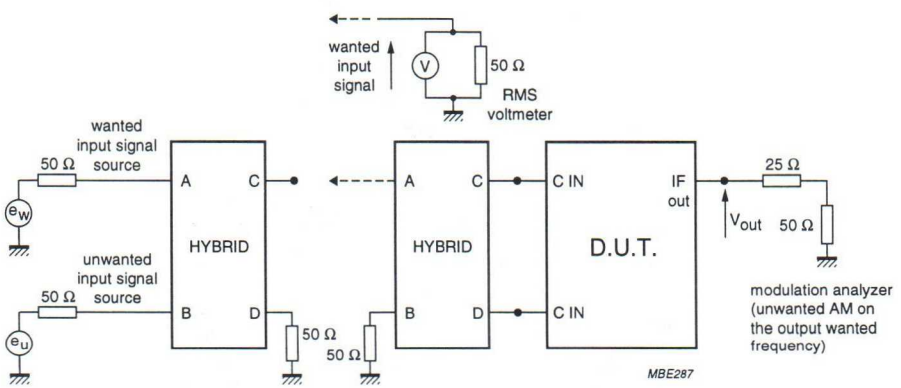
$V_i = V_{meas}$; $V_o = V_{meas} \times (50 + 25)/50$; voltage gain for band B = $20\log(V_o/V_i) + loss_{(hybrid)}$; voltage gain for band C = $20\log(V_o/V_i) + loss_{(hybrid)}$.

Fig.4 Bands B and C gain measurement.



Wanted input signal = 80 dBμV; V_o = output voltage from mixer A (including the IF amplifier) for a wanted output signal with 0.3% AM.

Fig.5 Band A 1% cross-modulation.



Wanted input signal = 70 dBμV; V_o = output voltage from mixer B (mixer C)(including the IF amplifier) for a wanted output signal with 0.3% AM.

Fig.6 Bands B and C 1% cross-modulation.

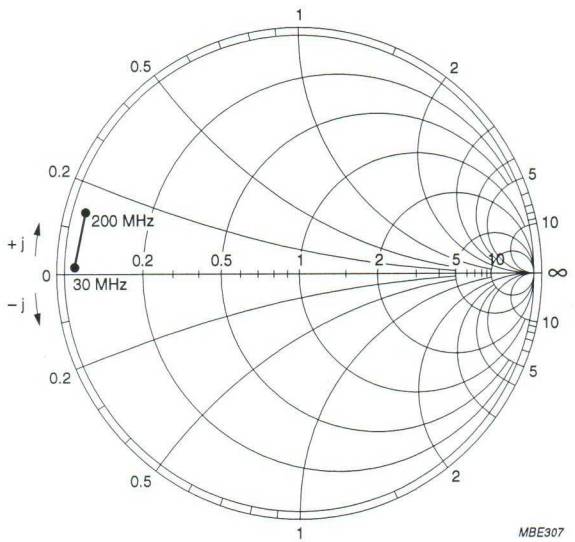


Fig.7 Input admittance (S_{11}) of the band A mixer input (30 to 200 MHz) (Y chart).

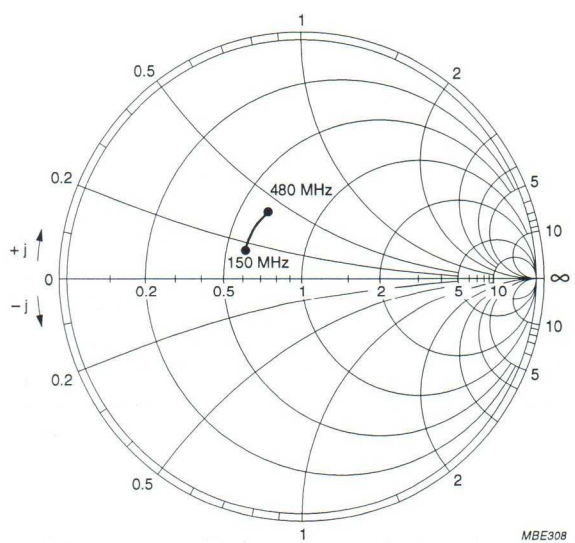


Fig.8 Input impedance (S_{11}) of the band B mixer input (150 to 480 MHz) (Z chart).

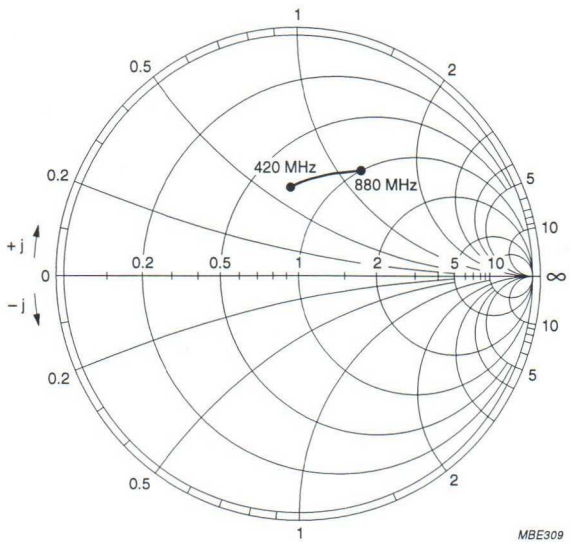


Fig.9 Input impedance (S_{11}) of the band C mixer input (430 to 880 MHz) (Z chart).

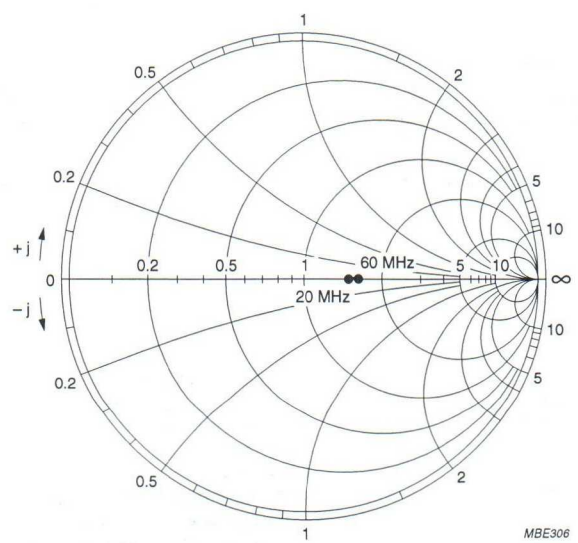


Fig.10 Output impedance (S_{22}) of the IF amplifier (20 to 60 MHz) (Z chart).

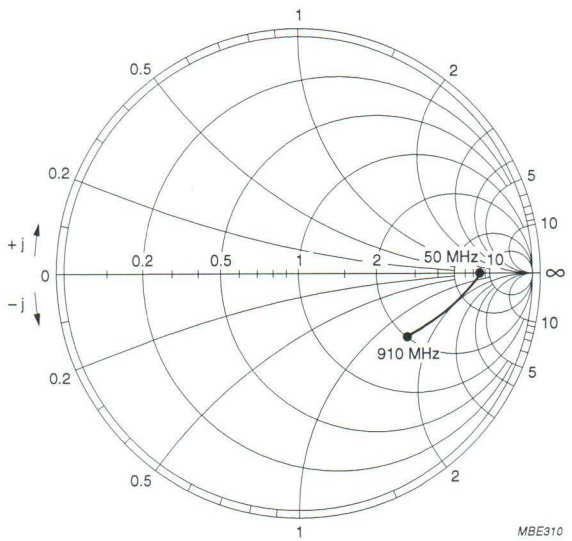
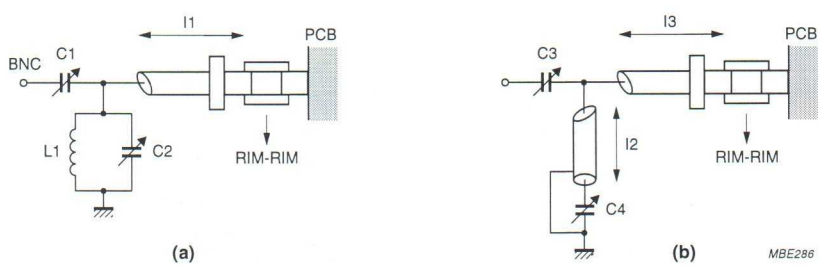


Fig.11 Output impedance (S_{22}) of the LO amplifier (50 to 910 MHz) (Z chart).

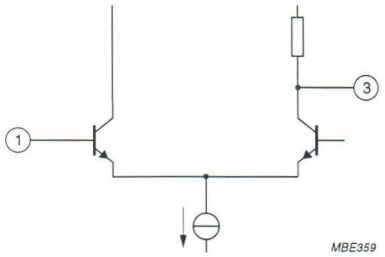
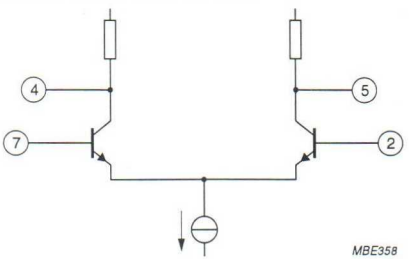
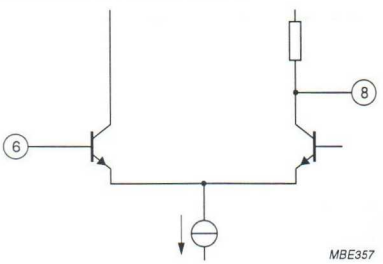
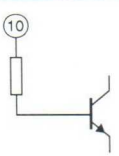


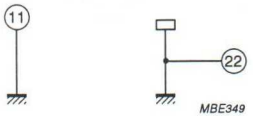
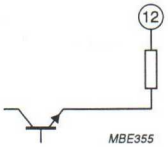
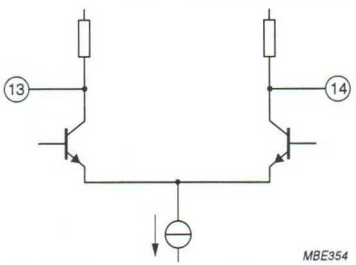
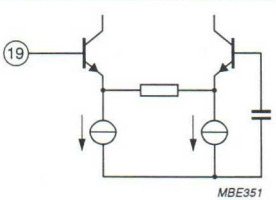
(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (5.5 mm, wire diam. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

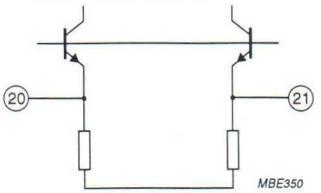
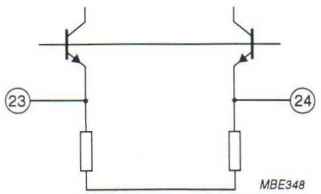
(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.12 Input circuit for minimum noise figure.

Table 1 Internal pin configuration

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
1	AOSCIB		2.1	1.0	1.0
3	AOSCOC		3.8	5.8	5.8
2	COSCIB1		1.4	1.4	2.3
4	COSCOC1		5.8	5.8	4.2
5	COSCOC2		5.8	5.8	4.2
7	COSCIB2		1.4	1.4	2.3
6	BOSCIB		1.2	2.3	1.2
8	BOSCOC		5.8	3.4	5.8
9	GND1		0	0	0
15	GND2		0	0	0
10	BS		$V_{SW(A)}$	$V_{SW(B)}$	$V_{SW(C)}$

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
11	IFGND		0	0	0
22	RFGND		0	0	0
12	IFOUT		4.5	4.5	4.5
13	LOOUT1		5.6	5.6	5.6
14	LOOUT2		5.6	5.6	5.6
16	MIXOUT1		8.4	8.4	8.4
17	MIXOUT2		8.4	8.4	8.4
18	V_P	supply voltage	9.0	9.0	9.0
19	AIN		2.2	1.2	1.2

PIN	SYMBOL	CONFIGURATION	AVERAGE DC VOLTAGE		
20	BIN1		0	2.2	0
21	BIN2		0	2.2	0
23	CIN1		0	0	2.2
24	CIN2		0	0	2.2

APPLICATION INFORMATION

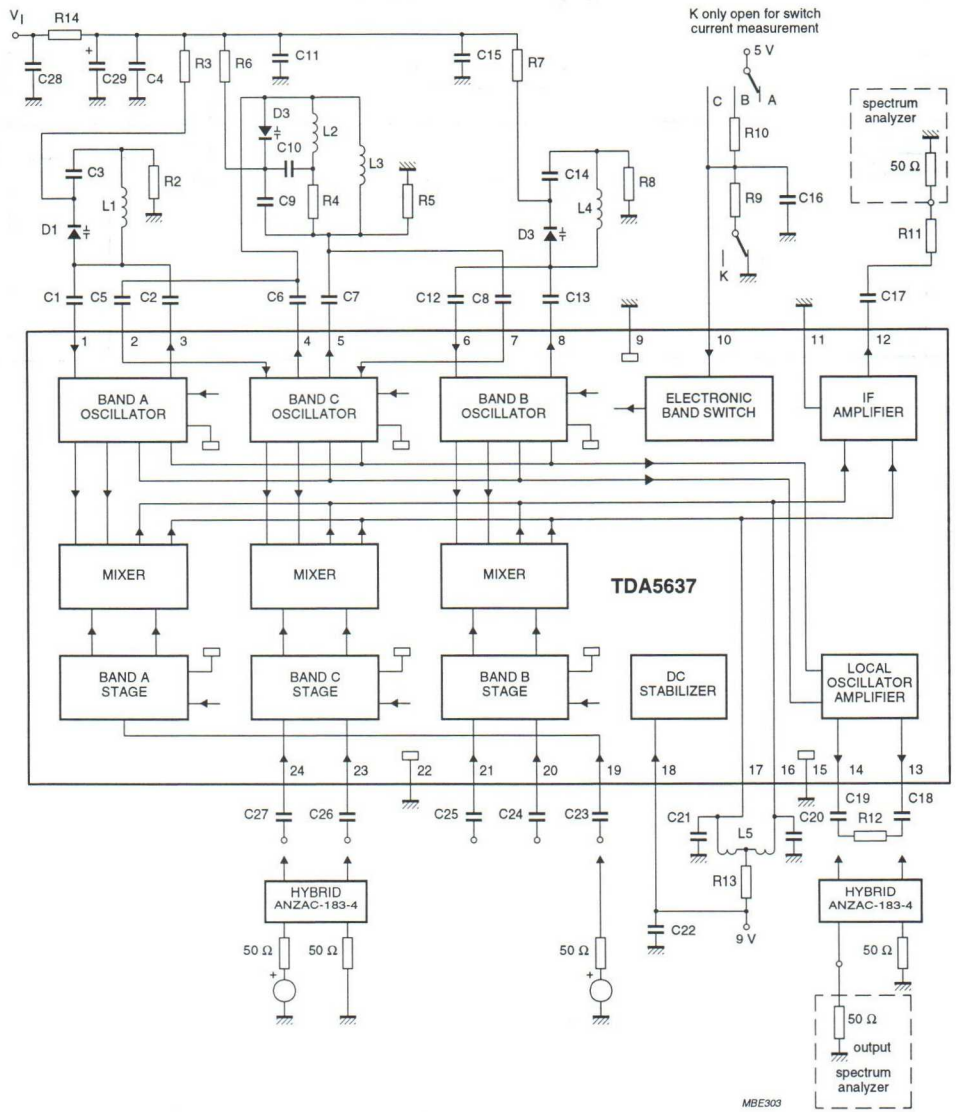


Fig.13 Application diagram.

Application diagram components values

Table 2 Capacitors (all SMD and NP0 except C5 to C9 and C29)

NUMBER	VALUE
C1	2 pF
C2	2 pF
C3	82 pF
C4	2.2 nF
C5	1 pF (N750)
C6	1 pF (N750)
C7	1 pF (N750)
C8	1 pF (N750)
C9	6 pF (N470)
C10	100 pF
C11	2.2 nF
C12	2 pF
C13	4 pF
C14	150 pF
C15	2.2 nF
C16	1.2 nF
C17	1 nF
C18	1 nF
C19	1 nF
C20	12 pF
C21	12 pF
C22	22 nF
C23	1 nF
C24	1 nF
C25	1 nF
C26	1 nF
C27	1 nF
C28	2.2 nF
C29	1 µF (40 V electrolytic capacitor)

Table 3 Resistors (all SMD)

NUMBER	VALUE
R2	22 Ω
R3	47 kΩ
R4	2.2 kΩ
R5	22 kΩ
R6	47 kΩ
R7	47 kΩ
R8	12 Ω
R9	15 kΩ
R10	33 kΩ
R11	27 Ω
R12	100 Ω
R13	150 Ω
R14	47 kΩ

Table 4 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB146
Coils(1)	
L1	8 t (3 mm)
L2	2 t (2.5 mm)
L3	3 t (2.5 mm)
L4	2 t (4 mm)

Note

1. Wire size for L1 to L4 is 0.4 mm

Transformer (L5 = 2 × 6)

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5731M

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- 3-pin oscillator for band C
- Balanced mixer with a common base input for band B and C (balanced input)
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Electronic band switch.

GENERAL DESCRIPTION

The TDA5731M is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 5 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

In addition, when hyperband is not required, the TDA5731M may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHFI and VHFIII in band A and the tuned circuit of band C for UHF.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	36	–	mA
f_R	frequency range	band A	42	–	180	MHz
		band B	160	–	470	MHz
		band C	430	–	860	MHz
N	noise figure	band A	–	7.5	–	dB
		band B	–	8.0	–	dB
		band C	–	9.0	–	dB
IP	intermodulation	band A	–	–66	–	dB
		band B	–	–66	–	dB
		band C	–	–66	–	dB
G_v	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	33	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5731M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

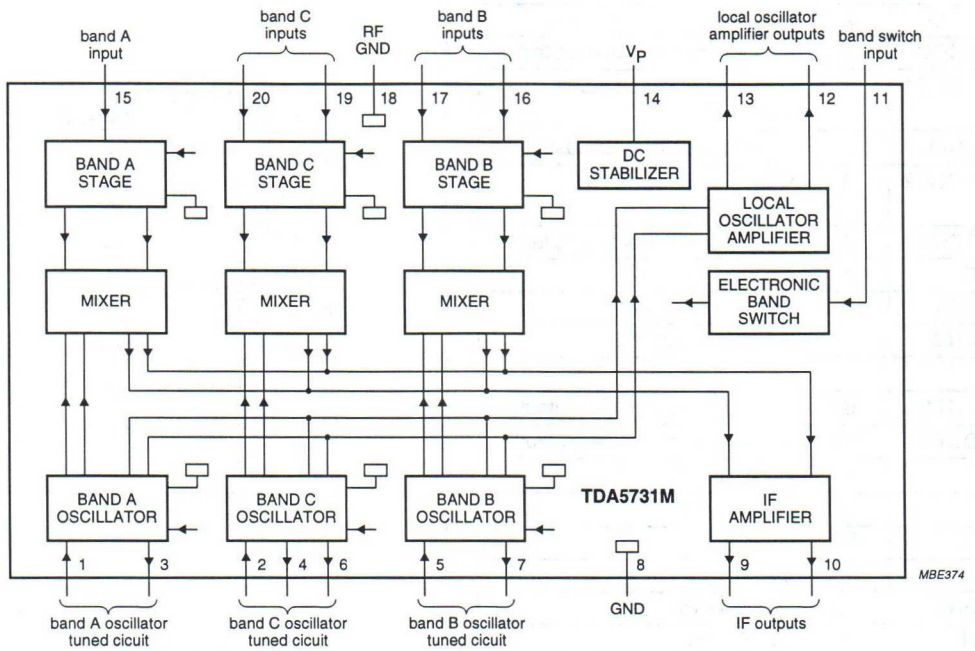


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
COSCIB	2	band C oscillator input base
AOSCOC	3	band A oscillator output collector
COSCOC1	4	band C oscillator output collector 1
BOSCIB	5	band B oscillator input base
COSCOC2	6	band C oscillator output collector 2
BOSCOC	7	band B oscillator output collector
GND	8	ground (0 V)
IFOUT1	9	IF amplifier output 1
IFOUT2	10	IF amplifier output 2
BS	11	band switch input
LOOUT1	12	local oscillator amplifier output 1
LOOUT2	13	local oscillator amplifier output 2
V_P	14	supply voltage
AIN	15	band A input
BIN1	16	band B input 1
BIN2	17	band B input 2
RFGND	18	ground for RF input
CIN1	19	band C input 1
CIN2	20	band C input 2

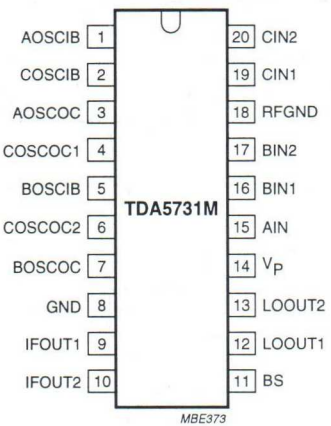


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX/	UNIT
V_P	supply voltage	−0.3	+7.0	V
$V_{SW(max)}$	maximum switching voltage	−0.3	+7.5	V
$V_{P(op)}$	operating supply voltage	4.5	5.5	V
$V_{n(max)}$	maximum voltage on each pin with a 22 kΩ resistor connected in series	−	35	V
I_O	output current of each pin to ground	−	−10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	−	10	s
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	−	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Human Body Model: GND (8), RFGND (18), V_P (14) shorted together. Pins 4, 6 and 7 withstand 500 V. All other pins withstand 2000 V.

Machine Model: GND (8), RFGND (18), V_P (14) shorted together. Pins 4, 6 and 7 withstand 50 V. All other pins withstand 200 V.

IF AMPLIFIER CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; differentialy measured at 36 MHz; measured in circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX.	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	note 1; see Fig.11	−	−14	+9	−	dB/°C
Z_o	output impedance (R_s + L_s)	R_s	−	74		−	Ω
		L_s	−	21		−	nH

Note

1. All S parameters are referenced to a 50 Ω system.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		28	36	44	mA
V_{SW}	switching voltage (depending on supply voltage V_P)	band A	0	–	$0.18V_P$	V
		band B	$0.26V_P$	–	$0.47V_P$	V
		band C	$0.55V_P$	–	V_P	V
I_{SW}	switching current	band A	–	–	2	μA
		band B	–	–	10	μA
		band C	–	–	25	μA
Band A mixer (including IF amplifier)						
f_R	frequency range		42	–	180	MHz
N	noise figure	f_i = 50 MHz; see Fig.3	–	7.5	9	dB
		f_i = 180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for minimum noise figure	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1.1	–	mS
Y_I	input admittance (G_P//C_P)	f_i = 50 MHz; see Fig.7	–	0.27	–	mS
		f_i = 180 MHz; see Fig.7	–	0.34	–	mS
		f_i = 50 to 180 MHz; see Fig.7	–	1.9	–	pF
IP3	intermodulation using the 3 signals method	f_N = 180 MHz; note 1	–	−66	−60	dB
V_i	input voltage	10 kHz pulling in channel; f_i = 180 MHz	96	100	–	dBμV
G_v	voltage gain	$20\log(V_{9\text{-}10}/V_{15})$; f_i = 50 MHz; note 2	20.5	23	25.5	dB
		$20\log(V_{9\text{-}10}/V_{15})$; f_i = 180 MHz; note 2	20.5	23	25.5	dB
Band A oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	80	–	210	MHz
f_{shift}	frequency shift	ΔV_p = ±5%; note 3	–	–	200	kHz
$\chi_{ripple(p\text{-}p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 80 MHz; note 4	20	–	–	mV
$f_{ripple(p\text{-}p)}$	frequency ripple (peak-to-peak value)	from 20 Hz to 500 kHz; f_i = 210 MHz	20	–	–	mV
f_{drift}	frequency drift	without compensation: notes 5 and 6	–	–	600	kHz
		5 s to 15 min after switching on; without compensation: note 7	–	–	200	kHz

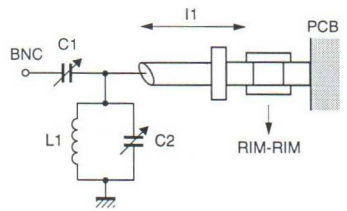
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (including IF amplifier); measurements using hybrid; note 8						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz	–	8.0	10	dB
		f_i = 470 MHz	–	8.0	10	dB
Z_I	input impedance ($R_s + L_s$)	f_i = 160 to 470 MHz; see Fig.8	–	23	–	Ω
		f_i = 160 to 470 MHz; see Fig.8	–	10	–	nH
IP3	intermodulation using the 3 signal method	f_N = 170 MHz; note 1	–	–66	–60	dB
		f_N = 470 MHz; note 1	–	–66	–60	dB
V_i	input voltage	f_i = 470 MHz; 10 kHz pulling; in channel	83	87	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 470 MHz; note 9	–	62	–	dBμV
G_v	voltage gain	f_i = 170 MHz; note 2	31	34	37	dB
		f_i = 470 MHz; note 2	31	34	37	dB
Band B oscillator						
f_R	frequency range	T_{amb} = –10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	205	–	490	MHz
f_{shift}	frequency shift	ΔV_P = ±5%; note 3	–	–	400	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 205 MHz; note 8	20	–	–	mV
$f_{ripple(p-p)}$	frequency ripple (peak-to-peak value)	from 20 Hz to 500 kHz; f_i = 490 MHz	10	–	–	mV
f_{drift}	frequency drift	without compensation; notes 5 and 6	–	–	2	MHz
		5 s to 15 min after switching on; without compensation; note 7	–	–	300	kHz
Band C Mixer (including IF amplifiers); measurements using hybrid; note 8						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz	–	9	11	dB
		f_i = 860 MHz	–	9	11	dB
Z_I	input impedance; ($R_s + L_s$)	f_i = 430 MHz; see Fig.9	–	34	–	Ω
		f_i = 860 MHz; see Fig.9	–	45	–	Ω
		f_i = 430 to 860 MHz; see Fig.9	–	9	–	nH
IP3	intermodulation using the 3 signal method	f_N = 430 MHz; note 1	–	–66	–60	dB
		f_N = 860 MHz; note 1	–	–66	–60	dB
V_i	input voltage	10 kHz pulling in channel; f_i = 860 MHz; note 2	83	87	–	dBμV
		N + 5 – 1 MHz pulling; f_i = 860 MHz; note 9	–	61	–	dBμV
G_v	voltage gain	f_i = 430 MHz; note 2	30	33	36	dB
		f_i = 860 MHz; note 2	30	33	36	dB

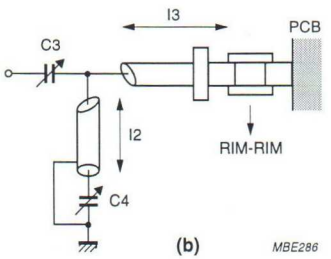
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	485	–	900	MHz
f_{shiift}	frequency shift	ΔV_P = ±5%; note 3	–	–	400	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 485 MHz; note 4	20	–	–	mV
$f_{ripple(p-p)}$	frequency ripple (peak-to-peak value)	from 20 Hz to 500 kHz; f_i = 900 MHz	10	–	–	mV
f_{drift}	frequency drift	without compensation; notes 5 and 6	–	–	2.5	MHz
		5 s to 15 min after switching on; without compensation; note 7	–	–	600	kHz
LO output						
Y_O	output admittance (G_P//C_P)	f_i = 80 MHz; see Fig.10	–	2.4	–	mS
		f_i = 80 MHz; see Fig.10	–	0.9	–	pF
		f_i = 900 MHz; see Fig.10	–	4.6	–	mS
		f_i = 900 MHz; see Fig.10	–	0.9	–	pF
V_o	output voltage	R_L = 50 Ω; T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	80	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; note 10	–	–	−10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω; T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	–	–	−10	dB

Notes

1. Cross modulation measurement is achieved using the 3 equal signals method (see Fig.4).
2. The gain is defined as the transducer gain (measured in Fig.8) plus the voltage transformation ratio of L7 to L8 (5:1, 15.4 dB).
3. The frequency shift is defined as a change in oscillator frequency for a variation of supply voltage. In one instance V_P = 5 to 4.75 V and in the other instance V_P = 5 to 5.25 V. In both cases, the frequency shift is below the specified value.
4. The frequency ripple susceptibility is measured at 500 kHz at the LO output (see Fig.5). The level of the ripple signal is increased until a difference of 53.5 dB is reached at the IF output.
5. The frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from T_{amb} = 25 °C to T_{amb} = 0 °C and on the other hand from T_{amb} = 25 °C to T_{amb} = 50 °C.
6. The capacitors in the oscillator circuits of Fig.8 are as follows:
   a) Band A: C1, C5 and C7.
   b) Band B: C4 and C9 and C11.
   c) Band C: C2, C3, C6, C8,and C10 are NP0 types.
7. Switching on drift is the change in oscillator frequency between 5 seconds and 15 minutes after switching on.
8. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.

9. The input level of a N + 5 – 1 MHz signal which gives a signal 30 dB below the oscillator carrier at the LO output.
10. Measured at 50 Ω with the following RF input voltages;
    a) RF voltage level = 120 dBμV at f_i < 180 MHz.
    b) RF voltage level = 107.5 dBμV at f_i = 180 to 225 MHz.
    c) RF voltage level = 97 dBμV at f_i = 225 to 860 MHz.





(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.

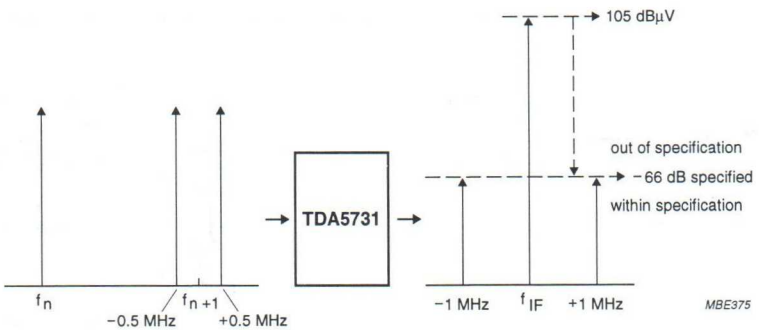


Fig.4 Cross modulation/incidental FM measurement.

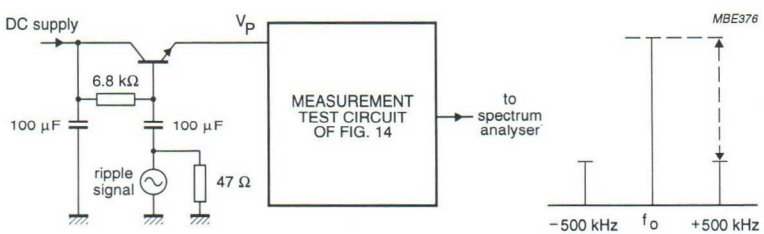


Fig.5 Ripple susceptibility measurement.

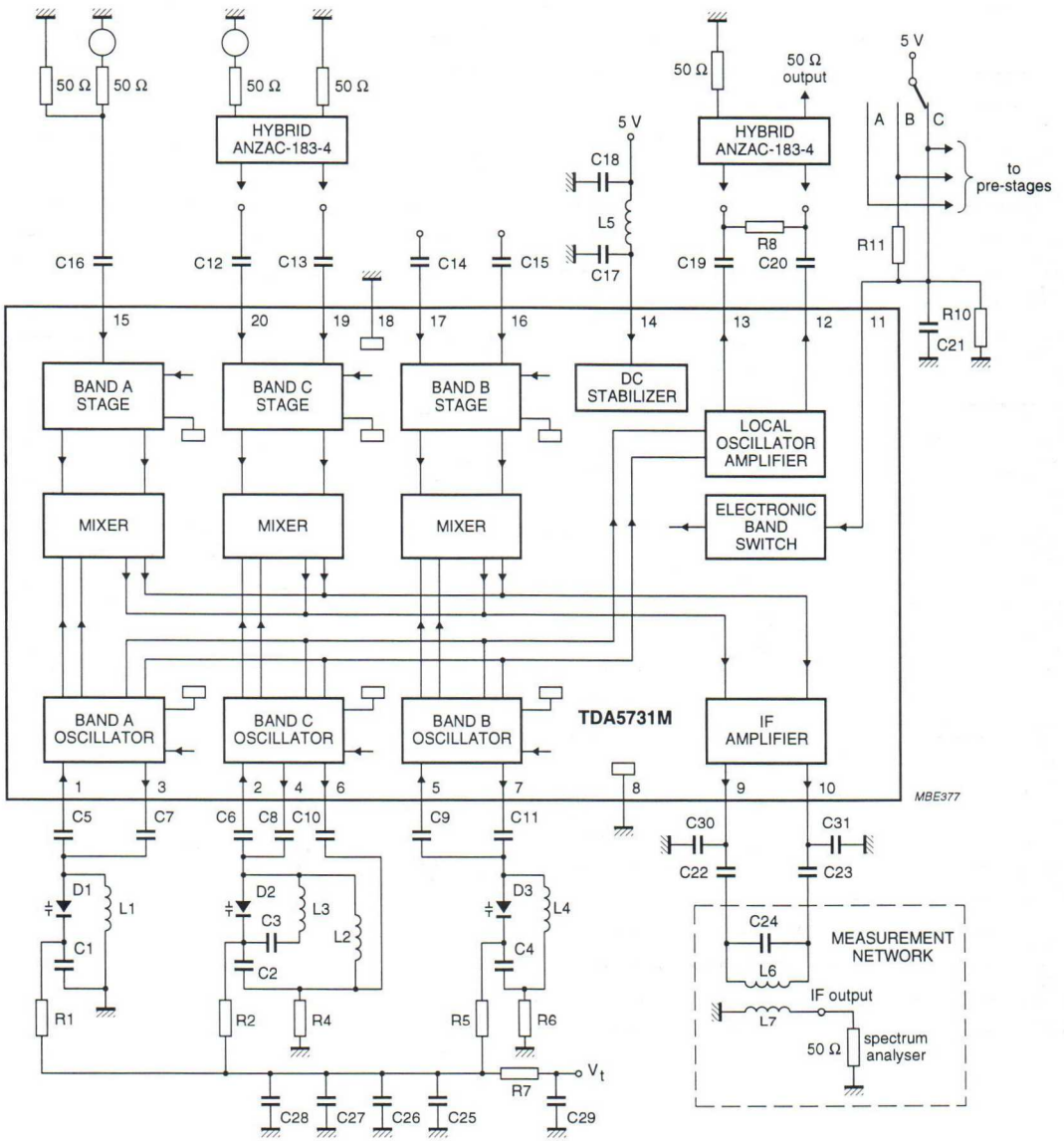


Fig.6 Reference measurement set-up.

Components values for Fig.8

Table 1 Capacitors (all SMD and NP0 except C28)

NUMBER	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	100 pF
C5	2.2 pF
C6	1 pF
C7	2.2 pF
C8	1 pF
C9	2.2 pF
C10	2.2 pF
C11	2.7 pF
C12	1 nF
C13	1 nF
C14	1 nF
C15	1 nF
C16	1 nF
C17	10 nF
C18	10 nF
C19	1 nF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	18 pF
C25	1 nF
C26	1 nF
C27	1 nF
C28	150 nF
C29	1 nF
C30	3 pF
C31	3 pF

Table 2 Resistors (all SMD)

NUMBER	VALUE
R1	47 kΩ
R2	24 kΩ
R4	24 kΩ
R5	47 kΩ
R6	15 Ω
R7	10 kΩ
R8	100 Ω
R10	15 kΩ
R11	27 kΩ

Table 3 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB133
Coils(1)	
L1	7.5 turns (3 mm)
L2	2.5 turns (3.5 mm)
L3	1.5 turns (2.5 mm)
L4	1.5 turns (4 mm)
L5	2.2 μH (choke coil)

Note

1. Wire size for L1 to L4 is 0.4 mm

Transformers (L6 = 2 × 5 turns and L7 = 2 turns))

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

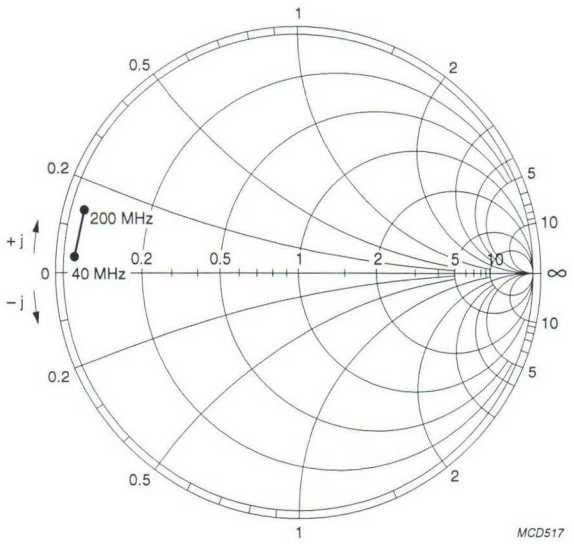


Fig.7 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

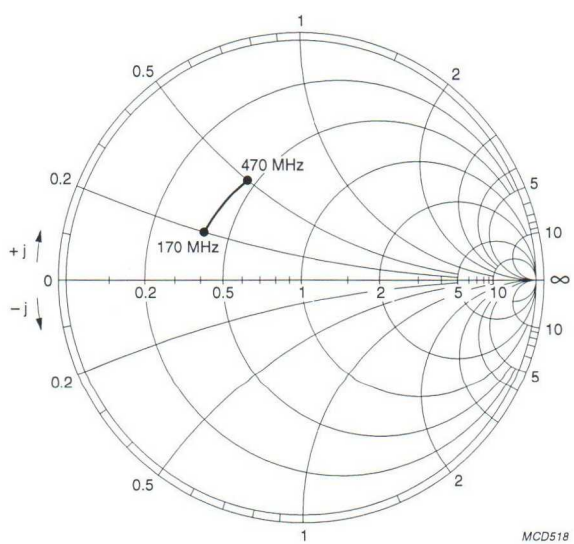


Fig.8 Input impedance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

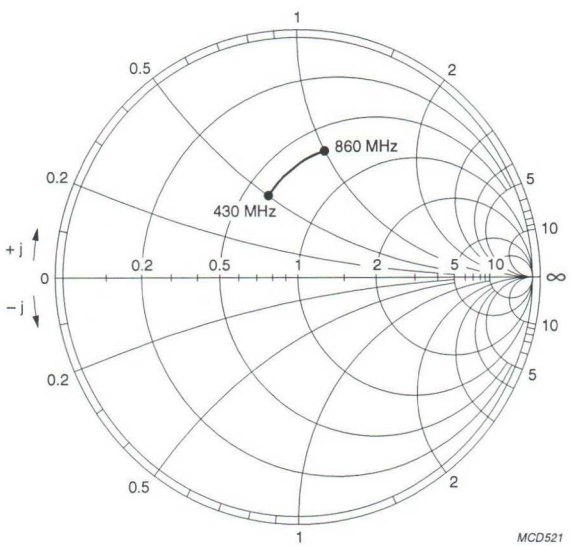


Fig.9 Input impedance (S_{11}) of the band C mixer input (460 to 880 MHz) (Z chart).

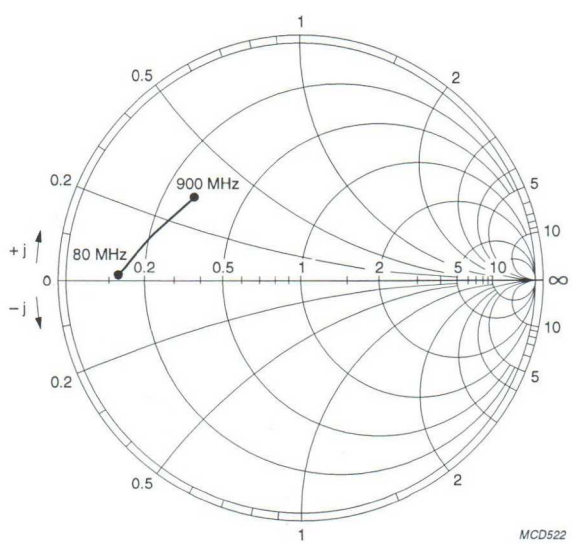


Fig.10 Output admittance (S_{22}) of the IF amplifier (80 to 900 MHz) (Y chart).

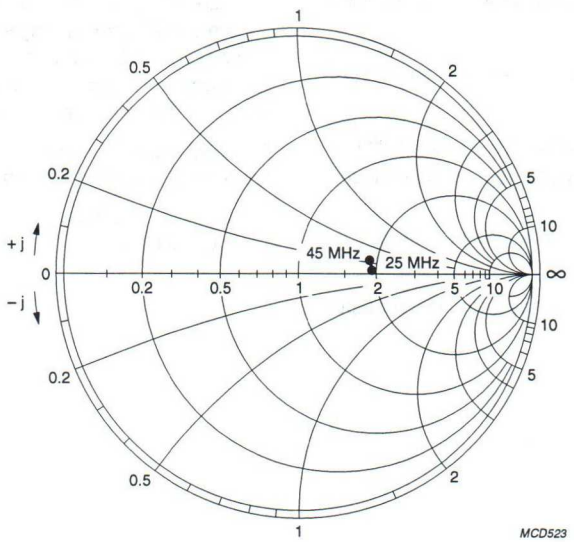


Fig.11 Output reflection coefficient (S_{22}) of the LO amplifier (25 to 45 MHz) (Z chart).

Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners

TDA5732M

FEATURES

- Balanced mixer with a common emitter input for band A
- 2-pin oscillator for band A
- Balanced mixer with a common base input for band C
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance of 75 Ω
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter connected between the mixer output and the IF amplifier input.

DESCRIPTION

The TDA5732M is a monolithic integrated circuit that performs VHF I, VHF III, hyperband and UHF mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 5 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 2-band tuner.

The tuner development time can be drastically reduced by using this device.

APPLICATIONS

- 2-band TV tuners
- 2-band VCR tuners.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	50	–	mA
f_R	frequency range	band A	55.25	–	361.25	MHz
		band C	367.25	–	801.25	MHz
N	noise figure	band A	–	9.5	–	dB
		band C	–	10	–	dB
V_o	IF output voltage	band A; R_L = 75 Ω; 1% cross-modulation	–	108	–	dBμV
		band C; R_L = 75 Ω 1% cross-modulation;	–	108	–	dBm
G_v	voltage gain	band A; R_L = 75 Ω	–	19	–	dB
		band C; R_L = 75 Ω	–	29	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5732M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

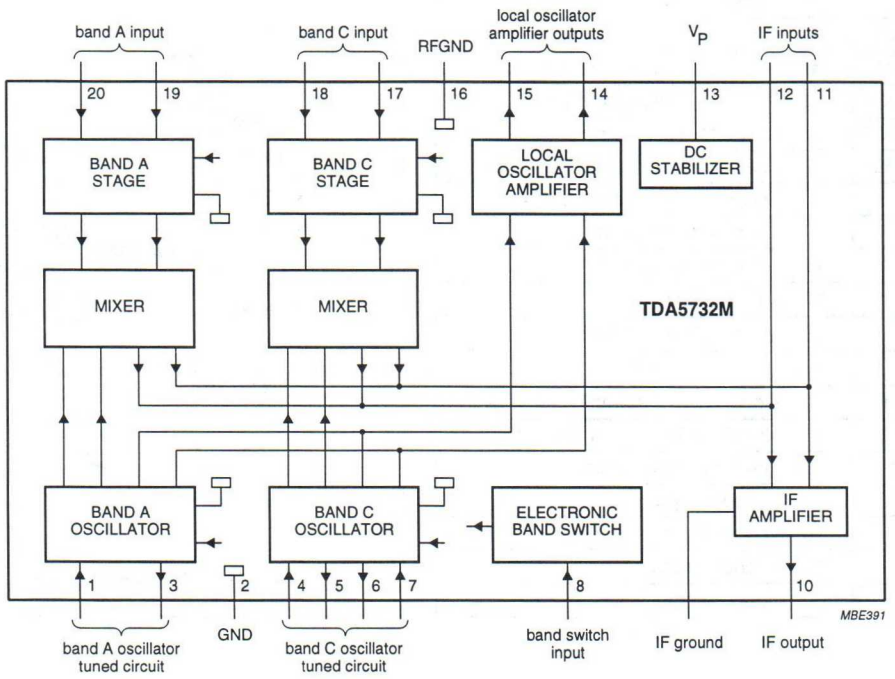


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AOSCIB	1	band A oscillator input base
GND	2	ground (0 V)
AOSCOC	3	band A oscillator output collector
COSCIB1	4	band C oscillator input base 1
COSCOC1	5	band C oscillator output collector 1
COSCOC2	6	band C oscillator output collector 2
COSCIB2	7	band C oscillator input base 2
BS	8	electronic band switch input
IFGND	9	ground for IF inputs
IFOUT	10	IF amplifier output
IFIN1	11	IF amplifier input 1
IFIN2	12	IF amplifier input 2
V_P	13	supply voltage
LOOUT1	14	local oscillator amplifier output 1
LOOUT2	15	local oscillator amplifier output 2
RFGND	16	ground for RF inputs
CIN1	17	band C input 1
CIN2	18	band C input 2
AIN1	19	band A input 1
AIN2	20	band A input 2

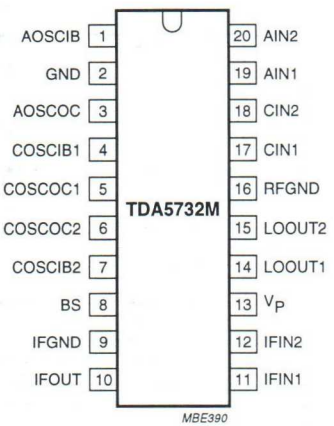


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+7.0	V
$V_{P(op)}$	operating supply voltage	4.5	5.5	V
$V_{n(max)}$	maximum voltage on each pin with a 22 kΩ resistor connected in series	–	35	V
V_{SW}	switching voltage	0	7.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−20	+85	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Human body model: the IC withstands 2000 V (except pins 17 and 18 which withstand 1000 V) in accordance with *UZW-BO-FQ-A302*; R = 1.5 kΩ; C = 100 pF.

Machine model: the IC withstands 200 V in accordance with *UZW-BO-FQ-B302*; R = 0 Ω; C = 200 pF.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; unless otherwise specified.

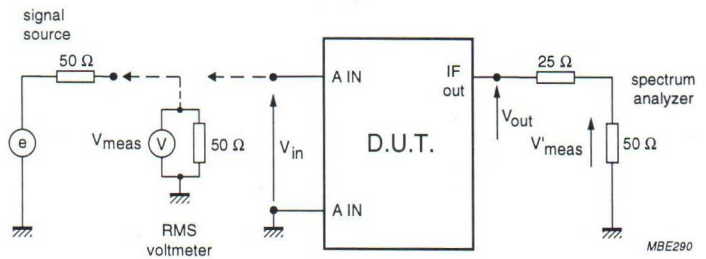
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	$I_{P(max)}$ measured at $V_{P(max)}$	–	50	64	mA
V_{SW}	switching voltage	band A	0	–	2.0	V
		band C	3.0	–	V_P	V
I_{SW}	switching current	band A; V_{SW} = 0 V	–	–	2	µA
		band C; V_{SW} = 5 V	–	4.5	10	µA
		$V_{P(max)}$	–	6	–	µA
IF amplifier						
S_{22}	output reflection coefficient	f_i = 43.5 MHz; see Fig.12	–	–13.1	–	dB
		f_i = 43.5 MHz; see Fig.12	–	2.9	–	deg
		f_i = 58.75 MHz; see Fig.12	–	–13.1	–	dB
		f_i = 58.75 MHz; see Fig.12	–	2.2	–	deg
Z_O	output impedance	f_i = 43.5 MHz; see Fig.12	–	78.4	–	Ω
		f_i = 43.5 MHz; see Fig.12	–	1.8	–	Ω
		f_i = 58.75 MHz; see Fig.12	–	78.4	–	Ω
		f_i = 58.75 MHz; see Fig.12	–	–1.4	–	Ω
SLO	visibility of the LO frequency at the IF output (worst case in the frequency range of band A and band C)	R_L = 75 Ω	–	85	–	dBµV
Band A mixer (including IF amplifier)						
f_R	frequency range	VHFI	55.25	–	127.25	MHz
		VHFIII	133.25	–	361.25	MHz
N_A	noise figure	f_i = 50 MHz; see Fig.7	–	8.5	9.5	dB
		f_i = 150 MHz; see Fig.7	–	8.5	10.5	dB
		f_i = 300 MHz; see Fig.7	–	9.5	12.5	dB
g_{os}	optimum source conductance	f_i = 50 MHz; see Fig.7	–	0.7	–	mS
		f_i = 150 MHz; see Fig.7	–	0.9	–	mS
		f_i = 300 MHz; see Fig.7	–	1.5	–	mS
Y_I	input admittance (G_P//C_P)	G_P; f_i = 55.25 MHz; see Fig.9	–	0.25	–	mS
		G_P; f_i = 361.25 MHz; see Fig.9	–	0.5	–	mS
		C_P; f_i = 55.25 to 361.25 MHz; see Fig.9	–	1.3	–	pF
$V_{oA(IF)}$	IF output voltage	1% cross modulation; in channel; f_i = 55.25 to 361.25 MHz; R_L = 75 Ω; wanted frequency sound carrier; unwanted frequency picture carrier; see Fig.5	105	108	–	dBµV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(RF)}$	RF input voltage	f_i = 173 MHz; note 1	–	91	–	dBμV
		f_i = 407 MHz; note 1	–	83	–	dBμV
$G_{v(A)}$	voltage gain at the channel centre	f_{IF} = 43.5 MHz; R_L = 75 Ω; see Fig.3	16.5	19	21.5	dB
Band A oscillator						
f_R	frequency range	VHFI	101	–	173	MHz
		VHFIII	179	–	407	MHz
f_{shift}	frequency shift (worst case in the frequency range)	ΔV_P = 5%; note 2	–	44	100	kHz
		ΔV_P = 10%; note 2	–	220	–	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of the supply voltage (peak-to-peak value	V_P = 4.75 to 5.25 V; f_i = 101 MHz; note 3	–	78	–	mV
		V_P = 4.75 to 5.25 V; f_i = 173 MHz; note 3	–	34	–	mV
		V_P = 4.75 to 5.25 V; f_i = 179 MHz; note 3	–	8.0	–	mV
		V_P = 4.75 to 5.25 V; f_i = 407 MHz; note 3	–	10	–	mV
f_{drift}	frequency drift (worst case in the frequency range)	ΔT = 25 °C with no compensation; NP0 capacitors; note 4	–	1800	2200	kHz
		5 s to 15 min after switch on; note 5	–	630	1100	kHz
Φ_N	phase noise, carrier-to-noise sideband (worst case in the frequency range)	±50 kHz; frequency offset; B = 3 kHz	–	60	–	dBc
Band C mixer (including IF amplifier)						
f_R	frequency range, picture carrier		367.25	–	801.25	MHz
N_C	noise figure (not corrected for image)	f_i = 367.25 MHz	–	9	11	dB
		f_i = 801.25 MHz	–	10	12	dB
Z_I	input impedance (R_s + L_s)	R_s; f_i = 367.25 MHz; see Fig.10	–	30	–	Ω
		L_s; f_i = 367.25 MHz; see Fig.10	–	9	–	nH
		R_s; f_i = 801.25 MHz; see Fig.10	–	38	–	Ω
		L_s; f_i = 801.25 MHz; see Fig.10	–	6	–	nH
$V_{oC(IF)}$	IF output voltage	1% cross modulation; in channel; f_i = 365.25 to 801.25 MHz; R_L = 75 Ω; wanted frequency sound carrier; unwanted frequency picture carrier; see Fig.6	105	108	–	dBμV
$V_{i(RF)}$	RF input voltage	f_i = 847 MHz; note 1	–	66	–	dBμV
$G_{v(C)}$	voltage gain	f_{IF} = 43.5 MHz; R_L = 75 Ω; see Fig.4	26	29	32	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range		413	–	847	MHz
f_{shift}	frequency shift	ΔV_P = 5%; note 2	–	46	200	kHz
		ΔV_P = 10%; note 2	–	200	–	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of the supply voltage (peak-to-peak value	V_P = 4.75 to 5.25 V; f_i = 413 MHz	–	203	–	mV
		V_P = 4.75 to 5.25 V; f_i = 847 MHz; note 3	–	22	–	mV
f_{drift}	frequency drift (worst case in the frequency range)	ΔT = 25 °C with compensation; note 4	–	1100	2500	kHz
		5 s to 15 min after switching on; note 5	–	300	1300	kHz
Φ_N	phase noise, carrier-to-noise sideband (worst case in the frequency range)	±50 kHz; frequency offset; B = 3 kHz	–	64	–	dBc
LO output						
Y_O	output admittance (G_P//C_P)	G_P; f_i = 101 MHz; see Fig.11	–	2.4	–	mS
		G_P; f_i = 847 MHz; see Fig.11	–	3.1	–	mS
		C_P; f_i = 101 to 847 MHz; see Fig.11	–	0.5	–	pF
V_O	output voltage	R_L = 50 Ω; V_P = 4.5 to 5.5 V; V_t = 0 to 28 V	83	90	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; note 6	–	–15	–10	dB
HLO	LO signal harmonics w.r.t. LO signal	R_L = 50 Ω	–	–10.5	–9.5	dB

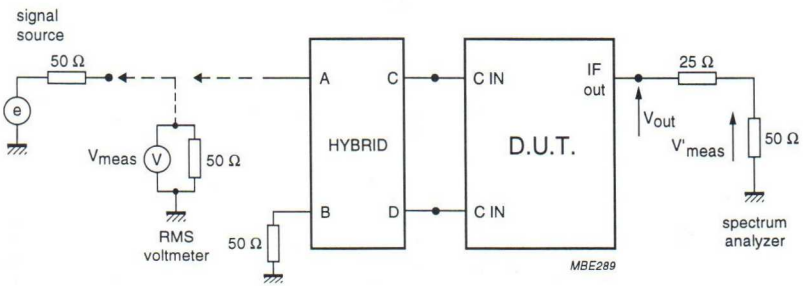
Notes

1. The RF signal is modulated with 50% AM at 15 kHz: The level of the RF signal is increased until there is a 23 dB difference between the LO carrier and the sideband components.
2. The frequency shift is defined as a variation in oscillator frequency when the supply voltage varies from V_P = 5 to 4.75 V or from V_P = 5 to 5.75 V.
3. The ripple susceptibility is measured for a 500 kHz ripple at the LO output with the set-up as illustrated in Fig.8. The level of the ripple signal is increased until there is a 53.5 dB difference between the LO carrier and the sideband components.
4. The frequency shift is defined as a variation in oscillator frequency when the supply voltage varies from T_{amb} = 25°C to 0°C or from T_{amb} = 25°C to 50°C.
5. The switching on drift is defined as the variation in oscillator frequency between 5 seconds and 15 minutes after switching on.
6. SRF: spurious signal on LO with respect to LO output signal;
   a) RF voltage level = 1 V at f_i = 55.25 to 225 MHz.
   b) RF level = 2.5 dBm at f_i = 225 to 361.25 MHz.
   c) RF level = –10 dBm at f_i = 367.25 to 801.25 MHz.



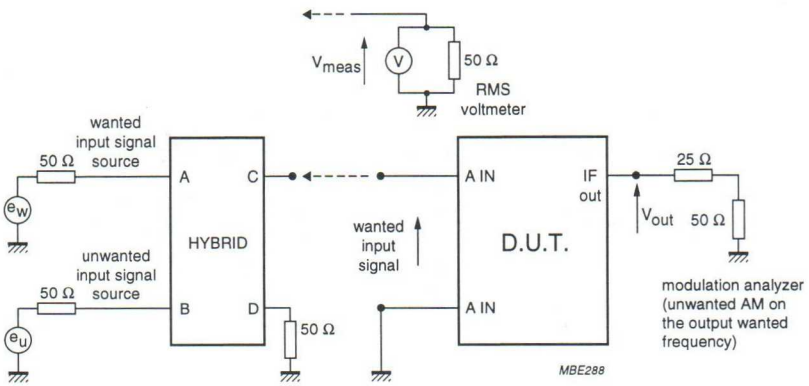
$Z_i >> 50\ \Omega \geq V_i = 2V_{meas}$; ($V_i$ = 80 dBμV); $V_o = V'_{meas} \times (50 + 25)/50$; voltage gain for band A = $20\log(V_o/V_i)$.

Fig.3 Band A gain measurement.



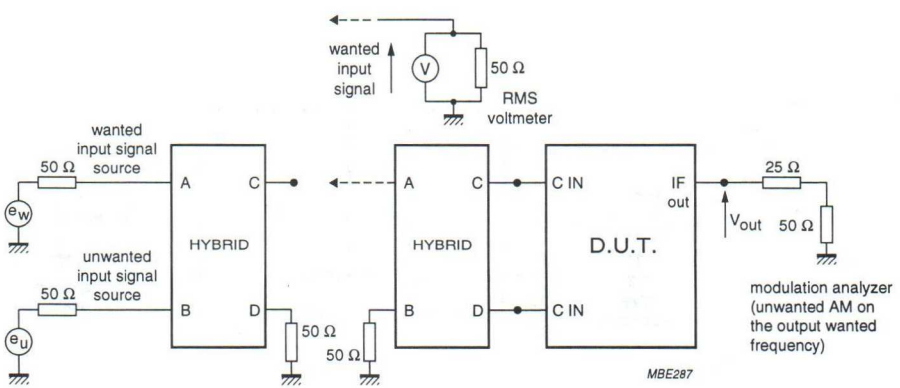
$V_i = V_{meas}$; (V_i = 70 dBμV); $V_o = V'_{meas} \times (50 + 25)/50$; voltage gain for band C = $20\log(V_o/V_i)$.

Fig.4 Band C gain measurement.



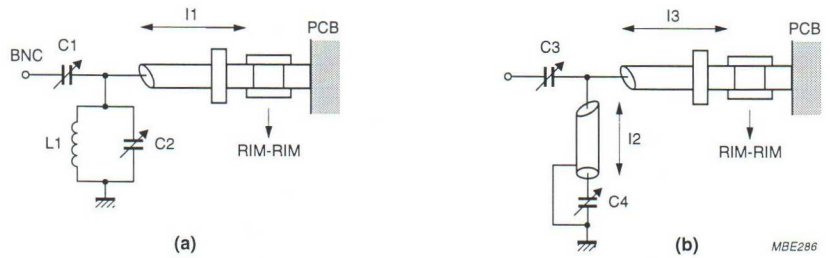
Wanted input signal = 80 dBμV; Zi >> 50 Ω ≥ wanted input signal = $2V_{meas}$; unwanted input signal modulated with 30% AM; $V_{oA(IF)}$ = unwanted output signalV_o when the output wanted signal is modulated with 0.3% AM.

Fig.5 Band A 1% cross-modulation.



Wanted input signal = 70 dBμV; unwanted input signal modulated with 30% AM; $V_{oA(IF)}$ = unwanted output signalV_o when the output wanted signal is modulated with 0.3% AM.

Fig.6 Band C 1% cross-modulation.



(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (5.5mm, wire diam. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.7 Input circuit for minimum noise figure.

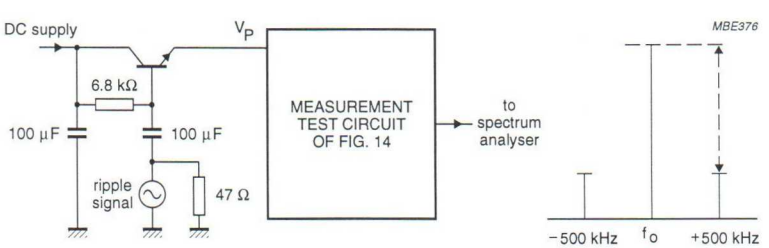


Fig.8 Measurement set-up for ripple measurement,

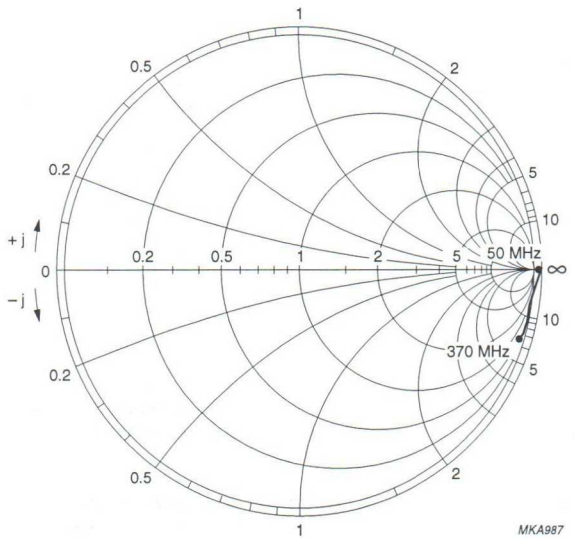


Fig.9 S_{11} on VHF mixer input (Z chart; Z_o = 50 Ω).

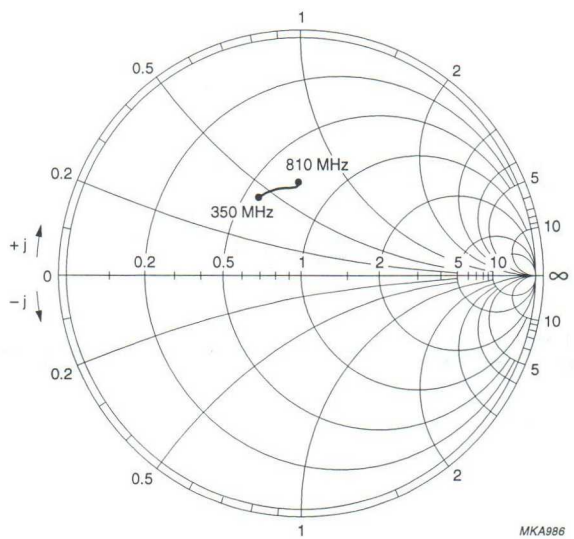


Fig.10 S_{11} on UHF mixer input (Z chart; Z_o = 50 Ω).

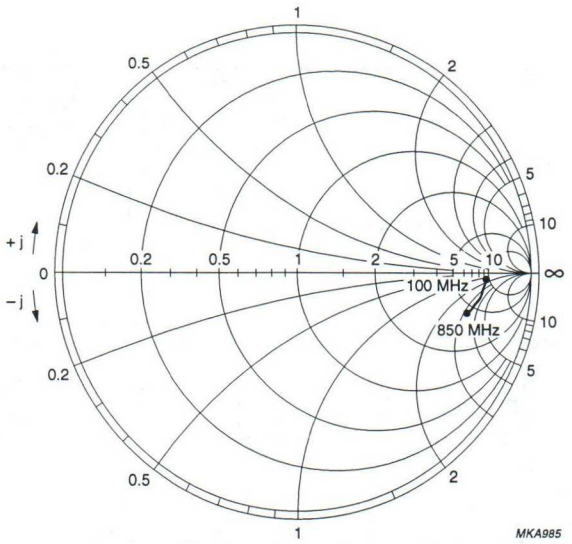


Fig.11 S_{22} on LO output (Z chart; Z_o = 50 Ω).

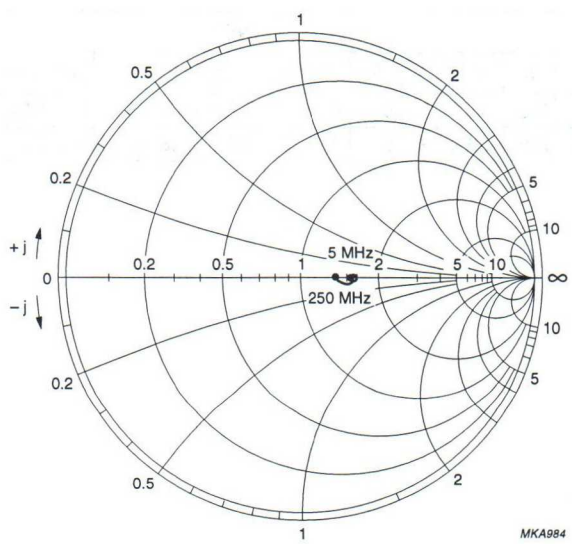


Fig.12 S_{22} on IFoutput (Z chart; Z_o = 50 Ω).

INTERNAL PIN CONFIGURATION

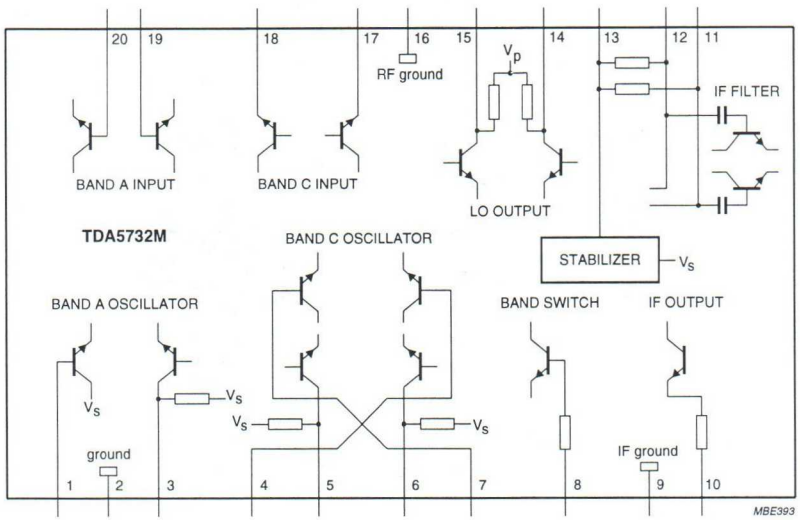


Fig.13 Internal pin configuration.

Table 1 Average DC voltage on pins

UHF/ VHF	PINS																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
VHF	1.8	0	3	-	3.6	3.6	–	0	0	2.1	3.6	3.6	5	4.2	4.2	0	–	–	1.8	1.8
UHF	–	0	3.6	1.9	2.9	2.9	1.9	5	0	2.1	3.6	3.6	5	4.2	4.2	0	1	1	–	–

APPLICATION INFORMATION

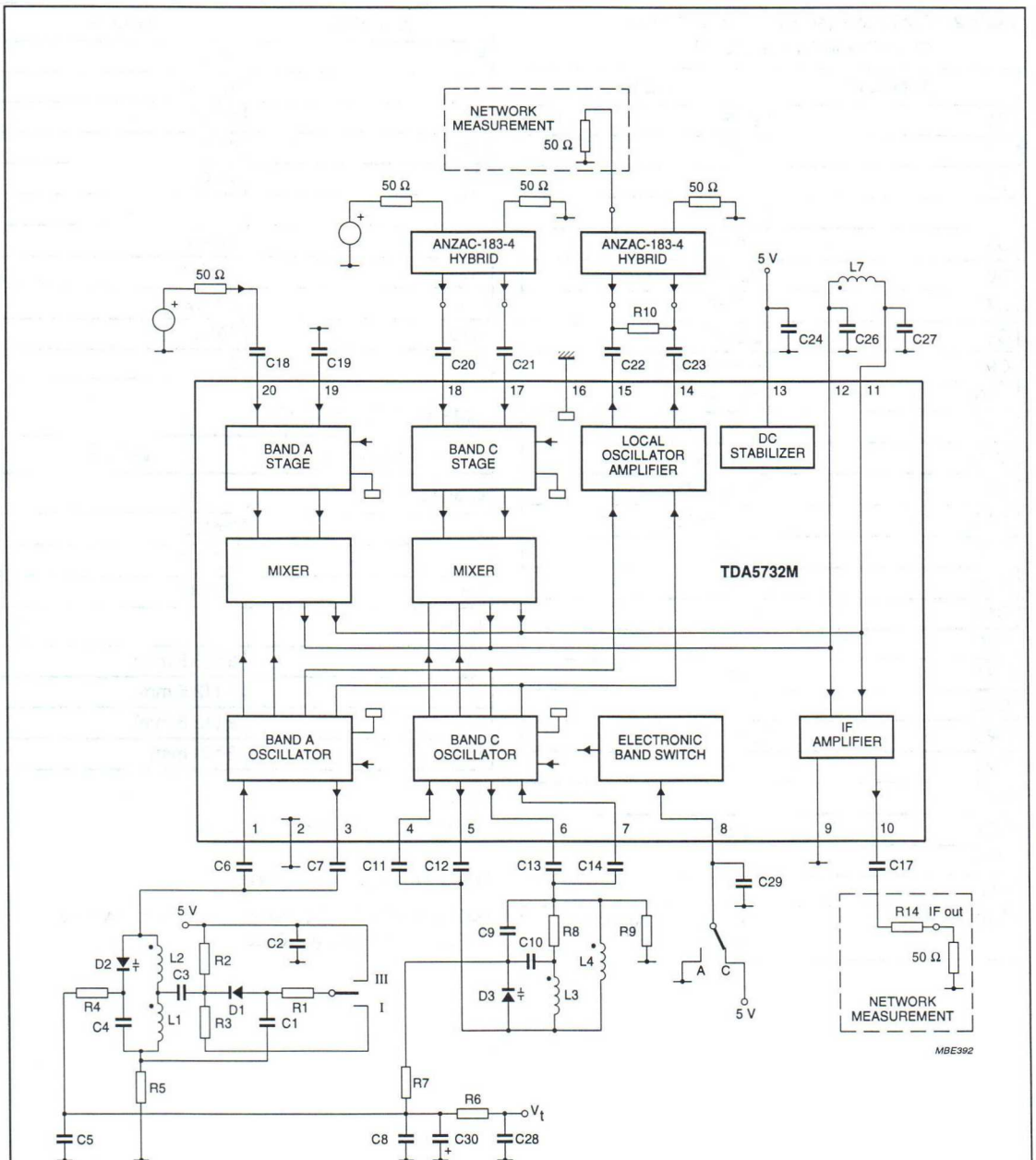


Fig.14 Measurement test circuit.

Application diagram components values

Table 2 Capacitors (all SMD and NP0 except C9 to C11 to C14 and C29)

NUMBER	VALUE
C1	1 nF
C2	1 nF
C3	1 nF
C4	82 pF
C5	2.2 nF
C6	2.2 nF
C7	1.5 pF
C8	2.2 nF
C9	6 pF (N750)
C10	100 pF
C11	1 pF (N1500)
C12	2 pF (N750)
C13	2 pF (N750)
C14	1 pF (N1500)
C17	1 nF
C18	1 nF
C19	1 nF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C26	15 pF
C27	15 pF
C28	2.2 nF
C29	1 nF
C30	1 µF (40 V electrolytic capacitor)

Table 3 Resistors (all SMD)

NUMBER	VALUE
R1	10 Ω
R2	12 kΩ
R3	2.7 kΩ
R4	47 kΩ
R5	10 Ω
R6	47 kΩ
R7	22 kΩ
R8	2.2 kΩ
R9	22 kΩ
R10	100 Ω
R14	27 Ω

Table 4 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BA792
D2	BB133
D3	BB134
Coils(1)	
L1	6 t (3.5 mm)
L2	3 t (2.5 mm)
L3	2 t (2.5 mm)
L4	3 t (3 mm)

Note

1. Wire size for L1 to L4 is 0.4 mm

Transformer (L7 = 2 turns)

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5736M

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- 3-pin oscillator for band B
- Balanced mixer with a common base input for band B and C (balanced input)
- 4-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Electronic band switch.

GENERAL DESCRIPTION

The TDA5736M is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 5 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

In addition, when hyperband is not required, the TDA5736M may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHFI and VHFIII in band A and the tuned circuit of band C for UHF.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	50	–	mA
f_R	frequency range	band A	42	–	180	MHz
		band B	160	–	470	MHz
		band C	430	–	860	MHz
N	noise figure	band A	–	7.5	–	dB
		band B	–	8.0	–	dB
		band C	–	9.0	–	dB
V_O	output voltage level of unwanted signal for 0.28% AM or 2.12 kHz ICFM	band A	–	109	–	dBμV
		band B	–	109	–	dBμV
		band C	–	109	–	dBμV
G_v	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	34	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5736M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

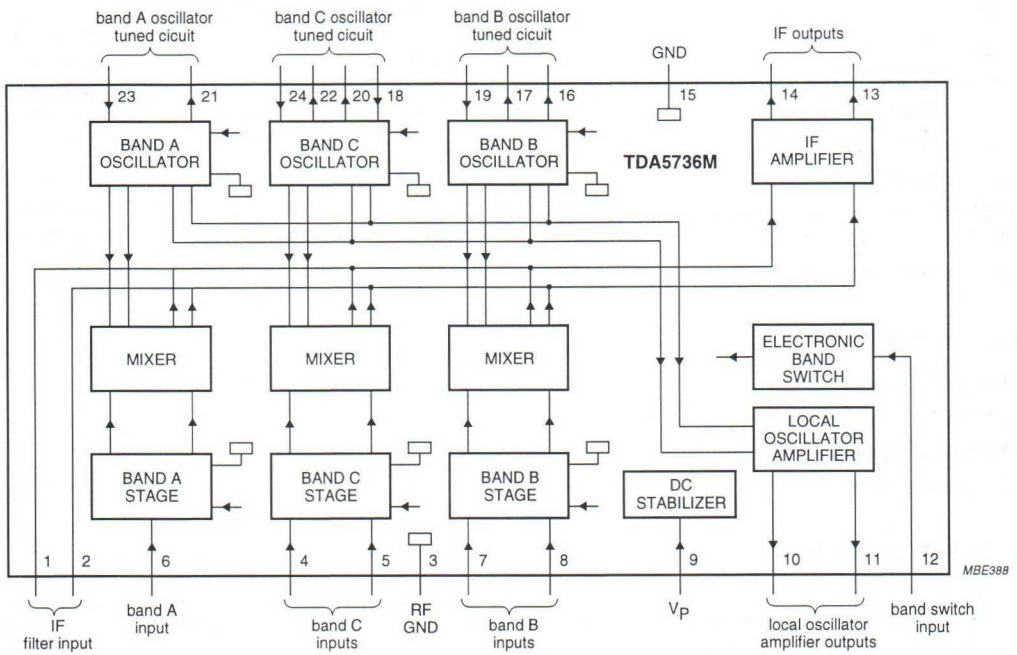


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IFIN1	1	IF filter input 1
IFIN2	2	IF filter input 2
RFGND	3	ground for RF input
CIN1	4	band C input 1
CIN2	5	band C input 2
AIN	6	band A input
BIN1	7	band B input 1
BIN2	8	band B input 2
V_P	9	supply voltage
LOOUT1	10	local oscillator amplifier output 1
LOOUT2	11	local oscillator amplifier output 2
BS	12	band switch input
IFOUT1	13	IF amplifier output 1
IFOUT2	14	IF amplifier output 2
GND	15	ground (0 V)
BOSCOC1	16	band B oscillator output collector 1
BOSCOC2	17	band B oscillator output collector 2
COSCIB1	18	band C oscillator input base 1
BOSCIB	19	band B oscillator input base
COSCOC1	20	band C oscillator output collector 1
AOSCOC	21	band A oscillator output collector
COSCOC2	22	band C oscillator output collector 2
AOSCIB	23	band A oscillator input base
COSCIB2	24	band C oscillator input base 2

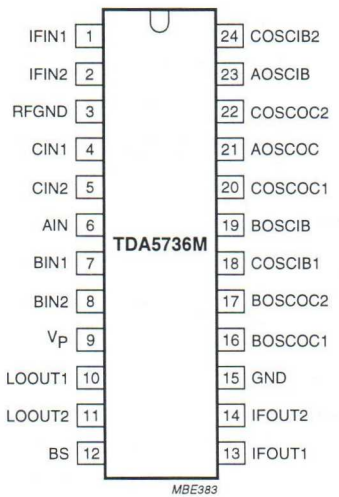


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX/	UNIT
V_P	supply voltage	−0.3	+7.0	V
$V_{SW(max)}$	maximum switching voltage	−0.3	+7.0	V
$V_{P(op)}$	operating supply voltage	4.5	5.5	V
$V_{n(max)}$	maximum voltage on each pin with a 22 kΩ resistor connected in series	–	35	V
I_O	output current of each pin to ground	–	−10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	–	10	s
T_{stg}	IC storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	118	K/W

HANDLING

Human Body Model: GND (15), RFGND (3), V_P (9) separately. Pins 16 and 17 withstand 1000 V in accordance with the *UZW-BO/FQ-A302*. All other pins withstand 2000 V in accordance with the *UZW-BO/FQ-A302*.

Machine Model: GND (15), RFGND (3), V_P (9) separately. Pins 16 and 17 withstand 100 V in accordance with the *UZW-BO/FQ-B302*. All other pins withstand 200 V in accordance with the *UZW-BO/FQ-B302*.

IF AMPLIFIER CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; differentialy measured at 36 MHz; measured in circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX.	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	note 1; see Fig.13	–	−16	12	–	dB/°C
Z_o	output impedance ($R_s + L_s$)	R_s	–	67		–	Ω
		L_s	–	20		–	nH
$V_{CM(LO)}$	common mode LO leakage at IF terminals including harmonics up to 1.75 GHz	band A; see Fig.8	–	–		75	dBμV
		band B; see Fig.8	–	–		75	dBμV
		band C; see Fig.8	–	–		70	dBμV

Note

1. All S parameters are referenced to a 50 Ω system.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		42	50	58	mA
V_{SW}	switching voltage (depending on supply voltage V_P)	band A	0	–	$0.18V_P$	V
		band B	$0.26V_P$	–	$0.47V_P$	V
		band C	$0.55V_P$	–	V_P	V
I_{SW}	switching current	band A	–	–	2	µA
		band B	–	–	10	µA
		band C	–	–	25	µA
Band A mixer (including IF amplifier)						
f_R	frequency range		42	–	180	MHz
N	noise figure	f_i = 50 MHz; see Fig.3	–	7.5	9	dB
		f_i = 180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for minimum noise figure	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1.1	–	mS
Y_I	input admittance (G_P//C_P)	f_i = 50 to 180 MHz; see Fig.9	–	0.3	–	mS
		f_i = 50 to 180 MHz; see Fig.9	–	1.9	–	pF
$V_{o(IF)}$	IF output voltage level for 0.28% AM or 2.12 kHz ICFM	f_N = 50 MHz; note 1	106	109	–	dBµV
		f_N = 180 MHz; note 1	106	109	–	dBµV
V_i	input voltage	10 kHz pulling in channel; f_i = 180 MHz	96	100	–	dBµV
OSC_{pull}	750 kHz oscillator pulling	f_i = 50 to 180 MHz; note 2	−10	–	–	dB
G_v	voltage gain	$20\log(V_{11\text{-}12}/V_{19})$; f_i = 50 MHz; note 3	20.5	23	25.5	dB
		$20\log(V_{11\text{-}12}/V_{19})$; f_i = 180 MHz; note 3	20.5	23	25.5	dB
NB	nearby breakthrough	f_i = 50 to 180 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 50 to 180 MHz; note 5	6	–	–	dB
SO2	2IF beat	note 6	–	–	−53	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band A oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	80	–	210	MHz
f_{shift}	frequency shift	ΔV_p = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 80 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
		f_i = 210 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8;	20	–	–	mV
f_{drift}	frequency drift	without compensation: notes 9 and 10	–	–	650	kHz
		with compensation: notes 9 and 11	–	–	500	kHz
		5 s to 15 min after switching on; without compensation: note 12	–	–	250	kHz
		5 s to 15 min after switching on; with compensation: note 12	–	–	120	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBµV	81	–	–	dBc/Hz
Band B mixer (including IF amplifier); measurements using hybrid; note 13						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz	–	8.0	10	dB
		f_i = 470 MHz	–	8.0	10	dB
Z_I	input impedance (R_s + L_s)	f_i = 160 to 470 MHz; see Fig.10	–	23	–	Ω
		f_i = 160 to 470 MHz; see Fig.10	–	9	–	nH
$V_{o(IF)}$	output voltage level of unwanted IF for 0.28% AM or 2.12 kHz ICFM	f_N = 170 MHz; note 1	106	109	–	dBµV
		f_N = 470 MHz; note 1	106	109	–	dBµV
V_i	input voltage	f_i = 470 MHz; 10 kHz pulling; in channel	83	87	–	dBµV
OSC_{pull}	750 kHz oscillator pulling	f_i = 170 to 470 MHz; note 2	−7	–	–	dB
G_v	voltage gain	f_i = 170 MHz; note 3	31	34	37	dB
		f_i = 470 MHz; note 3	31	34	37	dB
NB	nearby breakthrough	f_i = 170 to 470 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 170 to 470 MHz; note 5	5	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	205	–	490	MHz
f_{shift}	frequency shift	ΔV_P = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 205 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
		f_i = 490 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8;	20	–	–	mV
f_{drift}	frequency drift	without compensation; notes 9 and 10	–	–	2	MHz
		with compensation; notes 9 and 11	–	–	7.3	MHz
		5 s to 15 min after switching on; without compensation; note 12	–	–	750	kHz
		5 s to 15 min after switching on; with compensation; note 12	–	–	550	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBμV	81	–	–	dBc/Hz
Band C Mixer (including IF amplifiers); measurements using hybrid; note 13						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz	–	9	11	dB
		f_i = 860 MHz	–	9	11	dB
Z_I	input impedance; (R_s + L_s)	f_i = 430 to 860 MHz; see Fig.11	–	28	–	Ω
		f_i = 430 to 860 MHz; see Fig.11	–	10	–	nH
$V_{o(IF)}$	IF output voltage level for 0.28% AM or 2.12 kHz ICFM	f_N = 430 MHz; note 1	106	109	–	dBμV
		f_N = 860 MHz; note 1	106	109	–	dBμV
V_i	input voltage	10 kHz pulling in channel; f_i = 860 MHz	91	95	–	dBμV
OSC_{pull}	750 oscillator pulling	f_i = 430 to 860 MHz; note 2	−10	–	–	dB
G_v	voltage gain	f_i = 430 MHz; note 3	31	34	37	dB
		f_i = 860 MHz; note 3	31	34	37	dB
NB	nearby breakthrough	f_i = 430 to 860 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 430 to 860 MHz; note 5	1	–	–	dB

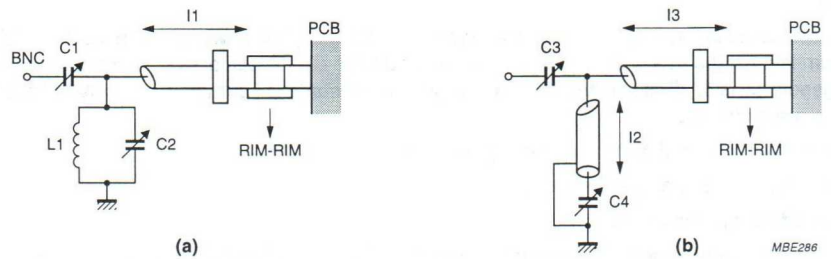
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	485	–	900	MHz
f_{shiift}	frequency shift	ΔV_P = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 485 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
		f_i = 900 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	18	–	–	mV
f_{drift}	frequency drift	without compensation; notes 9 and 10	–	–	2.8	MHz
		with compensation; notes 9 and 11	–	–	1.9	MHz
		5 s to 15 min after switching on; without compensation; note 12	–	–	700	kHz
		5 s to 15 min after switching on; with compensation; note 12	–	–	450	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBμV	81	–	–	dBc/Hz
LO output						
Y_O	output admittance (G_P//C_P)	f_i = 80 MHz; see Fig.12	–	2.5	–	mS
		f_i = 900 MHz; see Fig.12	–	5	–	mS
		f_i = 80 to 900 MHz; see Fig.12	–	0.9	–	pF
V_o	output voltage	R_L = 50 Ω; V_{tune} = 0 to 35 V T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	80	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; V_{tune} = 0.2 to 35 V; T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; note 14	–	–	−10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω; V_{tune} = 0 to 35 V T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	–	–	−10	dB

Notes

1. Cross modulation/incidental FM: Unwanted IF output voltage level causing 0.28% cross modulation or 2.12 kHz ICFM (whichever is more severe) in all bands in any channel. The conditions are as follows:
   a) The actual measurement is achieved using the 3 equal signals method (see Fig.5).
   b) The 3 input levels are increased until a difference of 66 dB is reached at the output. The output level is recorded (0.28% cross modulation for 109 dBμV at the output is equivalent to a difference of 66 dB for 105 dBμV at the output using the 3 equal signals method).
2. 750 kHz oscillator pulling: The requirement is that the mixer input can accept an unwanted signal at $f_W + f_{IF}$ − 750 kHz with a level higher than the level of the wanted signal (band A = −10 dB, band B = −7 dB and band C = −10 dB) when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier. In any channel and any band. The condition is that the interfering frequency is adjusted such that the sideband is at 750 kHz from the wanted IF. If two sidebands appear then the highest of both sidebands is recorded.

3. The gain is defined as the transducer gain (measured in Fig.8) plus the voltage transformation ratio of L7 to L8 (5:1, 15.4 dB).
4. Nearby breakthrough: the requirements are that the mixer accept an unwanted signal in the range (N ±2) ±2 MHz with a minimum level of 15 dB above the wanted signal when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier (see Fig.4). The conditions are as follows:
   a) Measured on the test board using two signal generators.
   b) The wanted IF output signal is 105 dBμV.
   c) Tuned to any frequency in bands A, B or C.
   d) An interfering frequency is adjusted such that interference is 57 dB down and 750 kHz away from the wanted IF. If two sidebands appear (pulling) then the highest is taken. The unwanted mixer input is referenced to the wanted signal level.
5. N + ½IF susceptibility: the requirement is that the mixer input can accept an unwanted signal at $f_W + \frac{1}{2}f_{IF} - 375$ kHz with a minimum level of (band A = 6 dB, band B = –5 dB and band C = –1 dB) above the wanted signal when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier. In any channel and in any band. The conditions are as follows:
   a) Measured on the test board using two signal generators.
   b) The wanted IF output signal is 105 dBμV.
   c) Tuned to any frequency in bands A, B or C.
   d) If two sidebands appear (pulling) then the highest is taken. The unwanted mixer input, referenced to the wanted signal level is recorded.
6. 2IF beat: 2 × IF beat < –53 dB (see Fig.6). The conditions are as follows:
   a) Measured on the test board at the IF output.
   b) Tuned to band A; $f_W \approx 77.8$ MHz, $f_{osc} = 116.7$ MHz, $f_{IF} = 38.9$ MHz; f_W level at the IF output = 105 dBμV (the second harmonic of the generator > 63 dB down). The 2 × IF beat is measured at 100 kHz distance < –53 dB with respect to the wanted signal.
7. The frequency shift is defined as a change in oscillator frequency for a variation of supply voltage. In one instance $V_P = 5$ to 4.75 V and in the other instance $V_P = 5$ to 5.25 V. In both cases, the frequency shift is below the specified value.
8. The frequency ripple susceptibility is measured at 500 kHz at the LO output (see Fig.7). The level of the ripple signal is increased until a difference of 53.5 dB is reached at the LO output.
9. The frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from $T_{amb} = 25$ °C to $T_{amb} = 0$ °C and on the other hand from $T_{amb} = 25$ °C to $T_{amb} = 50$ °C.
10. The capacitors in the oscillator circuits of Fig.8 are as follows:
    a) Band A: C1, C6 and C8 are NP0 types.
    b) Band B: C4 and C11 to C13 are NP0 types.
    c) Band C: C2, C3, C5, C7, C9 and C10 are NP0 types.
11. The capacitors in the oscillator circuits of Fig.8 have the following temperature coefficients:
    a) Band A: C6 and C8 are N750 types.
    b) Band B: C4 and C11 to C13 are N750 types.
    c) Band C: C7 to C9 are type N750, C2, C5 and C10 are type N470 types.

12. Switching on drift is the change in oscillator frequency between 5 seconds and 15 minutes after switching on.
13. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
14. Measured at 50 Ω with the following RF input voltages;
    a) RF voltage level = 120 dBμV at f_i < 180 MHz.
    b) RF voltage level = 107.5 dBμV at f_i = 180 to 225 MHz.
    c) RF voltage level = 97 dBμV at f_i = 225 to 860 MHz.



(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.

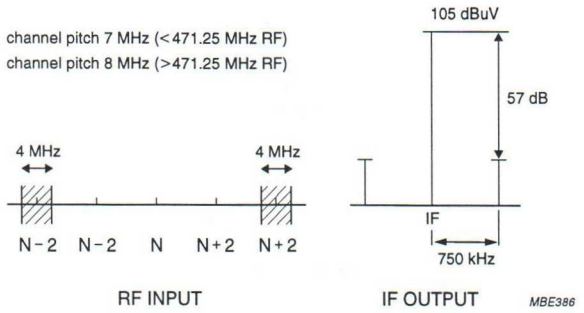


Fig.4 Nearby breakthrough measurement.

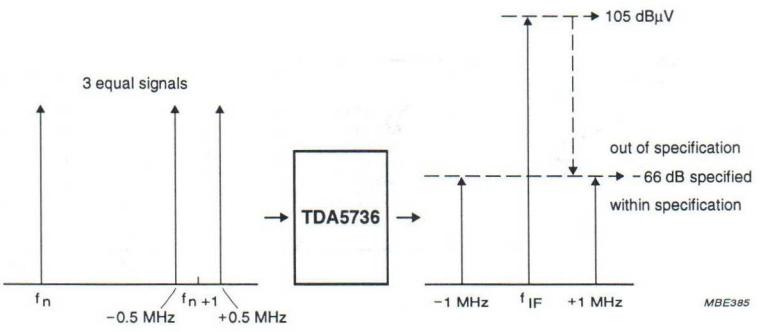


Fig.5 Cross modulation/incidental FM measurement.

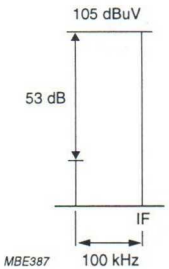


Fig.6 IF beat measurement.

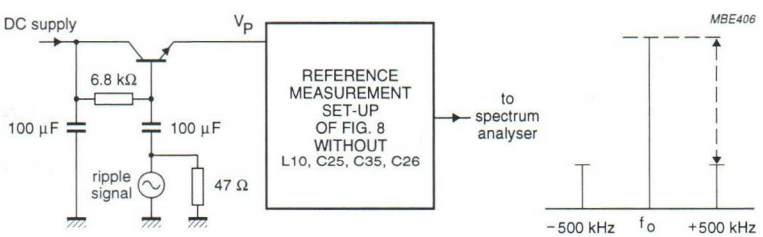


Fig.7 Ripple susceptibility measurement.

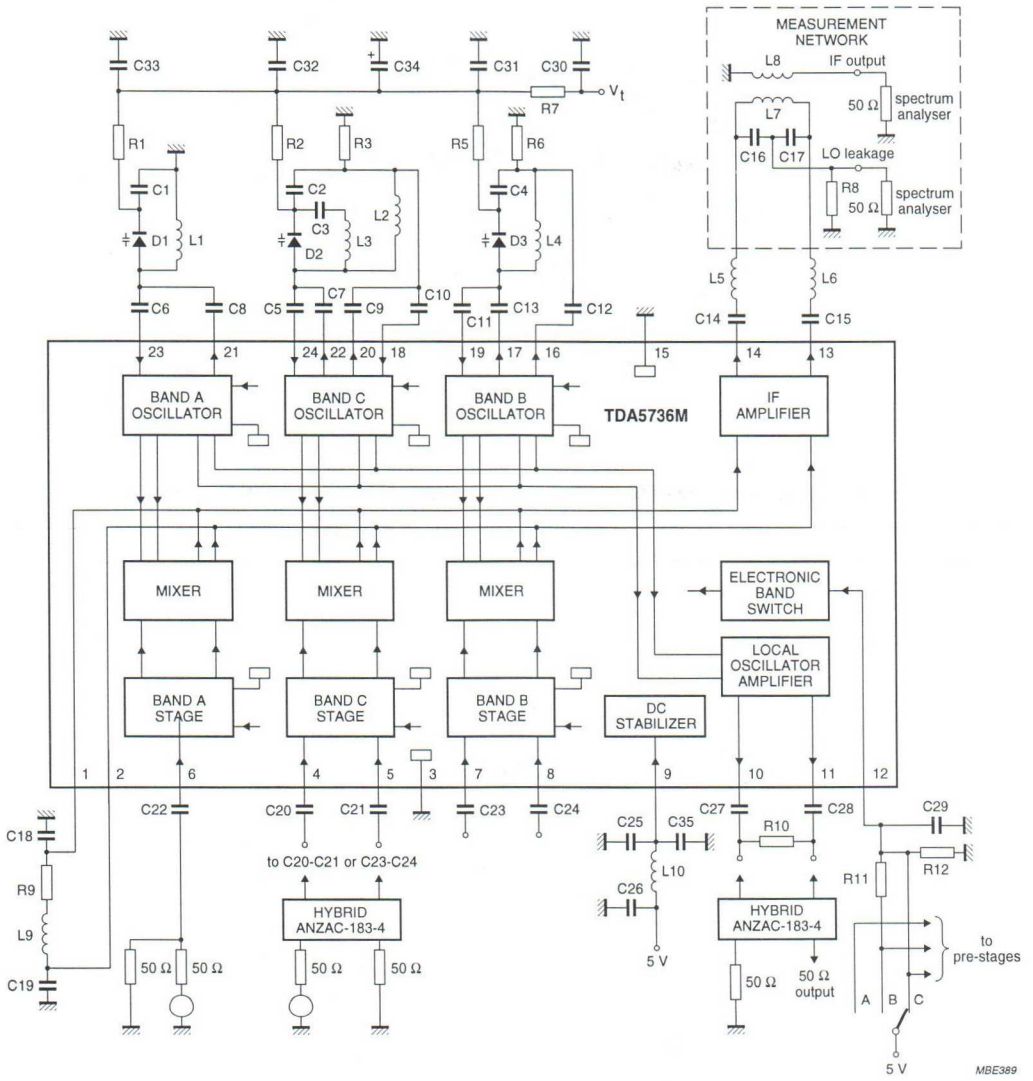


Fig.8 Reference measurement set-up.

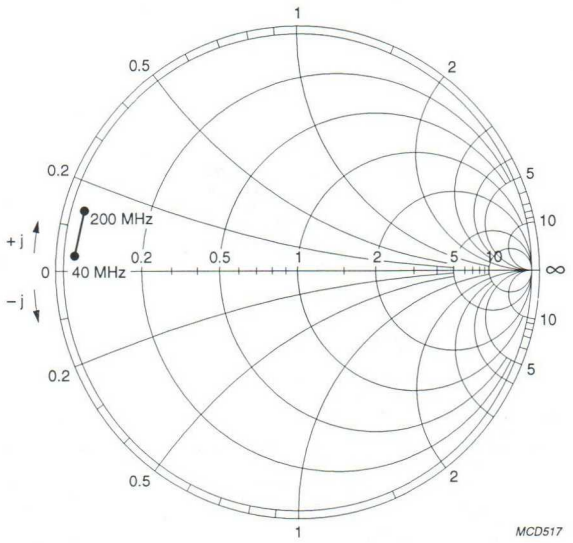


Fig.9 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

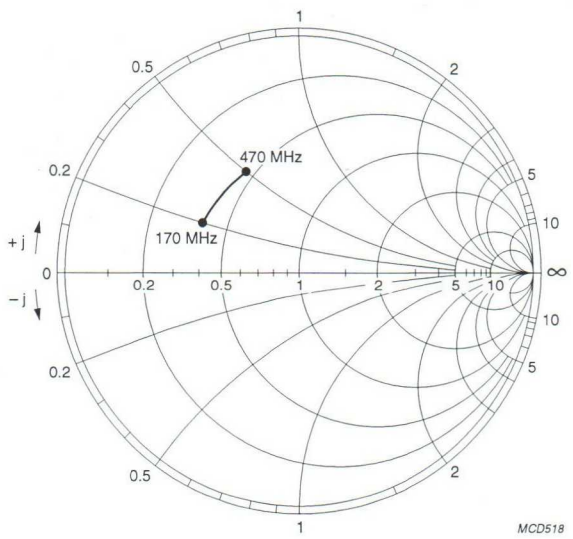


Fig.10 Input impedance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

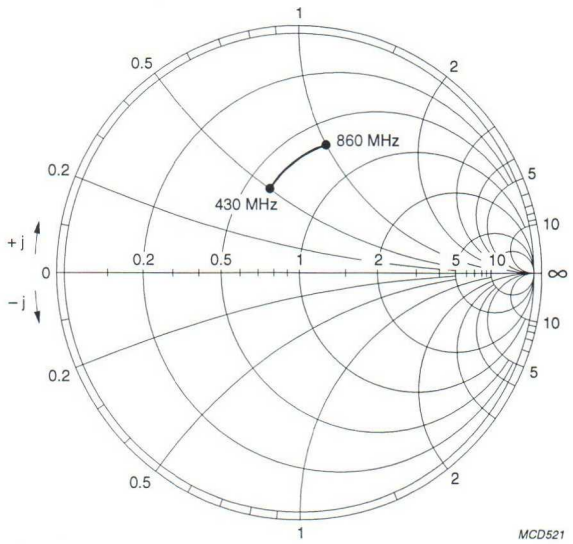


Fig.11 Input impedance (S_{11}) of the band C mixer input (460 to 880 MHz) (Z chart).

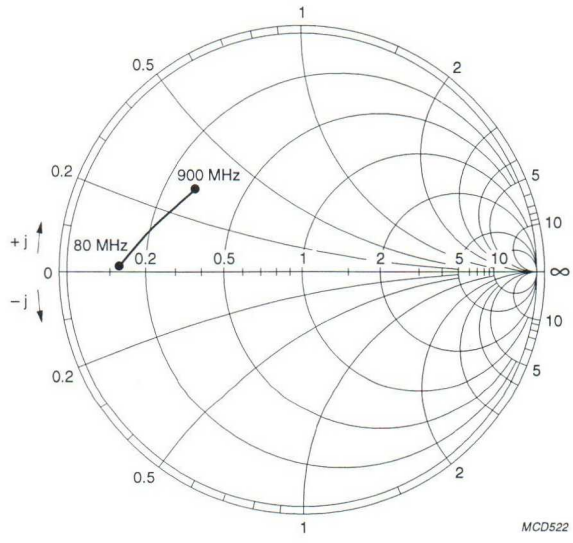


Fig.12 Output reflection coefficient (S_{22}) of the IF amplifier (80 to 900 MHz) (Y chart).

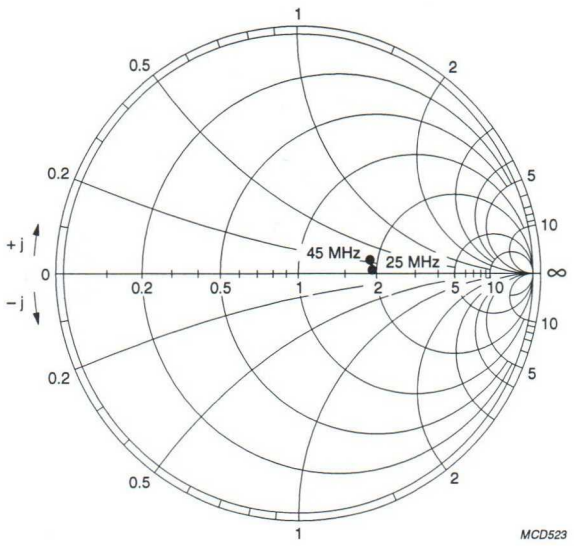


Fig.13 Output reflection coefficient (S_{22}) of the LO amplifier (25 to 45 MHz) (Z chart).

INTERNAL PIN CONFIGURATION

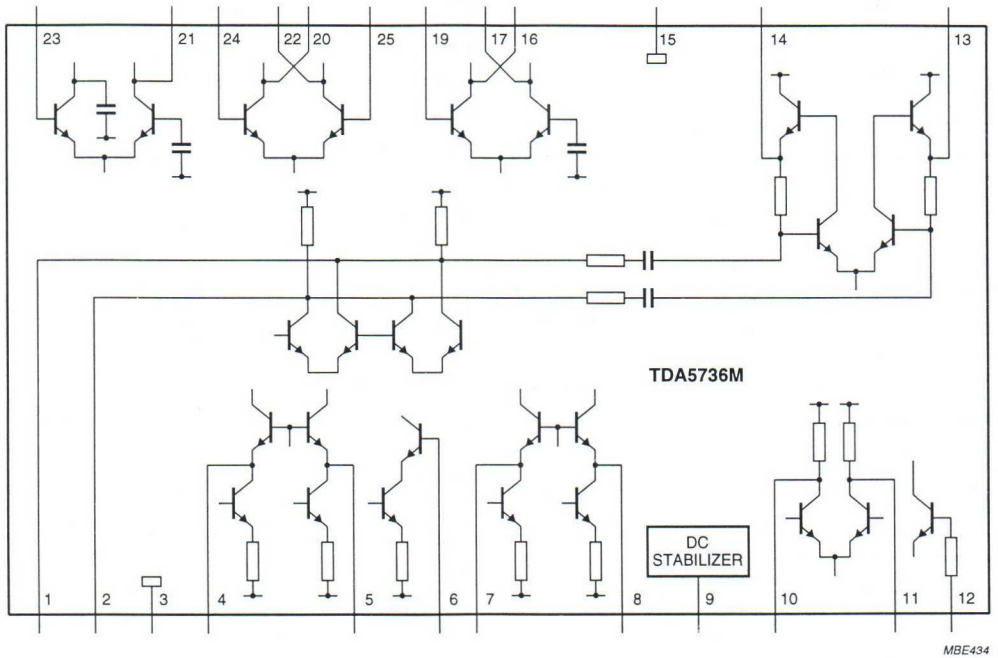


Fig.14 Internal pin configuration.

APPLICATION INFORMATION

Components values for Fig.8

Table 1 Capacitors (all SMD and NP0 except C34 and C35)

NUMBER	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	82 pF
C5	1 pF
C6	2 pF
C7	2 pF
C8	2 pF
C9	2 pF
C10	1 pF
C11	3.3 pF
C12	3.3 pF
C13	4.7 pF
C14	1 nF
C15	1 nF
C16	39 pF
C17	39 pF
C18	68 pF
C19	68 pF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C25	2.2 nF
C26	1 nF
C27	1 nF
C28	1 nF
C29	1 nF
C30	1 nF
C31	1 nF
C32	1 nF
C33	1 nF
C34	2.2 µF
C35	4.7 nF

Table 2 Resistors (all SMD)

NUMBER	VALUE
R1	47 kΩ
R2	22 kΩ
R3	22 kΩ
R5	27 kΩ
R6	27 kΩ
R7	10 kΩ
R8	50 Ω
R9	4.7 Ω
R10	100 Ω
R11	27 kΩ
R12	15 kΩ

Table 3 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB133
Coils(1)	
L1	7.5 turns (3 mm)
L2	2.5 turns (3.5 mm)
L3	1.5 turns (2.5 mm)
L4	2.5 turns (3 mm)
L5	5.5 turns (2.5 mm)
L6	5.5 turns (2.5 mm)
L9	12.5 turns (5 mm)
L10	2.2 µH (choke coil)

Note

1. Wire size for L1 to L6 is 0.4 mm

Transformers (L7 = 2 × 5 turns and L8 = 2 turns))

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5737M

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- 3-pin oscillator for band B
- Balanced mixer with a common base input for band B and C (balanced input)
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Electronic band switch.

GENERAL DESCRIPTION

The TDA5737M is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This low power mixer/oscillator circuit requires a power supply of 5 V and is available in a very small package outline. This device gives the designer the capability to design an economical and physically small 3-band tuner. The tuner development time can be drastically reduced by using this device.

In addition, when hyperband is not required, the TDA5737M may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHFI and VHFIII in band A and the tuned circuit of band C for UHF.

APPLICATIONS

- 3-band TV tuners
- 3-band TV front-ends
- 3-band VCR tuners
- 3-band VCR front-ends.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	50	–	mA
f_R	frequency range	band A	42	–	180	MHz
		band B	160	–	470	MHz
		band C	430	–	860	MHz
N	noise figure	band A	–	7.5	–	dB
		band B	–	8.0	–	dB
		band C	–	9.0	–	dB
V_O	output voltage level of unwanted signal for 0.28% AM or 2.12 kHz ICFM	band A	–	109	–	dBμV
		band B	–	109	–	dBμV
		band C	–	109	–	dBμV
G_v	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	34	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5737M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5737M

BLOCK DIAGRAM

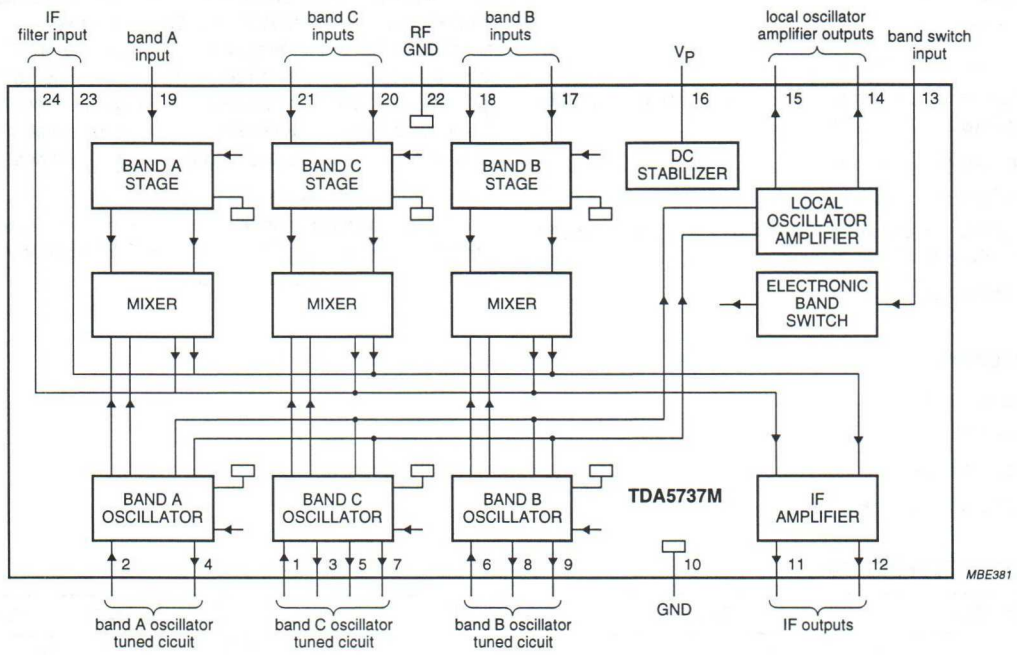


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
COSCIB1	1	band C oscillator input base 1
AOSCIB	2	band A oscillator input base
COSCOC1	3	band C oscillator output collector 1
AOSCOC	4	band A oscillator output collector
COSCOC2	5	band C oscillator output collector 2
BOSCIB	6	band B oscillator input base
COSCIB2	7	band C oscillator input base 2
BOSCOC1	8	band B oscillator output collector 1
BOSCOC2	9	band B oscillator output collector 2
GND	10	ground (0 V)
IFOUT1	11	IF amplifier output 1
IFOUT2	12	IF amplifier output 2
BS	13	band switch input
LOOUT1	14	local oscillator amplifier output 1
LOOUT2	15	local oscillator amplifier output 2
V_P	16	supply voltage
BIN1	17	band B input 1
BIN2	18	band B input 2
AIN	19	band A input
CIN1	20	band C input 1
CIN2	21	band C input 2
RFGND	22	ground for RF input
IFIN1	23	IF filter input 1
IFIN2	24	IF filter input 2

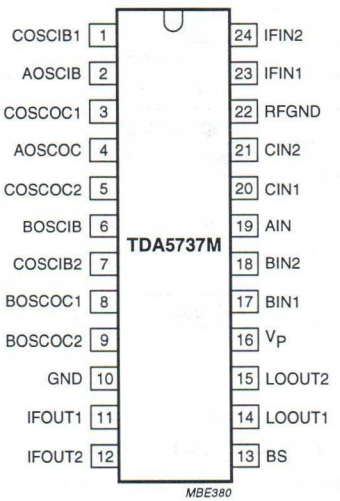


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX/	UNIT
V_P	supply voltage	−0.3	+7.0	V
$V_{SW(max)}$	maximum switching voltage	−0.3	+7.0	V
$V_{P(op)}$	operating supply voltage	4.5	5.5	V
$V_{n(max)}$	maximum voltage on each pin with a 22 kΩ resistor connected in series	–	35	V
I_O	output current of each pin to ground	–	−10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	–	10	s
T_{stg}	IC storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C
T_j	junction temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	118	K/W

HANDLING

Human Body Model: GND (10), RFGND (22), V_P (16) separately. Pins 8 and 9 withstand 1000 V in accordance with the *UZW-BO/FQ-A302*. All other pins withstand 2000 V in accordance with the *UZW-BO/FQ-A302*.

Machine Model: GND (10)), RFGND (22), V_P (16) separately. Pins 8 and 9 withstand 100 V in accordance with the *UZW-BO/FQ-B302*. All other pins withstand 200 V in accordance with the *UZW-BO/FQ-B302*.

IF AMPLIFIER CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; differentialy measured at 36 MHz; measured in circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX.	UNIT
				MOD.	PHASE		
S_{22}	output reflection coefficient	note 1; see Fig.13	–	−16	12	–	dB/°C
Z_o	output impedance (R_s + L_s)	R_s	–	67		–	Ω
		L_s	–	20		–	nH
$V_{CM(LO)}$	common mode LO leakage at IF terminals including harmonics up to 1.75 GHz	band A; see Fig.8	–	–		75	dBμV
		band B; see Fig.8	–	–		75	dBμV
		band C; see Fig.8	–	–		70	dBμV

Note

1. All S parameters are referenced to a 50 Ω system.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		42	50	58	mA
V_{SW}	switching voltage (depending on supply voltage V_P)	band A	0	–	$0.18V_P$	V
		band B	$0.26V_P$	–	$0.47V_P$	V
		band C	$0.55V_P$	–	V_P	V
I_{SW}	switching current	band A	–	–	2	μA
		band B	–	–	10	μA
		band C	–	–	25	μA
Band A mixer (including IF amplifier)						
f_R	frequency range		42	–	180	MHz
N	noise figure	f_i = 50 MHz; see Fig.3	–	7.5	9	dB
		f_i = 180 MHz; see Fig.3	–	9	10	dB
g_{os}	optimum source conductance for minimum noise figure	f_i = 50 MHz	–	0.5	–	mS
		f_i = 180 MHz	–	1.1	–	mS
Y_I	input admittance (G_P//C_P)	f_i = 50 to 180 MHz; see Fig.9	–	0.3	–	mS
		f_i = 50 to 180 MHz; see Fig.9	–	1.9	–	pF
$V_{o(IF)}$	IF output voltage level for 0.28% AM or 2.12 kHz ICFM	f_N = 50 MHz; note 1	106	109	–	dBμV
		f_N = 180 MHz; note 1	106	109	–	dBμV
V_i	input voltage	10 kHz pulling in channel; f_i = 180 MHz	96	100	–	dBμV
OSC_{pull}	750 kHz oscillator pulling	f_i = 50 to 180 MHz; note 2	−10	–	–	dB
G_v	voltage gain	$20\log(V_{11\text{-}12}/V_{19})$; f_i = 50 MHz; note 3	20.5	23	25.5	dB
		$20\log(V_{11\text{-}12}/V_{19})$; f_i = 180 MHz; note 3	20.5	23	25.5	dB
NB	nearby breakthrough	f_i = 50 to 180 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 50 to 180 MHz; note 5	6	–	–	dB
SO2	2IF beat	note 6	–	–	−53	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band A oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	80	–	210	MHz
f_{shift}	frequency shift	ΔV_p = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 80 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
		f_i = 210 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
f_{drift}	frequency drift	without compensation: notes 9 and 10	–	–	650	kHz
		with compensation: notes 9 and 11	–	–	500	kHz
		5 s to 15 min after switching on; without compensation: note 12	–	–	850	kHz
		5 s to 15 min after switching on; with compensation: note 12	–	–	120	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBμV	81	–	–	dBc/Hz
Band B mixer (including IF amplifier); measurements using hybrid; note 13						
f_R	frequency range		160	–	470	MHz
N	noise figure (not corrected for image)	f_i = 170 MHz	–	8.0	10	dB
		f_i = 470 MHz	–	8.0	10	dB
Z_I	input impedance (R_s + L_s)	f_i = 160 to 470 MHz; see Fig.10	–	23	–	Ω
		f_i = 160 to 470 MHz; see Fig.10	–	9	–	nH
$V_{o(IF)}$	output voltage level of unwanted IF for 0.28% AM or 2.12 kHz ICFM	f_N = 170 MHz; note 1	106	109	–	dBμV
		f_N = 470 MHz; note 1	106	109	–	dBμV
V_i	input voltage	f_i = 470 MHz; 10 kHz pulling; in channel	83	87	–	dBμV
OSC_{pull}	750 kHz oscillator pulling	f_i = 170 to 470 MHz; note 2	−7	–	–	dB
G_v	voltage gain	f_i = 170 MHz; note 3	31	34	37	dB
		f_i = 470 MHz; note 3	31	34	37	dB
NB	nearby breakthrough	f_i = 170 to 470 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 170 to 470 MHz; note 5	5	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	205	–	490	MHz
f_{shift}	frequency shift	ΔV_P = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 205 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
		f_i = 490 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
f_{drift}	frequency drift	without compensation; notes 9 and 10	–	–	2	MHz
		with compensation; notes 9 and 11	–	–	1.3	MHz
		5 s to 15 min after switching on; without compensation; note 12	–	–	750	kHz
		5 s to 15 min after switching on; with compensation; note 12	–	–	550	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBμV	81	–	–	dBc/Hz
Band C Mixer (including IF amplifiers); measurements using hybrid; note 13						
f_R	frequency range		430	–	860	MHz
N	noise figure (not corrected for image)	f_i = 430 MHz	–	9	11	dB
		f_i = 860 MHz	–	9	11	dB
Z_I	input impedance; (R_s + L_s)	f_i = 430 to 860 MHz; see Fig.11	–	28	–	Ω
		f_i = 430 to 860 MHz; see Fig.11	–	10	–	nH
$V_{o(IF)}$	IF output voltage level for 0.28% AM or 2.12 kHz ICFM	f_N = 430 MHz; note 1	106	109	–	dBμV
		f_N = 860 MHz; note 1	106	109	–	dBμV
V_i	input voltage	10 kHz pulling in channel; f_i = 860 MHz	91	95	–	dBμV
OSC_{pull}	750 kHz oscillator pulling	f_i = 430 to 860 MHz; note 2	−10	–	–	dB
G_v	voltage gain	f_i = 430 MHz; note 3	31	34	37	dB
		f_i = 860 MHz; note 3	31	34	37	dB
NB	nearby breakthrough	f_i = 430 to 860 MHz; note 4	15	–	–	dB
χ	N + ½IF susceptibility	f_i = 430 to 860 MHz; note 5	1	–	–	dB

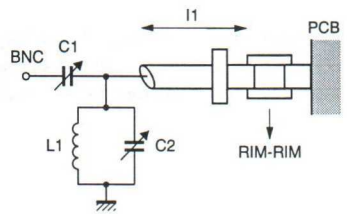
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C oscillator						
f_R	frequency range	T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; V_{tune} = 0.45 to 28 V	485	–	900	MHz
f_{shiift}	frequency shift	ΔV_P = ±5%; note 7	–	–	53	kHz
$\chi_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	f_i = 485 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	20	–	–	mV
$f_{ripple(p-p)}$	frequency ripple (peak-to-peak value)	f_i = 900 MHz; V_P = 4.75 to 5.25 V; f_{ripple} = 20 Hz to 500 kHz; note 8	18	–	–	mV
f_{drift}	frequency drift	without compensation; notes 9 and 10	–	–	2.8	MHz
		with compensation; notes 9 and 11	–	–	1.9	MHz
		5 s to 15 min after switching on; without compensation; note 12	–	–	700	kHz
		5 s to 15 min after switching on; with compensation; note 12	–	–	450	kHz
Φ_N	phase noise	10 kHz offset; IF output = 105 dBμV	81	–	–	dBc/Hz
LO output						
Y_O	output admittance (G_P//C_P)	f_i = 80 MHz; see Fig.12	–	2.5	–	mS
		f_i = 900 MHz; see Fig.12	–	5	–	mS
		f_i = 80 to 900 MHz; see Fig.12	–	0.9	–	pF
V_o	output voltage	R_L = 50 Ω; V_{tune} = 0 to 35 V T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	80	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; V_{tune} = 0.2 to 35 V; T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V; note 14	–	–	−10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω; V_{tune} = 0 to 35 V T_{amb} = −10 to +80 °C; V_P = 4.5 to 5.5 V;	–	–	−10	dB

Notes

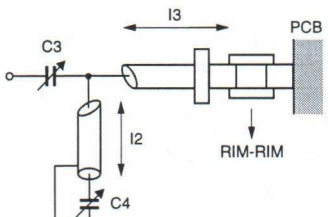
1. Cross modulation/incidental FM: Unwanted IF output voltage level causing 0.28% cross modulation or 2.12 kHz ICFM (whichever is more severe) in all bands in any channel. The conditions are as follows:
   a) The actual measurement is achieved using the 3 equal signals method (see Fig.5).
   b) The 3 input levels are increased until a difference of 66 dB is reached at the output. The output level is recorded (0.28% cross modulation for 109 dBμV at the output is equivalent to a difference of 66 dB for 105 dBμV at the output using the 3 equal signals method).
2. 750 kHz oscillator pulling: The requirement is that the mixer input can accept an unwanted signal at $f_W + f_{IF}$ − 750 kHz with a level higher than the level of the wanted signal (band A = −10 dB, band B = −7 dB and band C = −10 dB) when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier. In any channel and any band. The condition is that the interfering frequency is adjusted such that the sideband is at 750 kHz from the wanted IF. If two sidebands appear then the highest of both sidebands is recorded.

3. The gain is defined as the transducer gain (measured in Fig.8) plus the voltage transformation ratio of L7 to L8 (5:1, 15.4 dB).
4. Nearby breakthrough: the requirements are that the mixer accept an unwanted signal in the range (N ±2) ±2 MHz with a minimum level of 15 dB above the wanted signal when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier (see Fig.4). The conditions are as follows:
   a) Measured on the test board using two signal generators.
   b) The wanted IF output signal is 105 dBμV.
   c) Tuned to any frequency in bands A, B or C.
   d) An interfering frequency is adjusted such that interference is 57 dB down and 750 kHz away from the wanted IF. If two sidebands appear (pulling) then the highest is taken. The unwanted mixer input is referenced to the wanted signal level.
5. N + ½IF susceptibility: the requirement is that the mixer input can accept an unwanted signal at $f_W + \frac{1}{2}f_{IF} - 375$ kHz with a minimum level of (band A = 6 dB, band B = –5 dB and band C = –1 dB) above the wanted signal when the disturbance generated is 57 dB down and 750 kHz away from the wanted IF carrier. In any channel and in any band. The conditions are as follows:
   a) Measured on the test board using two signal generators.
   b) The wanted IF output signal is 105 dBμV.
   c) Tuned to any frequency in bands A, B or C.
   d) If two sidebands appear (pulling) then the highest is taken. The unwanted mixer input, referenced to the wanted signal level is recorded.
6. 2IF beat: 2 × IF beat < –53 dB (see Fig.6). The conditions are as follows:
   a) Measured on the test board at the IF output.
   b) Tuned to band A; $f_W \approx 77.8$ MHz, $f_{osc} = 116.7$ MHz, $f_{IF} = 38.9$ MHz; f_W level at the IF output = 105 dBμV (the second harmonic of the generator > 63 dB down). The 2 × IF beat is measured at 100 kHz distance < –53 dB with respect to the wanted signal.
7. The frequency shift is defined as a change in oscillator frequency for a variation of supply voltage. In one instance $V_P = 5$ to 4.75 V and in the other instance $V_P = 5$ to 5.25 V. In both cases, the frequency shift is below the specified value.
8. The frequency ripple susceptibility is measured at 500 kHz at the LO output (see Fig.7). The level of the ripple signal is increased until a difference of 53.5 dB is reached at the LO output.
9. The frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from $T_{amb} = 25$ °C to $T_{amb} = 0$ °C and on the other hand from $T_{amb} = 25$ °C to $T_{amb} = 50$ °C.
10. The capacitors in the oscillator circuits of Fig.8 are as follows:
    a) Band A: C1, C6 and C8 are NP0 types.
    b) Band B: C4 and C11 to C13 are NP0 types.
    c) Band C: C2, C3, C5, C7, C9 and C10 are NP0 types.
11. The capacitors in the oscillator circuits of Fig.8 have the following temperature coefficients:
    a) Band A: C6 and C8 are N750 types.
    b) Band B: C4 and C11 to C13 are N750 types.
    c) Band C: C7 to C9 are type N750, C2, C5 and C10 are type N470.

12. Switching on drift is the change in oscillator frequency between 5 seconds and 15 minutes after switching on.
13. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
14. Measured at 50 Ω with the following RF input voltages;
    a) RF voltage level = 120 dBμV at f_i < 180 MHz.
    b) RF voltage level = 107.5 dBμV at f_i = 180 to 225 MHz.
    c) RF voltage level = 97 dBμV at f_i = 225 to 860 MHz.



(a)



(b) MBE286

(a) For f_R = 50 MHz:
mixer A frequency response measured = 57 MHz, loss = 0 dB
image suppression = 16 dB
C1 = 9 pF
C2 = 15 pF
L1 = 7 turns (Δ 5.5 mm, wire dia. = 0.5 mm)
l1 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω, 96 pF/m).

(b) For f_R = 180 MHz:
mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB
image suppression = 13 dB
C3 = 5 pF
C4 = 25 pF
l2 = rigid cable (RIM): 30 cm long
l3 = rigid cable (RIM): 5 cm long
(rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.3 Input circuit for optimum noise figure.

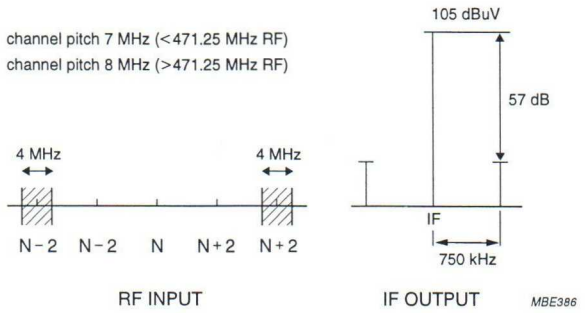


Fig.4 Nearby breakthrough measurement.

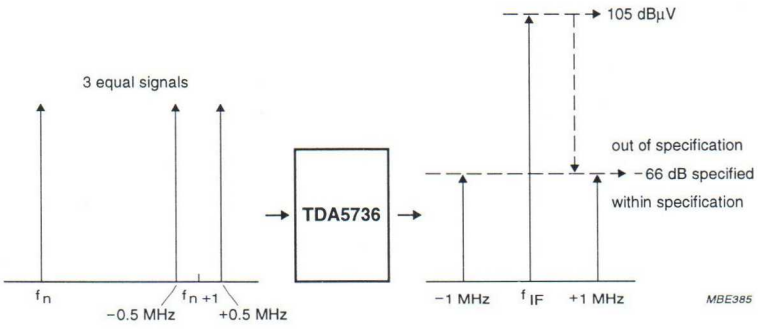


Fig.5 Cross modulation/incidental FM measurement.

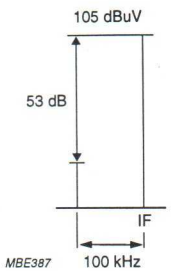


Fig.6 IF beat measurement.

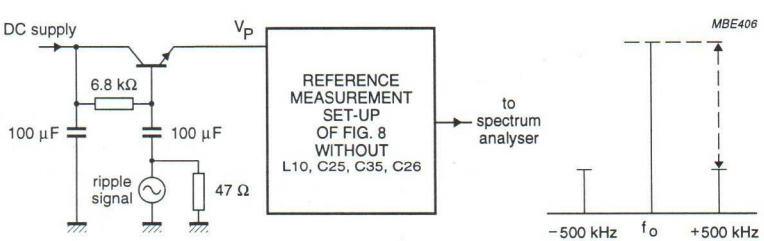


Fig.7 Ripple susceptibility measurement.

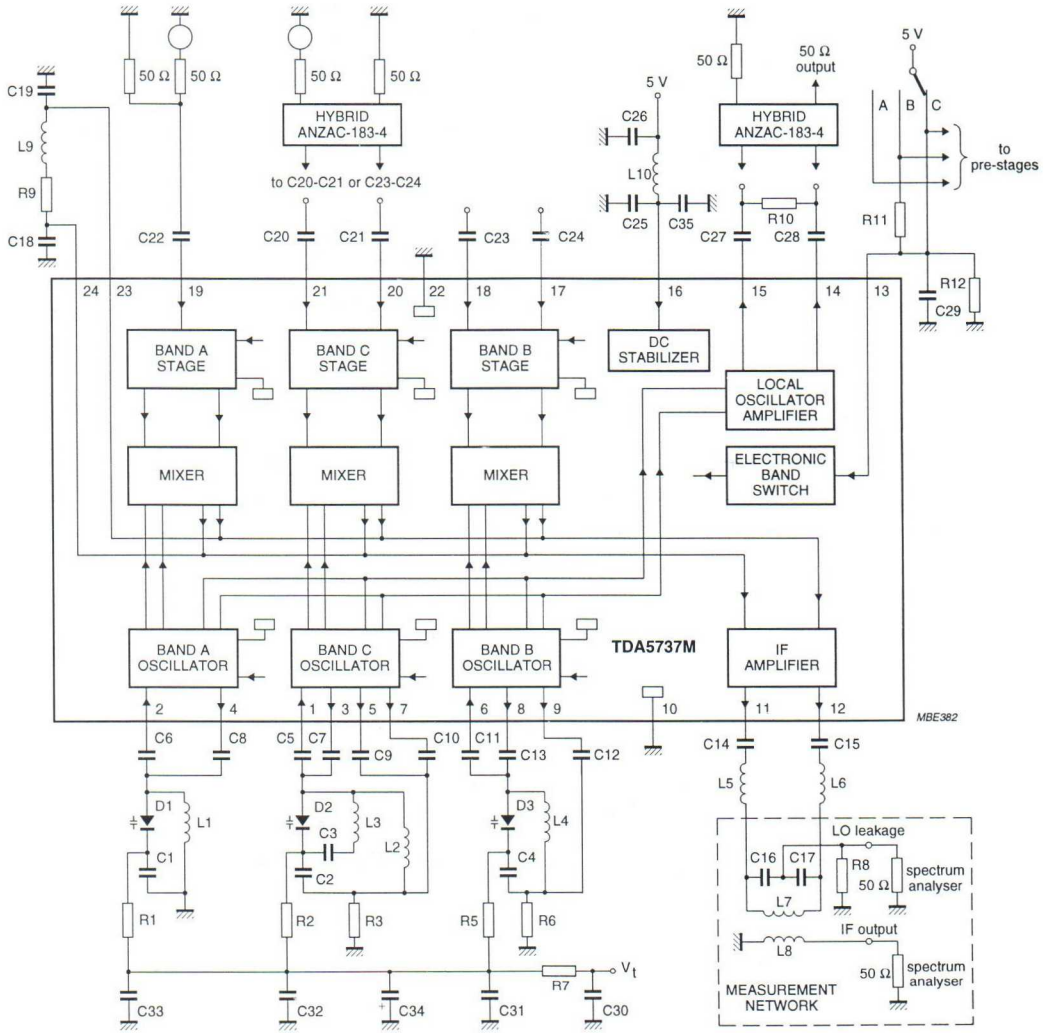


Fig.8 Reference measurement set-up.

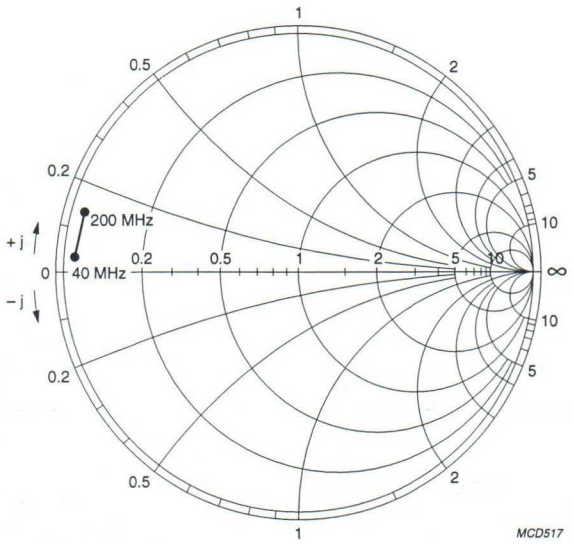


Fig.9 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

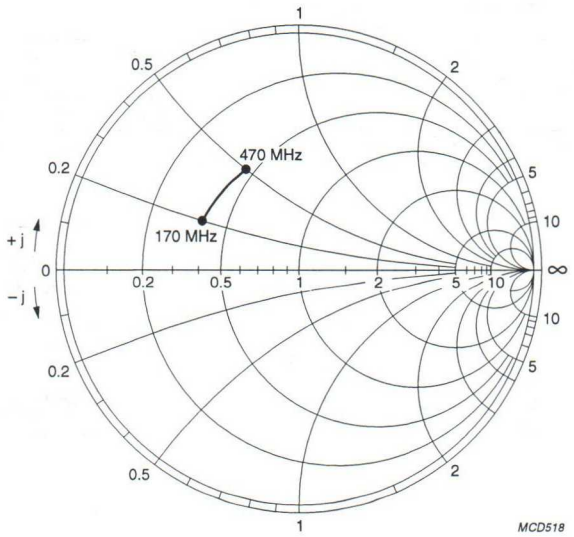


Fig.10 Input impedance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

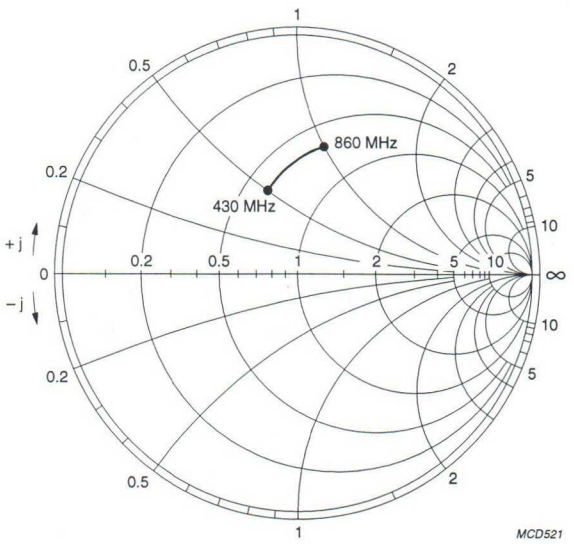


Fig.11 Input impedance (S_{11}) of the band C mixer input (460 to 880 MHz) (Z chart).

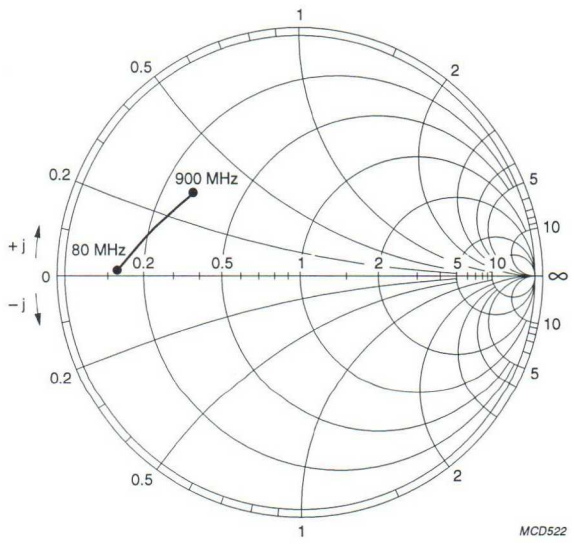


Fig.12 Output reflection coefficient (S_{22}) of the IF amplifier (80 to 900 MHz) (Y chart).

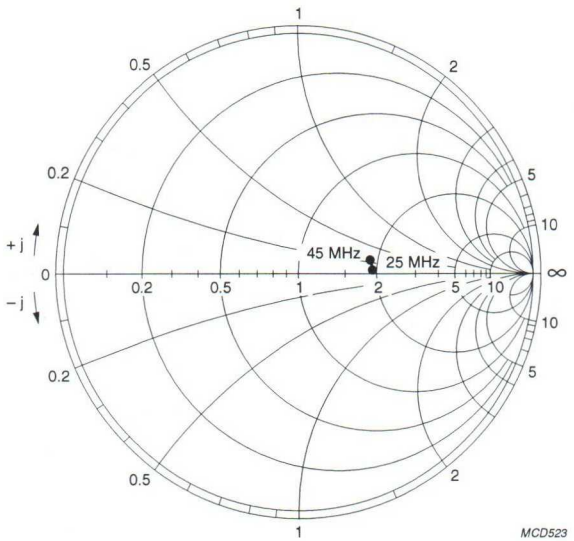


Fig.13 Output reflection coefficient (S_{22}) of the LO amplifier (25 to 45 MHz) (Z chart).

APPLICATION INFORMATION

Components values for Fig.8

Table 1 Capacitors (all SMD and NP0 except C34 and C35)

NUMBER	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	82 pF
C5	1 pF
C6	2 pF
C7	2 pF
C8	2 pF
C9	2 pF
C10	1 pF
C11	3.3 pF
C12	3.3 pF
C13	4.7 pF
C14	1 nF
C15	1 nF
C16	39 pF
C17	39 pF
C18	68 pF
C19	68 pF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C25	2.2 nF
C26	1 nF
C27	1 nF
C28	1 nF
C29	1 nF
C30	1 nF
C31	1 nF
C32	1 nF
C33	1 nF
C34	2.2 µF
C35	4.7 nF

Table 2 Resistors (all SMD)

NUMBER	VALUE
R1	47 kΩ
R2	22 kΩ
R3	22 kΩ
R5	27 kΩ
R6	27 kΩ
R7	10 kΩ
R8	50 Ω
R9	4.7 Ω
R10	100 Ω
R11	27 kΩ
R12	15 kΩ

Table 3 Diodes and coils

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB133
Coils(1)	
L1	7.5 turns (3 mm)
L2	2.5 turns (3.5 mm)
L3	1.5 turns (2.5 mm)
L4	2.5 turns (3 mm)
L5	5.5 turns (2.5 mm)
L6	5.5 turns (2.5 mm)
L9	12.5 turns (5 mm)
L10	2.2 µH (choke coil)

Note

1. Wire size for L1 to L6 is 0.4 mm

Transformers (L7 = 2 × 5 turns and L8 = 2 turns))

Coil type: TOKO 7kN; material: 113kN, screw core (03-0093), pot core (04-0026).

Video output amplifier TDA6101BQ

FEATURES

- High bandwidth and high slew rate
- Maximum operating voltage 250 V
- Black-current measurement output for automatic black current stabilization (ABS)
- Two cathode outputs: one for DC currents and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing CRT flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input, with a designed maximum common mode input capacitance of 3 pF; a differential mode input capacitance of 2 pF and a differential input voltage temperature drift of 0.4 mV/K.

GENERAL DESCRIPTION

The TDA6101BQ is a video output amplifier with an 8 MHz bandwidth. The device is contained in a SIL9 MP (single in-line 9 pin medium power) package. The device employs high voltage DMOS technology, and is designed to drive the cathode of a CRT.

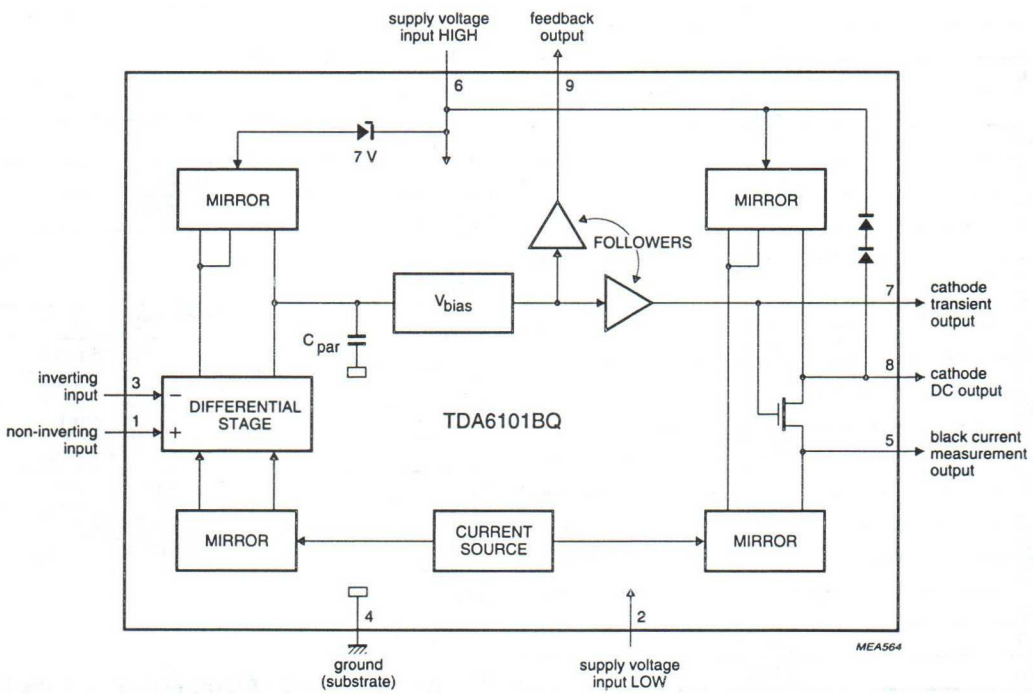


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6101BQ	9	DBS	plastic	SOT111

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non inverting input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting input
GND	4	ground; substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient output
V_{oc}	8	cathode DC output
V_{of}	9	feedback output

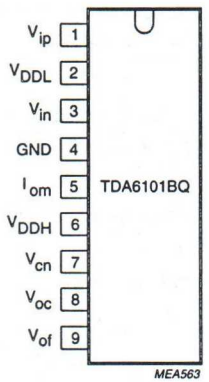


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Dissipation

A distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6101BQ is due to HIGH and LOW voltage supply currents and load currents in the feedback network and CRT.

$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{of} \times V_{of}/Rt$

Where R_t = value of feedback resistor and I_{oc} = DC value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (C_L + C_t + C_{int}) \times f \times V_{O\ (p\text{-}p)} \times b$

Where:

C_L = load capacitance

C_t = feedback capacitance

C_{int} = internal load capacitance (4 pF)

f = frequency

$V_{O\ (p\text{-}p)}$ = output voltage (peak-to-peak value)

b = non-blanking duty cycle

The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages with respect to pin 4 (ground) unless otherwise specified, currents specified as in Fig.1.

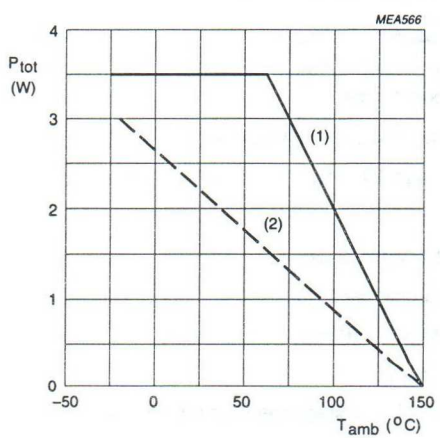
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDH}	HIGH level supply voltage	0	280	V
V_{DDL}	LOW level supply voltage	0	14	V
V_I	input voltage	0	V_{DDL}	V
$V_{I,dm}$	differential mode input voltage	−6	+6	V
V_{om}	measurement output voltage	0	V_{DDL}	V
V_{oc}, V_{of}	output voltage	V_{DDL}	V_{DDH}	V
I_{in}, I_{ip}	input current	0	1	mA
I_{OCL}	LOW non-repetitive peak cathode output current (50 μC)	0	5	A
I_{OCH}	HIGH non-repetitive peak cathode output current (100 nC)	0	10	A
P_{tot}	total power dissipation	0	1.9	W
T_{stg}	storage temperature	−55	+150	°C
T_j	junction temperature	−20	+150	°C
V_{ESD}	voltage peak (ESD-HBM)	−	> 2000	V
V_{ESD}	voltage peak (ESD-MM)	−	> 400	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	56 K/W
$R_{th\ j\text{-}c}$	from junction to mounting case	12 K/W

Quality specification

Quality specification SNW-FQ-611 part E is applicable.



(1) Mounted on heatsink of 12 K/W.
(2) No external heatsink.

Fig.3 Power derating curves.

CHARACTERISTICS

Operating range: T_{amb} = −20 to 65 °C; V_{DDH} = 180 to 250 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.
Test conditions: (unless otherwise specified) T_{amb} = 25 °C; V_{DDH} = 230 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance). Measured in Test circuit Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = V_{DDH}/2$	3.7	4.6	5.7	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = V_{DDH}/2$	2.3	2.9	3.6	mA
I_{bias}	input bias current	$V_{oc} = V_{DDH}/2$	0	–	20	µA
$I_{i,OFF}$	input offset current	$V_{oc} = V_{DDH}/2$	−3	–	+3	µA
$I_{om,OFF}$	offset current of measurement output	I_{oc} = 0 µA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	−5	0	+5	µA
$\Delta I_{om} / \Delta I_{oc}$	linearity of current transfer	−10 µA < I_{oc} < 3 mA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	0.9	1	1.1	
$V_{i,OFF}$	input offset voltage	$V_{oc} = V_{DDH}/2$	−50	–	+50	mV
$V_{oc\ min}$	minimum output voltage	V_{1-3} = −1 V	–	–	20	V
$V_{oc\ max}$	maximum output voltage	V_{1-3} = 1 V	V_{DDH}−12	–	–	V
GB	gain-bandwidth product of open-loop gain: $V_{or}/V_{i,dm}$	f = 500 kHz; $V_{oc-DC} = V_{DDH}/2$	–	0.9	–	GHz
B_S	small signal bandwidth	V_{oc-AC} = 60 V (p-p); $V_{oc-DC} = V_{DDH}/2$	6.5	9	–	MHz
B_L	large signal bandwidth	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$	5	7	–	MHz
t_{prop}	cathode output propagation time 50% input to 50% output (see Fig.5 and Fig.6)	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$; square wave: f < 1 MHz; $t_{r,i}$, $t_{f,i}$ = 40 ns	25	36	47	ns
t_r	cathode output rise time 10% output to 90% output (see Fig.5)	V_{oc} = 65 to 165 V; square wave: f < 1 MHz; t_f, input = 40 ns;	38	50	63	ns
t_f	cathode output fall time 90% output to 10% output (see Fig.6)	V_{oc} = 165 to 65 V; square wave: f < 1 MHz; t_r, input = 40 ns;	38	50	63	ns
t_s	settling time 50% input – (99% < output < 101%) (see Fig.5 and Fig.6)	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$;; square wave: < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	–	350	ns
SR	slew rate between 50 V to 150 V	V_{1-3} = 2 V(p-p) square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	1700	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_V	cathode output voltage overshoot (see Fig.5 and Fig.6)	V_{oc-AC} = 100 V (p-p); $V_{oc-DC} = V_{DDH}/2$;; square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns; note 1	–	7	–	%
R_i	differential input resistance		–	100	–	kΩ
SVRRH	HIGH voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB
SVRRL	LOW voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB

Notes

1. If the difference between V_{DDL} and V_{ip} is less then 7 V, overshoot cannot be specified.
2. SVRR is the ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 μC.

The cathode output is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

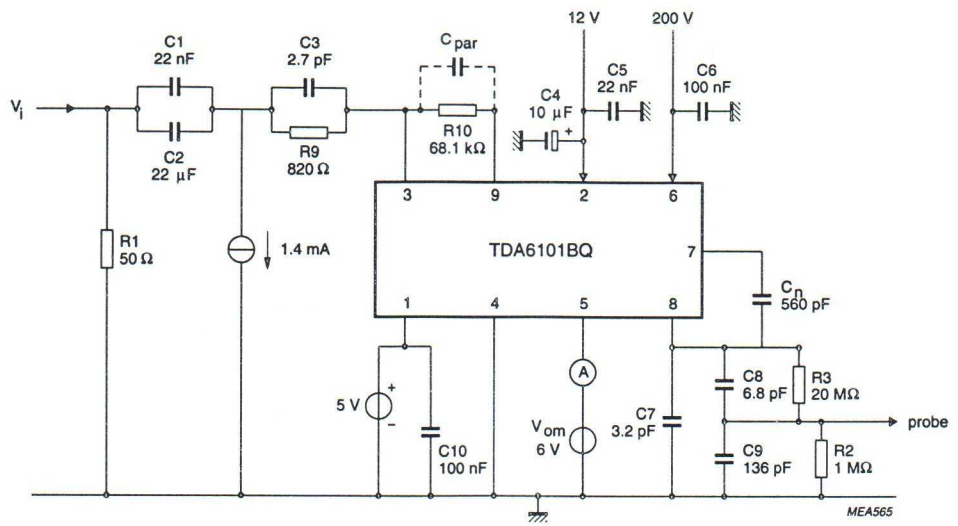


Fig.4 Test circuit with feedback factor 1/83; C_{par} is approximately 150 fF.

Note to Fig.4

FLASHOVER PROTECTION

The TDA6101BQ incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage until maximum $V_{DDH} + V_{diode}$. To limit the diode current, an external 1 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are required. For this resistor value the ground connection for the CRT must be connected to the main printed-circuit board. This addition produces an increase in the 'rise' and 'fall' times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

V_{DDH} – GND must be decoupled:

(a) With a capacitor > 20 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pin 6 and pin 4, definitely within 5 mm.

(b) With a capacitor > 10 µF on the picture tube base print (common for three output stages).

V_{DDL} – GND must be decoupled with a capacitor > 20 nF with good HF behaviour (e.g. ceramic). This capacitor must be placed as close as possible to pin 2 and pin 4, definitely within 10 mm.

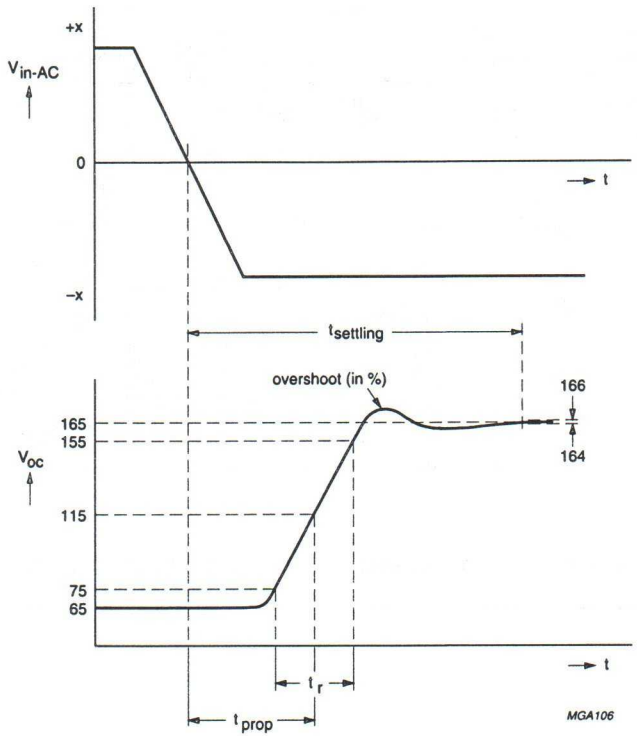


Fig.5 Output rising edge as a function of input signal.

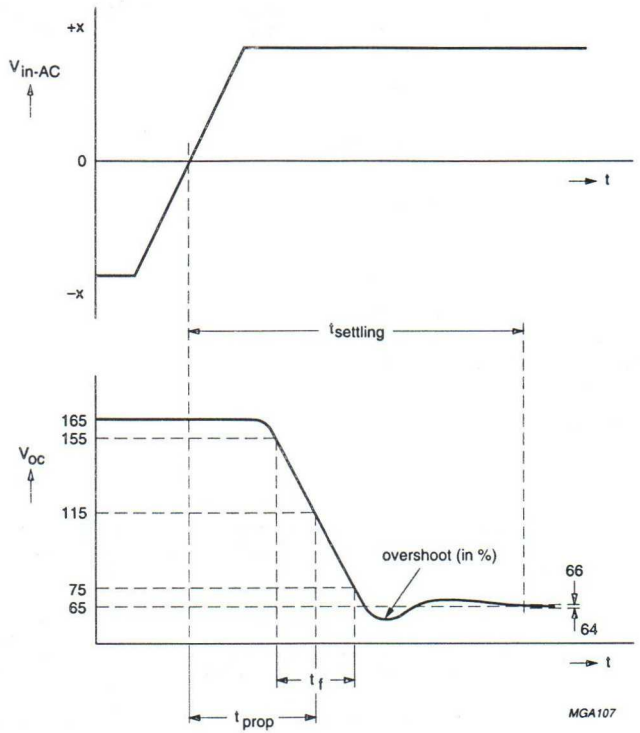


Fig.6 Output falling edge as a function of input signal.

Video output amplifier TDA6101Q

FEATURES

- High bandwidth and high slew rate
- No external heatsink required
- Black-current measurement output for Automatic Black-current Stabilization (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3 pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 20 μV/K
- Defined switch-off behaviour.

GENERAL DESCRIPTION

The TDA6101Q is a video output amplifier with 9 MHz bandwidth. The device is contained in a single in-line 9-pin medium power (DBS9MPF) package, using high-voltage DMOS technology, intended to drive the cathode of a colour CRT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDH}	high level supply voltage		0	–	250	V
V_{DDL}	low level supply voltage		0	–	14	V
I_{DDH}	quiescent high voltage supply current	$V_{oc} = 0.5V_{DDH}$	3.5	4.4	5.5	mA
I_{DDL}	quiescent low voltage supply current	$V_{oc} = 0.5V_{DDH}$	2.2	2.8	3.5	mA
V_I	input voltage		0	–	V_{DDL}	V
V_{oc}, V_{fb}	output voltage		V_{DDL}	–	V_{DDH}	V
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+65	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6101Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

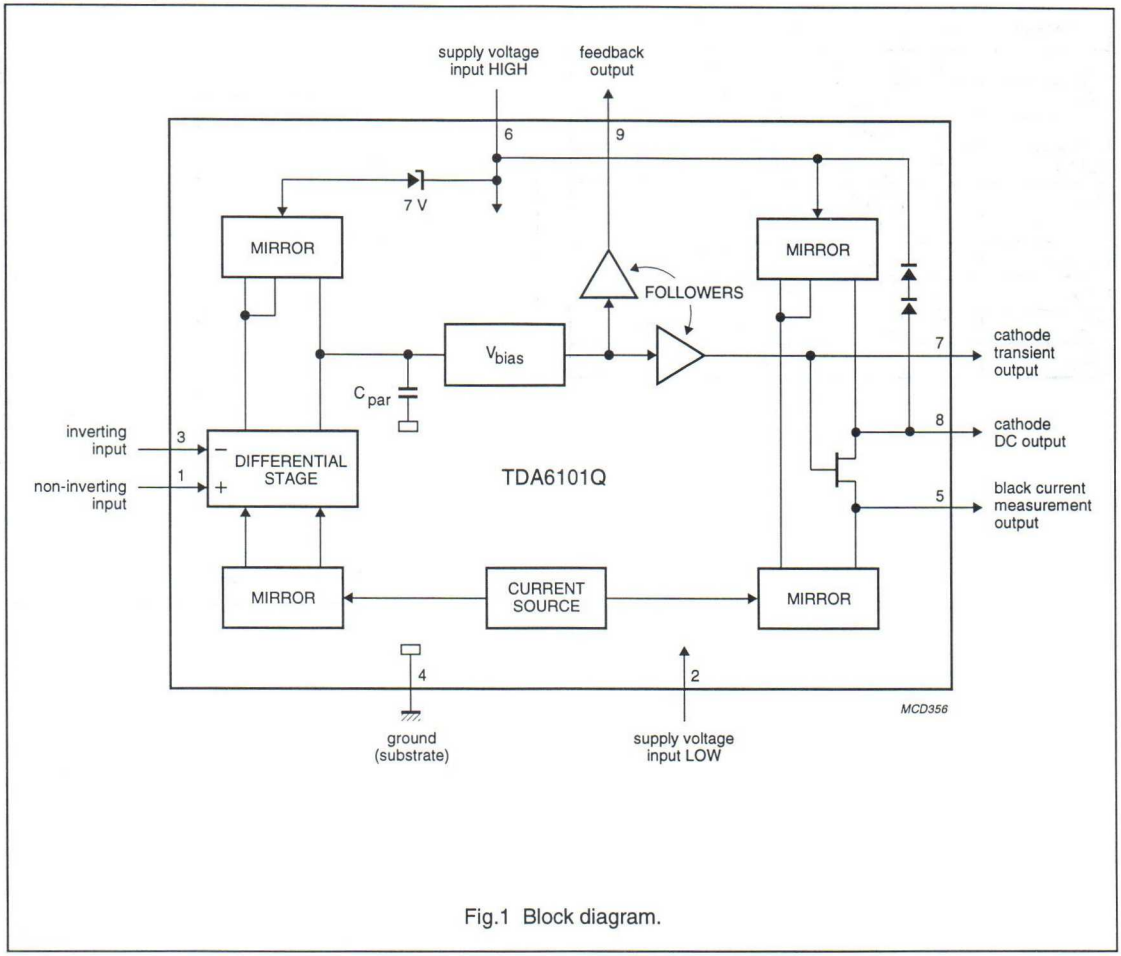


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non-inverting voltage input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting voltage input
GND	4	ground, substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient voltage output
V_{oc}	8	cathode DC voltage output
V_{fb}	9	feedback voltage output

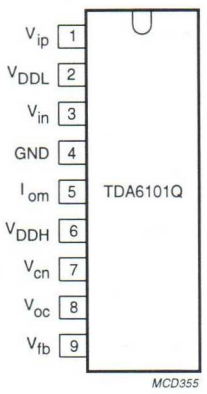


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDH}	high level supply voltage		0	250	V
V_{DDL}	low level supply voltage		0	14	V
V_I	input voltage		0	V_{DDL}	V
V_{Idm}	differential mode input voltage		−6	+6	V
V_{om}	measurement output voltage		0	V_{DDL}	
V_{oc}	cathode output voltage		V_{DDL}	V_{DDH}	V
V_{fb}	feedback output voltage		V_{DDL}	V_{DDH}	V
I_{in},I_{ip}	input current		0	1	mA
I_{ocsmL}	low non-repetitive peak cathode output current	flashover discharge = 100 μC	0	5	A
I_{ocsmH}	high non-repetitive peak cathode output current	flashover discharge = 100 nC	0	10	A
P_{tot}	total power dissipation		0	1.9	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		–	> 1500	V
	machine model (MM)		–	> 400	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable, except for ESD Human body model see Chapter "Limiting values", and can be found in the *"Quality reference handbook"* (ordering number 9398 510 63011).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER[1]	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	56	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	12	K/W

Note

1. External heatsink not required.

CHARACTERISTICS

Operating range: T_{amb} = –20 to 65 °C; V_{DDH} = 180 to 210 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.

Test conditions (unless otherwise specified): T_{amb} = 25 °C; V_{DDH} = 200 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); measured in test circuit Fig.3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = 0.5V_{DDH}$	3.5	4.4	5.5	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = 0.5V_{DDH}$	2.2	2.8	3.5	mA
I_{bias}	input bias current	$V_{oc} = 0.5V_{DDH}$	0	–	20	µA
I_{offset}	input offset current	$V_{oc} = 0.5V_{DDH}$	–3	–	+3	µA
$I_{om(offset)}$	offset current of measurement output	I_{oc} = 0 µA; –1.0 V < V_{1-3} < 1.0 V; 1.4 V < V_{om} < V_{DDL}	–5	0	+5	µA
$\frac{\Delta I_{om}}{\Delta I_{oc}}$	linearity of current transfer	–10 µA < I_{oc} < 3 mA; –1.0 V < V_{1-3} < 1.0 V; 1.4 V < V_{om} < V_{DDL}	0.9	1.0	1.1	
V_{offset}	input offset voltage	$V_{oc} = 0.5V_{DDH}$	–50	–	+50	mV
$V_{oc(min)}$	minimum output voltage	V_{1-3} = –1 V	–	–	20	V
$V_{oc(max)}$	maximum output voltage	V_{1-3} = –1 V	V_{DDH} – 12	–	–	V
GB	gain-bandwidth product of open-loop gain: V_{fb} / $V_{i, dm}$	f = 500 kHz; V_{ocDC} = 100 V	–	0.8	–	GHz
B_S	small signal bandwidth	V_{ocAC} = 60 V (p-p); V_{ocDC} = 100 V	7	9	–	MHz
B_L	large signal bandwidth	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V	5.5	7	–	MHz
t_{pd}	cathode output propagation delay time 50% input to 50% output	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns; see Figs 4 and 5	27	38	49	ns
t_r	cathode output rise time 10% output to 90% output	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns; see Fig.4	43	55	68	ns
t_f	cathode output fall time 90% output to 10% output	V_{oc} = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns; see Fig.5	43	55	68	ns
t_s	settling time 50% input to (99% < output < 101%)	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns; see Figs 4 and 5	–	–	350	ns
SR	slew rate between 50 V to 150 V	V_{1-3} = 2 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns	–	1700	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_v	cathode output voltage overshoot	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns; see Figs 4 and 5; note 1	–	9	–	%
SVRRH	high supply voltage rejection ratio	f < 50 kHz; note 2	–	85	–	dB
SVRRL	low supply voltage rejection ratio	f < 50 kHz; note 2	–	70	–	dB

Notes

1. If the difference between V_{DDL} and V_{ip} is less than 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100 μC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

Flashover protection

The TDA6101Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output pin to the V_{DDH} pin. The DC supply voltage at the V_{DDH} pin has to be within the operating range of 180 to 210 V to ensure that the Absolute Maximum Rating for V_{DDH} of 250 V will not be exceeded during flashover. To limit the diode current, an external 820 Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

V_{DDH} to GND must be decoupled:

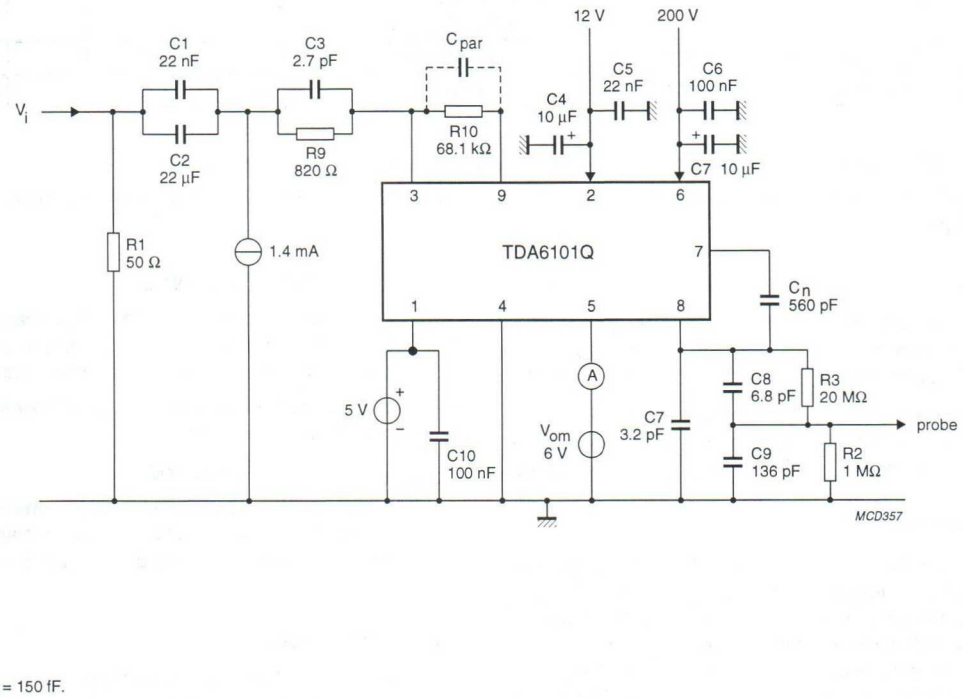
1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 μF on the picture tube base print (common for three output stages).

V_{DDL} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pins 2 and 4, but definitely within 10 mm.

Switch-off behaviour

The switch-off behaviour of the TDA6101Q is defined: when the bias current becomes zero, at V_{DDL} (pin 2) lower than approximately 5 V, all the output pins (pins 7, 8 and 9) will be high.



C_{par} = 150 fF.

Fig.3 Test circuit with feedback factor $1/83$.

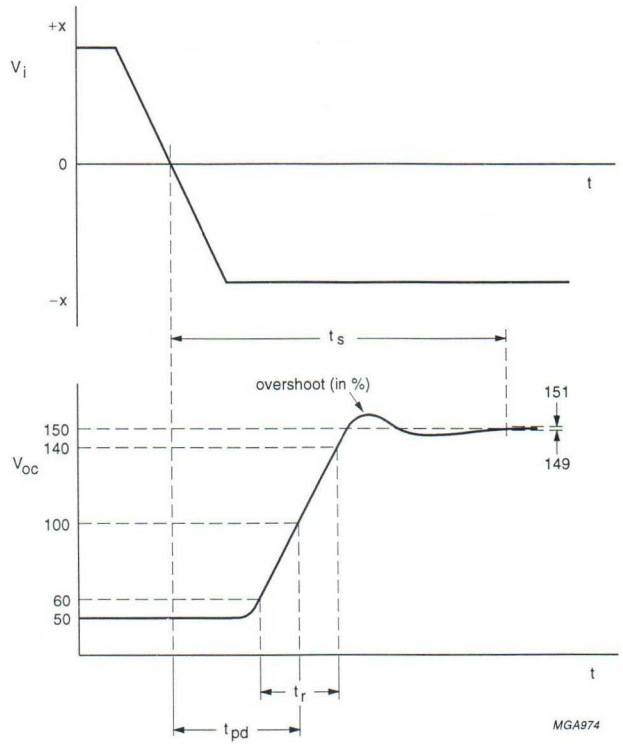


Fig.4 Output voltage (pin 8) rising edge as a function of the AC input signal.

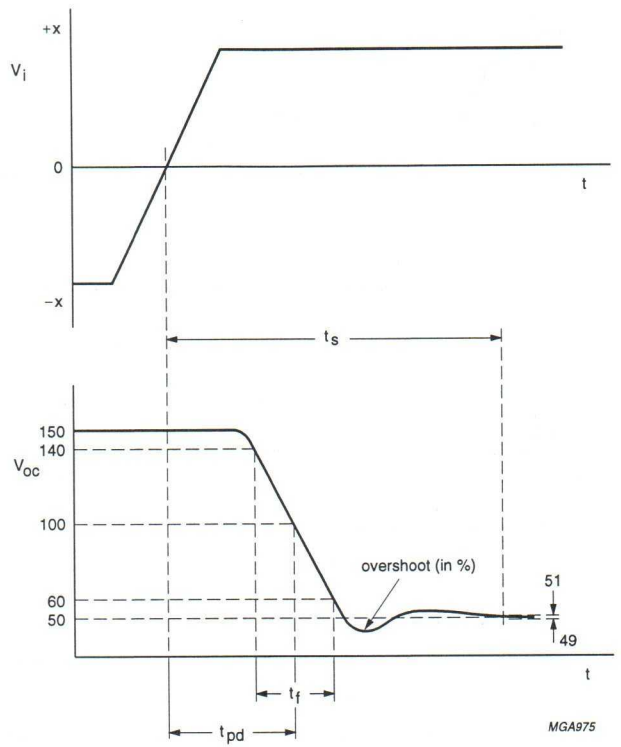


Fig.5 Output voltage (pins 8) falling edge as a function of the AC input signal.

TEST AND APPLICATION INFORMATION

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6101Q is due to high and low voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{fb} \times \left(\frac{V_{fb}}{R_{fb}} \right)$$

R_{fb} = value of feedback resistor.

I_{oc} = DC value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (C_L + C_{fb} + C_{int}) \times f_i \times V_{o(p-p)} \times \delta$

C_L = load capacitance.

C_{fb} = feedback capacitance ($\approx$ 150 fF).

C_{int} = internal load capacitance ($\approx$ 4 pF).

f_i = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

δ = non-blanking duty-cycle ($\approx$ 0.8).

The IC must be mounted on the picture tube base print to minimize the load capacitance (C_L).

Triple video output amplifier TDA6103Q

FEATURES

- High bandwidth: 7.5 MHz typical; 60 V (peak-to-peak value)
- High slew rate: 1600 V/μs
- Simple application with a variety of colour decoders
- Only one supply voltage needed
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- One non-inverting input with a low minimum input voltage of 1 V
- Thermal protection
- Controllable switch-off behaviour.

GENERAL DESCRIPTION

The TDA6103Q includes three video output amplifiers in one single in-line 9-pin medium power (SIL9MP) package SOT111BE, using high-voltage DMOS technology, intended to drive the three cathodes of a colour CRT.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6103Q	9	DBS9	plastic	SOT111BE

BLOCK DIAGRAM

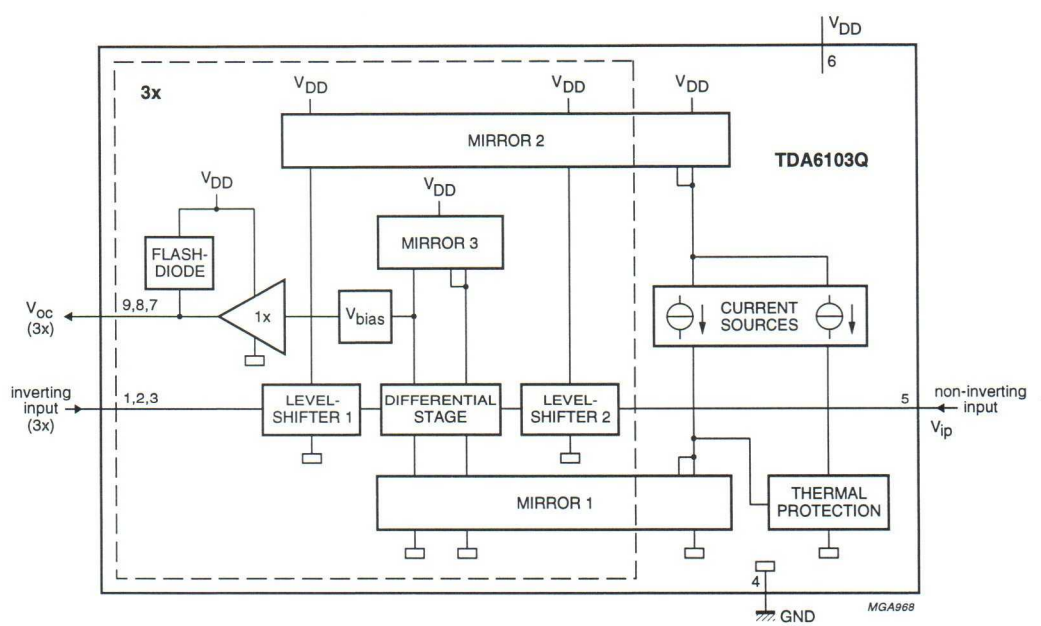


Fig.1 Block diagram (one amplifier shown).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{i1}	1	inverting input 1
V_{i2}	2	inverting input 2
V_{i3}	3	inverting input 3
GND	4	ground, fin
V_{ip}	5	non-inverting input
V_{DD}	6	supply voltage
V_{oc3}	7	cathode output 3
V_{oc2}	8	cathode output 2
V_{oc1}	9	cathode output 1

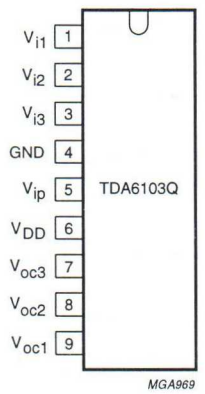


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_i	input voltage		0	12	V
V_{idm}	differential mode input voltage		−6	+6	V
V_{oc}	cathode output voltage		0	V_{DD}	V
I_{ocsmL}	LOW non-repetitive peak cathode output current	flashover discharge = 50 μC	0	5	A
I_{ocsmH}	HIGH non-repetitive peak cathode output current	flashover discharge = 100 nC	0	10	A
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		−	tbf	V
	machine model (MM)		−	tbf	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

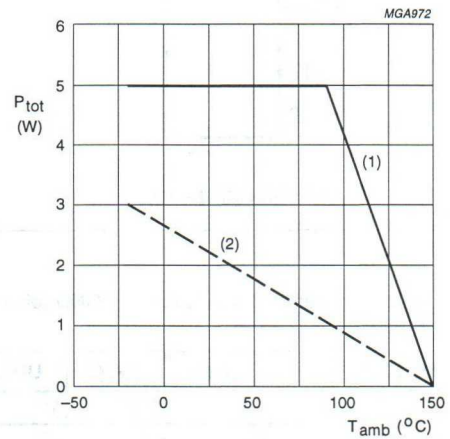
Quality specification *"SNW-FQ-611 part E"* is applicable and can be found in the *"Quality reference pocketbook"* (ordering number 9398 510 34011).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}fin}$	from junction to fin; note 1	11 K/W
$R_{th\ h\text{-}a}$	from heatsink to ambient	18 K/W

Note

1. An external heatsink is necessary.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10% decrease at 130 °C and 30% decrease at 145 °C (typical values on the spot of the thermal protection circuit).

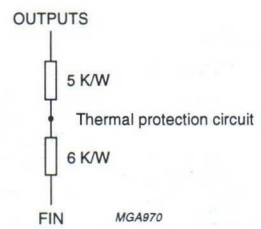


Fig.4 Equivalent thermal resistance network.

CHARACTERISTICS

Operating range: T_j = –20 to 150 °C; V_{DD} = 180 to 210 V; V_{ip} = 1 to 4 V.

Test conditions (unless otherwise specified): T_{amb} = 25 °C; V_{DD} = 200 V; V_{ip} = 1.3 V; $V_{oc1} = V_{oc2} = V_{oc3} = \frac{1}{2}V_{DD}$; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\ h\text{-}a}$ = 18 K/W; measured in test circuit Fig.5.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	quiescent supply current		7.0	9.25	11.5	mA
I_{bias}	input bias current inverting inputs (pins 1, 2 and 3)		–5	–1	+1	μA
I_{bias}	input bias current non-inverting input (pin 5)		–15	–3	+1	μA
$V_{i(offset)}$	input offset voltage (pins 1, 2 and 3)		–50	–	+50	mV
$\Delta V_{i(offset)}$	differential input offset voltage temperature drift between pins 1 and 5; 2 and 5; 3 and 5		–	tbf	–	mV/K
C_{icm}	common-mode input capacitance (pins 1, 2 and 3)		–	5	–	pF
C_{icm}	common-mode input capacitance (pin 5)		–	10	–	pF
C_{idm}	differential mode input capacitance between 1 and 5; 2 and 5; 3 and 5		–	1	–	pF
$V_{oc(min)}$	minimum output voltage (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5}$ = –1 V	–	5	10	V
$V_{oc(max)}$	maximum output voltage (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5}$ = 1 V; note 1	V_{DD} – 10	V_{DD} – 6	–	V
GB	gain-bandwidth product of open-loop gain: $V_{oc1, 2, 3} / V_{i1\text{-}5,\ 2\text{-}5,\ 3\text{-}5}$	f = 500 kHz	–	0.75	–	GHz
B_S	small signal bandwidth (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 60 V	6	7.5	–	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V	5	7	–	MHz
t_{pd}	cathode output propagation delay time 50% input to 50% output (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	38	–	ns
Δt_p	difference in cathode output propagation time 50% input to 50% output (pins 7 and 8, 7 and 9 and 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–10	0	+10	ns
t_r	cathode output rise time 10% output to 90% output (pins 7, 8 and 9)	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3); see Fig.7	48	60	73	ns
t_f	cathode output fall time 90% output to 10% output (pins 7, 8 and 9)	V_o = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns (pins 1, 2 and 3); see Fig.8	48	60	73	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_s	settling time 50% input to (99% < output < 101%)	$V_{oc(p-p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	–	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V); (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5}$ = 2 V square wave (p-p); f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–	1600	–	V/µs
O_v	cathode output voltage overshoot (pins 7, 8 and 9)	$V_{oc(p-p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	5	–	%
SVRR	supply voltage rejection ratio	f < 50 kHz; note 2	–	70	–	dB

Notes

1. See also Fig.6 for the typical low-frequency response of V_i to V_{oc}.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 µC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

The DC voltage of V_{DD} (pin 6) must be within the operating range of 180 to 210 V during the peak currents.

Flashover protection

The TDA6103Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage up to a maximum of $V_{DD} + V_{diode}$. To limit the diode current, an external 1.5 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise- and fall times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

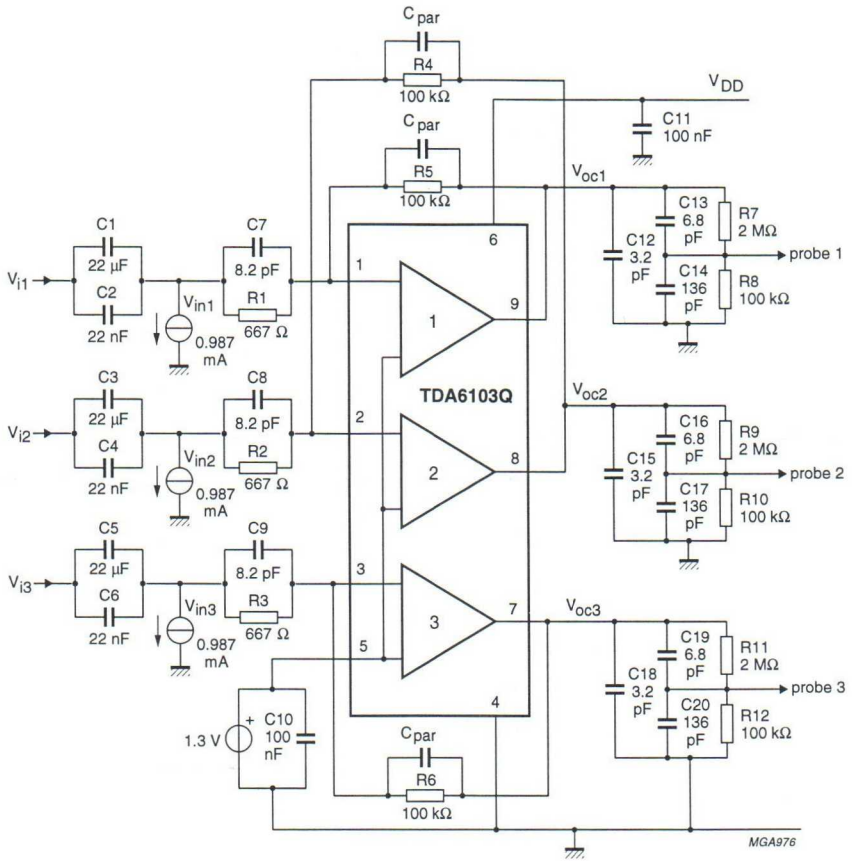
V_{DD} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 µF on the picture tube base print.

Switch-off behaviour

The switch-off behaviour of the TDA6103Q is controllable. This is due to the fact that the output pins of the TDA6103Q are still under control of the input pins for relative low-power supply voltages (approximately 30 V and higher).

Test circuit



C_{par} = 70 fF.

Fig.5 Test circuit with feedback factor $1/150$.

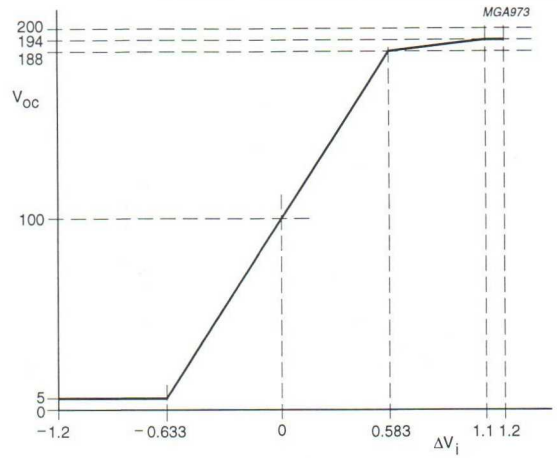


Fig.6 Typical low-frequency (f < 1 MHz) response of $\Delta V_{i1, 2,3}$ to $V_{oc1, 2,3}$.

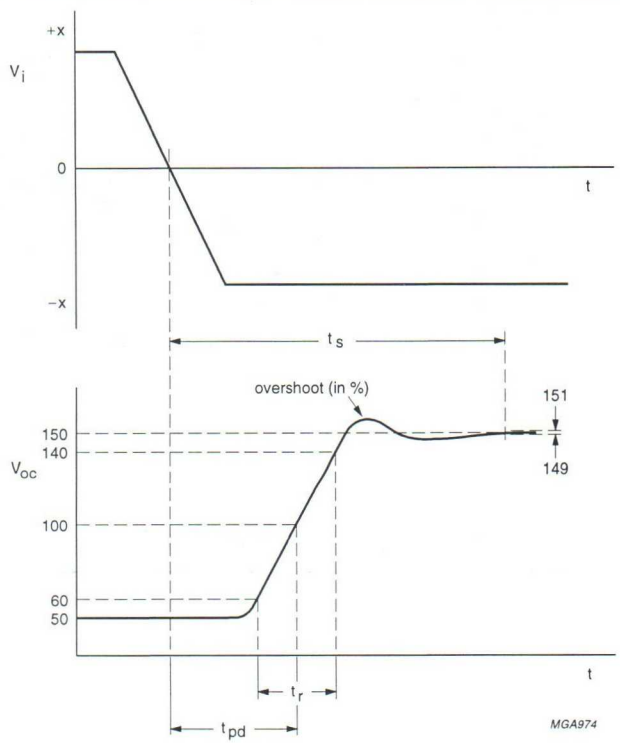


Fig.7 Output voltage (pins 7, 8 and 9) rising edge as a function of the AC input signal.

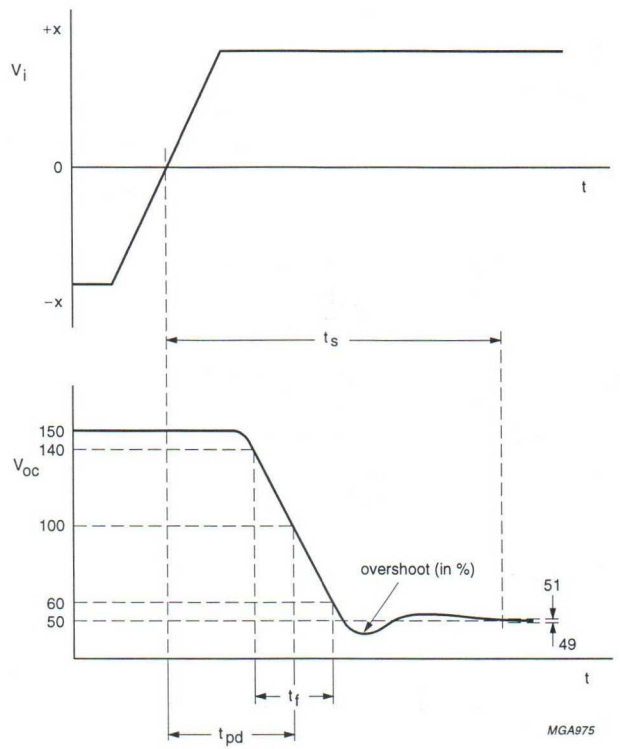


Fig.8 Output voltage (pins 7, 8 and 9) falling edge as a function of the AC input signal.

TEST AND APPLICATION INFORMATION

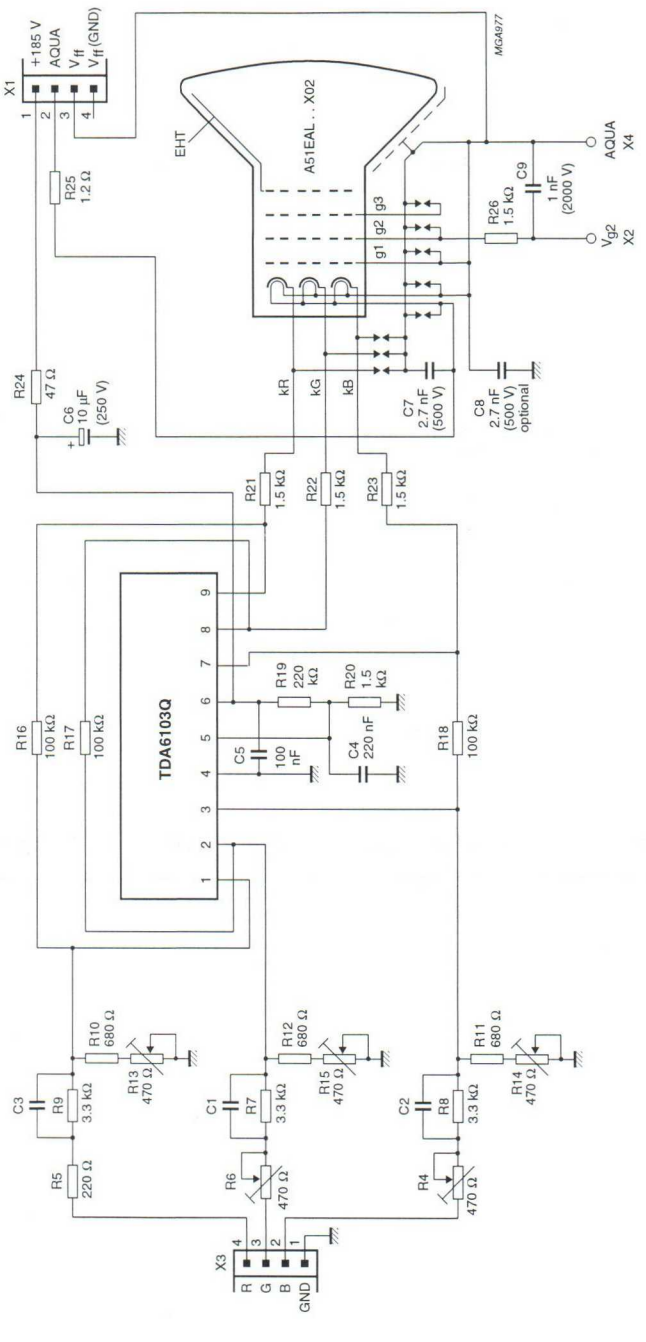
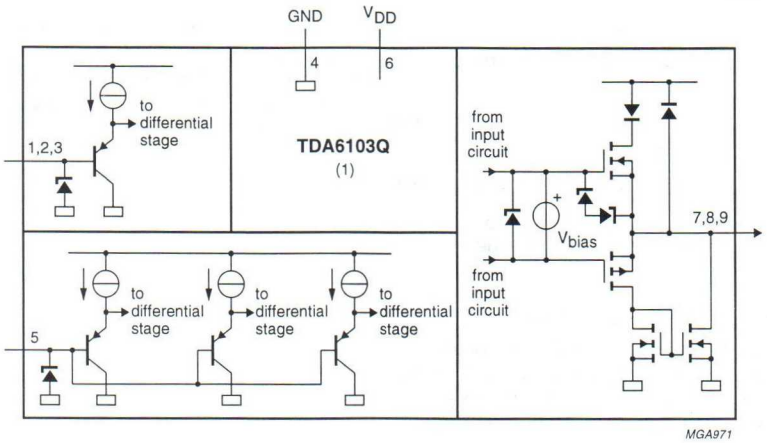


Fig.9 Application diagram.



(1) All pins have an energy protection for positive or negative overstress situations.

Fig.10 Internal pin configuration.

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6103Q is due to voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$P_{stat} = V_{DD} \times I_{DD} - 3 \times V_{oc} \times (V_{oc}/R_{fb} - I_{OC})$

R_{fb} = value of feedback resistor.

I_{OC} = DC-value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = 3 \times V_{DD} \times (C_L + C_{fb} + C_{int}) \times f_i \times V_{o(p-p)} \times \delta$

C_L = load capacitance.

C_{fb} = feedback capacitance.

C_{int} = internal load capacitance (≈4 pF).

f_i = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

δ = non-blanking duty-cycle.

The IC must be mounted on the picture tube base print to minimize the load capacitance (C_L).

Video output amplifier TDA6111Q

FEATURES

- High bandwidth and high slew rate
- Black-current measurement output for Automatic Black-current Stabilization (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3 pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 50 μV/K
- Defined switch-off behaviour.

GENERAL DESCRIPTION

The TDA6111Q is a video output amplifier with 16 MHz bandwidth. The device is contained in a single in-line 9-pin medium power (DBS9MPF) package, using high-voltage DMOS technology, intended to drive the cathode of a colour CRT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDH}	high level supply voltage		0	–	250	V
V_{DDL}	low level supply voltage		0	–	14	V
I_{DDH}	quiescent high voltage supply current	$V_{oc} = 0.5V_{DDH}$	7.0	9.0	11.0	mA
I_{DDL}	quiescent low voltage supply current	$V_{oc} = 0.5V_{DDH}$	5.0	6.8	8.0	mA
V_I	input voltage		0	–	V_{DDL}	V
V_{oc}, V_{fb}	output voltage		V_{DDL}	–	V_{DDH}	V
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+65	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6111Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

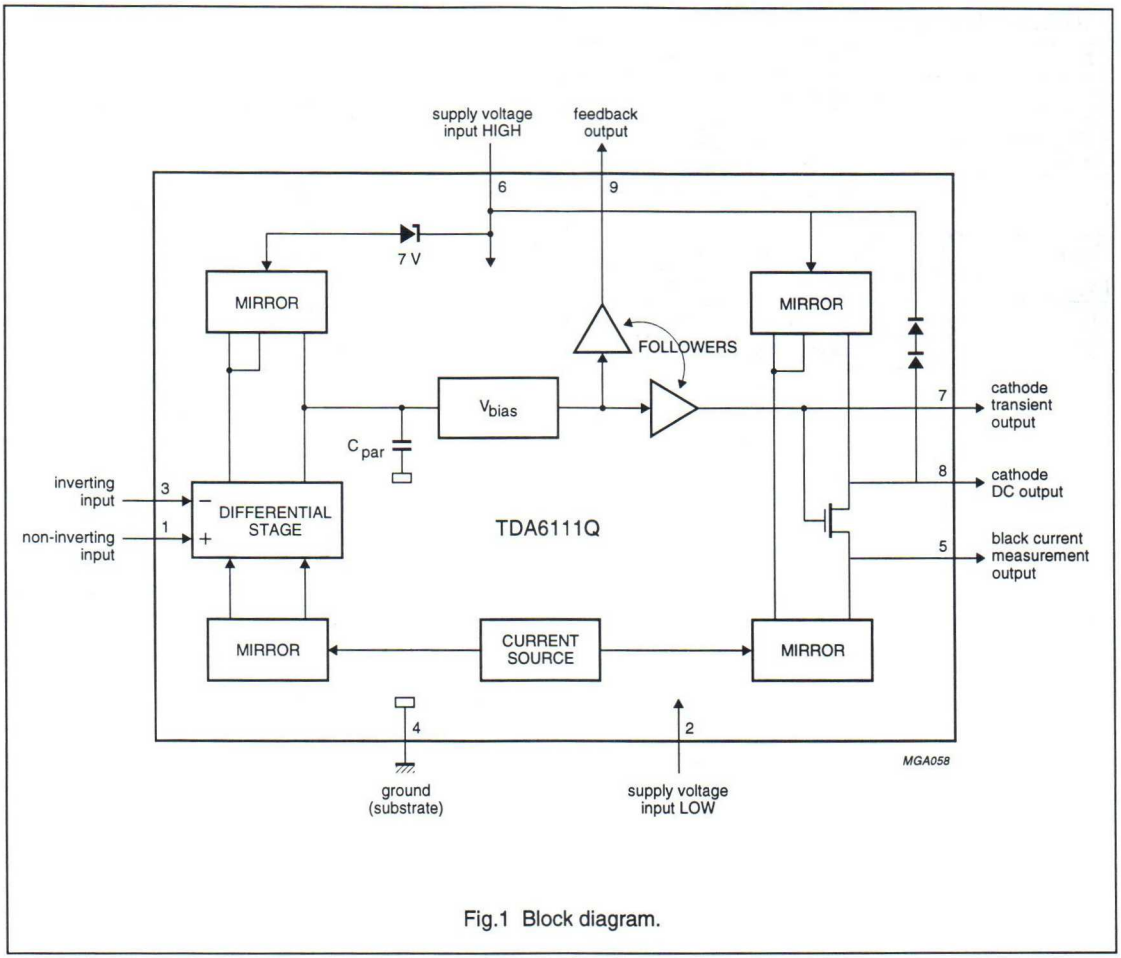


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non-inverting voltage input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting voltage input
GND	4	ground, substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient voltage output
V_{oc}	8	cathode DC voltage output
V_{fb}	9	feedback voltage output

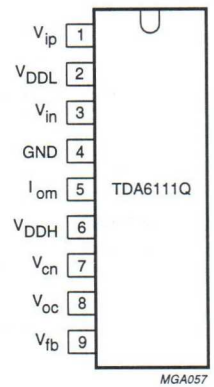


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDH}	high level supply voltage		0	250	V
V_{DDL}	low level supply voltage		0	14	V
V_I	input voltage		0	V_{DDL}	V
V_{Idm}	differential mode input voltage		−6	+6	V
V_{om}	measurement output voltage		0	V_{DDL}	
V_{oc}	cathode output voltage		V_{DDL}	V_{DDH}	V
V_{fb}	feedback output voltage		V_{DDL}	V_{DDH}	V
I_{in},I_{ip}	input current		0	1	mA
I_{ocsmL}	low non-repetitive peak cathode output current	flashover discharge = 100 μC	0	5	A
I_{ocsmH}	high non-repetitive peak cathode output current	flashover discharge = 100 nC	0	10	A
P_{tot}	total power dissipation		0	4	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		−	> 1500	V
	machine model (MM)		−	> 400	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable, except for ESD Human body model see Chapter "Limiting values", and can be found in the *"Quality reference handbook"* (ordering number 9398 510 63011).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case (note 1)	12	K/W

Note

1. External heatsink is required.

CHARACTERISTICS

Operating range: T_{amb} = –20 to 65 °C; V_{DDH} = 180 to 210 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.

Test conditions (unless otherwise specified): T_{amb} = 25 °C; V_{DDH} = 200 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\text{-}heatsink}$ = 10 K/W; measured in test circuit Fig.3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = 0.5V_{DDH}$	7.0	9.0	11.0	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = 0.5V_{DDH}$	5.0	6.8	8.0	mA
I_{bias}	input bias current	$V_{oc} = 0.5V_{DDH}$	0	–	40	µA
I_{offset}	input offset current	$V_{oc} = 0.5V_{DDH}$	–6	–	+6	µA
$I_{om(offset)}$	offset current of measurement output	I_{oc} = 0 µA; –1.0 V < V_{1-3} < 1.0 V; 1.4 V < V_{om} < V_{DDL}	–10	0	+10	µA
$\frac{\Delta I_{om}}{\Delta I_{oc}}$	linearity of current transfer	–10 µA < I_{oc} < 3 mA; –1.0 V < V_{1-3} < 1.0 V; 1.4 V < V_{om} < V_{DDL}	0.9	1.0	1.1	
V_{offset}	input offset voltage	$V_{oc} = 0.5V_{DDH}$	–50	–	+50	mV
$V_{oc(min)}$	minimum output voltage	V_{1-3} = –1 V	–	–	20	V
$V_{oc(max)}$	maximum output voltage	V_{1-3} = –1 V	V_{DDH} – 12	–	–	V
GB	gain-bandwidth product of open-loop gain: V_{fb} / $V_{i,\,dm}$	f = 500 kHz; V_{ocDC} = 100 V	–	1.6	–	GHz
B_S	small signal bandwidth	V_{ocAC} = 60 V (p-p); V_{ocDC} = 100 V	13	16	–	MHz
B_L	large signal bandwidth	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V	10	13	–	MHz
t_{pd}	cathode output propagation delay time 50% input to 50% output	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5	17	23	29	ns
t_r	cathode output rise time 10% output to 90% output	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_f = 22 ns; see Fig.4	23	30	36	ns
t_f	cathode output fall time 90% output to 10% output	V_{oc} = 150 to 50 V square wave; f < 1 MHz; t_r = 22 ns; see Fig.5	23	30	36	ns
t_s	settling time 50% input to (99% < output < 101%)	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5	–	–	350	ns
SR	slew rate between 50 V to 150 V	V_{1-3} = 2 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 22 ns	–	3000	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_v	cathode output voltage overshoot	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5; note 1	–	9	–	%
SVRRH	high supply voltage rejection ratio	f < 50 kHz; note 2	–	85	–	dB
SVRRL	low supply voltage rejection ratio	f < 50 kHz; note 2	–	70	–	dB

Notes

1. If the difference between V_{DDL} and V_{ip} is less than 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100 μC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

Flashover protection

The TDA6111Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output pin to the V_{DDH} pin. The DC supply voltage at the V_{DDH} pin has to be within the operating range of 180 to 210 V to ensure that the Absolute Maximum Rating for V_{DDH} of 250 V will not be exceeded during flashover. To limit the diode current, an external 680 Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 5 ns and a decrease in the overshoot of approximately 4%.

V_{DDH} to GND must be decoupled:

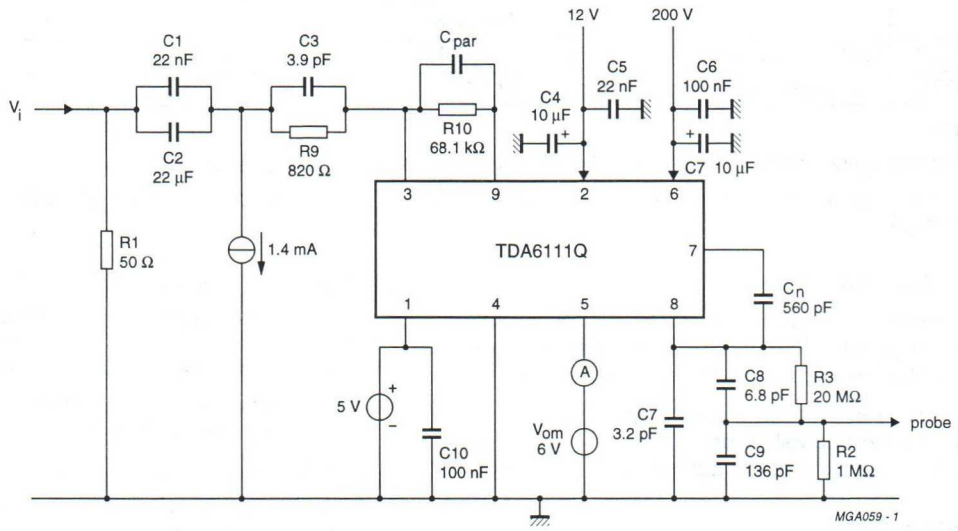
1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 μF on the picture tube base print (common for three output stages).

V_{DDL} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pins 2 and 4, but definitely within 10 mm.

Switch-off behaviour

The switch-off behaviour of the TDA6111Q is defined: when the bias current becomes zero, at V_{DDL} (pin 2) lower than approximately 5 V, all the output pins (pins 7, 8 and 9) will be high.



C_{par} = 150 fF.

Fig.3 Test circuit with feedback factor $1/83$.

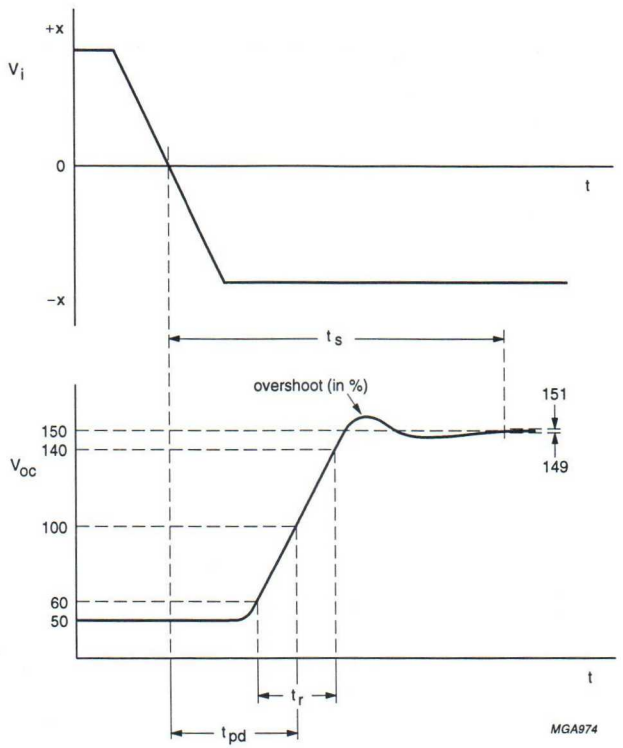


Fig.4 Output voltage (pin 8) rising edge as a function of the AC input signal.

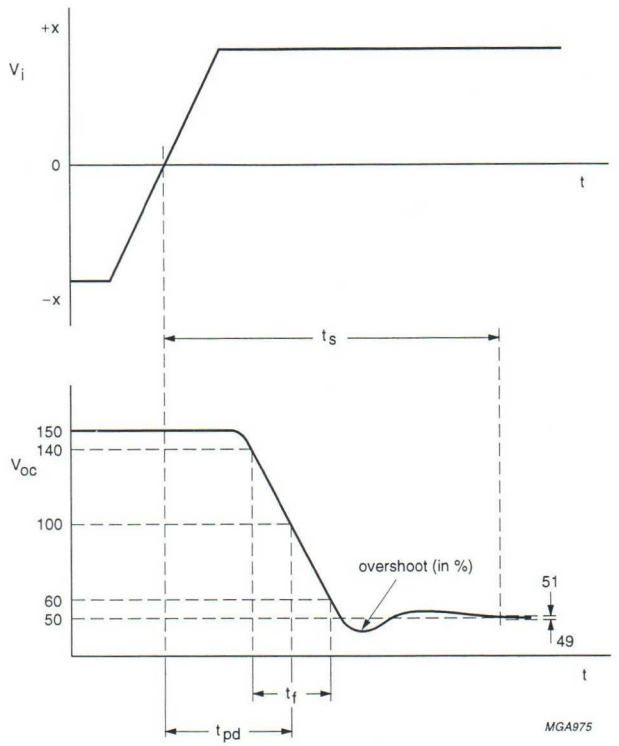


Fig.5 Output voltage (pins 8) falling edge as a function of the AC input signal.

TEST AND APPLICATION INFORMATION

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6111Q is due to high and low voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{fb} \times \left(\frac{V_{fb}}{R_{fb}} \right)$$

R_{fb} = value of feedback resistor.

I_{oc} = DC value of cathode current.

With $V_{fb} = V_{oc} = 100$ V, $R_{fb} = 68$ kΩ, $I_{oc} = 0.6$ mA and other typical conditions as mentioned in Chapter "Characteristics", the static dissipation $P_{stat} = 2.0$ W.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (C_L + C_{fb} + C_{int}) \times f_i \times V_{o(p-p)} \times \delta$

C_L = load capacitance.

C_{fb} = feedback capacitance (≈ 150 fF).

C_{int} = internal load capacitance (≈ 4 pF).

f_i = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

δ = non-blanking duty-cycle (≈ 0.8).

With $C_L = 10$ pF, $C_{fb} = 0$, $C_{int} = 4$ pF, $f_i = 8$ MHz (simulation of worst-case noise), $V_{o(p-p)} = 100$ V and $\delta = 80\%$ then $P_{dyn} = 1.8$ W

The IC must be mounted on the picture tube base print to minimize the load capacitance (C_L).

The total power dissipation, $P_{tot} = P_{stat} + P_{dyn}$ thus amounts to 3.6 W under given conditions.

From $T_j = T_{amb} + P_{tot} \times R_{th\ j\text{-}a} < T_{j(max)} = 150$ °C, $R_{th\ j\text{-}a}$ of the package and heatsink together must be < 24 K/W.

VIDEO MODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA6800 is a modulator circuit for modulation of video signals on a VHF/UHF carrier. The circuit requires a 5 V power supply and few external components for the negative modulation mode. For positive modulation an external clamp circuit is required. This circuit can be used as a general purpose modulator without additional external components.

Features

- Balanced modulator
- Symmetrical oscillator
- Video clamp circuit for negative modulation
- Frequency range 50 to 800 MHz

QUICK REFERENCE DATA

		min.	typ.	max.	
Supply voltage range	$V_{5\text{-}4}$	4,5	–	5,5	V
Supply current consumption	I_5	–	9	–	mA
Video input voltage	$V_{8(p\text{-}p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Output voltage (50 MHz)	$V_{6\text{-}7}$	–	13	–	mV
Output voltage (600 MHz)	$V_{6\text{-}7}$	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation distortion	d_{int}	–	–80	–	dB

PACKAGE OUTLINE

TDA6800 : 8-lead dual in-line; plastic (SOT97A).
TDA6800T: 8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{5-4}	max.	7 V
Input voltage	V_{8-4}	max.	4 V
Output voltage	$V_{6,7-4}$	max.	9 V
Storage temperature	T_{stg}	max.	125 °C
Junction temperature	T_j	max.	125 °C
Operating ambient temperature range	T_{amb}		−25 to + 85 °C

THERMAL RESISTANCE

From junction to ambient in free air		
TDA6800T	$R_{th\ j\text{-}a}$	260 K/W
TDA6800	$R_{th\ j\text{-}a}$	120 K/W

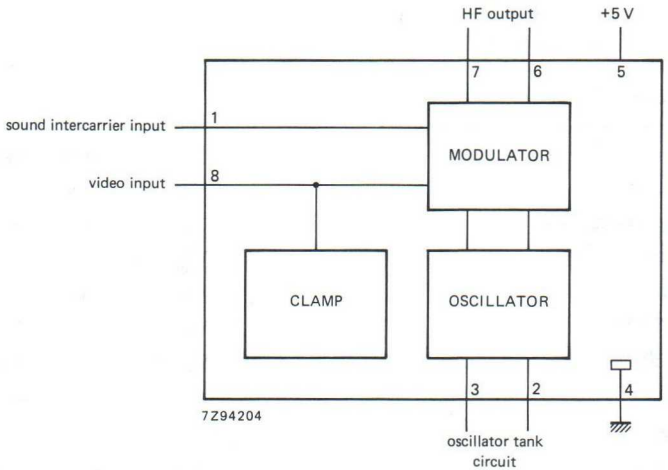


Fig. 1 Block diagram TDA6800 and TDA6800T.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	13	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Voltage (d.c.) at video input (clamp voltage)	V_8	–	1,4	–	V
Voltage (d.c.) at sound input	V_1	–	2,5	–	V
Output voltage f = 50 MHz; R_L = 75 Ω	V_{6-7}	–	13	–	mV
Output voltage f = 600 MHz; R_L = 75 Ω	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation (1,1 MHz) (note 1)		–	–80	–60	dB
Frequency shift V_b = 5%, f = 600 MHz	Δ_f	–	–	100	kHz
Frequency shift V_b = 5%, f = 800 MHz	Δ_f	–	tbf	–	kHz
Frequency drift 25 to 40 °C	Δ_f	–	–	100	kHz
Frequency drift 15 to 55 °C	Δ_f	–	–	300	kHz
Positive modulation (see Fig. 3)					
Residual carrier voltage	V_r	–	–	2,5	%
Cross modulation (note 2)	α	–	0,1	0,25	%

NOTES TO THE CHARACTERISTICS

1. Input signal: d.c. 0,45 V (V_{8-4} = 1,85 V)
   4,4 MHz; input voltage (p-p) = 0,6 V
   5,5 MHz; input voltage (p-p) = 1,26 V
   measured with respect to picture carrier, at f = 600 MHz.
2. Input signal: d.c. 1 V (V_{8-4} = 3,5 V)
   5,5 MHz AM modulated, f_m = 100 kHz
   m = 0,8; input voltage (p-p) = 2,27 V (including modulation)
   measured with respect to the picture carrier, at f = 600 MHz.

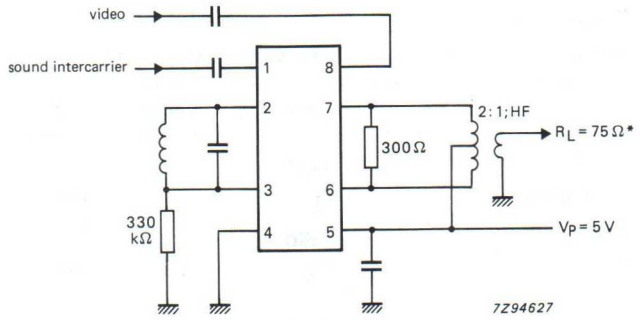


Fig. 2.
Application for negative modulation.

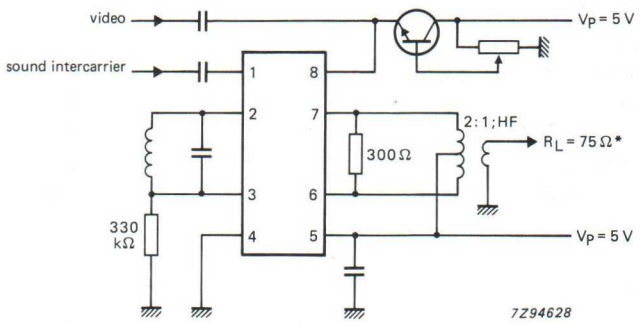


Fig. 3.
Application for positive modulation.

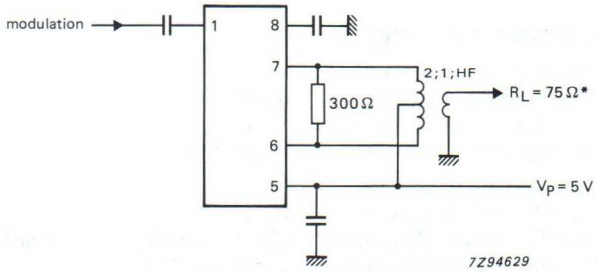


Fig. 4.
Application for general purpose modulation.

* Close to output transformer.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

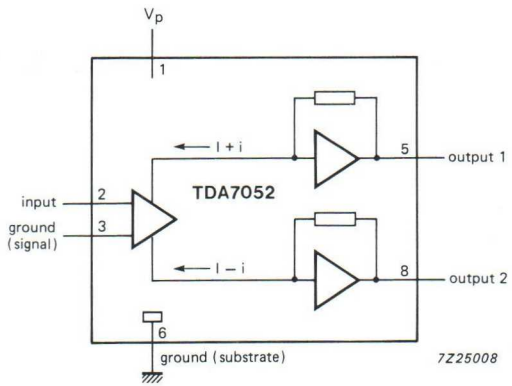


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	R_L = 8 Ω; V_P = 6 V	1.0	1.1	–	W
	TDA7052AT	R_L = 16 Ω; V_P = 6 V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

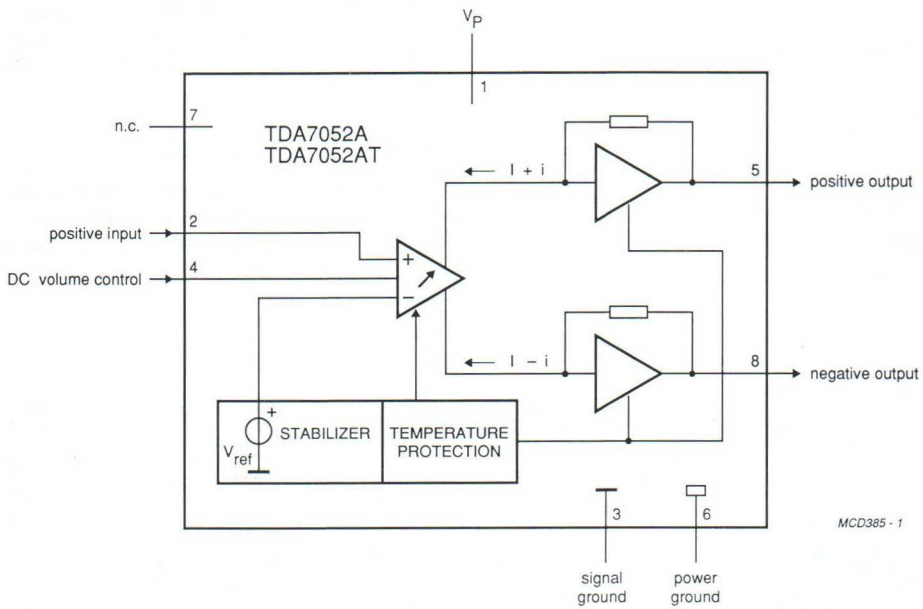


Fig.1 Block diagram.

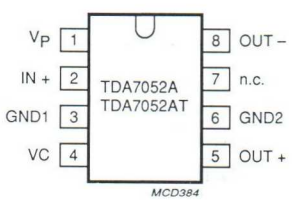


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

Mono BTL audio amplifier with DC volume control

TDA7052B; TDA7052BT

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7052B; BT are 1 W and 0.5 W mono BTL output amplifiers with DC volume control. They have been designed for use in TV and monitors, but are also suitable for use in battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power					
	TDA7052B	R_L = 8 Ω; V_P = 6 V	0.9	1.0	–	W
	TDA7052BT	R_L = 16 Ω; V_P = 6 V	0.5	0.55	–	W
G_v	maximum total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	9.2	13	mA
THD	total harmonic distortion					
	TDA7052B	P_O = 0.5 W	–	0.3	1	%
	TDA7052BT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052B	8	DIL	plastic	SOT97DE
TDA7052BT	8	SO8	plastic	SOT96AG

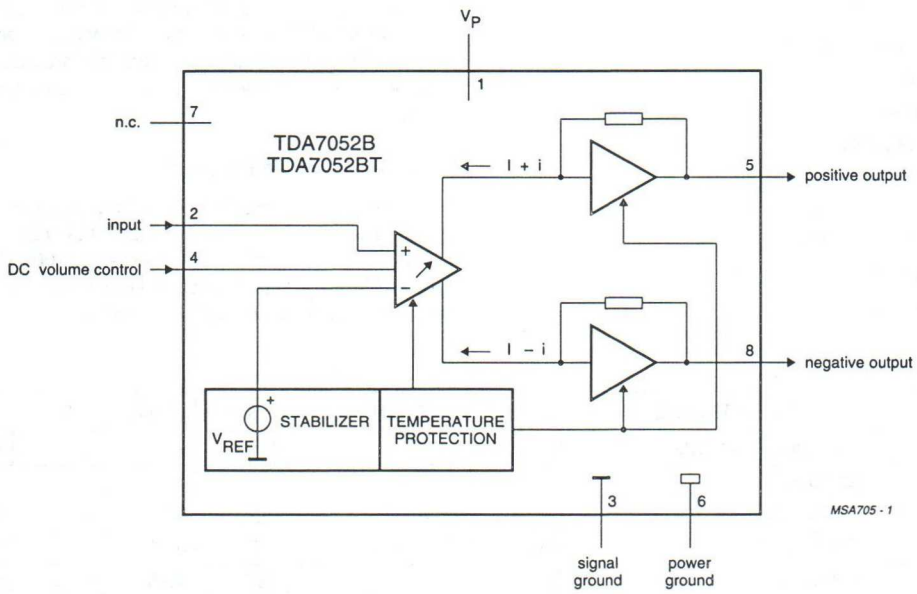


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

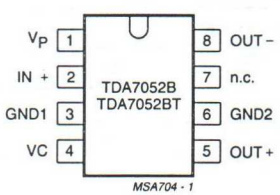


Fig.2 Pin configuration.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	18	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_v	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

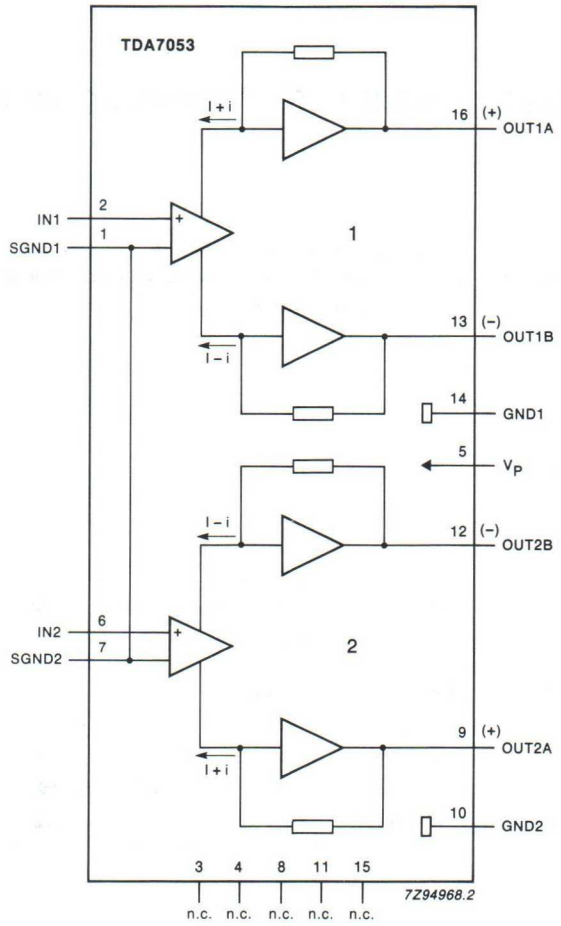


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

Stereo BTL audio output amplifiers with DC volume control

TDA7053A; TDA7053AT

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2 x 1 W) and TDA7053AT (2 x 0.5 W) are stereo BTL output amplifiers wih DC volume control. The devices are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	–	W
	TDA7053AT	R_L = 16 Ω	0.5	0.55	–	W
G_v	total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control range		68	73.5	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	15	25	mA
THD	total harmonic distortion					
	TDA7053A	P_O = 0.5 W	–	0.3	1	%
	TDA7053AT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7053A	16	DIL	plastic	SOT38
TDA7053AT	16	mini-pack	plastic	SOT162A

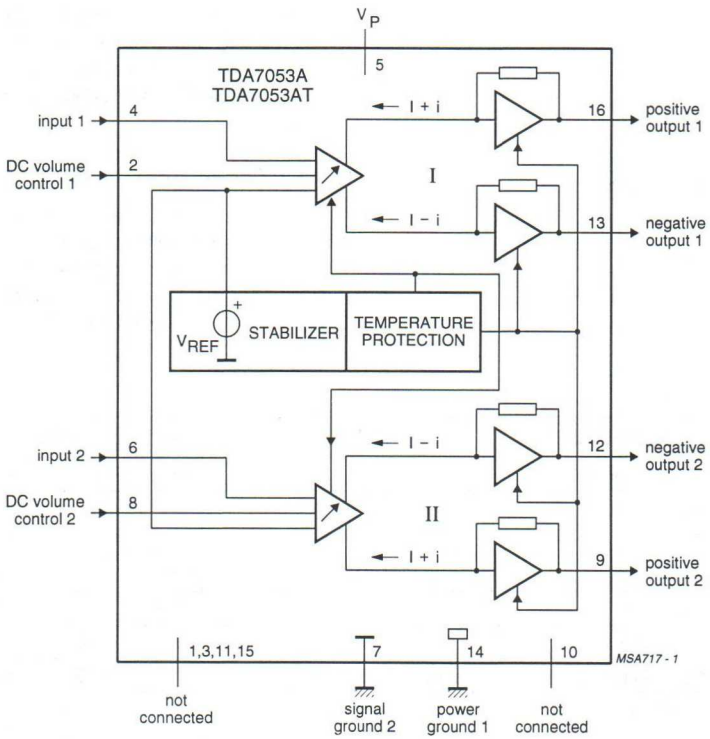


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume control 1
n.c.	3	not connected
$V_{I(1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I(2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume control 2
OUT2+	9	positive output 2
n.c.	10	not connected
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
PGND	14	power ground
n.c.	15	not connected
OUT1+	16	positive output 1

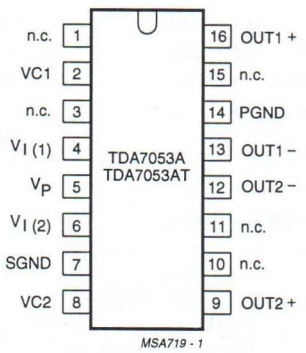


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7053A and TDA7053AT are stereo output amplifiers with two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.
In convential DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
The two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and yet a low offset voltage is maintained. Also the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to –33 dB.
If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	May 1992

TDA7056

3 Watt mono BTL audio output amplifier

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	2.5	3	-	W
G_V	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110

3 Watt mono BTL audio output amplifier TDA7056

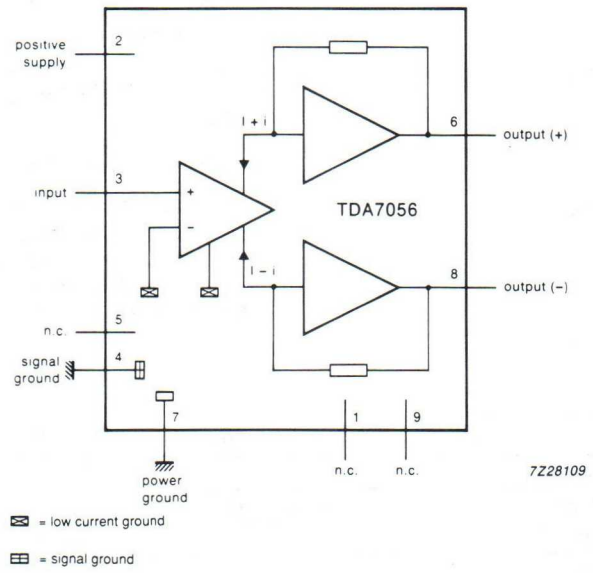


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (-)
9	n.c.

FUNCTIONAL DESCRIPTION

The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television.

For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.

The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power	R_L = 16 Ω; V_P = 12 V	3	3.5	–	W
G_v	voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	8	16	mA
THD	total harmonic distortion	V_P = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

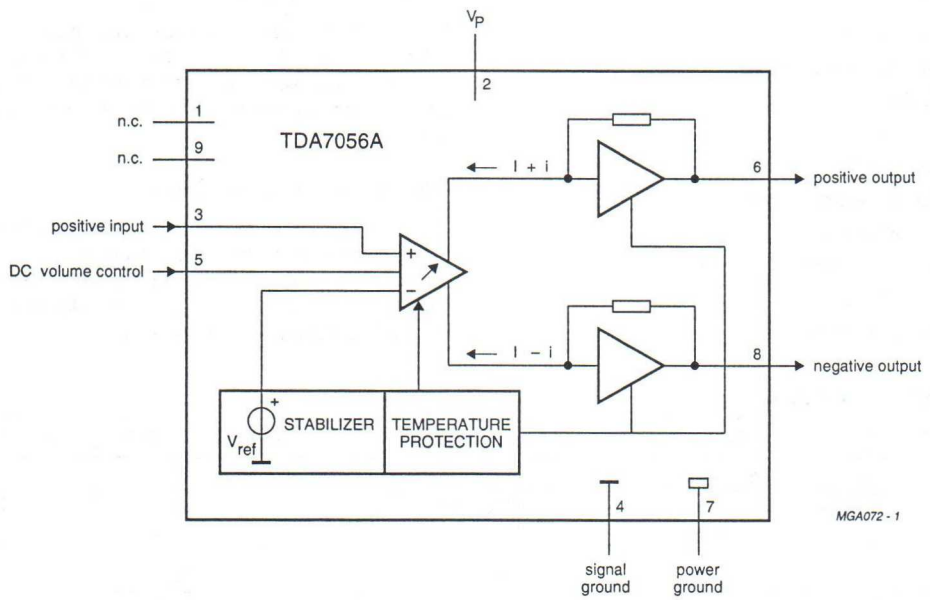


Fig.1 Block diagram.

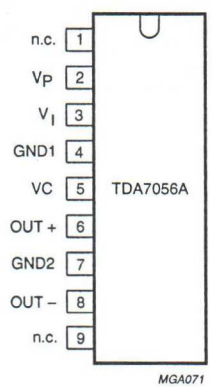


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

5 W mono BTL audio amplifier with DC volume control

TDA7056B

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056B is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but is also suitable for battery-fed portable recorders and radios. The device is contained in a 9-pin medium power package.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 12 V				
		R_L = 16 Ω	3	3.5	–	W
		R_L = 8 Ω	–	5	–	W
G_v	maximum voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	9.2	13	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056B	9	SIL	plastic	SOT110BE

5 W mono BTL audio amplifier with DC volume control

TDA7056B

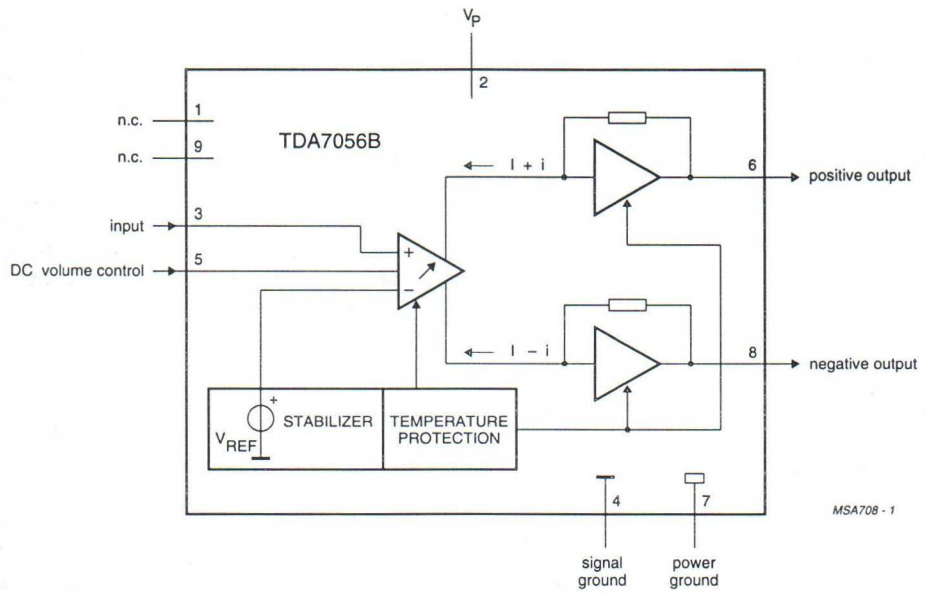


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

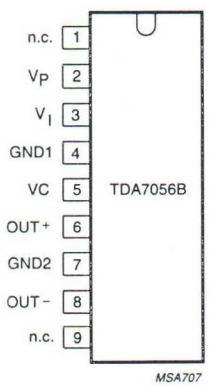


Fig.2 Pin configuration.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier wih DC volume control in a 13-pin medium power package. The device is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		4.5	–	18	V
P_O	output power	V_P = 12 V				
	R_L = 16 Ω		3	3.5	–	W
	R_L = 8 Ω		–	5	–	W
G_v	total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control range		68	73.5	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	15	25	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057AQ	13	SBD	plastic	SOT141

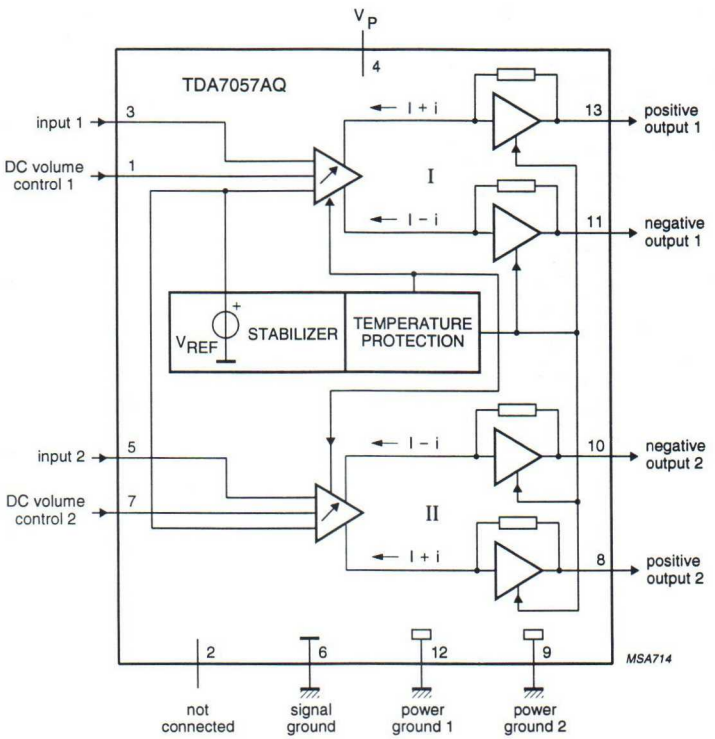


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

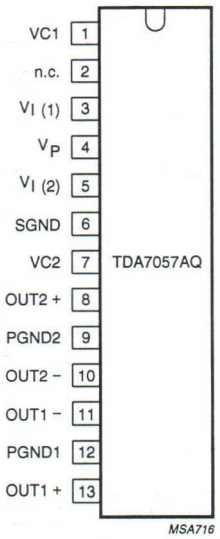


Fig.2 Pin configuration.

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FEATURES

- No external components
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Short-circuit proof
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057Q is a stereo output amplifier in a 13 pin power package. The device is designed for battery-fed portable stereo recorders and radios, but also suitable for mains-fed applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
P_O	output power	V_P = 11 V; R_L = 16 Ω	–	3	–	W
G_v	voltage gain		39	40	41	dB
I_P	total quiescent current	V_P = 11 V; R_L = ∞	–	10	14	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057Q	13	SBD	plastic	SOT141

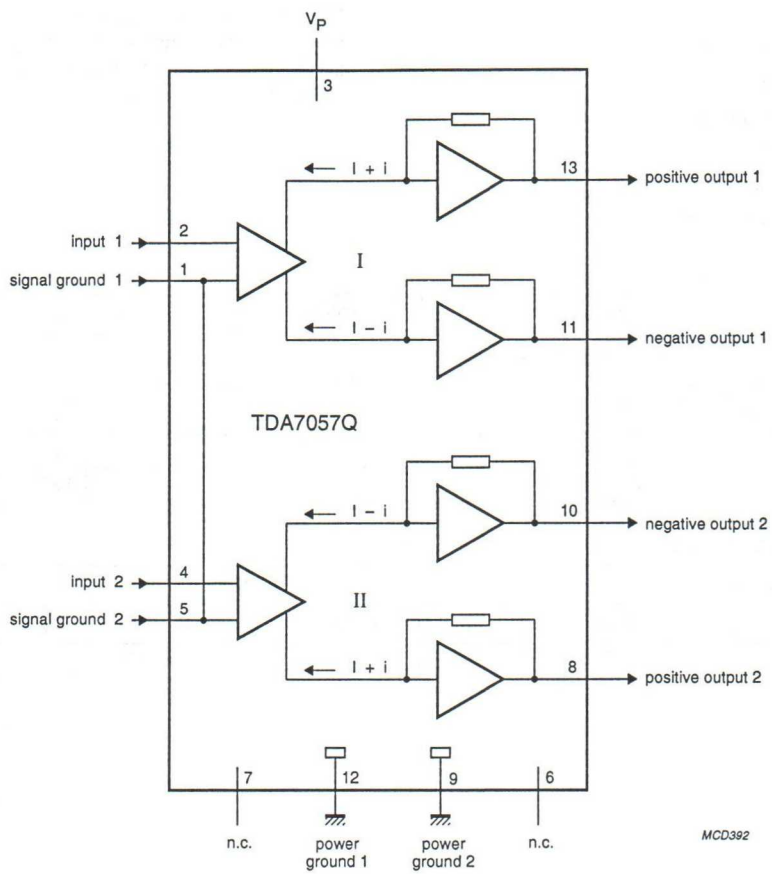


Fig.1 Block diagram.

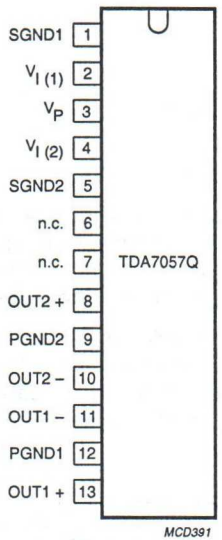


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
SGND1	1	signal ground 1
$V_{I(1)}$	2	voltage input 1
V_P	3	positive supply voltage
$V_{I(2)}$	4	voltage input 2
SGND2	5	signal ground 2
n.c.	6	not connected
n.c.	7	not connected
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

FUNCTIONAL DESCRIPTION

The TDA7057Q is a stereo output amplifier, designed for battery-fed applications e.g. portable radios, but also suitable for mains fed applications. The gain is internally fixed at 40 dB.

For space reason there is a trend to decrease the number of battery cells. This means a decrease in supply voltage, resulting in a reduction of output power at conventional output stages. The latter is not preferred. Using the BTL principle increases the output power.

The TDA7057Q can deliver an output power of 3 W in a speaker load of 16 Ω with 11 V supply.

The circuit is designed such that no external components are required. Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability. The load can be short-circuited at all input conditions.

Smart card interface | TDA8000

FEATURES

- Two protected I/O lines
- V_{CC} regulation (5 V ±4%, 100 mA max. with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V ±2.5%, 50 mA max. programmable by two bits, with controlled rise and fall times)
- Clock generation (up to 8 MHz)
- Short-circuit, thermal and take-off protections
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and deactivation sequences via an independent internal clock
- Enhanced ESD protections on card side (4 kV min.)
- ISO 7816 approval.

APPLICATIONS

- Pay TV
- Telematics
- Cashless payment
- Multipurpose card-readers, etc.

GENERAL DESCRIPTION

The TDA8000 is a complete, low-cost analog interface which can be positioned between a smart card or a memory card (ISO 7816) and a microcontroller. It is approved for banking, telecom and pay TV applications.

The complete supply, protection and control functions are realized with only some external components, making this product very attractive for consumer applications. Application report and support is available on request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; V_{DD} = 12 V	–	25	–	mA
		active modes; unloaded	–	32	–	mA
V_{th2}	threshold voltage on V_{SUP}		4.5	–	4.68	V
V_{CC}	card supply voltage		4.8	5.0	5.2	V
I_{CC}	card supply current		–	–	–100	mA
V_H	HIGH voltage supply for V_{PP}		–	–	30	V
I_{PP}	programming current	read mode; V_{PP} = 5 V	–	–	–50	mA
		write mode; V_{PP} > 5 V	–	–	–50	mA
t_{de}, t_{act}	deactivation/activation cycle duration		–	–	500	µs
P_{tot}	continuous total power dissipation	TDA8000; T_{amb} = 0 to +70 °C	–	–	2	W
		TDA8000T; T_{amb} = 0 to +70 °C	–	–	0.92	W
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	MATERIAL	CODE
TDA8000	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8000T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC18 OR DATA SHEET

BLOCK DIAGRAM

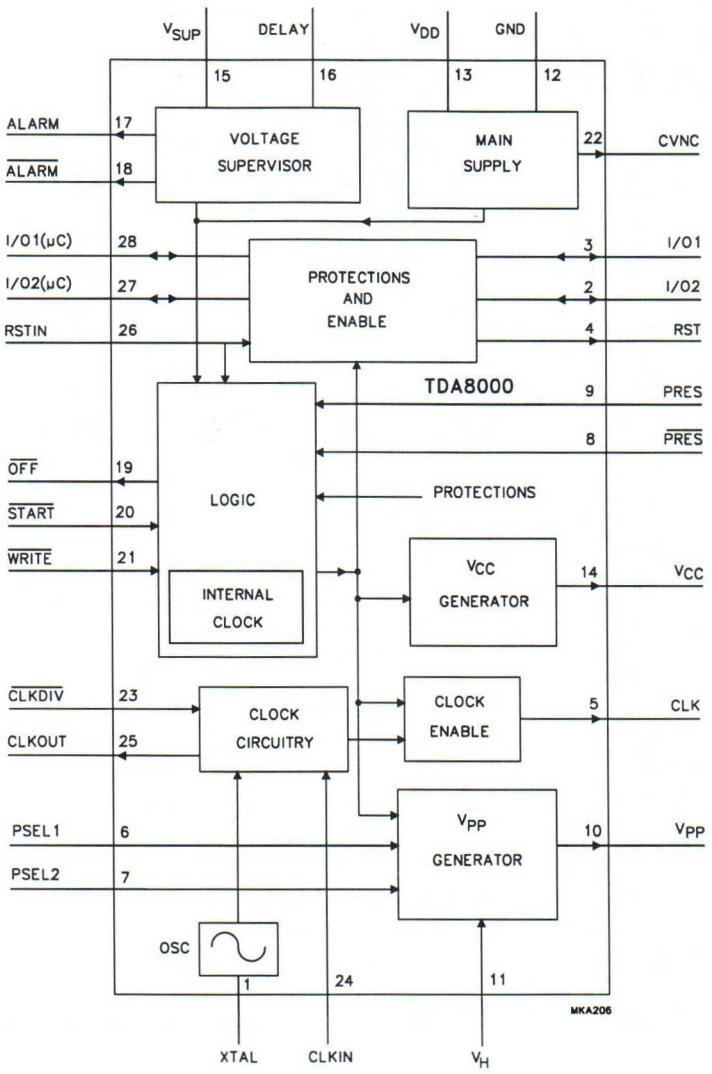


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal connection
I/O2	2	data line to/from the card
I/O1	3	data line to/from the card
RST	4	card reset output
CLK	5	clock output to the card
PSEL1	6	programming voltage selection input
PSEL2	7	programming voltage selection input
$\overline{PRES}$	8	card presence contact input (active LOW)
PRES	9	card presence contact input (active HIGH)
V_{PP}	10	card programming voltage output
V_H	11	high voltage supply for V_{PP} generation
GND	12	ground
V_{DD}	13	positive supply voltage
V_{CC}	14	card supply output voltage
V_{SUP}	15	voltage supervisor input
DELAY	16	external capacitor connection for delayed reset timing
ALARM	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{ALARM}$	18	open-collector reset output for the microcontroller (active LOW)
$\overline{OFF}$	19	interrupt output to the microcontroller (active LOW)
$\overline{START}$	20	microcontroller input for starting session (active LOW)
$\overline{WRITE}$	21	control input for applying programming voltage to the card (active LOW)
CVNC	22	internally generated 5 V reference, present when V_{DD} is on; to be decoupled externally (47 nF)
$\overline{CLKDIV}$	23	input for dividing/not dividing the CLKOUT frequency by two (active LOW)
CLKIN	24	external clock signal input
CLKOUT	25	clock output to the microcontroller, or another TDA8000
RSTIN	26	card reset input from the microcontroller (active HIGH)
I/O2(μC)	27	data line to/from the microcontroller; must not be left open-circuit, if not used tie to CVNC
I/O1(μC)	28	data line to/from the microcontroller; must not be left open-circuit, if not used tie to CVNC

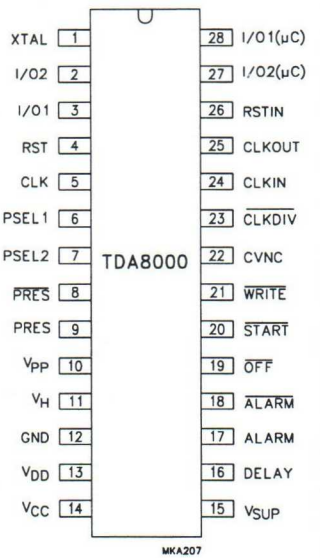


Fig.2 Pin configuration.

Smart card interface TDA8001

FEATURES

- Protected I/O line
- V_{CC} regulation (5 V ±5%, 100 mA max. with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V ±2.5%, 50 mA max., with controlled rise and fall times)
- CLOCK generation (up to 12 MHz), with synchronous frequency doubling
- Overloads, thermal and take-off protections
- Current limitations in case of short-circuit
- Idle mode and special circuitry for spikes killing during powering on and off
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and deactivation sequences through an independent internal clock
- Enhanced ESD protections on card side (6 kV min.)
- Easy chaining for multiple card readers
- ISO 7816 compatibility, GSM11-11 and banking specification capability.

APPLICATIONS

- Pay TV (multistandards conditional access system, videoguard, newscript, Euroscript)
- Multiapplications smart card readers (banking, vending machine, electronic payment identification).

GENERAL DESCRIPTION

The TDA8001 is a complete, low-cost analog interface which can be positioned between an asynchronous smart card (ISO 7816) and a microcontroller.

The complete supply, protection and control functions are realized with only some external components, making this product very attractive for consumer applications.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8001	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8001T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8001A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8001AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC18 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; V_{DD} = 12 V	–	32	–	mA
		active modes; unloaded	–	45	–	mA
V_{th2}	threshold voltage on V_{SUP}		4.5	–	4.72	V
V_{th4}	threshold voltage on V_{DD}		6	–	6.5	V
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	100	mA
		detection	–	150	–	mA
		limitation	–	–	200	mA
V_H	HIGH voltage supply for V_{PP}		–	–	30	V
V_{PP}	card programming voltage (P = 5, 12.5, 15 and 21 V)	including static and dynamic loads on 100 nF capacitor	P – 2.5%	–	P + 2.5%	V
I_{PP}	programming current (read or write mode)	operating	–	–	–50	mA
		detection	–	–75	–	mA
		limitation	–	–	–100	mA
SR	slew rate on V_{CC} and V_{PP} (rise and fall)	maximum load capacitor 150 nF	–	0.38	–	V/µs
t_{de}	deactivation cycle duration		75	100	125	µs
f_{clk}	clock frequency		0	–	12	MHz
P_{tot}	continuous total power dissipation	TDA8001; T_{amb} = 0 to +70 °C	–	–	0.92	W
		TDA8001T; T_{amb} = 0 to +70 °C	–	–	2	W
T_{amb}	operating ambient temperature		0	–	+70	°C

BLOCK DIAGRAM

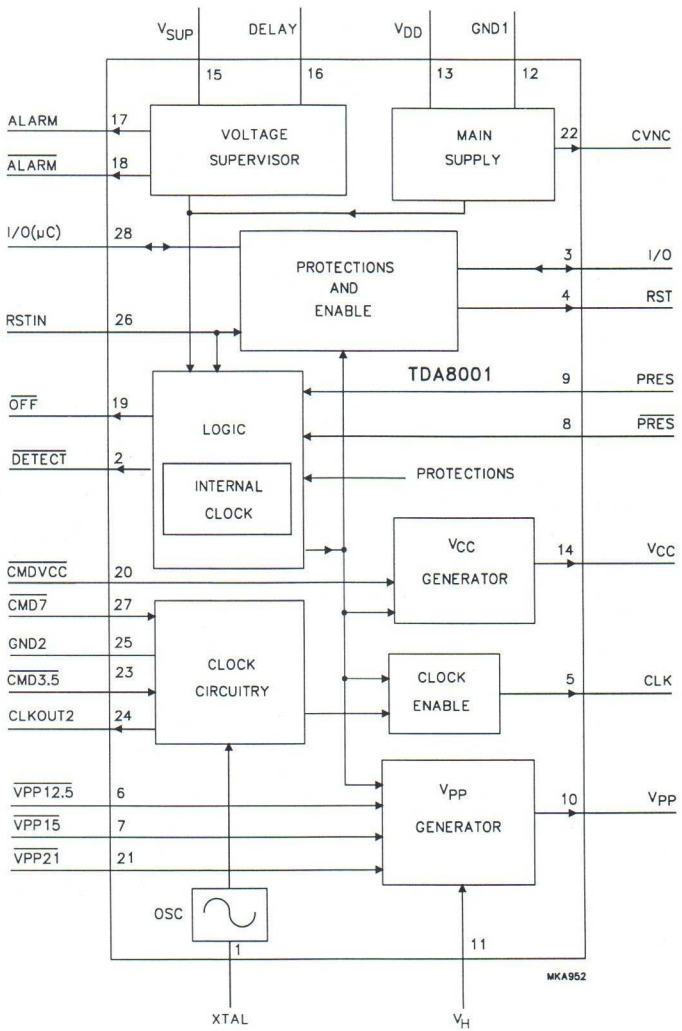


Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT117-1	SOT136-1	
XTAL	1	1	crystal connection
$\overline{\text{DETECT}}$	2	2	card take-off open collector output (active LOW)
I/O	3	3	data line to/from the card
RST	4	4	card reset output
CLK	5	5	clock output to the card
$\overline{\text{VPP12.5}}$	6	n.c.	control input for applying the 12.5 V programming voltage (active LOW)
$\overline{\text{VPP15}}$	7	n.c.	control input for applying the 15 V programming voltage (active LOW)
$\overline{\text{PRES}}$	8	8	card presence contact input (active LOW)
PRES	9	9	card presence contact input (active HIGH)
V_{PP}	10	n.c.	card programming voltage output
V_H	11	11	HIGH voltage supply for V_{PP} generation
GND1	12	12	ground 1
V_{DD}	13	13	supply voltage
V_{CC}	14	14	card supply output voltage
V_{SUP}	15	15	voltage supervisor input
DELAY	16	16	external capacitor connection for delayed reset timing
ALARM	17	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{\text{ALARM}}$	18	18	open-collector reset output for the microcontroller (active LOW)
$\overline{\text{OFF}}$	19	19	open-collector interrupt output to the microcontroller (active LOW)
$\overline{\text{CMDVCC}}$	20	20	control input for applying supply voltage to the card (active LOW)
$\overline{\text{VPP21}}$	21	n.c.	control input for applying the 21 V programming voltage (active LOW)
CVNC	22	22	Internally generated 5 V reference, present when V_{DD} is on. To be decoupled externally (47 nF).
$\overline{\text{CMD3.5}}$	23	23	control input for having the crystal frequency divided-by-4 at pin CLK
CLKOUT2	24	24	clock output to the microcontroller, or any other R4590 (crystal frequency divided-by-two)
GND2	25	25	ground 2
RSTIN	26	26	card reset input from the microcontroller (active HIGH)
$\overline{\text{CMD7}}$	27	27	control input for having the crystal frequency divided-by-2 at pin CLK
I/O(μC)	28	28	data line to/from the microcontroller

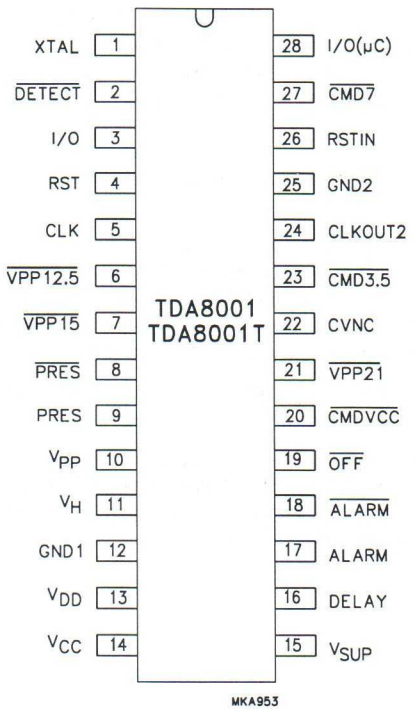


Fig.2 Pin configuration (DIP28).

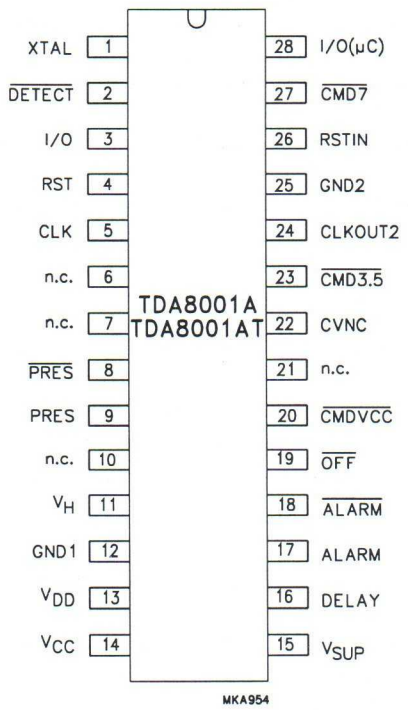


Fig.3 Pin configuration (SO28).

Low-power smart card coupler TDA8005

FEATURES

- V_{CC} generation (5 V ±5%, 20 mA max. with controlled rise and fall times)
- CLOCK generation (up to 8 MHz), with two times synchronous frequency doubling
- CLOCK STOP HIGH, STOP LOW or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816 and GSM11.11 requirements; Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications (doubler or tripler DC/DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads, thermal and take-off protections
- Current limitations in case of short-circuit
- Special circuitry for spikes killing during power on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low-power consumption
- Enhanced ESD protections on card side (6 kV min.)
- Control and communication through a standard RS232 full duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- CL51 core with 4 kbytes ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005 is a low cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11-11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low-power consumption in Power-down and sleep modes saves battery power. A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a standard CL51 controller.

Development tools, application report and support (hardware and software) are available.

The device can be supplied either as a masked chip with standard software handling all communication between smart card and a master controller in order to make the application easier, or as a maskable device.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.5	–	6	V
I_{DD}	supply current	Power-down mode; V_{DD} = 5 V; card inactive	–	–	100	µA
		sleep mode; card powered but clock stopped	–	–	500	µA
		operating mode; unloaded; f_{xtal} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	–	5.5	mA
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	30	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 150 nF (including typical 100 nF decoupling)	0.05	0.1	0.15	V/µs
t_{de}	deactivation cycle duration				100	µs
t_{act}	activation cycle duration				100	µs
f_{xtal}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005G	TQFP64[1]	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

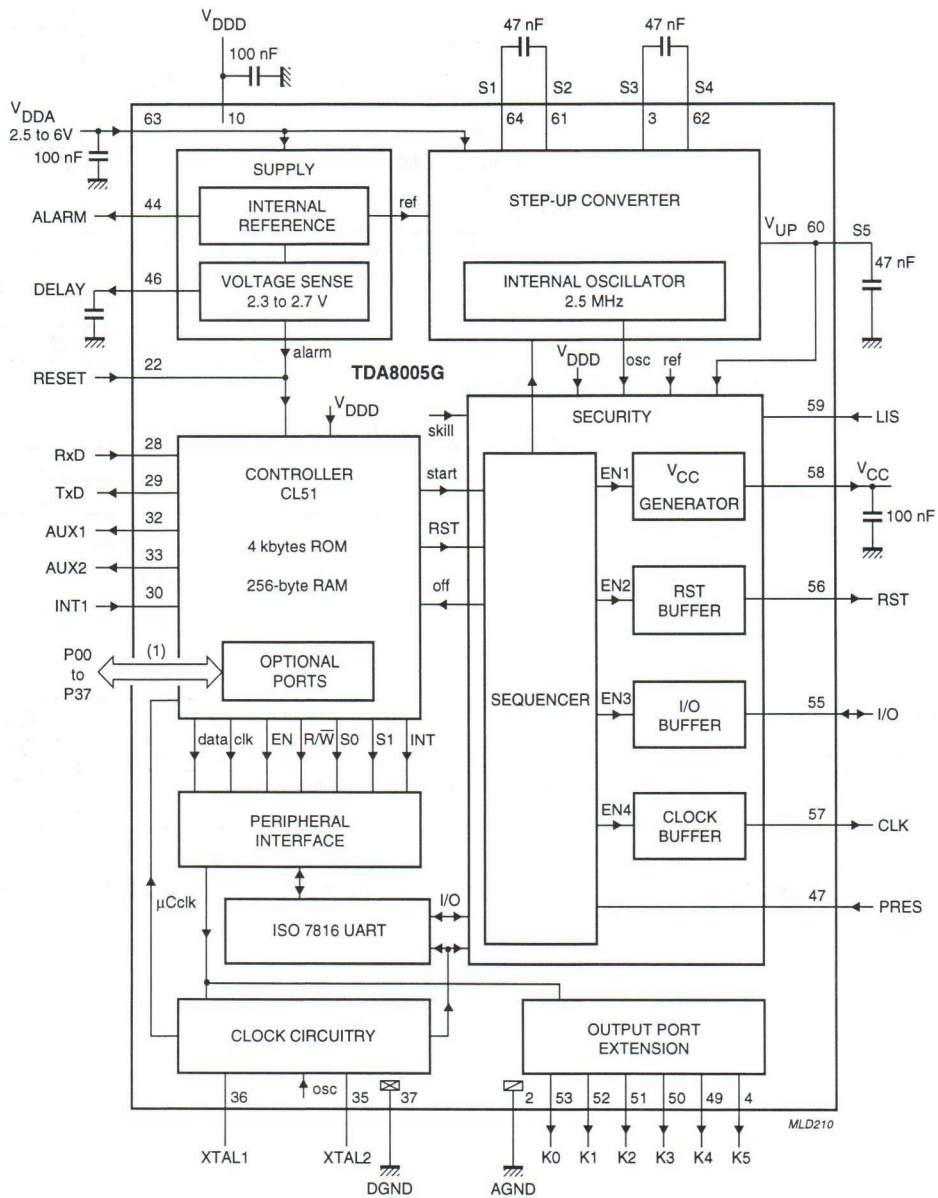


Fig.1 Block diagram (TQFP64; SOT314-2).

PINNING

SYMBOL	PIN		DESCRIPTION
	TQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to P03)
P02	6	4	general purpose I/O port (connected to P02)
P01	7	5	general purpose I/O port (connected to P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to P11)
P12	14	10	general purpose I/O port or interrupt (connected to P12)
P13	15	11	general purpose I/O port or interrupt (connected to P13)
P14	16	12	general purpose I/O port or interrupt (connected to P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to P15)
P16	19	14	general purpose I/O port or interrupt (connected to P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to P33)
T0	31	21	general purpose I/O port (connected to P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer P36)
P37	34	24	general purpose I/O port (connected to P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	TQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to P20)
P21	41	–	general purpose I/O port (connected to P21)
P22	42	29	general purpose I/O port (connected to P22)
P23	43	30	general purpose I/O port (connected to P23)
ALARM	44	–	open-drain output for Power-On Reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

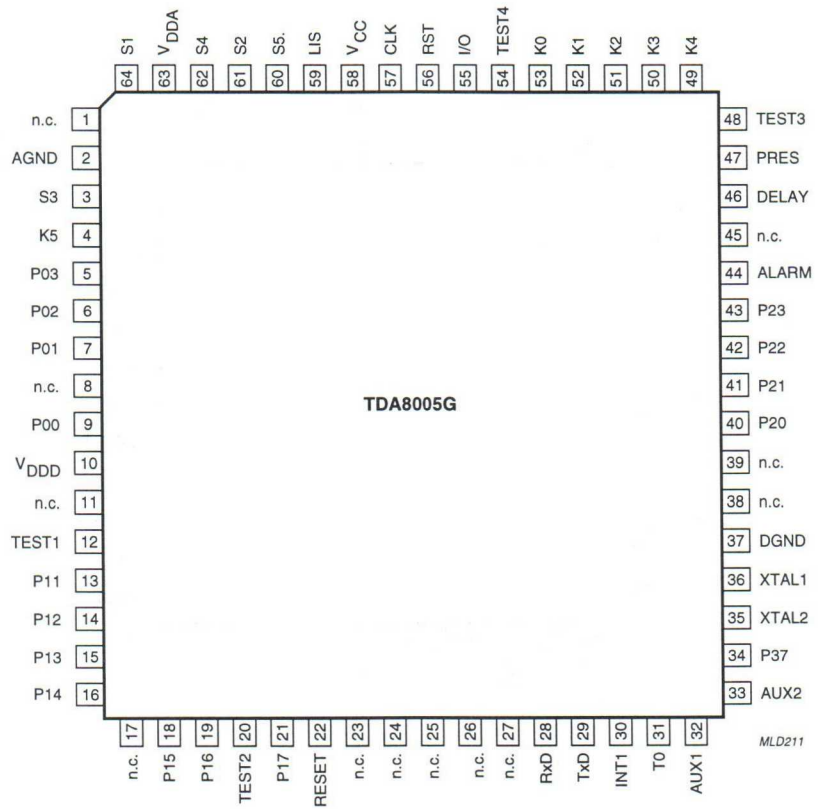


Fig.2 Pin configuration (TQFP64; SOT314-2).

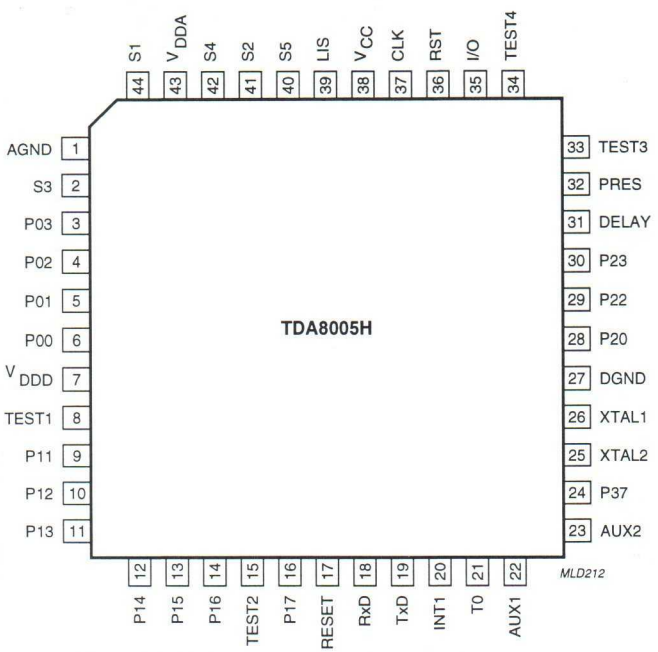


Fig.3 Pin configuration (QFP44; SOT307-2).

IF amplifier for satellite TV receivers TDA8011T

FEATURES

- High voltage gain, up to 860 MHz
- Low noise
- Large dynamic gain control
- High impedance differential input stage
- Low output impedance.

APPLICATIONS

- Second IF amplifier for satellite TV receivers.

DESCRIPTION

The TDA8011T is a broadband low-noise AGC amplifier which is used for the second IF amplifier in satellite TV receivers. The amplifier is powered from a single 5 V supply. The amplifier gain can be easily controlled over a large dynamic range by using a single ground reference voltage. The two outputs are 180° out of phase and are separately buffered. The two outputs can therefore, be used in either the differential or asymmetrical mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	V_{CC} = 5 V; T_{amb} = 25 °C; I_{AGC} = 0 mA	27	35	45	mA
V_i	input voltage level		–	–	96	dBμV
V_o	output voltage level		–	–	85	dBμV
$G_{v(max)}$	maximum voltage gain		25	–	–	dB
$G_{v(min)}$	minimum voltagegain		–	–	–21	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8011T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

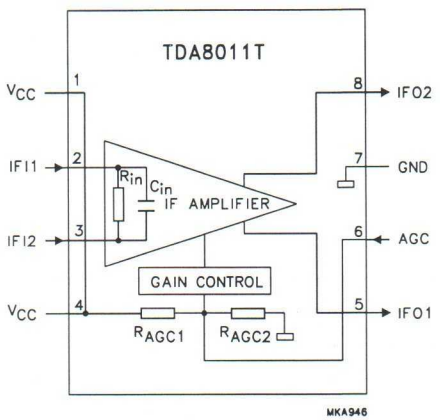


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	supply voltage
IFI1	2	IF input 1
IFI2	3	IF input 2
V_{CC}	4	supply voltage
IFO1	5	IF output 1
AGC	6	AGC input
GND	7	ground
IFO2	8	IF output 2

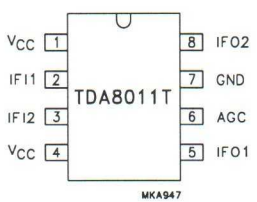


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6.0	V
$V_{(max)}$	maximum voltage on all pins	−0.3	V_{CC}	V
$I_{source(max)}$	maximum output source current	–	10	mA
$t_{sc(max)}$	maximum short-circuit time on outputs	–	10	s
T_{stg}	storage temperature	−55	+150	°C
T_j	junction temperature	–	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	160	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{CC} = 5 V; f_i = 70, 480 and 610 MHz; T_{amb} = 25 °C; measured in application circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current		27	35	45	mA
IF amplifier						
$G_{v(max)}$	maximum voltage gain	$V_{AGC} = 0.9V_{CC}$; note 1	25	–	–	dB
$G_{v(min)}$	minimum voltage gain	$V_{AGC} = 0.1V_{CC}$; note 1	–	–	−21	dB
ΔG	tilt	Δf_i = 20 MHz; note 2	–	0.4	–	dB
V_i	input voltage level		–	–	96	dBμV
$V_{I(DC)}$	DC input voltage level		–	2.5	–	V
V_o	output voltage level		–	–	85	dBμV
$V_{O(DC)}$	DC output voltage level		–	2.2	–	V
F	noise figure	unmatched configuration; note 3	–	–	15	dB
$F_{(min)}$	minimum noise figure	note 4	–	–	11	dB
IM3	third-order intermodulation distance	note 5	–	40	–	dB
$R_{i(diff)}$	differential input resistance	note 6	–	4	–	kΩ
$C_{i(diff)}$	differential input capacitance	note 6	–	0.75	–	pF
$R_{o(SE)}$	single-ended output resistance		–	50	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain control						
V_{AGC}	AGC input voltage	$G \leq G_{v(min)}$	$0.1V_{CC}$	–	–	V
		$G \geq G_{v(max)}$	–	–	$0.9V_{CC}$	V
R_{AGC1}	AGC resistor 1		–	4.3	–	kΩ
R_{AGC2}	AGC resistor 2		–	110	–	kΩ

Notes

1. The voltage gain G_v is defined as the ratio between the single-ended output voltage and the differential input voltage with a 150 Ω output load: $G = 20 \times \log\left(\frac{V_{IFO}}{V_i}\right)$
2. The tilt is defined as the maximum absolute difference between the gain at the frequency f_o = 480 MHz and the gain at the frequency f_o = 480 MHz ±20 MHz. Where $\Delta G_v = \max |G(f_o \pm \Delta f) - G(f_o)|$
3. The unmatched noise figure (F) is measured at f_i = 480 MHz in the application circuit (see Fig.6). With the hybrid coupler used, the equivalent source impedance is equal to 100 Ω.
4. The minimum noise figure [$F_{(min)}$] is measured at f_i = 480 MHz with the input matching circuit shown in Fig.3; (L1: 4.5 turns on, Φ_{int} = 3 mm, wire = 0.4 mm; L2: 11 turns on, Φ_{int} = 3 mm, wire = 0.4 mm).
5. The third-order intermodulation distance (IM3) is measured with an AGC voltage set to obtain a gain of –17 dB. The input signal applied to the amplifier consists of two sine wave signals at f_i = 479.5 MHz and f_i = 480.5 MHz with an amplitude equal to 90 dBμV for each tone.
6. The differential input impedance is represented by an equivalent parallel resistance and capacitance as shown in Fig.1. The specified values are measured at f_i = 480 MHz.

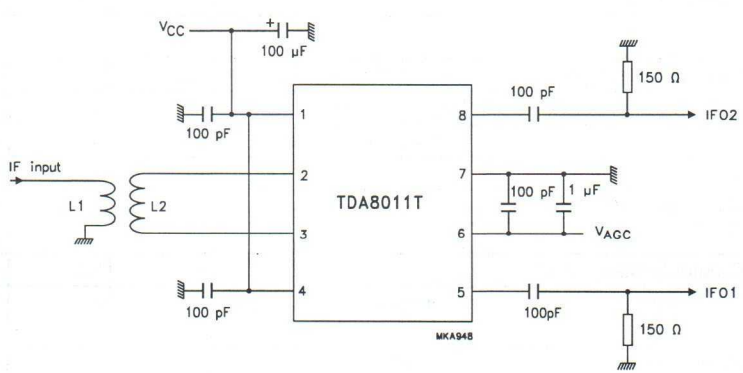


Fig.3 Input matching circuit.

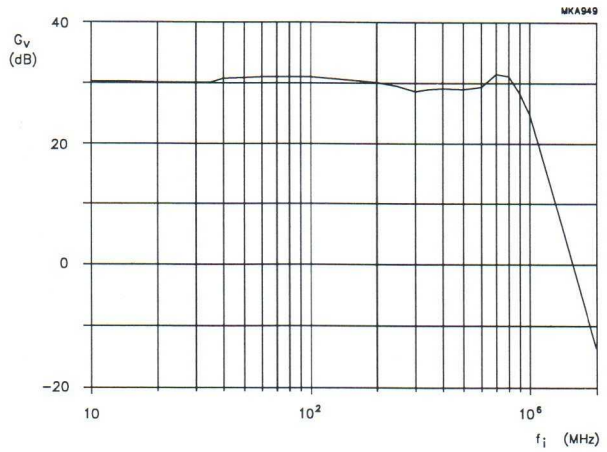


Fig.4 Typical frequency response curve.

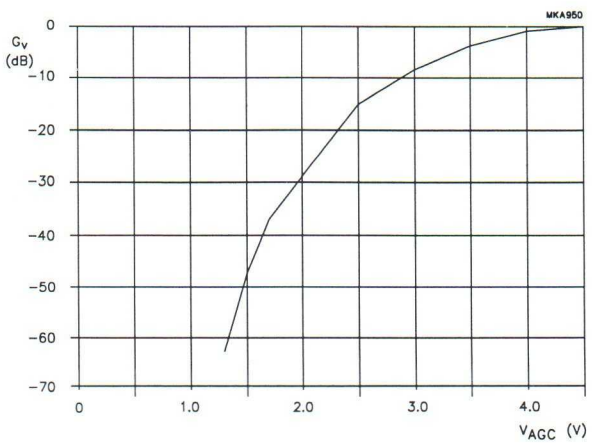


Fig.5 Typical gain control response curve.

APPLICATION INFORMATION

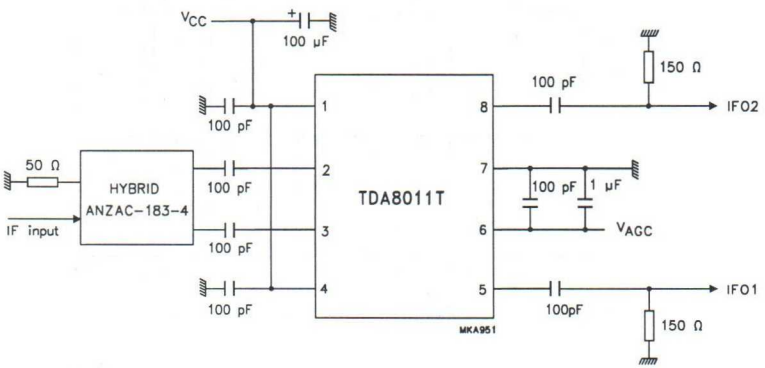


Fig.6 Application circuit.

Low power PLL FM demodulator for satellite TV receivers

TDA8012M

FEATURES

- High input sensitivity
- Fully balanced two-pin Voltage Controlled Oscillator (VCO)
- Low input impedance (50 Ω)
- Low impedance video baseband output
- Internal voltage stabilizer
- Keyed AFC or peak-to-peak AFC
- Carrier detector
- AGC output
- Suitable for High Definition TV (HDTV).

APPLICATIONS

- Direct Broadcast Satellite (DBS) receivers.

GENERAL DESCRIPTION

The TDA8012M is a sensitive PLL FM demodulator which is used for the second IF in satellite receivers. It provides Automatic Gain Control (AGC) and Automatic Frequency Control (AFC) outputs that can be used to optimize the level and the frequency of the signal applied to the input. During the searching procedure, the AFC output provides a signal which is used for carrier detection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	V_{CC} = 5 V; T_{amb} = 25 °C	50	60	70	mA
V_i	input signal voltage level		53	57	61	dBμV
$V_{o(p-p)}$	video output signal voltage amplitude (peak-to-peak value)	Δf_o = 25 MHz (p-p)	–	1	–	V
f_i	operating input frequency		–	480	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGES		
	NAME	DESCRIPTION	VERSION
TDA8012M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

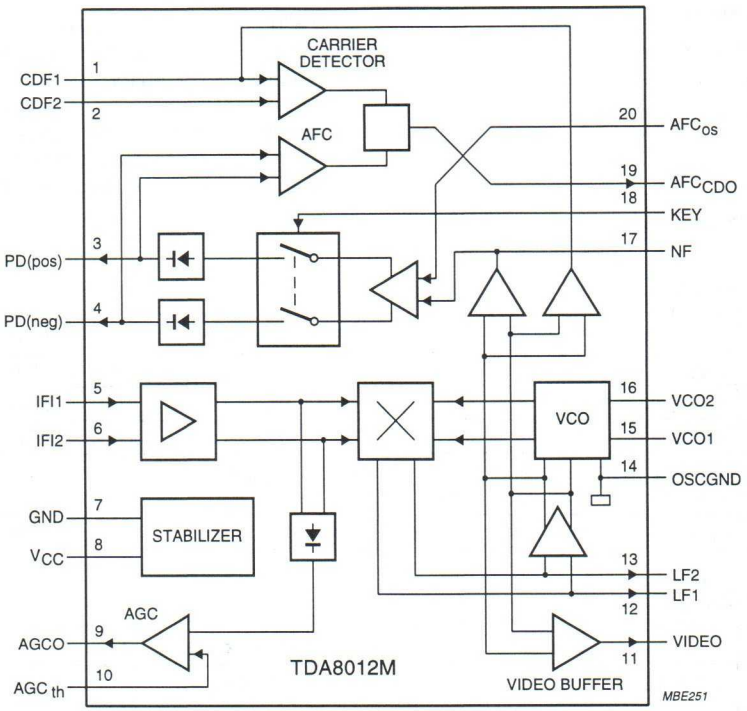


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CDF1	1	carrier detector filter 1 input
CDF2	2	carrier detector filter 2 input
PD(pos)	3	positive peak detector output
PD(neg)	4	negative peak detector output
IFI1	5	IF input 1
IFI2	6	IF input 2
GND	7	ground
V_{CC}	8	supply voltage
AGCO	9	AGC output
AGC_{th}	10	AGC threshold voltage input
VIDEO	11	baseband signal output
LF1	12	loop filter 1 input
LF2	13	loop filter 2 input
OSCGND	14	oscillator ground
VCO1	15	oscillator tank circuit 1 input
VCO2	16	oscillator tank circuit 2 input
NF	17	noise filter input
KEY	18	key pulse input
AFC_{CDO}	19	AFC and carrier detector output
AFC_{os}	20	AFC offset input

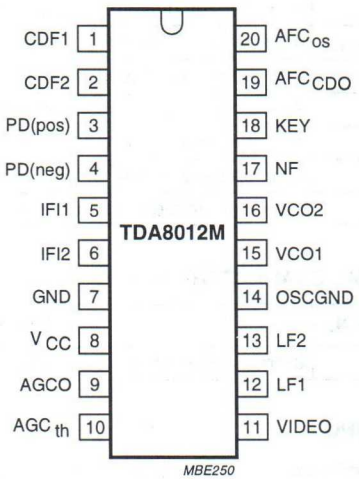


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8012M is a low power PLL FM demodulator designed for use in satellite TV reception systems.

The demodulator is based on a Phase-Locked Loop (PLL) structure including a fully balanced two-pin VCO. A high gain IF amplifier ensures a high input sensitivity. The video output voltage is supplied via a highly linear video buffer which has a low output impedance. The centre frequency of the VCO and the loop characteristics can be set using external components.

The circuit provides an AGC signal which is used to drive a gain-controlled IF amplifier (TDA8011T) to ensure a stable PLL demodulation characteristic.

An analog AFC voltage is also made available. This signal can be suitably applied to the input of the ADC port of the PLL frequency synthesizer (TSA5055). The AFC function may be keyed to address D2MAC and MUSE systems.

The TDA8012M includes a Carrier Detector (CD) which is used for channel detection during search procedures.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6.0	V
$V_{i(max)}$	maximum input voltage on all pins	−0.3	V_{CC}	V
$I_{source(max)}$	maximum output source current	–	10	mA
t_{sc}	maximum short-circuit time on all outputs	–	10	s
Z_L	AC load impedance at video output	600	–	Ω
T_{stg}	storage temperature	−55	+150	°C
T_j	junction temperature	–	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{CC} = 5 V; f_i = 480 MHz; V_i = 57 dBμV; T_{amb} = 25 °C; measured in application circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	note 1	50	60	70	mA
Voltage controlled oscillator						
K_{VCO}	voltage controlled oscillator constant	$4.75 < V_{CC} < 5.25$ V; T_{amb} = −10 to +80 °C	22.5	25	27.5	MHz/V
$\delta f_o/\delta T$	voltage controlled oscillator drift	note 2	–	-70×10^{-6}	–	$°C^{-1}$
Δf_o	voltage controlled oscillator shift	V_{CC} = 4.75 to 5.25 V	–	–	±750	kHz
Frequency demodulator						
V_i	input signal voltage level	note 3	53	57	61	dBμV
Z_i	input impedance	real part; note 4	–	50	–	Ω
		parallel inductive part; note 4	–	130	–	nH
K_{PD}	phase detector constant	V_i = 57 dBμV	–	0.37	–	V/rad
G_v	phase-lock loop gain	drift; note 5	–	2	–	dB
		shift; note 5	–	2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{o(diff)}$	differential output impedance of the phase detector		1.6	2	2.4	kΩ
CR_{PLL}	phase-lock loop capture range	note 6	–	±17	–	MHz
G_{diff}	differential gain	note 7	–	±2	–	%
Φ_{diff}	differential phase	note 7	–	±2	–	deg
IM3	third-order intermodulation distortion	note 8	50	–	–	dB
Video output						
$V_{o(p-p)}$	baseband output signal amplitude (peak-to-peak value)	Δf_o = 25 MHz	0.9	1.0	1.1	V
$V_{O(DC)}$	DC voltage level of video output		2.1	2.35	2.6	V
Z_o	output impedance		–	10	50	Ω
Automatic gain control (note 9)						
AGC_{th}	AGC threshold as a function of the voltage applied to pin 10	I_{AGC} = 0.5 mA; $0.1V_{CC}$	–	–	53	dBμV
		I_{AGC} = 0.5 mA; $0.9V_{CC}$	61	–	–	dBμV
LD	level detector	shift; V_{CC} = 4.75 to 5.25 V	–	1	–	dB
		drift; T_{amb} = −10 to +80 °C	–	1	–	dB
	AGC steepness	I_{AGC} = 0.5 mA; note 10	–	8	–	mA/dB
$V_{sat(AGC)}$	low level AGC output saturation voltage	I_{AGC} = 1 mA	–	200	500	mV
Keying pulse						
t_{key}	input keyed pulse time period		–	64	–	μs
$t_{W(key)}$	keyed pulse width		8	–	–	μs
V_{IL}	LOW level input keyed pulse voltage	key on	–	–	0.8	V
V_{IH}	HIGH level input keyed pulse voltage	key off	2.7	–	–	V
Z_i	input impedance		1	–	–	kΩ
AFC and carrier detector output (note 11)						
$\delta V_{AFC}/\delta_f$	AFC steepness		4.9	5.5	6.1	V/MHz
AFC_{shift}	shift of AFC voltage in relation to VCO shift with unmodulated 480 MHz input signal	ΔV_{CC} = ±5%	–	±180	±500	kHz
AFC_{drift}	drift of AFC voltage in relation to the VCO	T_{amb} = 80 °C; note 12	–	−400	–	kHz

Notes

1. The DC supply current is defined for V_{CC} = 5 V.
2. This typical value of -70×10^{-6} ppm/°C can be found in the reference measuring set-up shown in Fig.3. The temperature drift may be adjusted by the temperature coefficient of the external capacitor in the tank circuit.
3. The circuit is designed for an input level of 57 dBμV. The maximum allowable input level is 61 dBμV. However, for levels other than 57 dBμV the optimum loop filter values will be different from those given for the 57 dBμV input level in the reference measuring set-up.
4. The input impedance is reduced to a resistor with a parallel reactance. The values are given at 480 MHz. In order to reduce the radiation from the oscillator to the RF input, it is recommended to use a symmetrical drive.
5. The PLL loop gain shift and drift are given without loop filter shift and drift (non-temperature compensated external components).
6. The capture range or lock-in range is defined as the PLL normal operating range. This value depends strongly on the loop filter characteristics.
7. Measurements with test signals in accordance with CCIR recommendation 473-3. FM modulated signal with DBS parameters:
   a) 625 lines PAL TV system
   b) 25 MHz/V modulator sensitivity
   c) 1 V (p-p) video signal
   d) No SAW filter is used.
8. No SAW filter is used at the input:
   a) 16 MHz/V modulator sensitivity
   b) 4.43 MHz sine wave colour signal [660 mV (p-p)]
   c) 3.25 MHz sine wave luminance signal [700 mV (p-p)]
   d) Two Wegner sound sub-carriers at 7.02 and 7.2 MHz (100 mV)
   e) Intermodulation distance is defined as the distance between the luminance signal and the intermodulation products.
9. The characteristics of the AGC function are measured in the application circuit of Fig.4. The circuit illustrated in Fig.4 has been designed to set the maximum AGC current of 1 mA. The output of the AGC function is capable of handling up to 5 mA. The maximum AGC current can be increased to 5 mA by decreasing the value of the resistor connected between pins 8 and 9.
10. In the application circuit (see Fig.4) the voltage at the AGC output decreases when the IF input level increases above the adjusted AGC threshold.
11. The outputs from the AFC and carrier detector are combined at pin 19 (see Fig.3). During search tuning, when the input frequency is outside the capture range, the combined output (carrier detector function) is at a LOW level (any voltage below $0.6V_{CC}$). When the PLL becomes locked, the voltage at pin 19 rises to a HIGH level ($V_{19} = 0.8V_{CC}$ to V_{CC}). When the input channel is close to the centre frequency, V_{19} falls to the LOW level. As shown in Fig.3, the voltage at pin 19 is now a function of the centre frequency (AFC function). This information may be read by a microcontroller via the ADC of the satellite frequency synthesizer (TSA5055) and the I^2C-bus.
12. The drift of the AFC voltage is measured in accordance with the following method:
    a) At room temperature (T_{amb} = 25 °C) the TDA8012M is driven by a 480 MHz unmodulated signal. The voltage at pin 20 must be adjusted to obtain a 1.5 V output at the AFC output (pin 19).
    b) At T_{amb} = 80 °C, due to its temperature drift, the AFC output voltage differs from 1.5 V. The input frequency must, therefore, be adjusted to obtain 1.5 V at the AFC output. The drift of the AFC voltage will then be equal to the difference between the new input frequency and 480 MHz.

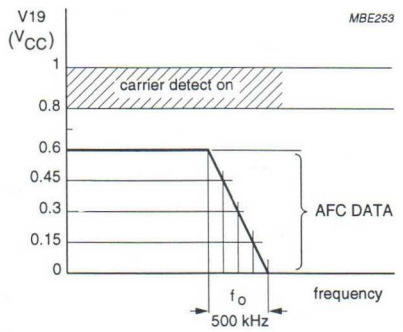


Fig.3 AFC and carrier detector output.

APPLICATION INFORMATION

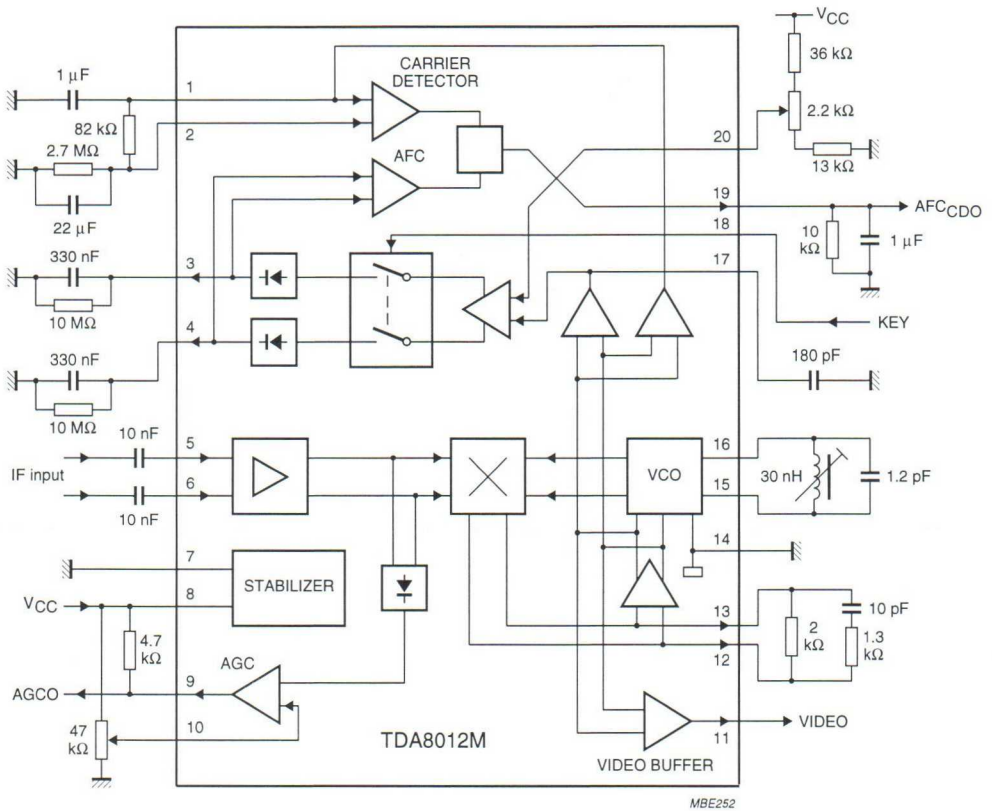


Fig.4 Application circuit.

Quadrature demodulator TDA8040T

FEATURES

- +5 V supply voltage
- Bandgap internal reference voltage
- Low crosstalk between I (in-phase) and Q (quadrature) channel outputs
- High operating input sensitivity
- High CNR (Carrier-to-Noise Ratio) of the VCO.

APPLICATIONS

- QPSK (Quadrature Phase Shift Keying) demodulation.

GENERAL DESCRIPTION

The TDA8040T is a monolitic bipolar IC dedicated for quadrature demodulation. It has been designed to operate in conjunction with the TDA8041H to provide a complete QPSK demodulator.

The design of this circuit has been optimized to provide the best quadrature accuracy necessary for digital receiver applications and particularly for digital television.

The TDA8040T includes two matched mixers, an RF amplifier, a symmetrical Voltage Controlled Oscillator (VCO), a frequency divider and two matched amplifiers. Two external filters are required for the baseband filtering.

The VCO requires an external LC tank circuit with two varicap diodes. This oscillator operates at twice the IF carrier frequency and can be used in a carrier recovery AFC loop.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
$I_{CC(tot)}$	total supply current	V_{CC} = 5 V	70	79	90	mA
$V_{i(RF)}$	operating input voltage level		64	67	70	dBμV
$f_{i(RF)}$	RF input signal frequency		10.7	–	150	MHz
$V_{oIQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.5	–	V
$E\phi_{(IQ)}$	phase error between the I and Q channels		–	–	3	deg
$E_{G(IQ)}$	gain error between the I and Q channels		–	–	1	dB
$E_{G(tilt)}$	gain tilt error in the I and Q channels		–	–	1	dB
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels		30	–	–	dB
IM3	intermodulation distortion in the I and Q channels		40	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8040T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

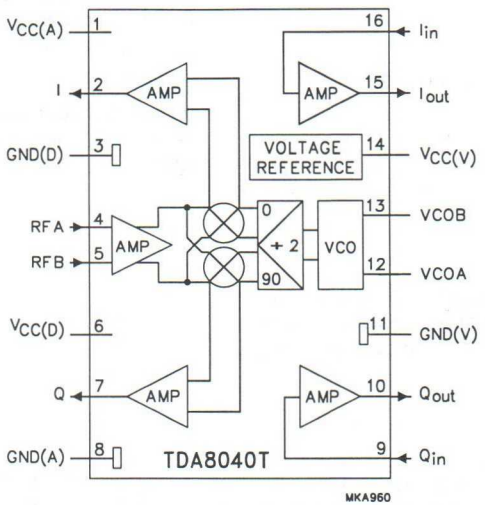


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The QPSK modulated RF signal is applied at the input of a high gain RF amplifier. The amplified signal is then mixed in a pair of mixers with two LO signals, which are 90 degrees out of phase, to produce the in-phase (I) and quadrature (Q) signals. These two signals are separately buffered to drive the external low-pass filters used for the baseband filtering. The I and Q signals are then amplified by two matched amplifiers designed to avoid crosstalk between channels.

The VCO operates at twice the carrier frequency. Its output signal is applied to a frequency divider (divide-by-2) to produce the two LO signals which are 90 degrees out of phase. The VCO is powered from the internal voltage stabilizer to ensure good shift performance.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{CC(A)}$	1	supply voltage for I and Q amplifiers
I	2	I channel buffer output
GND(D)	3	demodulator ground
RFA	4	RF input A
RFB	5	RF input B
$V_{CC(D)}$	6	supply voltage for demodulator
Q	7	Q channel buffer output
GND(A)	8	I and Q amplifiers ground
Q_{in}	9	Q channel amplifier input
Q_{out}	10	Q channel amplifier output
GND(V)	11	VCO ground
VCOB	12	VCO tank circuit B
VCOA	13	VCO tank circuit A
$V_{CC(V)}$	14	supply voltage for VCO
I_{out}	15	I channel amplifier output
I_{in}	16	I channel amplifier input

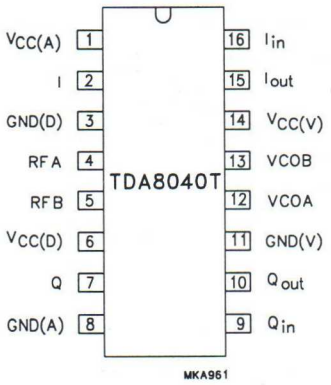


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	supply voltage for I and Q amplifiers		−0.3	6.0	V
$V_{CC(D)}$	supply voltage for demodulator		−0.3	6.0	V
$V_{CC(V)}$	supply voltage for VCO		−0.3	6.0	V
$V_{n(max)}$	maximum voltage on all pins		−0.3	V_{CC}	V
I_{max}	maximum sink or source current		–	10	mA
$t_{sc(max)}$	maximum short-circuit time on outputs		–	10	s
$Z_{L(IQ)}$	AC load impedance for I and Q channels	f_i = 15 MHz	35	–	Ω
$Z_{LA(IQ)}$	AC load impedance for I and Q output amplifiers	f_i = 15 MHz	300	–	Ω
$V_{VCO(p-p)}$	voltage drive level for external oscillator signal (peak-to-peak value)		–	0.6	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{CC(A)} = V_{CC(D)} = V_{CC(V)} = 5$ V; $f_{i(RF)} = 70$ MHz; $f_{i(VCO)} = 140$ MHz; $V_{i(RF)} = 67$ dBμV; $T_{amb} = 25$ °C; measured in application circuit of Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{CC(A)}$	supply voltage for I and Q channel amplifier		4.75	5.0	5.25	V
$V_{CC(D)}$	supply voltage for demodulator		4.75	5.0	5.25	V
$V_{CC(V)}$	supply voltage for VCO		4.75	5.0	5.25	V
$I_{CC(A)}$	supply current for I and Q channel amplifier	note 1	–	29	–	mA
$I_{CC(D)}$	supply current for demodulator	note 1	–	16	–	mA
$I_{CC(V)}$	supply current for VCO	note 1	–	34	–	mA
QPSK demodulator						
$f_{i(RF)min}$	minimum input IF frequency		–	–	10.7	MHz
$f_{i(RF)max}$	maximum input IF frequency		150	–	–	MHz
$R_{i(RF)}$	resistive input impedance		–	50	–	Ω
$X_{i(RF)}$	reactive input impedance		–	5	–	Ω
$V_{i(RF)}$	operating input voltage		64	67	70	dBμV
$R_{o(IQ)}$	output resistance for I and Q channels		45	50	55	Ω
$V_{oIQ(p-p)}$	output voltage for I and Q channels (peak-to-peak value)	note 2	–	85	–	mV
$G_{ch(IQ)}$	I and Q channel gain	note 3	21	22.5	24	dB
$E_{\phi(IQ)}$	phase error between I and Q channels	note 4	–	–	3	deg
$E_{G(IQ)}$	gain error between I and Q channels	note 4	–	–	0.5	dB
$E_{G(tilt)}$	gain tilt error between I and Q channels	note 5	–	–	0.8	dB
NF	double sideband noise figure	$Z_{source} = 50$ Ω; note 6	–	17	20	dB
IM3	intermodulation distortion in the I and Q channels	note 7	45	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator (VCO)						
$f_{iVCO(min)}$	minimum input oscillator frequency		–	–	21.4	MHz
$f_{iVCO(max)}$	maximum input oscillator frequency		300	–	–	MHz
Δf	frequency deviation		–	6	–	MHz
Δf_{drift}	frequency drift	note 8	–	–	100	kHz
Δf_{shift}	frequency shift	ΔV_{CC} = 5%	–	–	100	kHz
CNR_{osc}	oscillator carrier-to-noise ratio	at 10 kHz; note 9	–	85	–	dBc/Hz
		at 100 kHz; note 9	–	105	–	dBc/Hz
$V_{osc(p-p)}$	required voltage drive level for external oscillator injection (peak-to-peak value)		100	–	–	mV
$R_{source(osc)}$	source resistance for external oscillator generator		–	–	50	Ω
I and Q amplifiers						
$V_{ilQ(p-p)}$	I and Q channel input voltage (peak-to-peak value)	note 10	–	0.1	–	V
$V_{olQ(p-p)}$	I and Q channel output voltage (peak-to-peak value)	note 10	–	0.5	–	V
		at 1 dB gain compression; note 10	1.0	–	–	V
IM3	intermodulation distortion in the I and Q channels	note 11	40	–	–	dB
B_{IQ}	bandwidth of I and Q amplifiers	at 0.5 dB	25	–	–	MHz
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels	note 12	30	–	–	dB
$V_{O(IQ)}$	DC output voltage level for the I and Q amplifier		–	2.45	–	V
$Z_{I(IQ)}$	input impedance of the I and Q channels		–	10	–	kΩ
$Z_{O(IQ)}$	output impedance of the I and Q channels		–	50	–	Ω

Notes to the characteristics

1. Typical supply currents are defined for V_{CC} = 5 V.
2. The I and Q channel output voltages are measured with the following conditions:
   a) $f_{i(RF)} = f_{i(VCO)}/2$ + 500 kHz (70.5 MHz)
   b) the higher frequencies (140.5 MHz) are filtered out.
3. The I and Q channels gain is defined by $G_{IQ} = V_{IQ(rms)}/V_{iRF(RMS)}$. The gains are measured with the conditions defined in note 2.
4. The phase and gain error between the I and Q channel outputs is measured as follows:
   a) the oscillator is tuned at $f_{i(VCO)}$ = 140 MHz
   b) a sine wave signal $f_{i(RF)} = f_{i(VCO)}/2$ + 500 kHz (70.5 MHz) is applied at the IF input
   c) the higher frequencies (140.5 MHz) are filtered out.

   Under these conditions, in each I and Q channel, a sine wave with a frequency of 500 kHz will be present. These sine waves should be 90 degrees out of phase.
   The phase error is defined as the phase quadrature imbalance between the I and Q channels.
   The gain error is defined as the gain difference between the I and Q channels.
5. The tilt is defined as the difference between the maximum and the minimum channel gain measured in a frequency band of 25 MHz around $f_{i(RF)}$. The specified tilt is the maximum tilt value found in one of the I or Q channels.
6. The specified noise figure is the maximum value obtained from I and Q channel noise measurement. The noise meter is tuned to 10.7 MHz.
7. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in the I and Q channels. Intermodulation is measured with two sine wave signals at $f_{i(RF)}$ = 79 MHz and $f_{i(RF)}$ = 81 MHz with an amplitude of 67 dBμV for each tone. The difference in level between the converted carriers (9 MHz and 11 MHz) and the intermodulation products after frequency conversion (7 MHz and 13 MHz) is defined as IM3 (see Fig.3).
8. The temperature for the VCO frequency drift is defined for ΔT_{amb} = 25 °C. It is measured in the application circuit of Fig.10 with the following component values for the tank circuit:
   a) L1: 22 nH (TOKO NE545BNA5 - 100082)
   b) C1: 15 pF NP0
   c) C2: 33 pF N220 (220 ppm/°C)
   d) C3 and C4: 1 nF
   e) C5: 3.3 μF
   f) D1 and D2: BB133
   g) R1 and R2: 100 kΩ
   h) R3: 1 kΩ.
9. The phase noise is measured at the oscillator frequency (140 MHz). Due to the frequency divider, the phase noise at the input of the mixers is 6 dB better (111 dBc/Hz at 100 kHz).
10. Output amplifiers are measured separately with an external DC bias applied at pins 9 and 16. The gain is measured for an output signal of 500 mV(p-p) at f_i = 500 kHz.
11. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in the I and Q output amplifier. Intermodulation is measured with two sine wave signals at f_i = 9 MHz and f_i = 11 MHz at an output level of 500 mV(p-p) for each tone.
12. The crosstalk between the I and Q amplifiers is defined as the ratio between the wanted output signal and the disturbing signal from the other channel. To measure the crosstalk of the I and Q amplifiers, a sine wave 15 MHz, 0.1 V(p-p) is applied at the I input and a sine wave 15.5 MHz, 0.1 V(p-p) is applied at the Q input. For each output, the difference in level is measured between the 15 MHz and the 15.5 MHz component. This difference is the value of the crosstalk between the I and Q amplifiers.

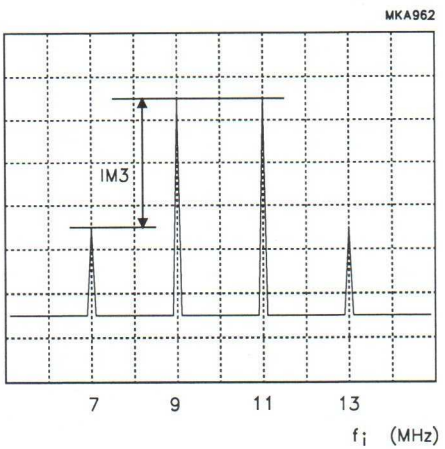


Fig.3 IM3 definition.

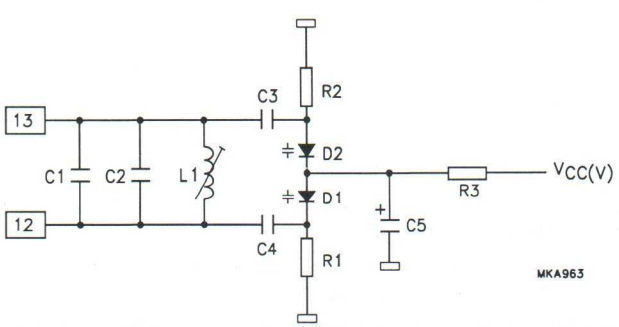


Fig.4 Tank circuit.

INPUT PIN CONFIGURATION

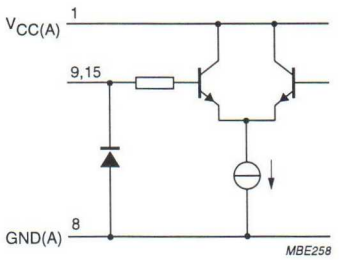


Fig.5 Input circuitry $V_{CC(A)}$ to GND(A).

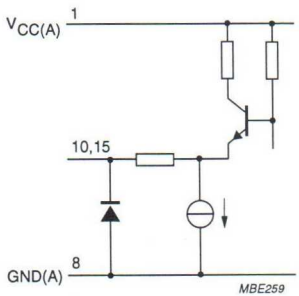


Fig.6 Input circuitry $V_{CC(A)}$ to GND(A).

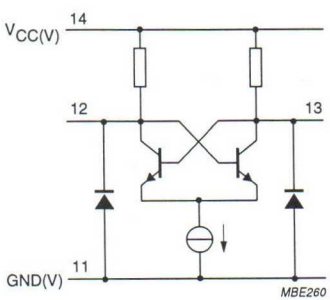


Fig.7 Input circuitry $V_{CC(V)}$ to GND(V).

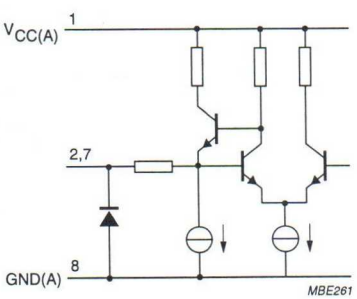


Fig.8 Input circuitry $V_{CC(A)}$ to GND(A).

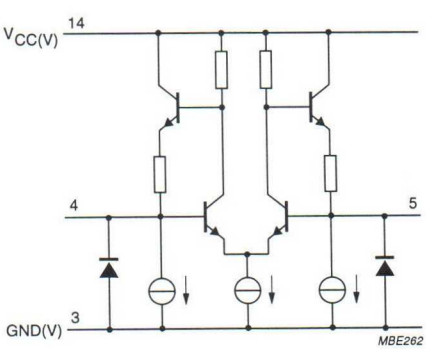


Fig.9 Input circuitry $V_{CC(V)}$ to GND(V).

APPLICATION INFORMATION

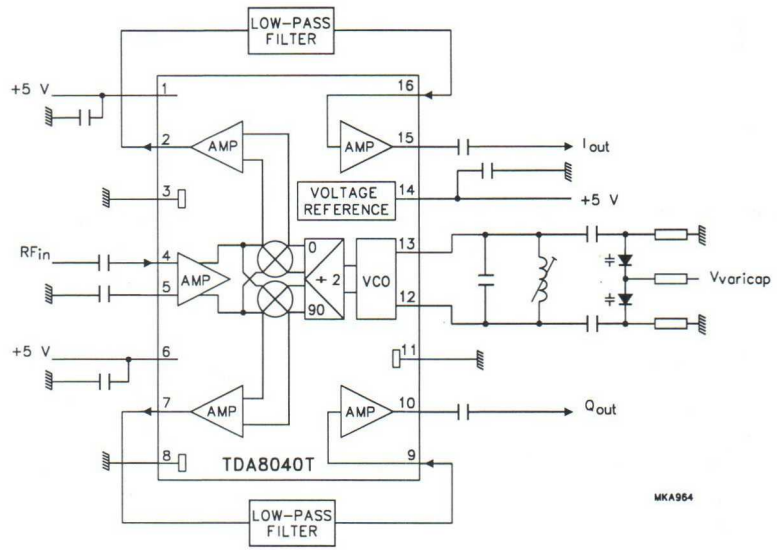


Fig.10 Application circuit.

Quadrature demodulator controller TDA8041H

FEATURES

- Generates all control signals for Quadrature Phase-Shift Keying (QPSK) and Binary Phase-Shift Keying (BPSK) demodulation
- Can be used in applications with low E_b/N_o and high symbol rate (up to 30×10^6 symbols/s)
- Digital I and Q outputs (3 bits) for soft decision within error correction
- Two matched analog-to-digital converters to quantize the I and Q signals
- A digital detector for each control loop to generate the required control signals
- Digital-to-analog converters and operational amplifiers to allow high flexibility for loop time constants
- Special input stage to interface with the voltage controlled crystal oscillator
- Positive 5 V supply voltage.

APPLICATIONS

- Demodulation of BPSK and QPSK modulated signals in satellite and telephone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		4.75	5.0	5.25	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		4.75	5.0	5.25	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		4.75	5.0	5.25	V
V_{DDD}	supply voltage for digital section (pin 35)		4.75	5.0	5.25	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	V_{DD} = 5 V	–	30	–	mA
V_{IQ}	I and Q input voltage		–	1.0	–	V
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$I_{O(DAC)}$	DAC output current		–100	–	+100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8041H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height	SOT307-2

Note

1. When using reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

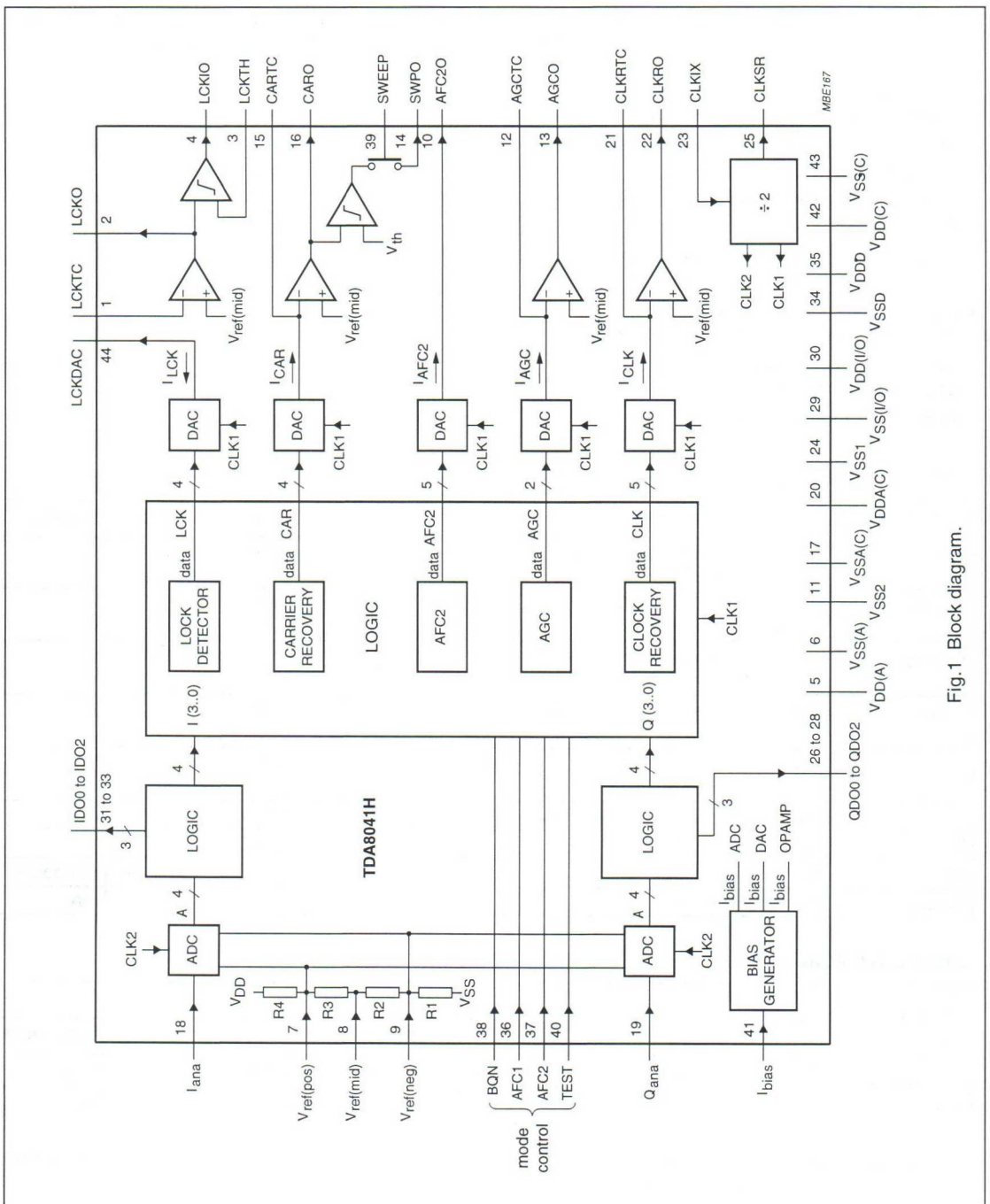


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LCKTC	1	carrier lock time constant
LCKO	2	carrier lock output
LCKTH	3	carrier lock threshold voltage
LCKIO	4	carrier lock indicator output
$V_{DD(A)}$	5	supply voltage for operational amplifiers
$V_{SS(A)}$	6	negative supply voltage for operational amplifiers
$V_{ref(pos)}$	7	positive reference voltage for converters
$V_{ref(mid)}$	8	middle reference voltage for converters
$V_{ref(neg)}$	9	negative reference voltage for converters
AFC2O	10	AFC 2 output
V_{SS2}	11	negative supply voltage 2
AGCTC	12	automatic gain control time constant
AGCO	13	automatic gain control output
SWPO	14	sweep current output
CARTC	15	carrier recovery time constant
CARO	16	carrier recovery output
$V_{SSA(C)}$	17	analog negative supply voltage for converters
I_{ana}	18	analog input I
Q_{ana}	19	analog input Q
$V_{DDA(C)}$	20	analog supply voltage for converters
CLKRTC	21	clock recovery time constant
CLKRO	22	clock recovery output
CLKIX	23	clock input from crystal circuit (at double symbol rate)

SYMBOL	PIN	DESCRIPTION
V_{SS1}	24	negative supply voltage 1
CLKSR	25	clock output at symbol rate
QDO2	26	Q digital output (bit 2)
QDO1	27	Q digital output (bit 1)
QDO0	28	Q digital output (bit 0)
$V_{SS(I/O)}$	29	negative supply voltage for digital inputs/outputs
$V_{DD(I/O)}$	30	supply voltage for digital inputs/outputs
IDO2	31	I digital output (bit 2)
IDO1	32	I digital output (bit 1)
IDO0	33	I digital output (bit 0)
V_{SSD}	34	negative supply voltage for digital section
V_{DDD}	35	supply voltage for digital section
AFC1	36	AFC control switch 1 (1 = on; 0 = off)
AFC2	37	AFC control switch 2 (1 = on; 0 = off)
BQN	38	BPSK/QPSK control switch (1 = BPSK; 0 = QPSK)
SWEEP	39	sweep control switch (1 = on; 0 = off)
TEST	40	test control switch (1 = on; 0 = off)
I_{bias}	41	input bias current for analog blocks
$V_{DD(C)}$	42	supply voltage for digital part of ADC and DAC
$V_{SS(C)}$	43	negative supply voltage for digital part of ADC and DAC
LCKDAC	44	carrier lock DAC output

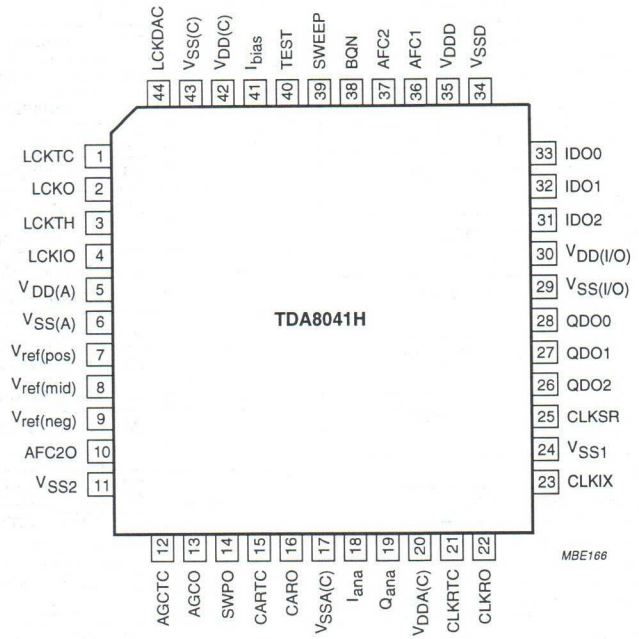


Fig.2 Pin configuration.

GENERAL DESCRIPTION

The quadrature demodulator controller TDA8041H, generates all control signals required for demodulation of BPSK and QPSK modulated signals. This device is specially designed to be used in conjunction with the quadrature demodulator IC, TDA8040T.

The quadrature demodulator controller generates the following signals:

- Symbol clock recovery control signal; this signal locks the VCXO to the received symbol clock. The clock recovery algorithm used in this device operates independently from the other loops.
- Carrier recovery control signal; depending on the selected mode (BPSK or QPSK), this signal will adjust the phase of the I and Q input signal. This adjustment will be such that the constellation points are as defined in Fig.4.
- Frequency control signals (AFC1 and AFC2); to serve a broad range of applications, two different AFC detectors and a sweep function are built-in:
  - AFC1: this is a robust detector which forces the offset frequency in the I and Q branch to zero. This detector can handle frequency offset up to 1/8 × symbol rate.
  - AFC2: this detector can handle frequency offsets greater than 1/8 × symbol frequency. However this AFC algorithm will bring the offset frequency only close to zero.
  - Sweep: this signal generates a triangular current output which can tune a VCO over its complete frequency range. Sweeping must be switched off as soon as the logical output of the lock detect function becomes positive. The value of the sweep current is set by an external resistor.
- Amplitude control signals (AGC); this signal adjusts a variable gain amplifier so that the amplitude of the I and Q signals is in accordance with the specified constellation points of Fig.4.
- Lock detect signal; this signal is related to the E_b/N_o of the incoming I and Q signals. This lock detect signal can be used for two purposes:
  - Lock detection by comparing the lock detect signal with an external set reference voltage, one can obtain a logical signal indicating lock detect.
  - The relationship between E_b/N_o can be used to display the E_b/N_o for antenna adjustment.

FUNCTIONAL DESCRIPTION

The TDA8041H has a 3-bit-wide digital I and Q output for soft error correction. These 3-bit outputs represent the main symbols only. The relationship between the 4-bits ADC signals and the 3-bit output signals is illustrated in Fig.3.

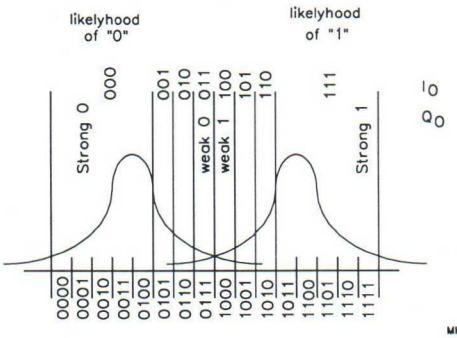


Fig.3 I and Q output levels for soft error decision FEC.

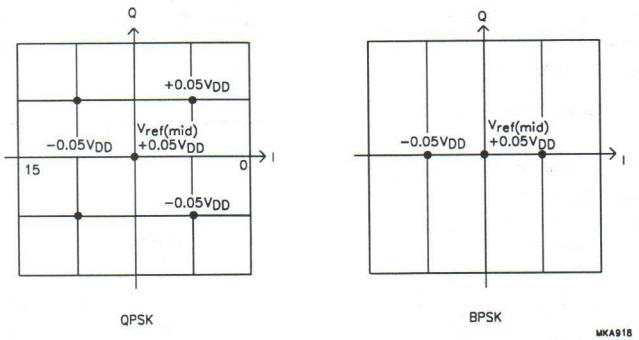


Fig.4 Constellation points.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		−0.5	+6.5	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		−0.5	+6.5	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		−0.5	+6.5	V
V_{DDD}	supply voltage for digital section (pin 35)		−0.5	+6.5	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		−0.5	+6.5	V
$V_{n(max)}$	maximum voltage on all pins		0	V_{DD}	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{DD} = 4.75 to 5.25 V; R_{sym} = 30 × 10^6 symbols/s; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs (pins 26 to 28 and 31 to 33)						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage	see Fig.6	$0.9V_{DD}$	–	V_{DD}	V
t_d	delay time	see Fig.6	t_h	–	22	ns
t_h	hold time		8	–	t_d	ns
Digital inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
Clock output (pins 22 and 25); see Fig.5						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
T_{cy}	cycle time		33	–	–	ns
t_W	pulse width	duty cycle 40/60	13.2	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	6	ns
t_f	fall time	C_L = 30 pF	–	–	6	ns
Clock input (pin 23)						
R_{source}	source resistance		–	–	50	Ω
f_s	sampling frequency		–	–	60	MHz
Analog inputs (pins 18 and 19)						
R_{sym}	symbol rate		–	–	30 × 10^6	symbols/s
$V_{ref(pos)}$	positive reference voltage	I_O = 0	–	$0.48V_{DD}$	–	V
$V_{ref(mid)}$	middle reference voltage	I_O = 0	–	$0.38V_{DD}$	–	V
$V_{ref(neg)}$	negative reference voltage	I_O = 0	–	$0.28V_{DD}$	–	V
I_L	load current at pin 8	note 1	–5	–	+5	mA
$V_{i(I,Q)}$	I and Q input voltage		0	–	V_{DD}	V
$V_{I,Q(op)}$	I and Q operating voltage		$0.28V_{DD}$	–	$0.48V_{DD}$	V
R_I	input resistance		50	–	–	kΩ
C_I	input capacitance		–	–	20	pF
I_{bias}	input bias current	R_L = 100 kΩ	–	–37	–	mA
DAC outputs (pins 10, 12, 15 and 21)						
$I_{o(av)}$	average output current	$V_{DAC} = V_{ref(mid)}$; note 2	–	100	–	mA
D_{Io}	matching of positive and negative output currents	$V_{DAC} = V_{ref(mid)}$; note 2	–7	–	+7	%
I_o	zero output current		–25	–	+25	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sweep current (pin 14)						
V_{OH}	HIGH level output voltage		–	$2V_{ref(mid)}$	–	V
V_{OL}	LOW level output voltage		–	0	–	V
Z_O	output impedance	SWEEP = 1	–	2	–	kΩ
		SWEEP = 0	10	–	–	MΩ
$V_{CARO(min)}$	LOW switching level		$0.1V_{DD}$	–	$0.2V_{DD}$	V
$V_{CARO(max)}$	HIGH switching level		$0.8V_{DD}$	–	$0.9V_{DD}$	V
Loop amplifiers						
V_o	output voltage		$0.1V_{DD}$	–	$0.9V_{DD}$	V
G_v	open loop gain		–.	60	–	dB
G_B	gain bandwidth		–	1	–	MHz
R_L	load resistance		5	–	–	kΩ

Notes

1. $V_{ref(mid)}$ is usually open-circuit. However, this pin may also be used as a reference output for an external buffer.

2. $I_{o(av)} = \frac{(I_{pos} - I_{neg})}{2}$; $D_{Io} = 100 \times \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})}$

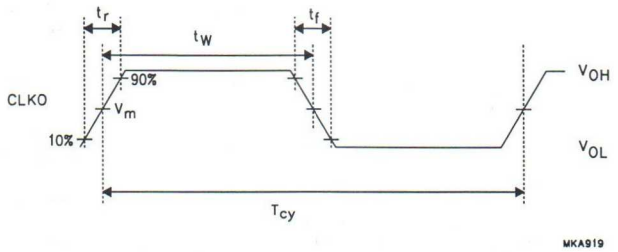


Fig.5 Timing of CLKO.

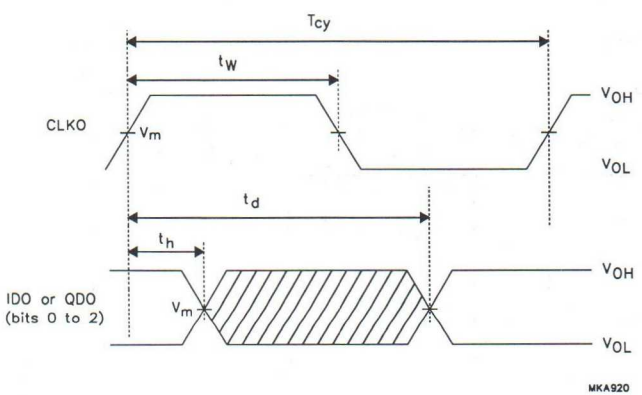


Fig.6 Timing definition of digital outputs.

APPLICATION INFORMATION

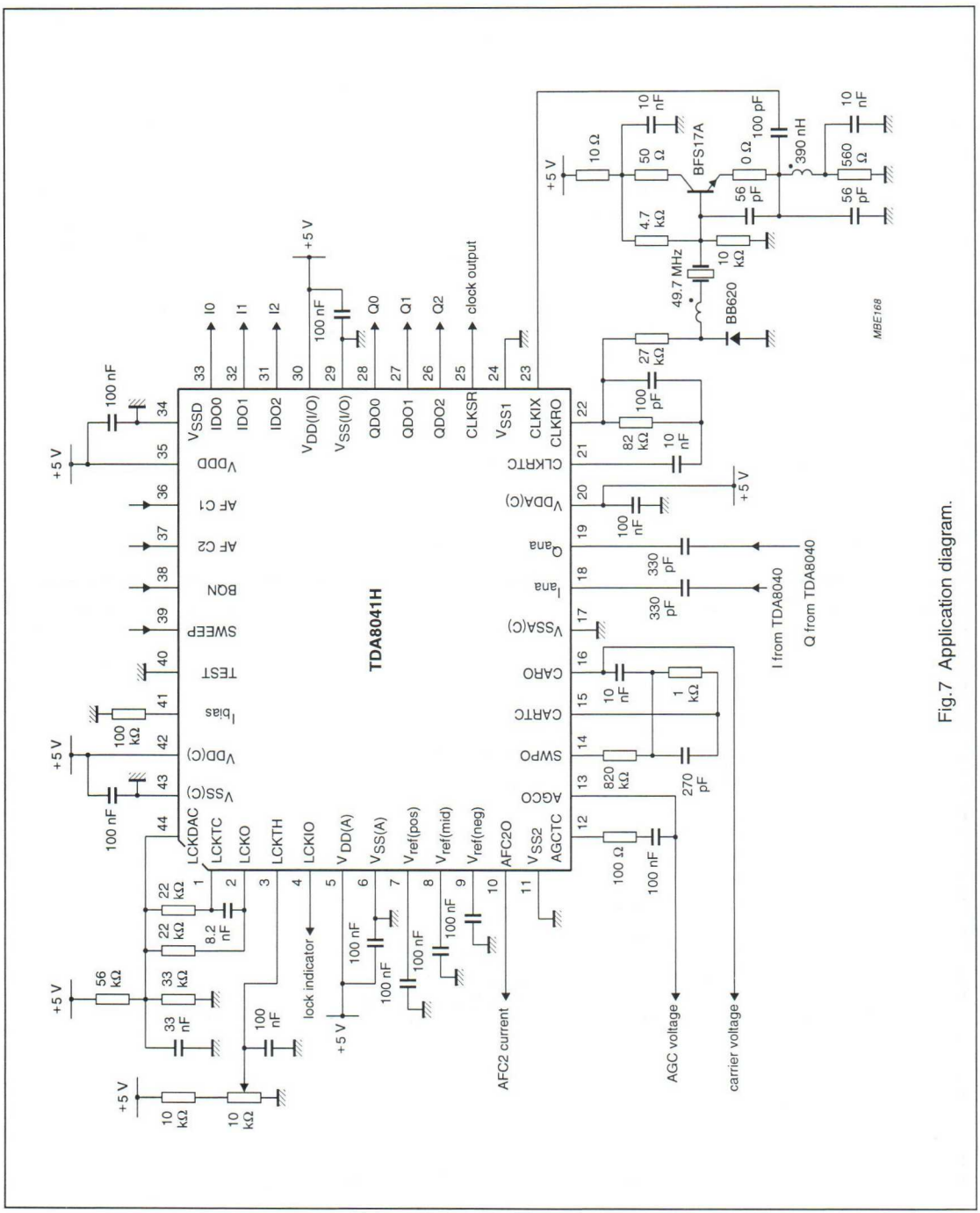


Fig.7 Application diagram.

Small signal combination IC for colour TV

TDA8302

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative demodulation
- AGC detector operating on peak sync
- Tuner AGC
- AFC circuit with sample-and-hold and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator for 60 Hz only
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch.

GENERAL DESCRIPTION

The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8302	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync, where a non-modulated carrier is present. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
V_{14}	video transmitter identification output no signal condition signal condition		 - -	 0.3 12	 - -	 V V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

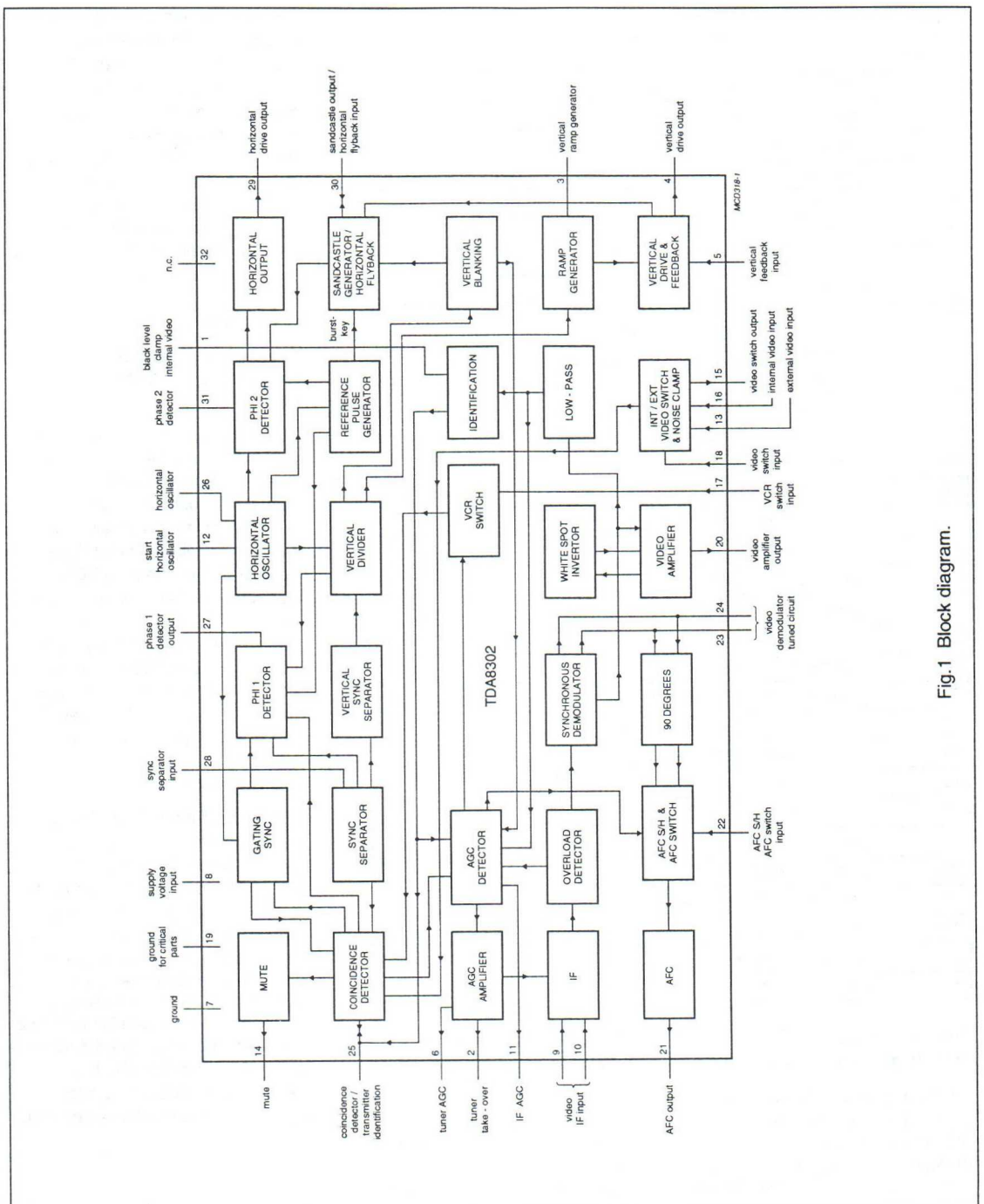


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator
13	external video input
14	mute
15	video switch output
16	internal video input
17	VCR switch input
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	not connected

The transmitter identification/coincidence detector

A mute signal (see Table 1) is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. This prevents the emission of excessive noise from the loudspeaker, particularly when selecting an alternative program channel.

When the video switch is in the internal mode, the coincidence detector will be used as transmitter identification. Pin 25 is HIGH when the horizontal loop is synchronized with the video signal and LOW in the case of no-synchronization. In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

VCR switch

The TDA8302 has a separate pin (pin 17) for the VCR switch, see tables 2 and 4.

Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the auto VCR mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a slow time constant.

Video-switch

Video output from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8302 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18, see Table 3. The AGC detector is not gated during the external video mode, the first detector is also not gated and operates with a short time constant.

Table 1 MUTE truth Table

INPUT/OUTPUT	STATUS	STATUS	STATUS	STATUS	STATUS
Input signal Pins 9 and 10	60 Hz	none	60 Hz	60 Hz	none
output pin 25	9.5 V	0.3 V	9.5 V	9.5 V	0.3 V
input pin 28	60 Hz	none	60 Hz	none	60 Hz
input pin 18	LOW	LOW/ HIGH	HIGH	HIGH	HIGH
output pin 14	12 V	0.3 V	12 V	12 V	0.3 V

Table 2 VCR switch operation

INPUT	VCR MODE	AUTO VCR MODE	TV MODE
pin 17 (pin 18 = LOW)	HIGH	n.c.	LOW

Table 3 Video switch operation

INPUT	INTERNAL VIDEO	EXTERNAL VIDEO
pin 18	LOW	HIGH

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

Gain-reduction in the external video mode

The TDA8302 has an option to reduce the gain of the IF amplifier to prevent crosstalk from the IF to the horizontal oscillator when the circuit is in the external mode and there is no signal at the RF. The gain of the IF amplifier is reduced with 20 dB when the video-switch (see Table 3) is in the external video mode and pin 17 is connected with a resistor of 39 kΩ to ground. Without this resistor the IF remains at full gain. In the external video mode the 39 kΩ resistor has to be disconnected to achieve the auto VCR mode.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8302 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance.
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8302 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The advantage of the divider is that the vertical frequency is alignment free, and the provision of a maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window: divider ratio between 488 and 576.

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz).

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 approved vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 12.
- The divider is switched to count 525 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.

CHARACTERISTICS

T_{amb} = 25 °C; V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9\text{-}10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	μV
$R_{9\text{-}10}$	differential input resistance	note 3	-	1300	-	Ω
$C_{9\text{-}10}$	differential input capacitance	note 3	-	5	-	pF
$G_{9\text{-}10}$	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
$V_{9\text{-}10}$	maximum input signal		100	170	-	mV
Video Amplifier (notes 5 and 6)						
V_{20}	zero signal output level		4.7	4.9	5.1	V
V_{20}	peak sync level		2.5	2.7	2.9	V
V_{20}	white spot threshold level		-	5.5	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 7	-	2	5	%
φ	differential phase	note 7	-	2	5	°
NL	video non linearity	note 8	-	2	5	%
	intermodulation	note 9				
	1.1 MHz; blue		50	60	-	dB
	1.1 MHz; yellow		50	60	-	dB
	3.3 MHz; blue		55	65	-	dB
	3.3 MHz; yellow		55	65	-	dB
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 10; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_1	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
Video Switching Circuit (note 12)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V
INTERNAL VIDEO INPUT						
$V_{16(p\text{-}p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
POSITIVE VIDEO OUTPUT						
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 12 and 13	-	55	-	dB
α	crosstalk internal to external	notes 12 and 13	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
AFC-circuit (note 14)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current (pin 22)		-	-	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 11 and 15	-	11	-	V
	control slope	notes 11 and 15	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 11 and 15	-	−2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 16	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	μA
		V_{28} = 0 V	-	−10	-	mA
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 17	see Fig.7			
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 18	-	100	-	
t_d	control range		-	25	-	μs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	μA/μs
α	maximum allowed phase shift		-	±2	-	μs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15750	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 9.5 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 11	-	−1.6	-	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 11	-	-	500	Hz
Horizontal output (pin 29; open collector)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 19)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
t_W	burstkey pulse width		2.9	3.3	3.7	µs
VERTICAL BLANKING						
	divider in search window		-	17	-	lines
	divider in narrow window		-	21	-	lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse trailing edge rising edge		 - 4.7	 - 5.4	 9.4 6.1	 µs µs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		-	-	5	kΩ
I_{17}	output current	pin 17 = 0 V	-	-	0.5	mA
VCR switch (auto-VCR mode)						
I_{source}	source current (pin 17)		-	-	30	µA
I_{sink}	sink current (pin 17)		-	-	30	µA
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)	pin 17 = n.c.	-	2.2	-	mV
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		-	-	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	-	-	1	mA
Vertical ramp generator (note 20)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p\text{-}p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 11	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	temperature dependency of the amplitude	note 11 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level guard level LOW guard level HIGH	note 21	 - -	 1.5 2	 - -	 V V
Coincidence detector/transmitter identification (note 22)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2	-	V
Video transmitter identification output (open collector)						
V_{14}	output voltage active	no sync; I = 1 mA	-	0.3	0.5	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	µA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. Measured according to the test line given in Fig.3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
8. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
9. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV RMS.
10. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at} \ B = 5 \ \textit{MHz}}$$

11. These figures are based on test samples.
12. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
13. Defined as $20 \log \frac{V_O \textit{ unwanted video black-to-white}}{V_O \textit{ wanted video-black-to-white}}$; measured at 4.4 MHz.
14. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
15. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
16. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
17. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
18. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
19. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
20. The vertical scan is synchronized by means of a divider system. Therefore no frequency adjustment is required for the V-ramp generator.
21. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
22. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.

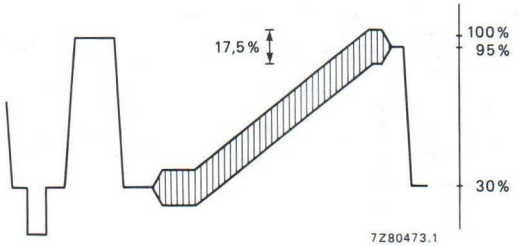


Fig.2 Video output signal.

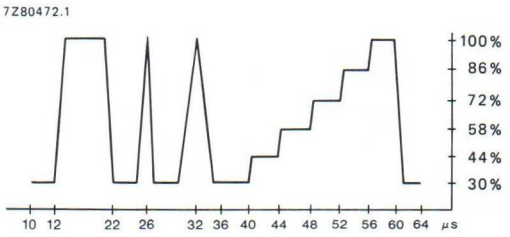
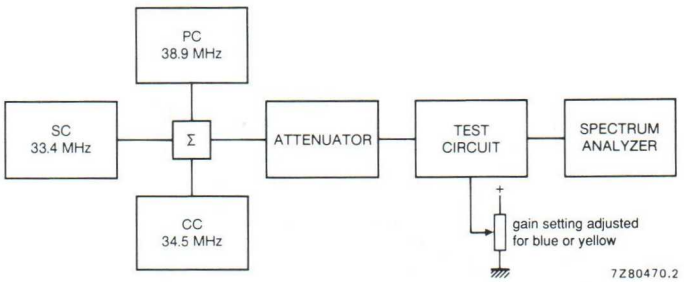
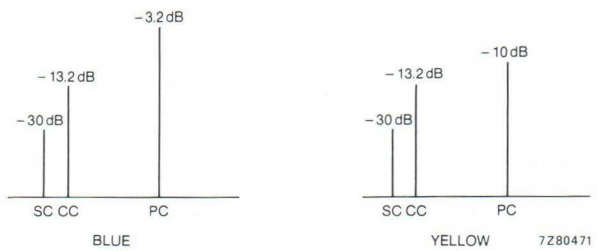


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$\textit{Value at } 1.1\textit{MHz}: 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 1.1\textit{MHz}} + 3.6\textit{dB}$$

$$\textit{Value at } 3.3\textit{MHz}: 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 3.3\textit{MHz}}$$

Fig.4 Test set-up intermodulation.

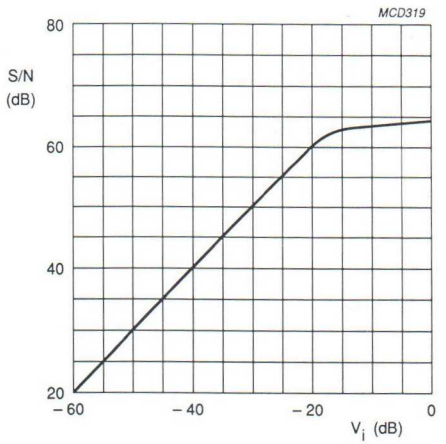
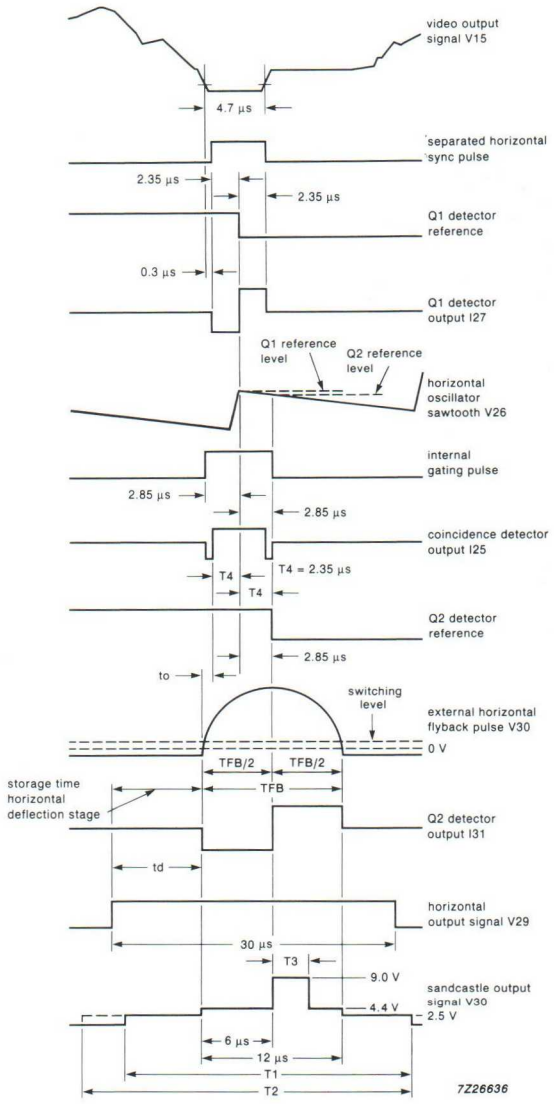


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 34p; $p = 1/2f_H$

T2: divider in narrow window: 42p

T3: 3.3 µs

Fig.6 Timing diagram.

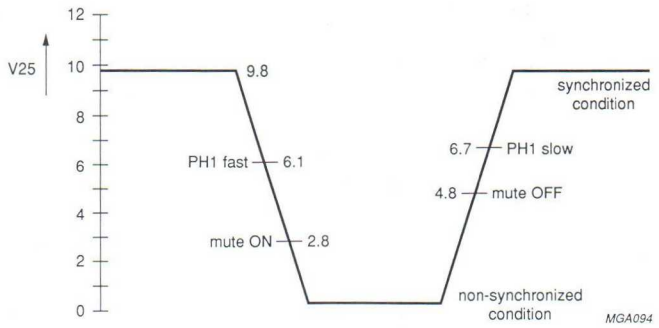


Fig.7 Switching levels coincidence detector.

Table 4

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
			T2 - T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} > 6.7 V and strong signal	11.3	7.6
		V_{25} > 6.7 V and weak signal	1.3	1.3
		V_{25} < 6.1 V and strong signal	11.3	7.6
		V_{25} < 6.1 V and weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V	1.3	1.3
		V_{25} < 6.1 V	11.3	7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

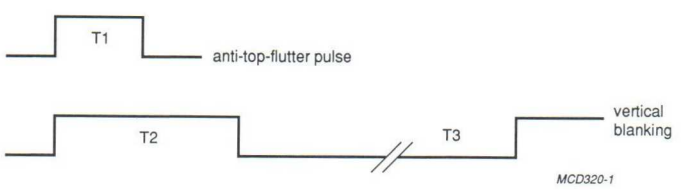


Fig.8 Anti-top-flutter pulse.

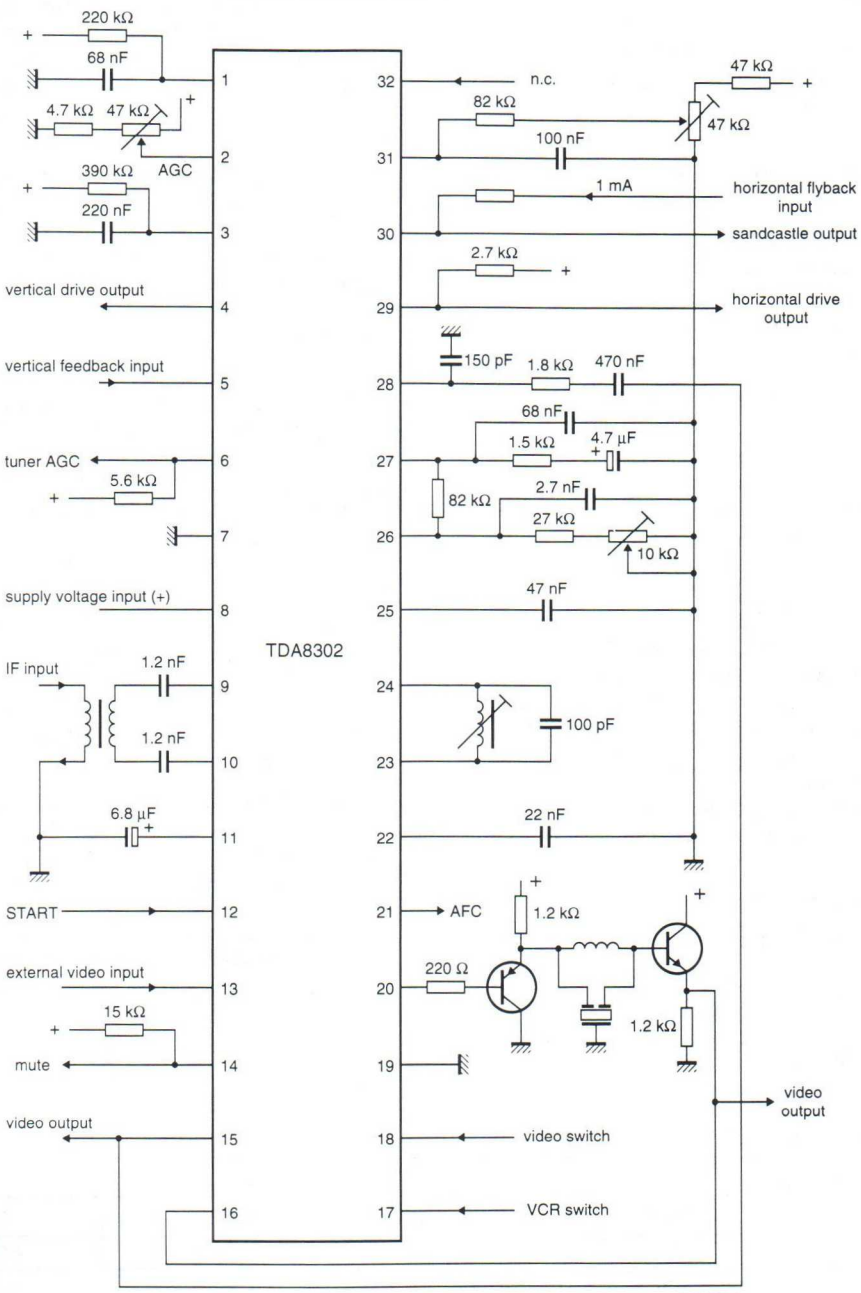


Fig.9 Application diagram.

Small signal combination IC for black/white TV

TDA8303
TDA8303A

FEATURES

- Video IF amplifier with synchronous demodulator
- Automatic gain control (AGC) detector suitable for negative modulation
- AGC tuner
- Automatic frequency control (AFC) circuit with sample-and-hold
- Video preamplifier
- Sound IF amplifier and demodulator
- DC volume control or separate supply for starting the horizontal oscillator
- Audio preamplifier
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)

GENERAL DESCRIPTION

The TDA8303/TDA8303A combines all small signal functions (except the tuner) which are required for a monochrome television receiver. For a complete black and white receiver only the output stages for video, sound, horizontal and vertical deflection and a tuner have to be added.
The TDA8303 is for applications with npn tuners and the TDA8303A for pnp tuners.

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB. An additional advantage is the symmetry of the amplifier which results in a less critical application.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. The limiter has a very low differential phase shift which results in good differential gain and phase figures.

The video amplifier also contains a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level. This circuit is more effective than a noise inverter and results in an improved picture stability, with respect to interference.

AFC-circuit

The reference signal for the AFC circuit is obtained from the demodulator tuned circuit. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The disadvantage with this method is that the frequency spectrum of the signal fed to the detector is determined by the SAW filter characteristic. This spectrum is asymmetrical with respect to the picture carrier so that the AFC output voltage is dependent on the video signal.

To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit which samples during the sync level of the signal. This means that only the carrier signal is available to the AFC and it will not be affected by the video information.

At very weak input signals the drive signal of the AFC circuit will contain substantial noise. This noise has an asymmetrical frequency spectrum causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance, therefore the steepness of the of the AFC control voltage is dependent on the load impedance.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8303	28	DIL	plastic	SOT117
TDA8303A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage (pin 7)		9.5	12	13.2	V
I_P	supply current (pin 7)		90	125	160	mA
I_{start}	start current (pin 11)	note 1	–	6.5	9	mA
Video						
$V_{8\text{-}9(RMS)}$	IF sensitivity (RMS value)	at 38.9 MHz; note 2	20	40	65	μV
$G_{8\text{-}9}$	IF gain control range		–	74	–	dB
S/N	signal-to-noise ratio	input signal = 10 mV	–	57	–	dB
$V_{18(p\text{-}p)}$	AFC output voltage swing (peak-to-peak value)		10.5	–	11.5	V
Sound						
$V_{12(RMS)}$	AF output signal (RMS value)	note 3	400	600	800	mV
AMS	AM suppression	at V_I = 50 mV	–	58	–	dB
THD	total harmonic distortion		–	0.5	–	%
Sync						
V_{25}	required sync pulse amplitude	note 4	200	–	–	mV
I_{27}	required input current during flyback pulse		0.1	–	2	mA
V_{22}	coincidence detector output voltage					
	in synchronized condition		–	9.7	–	V
	in no signal condition		–	1.5	–	V
V_{22}	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{22(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		–	1.2	–	V

Notes to the quick reference data

1. Pin 11 has a double function. When during switch-on a current of 9 mA is supplied to this pin, it is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The output signal is measured at Δf = 7.5 kHz and maximum volume control.
4. The minimum value is obtained by connecting a 1.8 kΩ resistor and a 470 nF capacitor in series between the video output and pin 25. The slicing level can be varied by changing the value of this resistor (higher resistance value results in a larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

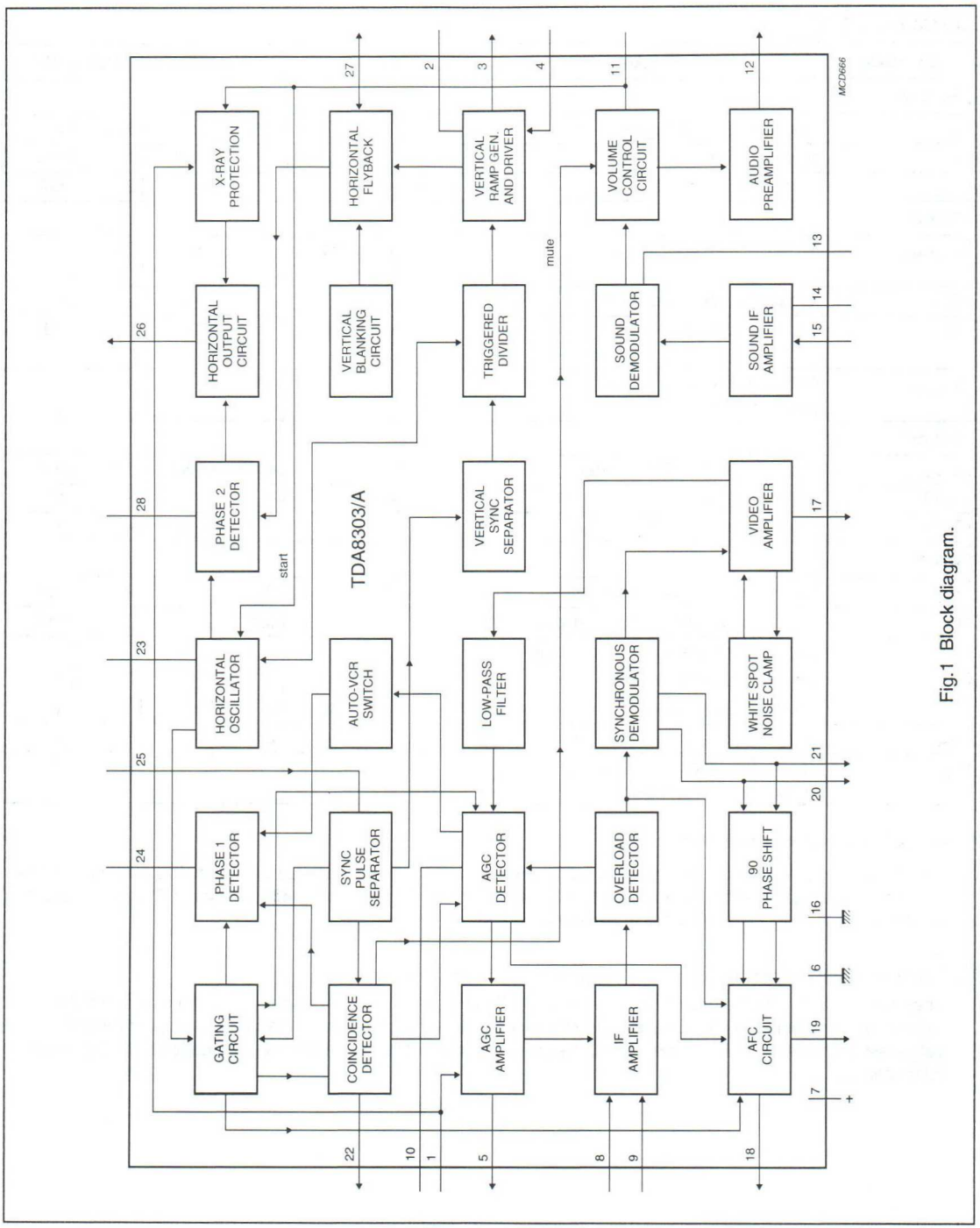


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	AGC take-over
2	vertical ramp generator
3	vertical drive
4	vertical feedback
5	tuner AGC
6	ground
7	supply voltage input
8	video IF input
9	video IF input
10	IF AGC
11	volume control/start horizontal oscillator
12	audio output
13	sound demodulator
14	sound IF decoupling
15	sound IF input
16	ground (for some critical parts)
17	video amplifier output
18	AFC output
19	AFC S/H, AFC switch
20	video demodulator tuned circuit
21	video demodulator tuned circuit
22	coincidence detector
23	horizontal oscillator
24	phase 1 detector
25	sync separator input
26	horizontal drive output
27	horizontal flyback input
28	phase 2 detector

AGC circuit

The AGC circuit of the TDA8303/TDA8303A is a top-sync detector. The video signal coming from the video amplifier passes a 2nd order low-pass filter before it is compared with an internal reference level. The comparator stage is gated when the horizontal oscillator is synchronized with the video signal, such that interference pulses outside the gating time have no influence on the gain control.

Sound circuit

The sound quality of the TDA8303/TDA8303A compared with the predecessors has been improved at weak signal conditions. The improvement has been achieved by the new IF amplifier which is less sensitive for radiation from the sound IF amplifier and by change of the ground and supply connections in the IC. When out-of-sync condition is detected by the coincidence detector the sound output is muted. When no mute is required the minimum voltage level on pin 22 should be clamped to a high level of 5 V. At this level the gating of the AGC is switched off and the phase 1 detector has a high output current for reliable catching of a new transmitter.

Vertical synchronization

The TDA8303/TDA8303A embodies a synchronized divider system for generating the vertical sawtooth at pin 2 having several advantages and features such as:

- The vertical frequency is alignment free. The divider automatically adapts to a vertical frequency of 50 Hz or 60 Hz including automatic amplitude correction and its operating modes offer maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse. Internally clock pulses are generated by doubling the line frequency. The divider operates in the 60 Hz mode when the trigger pulse appears before count 576, otherwise the 50 Hz mode will be active.
- The divider system operates with two different reset windows for maximum interference/disturbance protection. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is decreased by 1.

Modes of operation

Large search window: divider ratio between 488 and 576.

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 and 528 (60 Hz); or 622 and 628 (50 Hz).

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 approved vertical sync pulses
- When the divider operates in the narrow window mode and a vertical sync pulse is missing within the window, the divider is reset at the end of that window and the counter value is decreased by 1
- At a counter value below 10 the divider system switches over to the large window mode
- The divider system also generates an anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode

VCR switch

An extra time constant switch in the horizontal phase detector makes an external VCR switch redundant. The time constant is automatically switched depending on the signal strength of the IF input (pins 8/9) and the coincidence detector.
When a strong signal is detected ($V_{8/9}$ > 2.2 mV) and the circuit is synchronized the time constant of the phase detector is optimum for VCR playback, a fast time constant during the vertical retrace to correct head errors of the VCR and during scan a sufficient time constant to correct fluctuations of the horizontal sync
During weak signal and synchronized conditions the time constant is enlarged and the phase detector is gated. This ensures a stable display which is not disturbed by the noise in the video signal. When the circuit is not synchronized the time constant is fast and not gated to ensure a short catching time.

Combination of DC volume control and start-up feature

Pin 11 of the IC can be used as a DC volume control or as a start-up feature of the horizontal oscillator/output circuit dependent on the application.
Volume control is achieved by connecting a 4.7 kΩ potentiometer or a DC voltage of 0 to 3 V to pin 11.
When a current of 9 mA is supplied to pin 11 the volume control is set to a fixed output signal level and the circuit will generate drive pulses for the horizontal deflection and the main supply can be derived from the deflction.

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC-coupled to the sync separator input. It is possible to interrupt this connection and drive the sync separator from other sources.
When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- Mute circuit not active, sound channel remains switched on
- Phase detector 1 has an optimum time constant for external video sources and is not gated

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	–	13.2	V
P_{tot}	total power dissipation	–	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

CHARACTERISTICS

V_P = 12 V;T_{amb} = 25 °C; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 7)						
V_P	supply voltage range		9.5	12	13.2	V
I_P	supply current	no input	90	125	160	mA
I_{11}	start current (pin 11)	note 1	–	6.5	9	mA
V_{11}	start voltage horizontal oscillator		9.5	–	–	V
V_{11}	start protection level	I_{11} = 12 mA	–	–	16.5	V
IF Amplifier (pins 8 and 9)						
$V_{8\text{-}9(RMS)}$	input sensitivity (RMS value)	at 38.9 MHz; note 2	25	40	65	μV
$V_{8\text{-}9(RMS)}$	input sensitivity (RMS value)	at 45.75 MHz; notes 2 and 25	25	40	65	μV
$R_{8\text{-}9}$	differential input resistance	note 3	–	1300	–	Ω
$C_{8\text{-}9}$	differential input capacitance	note 3	–	5	–	pF
$G_{8\text{-}9}$	gain control range		–	74	–	dB
ΔV_{17}	output signal expansion for 46 dB input signal variation	note 4	–	1	–	dB
$V_{8\text{-}9}$	maximum input signal		100	170	–	mV
Video Amplifier (note 5)						
V_{17}	zero signal output level	note 6	–	5.4	–	V
V_{17}	peak sync level		2.3	2.5	2.7	V
V_{17}	video output signal amplitude	note 7	2.3	2.65	3.0	V
V_{17}	white spot threshold level		–	5.7	–	V
V_{17}	white spot insertion level		–	3.8	–	V
Z_{17}	video output impedance		–	25	–	Ω
I_{17}	internal bias current of npn emitter follower output transistor		1.4	1.8	–	mA
I_{source}	maximum source current (pin 17)		10	–	–	mA
B	bandwidth of demodulated output signal		5	7	–	MHz
G_{17}	differential gain	note 8	–	4	8	%
φ	differential phase	note 8	–	2	5	deg.
NL	video non linearity	note 9	–	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	–	dB
	1.1 MHz; yellow		50	60	–	dB
	3.3 MHz; blue		55	65	–	dB
	3.3 MHz; yellow		55	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	10 mV input signal	50	57	–	dB
S/N	signal-to-noise ratio	end of gain control range	50	62	–	dB
V_{17}	residual carrier signal		–	2	10	mV
V_{17}	residual 2nd harmonic of carrier signal		–	2	10	mV
Tuner AGC						
$V_{8\text{-}9(RMS)}$	minimum starting point for tuner take–over (RMS value)		–	–	0.2	mV
$V_{8\text{-}9(RMS)}$	maximum starting point for tuner take–over (RMS value)		100	150	–	mV
I_5	maximum tuner AGC output swing	V_5 = 3 V	4	–	–	mA
V_5	output saturation voltage	I_5 = 2 mA	–	–	300	mV
I_L	leakage current (pin 5)		–	–	1	µA
ΔV_I	input signal variation complete tuner control		0.2	2	4	dB
V_1	minimum voltage tuner take–over		–	–	1	V
AFC circuit						
I_{19}	AFC sample-and-hold switch-off current		0.1	–	–	mA
I_O	output current (pin 19)	V_{19} = 0 V	–	0.1	0.3	mA
I_{LO}	output leakage current (pin 19)		–	–	2	µA
V_{18}	AFC output voltage swing	notes 18 and 19	10.5	–	11.5	V
I_{18}	available output current		0.2	–	–	mA
	control slope		–	100	–	mV/kHz
V_O	output voltage (pin 18)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		–	40	–	kΩ
V_{18}	output voltage swing	notes 25 and 26	–	11	–	V
	control slope	notes 25 and 26	–	80	–	mV/kHz
V_{18}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 25 and 26	–	–2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound circuit (note 12)						
V_{15}	input limiting voltage	$V_{O(max)}$ = –3 dB	–	400	800	μV
R_{15}	input resistance		–	2.6	–	kΩ
C_{15}	input capacitance		–	6	–	pF
AMS	AM suppression	note 13	53	58	–	dB
$V_{12(RMS)}$	AF output signal (RMS value)	note 14	400	600	800	mV
$V_{12(RMS)}$	AF output signal when pin 11 is used as a starting pin or connected to V_P (RMS value)	Δf = 50 kHz	500	900	1500	mV
Z_{12}	AF output impedance		–	25	100	Ω
THD	total harmonic distortion	note 15	–	0.5	2	%
RR	ripple rejection	volume control –20 dB; f_k = 100 Hz	–	35	–	dB
V_{12}	output voltage when muted		–	2.5	–	V
V_{12}	output level shift due to muting	volume control –20 dB	–	–	0.5	dB
S/N	signal-to-noise ratio	note 16	–	47	–	dB
V_{11}	voltage with pin 11 disconnected		–	6	–	V
I_{11}	current with pin 11 short-circuited to ground		–	1	–	mA
V_{12}	temperature dependance of the output signal amplitude	T_{amb} = 20 to 65 °C; –30 dB volume control and voltage of pin 11 fixed; note 27	–	2.5	–	dB
Volume control (note 17; see Fig.8)						
R_{11}	external control resistor	note 17	–	4.7	–	kΩ
OSS	suppression of output signal during mute condition		60	66	–	dB
Horizontal synchronization circuit (see Fig.9)						
SYNC SEPARATOR						
V_{25}	required sync pulse amplitude	note 20	200	750	–	mV
I_{25}	input current (pin 25)	V_{25} > 5 V	–	8	–	μA
		V_{25} = 0 V	–	10	–	mA
FIRST CONTROL LOOP						
±Δf	PLL holding range		–	1500	2000	Hz
±Δf	PLL catching range		600	1500	–	Hz
	control sensitivity to oscillator	note 21	see Fig.10			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{8-9}	IF input signal at which the time constant is switched (RMS value)	strong-to-weak	–	2.2	–	mV
SECOND CONTROL LOOP (POSITIVE EDGE)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity	note 22	–	100	–	
t_d	control range		–	25	–	µs
PHASE ADJUSTMENT (VIA SECOND CONTROL LOOP)						
	control sensitivity		–	25	–	µA/µs
α	maximum allowed phase shift		–	±2	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency	R = 34.3 kΩ; C = 2.7 nF	–	15625	–	Hz
Δf	spread with fixed external components		–	–	4	%
Δf_{fr}	frequency variations with supply voltage from 9.5 to 13.2 V		–	–	2	%
Δf_T	frequency variation with temperature	note 25	–	–1.6	–	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		–	–	10	%
Δf	frequency variation when only noise is received	note 25	–	–	500	Hz
HORIZONTAL OUTPUT (PIN 26; OPEN COLLECTOR)						
V_{26}	output limiting voltage		–	–	16.5	V
V_{OL}	LOW level output voltage	I_{sink} = 10 mA	–	0.2	0.5	V
I_{sink}	maximum sink current		10	–	–	mA
	duty factor of output signal		–	46	–	%
t_r	rise time of output pulse		–	260	–	ns
t_f	fall time of output pulse		–	100	–	ns
HORIZONTAL FLYBACK INPUT (PIN 27)						
I_{27}	required input current during flyback pulse		0.01	–	1.0	mA
COINCIDENCE DETECTOR						
V_{22}	voltage for in-sync condition		–	9.8	–	V
V_{22}	voltage for no-sync condition	no signal	–	1.5	–	V
V_{22}	switching level to the phase detector from fast to slow		6.2	6.7	7.2	V
V_{22}	hysteresis slow to fast		–	0.6	–	V
V_{22}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{22}	hysteresis mute function		–	2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay of mute release after transmitter insertion		–	–	300	µs
	allowable load on pin 22		–	–	10	µA
V_{22}	external video mode		–	–	0.7	V
I_{22}	current at pin 22	V_{22} = 0 V	–	–	0.8	mA
Vertical circuit (note 24)						
VERTICAL RAMP GENERATOR						
I_2	input current during scan		–	–	2	µA
I_2	discharge current during retrace		–	0.8	–	mA
$V_{2(p-p)}$	sawtooth amplitude (peak-to-peak value)		–	1.9	–	V
t	interlace timing of the internal pulses		30	32	34	µs
VERTICAL OUTPUT						
I_3	available output current	V_3 = 4 V	–	–	3	mA
V_3	maximum available output voltage	I_3 = 0.1 mA	4.4	5	–	V
VERTICAL FEEDBACK INPUT						
V_4	DC input voltage		2.9	3.3	3.7	V
$V_{4(p-p)}$	AC input voltage (peak-to-peak value)		–	1	–	V
I_4	input current		–	–	12	µA
Δt_p	internal pre-correction to sawtooth		–	3	–	%
	deviation amplitude	50/60 Hz	–	–	4	%
	temperature dependency of the amplitude	T_{amb} = 20 to 65 °C	–	–	2	%

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 9 mA is supplied to this pin, it is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS top sync input signal.
6. Projected zero point; i.e. with switched demodulator.
7. White 10% of the top sync amplitude.
8. Measured according to the test line illustrated by Fig.2. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig.3. The non–linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.

10. The test set–up and input conditions are illustrated by Fig.4. The figures are measured at an input signal of 10 mV RMS.
11. Measured with a source impedance of 75 Ω.

$$\textit{The signal–to–noise ratio} = 20 \log \frac{V_O \textit{ black–to–white}}{V_{n(RMS)} \textit{ at } B = 5 \textit{ MHz}}$$

12. The sound circuit is measured (unless otherwise specified) with an input signal of V_{15} of 50 mV RMS, a carrier frequency of 5.5 MHz at a Δf of 27.5 kHz. The QL of the demodulator tuned circuit is 16 and the volume control is connected to the supply. The reference circuit must be tuned in such a way tha the output is symmetrical clipping at maximum volume.
13. The test set-up is illustrated by Fig.6. The AM rejection curve (typical) is illustrated by Fig.7.
14. The output signal is measured at a Δf = 7.5 kHz and maximum volume control.
15. The demodulator tuned circuit must be tuned at minimum distortion.
16. Weighted noise, measured in accordance with CCIR 468.
17. See also note 1. The volume can be controlled by using a potentiometer connected to ground (value 4.7 kΩ) or by means of a variable direct voltage. In the latter event the relatively low input impedance must be taken into account.
18. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90 degree phase shift network.The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is followed by a sample-and-hold circuit which samples during the sync level. As a result the AFC output voltage contains no video information. The specified control slope decreases when the AFC oputput is loaded with two resistors between the voltage supply and ground.
19. At very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. The characteristics given for weak signals are measured with a SAW filter (OFW 1956) connected in front of the IC input signal such that the input signal of the IC is 150 μV RMS.
20. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 17 and 25. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
21. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 25) to the voltage supply. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head–errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
22. This figure is valid for an external load impedance of 82 kΩ between pin 28 and the phase adjustment potentiometer.
23. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse.
24. The vertical scan is synchronized by means of a divider system. Therefore no frequency adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
25. These figures are based on test samples.
26. Measured at an input signal amplitude of 150 μV RMS (pin 18).

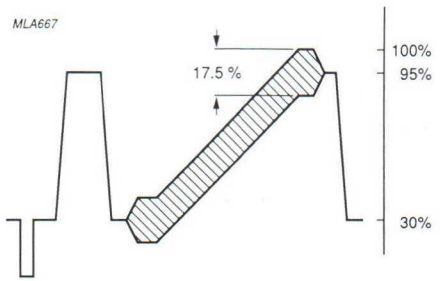


Fig.2 Video output signal.

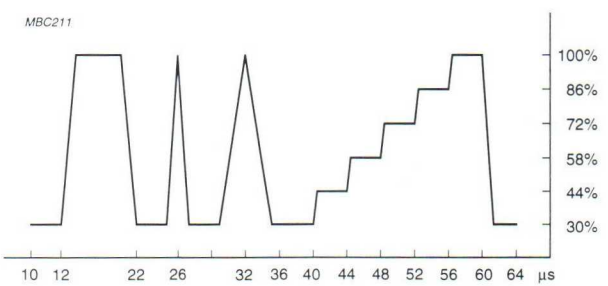
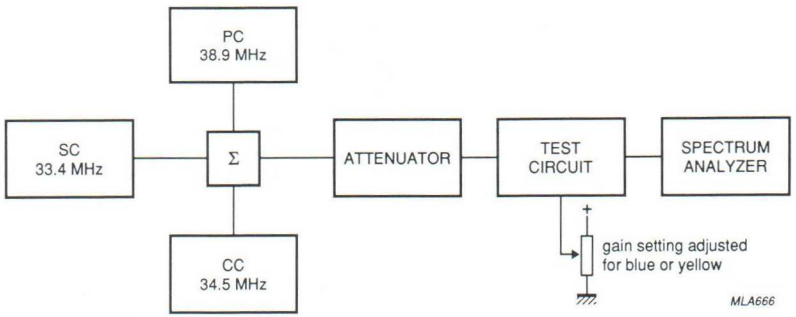
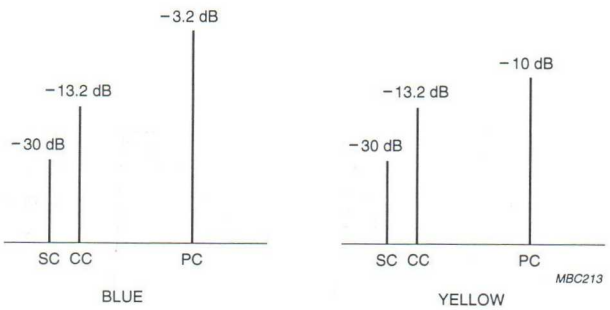


Fig.3 EBU test signal waveform (line 330).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to top sync level

$$\textit{Value at } 1.1\textit{MHz}: 20 \log \frac{V_O \textit{ at } 4.4\textit{MHz}}{V_O \textit{ at } 1.1\textit{MHz}} + 3.6\textit{dB}$$

$$\textit{Value at } 3.3\textit{MHz}: 20 \log \frac{V_O \textit{ at } 4.4\textit{MHz}}{V_O \textit{ at } 3.3\textit{MHz}}$$

Fig.4 Test set–up intermodulation.

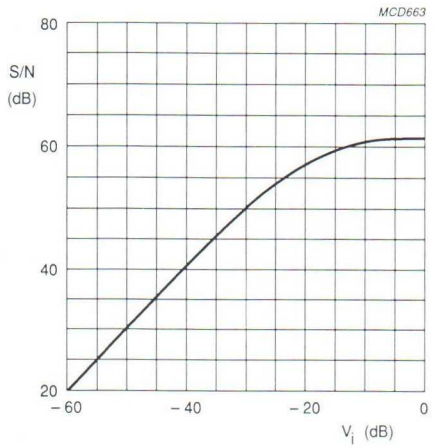


Fig.5 Signal-to-noise ratio as a function of the input voltage (0 dB = 100 mV).

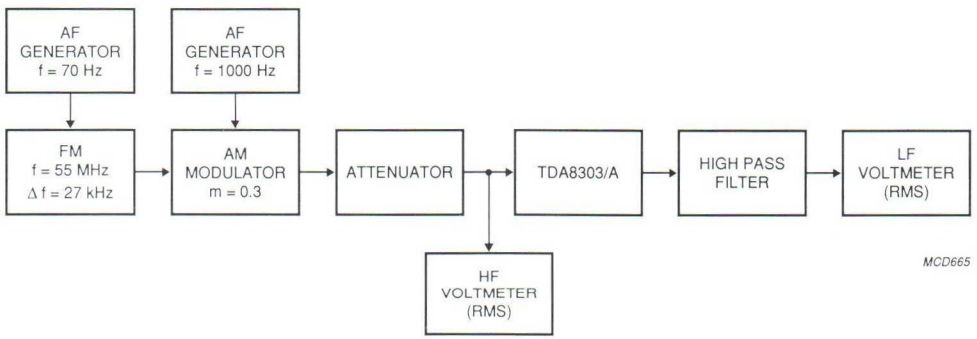


Fig.6 Test set-up AM suppression.

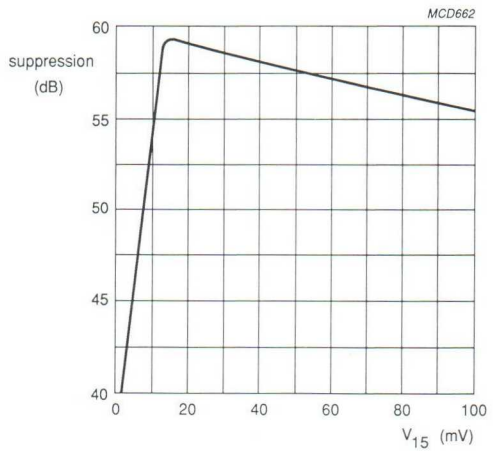


Fig.7 AM suppression.

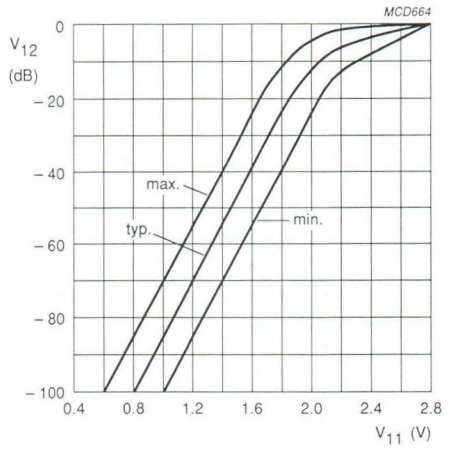


Fig.8 Volume control characteristics.

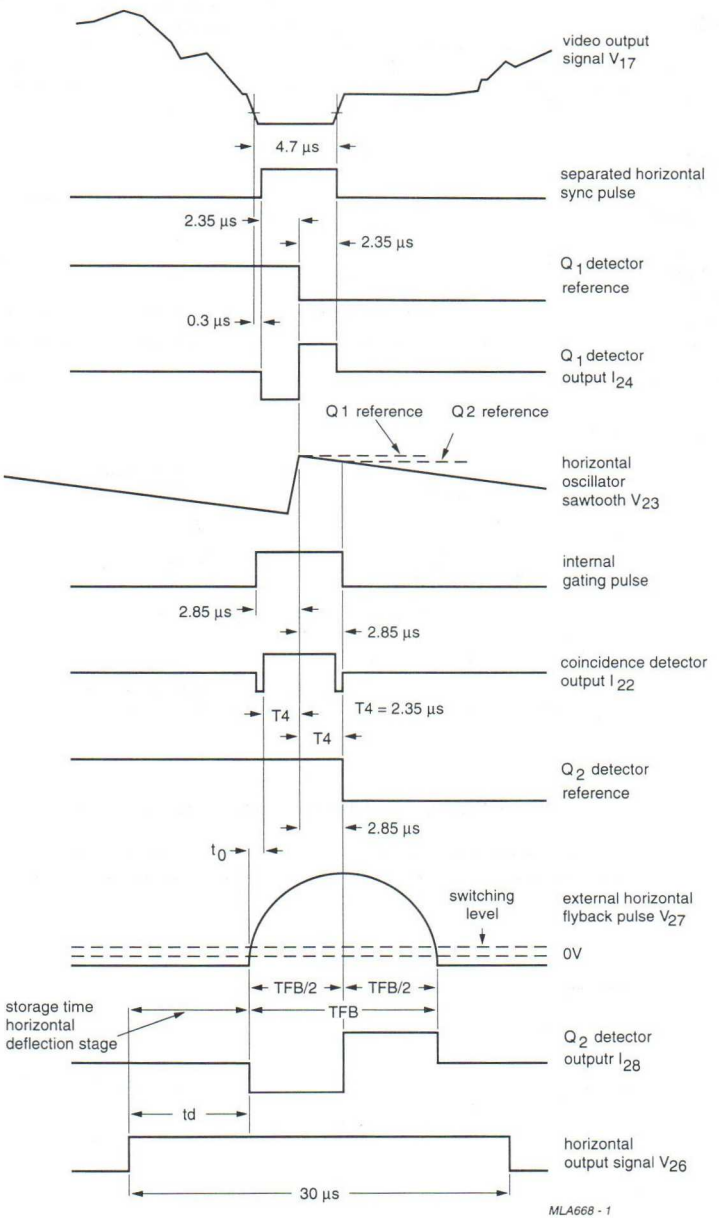


Fig.9 Timing diagram.

Table 1 Switching levels coincidence detector

CONDITION V_{22}	CONTROL SENSITIVITY HORIZONTAL OSCILLATOR (kHz/µs)	
	T2 – T1	T3 = SCAN
$V_{22} > 6.7$ V and strong signal weak signal	 11.3 1.3	 7.6 1.3
$1 < V_{22} < 5.7$ V and strong signal weak signal	 11.3 11.3	 7.6 7.6
$V_{22} < 0.7$	11.3	7.6

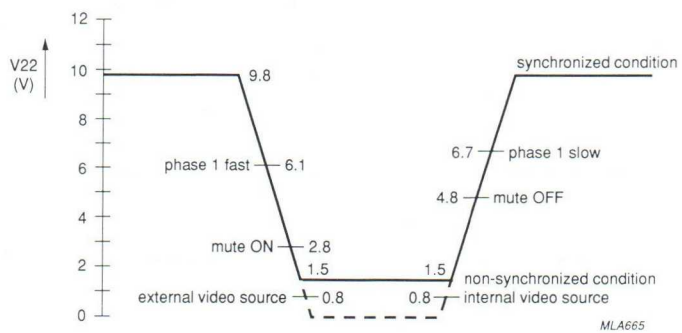


Fig.10 Switching levels coincidence detector.

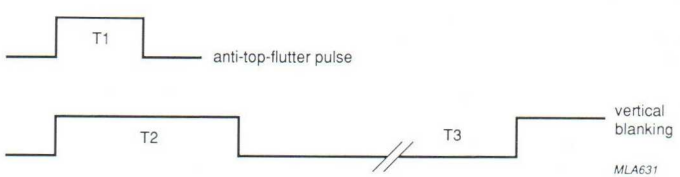


Fig.11 Anti-top-flutter pulse.

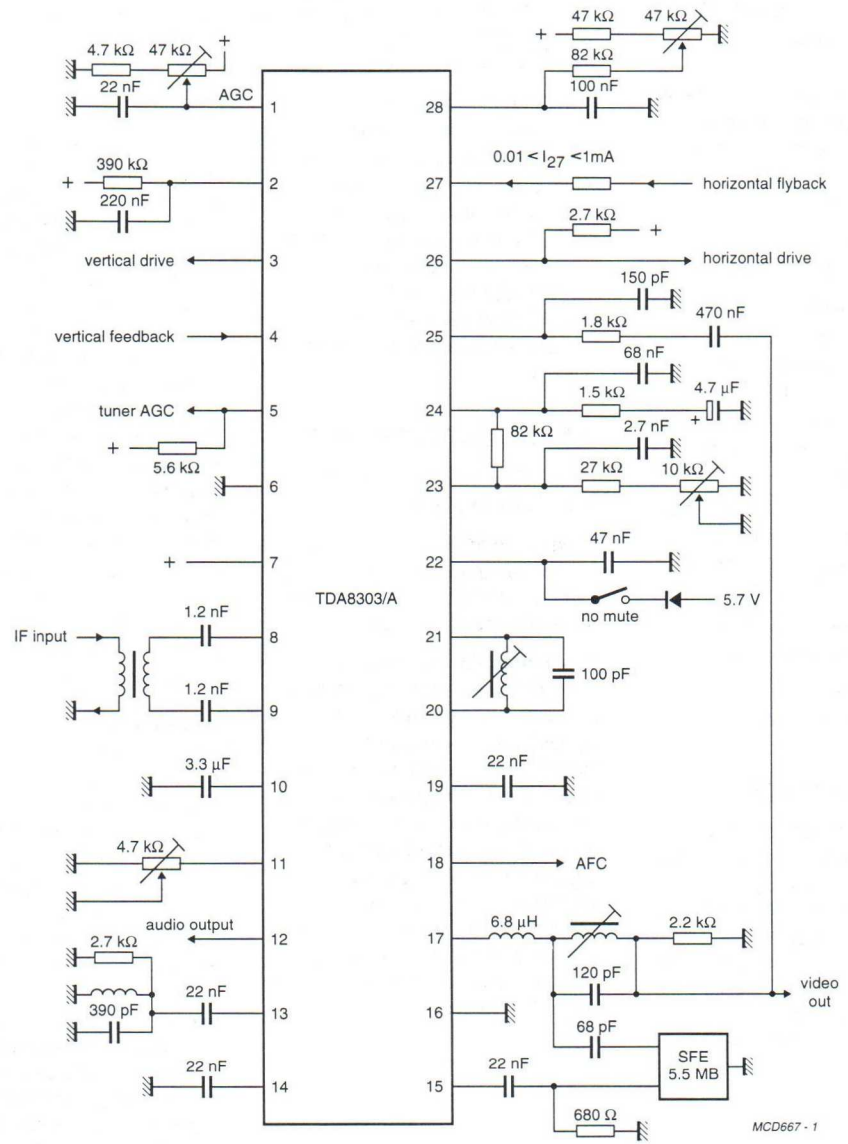


Fig.12 Application diagram.

Small signal combination IC for colour TV

TDA8304

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on vision peak white level for positive demodulation
- Tuner AGC
- AFC circuit with on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- Auto VCR switch
- 50/60 Hz identification

GENERAL DESCRIPTION

The TDA8304 possesses the capability to demodulate IF signals having either positive or negative-going video information. It is housed within a 32-pin encapsulation. The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8304	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync (where a non-modulated carrier is present). When receiving signals with positive modulation the AFC is continuously active but extensively filtered. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
V_{25}	video transmitter identification output no signal condition signal condition		 - -	 0.3 9.8	 - -	 V V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

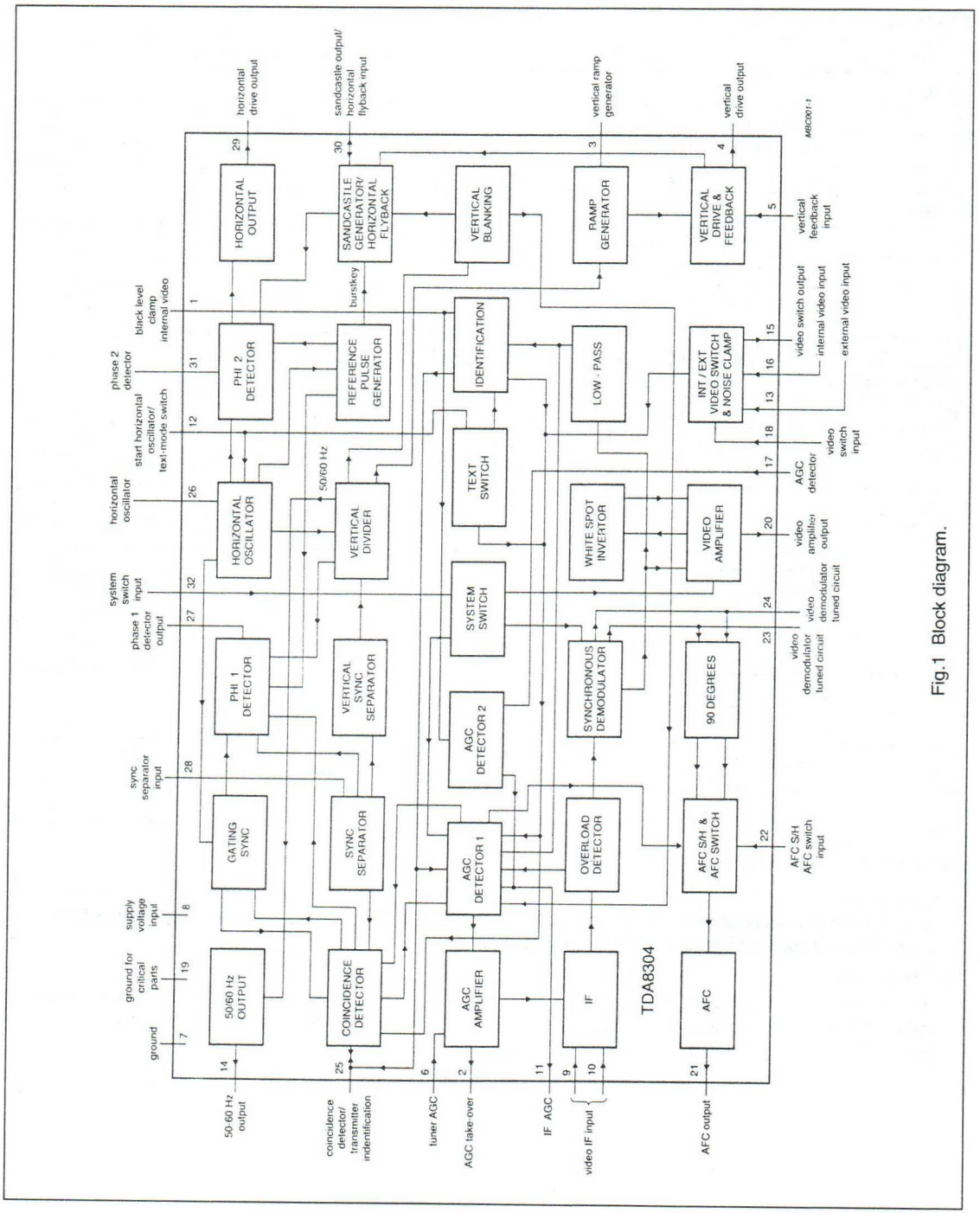


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator/text-mode switch
13	external video input
14	50 - 60 Hz output
15	video switch output
16	internal video input
17	AGC detector
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	system switch input

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level and on peak white level with those having positive modulation. Selection is facilitated by the system switch (pin 32), see Table 1.

The charge current at positive modulation (see Table 2) is only present during the vertical sync or when the level at pin 1 drops 200 mV below the level of pin 17 as a result of input signal variations. To obtain rapid AGC action when executing a search tuning operation when the circuit is set for peak white AGC, the charge current is increased to 55 μA until the detection of a transmitted signal. With an AGC capacitor of 6.8 μF the video tilt will be < 2% for positive and for negative modulated signals.

VCR switch

The TDA8304 has an auto VCR-switch facility. Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the internal video mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a long time constant. The phase detector is not gated in the 'VCR' mode and operates with a short time constant. The TDA8304 is active in the 'VCR' mode only at reception of an external video signal.

Video-switch

Selection between internal video (pin 16) and external video (pin 13) is made by applying a switching potential to pin 18 (see Table 3). Video output (pin 20) from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8304 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. The AGC detector is not gated during the external video mode, the first phase detector is also not gated and operates with a short time constant. The gain of the

IF amplifier (in the external video mode) is reduced to prevent crosstalk of the video amplifier to the horizontal oscillator during the no-signal condition.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8304 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8304 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The vertical frequency is alignment free. The divider automatically adapts to a vertical frequency of 50 Hz or 60 Hz including automatic amplitude correction and its operating modes offer maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse. Internally clockpulses are generated by doubling the line frequency. The divider operates in the 60 Hz mode when the trigger pulse appears before count 576, otherwise the 50 Hz mode will be active.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window (divider ratio between 488 and 722). This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz) or 622 - 628 (50 Hz)

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for 50 Hz and at count 12 for 60 Hz.
- The divider is switched to count 625 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.
- The divider is switched to the large window mode when enlarged vertical sync pulses are detected.

Table 1 AGC circuit operation

STATE	POSITIVE MODULATION	NEGATIVE MODULATION
input pin 32	HIGH/open	LOW

Table 2 AGC detector currents

STATE	POSITIVE MODULATION		NEGATIVE MODULATION	
action	current	condition	current	condition
charge	10 μA	V-sync signal	55 μA	-
charge	55 μA	pin 25 = LOW	-	-
discharge	3 mA	VITS signal	1.5 mA	H-sync signal

Table 3 Video switch operation

STATE	INTERNAL VIDEO	EXTERNAL VIDEO
input pin 18	LOW	HIGH

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

The transmitter identification/coincidence detector

Pin 25 of the TDA8304 serves as the transmitter identification and/or coincidence detector (see Table 4). Pin 25 is HIGH (= 9.8 V) when a transmitter is present and LOW (= 0.3 V) when of no transmitter signal is detected. When the video switch is in the internal mode, the signal at the sync separator input (pin 28) is the demodulated IF signal, pin 25 will act as a coincidence detector. Pin 25 is HIGH when the horizontal oscillator loop is synchronized with the video signal and LOW in case of no synchronization. In the external video mode and in the text mode, pin 25 will be active as transmitter identification. The system relies upon the detection of sync pulses on the incoming IF signal. Pin 25 is charged with a current of 125 μA by the separated horizontal sync pulse and discharged continuously with a current of 4 μA. The high impedance of pin 25 should be taken into account in the application concept.

The 50/60 Hz identification

The 50/60 Hz information (see Table 5) derived from the divider system is available at the open collector output pin 14.

Table 4 Transmitter identification/coincidence detector

STATE	INTERNAL VIDEO					EXTERNAL VIDEO	
input pin 18	LOW					HIGH	
input pin 12	TV mode = HIGH		Text mode = LOW				
Input signal pins 9 and 10	yes	none	yes	none	none	yes	none
input pin 28	50/60 Hz	none	50/60 Hz	VCS text	none	don't care	don't care
output pin 25	9.8 V	0.3 V	9.8 V	0.3 V	0.3 V	9.8 V	0.3 V

Table 5 50/60 Hz identification

INPUT/OUTPUT	STATUS	STATUS	STATUS
Input signal pins 9 and 10	don't care	don't care	don't care
input pin 28	50 Hz	60 Hz	none
output pin 14	0.3 V	12 V	0.3 V

CHARACTERISTICS

T_{amb} = 25 °C; V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9\text{-}10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	μV
$R_{9\text{-}10}$	differential input resistance	note 3	-	1300	-	Ω
$C_{9\text{-}10}$	differential input capacitance	note 3	-	5	-	pF
$G_{9\text{-}10}$	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
$V_{9\text{-}10}$	maximum input signal		100	170	-	mV
$V_{9\text{-}10(rms)}$	input sensitivity in external mode (RMS value)	note 2	250	400	650	μV
Video Amplifier (notes 5 and 6)						
V_{20}	negative modulation, zero signal level		4.7	4.9	5.1	V
V_{20}	positive modulation, zero signal level		2.5	2.7	2.9	V
V_{20}	peak sync (negative modulation)	note 7	2.5	2.75	3.0	V
V_{20}	white level (positive modulation)	note 7	4.7	4.9	5.1	V
V_{20}	white spot threshold level		-	5.7	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 8	-	2	5	%
φ	differential phase	note 8	-	2	5	deg
NL	video non-linearity	note 9	-	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	-	dB
	1.1 MHz; yellow		50	60	-	dB
	3.3 MHz; blue		55	65	-	dB
	3.3 MHz; yellow		55	65	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 11; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV
System switch (note 12)						
AGC ON PEAK SYNC LEVEL FOR NEGATIVE MODULATION SIGNALS						
V_{32}	control voltage		0	-	0.8	V
I_{32}	input current		−100	-	−500	µA
AGC ON WHITE LEVEL FOR POSITIVE MODULATION SIGNALS						
V_{32}	control voltage		2	-	12	V
I_{32}	input current		0	-	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_1	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
AGC detection level						
I_{17}	charge current		-	200	-	µA
I_{17}	discharge current		-	20	-	µA
V_{17}	clamp level		-	2.9	-	V
Video switching circuit (note 13)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
$V_{16(p-p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 14 and 24	-	55	-	dB
α	crosstalk internal to external	notes 14 and 24	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
Text/TV switch						
V_{12}	input voltage for text mode		-	-	0.8	V
V_{12}	input voltage for TV mode		2	-	V_P	V
I_{12}	maximum current	V_{12} = 0 V	-	-	0.3	mA
		V_{12} = 11.5 V	-	-	1.5	mA
AFC-circuit (note 15)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{LI}	leakage current (pin 22)		-	-	1	µA
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 16 and 24	-	11	-	V
	control slope	notes 16 and 24	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 16 and 24	-	–2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	µA
		V_{28} = 0 V	-	–10	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow (RMS value)		-	2.2	-	mV
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 19	-	100	-	
t_d	control range		-	25	-	µs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	µA/µs
α	maximum allowed phase shift		-	±2	-	µs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15625	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 10 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 24	-	−1.6	-	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 24	-	-	500	Hz
Horizontal output (open collector; pin 29)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 20)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
t_W	pulse width of burstkey at 60 Hz signals at 50 Hz signals		 2.9 3.2	 3.3 3.6	 3.7 4	 µs µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input and sandcastle output (note 20)						
	width of horizontal blanking pulse		flyback pulse width			
	width of vertical blanking pulse					
	divider in search window	50 Hz	-	21	-	lines
		60 Hz	-	17	-	lines
	divider in narrow window	50 Hz	-	25	-	lines
		60 Hz	-	21	-	lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse	60 Hz				
	trailing edge		-	-	9.3	µs
	rising edge		4.7	5.4	6.1	µs
Vertical ramp generator (note 22)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 24	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%
	deviation amplitude 50/60 Hz		-	-	2	%
	temperature dependency of the amplitude	note 24 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 23; V_{30} = 2.5 V				
	guard level LOW		-	1.5	-	V
	guard level HIGH		-	2	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Coincidence detector/transmitter identification (note 21)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2.0	-	V
I_{25}	load (allowed) at pin 25		–2	-	2	μA
50/60 Hz identification (open collector output)						
V_{14}	output voltage at 50 Hz (no signal)		-	0.3	0.5	V
V_{14}	output voltage at 60 Hz		-	V_p	-	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	μA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. The output signal amplitude is determined by the AGC detector. For negative modulation the peak sync level is used as reference. With positive modulation the white level is stabilized.
8. Measured according to the test line given in Fig. 3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig. 5. The figures are measured at an input signal of 10 mV RMS.
11. Measured with a source impedance of 75 Ω.

    $$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at} \ B = 5 \ \textit{MHz}}$$

12. By means of the system switch 2 conditions can be obtained. Negative modulation with peak sync level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.

13. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
14. Defined as 20 log $\frac{V_O \textit{ unwanted video black-to-white}}{V_O \textit{ wanted video-black-to-white}}$; measured at 4.4 MHz.
15. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
16. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
19. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
22. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
23. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level (V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
24. These figures are based on test samples.

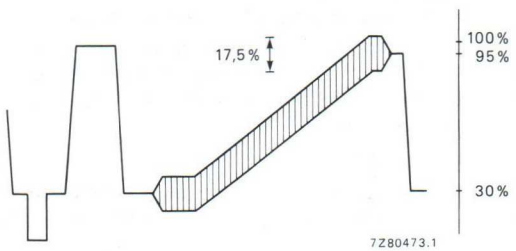


Fig.2 Video output signal.

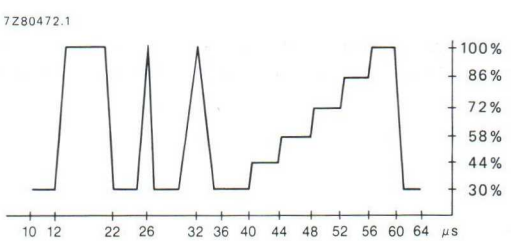
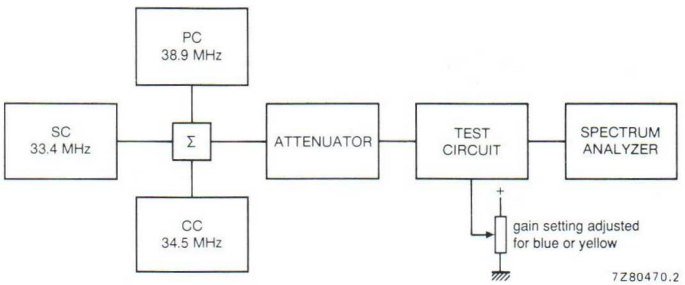
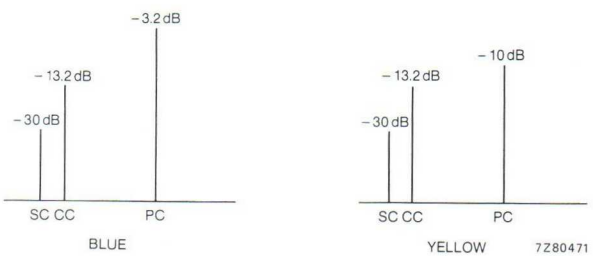


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$\textit{Value at } 1.1\textit{MHz} : 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 1.1\textit{MHz}} + 3.6\textit{dB}$$

$$\textit{Value at } 3.3\textit{MHz} : 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 3.3\textit{MHz}}$$

Fig.4 Test set-up intermodulation.

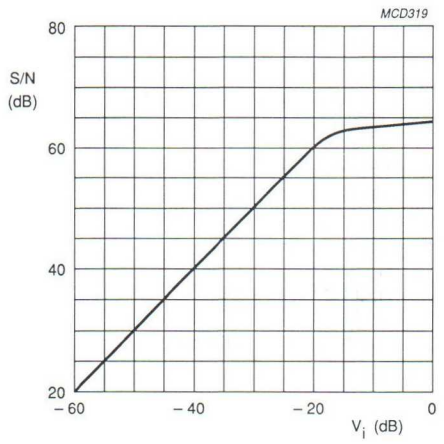
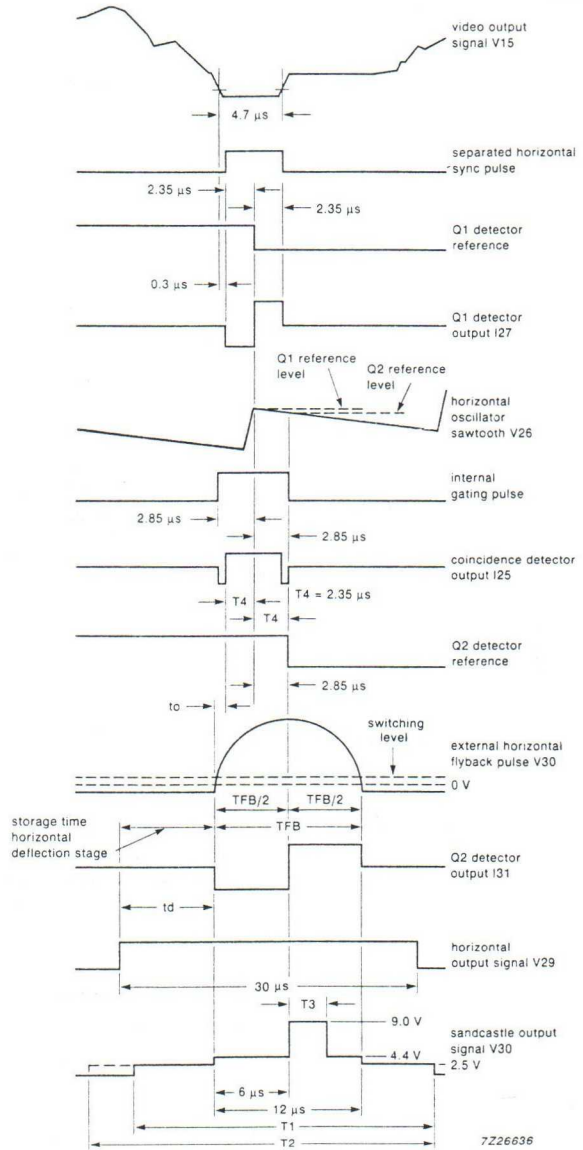


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 42p (50 Hz); 34p (60 Hz); $p = 1/2f_H$

T2: divider in narrow window: 50p (50 Hz); 42p (60 Hz)

T3: 3.6 µs (50 Hz); 3.3 µs (60 Hz)

Fig.6 Timing diagram.

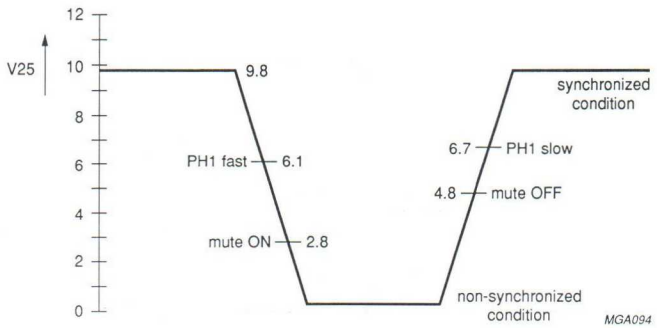


Fig.7 Switching levels coincidence detector.

CONDITION PIN 18 VIDEO SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
		T2 - T1	T3 = SCAN
Low internal video	V_{25} > 6.7 V and strong signal	11.3	7.6
	V_{25} > 6.7 V and weak signal	1.3	1.3
	V_{25} < 6.1 V and strong signal	11.3	7.6
	V_{25} < 6.1 V and weak signal	11.3	7.6
HIGH or floating external video	don't care	11.3	7.6

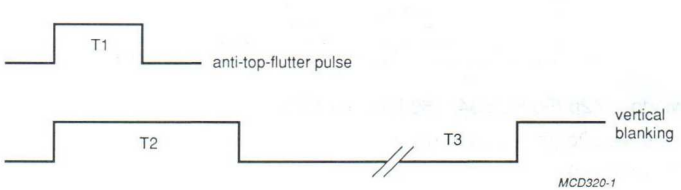


Fig.8 Anti-top-flutter-pulse.

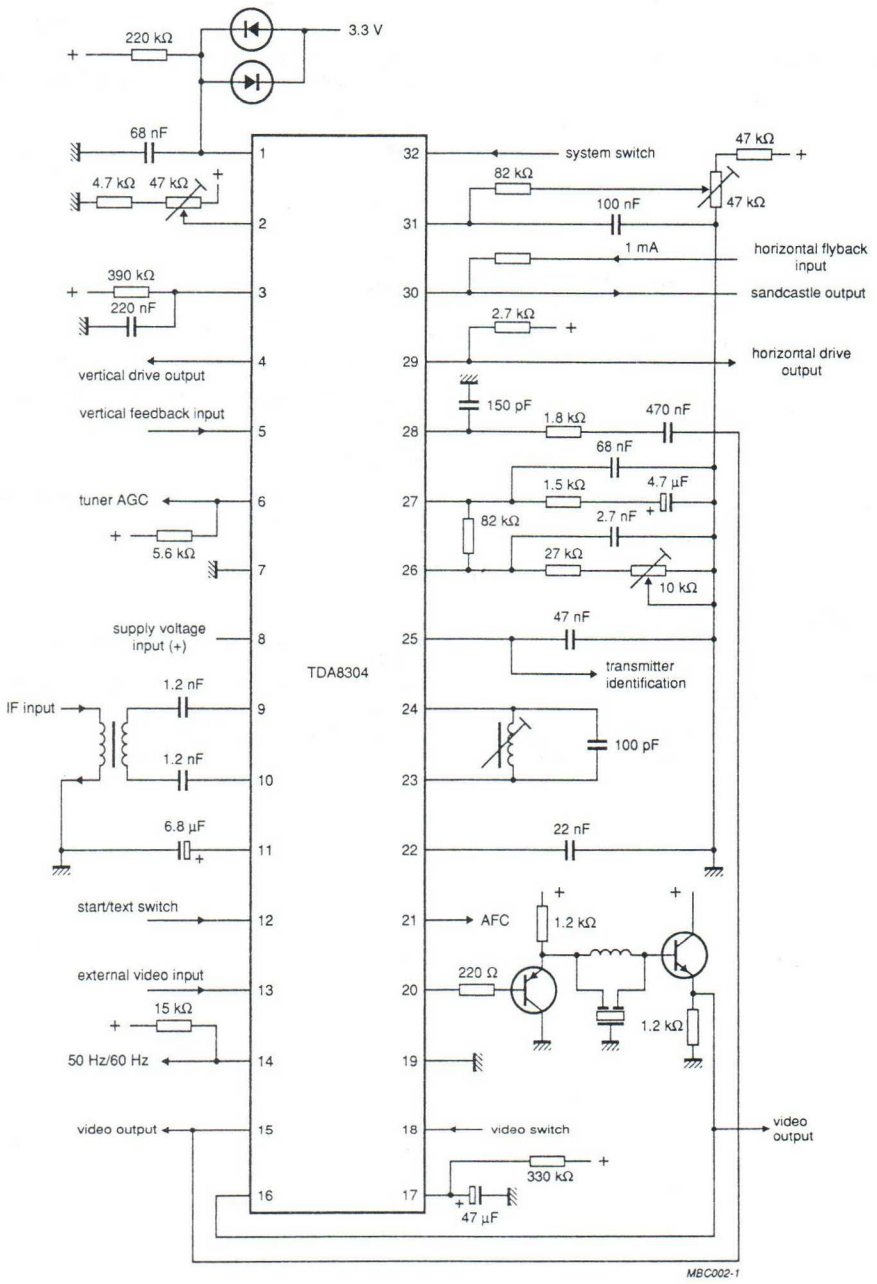


Fig.9 Application diagram.

PAL/NTSC colour processor for PIP applications

TDA8310

FEATURES

- Multistandard vision IF circuit (positive and negative modulation)
- Video switch which automatically detects whether the incoming signal is CVBS or Y/C
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Automatic PAL/NTSC decoder which can decode all standards available in the world
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- Horizontal PLL with an alignment-free horizontal oscillator
- Vertical count-down circuit
- RGB/YUV and fast blanking switch with 3-state output and active clamping
- Low dissipation (560 mW)
- Small amount of peripheral components compared with competition ICs.

GENERAL DESCRIPTION

The TDA8310 is an alignment-free PAL/NTSC colour processor for Picture-in-Picture (PIP) applications. The circuit contains a vision IF amplifier, a PAL/NTSC colour decoder, horizontal and vertical synchronization and an RGB/YUV switch.

As input for the colour decoder and sync processor the demodulated IF signal can be chosen but the circuit also has a video input which automatically detects whether the incoming signal is CVBS or Y/C. The output signals for the PIP processor are:

Luminance signal

Colour difference signals (U and V)

Horizontal and vertical synchronization pulses.

The RGB/YUV switch can select between two RGB or YUV sources, e.g. between the PIP processor and the SCART input signal.

The supply voltage for the IC is 8 V. It is available in a 52-pin SDIP package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8310	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 19 and 41)	7.2	8.0	8.8	V
I_P	supply current	–	70	–	mA
Input voltages					
$V_{i(rms)}$	vision IF amplifier input sensitivity (RMS value)	–	70	100	μV
$V_{17,20(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	–	1	1.4	V
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	–	0.3	–	V
$V_{i(p-p)}$	RGB/YUV input signal voltage amplitude (peak-to-peak value)	–	–	1.3	V
Output signals					
$V_{o(p-p)}$	demodulated CVBS output voltage (peak-to-peak value)	–	2.5	–	V
V_{29}	tuner AGC control output voltage	0	–	12	V
$V_{o(p-p)}$	luminance output voltage (peak-to-peak value)	–	1.4	–	V
$V_{50(p-p)}$	(B–Y) output voltage (peak-to-peak value)	1.06	1.33	1.60	V
$V_{51(p-p)}$	(R–Y) output voltage (peak-to-peak value)	0.84	1.05	1.26	V
V_{39}	horizontal sync pulse output voltage	–	4	–	V
V_{36}	vertical sync pulse output voltage	–	4	–	V
G_v	voltage gain of the RGB switches	–0.5	0	+0.5	dB
Control voltage					
$V_{control}$	control voltage for HUE	0	–	5	V

BLOCK DIAGRAM

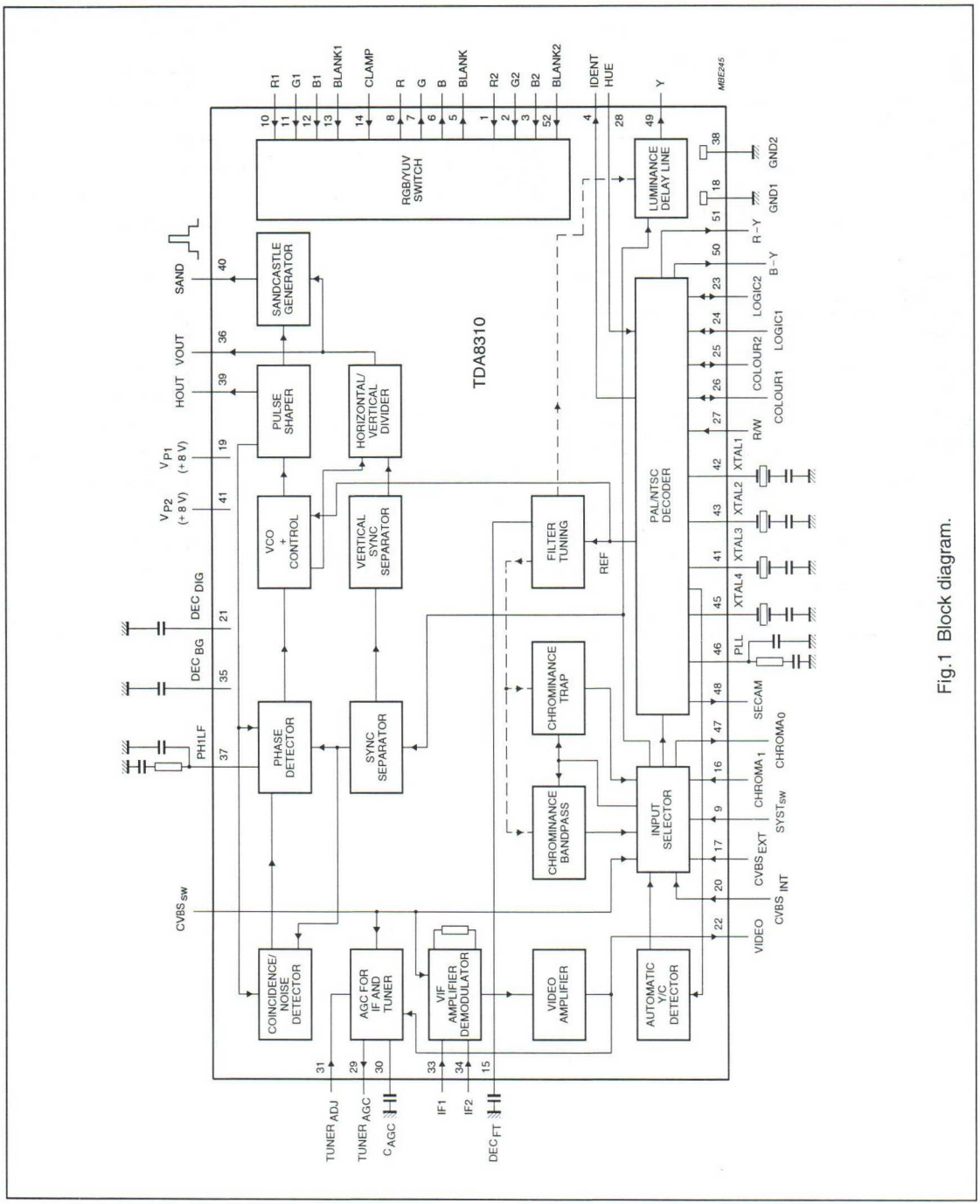


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
R2	1	RED input 2 (PIP)
G2	2	GREEN input 2 (PIP)
B2	3	BLUE input 2 (PIP)
IDENT	4	colour standard identification output
BLANK	5	blanking output
B	6	BLUE output
G	7	GREEN output
R	8	RED output
$SYST_{SW}$	9	system switch
R1	10	RED input 1
G1	11	GREEN input 1
B1	12	BLUE input 1
BLANK1	13	blanking input 1
CLAMP	14	clamping pulse input
DEC_{FT}	15	decoupling filter tuning
$CHROMA_I$	16	chrominance input
$CVBS_{EXT}$	17	external CVBS input
GND1	18	ground 1 (0 V)
V_{P1}	19	supply voltage 1 (+8 V)
$CVBS_{INT}$	20	internal CVBS input
DEC_{DIG}	21	decoupling digital supply
VIDEO	22	IF video output
LOGIC2	23	crystal logic 2 input/output
LOGIC1	24	crystal logic 1 input/output
COLOUR2	25	colour system logic 2 input/output
COLOUR1	26	colour system logic 1 input/output
R/W	27	read/write selection input

SYMBOL	PIN	DESCRIPTION
HUE	28	HUE control input
$TUNER_{AGC}$	29	tuner AGC output
C_{AGC}	30	AGC filter capacitor
$TUNER_{ADJ}$	31	tuner take-over adjustment input
$CVBS_{SW}$	32	CVBS positive/negative modulation control switch input
IF1	33	IF input 1
IF2	34	IF input 2
DEC_{BG}	35	bandgap decoupling
VOUT	36	vertical sync output pulse
PH1LF	37	phase 1 loop filter
GND2	38	ground 2 (0 V)
HOUT	39	horizontal sync output pulse
SAND	40	sandcastle pulse output
V_{P2}	41	supply voltage 2 (+8 V)
XTAL1	42	4.4336 MHz crystal
XTAL2	43	3.5820 MHz crystal for PAL-N
XTAL3	44	3.5756 MHz crystal for PAL-M
XTAL4	45	3.5795 MHz crystal for NTSC
PLL	46	PLL colour filter
$CHROMA_O$	47	chrominance output for TDA8395
SECAM	48	SECAM reference output
Y	49	Y output
B–Y	50	B–Y output
R–Y	51	R–Y output
BLANK2	52	blanking/insertion input 2 (PIP)

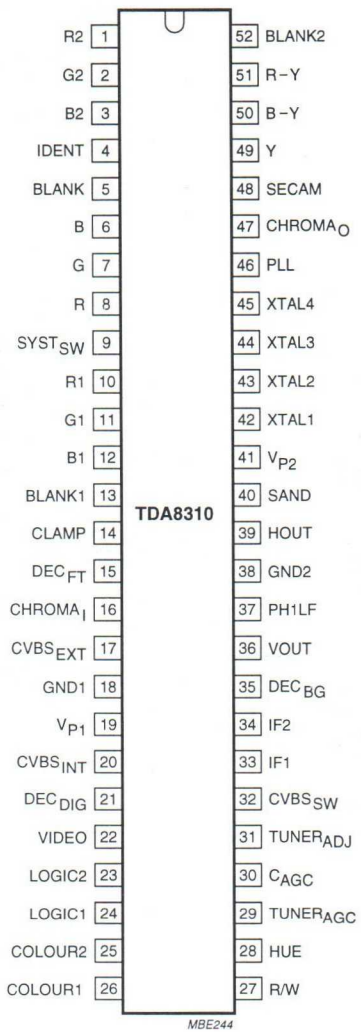


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The IF amplifier contains three AC-coupled control stages with a total gain control range >60 dB. The sensitivity of the circuit is comparable with that of modern IF-ICs. The demodulation of the IF signal is achieved by a multiplier. The demodulator is alignment-free and does not require external components.

The polarity of the demodulator can be switched to make the circuit suitable for positive and negative modulated signals.

The AGC detector operates on top-sync or top white-level depending on the position of the demodulator. The AGC detector time-constant capacitor is externally connected to facilitate flexibility of the application. During positive modulation the time-constant of the AGC system is too long to avoid visible variations of the signal amplitude. To obtain an acceptable speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When no action is detected during three frame periods the speed of the system is increased.

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are then fed to the slicing stage (separator) which operates at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used to detect whether the line oscillator is synchronized and for transmitter identification. The first PLL has a very high static steepness, this ensures that the phase of the picture is independent of the line frequency. The line oscillator operates at twice the line frequency.

The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC.

The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.

The horizontal output pulse is derived from the horizontal oscillator via a pulse shaper. The pulse width of the output pulse is 5.4 μs, the front edge of this pulse coincides with the front edge of the sync pulse at the input.

The vertical output pulse is generated by a count-down circuit. The pulse width is approximately 380 μs. Both the horizontal and vertical pulses will always be available at the outputs even when no input signal is available.

In addition to the horizontal and vertical sync pulse outputs the IC has a sandcastle pulse output which contains burst key and blanking pulses.

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by gyrator circuits that are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. When a Y/C signal is supplied to the input the chrominance trap is automatically switched off by the Y/C detection circuit, but it is also possible to force the filters in the CVBS or Y/C position.

The luminance delay line is also realised by gyrator circuits.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally.

The colour decoder is very flexible. Together with the SECAM decoder TDA8395 an automatic multistandard decoder can be designed but it is also possible to use it for one standard when only one crystal is connected to the IC. The decoder can be forced to one of the standards via the "forced mode" pins. The crystal pins which are not used must be connected to the positive supply line via a 8.2 kΩ resistor. It is also possible to connect the non-used pins with one resistor to the positive supply line. In this event the resistor must have a value of 8.2 kΩ divided by the number of pins.

The chrominance output signal of the video switch is externally available and must be used as an input signal for the SECAM decoder.

RGB/YUV switch

The RGB/YUV switch is for switching between two RGB or YUV video sources. The outputs of the switch can be set to high impedance state so that other switches can be used in parallel.

The switch is controlled via pins 13 and 52. The details of switch control are shown in Table 5.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–25	+70	°C
T_{sld}	soldering temperature for 5 s		–	260	°C
T_j	maximum operating junction temperature		–	150	°C
V_{es}	electrostatic discharge	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model 100 pF, 1500 Ω.
2. Machine model 200 pF, 0 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	≤40	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011. All pins are protected against electrostatic discharge by means of internal clamping diodes.

Latch up

At T_{amb} = 70 °C most pins meet the specification:

$I_{trigger} \geq 100$ mA or $\geq 1.5\ V_{DDmax}$

$I_{trigger} \leq -100$ mA or $\leq -0.5\ V_{DDmax}$.

The following pins do not meet this specification:

pin 7 +90 mA

pin 21 +90 mA

pin 32 –90 mA

pin 46 +90 mA.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pins 19 and 41)		7.2	8.0	8.8	V
I_{P1}	supply current (pin 19)		45	65	80	mA
I_{P2}	supply current (pin 41)		3	5	10	mA
P_{tot}	total power dissipation		–	560	–	mW
IF circuit						
VISION IF AMPLIFIER INPUT (PINS 33 AND 34)						
$V_{i(rms)}$	input sensitivity (RMS value)	note 1				
		f_i = 38.90 MHz	–	70	100	μV
		f_i = 45.75 MHz	–	70	100	μV
		f_i = 58.75	–	70	100	μV
R_I	Input resistance (differential)	note 2	1.6	2.0	2.4	kΩ
C_I	Input capacitance (differential)	note 2	–	3	–	pF
G_{cr}	gain control range	note 3	64	–	–	dB
$V_{i(rms)}$	maximum input signal (RMS value)		100	150	–	mV
VIDEO AMPLIFIER OUTPUT; note 4 (PIN 22)						
$V_{22(neg)}$	negative modulation					
	zero signal output level	note 5	4.45	4.60	4.75	V
	top sync level		1.9	2.0	2.1	V
$V_{22(pos)}$	positive modulation					
	zero signal output level	note 5	1.85	2.00	2.15	V
	white level		4.2	4.3	4.4	V
ΔV_{22}	difference in amplitude between negative and positive modulation		–	0	15	%
Z_O	video output impedance		–	–	75	Ω
I_{bias}	internal bias current of NPN emitter follower output transistor		1	–	–	mA
I_{source}	maximum source current		–	–	5	mA
S/N	signal-to-noise ratio	notes 6 and 7				
		V_i = 10 mV	52	60	–	dB
		end of control range	52	61	–	dB
$V_{22(rc)}$	residual carrier signal	note 6	–	2.5	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AND TUNER AGC						
Timing of IF-AGC (C_{30} = 2.2 µF)						
	modulated video interference	30% AM for 1 to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
t_{inc}	response time for an IF input signal amplitude increase of 52 dB for positive and negative modulation		–	2	5	ms
t_{dec}	response time for an IF input signal amplitude decrease of 52 dB					
	for negative modulation		–	25	50	ms
	for positive modulation		–	100	200	ms
I_{leak}	allowed leakage current of the AGC capacitor	note 8				
	for negative modulation		–	–	10	µA
	for positive modulation		–	–	200	nA
Tuner take-over adjustment (pin 31)						
$V_{31(rms)}$	minimum starting level voltage for tuner take-over (RMS value)		–	0.2	0.5	mV
$V_{31(rms)}$	maximum starting level voltage for tuner take-over (RMS value)		100	150	–	mV
V_{cr}	control voltage range		0.5	–	4.5	V
Tuner control output (pin 29)						
V_{29}	maximum tuner AGC output voltage	maximum gain	–	–	12	V
$V_{29(sat)}$	output saturation voltage	minimum gain; I_{29} = 2 mA	–	–	300	mV
I_{29}	maximum tuner AGC output current swing		5	–	–	mA
I_{leak}	leakage current RF AGC		–	–	1	µA
ΔV_{29}	input signal voltage variation for complete tuner control	$I_{O(max)}$ = 1 mA	0.5	2.0	4.0	dB
CVBS and Y/C switch						
INTERNAL CVBS AND EXTERNAL CVBS/Y INPUTS (PINS 20 AND 17)						
$V_{20,17(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	notes 2 and 9	–	1	1.4	V
$I_{20,17}$	input current		–	4	6	µA
V_{clamp}	top sync clamping voltage level		–	3.3	–	V
I_{clamp}	clamping input current		80	100	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE INPUT (PIN 16)						
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	notes 2, 10 and 17	–	0.3	–	V
$V_{16(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 6	1.0	–	–	V
R_I	chrominance input resistance		14	20	26	kΩ
C_I	chrominance input capacitance	note 2	–	–	5	pF
CHROMINANCE OUTPUT (PIN 47)						
$V_{47(p-p)}$	output signal voltage amplitude (peak-to-peak value)		0.18	0.20	0.22	V
Z_O	output impedance		200	250	300	Ω
V_O	DC output voltage	open-circuit output	1.2	1.4	1.6	V
SWITCH CONTROL INPUT FOR INTERNAL/EXTERNAL POSITIVE/NEGATIVE MODULATION; note 11 (PIN 32)						
V_{32}	internal CVBS signal selected with negative modulation with positive modulation	 note 12	 – 2	 – –	 1 3	 V V
V_{32}	external CVBS or Y/C signal selected	IF switched to negative modulation	3.9	–	V_P	V
Z_I	input impedance		25	–	–	kΩ
ISS	suppression of non-selected video input signal	note 6	50	–	–	dB
SWITCH CONTROL INPUT FOR EXTERNAL CVBS OR Y/C SELECTION (PIN 9)						
V_9	filters switched to CVBS condition		–	–	1	V
V_9	filters switched to Y/C condition	note 12	2	–	3	V
V_9	automatic selection of CVBS or Y/C		3.9	–	V_P	V
Z_I	input impedance		25	–	–	kΩ
Chrominance filters, luminance delay line and luminance output						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{osc}	–	MHz
QF	trap quality factor	notes 6 and 13	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BANDPASS CIRCUIT						
f_c	centre frequency		–	f_{osc}	–	MHz
QBP	bandpass quality factor	note 6	–	3	–	
Y DELAY LINE						
Δt_d	difference in delay time between the luminance and the demodulated chrominance signals	note 6	0	50	100	ns
B	bandwidth of internal delay line	note 6	8	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Y OUTPUT (PIN 49)						
$V_{49(b-w)}$	output signal voltage amplitude (black-to-white value)	note 29	0.8	1.0	1.2	V
Z_O	output impedance		80	100	120	Ω
$V_{49(DC)}$	DC output voltage level (top sync)		2.7	2.9	3.1	V
I_{bias}	internal bias current of NPN emitter follower output transistor		0.4	0.5	–	mA
I_{source}	maximum source current		–	–	2	mA
Horizontal and vertical synchronization circuits						
SYNC VIDEO INPUT (PINS 17 AND 20)						
$V_{17,20}$	sync pulse voltage amplitude	note 2	50	300	–	mV
SL	slicing level	note 14	–	50	–	%
VERTICAL SYNC						
t_W	width of the vertical sync pulse without sync instability	note 15	22	–	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency		–	15625	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8 V ±10%; note 6	–	0.2	0.5	%
Δf_{osc}	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	–	80	Hz
$\Delta f_{osc(max)}$	maximum frequency deviation at the start of the horizontal output	no calibration	–	–	75	%
HORIZONTAL PLL; note 16 (FILTER CONNECTED TO PIN 37)						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL	note 6	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		14	20	26	dB
HYS	hysteresis at the switching point		1	3	6	dB
HORIZONTAL OUTPUT (PIN 39)						
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
I_{sink}	sink current		–	–	2	mA
I_{source}	source current		–	–	2	mA
t_W	pulse width		–	5.4	–	µs
t_d	delay between the positive edge of the horizontal output pulse and the start of the horizontal sync pulse at the input		–	0	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL OUTPUT; note 17 (PIN 36)						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	lines
	locking range		488	–	722	lines/ frame
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
I_{sink}	sink current		–	–	2	mA
I_{source}	source current		–	–	2	mA
t_W	pulse width		–	380	–	µs
t_d	delay between the start of the vertical sync pulse at the input and the positive edge of the output pulse		–	37.5	–	µs
SANDCASTLE PULSE OUTPUT; note18 (PIN 40)						
V_O	output voltage during scan	I_O = 1 mA; note 30	–	–	0.9	V
V_O	output voltage during burst key	I_O = 1 mA; note 30	4.1	–	5.2	V
Z_O	output impedance during blanking		1.0	–	–	MΩ
t_W	pulse width					
	burst key		3.3	3.5	3.7	µs
	line blanking		8.4	8.7	9.0	µs
	vertical blanking		–	14	–	lines
t_d	delay of start of burst key to start of sync		5.2	5.4	5.6	µs
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 19	26	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		–38	–41	–44	dB
HYS_{off}	hysteresis colour killer OFF	note 6				
	strong input signal	S/N ≥ 40 dB	0	+3	+6	dB
	noisy input signal		0	+1	+8	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REFERENCE PART						
Phase-locked loop; note 20						
f_{CR}	catching range		300	500	–	Hz
$\Delta\varphi$	phase shift for a ±300 Hz deviation of the oscillator frequency	note 6	–	–	2	deg
Oscillator						
TC_{osc}	temperature coefficient of f_{osc}	note 6	–	2.0	2.5	Hz/K
Δf_{osc}	f_{osc} deviation with respect to V_P	note 6; V_P = 8 V ±10%	–	–	250	Hz
R_I	input resistance (pins 43 to 45)	f_i = 3.58 MHz; note 2	–	1.5	–	kΩ
R_I	input resistance (pin 42)	f_i = 4.43 MHz; note 2	–	1	–	kΩ
C_I	input capacitance (pins 42 to 45)	note 2	–	–	10	pF
R	required resistance to V_P for a crystal pin which is not used	note 21	7.8	8.2	8.6	kΩ
HUE CONTROL INPUT; note 22 (PIN 28)						
HUE_{cr}	HUE control range	see also Fig.3	±35	±40	–	deg
R_I	input resistance		45	–	–	kΩ
$V_{control}$	control voltage to switch the colour PLL in the free-running mode	note 20	V_P–1	–	–	V
DEMODULATOR OUTPUTS (PINS 50 AND 51)						
$V_{50(p-p)}$	(B–Y) output signal voltage amplitude (peak-to-peak value)	note 31	1.06	1.33	1.60	V
$V_{51(p-p)}$	(R–Y) output signal voltage amplitude (peak-to-peak value)	note 31	0.84	1.05	1.26	V
	spread of signal amplitude ratio PAL/NTSC	note 6	–1	–	+1	dB
Z_O	output impedance (R–Y)/(B–Y) output		–	–	500	Ω
B	bandwidth of demodulators	–3 dB; note 23	–	650	–	kHz
$V_{50(p-p)}$	(B–Y) residual carrier output voltage (peak-to-peak value)	$f = f_{osc}$	–	–	1	mV
		$f = 2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	(R–Y) residual carrier output voltage (peak-to-peak value)	$f = f_{osc}$	–	–	1	mV
		$f = 2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	H/2 ripple at (R–Y) output (peak-to-peak value)	only burst fed to input	–	–	25	mV
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature	note 6	–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage	note 6	–	–	±0.1	dB
I_{bias}	internal bias current of NPN emitter follower output transistor		0.16	0.20	–	mA
I_{source}	maximum source current		–	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATION ANGLE AND GAIN RATIO						
	demodulation angle		85	90	95	deg
G	gain ratio of both demodulators G(B–Y) to G(R–Y)		1.60	1.78	1.96	
REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 48)						
f_{ref}	reference frequency	note 24	–	4.43	–	MHz
$V_{48(p-p)}$	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_O	output voltage level	PAL/NTSC identified	1.5	1.6	1.7	V
V_O	output voltage level	no PAL/NTSC; SECAM (by TDA8395) identified	4.3	4.5	4.7	V
I_{48}	required current to force the decoder in SECAM mode		120	–	–	µA
STANDARD IDENTIFICATION AND FORCED SYSTEM SWITCHING; note 25 (PINS 4 AND 23 TO 27)						
$V_{I/O}$	input/output voltage					
	in "low" condition		–	–	1	V
	in "high" condition		4.0	–	5.3	V
$V_{I(max)}$	maximum input voltage	note 26	–	–	V_P	V
I_{load}	maximum load current (pins 23 to 26)		–	–	1	mA
I_I	input current (pins 23 to 26)					
	in "low" or "high" condition		–	–	1	µA
	when connected to V_P	note 26	–	–	10	µA
R_I	input resistance (pin 27)		80	–	–	kΩ
V_O	output voltage (pin 4)	notes 27 and 30				
	during PAL		–	–	0.9	V
	during SECAM		4.1	–	5.5	V
Z_O	output impedance pin 4 during NTSC	note 27	1	–	–	MΩ
I_{load}	maximum load current (pin 4)		–	–	0.5	mA
RGB switch						
RGB INPUTS (PINS 1 TO 3 AND 10 TO 12)						
$V_{i(p-p)}$	signal voltage amplitude (peak-to-peak value)		–	–	1.3	V
Z_I	input impedance		100	–	–	kΩ
V_{clamp}	active clamping voltage level		2.6	2.8	3.0	V
I_{LI}	input leakage current	note 6	–	–	3	µA
I_{clamp}	active clamping current		–200	–	+200	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING/SWITCH INPUTS; note 28 (PINS 13 AND 52)						
V_{IH}	HIGH level input voltage		0.9	–	3.0	V
V_{IL}	LOW level input voltage		0	–	0.5	V
I_I	input current		–	–0.2	–0.3	mA
t_d	delay between input and output pulse		–	–	50	ns
t_d	delay between switch input and RGB output		–	–	70	ns
V_{13}	input voltage on pin 13 to make RGB outputs and the fast blanking output high-ohmic		4	–	V_P	V
CLAMPING PULSE INPUT (PIN 14)						
V_{IH}	HIGH level input voltage		4.0	4.5	V_P	V
V_{IL}	LOW level input voltage		–	–	1	V
Z_I	input impedance		1	–	–	MΩ
RGB OUTPUTS (PINS 6 TO 8)						
G_v	voltage gain of the switches	f = 1 MHz	–0.5	0	+0.5	dB
G_{diff}	gain difference of the three channels		–	–	0.5	dB
Z_O	output impedance		–	–	150	Ω
$Z_{O(off)}$	output impedance in the "off" state	f = 10 MHz	100	–	–	kΩ
V_O	output voltage during blanking	open-circuit output	1.2	1.4	1.6	V
V_{os}	blanking off-set voltage of the two sources		–	–	5	mV
I_{bias}	internal bias current of NPN emitter follower output transistor		0.16	0.2	–	mA
$I_{source(max)}$	maximum source current		–	–	1	mA
ISS	input signal suppression when RGB outputs are high-ohmic	f = 5 MHz; note 6	60	–	–	dB
		f = 10 MHz; note 6	50	–	–	dB
		f = 22 MHz; note 6	40	–	–	dB
CT	crosstalk between the two RGB channels	f = 5 MHz; note 6	–60	–	–	dB
		f = 10 MHz; note 6	–50	–	–	dB
		f = 22 MHz; note 6	–40	–	–	dB
B	bandwidth of the RGB channels	C_L = 20 pF; note 6				
	gain reduction –0.5 dB		5	–	–	MHz
	gain reduction –1 dB		10	–	–	MHz
	gain reduction –3 dB		22	–	–	MHz
t_d	delay from RGB input to output	note 6	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING OUTPUT (PIN 5)						
V_{OH}	HIGH level output voltage		2	–	3	V
V_{OL}	LOW level output voltage		0	–	0.3	V
Z_O	output impedance		–	–	300	Ω
$Z_{O(off)}$	output impedance in the "off" state		100	–	–	kΩ
t_r	rise time of the output pulse		–	–	30	ns
t_f	fall time of the output pulse		–	–	30	ns
t_d	delay difference between fast blanking and RGB at the outputs		–	–	30	ns
I_{load}	maximum load current		–	–	1	mA

Notes

1. On set AGC.
2. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
3. Measured with 0 dB = 500 μV.
4. Measured at 10 mV RMS top sync input signal.
5. So called projected zero point, i.e. with switched demodulator.
6. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
7. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_O \text{ (black-to-white)}}{V_{m\,(rms)}\ (B = 5\ MHz)}$$

8. When the leakage current of the capacitor exceeds this value it will result in a reduced performance of the AGC (amplitude variation during line or frame up to 20% maximum) but it will not result in a hang-up situation.
9. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
10. Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
11. The IC has two 3-level switch control inputs for the selection of the video signal for the decoder and synchronization circuits. The video source for internal or external signal is selected via pin 32, also the polarity of the demodulation for the internal signal. When the video switch is in the external position the voltage level of pin 9 determines whether the video filters are switched to CVBS or Y/C. It is also possible via pin 9 to select an automatic detection of the Y/C signal.
12. This value is internally generated when the pin is left open-circuit (the minimum value of the series resistor is 25 kΩ).
13. The –3 dB bandwidth of the circuit can be calculated by means of the following equation:

$$f_{-3\ dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

14. Slicing level is independent of sync pulse amplitude.
15. The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization. The value given is the delay caused by the vertical sync pulse integrator. The integrator has been designed such that the vertical sync is not disturbed for special anti-copy tapes with vertical sync pulses with an on/off time of 10/22 μs.

16. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when excessive noise is present in the signal. This occurs when the internal video signal is selected or for an external CVBS signal when the chrominance input (pin 16) is left open-circuit. The time constant is always 'fast' when the chrominance input pin is connected to ground and the input is switched to the Y/C mode. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible.

    During weak signal conditions (noise detector active) the phase detector is gated and the width of the gate pulse has a value of 5.7 µs so that the effect of the noise is reduced to a minimum.

    The output current of the phase detector for the various conditions is shown in Table 1.

17. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 2 search modes of operation:

    a) The 'large window' mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz)

    b) The 'narrow window' mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

18. To obtain a simple interface between the TDA8310 and the PIP processor the sandcastle output has been designed such that the output is pulled down during scan and pulled up during the burst key pulse. During blanking the output is high-ohmic and therefore the output voltage is determined by the load.

19. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) as given in Characteristics first parameter of Section "Chrominance input (pin 16)" the dynamic range of the ACC is +6 and –20 dB.

20. All frequency variations are referenced to 3.58/4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9922 520. If the spurious response of the 4.43 MHz crystal is lower than –3 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequency is guaranteed. The spurious response of the 3.58 MHz crystal must be lower than –3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ. The catching and detuning range are measured for nominal crystal parameters. These are:

    a) load resonance frequency f_0 (C_L = 20 pF) = 4.433619 or 3.579545 MHz

    b) motional capacitance C_M = 20.6 fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal)

    c) parallel capacitance C_0 = 5.5 pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).

    The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.

    The free-running frequency of the oscillator can be checked by the HUE control pin to the positive supply rail. In that condition the colour killer is not active so that the frequency off-set is visible on the screen. When two or more crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator continuously switching between the various frequencies.

21. The crystal pins which are not used must be connected to the positive supply line via an 8.2 kΩ resistor. It is also possible to connect the non-used pins together and use a resistor with a value of 8.2 kΩ divided by the number of pins which are not used.

22. When this pin is left open-circuit the HUE control is set to the nominal value.

23. This value indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the demodulator low-pass filter is approximately 1 MHz.

24. The reference signal for the TDA8395 is available only when the crystal oscillator is operating at a frequency of 4.43 MHz. When a SECAM signal is identified this signal is only available during the vertical retrace period thus avoiding crosstalk with the incoming SECAM signal during scan.
25. The identified colour standard can be read from the IC in two ways:
    a) From the voltage level of pin 4. The voltage during the demodulation of the various standards is given in the last three parameters of this section.
    b) From the pins 23 to 26 when pin 27 is in the "read" mode.

    When pin 27 is in the "write" mode the colour decoder can be forced to one of the colour standards. The levels for the various standards are given in Tables 2, 3 and 4.
26. When one or more pins have to be connected to the positive supply line the **total** current must be limited to 40 μA. This can be achieved by connecting these pins together and connecting them to a positive supply line via a 100 kΩ resistor. When separate resistors are used a resistor with a higher value must be used so that the total current is limited to the required level.
27. The output of pin 4 is designed similar to the sandcastle output. The output is pulled down during PAL and pulled up during SECAM. During NTSC the pin is floating so that the output level is determined by the load.
28. The control possibilities of the RGB switch via pins 13 and 52 are shown in Table 5.
29. This output signal value is obtained when the CVBS or Y input signal at pins 17 and/or 20 has an amplitude of 0.7 V (black-to-white value).
30. The output buffer consists of a combination of a PMOS and an NMOS. The maximum output impedance in the low state can be calculated by dividing the maximum output voltage (for this parameter 0.9 V) by the specified current. For the high state this resistance can be calculated by dividing the difference between the maximum and minimum output voltage by the specified current. The output impedance is independent of the value of the output current.
31. These output signal values are obtained for a colour bar input signal with 75% saturation.

Table 1 Output current of phase detector

CURRENT PHASE DETECTOR DURING	SCAN (μA)	VERTICAL RETRACE (μA)	GATED YES/NO
Weak signal and synchronized	30	30	YES (5.7 μs)
Strong signal and synchronized	180	270	NO
Not synchronized	180	270	NO

Table 2 Read/write pin input (pin 27)

MODE	LEVEL
Decoder automatic	LOW
Forced decoder mode	HIGH

Table 3 Colour system logic (pins 25 and 26)

PIN 25	PIN 26	STANDARD
LOW	LOW	auto/no colour
LOW	HIGH	PAL
HIGH	LOW	NTSC
HIGH	HIGH	SECAM

Table 4 Crystal logic (pins 23 and 24)

PIN 23	PIN 24	SELECTED CRYSTAL (MHz)
LOW	LOW	4.43
LOW	HIGH	3.579 (NTSC)
HIGH	LOW	3.575 (PAL-M)
HIGH	HIGH	3.582 (PAL-N)

Table 5 Control logic RGB switch (pins 13 and 52)

PIN 13	PIN 52	RGB OUTPUT	FAST BLANKING OUTPUT
LOW	LOW	black	LOW
LOW	HIGH	RGB 2	HIGH
HIGH	LOW	RGB 1	HIGH
HIGH	HIGH	RGB 2	HIGH

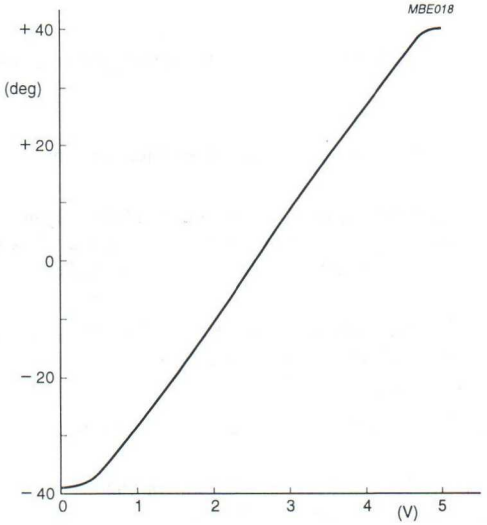


Fig.3 HUE control curve.

Integrated NTSC decoder and sync processor

TDA8315T

FEATURES

- CVBS or Y/C input
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Alignment-free NTSC colour decoder
- Horizontal PLL with an alignment-free horizontal oscillator
- Vertical count-down circuit
- Low dissipation (320 mW)
- Small amount of peripheral components compared with competition ICs.

GENERAL DESCRIPTION

The TDA8315T is an alignment-free NTSC decoder/sync processor. The device can be used for normal television applications and for Picture-in-Picture (PIP) applications.

The input signal can be either CVBS or Y/C and at the outputs the following signals are available:

Luminance signal

Colour difference signals (U and V)

Horizontal and vertical synchronization pulses

Back porch clamping pulse (burst-key pulse).

The supply voltage for the IC is 8 V. It is available in a 24-pin SO package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 11 and 12)	7.2	8.0	8.8	V
I_P	supply current	–	40	–	mA
Input voltages					
$V_{13(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	–	1	–	V
$V_{15(p-p)}$	chrominance input voltage (peak-to-peak value)	–	0.3	–	V
Output signals					
$V_{O(b-w)}$	luminance output voltage (blank-to-white value)	–	1.65	–	V
$V_{21(p-p)}$	–U output voltage (peak-to-peak value)	–	1.5	–	V
$V_{20(p-p)}$	–V output voltage (peak-to-peak value)	–	1.5	–	V
V_2	horizontal sync pulse	–	4	–	V
V_7	vertical sync pulse	–	4	–	V
V_{10}	back porch clamping pulse	–	4	–	V
Control voltages					
$V_{control}$	control voltages for Saturation and Hue	0	–	5	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8315T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

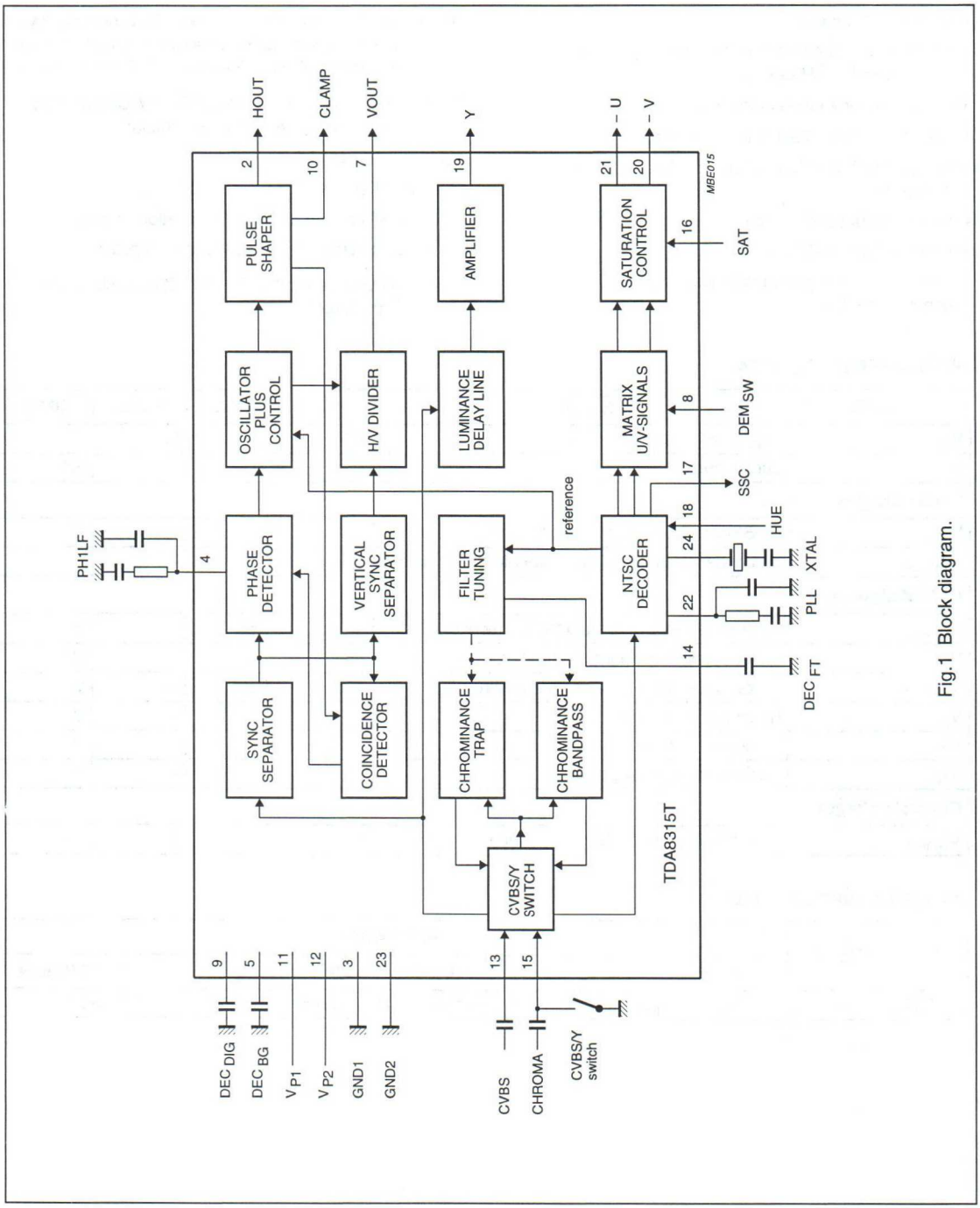


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TEST1[1]	1	test pin 1
HOUT	2	horizontal output pulse
GND1	3	ground 1 (0 V)
PH1LF	4	phase 1 loop filter
DEC_{BG}	5	bandgap decoupling
TEST2[1]	6	test pin 2
VOUT	7	vertical output pulse
DEM_{SW}	8	demodulation angle switch
DEC_{DIG}	9	decoupling digital supply
CLAMP	10	back porch clamping pulse
V_{P1}	11	supply voltage 1 (+8 V)
V_{P2}	12	supply voltage 2 (+8 V)
CVBS/Y	13	CVBS/Y input
DEC_{FT}	14	decoupling filter tuning
CHROMA	15	chrominance and switch input
SAT	16	saturation control input
SCS	17	sub-carrier signal output
HUE	18	hue control input
Y	19	Y output
–V	20	–V output
–U	21	–U output
PLL	22	PLL colour filter
GND2	23	ground 2 (0 V)
XTAL	24	3.58 MHz crystal connection

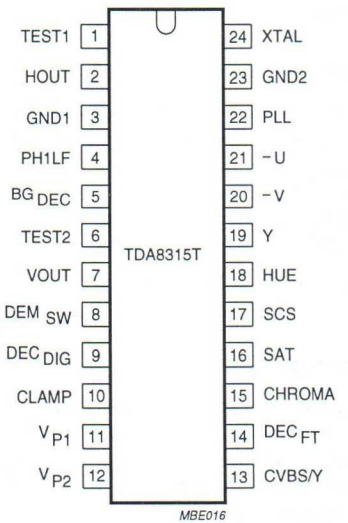


Fig.2 Pin configuration.

Note

1. In the application the test pins must be connected to ground.

FUNCTIONAL DESCRIPTION

CVBS or Y/C input

The TDA8315T has a video input which can be switched to CVBS (with internal chrominance bandpass and trap filters) and to Y/C (without chrominance bandpass and trap filters). The switching between CVBS and Y/C is achieved by the DC level of the CHROMA input (pin 15).

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by gyrator circuits that are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. The chrominance trap can be switched off by the DC level of the CHROMA input.

The luminance delay line is also realised by gyrator circuits.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The gain of the two colour difference signal demodulators is identical and the phase angle of the reference carrier signals is 90°. This phase shift is achieved internally. It is possible to switch the demodulator angle to 110° by an internal matrix circuit. The switching is obtained externally via pin 8.

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are then fed to the slicing stage (separator) which operates at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used to detect whether the line oscillator is synchronized. The PLL has a very high static steepness, this ensures that the phase of the picture is independent of the line frequency. The line oscillator operates at twice the line frequency.

The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC.
The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.

The horizontal output pulse is derived from the horizontal oscillator via a pulse shaper. The pulse width of the output pulse is 5.4 µs, the front edge of this pulse coincides with the front edge of the sync pulse at the input.

The vertical output pulse is generated by a count-down circuit. The pulse width is approximately 380 µs. Both the horizontal and vertical pulses will always be available at the outputs even when no input signal is available.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–	9.0	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C
T_{sld}	soldering temperature for 5 s	–	260	°C
T_j	maximum operating junction temperature	–	125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	≤65	K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pins 11 and 12)		7.2	8.0	8.8	V
I_P	supply current (pins 11 and 12)		–	40	–	mA
P_{tot}	total power dissipation		–	320	–	mW
CVBS or Y/C input						
CVBS/Y INPUT (PIN 13)						
$V_{13(p\text{-}p)}$	CVBS/Y input voltage (peak-to-peak value)	notes 1 and 2	–	1	1.4	V
I_{13}	CVBS/Y input current		–	4	–	µA
COMBINED CHROMINANCE AND SWITCH INPUT (PIN 15)						
$V_{15(p\text{-}p)}$	chrominance input voltage (peak-to-peak value)	notes 2 and 3	–	0.3	–	V
$V_{15(p\text{-}p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 2	1	–	–	V
R_I	chrominance input resistance		–	15	–	kΩ
C_I	chrominance input capacitance	note 4	–	–	5	pF
V_{15}	DC input voltage for Y/C operation		3	4	5	V
V_{15}	DC input voltage for CVBS operation		–	–	1	V
Chrominance filters and luminance delay line						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	3.58	–	MHz
B	luminance signal bandwidth	note 2	–	2.7	–	MHz
SR	colour subcarrier rejection		20	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE BANDPASS CIRCUIT						
f_c	centre frequency		–	3.58	–	MHz
QBP	bandpass quality factor		–	3	–	
Y DELAY LINE						
t_d	delay time	note 2	–	390	–	ns
B	bandwidth of internal delay line	note 2	8	–	–	MHz
Y OUTPUT SIGNAL (PIN19)						
$V_{19(p-p)}$	output signal amplitude (peak-to-peak value)	note 1	–	2.27	–	V
Z_O	output impedance		–	350	–	Ω
V_{19}	top sync level		–	2.85	–	V
S/N	signal-to-noise ratio	notes 2 and 5	–	56	–	dB
Colour decoder						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 6	24	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		tbf	–31	tbf	dB
HYS_{off}	hysteresis colour killer OFF	note 2				
	strong input signal	S/N ≥ 40 dB	–	+3	–	dB
	noisy input signal		–	+1	–	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	
REFERENCE PART						
Phase-locked loop; note 7 (filter connected to pin 22)						
f_{CR}	catching range		300	500	–	Hz
Δφ	phase shift for a ±400 Hz deviation of the oscillator frequency	note 7	–	–	2	deg
Oscillator (pin 24)						
TC_{osc}	temperature coefficient of f_{osc}	note 2	–	2.0	2.5	Hz/K
Δf_{osc}	f_{osc} deviation with respect to V_P	note 2; V_P = 8 V±10%	–	–	250	Hz
R_I	input resistance	note 4	–	1.5	–	kΩ
C_I	input capacitance	note 4	–	–	10	pF
HUE CONTROL INPUT (PIN 18)						
HUE_{cr}	hue control range	see also Fig.3	±35	±45	–	deg
SATURATION CONTROL INPUT (PIN 16)						
SAT_{cr}	saturation control range	see also Fig.4	52	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATOR OUTPUTS (PINS 20 AND 21)						
B	bandwidth of demodulators	–3 dB; note 8	–	650	–	kHz
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature	note 2	–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage	note 2	–	–	±0.1	dB
G	gain ratio of demodulator G(–U)/G(–V)		0.9	1.0	1.1	
	demodulator angle pin 8 LOW pin 8 HIGH		 85 105	 90 110	 95 115	 deg deg
$V_{21(p-p)}$	–U output signal amplitude at nominal saturation (peak-to-peak value)	note 9	–	1.5	–	V
$V_{20(p-p)}$	–V output signal amplitude at nominal saturation (peak-to-peak value)	note 9	–	1.5	–	V
Z_O	output impedance (–U)/(–V) output		–	–	500	Ω
V_O	DC output voltage		–	3	–	V
DEMODULATION ANGLE SWITCH INPUT (PIN 8)						
V_8	input voltage for 90° angle		–	–	1	V
V_8	input voltage for 110° angle		$V_P - 1$	–	–	V
SUBCARRIER OUTPUT SIGNAL (PIN 17)						
$V_{17(p-p)}$	output signal amplitude (peak-to-peak value)		–	300	–	mV
Z_O	output impedance		–	250	–	Ω
V_O	DC output voltage		–	1.6	–	V
Horizontal and vertical synchronization circuits						
SYNC VIDEO INPUT (PIN 13)						
V_{13}	sync pulse amplitude	note 4	50	300	–	mV
SL	slicing level	note 10	–	50	–	%
VERTICAL SYNC						
t_W	width of the vertical sync pulse without sync instability	note 11	22	–	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free-running frequency		–	15734	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8 V±10%; note 2	–	0.2	0.5	%
$\Delta f_{osc}/\Delta T$	frequency variation with temperature	note 2	–	–	tbf	Hz/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL PLL; NOTE 12 (FILTER CONNECTED TO PIN 4)						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL	note 2	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
HYS	hysteresis at the switching point		–	3	–	dB
HORIZONTAL OUTPUT (PIN 2)						
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
$I_{O(sink)}$	output sink current		–	–	2	mA
$I_{O(source)}$	output source current		–	–	2	mA
t_W	pulse width	note 13	–	5.4	–	µs
t_d	delay time between positive edge of the horizontal output pulse and start of the horizontal sync pulse at the input		–	0	–	µs
BACK PORCH CLAMPING OUTPUT (PIN 10)						
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
$I_{O(sink)}$	output sink current		–	–	2	mA
$I_{O(source)}$	output source current		–	–	2	mA
t_W	pulse width		3.2	3.4	3.6	µs
t_d	delay time between start of clamping pulse and start of the start sync pulse		5.2	5.4	5.6	µs
VERTICAL OUTPUT (PIN 7); NOTE 14						
f_{fr}	free-running frequency		–	60	–	Hz
f_{lock}	locking range		54.6	–	64.5	Hz
	divider value not locked		–	525	–	
	locking range (lines/frame)		488	–	576	
V_{OH}	HIGH level output voltage	I_O = 2 mA	2.4	4.0	–	V
V_{OL}	LOW level output voltage	I_O = 2 mA	–	0.3	0.6	V
$I_{O(sink)}$	output sink current		–	–	2	mA
$I_{O(source)}$	output source current		–	–	2	mA
t_W	pulse width (6 line periods)		–	380	–	µs
t_d	delay time between start of the vertical sync pulse at the input and the positive edge of the output pulse		–	37.5	–	µs

Notes to the characteristics

1. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
2. This parameter is not tested during production and is guaranteed by the design and qualified by matrix batches which are made in the pilot production period.
3. Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
4. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
5. The signal-to-noise ratio is specified as a peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
6. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and −18 dB.
7. All frequency variations are referenced to 3.58 MHz carrier frequency.
   All oscillator specifications are measured with the Philips crystal series 9922 520.
   If the spurious response of the crystal is lower than −3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ, oscillation at the fundamental frequency is guaranteed.

   The catching and detuning range are measured for nominal crystal parameters. These are:

   a) load resonance frequency f_0 (C_L = 20 pF) = 3.579545 MHz

   b) motional capacitance C_M = 14.5 fF

   c) parallel capacitance C_0 = 4.5 pF.

   The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.
   The free-running frequency of the oscillator can be checked by pulling the saturation control pin to the positive supply rail. In that condition the colour killer is not active so that the frequency offset is visible on the screen.
8. This value indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the demodulator low-pass filter is approximately 1 MHz.
9. Output signal amplitude for a standard colour bar signal with 75% saturation and a demodulation angle of 90°. For a demodulation angle of 110° the −V signal amplitude will decrease to 1.2 V (p-p) and the −U signal amplitude remains unchanged. The nominal saturation is specified as maximum −6 dB.
10. Slicing level independent of sync pulse amplitude. The slicing level of the vertical sync separator is 70% (slicing level in direction of black level) during strong signal reception (no noise detected in the incoming signal) and 30% during weak signal reception.
11. The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization. The value given is the delay caused by the vertical sync pulse integrator. The integrator has been designed such that the vertical sync is not disturbed for special anti-copy tapes with vertical sync pulses with an on/off time of 10/22 µs.
12. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when excessive noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible.

    To prevent the horizontal synchronization being disturbed by anti-copy guard signals such as Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The width of the gate pulse is approximately 12 µs. during weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 µs so that the effect of the noise is reduced to a minimum.

    The output current of the phase detector in the two modes is shown in Table 1.

13. The horizontal output pulses are obtained from the horizontal oscillator by a pulse shaper. The width of the output pulse is approximately 5.4 μs and the rising edge of the pulse symmetrically coincides with the start of the sync pulse at the input.
14. The vertical output pulses are generated by a divider circuit. The vertical output pulse has a delay of 37.5 μs with respect to the start of the vertical sync pulse at the input. This is caused by the clock frequency of the divider being twice the horizontal frequency.

    This divider circuit has 2 modes of operation:

    Search mode (large window).

    This mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame outside the range is between 261 and 264). In the search mode the divider can be triggered between line 244 and line 288 (approximately 54 to 64.5 Hz).

    Standard mode (narrow window).

    This mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the output pulse is generated at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window. When no input signal is available the divider generates output pulses with a timing of 262.5 lines (standard 60 Hz signal).

Table 1 Output current of phase detector.

CURRENT PHASE DETECTOR DURING	SCAN (μA)	VERTICAL RETRACE (μA)	GATED YES/NO
Weak signal and synchronized	30	30	YES (5.7 μs)
Strong signal and synchronized	180	270	YES (12 μs)[1]
Not synchronized	180	270	NO

Note

1. Vertical retrace.

QUALITY SPECIFICATION

Quality level in accordance with SNW-FQ-611-part E.

SYMBOL	PARAMETER	RANGE A[2]	RANGE B[3]	UNIT
ESD	protection circuit specification (note 1)	>2000	>200	V
		100	200	pF
		1500	0	Ω

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Range A is for Human body model.
3. Range B is for machine model.

Latch up

All pins meet the specification:

$I_{trigger} \geq 100$ mA or $\geq 1.5\ V_{DDmax}$

$I_{trigger} \leq -100$ mA or $\leq -0.5\ V_{DDmax}$.

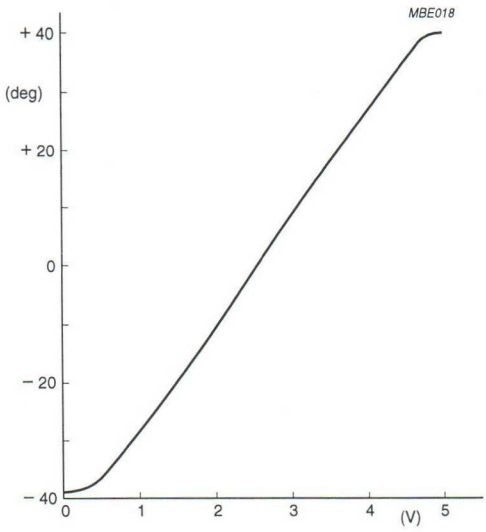


Fig.3 Hue control curve

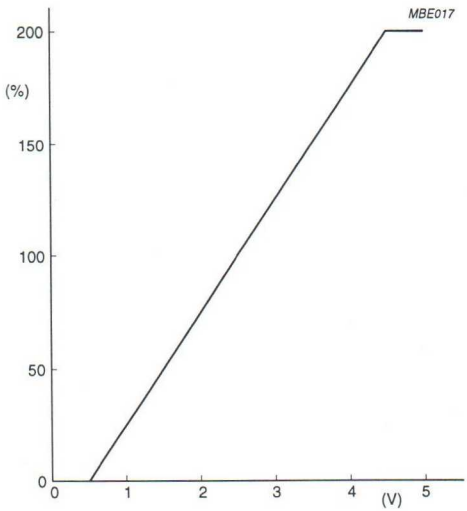


Fig.4 Saturation control curve.

TELEVISION IF AMPLIFIER AND DEMODULATOR

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11\text{-}13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1\text{-}16(rms)}$	20	40	80	μV
IF gain control range		G_V	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12\text{-}13(p\text{-}p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38).

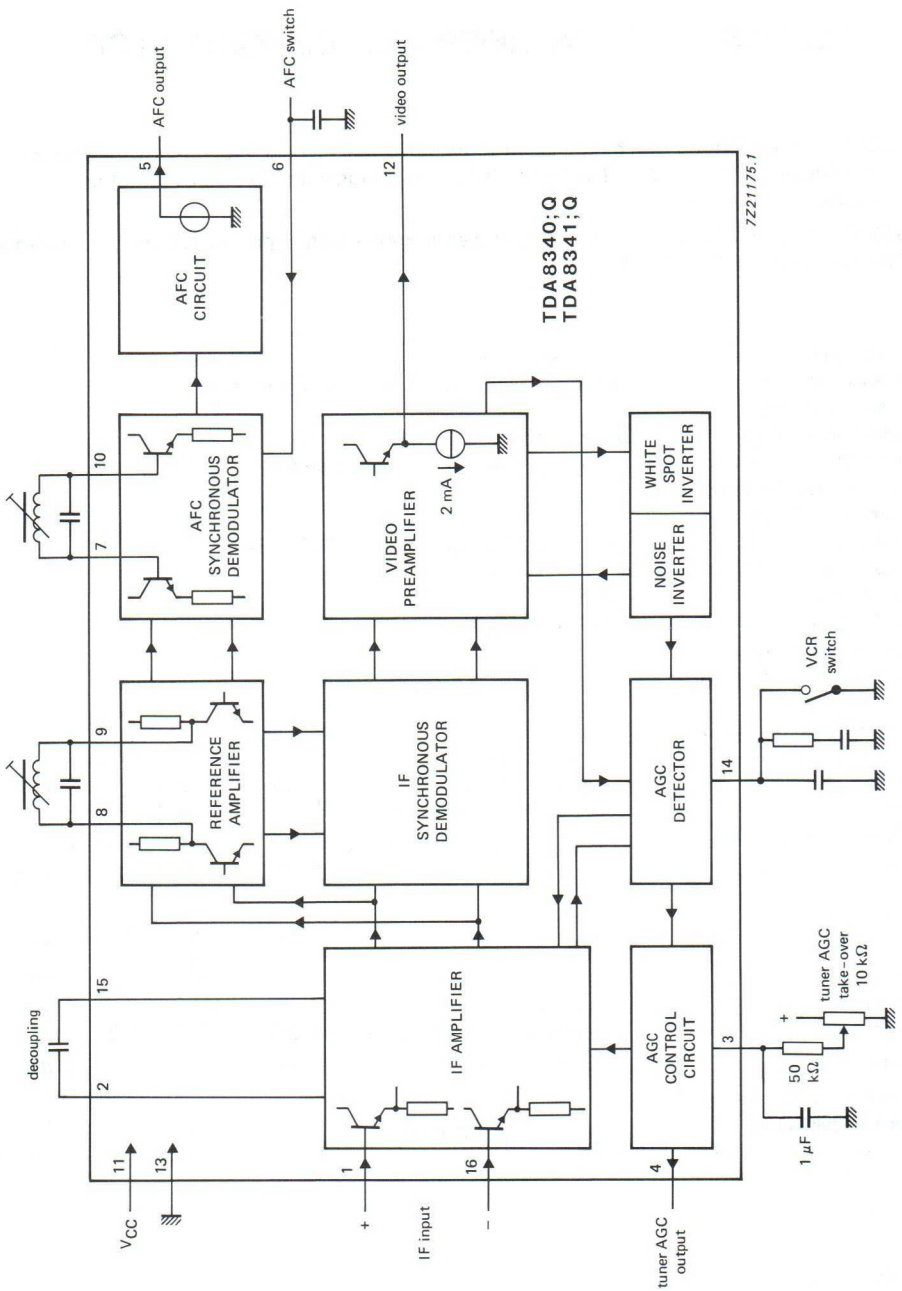


Fig. 1 Block diagram.

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier $\pi/2$ rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwith of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 μH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC dectector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No 'hang-up' occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

FUNCTIONAL DESCRIPTION (continued)

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 11)	$V_{CC} = V_{11-13}$	9,4	13,2	V
IF AGC voltage/VCR switch	V_{14-13}	–	13,2	V
Tuner AGC voltage	V_{4-13}	–	12	V
AFC switch voltage	V_{6-13}	–	13,2	V
Maximum voltage level with VCR switch active	V_{12-13}	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature	T_{amb}	–25	+70	°C

CHARACTERISTICS

Measured in circuit of Fig. 3; V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	μV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point	R_{3-11} = 39 kΩ	V_{1-16}	–	–	3	mV
(note 3)	R_{3-13} = 39 kΩ	V_{1-16}	70	–	–	mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; I_4 = 1 to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	I_4 = 7 mA	V_{4-13}	–	200	300	mV
Leakage current	V_4 = 12 V	I_4	–	–	1	μA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwith of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Video output (continued)						
Residual 2nd harmonic of carrier signal (r.m.s. value)	note 8	$V_{12\text{-}13(rms}$	–	2	10	mV
Variation of video voltage for ΔV_{CC} = 1 V		$\frac{\Delta V_{12\text{-}13(p\text{-}p)}}{\Delta V_{11\text{-}13}}$	0,1	0,2	0,3	
Intermodulation	notes 8 and 9;					
	1,1 MHz, blue	α	–	–65	–60	dB
	1,1 MHz, yellow	α	–	–60	–56	dB
	3,3 MHz	α	–	–	–68	dB
Signal-to-noise ratio	note 10;					
	V_i = 10 mV	S/(S+N)	50	58	–	dB
	max. gain	S/(S+N)	54	61	–	dB
Spot inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	6,3	6,8	7,3	V
Insertion level		$V_{12\text{-}13}$	4,2	4,5	4,8	V
Noise inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	1,6	1,8	2,0	V
Insertion level		$V_{12\text{-}13}$	3,5	3,8	4,1	V
VCR switch						
Level below which video output switches off		$V_{14\text{-}13}$	1,8	2,2	2,6	V
Switch current	$V_{12\text{-}13}$ = 0,7 V	$-I_{14}$	40	60	100	μA
AFC circuit (note 12)						
Output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V
Change of frequency for an AFC output voltage swing of 10 V		Δf	–	60	120	kHz
AFC output voltage	at f = 38,9 MHz	$V_{5\text{-}13}$	–	6	–	V
	no input signal	$V_{5\text{-}13}$	2	6	10	V
	during AFC off	$V_{5\text{-}13}$	5	6	7	V
AFC output resistance		$R_{5\text{-}13}$	–	500	–	Ω
AFC switch: level below which AFC output switches off		$V_{6\text{-}13}$	1,4	2,0	2,8	V
AFC switch current	during AFC on	I_6	–	200	500	μA
Max. AFC switch current	during AFC off;					
	$V_{6\text{-}13}$ = 0 V	I_6	–	–	5	mA

Notes to the characteristics

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Tuner AGC starting point is defined as 'level of input signal when tuner AGC current = 1 mA'.
4. Measured with pin 3 connected via 39 kΩ resistor to V_{CC} (pin 11), with an r.m.s. voltage of 10 mV top sync input signal and with pin 12 not loaded.
5. At the 'projected zero point', e.g. with switched demodulator.
6. Measured in the circuit of Fig. 7:

   the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level;

   the differential phase is defined as 'the difference (in degrees) between the largest and smallest phase angles'.
7. Measured according to the test line shown in Fig. 9:

   the non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step;

   the mean step is (white level − black level) divided by the number of steps.
8. Measured up to 45 dB gain control.
9. Test set-up and input conditions for intermodulation measurements as in Figs 6 and 7.
10. Measured with a 75 Ω source:

    $$S/(S+N) = 20 \log \frac{V_{\text{out black to white}}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$
11. Video output waveform showing white spot and noise inverter threshold levels.
12. Measured with input signal $V_{1\text{-}16}$ = 10 mV and with no load at AFC output.

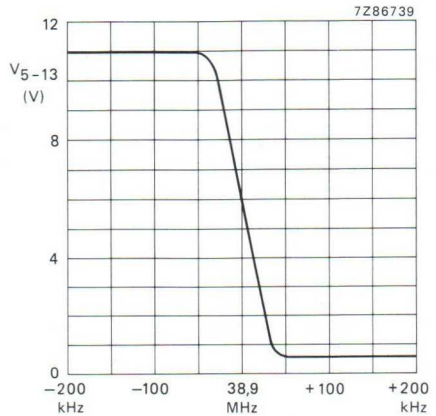


Fig. 2 AFC output voltage as a function of frequency.

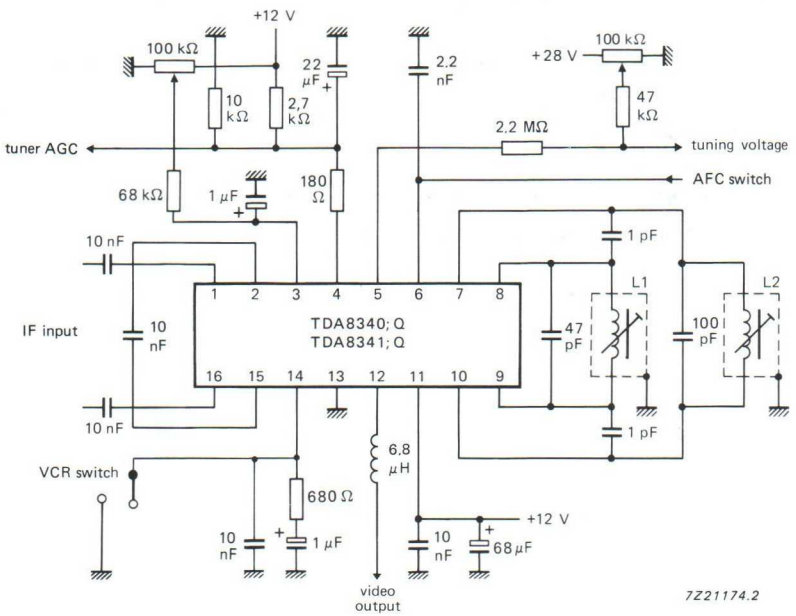


Fig. 3 Typical application circuit diagram;
Q of L1 and L2 = 80; f_o = 38,9 MHz.

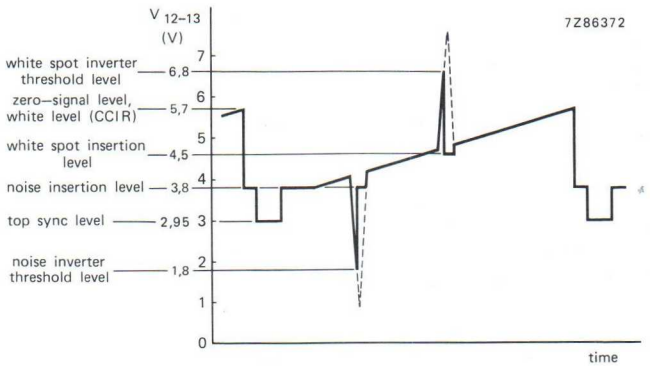


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

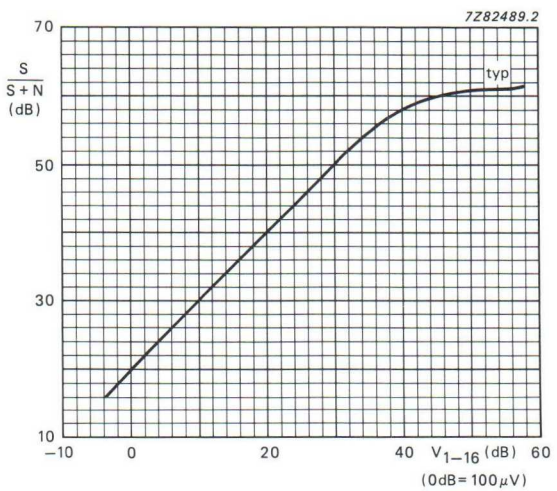
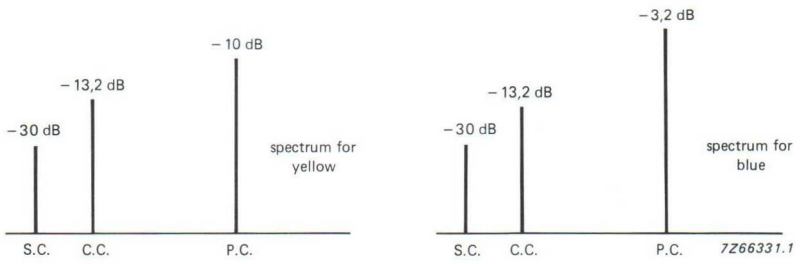


Fig. 5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

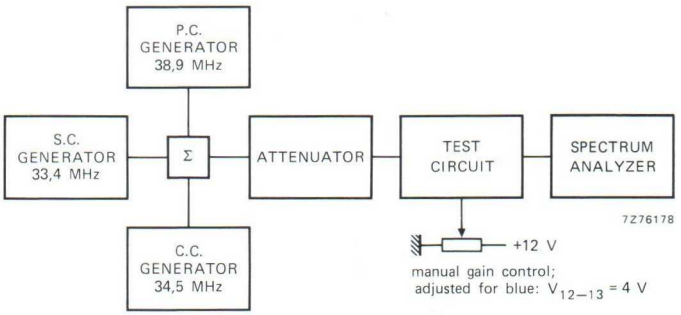


Fig. 7 Test set-up for intermodulation measurements.

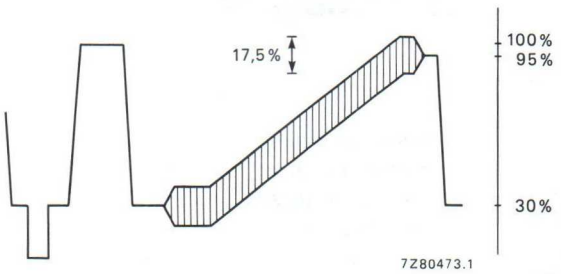


Fig. 8 Video output signal.

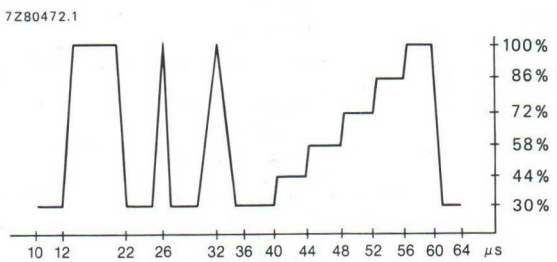


Fig. 9 E.B.U. test signal waveform (line 330).

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA8349A

Multistandard IF amplifier and demodulator

GENERAL DESCRIPTION

The TDA8349A is a multistandard IF amplifier and demodulator with AGC and AFC functions for television receivers. The device has a video recognition circuit and a video switch for internal or external video for full SCART applications.

FEATURES

- Full range gain-controlled wide-band IF amplifier up to 60 MHz
- Wide-band video amplifier with good linearity and a class AB output stage to ensure a very low output impedance
- Supply independent video output level
- Small second harmonic IF output
- AGC circuit which operates on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC) with reduced sensitivity for high sound carriers
- AFC circuit with an internal 90° phase shift circuit, a sample-and-hold circuit for negatively modulated signals to reduce video dependent AFC information and an analog or digital output
- Video recognition possibility based on horizontal pulse duty cycles
- Video switch for selection of internal or external video signals
- Wide supply voltage range and ripple rejection
- Requires few external components
- Tuner AGC output for npn and pnp tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current (pin 14)	V_i = 10 mV	40	55	65	mA
$V_{1-2(RMS)}$	IF input sensitivity (RMS value)		-	50	80	μV
G_v	IF gain control range		66	72	-	dB
$V_{11-17(p-p)}$	video output voltage (peak-to-peak value)		1.7	1.9	2.1	V
S/N	signal-to-noise ratio	V_i = 10 mV	54	61	-	dB
$V_{8-17(p-p)}$	AFC output voltage swing (peak-to-peak value)		10	-	11	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8349A	20	DIL	plastic	SOT146

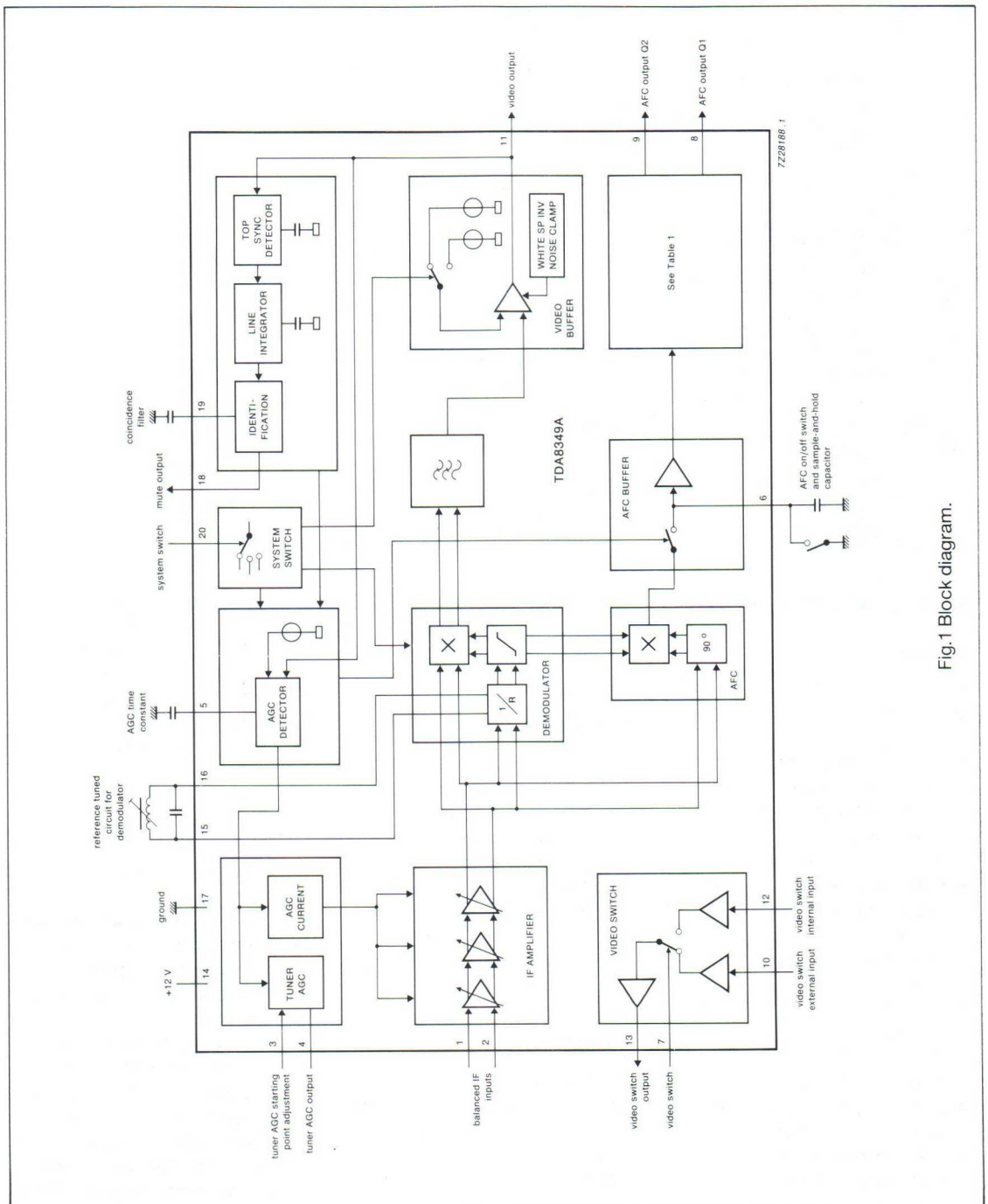


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1,2	balanced IF inputs
3	tuner AGC starting point adjustment
4	tuner AGC output
5	AGC time constant
6	AFC on/off switch and sample-and-hold capacitor
7	video switch
8	AFC output Q1
9	AFC output Q2
10	video switch external input
11	video output
12	video switch internal input
13	video switch output
14	positive supply voltage
15,16	reference tuned circuit for demodulator
17	ground
18	mute output
19	coincidence filter
20	system switch

FUNCTIONAL DESCRIPTION

General

The IC consists of the following parts as illustrated in Fig.1:

- Gain controlled video IF amplifier
- Quasi-synchronous demodulator
- Video amplifier/buffer with white spot clamp/inverter and noise clamp
- AGC circuit which operates either on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC)
- AFC circuit with sample-and-hold circuit for negatively modulated signals, on/off switch and a digital or analog output (switchable)
- Circuit for switching between positive and negative modulation
- Video recognition circuit for sound muting and tuning indication
- Video switch which facilitates selection between two different video signals, with different gain settings

IF amplifier

The IF amplifier consists of three AC coupled differential gain stages with adjustable feedback in the emitter. The AC coupling allows simple biasing, cascades can be used and no DC feedback is required. This provides a control range above 70 dB with good linearity. The minimum input signal to obtain the nominal output amplitude is 50 μV RMS.

Demodulator

The demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and a tuned circuit for selectivity. The regenerated carrier signal is limited by a clamping circuit before it is fed to the demodulator. Switching between positive and negative modulation is achieved by the system switch which provides currents to the demodulator in a positive or negative direction.

Video amplifier

The video amplifier based on the feedback principle improves the linearity of the video output buffer. It has an internal bandgap reference to ensure a stable video output at different supply voltages and temperatures. This bandgap also reduces the supply ripple on the video output to values less than −30 dB. The video amplifier has a typical bandwidth of 10 MHz which allows application for all new video standards with bandwidths of up to 10 to 12 MHz. The video output signal has an amplitude of 2 V (p-p).

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers. A switchable DC shift for positively modulated IF signals ensures correct signal handling. This switching is obtained via pin 20, which is the same pin used for switching the demodulation polarity in the demodulator.

The circuit also has a noise clamp which prevents the video output becoming less than ±400 mV below the top sync level at noise peaks.

The output buffer of the video amplifier consists of a class A/B circuit which can handle large source as well as large sink currents. This makes the circuit more flexible in several applications with one or more ceramic filters connected to this output buffer.

AGC control circuit

This converts the AGC detector voltage (pin 5) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted by a voltage between 3 and 5 V for pnp tuners and between 7 and 9 V for npn tuners via pin 3.

AGC circuit

A new AGC system has been designed for the AGC. It will be a top sync-detector for negatively modulated signals and a top white level AGC for positively modulated signals.

For optimal flexibility reasons the load and unload currents of the AGC are chosen such that both, a relatively fast set, as well as a set with a low tilt are possible for positive (L) and negative (B/G) modulated signals. For this reason a tilt ratio between positive (L) and negative (B/G) of approximately 3:1 has been chosen. This means that in a fast set the choice of a typical tilt for negatively modulated signals of 2% will obtain a typical tilt for positively modulated signals (L) of 6%. For a digital set which requires a small tilt the choice of tilt can be a factor of 5 or 10 smaller by increasing the AGC capacitor.

The chosen AGC currents:

MODE	UNLOAD CURRENT	LOAD CURRENT	TILT AT 2.2 μF
B/G	50 μA	1.5 mA	typ. 0.5% (line tilt)
L	500 nA*	1.5 mA	typ. 1.5% (field tilt)
MAC(positive)	200 nA	1.5 mA	typ. 1.2% (frame tilt)
MAC(negative)	500 nA	1.5 mA	typ. 1.5% (field tilt)

Switching between the first three modes can be achieved by the system switch. This is a 3-level switch which when grounded selects B/G; open or 5 V selects L, and with pin 20 connected to V_{CC} selects positively modulated MAC. The IC operates in a fourth mode if the identification capacitor at pin 19 is connected to V_{CC}, it can be used for negatively modulated MAC.

During channel switching a situation can occur that requires the AGC to increase the gain more than for example 50 dB. If this increase of gain has to be done for a positively modulated (L) signal, it will be achieved by the 500 nA load current and is therefore extremely slow. Because the identification information can be used to indicate that the signal is too small, in this event the identification circuit will mute, it is possible to increase the positive unload current to the same value as that used for negatively modulated signals. This switching is fully automatic and cannot be switched off.

AFC circuit

The AFC circuit consists of a demodulator stage which is fed with signals 90°out of phase. A very accurate internally realized 90° phase shift circuit makes it possible to use the demodulator IF regenerator tuned circuit for tuning the AFC circuit. To prevent video ripple on the AFC output voltage a sample-and-hold circuit is used for negatively modulated signals. The output signal of the demodulator is sampled during

* As long as no signal has been identified by the identification detector the unload current will be 50 μA.

sync level of the video signal and will be stored with the aid of an external capacitor. This sample-and-hold circuit is not used in the L mode, but it will function as a low-pass filter in this mode and therefore also reduces the video dependency of the AFC. A gain stage amplifies the voltage swing by 5 times. The output of the AFC circuit will be an inverse analog output on pin 8 when pin 9 is connected to a voltage above 8 V. If pin 9 is connected to a voltage above 10 V the output will be a normal analog output. Normally pins 8 and 9 together provide digital AFC information.

Video recognition circuit

For full scart functions it is necessary to implement a second mute function for non-video signals in the whole television concept. This is realized in this IF-IC. With an internal sync separator and an internal integrator it is possible to achieve a very sensitive identification circuit, which measures the mean frequency of the input signal. This is normally approximately 16 kHz. The integrator capacitor will be loaded during the whole line time and unloaded during the sync pulse. The maximum voltage at this internal capacitor is a value for the main frequency of the video signal. By changing the value of an external capacitor it is possible to influence the speed and sensitivity of the recognition circuit. It is possible to gain sensitivity performance at disturbed signals by increasing the value of the external capacitor, however this will reduce the speed of the identification circuit.

Video switch circuit

The video switch also provides application for full SCART functions. The circuit has two inputs, one output and a control pin. The switch selects either internal or external video signals. A x 2 gain stage for the external input provides an equal output level for internal or external video from the SCART. The crosstalk of the unwanted signal is better than –50 dB and the total signal handling meets all the requirements for SCART specifications.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)	–0.5	13.2	V
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+ 75	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; carrier frequency 38.9 MHz; negative modulation; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
supply						
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current	V_i = 10 mV	40	55	65	mA
IF amplifier (note 1)						
V_{1-2}	input sensitivity	note 2	-	50	80	μV
R_{1-2}	differential input resistance	note 3	-	2	-	kΩ
C_{1-2}	differential input capacitance	note 3	-	2	-	pF
ΔG_{1-2}	gain control range		66	72	-	dB
ΔV_{11}	output signal for 50 dB input signal variation	note 4	-	0.5	-	dB
V_{1-2}	maximum input signal		100	-	-	mV
f_{1-2}	maximum operating frequency		60	-	-	MHz
Video output (note 5)						
	zero signal output level	note 6				
V_{11}	negative modulation		-	4.75	-	V
V_{11}	positive modulation		-	2.65	-	V
V_{11}	top sync level (top sync AGC)	note 7	-	2.7	-	V
V_{11}	white level (white level AGC)	note 8	-	4.6	-	V
$V_{11(p-p)}$	amplitude of video output signal (peak-to-peak value)		1.7	1.9	2.1	V
V_{11}	amplitude difference (positive/negative)		-	0	10	%
V_{11}	video output voltage variation	ΔV_P = 1 V	-	–30	-	dB
V_{11}	white spot threshold level	see Fig.3	-	5.6	-	V
V_{11}	white spot insertion level	see Fig.3	-	3.8	-	V
V_{11}	noise clamping level	see Fig.3	-	2.3	-	V
Z_{11}	output impedance		-	-	10	Ω
I_{11}	maximum sink current		5	-	10	mA
I_{11}	maximum source current		5	-	10	mA
B_{11}	bandwidth of demodulated output signal		7.5	10.0	-	MHz
G_d	differential gain	note 9	-	2	-	%
φ_d	differential phase	note 9	-	7	-	deg
Y_{nl}	luminance non-linearity	note 10	-	2	5	%
	intermodulation	see Figs 6 and 7				
α	1.1 MHz blue		-	–66	-	dB
α	1.1 MHz yellow		-	–60	-	dB
α	3.3 MHz blue		-	–60	-	dB
α	3.3 MHz yellow		-	–60	-	dB
	signal-to-noise ratio	note 11				
S/N		V_i = 10 mV	54	61	-	dB
S/N		minimum gain	60	66	-	dB
$V_{1(rms)}$	residual carrier signal (RMS value)		-	10	20	mV
$V_{11(rms)}$	residual 2nd harmonic of carrier signal (RMS value)		-	3	10	mV
System switch (note 12)						
V_{20}	maximum voltage for mode B/G		1.4	-	-	V
I_{20}	input current	V_{20} = 0 V	-	–300	-	μA
V_{20}	minimum voltage for mode L		-	-	3	V
V_{20}	maximum voltage for mode L		7	-	-	V
I_{20}	input current	3 V ≤ pin 20 ≤ 7 V	–150	-	250	μA
V_{20}	minimum voltage for MAC (positive)		-	-	9.5	V
I_{20}	input current	V_{20} = V_P	-	500	-	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC control circuit						
t_{11}	response to an amplitude increase of 52 dB of the IF input with the AGC switched to mode B/G	note 13	-	2	-	ms
t_{11}	response to an amplitude decrease of 52 dB of the IF input with the AGC switched to mode B/G	note 14	-	25	-	ms
	allowed leakage current of the AGC capacitor					
I_5	top sync level AGC		-	10	-	μA
I_5	white level AGC		-	200	-	nA
I_5	positive MAC AGC		-	50	-	nA
I_5	negative MAC AGC		-	200	-	nA
Tuner AGC (note 15)						
	input voltage for tuner AGC starting point					
V_3	IF input = 200 μV; negative slope		3.0	3.5	-	V
V_3	IF input = 100 mV; negative slope		-	5.0	5.5	V
V_3	IF input = 200 μV; positive slope		7.0	7.5	-	V
V_3	IF input = 100 mV; positive slope		-	9.0	9.5	V
I_4	maximum current swing of tuner AGC output		3	5	-	mA
V_4	output saturation voltage	I_4 = 2 mA	-	-	300	mV
I_4	leakage current		-	-	1	μA
ΔV_i	input signal variation complete tuner control		0.5	2.0	4.0	dB
V_3	minimum tuner take over voltage		-	-	1	V
Video switching circuit						
EXTERNAL VIDEO INPUT (AC coupled)						
$V_{10(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	1.0	-	V
I_{10}	input current		-	3.5	-	μA
V_{10}	top sync clamping level	I_{10} = 1 mA	-	3.3	-	V
INTERNAL VIDEO INPUT (DC coupled)						
$V_{12(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	2.0	-	V
$\lvert Z_{12} \rvert$	input impedance		-	2.0	-	kΩ
V_{12}	black level input voltage		-	3.3	-	V
VIDEO OUTPUT						
$V_{13(p-p)}$	output signal voltage (peak-to-peak value)		-	2.0	-	V
V_{13}	top sync level		-	2.7	-	V
V_{13}	noise clamping voltage level	I_{13} = 1 mA	-	2.5	-	V
I_{13}	internal bias current of npn emitter follower output transistor		-	1.5	-	mA
I_{13}	maximum source current		5	-	10	mA
B_{13}	bandwidth of output signal		-	5	-	MHz
	crosstalk of video signal	note 16				
α	external to internal		-	60	55	dB
α	internal to external		-	55	50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO SWITCH INPUT (note 17)						
V_7	maximum voltage for external video signal		-	-	2	V
V_7	minimum voltage for internal video signal		1	-	-	V
I_7	minimum source current for internal video signal		-	-	300	µA
I_7	input current	$V_7 = 0$ V	-	-	–1	mA
I_7	input current	$V_7 = V_P$	-	-	3	µA
AFC circuit (note 18)						
AFC SAMPLE-AND-HOLD/SWITCH (note 19)						
I_6	AFC switch: current level below which AFC outputs switches off		-	-	–500	µA
I_6	maximum AFC switch current	$V_6 = 0$ V	-	-	–1	mA
I_6	maximum leakage current		-	-	1	µA
AFC ANALOG OUTPUT ($V_9 > 8$ V; see Figs 4 and 5)						
$V_{8(p-p)}$	output voltage swing (peak-to-peak value)		10	-	11	V
I_8	maximum output current		500	-	-	µA
	control steepness		60	75	100	mV/kHz
V_8	AFC output voltage	AFC off	5	6	7	V
AFC DIGITAL OUTPUT (see Table 1)						
$V_{8,9}$	output voltage LOW		-	-	0.5	V
$V_{8,9}$	output voltage HIGH	50 kΩ load	4.5	-	5.5	V
Δf	frequency swing for switching AFC output Q1		65	80	100	kHz
$I_{8,9}$	maximum allowable output current		500	-	-	µA
AFC Analog SWITCH (note 20)						
I_9	minimum sink current for analog AFC		-	-	1.5	mA
V_9	minimum voltage for negative slope		-	-	10.2	V
V_9	minimum voltage for positive slope		-	-	8.0	V
V_9	maximum voltage for positive slope		10.2	-	-	V
I_9	output current	$V_9 = V_P$	-	500	-	µA
I_9	output current	$V_9 = 8$ to 10 V	-	150	-	µA
Video transmitter identification output (note 21)						
V_{18}	output voltage active	no sync; $I_{18} = 1$ mA	-	0.3	0.5	V
I_{18}	output current inactive	sync	-	-	3	µA
t_d	delay time of mute release after sync insertion		-	-	10	ms
I_{19}	allowed leakage current of identification detector capacitor		-	-	50	nA

Notes to the characteristics

1. All input signals are measured in RMS values at 100% carrier level and a frequency of 38.9 MHz.
2. On set AGC.
3. Input impedance selected so that a SAW filter can be applied without extra components.
4. Measured with 0 dB = 200 μV.
5. Measured at 10 mV(RMS) top sync input signal and the video output unloaded.
6. Projected zero point with internally switched demodulator.
7. With the AGC switch switched to ground, for the B/G standard, or with the identification capacitor switched to V_{CC} for the negative MAC standard.
8. With the AGC switch switched open for the L standard, or switched to V_{CC} for the positive MAC standard.
9. Measured in accordance with the test line given in Fig.8.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the phase angle of the 4.4 MHz signal at 20% and 80% luminance signal.
10. Measured in accordance with the test line shown in Fig.9.
    - The non-linearity is measured by comparing the differences between adjacent pairs of six luminance levels that make up the 5 step staircase. The measurement result is the largest percentage deviation in adjacent step values. The sign is always positive.
11. Measured with a 75 Ω source:

$$S/N = 20 \log \frac{V_{o\ \text{black-to white}}}{V_{n\ (RMS)\ \text{at}\ B = 5\ MHz}}$$

12. The internal circuit of pin 20 behaves as an internal voltage source of 4.5 V with an input resistance of 15 kΩ. Using the system switch three conditions can be obtained:
    - Negative modulation with top sync level AGC. This is achieved with pin 20 connected to ground.
    - Positive modulation with white level AGC. This is achieved with pin 20 open, or connected to 5 V.
    - Positive modulation with top white AGC and an increased time constant for MAC signals. This is achieved with pin 20 connected to V_{CC}.
13. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 200 μV to 80 mV input signals.
14. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 80 mV to 200 μV input signals.
15. It is possible to adjust the tuner AGC over the whole AGC range of the IF amplifier for both pnp and npn tuners. Tuner AGC starting point is defined as an output current of 0.2 mA for pnp and 1.8 mA for npn, in an application with a resistance of 6 kΩ to V_P at pin 4.
16. Crosstalk is defined as:

$$20 \log \frac{V_o\ \text{unwanted video black-to-white}}{V_o\ \text{wanted video black-to-white}} \quad \text{measured at 4.4 MHz}$$

17. The video switch is controlled by a voltage on pin 7. The switching level is approximately 1.4 V. With pin 7 open-circuit internal video is selected; with pin 7 pulled to ground external video is selected.
18. Measurement taken with an input 10 mV(RMS). The unloaded Q factor of the reference tuned circuit is 70.
19. Switching off the AFC is obtained by a voltage of less than 2 V on pin 6. Normally this is achieved by pulling pin 6 to ground.

Notes to the characteristics (continued)

20. Switching to the normal analog AFC mode can be done by pulling pin 9 to a voltage above 10.2 V. Normally this is achieved by pulling pin 9 to V_P.
    The inverse analog AFC mode can only be obtained by a voltage of between 8 and 10 V applied to pin 9.
21. All timing figures defined with a capacitor of 2.2 nF at pin 19. The identification can be speeded up by lowering the value of this capacitor, however this makes the circuit also less sensitive if the video signal is disturbed (airplane flutter etc.). If the identification is only used as a sound mute a capacitor of 47 nF is recommended to improve the sensitivity.

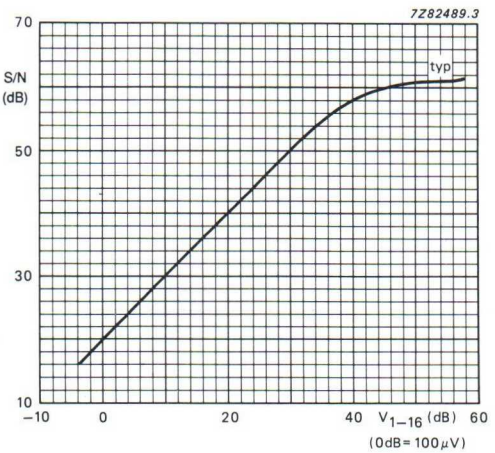


Fig.2 Signal-to-noise ratio as a function of video input.

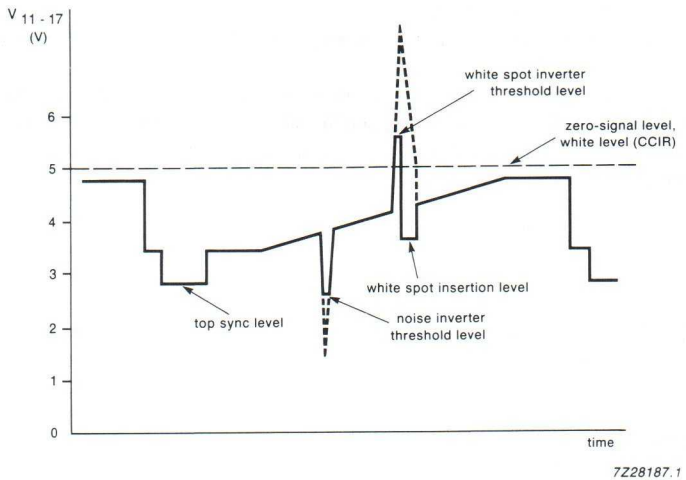


Fig.3 Video waveform showing white spot threshold and insertion levels, and noise clamping level.

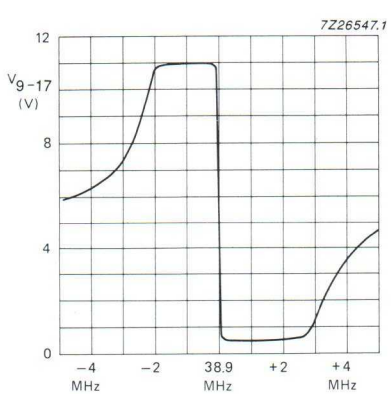


Fig.4 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

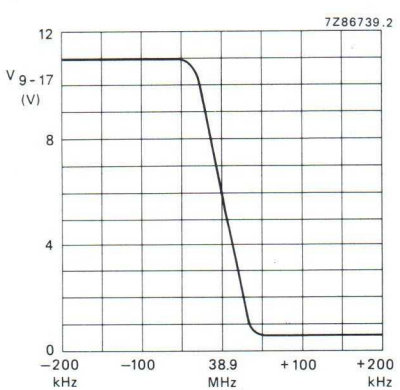
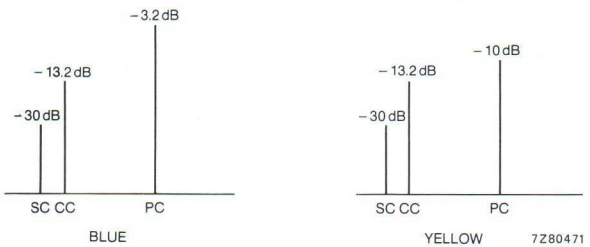


Fig.5 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

Table 1 Digital AFC truth table

INPUT FREQUENCY	Q1	Q2
> IF +40 kHz	0	1
> IF	1	1
< IF	1	0
< IF –40 kHz	0	0



SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level

Fig.6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

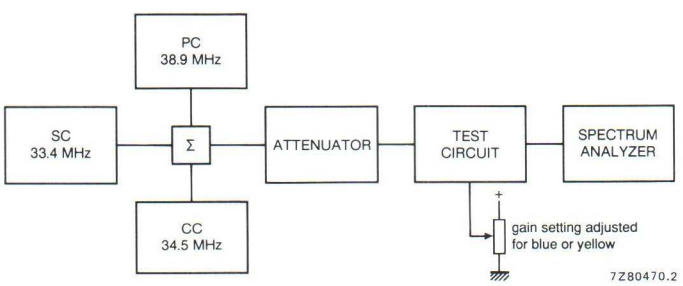


Fig.7 Test set-up intermodulation measurements.

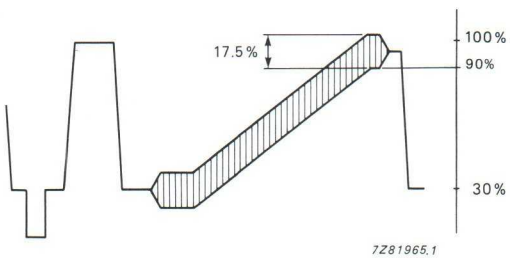


Fig.8 Video output signal.

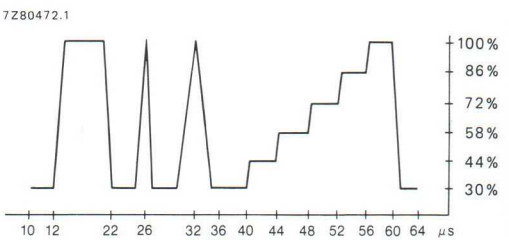


Fig.9 E.B.U. test signal wave form (line 330).

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins
  - short-circuit of the output pins to V_P
- High EMC immunity due to common mode inputs
- Temperature (thermal) protection
- East-West output stage with one single conversion resistor.

GENERAL DESCRIPTION

The TDA8350Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system and an East-West driver for sinking the diode modulator current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_P	quiescent current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
East-West amplifier						
$I_{O(sink)}$	output current (sink only)		–	–	500	mA
$V_{O(sink)}$	peak output voltage	$I_{O(sink)}$ = 10 μA	–	–	40	V
I_{bias}	input bias current		–	–	1	μA
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–65	–	150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8350Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

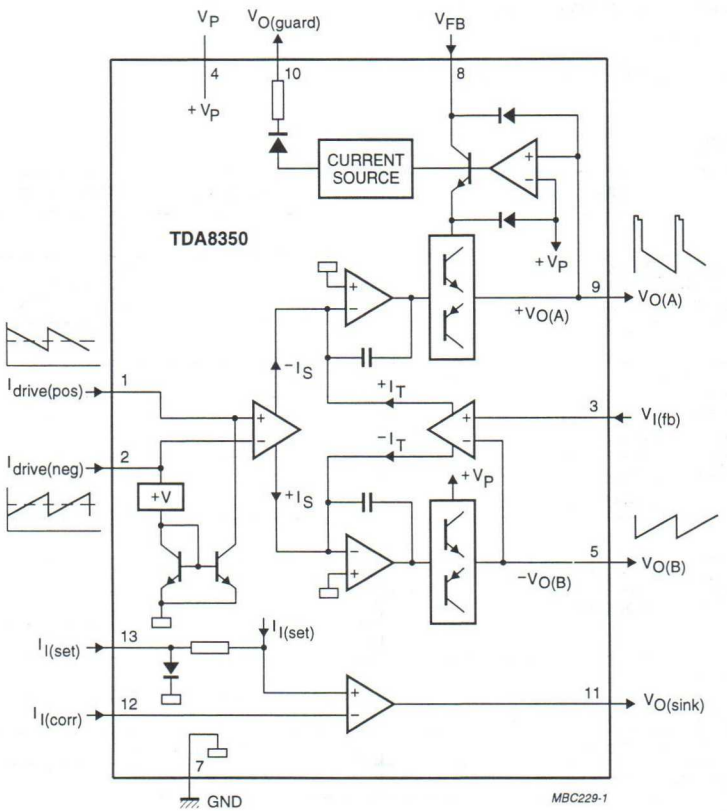


Fig.1 Block diagram.

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
$V_{I(fb)}$	3	feedback voltage input
V_P	4	supply voltage
$V_{O(B)}$	5	output voltage B
n.c.	6	not connected
GND	7	ground
V_{FB}	8	flyback supply voltage
$V_{O(A)}$	9	output voltage A
$V_{O(guard)}$	10	guard output voltage
$V_{O(sink)}$	11	East-West amplifier driver (sink) output voltage
$I_{I(corr)}$	12	East-West amplifier input correction current (negative)
$I_{I(set)}$	13	East-West amplifier set input current (positive)

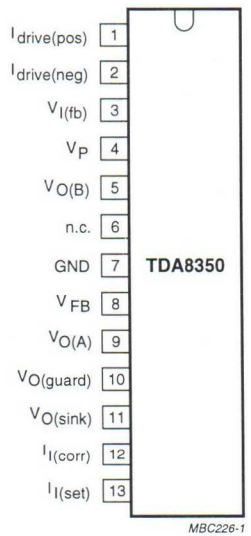


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feed back information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8367 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{(coil)} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 5 and 9)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during various short-circuit possibilities at the output pins
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

An East-West amplifier is also provided. This amplifier is an inverting amplifier which is current driven with sink current only capabilities.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
		note 1		60	V
Vertical circuit					
I_O	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 9)		–	52	V
		note 1		62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
East-West amplifier					
$V_{O(sink)}$	output voltage	$I_{O(sink)}$ = 10 µA; note 3	–	40	V
$I_{O(sink)}$	output current	$V_{O(sink)}$ = 2 V; note 3	–	500	mA
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–65	150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj\text{-}c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj\text{-}a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 4	–	1	hr

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. I_O maximum determined by current protection.
3. The operating area is limited by a straight line between the points $V_{O(sink)}$ = 40 V; $I_{O(sink)}$ = 10 µA and $V_{O(sink)}$ = 2 V; $I_{O(sink)}$ = 500 mA.
4. Up to V_p = 18 V.

CHARACTERISTICS

V_P = 17.5 V; V_{FB} = 45 V; $V_{O(sink)}$ = 20 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 µA; T_{amb} = 25°C; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9	–	25	V
V_{FB}	flyback supply voltage		V_p	–	50	V
		note 1	–	–	60	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 3 A (p-p)	19.8	–	–	V
LE	linearity error	I_O = 3 A (p-p);	–	1	2	%
		I_O = 50 mA (p-p); note 2	–	1	2	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1.5 A (M)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = –1.5 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	30	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier $V_{I(fb)}$ - $V_{O(B)}$	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	18	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0;	–	–	72	µV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 3	–	8	–	V
G_v	open loop voltage gain (V_{9-5}/V_{1-2})	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V_{9-5}/V_{3-5}; V_{1-2} = 0)	note 4	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{3-5}		–	0	–	dB
f_{res}	frequency response (–3 dB)	note 6	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
$\Delta G_I T$	current gain drift as a function of temperature		–	–	10^{-4}	/K
$I_{I(sb)}$	signal bias current		50	400	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
PSRR	power supply ripple rejection	note 7	–	80	–	dB
$V_{I(DC)}$	DC voltage at the input		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	µA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 µA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
East-West amplifier						
$V_{O(sink)}$	saturation voltage	$I_{O(sink)}$ = 500 mA; $I_{I(corr)}$ = 0 μA; note 8	–	2.0	2.5	V
G_v	open loop voltage gain (V_{11}/V_{12})		–	47	–	dB
f_{res}	frequency response (–3 dB)		–	4000	–	Hz
LE	linearity error	$V_{O(sink)}$ = 3 V	–	–	1	%
		$V_{O(sink)}$ = 10 V; note 2	–	–	0.5	%
I_{bias}	input bias current (pin 12)		–	–	2	μA
$V_{I(DC)}$	DC input voltage		–	1	–	V
I_{set}	offset voltage set current		–	1	–	mA
V_{13-7}	maximum allowed voltage at pin 13		–	–	0.3	V
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	μA
	output current	active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage	I_O = 100 μA	–	–	5.5	V
	allowable voltage on pin 10	maximum leakage current = 10 μA	–	–	40	V

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_5 - I_9 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below;

   $$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} ; NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

3. Referenced to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{9-5}/V_{1-2} = voltage value across pins 9 and 5 divided by voltage value across pins 1 and 2.
5. V_{3-5} AC short-circuited.
6. Frequency response V_{9-5}/V_{3-5} is equal to frequency response V_{9-5}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.
8. The output pin 11 requires a capacitor of minimum value 68 nF.

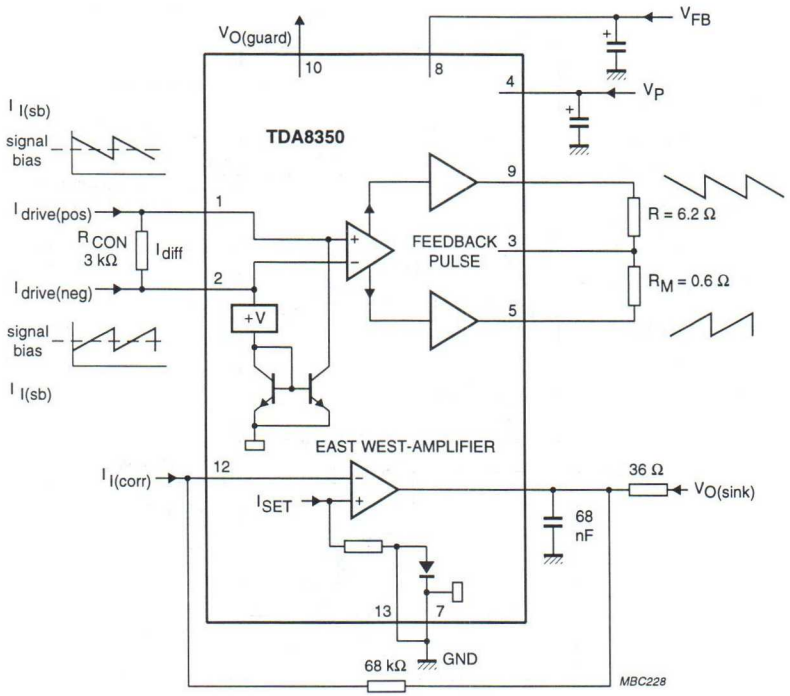
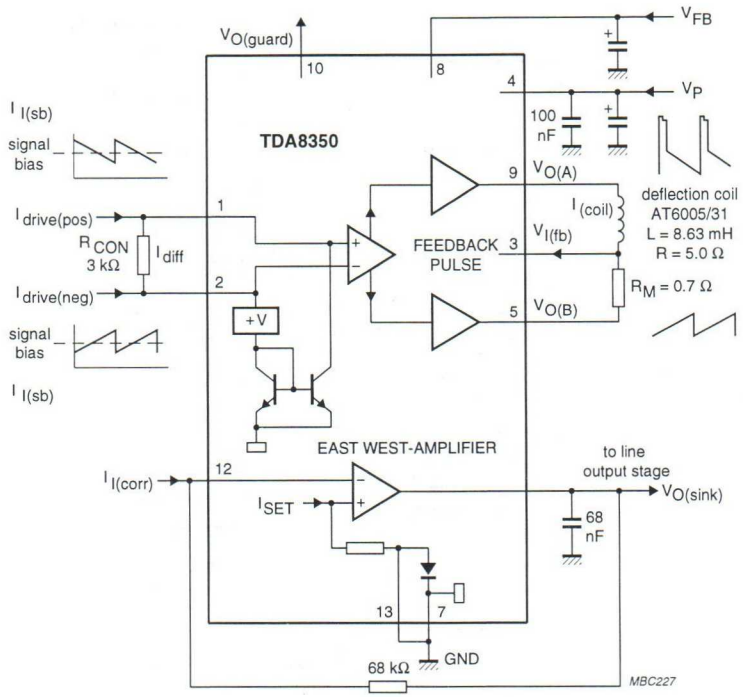


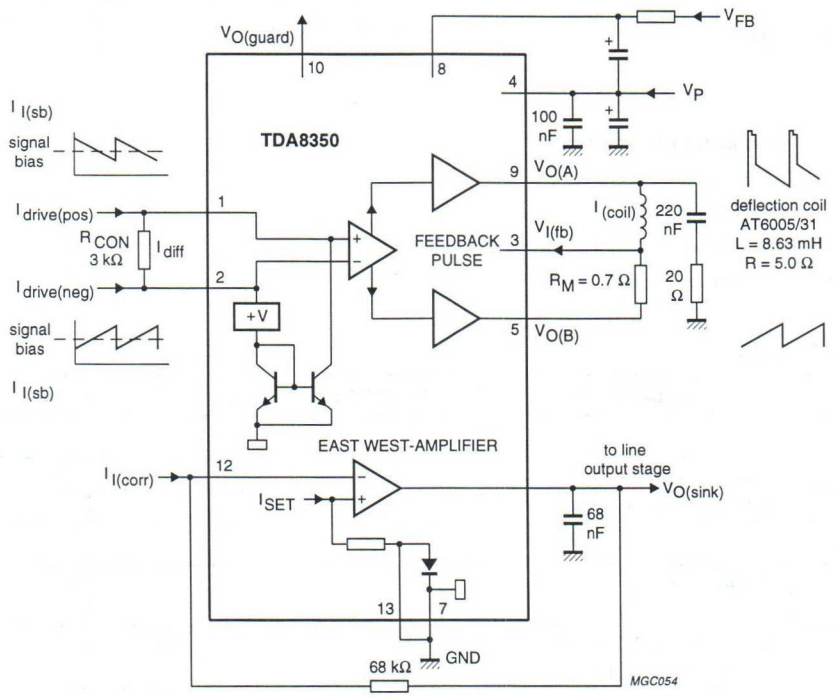
Fig.3 Test circuit.

APPLICATION INFORMATION



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p-p)}$ = 500 µA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.4 Application diagram.



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p-p)}$ = 500 μA; V_{FB} = 60 V; t_{FB} = 0.4 ms.

Fig.5 Application circuit; 50 V ≤ V_{FB} ≤ 60 V.

DC-coupled vertical deflection circuit TDA8351

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (7 and 4)
  - short-circuit of the output pins to V_P
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_q	quiescent supply current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

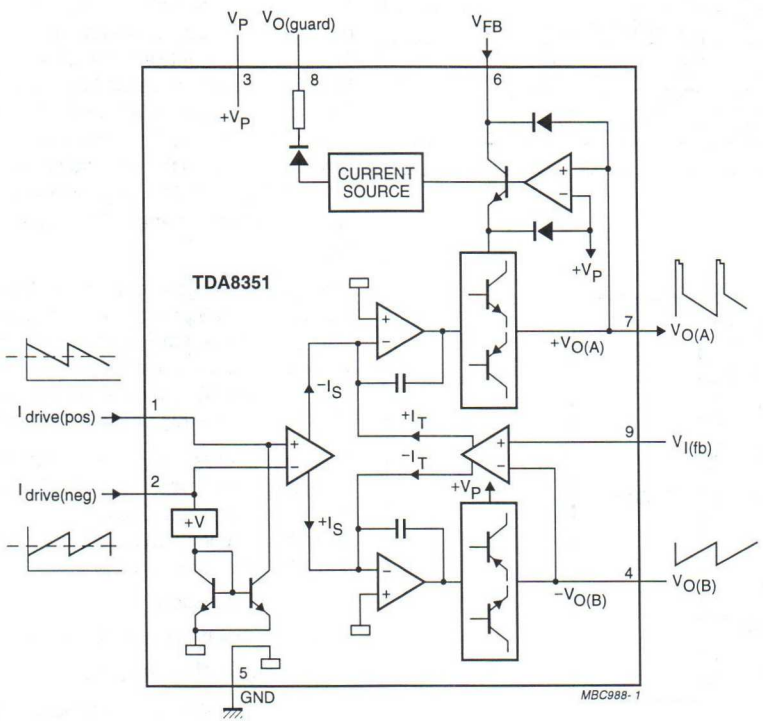
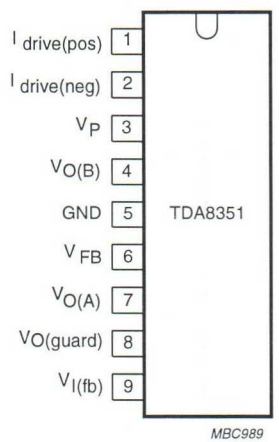


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



Metal block connected to substrate pin 5.
Metal on back.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to V_P or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
		note 1	–	60	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
		note 1	–	62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj-c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 3	–	1	hr

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. I_O maximum determined by current protection.
3. Up to V_P = 18 V.

CHARACTERISTICS

V_P = 17.5 V; T_{amb} = 25 °C; V_{FB} = 45 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 µA; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9.0	–	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
		note 1	V_P	–	60	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 3 A (p-p)	19.8	–	–	V
LE	linearity error	I_O = 3 A (p-p); note 2	–	1	2	%
		I_O = 50 mA (p-p); note 2	–	1	2	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1.5 A (M)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = –1.5 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	30	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier ($V_{I(fb)}$ - $V_{O(B)}$)	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	18	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0	–	–	72	µV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 3	–	8.0	–	V
G_{vo}	open-loop voltage gain (V_{7-4}/V_{1-2})	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V_{7-4}/V_{9-4}; V_{1-2} = 0)	note 4	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{9-4}		–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop; note 6	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
$\Delta G_c T$	current gain drift as a function of temperature		–	–	10^{-4}	K
$I_{I(sb)}$	signal bias current		50	400	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
PSRR	power supply ripple rejection	note 7	–	80	–	dB
$V_{I(DC)}$	DC input voltage		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	µA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 µA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	µA
		active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage on pin 8	I_O = 100 µA	–	–	5.5	V
	allowable voltage on pin 8	maximum leakage current = 10 µA;	–	–	40	V

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_4 - I_7 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} ; NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

3. Referenced to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{7-4}/V_{1-2} = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
5. V_{9-4} AC short-circuited.
6. Frequency response V_{7-4}/V_{9-4} is equal to frequency response V_{7-4}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.

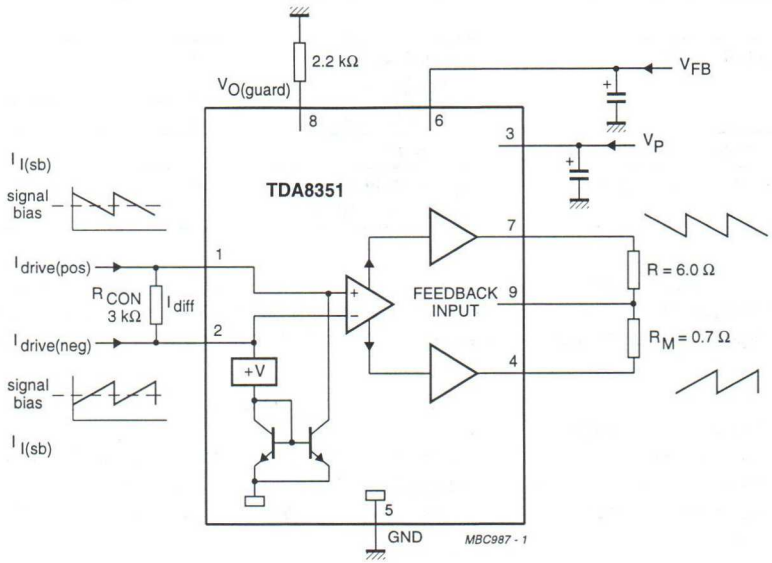


Fig.3 Test diagram.

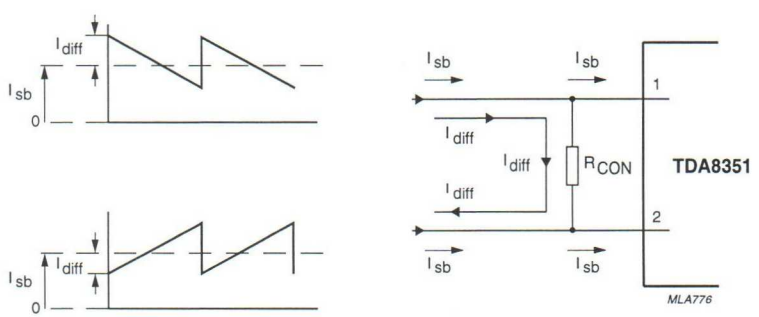
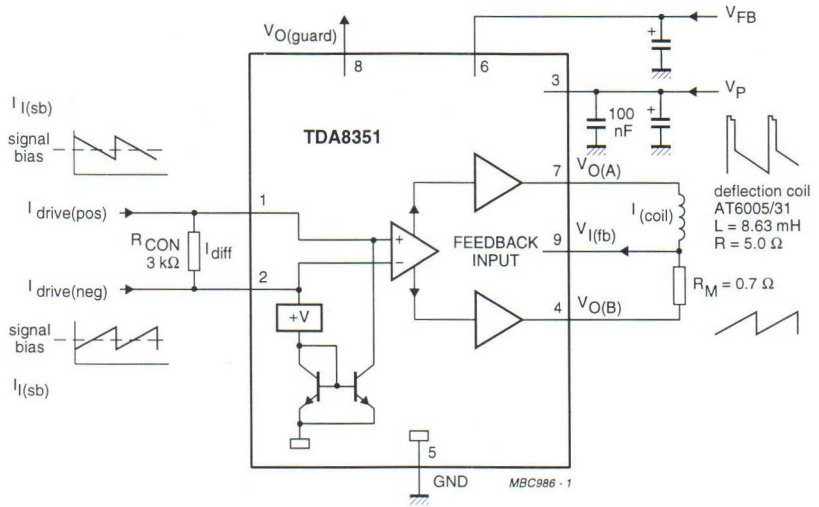


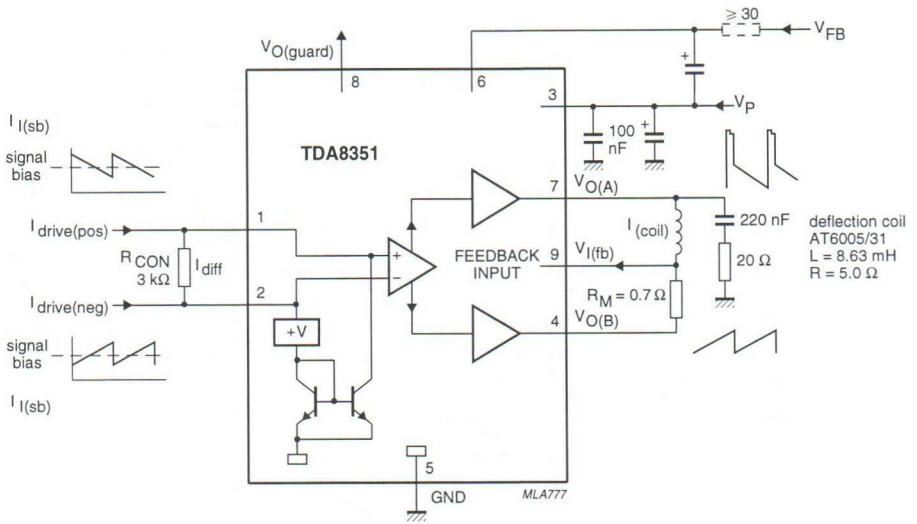
Fig.4 Input currents.

APPLICATION INFORMATION



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p-p)}$ = 500 μA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.5 Application diagram.



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p-p)}$ = 500 µA; V_{FB} = 60 V; t_{FB} = 0.4 ms.

Fig.6 Application circuit; 50 V ≤ V_{FB} ≤ 60 V.

DC-coupled vertical deflection output circuit

TDA8351A

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (9 and 5)
  - short-circuit of the output pins to V_P
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351A is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	16	25	V
I_q	quiescent supply current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.8	–	V
Flyback switch						
I_M	peak output current	$t \leq 1.5$ ms	–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 9 and pin 5. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).

DC-coupled vertical deflection output circuit

TDA8351A

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351A	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

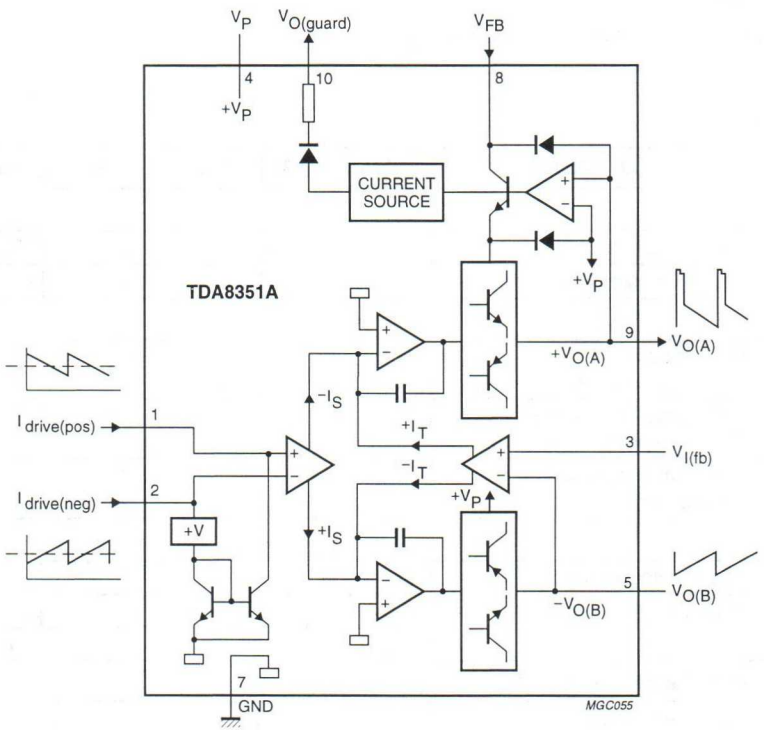


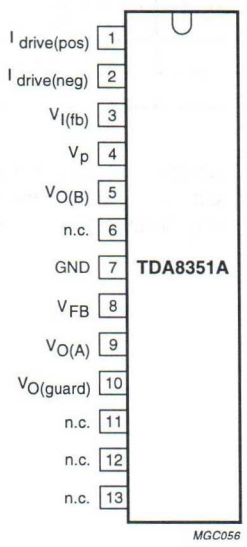
Fig.1 Block diagram.

DC-coupled vertical deflection output circuit

TDA8351A

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
$V_{I(fb)}$	3	input feedback voltage
V_P	4	supply voltage
$V_{O(B)}$	5	output voltage B
n.c.	6	not connected
GND	7	ground
V_{FB}	8	input flyback supply voltage
$V_{O(A)}$	9	output voltage A
$V_{O(guard)}$	10	guard output voltage
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected



The die has been glued to the metal block of the package. If the metal block is not insulated from the heat sink, the heat sink may only be connected directly to pin 7.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8367 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 5 and 9)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 5 and 9) to V_P or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
		note 1	–	60	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
		note 1	–	62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj-c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 3	–	1	hr

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. I_O maximum determined by current protection.
3. Up to V_P = 18 V.

CHARACTERISTICS

V_P = 17.5 V; V_{FB} = 45 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 µA; T_{amb} = 25 °C; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9.0	–	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
		note 1	V_P	–	60	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 3 A (p-p)	19.8	–	–	V
LE	linearity error	I_O = 3 A (p-p); note 2	–	1	2	%
		I_O = 50 mA (p-p); note 2	–	1	2	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1.5 A (M)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = −1.5 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	30	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier ($V_{I(fb)}$ - $V_{O(B)}$)	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	18	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0	–	–	72	µV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 3	–	8.0	–	V
G_{vo}	open-loop voltage gain (V_{7-4}/V_{1-2})	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V_{7-4}/V_{9-4}; V_{1-2} = 0)	note 4	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{9-4}		–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop; note 6	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
$\Delta G_c T$	current gain drift as a function of temperature		–	–	10^{-4}	K
$I_{I(sb)}$	signal bias current		50	400	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
PSRR	power supply ripple rejection	note 7	–	80	–	dB
$V_{I(DC)}$	DC input voltage		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	µA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 µA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	μA
		active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage on pin 8	I_O = 100 μA	–	–	5.5	V
	allowable voltage on pin 8	maximum leakage current = 10 μA;	–	–	40	V

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 9 and pin 5. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_5 - I_9 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} ; NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

3. Referenced to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{9-5}/V_{1-2} = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
5. V_{9-4} AC short-circuited.
6. Frequency response V_{9-5}/V_{3-5} is equal to frequency response V_{9-5}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.

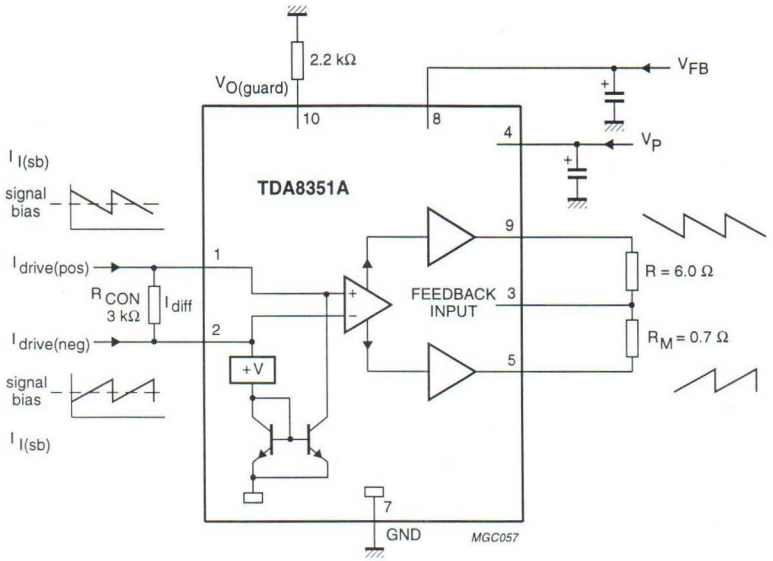
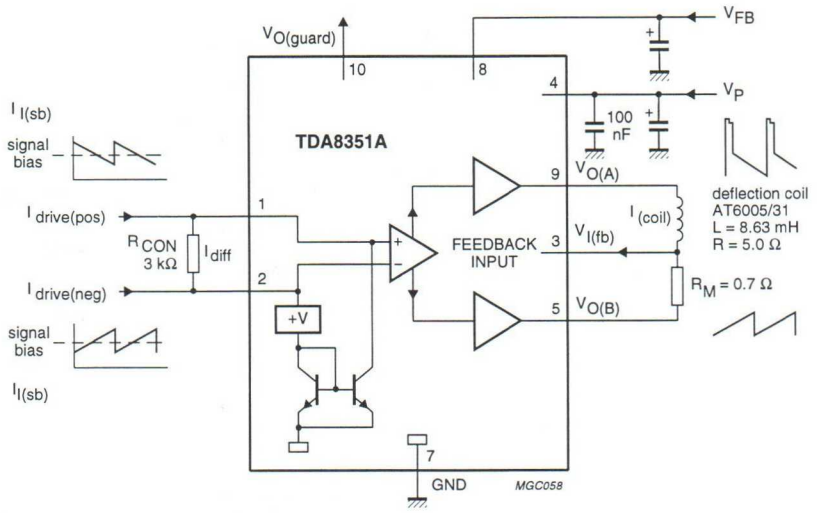


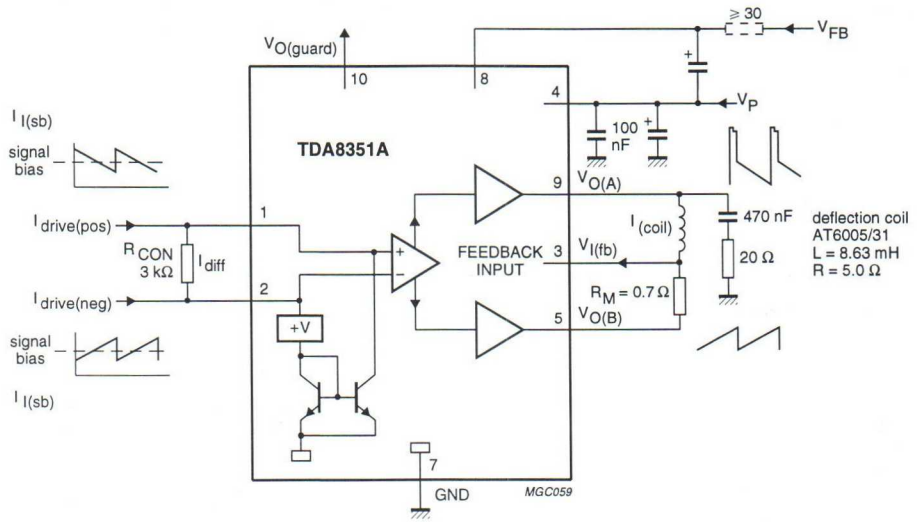
Fig.3 Test diagram.

APPLICATION INFORMATION



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p-p)}$ = 500 µA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.4 Application diagram.



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p-p)}$ = 500 μA; V_{FB} = 60 V; t_{FB} = 0.4 ms.

Fig.5 Application circuit; 50 V ≤ V_{FB} ≤ 60 V.

DC-coupled vertical deflection circuit TDA8356

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (7 and 4)
  - short-circuit of the output pins to V_P
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8356 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage	9	4.5	25	V
I_q	quiescent supply current	–	30	–	mA
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	–	–	2	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)	–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)	–	1.5	1.8	V
Flyback switch					
I_M	peak output current	–	–	±1	A
V_{FB}	flyback supply voltage	–	–	50	V
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature	–55	–	+150	°C
T_{amb}	operating ambient temperature	–25	–	+75	°C
T_{vj}	virtual junction temperature	–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8356	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

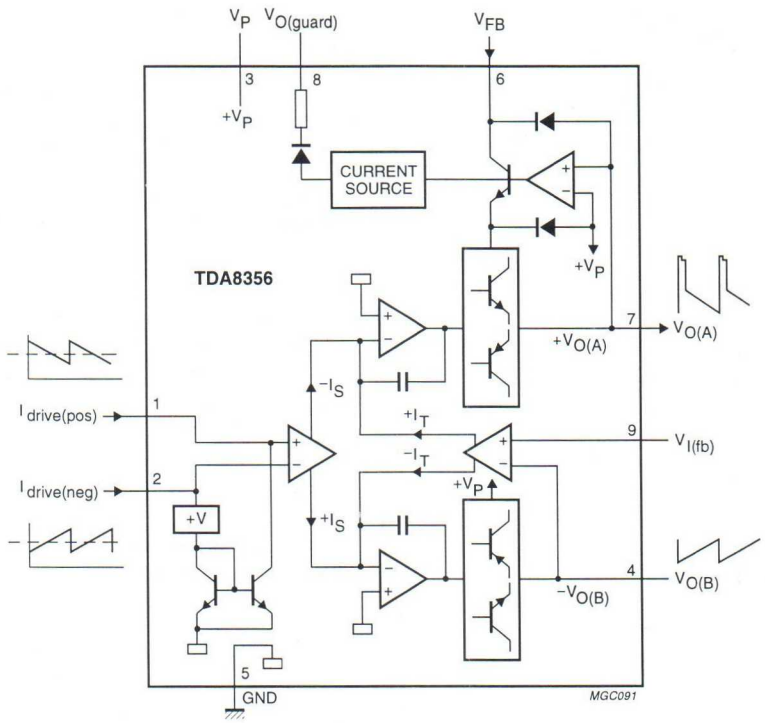
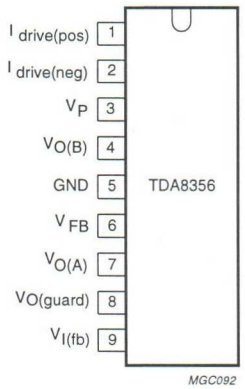


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



Metal block connected to substrate pin 5.
Metal on back.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 2 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to V_P or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 1	–	2	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj-c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 2	–	1	hr

Notes

1. I_O maximum determined by current protection.
2. Up to V_P = 18 V.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; V_{FB} = 45 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 µA; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9.0	4.5	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 2 A (p-p)	13.2	–	–	V
LE	linearity error	I_O = 2 A (p-p); note 1	–	1	4	%
		I_O = 50 mA (p-p); note 1	–	1	4	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1 A (M)	–	40	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = –1 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	40	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier ($V_{I(fb)}$ - $V_{O(B)}$)	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	24	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0	–	–	72	µV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 2	–	6.5	–	V
G_{vo}	open-loop voltage gain (V_{7-4}/V_{1-2})	notes 3 and 4	–	80	–	dB
	open loop voltage gain (V_{7-4}/V_{9-4}; V_{1-2} = 0)	note 3	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{9-4}		–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop; note 5	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
$\Delta G_c T$	current gain drift as a function of temperature		–	–	10^{-4}	K
$I_{I(sb)}$	signal bias current		50	400	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
PSRR	power supply ripple rejection	note 6	–	80	–	dB
$V_{I(DC)}$	DC input voltage		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	µA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 µA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	µA
		active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage on pin 8	I_O = 100 µA	–	–	5.5	V
	allowable voltage on pin 8	maximum leakage current = 10 µA;	–	–	40	V

Notes

1. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_4 - I_7 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below

   $$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}}; \quad NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

2. Related to V_P.
3. V values within formulae, relate to voltages at or between relative pin numbers, i.e. $V_{7\text{-}4}/V_{1\text{-}2}$ = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
4. $V_{9\text{-}4}$ AC short-circuited.
5. Frequency response $V_{7\text{-}4}/V_{9\text{-}4}$ is equal to frequency response $V_{7\text{-}4}/V_{1\text{-}2}$.
6. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.

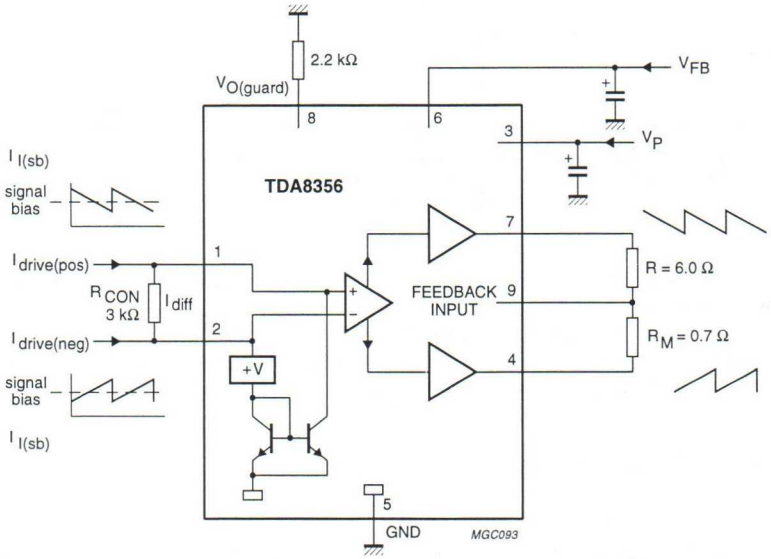


Fig.3 Test diagram.

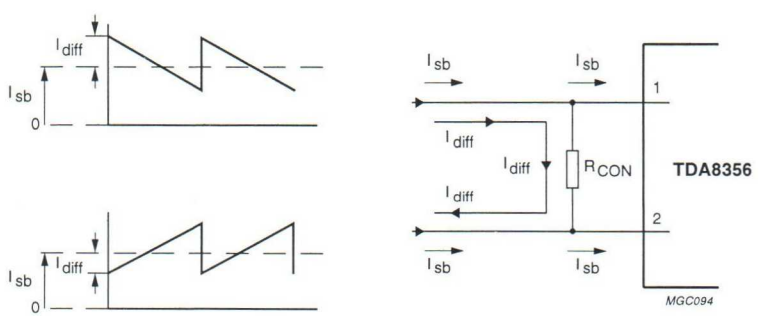
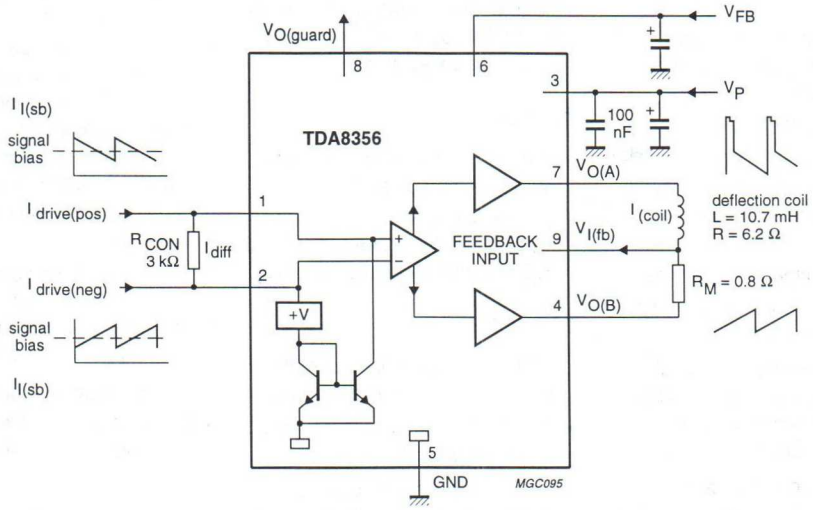


Fig.4 Input currents.

APPLICATION INFORMATION



V_P = 13.5 V; $I_{O(p-p)}$ = 1.87 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p-p)}$ = 500 μA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.5 Application diagram.

Integrated PAL and PAL/NTSC TV processors

TDA8360; TDA8361; TDA8362

FEATURES

Available in TDA8360, TDA8361 and TDA8362

- Vision IF amplifier with high sensitivity and good differential gain and phase
- Multistandard FM sound demodulator (4.5 MHz to 6.5 MHz)
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- RGB control circuit with linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator without external components
- Vertical count-down circuit (50/60 Hz) and vertical preamplifier
- Low dissipation (700 mW)
- Small amount of peripheral components compared with competition ICs
- Only one adjustment (vision IF demodulator)
- The supply voltage for the ICs is 8 V. They are mounted in a shrink DIL envelope with 52 pins and are pin compatible.

Additional features

TDA8360

- Alignment-free PAL colour decoder for all PAL standards, including PAL-N and PAL-M.

TDA8361

- PAL/NTSC colour decoder with automatic search system
- Source selection for external audio/video (A/V) inputs (separate Y/C signals can also be applied).

TDA8362

- Multistandard vision IF circuit (positive and negative modulation)
- PAL/NTSC colour decoder with automatic search system
- Source selection for external A/V inputs (separate Y/C signals can also be applied)
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications.

GENERAL DESCRIPTION

The TDA8360, TDA8361 and TDA8362 are single-chip TV processors which contain nearly all small signal functions that are required for a colour television receiver. For a complete receiver the following circuits need to be added: a base-band delay line (TDA4661), a tuner and output stages for audio, video and horizontal and vertical deflection.

Because of the different functional contents of the ICs the set maker can make the optimum choice depending on the requirements for the receiver.

The TDA8360 is intended for simple PAL receivers (all PAL standards, including PAL-N and PAL-M are possible).

The TDA8361 contains a PAL/NTSC decoder and has an A/V switch.

For real multistandard applications the TDA8362 is available. In addition to the extra functions which are available in the TDA8361, the TDA8362 can handle signals with positive modulation and it supplies the signals which are required for the SECAM decoder TDA8395.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8360	52	shrink DIL	plastic	SOT247AG
TDA8361	52	shrink DIL	plastic	SOT247AG
TDA8362	52	shrink DIL	plastic	SOT247AG

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current		–	80	–	mA
Input voltages						
$V_{45,46(rms)}$	video IF amplifier sensitivity (RMS value)		–	70	100	μV
$V_{5(rms)}$	sound IF amplifier sensitivity (RMS value)		–	1	–	mV
$V_{6(rms)}$	external audio input (RMS value)	TDA8361, TDA8362	–	350	–	mV
$V_{15(p-p)}$	external CVBS input (peak-to-peak value)	TDA8361, TDA8362	–	1	–	V
$V_{22,23,24(p-p)}$	RGB inputs (peak-to-peak value)		–	0.7	–	V
Output signals						
$V_{O(p-p)}$	demodulated CVBS output (peak-to-peak value)		–	2.4	–	V
I_{47}	tuner AGC control current		0	–	5	mA
V_{44}	AFC output voltage swing		–	6	–	V
$V_{50(rms)}$	audio output voltage (RMS value)		–	700	–	mV
$V_{18,19,20(p-p)}$	RGB output signal amplitudes (peak-to-peak value)		–	4	–	V
I_{37}	horizontal output current		10	–	–	mA
I_{43}	vertical output current		1	–	–	mA
Control voltages						
$V_{control}$	control voltages for Volume, Contrast, Saturation, Brightness, Hue and Peaking		0	–	5	V

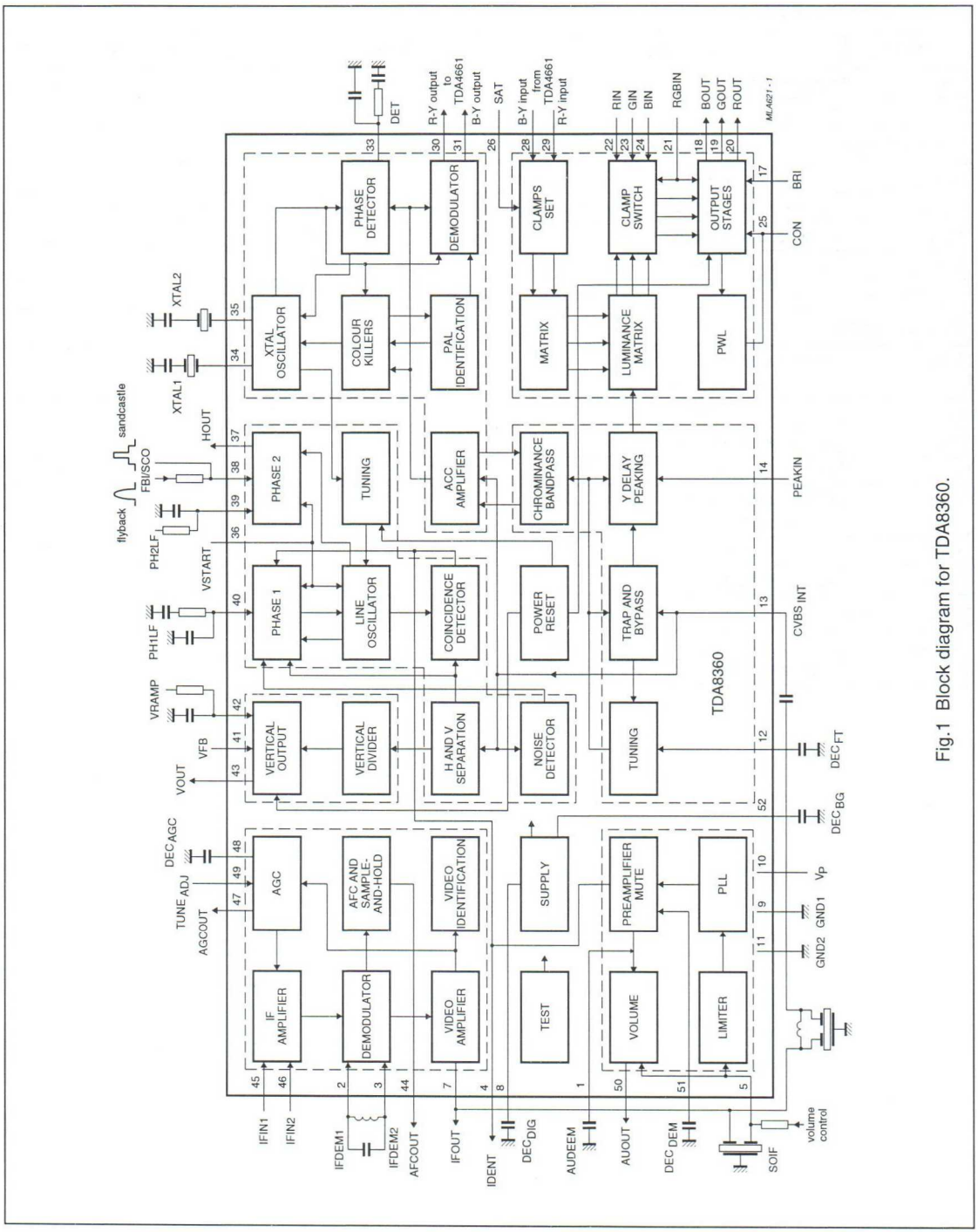


Fig.1 Block diagram for TDA8360.

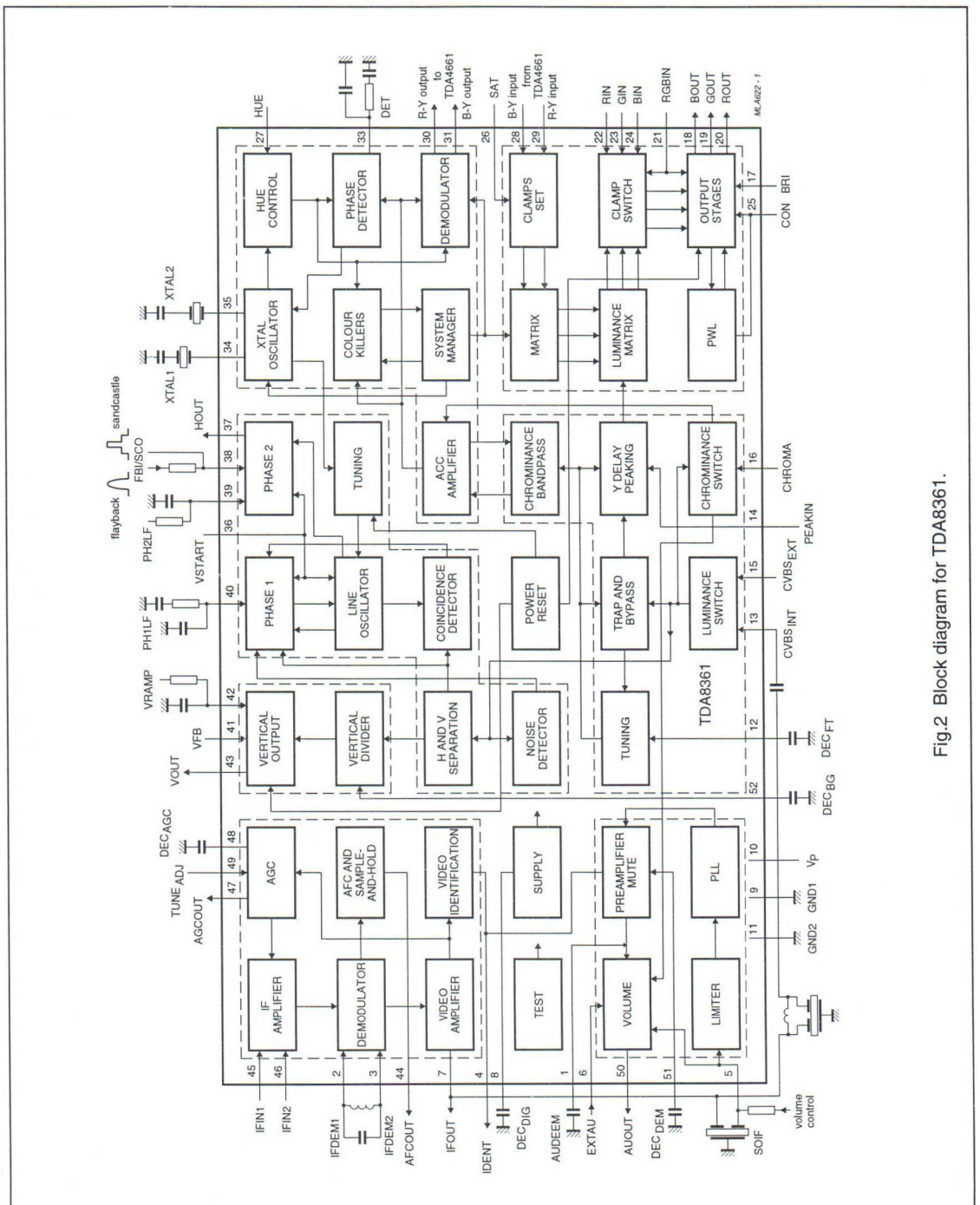


Fig.2 Block diagram for TDA8361.

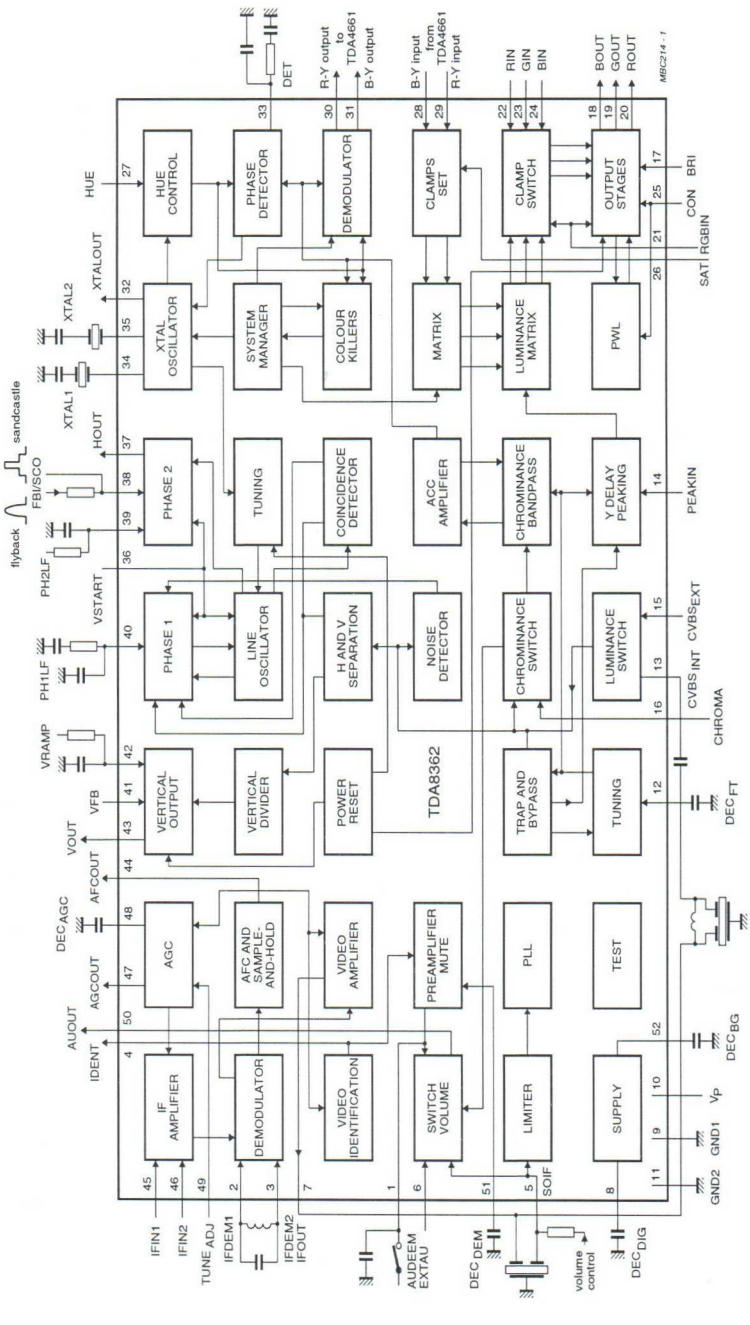


Fig.3 Block diagram for TDA8362.

PINNING (TDA8362)

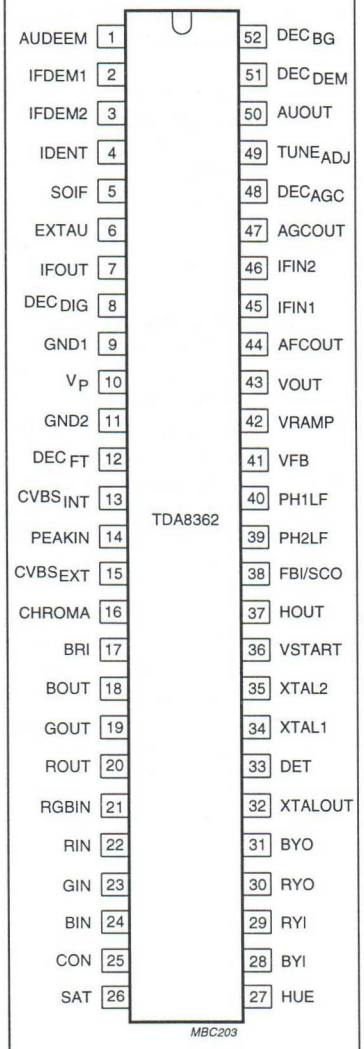


Fig.4 Pin configuration for TDA8362.

SYMBOL	PIN	DESCRIPTION
AUDEEM	1	audio de-emphasis and ± modulation switch
IFDEM1	2	IF demodulator tuned circuit
IFDEM2	3	IF demodulator tuned circuit
IDENT	4	video identification output/$\overline{\text{MUTE}}$ input
SOIF	5	sound IF input and volume control
EXTAU	6	external audio input
IFOUT	7	IF video output
DEC_{DIG}	8	decoupling digital supply
GND1	9	ground 1
V_P	10	supply voltage (+8 V)
GND2	11	ground 2
DEC_{FT}	12	decoupling filter tuning
$CVBS_{INT}$	13	internal CVBS input
PEAKIN	14	peaking control input
$CVBS_{EXT}$	15	external CVBS input
CHROMA	16	chrominance and A/V switch input
BRI	17	brightness control input
BOUT	18	blue output
GOUT	19	green output
ROUT	20	red output
RGBIN	21	RGB insertion and blanking input
RIN	22	red input
GIN	23	green input
BIN	24	blue input
CON	25	contrast control input
SAT	26	saturation control input
HUE	27	hue control input (or chrominance output)
BYI	28	B–Y input signal
RYI	29	R–Y input signal
RYO	30	R–Y output signal
BYO	31	B–Y output signal
XTALOUT	32	4.43 MHz output for TDA8395
DET	33	loop filter burst phase detector
XTAL1	34	3.58 MHz crystal connection
XTAL2	35	4.43 MHz crystal connection
VSTART	36	supply/start horizontal oscillator
HOUT	37	horizontal output
FBI/SCO	38	flyback input/sandcastle output
PH2LF	39	phase 2 loop filter
PH1LF	40	phase 1 loop filter

SYMBOL	PIN	DESCRIPTION
VFB	41	vertical feedback input
VRAMP	42	vertical ramp generator
VOUT	43	vertical output
AFCOUT	44	AFC output
IFIN1	45	IF input 1
IFIN2	46	IF input 2
AGCOUT	47	tuner AGC output
DEC_{AGC}	48	AGC decoupling capacitor
$TUNE_{ADJ}$	49	tuner take-over adjustment
AUOUT	50	audio output
DEC_{DEM}	51	decoupling sound demodulator
DEC_{BG}	52	decoupling bandgap supply

TDA8360

The TDA8360 has the following differences to the pinning:

Pin 6: external audio input not connected

Pin 15: external CVBS input not connected

Pin 16: chrominance and A/V switch input not connected

Pin 27: hue control input not connected.

TDA8361

The TDA8361 has the following differences to the pinning:

Pin 1: only audio de-emphasis

Pin 27: only hue control

Pin 32: 4.43 MHz output for TDA8395 is not connected.

FUNCTIONAL DESCRIPTION

Video IF amplifier

The IF amplifier contains 3 AC-coupled control stages with a total gain control range of greater than 60 dB. The sensitivity of the circuit is comparable with that of modern IF ICs.

The reference carrier for the video demodulator is obtained by means of passive regeneration of the picture carrier. The external reference tuned circuit is the only remaining adjustment of the IC.

In the TDA8362 the polarity of the demodulator can be switched so that the circuit is suitable for both positive and negative modulated signals.

The AFC circuit is driven with the same reference signal as the video demodulator. To ensure that the video content does not disturb the AFC operation a sample-and-hold circuit is incorporated; the capacitor for this function is internal. The AFC output voltage is 6 V.

The AGC detector operates on levels, top sync for negative modulated and top white for positive modulated signals.The AGC detector time constant capacitor is connected externally. This is mainly because of the flexibility of the application.

The time constant of the AGC system during positive modulation (TDA8362) is slow, this is to avoid any visible picture variations. This, however, causes the system to react very slowly to sudden changes in the input signal amplitude.

To overcome this problem a speed-up circuit has been included which detects whether the AGC detector is activated every frame period. If, during a 3-frame period, no action is detected the speed of the system is increased. When the incoming signal has no peak white information (e.g. test lines in the vertical retrace period) the gain would be video signal dependent. To avoid this effect the circuit also contains a black level AGC detector which is activated when the black level of the video signal exceeds a certain level.

The TDA8361 and TDA8362 contain a video identification circuit which is independent of the synchronization circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. In the TDA8360 this circuit is only used for stable OSD at no signal input. In the normal television mode the identification output is connected to the coincidence detector, this applies to all three devices. The identification output voltage is LOW when no transmitter is identified. In this condition the sound demodulator is switched off (mute function). When a transmitter is identified the output voltage is HIGH. The voltage level is dependent on the frequency of the incoming chrominance signal.

Sound circuit

The sound bandpass and trap filters have to be connected externally. The filtered intercarrier signal is fed to a limiter circuit and is demodulated by means of a PLL demodulator. The PLL circuit tunes itself automatically to the incoming signal, consequently, no adjustment is required.

The volume is DC controlled. The composite audio output signal has an amplitude of 700 mV RMS at a volume control setting of –6 dB. The de-emphasis capacitor has to be connected externally. The non-controlled audio signal can be obtained from this pin via a buffer stage. The amplitude of this signal is 350 mV RMS.

The TDA8361 and TDA8362 external audio input signal must have an amplitude of 350 mV RMS. The audio/video switch is controlled via the chrominance input pin.

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are then fed to the slicing stage (separator) which operates at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used for transmitter identification and to detect whether the line oscillator is synchronized. When the circuit is not synchronized the voltage on the peaking control pin (pin 14) is LOW so that this condition can be detected externally. The first PLL has a very high static steepness, this ensures that the phase of the picture is independent of the line frequency. The line oscillator operates at twice the line frequency.

The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC. The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.

The circuit employs a second control loop to generate the drive pulses for the horizontal driver stage.

X-ray protection can be realised by switching the pin of the second control loop to the positive supply line. The detection circuit must be connected externally. When the X-ray protection is active the horizontal output voltage is switched to a high level. When the voltage on this pin returns to its normal level the horizontal output is released again.

The IC contains a start-up circuit for the horizontal oscillator. When this feature is required a current of 6.5 mA has to be supplied to pin 36. For an application without start-up both supply pins (10 and 36) must be connected to the 8 V supply line.

The drive signal for the vertical ramp generator is generated by means of a divider circuit. The RC network for the ramp generator is external.

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by means of gyrator circuits and are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder.
In the TDA8361 and TDA8362 the chrominance trap is active only when the separate chrominance input pin is connected to ground or to the positive supply voltage and when a colour signal is recognized.

When the pin is left open-circuit the trap is switched off so that the circuit can also be used for S-VHS applications.

The luminance delay line and the delay for the peaking circuit are also realised by means of gyrator circuits.

Colour decoder

The colour decoder in the various ICs contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally. Because the main differences of the 3 ICs are found in the colour decoder the various types will be discussed.

TDA8360

This IC contains only a PAL decoder. Depending on the frequency of the crystals which are connected to the IC the decoder can demodulate all PAL standards. Because the horizontal oscillator is calibrated by using the crystal frequency as a reference the 4.4 MHz crystal must be connected to pin 35 and the 3.5 MHz crystal to pin 34. When only one crystal is connected to the IC the other crystal pin must be connected to the positive supply rail via a 47 kΩ resistor. For applications with two 3.5 MHz crystals both must be connected to pin 34 and the switching between the crystals must be made externally. Switching of the crystals is only allowed directly after the vertical retrace. The circuit will indicate whether a PAL signal has been identified by the colour decoder via the saturation control pin.

When two crystals are connected to the IC the output voltage of the video identification circuit indicates the frequency of the incoming chrominance signal.

The conditions are:

- Signal identified at f_{osc} = 3.6 MHz; V_O = 6 V
- Signal identified at f_{osc} = 4.4 MHz (or no colour); V_O = 8 V.

This information can be used to switch the sound bandpass filter and trap filter.

TDA8361

This IC contains an automatic PAL/NTSC decoder. The conditions for connecting the reference crystals are the same as for the TDA8360. The decoder can be forced to PAL when the hue control pin is connected to the positive supply voltage via a 5 kΩ or 10 kΩ resistor (approximately). The decoder cannot be forced to the NTSC standard. It is also possible to see if a colour signal is recognized via the saturation pin.

TDA8362

In addition to the possibilities of the TDA8361, the TDA8362 can co-operate with the SECAM add-on decoder TDA8395.
The communication between the two ICs is achieved via pin 32. The TDA8362 supplies the reference signal (4.43 MHz) for the calibration system of the TDA8395, identification of the colour standard is via the same connection. When a SECAM signal is detected by the TDA8395 the IC will draw a current of 150 µA. When TDA8362 has not identified a colour signal in this condition it will go into the SECAM mode, that means it will switch off the R–Y and B–Y outputs and increase the voltage level on pin 32.

This voltage will switch off the colour-killer in the TDA8395 and switch on the R–Y and B–Y outputs of the TDA8395. Forcing the system to the SECAM standard can be achieved by loading pin 32 with a current of 150 µA. Then the system manager in the TDA8362 will not search for PAL or NTSC signals. Forcing to NTSC is not possible.
For PAL/SECAM applications the input signal for the TDA8395 can be obtained from pin 27 (hue control) when this pin is connected to the positive supply rail via the 5 kΩ or 10 kΩ resistor. An external source selector is required by the TDA8395/TDA8362 combination for PAL/SECAM/NTSC applications.

RGB output circuit

The colour difference signals are matrixed with the luminance signal to obtain the RGB signals. Linear amplifiers have been chosen for the RGB inputs so that the circuit is suitable for incoming signals from the SCART connector. The contrast and brightness controls operate on internal and external signals.

The fast blanking pin has a second detection level at 3.5 V.
When this level is exceeded the RGB outputs are blanked so that "On-Screen-Display" signals can be applied to the outputs.
The output signal has an amplitude of approximately 4 V, black-to-white, with nominal input signals and nominal control settings. The nominal black level is 1.3 V.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–	9.0	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C
T_{sol}	soldering temperature for 5 s	–	260	°C
T_j	maximum junction temperature (operating)	–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pin 10)		7.2	8.0	8.8	V
I_P	supply current (pin 10)		–	80	–	mA
I_{HOSC}	horizontal oscillator start current (pin 36)	note 1	6.5	–	–	mA
P_{tot}	total power dissipation	including start supply	–	0.7	–	W
IF circuit						
VISION IF AMPLIFIER INPUTS (PINS 45 AND 46)						
$V_{i(rms)}$	input sensitivity (RMS value)	note 2				
		f_i = 38.90 MHz	–	70	100	μV
		f_i = 45.75 MHz	–	70	100	μV
		f_i = 58.75 MHz	–	70	100	μV
R_I	Input resistance (differential)	note 3	–	2	–	kΩ
C_I	Input capacitance (differential)	note 3	–	3	–	pF
G_{cr}	gain control range		64	–	–	dB
$V_{i(rms)}$	maximum input signal (RMS value)		100	–	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER OUTPUT; NOTE 4 (PIN 7)						
V_7	negative modulation					
	zero signal output level	note 5	4.45	4.6	4.75	V
	top sync level		1.9	2	2.1	V
V_7	positive modulation (TDA8362)					
	zero signal output level	note 5	1.85	2	2.15	V
	white level		4.2	4.3	4.4	V
ΔV_7	difference in amplitude between negative and positive modulation		–	0	15	%
V_7	detection level of black level for positive modulation when no peak white is available in the signal		–	3.1	–	V
Z_O	video output impedance		–	–	50	Ω
I_{bias}	internal bias current of NPN emitter follower output transistor		1	–	–	mA
I_{source}	maximum source current		–	–	5	mA
B	bandwidth of demodulated output signal	–3 dB	6	9	–	MHz
G_{diff}	gain differential	note 6	–	2	5	%
Φ_{diff}	phase differential	notes 6 and 7	–	1	5	deg
NL_{vid}	video non linearity	note 8	–	–	5	%
V_{th}	white spot threshold voltage level		–	4.8	–	V
V_{ins}	white spot insertion voltage level		–	3.2	–	V
N_{clamp}	noise inverter clamping voltage level		–	1.4	–	V
N_{ins}	noise inverter insertion level	note 9	–	2.6	–	V
δ_{mod}	intermodulation	notes 7 and 10				
	blue	V_o = 0.92 or 1.1 MHz	60	66	–	dB
	yellow	V_o = 0.92 or 1.1 MHz	56	62	–	dB
	blue	V_o = 2.66 or 3.3 MHz	60	66	–	dB
	yellow	V_o = 2.66 or 3.3 MHz	60	66	–	dB
S/N	signal-to-noise ratio	notes 7 and 11				
		V_i = 10 mV	52	60	–	dB
		end of control range	52	61	–	dB
V_7	residual carrier signal	note 7	–	1	–	mV
V_7	residual 2nd harmonic of carrier signal	note 7	–	0.5	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AND TUNER AGC; NOTE 12						
Timing of IF-AGC (C48 = 2.2 µF)						
	modulated video interference	30% AM for 1 to 100 mV; 0 to 200 Hz	–	–	10	%
t_{inc}	response time for an IF input signal amplitude increase of 52 dB for positive and negative modulation		–	2	–	ms
t_{dec}	response time for an IF input signal amplitude decrease of 52 dB					
	for negative modulation		–	25	–	ms
	for positive modulation (TDA8362)		–	100	–	ms
I_{leak}	allowed leakage current of the AGC capacitor	note 13				
	for negative modulation		–	–	10	µA
	for positive modulation		–	–	200	nA
Tuner take-over adjustment (pin 49)						
$V_{49(rms)}$	minimum starting level voltage for tuner take-over (RMS value)		–	0.2	0.5	mV
$V_{49(rms)}$	maximum starting level voltage for tuner take-over (RMS value)		100	150	–	mV
V_{cr}	control voltage range		0.5	–	4.5	V
Tuner control output (pin 47)						
V_{47}	maximum tuner AGC output voltage	maximum gain	–	–	$V_P + 1$	V
$V_{47(sat)}$	output saturation voltage	minimum gain; I_{47} = 2 mA	–	–	300	mV
I_{47}	maximum tuner AGC output swing		5	–	–	mA
I_{leak}	leakage current RF AGC		–	–	1	µA
ΔV_{47}	input signal variation for complete tuner control	$I_{O(max)}$ = 1 mA	1	2	4	dB
AFC OUTPUT; NOTE 14 (PIN 44)						
V_{44}	output voltage swing		–	6	–	V
f_{sl}	AFC slope		–	33	–	mV/kHz
f_{os}	AFC offset	note 7	–	–	50	kHz
V_O	output voltage at centre frequency		–	3.5	–	V
Z_O	output impedance		–	50	–	kΩ
SWITCHING TO POSITIVE MODULATION (TDA8362); NOTE 15 (PIN 1)						
V_1	minimum voltage on pin 1 to switch the video demodulator and AGC to positive modulation		–	–	$V_P - 1$	V
I_I	input current		–	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO IDENTIFICATION OUTPUT (PIN 4)						
V_O	output voltage	video not identified	–	–	0.5	V
Z_O	output impedance		–	25	–	kΩ
V_O	output voltage	video identified; colour signal available; f_{osc} = 3.5 MHz	–	6	–	V
		video identified; colour signal available/unavailable ;f_{osc} = 4.4 MHz	–	8	–	V
t_d	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms
I_4	maximum load current at pin 4		–	–	25	μA
Sound circuit						
DEMODULATOR INPUT; NOTE 16 (PIN 5)						
$V_{5(rms)}$	input limiting for PLL catching range (RMS value)		–	1	2	mV
Δf	catching range PLL	note 17	4.2	–	6.8	MHz
R_I	DC input resistance	note 3	100	–	–	kΩ
C_I	input capacitance	note 3	–	15	–	pF
AMR	AM rejection	V_I = 50 mV RMS; note 18	60	66	–	dB
DE-EMPHASIS (PIN 1)						
$V_{O(rms)}$	output signal amplitude (RMS value)	note 17	–	350	–	mV
R_O	output resistance		–	15	–	kΩ
V_1	DC output voltage		–	3	–	V
AUDIO ATTENUATOR OUTPUT (PIN 50)						
$V_{50(rms)}$	controlled output signal amplitude (RMS value)	–6 dB; note 17	500	700	900	mV
R_O	output resistance		–	250	–	Ω
V_{50}	DC output voltage		–	3.3	–	V
THD	total harmonic distortion	note 19	–	–	0.5	%
S/N_{int}	internal signal-to-noise ratio	note 7	–	60	–	dB
S/N_{ext}	external signal-to-noise ratio	note 7	–	80	–	dB
VOL_{cr}	control range	see also Fig.5	–	80	–	dB
OSS	suppression of output signal when mute is active		–	80	–	dB
ΔV_{50}	DC shift of the output when mute is active	note 20	–	10	50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EXTERNAL AUDIO INPUT (TDA8361, TDA8362); NOTE 21 (PIN 6)						
$V_{6(rms)}$	input signal amplitude (RMS value)		–	350	700	mV
R_I	input resistance		–	25	–	kΩ
ΔG_V	voltage gain difference between input and output	maximum volume	–	12	–	dB
α_{cr}	crosstalk between internal and external audio signals		60	–	–	dB
CVBS/On-Screen Display and CD inputs						
INTERNAL AND EXTERNAL CVBS INPUTS (PINS 13 AND 15)						
$V_{13(p-p)}$	internal CVBS input voltage (peak-to-peak value)	notes 3 and 22	–	2	2.8	V
I_{13}	internal CVBS input current		–	4	–	μA
$V_{15(p-p)}$	external CVBS input voltage; TDA8361, TDA8362 (peak-to-peak value)	note 3	–	1	1.4	V
I_{15}	external CVBS input current; TDA8361, TDA8362		–	4	–	μA
ISS	suppression of non-selected CVBS input signal; TDA8361, TDA8362	note 23	50	–	–	dB
COMBINED CHROMINANCE AND SWITCH INPUT (TDA8361, TDA8362; PIN 16)						
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	notes 3 and 24	–	0.3	–	V
$V_{16(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 7	1	–	–	V
R_I	chrominance input resistance		–	15	–	kΩ
C_I	chrominance input capacitance	note 3	–	–	5	pF
V_{16}	DC input voltage to switch the A/V switch to internal mode		–	–	0.5	V
V_{16}	DC input voltage to switch the A/V switch to external mode		$V_P - 0.5$	–	–	V
V_{16}	DC input voltage for chrominance insertion		3	4	5	V
SS_{CVBS}	suppression of non-selected chrominance signal from CVBS input	notes 7 and 23	50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB INPUTS FOR ON-SCREEN DISPLAY (PINS 22, 23 AND 24)						
$V_{22,23,24(p-p)}$	input signal amplitude for an output signal of 4V (black-to-white) (peak-to-peak value)	note 25	–	0.7	0.8	V
$V_{22,23,24(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)		1	–	–	V
V_{diff}	difference of black level of internal and external signals at the outputs		–	–	100	mV
$I_{22,23,24}$	input currents		–	0.1	–	µA
FAST BLANKING (PIN 21)						
V_I	fast blanking input voltage	no data insertion	–	–	0.4	V
V_I	fast blanking input voltage	data insertion	0.9	–	–	V
$V_{21(max)}$	maximum input pulse	data insertion	–	–	3	V
t_d	delay of data insertion		–	–	20	ns
I_{21}	input current		–	0.2	–	mA
SS_{int}	suppression of internal RGB signals with data insertion at f = 0 to 5 MHz	note 23	46	–	–	dB
SS_{ext}	suppression of external RGB signals with data insertion at f = 0 to 5 MHz	note 23	46	–	–	dB
V_I	input voltage to blank the RGB outputs to facilitate 'On-Screen-Display' signals being applied to these outputs	note 26	4	–	–	V
t_d	delay between the input pulse and the blanking at the output	note 7	–	30	–	ns
COLOUR DIFFERENCE INPUT SIGNALS (PINS 28 AND 29)						
$V_{29(p-p)}$	input signal amplitude (R–Y) (peak-to-peak value)		–	1.05	–	V
$V_{28(p-p)}$	input signal amplitude (B–Y) (peak-to-peak value)		–	1.35	–	V
$I_{28,29}$	input current for both inputs		–	0.1	1.0	µA
Chrominance filters						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{SC}	–	MHz
QF	trap quality factor	notes 7 and 27	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BANDPASS CIRCUIT						
f_c	centre frequency		–	f_{SC}	–	MHz
QBP	bandpass quality factor	note 7	–	3	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delay line and peaking circuit						
Y DELAY LINE						
t_d	delay time	note 7	–	480	–	ns
B	bandwidth of internal delay line	note 7	8	–	–	MHz
PEAKING CONTROL; NOTE 28, SEE ALSO FIG.6 (PIN 14)						
t_W	width of preshoot or overshoot	at 50% of pulse; note 7	–	160	–	ns
S_{cth}	peaking signal compression threshold		–	50	–	IRE
I_{14}	input current when no video input signal present		–	1	–	mA
V_I	voltage level to switch off peaking		–	7	–	V
Horizontal and vertical synchronization circuits						
SYNC VIDEO INPUT (TDA8361, TDA8362; PINS 13 AND 15)						
V_{13}	sync pulse amplitude	referenced to pin 15; note 3	50	300	–	mV
SL	slicing level	note 29	–	50	–	%
VERTICAL SYNC						
t_W	width of the vertical sync pulse without sync instability	note 30	22	–	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency	note 44	–	15625	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8 V ±10%; note 7	–	0.2	0.5	%
$\Delta f_{osc}/\Delta T$	frequency variation with temperature	T_{amb} = 25 °C ±50 °C; note 7	–	1	–	Hz/K
$\Delta f_{osc(max)}$	maximum frequency deviation at the start of the horizontal output		–	–	75	%
FIRST CONTROL LOOP; NOTE 31 (FILTER CONNECTED TO PIN 40)						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL	note 7	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
HYS	hysteresis at the switching point		–	3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECOND CONTROL LOOP; NOTE 32 (CAPACITOR CONNECTED TO PIN 39)						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity	without R_L on pin 39	–	150	–	µs/µs
t_{cr}	control range from start of horizontal output to flyback		11	12	–	µs
t_{shift}	maximum horizontal shift range	note 7	±2	–	–	µs
$\Delta\varphi_i/\Delta\varphi_o$	shift control sensitivity	note 7	–	3	–	µA/µs
V_{39}	voltage to switch on the X-ray protection		6	–	–	V
I_I	input current during protection		–	–	tbf	µA
HORIZONTAL OUTPUT (PIN 37)						
V_{OL}	LOW level output voltage	I_O = 10 mA	–	–	0.3	V
$I_{O(max)}$	maximum allowed output current		10	–	–	mA
$V_{O(max)}$	maximum allowed output voltage		–	–	V_P	V
δ_{df}	duty factor	note 7	–	50	–	%
FLYBACK INPUT/SANDCASTLE OUTPUT (PIN 38)						
I_{38}	required input current during flyback pulse	note 7	100	–	300	µA
V_O	output voltage during burst key		4.8	5.3	5.8	V
V_O	output voltage during blanking		1.8	2.0	2.2	V
V_{Icl}	clamped input voltage during flyback		2.6	3.0	3.4	V
t_W	burst key pulse width		3.3	3.5	3.7	µs
t_W	vertical blanking pulse width	note 33	–	14	–	lines
t_d	delay of start of burst key to start of sync		5.2	5.4	5.6	µs
VERTICAL SECTION; NOTE 34						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	
	locking range (lines/frame)		488	–	722	
VERTICAL RAMP GENERATOR (PIN 42)						
I_{42}	input current during scan	note 7	–	–	2	µA
I_{dis}	discharge current during retrace		–	0.3	–	mA
$V_{saw(p-p)}$	sawtooth amplitude (peak-to-peak value)	in 50 Hz mode	–	1.5	1.8	V
t_d	delay from field-to-field		–	–	1.6	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL OUTPUT (PIN 43)						
I_O	available output current	note 7	1	–	–	mA
I_{int}	internal bias current of NPN emitter follower		–	0.2	–	mA
$V_{O(max)}$	maximum available output voltage		4	–	–	V
$V_{O(min)}$	minimum available output voltage		–	–	0.3	V
VERTICAL FEEDBACK INPUT (PIN 41)						
V_{41}	DC input voltage		2.0	2.5	3.0	V
V_{41}	AC input voltage		–	1	–	V
I_{41}	input current		–	–	15	μA
Δt_p	internal pre-correction to sawtooth	note 35	–	3	–	%
$\Delta T/\Delta V$	temperature dependency on amplitude	ΔT = 40 °C	–	–	1	%
V_{GL}	vertical guard switching level with respect to the DC feedback level; switching level LOW		–	–	−1.5	V
V_{GH}	vertical guard switching level with respect to the DC feedback level; switching level HIGH		–	–	+1.5	V
t_d	delay of scan start	power on at 60 Hz	–	140	–	ms
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 36	26	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		−30	–	−38	dB
HYS_{off}	hysteresis colour killer OFF	note 7				
	strong input signal	S/N ≥ 40 dB	–	+3	–	dB
	noisy input signal		–	+1	–	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	
REFERENCE PART						
Phase-locked loop; note 37						
f_{CR}	catching range		300	–	–	Hz
$\Delta\varphi$	phase shift for a ±200 Hz deviation of the oscillator frequency	note 7	–	–	2	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
TC_{osc}	temperature coefficient of f_{osc}	note 7	–	2.0	2.5	Hz/K
Δf_{osc}	f_{osc} deviation with respect to V_P	note 7; V_P = 8 V ±10%	–	–	250	Hz
R_I	input resistance (pin 34)	f_i = 3.58 MHz; note 4	–	1.5	–	kΩ
R_I	input resistance (pin 35)	f_i = 4.43 MHz; note 4	–	1	–	kΩ
C_I	input capacitance (pins 34 and 35)	note 4	–	–	10	pF
R	required resistance to V_P to force the oscillator into one crystal mode		–	47	–	kΩ
HUE CONTROL AND CHROMINANCE OUTPUT (TDA8361, TDA8362); NOTE 38 (PIN 27)						
HUE_{cr}	hue control range	see also Fig.7	±45	±60	–	deg
ΔHUE	hue variation for ±10% V_P	note 7	–	0	5	deg
ΔHUE/ΔT	hue variation with temperature	T_{amb} = 0 to +7 °C; note 7	–	0	–	deg
R	value of resistor connected to V_P to switch the PAL decoder and to obtain a chrominance input signal for the TDA8395 (TDA8362)		4.7	10	12	kΩ
$V_{O(p-p)}$	chrominance output signal to the TDA8395 (peak-to-peak value)	nominal output signal	–	330	–	mV
DEMODULATORS						
$V_{30(p-p)}$	(R–Y) output signal amplitude (peak-to-peak value)	note 39	–	0.525	–	V
$V_{31(p-p)}$	(B–Y) output signal amplitude (peak-to-peak value)	note 39	–	0.675	–	V
G	gain ratio of both demodulators G(B–Y)/G(R–Y)		1.6	1.78	1.96	
	spread of signal amplitude ratio PAL/NTSC	note 7	–1	–	+1	dB
Z_O	output impedance (R–Y)/(B–Y) output		–	250	–	Ω
B	bandwidth of demodulators	–3 dB; note 40	–	650	–	kHz
$V_{30,31(p-p)}$	residual carrier output voltage (peak-to-peak value)	f = f_{osc}				
	(R–Y) output		–	–	10	mV
	(B–Y) output		–	–	10	mV
$V_{30,31(p-p)}$	residual carrier output voltage (peak-to-peak value)	f = $2f_{osc}$				
	(R–Y) output		–	–	10	mV
	(B–Y) output		–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATORS						
$V_{30(p-p)}$	H/2 ripple at (R–Y) output (peak-to-peak value)	only burst fed to input	–	–	25	mV
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature	note 7	–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage	note 7	–	–	±0.1	dB
φ_e	phase error in the demodulated signals		–	–	5	deg
COLOUR DIFFERENCE MATRIXES IN CONTROL CIRCUIT						
G–Y/–(R–Y)	PAL/SECAM mode with TDA8362/TDA8395	–(R–Y) and –(B–Y) not affected	–	–0.51 ±10%	–	
G–Y/–(B–Y)			–	–0.19 ±25%	–	
–(B–Y)	NTSC mode; the CD matrix results in the following signal (1.14/–10°)	nominal hue setting	$-1.12U_R - 1.12V_R$			
–(R–Y)	NTSC mode; the CD matrix results in the following signal (1.14/100°)	nominal hue setting	$-0.20U_R + 1.12V_R$			
G–Y	NTSC mode; the CD matrix results in the following signal (0.30/235°)	nominal hue setting	$-0.25V_R - 0.17U_R$			
REFERENCE SIGNAL OUTPUT FOR TDA8395 (TDA8362; PIN 32)						
f_{ref}	reference frequency	note 41	–	4.43	–	MHz
$V_{32(p-p)}$	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_O	output voltage level	PAL/NTSC identified	–	1.5	–	V
V_O	output voltage level	no PAL/NTSC; SECAM (by TDA8395) identified	–	5	–	V
I_{32}	required current to force TDA8362/TDA8395 combination in SECAM mode		150	–	–	µA
Control part						
SATURATION CONTROL; NOTE 25 (PIN 26)						
SAT_{cr}	saturation control range	see also Fig.8	52	–	–	dB
$\Delta SAT/\Delta V$	saturation level change	V_P = ±10%;note 7	–	0	–	%
I_I	input current	no colour identified	–	1	–	mA
V_{ctr}	control voltage to switch colour PLL in the free-running mode	note 37	$V_P - 1$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CONTRAST CONTROL; NOTE 25 (PIN 25)						
CON_{cr}	contrast control range	see also Fig.9	–	20	–	dB
	tracking between the three channels over a control range of 10 dB		–	–	0.7	dB
BRIGHTNESS CONTROL (PIN 17)						
BRI_{cr}	brightness control range	see also Fig.10	–	±1	–	V
RGB AMPLIFIERS (PINS 18, 19 AND 20)						
$V_{18,19,20(p-p)}$	output signal amplitudes (peak-to-peak value)	nominal luminance input signal and nominal contrast; note 25	3.5	4.0	4.5	V
$V_{20(p-p)}$	output signal amplitudes for the RED channel (peak-to-peak value)	nominal settings for contrast and saturation control and no luminance signal to the R–Y signal (PAL)	3.8	4.2	4.6	V
$V_{18,19,20}$	blanking level at the RGB outputs		0.5	0.6	0.8	V
$V_{18,19,20}$	black level at the RGB outputs	note 25	1.2	1.3	1.4	V
V_{pwl}	maximum peak white level	note 42	–	6	–	V
I_O	available output current		5	–	–	mA
Z_O	output impedance		–	150	–	Ω
I_{source}	current source of output stage		1.8	2.0	–	mA
	relative spread between the RGB output signals		–	–	5	%
S/N	signal-to-noise ratio of output signals	note 43				
	for RGB input	note 7	–	60	–	dB
	for CVBS input	note 7	50	56	–	dB
$f_{res(p-p)}$	residual frequency at f_{osc} in the RGB outputs (peak-to-peak value)	note 23	–	–	25	mV
$f_{res(p-p)}$	residual frequency at $2f_{osc}$ plus higher harmonics in the RGB outputs (peak-to-peak value)		–	–	25	mV
V_{diff}	difference in black level between the three outputs	nominal brightness	–	–	100	mV
V_{bl}	black level shift with picture content	note 7	–	0	–	mV
$\Delta bl/\Delta T$	variation of black level with temperature	note 7	–2	–	0	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIERS (PINS 18, 19 AND 20)						
$\Delta bl/\Delta CON$	variation of black level over contrast range	nominal saturation; note 7	–	–	100	mV
$\Delta bl/\Delta SAT$	variation of black level over saturation range	nominal contrast; note 7	–	–	50	mV
Δbl	relative variation in black level between the three channels during variations of					
	supply voltage (±10%)	nominal saturation	–	–	50	mV
	saturation (50 dB)	nominal contrast	–	–	25	mV
	contrast (20 dB)	nominal saturation	–	–	60	mV
	brightness (±0.5 V)	nominal controls	–	–	100	mV
V_{diff}	differential drift of black level over a temperature range of 40 °C	note 7	–	–	10	mV
B	bandwidth of output signals for	–3 dB				
	RGB input		8	–	–	MHz
	CVBS input	f_{osc} = 3.58 MHz	–	2.8	–	MHz
	CVBS input	f_{osc} = 4.43 MHz	–	3.5	–	MHz
	S-VHS input		8	–	–	MHz

Notes to the "Characteristics"

1. It is possible to start the horizontal oscillator when a current of 5.5 mA is supplied to this pin. In this condition the main part of the IC is not active and this results in the frequency of the oscillator not being controlled at the correct value. Consequently, the oscillator frequency will be higher than normal, the maximum deviation will be 75%. When the start-up function is used the maximum voltage on pin 36 must be limited to 8.8 volts.
2. On set AGC.
3. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
4. Measured at 10 mV RMS top sync input signal.
5. So called projected zero point, i.e. with switched demodulator.
6. Measured in accordance with the test line given in Fig.11. For the differential phase test the peak white setting is reduced to 87%.

   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

   The phase difference is defined as the difference in degrees between the largest and smallest phase angle.
7. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
8. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.12.
9. Insertion (suppression of the interference pulses) to a level of 2.6 V is active only during a strong input signal. This is because the noise inverter has a negative effect on the sound performance at a weak input signal.
10. The test set-up and input conditions are given in Fig.13. The figures are measured with an input signal of 10 mV RMS.

11. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_O \text{ (black-to-white)}}{V_{m\,(rms)} \text{ (B = 5 MHz)}}$$

12. To obtain a good noise immunity of the AGC circuit the AGC detector is gated during the sync pulse. This gating is switched off during the vertical retrace to avoid disturbances of the signal amplitude due to phase errors of the incoming video signal which are caused by the head-switching of VCRs.
13. When the leakage current of the capacitor exceeds this value it will result in a reduced performance of the AGC (amplitude variation during line or frame) but it will not result in a hang-up situation.
14. The AFC slope is directly related to the Q-factor of the demodulator tuned circuit. The given AFC steepness is obtained with a Q-factor of 60. When a lower steepness is required this can be obtained by connecting an external resistor to the AFC output (the output impedance is 50 kΩ). The AFC off-set is tested with a double sideband input signal and with the reference tuned circuit tuned to minimum AGC voltage (optimum tuning for the demodulator).
15. For positive modulated signals the FM sound demodulator for the sound is not required. This is because the sound signal is amplitude modulated. Therefore the TDA8362 can be switched to positive modulation via the de-emphasis pin (pin 1). When switched to positive modulation the audio switch is set to 'external' so that the demodulated audio signal can be supplied to the input. The option between AM sound and SCART audio signals is achieved by means of an external switch.
16. The sound IF input is combined with the AF volume control. The IF signal is internally AC coupled to the limiter amplifier. The volume control voltage must be supplied to this pin via a resistor.
17. V_I = 100 mV RMS; FM: 1 kHz, $\Delta f = \pm 50$ kHz.
18. V_I = 50 mV RMS, f = 4.5/5.5 MHz;
    FM: 70 Hz ±50 kHz deviation
    AM: 1 kHz at 30% modulation.
19. V_I = 100 mV RMS, 5.5 MHz; FM: 1 kHz, ±17.5 kHz deviation; 15 kHz bandwidth; audio attenuator at −6 dB.
20. Audio attenuator at −20 dB; temperature range 10 to 50 °C.
21. In the TDA8361 and TDA8362 the audio and CVBS switches are controlled via the chrominance input pin. Table 1 lists the various possibilities.

    When the DC voltage has a value between 3 and 5 V the switches are set to the S-VHS position. The chrominance trap is then switched off and separate Y and chrominance signals have to be applied to the inputs (the audio switch is set to external in this condition). The audio switch is also set to external when the IF amplifier is switched to positive modulation (see also note 15).
22. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
23. This parameter is measured at nominal settings of the various control voltages.
24. Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
25. Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation as maximum −12 dB. The nominal brightness control voltage is 2.5 V.
26. When the data blanking input pulse exceeds a level of 4 V the RGB outputs are blanked. In this condition it is possible to supply 'On-Screen-Display' signals to the outputs. This blanking overrules both the internal and external RGB signals.
27. The −3 dB bandwidth of the circuit can be calculated by means of the following equation:

$$f_{-3\,dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

28. The amplitude response curve can be expressed as follows:

    $A(f) = 1 + K1 - \cos(180 \times f/3.1\ MHz)$

    and is realised with a transversal peaking filter having delay sections of 160 ns each. In the 'neutral' setting $K = 0$ and in the minimum setting $K = -0.5$.

    The peaking signal amplifier is linear for 250 ns step input signals up to 50 IRE units. For higher amplitudes the marginal gain is reduced. When the horizontal PLL is not synchronized (no signal present at the video input) the peaking control voltage is pulled down by means of an internal current. This information can be used to detect whether an input signal is available.

29. Slicing level independent of sync pulse amplitude.

30. The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization. The value given is the delay caused by the vertical sync pulse integrator. The integrator has been designed such that the vertical sync is not disturbed for special anti-copy tapes with vertical sync pulses with an on/off time of 10/22 µs.

31. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when excessive noise is present in the signal (only when the internal video signal is selected, when the video switch is in the external mode the time constant is always 'fast'). In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible.

    When no video signal is received the time constant of the first loop is switched to 'very slow'. This ensures a stable OSD when the receiver is switched to a channel without transmitter.

    The output current of the phase detector for the various conditions is shown in Table 2.

32. Picture shift can be obtained by means of a variable external load on the second phase detector. The control range is ±2 µs; the required current for this phase shift is ±6 µA.

33. The vertical blanking pulse in the RGB outputs has a width of 22 or 17.5 lines (50 or 60 Hz system). The width of the vertical sync pulse in the sandcastle pulse is 14 lines. This is to prevent a phase distortion on top of the picture due to a timing modulation of the incoming flyback pulse.

34. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 2 search modes of operation:

    The 'large window' mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz)

    The 'narrow window' mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

35. This precorrection is intended to compensate for non-linearity of AC coupled vertical output stages. The value given indicates the amplitude of the correction waveform with respect to the sawtooth amplitude.

36. At a chrominance input voltage (related to CVBS2) of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and –20 dB.

37. All frequency variations are referenced to 3.58/4.43 MHz carrier frequency.
All oscillator specifications are measured with the Philips crystal series 9922 520.
If the spurious response of the 4.43 MHz crystal is lower than –3 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequency is guaranteed.
The spurious response of the 3.58 MHz crystal must be lower than –3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.

    The catching and detuning range are measured for nominal crystal parameters. These are:

    a) load resonance frequency f_0 (C_L = 20 pF) = 4.433619 or 3.579545 MHz

    b) motional capacitance C_M = 20.6 fF (4.43 MHz crystal) or (3.58 MHz crystal)

    c) parallel capacitance C_0 = 5.5 pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).

    The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.
    The free-running frequency of the oscillator can be checked by pulling the saturation control pin to the positive supply rail. In that condition the colour killer is not active so that the frequency off-set is visible on the screen. When two crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator continuously switching between the two frequencies.

38. In the TDA8362 the hue control pin has a double function. When the control voltage has a value of 0 to 5 V (normal control range) the hue can be controlled when NTSC signals are decoded. When this voltage is increased to a value greater than 5.5 V the decoder is forced to the PAL standard. When this pin is connected to the positive supply line via a 10 kΩ resistor the selected CVBS signal, of the CVBS switch, is available. This signal can be applied to the SECAM decoder TDA8395.
The phase shift of the hue control can be measured at the colour difference outputs (pins 30 and 31).

39. The –(R–Y) and –(B–Y) signals are demodulated with the 90° phase difference of the reference carrier and a gain ratio –(B–Y)/–(R–Y) = 1.78. The matrixing to the required signals is achieved in the control part.

40. This value indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the demodulator low-pass filter is approximately 1 MHz.

41. The reference signal for the TDA8395 is available only when the crystal oscillator is operating at a frequency of 4.43 MHz. When a SECAM signal is identified this signal is only available during the vertical retrace period thus avoiding crosstalk with the incoming SECAM signal during scan.

42. When one of the three output signals exceeds this level the gain of the amplifiers is reduced. This is achieved by a reduction of contrast and thus avoids clipping of the output signals. The discharge current at pin 25 is 0.2 mA. When the black level exceeds a value of 2 V the maximum peak-to-peak value of the video output signal will be less than 4 V (p-p); this is due to the operation of the peak-white limiter.

43. The signal-to-noise ratio is specified as a peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz). During the measurement the peaking control voltage is set to nominal.

44. The typical free running frequency is dependent on the crystal which is used for calibration. With 4.4 MHz the typical free running frequency is 15625, with 3.58 MHz the typical free running frequency is 15734.
Calibration during start-up is always carried out with a 4.4 MHz crystal if no forced mode is used.

Table 1 Audio and CVBS switch selection.

LEVEL (pin 16)	INTERNAL CVBS	EXTERNAL CVBS/Y	CHROMINANCE	CHROMINANCE TRAP	AUDIO
DC ≤ 0.5 V	ON	OFF	OFF	ON	internal
3 ≤ DC ≤ 5 V	OFF	ON (Y)	ON	OFF	external
DC ≥ 7.5 V	OFF	ON (CVBS)	OFF	ON	external

Table 2 Output current of phase detector.

CURRENT Φ1 DURING	SCAN (μA)	VERTICAL RETRACE (μA)	GATED YES/NO
Weak signal and synchronized	30	30	YES (5.7 μs)
Strong signal and synchronized	180	270	NO
Not synchronized	180	270	NO
No video identification	6	6	NO

QUALITY SPECIFICATION

Quality level in accordance with UZW B0/FQ-0601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	200	V
		100	200	pF
		1500	0	Ω

Note

1. All pins are protected against ESD by means of internal clamping diodes.

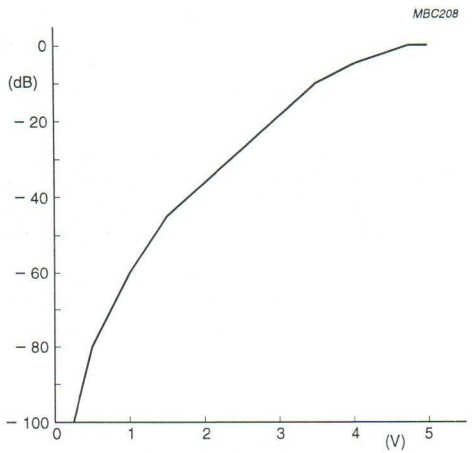


Fig.5 Volume control curve.

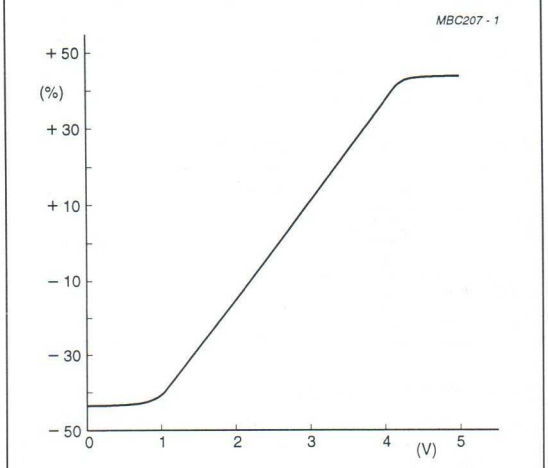


Fig.6 Peaking control curve.

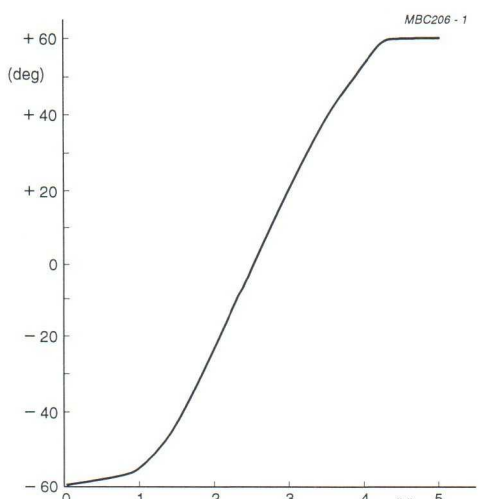


Fig.7 Hue control curve

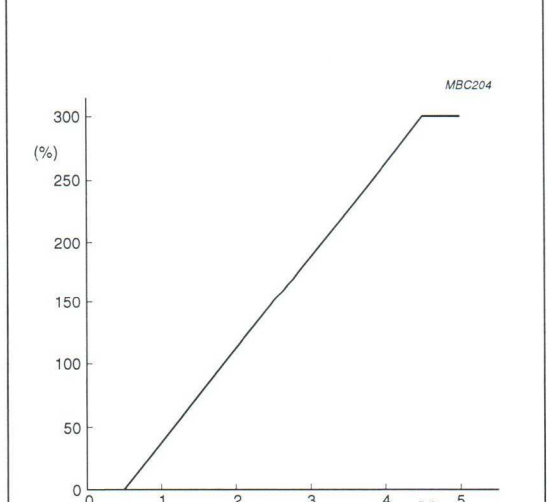


Fig.8 Saturation control curve.

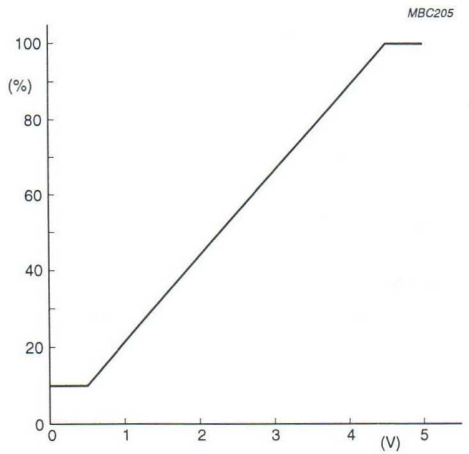


Fig.9 Contrast control curve.

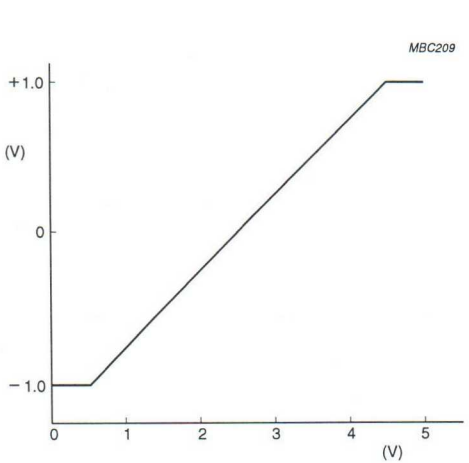


Fig.10 Brightness control curve.

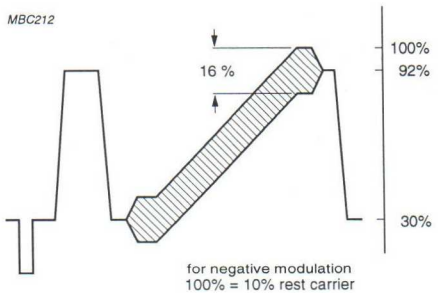


Fig.11 Video output signal.

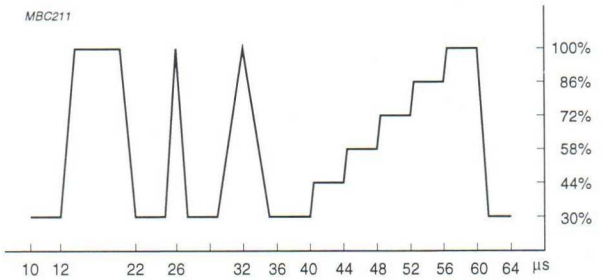
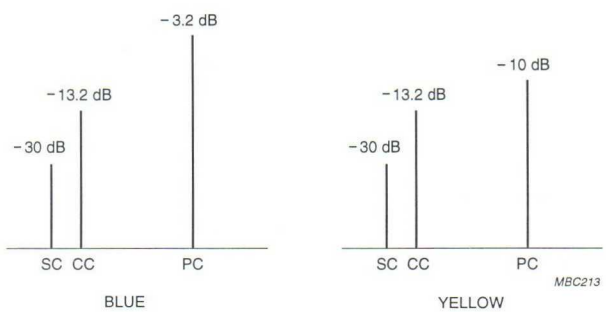
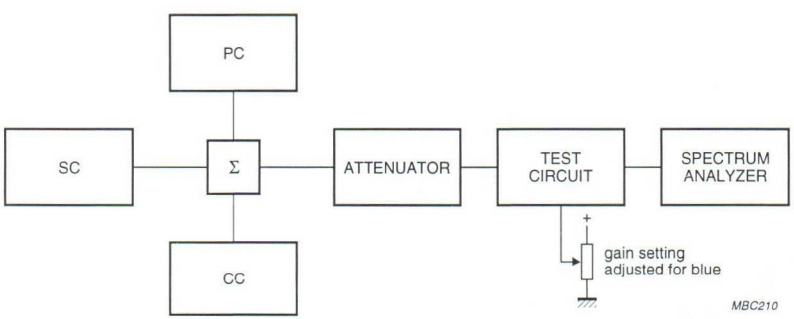


Fig.12 Test signal waveform.





Input signal conditions: SC = sound carrier; CC = colour carrier; PC = picture carrier.
All amplitudes with respect to top sync level.

$$\text{Value at 0.92 or 1.1 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 0.92 or 1.1 MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 2.66 or 3.3 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 2.66 or 3.3 MHz}}$$

Fig.13 Test set-up intermodulation.

I²C-bus controlled PAL/NTSC TV processor

TDA8366

FEATURES

- Multistandard vision IF circuit (positive and negative modulation)
- Video identification circuit in the IF circuit which is independent of the synchronization for stable On Screen Display (OSD) under 'no-signal' conditions
- Source selection with 2 Colour Video Blanking Synchronization (CVBS) inputs and a Y/C (or extra CVBS) input
- Output signals of the video switch circuit for the teletext decoder and a Picture-In-Picture (PIP) processor
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Asymmetrical peaking in the luminance channel with a (defeatable) noise coring function
- PAL/NTSC colour decoder with automatic search system
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- RGB control circuit with black-current stabilization and white point adjustment; to obtain a good grey scale tracking the black-current ratio of the 3 guns depends on the white point adjustment
- Linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Geometry correction by means of modulation of the vertical and EW drive
- I²C-bus control of various functions
- Low dissipation (850 mW)
- Small amount of peripheral components compared with competition ICs
- Only one adjustment (vision IF demodulator)
- Y, U and V inputs and outputs.

GENERAL DESCRIPTION

The TDA8366 is an I²C-bus controlled PAL/NTSC TV processor. The circuit has been designed for use with the baseband chrominance delay line TDA4665 and for DC-coupled vertical and East-West (EW) output stages.

The device can process both CVBS and Y/C input signals and has a linear RGB-input with fast blanking.

The peaking circuit generates asymmetrical overshoots (the amplitude of the 'black' overshoots is approximately 2 times higher as the one of the 'white' overshoots) and contains a (defeatable) coring function.

The RGB control circuit contains a black-current stabilizer circuit with internal clamp capacitors. The white point of the picture tube is adjusted via the I²C-bus.

The deflection control circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an East-West drive current for the East-West output stage.These signals can be manipulated for geometry correction of the picture.

The supply voltage for the IC is 8 V. The IC is available in an SDIP package with 52 pins and in a QFP package with 64 pins (see Chapter "Ordering information").

The pin numbers indicated in this document are referenced to the SDIP52; SOT247-1 package; unless otherwise indicated.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8366	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
TDA8366H	QFP64[1]	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current	–	100	–	mA
Input voltages					
$V_{46,47(rms)}$	video IF amplifier sensitivity (RMS value)	–	70	–	μV
$V_{15(p-p)}$	external CVBS input (peak-to-peak value)	–	1.0	–	V
$V_{9(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)	–	1.0	–	V
$V_{8(p-p)}$	S-VHS chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{21,22,23(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
Output signals					
$V_{o(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.5	–	V
I_{52}	tuner AGC output current range	0	–	5	mA
$V_{36(p-p)}$	TXT output voltage (peak-to-peak value)	–	1.0	–	V
$V_{13(p-p)}$	PIP output voltage (peak-to-peak value)	–	1.0	–	V
$V_{28(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	–	525	–	mV
$V_{27(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	–	675	–	mV
V_{26}	Y output voltage	–	450	–	mV
$V_{19,18,17(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{38}	horizontal output current	10	–	–	mA
$I_{44,45}$	vertical output current	1	–	–	mA
I_{43}	EW drive output current	0.5	–	–	mA

BLOCK DIAGRAM

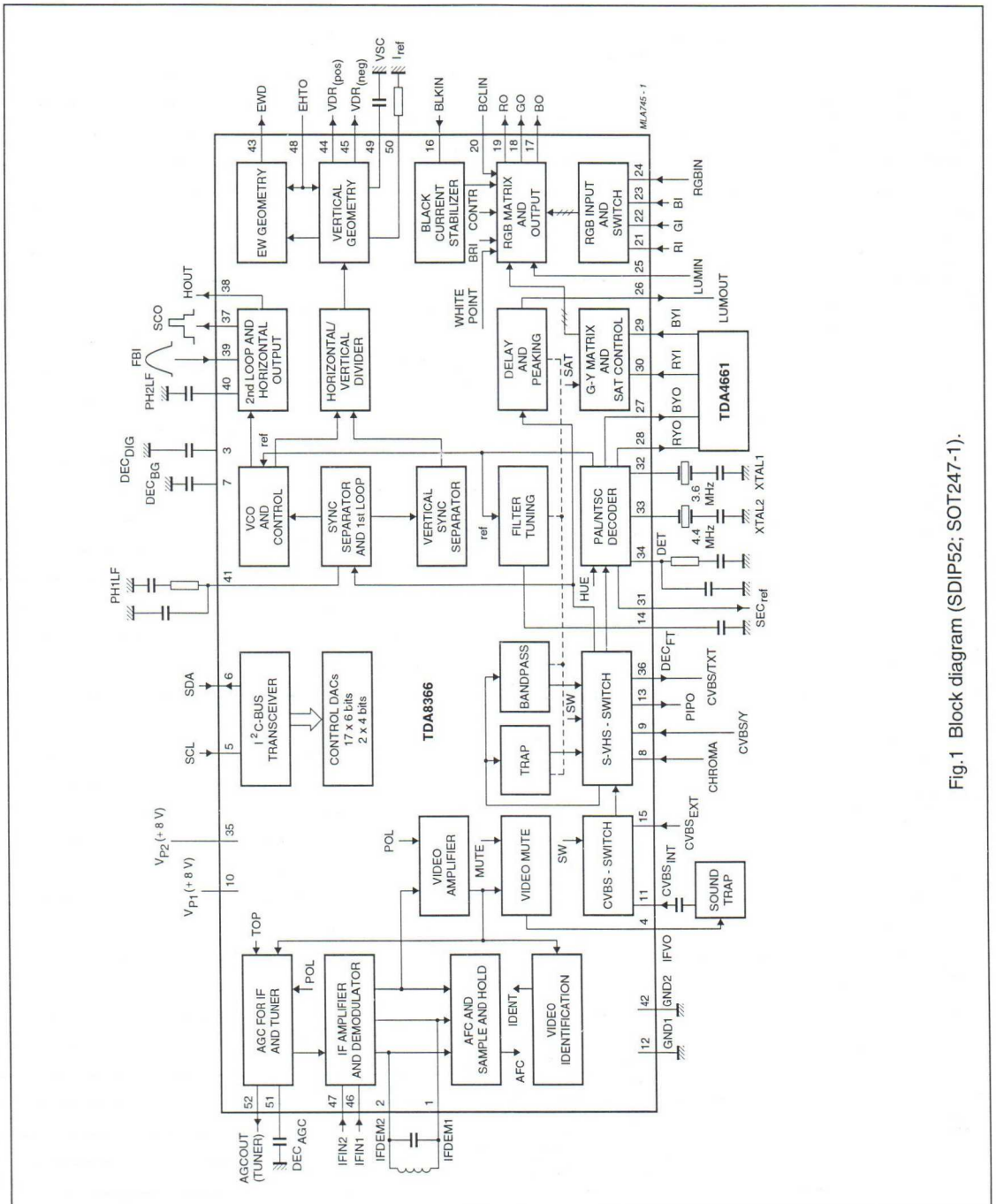


Fig.1 Block diagram (SDIP52; SOT247-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64	
IFDEM1	1	11	IF demodulator tuned circuit 1
IFDEM2	2	12	IF demodulator tuned circuit 2
DEC_{DIG}	3	13	decoupling digital supply
IFVO	4	14	IF video output
SCL	5	16	serial clock input
SDA	6	17	serial data input/output
DEC_{BG}	7	18	bandgap decoupling
CHROMA	8	20	chrominance input (S-VHS)
CVBS/Y	9	21	external CVBS/Y input
V_{P1}	10	22	main supply voltage 1 (+8 V)
$CVBS_{INT}$	11	29	internal CVBS input
GND1	12	25	ground 1
PIPO	13	27	picture-in-picture output
DEC_{FT}	14	28	decoupling filter tuning
$CVBS_{EXT}$	15	24	external CVBS input
BLKIN	16	30	black-current input
BO	17	31	blue output
GO	18	32	green output
RO	19	33	red output
BCLIN	20	35	beam current limiter input
RI	21	37	red input for insertion
GI	22	38	green input for insertion
BI	23	39	blue input for insertion
RGBIN	24	40	RGB insertion input
LUMIN	25	42	luminance input
LUMOUT	26	43	luminance output
BYO	27	44	(B–Y) signal output
RYO	28	45	(R–Y) signal output
BYI	29	46	(B–Y) signal input
RYI	30	47	(R–Y) signal input
SEC_{ref}	31	48	SECAM reference output
XTAL1	32	49	3.58 MHz crystal connection
XTAL2	33	50	4.43/3.58 MHz crystal connection
DET	34	52	loop filter phase detector
V_{P2}	35	54	horizontal oscillator supply voltage (+8 V)
CVBS/TXT	36	55	CVBS/TXT output
SCO	37	56	sandcastle output
HOUT	38	57	horizontal output

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64	
FBI	39	58	flyback input
PH2LF	40	59	phase-2 filter
PH1LF	41	60	phase-1 filter
GND2	42	26	ground 2
EWD	43	63	east-west drive output
$VDR_{(pos)}$	44	64	vertical drive 1 positive output
$VDR_{(neg)}$	45	1	vertical drive 2 negative output
IFIN1	46	2	IF input 1
IFIN2	47	3	IF input 2
EHTO	48	4	EHT/overvoltage protection input
VSC	49	5	vertical sawtooth capacitor
I_{ref}	50	6	reference current input
DEC_{AGC}	51	7	AGC decoupling capacitor
AGCOUT	52	8	tuner AGC output
n.c.	–	9	not connected
n.c.	–	10	not connected
n.c.	–	15	not connected
n.c.	–	19	not connected
n.c.	–	34	not connected
n.c.	–	36	not connected
n.c.	–	41	not connected
n.c.	–	51	not connected
n.c.	–	53	not connected
V_{P3}	–	23	supply voltage 3 (+8 V)
GND3	–	61	ground 3
GND4	–	62	ground 4

The pin numbers mentioned in the rest of this document are referenced to the SDIP52 (SOT247-1) package.

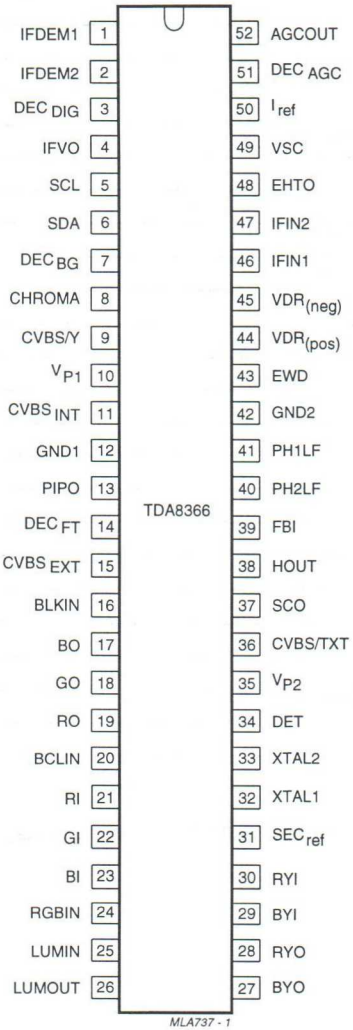


Fig.2 Pin configuration (SDIP52).

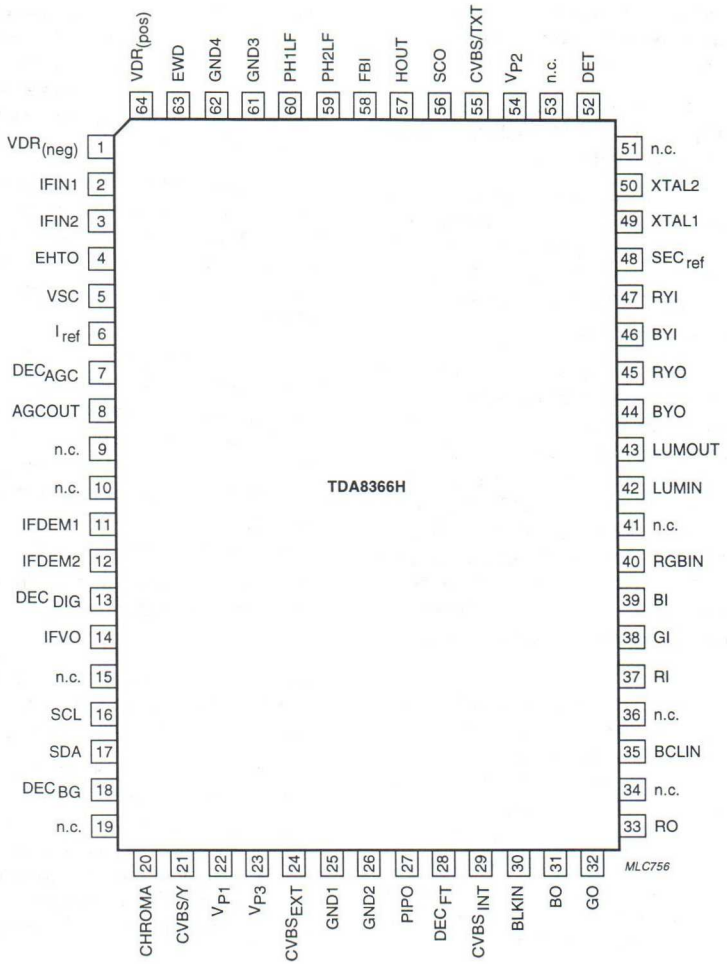


Fig.3 Pin configuration (QFP64).

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The IF-amplifier contains 3 AC-coupled control stages with a total gain control range which is in excess of 66 dB. The sensitivity of the circuit is comparable with that of modern IF-ICs. The reference carrier for the video demodulator is obtained by means of passive regeneration of the picture carrier. The external reference tuned circuit is the only remaining adjustment of the IC.

The polarity of the demodulator can be switched via the I²C-bus in such a way that the circuit is suitable for both positive and negative modulated signals.

The AFC-circuit is driven with the same reference signal as the video demodulator. To avoid that the video content disturbs the AFC operation a sample-and-hold circuit is applied for signals with negative modulation. The capacitor for this function is internal. The AFC information is supplied to the tuning system via the I²C-bus.

The AGC-detector operates on top-sync or top white-level depending on the polarity of the demodulator. The demodulation polarity is switched via the I²C-bus. The AGC detector time-constant capacitor is connected externally (this mainly because of the flexibility of the application). The time-constant of the AGC system during positive modulation is rather long to avoid visible variations of the signal amplitude. To obtain an acceptable speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 frame periods no action is detected the speed of the system is increased.

The circuit contains a video identification circuit which is independent of the synchronization circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. The identification output is supplied to the tuning system via the I²C-bus. The information of this identification circuit can also be used to switch the phase-1 (φ_1) loop to a low gain when no signal is received so that a stable OSD display is obtained. The coupling of the video identification circuit with the φ_1 loop can be switched on and off via the I²C-bus.

Synchronization circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is only used to detect whether the line oscillator is synchronized and not for transmitter identification. The first Phase-Locked Loop (PLL) has a very high-statical steepness so that the phase of the picture is independent of the line frequency.

The line oscillator is running at twice the line frequency. The oscillator capacitor is internal. Because of the spreads of internal components an automatic adjustment circuit has been added to the IC. It compares the oscillator frequency with that of the crystal oscillator in the colour decoder.

To protect the horizontal output transistor the horizontal drive is switched-off when a power-on-reset is detected. The frequency of the oscillator is calibrated again when all subaddress bytes have been sent. When the oscillator has the right frequency the calibration stops and the horizontal drive is switched-on again via the soft start procedure (standby bit in normal mode). When the IC is switched-on the same procedure is followed.

When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated.

The circuit has a second control loop to generate the drive pulses for the horizontal driver stage. During the start-up procedure the duty cycle of the horizontal output pulse increases from 0 to 50% in approximately 100 lines.

The vertical sawtooth generator drives the vertical output and EW correction drive circuits. The geometry processing circuits provide control of horizontal shift, EW width, EW parabola/width ratio, EW corner/parabola ratio, trapezium correction, vertical shift, vertical slope, vertical amplitude, and the S-correction. All these controls can be set via the I²C-bus. The geometry processor has a differential current

output for the vertical drive signal and a single-ended output for the EW drive. Both the vertical drive and the EW drive outputs can be modulated for EHT compensation. The EHT compensation pin is also used for overvoltage protection.

The geometry processor also offers the possibilities for vertical compression (for display of 16 : 9 pictures on a 4 : 3 screen) and vertical expansion (for display of 4 : 3 pictures on a 16 : 9 screen with full picture width, or for display of 'letter-box' transmissions on a 4 : 3 screen with full picture height). For the expand mode it is possible to shift the picture vertically (only one fixed position).

Also the de-interlace of the vertical output can be set via the I²C-bus.

To avoid damage of the picture tube when the vertical deflection fails the guard output current of the TDA8350 can be supplied to the sandcastle output. When a failure is detected the RGB-outputs are blanked and a bit is set (NDF) in the status byte of the I²C-bus. When no vertical deflection output stage is connected this guard circuit will also blank the output signals. This can be overruled by means of the EVG bit of subaddress 0A (see Table 1).

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The chrominance trap filter in the luminance path is designed for a symmetrical step response behaviour. The filters are realized by means of gyrator circuits and they are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realized by means of gyrator circuits.

It is possible to connect a Colour Transient Improvement (CTI) or Picture Signal Improvement (PSI) IC to the TDA8366. Therefore the luminance signal which has passed the filter and delay line circuit is externally available. The output signal of the transient improvement circuit must be supplied to the luminance input circuit. When the CTI function is not required the two pins must be AC-coupled.

Video switches

The circuit has two CVBS inputs and an Super-Video Home System (S-VHS) input. The input can be chosen by the I²C-bus. The input selector also has a position in which $CVBS_{EXT}$ is processed, unless there is a signal on the S-VHS input. When the input selector is in this position it switches to the S-VHS input if the S-VHS detector detects sync pulses on the S-VHS luminance input. The S-VHS detector output can be read by the I²C-bus. When the S-VHS option is not used the luminance input can be used as a second input for external CVBS signals. The choice is made via the CVS-bit (see Table 1).

The video switch circuit has two outputs which can be programmed in a different way. The input signal for the decoder is also available on the TXT output. Therefore this signal can be used to drive the teletext decoder and the SECAM add-on decoder. The signal on the PIP output can be chosen independent of the TXT output. If S-VHS is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a killer circuit and the colour difference demodulators. The 90° phase shift for the reference signal is made internally. The demodulation angle and gain ratio for the colour difference signals for PAL and NTSC are adapted to the standard.

The colour decoder is very flexible. Together with the SECAM decoder TDA8395 an automatic multistandard decoder can be designed.

Which standard the IC can decode depends on the external crystals. If a 4.4 MHz and a 3.5 MHz crystal are used PAL 4.4, NTSC 4.4, NTSC 3.5 and PAL 3.5 can be decoded. If two 3.5 MHz crystals are used PAL N and M can be decoded. If one crystal is connected only PAL/NTSC 4.4 or PAL/NTSC 3.5 can be decoded. The crystal frequency of the decoder is used to tune the line oscillator. Therefore the value of the crystal frequency must be given to the IC via the I²C-bus.

RGB output circuit and black-current stabilization

The colour-difference signals are matrixed with the luminance signal to obtain the RGB-signals. For the RGB-inputs linear amplifiers have been chosen so that the circuit is suited for signals coming from the SCART connector. The contrast and brightness control operate on internal and external signals.

The output signal has an amplitude of approximately 2 V black-to-white at nominal input signals and nominal settings of the controls.

The black current stabilization is realized by means of a feedback from the video output amplifiers to the RGB control circuit. The 'black current' of the 3 guns of the picture tube is internally measured and stabilized. The black level control is active during 4 lines at the end of the vertical blanking. During the first line the leakage current is measured and the following 3 lines the 3 guns are adjusted to the required level. The maximum acceptable leakage current is ±100 μA. The nominal value of the 'black current' is 10 μA. The ratio of the currents for the various guns automatically tracks with the white point adjustment so that the back-ground colour is the same as the adjusted white point.

The input impedance of the 'black-current' measuring pin is 15 kΩ. Therefore the beam current during scan will cause the input voltage to exceed the supply voltage. The internal protection will start conducting so that the excessive current is bypassed.

When the TV receiver is switched-on the black current stabilization circuit is not active, the RGB outputs are blanked and beam current limiting input pin is short-circuited. Only during the measuring lines will the outputs supply a voltage of 5 V to the video output stage so that it can be detected if the picture tube is warming up. These pulses are switched-on after a waiting time of approximately 0.5 s. This ensures that the vertical deflection is activated so that the measuring pulses are not visible on the screen. As soon as the current supplied to the measuring input exceeds a value of 190 μA the stabilization circuit is activated. After a waiting time of approximately 0.8 s the blanking and the beam current limiting input pin are released. The remaining switch-on behaviour of the picture is determined by the external time constant of the beam current limiting network.

I²C-BUS SPECIFICATION

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	0	1	X

MLA743

X = don't care.

Fig.4 Slave address (8A).

Valid subaddresses: 00 to 13; subaddress FE is reserved for test purposes. Auto-increment mode is available for subaddresses.

Start-up procedure

Read the status bytes until POR = 0 and send all subaddress bytes. The horizontal output signal is switched-on when the oscillator is calibrated. It is possible to have the horizontal output signal available before calibration. Then the SFM bit must be set to logic 0.

Each time before the data in the IC is refreshed, the status bytes must be read. If POR = 1, the procedure mentioned above must be carried out to restart the IC.

When this procedure is not followed the horizontal frequency may be incorrect after power-up or after a power dip.

Inputs

Table 1 Input status bits; note 1

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Source select	00	INA	INB	INC	IND	FOA	FOB	XA	XB
Decoder mode	01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	02	X	X	A5	A4	A3	A2	A1	A0
Horizontal shift (HS)	03	X	X	A5	A4	A3	A2	A1	A0
EW width (EW)	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width (PW)	05	X	X	A5	A4	A3	A2	A1	A0
EW corner parabola (CP)	06	X	X	A5	A4	A3	A2	A1	A0
EW trapezium (TC)	07	X	X	A5	A4	A3	A2	A1	A0
Vertical slope (VS)	08	NCIN	X	A5	A4	A3	A2	A1	A0
Vertical amplitude (VA)	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction (SC)	0A	HCO	EVG	A5	A4	A3	A2	A1	A0
Vertical shift (VSH)	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point R	0C	EXP	CL	A5	A4	A3	A2	A1	A0
White point G	0D	SFM	CVS	A5	A4	A3	A2	A1	A0
White point B	0E	MAT	PHL	A5	A4	A3	A2	A1	A0
Peaking	0F	YD3	YD2	YD1	YD0	A3	A2	A1	A0
Brightness	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	11	IE1	X	A5	A4	A3	A2	A1	A0
Contrast	12	AFW	IFS	A5	A4	A3	A2	A1	A0
AGC take-over	13	MOD	VSW	A5	A4	A3	A2	A1	A0

Note

1. X = don't care.

Table 2 Output status bits; note 1

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	STS	SL	XPR	CD2	CD1	CD0
	01	NDF	IN1	X	IFI	AFA	AFB	X	X

Note

1. X = don't care.

INPUT CONTROL BITS

Table 3 Source select 1

INA	INB	DECODER AND TXT
0	0	$CVBS_{INT}$
0	1	$CVBS_{EXT}$
1	0	S-VHS
1	1	S-VHS ($CVBS_{EXT}$)

Table 4 Source select 2

INC	IND	PIP
0	0	$CVBS_{INT}$
0	1	$CVBS_{EXT}$
1	0	S-VHS
1	1	S-VHS ($CVBS_{EXT}$)

Table 5 Phase 1 (φ_1) time constant

FOA	FOB[1]	MODE
0	0	normal
0	1	slow
1	X	fast

Note

1. X = don't care.

Table 6 Crystal indication

XA	XB	CRYSTAL
0	0	two 3.6 MHz
0	1	one 3.6 MHz (pin 32)
1	0	one 4.4 MHz (pin 33)
1	1	3.6 MHz (pin 32) and 4.4 MHz (pin 33)

Table 7 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not synchronized)
0	1	60 Hz; note 1
1	0	50 Hz; note 1
1	1	auto (50 Hz when line not synchronized)

Note

1. When the forced mode is selected the divider will only switch to that position when the horizontal oscillator is not synchronized.

Table 8 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 9 Standby

STB	MODE
0	standby
1	normal

Table 10 Synchronization mode

POC	MODE
0	active
1	not active

Table 11 Colour decoder mode

CM2	CM1	CM0	DECODER MODE
0	0	0	not forced, own intelligence
0	0	1	forced NTSC 3.6 MHz
0	1	0	forced PAL 4.4 MHz
0	1	1	forced SECAM
1	0	0	forced NTSC 4.4 MHz
1	0	1	forced PAL 3.6 MHz (pin 32)
1	1	0	forced PAL 3.6 MHz (pin 33)
1	1	1	no function

Table 12 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 13 Video ident mode

VID	VIDEO IDENT MODE
0	φ_1 loop switched on and off
1	not active

Table 14 Long blanking mode

LBM	BLANKING MODE
0	adapted to standard (50 or 60 Hz)
1	fixed in accordance with 50 Hz standard

Table 15 EHT tracking mode

HCO	TRACKING MODE
0	EHT tracking only on vertical
1	EHT tracking on vertical and EW

Table 16 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 17 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 18 Overvoltage input mode

PRD	OVERVOLTAGE MODE
0	detection mode
1	protection mode

Table 19 Vertical deflection mode

EXP	CL	VERTICAL DEFLECTION MODE
0	0	normal
0	1	compress
1	0	expand
1	1	expand and lift

Table 20 Horizontal frequency during switch-on

SFM	START-UP FREQUENCY
0	maximum
1	nominal

Table 21 Condition Y/C input

CVS	Y-INPUT MODE
0	switched to Y/C mode
1	switched to CVBS mode

Table 22 PAL/NTSC matrix

MAT	MATRIX
0	adapted to standard
1	PAL

Table 23 Colour crystal PLL

PHL	STATE
0	PLL closed
1	oscillator free-running

Table 24 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	YD3 * 160 ns +
YD2	YD2 * 80 ns +
YD1	YD1 * 40 ns +
YD0	YD0 * 40 ns

Note

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

Table 25 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 26 Noise coring (peaking)

COR	NOISE CORING
0	off
1	on

Table 27 Enable fast blanking

IE1	FAST BLANKING
0	not active
1	active

Table 28 AFC window

AFW	AFC WINDOW
0	normal
1	enlarged

Table 29 IF sensitivity

IFS	IF SENSITIVITY
0	normal
1	reduced

Table 30 Modulation standard

MOD	MODULATION
0	negative
1	positive

Table 31 Video mute

VSW	STATE
0	normal operation
1	IF-video signal switched off

OUTPUT CONTROL BITS

Table 32 Power-on-reset

POR	MODE
0	normal
1	power-down

Table 33 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 34 S-VHS status

STS	S-VHS INPUT
0	no signal
1	signal

Table 35 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 36 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 37 Colour decoder mode

CD2	CD1	CD0	STANDARD
0	0	0	no colour standard identified
0	0	1	NTSC 3.6 MHz
0	1	0	PAL 4.4 MHz
0	1	1	SECAM
1	0	0	NTSC 4.4 MHz
1	0	1	PAL 3.6 MHz (pin 32)
1	1	0	PAL 3.6 MHz (pin 33)
1	1	1	spare

Table 38 Output vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 39 Indication RGB insertion

IN1	RGB INSERTION
0	no (pin 24 LOW)
1	yes (pin 24 HIGH)

Table 40 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 41 AFC output

AFA	AFB	CONDITION
0	0	outside window; too low
0	1	outside window; too high
1	0	in window; below reference
1	1	in window; above reference

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	operating junction temperature		–	150	°C
V_{es}	electrostatic handling	HBM; all pins; notes 1 and 2	–2000	+2000	V
		MM; all pins; notes 1 and 3	–200	+200	V

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Machine Model (MM): R = 0 Ω; C = 200 pF.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP52	40	K/W
	QFP64	50	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

Latch-up

- $I_{trigger} \geq 100$ mA or $\geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100$ mA or $\leq -0.5V_{DD(max)}$.

Following pins do not meet the above specification:

Pin 7: –90 mA

Pin 17: 90 mA

Pin 18: 90 mA

Pin 19: 90 mA

Pin 24: –90 mA

Pin 34: 60 mA

Pin 49: –90 mA

Pin 50: ±90 mA.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY (PIN 10)						
V_{P1}	supply voltage		7.2	8.0	8.8	V
I_{P1}	supply current		–	100	–	mA
P_{tot}	total power dissipation		–	850	–	W
HORIZONTAL OSCILLATOR SUPPLY (PIN 35)						
V_{P2}	supply voltage		7.2	8.0	8.8	V
I_{P2}	supply current		–	6	–	mA
IF circuit						
VISION IF AMPLIFIER INPUTS (PINS 46 AND 47)						
$V_{i(rms)}$	input sensitivity (RMS value)	note 1				
		f_i = 38.90 MHz	–	70	100	μV
		f_i = 45.75 MHz	–	70	100	μV
		f_i = 58.75 MHz	–	70	100	μV
R_I	input resistance (differential)	note 2	–	2	–	kΩ
C_I	input capacitance (differential)	note 2	–	3	–	pF
G_{cr}	gain control range		64	–	–	dB
$V_{i\ max(rms)}$	maximum input signal (RMS value)		100	150	–	mV
VIDEO AMPLIFIER OUTPUT (PIN 4); note 3						
V_o	zero signal output level	negative modulation; note 4	–	4.7	–	V
		positive modulation; note 4	–	2.0	–	V
V_4	top sync level	negative modulation	1.9	2.0	2.1	V
V_4	white level	positive modulation	–	4.5	–	V
ΔV_4	difference in amplitude between negative and positive modulation		–	0	15	%
Z_o	video output impedance		–	50	–	Ω
I_{bias}	internal bias current of NPN emitter follower output transistor		1.0	–	–	mA
$I_{source(max)}$	maximum source current		–	–	5	mA
B	bandwidth of demodulated output signal	at –3 dB	6	9	–	MHz
G_{diff}	differential gain	note 5	–	2	5	%
φ_{diff}	differential phase	notes 5 and 6	–	–	5	deg
NL_{vid}	video non-linearity	note 7	–	–	5	%
V_{th}	white spot threshold level		–	5.0	–	V
V_{ins}	white spot insertion level		–	3.3	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER OUTPUT (CONTINUED)						
N_{clamp}	noise inverter clamping level		–	1.4	–	V
N_{ins}	noise inverter insertion level (identical to black level)		–	2.6	–	V
δ_{mod}	intermodulation	notes 6 and 8				
	blue	V_o = 0.92 or 1.1 MHz	60	66	–	dB
		V_o = 2.66 or 3.3 MHz	60	66	–	dB
	yellow	V_o = 0.92 or 1.1 MHz	56	62	–	dB
		V_o = 2.66 or 3.3 MHz	60	66	–	dB
S/N	signal-to-noise ratio	notes 6 and 9				
		V_i = 10 mV	52	60	–	dB
		end of control range	52	61	–	dB
V_4	residual carrier signal	note 6	–	5.5	–	mV
V_4	residual 2nd harmonic of carrier signal	note 6	–	2.5	–	mV
IF AND TUNER AGC; note 10						
timing of IF-AGC with a 2.2 µF capacitor (pin 51)						
	modulated video interference	30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
t_{inc}	response time to an IF input signal amplitude increase of 52 dB	positive and negative modulation	–	2	–	ms
t_{dec}	response to an IF input signal amplitude decrease of 52 dB	negative modulation	–	50	–	ms
		positive modulation	–	100	–	ms
I_L	allowed leakage current of the AGC capacitor	negative modulation	–	–	10	µA
		positive modulation	–	–	200	nA
Tuner take-over adjustment (via I²C-bus)						
$V_{51min(rms)}$	minimum starting level for tuner take-over (RMS value)		–	0.4	0.8	mV
$V_{51max(rms)}$	maximum starting level for tuner take-over (RMS value)		40	80	–	mV
Tuner control output (pin 52)						
V_{52max}	maximum tuner AGC output voltage	maximum tuner gain; note 2	–	–	V_P + 1	V
$V_{52(sat)}$	output saturation voltage	minimum tuner gain; I_{47} = 2 mA	–	–	300	mV
I_{52max}	maximum tuner AGC output swing		5	–	–	mA
I_L	leakage current RF AGC		–	–	1	µA
ΔV_i	input signal variation for complete tuner control		0.5	2	4	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC OUTPUT (VIA I²C-BUS); note 11						
RES	AFC resolution		–	2	–	bits
W_{sen}	window sensitivity		65	80	100	kHz
W_{senL}	window sensitivity in large window mode		195	240	300	kHz
f_{os}	AFC offset	note 6	–	–	50	kHz
VIDEO IDENTIFICATION OUTPUT (VIA I²C-BUS)						
t_d	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms
CVBS and S-VHS input switch						
INTERNAL AND EXTERNAL CVBS INPUTS (PINS 11 AND 15)						
$V_{11(p-p)}$	CVBS input voltage (peak-to-peak value)	note 12	–	1.0	1.4	V
I_{11}	CVBS input current		–	4	–	µA
SS_{CVBS}	suppression of non-selected CVBS input signal	notes 6 and 13	50	–	–	dB
S-VHS INPUT (PINS 8 AND 9)						
$V_{9(p-p)}$	luminance input voltage (peak-to-peak value)		–	1.0	1.4	V
$I_{9(p-p)}$	luminance input current		–	4	–	µA
V_8	chrominance input voltage (burst amplitude)	note 14	–	0.3	0.45	V
I_8	chrominance input current		–	4	–	µA
TXT AND PIP OUTPUT SIGNALS (PINS 36 AND 13)						
$V_{o(p-p)}$	output signal amplitude (peak-to-peak value)		–	1.0	–	V
Z_o	output impedance		–	–	250	Ω
V_{TS}	top sync level		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB inputs, colour difference inputs, luminance inputs and outputs						
RGB INPUTS (PINS 21, 22 AND 23)						
$V_{21,22,23(p-p)}$	input signal amplitude for an output signal of 2 V (black-to-white) (peak-to-peak value)	note 15	–	0.7	0.8	V
$V_{21,22,23(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 6	1.0	–	–	V
ΔV_o	difference between black level of internal and external signals at the outputs		–	–	20	mV
$I_{21,22,23}$	input currents	no clamping; note 2	–	–	0.5	µA
Δt_d	delay difference for the three channels	note 6	–	0	20	ns
FAST BLANKING (PIN 24)						
V_i	input voltage	no data insertion	–	–	0.4	V
		data insertion	0.9	–	–	V
$V_{24(max)}$	maximum input pulse	insertion	–	–	3.0	V
t_d	delay time from RGB in to RGB out	data insertion; note 6	–	100	–	ns
Δt_d	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 6	–	50	–	ns
I_{24}	input current		–	–	0.2	mA
SS_{int}	suppression of internal RGB signals	notes 6 and 12; insertion; f_i = 0 to 5 MHz	55	–	–	dB
SS_{ext}	suppression of external RGB signals	notes 6 and 12; no insertion; f_i = 0 to 5 MHz	55	–	–	dB
V_I	input voltage to blank the RGB outputs to facilitate 'On Screen Display' signals being applied to the outputs		4	–	–	V
COLOUR DIFFERENCE INPUT SIGNALS (PINS 29 AND 30)						
$V_{30(p-p)}$	input signal amplitude (R–Y) (peak-to-peak value)	note 2	–	1.05	–	V
$V_{29(p-p)}$	input signal amplitude (B–Y) (peak-to-peak value)	note 2	–	1.35	–	V
$I_{29,30}$	input current for both inputs	note 2	–	0.1	1.0	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LUMINANCE INPUTS AND OUTPUTS (PINS 25 AND 26)						
$V_{26(p-p)}$	output signal amplitude (peak-to-peak value)	top sync-white	–	0.45	0.63	V
V_{TS}	top sync level		–	2.5	–	V
Z_o	output impedance		–	250	–	Ω
$V_{25(p-p)}$	input signal amplitude (peak-to-peak value)		–	0.45	–	V
I_{clamp}	clamp current	during burst key pulse	–	200	–	μA
I_i	input current	no clamp	–	–	0.5	μA
Chrominance filters						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{osc}	–	MHz
QF	trap quality factor	note 16	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BANDPASS CIRCUIT						
f_c	centre frequency		–	f_{osc}	–	MHz
QBP	bandpass quality factor		–	3	–	
Delay line and peaking circuit						
Y DELAY LINE						
t_d	delay time	note 6	–	480	–	ns
t_{d1}	tuning range delay time	8 steps	–160	–	+160	ns
B	bandwidth of internal delay line	note 6	5	–	–	MHz
PEAKING CONTROL; note 17						
$f_{c(p)}$	peaking centre frequency		–	3	–	MHz
t_W	width of preshoot or overshoot	note 2	–	160	–	ns
OS	overshoot	positive	–	20	–	%
		negative	–	36	–	%
	peaking control curve	16 steps	see Fig.5			
CORING STAGE						
S	coring range		–	15	–	IRE
G_W	wave gain	$\frac{\text{negative half wave gain}}{\text{positive half wave gain}}$	–	1.8	–	
Horizontal synchronization circuits						
SYNC VIDEO INPUT (PINS 9, 11 AND 15)						
$V_{9,11,15}$	sync pulse amplitude	note 2	50	300	–	mV
SL_{HS}	slicing level for horizontal sync	note 18	–	50	–	%
SL_{VS}	slicing level for vertical sync		–	30	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency		–	15625	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8.0 V ±10%; note 6	–	0.2	0.5	%
$\Delta f_{(max)}$	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	–	80	Hz
$\Delta f_{osc(max)}$	maximum frequency deviation at the start of the horizontal output		–	–	75	%
FIRST CONTROL LOOP (FILTER CONNECTED TO PIN 41); note 19						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL	note 6	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
HYS	hysteresis at the switching point		–	1	–	dB
SECOND CONTROL LOOP (CAPACITOR CONNECTED TO PIN 40)						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity		–	150	–	µs/µs
t_{cr}	control range from start of horizontal output to flyback at nominal shift position		11	12	–	µs
t_{shift}	horizontal shift range	63 steps	±2	–	–	µs
	control sensitivity for dynamic compensation		–	5.3	–	µs/V
HORIZONTAL OUTPUT (PIN 38); note 20						
V_{OL}	LOW level output voltage	I_O = 10 mA	–	–	0.3	V
$I_{O(max)}$	maximum allowed output current		10	–	–	mA
$V_{O(max)}$	maximum allowed output voltage		–	–	V_P	V
δ	duty factor	note 6	–	50	–	%
FLYBACK PULSE INPUT (PIN 39)						
V_{HSW}	switching level for horizontal blanking		–	0.4	–	V
$V_{\varphi 2(SW)}$	switching level for phase-2 loop		–	4.0	–	V
$V_{39(max)}$	maximum input voltage	note 2	–	8.0	–	V
Z_i	input impedance	note 2	–	10	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SANDCASTLE PULSE OUTPUT (PIN 37)						
V_{37}	output voltage	during burst key	4.8	5.3	5.8	V
		during blanking	1.8	2.0	2.2	V
t_W	pulse width	burst key pulse	3.3	3.5	3.7	µs
		vertical blanking (50 Hz)	–	25	–	lines
		vertical blanking (60 Hz)	–	21	–	lines
V_{clamp}	clamp level for vertical guard detection		–	2.7	–	V
$I_{37(min)}$	minimum input current to activate guard detection		–	–	0.5	mA
$I_{37(max)}$	maximum allowable input current		2.5	–	–	mA
t_d	delay of start of burst key to start of sync		–	5.4	–	µs
SOFT START; note 21						
δ_{df}	duty factor control range		0	–	50	%
t_{ss}	soft start time		–	100	–	lines
Vertical synchronization and geometry correction						
VERTICAL OSCILLATOR; note 22						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	lines
	locking range		488	–	722	lines/ frame
VERTICAL RAMP GENERATOR (PIN 49)						
$V_{49(p-p)}$	sawtooth amplitude (peak-to-peak value)	VS = 1FH; C = 100 nF; R = 39 kΩ	–	3.5	–	V
I_{dis}	discharge current		–	1	–	mA
I_{charge}	charge current set by external resistor	note 23	–	19	–	µA
VS	vertical slope	control range (63 steps)	–14	–	+14	%
		compress mode	–	75	–	%
		expand mode	–	133	–	%
ΔI_{49}	charge current increase	f = 60 Hz	–	20	–	%
V_{49L}	LOW level of ramp	normal or expand mode	–	2.07	–	V
		compress mode	–	2.55	–	V
VERTICAL DRIVE OUTPUTS (PINS 44 AND 45)						
$I_{diff(p-p)}$	differential output current (peak-to-peak value)	VA = 1FH	–	1	–	mA
I_{CM}	common mode current		–	400	–	µA
V_o	output voltage range		0	–	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EHT TRACKING/OVERVOLTAGE PROTECTION (PIN 48)						
ΔV_{48}	input voltage		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
φ_{vert}	vertical sensitivity		–	7.5	–	%/V
φ_{EW}	EW sensitivity	when switched-on	–	–7.5	–	%/V
I_{eq}	EW equivalent output current		+120	–	–120	µA
V_{48}	overvoltage detection level		–	3.9	–	V
DE-INTERLACE						
	first field delay		–	0.5H	–	
EW WIDTH						
CR	control range	63 steps	100	–	80	%
I_{eq}	equivalent output current		0	–	400	µA
V_o	EW output voltage range		1.0	–	8.0	V
I_o	EW output current range		0	–	900	µA
EW PARABOLA/WIDTH						
CR	control range	63 steps	0	–	24	%
I_{eq}	equivalent output current	EW = 3FH	0	–	480	µA
EW CORNER/PARABOLA						
CR	control range	63 steps	–44	–	0	%
I_{eq}	equivalent output current	PW = 3FH; EW = 3FH	–210	–	0	µA
EW TRAPEZIUM						
CR	control range	63 steps	–4	–	+4	%
I_{eq}	equivalent output current		–80	–	+80	µA
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00H	80	–	120	%
		63 steps; SC = 3FH	86	–	112	%
$I_{eqdiff(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	800	–	1200	µA
VERTICAL SHIFT						
CR	control range	63 steps	–4	–	+4	%
$I_{eqdiff(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)		–40	–	+40	µA
S-CORRECTION						
CR	control range	63 steps	0	–	25	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 24	26	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		–23	–26	–29	dB
HYS_{off}	hysteresis colour killer OFF	strong signal conditions; S/N ≥ 40 dB; note 6	–	+3	–	dB
		noisy input signals; note 6	–	+1	–	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	
REFERENCE PART						
Phase-locked loop; note 25						
f_{CR}	catching range		300	500	–	Hz
$\Delta\varphi$	phase shift for a ±400 Hz deviation of the oscillator frequency	note 6	–	–	2	deg
Oscillator						
TC_{osc}	temperature coefficient of the oscillator frequency	note 6	–	2.0	2.5	Hz/K
Δf_{osc}	oscillator frequency deviation with respect to the supply	note 6; V_P = 8 V ±10%	–	–	250	Hz
R_i	input resistance	pin 32; f = 3.58 MHz; note 2	–	1.5	–	kΩ
		pin 33; f = 4.43 MHz; note 2	–	1.0	–	kΩ
C_i	input capacitance	pins 32 and 33; note 2	–	–	10	pF
HUE CONTROL						
HUE_{cr}	hue control range	63 steps; see Fig.6	±35	±40	–	deg
ΔHUE	hue variation for ±10% V_P	note 6	–	0	–	deg
$\Delta HUE/\Delta T$	hue variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	0	–	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATORS (PINS 27 AND 28)						
$V_{28(p-p)}$	(R–Y) output signal amplitude (peak-to-peak value)	note 26	–	0.525	–	V
$V_{27(p-p)}$	(B–Y) output signal amplitude (peak-to-peak value)	note 26	–	0.675	–	V
G	gain between both demodulators G(B–Y) and G(R–Y)		1.60	1.78	1.96	
ΔV	spread of signal amplitude ratio PAL/NTSC	note 6	–1	–	+1	dB
Z_o	output impedance (R–Y)/(B–Y) output	note 6	–	500	–	Ω
B	bandwidth of demodulators	–3 dB; note 27	–	650	–	kHz
$V_{27,28(p-p)}$	residual carrier output (peak-to-peak value)	$f = f_{osc}$; (R–Y) output			5	mV
		$f = f_{osc}$; (B–Y) output	–	–	5	mV
		$f = 2f_{osc}$; (R–Y) output			5	mV
		$f = 2f_{osc}$; (B–Y) output	–	–	5	mV
$V_{28(p-p)}$	H/2 ripple at (R–Y) output (peak-to-peak value)		–	–	25	mV
$\Delta V_o/\Delta T$	change of output signal amplitude with temperature	note 6	–	0.1	–	%/K
$\Delta V_o/\Delta V_P$	change of output signal amplitude with supply voltage	note 6	–	–	±0.1	dB
φ_e	phase error in the demodulated signals		–	–	±5	deg
COLOUR DIFFERENCE MATRICES IN CONTROL CIRCUIT						
PAL or (SECAM mode with TDA8395); (R–Y) and (B–Y) not affected						
(G–Y)/(R–Y)	ratio of demodulated signals		–	–0.51 ±10%	–	
(G–Y)/(B–Y)	ratio of demodulated signals		–	–0.19 ±25%	–	
NTSC mode; the colour-difference matrix results in the following signals (nominal hue setting)						
(B–Y)	(B–Y) signal		(B–Y)			
(R–Y)	(R–Y) signal		1.39(R–Y) – 0.07(B–Y)			
(G–Y)	(G–Y) signal		–0.46(R–Y) – 0.15(B–Y)			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 31)						
f_{ref}	reference frequency		–	4.43	–	MHz
$V_{31(p-p)}$	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_o	output level	PAL/NTSC identified	–	1.5	–	V
		no PAL/NTSC identified; SECAM (by TDA8395) identified	–	5.0	–	V
I_{31}	required current to stop PAL/NTSC identification circuit during SECAM		150	–	–	µA
Control part						
SATURATION CONTROL; note 15						
SAT_{cr}	saturation control range	63 steps; see Fig.7	52	–	–	dB
CONTRAST CONTROL; note 15						
CON_{cr}	contrast control range	63 steps	–	20	–	dB
	tracking between the three channels over a control range of 10 dB	see Fig.8	–	–	0.5	dB
BRIGHTNESS CONTROL						
BRI_{cr}	brightness control range	63 steps; see Fig.9	–	±0.7	–	V
RGB AMPLIFIERS (PINS 17, 18 AND 19)						
$V_{17,18,19(p-p)}$	output signal amplitude (peak-to-peak value)	at nominal luminance input signal, nominal contrast and white-point adjustment; note 15	tbf	2.0	tbf	V
		at maximum white point setting	–	3.0	–	V
$V_{BWmax(p-p)}$	maximum signal amplitude (black-to-white)	note 28	–	2.6	–	V
		at maximum white point setting	–	3.6	–	V
$V_{RED(p-p)}$	output signal amplitude for the 'red' channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL)	tbf	2.1	tbf	V
V_{blank}	blanking level at the RGB outputs		0.7	0.8	0.9	V
I_{bias}	internal bias current of NPN emitter follower output transistor		–	1.5	–	mA
I_o	available output current		–	5	–	mA
Z_o	output impedance		–	150	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIERS (CONTINUED)						
CR_{bl}	control range of the black-current stabilization	nominal brightness and white-point adjustment (with respect to the measuring pulse); V_{blk} = 2.5 V	–	–	±1	V
V_{bl}	black level shift with picture content	note 6	–	–	20	mV
V_o	output voltage of the 4-L pulse after switch-on		–	4.2	–	V
$\Delta bl/\Delta T$	variation of black level with temperature	note 6	–	1.0	–	mV/K
Δbl	relative variation in black level between the three channels during variations of	note 6				
	supply voltage (±10%)	nominal controls	–	–	tbf	mV
	saturation (50 dB)	nominal contrast	–	–	tbf	mV
	contrast (20 dB)	nominal saturation	–	–	tbf	mV
	brightness (±0.5 V)	nominal controls	–	–	tbf	mV
	temperature (range 40 °C)		–	–	tbf	mV
S/N	signal-to-noise ratio of the output signals	RGB input; note 29	60	–	–	dB
		CVBS input; note 29	50	–	–	dB
$V_{res(p-p)}$	residual voltage at the RGB outputs (peak-to-peak value)	at f_{osc}	–	–	15	mV
		at $2f_{osc}$ plus higher harmonics in RGB outputs	–	–	15	mV
B	bandwidth of output signals	RGB input; at –3 dB	8	–	–	MHz
		CVBS input; at –3 dB; f_{osc} = 3.58 MHz	–	2.8	–	MHz
		CVBS input; at –3 dB; f_{osc} = 4.43 MHz	–	3.5	–	MHz
		S-VHS input; at –3 dB	5	–	–	MHz
WHITE-POINT ADJUSTMENT						
	I²C-bus setting for nominal gain	HEX code	–	20H	–	
$G_{inc(max)}$	maximum increase of the gain	HEX code 3FH	40	50	60	%
$G_{dec(max)}$	maximum decrease of the gain	HEX code 00H	40	50	60	%
BLACK-CURRENT STABILIZATION (PIN 16); note 30						
I_{bias}	bias current for the picture tube cathode		–	10	–	µA
I_{leak}	acceptable leakage current		–	100	–	µA
$I_{scan(max)}$	maximum current during scan		–	0.3	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BEAM CURRENT LIMITING (PIN 20); note 28						
V_{CR}	contrast reduction starting voltage		–	4	–	V
V_{diffCR}	voltage difference for full contrast reduction		–	2	–	V
V_{BR}	brightness reduction starting voltage		–	3	–	V
V_{diffBR}	voltage difference for full brightness reduction		–	2	–	V
V_{bias}	internal bias voltage		–	4.5	–	V
$I_{ch(int)}$	internal charge current		–	40	–	µA
I_{disch}	discharge current due to 'peak-white limiting'		–	200	–	µA

Notes

1. On set AGC.
2. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
3. Measured at 10 mV (RMS) top sync input signal.
4. So called projected zero point, i.e. with switched demodulator.
5. Measured in accordance with the test line given in Fig.10. For the differential phase test the peak white setting is reduced to 87%.
   a) The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   b) The phase difference is defined as the difference in degrees between the largest and smallest phase angle.
6. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
7. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.11.
8. The test set-up and input conditions are given in Fig.12. The figures are measured with an input signal of 10 mV RMS.
9. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_O \text{ (black-to-white)}}{V_{m\,(rms)}\ (B = 5\ MHz)}$$

10. To obtain a good noise immunity of the AGC circuit the AGC detector is gated during the sync pulse. This gating is switched-off during the vertical retrace to avoid disturbances of the signal amplitude due to phase errors of the incoming video signal which are caused by the head-switching of VCRs.

11. The AFC slope is directly related to the Q-factor of the demodulator tuned circuit. The given AFC steepness is obtained with a Q-factor of 60. The AFC off-set is tested with a double sideband input signal and with the reference tuned circuit tuned to minimum AGC voltage (optimum tuning for the demodulator).

    The tuning information is supplied to the tuning system via the I²C-bus. Two bits have been reserved for this function. The first bit indicates whether the tuning is within the given window. The second bit indicates the direction of the tuning. Bit indications:

    a) AFA = 1; tuning inside window.

    b) AFA = 0; tuning outside window.

    c) AFB = 1; tuning too high.

    d) AFB = 0; tuning too low.

    To improve the speed of search tuning systems the AFC window can be increased to about 240 kHz. The width of the window can be set by means of the AFW bit in subaddress 03.

12. Signal with negative-going sync. Amplitude includes sync pulse amplitude.

13. This parameter is measured at nominal settings of the various controls.

14. Indicated is a signal for a colour bar with 75% saturation (chroma : burst ratio = 2.2 : 1).

15. Nominal contrast is specified with the DAC in position 20H. Nominal saturation as maximum –10 dB. In the nominal brightness setting the black level at the outputs is identical to the level of the black-current measuring pulses.

16. The –3 dB bandwidth of the circuit can be calculated by means of the following equation:

$$f_{-3\,dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

17. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.

18. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch).

19. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the I²C-bus. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when too much noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching between the two modes can be automatically or overruled by the I²C-bus.

    The circuit contains a video identification circuit which is independent of first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input. The coupling of the video identification circuit with the first loop can be defeated via the I²C-bus.

    When the horizontal PLL is set to the 'slow' mode (via I²C-bus bits FOA and FOB) or during weak signal conditions in the 'automatic' mode the phase detector is gated to obtain a good noise immunity. The width of the gating pulse is 5.7 µs.

    The output current of the phase detector in the various conditions are shown in Table 42.

20. During the start-up period of the oscillator the duty factor of the output pulse rises gradually from 0% to 50% (time approximately 100 lines).

21. The start-up frequency depends on the SFM bit in the I²C-bus protocol. When SFM = 0 the frequency starts at a high (non calibrated) value. When SFM = 1 the output signal will only be available after calibration.

22. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 3 modes of operation:

    a) Search mode 'large window'.

    This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).

    b) Standard mode 'narrow window'.

    This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz).

    When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

    When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 08.

23. Conditions: frequency is 50 Hz; normal mode; VS = 1F.

24. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and –20 dB.

25. All frequency variations are referenced to 3.58 or 4.43 MHz carrier frequency.
    All oscillator specifications are measured with the Philips crystal series 9922 520.
    If the spurious response of the 4.43 MHz crystal is lower than –1 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequency is guaranteed.
    The spurious response of the 3.58 MHz crystal must be lower than –1 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.

    The catching and detuning range are measured for nominal crystal parameters. These are:

    a) Load resonance frequency f_0 = 4.433619 or 3.579545 MHz; C_L = 20 pF.

    b) Motional capacitance C_1 = 20.6 fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal).

    c) Parallel capacitance C_0 = 5.5 pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).

    The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.

    Philips Components has developed a special crystal which is tuned to the correct frequency in an application without series capacitance (code number 9922 520 0038X; see Table 43). This has the advantage that the tuning (catching) range is increased with approximately 50% without negative effects on spurious responses. When the catching range of 300 Hz is considered too low this special crystal is a suitable alternative.

    The free-running frequency of the oscillator can be checked by opening the colour PLL via the I²C-bus. In that condition the colour killer is not active so that the frequency off-set is visible on the screen. When two crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator switching continuously between the two frequencies.

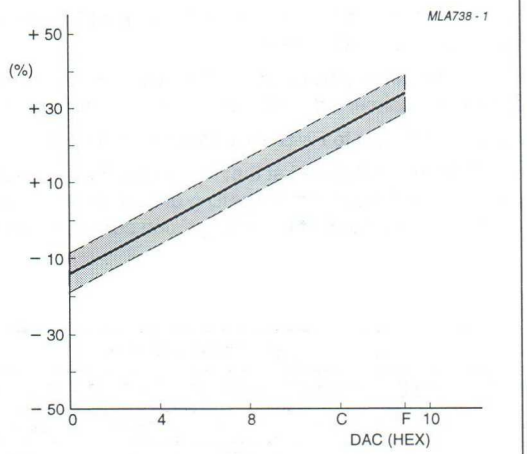
26. The (R–Y) and (B–Y) signals are demodulated with a phase difference of the reference carrier of 90° and a gain ratio $\frac{(B-Y)}{(R-Y)} = 1.78$. The matrixing to the required signals is achieved in the control part.
27. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.
28. At nominal setting of the gain control. When this amplitude is exceeded the peak-white limiting circuit will reduce the contrast. The control voltage is generated via the external capacitor connected to the beam-current limiting input.
29. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
30. This is a current input. The indicated value of the nominal bias current is obtained at the nominal setting of the gain (white point) control. The actual value of the bias current depends on the gain control setting of each channel. As a result the 'black-current' of each gun is adapted to the white point setting so that the back-ground colour will follow the white point adjustment.

Table 42 Output current of the phase detector in the various conditions

I²C-BUS COMMANDS				IC CONDITIONS			φ-1 CURRENT/MODE			
VID	POC	FOA	FOB	IDENT	COIN	NOISE	SCAN	V-RETR	GATING	MODE
–	0	0	0	yes	yes	yes	30	30	yes	auto
–	0	0	0	yes	no	–	180	270	no	auto
–	0	0	1	yes	yes	–	30	30	yes	slow
–	0	0	1	yes	no	–	180	270	no	slow
–	0	1	–	yes	–	–	180	270	no	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

Table 43 Code numbers for special crystals

SYSTEM	FREQUENCY (MHz)	CODE NUMBER
PAL-N	3.582056	9922 520 00381
NTSC-M	3.579545	9922 520 00382
PAL-M	3.575611	9922 520 00383
PAL-B/G	4.433619	9922 520 00384



Overshoot in direction 'black'.

Fig.5 Peaking control curve.

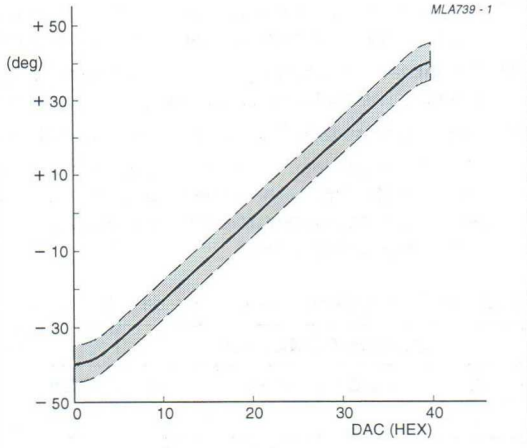


Fig.6 Hue control curve.

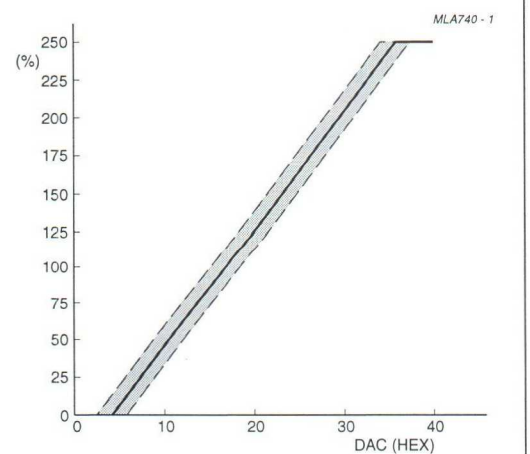


Fig.7 Saturation control curve.

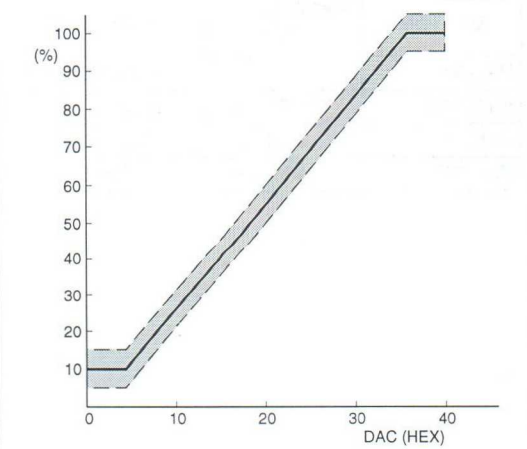
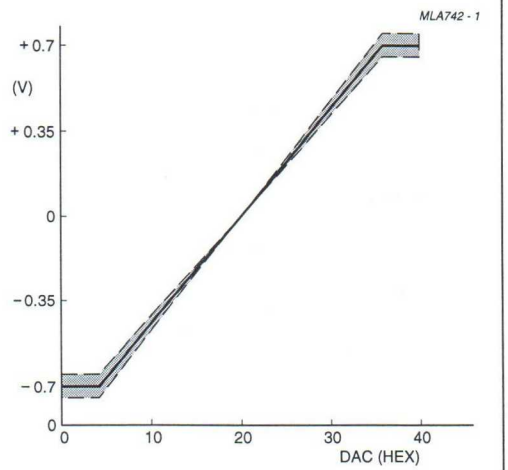


Fig.8 Contrast control curve.



Relative variation with respect to the measuring pulse.

Fig.9 Brightness control curve.

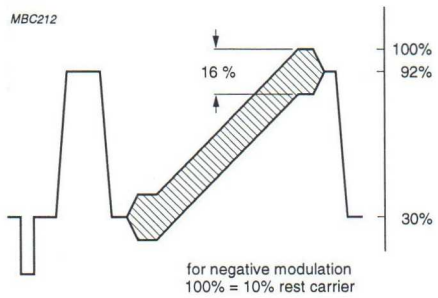


Fig.10 Video output signal.

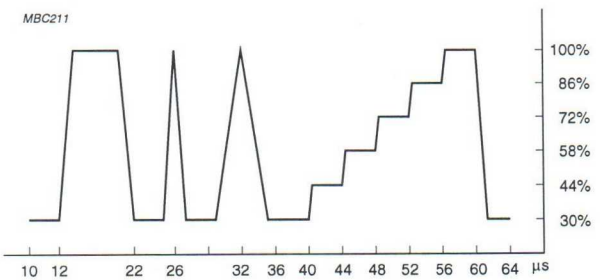
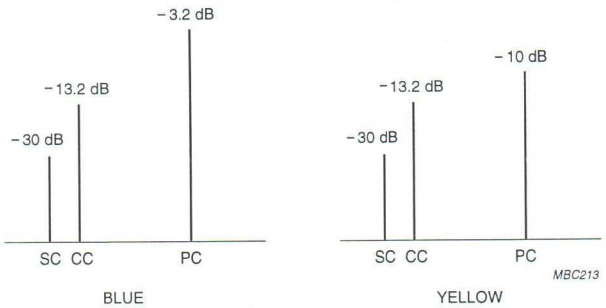
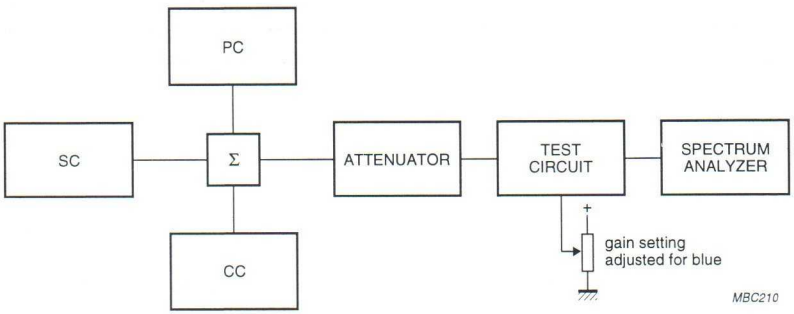


Fig.11 Test signal waveform.





Input signal conditions: SC = sound carrier; CC = colour carrier; PC = picture carrier.
All amplitudes with respect to top sync level.

$$\text{Value at 0.92 or 1.1 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 0.92 or 1.1 MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 2.66 or 3.3 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 2.66 or 3.3 MHz}}$$

Fig.12 Test set-up intermodulation.

TEST AND APPLICATION INFORMATION

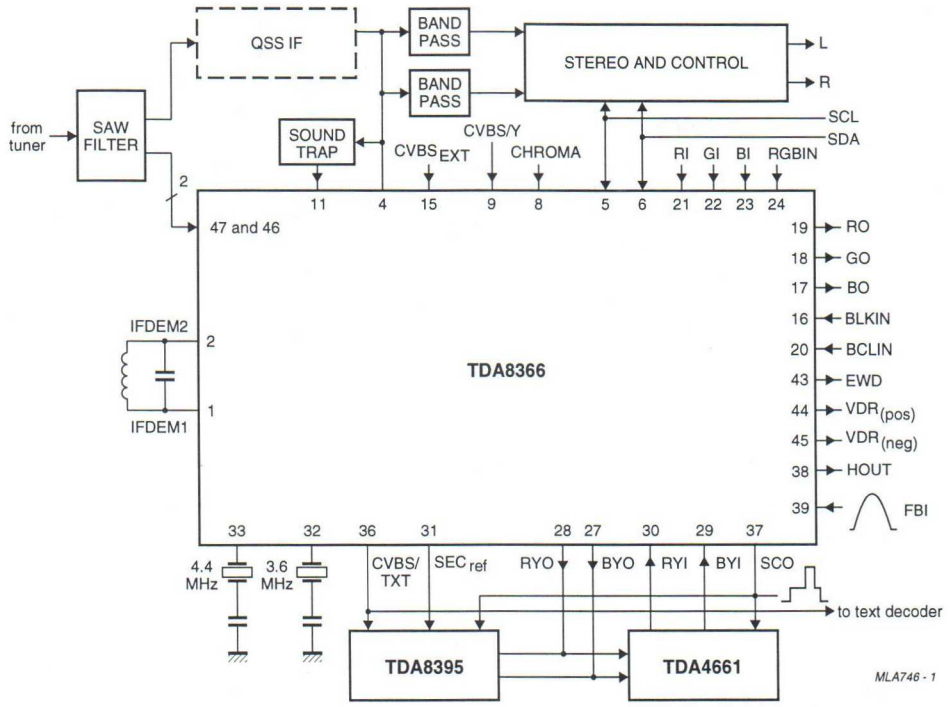


Fig.13 Application diagram.

East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Fig.14.

Resistor R_{EW} determines the gain of the EW output stage. Resistor R_c determines the reference current for both the vertical sawtooth generator and the geometry processor.

The preferred value of R_c is 39 kΩ which results in a reference current of 100 μA (V_{ref} = 3.9 V).

The value of R_{EW} must be:

$$R_{EW} = R_c \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With V_{ref} = 3.9 V; R_c = 39 kΩ and V_{scan} = 120 V then R_{EW} = 68 kΩ.

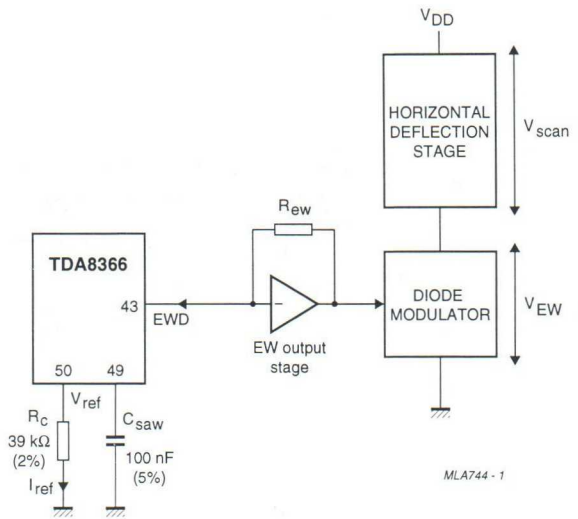
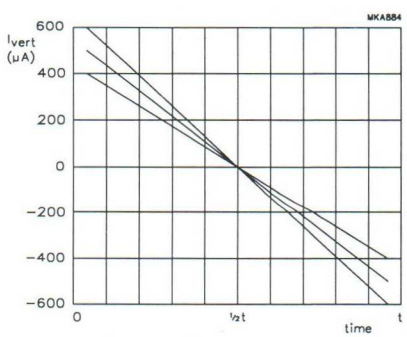
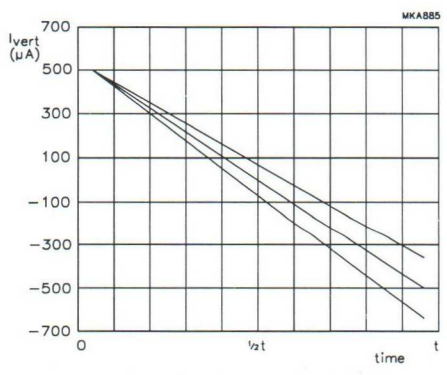


Fig.14 East-West output stage.



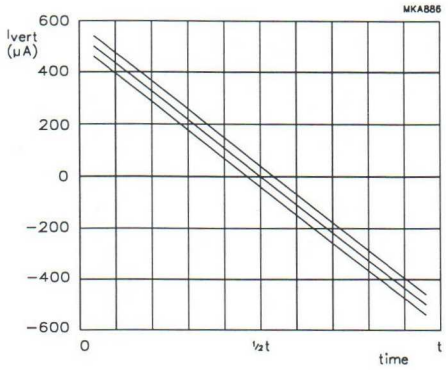
VA = 0, 31H and 63H; VSH = 31H; SC = 0.

Fig.15 Control range of vertical amplitude.



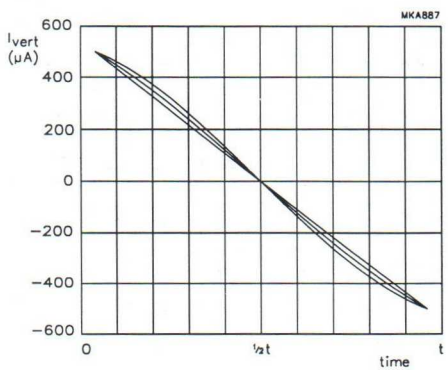
VS = 0, 31H and 63H; VA = 31H; VHS = 31H; SC = 0.

Fig.16 Control range of vertical slope.



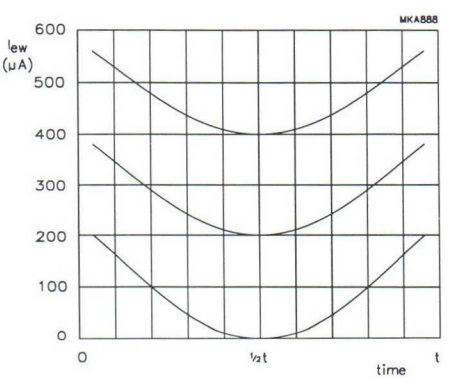
VSH = 0, 31H and 63H; VA = 31H; SC = 0.

Fig.17 Control range of vertical shift.



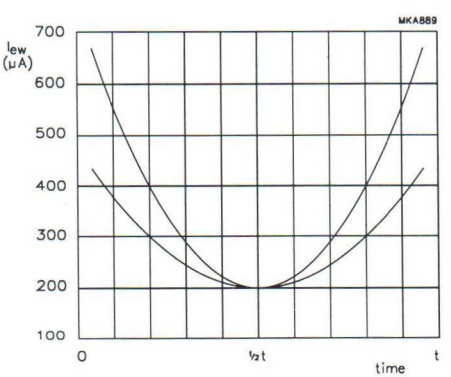
SC = 0, 31H and 63H; VA = 31H; VHS = 31H.

Fig.18 Control range of S-correction.



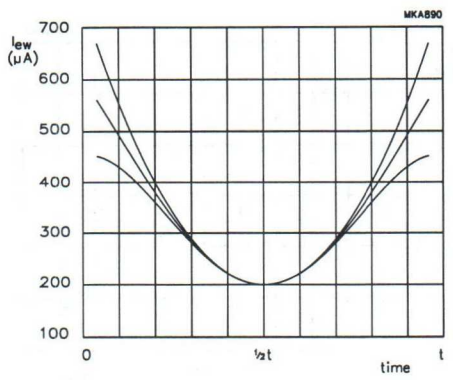
EW = 0, 31H and 63H; PW = 31H; CP = 31H.

Fig.19 Control range of EW width.



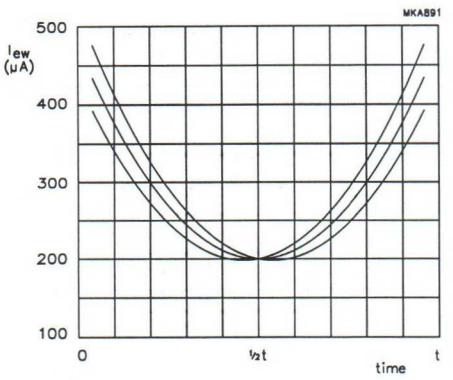
PW = 0, 31H and 63H; EW = 31H; CP = 31H.

Fig.20 Control range of EW parabola/width ratio.



CP = 0, 31H and 63H; EW = 31H; PW = 63H.

Fig.21 Control range of EW corner/parabola ratio.



TC = 0, 31H and 63H; EW = 31H; PW = 31H.

Fig.22 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA8366 offers nine control parameters for picture alignment:

- Vertical picture alignment
  - S-correction
  - vertical amplitude
  - vertical slope
  - vertical shift
- Horizontal picture alignment
  - horizontal shift
  - EW width
  - EW parabola/width
  - EW corner/parabola
  - EW trapezium correction.

It is important to notice that the TDA8366 is designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and EW output stage it is determined which are the required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio. These parameters can be preset via the I²C-bus, and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is meant for compensation of off-sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off-sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off-set, and to the square of the S-correction needed. The necessity to use the vertical shift alignment depends on the expected off-sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the right setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1F). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the EW width and the horizontal shift. Finally (if necessary) the left- and right-hand sides of the picture are aligned in parallel by adjusting the EW trapezium control.

After adjustment of the picture for normal vertical deflection as described, no additional adjustment is necessary for the compress and expand mode. If required a small correction of the picture height can be made by adjusting the vertical slope. This will not effect the linearity.

SUPERSEDES DATA OF OCTOBER 1993

CONTROL CIRCUIT FOR SWITCHED MODE POWER SUPPLIES

GENERAL DESCRIPTION

The TDA8380A is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380A operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

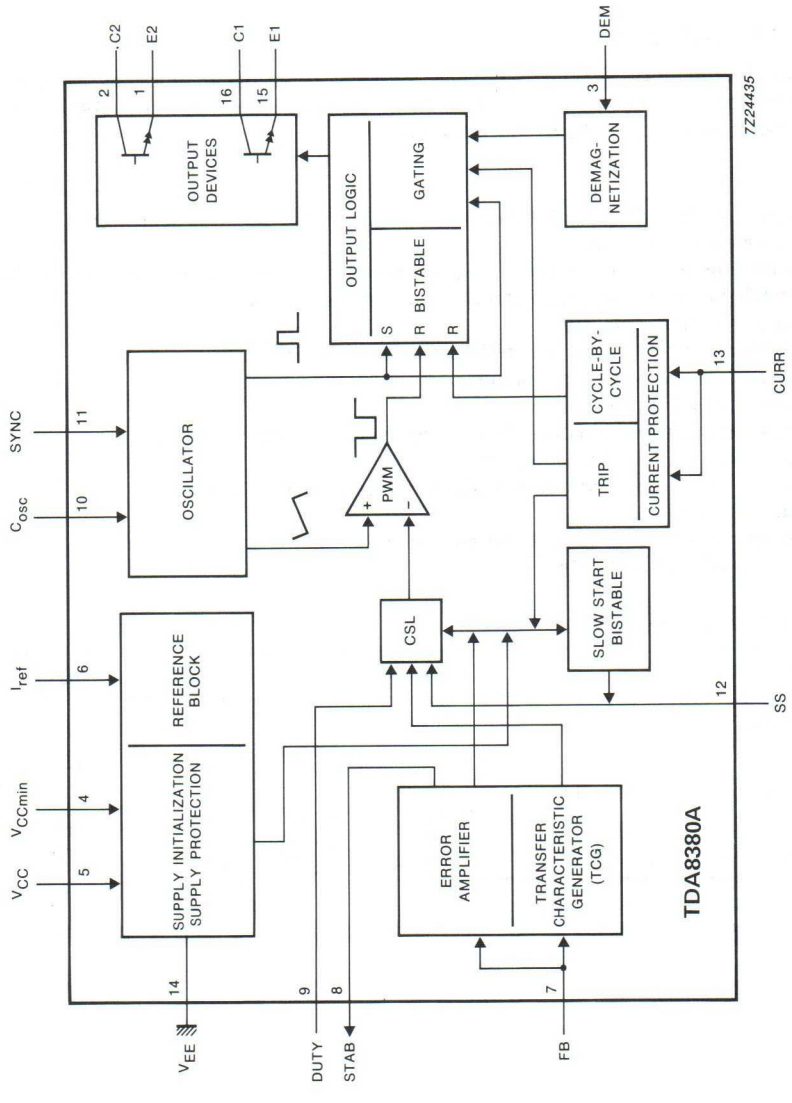


Fig.1 Block diagram.

PINNING

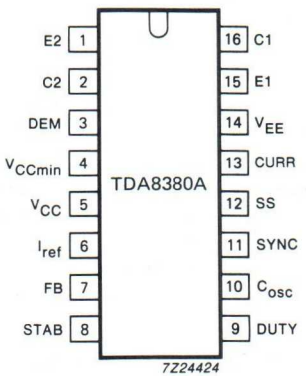


Fig.2 Pinning diagram.

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380A is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

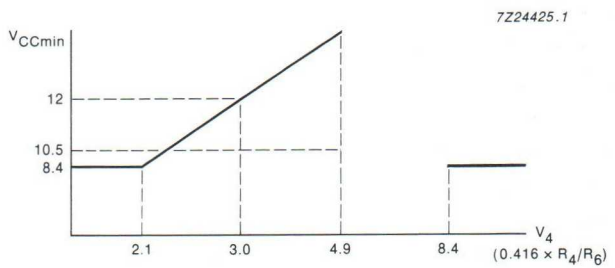


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

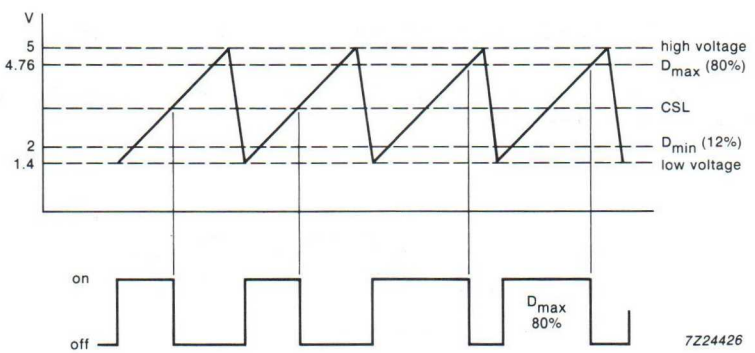


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

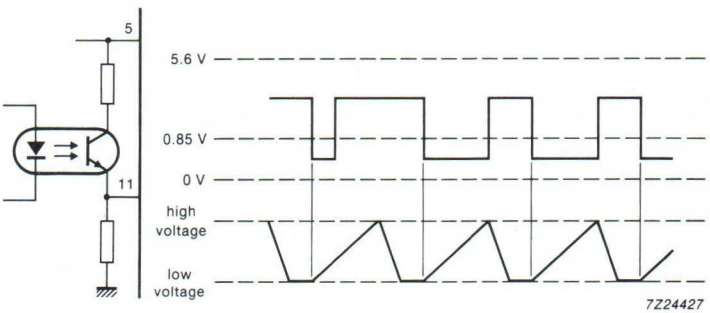


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

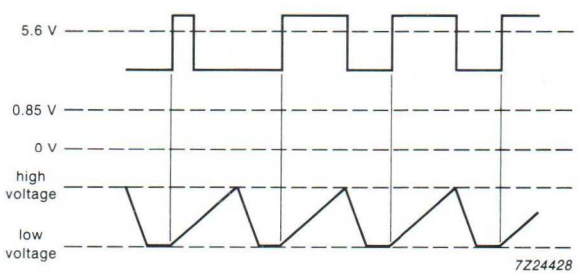
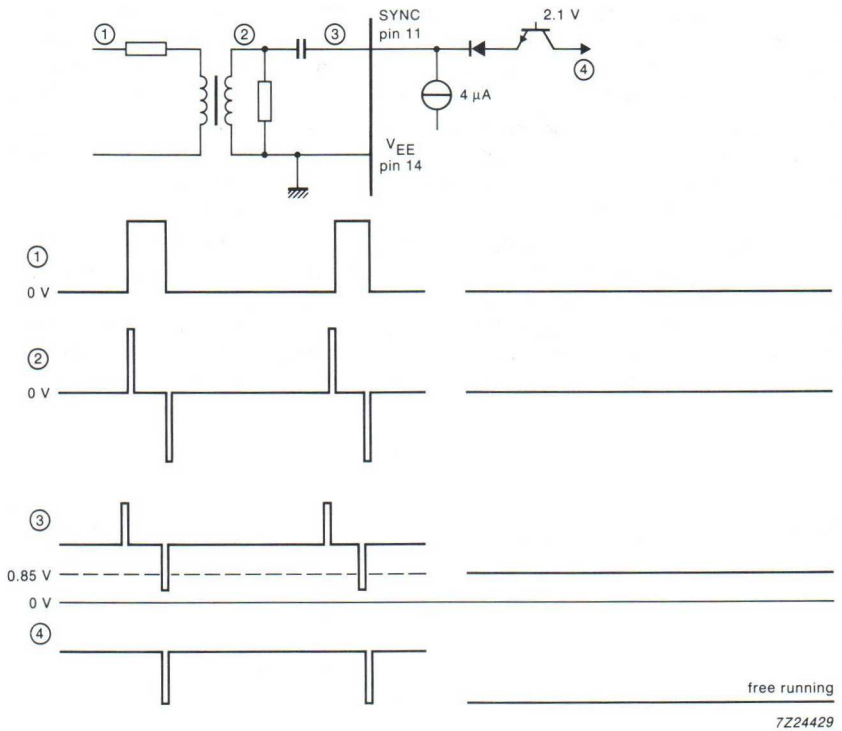


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

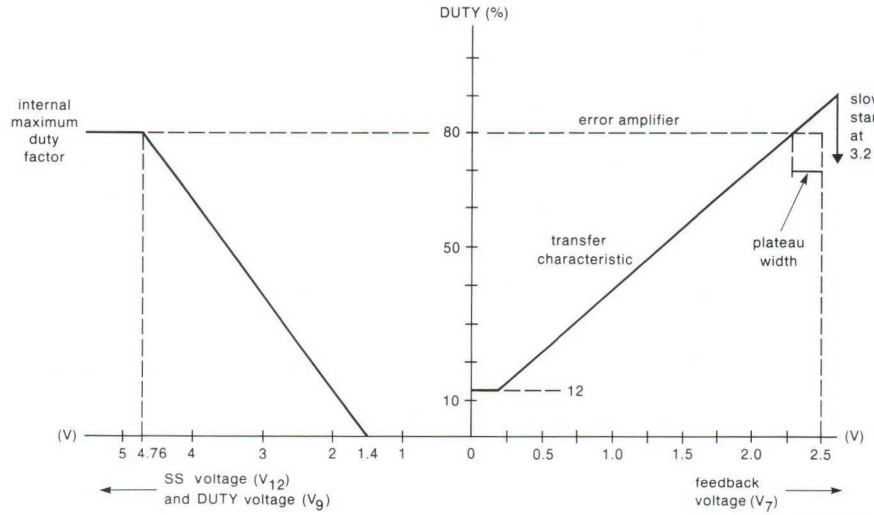


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

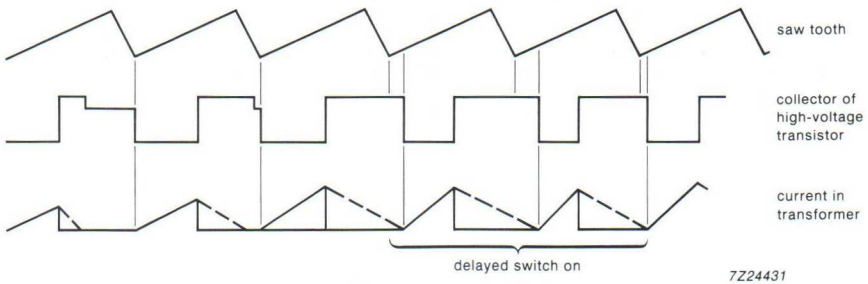


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

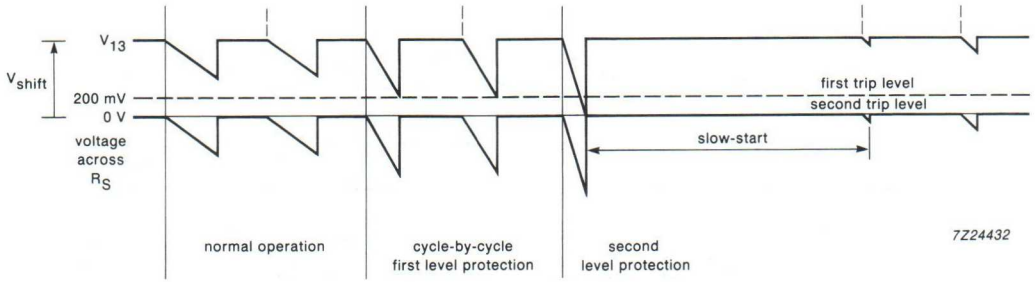


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

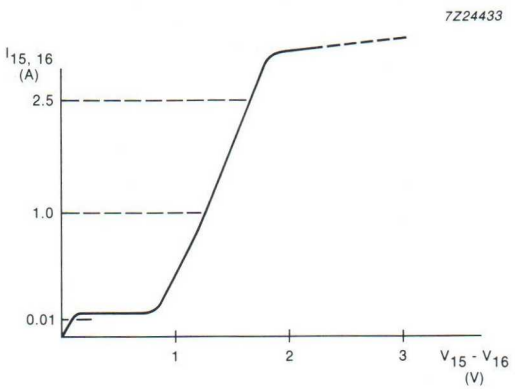


Fig.10 Saturation curve.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.11			
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 55$ K/W

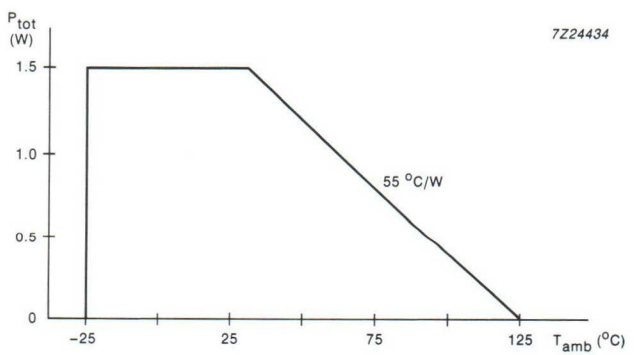


Fig.11 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	I_6/5.7	I_6/6	I_6/6.4	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	I_6/5.7	I_6/6	I_6/6.3	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	–	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	–	V
at 1 A		$V_{16} - V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	–	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16\text{-}15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at −700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Switching voltage level		V_3	615	645	675	mV
Switching current level		I_3	−23	–	−39	μA
Current range of clamp circuits		I_3	−10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at −10 mA	V_3	–	−800	–	mV
Temperature coefficient		TC	–	−1.9	–	mV/K
Current protection						
Input current	note 1	I_{13}	I_6/5.7	I_6/6	I_6/6.3	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	−10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to −200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	−800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

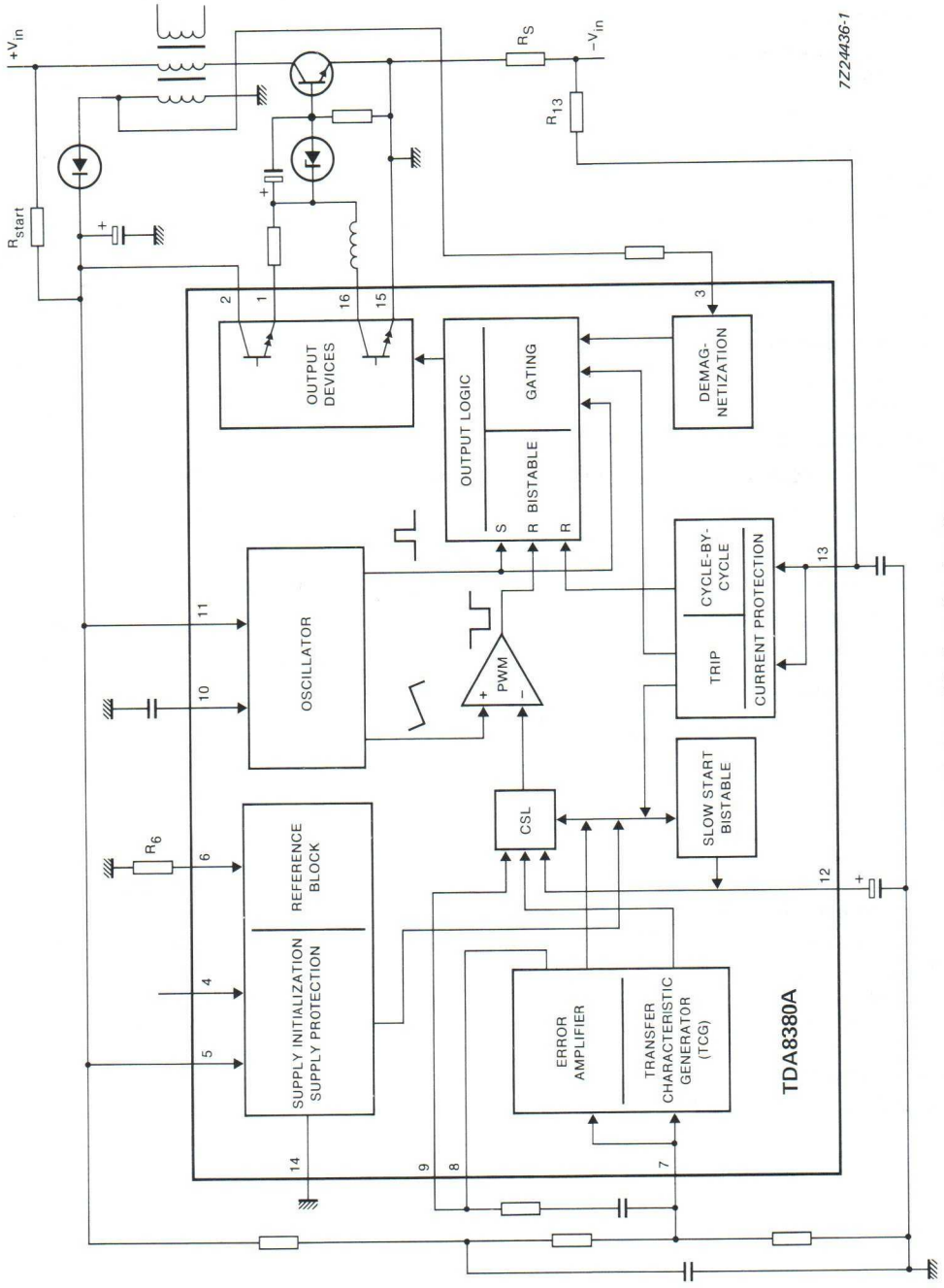


Fig.12 Simplified application diagram.

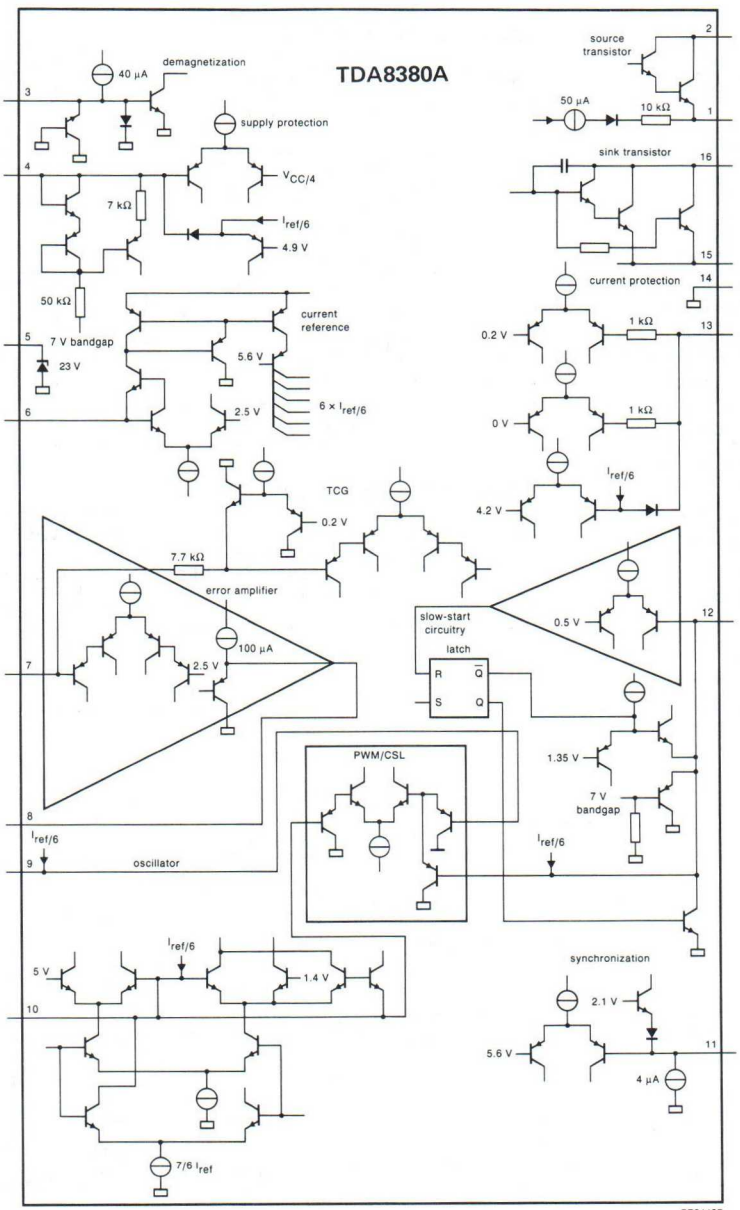


Fig.13 Input and output loading diagram.

SECAM decoder TDA8395

FEATURES

- Fully integrated filters
- Alignment free
- For use with baseband delay

GENERAL DESCRIPTION

The TDA8395 is a self-calibrating, fully integrated SECAM decoder. The IC should preferably be used in conjunction with the PAL/NTSC decoder TDA8362 or TDA8366 and with the switched capacitor baseband delay circuit TDA4660. The IC incorporates HF and LF filters, a demodulator and an identification circuit (luminance is not processed in this IC). The IC needs no adjustments and very few external components are required. A highly stable reference frequency is required for calibration and a two-level sandcastle pulse for blanking and burst gating.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage; pin 3	7.2	-	8.8	V
P_{tot}	total power dissipation	-	-	220	mW
$V_{16(p-p)}$	composite video input voltage (peak-to-peak value); pin 16	-	1.0	1.5	V
$V_{O(p-p)}$	-(R-Y) output voltage amplitude (peak-to-peak value); pin 9	-	1.05	-	V
$V_{O(p-p)}$	-(B-Y) output voltage amplitude (peak-to-peak value); pin 10	-	1.33	-	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8395	16	DIL	plastic	SOT38GE1

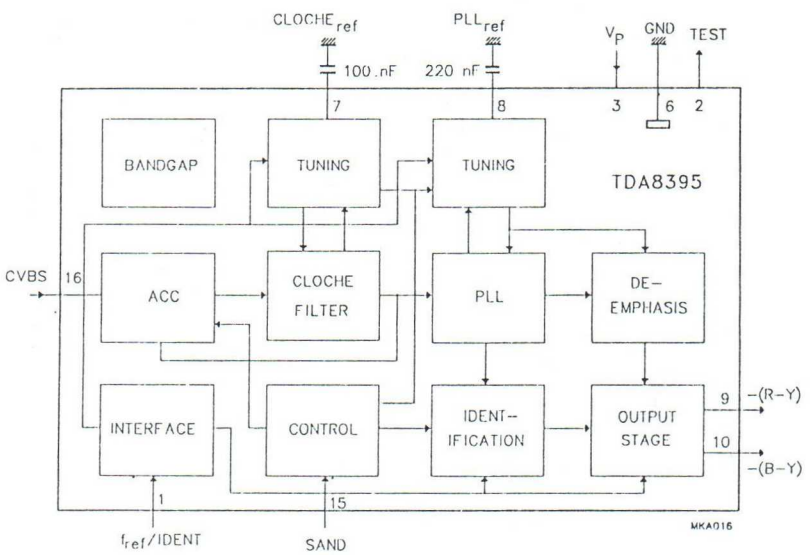


Fig.1 Block diagram.

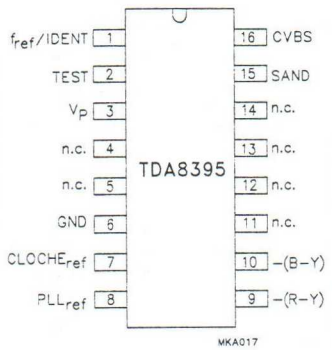


Fig.2 Pin configuration

PINNING

SYMBOL	PIN	DESCRIPTION
f_{ref}/IDENT	1	reference frequency input/identification input
TEST	2	test output
V_P	3	positive supply voltage
n.c.	4	not connected
n.c.	5	not connected
GND	6	ground
$CLOCHE_{ref}$	7	Cloche reference filter
PLL_{ref}	8	PLL reference
-(R-Y)	9	-(R-Y) output
-(B-Y)	10	-(B-Y) output
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
SAND	15	sandcastle pulse input
CVBS	16	video (chrominance) input

FUNCTIONAL DESCRIPTION

The TDA8395 is a self-calibrating SECAM decoder designed for use with a baseband delay circuit.

During frame retrace a 4.433619 MHz reference frequency is used to calibrate the filters and the demodulator. The reference frequency should be very stable during this period.

The Cloche filter is a gyrator-capacitor type filter the resonance frequency of which is controlled during the calibration period and offset during scan; this ensures the correct frequency during calibration.

The demodulator is a Phase-Locked Loop (PLL) type demodulator which uses the frequency reference and the bandgap reference to force the PLL to the required demodulation characteristic.
The low frequency de-emphasis is matched to the PLL and is controlled by the tuning voltage of the PLL.

A digital identification circuit scans the incoming signal for SECAM (only line-identification is implemented). The identification circuit needs to communicate with the TDA8362 to guarantee that the output signal from the decoder is only available when no PAL signal has been identified. If a SECAM signal is decoded a request for colour-on is transmitted to pin 1 (current is sunk). If the signal request is granted (i.e. pin 1 is HIGH therefore no PAL) the colour difference outputs (-(B-Y) and -(R-Y)) from the TDA8362 are high impedance and the output signals from the TDA8395 are switched ON.

If no SECAM signal is decoded during a two-frame period the demodulator will be initialized before another attempt is made also during a two-frame period. The CD outputs will be blanked or high-impedance depending on the logic level at pin 1.

A two-level sandcastle pulse generates the required blanking periods and, also, clocks the digital identification pulse on the falling edge of the burst gate pulse. To enable the calibration period to be defined the vertical retrace is discriminated from the horizontal retrace, this is achieved by measuring the width of the blanking period.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	-	8.8	V
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+70	°C

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 3)						
V_P	positive supply voltage		7.2	8.0	8.8	V
I_P	supply current		-	18	25	mA
P_{tot}	total power dissipation		-	144	220	mW
CVBS input (pin 16)						
$V_{16(p-p)}$	composite video input voltage (peak-to-peak value)		-	1.0	1.5	V
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	note 1	15	-	300	mV
Z_I	input impedance	note 2	-	15	-	kΩ
CLOCHE (pin 7)						
V_{tc}	tuning voltage		2.5	3.5	4.5	V
f_0	resonance frequency	note 3	4.266	4.286	4.306	MHz
B	bandwidth		241	268	295	kHz
Demodulator						
V_{td}	tuning voltage; pin 8		3.5	-	4.8	V
$V_{O(p-p)}$	output voltage amplitude (peak-to-peak value); pin 9	100/75 colour bar	0.97	1.05	1.13	V
$V_{O(p-p)}$	output voltage amplitude (peak-to-peak value); pin 10	100/75 colour bar	1.23	1.33	1.43	V
NLE	non-linearity error	100/75 colour bar; note 4	-	-	3	%
-(B-Y)/-(R-Y)	ratio of -(B-Y) and -(R-Y)		1.23	1.27	1.32	
$f_{be-(R-Y)}$	black-level error -(R-Y)	note 5	-	-	5	kHz
$f_{be-(B-Y)}$	black-level error -(B-Y)	note 5	-	-	7	kHz
V_O	output voltage level during blanking		-	2.8	-	V
B_O	output bandwidth		-	1.3	-	MHz
S/N	signal-to-noise ratio	note 6	40	-	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_p	pole-frequency LF de-emphasis		77	85	93	kHz
f_p/f_0	ratio of pole and zero frequency		-	3	-	
$V_{rh(p-p)}$	residual harmonic voltage (peak-to-peak value)		-	-	10	mV
$Z_{O(e)}$	output impedance SECAM enabled	pin 1 HIGH	-	-	600	Ω
$Z_{O(d)}$	output impedance SECAM disabled	pin 1 LOW	1	-	-	MΩ
Sandcastle pulse						
V_{bl}	blanking detection level		1.0	1.25	1.5	V
V_{bg}	burst gate detection level		3.5	3.85	4.2	V
t_f	falling edge of burst gate to start sync		8.5	9.0	9.5	µs
Reference/communication						
f_{ref}	reference frequency	note 7	-	4.4336	-	MHz
$V_{ref(p-p)}$	reference voltage amplitude (peak-to-peak value)		0.20	-	0.50	V
V_{ed}	SECAM enable detection level; pin 1		-	2.8	3.3	V
V_{dd}	SECAM disabled detection level; pin 1	note 8	1.5	2.0	-	V
I_s	sink current at SECAM identification; pin 1	note 9	-	150	-	µA
Identification						
t_i	identification time		-	4	-	frames
H	colour on/off hysteresis		3	-	-	dB

Notes to the characteristics

1. If measured in the burst-period of a blue line.
2. The video input is AC-coupled.
3. During scan.
4. Measured as 100% x $(|V_u| - |V_l|) / (|V_u| + |V_l|)$; see Fig. 3.
5. Converted to input frequency error.
6. Defined as the ratio between the peak-to-peak value of the B-Y component of the demodulated 100/75 colour bar and the peak-to-peak value of the noise.
7. The reference should be stable during frame blanking.
8. The SECAM enable and disable timing should preferrably be at the end of the frame blanking.
9. The externally supplied voltage should exceed 0.5 V.

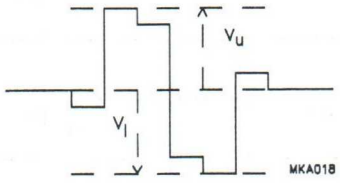


Fig.3 Non-linearity definition.

TIMING

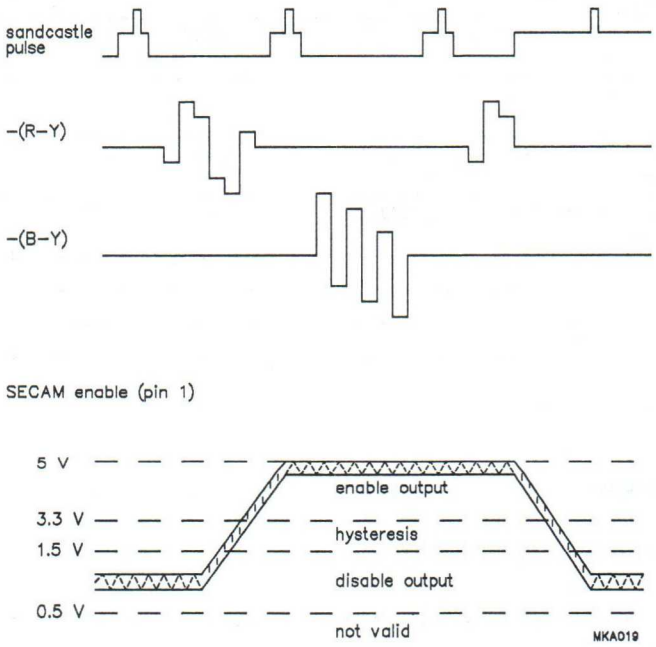


Fig.4 Timing waveforms.

APPLICATION INFORMATION

The leakage current at pin 8 should be well below 20 nA to meet the specification of the black levels (C8 = 220 nF). The leakage current at pin 7 should be well below 60 nA to meet the specification of the Cloche resonance frequency (C7 = 100 nF).

The capacitors C7 and C8 should be connected to the ground pin as close as possible to the package. If not, this can result in a black level error for both channels.

TEST INFORMATION

The performance of the Cloche filter can be measured at pin 2. The use of a FET-probe is advised for low capacitive loading.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8415 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8415 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Function and software are compatible with the TDA8405
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

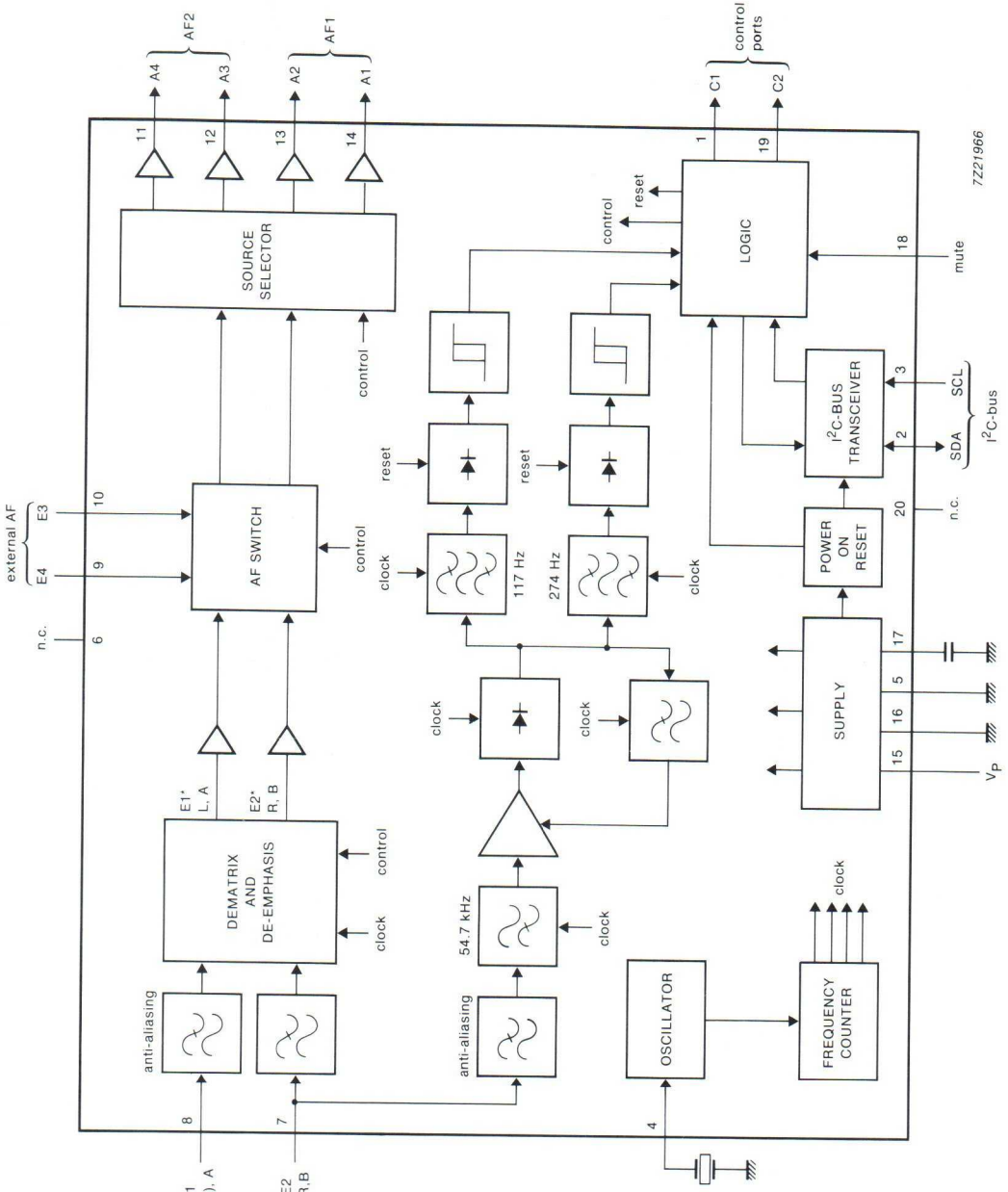


Fig.1 Block diagram.

DEVELOPMENT DATA

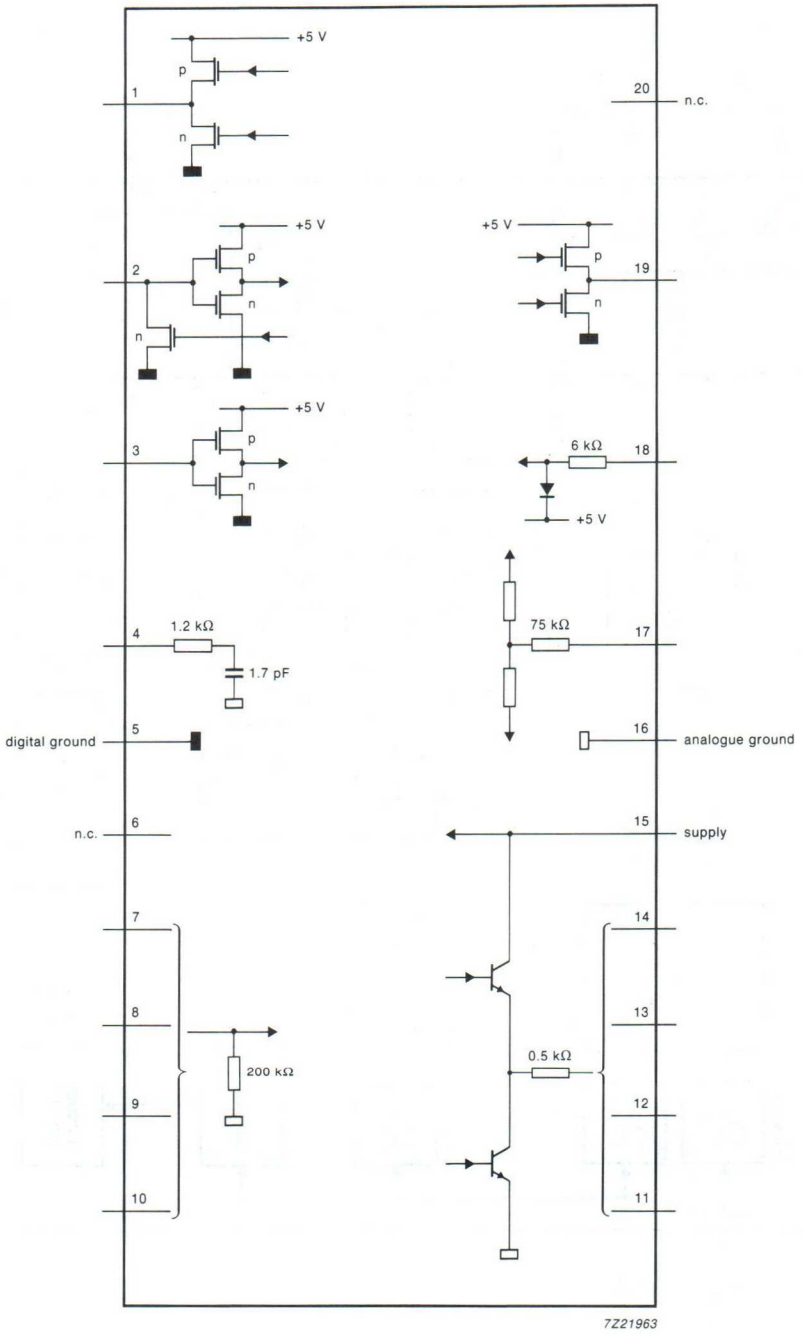


Fig.2 Input and output loading diagram.

PINNING

1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I^2C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I^2C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage V_P
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	External AF input (E3)	20	Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where L = left channel signal; R = right channel signal; A = first sound channel signal and B = second sound channel signal.

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

DEVELOPMENT DATA

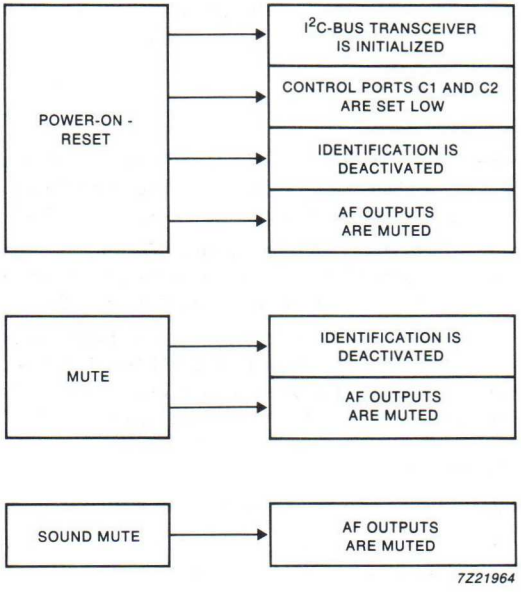


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8415 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

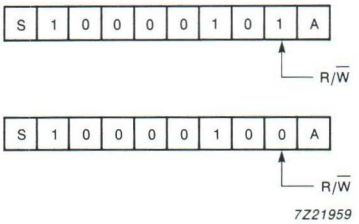
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8415

The TDA8415 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8415 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8415 is a slave transmitter)

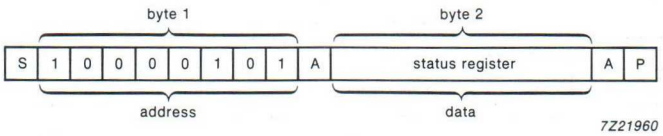
Write to (TDA8415 is a slave receiver)

Where S = start bit and A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8415

Reading the TDA8415 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

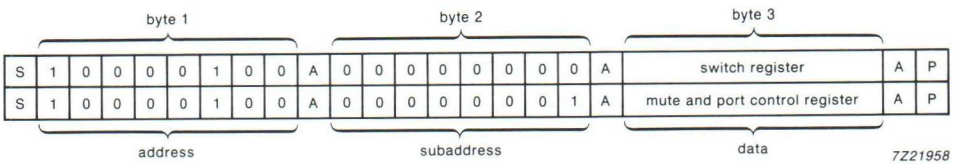
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission
1	1	not possible

Writing to the TDA8415

Writing to the TDA8415 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

DEVELOPMENT DATA

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where: X = don't care.

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)

Where: M = mono; St = stereo. DS = dual sound; R = right; L = left; L* = (L+R)/2; A = sound A; B = sound B.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)		500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

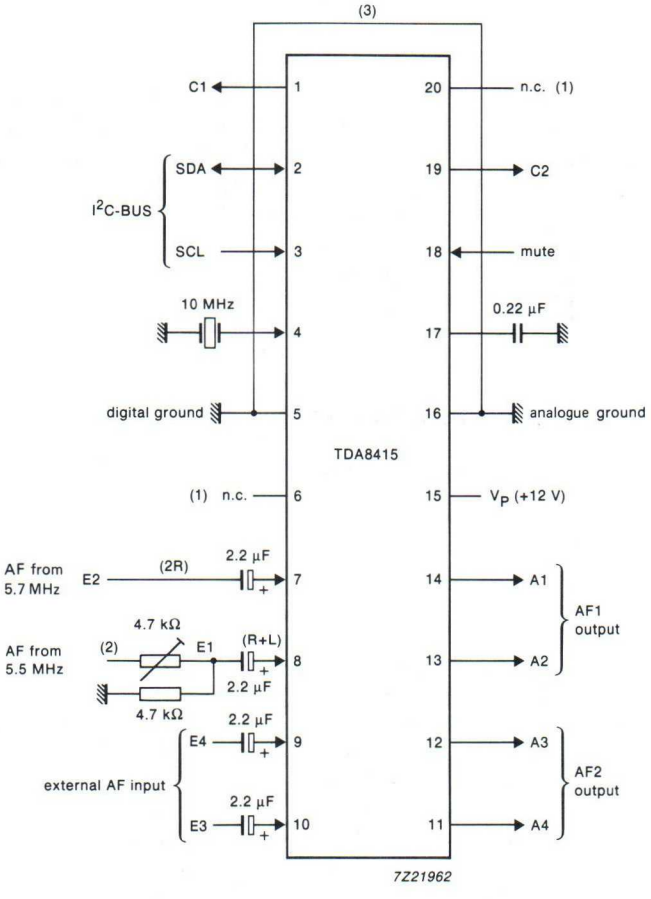
parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I^2C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. $f = 400$ Hz; $R_L = 1$ MΩ.
6. $40\ \text{Hz} \leqslant f \leqslant 15$ kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at $f = 3.183$ kHz.
10. $V_O = 1$ V RMS; $f = 1$ kHz.
11. Test circuit see Fig.7.

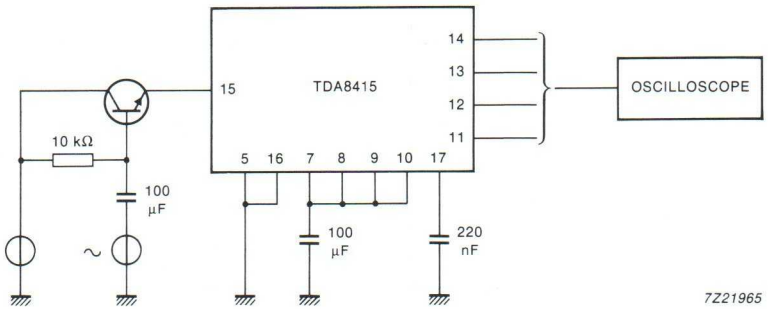


(1) These pins are not connected internally and should not be connected on the printed circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

DEVELOPMENT DATA

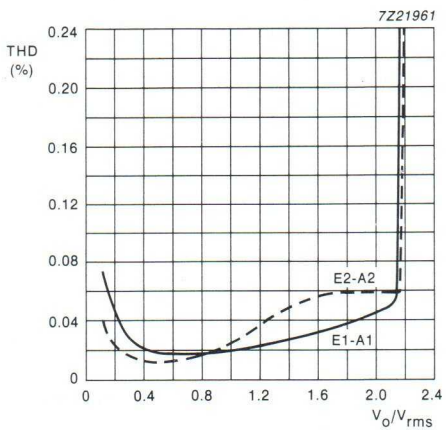


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

NOTES

NOTES

NOTES

NOTES

North American Sales Offices, Representatives and Distributors

PHILIPS SEMICONDUCTORS
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409

ALABAMA
Huntsville
Philips Semiconductors
Phone: (205) 464-0111
(205) 464-9101

Elcom, Inc.
Phone: (205) 830-4001

ARIZONA
Scottsdale
Thom Luke Sales, Inc.
Phone: (602) 451-5400

Tempe
Philips Semiconductors
Phone: (602) 820-2225

CALIFORNIA
Calabasas
Philips Semiconductors
Phone: (818) 880-6304

Irvine
Philips Semiconductors
Phone: (714) 453-0770

Loomis
B.A.E. Sales, Inc.
Phone: (916) 652-6777

San Diego
Philips Semiconductors
Phone: (619) 560-0242

San Jose
B.A.E. Sales, Inc.
Phone: (408) 452-8133

Sunnyvale
Philips Semiconductors
Phone: (408) 991-3737

COLORADO
Englewood
Philips Semiconductors
Phone: (303) 792-9011

Thom Luke Sales, Inc.
Phone: (303) 649-9717

CONNECTICUT
Wallingford
JEBCO
Phone: (203) 265-1318

FLORIDA
Clearwater
Conley and Assoc., Inc.
Phone: (813) 572-8895

Oviedo
Conley and Assoc., Inc.
Phone: (407) 365-3283

GEORGIA
Norcross
Elcom, Inc.
Phone: (404) 447-8200

ILLINOIS
Itasca
Philips Semiconductors
Phone: (708) 250-0050

Schaumburg
Micro-Tex, Inc.
Phone: (708) 885-8200

INDIANA
Indianapolis
Mohrfield Marketing, Inc.
Phone: (317) 546-6969

Kokomo
Philips Semiconductors
Phone: (317) 459-5355

MARYLAND
Columbia
Third Wave Solutions, Inc.
Phone: (410) 290-5990

MASSACHUSETTS
Chelmsford
JEBCO
Phone: (508) 256-5800

Westford
Philips Semiconductors
Phone: (508) 692-6211

MICHIGAN
Monroe
S-J Associates
Phone: (313) 242-0450

Novi
Philips Semiconductors
Phone: (810) 347-1700

MINNESOTA
Bloomington
High Technology Sales
Phone: (612) 844-9933

MISSOURI
Bridgeton
Centech, Inc.
Phone: (314) 291-4230

Raytown
Centech, Inc.
Phone: (816) 358-8100

NEW JERSEY
Toms River
Philips Semiconductors
Phone: (908) 505-1200
(908) 240-1479

NEW YORK
Ithaca
Bob Dean, Inc.
Phone: (607) 257-1111

Rockville Centre
S-J Associates
Phone: (516) 536-4242

Wappingers Falls
Philips Semiconductors
Phone: (914) 297-4074

Bob Dean, Inc.
Phone: (914) 297-6406

NORTH CAROLINA
Charlotte
Elcom, Inc.
Phone: (704) 543-1229

Greensboro
Elcom, Inc.
Phone: (919) 273-8887

Matthews
Elcom, Inc.
Phone: (704) 847-4323

OHIO
Columbus
S-J Associates, Inc.
Phone: (614) 885-6700

Kettering
S-J Associates, Inc.
Phone: (513) 298-7322

Solon
S-J Associates, Inc.
Phone: (216) 349-2700

Toledo
S-J Associates, Inc.
Phone: (419) 727-8051

OREGON
Beaverton
Philips Semiconductors
Phone: (503) 627-0110

Western Technical Sales
Phone: (503) 644-8860

PENNSYLVANIA
Erie
S-J Associates, Inc.
Phone: (216) 888-7004

Hatboro
Delta Technical Sales, Inc.
Phone: (215) 957-0600

Pittsburgh
S-J Associates, Inc.
Phone: (216) 349-2700

SOUTH CAROLINA
Greenville
Elcom, Inc.
Phone: (803) 370-9119

TENNESSEE
Dandridge
Philips Semiconductors
Phone: (615) 397-5053

TEXAS
Austin
Philips Semiconductors
Phone: (512) 339-9945

Synergistic Sales, Inc.
Phone: (512) 346-2122

Houston
Philips Semiconductors
Phone: (713) 999-1316

Synergistic Sales, Inc.
Phone: (713) 937-1990

Richardson
Philips Semiconductors
Phone: (214) 644-1610
(214) 705-9555

Synergistic Sales, Inc.
Phone: (214) 644-3500

UTAH
Salt Lake City
Electrodyne
Phone: (801) 264-8050

WASHINGTON
Bellevue
Western Technical Sales
Phone: (206) 641-3900

Spokane
Western Technical Sales
Phone: (509) 922-7600

WISCONSIN
Waukesha
Micro-Tex, Inc.
Phone: (414) 542-5352

CANADA
PHILIPS SEMICONDUCTORS CANADA, LTD.

Calgary, Alberta
Philips Semiconductors/
Components, Inc.
Phone: (403) 293-5969

Tech-Trek, Ltd.
Phone: (403) 241-1719

Kanata, Ontario
Philips Semiconductors
Phone: (613) 599-8720

Tech-Trek, Ltd.
Phone: (613) 599-8787

Montreal, Quebec
Philips Semiconductors/
Components, Inc.
Phone: (514) 424-7320

Mississauga, Ontario
Tech-Trek, Ltd.
Phone: (416) 238-0366

Richmond, B.C.
Tech-Trek, Ltd.
Phone: (604) 276-8735

Scarborough, Ontario
Philips Semiconductors/
Components, Ltd.
(416) 292-5161

Ville St. Laurent, Quebec
Tech-Trek, Ltd.
Phone: (514) 337-7540

MEXICO
Anzures Section
Philips Components
Phone: (800) 234-7381

El Paso, TX
Philips Components
Phone: (915) 775-4020

PUERTO RICO
Caguas
Mectron Group
Phone: (809) 746-3522

DISTRIBUTORS

Contact one of our local distributors:
Allied Electronics
Anthem Electronics
Arrow/Schweber Electronics
Future Electronics (Canada only)
Hamilton Hallmark
Marshall Industries
Newark Electronics
Richardson Electronics
Wyle Electronics
Zeus Electronics

03/30/95

©Philips Electronics North America Corporation 1995 Printed in U.S.A.

Philips Semiconductors - a worldwide company

Argentina: IEROD, Av. Juramento 1992 – 14.b (1428) BUENOS AIRES,
Tel. (541) 786 7633, Fax . (541) 786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02) 805 4455, Fax. (02) 805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01) 60 101-1236, Fax. (01) 60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40 783 749, Fax. (31)40 788 399

Brazil: Rua do Rocio 220 – 5th Floor, Suite 51
CEP: 04552-903 SÃO PAULO-SP, Brazil
P.O. Box 7383 (01064-970),
Tel. (011) 821-2333, Fax (011) 829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO,
Tel. (02) 773 816, Fax. (02) 777 6730

Colombia: IPRELENSO LTDA, Carrera 21 No. 56-17, 77621 BOGOTA,
Tel. (571)249 7624/(571)217 4609, Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. (032) 88 2636, Fax. (031) 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (9)0-50261, Fax. (9)0-520971

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 63 23, 20043 HAMBURG,
Tel. (040) 3296-0, Fax. (040) 3296 213

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01) 4894 339/4894 911, Fax. (01) 4814 240

Hong Kong: PHILIPS HONG KONG Ltd., 6/F Philips Ind. Bldg.,
24-28 Kung Yip St., KWAI CHUNG, N.T.,
Tel. (852)424 5121, Fax. (852)480 6960/480 6009

India: Philips INDIA Ltd., Shivsagar Estate, A Block,
Dr. Annie Besant Rd., Worli, BOMBAY 400 018,
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)640 000, Fax. (01)640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l.,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg. 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5028, Fax. (03)3740 0580

Korea (Republic of): Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)794-5011, Fax. (02)798-8022

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905,
Tel. 9-5 (800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB
Tel. (040)783749, Fax. (040)788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49, Fax. (021)577035/5874546

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. AntÓnio Loureiro Borges 5, Arquiparque – Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)4163160/4163333, Fax. (01)4163174/4163366

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road, Martindale, 2092 JOHANNESBURG,
P.O. Box 7430, Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (0)8-632 2000, Fax. (0)8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West Road,
Sec. 1. Taipeh, Taiwan ROC, P.O. Box 22978, TAIPEI 100,
Tel. (02)388 7666, Fax. (02)382 4382

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
BANGKOK 10260, Thailand
Tel. (662)398-0141, Fax. (662)398-3319

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 2770, Fax. (0212)282 6707

United Kingdom: Philips Semiconductors Ltd.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX
Tel. (0181)730-5000, Fax. (0181)754-8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax (02)92 0601

Internet: http://www.semiconductors.philips.com/ps/

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-p,
P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax +31-40-724825

SCD38 ©Philips Electronics N.V. 1995

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or industrial or intellectual property rights.

Printed in the USA

5170G/533051/21M/02/pp1648 (out of 4840) Date of release: 04-95

Document order number: 9397-750-00074

Philips Semiconductors

PHILIPS