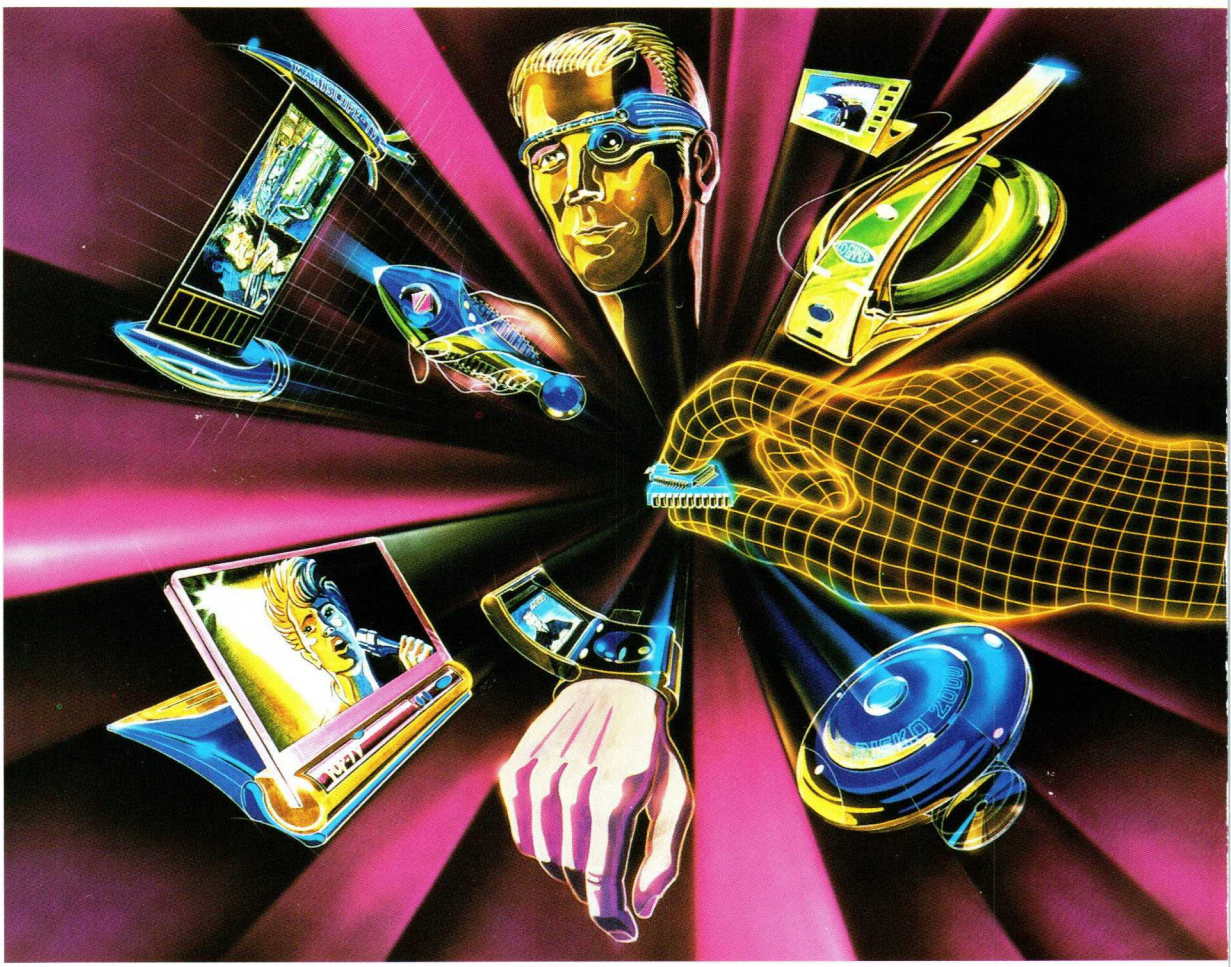
INTEGRATED CIRCUITS

Semiconductors for Television and Video Systems

TDA8416 to μA733; 733C



1995

DATA HANDBOOK IC02c

Philips
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Semiconductors for Television and Video Systems

CONTENTS

Page

PART A

SELECTION GUIDE
- Functional index 4
- Alphanumerical index 21

GENERAL
- Quality 36
- Rating systems 37
- Pro electron type numbering system of integrated circuits 39
- Handling MOS devices 41

DEVICE DATA
- 80/83C528 to TDA2555;TDA2557 44

PART B

SELECTION GUIDE
- Functional index 1588
- Alphanumerical index 1605

DEVICE DATA
- TDA2578A to TDA8415 1621

PART C

SELECTION GUIDE
- Functional index 3236
- Alphanumerical index 3253

DEVICE DATA
- TDA8416 to μA733;733C 3269

PACKAGE INFORMATION
- Package outlines 4789
- Soldering 4845

DATA HANDBOOK SYSTEM 4847

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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SELECTION GUIDE

	Page
Functional index	3236
Alphanumerical index	3253

		PAGE
TUNING/TUNER		
Tuning		
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8725T	Antenna signal processor	3785
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
TSA5527; TSA5527		
Tuner		
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BF547	NPN 1 GHz wideband transistor	128
BF747	NPN 1 GHz wideband transistor	133
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
SAA1300	Tuner switching circuit; I²C-bus	397
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701

		PAGE
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
Varicap		
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113

		PAGE
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BY229 series	Rectifier diodes fast, soft-recovery	156
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
Dual gate n-channel MOSFET		
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
IF		
Vision IF		
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301

		PAGE
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
Sound IF		
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
AM demodulator		
TDA9830	TV sound AM demodulator and audio source switch	4463
FM demodulator		
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
Nicam demodulator		
TDA8732	NICAM-728 demodulator (NIDEM)	3798

		PAGE
SOUND		
Sound decoding - Stereo decoder/dual language		
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
NICAM		
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SOUND		
Sound control		
TDA1029	Signal-sources switch	1461
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA9860	Universal hi-fi audio processor for TV	4607

		PAGE
Sound ADC		
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
SAD1009	Universal DAC (UDAC)	1395
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
Sound output		
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2905
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2907
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
VISION		
Colour decoding		
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027

		PAGE
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229

		PAGE
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA8395	SECAM decoder	3206
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4042
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I²C-bus	4148
TEA7650H	Video signal processor for CD-video/laser vision	4655
Video and high-speed ADC and DAC		
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636

		PAGE
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDF8704	8-bit high-speed analog-to-digital converter	4620
Memory based features		
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I²C-bus	1359
Scan conversion		
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
SAA4940H	NOise reduction IC	490
SAA7158	Back END IC	1033
Video output		
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
High voltage transistors		
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127

		PAGE
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
SYNC/DEFLECTION/SMPS		
Sync and deflection		
BY228	Parallel efficiency diode	155
BY328	32 kHz parallel efficiency diode	157
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYW54 to 56	Controlled avalanche rectifier diodes	166
TDA1082	East-west correction driver circuit	1475
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4820T	Sync separation circuit for video applications	2473
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112

		PAGE
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA9150B	Programmable deflection controller; I²C-bus	4065
TDA9151B	Programmable deflection controller; I²C-bus	4094
Power supply		
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Combi		
TDA4504B	Small signal combination for multistandard colour TV	2075
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
CONTROL		
Clock/calendar		
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8593	Low power clock calendar; I²C-bus	338
Display drivers		
PCF1303T	18-element bar graph LCD driver	271
PCF2116 family	LCD controller/drivers; I²C-bus	276
PCF2114X; PCF2116X		
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326

		PAGE
LED driver		
SAA1064	4-digit LED driver with I²C-bus interface	373
On Screen Display (OSD)		
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
Memories - SRAM		
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
EEPROM		
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
MICROCONTROLLERS		
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I²C-bus	62
84C44X/84C64X/84C84X	8-bit microcontrollers with OSD and VST; I²C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	83
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontroller for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266

		PAGE
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
Remote I/O expanders		
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8584	I²C-bus controller	331
TDA8722	I²C-bus programmable modulator for negative video modulation and FM sound	3766
Remote control transmitter		
PCA84C122; 222;422; 622; 822	8-bit microcontrollers for remote control transmitters	245
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
TELETEXT		
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859

		PAGE
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SATELLITE TV		
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8735	PLL frequency synthesizer; I²C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA 8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I²C-bus control	3860
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
PAY TV		
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
Miscellaneous		
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219

		PAGE
TDA6800; TDA6800T	Video modulator circuit	2893
TDA8442	I²C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I²C-bus	3443
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
μA733; 733C	Differential video amplifier	4782
VCR/Camera/Recorder		
SAA1101	Universal sync generator (USG)	385
SAA1310	Control interface for VHS video recorders	400
SAA4700	VPS data line processor; I²C-bus	472
SAA4700T	VPS data line processor; I²C-bus	481
SAD1009	Universal DAC (UDAC)	1395
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I²C-bus	1421
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA6800; TDA6800T	Video modulator circuit	2893
TDA9610H	Audio FM processor for VHS hi-fi audio; I²C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I²C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TEA7650H	Video signal processor for CD-video/laser vision	4655

		PAGE
MONITOR CIRCUITS		
Sync		
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
Deflection		
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
SMPS		
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Video control		
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
Miscellaneous		
TDA8442	I^2C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I^2C-bus	3443

ALPHANUMERICAL INDEX

		PAGE
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I²C-bus	62
84C44X; 84C64X; 84C84X	8-bit microcontrollers with OSD and VST; I²C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	83
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118

		PAGE
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127
BF547	NPN 1 GHz wideband transistor	128
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF747	NPN 1 GHz wideband transistor	133
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
BY228	Parallel efficiency diode	155
BY229 series	Rectifier diodes fast, soft-recovery	156
BY328	32 kHz parallel efficiency diode	157

		PAGE
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
BYW54 to 56	Controlled avalanche rectifier diodes	166
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontrollers for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C122; 222; 422; 622; 822	8-bit microcontrollers for remote control transmitters	245
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
PCF1303T	18-element bar graph LCD driver	271
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF2116 family	LCD controller/drivers; I²C-bus	276
PCF2114X; PCF2116X		
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297

		PAGE
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8584	I²C-bus controller	331
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
PCF8593	Low power clock calendar	338
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
SAA1064	4-digit LED-driver with I²C-bus interface	373
SAA1101	Universal sync generator (USG)	385
SAA1300	Tuner switching circuit; I²C-bus	397
SAA1310	Control interface for VHS video recorders	400
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
SAA4700	VPS data line processor; I²C-bus	472
SAA4700T	VPS data line processor; I²C-bus	481
SAA4940H	NOise reduction IC	490
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635

		PAGE
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027
SAA7158	Back END IC	1033
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I²C-bus	1359
SAD1009	Universal DAC (UDAC)	1395

		PAGE
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I²C-bus	1421
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA1029	Signal-sources switch	1461
TDA1082	East-west correction driver circuit	1475
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733

		PAGE
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4504B	Small signal combination multistandard colour TV	2075
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135

		PAGE
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490

		PAGE
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/ oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773

		PAGE
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
TDA6800; TDA6800T	Video modulator circuit	2893
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2095
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2097
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072

		PAGE
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TDA8395	SECAM decoder	3206
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8442	I²C-bus interface for colour decoders	3421
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8444	Octuple 6-bit DAC with I²C-bus	3443
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646

		PAGE
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8722	I^2C-bus programmable modulator for negative video modulation and FM sound	3766
TDA8725T	Antenna signal processor	3785
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8732	NICAM-728 demodulator (NIDEM)	3798
TDA8735	PLL frequency synthesizer; I^2C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I^2C-bus control	3860
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I^2C-bus	4042
TDA9150B	Programmable deflection controller; I^2C-bus	4065
TDA9151B	Programmable deflection controller; I^2C-bus	4094
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I^2C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I^2C-bus	4148
TDA9610H	Audio FM processor for VHS hi-fi audio; I^2C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I^2C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332

		PAGE
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TDA9830	TV sound AM demodulator and audio source switch	4463
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TDA9860	Universal hi-fi audio processor for TV	4607
TDF8704	8-bit high-speed analog-to-digital converter	4620
TDF8712	8-bit digital-to-analog converters	3711
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
TEA7650H	Video signal processor for CD-video/laser vision	4655
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A; TSA5527; TSA5527A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
µA733; 733C	Differential video amplifier	4782

DEVICE DATA

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8416 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8416 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_O	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

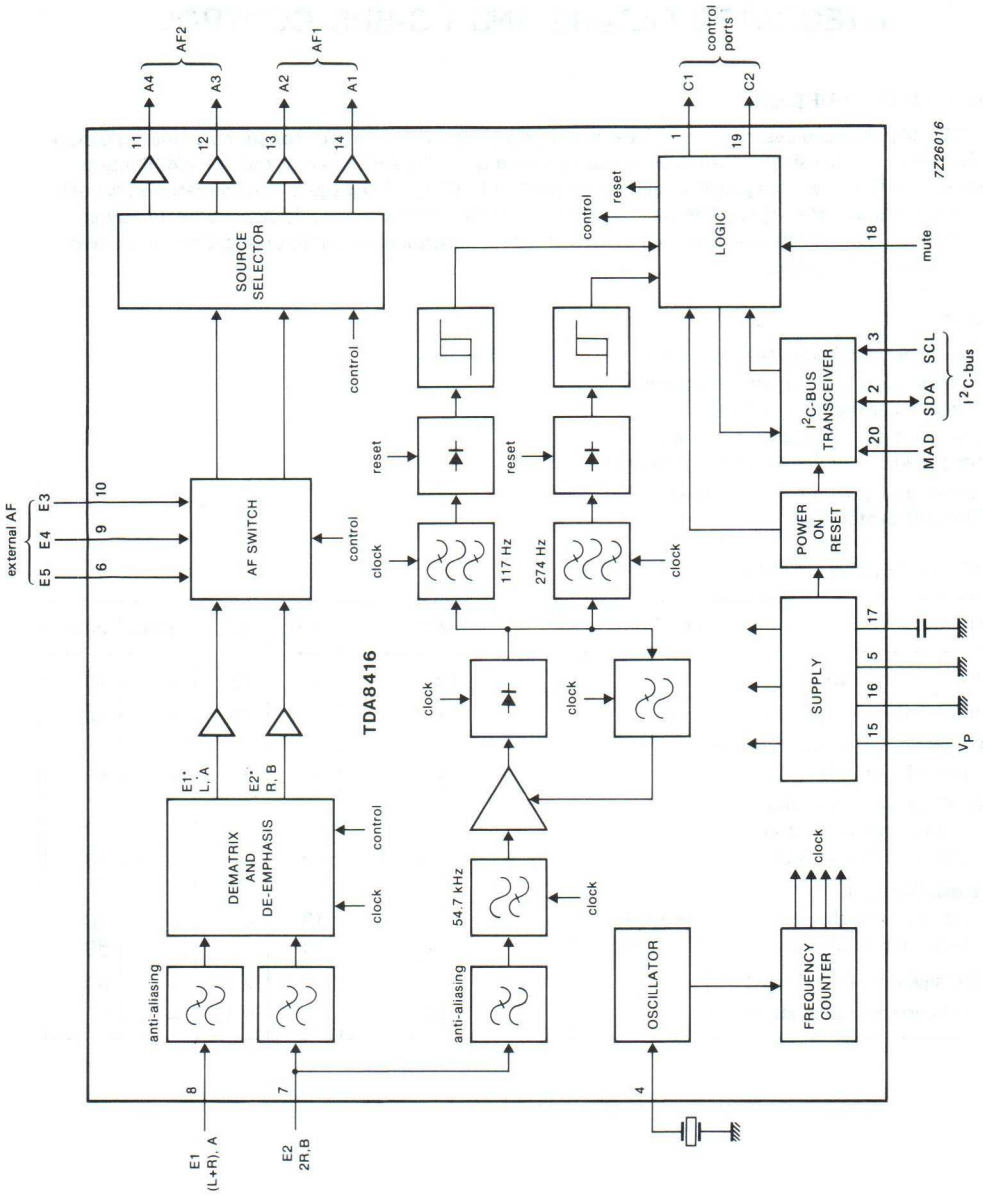


Fig. 1 Block diagram.

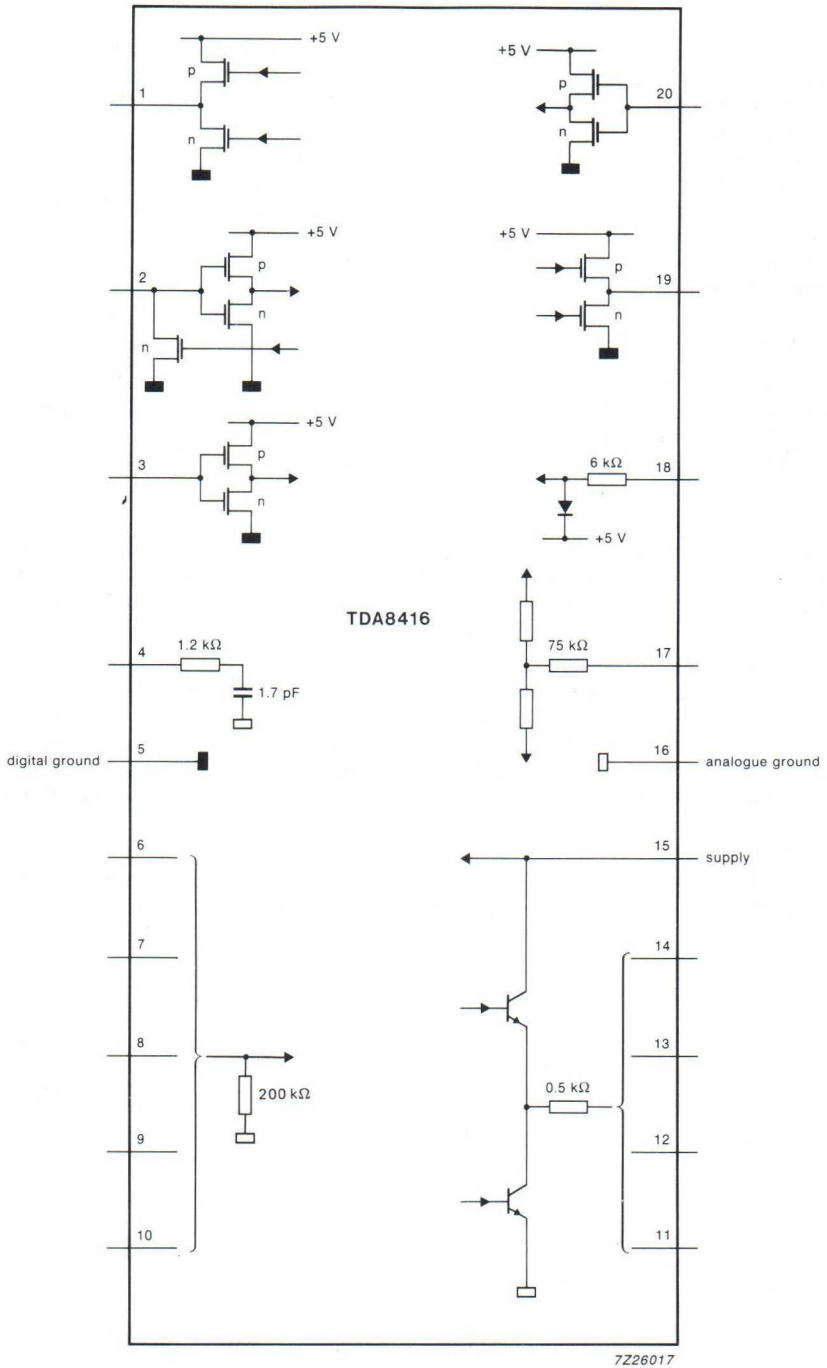


Fig.2 Input and output loading diagram.

PINNING

1 Control port C1
2 SDA, serial data line (I^2C-bus)
3 SCL, serial clock line (I^2C-bus)
4 Oscillator input (or quartz)
5 Digital ground (0 V)
6 External AF input (E5)
7 Sound channel input AF2 (E2)
8 Sound channel input AF1 (E1)
9 External AF input (E4)
10 External AF input (E3)
11 Output A4 AF 2 output
12 Output A3 AF 2 output
13 Output A2 AF 1 output
13 Output A1 AF 1 output
15 Supply voltage V_P
16 Analogue ground (0 V)
17 Ripple rejection improvement
18 Mute input
19 Control port C2
20 Module address (MAD)

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

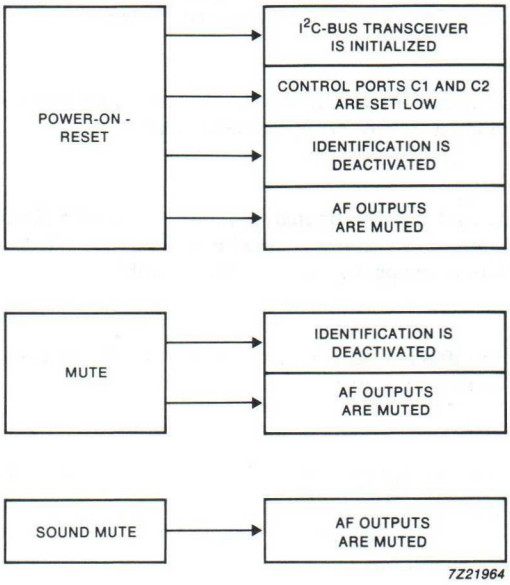


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8416 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

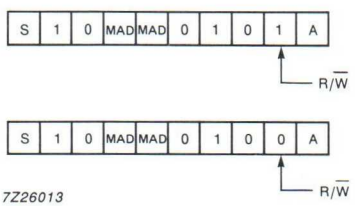
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8416

The TDA8416 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8416 is to be read from (status register) or written to (switch register or mute and port control register).



7Z26013

Read from (TDA8416 is a slave transmitter)

Write to (TDA8416 is a slave receiver)

Where:

S = start bit
A = acknowledge bit
MAD = module address bit

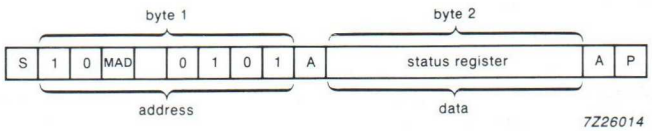
The MAD input (pin 20) allows the TDA8416 to operate from two different addresses:

MAD = LOW => A3 = A4 = 0 -> slave address = 1000 010
MAD = HIGH => A3 = A4 = 1 -> slave address = 1011 010

Fig.4 Address byte.

Reading the TDA8416

Reading the TDA8416 means reading the status register and the data stream will have the format as illustrated in Fig.5.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

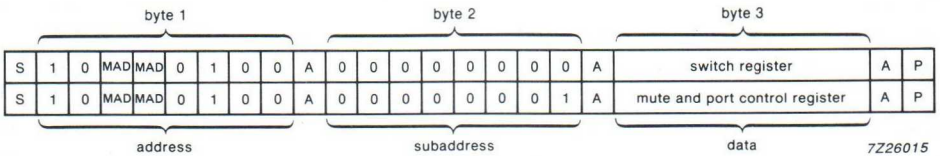
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8416

Writing to the TDA8416 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

DEVELOPMENT DATA

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	E5	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	—	—	—	—	—	—	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	—	—	—	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	—	—	—	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	—	—	—	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	—	—	—	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	—	—	—	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	—	—	—	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	—	—	—	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	—	—	—	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	—	—	—	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	—	—	—	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	—	—	—	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	—	—	—	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	—	—	—	E3	E4	—	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	—	—	—	E3	E4	—	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	—	—	—	E3	E4	—	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	—	—	—	E3	E4	—	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	—	—	—	E3	E4	—	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	—	—	—	E3	E4	—	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	—	—	—	E3	E4	—	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	—	—	—	E3	E4	—	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	—	—	—	E3	E4	—	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)
	—	—	—	—	—	E5	E5	E5	E5	E5	1	0	0	0	0	0	0	0	(80)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 6 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA
MAD (pin 20)						
Input voltage LOW		V_{20-5}	–	–	2.0	V
Input voltage HIGH		V_{20-5}	3.0	–	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 6, 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

DEVELOPMENT DATA

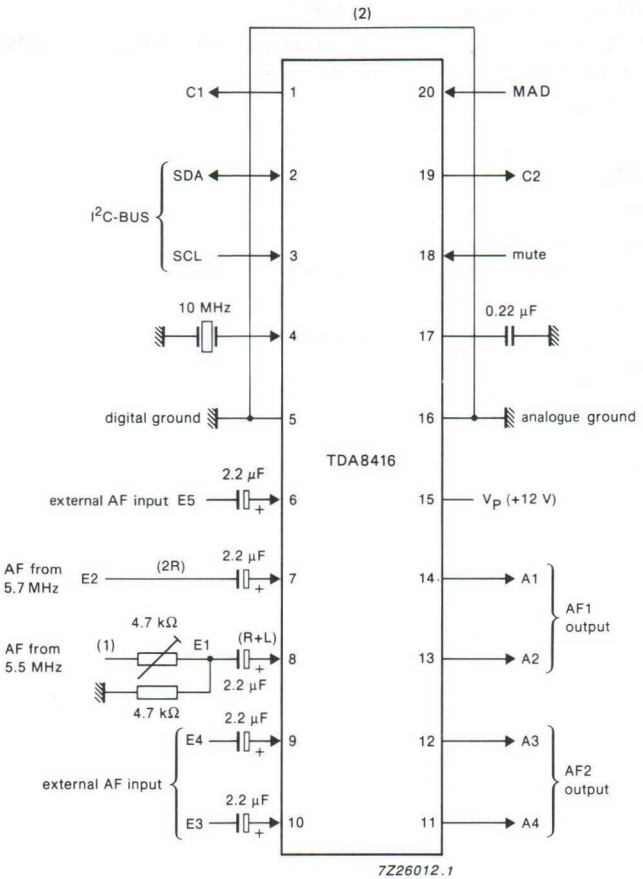
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I^2C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_O = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

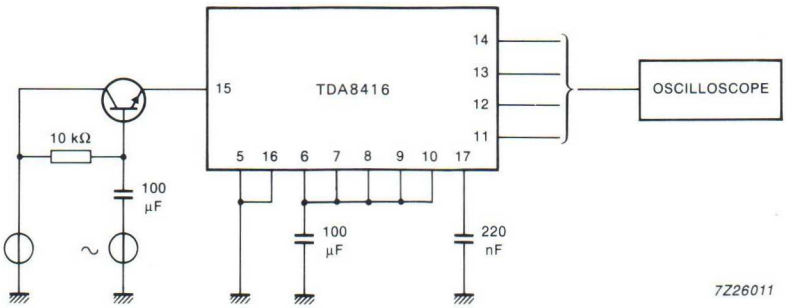
DEVELOPMENT DATA



(1) This potentiometer has to be adjusted to achieve the best stereo separation.

(2) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

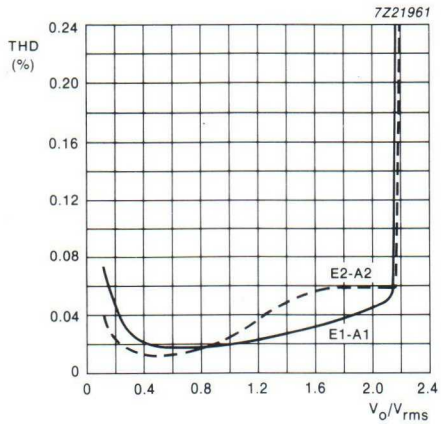


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8417 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8417 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

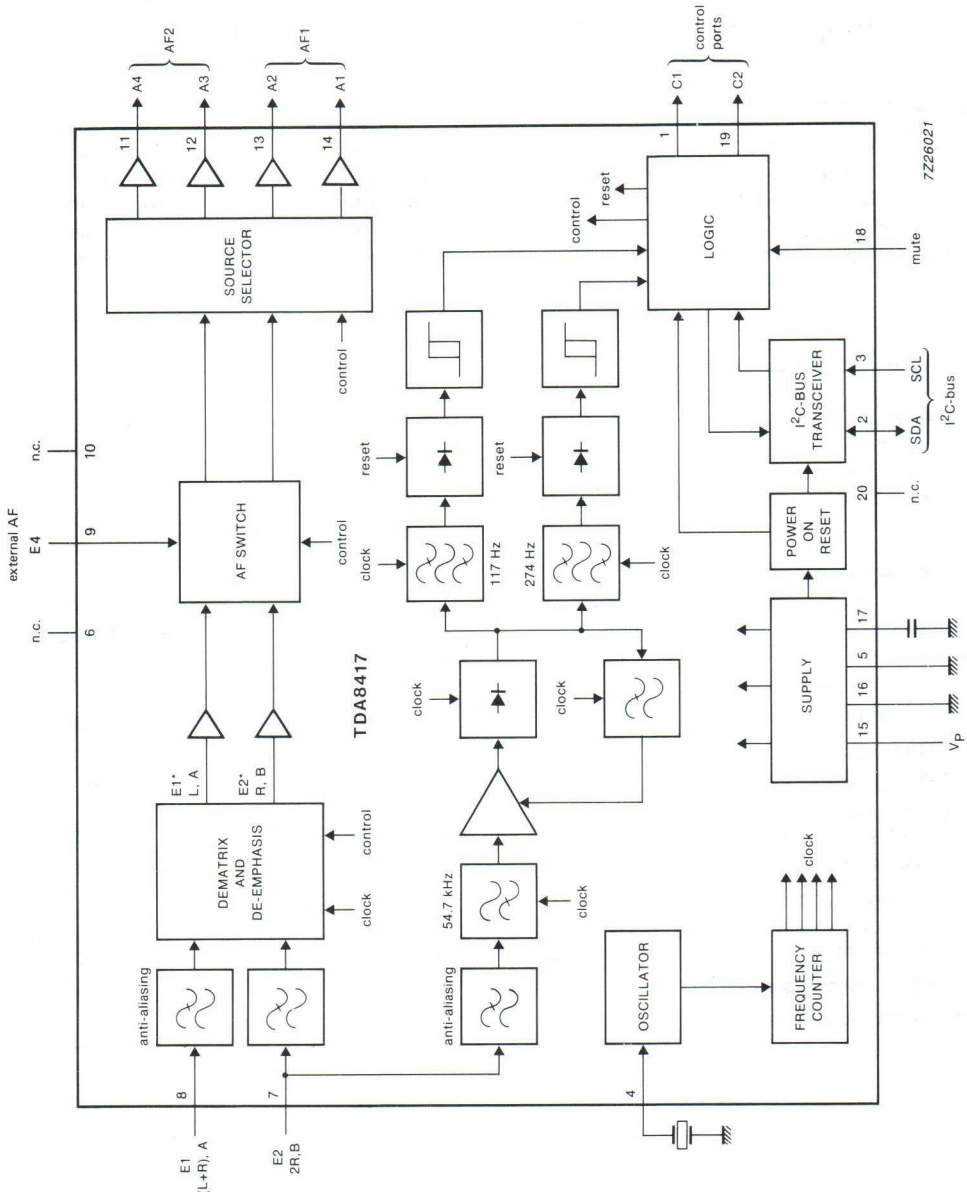


Fig.1 Block diagram.

DEVELOPMENT DATA

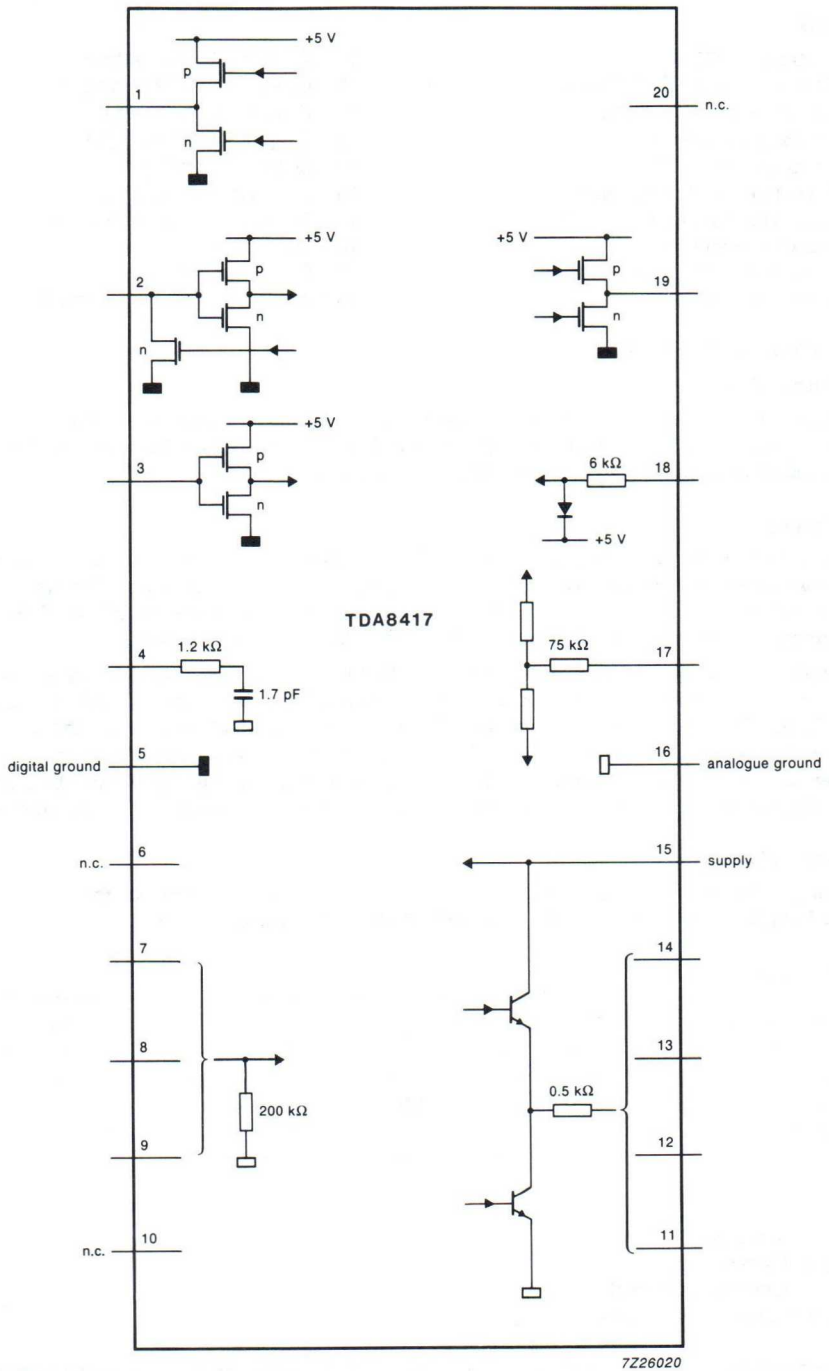


Fig.2 Input and output loading diagram.

PINNING

1 Control port C1
2 SDA, serial data line (I^2C-bus)
3 SCL, serial clock line (I^2C-bus)
4 Oscillator input (or quartz)
5 Digital ground (0 V)
6 Not connected, but reserved
7 Sound channel input AF2 (E2)
8 Sound channel input AF1 (E1)
9 External AF input (E4)
10 Not connected, but reserved
11 Output A4 AF 2 output
12 Output A3 AF 2 output
13 Output A2 AF 1 output
13 Output A1 AF 1 output
15 Supply voltage V_P
16 Analogue ground (0 V)
17 Ripple rejection improvement
18 Mute input
19 Control port C2
20 Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

FUNCTIONAL DESCRIPTION (continued)

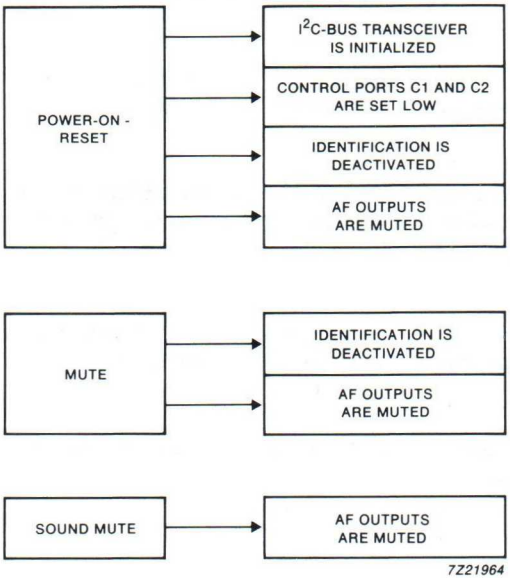


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8417 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

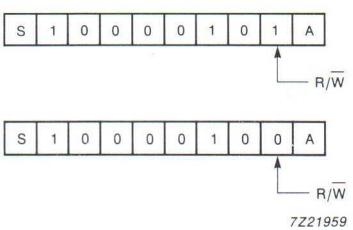
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8417

The TDA8417 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8417 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8417 is a slave transmitter)

Write to (TDA8417 is a slave receiver)

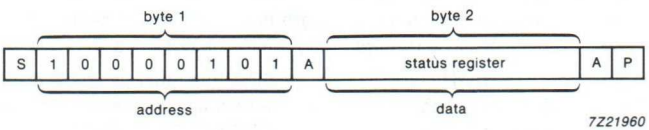
Where:

S = start bit
A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8417

Reading the TDA8417 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

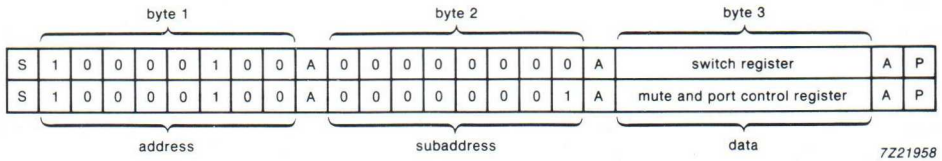
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8417

Writing to the TDA8417 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

DEVELOPMENT DATA

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 9)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

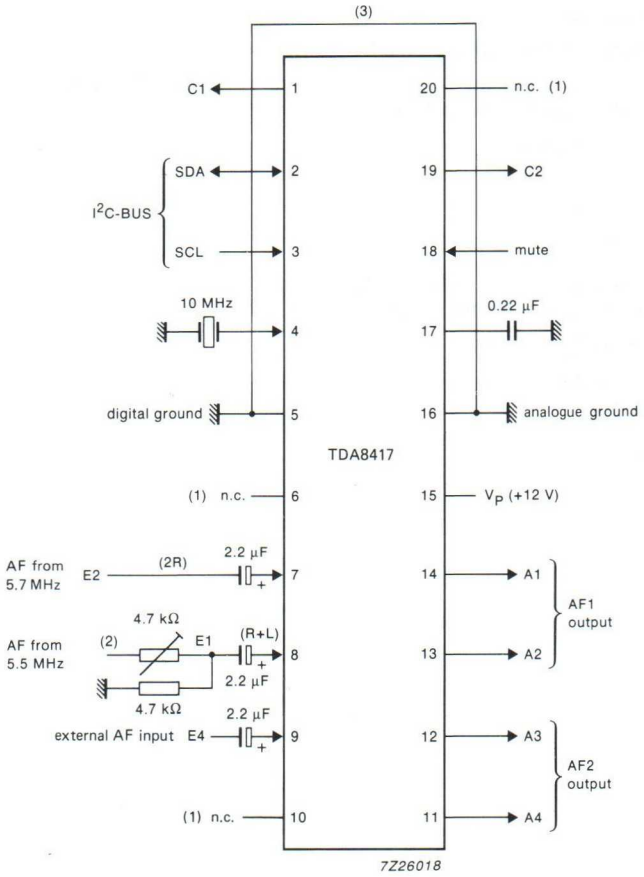
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_o = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

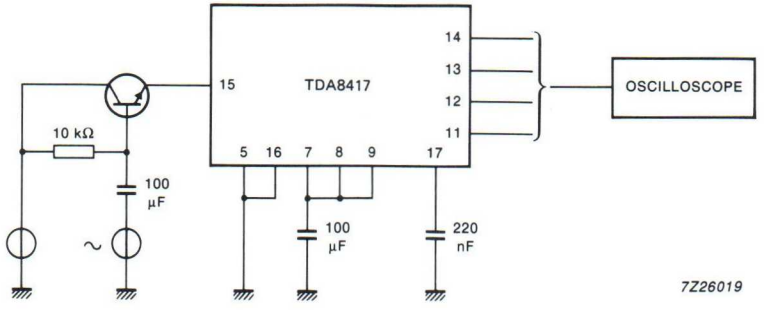


(1) These pins are not connected internally and should not be connected on the printed-circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

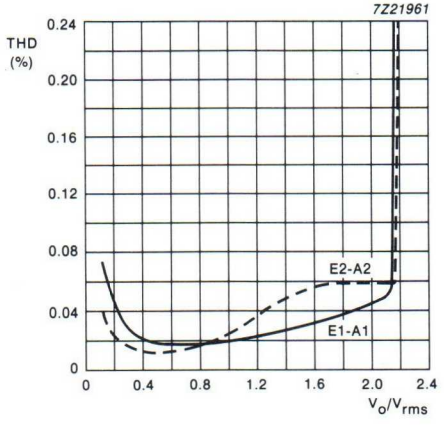


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

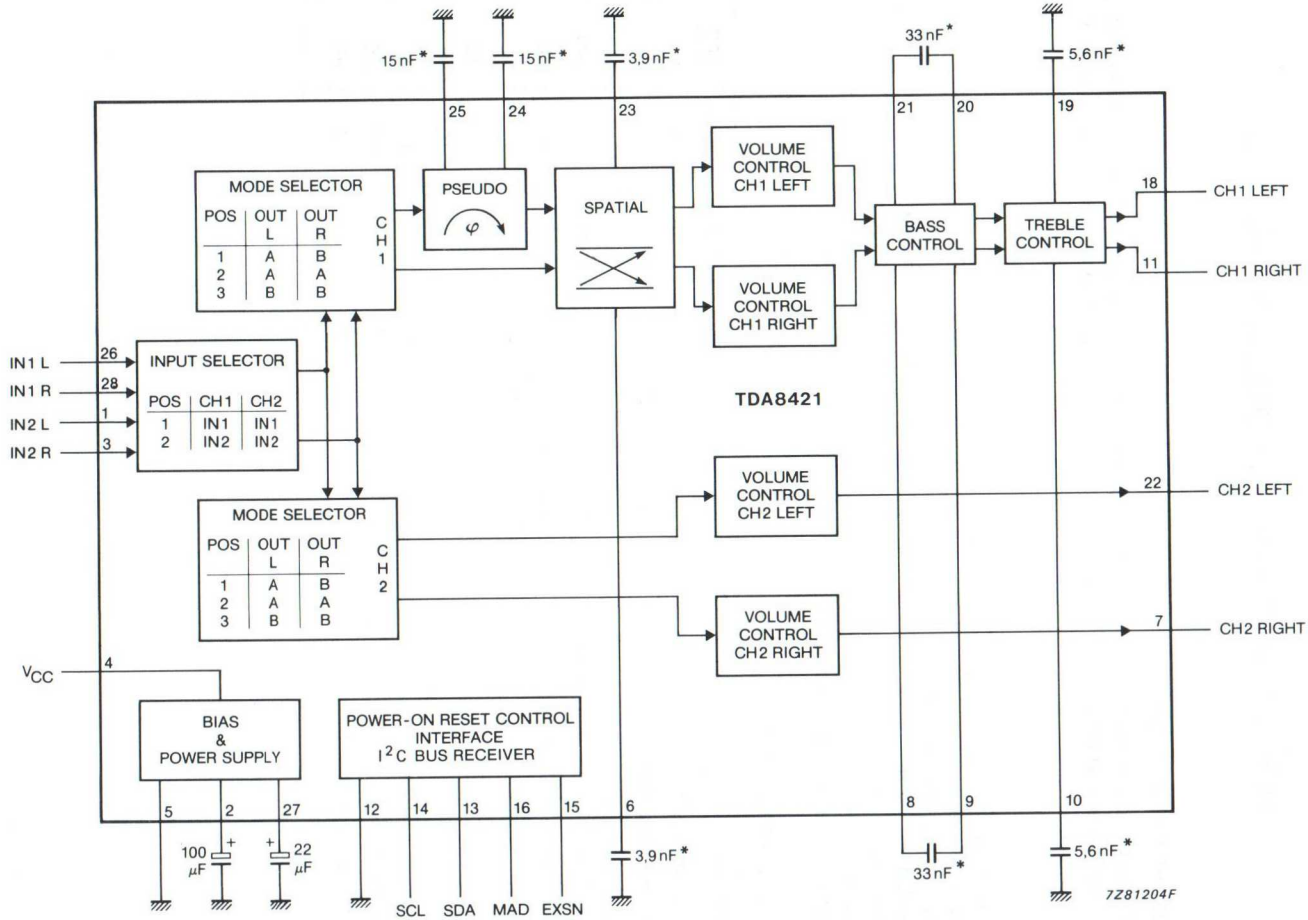


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

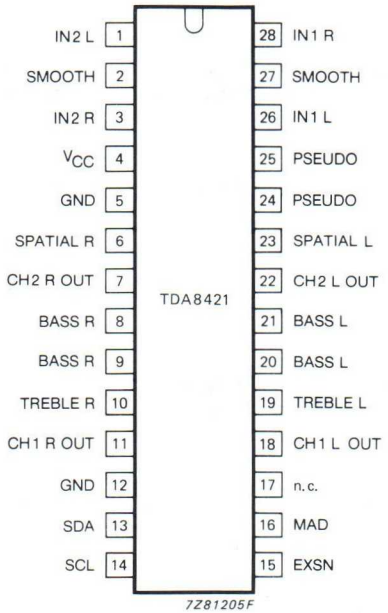


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

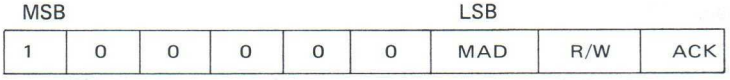


Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
CH2	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

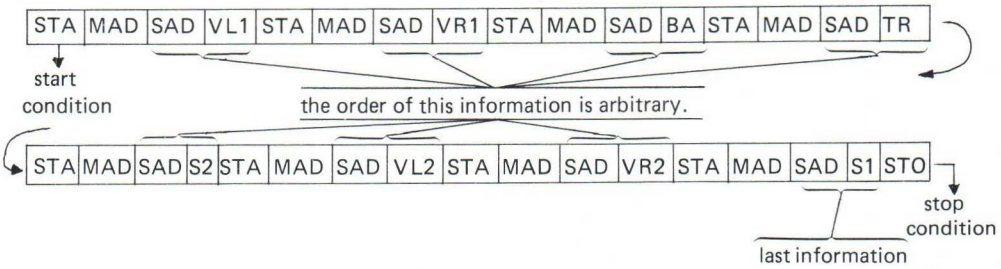


Fig. 4 Data transmission after a power-on reset.

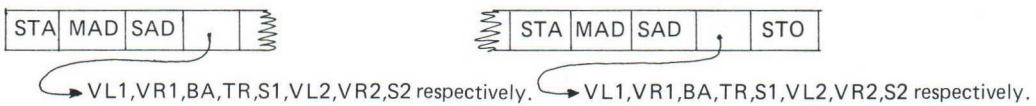


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	150	°C
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift (see Fig. 15)					

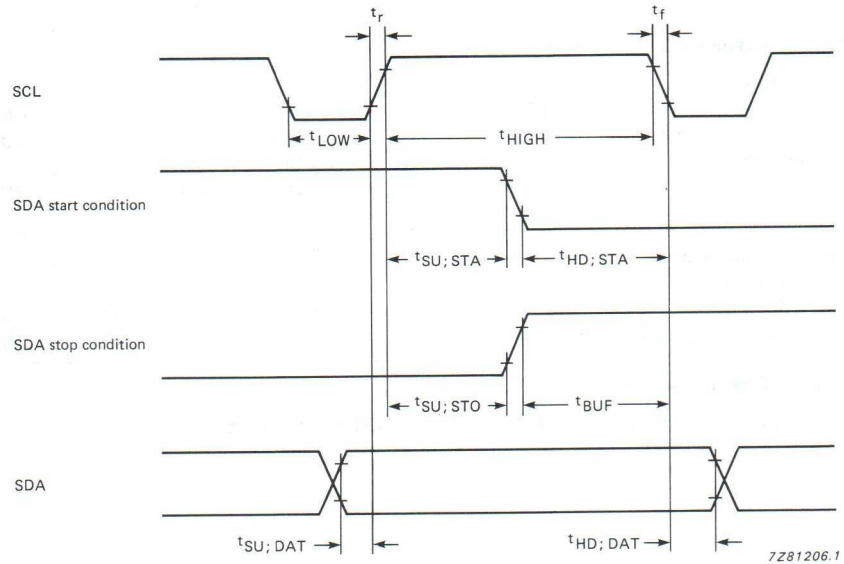
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time
t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

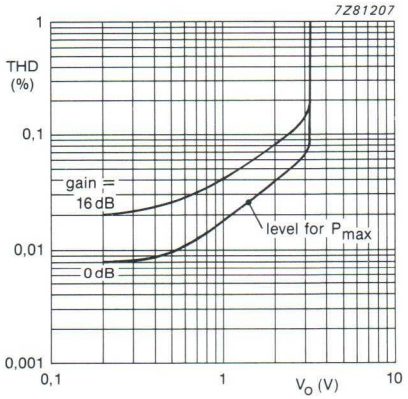


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

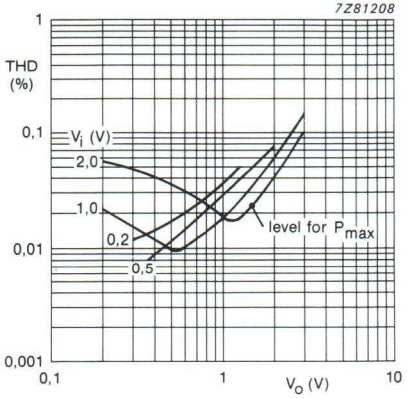


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

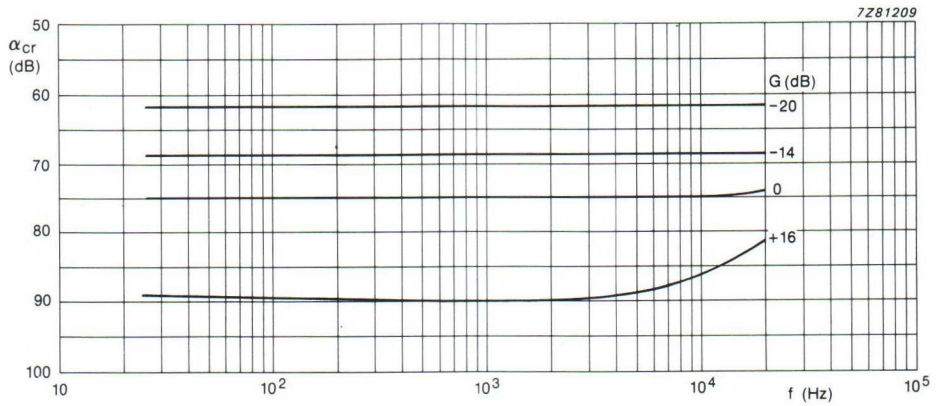


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

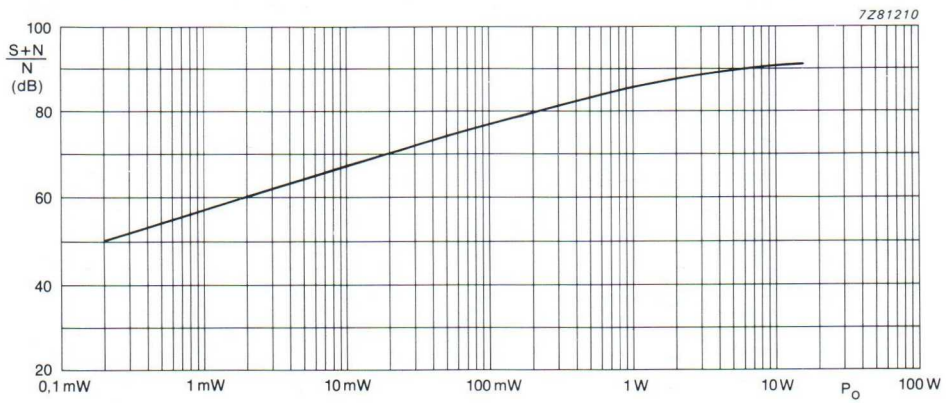


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

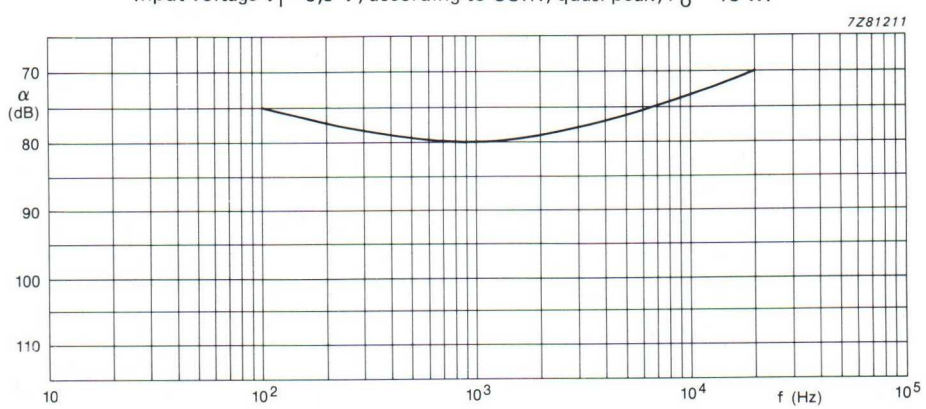


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

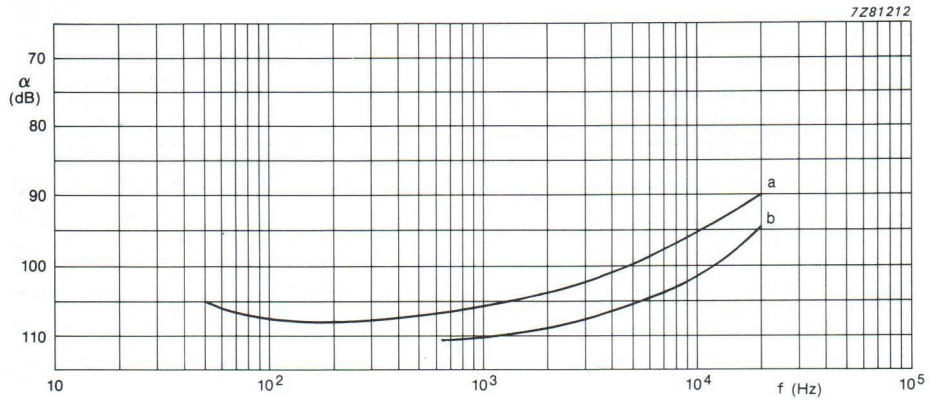


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

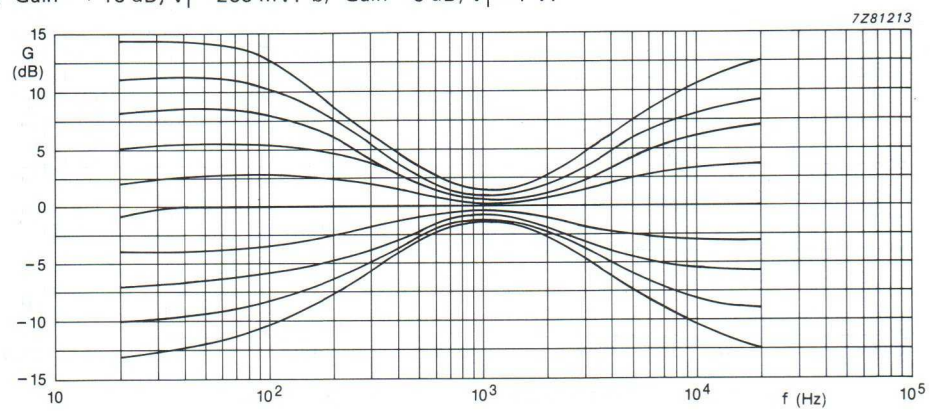


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

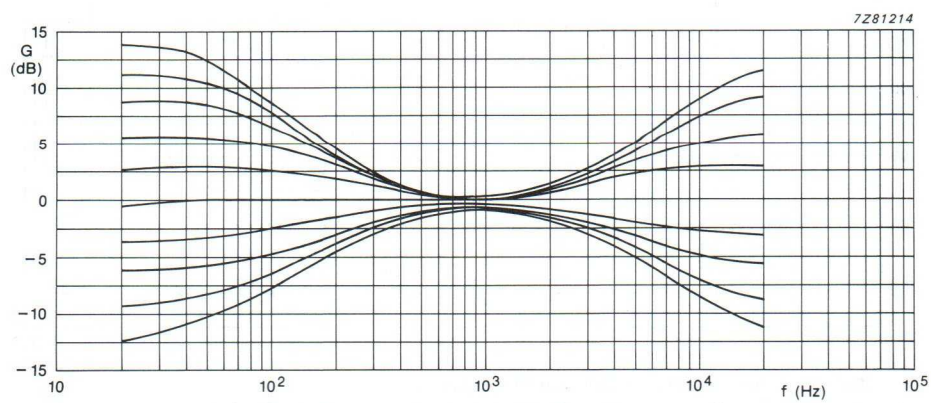
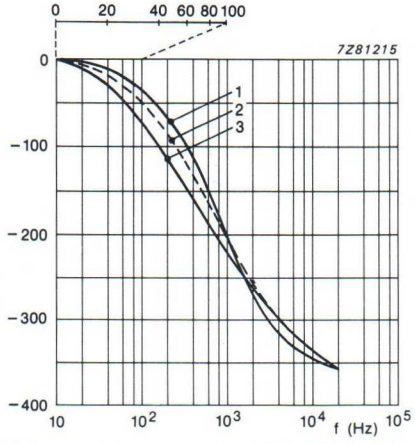


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

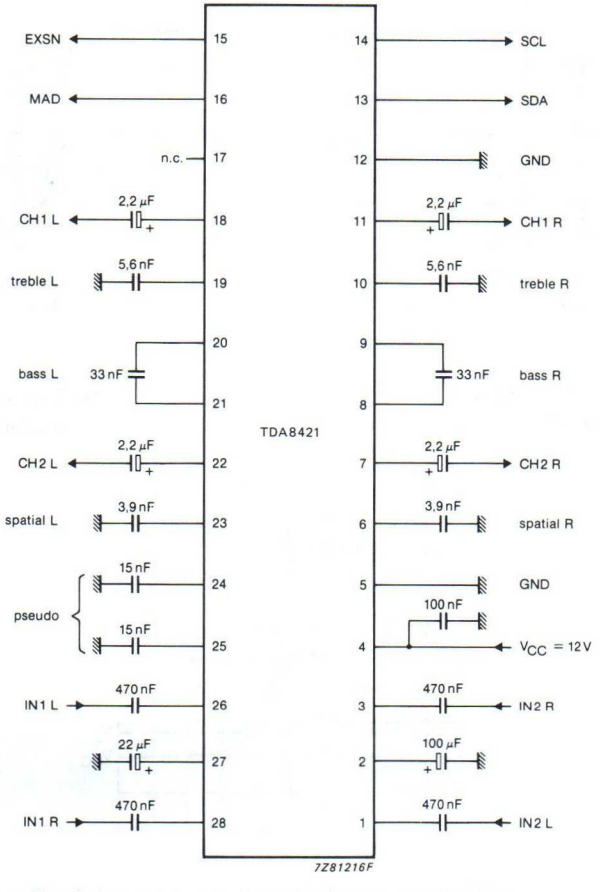
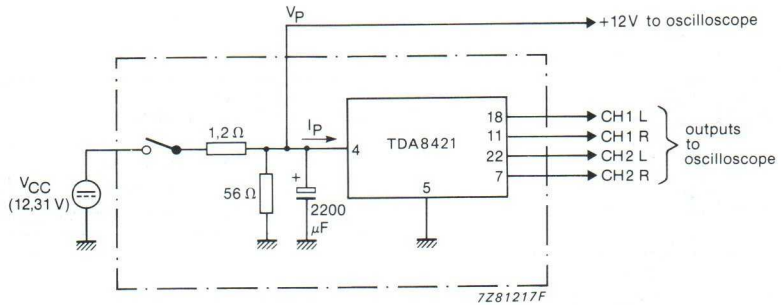


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

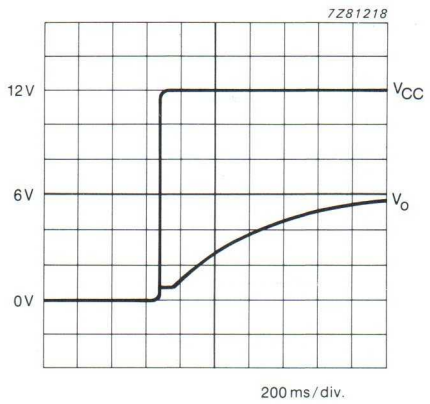


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

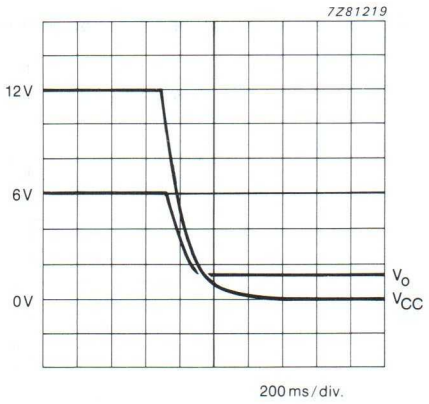


Fig. 19 Turn-off behaviour;
without modulation.

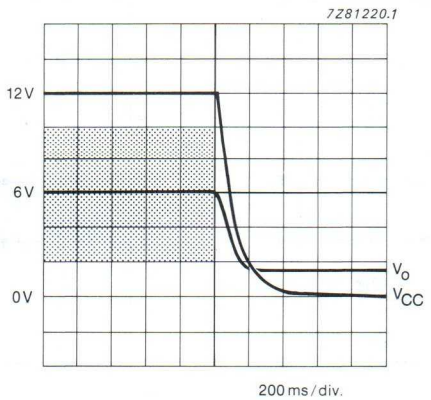


Fig. 20 Turn-off behaviour; with modulation (shaded area).

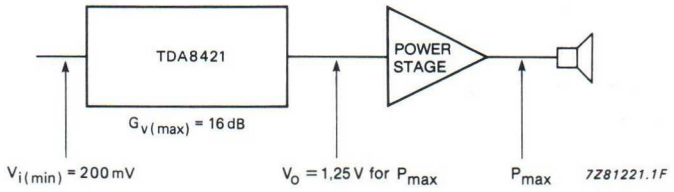


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

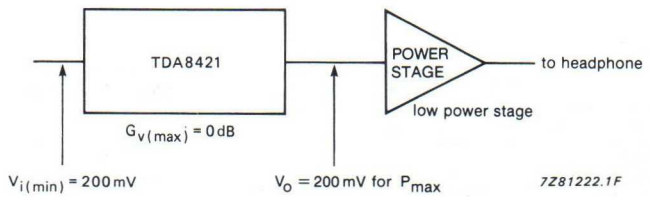


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Hi-Fi stereo audio processor; I²C-bus TDA8424

FEATURES

- Mode selector
- Spatial stereo, stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

GENERAL DESCRIPTION

The TDA8424 is monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage (pin 4)	10.8	12.0	13.2	V
V_I	input signal handling	2	–	–	V
V_i	input sensitivity with full power at the output stage	–	300	–	mV
(S+N)/N	signal plus noise-to-noise ratio	–	86	–	dB
THD	total harmonic distortion	–	0.05	–	%
α_{cs}	channel separation	–	80	–	dB
G_{vol}	volume control range	–64	–	+6	dB
G_{tre}	treble control range	–12	–	+12	dB
G_{bass}	bass control range	–12	–	+15	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8424	20	DIL	plastic	SOT146

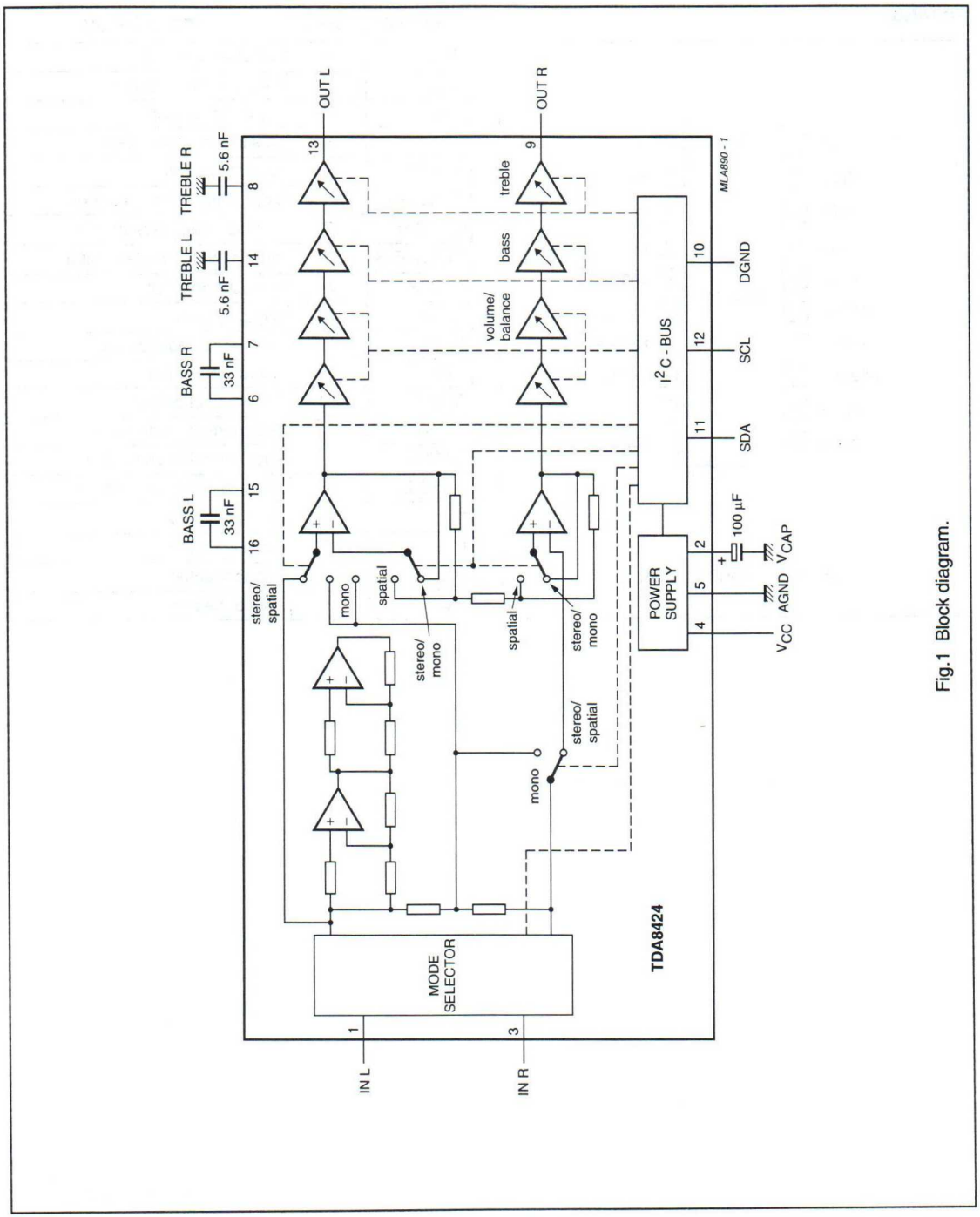


Fig.1 Block diagram.

PINNING

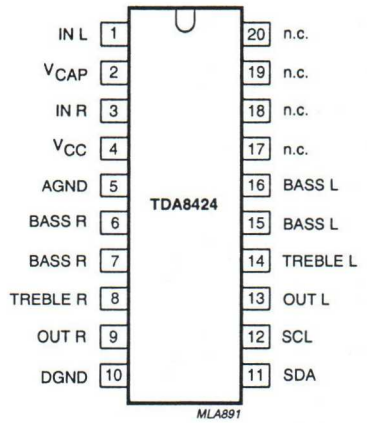


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
IN L	1	left channel input
V_{CAP}	2	decoupling capacitor
IN R	3	right channel input
V_{CC}	4	positive supply voltage
AGND	5	analog ground
BASS R	6	right channel bass control
BASS R	7	right channel bass control
TREBLE R	8	right channel treble control
OUT R	9	right channel output
DGND	10	digital ground
SDA	11	serial data input/output
SCL	12	serial clock input
OUT L	13	left channel output
TREBLE L	14	left channel treble control
BASS L	15	left channel bass control
BASS L	16	left channel bass control
n.c.	17	not connected
n.c.	18	not connected
n.c.	19	not connected
n.c.	20	not connected

FUNCTIONAL DESCRIPTION

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bi-lingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of ≥ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Stereo, spatial stereo and forced mono mode

It is possible to select three modes: stereo, spatial stereo or forced mono. The spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from +12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8424 includes a bias and power supply stage, which generates a voltage of $0.5V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I²C-bus receiver and data handling

BUS SPECIFICATION

The TDA8424 is controlled via the 2-wire I²C-bus by a microcontroller.
The two wires (SDA - serial data, SCL - serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock on the SCL line is LOW. The set-up and hold times are specified in the AC CHARACTERISTICS.
A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered free again after a stop condition.

Module address

Data transmission to the TDA8424 starts with the module address MAD.

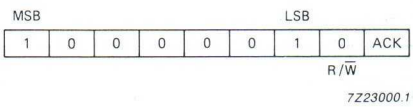


Fig.3 TDA8424 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8424. Table 1 defines the coding of the second byte after the module address MAD.

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig.5).

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
FUNCTION	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Volume left	0	0	0	0	0	0	0	0
Volume right	0	0	0	0	0	0	0	1
Bass	0	0	0	0	0	0	1	0
Treble	0	0	0	0	0	0	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
Switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8424. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

		MSB							LSB
FUNCTION		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Volume left	VL	1	1	V05	V04	V03	V02	V01	V00
Volume right	VR	1	1	V15	V14	V13	V12	V11	V10
Bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
Treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
Switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	1

Truth tables

Tables 3, 4 and 5 are truth tables for the switch functions

Table 3 Mode selector

FUNCTION	ML1	ML0	IS
Stereo	1	1	1*
Sound A	0	1	1*
Sound B	1	0	1*

* Must be set to logic 1

Table 4 Stereo/spatial stereo/forced mono

CHOICE	STL	EFL
Spatial stereo	1	1
Stereo	1	0
Forbidden status	0	1
Forced mono	0	0

Table 5 Mute

MUTE	MU
Active; automatic after POR	1
Not active	0

Where: POR = Power-on reset.

Tables 6, 7 and 8 are truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/STEP (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
2	1	1	1	1	0	1
0	1	1	1	1	0	0
−2	1	1	1	0	1	1
−4	1	1	1	0	1	0
−6	1	1	1	0	0	1
−8	1	1	1	0	0	0
−10	1	1	0	1	1	1
−20	1	1	0	0	1	0
−30	1	0	1	1	0	1
−40	1	0	1	0	0	0
−50	1	0	0	0	1	1
−60	0	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
−80	0	1	1	0	1	1

Table 7 Bass control

3 dB/STEP (dB)	BA3	BA2	BA1	BA0
15	1	0	1	1
12	1	0	1	0
9	1	0	0	1
6	1	0	0	0
3	0	1	1	1
0	0	1	1	0
–3	0	1	0	1
–6	0	1	0	0
–9	0	0	1	1
–12	0	0	1	0

Table 8 Treble control

3 dB/STEP (dB)	TR3	TR2	TR1	TR0
12	1	0	1	0
9	1	0	0	1
6	1	0	0	0
3	0	1	1	1
0	0	1	1	0
–3	0	1	0	1
–6	0	1	0	0
–9	0	0	1	1
–12	0	0	1	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

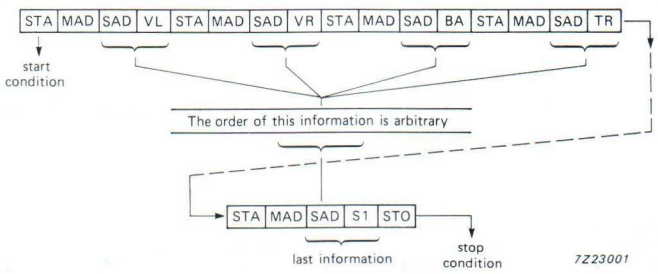


Fig.4 Data transmission after a power-on reset.

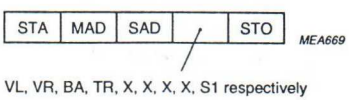


Fig.5 Data transmission after a power-on reset with auto increment.

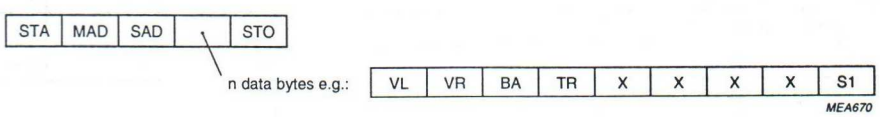


Fig.6 Data transmission except after a power-on reset.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	0	16	V
V_{cap}	voltage range for pins with external capacitors	0	V_{CC}	V
$V_{SDA, SCL}$	voltage range for pins 11 and 12	0	V_{CC}	V
$V_{I/O}$	voltage range at pins 1, 3, 9, 11, 12 and 13	0	V_{CC}	V
I_O	output current at pins 9 and 13	–	45	mA
P_{tot}	total power dissipation at $T_{amb} < 70$ °C	–	450	mW
T_{amb}	operating ambient temperature range	0	+70	°C
T_{stg}	storage temperature range	–25	+150	°C
V_{stat}	electrostatic handling	see note		

Note

Electrostatic handling Human body model: C = 100 pF, R = 1.5 kΩ and V ≥ 3 kV; charge device model: C = 200 pF, R = 0 Ω and V ≥ 400 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage range		10.8	12.0	13.2	V
I_{CC}	supply current	at V_{CC} = 12 V	–	26	35	mA
V_{ref}	internal reference voltage		5.4	$0.5V_{CC}$	6.6	V
V_I	internal voltage at pins 1 and 3	DC voltage internally generated; capacitive coupling recommended	–	V_{ref}	–	V
V_O	internal voltage at pins 9 and 13		–	V_{ref}	–	V
SDA; SCL (pins 11 and 12)						
V_{IH}	HIGH level input voltage		3.0	–	V_{CC}	V
V_{IL}	LOW level input voltage		–3.0	–	1.5	V
I_{IH}	HIGH level input current		–	–	+10	µA
I_{IL}	LOW level input current		–10	–	–	µA
	output voltage at pins with external capacitors					
$V_{cap.n}$	pins 6 to 8, 14 to 16		–	V_{ref}	–	V
$V_{cap.2}$	pin 2		–	V_{CC}–0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; stereo mode; spatial stereo off; R_L > 10 kΩ; C_L < 1000 pF; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.7)						
SDA, SCL (PINS 11 AND 12)						
f_{SCL}	clock frequency range		0	–	100	kHz
t_{HIGH}	clock HIGH period		4	–	–	µs
t_{LOW}	clock LOW period		4.7	–	–	µs
t_r	SCL rise time		–	–	1	µs
t_f	SCL fall time		–	–	0.3	µs
$t_{SU;STA}$	set-up time for start condition		4.7	–	–	µs
$t_{HD;STA}$	hold time for start condition		4	–	–	µs
$t_{SU;STO}$	set-up time for stop condition		4.7	–	–	µs
t_{BUF}	time bus must be free before a new transmission can start		4.7	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
Inputs						
IN L (PIN 1) IN R (PIN 3)						
$V_{i(RMS)}$	input signal handling (RMS value)	at V_u = −12 dB; THD ≤ 0.5%	2	–	–	V
R_i	input resistance		20	30	40	kΩ
f	frequency response (0.5 dB)		20	–	20 000	Hz
Outputs						
OUT R (PIN 9) OUT L (PIN 13)						
$V_{o(RMS)}$	output voltage range (RMS value)	at $V_{i(max)}$ ≤ 2 V; THD ≤ 0.7%	0.6	–	–	V
R_L	load resistance		10	–	–	kΩ
Z_O	output impedance		–	–	100	Ω
(S+N)/N	signal plus noise-to-noise ratio	weighted in accordance with CCIR 468-2; V_o = 600 mV				
	gain = 6 dB		–	78	–	dB
	gain = 0 dB		–	86	–	dB
	gain ≤ −20 dB		–	68	–	dB
THD	total harmonic distortion	f = 20 Hz to 12.5 Hz				
	gain = +6 dB to −40 dB	$V_{i(RMS)}$ = 0.3 V	–	0.05	–	%
	gain = 0 dB to −40 dB	$V_{i(RMS)}$ = 0.6 V	–	0.07	0.4	%
	gain = −12 dB to −40 dB	$V_{i(RMS)}$ = 2.0 V	–	0.1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
α_{cs}	channel separation at 10 kHz	gain = 0 dB	–	80	–	dB
RR_{100}	ripple rejection	f_{ripple} = 100 Hz; $V_{r(RMS)}$ < 200 mV gain = 0 dB	–	50	–	dB
α_L	crosstalk attenuation from logic inputs to AF outputs	gain = 0 dB	–	100	–	dB
Volume control (see Table 6)						
	control range (36 steps)	f = 1 kHz				
G_{max}	maximum voltage gain	6 dB step	5	6	–	dB
G_{min}	mimimum voltage gain	–64 dB step	–63	–64	–	dB
G_{mute}	mute position		–80	–90	–	dB
G_{err}	gain tracking error; balance in mid-position		–	–	2	dB
G_{step}	step resolution					
	gain from +6 dB to –40 dB		1.5	2.0	2.5	dB/step
	gain from –42 dB to –64 dB		1.0	2.0	3.0	dB/step
Treble control (see Table 8)						
	control range	C_{8-5}; C_{14-5} = 5.6 nF				
G_{emp}	maximum emphasis at 15 kHz with respect to linear position		11	12	13	dB
G_{att}	maximum attenuation at 15 kHz with respect to linear position		11	12	13	dB
G_{step}	resolution		2.5	3.0	3.5	dB/step
Bass control (see Table 7)						
	control range	C_{6-7}; C_{15-16} = 33 nF				
G_{emp}	maximum emphasis at 40 Hz with respect to linear position		14	15	16	dB
G_{att}	maximum attenuation at 40 Hz with respect to linear position		11	12	13	dB
G_{step}	resolution		2.5	3.0	3.5	dB/step
Spatial function						
α	antiphase crosstalk		–	52	–	%

Note to the AC characteristics

1. Balance is obtained via software by different volume settings in both channels (left and right).

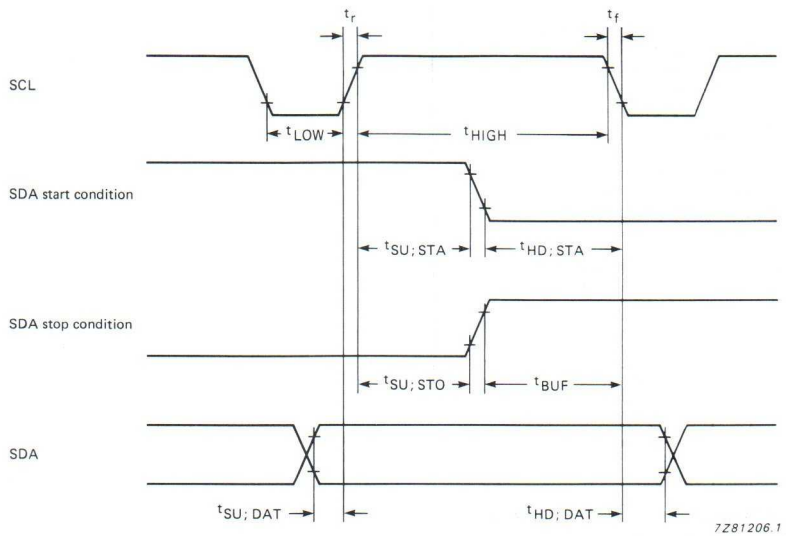


Fig.7 Timing requirements for I²C-bus.

Where:

$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.
t_{BUF} = bus free time.

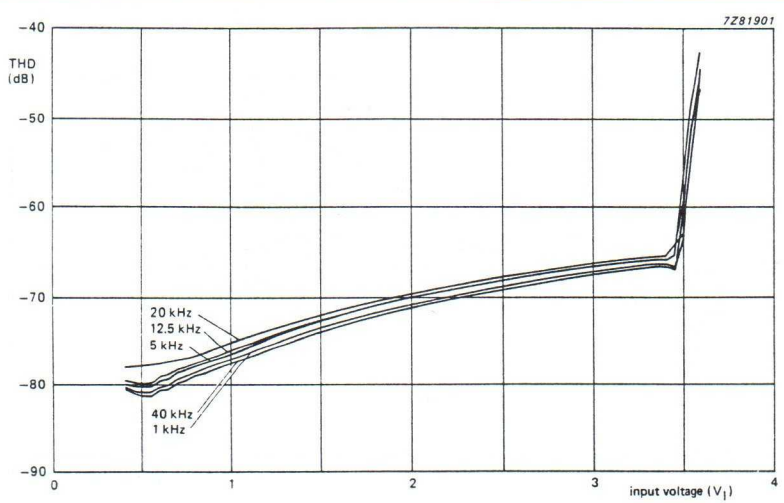


Fig.8 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

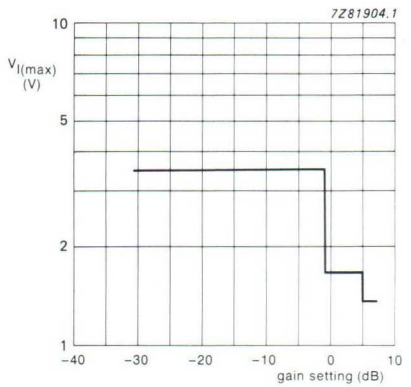


Fig.9 Input signal handling capability plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

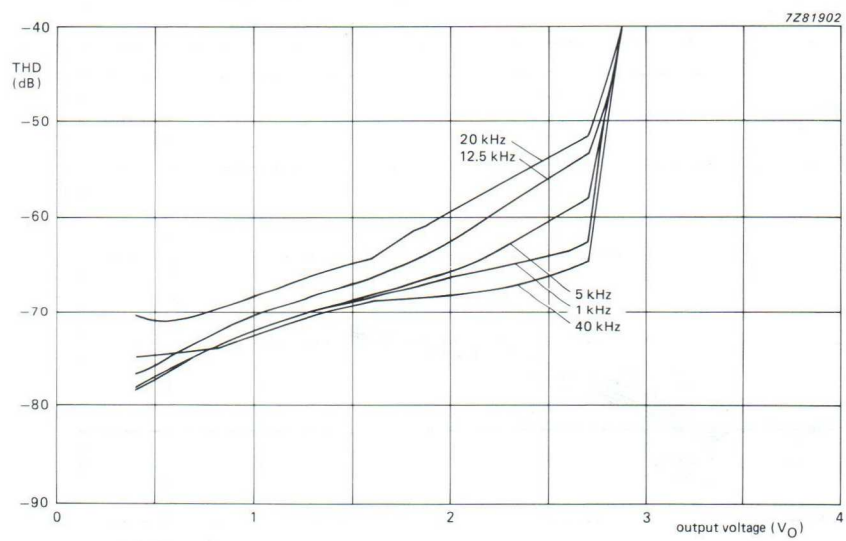
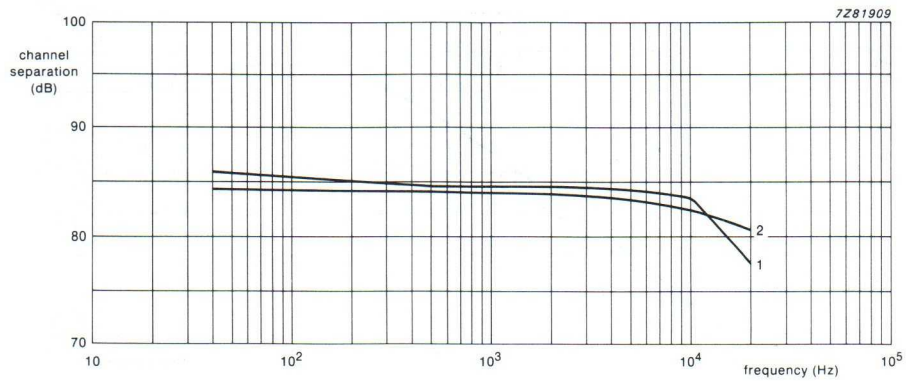


Fig.10 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.



1. gain = 0 dB; V_i = 1.0 V.
2. gain = 6 dB; V_i = 0.5 V.

Fig.11 Stereo channel separation as a function of frequency; R_S = 0 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

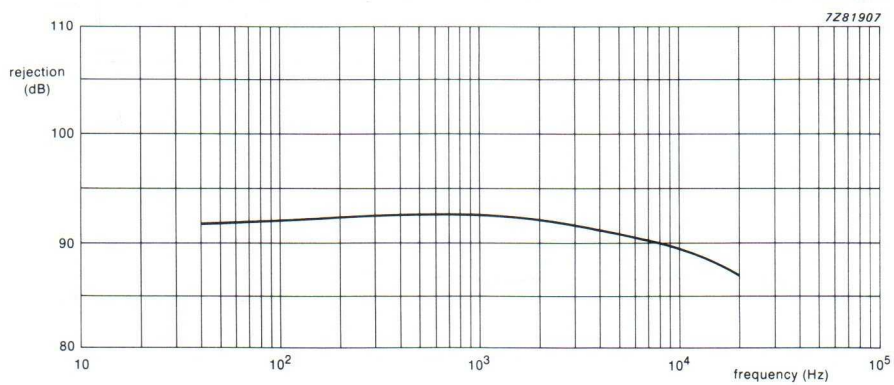


Fig.12 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

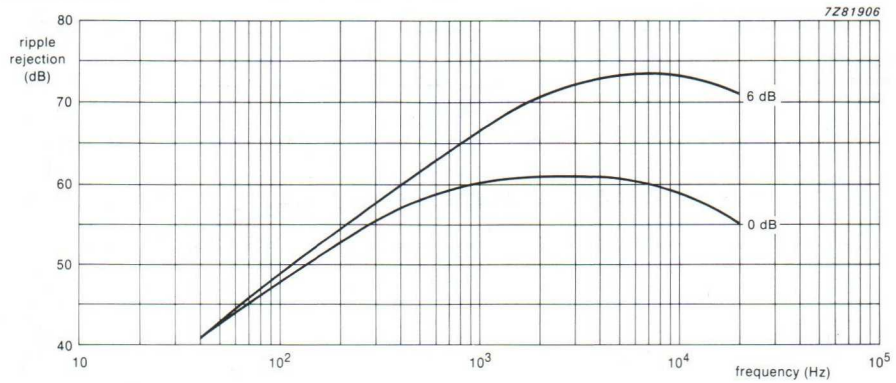


Fig.13 Ripple rejection as a function of frequency; V_{ripple} = 0.3 V (RMS); R_S = 0 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

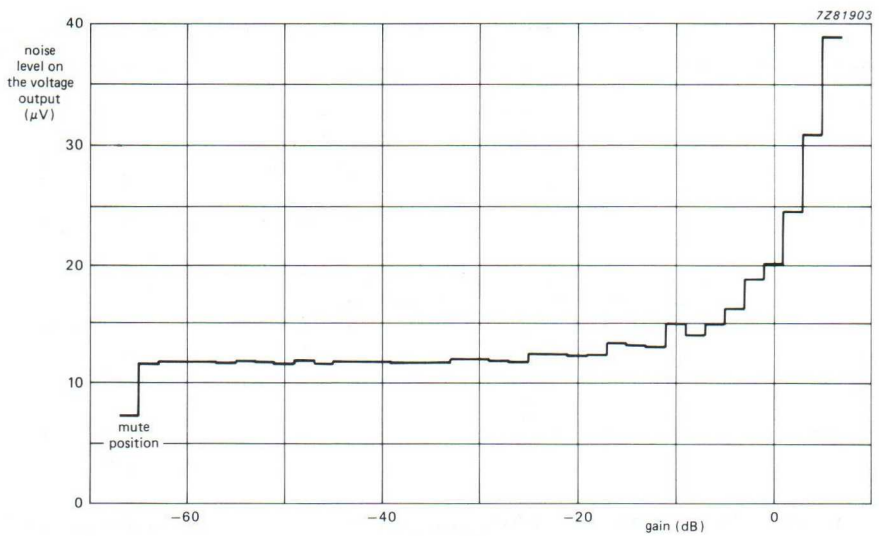


Fig.14 Noise output voltage as a function of gain; weighted CCIR 468 quasi peak gain, +6 dB to −64 dB; V_i = 0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/treble = 0 dB; V_{CC} = 12 V.

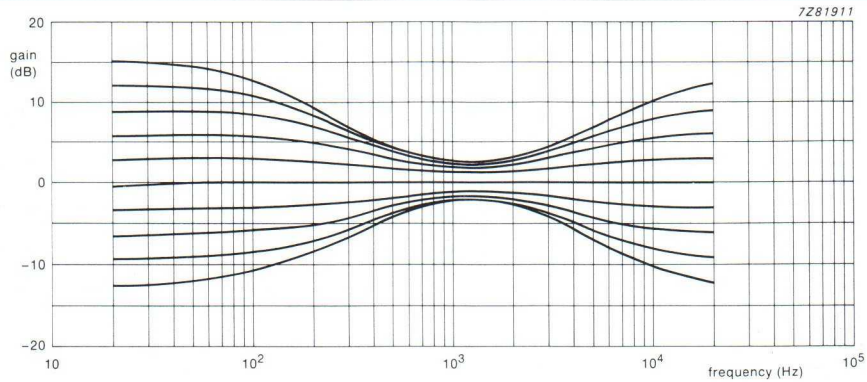


Fig.15 Frequency response of bass and treble control; bass and treble gain settings = −12 dB to +15 dB; gain = 0 dB; V_i = 0.1 V; R_S = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

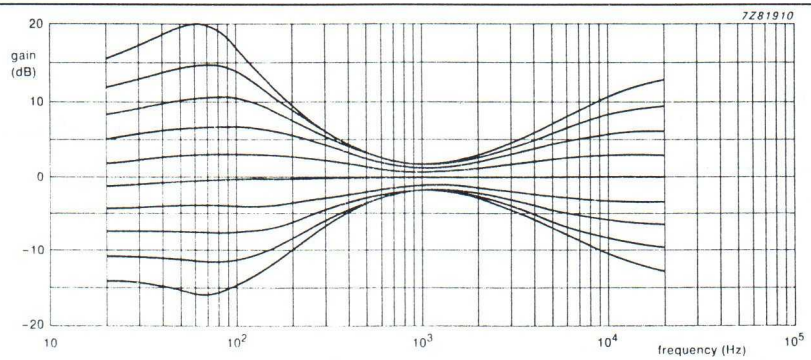


Fig.16 Tone control with T-filter.

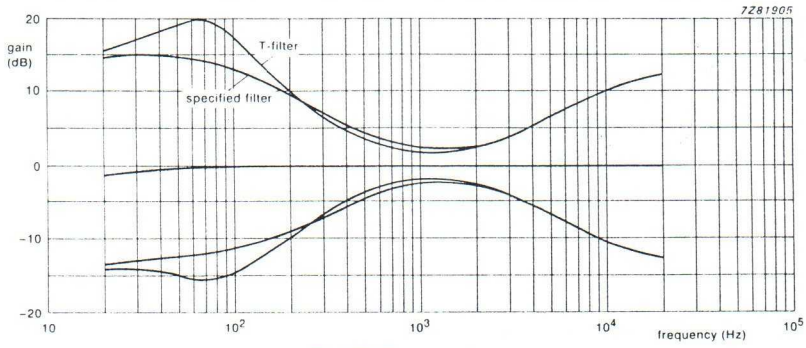


Fig.17 Tone control.

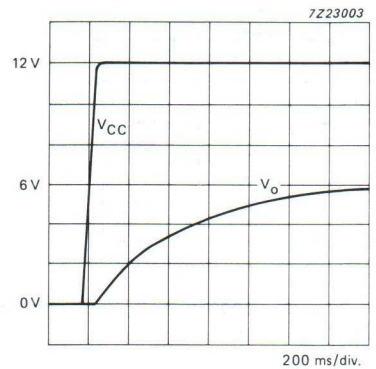


Fig.18 Turn-on behaviour; C = 2.2 µF; R_L = 10 kΩ.

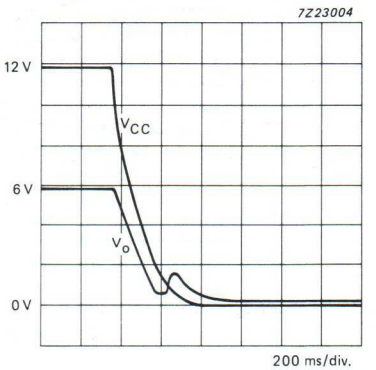


Fig.19 Turn-off behaviour; without modulation.

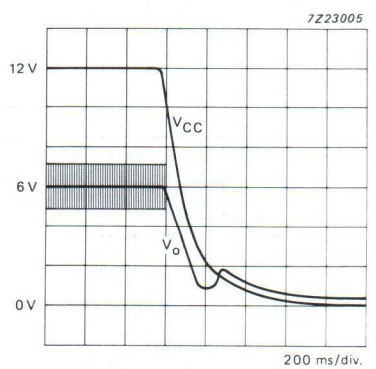


Fig.20 Turn-off behaviour; with modulation (shaded area).

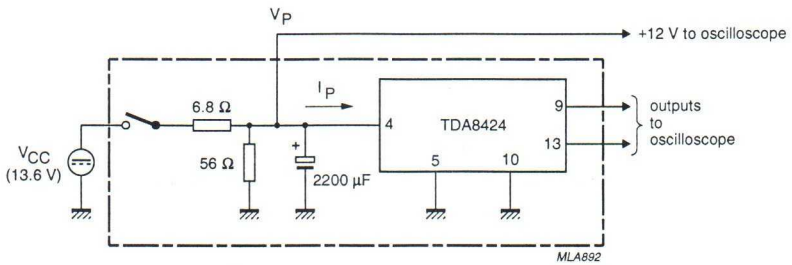


Fig.21 Turn-on/off power supply circuit diagram.

Where:

I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

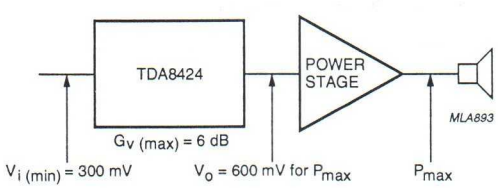


Fig.22 Level diagram.

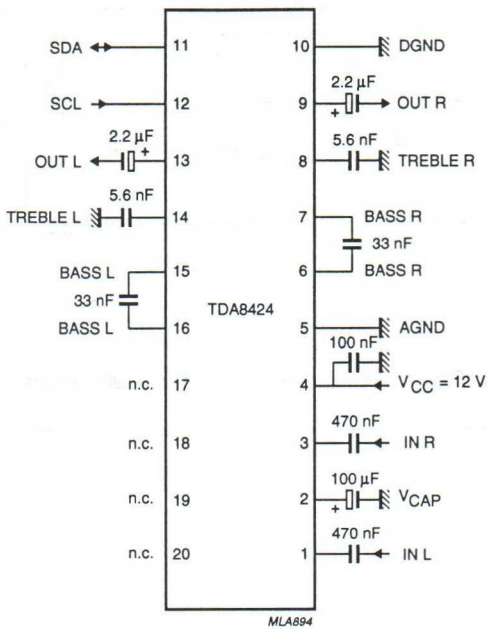


Fig.23 Test and application circuit diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

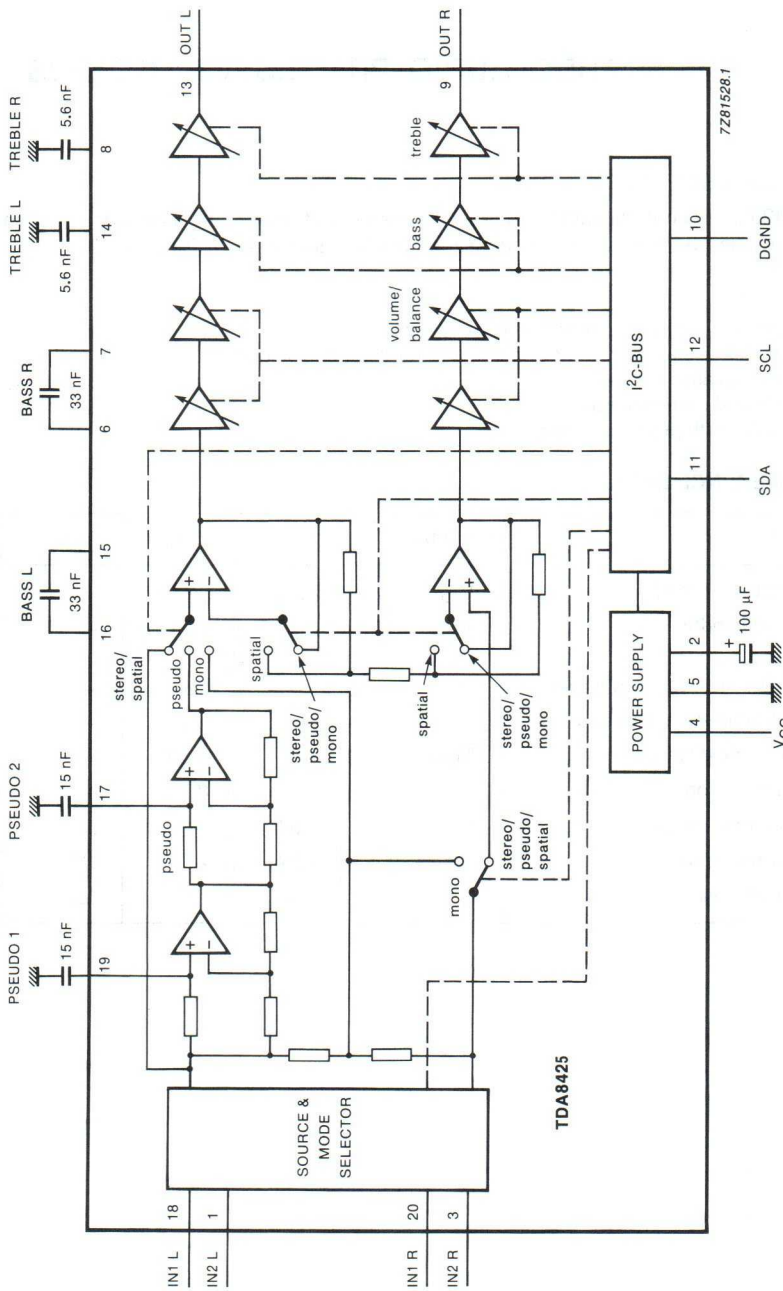


Fig. 1 Block diagram.

PINNING

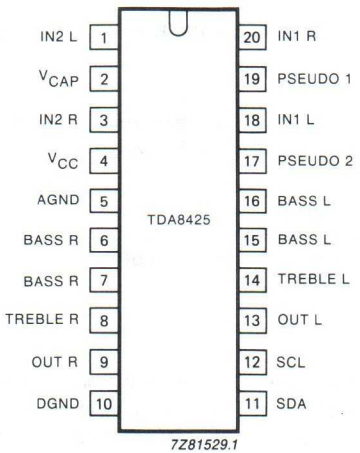


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

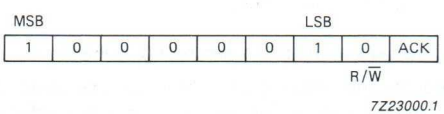


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

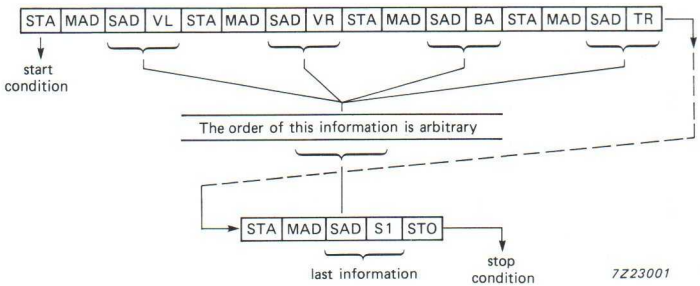


Fig. 4 Data transmission after a power-on reset.



Fig. 5 Data transmission after a power-on reset with auto increment.



Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70\ ^oC$	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	+ 150	^oC
Electrostatic handling, classification A*				

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)} \leqslant 2$ V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

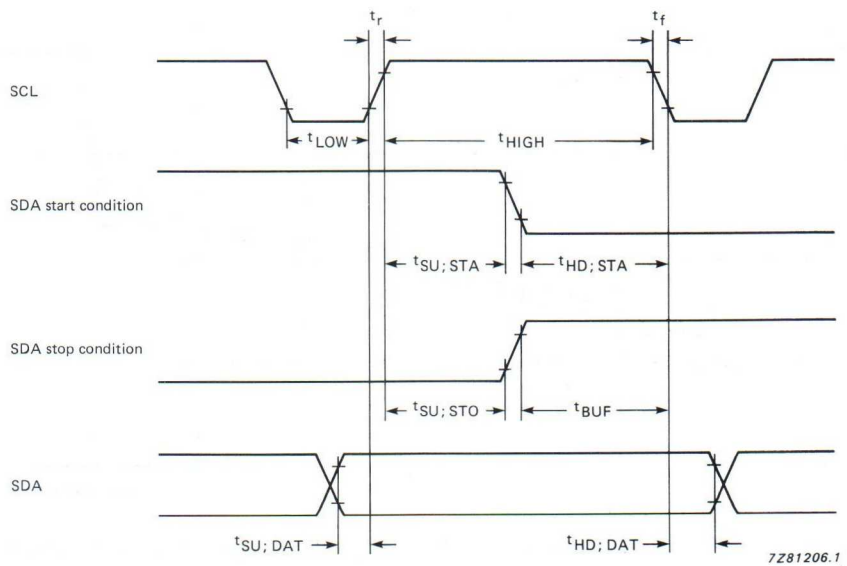
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

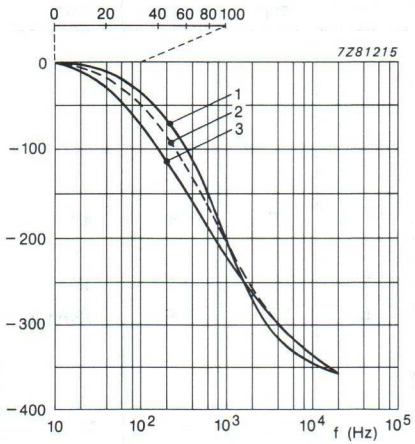
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

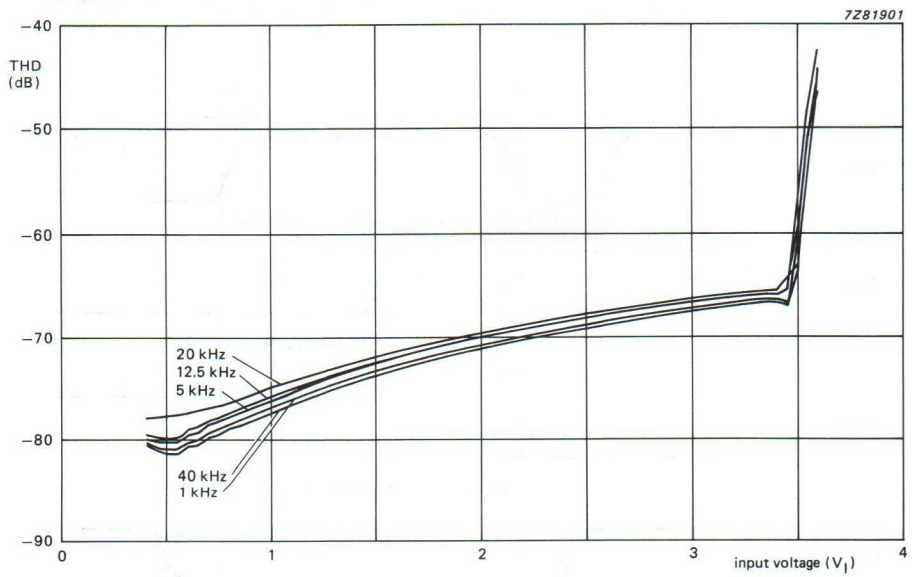


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

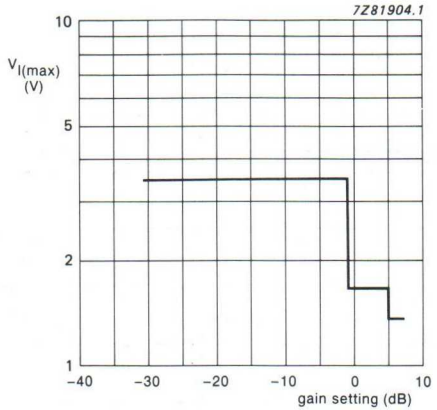


Fig. 10 Input signal handling capacility plotted against gain setting; THD = –60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

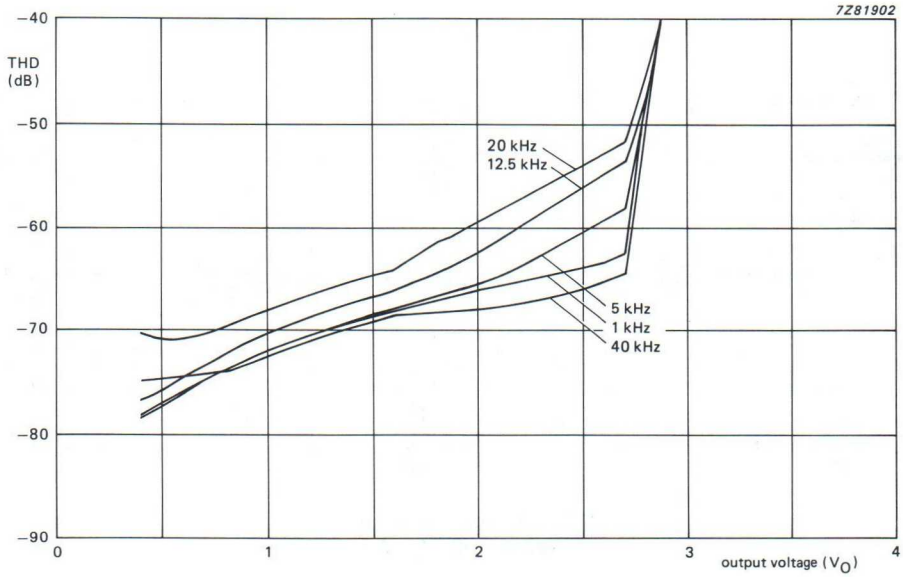


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

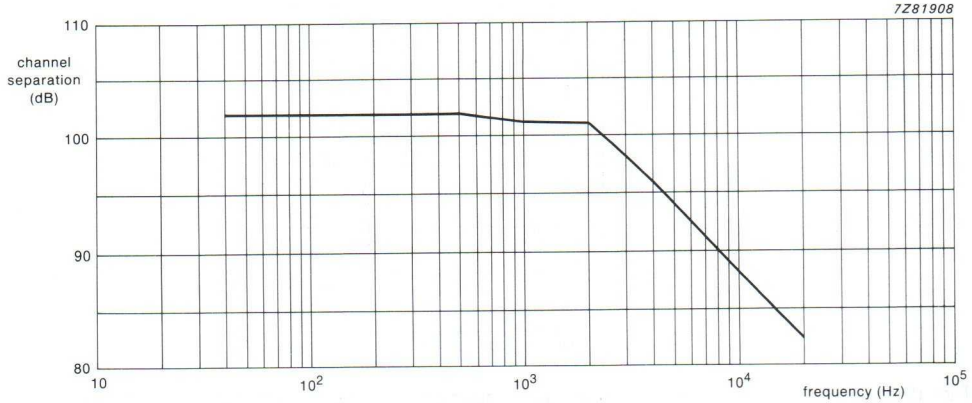
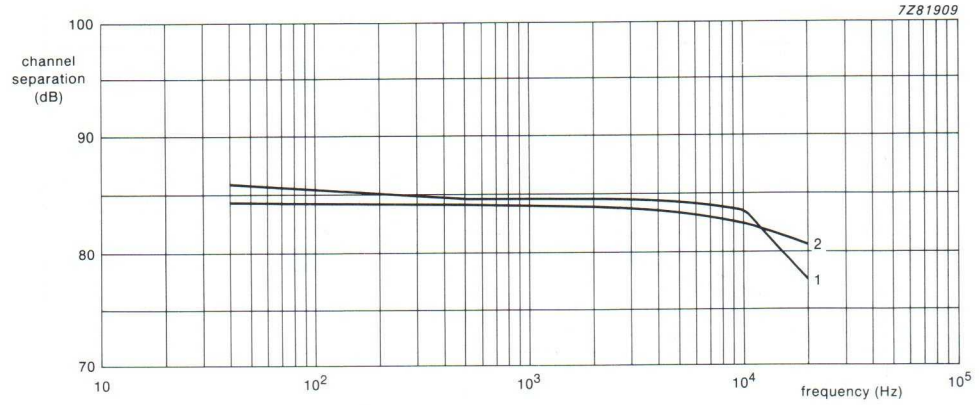


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

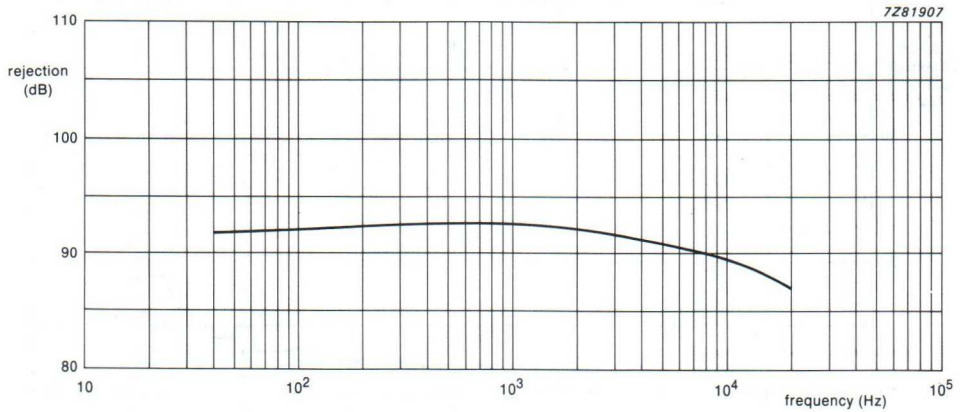


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

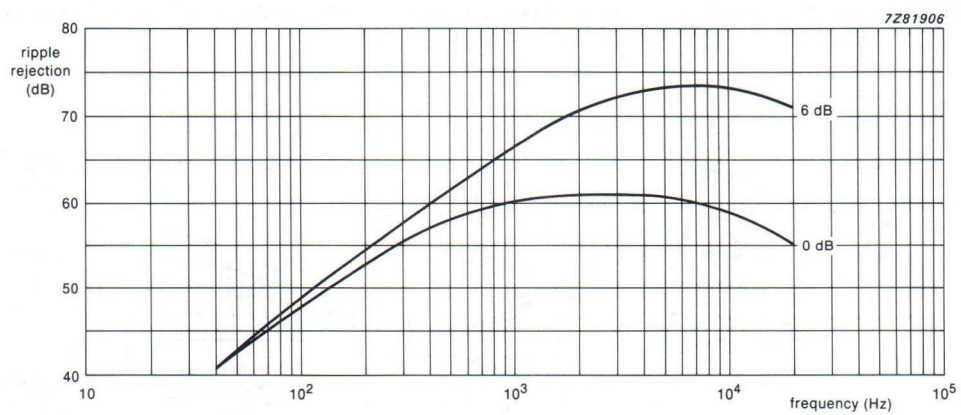


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

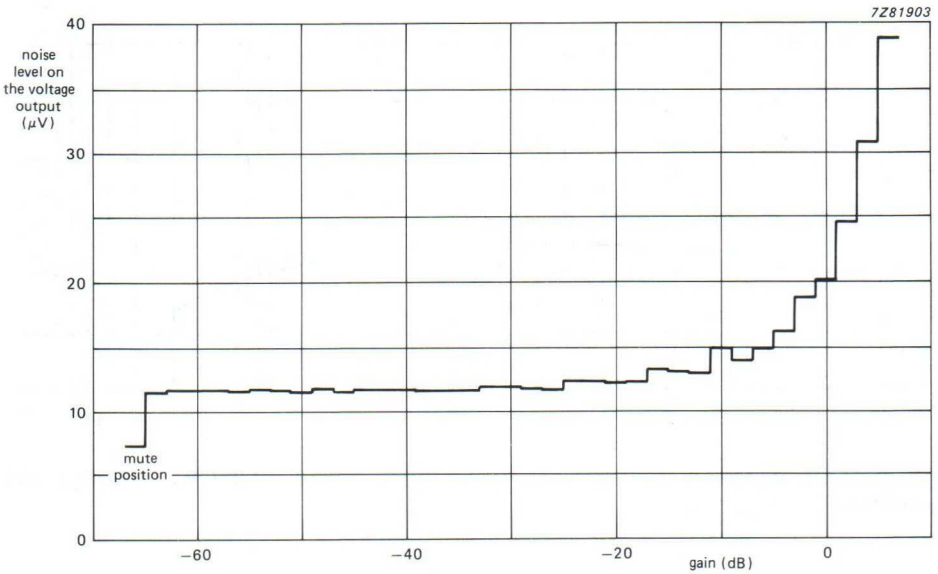


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

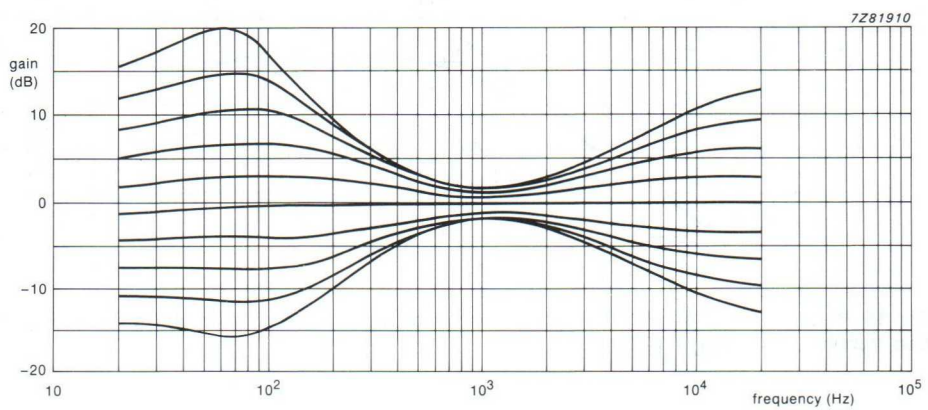


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{SG} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

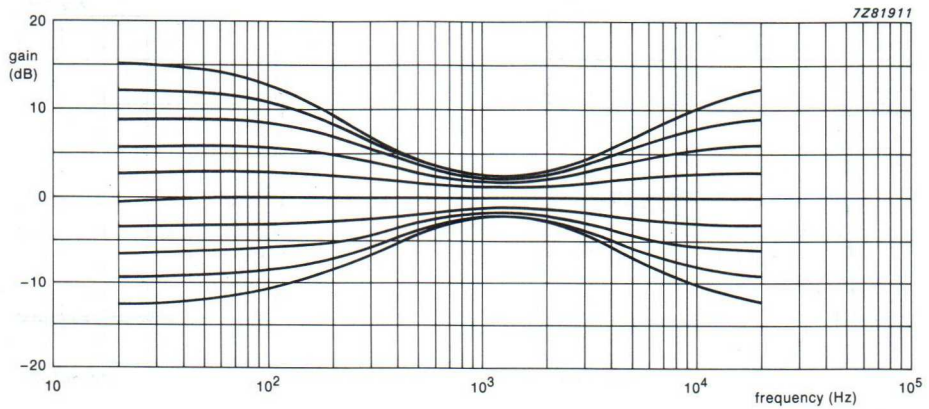


Fig. 18 Tone control with T-filter.

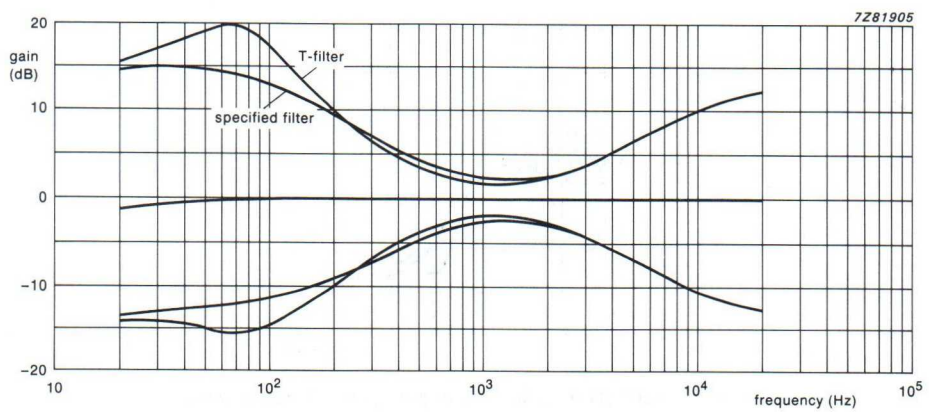


Fig. 19 Tone control.

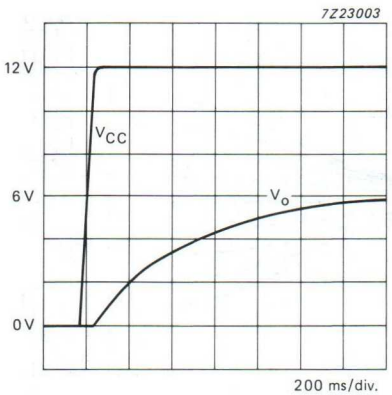


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

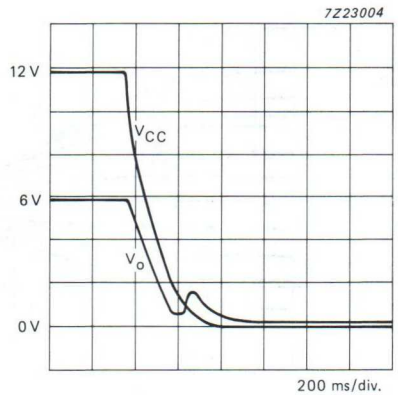


Fig. 21 Turn-off behaviour;
without modulation.

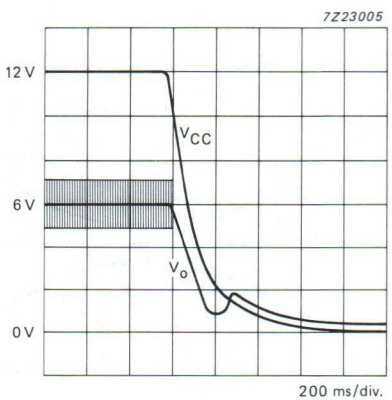
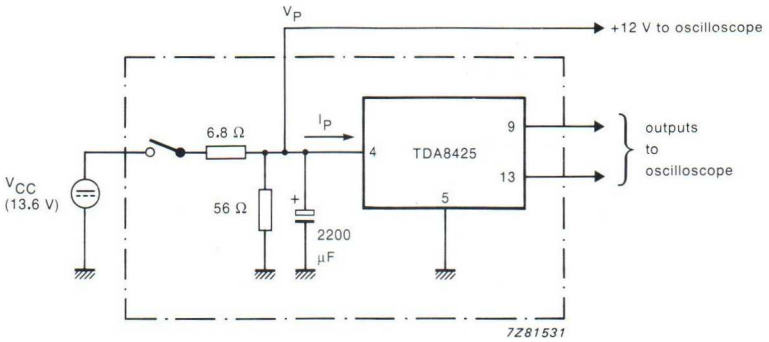


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

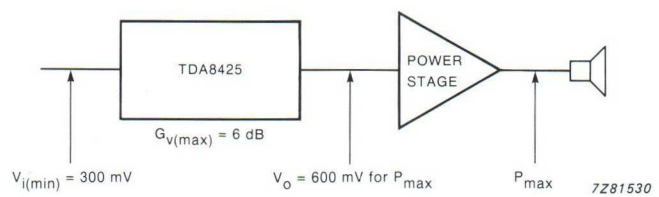


Fig. 24 Level diagram.

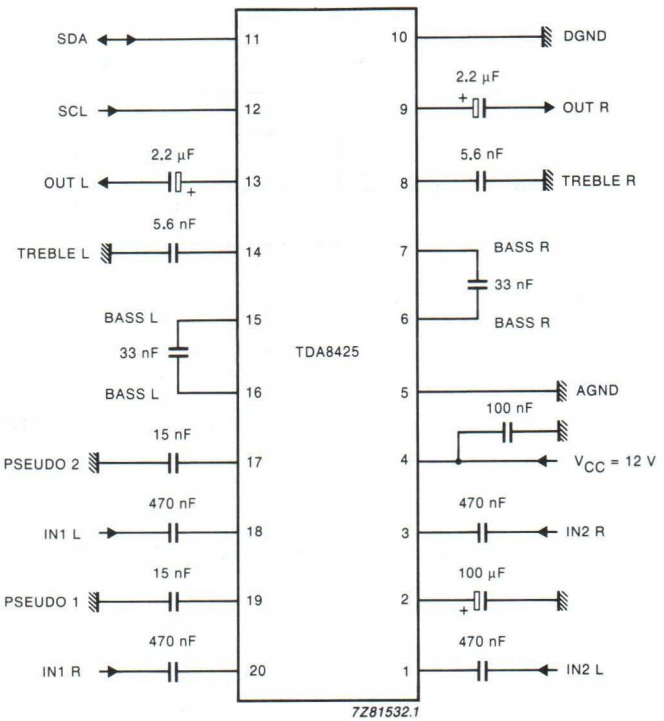


Fig. 25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8426 is a stereo sound circuit with a loudspeaker channel facility, digital controlled via the I²C-bus, for application in hi-fi audio and television sound. Reduced spatial antiphase crosstalk (30%) makes the device especially suitable for application in projection television receivers.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

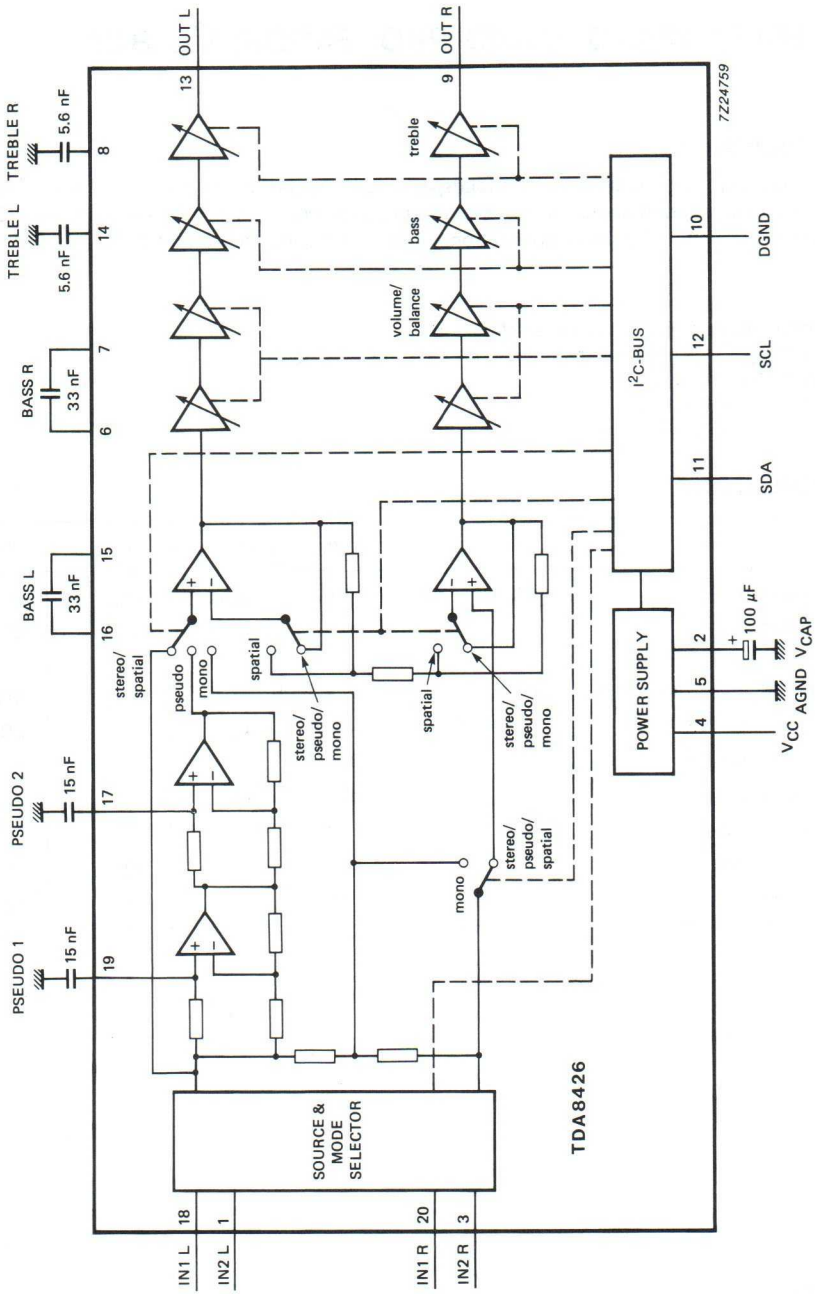


Fig.1 Block diagram.

PINNING

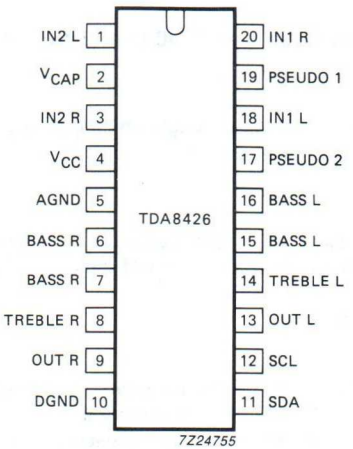


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8426 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8426 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8426 starts with the module address MAD.

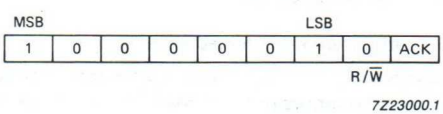


Fig. 3 TDA8426 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8426. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8426. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
–62	0	1	1	1	0	1
–64	0	1	1	1	0	0
$\leqslant$ –80	0	1	1	0	1	1
$\leqslant$ –80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

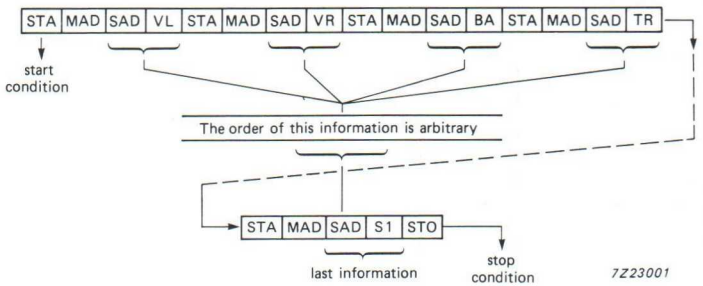


Fig. 4 Data transmission after a power-on reset.



Fig. 5 Data transmission after a power-on reset with auto increment.



Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C
Electrostatic handling, classification A*				

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{ref}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{ref}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{ref}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ≤ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ≤ 0.7%; $V_{i(max)} \leq 2$ V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ≤ −20 dB	(S+N)/N	–	68	–	dB

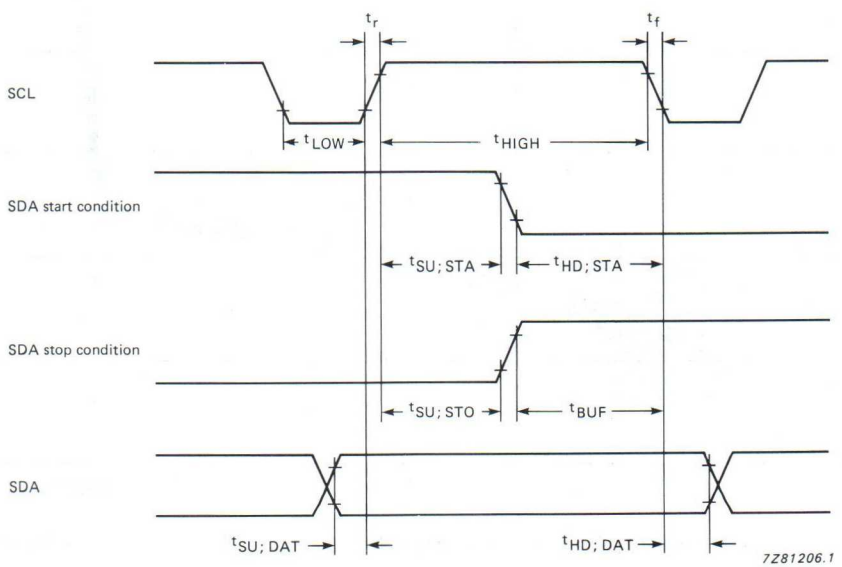
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	30	–	%
Pseudo: Phase shift (see Fig. 8)					

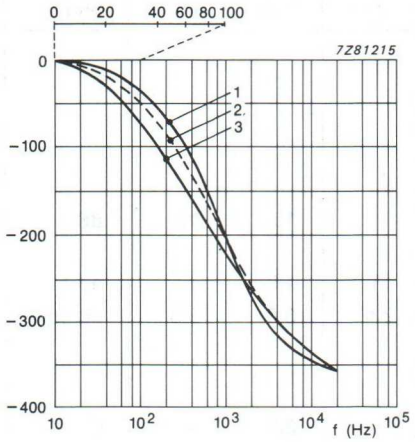
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

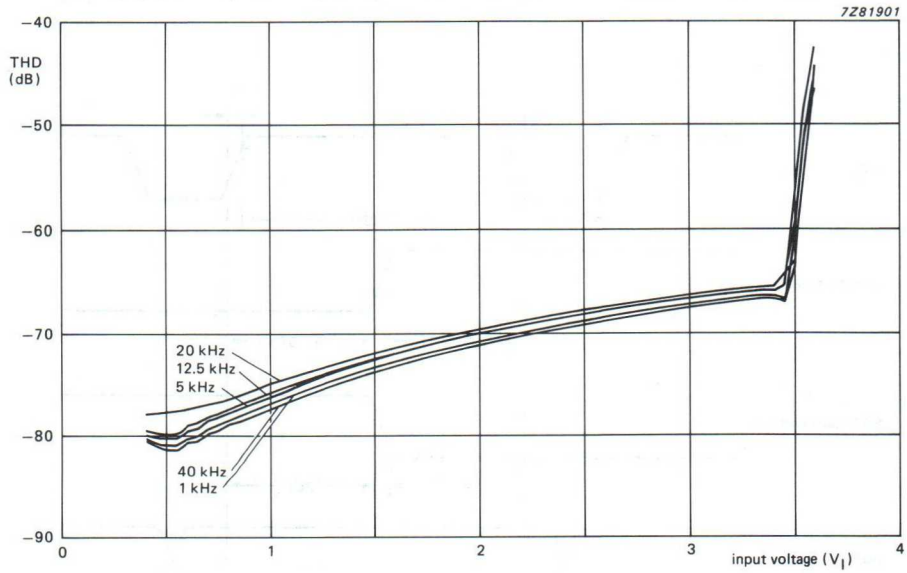


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

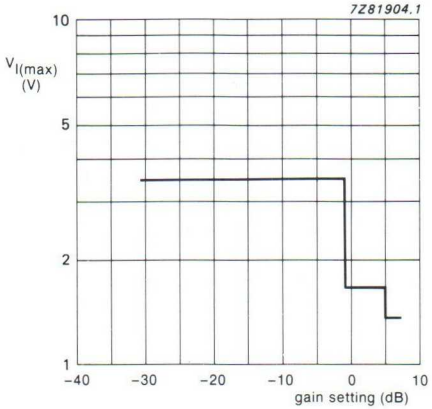


Fig. 10 Input signal handling capacility plotted against gain setting; THD = –60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

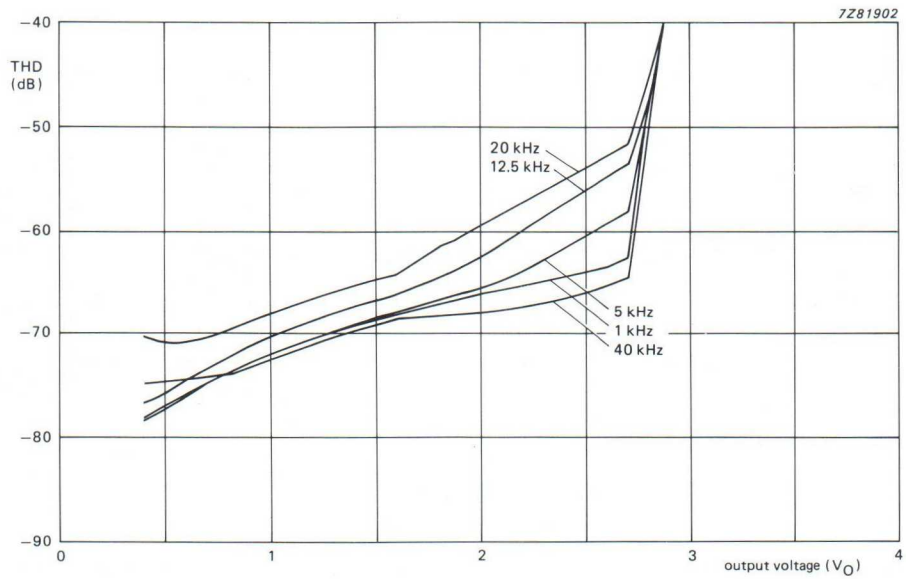


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

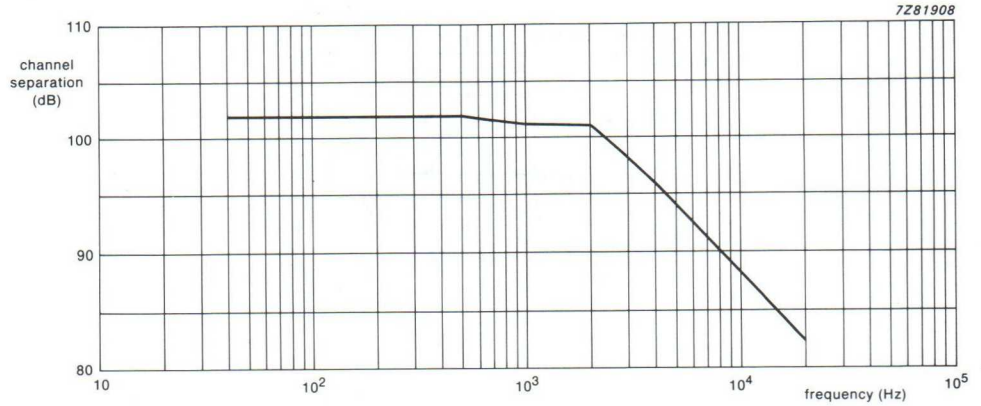
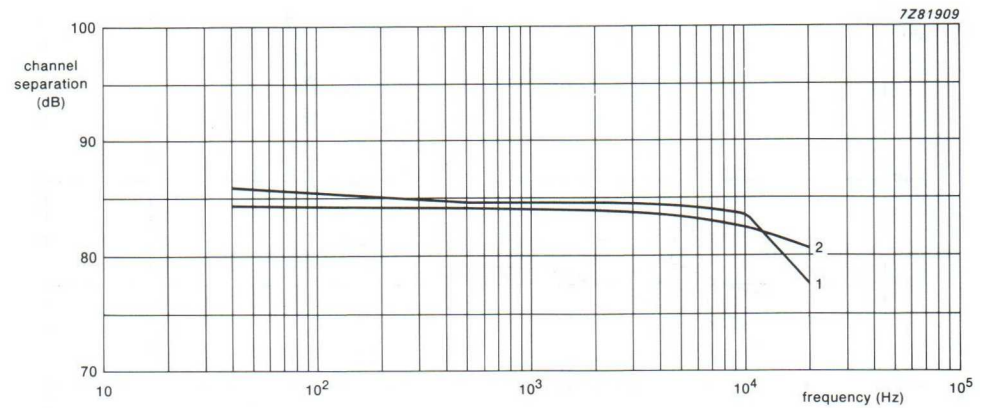


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

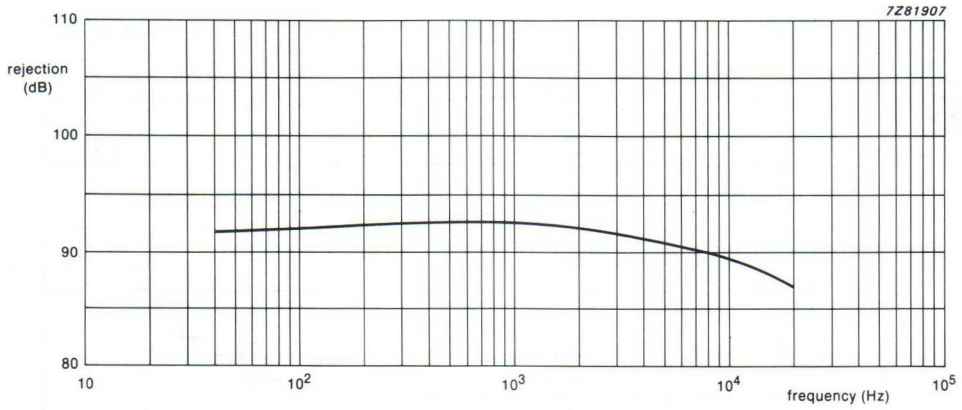


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

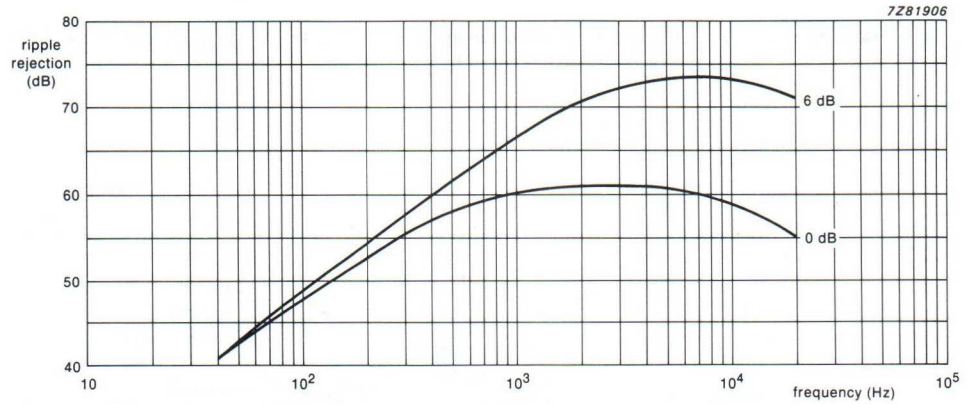


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

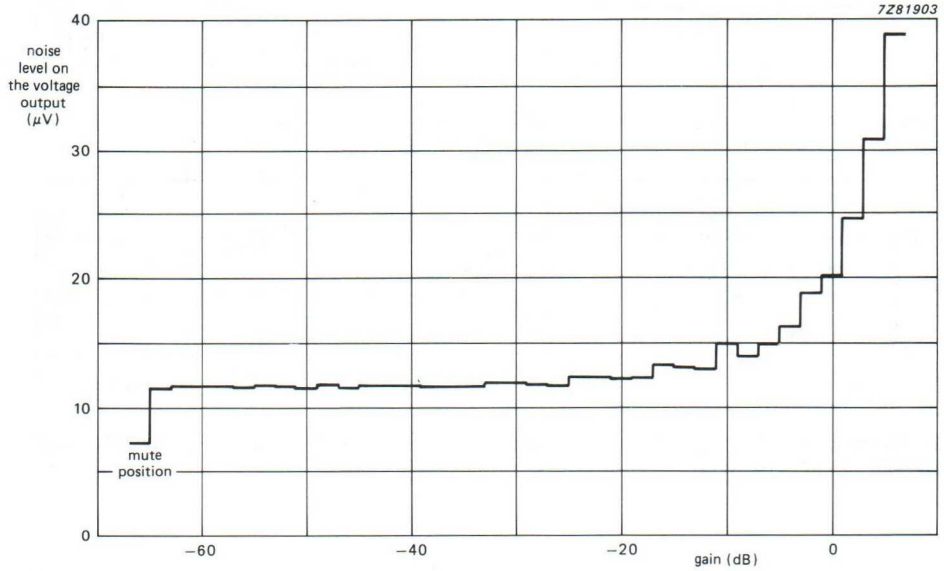


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

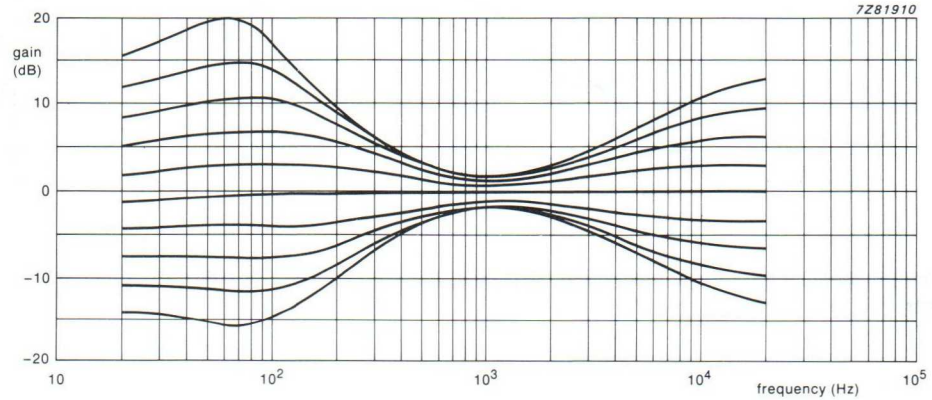


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

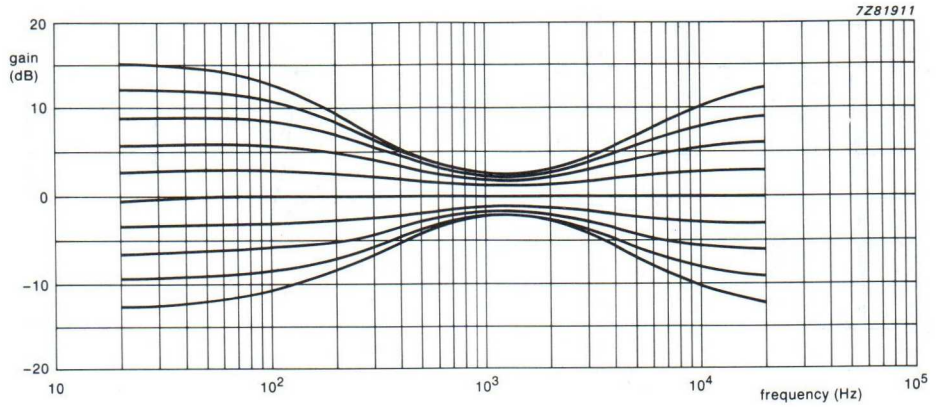


Fig. 18 Tone control with T-filter.

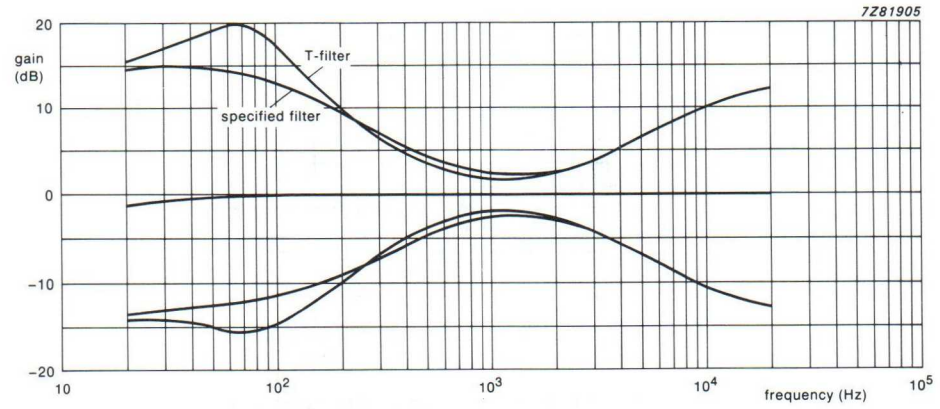


Fig. 19 Tone control.

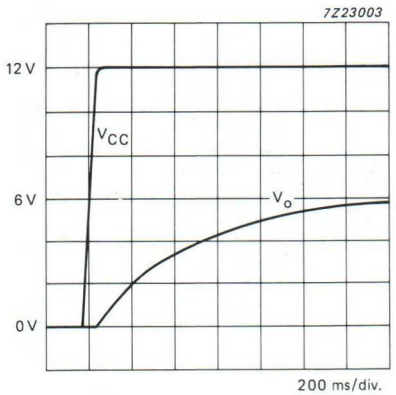


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

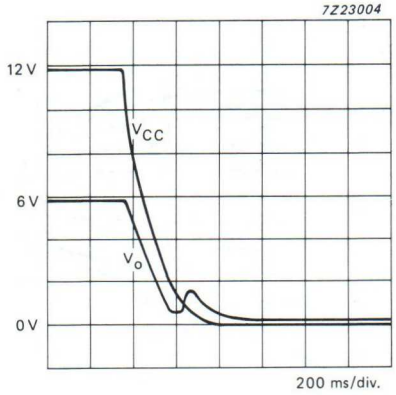


Fig. 21 Turn-off behaviour;
without modulation.

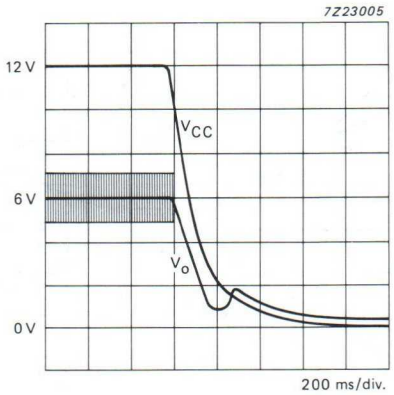
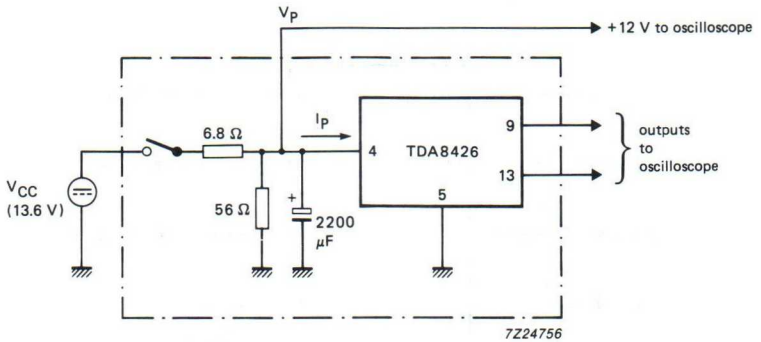


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig.23 Turn-on/off power supply circuit diagram.

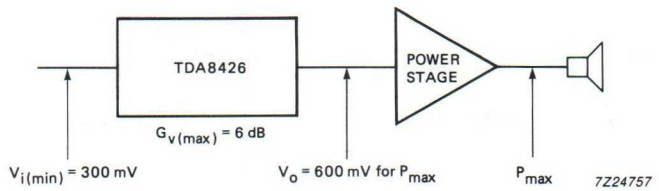


Fig.24 Level diagram.

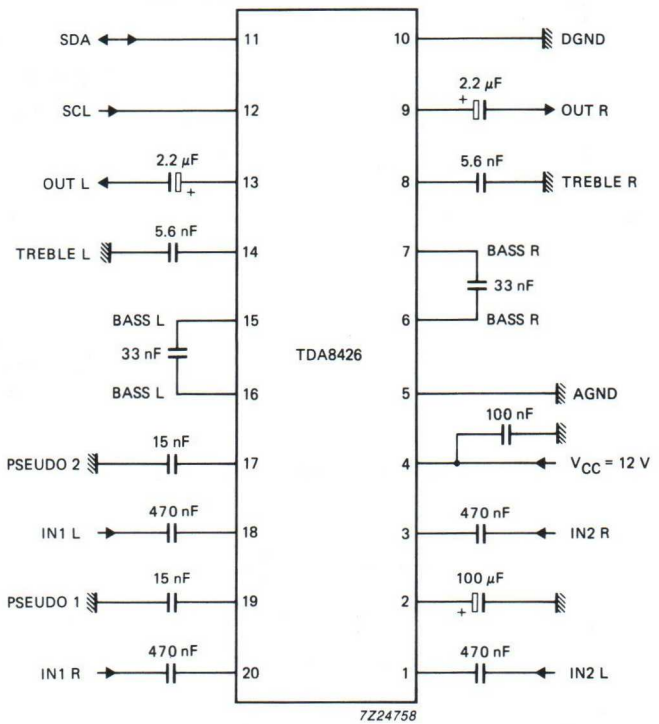


Fig.25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Deflection processor for computer controlled TV receivers

TDA8433

FEATURES

- I²C-bus interface
- Input for vertical sync
- Sawtooth generator with amplitude independent of frequency
- Vertical deflection output stage driver
- East-west raster correction drive output
- EHT modulation input
- Changes picture width and height without affecting geometry.

GENERAL DESCRIPTION

The TDA8433 is an I²C-bus controlled deflection processor which, together with a sync processor (e.g. TDA2579A, see Fig.6), contains the control and drive functions of the deflection part in a computer controlled TV receiver. The TDA8433 replaces all picture geometry settings which were previously set manually during manufacture.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (pin 12)	10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)	12	20	27	mA
V_2	vertical sync trigger level	–	3	–	V
V_{21}	vertical feedback (note 1) DC level AC level	 –1.7 1.65	 1.85 1.8	 2.05 1.95	 V V_P
V_{24}	EHT compensation operating range	1.7	–	6	V
V_{11-13}	inputs for control register data: not locked to video at 50 Hz status at 60 Hz status	 – 0.8 V_{CC} –	 0.7 – –	 1 – 0.7 V_{CC}	 V V V
V_{10-13}	HCENT comparator switching level	–	V_{17}	–	V
V_{14-13}	SDA I²C-bus switching level data input	–	3.5	–	V
V_{15}	SCL I²C-bus switching level clock input	–	3.5	–	V
V_1	device selection where: Ao = '1' Ao = '0'	 9.0 0	 – –	 V_{CC} 2.0	 V V

Note to the quick reference data

1. VR_{in} = 0; V-S-corr = 0; V_{shift} = 20 H; V_{ampl} = 20 H.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8433	24	DIL	plastic	SOT101

Deflection processor for computer controlled TV receivers

TDA8433

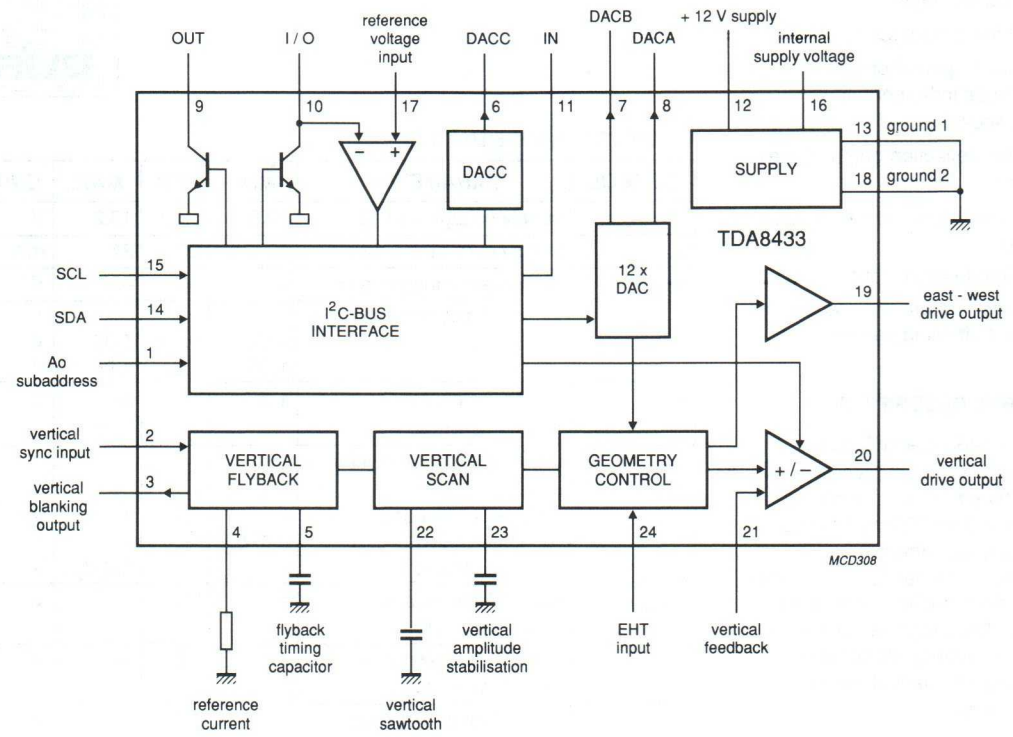


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	Ao subaddress
2	vertical sync input
3	vertical blanking output
4	I_{ref} resistor
5	vertical blanking/flyback timing capacitor
6	DACC (tau switching)
7	DACB (horizontal phase)
8	DACA (horizontal frequency)
9	OUT (video switch)
10	I/O (f_o adjustment)
11	IN (HLOCKN –50/60 Hz)
12	positive supply +12 V
13	ground 1
14	serial data input
15	serial clock input
16	internal supply voltage
17	voltage reference for I/O
18	ground 2 (waveform)
19	east-west drive output
20	vertical drive output
21	vertical feedback
22	vertical sawtooth capacitor
23	vertical amplitude capacitor
24	EHT input

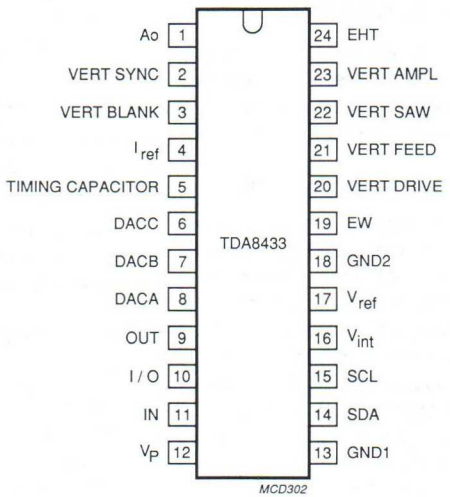


Fig.2 Pinning diagram.

PIN FUNCTIONS

Pin 1 - Ao subaddress

The Ao bit is the least significant bit of the bus-address. It enables two TDA8433s, with different addresses, to be connected to the same bus.

Pin 2 - Vertical sync input

Positive trigger pulses of > 3 V are sufficient to exceed the internal threshold of the ramp generator. Flyback and blanking will then start and, during the blanking period, the circuit will be inhibited for further input pulses (see Fig.3). It should be noted that the TDA8433 has no vertical oscillator therefore, the sync processor, which is used in this combination, has to provide trigger pulses as well when the video input is absent.

Pin 3 - Vertical blanking

The positive going blanking pulse is fed from a current source. The blanking period is fixed by the capacitor connected to pin 5 and the resistor connected to pin 4 (see Fig.3).

Pins 4 and 5 - Reference/flyback timing

The external resistor connected between pin 4 and ground provides a reference current for the triangle generator circuit. This circuit generates the triangle waveform at pin 5. The width of the blanking pulse is set by the external capacitor connected to pin 5.

Pin 6 - DACC (tau switching)

The output voltage, which depends on the VTRA and VTRC bits in the I²C-bus control register, is connected to the coincidence detector of the sync processor. In this way the time constants of the horizontal PLL (in the sync processor) can be set. If the TDA2579 is used (see Fig.6) the effect will be as listed in Table 1.

Table 1 Sync processor time constants

VTRA	VTRC	OUTPUT	TIME CONSTANT
'0'	'0'	12 V	automatic operation
'0'	'1'	5.3 V	medium
'1'	'0'	1.5 V	fast (video recorder)
'1'	'1'	0.2 V	not to be used

Pin 7 - DACB (horizontal phase)

The voltage at pin 7 is fed to the horizontal pulse modulator in the sync processor. This voltage, together with the signal produced by the phase 2 detector during horizontal flyback, sets the phase of the horizontal output with respect to the flyback pulse in the horizontal output stage. The voltage range is variable between 0.05 V and 10 V.

Pin 8 - DACA (horizontal frequency)

The frequency of the horizontal oscillator in the external sync processor is adjusted by the voltage level at pin 8. The voltage is variable in 63 steps from 0.05 V to 10 V (i.e. 0.158 V per step).

Pin 9 - OUT (video switch)

The output at pin 9 is controlled by the CVBS bit from the control register where

CVBS = logic 0; the output is HIGH (open collector)

CVBS = logic 1; the output is LOW (saturation voltage)

An external video selector can be controlled by means of this switching function.

Pins 10 and 17 - I/O and Voltage reference

Pin 10 is connected to the output of the phase 1 detector in the sync processor. Whether the pin is used as an input or an output is dependent on the PHI1 bit of the horizontal frequency (HFREQ) register. When PHI = logic 0 (output transistor open) pin 10 is used as an input. The DC information at this pin is compared with the reference voltage at pin 17 and is reflected in the HCENT of the status register.

HCENT = logic 0; input > V_{ref} at V_{17}
HCENT = logic 1; input < V_{ref} at V_{17}

In this way the free running frequency can be adjusted by computer while the oscillator is locked. Alternatively, when PHI1 = logic 1, pin 10 is switched to ground. The free running frequency of the oscillator can the be adjusted while watching the screen provided that pin 10 is connected to the video input of the sync processor.

Pin 11 -IN (HLOCKN and 50/60 Hz)

This pin is connected to the combined MUTE and 50/60 Hz pin of the sync processor. The various DC levels define the state of the HLOCKN and 50/60 Hz bits in the status register (see Table 2.)

Table 2 Status register bits

STATE OF SYNC PROCESSOR (TDA2579)	TYPICAL VOLTAGE AT PIN 11	STATE OF	
		HLOCKN	50/60 Hz
Not locked to computer video	< 0.7 V(min.)	'1'	'0'
60 Hz transmitter found	0.7 to 0.75 V_{CC}	'0'	'0'
50 Hz transmitter found	> 0.75 V_{CC} to V_{CC}	'0'	'1'

Pin 12 - Positive supply (12 V)

The nominal supply voltage at pin 12 is 12 V which should remain within the defined limits. The nominal current consumption is 20 mA.

Pins 13 and 18 - Ground (1 and 2)

Ground 1 (pin 13) is for the bus transceiver section
Ground 2 (pin 18) is for the sawtooth and picture geometry control section.

Pins 14 and 15 - SDA and SCL (serial data and serial clock)

Input serial data is applied to pin 14. The serial clock input from the I²C-bus is applied to pin 15.

Pin 16 - Internal supply voltage (+5 V)

In some applications it may be necessary to connect a capacitor to this pin to avoid interference.

Pin 19 - East-west drive output

The output drive for the East-west correction circuit has a nominal range from 1.6 to 11.7 V and contains 5 programmable parameters (see Fig.5). The parameters are:

- Picture width
- East-west raster correction
- East-west trapezium correction
- East-west corner correction
- Compensation for EHT variations

Pins 20 and 21 - Vertical drive output and vertical feedback input

The vertical comparator and drive output stage is designed so that the feedback signal applied to pin 21 can be inverted in the comparator by the V-out control bit. This enables the use of two different vertical output stages.
One output stage is without an internal comparator (e.g. TDA3654). The feedback signal at pin 21 has a negative slope during scan. During power-up the IC is adapted (preset) for this type of output stage.
The other output stage contains a comparator. The drive for this output stage is obtained by interconnecting pins 20 and 21 and switching the V-out polarity. The V-out bit will then be set to logic 1.
In both cases the drive signal available at pin 20 contains 5 parameters which can be set via the I²C-bus control;

- Picture hight
- Vertical linearity
- Vertical S-correction
- Vertical shift
- Extent of compensation for EHT variations (see Fig.4.)

Pins 22 and 23 - Vertical sawtooth/vertical amplitude capacitor

The 100 nF capacitor connected to pin 22 is charged and discharged by two current sources in the vertical ramp generator. In order to obtain an equal amplitude, at different frequencies, an amplitude comparator has been incorporated. The circuit, together with the 330 nF capacitor connected to pin 23, keeps the sawtooth amplitude at reference voltage level (7.1 V). The external load of the amplitude stabilization loop of pin 23 should be as low as possible. The recommended value is ≥ 500 MΩ.

Pin 24 - EHT input (Modulation)

A voltage between 1.7 and 6 V (depending on the EHT variations) applied to pin 24 will modulate the amplitude of the vertical drive sawtooth and the East-west drive output. In this way the effect of beam current variations can be virtually eliminated.

I²C-BUS CONTROL

The addresses for the I²C-bus are 100011Ao0 (write) and 100011Ao1 (read). The inclusion of the Ao bit makes it possible to control two different deflection processors. After receiving the address byte the I²C-bus transmits its status byte in which the status of the control bits is contained.

PONRES - Power-on-reset

After switch-on, or a power dip below 6.7 V, the PONRES bit is set to logic 1. After a status read operation PONRES is reset to logic 0.

HLOCKN - Horizontal lock

This bit indicates whether the horizontal oscillator in the sync processor is locked to the video signal. When the oscillator is locked HLOCKN is set to logic 0 ($V_{11} > 0.7$ V). When the oscillator is not locked HLOCKN is set to logic 1 ($V_{11} < 0.7$ V).

HCENT - Horizontal centre

This bit is set to logic 0 when the horizontal oscillator frequency is too high ($V_{10} > V_{ref}$). The bit is set to logic 1 when the frequency is too low $V_{10} < V_{ref}$).

IN - 50/60 Hz

The voltage at pin 11 also contains the 50/60 Hz information where:

logic 0 = $\leq V_{11}$ 0.75 V_{CC} (60 Hz or no transmitter)
logic 1 = $\geq V_{11}$ 0.75 V_{CC} (50 Hz)

The sequence of data in the status byte is: PONRES, HLOCKN, 50/60 Hz, 0 0 0 0.

A write operation starts with address byte 100011Ao0. The device is then ready to receive the subaddress byte e.g. trapezium (HEXOA) 00001010 followed by the data byte e.g. HEX20. The DAC will then set the trapezium correction signal into the selected position (see Fig.5). If more data bytes follow within one transmission then, by means of an auto-increment, the next highest subaddress will be selected. Wrap-around occurs after HEXOF.

Table 3 Registers

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
H-frequency	00	PHI-X-6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
H-phase	01	6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
Picture height $V_{21/20}$	02	6	01	00 3F	– +15	–19 +19	–22 –	% %
V-linearity	03	6	01	00 3F	0 13	– 17	1 21	% %
V-S correction	04	6	01	00 3F	0 15	– 19	1 –	% %
V-shift	05	6	01	00 3F	+17 –17	+19 –19	+22 +22	% %
V-compensation V_{24} = 1.7 V	06	5	01	00 1F	tbf –8	0 –10	– –12	– %
Picture width	07	6	01	00 3F	– 6.0	1.6 6.6	2.4 7.2	V V
E-W parabola (Reg: 07 = 0)	08	6	01	00 3F	– 7.0	0.07 7.5	0.1 8.5	V V
E-W corner (Reg: 08 = 3F)	09	6	01	00 3F	– 1.7	0 2.2	tbf 2.8	V V
Trapezium Reg: 07 = 00; 08 = 20H	0A	6	01	00 3F	0.75 1.0	1.25 1.9	– –	V V
H-compensation Reg. 07 = 00; 08 = 0; 09 = 00 V_{24} = 1.7 V	0B	5	01	00 1F	0 –	tbf 10	– –	% %

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
Not used	0C/0E	–	–		–	–	–	–
Control	0F	X-VOUT	–	40	11.5	11.9	V_{CC}	V
		VTRA–VTRC	–	50	5.0	5.3	5.6	V
		CVBS–X–X–X	–	60	1.2	1.5	1.8	V
				70	0	0.2	0.5	V
				40	5.5	7.5	9.5	kΩ
				50	2.4	3.3	4.2	kΩ
				60	0.7	1.0	1.35	kΩ
				70	–	50	–	Ω
				00	–	–	(VBS)	V
				08	–	–	0.4 (1 mA)	V
PHI1 bit	00	1	–	80	–	–	0.4 (–2 mA)	V
				00	–	–	V_{CC}	V
Not used	10–EF							
Test functions	F0–FF							

Note to Table 3

tbf = value to be fixed.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	10.8	13.2	V
I_{CC}	supply current	12	27	mA
P_{tot}	total power dissipation	–	360	mW
T_{amb}	operating ambient temperature range	–25	+75	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	–	35	K/W

CHARACTERISTICS

V_{CC} = 12 V; V_{24} = 1/2 x V_{CC}; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage (pin 12)		10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)		12	20	27	mA
Ao subaddresses (pin 1)						
V_1	switching level allowed voltage for Ao = '0' for Ao = '1'	note 1	– – 9	2.3 – –	– 2 V_{CC}	V V V
I_1	input current		–	–	+10	µA
V_1	not allowed voltage range		2.0	–	8.9	V
Vertical sync input (pin 2)						
V_2	switching level		2.5	3.0	3.5	V
I_2	current during non-active state	V_2 = 0 V	–	3	10	µA
Vertical blanking output (pin 3)						
$V_{3(p-p)}$	pulse amplitude (peak-to-peak value)	1 mA load	–	–	V_{CC}–2	V
V_3	output voltage	1 mA load	10.0	10.5	–	V
I_O	output source current		1	–	–	mA
t_W	pulse width	R_4 = 75 kΩ C_5 = 8.2 nF	–	1.13	–	ms
Reference (pin 4)						
V_4	reference voltage		6.8	7.15	7.5	V
I_4	current range		90	–	150	µA
Vertical blanking timing (pin 5)						
$V_{5(p-p)}$	amplitude of triangular pulse (peak-to-peak value)	R_4 = 75 kΩ C_5 = 8.2 nF	7.5	7.9	8.3	V
t_W	width of triangular pulse		–	1.3	–	ms
I_5	sink current	V_5 = 3.5 V; I_4 = 100 µA	85	105	125	µA
I_5	source current	V_5 = 3.5 V; I_4 = 100 µA	80	100	120	µA
DACC output (pin 6)						
V_6	voltages at VTR(A) and VTR(C) where: (A) = '0'; (C) = '0' (A) = '0'; (C) = '1' (A) = '1" (C) = '0' (A) = '1'; (C) = '1'		 11.5 5.0 1.2 0	 11.9 5.3 1.5 0.2	 – 5.6 1.8 0.5	 V V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACC output (pin 6)						
Z_6	output impedance at VTR(A) and VTR(C) where: (A) = '0'; (C) = '0' (A) = '0'; (C) = '1' (A) = '1'; (C) = '0' (A) = '1'; (C) = '1'		 5.5 2.4 0.7 –	 7.5 3.3 1.0 50	 9.5 4.2 1.35 –	 kΩ kΩ kΩ Ω
DACB horizontal phase (pin 7)						
V_7	output voltage at HEX00 at HEX3F		 – 9.4	 0.05 10.0	 0.2 11.0	 V V
ΔV_7	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_7	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
DACA horizontal frequency (pin 8)						
V_8	output voltage at HEX00 at HEX3F		 – 9.5	 0.05 10.0	 0.2 11.0	 V V
ΔV_8	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_8	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
OUT video switch (pin 9)						
FOR EXTERNAL CVBS SWITCH WHEN CVBS BIT = 1						
V_9	saturation voltage	I_{sink} = 1 mA	–	–	0.4	V
I_L	leakage current		–	–	2	µA
I/O combined input/output (pin 10)						
V_{10}	when used as an output (open collector) where PHI1 = '0' where PHI1 = '1'		 – –	 – –	 V_{CC} 0.4	 V V
I_{sink}	sink current		–	–	2	mA
V_{10}	when used as an input (switching point HCENT is '0' to '1')	PHI1 = '0'	V_{17} – 35 mV	V_{17}	V_{17} + 35 mV	V
I_{10}	input current		–	–	2	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IN HLOCKN and 50/60 Hz (pin 11)						
V_{11}	HLOCKN switching level		–	0.7	–	V
V_{11}	switching level where: HLOCKN = '0' HLOCKN = '1'		 1.0 –	 – –	 – 0.4	 V V
V_{11}	switching level where: 50/60 Hz = '0' 50/60 Hz = '1'	 state 50 Hz	 – 0.8 V_{CC}	 – –	 0.7 V_{CC} –	 V V
I_{11}	source current		10	25	35	µA
SDA serial data input (pin 14)						
V_{14}	switching level where: SDA = '0' SDA = '1'		 – 3.0	 – –	 1.5 –	 V V
I_{14}	sink current		–	0.5	10	µA
SCL serial clock input (pin 15)						
V_{15}	switching level where: SDA = '0' SDA = '1'		 – 3.0	 – –	 1.5 –	 V V
I_{15}	sink current		–	0.5	10	µA
Internal supply voltage						
V_{16}	maximum allowed load	1 mA load	4.5	5.0	5.5	V
V_{17}	voltage reference for pin 10 (pin 17)		1.0	–	V_{CC} – 1.5	V
I_{17}	input load current		–	–	2.0	µA
E-W drive output (pin 19; see application information)						
V_{19}	output voltage	1 mA load	0.5	–	11.5	V
I_{19}	output current		±1.0	–	±2.0	mA
RR	ripple rejection		24	30	–	dB
R_I	internal resistance		–	1	2	kΩ
t_R	response time		–	2	–	µs
Vertical drive output (pin 20; see application information)						
V_{20}	output voltage	1 mA load	0.5	–	10.5	V
I_{20}	output current		±1.5	±2.0	–	mA
RR	ripple rejection	note 2	35	40	–	dB
	DAC stepsize	note 3	10	–	190	%
Vertical feedback (pin 21; see application information: Register 02 = 20H, 03 = 0, 04 = 0, 05 = 20H, 06 = 0)						
V_{21}	DC input voltage		1.7	1.85	2.05	V
$V_{21(p-p)}$	AC output voltage (peak-to-peak value)	note 2	1.65	1.8	1.95	V
I_{21}	input current		–	–	–3	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sawtooth voltage (pin 22; see application information)						
V_{22}	top level of sawtooth		6.7	7.1	7.4	V
V_{22}	minimum level of sawtooth	I_{sink} = 0.5 mA	–	–	50	mV
I_{22}	discharge sink current	V_{22} = 3.5 V	6.5	9.5	15	mA
I_{22}	charge source current	V_{23} = 5 V; V_{22} = 3.5 V	1	20	35	µA
I_{22}	control range	5 V to 1 V	80	135	190	µA
$\|Z_{22}\|$	AC impedance		–	3	–	MΩ
C_{EXT}	external capacitance		–	100	–	nF
Vertical sawtooth stabilizer (pin 23; see application information)						
I_{23}	discharge sink current	V_{22} = 2 V	200	250	300	µA
I_{23}	charge source current	V_{22} = 9.75 V	185	235	285	µA
C_{EXT}	external capacitance		–	390	–	nF
I_L	leakage current	note 5	–	–	0.015	µA
EHT modulation input (pin 24; see application information)						
V_{24}	voltage operating range		1/7 V_{CC}	–	1/2 V_{CC}	V
I_{24}	input current		–	0.5	2.0	µA

Notes to the characteristics

1. Outside the test mode.
2. Test condition (hex values): register 02 = 3F; 03 = 00; 04 = 00; 05 = 20; 06 = 00; V_{22} = 1/2 V_4; f = 50 Hz to 30 kHz.
3. $\frac{Value\ StepN - Value\ StepN{-}1}{average\ step\ size} \times 100\%$ (63>*N*>1).
4. Applies to both modes.
5. External load of this pin (leakage current capacitor etc.) should be ≥ 500 MΩ.



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

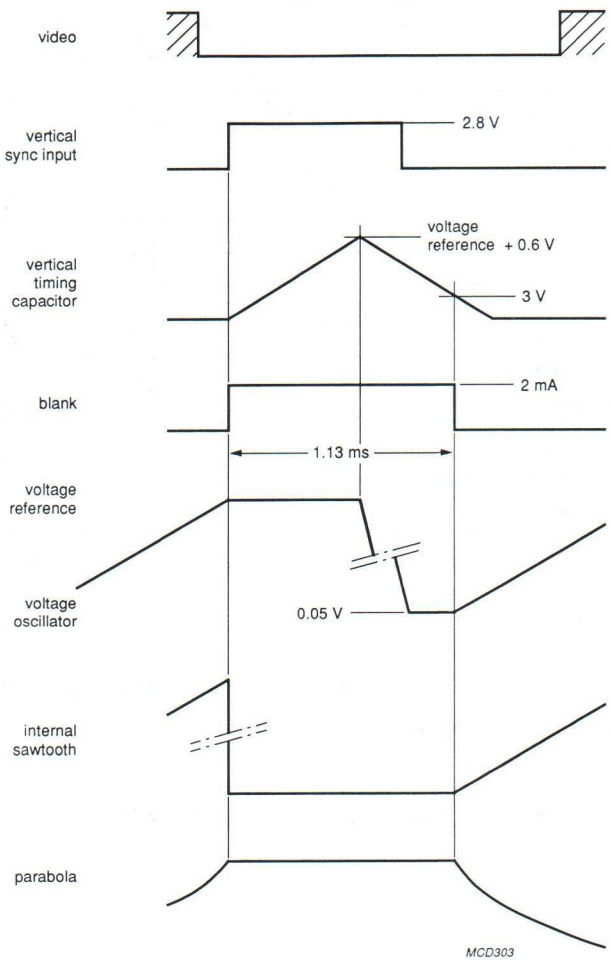


Fig.3 Vertical sawtooth timing.

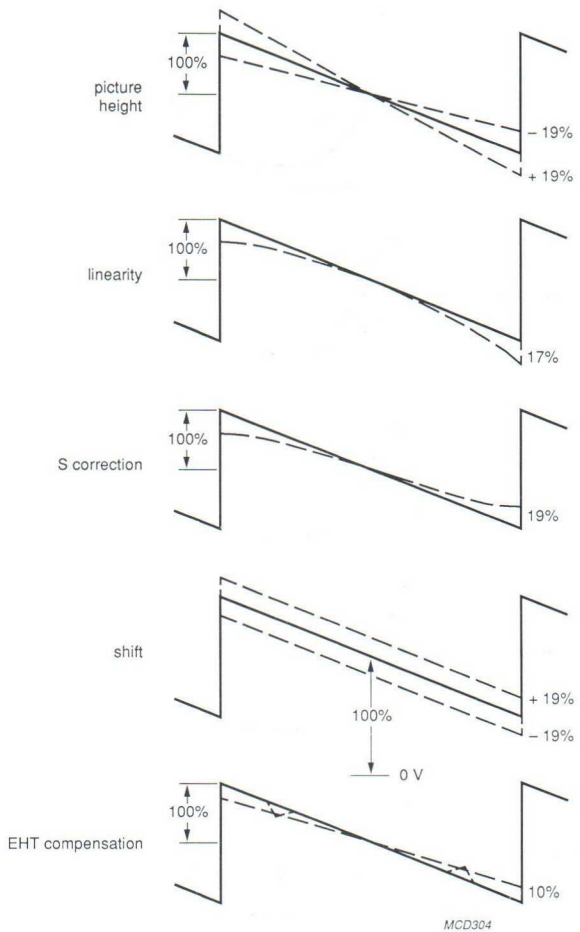


Fig.4 Vertical raster-corrections.

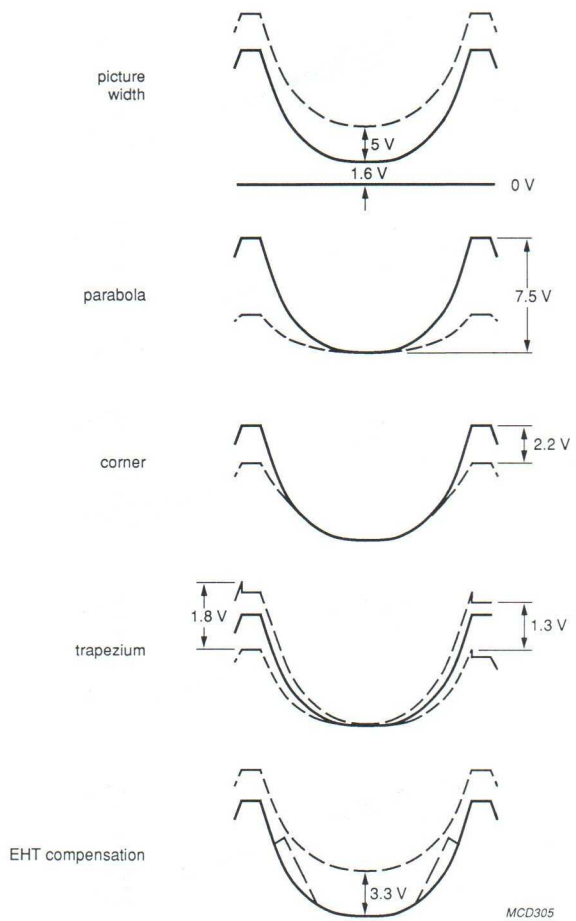


Fig.5 East-west raster-corrections.

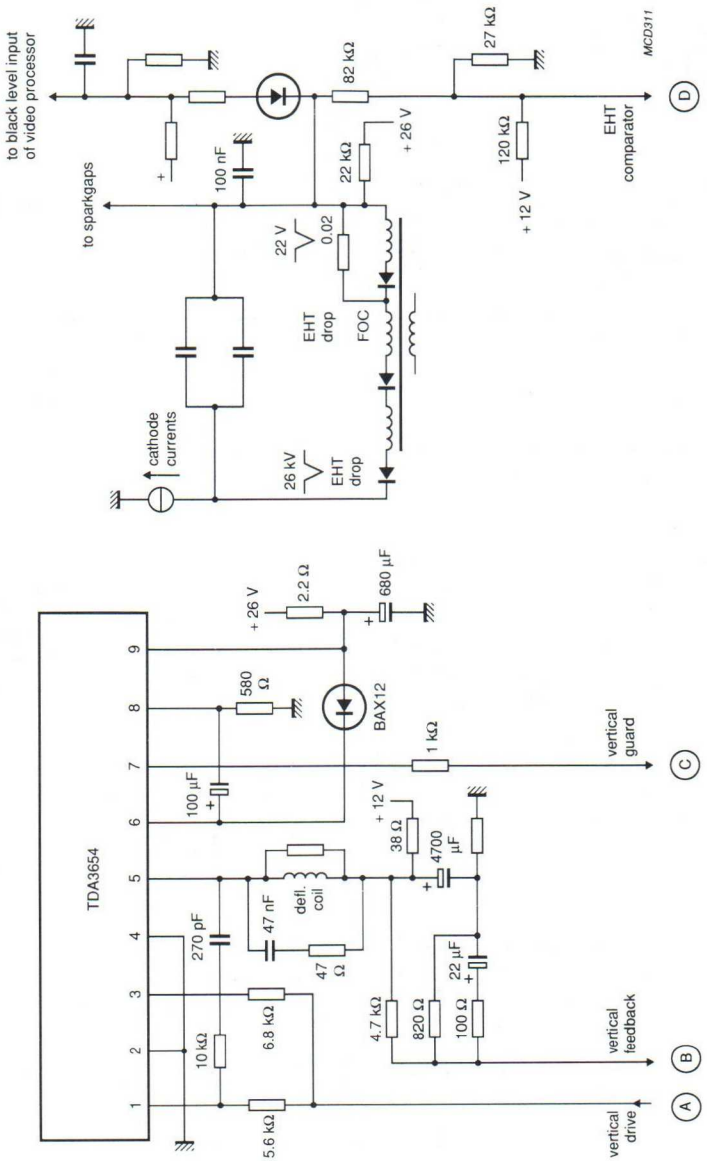


Fig.6 Application diagram (continued in Fig.7).

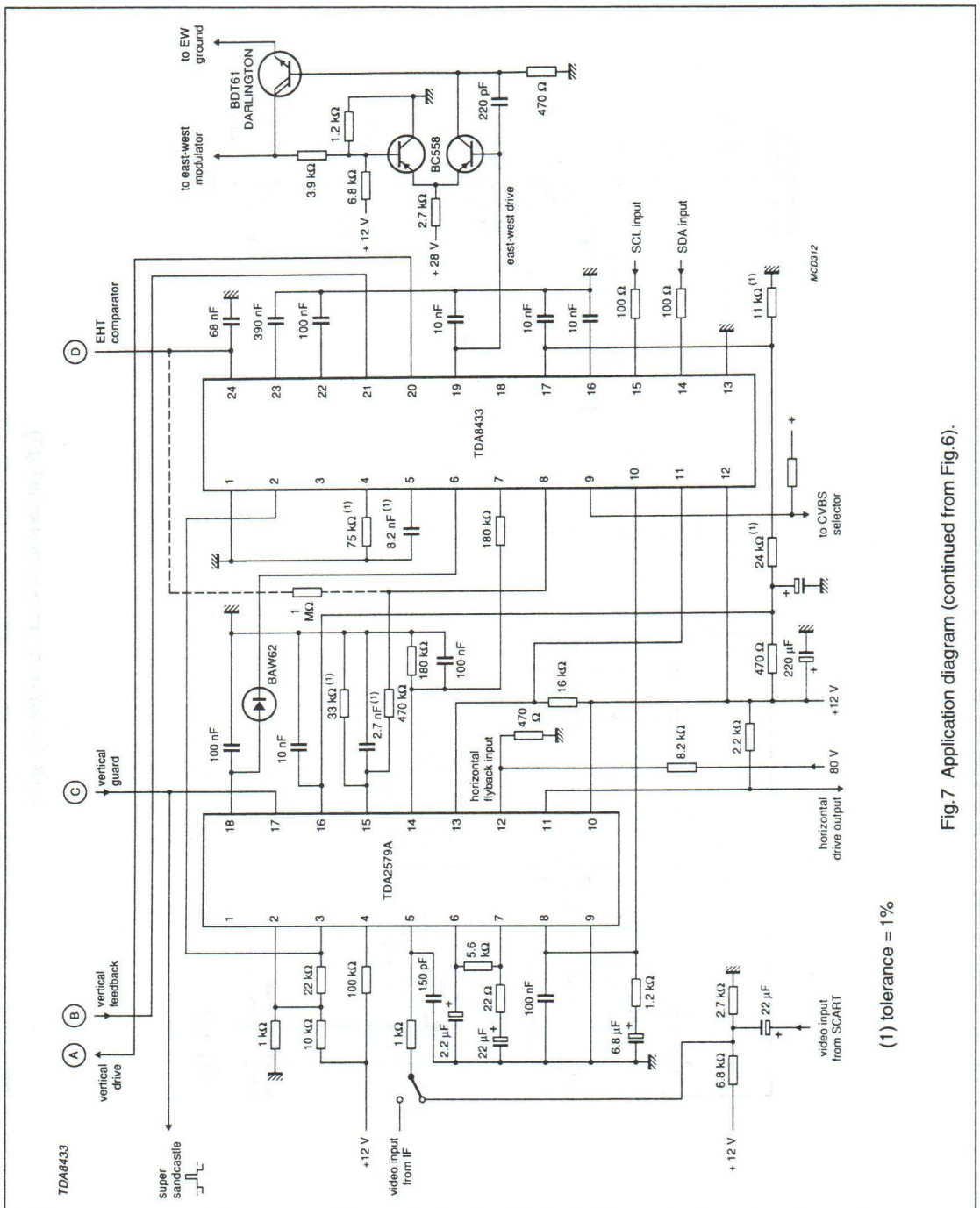


Fig.7 Application diagram (continued from Fig.6).

APPLICATION INFORMATION

The formulae from which the typical vertical drive and typical E-W drive waveforms are generated are given in the following sub-paragraphs. For this purpose a typical application diagram for the vertical drive stage is assumed to be as illustrated in Fig.7. Pin 20 is the vertical drive output which drives an inverting power amplifier. The feedback network, R1 to R4 and C1 and C2, has two functions;

- To transfer the voltage on the feedback pin (pin 21) to a voltage across the feedback resistor R1
- To stabilize the voltage across C1 at a fixed value.

For this typical application the formula for the vertical scan waveform refers to the voltage at pin 21.
The formula for the E-W drive waveform refers to the voltage at pin 19.

All DAC variables that control the vertical and E-W drive waveforms are normalized. Each DAC is defined as having a control range between 0 and 1. The 0 corresponds to a register value of HEX00 and the 1 to a maximum value of HEX1F (for a 5-bit DAC) or HEX3F (for a 6-bit DAC).

Table 4 DAC variables

a: Picture height	$0 < a < 1$	64 steps (6 bits)
y: V-linearity	$0 < y < 1$	64 steps (6 bits)
s: V-S correction	$0 < s < 1$	64 steps (6 bits)
d: V-shift	$0 < d < 1$	64 steps (6 bits)
v: V-compensation	$0 < v < 1$	32 steps (5 bits)
w: Picture width	$0 < w < 1$	64 steps (6 bits)
p: E-W parabola	$0 < p < 1$	64 steps (6 bits)
c: E-W corner	$0 < c < 1$	64 steps (6 bits)
t: Trapezium	$0 < t < 1$	64 steps (6 bits)
h: H-compensation	$0 < h < 1$	32 steps (5 bits)

Further definitions

V_{SAW} = Instantaneous sawtooth voltage (pin 22) normally; $V_{saw} > 0$ $V_{saw} < 7.1$ V; V_{CC} = supply voltage applied to pin 12.

V_{EHT} = EHT compensation voltage applied to pin 1, normally between 1/2 V_{CC} and 1/7 V_{CC}.

V_{OFF} = Internal offset voltage.

V_{int} = Internal reference voltage of 7.1 V (also on pin 4)

$A = 0.80\ (a + 2)/3$	$P = 0.55\ p$
$Y = 0.17\ y$	$C = 0.38\ c$
$S = 0.42\ s$	$T = 0.32\ (1 + 2t)$ volts
$D = 2.4 - 0.7\ d$ volts	$E = (V_{CC} / 2 - V_{EHT}) / 42$
$W = 0.16\ w$	$Z = -1 + 2 \times (V_{saw} - T)\ V_{int}$

If the Trapezium function (T) compensates for the internal offset voltage then the actual formula for Z will simplify to:

$Z = -1 + 2V_{saw}/V_{int}$

Since $0\ V < V_{SAW} < 7.1$ V, this is simply a negative going sawtooth and it follows that: $-1 < Z < 1$.

Vertical drive waveform

The vertical drive waveform has certain interactions between the parameters whereby:

- The S-correction influences the picture height
- The linearity correction can influence the picture shift.

The alignment can be made non-repetitive. Once correct values for the V-S correction and V-linearity are set, the picture height may be changed without affecting the V-S correction and V-linearity on the screen.
The formula for the vertical drive waveform at pin 21 is:

$V_{vert} = D + 1.32\ A\ \{(Z - SA^2\ Z^3)\ (1 - VE) + YZ^2\}$ volts.

Picture height

The amplitude of the sawtooth waveform is controlled by 'A'. It follows therefore that:

$0.53 < A < 0.8$

The nominal value for 'A' is found for a = 0.5, therefore A = 0.67. By programming the picture height, the sawtooth amplitude can be adjusted from −19% to +19%. Without S-correction (S = O) and linearity correction (Y = O), the nominal sawtooth amplitude is (with A = 0.67);

$1.32 \times 0.67 \times 2 = 1.77\ V_{(p-p)}$

V-linearity

This function is meant to compensate for non-linearity of AC coupled vertical output stages. The linearity correction changes proportionally to the picture height setting. The range for linearity control is typically 17% of the peak-to-peak value of the linear sawtooth (see Fig.7).

V-S correction

The range for the V-S correction (SA^2) is defined as a percentage of the undistorted peak-to-peak sawtooth voltage (see Fig.7). The actual S-correction component (SA^2) is dependent on the the picture height setting where:

At maximum picture height (A = 0.80) : $SA^2 = 0.282$
At nominal picture height (A = 0.62) : $SA^2 = 0.197$
At minimum picture height (A = 0.53) : $SA^2 = 0.125$

Picture shift

The DC level of the output is fixed by 'D'. It can be adjusted within a range of −19% to +19%. In actual application this will be used for shifting the picture vertically.

V-compensation

The vertical deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10%, if pin 24 is at $(V_{CC} / 2) - 4.3$ V (maximum modulation i.e. 1.7 V typical). Thus for maximum modulation, the V-drive waveform can be reduced to 90% of its value. There is no reduction when the EHT-compensation input is at $V_{CC} / 2$ V (i.e. 6 V typical).

Trapezium

The trapezium function is the only IC-confined adjustment and is intended to compensate for any internal offsets. The function is called Trapezium because of its effect on the picture if an AC-coupled vertical deflection stage is used. The trapezium function can alter the picture shift range by a maximum of 190 mV. If the trapezium function is used for purposes other than eliminating the internal offsets, then the V-linearity can affect the actual picture height. This can affect the symmetry of the S-correction which, in turn, can affect the V-linearity.

E-W drive waveform

In order to obtain independent control of the picture width, parabola function and th H-compensation on a screen each function has been designed to be dependent on the other two. With reference to Fig.8, the voltage across the H-deflection stage is:

$V_{def1} = V_{supply}\ (1 - W)\ (1 - P)\ (1 - E)$

Where:

V_{supply}	=	supply voltage for H-deflection stage
W	=	picture width alignment
P	=	parabola function
E	=	H-compensation

This shows for instance, that the H-compensation is made dependent on the actual value of the parabola function. For a TV set which needs a large parabola compensation and, also, a large EHT-compensation, this function allows an optimal EHT-compensation independent of the parabola function.
All correction voltages are related to the supply voltage. The TDA8433 is designed to accept a supply voltage of 30 V. Normally higher voltages are employed therefore a voltage amplifier, with a gain of $V_{supply}/30$, is used between the TDA8433 and the diode modulator.

The formula for the E-W drive output voltage at pin 19 is:

$$V_{E\text{-}W} = 30 \times \{1 - (1 - W)(1 - PA^2 Z^2 + CA^4 Z^4)(1 - 1.1 \times hE)\} + 1.8 \text{ V}$$

As can be seen from the formula, the picture width, parabola function and H-compensation are influenced by each other. The functions are discussed separately with the other compensations set to zero.

Picture width control (P-C-h-O)

It is possible to change the picture width by adjusting 'W' from 0 to 0.16. Thus the complete range for the picture control width is −10 to +10%. By only changing the picture width control the output voltage at pin 19 can vary between 1.8 and 6.6 V typical.

Parabola function

The parabola function is also dependent on the picture height function. The values given are valid for a nominal height setting (A = 0.67 V). The parabola function consists of two parts:

- A parabola part - E-W parabola is created by squaring a linear sawtooth. The range of this pure parabola varies from 0 to 25% typical i.e. the amplitude of the parabola waveform is programmable from 0 to 7.5 V (typical).
- A fourth order part - E-W corner is created by squaring the parabola. The range of this corner correction varies from 0 to 7% (typical) i.e. the amplitude of the corner correction waveform is programmable from 0 to −2.2 V (typical). A negative output voltage is not possible. The E-W corner correction waveform has to be subtracted from one of the other alignment functions.

The split-up into the E-W parabola and the E-W corner enables each television set to be aligned with straight vertical lines. The trapezium is also related to the parabola function. The main reason for the trapezium correction is to compensate for internal offsets in the geometry control part. Therefore:

- The amount of trapezium correction is fully dependent on the amount of parabola correction and corner correction that is needed. With no parabola and corner correction the trapezium output will be zero.
- The maximum possible trapezium output is 1.6 V (typical - see Fig.7). This is the case where: a = 0.5, c = 0 and p = 1 i.e. no corner correction and the maximum parabola correction at nominal picture height settings.

H-compensation control

The horizontal deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10% if the input at pin 7 is at $(V_{supply}/2) - 4.3$ V (maximum modulation is 1.7 V typical). With maximum modulation this range corresponds to an output voltage of 0 to 3.3 V. There is no reduction when the EHT-compensation input is at $V_{supply}/2$ V (typical 6 V).

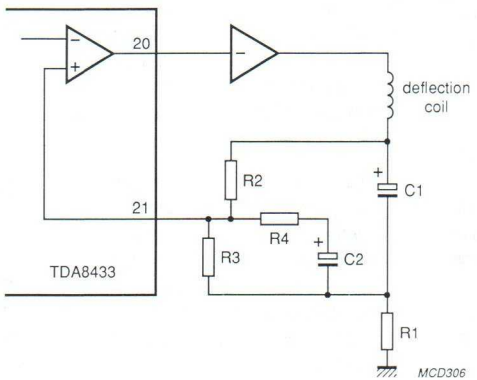


Fig.8 Application diagram of an AC coupled amplifier stage.

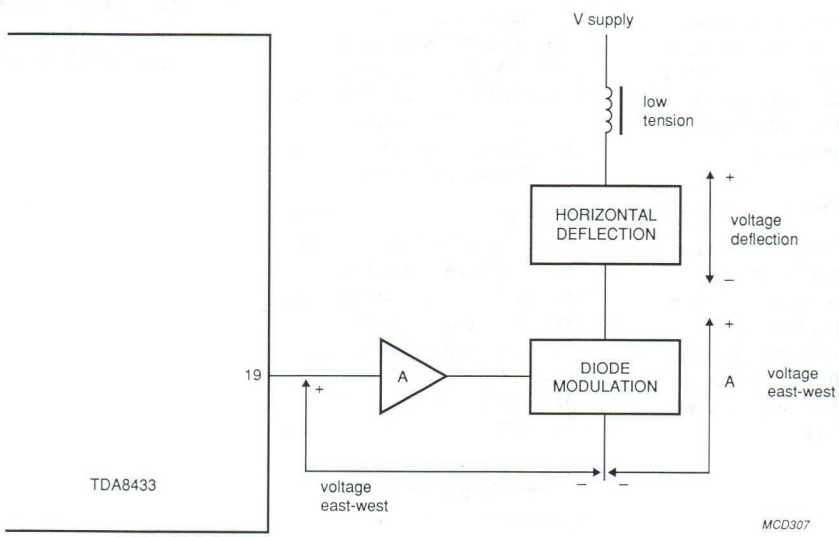


Fig.9 Application diagram for driving the diode modulator.

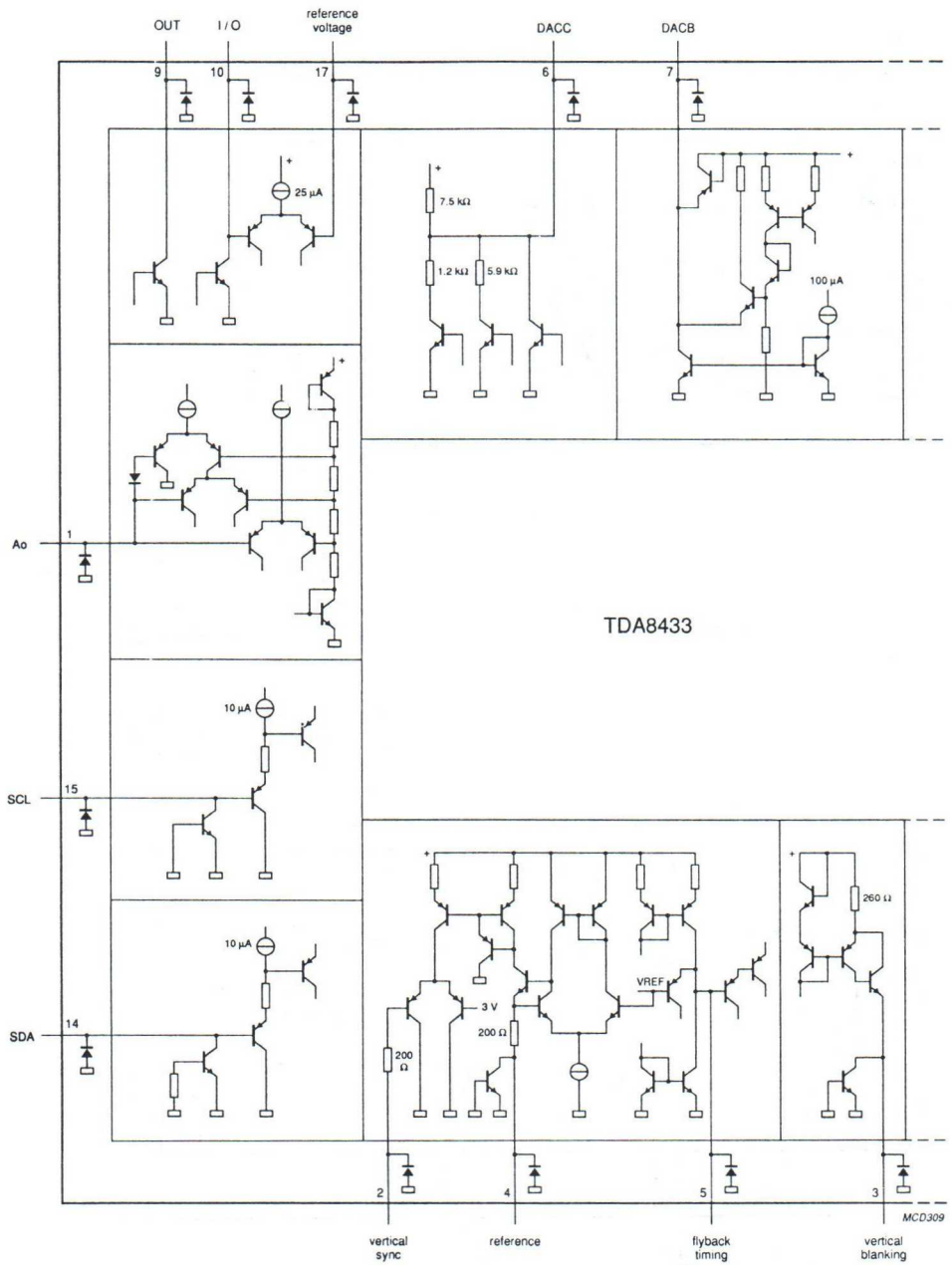


Fig.10 Input/output pin-configuration of TDA8433 (continued in Fig.11).

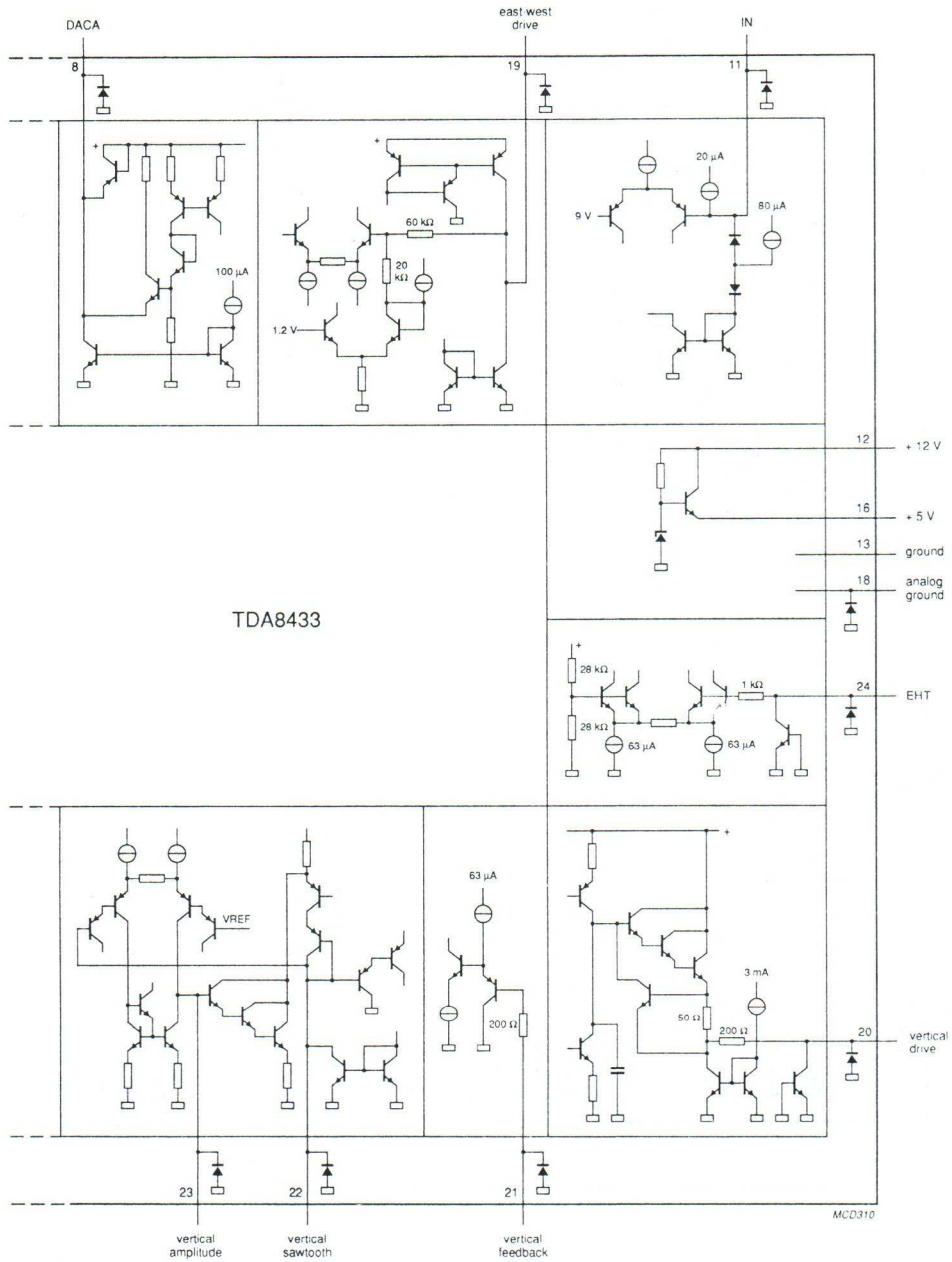


Fig.11 Input/output pin-configuration of TDA8433 (continued from Fig.10).

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

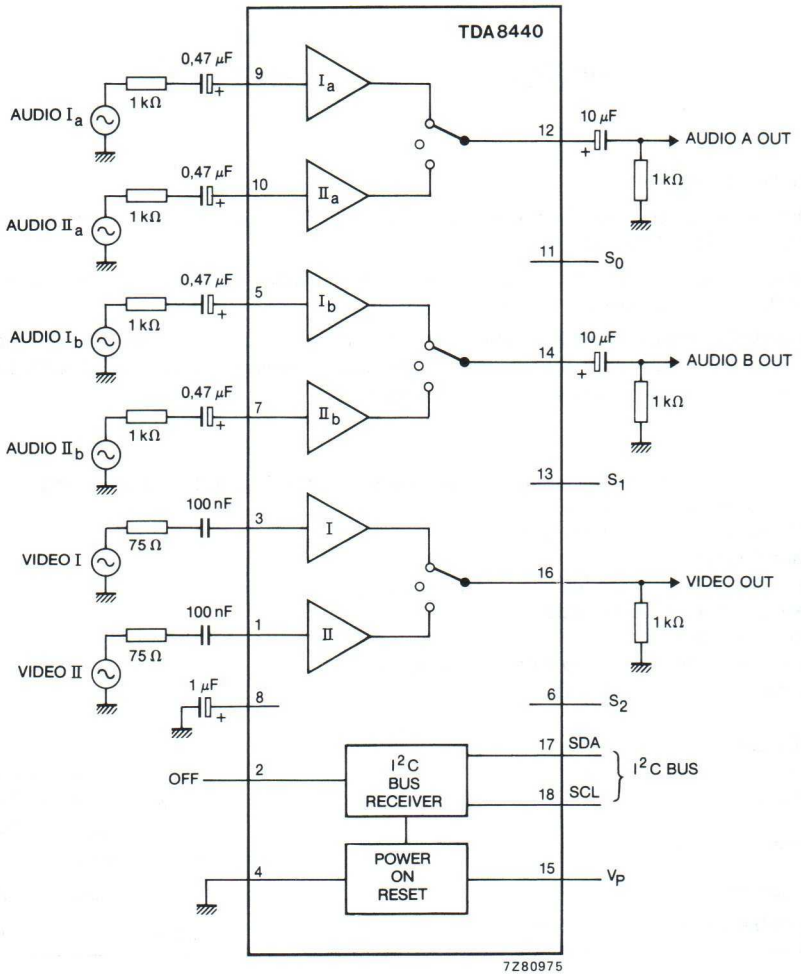
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
} Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	typ.	max.	unit
Supply voltage	pin 15 V_P	–	–	14	V
Input voltage range	pin 17 V_{SDA}	−0,3	–	V_P + 0,3	V
	pin 18 V_{SCL}	−0,3	–	V_P + 0,3	V
	pin 2 V_{OFF}	−0,3	–	V_P + 0,3	V
	pin 11 V_{S0}	−0,3	–	V_P + 0,3	V
	pin 13 V_{S1}	−0,3	–	V_P + 0,3	V
	pin 6 V_{S2}	−0,3	–	V_P + 0,3	V
Video output current	pin 16 $-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}	–	–	+ 125	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Junction temperature	T_j	–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{15-4}	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	A_{3-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{3-16}	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	A_{1-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{1-16}	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	V_{3-4}	–	–	4,5	V
Input video signal amplitude (gain times 1)	V_{1-4}	–	–	4,5	V
Output impedance	Z_{16-4}	–	7	–	Ω
Output impedance in 'OFF' state	Z_{16-4}	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	V_{16-4}	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	V_{16-4}	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9-4(rms)}$	–	–	2	V
	$V_{10-4(rms)}$	–	–	2	V
	$V_{5-4(rms)}$	–	–	2	V
	$V_{7-4(rms)}$	–	–	2	V
Input impedance	Z_{9-4}	50	100	–	kΩ
	Z_{10-4}	50	100	–	kΩ
	Z_{5-4}	50	100	–	kΩ
	Z_{7-4}	50	100	–	kΩ
Output impedance	Z_{12-4}	–	–	10	Ω
	Z_{14-4}	–	–	10	Ω
Output impedance (off state)	Z_{14-4}	100	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL, HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

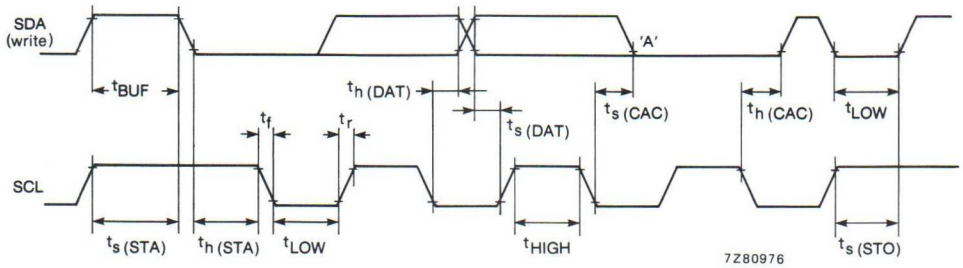


Fig. 2 Timing diagram I^2C bus.

DEVELOPMENT DATA

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

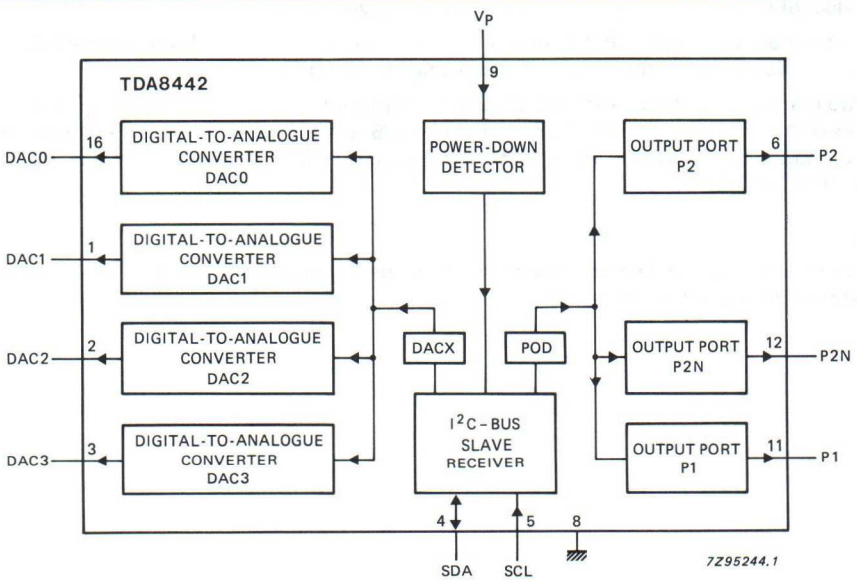


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

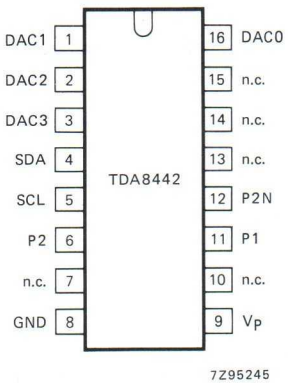


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

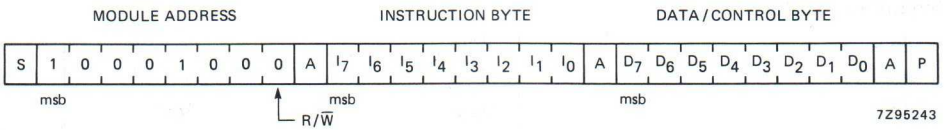


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

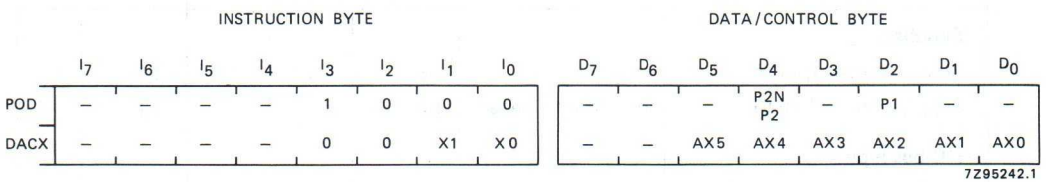


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	1ô	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

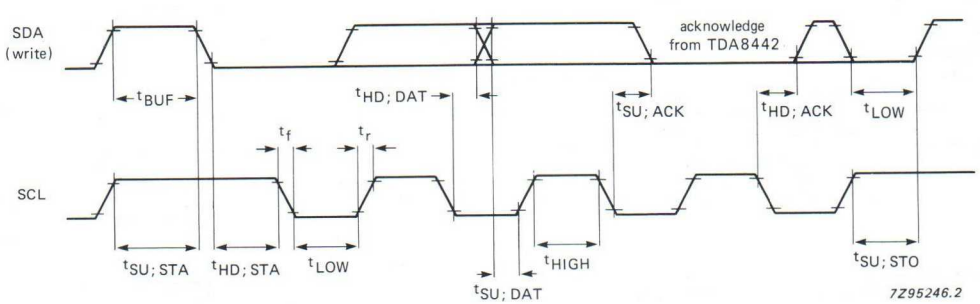
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

I²C-bus controlled YUV/RGB switch TDA8443A

FEATURES

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I²C-bus or non-I²C-bus mode
- Address selection for 7 devices
- Fast switching.

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.

The IC is controlled via I²C-bus by seven different addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		10.8	12.0	13.2	V
I_P	supply current		–	65	90	mA
RGB/YUV channels						
Z_{19-22}	output impedance (pin 19)		–	7	30	Ω
Z_{20-22}	output impedance (pin 20)		–	7	30	Ω
Z_{21-22}	output impedance (pin 21)		–	7	30	Ω
B	bandwidth	−3 dB; mode 0 or 2	–	25	–	MHz
		+3 dB; mode 0 or 2	–	12	–	MHz
		±3 dB; mode 1	–	10	–	MHz
$V_{O(p-p)}$	maximum output amplitude of YUV signals (peak-to-peak value)	gain × 1	2.1	–	–	V
		gain × 2	4.2	–	–	V
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8443A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1

BLOCK DIAGRAM

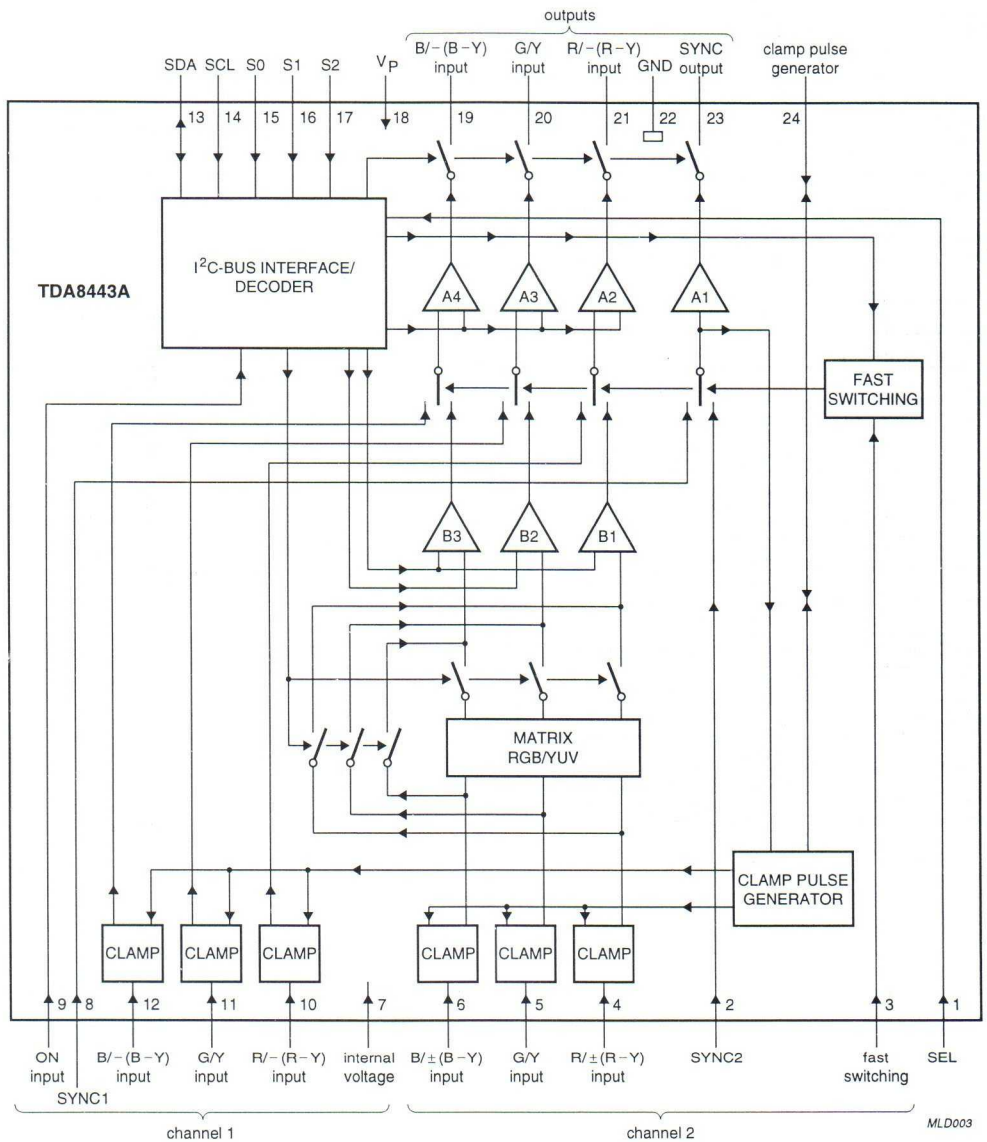


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SEL	1	select input (non-I²C-bus mode only)
SYNC2	2	synchronization input for Channel 2
FS	3	fast switching input
R/±(R–Y)IN	4	R or (R–Y) signal input
G/Y IN	5	G or Y signal input
B/±(B–Y)IN	6	B or (B–Y) signal input
VINT	7	internal voltage supply
SYNC1	8	synchronization input for Channel 1
ON	9	ON input
R/–(R–Y)IN	10	R or –(R–Y) signal input
G/Y IN	11	G or Y signal input
B/–(B–Y)IN	12	B or –(B–Y) signal input
SDA	13	serial data input/output; I²C-bus
SCL	14	serial clock input; I²C-bus
S0	15	address selection input 0
S1	16	address selection input 1
S2	17	address selection input 2
V_P	18	supply voltage
B/–(B–Y)OUT	19	B or –(B–Y) signal output
G/Y OUT	20	G or Y signal output
R/–(R–Y)OUT	21	R or –(R–Y) signal output
GND	22	ground
SYNC	23	synchronization output
CLAMP	24	clamping pulse generator input/output

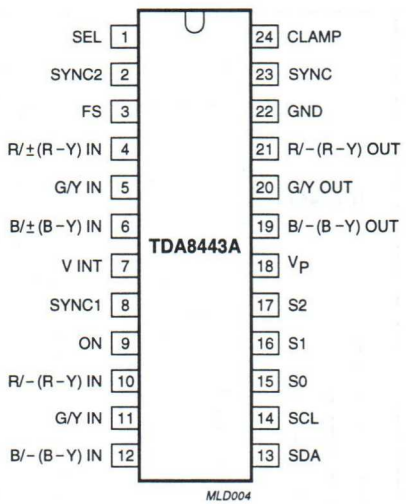


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

RGB signals of Channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of seven devices in parallel (I²C-bus mode).

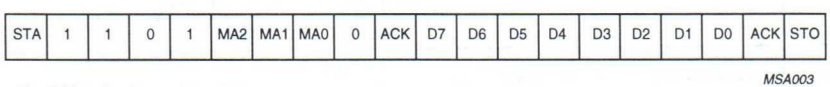
The circuit can be controlled by an I²C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.

Table 1 Protocol bit description

BIT	DESCRIPTION
STA	start condition
MA2 to MA0	address selection bits; see Table 2
ACK	acknowledge bit
D7	channel selection bit; see Table 3
D6	matrix selection bit; see Table 3
D5 to D3	gain control bits; see Table 4
D2	fast switching priority bit; see Table 5
D1 and D0	output state control bits; see Table 6
STO	stop condition



See Table 1.

Fig.3 I²C-bus protocol.

Table 2 Address selection

ADDRESS SELECT PINS[1][2]			ADDRESS SELECT BITS		
S2 (PIN 17)	**S1 (PIN 16)**	**S0 (PIN 15)**	**MA2**	**MA1**	**MA0**
L	L	L	*[3]	*[3]	*[3]
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Notes

1. L = LOW level input voltage.
2. H = HIGH level input voltage.
3. * = non-I²C-bus operation.

Table 3 Mode control bits D7 and D6

MODE	D7	D6	FUNCTION
0	0	0	Channel 2 selected, no matrix
1	0	1	Channel 2 selected, matrix active
2	1	0	Channel 1 selected
–	1	1	not allowed

Table 4 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	–1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed		–	–
0	1	1	1	1	–1	0.45
1	0	0	2	2	–1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	–1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3R + 0.59G + 0.11B$

$R-Y = 0.7R - 0.59G - 0.11B$

$B-Y = -0.3R - 0.59G + 0.89B$

Table 5 Priority/fast switching bit D2

D2	FAST SWITCHING (PIN 3)	MODE
0	X[1]	0 to 2, depending on D7, D6
1	0.4 V	2

Note

1. X = don't care.

Table 6 Output state control bits

D1	D0	PIN 9	FUNCTION
0	X[1]	X[1]	OFF
1	0	L	OFF
1	0	H	ON
1	1	X[1]	ON

Note

1. X = don't care.

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

Table 7 Non-I²C-bus mode (S2 = S1 = S0 = L)

CONTROL			MODE SWITCHED BY FS (PIN 3)	GAIN SETTINGS		B1, B3	B2
PIN 13	PIN 14	PIN 1		A1	A4, A3, A2		
L	L	L	2 or 0	1	1	1	1
L	L	H	2 or 0	1	2	1	1
L	H	L	2 or 1	1	1	−1	0.45
L	H	H	2 or 0	1	1	−1	0.45
H	L	L	2 or 0	2	1	1	1
H	L	H	2 or 0	2	2	1	1
H	H	L	2 or 1	2	1	−1	0.45
H	H	H	2 or 0	2	1	−1	0.45

Table 8 Fast switching input (pin 3)

FS	MODE SELECTED
≤0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 9 ON input (pin 9)

ON	FUNCTION
L	OFF; no output signal; high impedance OFF-state
H	function is determined in Table 7

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	–	14	V
$V_{I(SDA)}$	input voltage (pin 13)	–0.3	14	V
$V_{I(SCL)}$	input voltage (pin 14)	–0.3	14	V
V_n	input voltage any other pin	–0.3	V_P + 0.3	V
$I_{O(max)}$	maximum output current	–	20	mA
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	IC storage temperature range	–55	+125	°C
T_j	maximum junction temperature	–	+125	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		10.8	12.0	13.2	V
I_P	supply current		–	65	90	mA
RGB/YUV channels						
G_{abs}	absolute gain difference (programmed value)		–	0	10	%
G_{rel}	relative gain difference	between Y output and the (R–Y) and (B–Y) channel outputs	–	0	10	%
		between any other two channels	–	0	5	%
I_I	input current		–	0.5	1.0	μA
$\lvert Z_{19-22}\rvert$	output impedance (pin 19)		–	7	30	Ω
$\lvert Z_{20-22}\rvert$	output impedance (pin 20)		–	7	30	Ω
$\lvert Z_{21-22}\rvert$	output impedance (pin 21)		–	7	30	Ω
B	bandwidth	–3 dB; mode 0 or 2	–	25	–	MHz
		+3 dB; mode 0 or 2	–	12	–	MHz
		±3 dB; mode 1	–	10	–	MHz
t_{diff}	mutual time difference at output	all inputs of one source connected together	–	–	25	ns
$V_{o(p-p)}$	maximum output amplitude of YUV signals (peak-to-peak value)	gain × 1	2.1	–	–	V
		gain × 2	4.2	–	–	V
α_{ct}	crosstalk	note 1; f_i = 5 MHz; between inputs of same source	–	–	–30	dB
		note 1; between same source	–	–	–40	dB
α_{off}	isolation (OFF state)	f_i = 10 MHz	50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{diff(p-p)}$	differential gain at nominal output signals (peak-to-peak value)	R–Y = 1.05 V (p-p)	–	–	10	%
		B–Y = 1.33 V (p-p)	–	–	10	%
		Y = 0.34 V (p-p)	–	–	10	%
S/N	signal-to-noise ratio	nominal input; B = 5 MHz; note 2	50	–	–	dB
SVRR	supply voltage ripple rejection	note 3	30	–	–	dB
V_O	DC output levels during clamping		–	5.3	–	V
Synchronization channels						
G_{diff}	gain difference (programmed value)		–	–	10	%
B	bandwidth	–3 dB	–	50	–	MHz
		+3 dB; gain × 1	–	20	–	MHz
		±3 dB; gain × 2	–	13	–	MHz
$V_{i(p-p)}$	input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		0.2	–	2.5	V
$\|Z_{23-22}\|$	output impedance (pin 23)		–	20	30	Ω
$V_{o(p-p)}$	maximum undistorted output amplitude (pin 23) (peak-to-peak value)		2.5	–	–	V
V_O	DC output level on top of sync pulse		1.5	1.9	2.4	V
I²C-bus inputs for SDA, SCL						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
I²C-bus output for SDA (open collector)						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Address selection inputs for S0, S1, S2						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	10	µA
I_{IL}	LOW level input current		–50	–10	0	µA
Fast switching input						
V_{IH}	HIGH level input voltage		1	–	3	V
V_{IL}	LOW level input voltage		–0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	500	µA
I_{IL}	LOW level input current		–100	–	–	µA
t_{sw}	switching time	see Fig.5	–	10	–	ns
t_d	switching delay	see Fig.5	–	20	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Select input						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		−0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	10	μA
I_{IL}	LOW level input current		−50	−10	0	μA
ON input						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	μA
I_{IL}	LOW level input current		–	–	10	μA

Notes

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20\log\frac{V_{o(p-p)}}{V_{no(rms)}}$ (B = 5 MHz)
3. Supply voltage ripple rejection = $20\log\frac{V_{RR(supply)}}{V_{RR(at\ the\ output)}}$

TIMING CHARACTERISTICS

I²C-bus load conditions: 4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND; all values are referenced to V_{IH} = 3 V and V_{IL} = 1.5 V; see Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.
t_{BUF}	time bus must be free before start		4.7	–	µs
$t_{SU;STA}$	set-up time for start condition		4.7	–	µs
$t_{HD;STA}$	hold time for start condition		4.0	–	µs
t_{LOW}	SCL and SDA LOW time		4.7	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	µs
t_r	SCL and SDA rise time		–	1.0	µs
t_f	SCL and SDA fall time		–	0.3	µs
$t_{SU;DAT}$	data set-up time (write)		250	–	ns
$t_{HD;DAT}$	data hold time (write)	note 1	1.0	–	µs
$t_{SU;ACK}$	acknowledge set-up time		–	2	µs
$t_{HD;ACK}$	acknowledge hold time		0	–	µs
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. Timing $t_{HD;DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 µs must occur before transmission may be resumed.

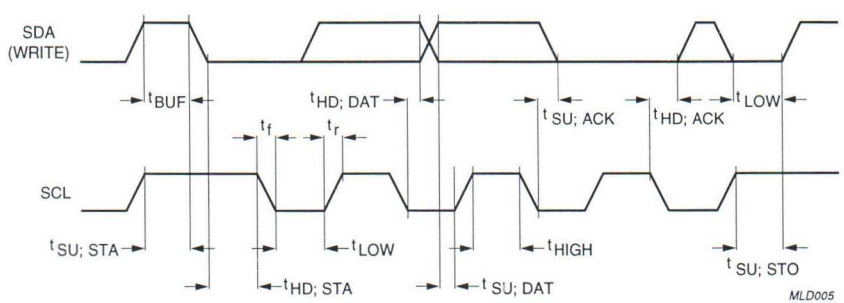


Fig.4 I²C-bus timing diagram.

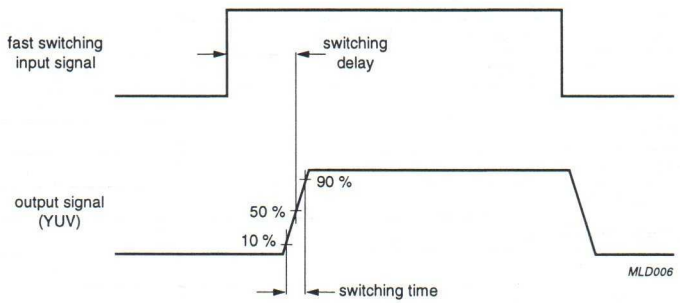


Fig.5 Fast switching signal diagram.

APPLICATION INFORMATION

Table 10 Channel input/output information

INPUT 1	INPUT 2	OUTPUT	MODE	D5	D4	D3
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	2	1	1	1
–	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	1	1	1	1
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	2	1	0	0
–	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	1	1	0	0
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	2	1	0	1
–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	0	1	0	1
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	2	1	1	0
–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	0	1	1	0

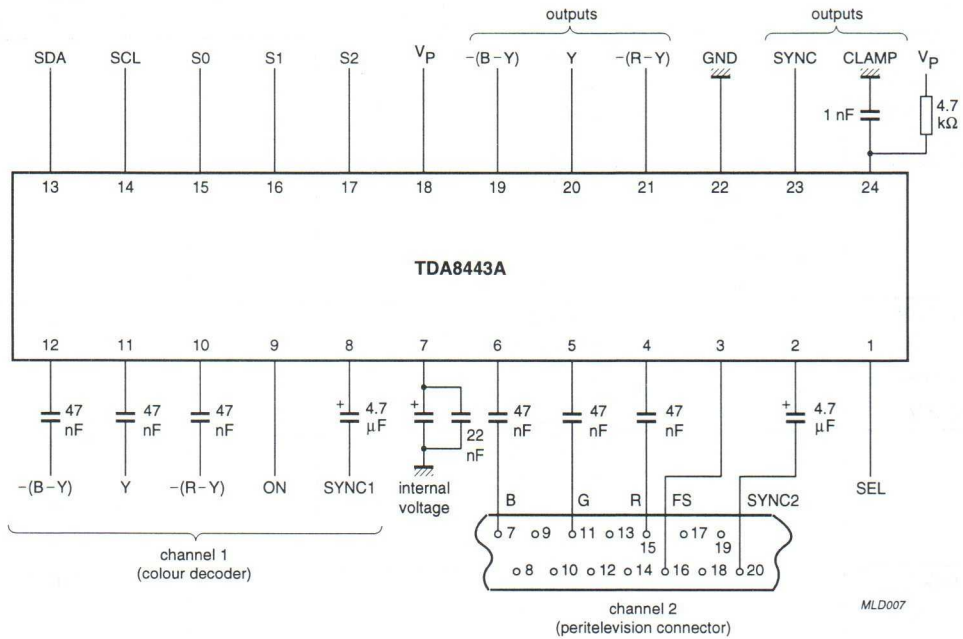


Fig.6 Application diagram (example).

Input clamps

The R, G, B respectively (R–Y), Y and (B–Y) video signals are AC-coupled to the IC where they are clamped on the black level. The timing information for this clamping action is derived from the associated synchronization signal SYNC, which could also consist of the composite video information signal CVBS. The syncsignal is AC-coupled to the IC where it is clamped on top-sync level, information obtained from this action is used to generate the clamp pulses.

The clamp pulses can be generated in two ways:

1. Using the sync information (internal clamping)

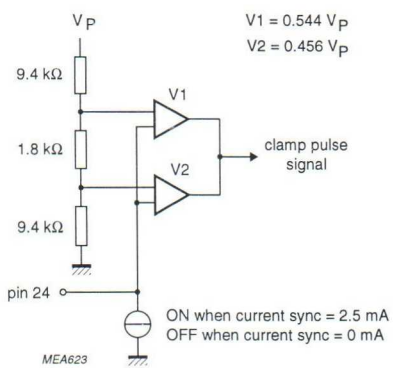
   The sync information is clamped on top-sync and the information obtained from this action is used to switch an internal current source at pin 24.

   Pin 24 should be connected to V_P via a 4.7 kΩ resistor, and a 1 nF capacitor to ground. During video scan the voltage at pin 24 will be HIGH (equals positive supply voltage). During the synchronization pulses the voltage at pin 24 will drop to zero because of the current sink (2.5 mA).

   When the synchronization pulse is over, the current source is switched off and the voltage at pin 24 will rise to its higher level. Because of the time constant at pin 24, the restoration will take some microseconds. The voltage at pin 24 is also sensed internally and at the time it is between $0.456V_P$ and $0.544V_P$, a time pulse is generated and used for the clamping action.

2. Using a sandcastle pulse (external clamping)

   If an associated sandcastle pulse is available, it can also be used as a clamping pulse. In this event the sandcastle pulse should be connected to pin 24, the top of the clamping pulse should be between $0.544V_P$ and $0.456V_P$. The timing of the internal clamping pulse will be equal to the timing of the higher part of the sandcastle pulse. If the sync signal is also connected, the current sink will also become active during the synchronization pulses. This means that the sandcastle pulse should be connected to pin 24 via a 1 kΩ dropping resistor. In this event only the sandcastle pulse at pin 24 will be influenced during sync pulses, but the sandcastle pulse at the sandcastle source will be unchanged.



Tolerance on V1 and V2 is given by $\Delta R/R$ and $\Delta V_P/V_P$. The diffusion process gives $\Delta R/R$ (max) = 1.5%.

Fig.7 Clamping circuit.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

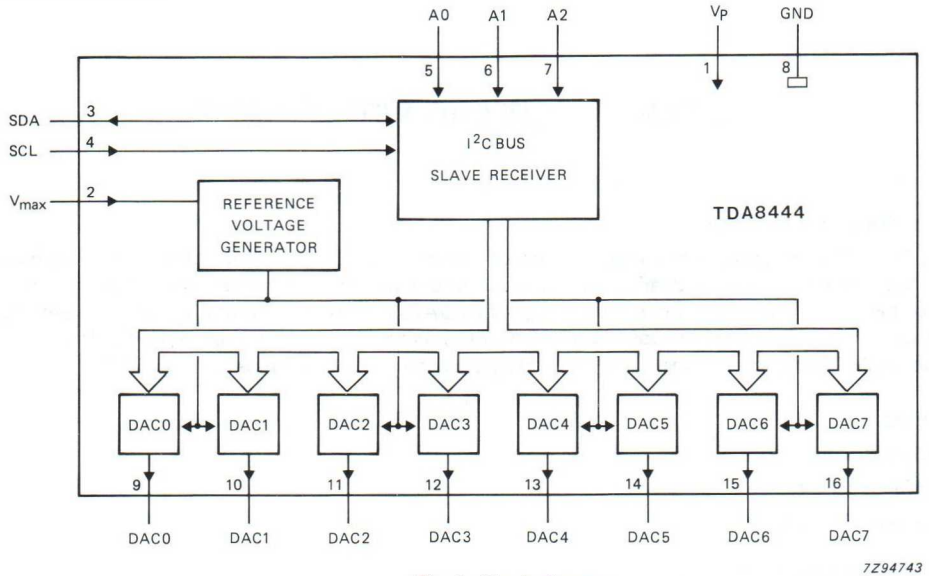


Fig. 1 Block diagram.

PINNING

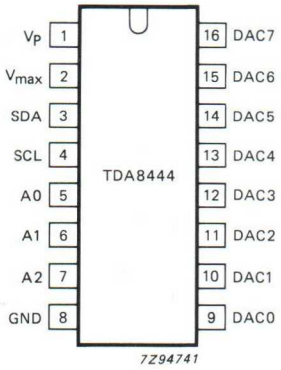


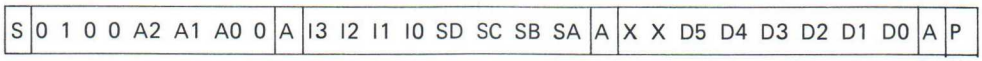
Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:



Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	5	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

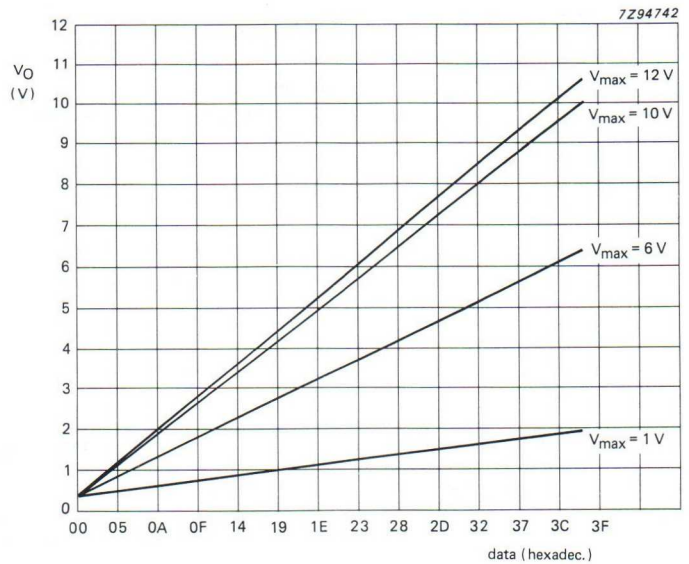


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

Fast RGB/YC switch for digital decoding TDA8446

FEATURES

- R, G, B clamped inputs
- Luminance and chrominance difference matrix
- Y-clamped inputs
- Fast switching between internal and external Y
- Chrominance input
- Amplifier with selectable gain
- 3-state switch for chrominance output.

DESCRIPTION

The TDA8446 is a video switch which has been designed for use in Digital Multistandard System Decoders (DMSD) in digital video system. The device is intended for matrixing incoming RGB signals and for switching between luminance signals. It generates a SYNC signal and TTL clamping pulses from any video signal with sync pulses.

APPLICATIONS

- Digital TV systems
- Desktop video architecture.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	10.8	–	13.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8446	DIP20	plastic dual in-line package; 20 leads; (300 mil)	SOT146-1
TDA8446T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

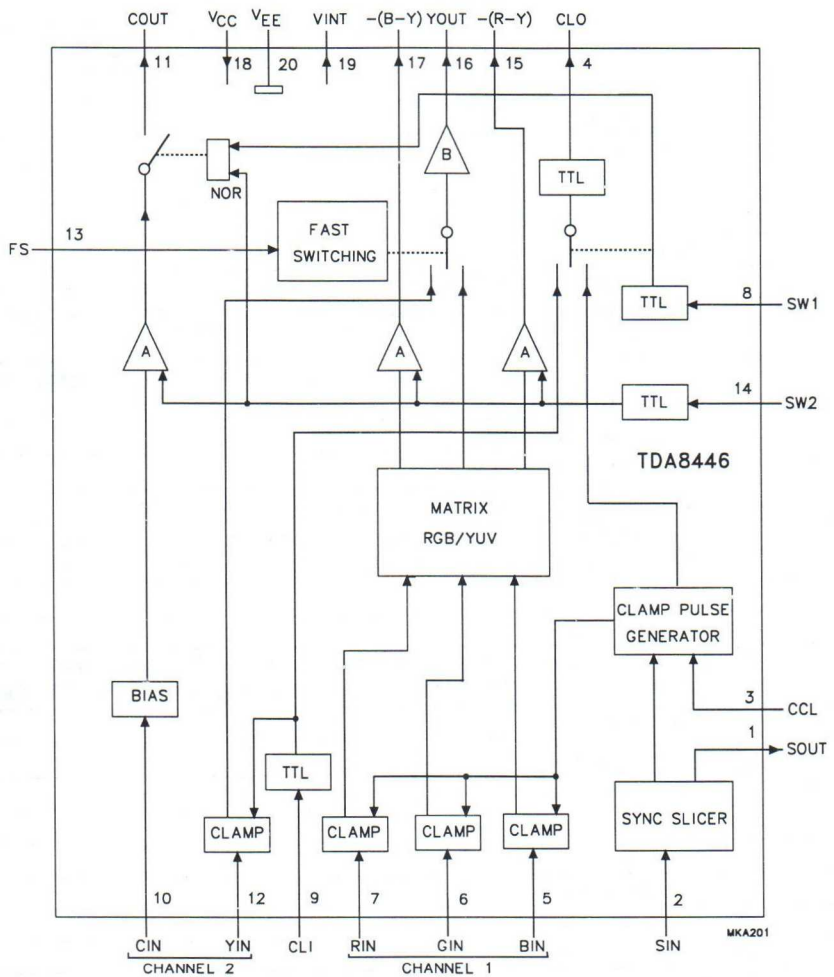


Fig.1 Block diagram (TDA8446).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP20	SO28	
SOUT	1	1	synchronization signal output; this output provides the synchronization information extracted from the incoming signal at pin 2 (SIN).
SIN	2	2	synchronization signal input; CSYNC or CVBS signal from the peri-connector
CCL	3	3	clamping capacitor connection; the clamping pulse is generated by external circuitry connected to this pin, the generated pulse clamps the RGB inputs.
n.c.	–	4	not connected
CLO	4	5	clamping pulse output
n.c.	–	6	not connected
BIN	5	7	B-signal input
GIN	6	8	G-signal input
RIN	7	9	R-signal input
SW1	8	10	clamping control signal input; this TTL signal is used to select the clamp signal, a LOW level at this input forces the circuit to output the generated clamping pulse.
n.c.	–	11	not connected
CLI	9	12	clamping pulse input; this TTL signal indicates the black level clamping period for the incoming Y signal (active-HIGH).
CIN	10	13	chrominance signal input
COUT	11	14	chrominance signal output
YIN	12	15	luminance signal input; this input also accepts the CVBS signal
FS	13	16	fast switching signal input; this signal is used to control fast switching of the luminance signals, a HIGH level at this input forces the circuit to output the internal Y signal.
n.c.	–	17	not connected
n.c.	–	18	not connected
SW2	14	19	gain control signal input; this TTL signal is used to set the gain of the chrominance amplifiers (A), a LOW level at this input forces the gain A to 6 dB (HIGH forces to 0 dB).
n.c.	–	20	not connected
–(R-Y)	15	21	–(R–Y) signal output
YOUT	16	22	luminance signal output
–(B–Y)	17	23	–(B–Y) signal output
n.c.	–	24	not connected
n.c.	–	25	not connected
V_{CC}	18	26	positive supply voltage (+12 V)
VINT	19	27	internal decoupling
V_{EE}	20	28	ground

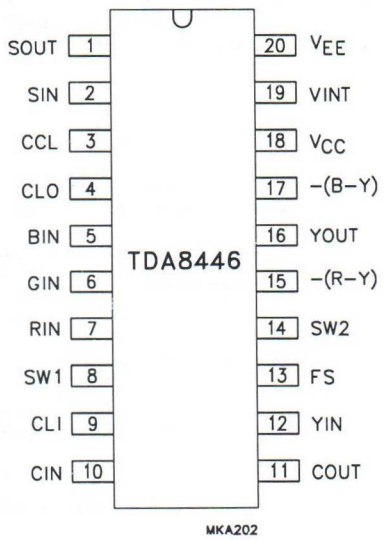


Fig.2 Pin configuration (DIP20).

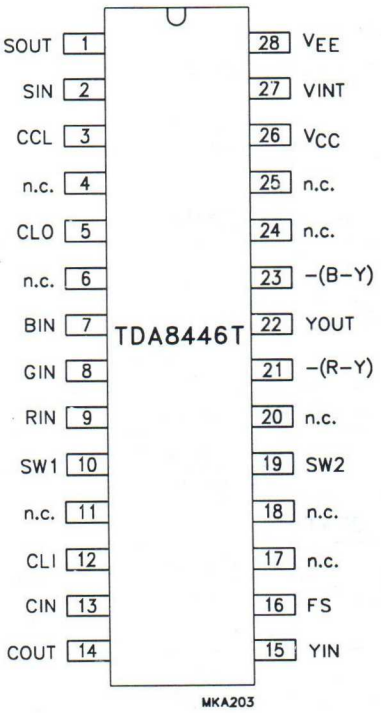


Fig.3 Pin configuration (SO28).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	+14	V
V_I	input voltage	−0.3	+12.3	V
T_{stg}	storage temperature	−55	+125	°C

HANDLING

Each pin will withstand the ESD test in accordance with MIL-STD-883C class 2 (2000 V to 2999 V). Method 3015 (Human body model: R = 1500 Ω; C = 100 pF) 3 pulses positive and 3 pulses negative on each pin as a function of ground. The IC will withstand 500 V in accordance with UZW-BO/FQ-B302 (Machine model: R = 0 Ω; C = 200 pF; L = 2.5 μH) 3 pulses positive and 3 pulses negative.

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply/temperature					
V_{CC}	supply voltage	10.8	–	13.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C
TTL inputs (SW1, SW2 and CLI)					
V_{IH}	HIGH level input voltage	2	–	V_{CC}	V
V_{IL}	LOW level input voltage	−0.3	–	+0.8	V
SYNC signal (SIN)					
$V_{S(p-p)}$	sync amplitude (peak-to-peak value)	0.2	–	2.5	V
Fast Switching input (FS)					
V_{IH}	HIGH level input voltage	1	–	3	V
V_{IL}	LOW level input voltage	0	–	0.4	V
Video inputs (RIN, GIN, BIN, CIN, YIN)					
$V_{i(p-p)}$	video amplitude on RIN, GIN and BIN inputs (peak-to-peak value)	–	0.7	1	V
C_I	input capacitance	–	100	–	nF
Clamping pulse generator (CCL)					
R_{clamp}	clamping resistance	–	4.7	–	kΩ
C_{clamp}	clamping capacitance	–	1	–	nF

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current		–	–	75	mA
SVRR	supply voltage rejection ratio	note 1	30	–	–	dB
Y and R, G, B channels						
I_{CL}	input clamping current	V_{CC} = 6 V; V_I = 0 V	0.3	–	–	mA
I_I	input current	V_I = 9 V	–1.5	+0.5	+1.5	µA
G_A	gain of amplifier A	f_i = 1 MHz; V_{SW2} = 2 V	–1	0	+1	dB
		f_i = 1 MHz; V_{SW2} = 0.8 V	5	6	7	dB
G_B	gain of amplifier B	f_i = 1 MHz	–1	0	+1	dB
	RGB matrixed according to the following equations: Y = 0.30R + 0.59G + 0.11B R–Y = 0.70R – 0.59G – 0.11B B–Y = –0.30R – 0.59G + 0.89B					
ΔG_{diff}	relative gain difference	note 2	–	0	10	%
$\lvert\Delta G\rvert$	maximum gain variation	100 kHz < f_i < 8 MHz	–	3	–	dB
R_O	output resistance		–	15	–	Ω
Δt	time difference at output	f_i = 1 MHz; note 3	–	–	25	ns
V_O	DC output level	V_{CCL} = 6 V	–	4.2	–	V
t_{fsd}	fast switching delay	see Fig.4	–	20	–	ns
t_{fs}	fast switching time	see Fig.4	–	10	–	ns
I_{IFS}	input current on fast switching control (pin 13)	V_I = 0.4 V	–	0.7	–	µA
		V_I = 1 V	–	0.5	–	µA
Chrominance channel (CIN, COUT)						
R_i	internal input resistance		–	50	–	kΩ
V_O	DC output level	I_I = 0	–	5	–	V
G_A	gain of amplifier A	f_i = 1 MHz; V_{SW1} = V_{SW2} = 2 V	–1	0	+1	dB
		f_i = 1 MHz; V_{SW2} = 0.8 V	5	6	7	dB
$\lvert\Delta G\rvert$	maximum gain variation	100 kHz < f_i < 8 MHz	–	3	–	dB
α_{off}	isolation (off state)	f_i = 5 MHz; V_{SW1} = V_{SW2} = 0.8 V	–	60	–	dB
Z_o	output impedance	V_{SW1} = V_{SW2} = 0.8 V	100	–	–	kΩ
R_o	output resistance		–	7	–	Ω
TTL inputs (SW1, SW2, CLI)						
I_{IH}	HIGH level input current	V_{IH} = 2 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0.8 V	–	–	–600	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp output (CLO)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 10 μA	2.4	–	–	V
Synchronization channel (SOUT)						
$V_{o(p-p)}$	output amplitude (peak-to-peak value)		0.2	–	1.5	V

Notes

1. Supply voltage rejection ratio = $20\log\frac{V_{R(CC)}}{V_{R(O)}}$
2. The relative gain difference is measured when only one input signal (R, G or B) is present.
3. The inputs RIN, GIN and BIN are interconnected; Δt is the maximum time coincidence error between the luminance and the chrominance signals.

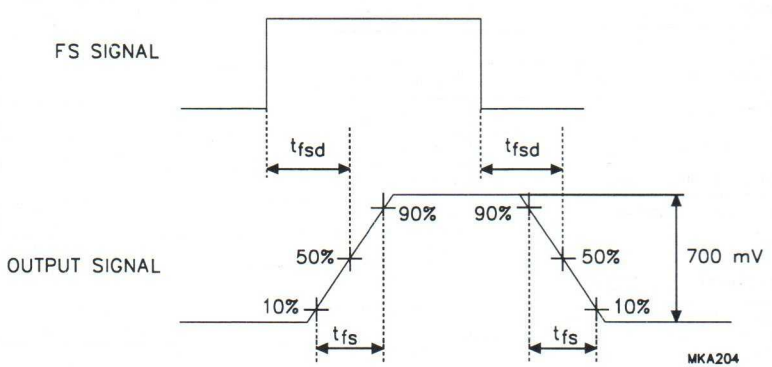


Fig.4 Fast switching times.

APPLICATION INFORMATION

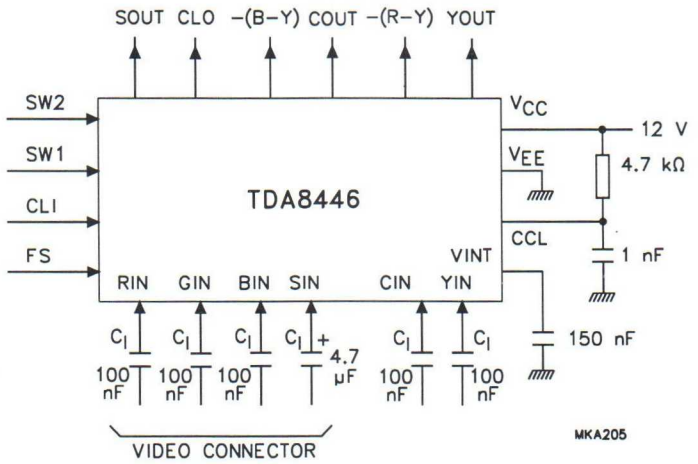


Fig.5 Typical application circuit.

P^2CCD DELAY LINE AND MATRIX

GENERAL DESCRIPTION

The TDA8451A is an integrated P^2CCD (Profiled Peristaltic Charge Coupled Device) delay line and matrix which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates two delay lines with a delay length of 1 line time for colour difference signals, adding circuits for the delayed and direct signals and clock drivers for the delay lines which are driven from an internal voltage controlled oscillator (VCO) locked to the sandcastle pulse.

The TDA8451A differs from the TDA8451 by the following:

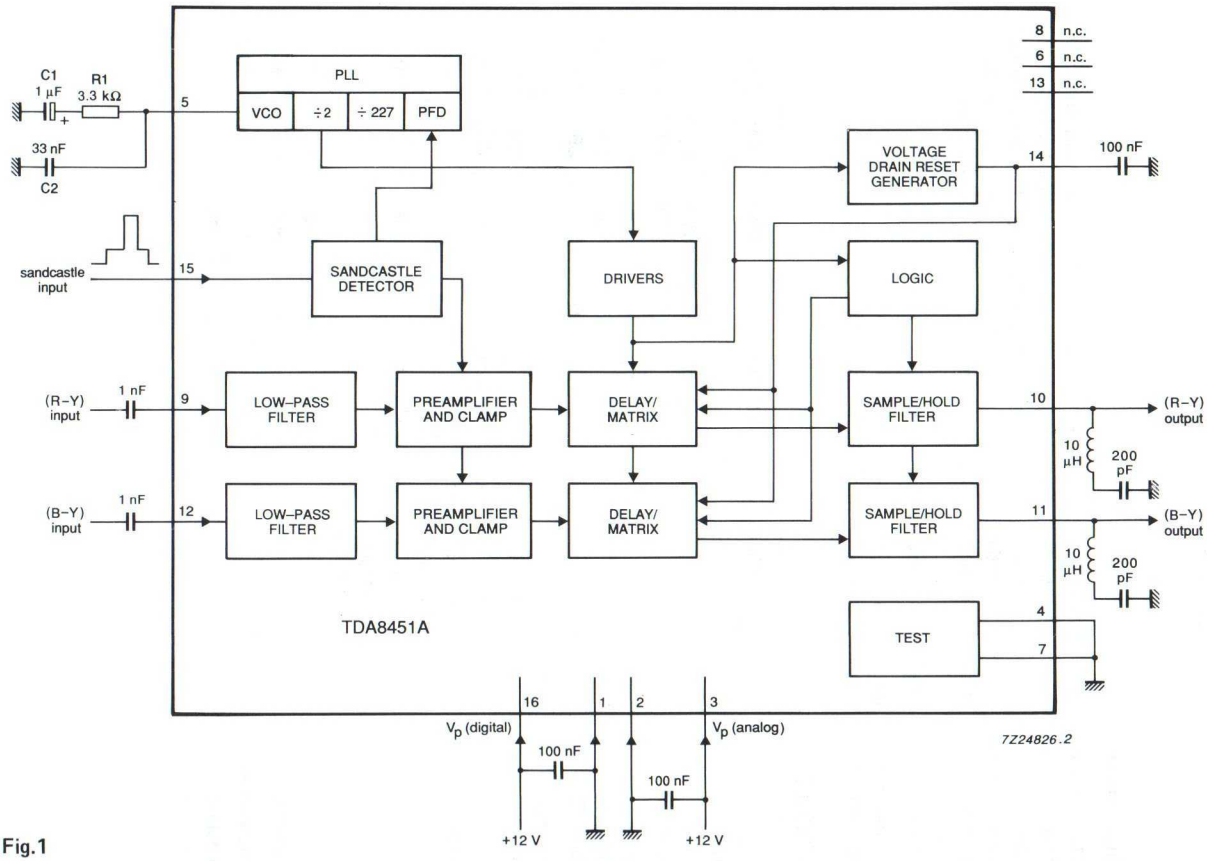
- The VCO is line locked instead of sub-carrier locked
- Adding direct and delayed signals occurs for PAL, SECAM and NTSC

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 3)		$V_{P(a)}$	10.8	12.0	13.2	V
digital (pin 16)		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 3)		$I_{P(a)}$	5	10	15	mA
digital (pin 16)		$I_{P(d)}$	10	22	35	mA
Colour difference input signals (peak-to-peak value)	PAL/NTSC mode	$V_{I(p-p)}$	–	–	1.1	V
	SECAM mode	$V_{I(p-p)}$	–	–	2.1	V
Output signals	PAL/NTSC mode 0.8 V(p-p) input	V_O	–	0.8	–	V
	SECAM mode 1.6 V(p-p) input	V_O	–	0.8	–	V
Output resistance		R_O	–	500	–	Ω
Frequency response		Δf	–	1.3	–	MHz
Additional delay		t_d	–	760	–	ns

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).



Notes to Fig.1

1. If the TDA8451A is followed by a TDA4566 (CTI), it is recommended to replace the LC trap (and the usual RC low-pass filter in front of the TDA4566) by an LC low-pass circuit where L = 47 μH and C = 270 pF.
2. For multistandard concepts, including NTSC, the following values are recommended; R1 = 47 kΩ, C1 = 100 nF and C2 = 2.2 nF.

Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

1	Ground (digital)
2	Ground (analog)
3	Supply voltage input (analog)
4	Test pin (grounded for normal operation)
5	PLL filter
6	Not connected
7	Test pin (grounded for normal operation)
8	Not connected
9	(R-Y) input
10	(R-Y) output
11	(B-Y) output
12	(B-Y) input
13	Not connected
14	Voltage drain reset generator decoupling
15	Sandcastle input
16	Supply voltage input (digital)

FUNCTIONAL DESCRIPTION

When the (R-Y) and (B-Y) signals have been demodulated in the decoder, the resultant signals are applied to pins 9 and 12. The colour difference signals are then applied via a low-pass filter, preamplifier and clamp circuit to the delay lines. The delayed and direct signals are added in the matrix circuit.

This action occurs for PAL, SECAM and NTSC signals. Consequently, the NTSC colour difference signals are combed.

The frequency generated by the PLL circuit is 454 times the sandcastle frequency. The delay lines are driven by the internal clock drivers at half on the PLL frequency. The outputs from the delay lines are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.

The P^2CCD delay line and matrix requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 14. A circuit for the TDA8451A together with PAL decoder (TDA8391) is illustrated in Fig.2. A circuit for the TDA8451A together with the PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.3. The TDA8490 can also be used in combination with the TDA8391.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_{P(a)}$		13.2	V
Supply voltage (digital)		$V_{P(d)}$		13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ 55 K/W

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3) analog		$V_{P(a)}$	10.8	12.0	13.2	V
Supply current (pin 3) analog		$I_{P(a)}$	5	10	15	mA
Supply voltage (pin 3) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	10	–	dB
Supply voltage (pin 16) digital		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current (pin 16) digital		$I_{P(d)}$	10	22	35	mA
Supply voltage (pin 16) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	25	–	dB
Total power dissipation		P_{tot}	–	0.38	0.66	W
Inputs for demodulated colour difference signals (pins 9 and 12)						
AC coupled and clamped by sandcastle pulse						
Input signal PAL/NTSC mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	1.1	V
Input signal SECAM mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	2.1	V
Input current (outside clamping time)		I_I	–	–	0.1	μA
Input capacitance		C_I	–	10	–	pF
Sandcastle input (pin 15)						
Input resistance		R_{15}	1000	–	–	kΩ
Detection level		V_{15}	6.0	6.8	7.5	V
CD signal output (pins 10 and 11)						
Output signals where input signal is PAL/NTSC at 0.8 V (peak-to-peak value)		$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V
Output signals where input signal is SECAM at 1.6 V (peak-to-peak value)	note 2	$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V

parameter	conditions	symbol	min.	typ.	max.	unit
Output resistance		R_O	300	500	800	Ω
Internal current load of CD outputs		$I_{10;11}$	0.4	–	1.5	mA
DC output level		$V_{10;11}$	4	–	8	V
Rest clock signals (RMS value)	note 3					
at 3.55 MHz		$V_{10\text{-}11(rms)}$	–	–	5	mV
at 7.09 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
at 14.19 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
Signal-to-noise ratio	note 4	S/N	60	65	–	dB
Linearity of output signals (peak-to-peak value)	note 5					
(R-Y); pin 9 to 10 PAL/NTSC	V_I = 0.85 V	α	0.95	–	–	
(R-Y); pin 9 to 10 SECAM	V_I = 1.60 V	α	0.92	–	–	
(B-Y); pin 12 to 11 PAL/NTSC	V_I = 1.10 V	α	0.95	–	–	
(B-Y); pin 12 to 11 SECAM	V_I = 2.10 V	α	0.92	–	–	
Frequency response	at −3 dB	Δf	1.0	1.3	–	MHz
Difference in amplitude between delayed and undelayed signal			–	–	1.5	%
Difference in amplitude of the two output signals for equal input signals			–	–	5	%
Delay time with a 15625 kHz sandcastle pulse		t_d	–	760	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. The SVRR is measured with a 100 Ω resistor in series with a 1 nF capacitor connected between pin 9 and pin 2 and between pin 12 and pin 2.
2. During SECAM the input signal is available during one of two sequential lines. The output signal is thereby halved in comparison with the PAL signal condition.
   To compensate for this the input signal to the TDA8451A during SECAM is twice that during PAL.
3. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) which is connected directly to pin 1 and pin 10 or pin 1 and pin 11.
4. The signal-to-noise ratio (in the PAL mode) is calculated by:

$$\frac{V_{O(p\text{-}p)}}{V_{noise(rms)}\ (0\text{-}1\ MHz)}$$ at an input voltage of 0.8 V(p-p), 0 dB gain

5. The linearity is defined as the amplification of the given input voltage swing divided by the amplification when the input voltage swing is decreased to 70%.

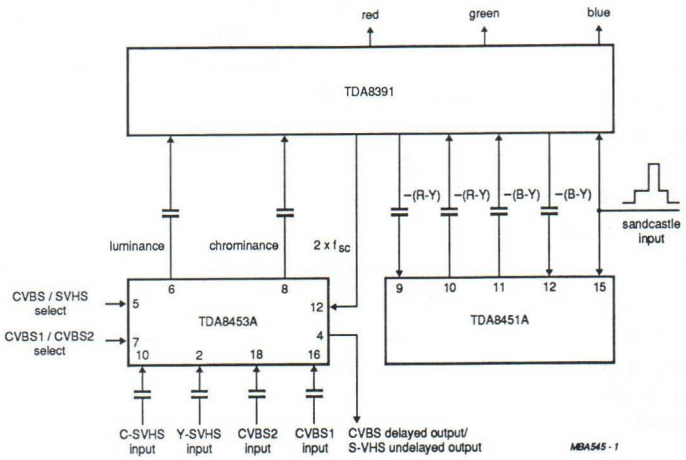


Fig.2 PAL decoder configuration.

DEVELOPMENT DATA

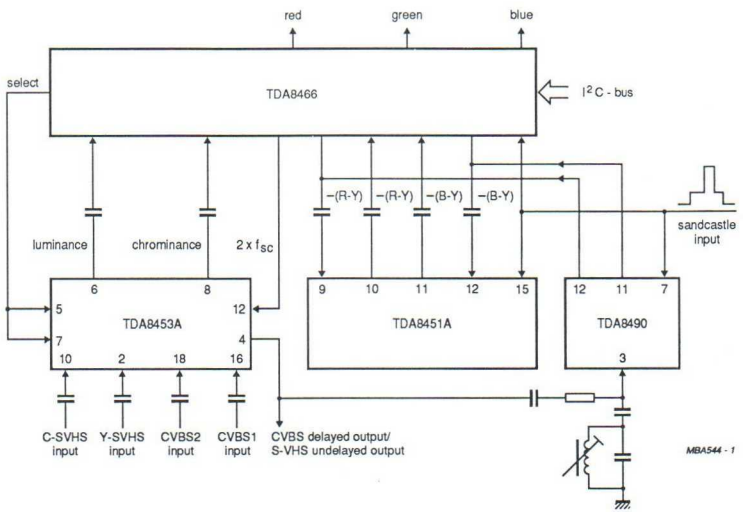


Fig.3 PAL-NTSC-SECAM decoder configuration.

P^2CCD FILTER COMBINATION FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8452A is a monolithic integrated P^2CCD (Profiled Peristaltic Charge Coupled Device) filter combination which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates a video input switch, a luminance delay line with different delay lengths for the 3.58 MHz and the 4.43 MHz TV systems, chrominance trap, a chrominance band-pass filter and clock drivers for the filters which are driven from an internal voltage controlled oscillator (VCO) locked to the 2 x f_{sc} signal. The 2 x f_{sc} signal is obtained from the decoder IC.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 2)		$V_{p(a)}$	10.8	12.0	13.2	V
digital (pin 12)		$V_{p(a)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 2)		$I_{p(a)}$	10	20	28	mA
digital (pin 12)		$I_{p(d)}$	20	45	70	mA
CVBS inputs (pins 14 and 16)						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Luminance output (pin 3)						
output signal (peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns
Bandwidth	at –3 dB	B	3.7	3.8	–	MHz
Chrominance output (pin 5)						
output signal (peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Bandwidth (Fig.3)	at –3 dB	B	–	1.15	–	MHz
CVBS output (pin 4)						
output signal (peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns
Bandwidth (Fig.4)	at –3 dB	B	5.5	6.5	–	MHz
Output resistance		R_O	300	500	800	Ω
Oscillator input signal						
(peak-to-peak value)		$V_{8(p-p)}$	200	–	–	mV

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).

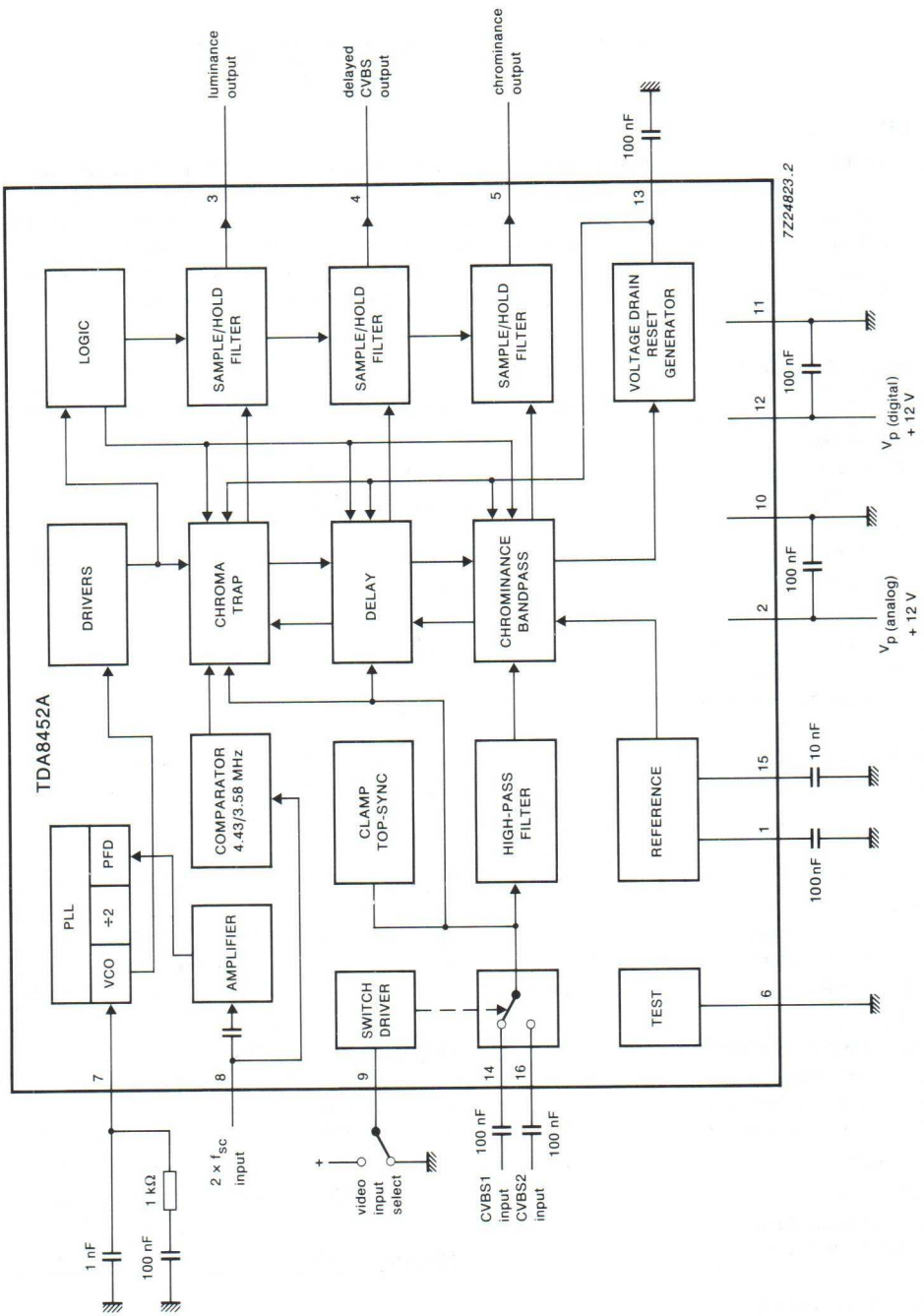


Fig.1 Block diagram.

PINNING

1 Reference decoupling
2 Analog supply voltage input
3 Luminance output
4 Delayed CVBS output
5 Chrominance output
6 Test pin (to be grounded for normal operation)
7 PLL filter
8 2 x f_{sc} input
9 CVBS input select
10 Ground (analog)
11 Ground (digital)
12 Digital supply voltage input
13 Voltage drain reset generator decoupling
14 CVBS1 input
15 Reference decoupling
16 CVBS2 input

FUNCTIONAL DESCRIPTION

The composite video signal (CVBS1 and CVBS2) is applied to pin 14 and/or pin 16. The signal is then routed through three separate paths before being applied to the sample-and-hold filter output stages as follows:

- via a delay line with a delay length of 0.62 μs (for the 4.43 MHz TV system) without filter characteristics. The output signal can be used to drive the sync separation circuit, teletext and SECAM decoders etc.
- via a luminance delay line with chrominance trap with a delay length of 2.09 μs (for the 4.43 MHz TV system). For the 3.58 MHz system the luminance signal will 'skip' part of the delay line so that the total delay of the chrominance signal and the luminance signal are the same (inclusive of the decoder delay and the direct delay of the TDA8451A). The decoder IC, TDA8466, detects whether the subcarrier frequency of the input signal is 3.58 or 4.43 MHz and applies it to the TDA8452A via the DC level of the 2 x f_{sc} reference signal.
- via a chrominance bandpass filter with a delay length of 1.02 μs (for the 4.43 MHz TV system).

The outputs from the delay lines and the bandpass filter are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.
The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, min. 200 mV(p-p)). The VCO operates at 4 x f_{sc} and the delay lines are 4 phase clocked at $4f_{sc}$.
The P^2CCD filter combination requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 13. A circuit for the TDA8452A together with PAL decoder (TDA8391) is illustrated in Fig.5. A circuit for the TDA8452A together with PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.6. The TDA8490 can also be used in combination with the TDA8391. Figures 7 and 8 illustrate the luminance and CVBS channel response on T and 2T pulse.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_p(a)$	–	13.2	V
Supply voltage (digital)		$V_p(d)$	–	13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$		55	K/W

QUALITY SPECIFICATION

Quality level according to URV-4-2-59/601
(except for pins 14 and 15; 700 V; Human body model)

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified (note 1).

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 2) analog		$V_p(a)$	10.8	12.0	13.2	V
Supply current (pin 2) analog		$I_p(a)$	10	20	28	mA
Supply voltage (pin 2) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Supply voltage (pin 12) digital		$V_p(d)$	10.8	12.0	13.2	V
Supply current (pin 12) digital		$I_p(d)$	20	45	70	mA
Supply voltage (pin 12) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Total power dissipation		P_{tot}	–	0.78	–	W
Composite video inputs (pins 14 and 16)						
AC coupled and clamped to top sync						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Input current (non-selected input)		I_I	–	–	0.1	μA
Input current during non-clamping period of selected input		I_I	1.0	3.0	5.0	μA
Input capacitance		C_I	–	5	–	pF
Crosstalk between selected/non-selected channels	R_I = 75 Ω					
at f_{sc} = 1.5 MHz		α	60	65	–	dB
at f_{sc} = 5.0 MHz		α	–	50	–	dB
Video switch control (pin 9)						
Video input (pin 14)		V_9	0	–	1.5	V
Video input (pin 16)		V_9	4	–	V_p	V
Oscillator input signal (pin 8)						
Input signal (peak-to-peak value)	2 x f_{sc}	$V_{8(p-p)}$	200	–	–	mV
Input capacitance		C_I	–	6	–	pF
Input resistance		R_I	–	80	–	kΩ
Input voltage for 3.58 MHz TV system		V_8	6.7	–	V_p	V
4.43 MHz TV system		V_8	0	–	5.3	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance signal output (pin 3)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	0.23	0.32	0.46	V
Output resistance		R_0	300	500	800	Ω
Output level for top sync		V_3	3.0	–	7.0	V
Luminance output internal load		I_3	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{3(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{3(rms)}$	–	–	4	mV
at 17.73 MHz		$V_{3(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity black-to-white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.95	–	–	
Linearity black-to-white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.94	–	–	
Bandwidth	at −3 dB	B	3.7	3.8	–	MHz
Frequency response with regard to 0 MHz (Fig.2)						
at 2.2 MHz		Δf	−1.0	0.5	2.0	dB
at 3.0 MHz		Δf	−0.5	1.0	2.5	dB
at 3.8 MHz		Δf	−4.0	−2.5	−1.0	dB
at 4.26 MHz		Δf	−19	−16	−10	dB
at 4.43 MHz		Δf	–	−25	−20	dB
at 4.64 MHz		Δf	−19	−12	−10	dB
at 5.5 MHz		Δf	−5.0	−2.5	0	dB
T and 2T response (Fig.7) (CVBS input signal = 0.6 V peak-to-peak value)						
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance signal output (pin 5)						
Output signal (chrominance input signal = 0.465 V peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Output resistance		R_0	300	500	800	Ω
DC output level		V_5	3.0	–	7.5	V
Internal load of chrominance output		I_5	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{5(rms)}$	–	–	0.2	mV
at 8.87 MHz		$V_{5(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{5(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity of output signals	note 4					
input = 0.45 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.97	–	
input = 0.65 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.95	–	
Bandwidth (Fig.3)	at –3 dB	B	–	1.15	–	MHz
Frequency response with regard to the top at 4.43 MHz (Fig.3)						
at 0.9 MHz		Δf	–	–22	–17	dB
at 1.9 MHz		Δf	–	–35	–30	dB
at 2.5 MHz		Δf	–	–30	–25	dB
at 3.0 MHz		Δf	–	–20	–16	dB
at 3.8 MHz		Δf	–3.5	–2.5	–1.5	dB
at 4.93 MHz		Δf	–4.0	–3.0	–2.0	dB
at 5.6 MHz		Δf	–	–20	–16	dB
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Delayed signal output (pin 4)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	0.49	0.70	0.98	V
Output resistance		R_0	300	500	800	Ω
Internal load of delayed output		I_4	0.4	–	1.5	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Output sync pulse (input sync pulse = 210 mV peak-to-peak value)		$V_{4(p-p)}$	210	–	–	mV
Output level for top sync		V_4	2.5	–	6.5	V
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{4(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{4(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{4(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	65	70	–	dB
Linearity black to white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.95	–	–	
Linearity black to white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.94	–	–	
Bandwidth (Fig.4)	at −3 dB	B	5.5	6.5	–	MHz
Frequency response with regard to 2.2 MHz (Fig.4)						
at 0.0 MHz		Δf	−2.5	−1.5	−0.5	dB
at 0.9 MHz		Δf	−2	−1	−0	dB
at at 3.1 MHz		Δf	0	1.0	1.5	dB
at 5.5 MHz		Δf	−3	−1	+0.5	dB
T and 2T response is given in Fig.7 (CVBS input signal = 0.6 V peak-to-peak value)						
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V (peak-to-peak value); 100% contrast; 75% saturation.
   In this condition the input signal is formed by the following components:
   210 mV(p-p) sync pulse
   490 mV(p-p) black-to-white
   465 mV(p-p) chrominance
2. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) connected directly to pins 1 and 3, pins 1 and 4 or pins 1 and 5.
3. The signal-to-noise ratio is specified as: nominal $V_{out(p-p)}/V_{noise(rms)}$ (0-5 MHz) at a CVBS input signal specified in note 1.
4. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

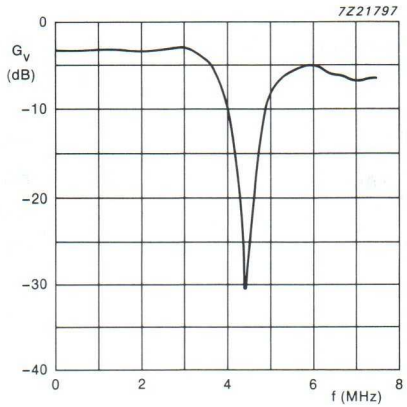


Fig.2 Typical frequency response of luminance signal.

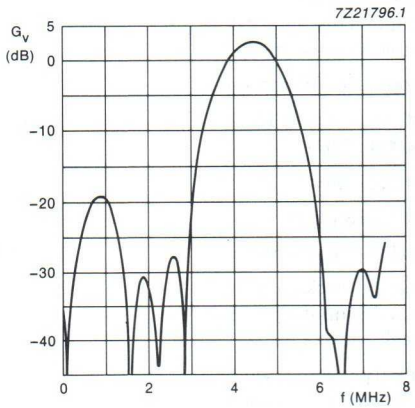


Fig.3 Typical frequency response of chrominance signal.

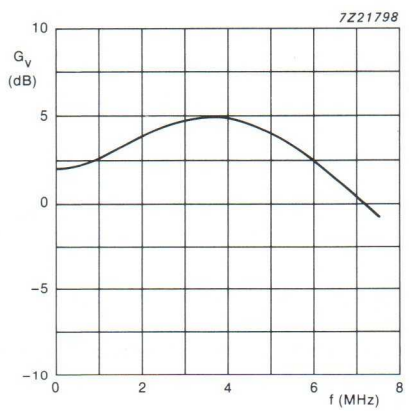


Fig.4 Typical frequency response of delayed signal.

DEVELOPMENT DATA

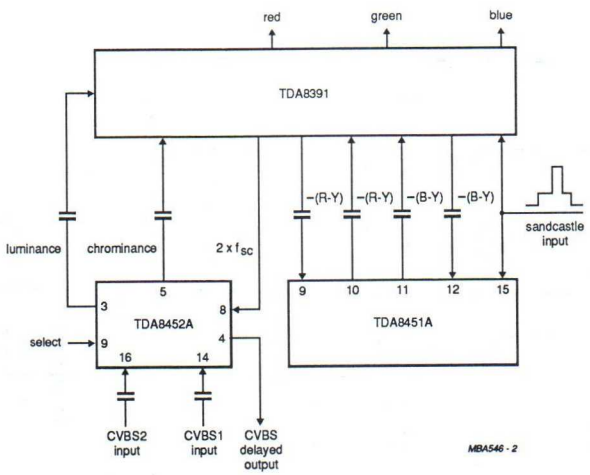


Fig.5 PAL decoder configuration.

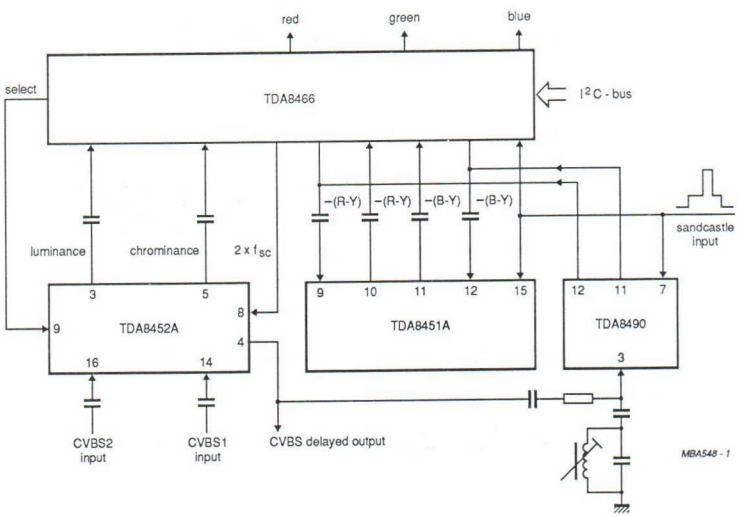


Fig.6 PAL-NTSC-SECAM decoder configuration.

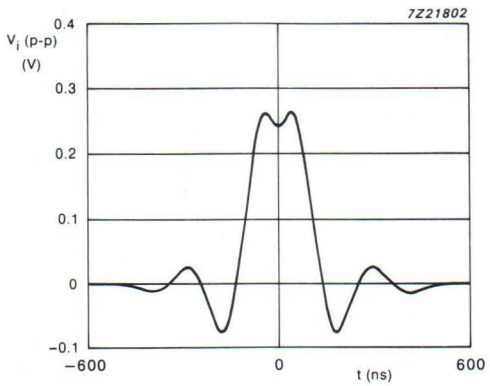


Fig.7(a) Luminance response (T pulse).

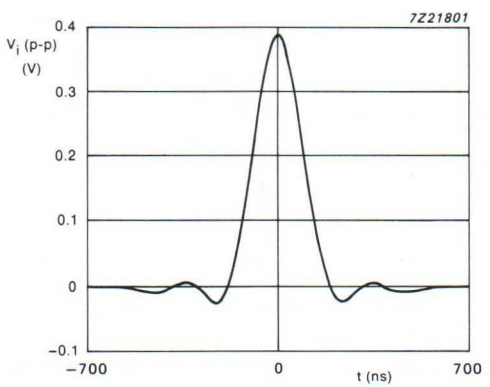


Fig.7(b) Luminance response (2T pulse).

DEVELOPMENT DATA

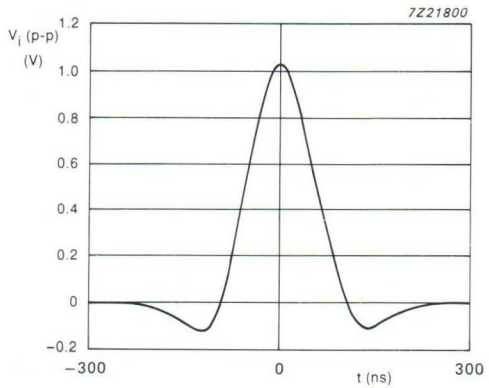


Fig.8(a) CVBS channel response (T pulse).

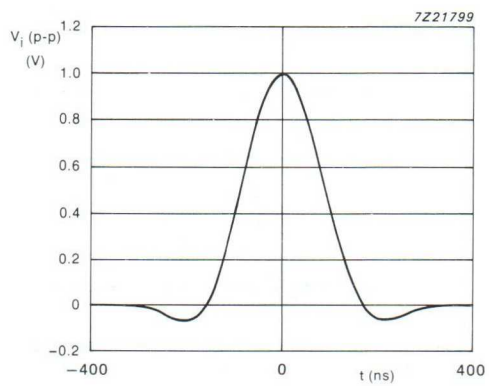


Fig.8(b) CVBS channel response (2T pulse).

P²CCD filter combination for CVBS and S-VHS

TDA8453A

GENERAL DESCRIPTION

The TDA8453A is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which can accommodate CVBS and S-VHS input signals. The device has been designed to be used in conjunction with various colour decoders and incorporates a luminance delay with chrominance trap, a chrominance bandpass filter, a wideband delay line, clock drivers for the filters which are driven from an internal VCO locked to the 2 x f_{sc} signal (obtained from the decoder oscillator), a video switch for three different input signals (2 x CVBS and 1 luminance S-SVHS) and a switch for the chrominance S-VHS. This IC replaces TDA8453.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8453A	18	DIL	plastic	SOT102RG.4

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
$V_{p(a)}$	analog (pin 3)		10.8	12.0	13.2	V
$V_{p(d)}$	digital (pin 13)		10.8	12.0	13.2	V
	supply current					
$I_{p(a)}$	analog (pin 3)		12	22	30	mA
$I_{p(d)}$	digital (pin 13)		20	50	70	mA
$V_{I(p-p)}$	CVBS input (pins 16 and 18) (peak-to-peak value)		–	0.7	1.0	V
$V_{I(p-p)}$	Y-SVHS input (pin 2) (peak-to-peak value)		–	1.0	1.42	V
$V_{I(p-p)}$	C-SVHS input (pin 10) (peak-to-peak value)		–	660	935	mV
$V_{6(p-p)}$	luminance output for CVBS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{6(p-p)}$	luminance output for S-VHS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{8(p-p)}$	chrominance output for CVBS (pin 8) (peak-to-peak value)		425	600	850	mV
$V_{8(p-p)}$	chrominance output for S-VHS (pin 8) (peak-to-peak value)		525	594	660	mV
$V_{4(p-p)}$	delayed CVBS output (pin 4) (peak-to-peak value)		–	1.0	–	V
$V_{4(p-p)}$	delayed S-VHS output (pin 4) (peak-to-peak value)		–	0.9	–	V
R_O	output resistance (pins 4, 6 and 8)		300	500	800	Ω
$V_{12(p-p)}$	oscillator input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV

P²CCD filter combination for CVBS and S-VHS

TDA8453A

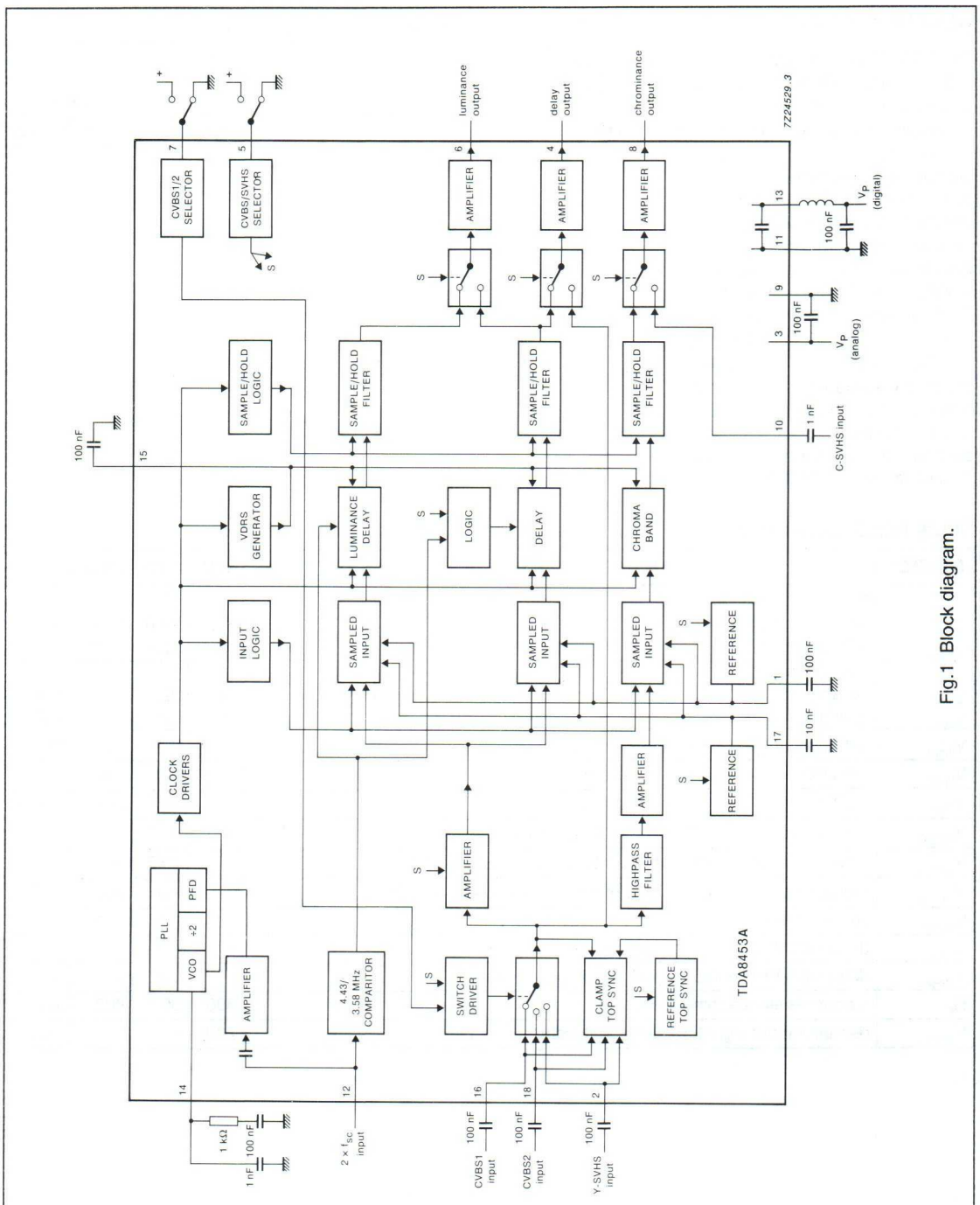


Fig.1 Block diagram.

P²CCD filter combination for CVBS and S-VHS

TDA8453A

FUNCTIONAL DESCRIPTION

The device has four AC-coupled video inputs; CVBS1 (pin 16), CVBS2 (pin 18), luminance S-VHS (Y-SVHS pin 2) and chrominance S-VHS (C-SVHS pin 10).

CVBS1, CVBS2 and S-VHS selectors (pins 5 and 7)

The device can accommodate three different video input signals:

- CVBS1 pins 5 and 7 LOW
- CVBS2 pin 5 LOW, pin 7 HIGH
- S-VHS contains Y-SVHS and C-SVHS; pin 5 HIGH

The slicing level of the CVBS/S-VHS selector and of the CVBS1/CVBS2 selector are different. This means, therefore, that the selectors can be controlled with one signal wire that has three different levels (e.g. by the TDA8466).

CVBS inputs (pins 16 and 18)

When either input is selected by the input switch the signal is routed through three separate paths before being applied to the sample-and-hold filter stages. The paths are via:

- A delay line used to drive the sync separator circuit, teletext and SECAM decoders etc.
- A luminance delay line with chrominance trap
- A chrominance bandpass filter.

The sample-and-hold lowpass filter stages are used to reduce the clock signals. For the 3.58 MHz TV systems the luminance signal will 'skip' part of the delay line to ensure equal delay times in the chrominance and luminance paths.

PINNING

PIN	DESCRIPTION
1	reference decoupling
2	luminance S-VHS input
3	analog supply voltage input
4	delayed CVBS output or undelayed Y-SVHS output
5	CVBS/S-VHS input selector
6	luminance output
7	CVBS1/CVBS2 input selector
8	chrominance output
9	analog ground
10	chrominance S-VHS input
11	digital ground
12	2 x f_{sc} plus 4.43/3.58 MHz selector input
13	digital supply voltage input
14	PLL filter
15	voltage drain reset generator decoupling
16	CVBS1 input
17	reference decoupling
18	CVBS2 input

S-VHS inputs (pins 2 and 10)

If the CVBS/S-VHS selector is in the S-VHS position (pin 5 HIGH), the luminance signal will be routed through two separate paths. The paths are:

- Directly through the input switch to the output switch (pin 4). This signal is used to drive the sync separator circuit
- Via a luminance delay without chrominance trap.

The chrominance S-VHS signal is routed directly to the chrominance output switch (pin 8).
To ensure that the delay of the luminance signal in both the 4.43 MHz and 3.58 MHz TV systems are equal to the total delay of the chrominance S-VHS signal (which is the sum of the delays in the decoder and the delay line IC), the delay line incorporates more stages in the 4.43 MHz TV system than the 3.58 MHz TV system.

Luminance, chrominance and delayed outputs (pins 6, 8 and 4)

The position of the three output switches depends on the selected input (CVBS or S-VHS). The device also incorporates three output amplifiers:

Luminance output (pin 6)

- CVBS luminance delay with chrominance trap
- S-VHS delayed Y-SVHS without chrominance trap

Delay output (pin 4)

- CVBS delayed CVBS signal
- S-VHS undelayed Y-SVHS signal

Chrominance output (pin 8)

- CVBS chrominance bandpass filter with delay
- S-VHS undelayed C-SVHS signal without bandpass filter

Because the amplitude of the CVBS and S-VHS input signals are different, the gain of the input amplifiers and the level of top sync are varied to obtain optimal biasing if S-VHS is selected.

Oscillator (pins 12 and 14)

The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, minimum 200 mV(p-p)). The VCO operates at 4 x f_{sc}, the delay lines and filters are 4 phase clocked at 4 x f_{sc}.
The information whether the incoming signal is 2 x 3.58 MHz or 2 x 4.43 MHz is generated in the decoder IC and fed to the TDA 8453A via the DC level of the 2 x f_{sc} oscillator signal (pin 12). The filter for the PLL is connected to pin 14.

Voltage drain reset generator decoupling (pin 15)

The TDA8453A requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 15 V). This voltage is generated internally with a decoupling capacitor connected to pin 15.

Decoupling reference (pins 1 and 17)

The reference for the sampled inputs of the delay lines and filters are decoupled externally. When S-VHS is selected the reference will vary to give an optimum bias for the sampled input to enable it to adapt to the change in amplification.

A circuit for the TDA8453A together with a PAL decoder (TDA8391) is illustrated in Fig.6. A circuit for the TDA8453A together with a PAL/NTSC decoder (TDA8466) and a SECAM decoder (TDA8490) is illustrated in Fig.7. The TDA8490 can also be used in combination with the TDA8391.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{p(a)}$	analog supply voltage	–	13.2	V
$V_{p(d)}$	digital supply voltage	–	13.2	V
P_{tot}	total power dissipation	–	1.45	W
T_{amb}	operating ambient temperature range	–25	+70	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	–	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (note 1)						
$V_{p(a)}$	analog supply voltage (pin 3)		10.8	12.0	13.2	V
$I_{p(a)}$	analog supply current (pin 3)		12	22	30	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 3)	f = 100 Hz	–	7	–	db
$V_{p(d)}$	supply voltage digital (pin 13)		10.8	12.0	13.2	V
$I_{p(d)}$	supply current digital (pin 13)		20	50	70	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 13)	f = 100 Hz	–	7	–	dB
P_{tot}	total power dissipation		–	0.86	1.3	W
Composite video inputs (pins 16 and 18)						
AC COUPLED AND CLAMPED ON TOP SYNC (NOTE 2)						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	0.7	1.0	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when CVBS1 or CVBS2 is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
Y-SVHS input (pin 2)						
AC COUPLED AND CAMPLED ON TOP SYNC; NOTE 3						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	1.0	1.42	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when Y-SVHS is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
C-SVHS input (pin 10); note 4						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	660	935	mV
R_I	input resistance		4	6	12	kΩ
C_I	input capacitance		–	4	–	pF
α	suppression of any other input signal when C-SVHS is selected (3.8 to 4.9 MHz)	R_i = 75 Ω	–	50	–	dB
CVBS switch control (pin 7)						
V_7	CVBS1 input (pin 16)	pin 5 LOW	0	–	1.5	V
V_7	CVBS2 input (pin 18)	pin 5 LOW	4	–	V_P	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS/S-VHS switch control (pin 5)						
V_5	CVBS1 or CVBS2 input		0	–	6.8	V
V_5	S-VHS input (pins 2 and 10)		8.2	–	V_P	V
PLL reference input signal (pin 12)						
$V_{12(p-p)}$	input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV
C_I	input capacitance		–	6	–	pF
R_I	input resistance		1	–	–	MΩ
V_{12}	DC level for: 4.43 MHz signal 3.58 MHz signal		 0 6.7	 – –	 5.3 V_P	 V V
Luminance signal output (pin 6)						
R_O	output resistance		300	500	800	Ω
V_6	output level for top sync		3	–	7	V
I_6	luminance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio		–	60	–	dB
Luminance signal output for CVBS (pin 5 LOW); note 2						
$V_{6(p-p)}$	output signal (peak-to-peak value)	CVBS input signal = 0.7 V	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white (peak-to peak-value)	note 7 CVBS input signal = 0.7 V CVBS input signal = 1.0 V	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	3.7	3.8	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.2) at 2.2 MHz at 3.0 MHz at 3.8 MHz at 4.26 MHz at 4.43 MHz at 4.64 MHz at 5.5 MHz		 –1.0 –0.5 –4.0 –20 – –18 –5.0	 0.5 1.0 –2.5 –15 –25 –12 –2.0	 2.0 2.5 –1.0 –12 –20 –10 1.0	 dB dB dB dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz reference input		 2060 2270	 2090 2300	 2120 2330	 ns ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance signal output for S-VHS (pin 5 HIGH); note 3						
$V_{6(p-p)}$	output signal	V_2 = 1 V(p-p)	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white	note 7 V_2 = 1 V(p-p) V_2 = 1.42 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.3) at 2.2 MHz at 3.0 MHz at 4.43 MHz at 5.5 MHz		 0 0.5 1.0 –1.0	 1.0 1.5 2.0 0.5	 2.5 3.0 3.5 +2.0	 dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz		 1045 1010	 1075 1040	 1105 1070	 ns ns
Chrominance signal output (pin 8)						
R_0	output resistance		300	500	800	Ω
V_8	DC output level		3.0	–	7.5	V
I_8	chrominance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Chrominance signal output for CVBS						
$V_{8(p-p)}$	output signal (peak-to-peak value)	$V_{16, 18}$ = 0.465 V(p-p)	425	600	850	mV
$V_{8(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 0.2 10 12	 mV mV mV
$L_{8(p-p)}$	linearity of output signals	note 7 $V_{16, 18}$ = 0.465 V(p-p) $V_{16, 18}$ = 0.66 V(p-p)	 – –	 0.97 0.95	 – –	
B	bandwidth	at –3 dB	–	1.15	–	MHz
Δf	frequency response with regard to 4.43 MHz (Fig.4) at 0.9 MHz at 1.9 MHz at 2.5 MHz at 3.0 MHz at 3.8 MHz at 4.93 MHz at 5.6 MHz		 – – – – –3.5 –4.0 –	 –20 –35 –30 –20 –2.5 –3.0 –16	 –15 –30 –25 –16 –1.5 –2.0 –14	 dB dB dB dB dB dB dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Chrominance signal output for CVBS						
t_d	chrominance filter delay at 8.87 MHz reference input at 7.16 MHz reference input		 990 1220	 1020 1250	 1050 1280	 ns ns
Chrominance signal output for S-VHS (pin 5 HIGH); note 4						
$V_{8(p-p)}$	output signal (peak-to-peak value)	V_8 = 0.66 V(p-p)	525	594	660	mV
$V_{8(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 0.2 10 12	 mV mV mV
$L_{8(p-p)}$	linearity of the output signal	note 7 $V_{16, 18}$ = 0.66 V(p-p) $V_{16, 18}$ = 0.935 V(p-p)	 0.97 0.95	 – –	 – –	
B	bandwidth	at –3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 4.43 MHz at 0.9 MHz at 3.0 MHz at 5.6 MHz		 –0.5 –0.5 –1.0	 0 0 0	 +0.5 +0.5 +0.5	 dB dB dB
t_d	chrominance signal delay		–	30	–	ns
Delayed signal output (pin 4)						
R_0	output resistance		300	500	800	Ω
V_4	output level for top sync		2.5	–	7.0	V
I_4	delayed output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Delayed signal output for CVBS						
$V_{4(p-p)}$	output signal (peak-to-peak value)	input signal = 0.7 V CVBS(p-p)	–	1.0	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	0.49	0.70	0.98	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 210 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 4	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{4(p-p)}$	linearity black-to-white	note 7 $V_{16, 18}$ = 0.7 V(p-p) $V_{16, 18}$ = 1 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delayed signal output for CVBS						
Δf	frequency response with regard to 0 MHz (Fig.5)					
	at 0.9 MHz		−0.5	0.5	1.5	dB
	at 2.2 MHz		0	1.0	2.5	dB
	at 3.1 MHz		0	1.5	2.5	dB
	at 5.5 MHz		−3.0	−1.5	0.5	dB
t_d	CVBS signal delay					
	at 8.87 MHzreference input		595	695	655	ns
	at 7.16 MHz reference input		730	760	790	ns
Delayed signal output for S-VHS (pin 5 HIGH); note 3						
$V_{4(p-p)}$	output signal (peak-to-peak value)	V_2 = 1 V(p-p)	–	0.9	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	0.55	0.63	0.70	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 300 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value)	note 4				
	at 4.43 MHz		–	–	1	mV
	at 8.87 MHz		–	–	10	mV
	at 17.73 MHz		–	–	12	mV
$L_{4(p-p)}$	linearity black-to-white	note 7				
		V_2 = 1 V(p-p)	0.95	–	–	
		V_2 = 1.42 V(p-p)	0.94	–	–	
B	bandwidth	at −3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 0 MHz					
	at 2.2 MHz		−0.5	0	0.5	dB
	at 5.5 MHz		−1.0	0	0.5	dB
t_d	Y-SVHS signal delay		–	40	–	ns

Notes to the characteristics

1. To prevent linearities and rest clock signals from deteriorating, it is recommended that the difference between the supply voltages at pins 3 and 13 should be less than 500 mV.
2. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V(p-p); 100% contrast; 75% saturation.

   In this condition the input signal is formed by the following components:

   210 mV(p-p) sync pulse

   490 mV(p-p) black-to-white

   465 mV(p-p) chrominance
3. The figures are related to a Y-SVHS input signal of 1 V(p-p), 100% contrast. In this condition the input signal is formed by the following components:

   300 mV(p-p) sync pulse

   700 mV(p-p) luminance

Notes to the characteristics

4. The figures are related to a C-SVHS input signal of 660 mV(p-p). This amplitude corresponds to a video signal of 1 V(p-p). 100% contrast and 75% saturation.
5. The signal-to-noise ratio is specified as nominal $V_{out(p-p)}/V_{noise(rms)}$ (0 to 5 MHz).
6. The rest clock signals are measured with an FET probe (3.5 pF in parallel with a 1 MΩ resistor) connected directly to pins 4 and 9, pins 6 and 9 or pins 8 and 9.
7. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

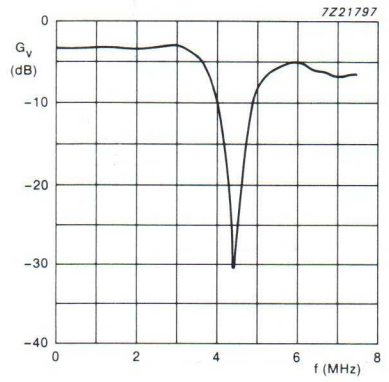


Fig.2 Typical frequency response of luminance signal (CVBS).

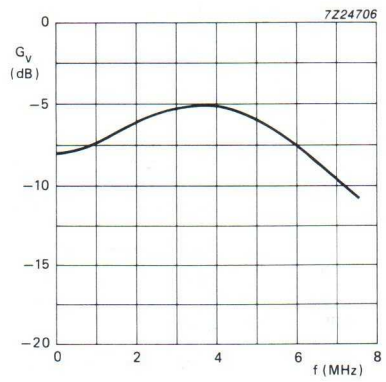


Fig.3 Typical frequency response of luminance signal (S-VHS).

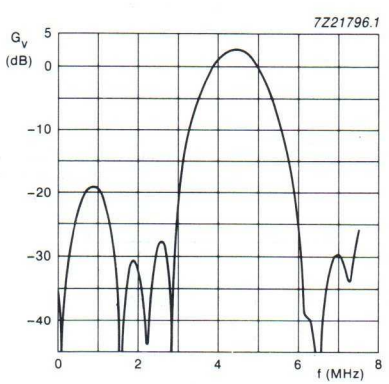


Fig.4 Typical frequency response of chrominance signal (CVBS).

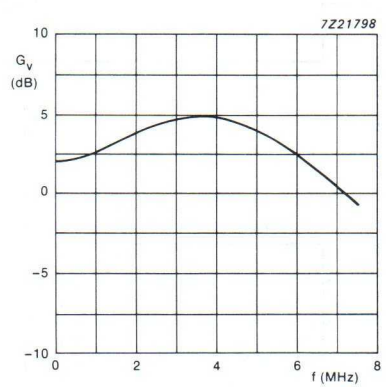


Fig.5 Typical frequency response of delayed signal (CVBS).

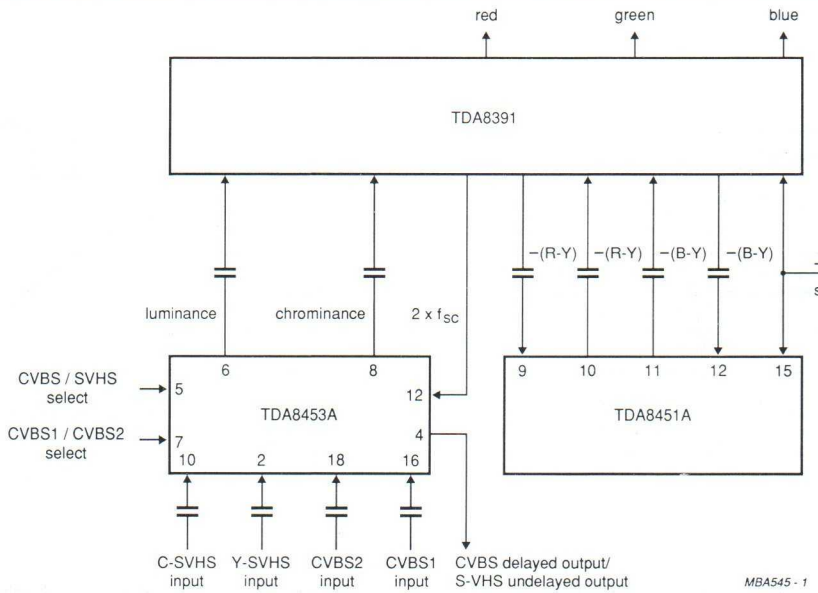


Fig.6 PAL decoder configuration.

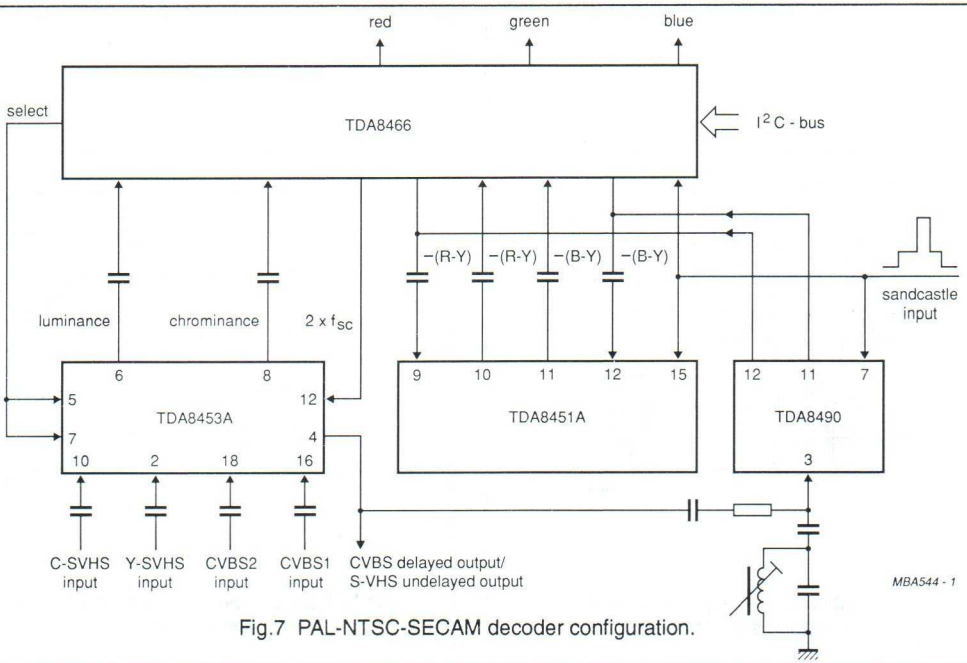


Fig.7 PAL-NTSC-SECAM decoder configuration.

RGB gamma-correction processor TDA8480T

FEATURES

- Alignment free
- Low power
- High performance brightness control.

GENERAL DESCRIPTION

The TDA8480T is an I²C-bus controlled, RGB gamma-correction processor. The device can be used as a brightness control for LCDs, with crossed polarity filters, and for CRT applications. The variable gamma function offers an adjustable non-linear amplification of the RGB input signals which results in more expansion near black and more compression near white. The equivalent gamma value can be varied between 1 (the path from input to output is transparent) and 0.25. Separate inputs are available for video and data (TXT) which can be selected via a fast acting switch.

The RGB video and data inputs are AC-coupled externally. Black restoration is achieved during the clamping interval which is defined at pin 18. For the video channel the black level during scan can be adjusted to within 10%. This is activated by setting the Msys bit in the status/control register via the I²C-bus. Adjustment is realized by external hardwiring, thus defining a voltage at pin 9 . This option is required for some NTSC M-system transmitters.

The TDA8480T also contains a bandgap voltage generator and a power-down detector. If a power-down is detected, the POR-bit in the status/control register will be set which can be read by the I²C-bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage	4.75	5.0	5.25	V
I_{CC}	supply current	–	10	–	mA
$V_{IRGB(p-p)}$	RGB amplifier input voltage, positive swing (peak-to-peak value)	–	0.7	1.0	V
$V_{IDAT(p-p)}$	DATA amplifier input voltage, positive swing (peak-to-peak value)	–	0.7	1.0	V
$V_{ORGB(p-p)}$	RGB amplifier output voltage, positive swing (peak-to-peak value)	–	0.7	1.0	V
$V_{ODAT(p-p)}$	DATA amplifier output voltage, positive swing (peak-to-peak value)	–	0.7	1.0	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8480T	20	SO	plastic	SOT163A

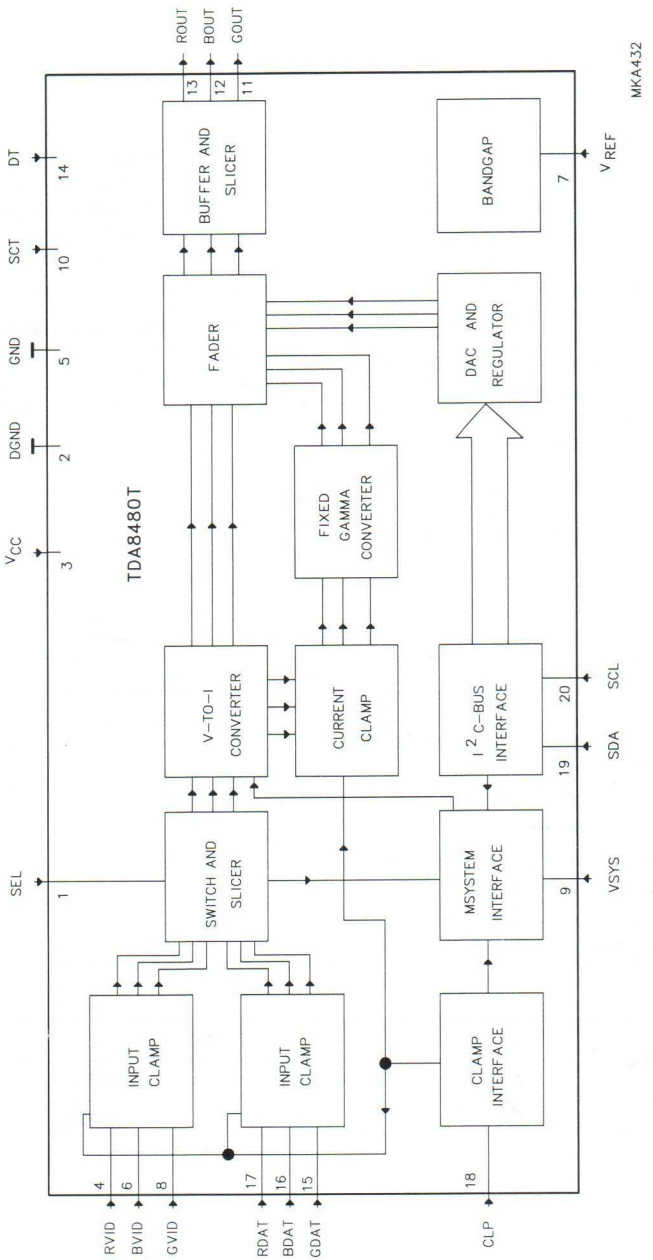


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SEL	1	select input
DGND	2	digital ground
V_{CC}	3	positive supply voltage
RVID	4	red video input
GND	5	ground
BVID	6	blue video input
V_{REF}	7	voltage reference output
GVID	8	green video input
VSYS	9	video system interface input
SCT	10	test purposes only
GOUT	11	green output
BOUT	12	blue output
ROUT	13	red output
DT	14	test purposes only
GDAT	15	green data output
BDAT	16	blue data output
RDAT	17	red data output
CLP	18	clamp input
SDA	19	serial data input/output
SCL	20	serial clock input

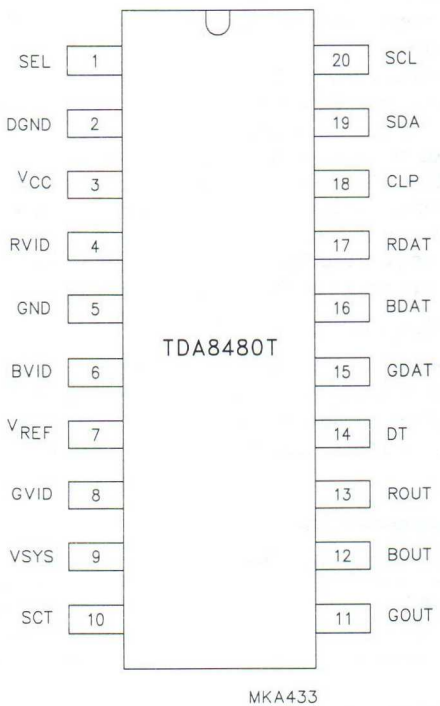


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic function of the TDA8480T is to provide variable gamma correction. Each channel (R,G and B) is separated into a linear and a gamma converted path each with a fixed gamma value. A fader combines the outputs of the two paths with different weights (depending on the binary word) which are stored in the DAC that controls the fader.
The gamma function is defined as $y = x \,\hat{}\, \gamma$, with 'x' the input excitation normalized with respect to 0.7 V. As the theoretical infinite gain for $x = 0$ has a large impact on the system parameters, the inverse sinusoidal hyperbolic function (see also Figure 5) which is close to the ideal gamma function, as given in equation 1, is adopted:

$$\sinh^{-1}(g,x) = \ln \{gx + [(gx)^2+1]^{0.5} \} \quad (1)$$

The major advantage of the $\sinh^{-1}$ function is the limited gain for $x = 0$ (see also Figure 4). The value g can be fitted to an equivalent γ, within close approximation. When $\gamma = 0.25$ the parameter $g = 27.32$ can be found.

Both the adoption of the $\sinh^{-1}$ function and the fader action ensures that the converted output signals do not obey the ideal gamma conversion. However, it can be shown that the resulting error is negligible with respect to the colour reproduction if saturation correction is applied.

Three 6-bit DACs, controlled by the I²C-bus, set the output gamma values of the RGB channels. User control of the DACs for controlling the brightness (and in the event of LC panels the viewing angle) and the manufacturing control, (required when the gamma values of the display are not equal) must be supported by software programming. The DACs control the fader setting a_i where $0 <= a_i <= 1$ and $i = R, G$ or B. Depending on the fader setting a_i the output y_i can be written as per equation 2:

$$y_i = a_i \times X + (1-a_i) \times \sinh^{-1}(g,x)/\sinh^{-1}(g,1) \quad (2)$$

The relationship between a_i and the effective gamma (when $g = 27.32$) is shown in Figure 5.

I²C-bus conventions

Table 1 I²C-bus conventions.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	1	0	X

Valid sub-address = 00 to 03

Table 2 Auto-increment mode available for sub-address.

REGISTER	ADDRESS	MSB							LSB
Status	--	X	X	X	X	X	X	X	POR
Control	00	X	X	X	X	X	X	X	MSYS
Gamma control RED	01	X	X	R5	R4	R3	R2	R1	R0
Gamma control BLUE	02	X	X	B5	B4	B3	B2	B1	B0
Gamma control GREEN	03	X	X	G5	G4	G3	G2	G1	G0

Where X = don't care

Table 3 Gamma control word.

CONTROL WORD	ADDRESS								REMARKS
Maximum DAC setting	X	X	1	1	1	1	1	1	or linear mode (a_i = 1)
Minimum DAC setting	X	X	0	0	0	0	0	0	or maximum non-linearity (a_i = 0)

Where X = don't care

Table 4 NTSC Msystem black-level control.

MSYS	REMARKS
0	not activated
1	activated

Table 5 Power status convention.

POR	REMARKS
1	power-down or power dip detected
0	normal power mode

FAST SWITCHING CONVENTION

Table 6 Input selection.

SEL	REMARKS
0	VIDEO selected
1	DATA selected

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage	–	5.5	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−25	+80	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	75 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; C_L = 15 pF (pins 11 to 13); all ratios (%, dB) referenced to 700 mV; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current		–	10	15	mA
V_{REF}	reference voltage (pin 7)		1.22	1.25	1.28	V
Z_O	output impedance (pin 7)		–	–	250	Ω
Video and data inputs						
V_{clamp}	voltage level during clamping		–	2.5	–	V
$V_{I(p-p)}$	input voltage swing positive to black (peak-to-peak value)		–	0.7	1.0	V
V_{blk}	negative voltage swing with respect to black		–	–	–0.3	V
Z_{scan}	input impedance during scan		100	–	–	kΩ
Z_{clamp}	input impedance during clamping		–	600	–	Ω
I_I	input current		–	–	150	nA
RGB outputs						
$V_{O(p-p)}$	output voltage swing (peak-to-peak value)	a_i = 1	–	0.72	–	V
V_{Oblk}	black output voltage level		–	0.8	–	V
V_{blk}	negative voltage swing with respect to black	note 1; a_i = 0	–	–	–100	mV
Z_O	output impedance		–	–	250	Ω
B	bandwidth	note 2; a_i = 0	6	9	–	MHz
S/N	signal-to-noise ratio at full bandwidth	note 3; a_i = 0	52	–	–	dB
t_d	delay from input to output	note 4; a_i = 0	–	25	100	ns
$MSYS_{mis}$	mismatch Msystems offsets	a_i = 1	–	–	7.0	mV
α	crosstalk between RGB outputs	note 5; a_i = 1	–	–40	–	dB
Clamping (pin 18)						
V_{18}	detection level of clamping voltage		1.5	–	3.2	V
t_{clamp}	clamping period		2	–	–	µs
Z_I	input impedance		100	–	–	kΩ
SR	clamping input slew rate		24	–	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Select (pin 1)						
V_1	video voltage detection level		1.8	–	3.0	V
α	crosstalk from unselected input to equivalent output	note 5; $a_i = 0$	–	–	–46	dB
α	crosstalk from SEL edges to output	note 6; $a_i = 0$	–	–	70	mV
Δt	difference between transit time of signal and video switching	note 7; $a_i = 1$	–	25	–	ns
Z_i	input impedance		100	–	–	kΩ
MM_{blk}	mixed mode black-level offset	$a_i = 0$	–	0	–	%
Msystem input (pin 9)						
φ	black-level offset sensitivity	note 8	7	9	11	%/V
V_i	input voltage range		–	–	1.5	V
Z_i	input impedance	Msys = 1; SEL = 0	100	–	–	kΩ
I_{bias}	input bias current	Msys = 1; SEL = 0	–	–	300	nA
DAC accuracy						
IL	integral linearity		–	–	2	LSB
	matching accuracy between DAC control factors		–	–	0.5	LSB
Colour reproduction (note 9)						
	intersection accuracy at black or 0% FS	note 10	–	–	4	%
	intersection accuracy at white or FS	note 10	–	–	4	%
	amplitude tolerance at white or FS	note 11; $a_i = 1$	–	–	4	%
	absolute fader setting error		–	–	4	%
	transfer tolerance for each channel	note 12; $a_i = 0.6$	–	–	7	%
	matching tolerance between any channel for equal a_i	$0 < a_i < 1$; $V_i < 5\%$ FS	–	–	1+20 V_i/FS	%
		$0 < a_i < 1$; 5% FS $< V_i <$ FS	–	–	2	%

Notes to the characteristics

1. Input drive −0.3 V.
2. Measured at 10%, 50% and 90% of the nominal RGB input drive.
3. Measured at black.
4. Measured at 50% of a squarewave input signal of 0.7 V with rise and fall times of 20 ns and at 80% of the output signal.
5. Measured with a sinewave of 0.7 V (p-p) at a frequency of 5 MHz.
6. Rise time 20 ns.
7. Measured with rise time of 20 ns at 50% of input and output excursions. Video inputs at black, data inputs at nominal white.
8. Measuring black-level offset value with respect to nominal white.
9. All percentages given are relative to full scale (FS) and are derived from measuring the output voltages relative to the voltage level during clamping. FS differs for input related voltages (0.7 V) and output related voltages (0.72 V)
10. Fader position a_i running from minimum to maximum.
11. Absolute accuracy.
12. The transfer from input to output should match the theoretical faded inverse sinusoidal hyperbolic as formulated in relation (2) with the g-factor set to 29.3.

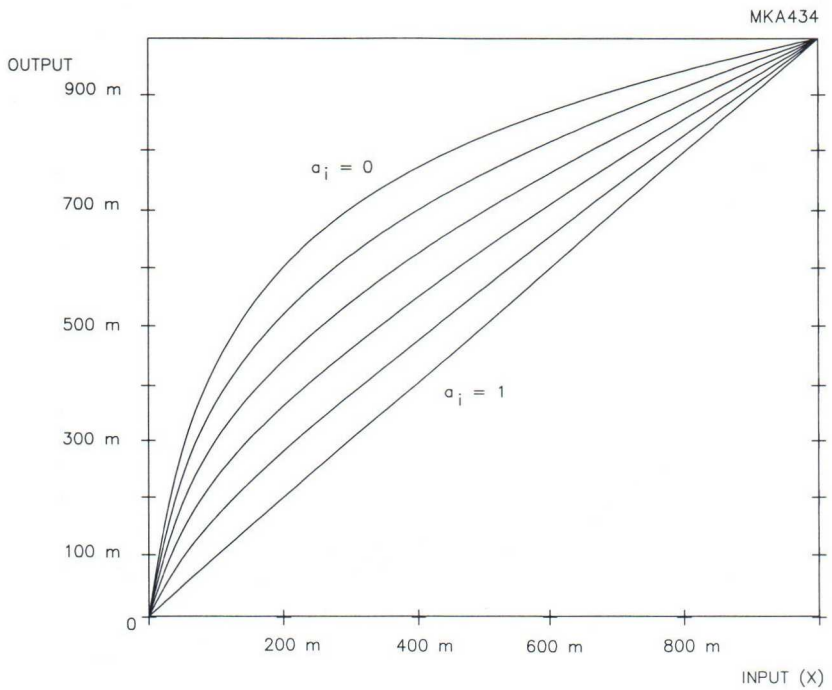


Fig.3 Output curves for the inverse sinusoidal hyperbolic converter (g = 29.3 and the fader position a_i runs from 0 to 1 in 0.2 step sizes).

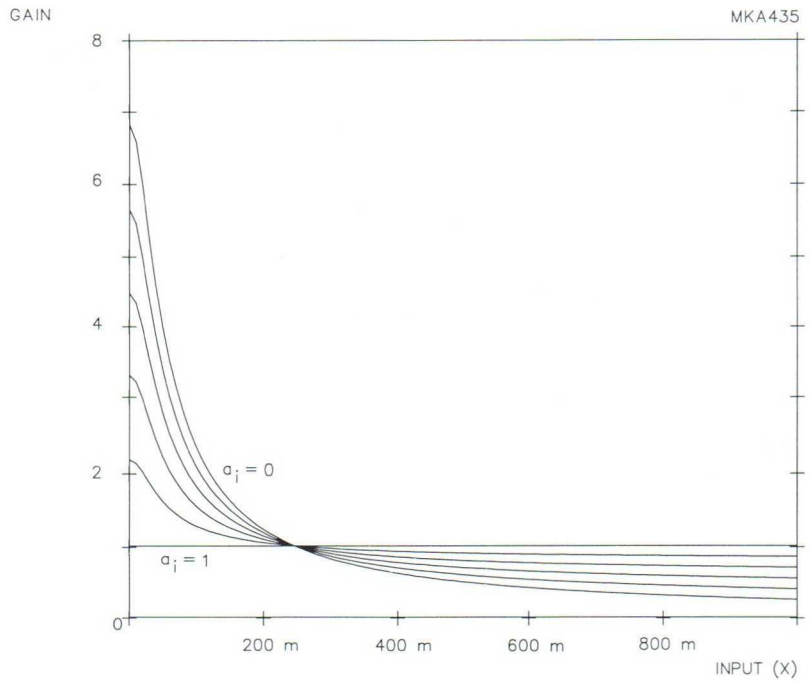


Fig.4 Local gain for the inverse sinusoidal hyperbolic converter (g = 29.3; the fader position a_i runs from 0 to 1 in 0.2 step sizes).

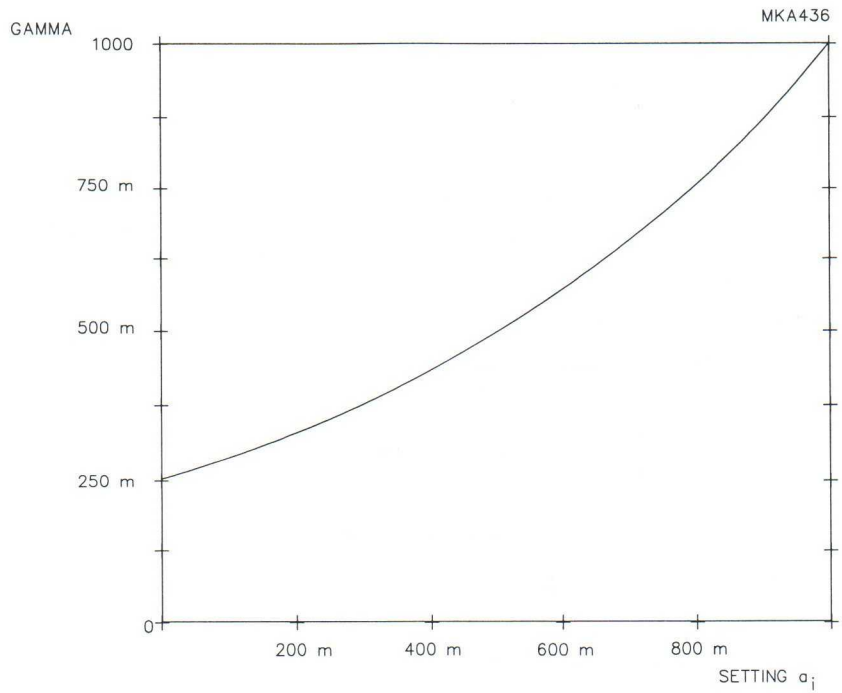


Fig.5 Relationship between the equivalent gamma value and the setting of the fader (g = 29.3).

APPLICATION INFORMATION

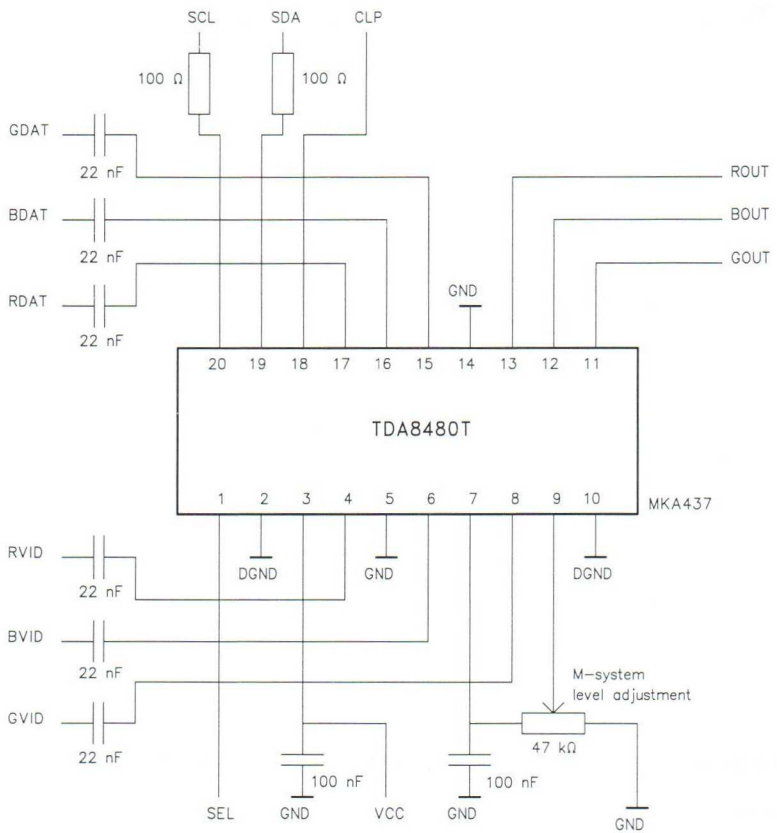


Fig.6 Application diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SECAM DECODER

GENERAL DESCRIPTION

The TDA8490 is a monolithic integrated SECAM decoder. This circuit is intended to be used in conjunction with TDA8390 or TDA8461 (PAL decoder), TDA8451 (delay) and TDA8452 (filter). In this application the TDA8490 is placed in parallel with the demodulation circuit of the PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply current		$I_P = I_9$	40	55	70	mA
Chrominance amplifier and demodulator						
Input signal (peak-to-peak value)	SECAM with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
Identification						
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Sandcastle detector and clamp pulse generator						
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heat spreader (SOT102).

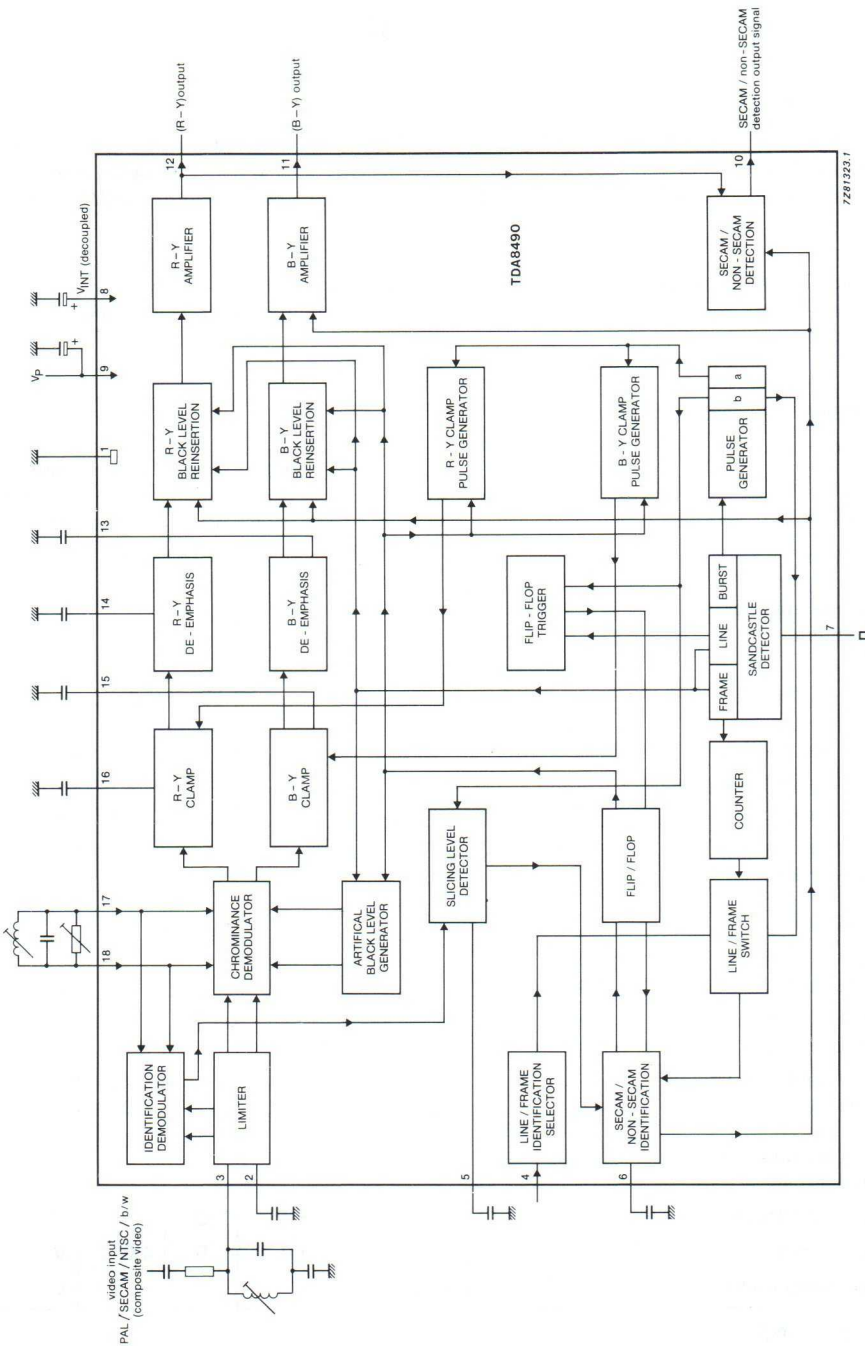


Fig. 1 Block diagram.

PINNING

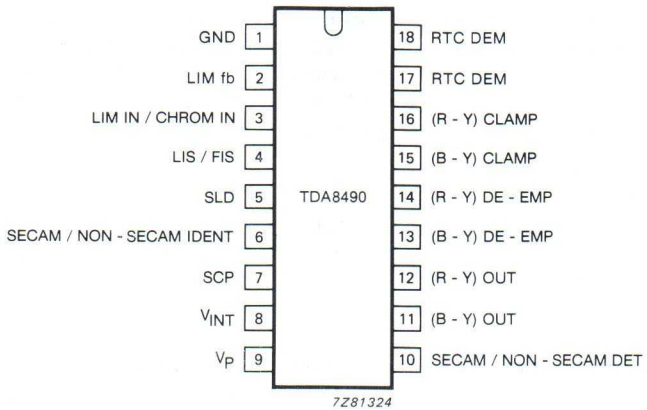


Fig. 2 Pinning diagram.

1	GND	ground	9	V_P	supply voltage
2	LIM fb	limiter feedback	10	SECAM/NON-SECAM DET	SECAM/non-SECAM detection circuit
3	LIM IN/ CHROM IN	limiter input/ chrominance input	11	(B-Y)OUT	(B-Y) signal output
4	LIS/FIS	line identification selector/ frame identification selector	12	(R-Y)OUT	(R-Y) signal output
			13	(B-Y)DE-EMP	(B-Y) de-emphasis circuit
5	SLD	slicing level detector	14	(R-Y)DE-EMP	(R-Y) de-emphasis circuit
6	SECAM/NON-SECAM IDENT	SECAM/non-SECAM identification circuit	15	(B-Y)CLAMP	(B-Y) clamping circuit
			16	(R-Y)CLAMP	(R-Y) clamping circuit
7	SCP	sandcastle pulse input	17	RTC DEM	reference tuned circuit demodulator
8	V_{INT}	internal supply voltage (decoupled)	18	RTC DEM	reference tuned circuit demodulator

FUNCTIONAL DESCRIPTION

Demodulation

The TDA8490 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 3 (applied via a bandpass filter with a bell-shaped response) is SECAM or non-SECAM (NTSC, PAL or black-and-white).

When the SECAM signal is detected, it is applied to a limiter/amplifier after which it is demodulated. The (R-Y) and (B-Y) signals are applied sequentially, therefore, only one demodulator is required. After demodulation the signals are applied to the (R-Y) and (B-Y) clamp circuits, where the black levels are clamped to the same DC level.

Artificial black levels are inserted during line blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signal (necessary in case there are no line burst signals available). The inserted signals may not be identical to the detected black levels, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

R-Y and B-Y output signals

The R-Y and B-Y signals are available every other line. A new black level is reinserted during blanking and timing b (Fig. 5). If a non-SECAM signal is present the R-Y output will generate a DC level of approximately 3,8 V (the same as the black level generated during normal SECAM condition on both outputs). The B-Y output generates a DC level of approximately 0,8 V in this condition.

SECAM or non-SECAM signals may also be identified by the information at pin 10:

- 2,6 V indicates a SECAM signal.
- 0 V indicates a non-SECAM signal.

The SECAM or non-SECAM signals can be identified by using the (B-Y) demodulator output level at pin 11. Depending on the PAL decoder used in conjunction with this device, the information can be passed to the microcomputer via the I^2C bus.

Priority identification

The two chrominance outputs of TDA8490 are connected to the chrominance outputs of the PAL decoder TDA8461 or TDA8390. The output signal of the TDA8490 and PAL decoder alternately determine the priority of the overall system. In the event of a clash on these outputs, caused by a reflected PAL signal being detected as a SECAM signal by TDA8490, the total system will default to PAL priority.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For line identification this comparison occurs during the internally generated pulse 'B' (Fig. 3). Only SECAM signals provide voltage difference from line to line during comparison. If the phase relationship between both the signals is incorrect, the flip-flop will receive an extra input pulse.

The identification (as above) occurs when the line identification system is active. When the frame identification system is switched on (pin 4), the system only compares the demodulator output voltage during a 4-line gate pulse, which is present during frame blanking. The 4-line gate pulse starts 10 burst gate pulses after the start of the vertical blanking part of the sandcastle signal. The operation is identical to the line identification. Timing of the 4-line gate pulse is shown in Fig. 4.

Sandcastle detector

The sandcastle pulse detector requires a 3-level sandcastle pulse. It detects the various blanking and gating pulses and generates the correct drive pulses for the clamping circuits (Fig. 3).

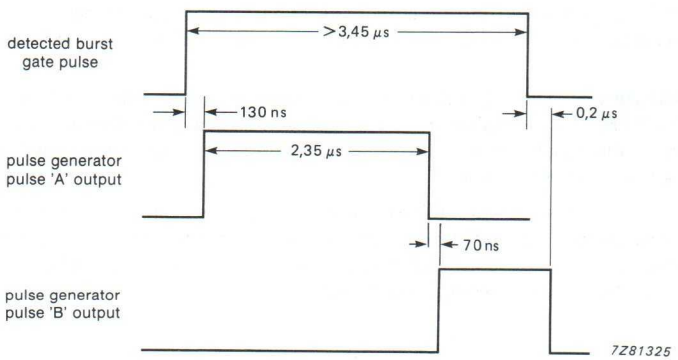


Fig. 3 Burst and derived pulses.

Note

The separated burst pulse is divided into two parts (Fig. 3). Required burst gate pulse: $> 3{,}45\ \mu s$.

Pulse 'A':

- timing R-Y clamp (only present during a red line)
- timing B-Y clamp (only present during a blue line)

Pulse 'B':

- SECAM line identification timing

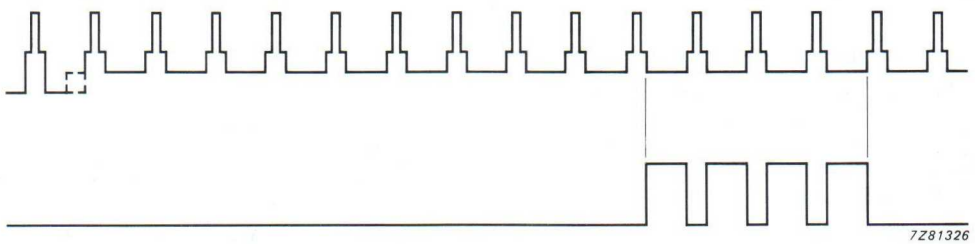


Fig. 4 above: Sandcastle signal during frame period (even and odd).

below: 4-line gate pulse.

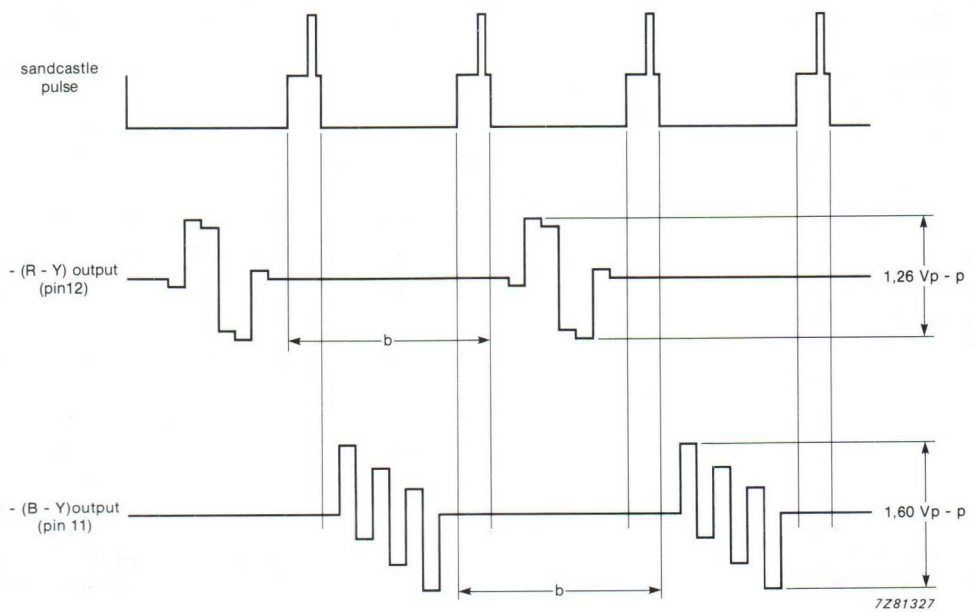


Fig. 5 $-$(R-Y) and $-$(B-Y) output signals compared to the sandcastle input signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 9	V_P	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	–25	+ 150	°C
Operating ambient temperature range		T_{amb}	–25	+ 65	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply voltage	decoupled, pin 8	$V_{INT} = V_{8-1}$	10,6	11,8	13,0	V
Supply current		$I_P = I_9$	40	55	70	mA
Total power dissipation		P_{tot}	–	660	840	mW
Thermal resistance from junction to ambient		$R_{th\ j\text{-}a}$	–	50	–	K/W
External capacitance	pin 8	$C_o = C_{8-1}$	–	–	4,7	μF
Chrominance amplifier and demodulator	note 1					
Input signal (peak-to-peak value)	non-SECAM signal	$V_{3-1(p-p)}$	–	–	1,1	V
Input signal (peak-to-peak value)	SECAM signal with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
Input resistance	pin 3	R_{3-1}	9,5	11,8	14,1	kΩ
Input capacitance	pin 3	C_{3-1}	–	–	5	pF
Input resistance	between pins 17 and 18	R_{17-18}	2,9	3,6	4,3	kΩ
Input capacitance	between pins 17 and 18	C_{17-18}	–	12	–	pF
De-emphasis output resistance	pins 13 and 14	R_{13-1} R_{14-1}	1,45	1,75	2,05	kΩ
Zero point stability of chrominance demodulator	note 2 pins 11 and 12	$f_{11, 12}$	–	5	–	kHz
(B-Y)/(R-Y) gain ratio	note 7		1,38	1,55	1,73	

parameter	conditions	symbol	min.	typ.	max.	unit
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12\text{-}1(p\text{-}p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11\text{-}1(p\text{-}p)}$	1,28	1,60	1,92	V
B-Y output signal level	SECAM		3,5	3,8	4,1	V
B-Y output signal level	non-SECAM		–	0,8	1,1	V
R-Y output signal level			3,5	3,8	4,1	V
R-Y signal linearity	note 3		88	95	102	%
B-Y signal linearity	note 4		85	92	99	%
Inserted black levels (demodulated)	function of temperature, note 6		–	0,22	–	kHz/K
Output impedance	pin 12	$\lvert Z_{12\text{-}1}\rvert$	–	30	–	Ω
Output impedance	pin 11	$\lvert Z_{11\text{-}1}\rvert$	–	30	–	Ω
Identification	SECAM, non-SECAM					
Input voltage for line identification	pin 4	$V_{4\text{-}1}$	4,1	–	13,2	V
Input voltage for frame identification	pin 4	$V_{4\text{-}1}$	0	–	2,9	V
Switching level for line/frame identification	pin 4	$V_{4\text{-}1}$	3,0	3,5	4,0	V
Input current	pin 4	I_4	–	–5	–25	μA
Voltage at pin 6	during non-SECAM	$V_{6\text{-}1}$	–	10,2	–	V
Voltage at pin 6	during SECAM	$V_{6\text{-}1}$	–	7,7	–	V
Identification level at pin 6		$V_{6\text{-}1}$	10,5	10,8	11,0	V
Internal colour 'OFF' (pin 6)	SECAM to non-SECAM	$V_{6\text{-}1}$	9,7	10,0	10,3	V
Internal colour 'ON' (pin 6)	non-SECAM to SECAM	$V_{6\text{-}1}$	8,9	9,2	9,5	V
Colour 'ON' to colour 'OFF' hysteresis	non-SECAM to SECAM	$V_{6\text{-}1}$	0,5	0,8	1,0	V
Voltage at pin 10	during non-SECAM	$V_{10\text{-}1}$	–	1,6	0,5	V
Voltage at pin 10	during SECAM	$V_{10\text{-}1}$	2,1	2,6	3,1	V
Output impedance at pin 10	during SECAM	$\lvert Z_{10\text{-}1}\rvert$	1,35	1,60	1,85	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle detector and clamp pulse generator	pin 7					
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V
Input current	V_{7-1} = 0,7 V	I_7	–	–30	–100	μA
Pulse width	see Fig. 3 pulse A		1,85	2,35	2,85	μs
Required pulse width	note 5, see Fig. 3 pulse B		0,6	–	–	μs

Notes to the characteristics

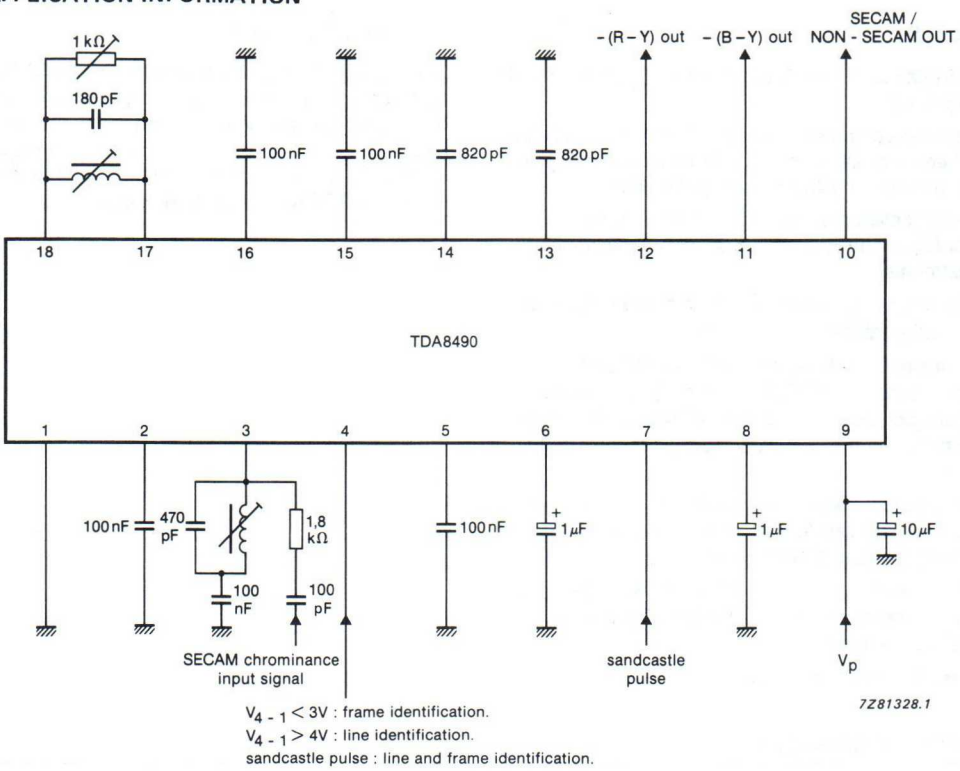
1. For alignment of the reference tuned circuit the input signal on pin 3 must be a SECAM signal at 100 mV(p-p) without deviation during a red and a blue line (black colour information, SECAM). The reference tuned circuit must be aligned to generate a colour output which corresponds to the new reinserted black level information.
2. If the input signal of the limiter is changed from 300 mV(p-p) to 15 mV(p-p), the zero point of the chrominance FM demodulator (f_o is typically 4,33 MHz) will typically shift by 5 kHz.
3. Definition of R-Y linearity = $V_{out\ cyan}/V_{out\ red}$:
   - $f_{nom\ cyan}$ = 4,68 MHz
   - $f_{nom\ red}$ = 4,12 MHz
4. Definition of B-Y linearity = $V_{out\ yellow}/V_{out\ blue}$:
   - $f_{nom\ yellow}$ = 4,02 MHz
   - $f_{nom\ blue}$ = 4,48 MHz
5. The burst gate pulse width must be larger than (2,85 + 0,6)=3,45 μs.
6. Demodulated black level at temperature X = A and at temperature Y = B.
   Artifical black level at temperature X = C and at temperature Y = D.
   Demodulated output signal ($f_o - \Delta f$) at temperature X = E1 and at temperature Y = F1.
   Demodulated output signal ($f_o + \Delta f$) at temperature X = E2 and at temperature Y = F2.

   $$E = \frac{E1 - E2}{2} \text{ and } F = \frac{F1 - F2}{2}$$

   $$\text{specification result} = \frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y\text{-}X} \times \Delta f\ (kHz)/^{o}C)$$

   for B-Y $f_o = f_{ob}$ = 4,25 MHz and Δf = 230 kHz.
   for R-Y $f_o = f_{or}$ = 4,40625 MHz and Δf = 280 kHz.
7. Due to different deviations (230 or 280 kHz) and correction figures (1,9 or 1,5 x) the total B-Y signal path needs a gain, which is 1,55 x higher than the R-Y path.

APPLICATION INFORMATION



$V_{4-1} < 3V$: frame identification.
$V_{4-1} > 4V$: line identification.
sandcastle pulse : line and frame identification.

Fig. 6 Application diagram.

PAL/NTSC encoder TDA8501

FEATURES

- Two input stages: R, G, B and –(R–Y), –(B–Y), Y with multiplexing
- Chrominance processing, highly integrated, includes low frequency filters for the colour difference signals, and after the modulator a bandpass filter
- Fully controlled modulator produces a signal according to the PAL or NTSC standard without adjustments
- A free running oscillator. Can be tuned by crystal or by an external frequency source
- Output stages with separated Y + SYNC and chrominance (Y + C, SVHS), and a CVBS output. Signal amplitudes are correct for 75 Ω driving via an external emitter follower. Internal generation of NTSC setup
- Sync separator circuit and pulse shaper, to generate the required pulses for the processing, clamping, blanking, FH/2, and burst pulse
- H/2 control pin. In PAL mode the internally generated H/2 is connected to this pin and the phase of this signal can be reset
- Internal bandgap reference.

GENERAL DESCRIPTION

The TDA8501 is a highly integrated PAL/NTSC encoder IC which is designed for use in all applications where R, G and B or Y, U and V signals require transformation to PAL or NTSC values. the specification of the input signals are fully compatible with the specification of those of the TDA8505 SECAM-encoder.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8501	24	DIL	plastic	SOT234AH2
TDA8501T	24	SO	plastic	SOT137AH1

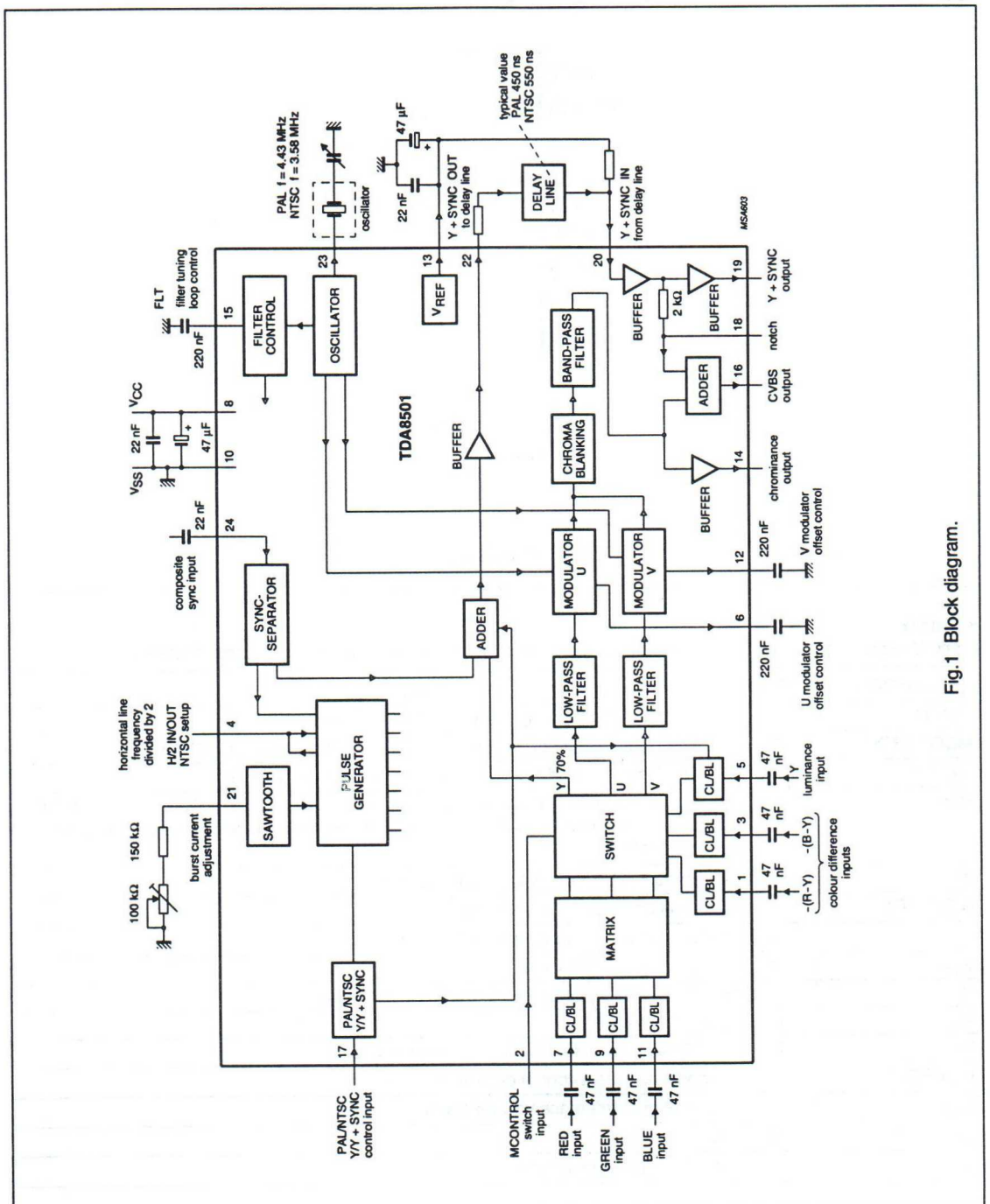


Fig.1 Block diagram.

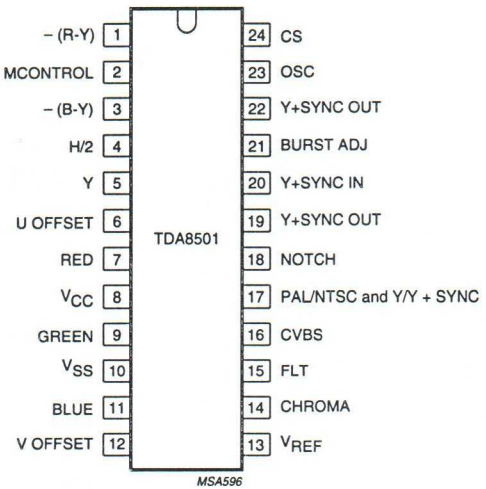


Fig.2 Pin configuration.

PINNING

U and V respectively, are the terms used to describe the colour difference signals at the output of the matrix.

SYMBOL	PIN	DESCRIPTION
–(R–Y)	1	colour difference input signal, for EBU bar (75%) 1.05 V (p-p)
MCONTROL	2	multiplexer switch control input; HIGH = RGB, LOW = –(R–Y), –(B–Y), Y
–(B–Y)	3	colour difference input signal, for EBU bar (75%) 1.33 V (p-p)
H/2	4	line pulse input/output divided-by-2 for synchronizing the internal H/2, if not used, this pin dependent on mode selected, is either left open-circuit, or connected to V_{CC} or to ground (note 1)
Y	5	luminance input signal 1 V nominal without sync
U OFFSET	6	U modulator offset control capacitor
R	7	RED input signal for EBU bar of 75% 0.7 V (p-p)
V_{CC}	8	supply voltage; 5 V nominal
G	9	GREEN input signal for EBU bar of 75% 0.7 V (p-p)
V_{SS}	10	ground (0 V)
B	11	BLUE input signal for EBU bar of 75% 0.7 V (p-p)
V OFFSET	12	V modulator offset control capacitor
V_{REF}	13	2.5 V internal reference voltage output
CHROMA	14	chrominance output
FLT	15	filter tuning loop capacitor

SYMBOL	PIN	DESCRIPTION
CVBS	16	composite PAL or NTSC output, 2 V (p-p) nominal
PAL/NTSC and Y/Y + SYNC	17	four level control pin (note 2)
NOTCH	18	Y + SYNC output via an internal resistor of 2 kΩ; a notch filter can be connected to this pin
Y + SYNC OUT	19	2 V (p-p) nominal Y + SYNC output
Y + SYNC IN	20	Y + SYNC input; (from pin 22) connected to the output of the external delay line
BURST ADJ	21	burst current adjustment via external resistor
Y + SYNC OUT	22	Y + SYNC output 1 V (p-p) nominal, connected to the input of the external delay line
OSC	23	oscillator tuning: connected to either a crystal in series with capacitor to ground, or to an external frequency source via a resistor in series with a capacitor
CS	24	composite sync input, 0.3 V (p-p) nominal

Notes

1. Pin 4: in PAL mode, if not connected to external H2 pulse, this pin is the output for the internally generated H/2 signal.
   Pin 4: in NTSC mode, for internal set-up this pin is connected to ground; when internal set-up is switched off, this pin is connected to V_{CC}.
2. The listed voltages connected to pin 17 (if V_{CC} = + 5 V) enable the following Y (via pin 5) input signal states:
   0 V = PAL mode; at pin 5, Y without sync and input blanking on
   5 V = NTSC mode; at pin 5, Y without sync and input blanking on
   1.8 V = PAL mode; at pin 5, Y with sync and input blanking off
   3.2 V = NTSC mode; at pin 5, Y with sync and input blanking off

FUNCTIONAL DESCRIPTION

The TDA8501 device comprises:

- encoder circuit
- oscillator and filter control
- sync separator and pulse shaper.

Within this functional description, the term Y is used to describe the luminance signal and the terms U and V respectively, are used to describe the colour difference signals.

Encoder circuit

INPUT STAGE

The input stage of the device uses two signal paths (see Fig.1). Fast switching between the two signal paths is achieved by means of the signal path selection switch MCONTROL (pin 2).

R, B AND G INPUT SIGNALS PATH

One signal path provides the connection for R, G and B signal inputs (via pins 7, 9 and 11) which are connected to a matrix via clamping and line blanking circuits. The signal outputs from the matrix are U, V and Y.

For an EBU colour bar of 75% the amplitude of the signal must be 0.7 V (peak-to-peak):

U = 0.493 (B–Y)

V = 0.877 (R–Y)

Y = 0.299 R + 0.587 G + 0.114 B

When selected (via MCONTROL), the U, V signals from the matrix are routed through the selection switch to the low pass filters. The Y signal from the matrix is routed through the selection switch to the adder and combined with the sync pulse from the sync separator and then connected via a buffer internally to pin 22 (Y + SYNC OUT to delay line).

–(R–Y), –(B–Y) AND Y INPUT SIGNALS PATH

A second signal path provides the connection for negative colour difference signal inputs –(R–Y), –(B–Y) i.e. V, U (via pins 1, 3) and luminance Y (via pin 5), which are routed directly to the switch inputs via clamping and line blanking circuits.

The Y input signal (via pin 5) differs from other signal inputs, in that the timing of the internal clamp is after the sync period.

The amplitude and polarity of these colour difference and luminance input signals are processed to provide suitable switch inputs of U, V and Y signal values.

The condition for 75% colour bar is:

pin 1 –(R–Y) = 1.05 V (peak-to-peak)

pin 3 –(B–Y) = 1.33 V (peak-to-peak)

pin 5 Y = 1 V (peak-to-peak) without sync

When selected (via MCONTROL), the U and V signals (via the switch) are routed to the low pass filters. The Y signal (via the switch) is routed via the adder and buffer to pin 22 (Y + SYNC OUT to delay line). Dependent on pin 17 conditioning, the Y signal may have external or internal sync added (see section Four level control pin).

FOUR LEVEL CONTROL PIN

The Y input signal (via pin 5) is conditioned by use of the 4-level control pin (pin 17) to emulate either the PAL or NTSC modes, with sync and input blanking off or without sync and input blanking on.

Pin 17 may be hard wire connected to either ground (LOW for PAL mode) or V_{CC} (HIGH for NTSC mode). External resistors can further modify the voltage level input at pin 17 to condition (pin 5) Y with sync and input blanking off or Y without sync and input blanking on. (see section PAL/NTSC and Y/Y + SYNC).

U AND V SIGNALS

In PAL and NTSC modes the U and V (colour difference) signals at the output of the switch are configured differently as follows:

PAL mode:

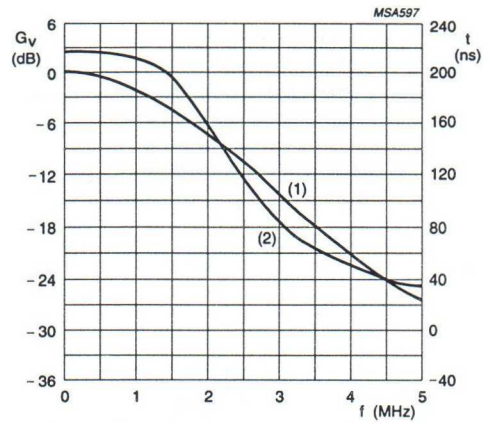
- after the adding of the burst pulse to U and V, these signals are connected to the input of the low pass filters. During the vertical sync period the burst pulse is suppressed.

NTSC mode:

- the burst pulse is only added to U and the gain of the U and V signals is 0.95 of the gain in PAL mode. During the vertical sync period the burst pulse is suppressed.

LOW PASS FILTERS

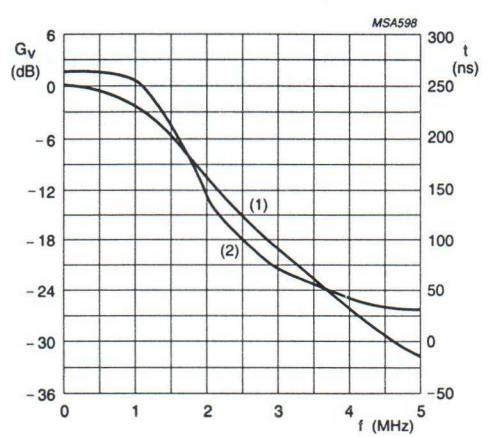
The –3dB nominal frequency response level of the low pass filters are different in PAL and NTSC modes.



(1) frequency response.

(2) group delay.

Fig.3 Low pass filter response for colour difference signals (PAL mode).



(1) frequency response.

(2) group delay.

Fig.4 Low pass filter response for colour difference signals (NTSC mode).

PAL mode: bandwidth = 1.35 MHz nominal (see Fig.3).

NTSC mode: bandwidth = 1.1 MHz nominal (see Fig.4).

The signal outputs of the low pass filters are connected to the signal inputs of the U and V modulators.

U AND V MODULATORS

Two four-quadrant multipliers are used for quadrature amplitude modulation of the U and V signals. The level of harmonics produced by the modulated signals are minimal, because of real multiplication with sinewave carriers.

The unbalance of the modulators is minimized by means of a control loop and two external capacitors, pin 6 for the U modulator and pin 12 for the V modulator. The timing of the control loop is triggered by the H/2 pulse, so that during one sync period the U control is active and during the next sync period the V control is active. In this way, when U and V are both zero, the suppressed carrier is guaranteed to be at a low level.

The internal oscillator circuit generates two sinewave carriers (0 degree and 90 degree). The '0 degree' (0) carrier is connected to the U modulator and the '90 degree' (1) carrier is connected to the V modulator.

PAL mode:

- switched sequentially by the H/2 pulse, the V signal is modulated alternately with the direct and inverse carrier.
- the internal H/2 pulse can be forced into a specific phase by means of an external pulse connected to pin 4 (H/2). Forcing is active at HIGH level. If not used pin 4 can be left open-circuit or connected to ground. If pin 4 is left open, the internally generated H/2 pulse (output) is connected to this pin.

NTSC mode:

- alternation of the V modulation is not allowed. If pin 4 is not used for set-up control (see Y + SYNC, CVBS and Chrominance outputs), it can be left open-circuit or connected to ground.

CHROMINANCE BLANKING

The signal outputs from the modulators are connected to the signal input of the chrominance blanking circuit. To avoid signal distortion that may be caused by the control loop, the signal outputs of the modulators are blanked during the sync period. This prevents signal distortion during the adding of the sync pulse at the CVBS output circuit.

BANDPASS FILTER

A wide symmetrical bandpass filter is used so that a maximum performance of the chrominance for Y + C (SVHS) is guaranteed. This wide curve is possible because of the minimal signal level of the harmonics within the modulators see Figs (PAL mode: 5 and 6); (NTSC mode: 7 and 8) which illustrate the nominal response for PAL and NTSC modes.

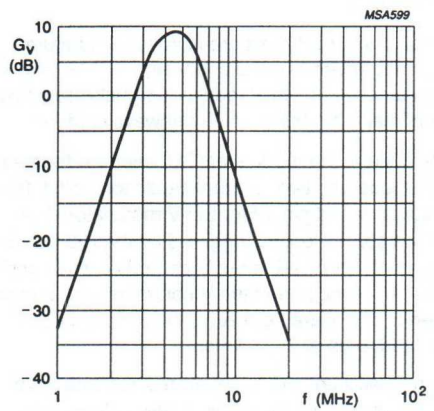
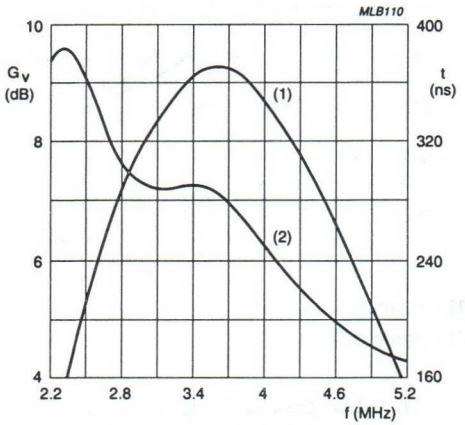


Fig.5 Band pass filter nominal frequency response (PAL mode).



(1) frequency response.
(2) group delay.

Fig.6 Band pass filter nominal frequency/group delay response (PAL mode).

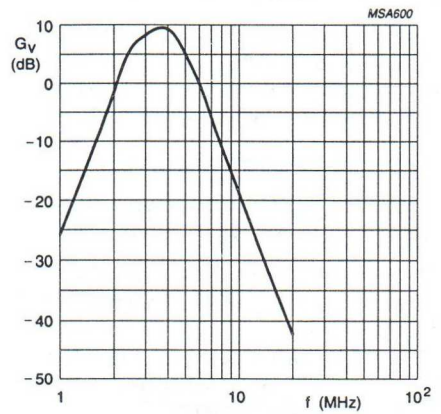
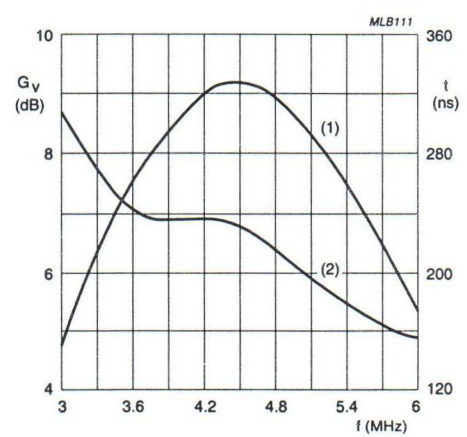


Fig.7 Band pass filter nominal frequency response (NTSC mode).



(1) frequency response.

(2) group delay.

Fig.8 Band pass filter nominal frequency/group delay response (NTSC mode).

Y + SYNC, CVBS AND CHROMINANCE OUTPUTS

The Y signal from the matrix, or the Y signal from pin 5, (selected via the switch) is added with the composite sync signal of the sync separator (dependent on pin 17 conditioning). The output of the adder, nominal 1 V (peak-to-peak), is connected to pin 22 (see Fig.1). Pin 22 is connected to an external delay line.

The delay line is necessary for correct timing of the Y + SYNC signal with the chrominance signal. The output resistor of the delay line is connected to V_{REF} (pin 13). The output of the external delay line is connected to (input) pin 20.

The Y + SYNC (delayed) input signal at pin 20 is amplified via a buffer to a level of 2 V (peak-to-peak) nominal and connected to pin 19 (Y + SYNC output).

The Y + SYNC (delayed) input signal at pin 20 is also connected via an internal resistor of 2 kΩ to the input of the CVBS adder stage. After the internal resistor of 2 kΩ, and before the input of the CVBS adder, an external notch filter can be connected via pin 18.

The chrominance output of the bandpass filter is added with Y + SYNC signal via the CVBS adder. The CVBS (combined video and blanking signal) output of the adder is connected to pin 16 with a nominal amplitude of 2 V (peak-to-peak).

The chrominance output of the bandpass filter is amplified via a buffer and connected to pin 14. The chrominance amplitude corresponds with the value of Y + SYNC signal output at pin 19. Together both outputs give the Y + C (SVHS) signals.

BLACK AND BLANKING LEVELS IN PAL AND NTSC MODES

PAL mode: Fig.9 illustrates the nominal Y + SYNC signal at pin 22, the difference between black and blanking level is 0 mV.

NTSC mode: Fig.10 illustrates the nominal Y + SYNC signal at pin 22, the difference between black and blanking level is 53 mV.

Because of the difference between the black and blanking level in the NTSC mode, there are two options for NTSC.

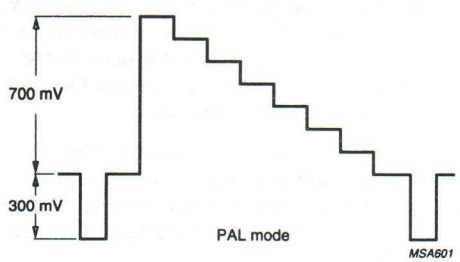


Fig.9 Nominal Y + SYNC signal level at pin 22 (PAL mode).

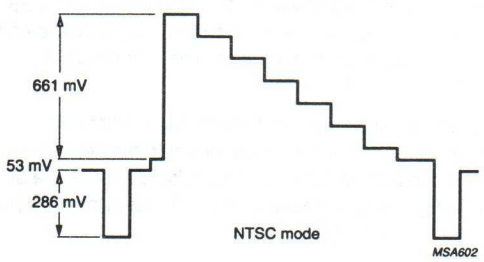


Fig.10 Nominal Y + SYNC signal level at pin 22 (NTSC mode).

NTSC option with internal set-up generation

Pin 4 connected to ground or left open-circuit. The set-up is generated internally and the input signals have the values already specified in section Input stage. The set-up is not suppressed during vertical sync.

NTSC option without internal set-up generation

Pin 4 connected to V_{CC}. This option places some restrictions on the input signals as follows:

- if the output signal must be according to the NTSC standard, the input signals must be generated with a specific set-up level
- for R, G and B inputs a set-up level of 53 mV is required, therefore the specified amplitude must be 753 mV (peak-to-peak) instead of 700 mV (peak-to-peak)
- for U, V and Y inputs a set-up level for Y of 76 mV is required, therefore the specified amplitude must be 1076 mV (peak-to-peak) (without sync) instead of 1 V (peak-to-peak). This option, combined with U, V and Y inputs, is not possible if V_{CC} is < 4.75 V.

Oscillator and Filter Control

The internal crystal oscillator is connected to pin 23 which provides for the external connection of a crystal in series with a trimmer to ground. It is possible to connect an external signal source to pin 23, via a capacitor in series with a resistor. The signal shape is not important. Figure 11 shows the external components connected to pin 23 and the required conditions. The minimum AC current of 50 μA must be determined by the resistors (R_{int} and R_{ext}) and the voltage of the signal source. For example, in this way an external sub-carrier, locked to the sync, can be used.

PAL mode: frequency of the oscillator is 4.433618 MHz.

NTSC mode: frequency of the oscillator is 3.579545 MHz.

The −3 dB of the low pass filters and the centre frequency of the bandpass filter are controlled by the filter control loop and directly coupled to the value of the frequency of the oscillator. The external capacitor of the control loop is connected to pin 15.

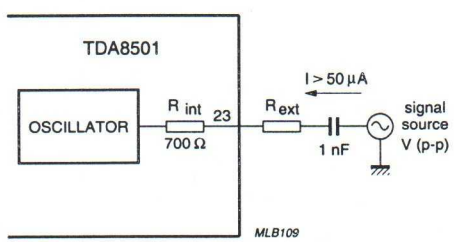


Fig.11 Tuning circuit for external signal source.

Sync separator and Pulse shaper

The composite sync (CS) input at pin 24 (via the sync separator) together with a sawtooth generator provide the source for all pulses necessary for the processing.

Pulses are used for:

- clamping
- video blanking
- H/2
- chrominance blanking
- burst pulse generation for adding to U, V
- pulses for the modulator offset control.

The value of the sawtooth generator output (current) is determined by the value of a fixed resistor to ground which is connected externally at pin 21 (BURST ADJ). When finer tolerance of the burst position is required, the fixed resistor is connected in series with a variable potentiometer to ground. By use of the potentiometer the burst position at the outputs can be finely adjusted, after which the pulse width of the burst and the position and pulse width of all other internal pulses are then determined. When using a fixed resistor with a tolerance of 2%, a tolerance of 10% of the burst position can be expected. Timing diagrams of the pulses are provided by Figs 12 and 13.

H/2 at pin 4 is only necessary in the PAL mode when the internal H/2 pulse requires locking with an external H/2 phase (two or more encoders locked in same phase). The forcing of the internal H/2 to a desired phase is possible by means of an external pulse. Forcing is active at HIGH level.

For the functioning of Pin 4 in the NTSC mode see also section Black and Blanking levels in PAL and NTSC modes.

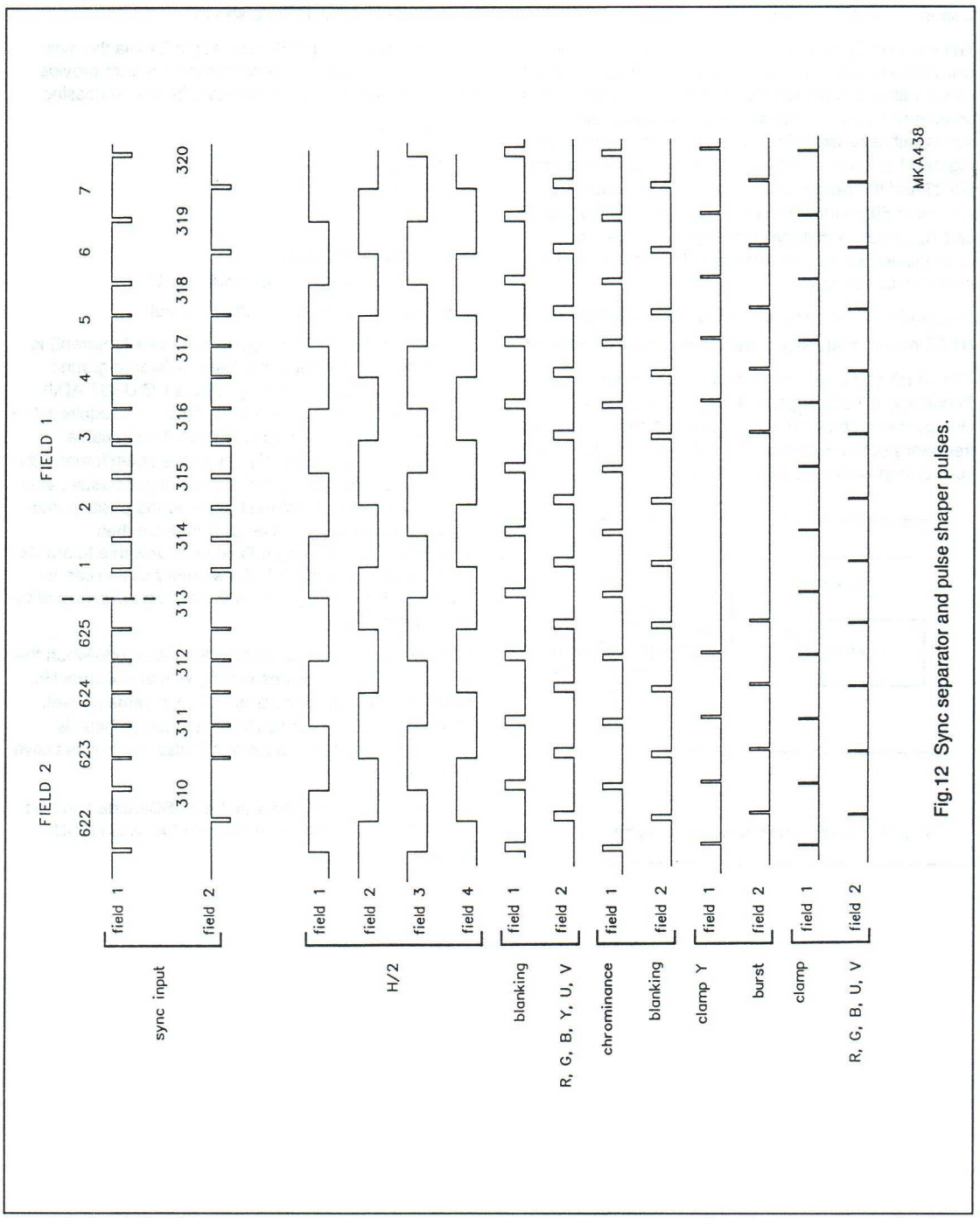


Fig.12 Sync separator and pulse shaper pulses.

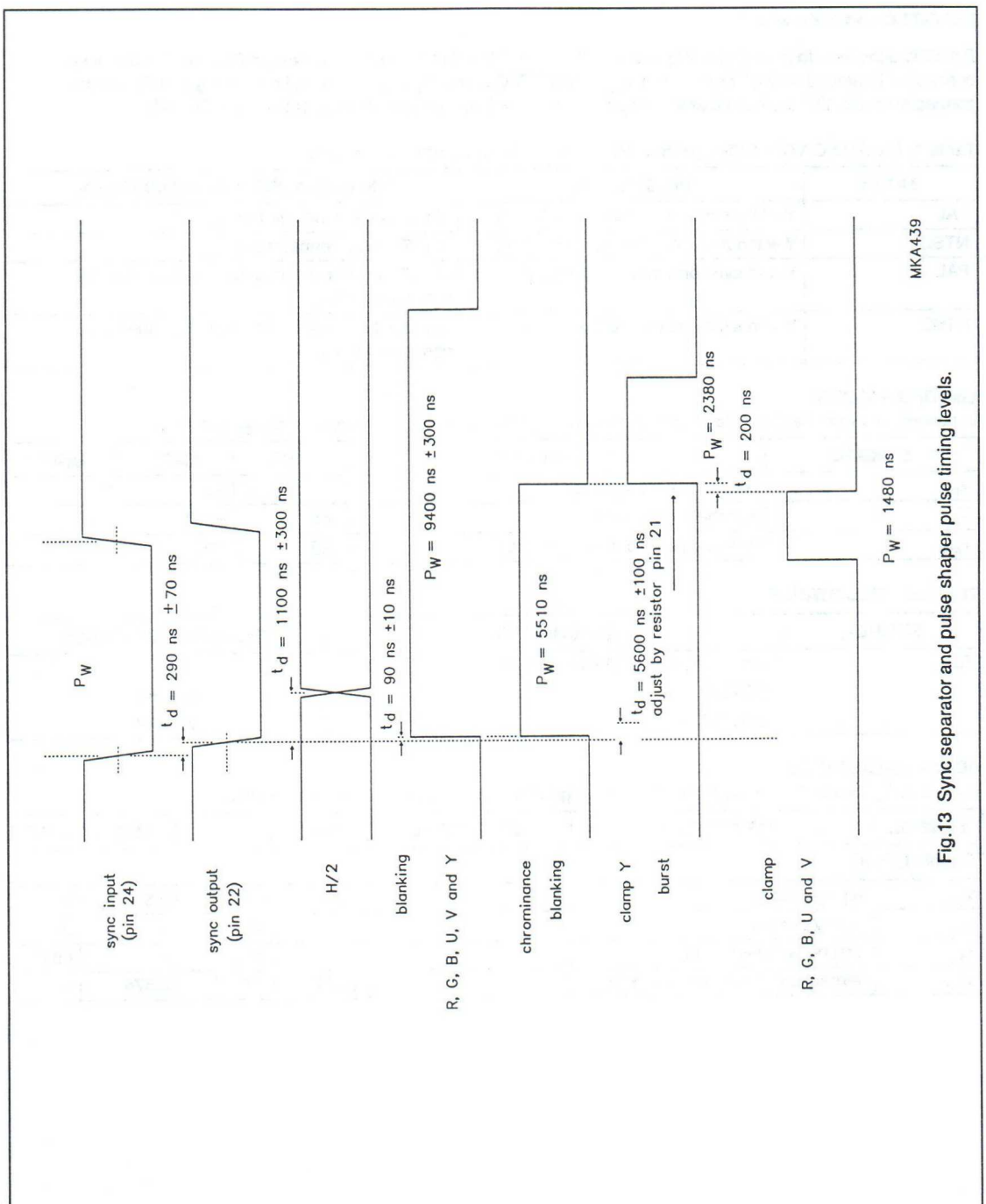


Fig.13 Sync separator and pulse shaper pulse timing levels.

PAL/NTSC and Y/Y + SYNC

Pin 17 is used as a four level control pin to condition the Y/Y + SYNC input signal (via pin 5). Pin 17 is normally connected to ground for PAL mode, or to V_{CC} for the NTSC mode. By use of external resistors (potential divider connected to pin 17), the input blanking at pin 5 can be switched on and off. (see Table 1 and Fig 14).

Table 1 PAL/NTSC Y/Y + SYNC pin 5 options (pin 17 connection configurations).

MODE	PIN 5 STATUS	PIN 17 CONNECTION REQUIREMENT
PAL	Y without sync and input blanking on	pin 17 LOW, connected to V_{SS}
NTSC	Y without sync and input blanking on	pin 17 HIGH, connected to V_{CC}
PAL	Y with sync and input blanking off	pin 17 with 39 kΩ connected to V_{CC} and 22 kΩ connected to V_{SS}
NTSC	Y with sync and input blanking off	pin 17 with 22 kΩ connected to V_{CC} and 39 kΩ connected to V_{SS}

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134); all voltages referenced to V_{SS} (pin 10).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage	0	5.5	V
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT234	66 K/W
	SOT137	75 K/W

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; all voltages referenced to ground (pin 10); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current		–	40	–	mA
P_{tot}	total power dissipation		–	200	–	mW
V_{REF}	reference voltage output (pin 13)		2.425	2.5	2.575	V

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; composite sync signal connected to pin 24; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Encoder circuit						
Input stage (pins 1, 3, 5, 7, 9 and 11); black level = clamping level						
	maximum signal					
$V_{n(max)}$	from black level positive		–	1.2	–	V
$V_{n(min)}$	from black level negative	only pins 1, 3 and 5	–	0.9	–	V
I_{bias}	input bias current	$V_I = V_{13}$	–	–	< 1	µA
V_I	input voltage clamped	input capacitor connected to ground	tbf	V_{13}	tbf	V
$\|Z_I\|$	input clamping impedance					
		I_I = 1 mA	–	80	–	Ω
		I_O = 1 mA	–	80	–	Ω
	matrix and gain tolerance of R, G and B signals		–	–	< 5	%
G	gain tolerance of Y, –(R–Y) and –(B–Y)		–	–	< 5	%
MCONTROL (pin 2; note 1)						
V_{IL}	LOW level input voltage Y, –(R–Y) and –(B–Y)		0	–	0.4	V
V_{IH}	HIGH level input voltage R, G and B		1	–	5	V
I_I	input current		–	–	–3	µA
t_{sw}	switching time		–	50	–	ns
U modulator offset control (pin 6)						
V_6	DC voltage control level		–	2.5	–	V
I_{LI}	input leakage current		–	–	100	nA
V_{LL}	limited level voltage LOW		–	1.8	–	V
V_{HL}	limited level voltage HIGH		–	3.2	–	V
V modulator offset control (pin 12)						
V_{12}	DC voltage control level		–	2.5	–	V
I_{LI}	input leakage current		–	–	100	nA
V_{LL}	limited level voltage LOW		–	1.8	–	V
V_{HL}	limited level voltage HIGH		–	3.2	–	V
Y + SYNC (pin 22 out to delay circuit)						
R_O	output resistance		–	–	< 25	Ω
I_{sink}	maximum sink current		350	–	–	µA
I_{source}	maximum source current		1000	–	–	µA
V_{BL}	black level output voltage		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL mode; pin 17 = 0 V						
V_{SYNC}	sync voltage amplitude		285	300	315	mV
V_Y	Y voltage amplitude		665	700	735	mV
V_{DIF}	difference between black and blanking level		–	0	–	mV
NTSC mode; pin 17 = 5 V and pin 4 open-circuit or ground						
V_{SYNC}	sync voltage amplitude		270	286	300	mV
V_Y	Y voltage amplitude		628	661	694	mV
V_{DIF}	difference between black and blanking level		–	53	–	mV
BW	frequency response	pin 22 with external load of R = 10 kΩ and C = 10 pF	10	–	–	MHz
	group delay tolerance		–	–	20	ns
t_d	sync delay from pin 24 to pin 22		220	290	360	ns
t_d	Y delay from pin 5 to pin 22		–	10	–	ns
α	Chrominance cross talk	0 dB = 1330 mV (peak-to-peak) = 75% RED	–	–	–60	dB
Y + SYNC IN (pin 20 from delay circuit; note 2)						
I_{bias}	input bias current		–	–	1	μA
V_I	maximum voltage amplitude		–	–	1	V
Y + SYNC OUT (pin 19 output Y (SVHS); note 2)						
R_O	output resistance		–	120	–	ω
I_{sink}	maximum sink current		650	–	–	μA
I_{source}	maximum source current		1000	–	–	μA
V_{BL}	black level output voltage		–	1.65	–	V
G	Y + SYNC gain; from pin 20 to pin 19		–	12	–	dB
BW	frequency response	pin 19 with external load of R = 10 kΩ and C = 10 pF	10	–	–	MHz
	group delay tolerance		–	–	20	ns
α	Chrominance cross talk	0 dB = 1330 mV (peak-to-peak) = 75% RED	–	–	–54	dB

Notes

1. The threshold level of this pin is 700 mV ±20 mV. The specification of the HIGH and LOW levels is according to the SCART fast blanking.
2. Pin 20 condition: black level of input signal must be 2.5 V; amplitude 0.5 V (peak-to-peak) nominal.

AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOTCH (pin 18)						
R_O	output resistance		1750	2000	2500	Ω
V_{CC}	DC voltage level		–	2.5	–	V
I_{sink}	maximum sink current		350	–	–	µA
Chrominance output (pin 14)						
I_{sink}	maximum sink current		700	–	–	µA
I_{source}	maximum source current		1000	–	–	µA
R_O	output resistance		–	120	–	Ω
ΔV_{DC}	variation of DC voltage level when chrominance signal is blanked and chrominance signal is not blanked		–	–	5	mV
PAL mode; pin 17 = 0 V						
V_O	chrominance output voltage (peak-to-peak) amplitude burst		480	600	720	mV
	ratio: chrominance (75% RED)/burst		2.1	2.2	2.3	
NTSC mode; pin 17 = 5 V						
V_O	chrominance output voltage (peak-to-peak) amplitude burst		460	570	680	mV
	ratio: chrominance (75% RED)/burst		2.1	2.2	2.3	
	carrier suppression when input-signals are 0 V	0 dB = 1330 mV (peak-to-peak)	–	37	–	dB
	phase accuracy (difference between 0 and 90 degree carriers)		–	–	2	degrees
LPF	Low-pass filters	see Figs 3 and 4				
BPF	Band-pass filters	see Figs 5 and 6				
V_n	noise level (RMS value)		–	–	4	mV
BP	burst phase; 0 degrees = phase U carrier					
	PAL mode		–	±135	–	degrees
	NTSC mode		–	180	–	degrees
α	Y + SYNC cross talk (0 to 6 MHz)	0 dB = 1400 mV (peak-to-peak)	–	–	–60	dB

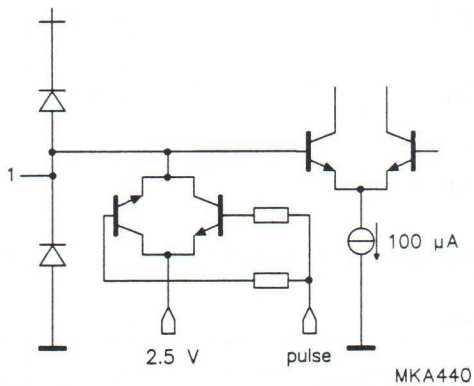
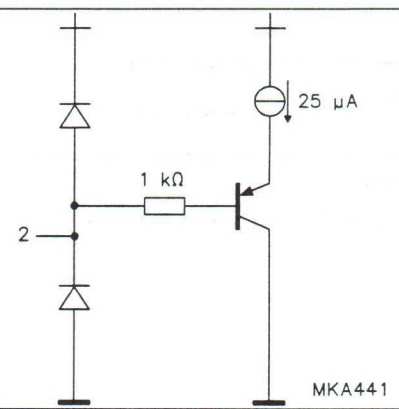
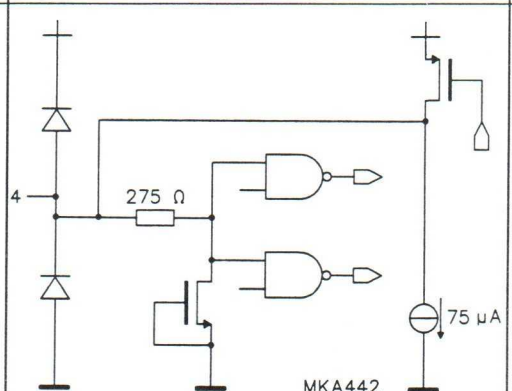
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS output (pin 16)						
I_{sink}	maximum sink current		650	–	–	µA
I_{source}	maximum source current		1000	–	–	µA
V_O	DC voltage level	Y + SYNC = 0	–	1.6	–	V
G	Y + SYNC gain; from pin 20 to pin 16		–	12	–	dB
G	chrominance difference; from pin 14 to pin 16		–	0	–	dB
G_ϕ	differential phase	note 1	–	–	3	degrees
G_V	differential gain	note 2	–	–	3	dB
R_O	output resistance		–	120	–	Ω
Oscillator output (pin 23)						
OSC	series-resonance	the resonance resistance of the crystal should be < 60 Ω and the parallel capacitance of the crystal should be < 10 pF.				
Filter tuning loop (pin 15)						
V_{DC}	DC control voltage level NTSC		–	0.83	–	V
V_{DC}	DC control voltage level PAL		–	0.88	–	V
V_{DCL}	limited DC-level LOW	I_O = 200 µA	–	0.27	–	V
V_{DCH}	limited DC-level HIGH	I_I = 200 µA	–	1.8	–	V
H2 (pin 4)						
V_{IL}	LOW level input voltage	inactive	0	–	1	V
V_{IH}	HIGH level input voltage	active	4	–	5	V
I_I	current for forcing HIGH		220	–	–	µA
I_O	current for forcing LOW		260	–	–	µA
V_O	voltage out LOW		–	–	< 0.5	V
V_O	voltage out HIGH		4	–	–	V
I_{sink}	maximum sink current		50	–	–	µA
I_{source}	maximum source current		50	–	–	µA
Composite sync input (pin 24)						
V_{SYNC}	SYNC pulse amplitude		75	300	600	mV(p-p)
	slicing level		–	50	–	%
I_I	input current		–	4	–	µA
I_O	maximum output current during SYNC		–	100	–	µA
BURST ADJ (pin 21; note 3)						
BP	DC voltage level		–	V_{REF} (V13)	–	V

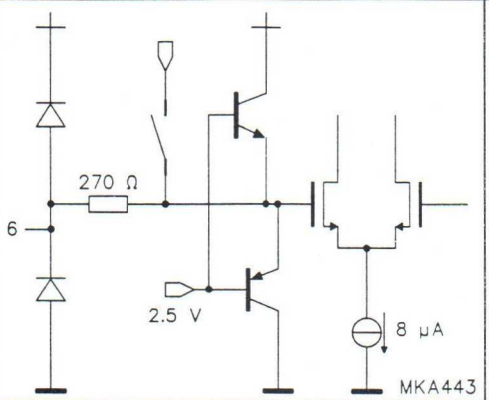
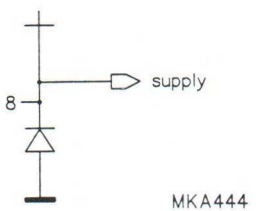
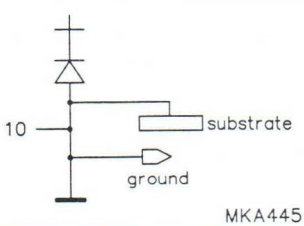
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control pin PAL/NTSC and Y/Y + SYNC (pin 17; note 4)						
V_I	PAL mode and blanking pin 5 active internal sync added to Y		0	–	1	V
V_I	PAL mode and blanking pin 5 inactive internal sync not added to Y		1.6	–	2.0	V
V_I	NTSC mode and blanking pin 5 active internal sync added to Y		4	–	5	V
V_I	NTSC mode and blanking pin 5 inactive internal sync not added to Y		3	–	3.4	V
I_{bias}	input bias current		–	–	–10	μA

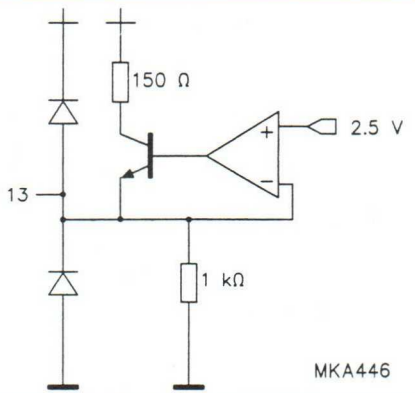
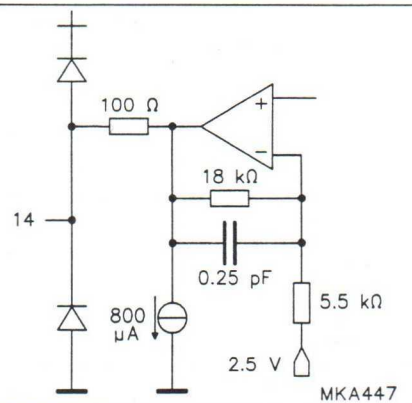
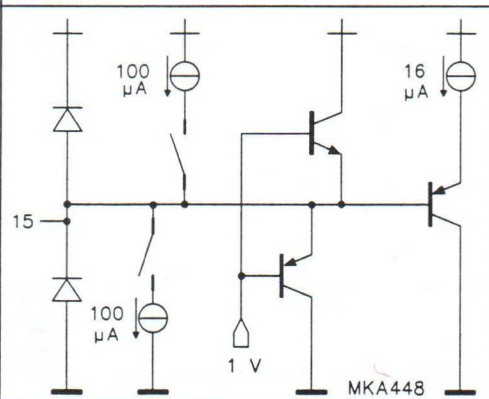
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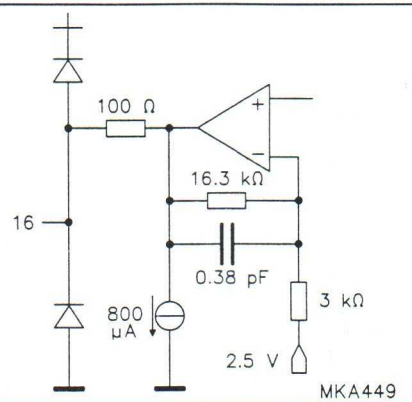
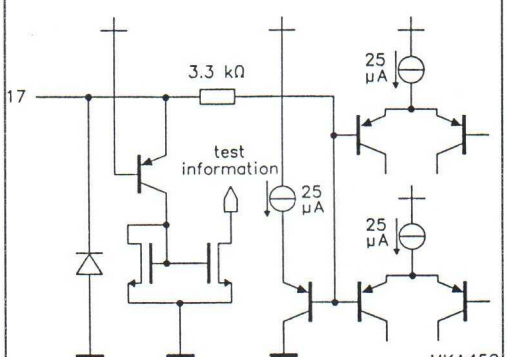
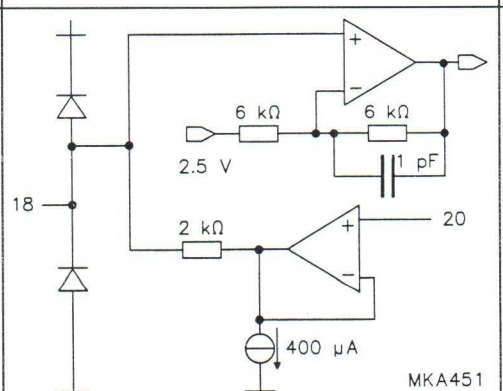
1. Definition: *maximum phase – minimum phase = difference phase*
2. Definition: $\frac{\textit{maximum gain} - \textit{minimum gain}}{\textit{maximum gain}} \times 100 = \textit{difference gain \%}$
3. The output impedance of this pin is low (< 100 Ω). The nominal value of the external resistor is 196 kΩ (see also section Sync separator and Pulse shaper).
4. The threshold levels are: 0.25 times V_{CC}, 0.5 times V_{CC} and 0.75 times V_{CC}.

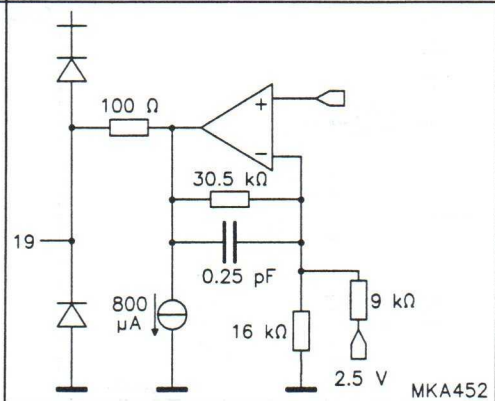
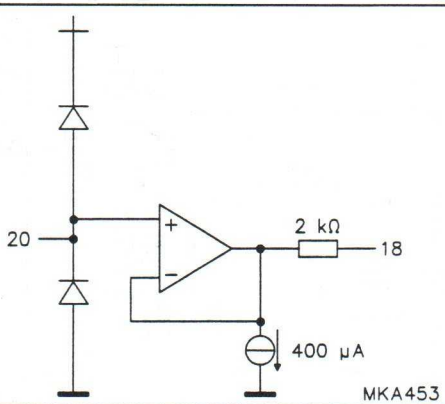
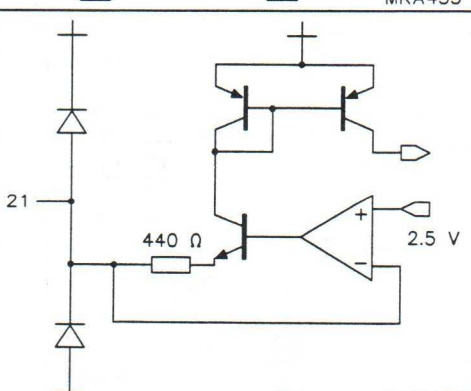
Table 2 Internal circuitry.

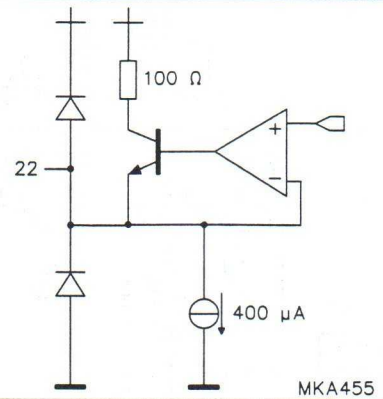
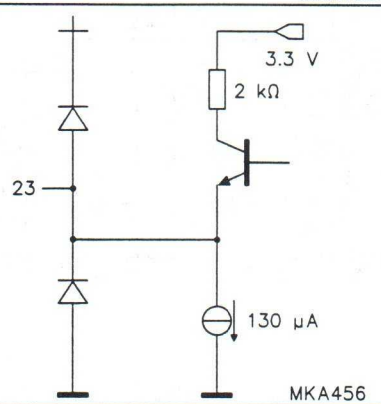
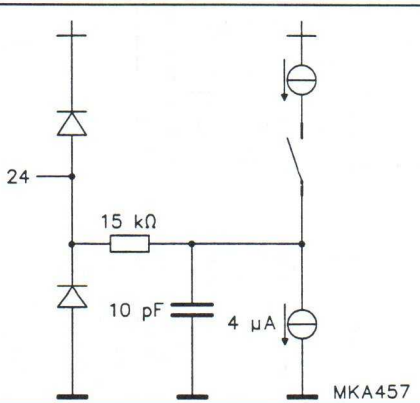
PIN	NAME	CIRCUIT	DESCRIPTION
1	–(R–Y)		–(R–Y) input; connected via 47 nF capacitor 1.05 V (p-p) for EBU bar of 75% see also pins 3, 5, 7, 9 and 11
2	MCONTROL		multiplexer switch control input < 0.4 V Y, U and V > 1 V R, G and B
3	–(B–Y)	see pin 1	–(B–Y) input; connected via 47 nF capacitor 1.33 V (p-p) for EBU bar of 75%
4	H/2 IN/OUT		H/2 input PAL MODE: pin open, output of internal H/2 Forcing possibility NTSC mode: 0 V set-up 5 V no set-up

PIN	NAME	CIRCUIT	DESCRIPTION
5	Y	see pin 1	Y input; connected via 47 nF capacitor 1 V (p-p) for EBU bar of 75%
6	U OFFSET		220 nF (low-leakage) connected to ground see also pin 12
7	R	see pin 1	RED input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%
8	V_{CC}		supply voltage 5 V nominal
9	G	see pin 1	GREEN input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%
10	V_{SS}		ground
11	B	see pin 1	BLUE input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%

PIN	NAME	CIRCUIT	DESCRIPTION
12	V OFFSET	see pin 6	220 nF (low-leakage) connected to ground
13	V_{REF}		2.5 V reference voltage decoupling with 47 µF and 22 nF capacitors
14	CHROMA		chrominance output; together with pin 19 the Y + C (SVHS) output
15	FLT		filter control pin 220 nF capacitor to ground

PIN	NAME	CIRCUIT	DESCRIPTION
16	CVBS		CVBS output
17	PAL/NTSC Y/Y + SYNC		4-level control pin Pin 5: 0 V PAL, Y 1.8 V PAL Y + SYNC 3.2 V NTSC Y + SYNC 5 V NTSC Y
18	NOTCH		pin for external notch filter

PIN	NAME	CIRCUIT	DESCRIPTION
19	Y + SYNC OUT		output of the Y + SYNC signal; together with pin 14 the Y + C (SVHS) output
20	Y + SYNC IN		input of the delayed Y + SYNC signal of the delay line black level must be 2.5 V
21	BURST ADJ		external resistor to ground for adjusting the position of the burst

PIN	NAME	CIRCUIT	DESCRIPTION
22	Y + SYNC OUT		output of the Y + SYNC signal, connected to the delay line via a resistor
23	OSC		subcarrier-crystal in series with a trimmer, or an external subcarrier signal, via 1 nF in series with a resistor
24	CS		composite SYNC signal input amplitude < 600 mV (p-p)

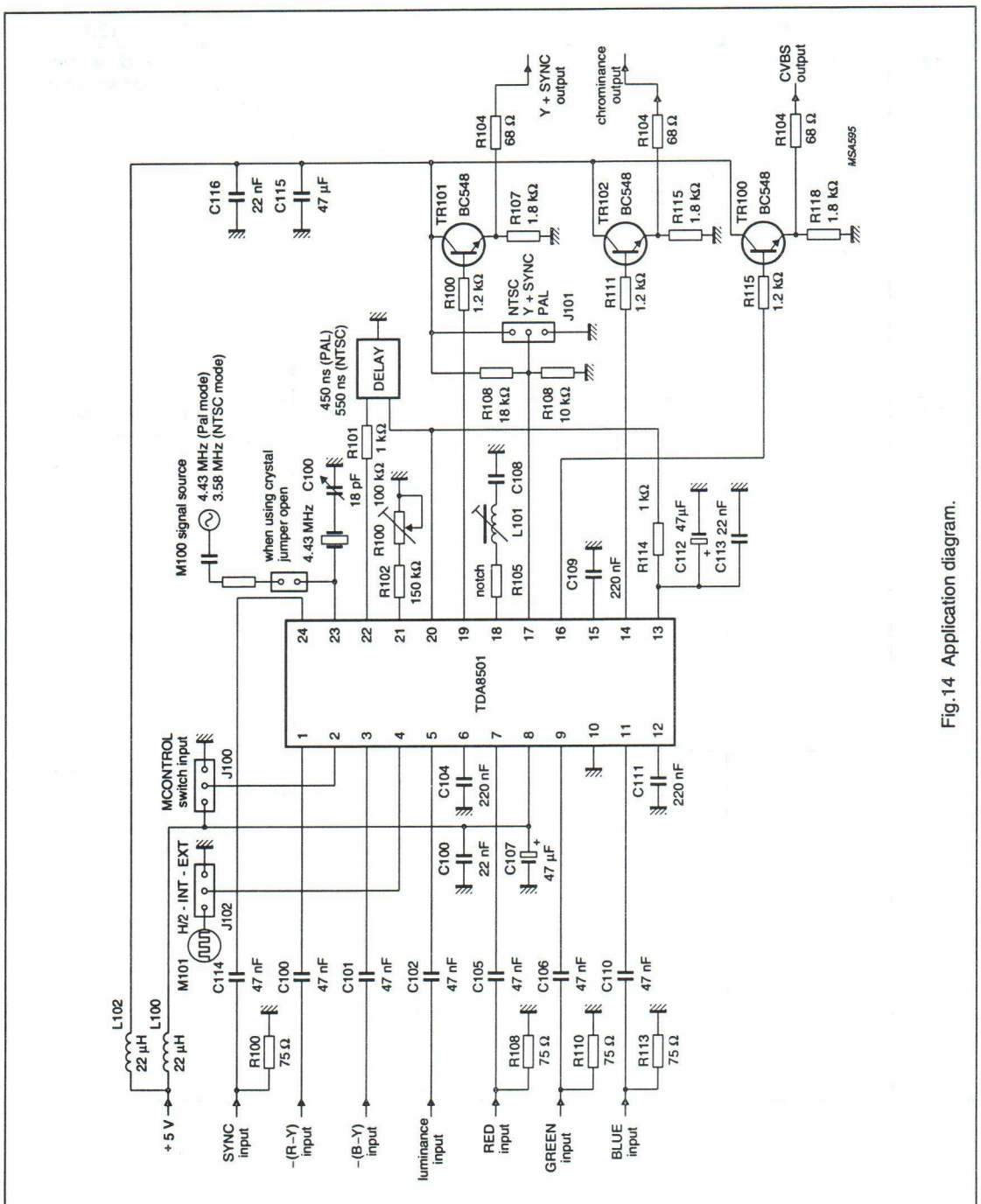


Fig.14 Application diagram.

SECAM encoder TDA8505

FEATURES

- Two input stages, R, G, B and Y, –(R–Y), –(B–Y) with multiplexing.
- Chrominance processing, highly integrated, includes vertical identification, low frequency pre-emphasis and high frequency pre-emphasis (anti-Cloche) and bandpass filter.
- Fully controlled FM modulator which produces a signal in accordance with the SECAM standard without adjustments.
- Two reference oscillators, one for D'R f_0 (4.40625 MHz) and one for D'B f_0 (4.250 MHz). These oscillators are tuned by PLL loop with the frequency of the line sync as reference. Crystal tuning, or tuning by external reference source, of the reference oscillators is possible.
- Output stages, CVBS and separated Y + SYNC and CHROMA. For CVBS output, signal amplitude 2 V (p–p) nominal, thus only an external emitter follower is required for 75 Ω driving.
- Sync separator circuit and pulse shaper, to generate the required pulses for the processing, line, frame, FH/2 and chrominance blanking.
- A 3-level sandcastle pulse is generated for PAL/NTSC to SECAM transcoding.
- FH/2 input for locking with another decoder.
- Colour killing on the internal colour difference signals.
- Internal bandgap reference.

GENERAL DESCRIPTION

The TDA8505 is a highly integrated SECAM encoding IC that is designed for use in all applications that require transformation of R, G and B signals or Y, U and V signals to a standard SECAM signal.

The specification of the input signals is fully compatible with those of the TDA8501 PAL/NTSC encoder.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8505	32	SDIP32	plastic	SOT232-1

BLOCK DIAGRAM

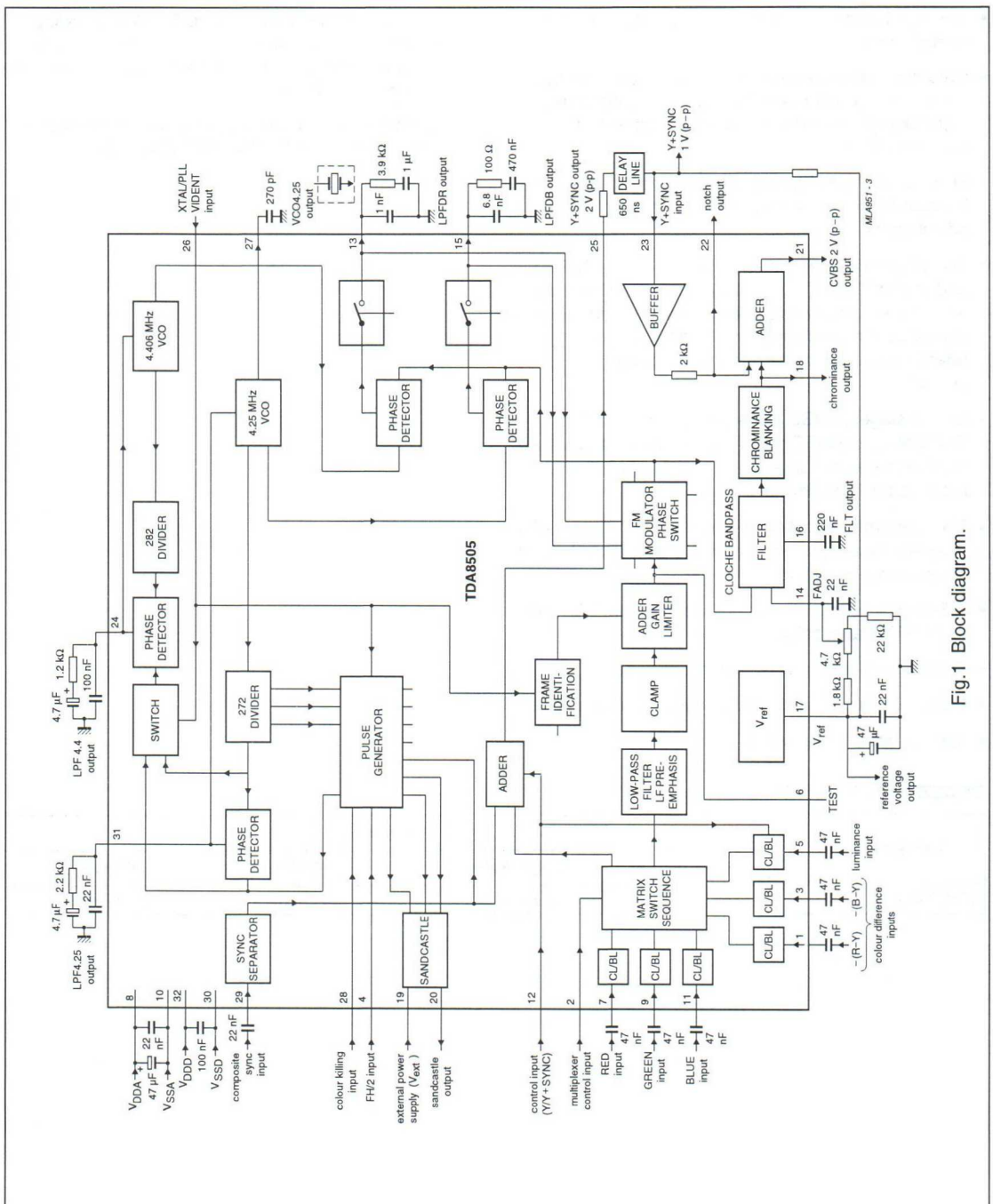


Fig.1 Block diagram.

PINNING

D'R and D'B are the colour difference signals at the output of the multiplexer circuit; D'R = −1.9(R−Y) and D'B = +1.5(B−Y), for an EBU bar of 75% the amplitudes are equal.

SYMBOL	PIN	DESCRIPTION
−(R−Y)	1	colour difference input signal, for EBU bar of 75% 1.05 V (peak-to-peak value)
MCONTR	2	multiplexer control; input HIGH = RGB, input LOW = −(R−Y), −(B−Y) and Y
−(B−Y)	3	colour difference input signal, for EBU bar of 75% 1.33 V (peak-to-peak value)
FH/2	4	line pulse input divided-by-2 for synchronizing two or more encoders; when not used this pin is connected to ground
Y	5	luminance input signal 1 V nominal without sync
TEST	6	test pin; must be connected to V_{CC} (pin 8), or left open-circuit
R	7	RED input signal for EBU bar of 75% 0.7 V (peak-to-peak value)
V_{DDA}	8	analog supply voltage for encoder part; 5 V nominal
G	9	GREEN input signal for EBU bar of 75% 0.7 V (peak-to-peak value)
V_{SSA}	10	analog ground
B	11	BLUE input signal for EBU bar of 75% 0.7 V (peak-to-peak value)
Y/Y+SYNC	12	when this control input is LOW, Y without sync is connected to pin 5, input blanking at pin 5 is active; when input is HIGH, Y+SYNC is connected to pin 5, input blanking at pin 5 is not active
LPFDR	13	modulator control loop filter output; black level of D'R = 4.40625 MHz
FADJ	14	adjustment pin for 4.286 MHz of HF pre-emphasis filter
LPFDB	15	modulator control loop filter output; black level of D'B = 4.250 MHz
FLT	16	filter tuning loop capacitor output
V_{ref}	17	2.5 V internal reference voltage output
CHROMA	18	chrominance output, amplitude corresponds with Y+SYNC at the output of the delay line
V_{ext}	19	external power supply for sandcastle generation; when not used this pin is connected to ground
SAND	20	3-level sandcastle output pulse
CVBS	21	composite SECAM output 2 V (peak-to-peak value) nominal
NOTCH	22	Y+SYNC output after an internal resistor of 2 kΩ; a notch filter can be connected
Y+SYNC IN	23	Y+SYNC input, connected to the output of the delay line
LPF4.4	24	loop filter output for 4.40625 MHz reference oscillator
Y+SYNC OUT	25	Y+SYNC output, 2 V (peak-to-peak value) nominal, connected to the input of the delay line
XTAL/PLL VIDENT	26	control pin; input HIGH = crystal tuning, input LOW = PLL tuning, both **without** vertical identification, 2.5 V = PLL tuning **with** vertical identification
VCO4.25	27	when used for PLL tuning a capacitor is connected; when used for crystal tuning a crystal has to be connected (in series with a capacitor)
COLKIL	28	colour killing; input HIGH = active, internal colour difference signals are blanked
CS	29	composite sync input, 0.3 V (peak-to-peak value) nominal

SYMBOL	PIN	DESCRIPTION
V_{SSD}	30	digital ground
LPF4.25	31	loop filter output for 4.25 MHz reference oscillator; connected to pin 17 (V_{ref}) when external tuning by crystal or signal source
V_{DDD}	32	supply voltage for the digital part

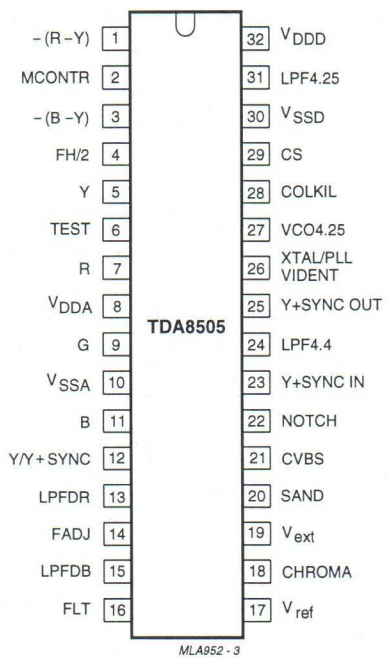


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The following three important circuits are integrated:

- Encoder circuit
- Modulator control circuit
- Sync separator and pulse shaper.

Encoder circuit

INPUT STAGE

R, G and B inputs are connected to the matrix via a clamping and a blanking circuit.

For an EBU colour bar of 75% the amplitude of the signal must be 0.7 V (peak-to-peak value). The outputs of the matrix are Y, D'R and D'B.

The second part of the input stage contains inputs for colour difference signals and a luminance signal. The condition for 75% colour bar is
$-(R-Y)$ = 1.05 V (peak-to-peak value) at pin 1,
$-(B-Y)$ = 1.33 V (peak-to-peak value) at pin 3 and
Y = 1 V (peak-to-peak value) without sync at pin 5. After clamping and blanking the amplitude and polarity are corrected such that the signals are equal to the signals of the matrix output. Signals are connected to a switch. Fast switching between the two input parts is possible by the multiplexer control pin (pin 2).

The Y output signal of the multiplexer is added to the sync pulse of the sync separator.

The Y input (pin 5) is different to the other 5 inputs. The timing of the internal clamping is after the sync period and there is no vertical blanking.

The input blanking of Y can be switched off by a HIGH at pin 12, and the internal sync separator signal is not added to the Y signal. In this way the Y+SYNC is allowed at pin 5 and after clamping internally connected directly to pin 25.

The colour difference signals are switched sequentially by H/2 and fed to the low frequency pre-emphasis circuit.

The colour-killing input signal at pin 28 can be used for completely blanking the internal colour difference signals at the input of the low frequency pre-emphasis filter.

LOW FREQUENCY PRE-EMPHASIS

This filter is fully integrated, Fig.3 illustrates the nominal response.

The transfer is guaranteed within the illustrated area for the whole ambient temperature range by a compensation circuit.

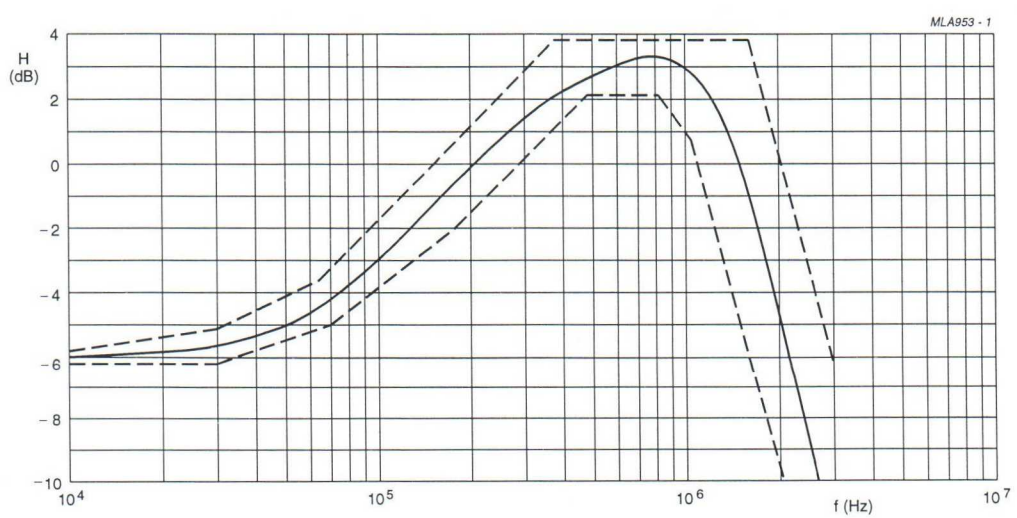


Fig.3 Nominal response for the low frequency pre-emphasis filter.

VERTICAL IDENTIFICATION

After the low frequency pre-emphasis the signal is clamped and, if desired the vertical identification sawtooth waveform can be added. The generation of the vertical identification is switched on/off by the logic level input at pin 26.

Figure 4 shows the sawtooth waveform at the input of the FM modulator with the corresponding frequency values after modulation.

Vertical identification is only possible if PLL tuning is selected.

GAIN + LIMITER

The gain of this amplifier is sequentially switched, so that the amplitude of D'R is 280/230 times the amplitude of D'B (based on an EBU colour bar). The signal is limited at a lower and upper level to ensure that the FM modulator frequencies are always between 3.9 MHz and 4.756 MHz. A DC offset between D'R and D'B is added which corresponds with the limiter levels.

FM MODULATOR

The signal of the gain + limiter stage is fed to the FM modulator.

The modulator control adjusts the DC level at pin 13 to set the frequency of the FM signal to 4.406 MHz at the black level of D'R. The modulator control also sets the DC level at pin 15 to adjust the FM frequency to 4.250 MHz at the black level of D'B.

At the start of every line the FM modulator is stopped and is started again by a short duration pulse of the pulse shaper. These stop/start pulses are operating such that after two lines starting in the same phase, the start phase of the third line is shifted 180 degrees. This sequence is inverted during each vertical blanking.

The FM signal is fed to the internal HF pre-emphasis filter.

HF PRE-EMPHASIS AND BANDPASS FILTER

An HF pre-emphasis filter combined with a bandpass filter is integrated.

Figures 5 and 6 illustrate the frequency response. Two resistors in series with a potentiometer at pin 14 adjusts the frequency to 4.286 MHz with a tolerance of ±20 kHz.

A tuning circuit integrated with an external capacitor connected to pin 16 guarantees a stable frequency response for the whole temperature range.

The output of the bandpass filter is connected directly to the chrominance blanking circuit.

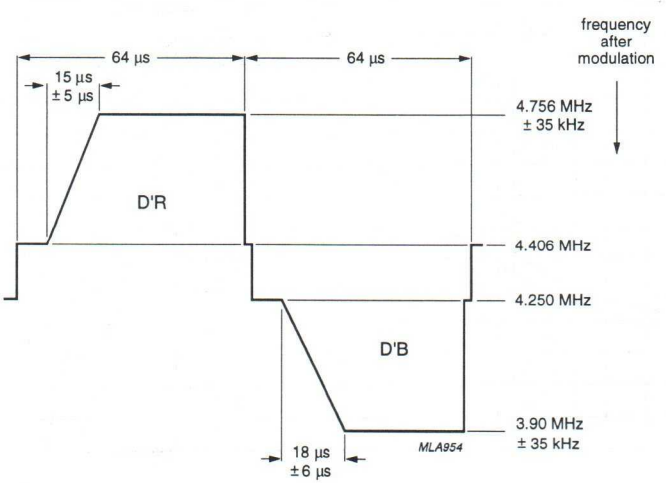


Fig.4 Vertical identification sawtooth waveform input.

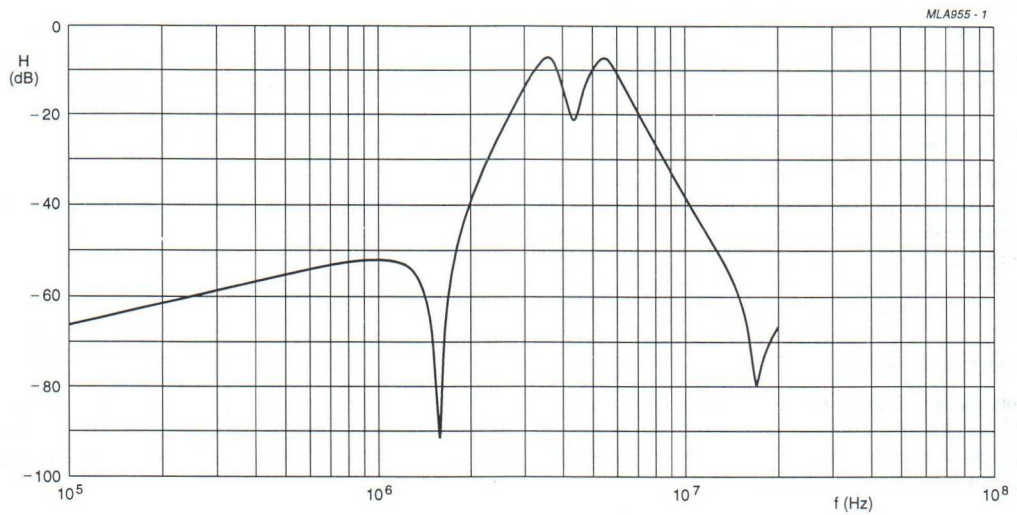


Fig.5 Frequency response of the HF pre-emphasis and bandpass filter; H as a function of frequency (1).

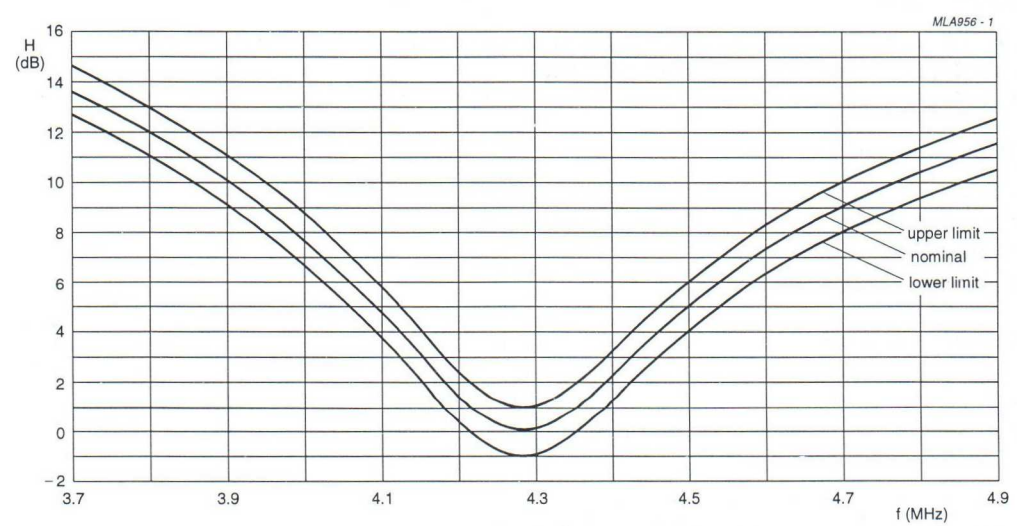


Fig.6 Frequency response of the HF pre-emphasis and bandpass filter; H as a function of frequency (2).

CHROMINANCE BLANKING

The chrominance signal is blanked by the internally generated chrominance blanking pulse. The output of this blanking stage is connected to the chrominance and CVBS output circuits.

Y+SYNC, CVBS, AND CHROMA OUTPUTS

The Y output signal of the matrix is added to the composite sync signal of the sync separator. The output of this adder at pin 25 is connected to the input of an external delay line which is necessary for correct timing of the Y+SYNC signal corresponding with the chrominance signal. The signal amplitude at pin 25 is 2 V (peak-to-peak value) nominal, so at the output of the delay line Y+SYNC is 1 V (peak-to-peak value).

The delay line has to be DC-coupled between pins 25 and 23 to ensure the required DC level at pin 23. The output resistor of the delay line has to be connected to pin 17 where (V_{ref} = 2.5 V).

The output of the delay line is connected to pin 23 which is the input of a buffer operational amplifier. The output of the buffer operational amplifier is connected to pin 22 and to the CVBS adder stage via an internal resistor of 2 kΩ. An external notch filter can be connected to pin 22. The CVBS signal amplitude output at pin 21 is 2 V (peak-to-peak value) nominal. An external emitter follower is used to provide a 75 Ω output load.

The amplitude of the chrominance output signal which is connected to pin 18 corresponds with the Y+SYNC signal at the output of the delay line.

Modulator control circuit

The modulator control circuit has two tuning modes which are controlled by the input at pin 26:

- Tuning by line frequency
- Tuning by crystal or external signal source.

TUNING BY LINE FREQUENCY

Two reference voltage controlled oscillators (VCOs) are integrated, the 4.4 MHz VCO with an internal capacitor and the 4.25 MHz VCO with an external capacitor at pin 27.

A PLL loop with divider circuits directly couples the frequencies of the two VCOs with the line frequency of the sync separator sync signal.

The loop filter for the 4.40625 MHz reference is at pin 24 and the loop filter for the 4.250 MHz reference is at pin 31.

The outputs of the 272 divider are also used for pulse shaping.

Within the vertical blanking period, another two Phase Locked Loops (PLLs) synchronizes the FM modulator during two lines with the 4.406 MHz reference VCO and during the following 2 lines with the 4.250 MHz reference VCO. The loop filters are connected to pins 13 and 15 respectively.

It is necessary to use low-leakage capacitors for these loop filters.

TUNING BY CRYSTAL OR EXTERNAL SIGNAL SOURCE

When the frequency of the sync pulse at pin 29 is not stable or is incorrect it is possible to tune the FM modulator using an external 4.250 MHz crystal connected to pin 27. The 4.25 MHz loop at pin 31 has to be connected to pin 17 (V_{ref}). A stable line frequency reference is generated by the 272 divider circuit which is used for the 4.406 MHz reference loop.

An external signal source, instead of a crystal, can be connected at pin 27 via a capacitor in series with a resistor.

The minimum AC current of 50 μA is determined by the resistor values (R_{int} + R_{ext}) and the output voltage of the signal source (see Fig.7).

When crystal tuning is used no vertical identification is possible.

Crystal tuning is recommended for VTR signals.

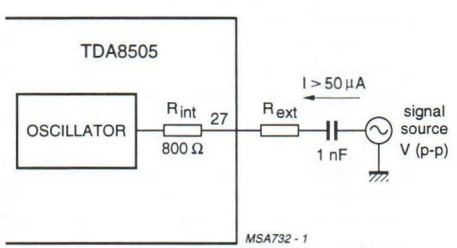


Fig.7 Tuning circuit for external signal source.

Sync separator and pulse shaper

The composite sync input at pin 29 together with the outputs of the 272 divider of the 4.250 MHz reference loop are the sources for all pulses necessary for the processing.

The pulses are used for:

- Clamping
- Video blanking
- FH/2
- Chrominance blanking
- Stop/start of modulator
- Vertical identification
- Timing for the modulator control
- Sandcastle pulse shaping at pin 20.

External FH/2 at pin 4 is only necessary when two or more SECAM encoders have to be locked in the same phase. The phase of the internal FH/2 can be locked with an external FH/2 connected at pin 4. A reset of the internal FH/2 is possible by forcing pin 4 to a HIGH level. This HIGH level corresponds with D'R. Pin 4 is connected to ground when not used.

Figures 9 and 10 show the generated pulses during vertical blanking for PLL tuning or crystal tuning respectively. Figure 11 shows the pulses during line blanking.

Transcoding application

A sandcastle pulse is necessary for the PAL/NTSC demodulator (i.e. TDA4510) for transcoding PAL or NTSC to SECAM.

Most of the demodulator ICs use a sandcastle pulse with an amplitude of 12 V or 8 V. A 12 V or 8 V sandcastle is not possible with the TDA8505 because of the 5 V power supply.

To generate a 3-level sandcastle pulse at pin 20 (see Fig.8) an external supply voltage must be connected to pin 19.

The PAL or NTSC CVBS signal is connected to the composite sync input (pin 29) for PLL tuning and pulse shaping. As previously mentioned the Y input at pin 5 can be used as the Y+SYNC input for the filtered Y+SYNC PAL or NTSC signal, when pin 12 is at a HIGH level.

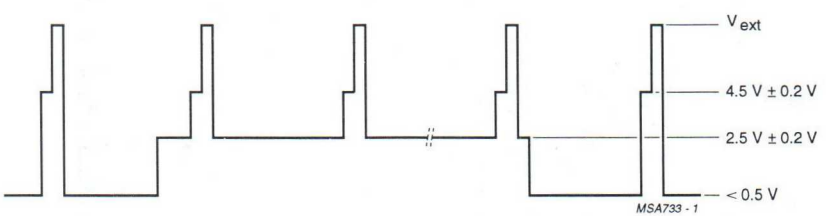


Fig.8 3-level sandcastle pulse.

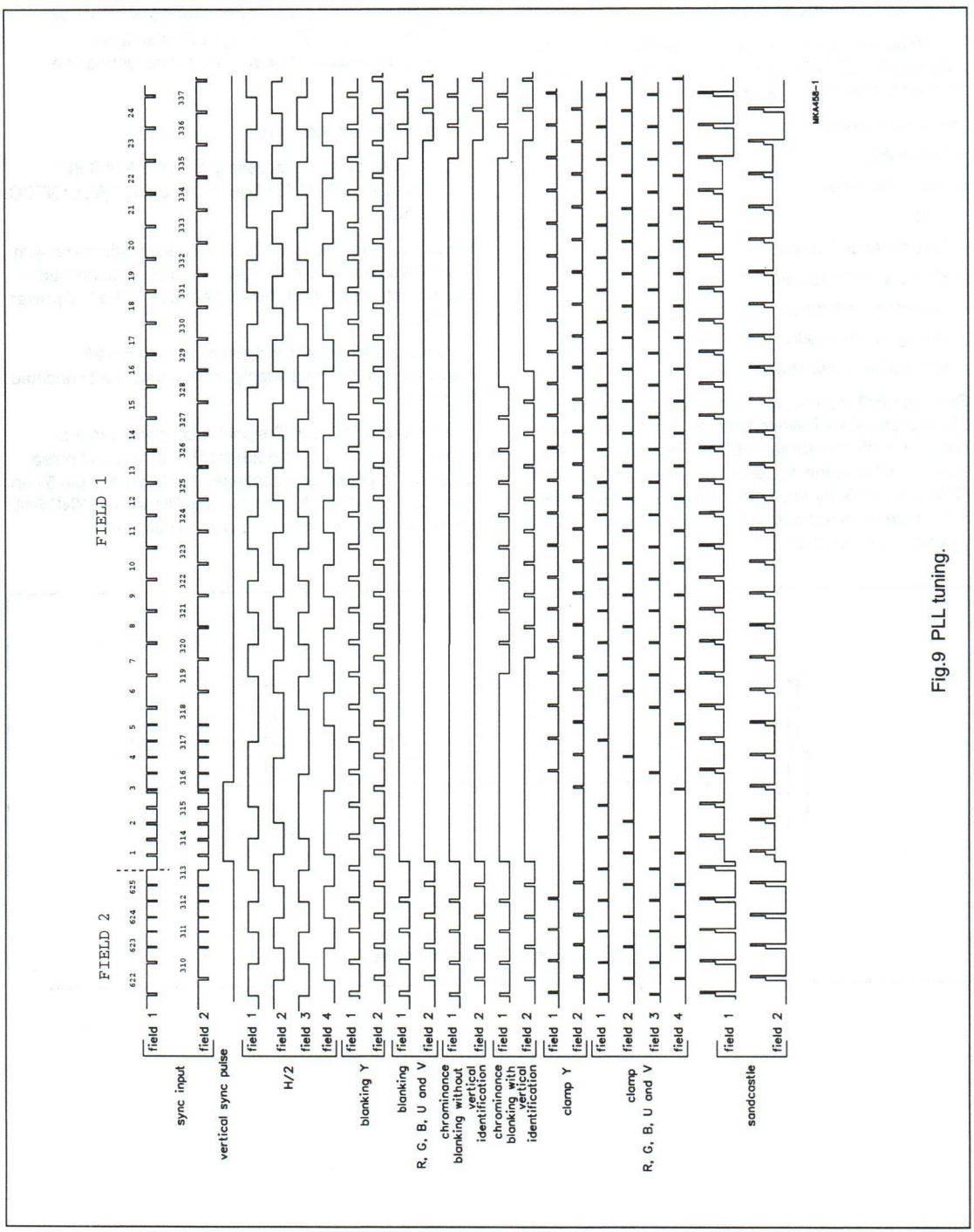


Fig.9 PLL tuning.

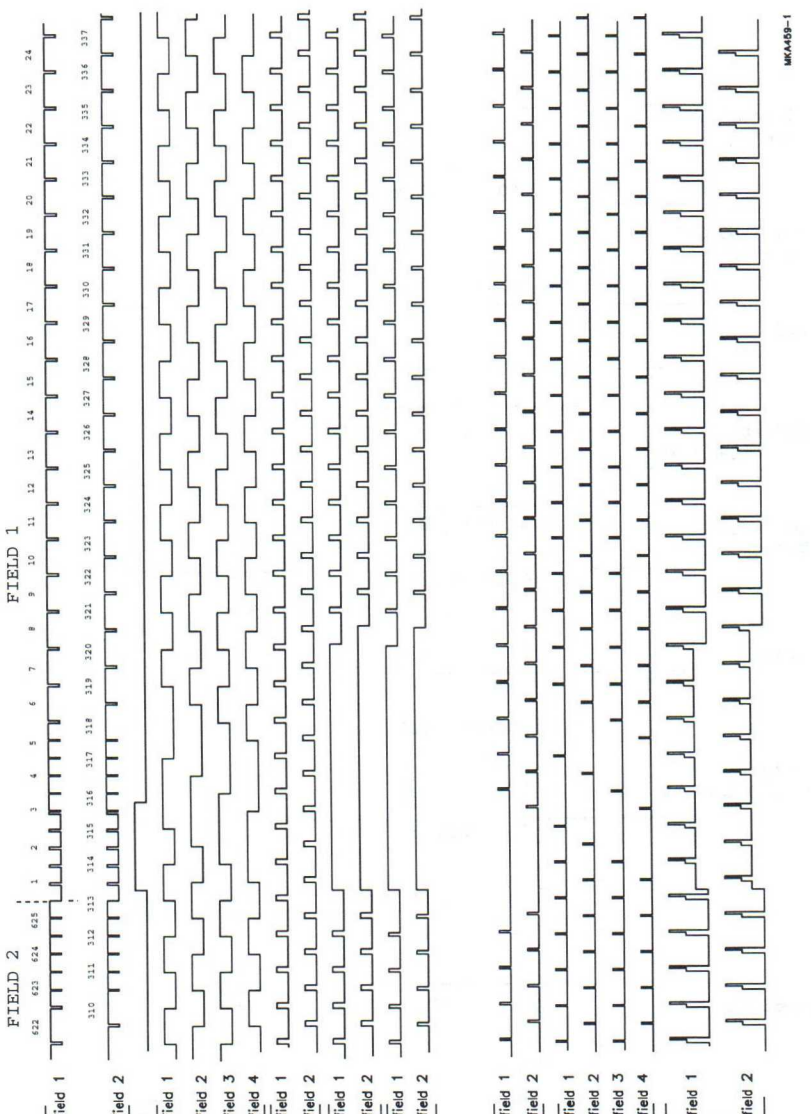


Fig.10 Crystal tuning.

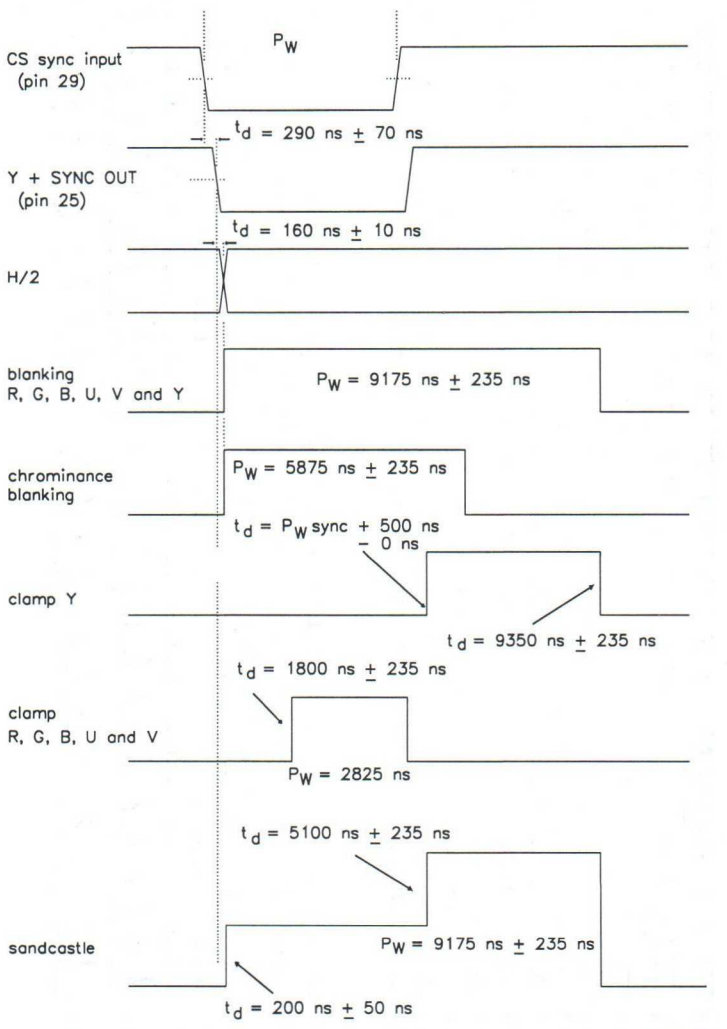


Fig.11 Pulses during line blanking.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to V_{SSA} pin 10.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage for encoder part	0	5.5	V
V_{DDD}	digital supply voltage	0	5.5	V
V_{ext}	external supply voltage for sandcastle generation	0	13.2	V
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

DC CHARACTERISTICS

V_{CC} and V_{DD} = 5 V; T_{amb} = 25 °C; all voltages referenced to pins 10 and 30; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage for encoder part (pin 8)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pin 32)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	39	–	mA
I_{DDD}	digital supply current	–	4	–	mA
V_{ext}	external supply voltage for sandcastle generation	0	8 to 12	13.2	V
P_{tot}	total power dissipation	–	215	–	mW
V_{ref}	reference voltage output (pin 17)	2.425	2.5	2.575	V

AC CHARACTERISTICS

V_{CC} and V_{DD} = 5 V; T_{amb} = 25 °C; composite sync signal connected to pin 29; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Encoder circuit: input stage (pins 1, 3, 5, 7, 9 and 11; black level = clamping level						
$V_{n(max)}$	voltage from black level positive		1.2	–	–	V
$V_{n(min)}$	voltage from black level negative	only pins 1, 3 and 5	0.9	–	–	V
$I_{bias(max)}$	maximum input bias current	$V_I = V_{17}$	–	–	1	µA
V_I	input voltage clamped	input capacitor connected to ground	–	V_{17}	–	V
Z_I	input clamping impedance	I_I = 1 mA	–	80	–	Ω
		I_O = 1 mA	–	80	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Multiplexer control (pin 2; note 1)						
V_{IL}	LOW level input voltage Y, –(R–Y) and –(B–Y)		0	–	0.4	V
V_{IH}	HIGH level input voltage R, G and B		1	–	5	V
I_I	input current		–	–	–3	µA
t_{sw}	switching time		–	50	–	ns
Control input Y/Y+SYNC (pin 12)						
V_{IL}	LOW level input voltage	blanking pin 5 active; internal sync added to Y	0	–	1	V
V_{IH}	HIGH level input voltage	blanking pin 5 inactive; internal sync not added to Y	4	–	5	V
$I_{I(max)}$	maximum input current		–	–	1	µA
XTAL/PLL and VIDENT input (pin 26)						
V_{IL}	LOW level input voltage	PLL mode; vertical identification off	0	–	1	V
V_{IH}	HIGH level input voltage	crystal tuning; vertical identification off	4	–	5	V
V_I	input voltage	pin 26 connected to pin 17; PLL tuning; vertical identification on; see Fig.4	–	V_{17}	–	V
I_I	input current		–	–	–6	µA
COLKIL input (pin 28)						
V_{IL}	LOW level input voltage	inactive	0	–	1	V
V_{IH}	HIGH level input voltage	active	4	–	5	V
$I_{I(max)}$	maximum input current		–	–	1	µA
FH/2 input (pin 4)						
V_{IL}	LOW level input voltage	inactive	0	–	1	V
V_{IH}	HIGH level input voltage	active	4	–	5	V
$I_{I(max)}$	maximum input current		–	–	1	µA
LF pre-emphasis (see Fig.3)						
HF pre-emphasis and bandpass (see Figs 5 and 6)						
FADJ input (pin 14) resistor value for correct adjustment; see Fig.1						
	input sensitivity		–	1.75	–	kHz/mV
$I_{I(max)}$	maximum input current		–	–	100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FLT output (pin 16)						
V_{DCL}	limited DC LOW level output voltage	I_O = 200 µA	–	0.27	–	V
V_{DCH}	limited DC HIGH level output voltage	I_I = 200 µA	–	1.8	–	V
V_{DC}	DC level output voltage		tbf	0.86	tbf	V
Y+SYNC output (pin 25)						
R_O	output resistance		–	–	40	Ω
$I_{sink(max)}$	maximum sink current		200	–	–	µA
$I_{source(max)}$	maximum source current		1	–	–	mA
V_{BL}	black level output voltage		–	1.6	–	V
V_{SYNC}	sync voltage amplitude		570	600	630	mV
V_Y	Y voltage amplitude		1330	1400	1470	mV
B	bandwidth frequency response	R_L = 10 kΩ; C_L = 10 pF	10	–	–	MHz
t_d	group delay time tolerance	R_L = 10 kΩ; C_L = 10 pF	–	–	20	ns
t_d	sync delay time from pin 29 to pin 25		220	290	360	ns
t_d	Y delay time from pin 5 to pin 25		–	10	–	ns
Y+SYNC input (pin 23; note 2)						
I_{bias}	input bias current		–	–	1	µA
$V_{I(max)}$	maximum Y voltage amplitude		–	–	1	V
NOTCH output (pin 22)						
R_O	output resistance		1750	2000	2250	Ω
V_{DC}	DC output voltage level		–	V_{23}	–	V
$I_{sink(max)}$	maximum sink current		300	–	–	µA
CHROMA output (pin 18)						
$I_{sink(max)}$	maximum sink current		200	–	–	µA
$I_{source(max)}$	maximum source current		1	–	–	mA
V_{DC}	DC voltage level		–	2.5	–	V
ΔV_{DC}	variation of DC voltage level	chrominance signal blanked	–	5	–	mV
		chrominance signal not blanked	–	5	–	mV
R_O	output resistance		–	120	–	Ω
$V_{O(p-p)}$	chrominance output voltage amplitude (peak-to-peak value)	f = 4.25 MHz	–	165	–	mV
		f = 4.406 MHz	–	205	–	mV

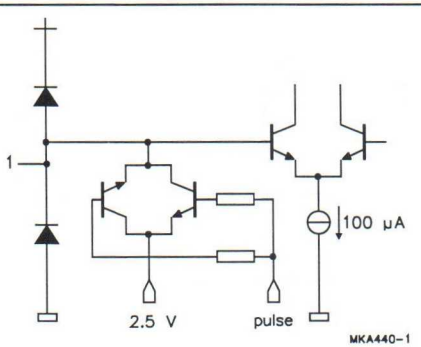
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FREQUENCY OF CHROMINANCE SIGNAL (NOTE 3)						
f_{OR}	black level of D'R		–	4406	–	kHz
f_{OB}	black level of D'B		–	4250	–	kHz
f_{max}	maximum frequency		4721	4756	4791	kHz
f_{min}	minimum frequency		3865	3900	3935	kHz
ΔD'R	deviation of D'R	EBU bar of 75%	252	280	308	kHz
ΔD'B	deviation of D'B	EBU bar of 75%	207	230	253	kHz
CVBS output (pin 21)						
$I_{sink(max)}$	maximum sink current		250	–	–	µA
$I_{source(max)}$	maximum source current		1	–	–	mA
V_{black}	black level voltage		–	1.6	–	V
G_Y	gain Y+SYNC (pin 23 to pin 21)		–	6	–	dB
G_{CHR}	gain CHROMA (pin 18 to pin 21)		–	6	–	dB
R_O	output resistance		–	120	–	Ω
LPFDR output (pin 13)						
V_O	DC control voltage level		tbf	2.4	tbf	V
	control sensitivity		–	0.2	–	kHz/mV
I_{LO}	output leakage current		–	–	50	nA
LPFDB output (pin 15)						
V_O	DC control voltage level		tbf	2.1	tbf	V
	control sensitivity		–	1.5	–	kHz/mV
I_{LO}	output leakage current		–	–	50	nA
LPF4.4 output (pin 24)						
V_O	DC control voltage level		tbf	2.3	tbf	V
	control sensitivity		–	1.5	–	kHz/mV
I_{LO}	output leakage current		–	–	100	nA
LPF4.25 output (pin 31; C_{ext} = 270 pF)						
V_O	DC control voltage level		tbf	2.3	tbf	V
	control sensitivity		–	5.3	–	kHz/mV
I_{LO}	output leakage current		–	–	100	nA
VCO4.25 (pin 27; note 4)						
CS input (pin 29)						
$V_{I(p-p)}$	sync pulse input amplitude (peak-to-peak value)		75	300	600	mV
	slicing level		–	50	–	%
I_I	input current		–	4	–	µA
$I_{O(max)}$	maximum output current	during sync	–	100	–	µA

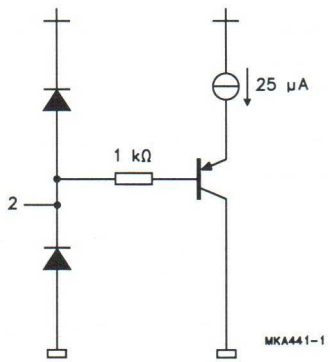
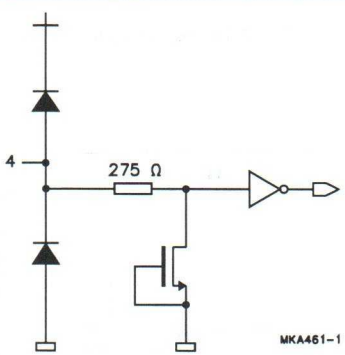
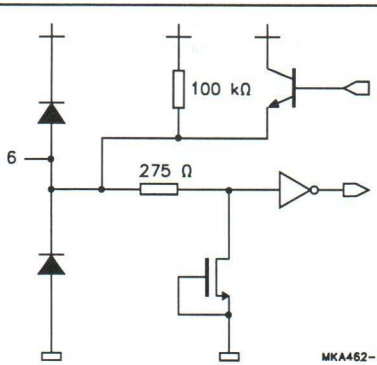
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ext} (pin 19)						
I_{ext}	external supply current		–	–	1.5	mA
SAND output (pin 20; V_{ext} = 13.2 V); see Fig.8						
$I_{sink(max)}$	maximum sink current		100	–	–	µA
$I_{source(max)}$	maximum source current		100	–	–	µA
V_{TL}	top voltage level	V_{ext} < 10 V	V_{ext} – 0.1	–	–	V
		V_{ext} > 10 V	10	–	–	V

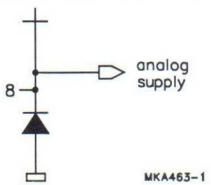
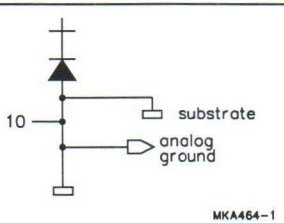
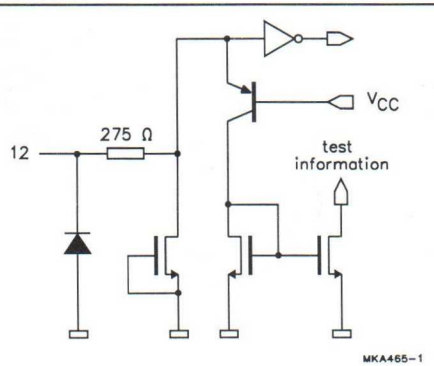
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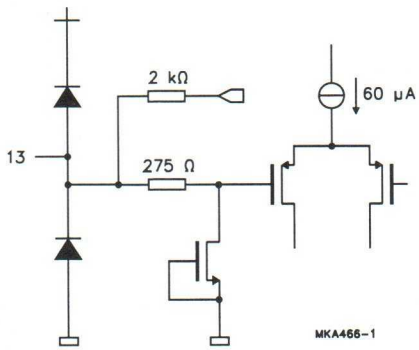
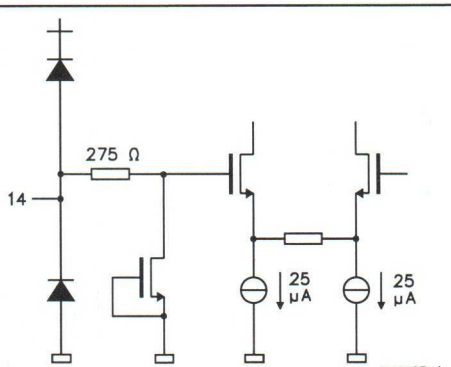
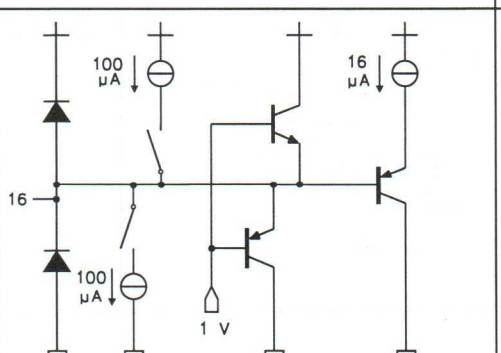
1. The threshold level of pin 2 is 700 ± 20 mV. The specification of the HIGH and LOW levels is in accordance with the scart fast blanking.
2. The black level of input signal must be 2 V; amplitude 1 V (peak-to-peak value) nominal (Y = 700 mV, SYNC = 300 mV).
3. The tolerances of f_{OR} and f_{OB} are with the printed-circuit board <±5 kHz. This value can be influenced by the print layout.
4. The oscillator operates in series-resonance. The resonance resistance of the crystal must be <60 Ω and parallel capacitance of the crystal <10 pF.

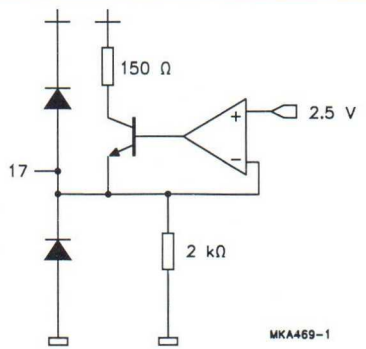
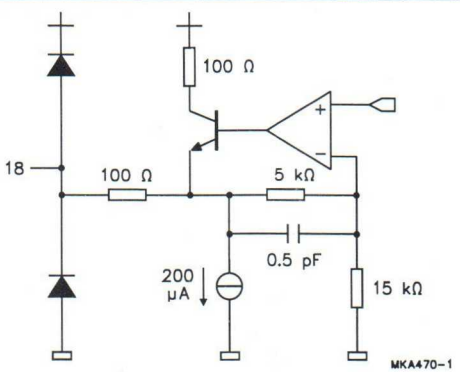
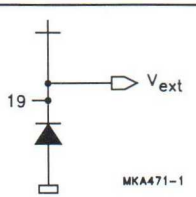
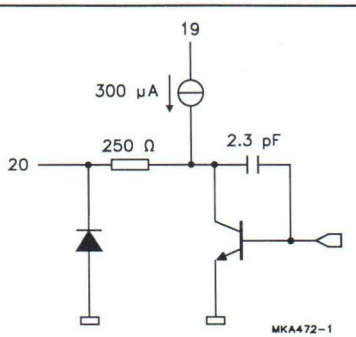
INTERNAL CIRCUITRY

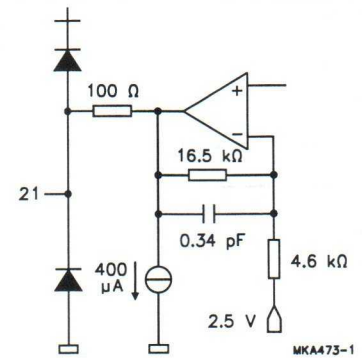
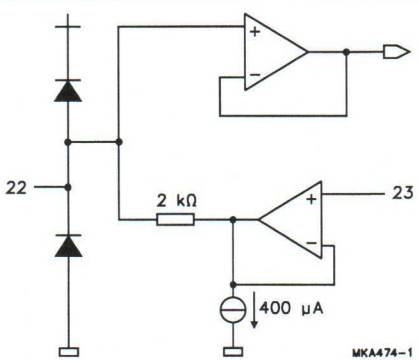
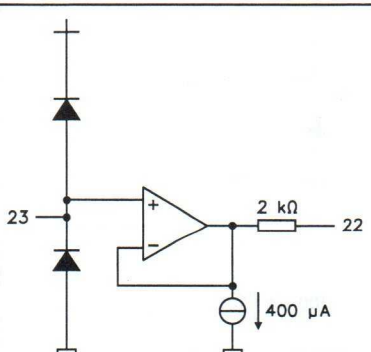
PIN	NAME	CIRCUIT	DESCRIPTION
1	–(R–Y)		–(R–Y) input; connected via 47 nF capacitor; 1.05 V (peak-to-peak value) for EBU bar of 75%; see also pins 3, 5, 7, 9 and 11

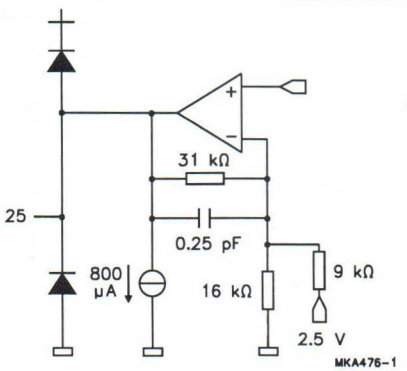
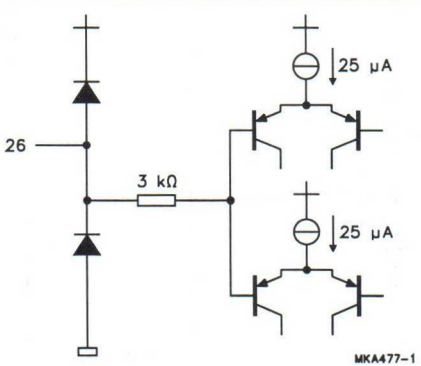
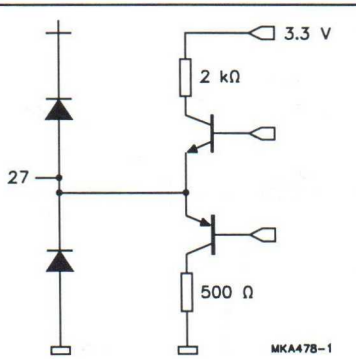
PIN	NAME	CIRCUIT	DESCRIPTION
2	MCONTR		multiplexer control input: <0.4 V Y, U and V >1 V R, G and B
3	–(B–Y)	see pin 1	–(B–Y) input; connected via 47 nF capacitor; 1.33 V (peak-to-peak value) for EBU bar of 75%
4	FH/2		FH/2 input; forcing possibility; when not used this pin is connected to ground
5	Y	see pin 1	Y input; connected via 47 nF capacitor; 1 V (peak-to-peak value) for EBU bar of 75%
6	TEST		test pin; connected to V_{CC} or left open-circuit

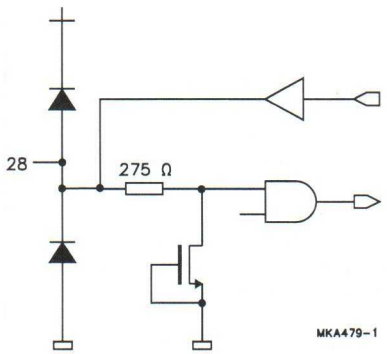
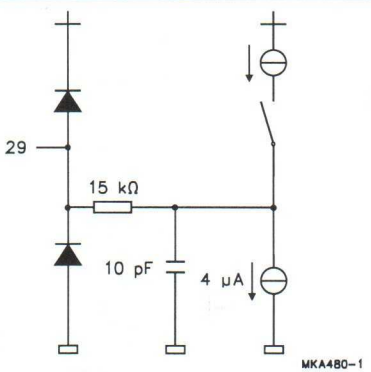
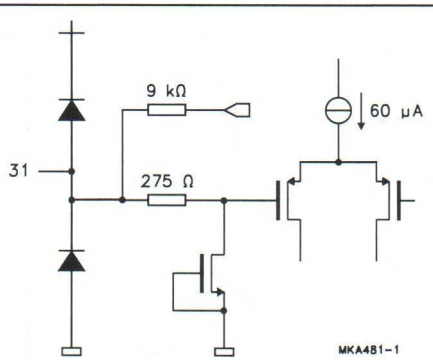
PIN	NAME	CIRCUIT	DESCRIPTION
7	R	see pin 1	RED input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75%
8	V_{DDA}		analog supply voltage for encoder part; 5 V nominal
9	G	see pin 1	GREEN input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75%
10	V_{SSA}		analog ground
11	B	see pin 1	BLUE input; connected via 47 nF capacitor; 0.7 V (peak-to-peak value) for EBU bar of 75%
12	Y/Y+SYNC		control pin: 0 V Y without sync supplied to pin 5 5 V Y with sync supplied to pin 5

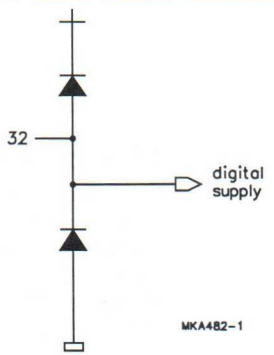
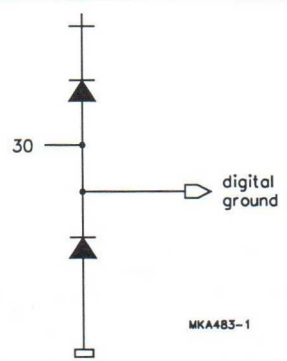
PIN	NAME	CIRCUIT	DESCRIPTION
13	LPFDR		modulator control loop filter with low leakage capacitors
14	FADJ		adjustment pin for 4.286 MHz: potentiometer in series with two resistors between ground and pin 17
15	LPFDB	see pin 13	modulator control loop filter with low leakage capacitors
16	FLT		filter control pin; 220 nF capacitor to ground

PIN	NAME	CIRCUIT	DESCRIPTION
17	V_{ref}		2.5 V reference voltage decoupling with 47 µF and 22 nF capacitors
18	CHROMA		chrominance output
19	V_{ext}		pin for external power supply, for sandcastle pulse; V_{ext} > 8 V; if not used, the pin should be connected to ground
20	SAND		sandcastle pulse

PIN	NAME	CIRCUIT	DESCRIPTION
21	CVBS		composite SECAM output
22	NOTCH		pin for external notch filter
23	Y+SYNC IN		input of the delayed Y+SYNC signal of the delay line; black level must be 2 V
24	LPF4.4	see pin 13	loop filter for 4.40625 MHz reference oscillator

PIN	NAME	CIRCUIT	DESCRIPTION
25	Y+SYNC OUT		output of the delayed Y+SYNC signal, connected to the delay line via a resistor
26	XTAL/PLL VIDENT		control pin: **without** vertical identification: 0 V PLL tuning 5 V crystal tuning **with** vertical identification: 2.5 V PLL tuning
27	VCO4.25		tuning of 4.25 MHz oscillator: PLL tuning: C = 270 pF to ground crystal tuning: crystal in series with a capacitor to ground external tuning: signal via 1 nF capacitor in series with a resistor

PIN	NAME	CIRCUIT	DESCRIPTION
28	COLKIL		colour killing input: 0 V not active 5 V active, internal D'R and D'B are blanked
29	CS		composite sync signal input; amplitude <600 mV (peak-to-peak value)
30	V_{SSD}		digital ground

PIN	NAME	CIRCUIT	DESCRIPTION
31	LPF4.25		loop filter for 4.25 MHz reference oscillator; connected to pin 17 if crystal or external tuning
32	V_{DDD}		supply voltage digital part; 5 V nominal

4 × 4 video switch matrix

TDA8540

FEATURES

- I²C-bus or non-I²C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Slave receiver in the I²C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.

GENERAL DESCRIPTION

The TDA8540 has been designed for switching between composite video signals, therefore the minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, to enable parallel connection of several devices.

APPLICATIONS

- Colour Television (CTV) receivers
- Peritelevision sets
- Satellite receivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	20	30	mA
I_{SO}	isolation 'OFF' state	at f = 5 MHz	60	80	–	dB
B	3 dB bandwidth		12	–	–	MHz
α_{ct}	crosstalk attenuation between channels		60	70	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8540	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA8540T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

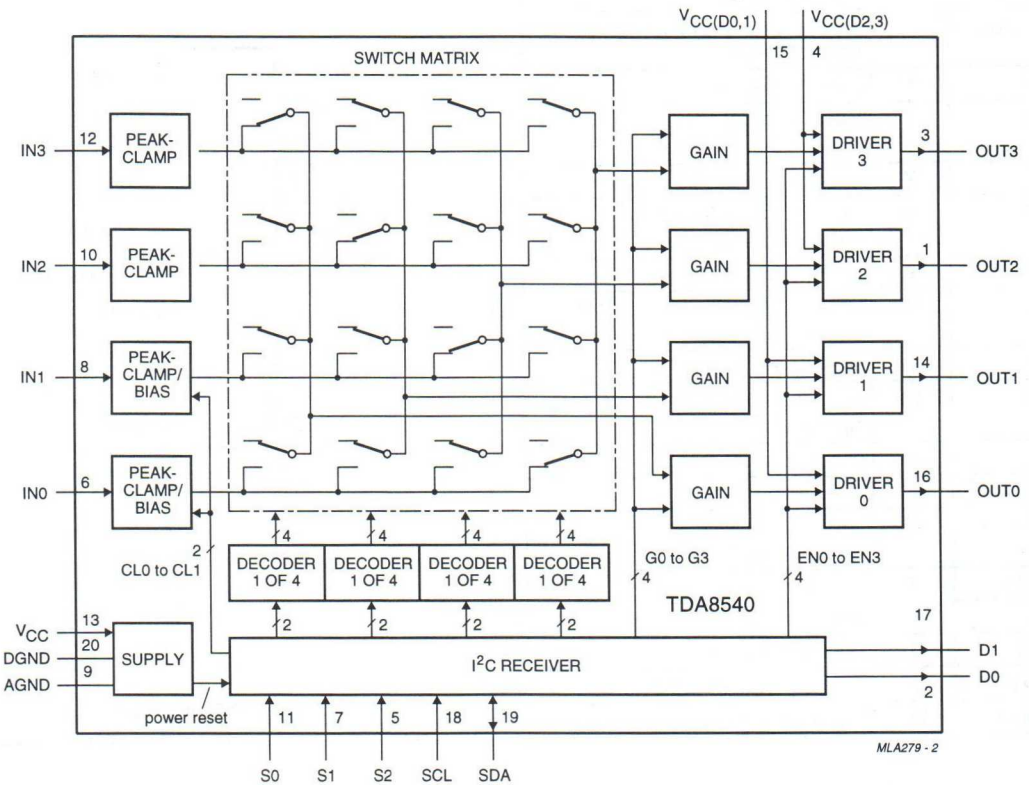


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT2	1	video output 2
D0	2	control output 0
OUT3	3	video output 3
$V_{CC(D2,3)}$	4	driver supply voltage; for drivers 2 and 3
S2	5	sub-address input 2
IN0	6	video input 0 (CVBS or chrominance signal)
S1	7	sub-address input 1
IN1	8	video input 1 (CVBS or chrominance signal)
AGND	9	analog ground
IN2	10	video input 2 (CVBS or luminance signal)
S0	11	sub-address input 0
IN3	12	video input 3 (CVBS or luminance signal)
V_{CC}	13	general supply voltage
OUT1	14	video output 1
$V_{CC(D0,1)}$	15	driver supply voltage; for drivers 0 and 1
OUT0	16	video output 0
D1	17	control output 1
SCL	18	serial clock input
SDA	19	serial data input/output
DGND	20	digital ground

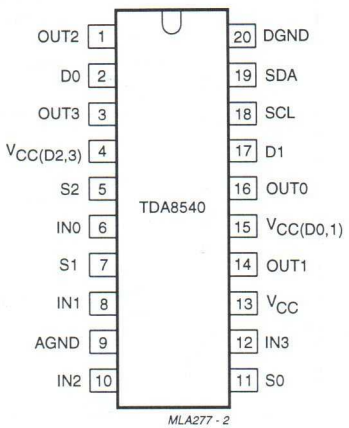


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus. 3 bits of the I²C address can be selected via the address pin, thus providing a facility for parallel connection of 7 devices.

Control options via the I²C-bus:

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 1× or 2×.
- Each of the four outputs can individually be connected to one of the four inputs.
- Each output can individually be set in a high impedance state.
- Two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18) can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses or switching to the non-I²C mode. Inputs S0 to S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

Table 1 I²C-bus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	A0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0 and D1 are at a LOW level.

Detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

The TDA8540 is a **slave receiver** and the protocol is given in Table 2.

Table 2 The TDA8540 protocol

SEQUENCE									
S[1]	SLV[2]	A[3]	SUB	A[3]	DATA	A[3]	DATA	A[3]	P[4]

Notes

1. S = START condition.
2. Data transmission to the TDA8540 starts with the slave address (SLV).
3. A = acknowledge bit, generated by TDA8540.
4. P = STOP condition.

Table 3 Data transmission to the TDA8540 begins with SLV

A6 MSB	A5	A4	A3	A2	A1	A0	R/$\overline{W}$ LSB
1	0	0	1	A2[1]	A1[1]	A0[1]	0[2]

Notes

1. A2 to A0: pin programmable slave address bits.
2. R/$\overline{W}$ = 0; write only.

After the SLV, a second byte, SUB, is required for selecting the functions, as shown in Table 4.

Table 4 The second byte: SUB

7 MSB	6	5	4	3	2	1	0 LSB
0	0	0	0	0	0	RS1	RS0

Options for SUB:

If SUB = 00H: access to switch control (SW1)

If SUB = 01H: access to gain/clamp/data control (GCO)

If SUB = 02H: access to output enable control (OEN).

Remarks:

If more than one data byte is sent, the SUB byte will be automatically incremented.

If more than 3 data bytes are sent, the internal counter will roll over and the device will then rewrite the first register.

Data Bytes

SWI (SUB = 00H): selects which input is connected to the different outputs, as shown in Table 5.

Table 5 SWI (SUB = 00H) selection of inputs connected to outputs

7 MSB	6	5	4	3	2	1	0 LSB
S31	S30	S21	S20	S11	S10	S01	S00

Table 6 Selection of inputs

OUTPUT	Sj1 AND Sj0[1]			
	00	01	10	11
OUTj	IN0	IN1	IN2	IN3

Note

1. For j = 0 to 3.
   Example: if S21 = 0 and S20 = 1, then OUT2 is connected to IN1.

GCO (SUB = 01H):

- Selects the gain of each output.
- Selects the clamp action or mean value on inputs 0 and 1.
- Determines the value of the auxiliary outputs D1 and D0.

Table 7 GCO byte

7 MSB	6	5	4	3	2	1	0 LSB
G3[1]	G2[1]	G1[1]	G0[1]	CL1[2]	CL0[2]	D1[3]	D0[3]

Notes

1. For j = 0 to 3: if Gj = 0 (1), then output j has a gain of 2 (1).
2. If CL0 (CL1) = 0, then input signal on IN0 (IN1) is clamped.
3. For j = 0 or 1: if Dj = 0 (1), then logical output j is LOW (HIGH).

OEN (SUB = 02H): selects, for each output, if the output is active or high impedance, see Table 8.

Table 8 OEN (SUB = 02H) determines which output is active or high impedance

7 MSB	6	5	4	3	2	1	0 LSB
X[1]	X[1]	X[1]	X[1]	EN3[2]	EN2[2]	EN1[2]	EN0[2]

Notes

1. X = don't care.
2. For j = 0 to 3: if ENj = 0 (1), then OUT j is high impedance (active).

After a power-on reset:

- The outputs are set to a high impedance state; the outputs are connected to IN0; the gains are set at two and inputs IN0 and IN1 are clamped.
- Programming of the device is necessary because the outputs are in high impedance state.

Non-I²C-bus control

If the S0, S1 and S2 pins are all connected to V_{CC} the device will enter the non-I²C-bus mode.

After a power-on reset:

- Gain is set at two for all outputs.
- All inputs are clamped.
- All outputs are active.
- The matrix position is given by the SDA and SCL voltage level.

Table 9 Non-I²C-bus control

OUTPUT	SCL AND SDA			
	00	01	10	11
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

SCL and SDA act as normal input pins:

SCL interchanges (OUT3 and OUT2) with (OUT1 and OUT0).

SDA interchanges OUT3 with OUT2 and OUT1 with OUT0.

Remark: For use with chrominance signals, the clamp action must be overruled by external bias.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (pin 13)		−0.3	+9.1	V
P_{tot}	total power dissipation		–	750	mW
$V_{CC(D0,1)}$, $V_{CC(D2,3)}$	driver supply voltage		−0.3	+13.8	V
IN0 to IN3	video input voltage		−0.3	+7.2	V
OUT0 to OUT3	video output voltage		−0.3	+7.2	V
D0, D1	control output voltage		−0.3	+7.2	V
SDA, SDL	I^2C input/output voltage		−0.3	+8.8	V
S0 to S2	sub-address input voltage		−0.3	+8.8	V
T_{stg}	IC storage temperature		−55	+125	°C
T_j	junction temperature		–	+150	°C
V_{es}	electrostatic handling	HBM; note 1	−1500	+1500	V
		MM; note 2	−200	+200	V

Notes

1. Human Body Model (HBM): in accordance with UZW-BO/FQ-A302.
2. Machine Model (MM): in accordance with UZW-BO/FQ-B302 (stress reference pins: AGND and DGND short-circuited and V_{CC}).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT146-1	60 (typ.)	K/W
	SOT163-1	85 (typ.)	K/W

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage (pin 13)		7.2	–	8.8	V
T_{amb}	operating ambient temperature		0	–	70	°C
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		–	100	–	nF
$V_{I(p\text{-}p)}$	C signal amplitude (peak-to-peak value)	note 1	–	–	1	V
$V_{I(p\text{-}p)}$	CVBS or Y-signal amplitude (peak-to-peak value)	note 2	–	–	1.5	V
Video drivers (pins 4 and 15)						
R_D	external collector resistor	note 3	–	25	–	Ω
C_D	external decoupling capacitor	note 4	–	22	–	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-address S0, S1 and S2 (pins 5, 7 and 11)						
V_{IH}	HIGH level input voltage		4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	1	V

Notes

1. Only for pins 6 and 8 when clamp action is not selected for these pins.
2. On all the video input pins, when non-I²C-bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C-bus control).
3. Connected between V_{CC} and pin 4 or pin 15.
4. Connected between AGND and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C-bus; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current	without load	–	20	30	mA
		OFF state	–	12	–	mA
Video inputs: IN0 to IN3 when the clamp is active (see Figs 3 and 4)						
I_{LI}	input leakage current	V_I = 3 V	–	0.4	1	µA
V_{clamp}	input clamping voltage	I_I = 5 µA	–	2.2	–	V
I_{clamp}	input clamping current	V_I = 0 V	1.2	–	–	mA
Video inputs: IN0 and IN2 when the clamp is not active (see Fig.3)						
V_{bias}	DC input bias level	I_I = 0	–	2.9	–	V
R_I	input resistance		–	10	–	kΩ
Video outputs: OUT0 to OUT3 (see Fig.5)						
Z_O	output impedance	OFF state	100	–	–	kΩ
R_O	output resistance		–	5	–	Ω
ISO	isolation	OFF state; f = 5 MHz	60	–	–	dB
V_O	output top sync level; (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2; load = 150 Ω	1.5	1.9	2.2	V
		G = 1; without load	1	1.3	1.6	V
G_v	voltage gain	G = 1; f = 1 MHz	−1	0	+1	dB
		G = 2; f = 1 MHz	5	6	7	dB
G_{diff}	differential gain	note 1	–	0.5	3	%
φ_{diff}	differential phase	note 1	–	0.6	–	deg
NL	non linearity	note 2	–	0.5	2	%
α_{ct}	crosstalk attenuation between channels	note 3	60	70	–	dB
SVRR	supply voltage rejection	note 4	36	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG	maximum gain variation	100 kHz < f < 5 MHz	–	0.5	–	dB
		100 kHz < f < 8.5 MHz	–	1	–	dB
		100 kHz < f < 12 MHz	–	3	–	dB
α_{ct}	crosstalk attenuation of I²C-bus signals		60	–	–	dB
Auxiliary outputs D0 and D1 (open collector)						
I_{OH}	HIGH level output current	V_{OH} = 5.5 V	–	–	10	µA
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.4	V
I²C-bus inputs SCL and SDA						
I_{IH}	HIGH level input current	V_{IH} = 3.0 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 1.5 V	−10	–	–	µA
C_i	input capacitance		–	–	10	pF
I²C-bus output SDA						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Sub-address S0, S1 and S2						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC}$	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	10	µA

Notes

1. Gain set at 2; R_L = 150 Ω; test signal D2 from CCIR 330.
2. Gain set at 2; R_L = 150 Ω; test signal D1 from CCIR 17.
3. Measured from any selected input to output; f = 5 MHz; R_L = 150 Ω; gain set at 2; V_I = 1.5 V (peak-to-peak value). This measurement requires an optimized board.
4. Supply voltage ripple rejection: $20 \log \frac{V_{ripple\ (supply)}}{V_{ripple\ (on\ output)}}$;
   measured at f = 1 kHz with $V_{ripple\ (supply\ max)}$ = 100 mV (peak-to-peak value).
   The supply voltage rejection ratio is >36 dB at f_{max} = 100 kHz.

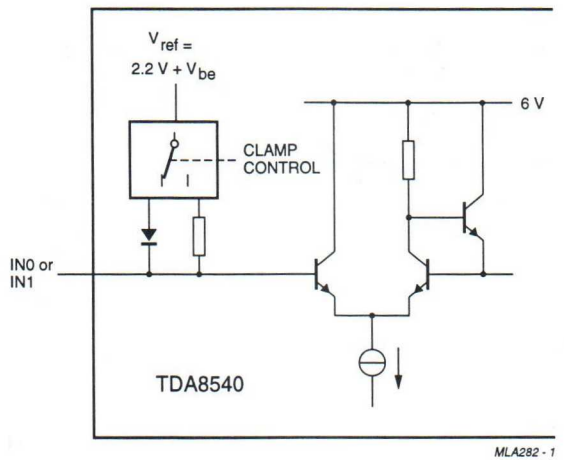


Fig.3 IN0 and IN1 inputs.

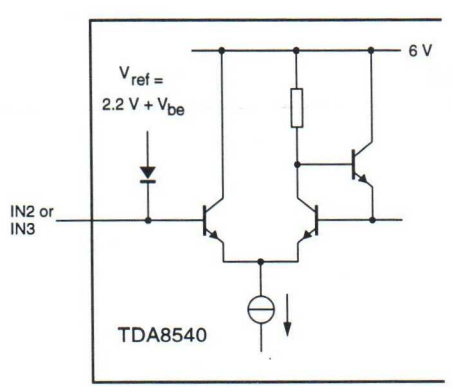


Fig.4 IN2 and IN3 inputs.

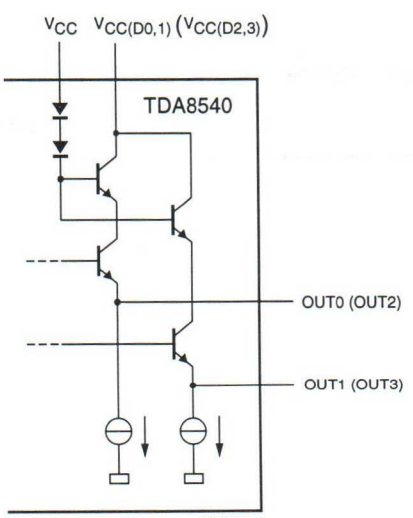
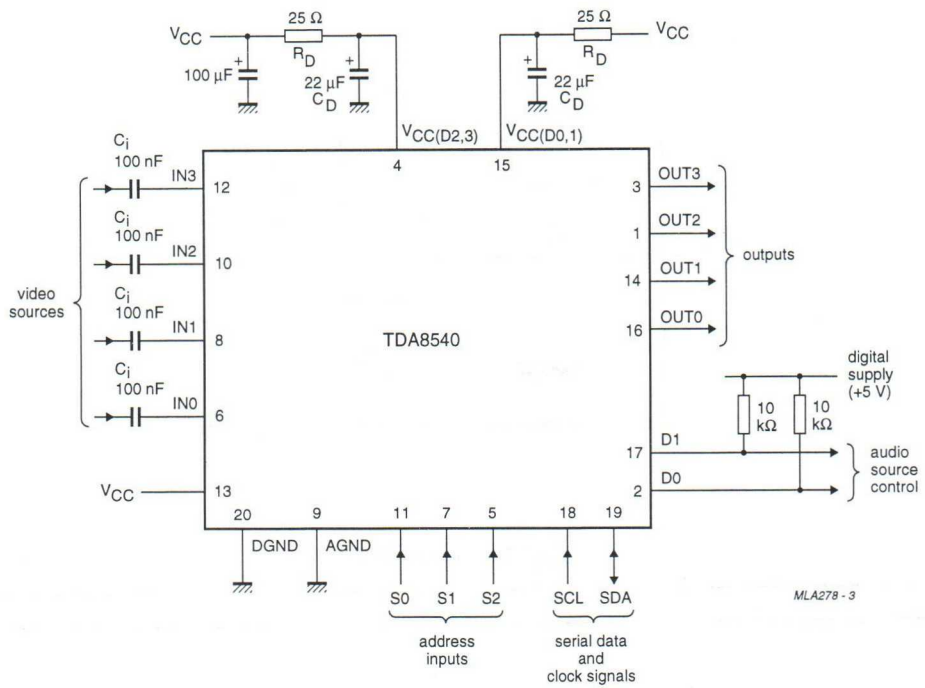


Fig.5 Driver output stage.

APPLICATION INFORMATION



V_{CC} = analog supply (+8 V).

Fig.6 Application diagram.

RGB/YUV and fast blanking switch TDA8601

FEATURES

- YUV/RGB and fast blanking switch
- 3-state output
- Selectable clamp, passive (with diodes) or active clamp
- Bandwidth greater than 22 MHz
- Fully ESD protected
- Latch-up free.

APPLICATIONS

- Standard and high definition television sets
- Peri-television sets.

GENERAL DESCRIPTION

The device is intended for switching between two RGB or YUV video sources. The outputs can be set to high-impedance state to enable parallel connection of several devices.

A HIGH level on SEL (pin 5) selects the video inputs of Channel 2. The IOCNTR control pin (pin 16) defines the 3-state outputs and clamp inputs:

- HIGH = 3-state outputs (also for test; active clamp)
- LOW = passive clamp at the video inputs (diode)
- Sandcastle = active clamp at the video inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
G_v	voltage gain		–0.5	0	0.5	dB
B	3 dB bandwidth		22	–	–	MHz
α_{ct}	crosstalk attenuation between two video channels	f_i = 5 MHz	–60	–	–	dB
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8601	16	DIP16	plastic	SOT38-1
TDA8601T	16	SO16	plastic	SOT109-1

BLOCK DIAGRAM

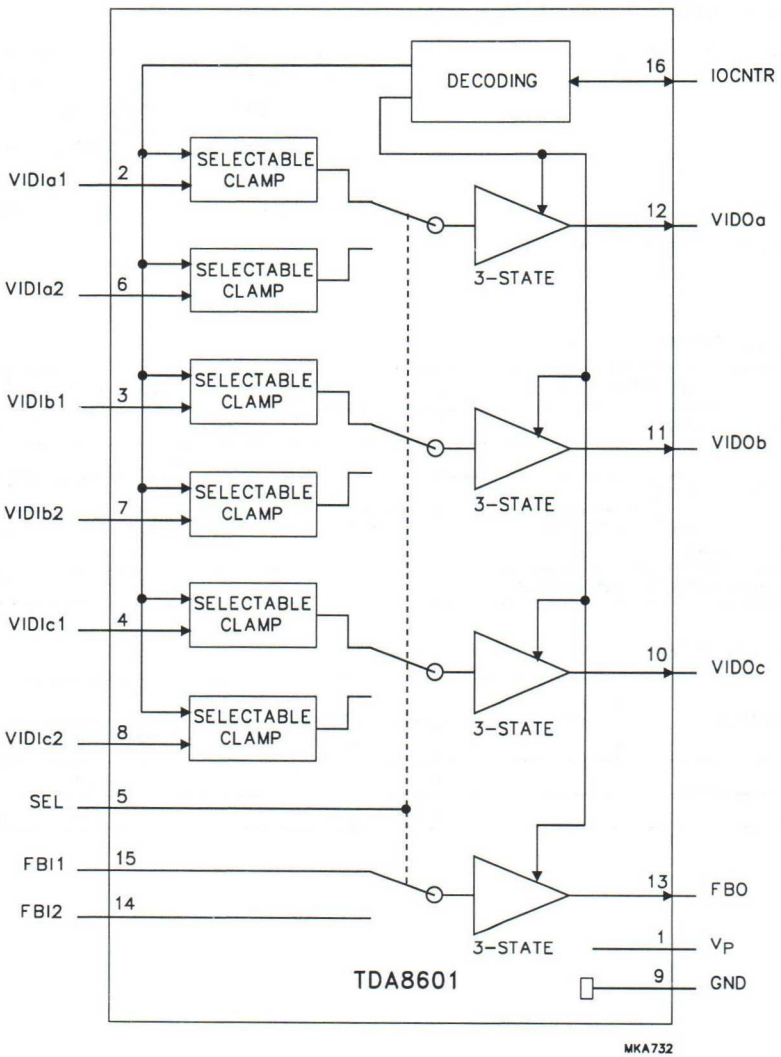


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage (8 V)
VIDIa1	2	video input a (channel 1)
VIDIb1	3	video input b (channel 1)
VIDIc1	4	video input c (channel 1)
SEL	5	channel selection
VIDIa2	6	video input a (channel 2)
VIDIb2	7	video input b (channel 2)
VIDIc2	8	video input c (channel 2)
GND	9	ground
VIDOc	10	video output c
VIDOb	11	video output b
VIDOa	12	video output a
FBO	13	fast blanking output signal
FBI2	14	fast blanking input signal (channel 2)
FBI1	15	fast blanking input signal (channel 1)
IOCNTR	16	video input/output control

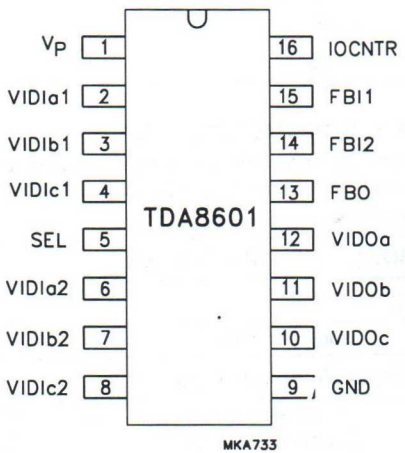


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+12	V
V_i	input voltage (pins 2 to 4 and 6 to 8) referenced to ground	0	8.8	V
T_j	junction temperature	–	125	°C
T_{stg}	storage temperature	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD in accordance with *"MIL STD 883C" - "Method 3015"*:

1. Human body model: 1500 Ω, 100 pF, 3 pulses positive and 3 pulses negative on each pin with respect to ground. Class 2: 2000 to 3999 V.
2. Machine model: 0 Ω, 200 pF, 3 pulses positive and 3 pulses negative on each pin with respect to ground. The IC withstands 200 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP16	70	K/W
	SO16	115	K/W

OPERATING CHARACTERISTICS

The operating characteristics are the conditions within the IC when it is functional; these conditions can have any value. For example, condition V_{IL} (pin 5) is fixed at 0.5 V. The IC will then operate over the full temperature range and supply voltage range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		7.2	8.0	8.8	V
Video inputs (pins 1 to 3 and 6 to 8)						
$V_{i(p\text{-}p)}$	input video signal amplitude (peak-to-peak value)	R, G, B signals	–	0.7	1	V
		Y signal; active clamp	–	1	1.4	V
		–(B – Y) signal; active clamp	–	1.05	1.5	V
		–(R – Y) signal; active clamp	–	1.33	1.9	V
C_i	input clamp capacitor		–	47	–	nF
Control inputs (pins 5 and 16)						
V_{IH}	HIGH level input voltage (pin 5)	I_{IH} = 10 µA	0.9	–	V_P	V
V_{IL}	LOW level input voltage (pin 5)	I_{IL} = –10 µA	–	–	0.5	V
V_{IH}	HIGH level input voltage (pin 16)	I_{IH} = 10 µA	2.0	–	V_P	V
V_{IL}	LOW level input voltage (pin 16)	I_{IL} = –10 µA	–	–	0.8	V
V_{sc}	sandcastle input voltage level (pin 16)	zero level	–	–	1.1	V
		blanking level	2.0	–	3.1	V
		clamp level	3.9	–	5.5	V
t_W	clamp pulse width	SECAM mode	–	3.6	–	µs
		PAL mode	–	2.5	–	µs
Fast blanking inputs (pins 14 and 15)						
V_{IH}	HIGH level input voltage		0.9	–	V_P	V
V_{IL}	LOW level input voltage		–	–	0.5	V
Video outputs (pins 10 to 12)						
C_L	output load capacitor		–	40	100	pF
R_L	output load resistor	note 1	1	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast blanking output (pin 13)						
C_L	output load capacitor		–	40	100	pF
R_L	output load resistor	note 1	1	–	–	kΩ

Note

1. For the DIP16 package, the thermal resistance is lower. The minimum value for the output load resistor is 270 Ω.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; C_L = 40 pF; no load resistor; measured in Fig.8 over full supply voltage and temperature range; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_P	supply current	no resistive load on the outputs	–	33	40	mA
SVRR	supply voltage rejection ratio	f_i = 40 Hz to 50 kHz; note 1	–	–	–36	dB
		f_i = 40 Hz; note 1	–	–51	–36	dB
Video inputs (pins 1 to 3 and 4 to 6)						
R_i	input resistance	for each type of clamp	10	–	–	kΩ
$C_{i(max)}$	maximum input capacitance		–	3	–	pF
V_{clamp}	input clamping voltage level	I_i = –50 mA; passive clamp	1.05	1.21	1.35	V
		I_i = 50 mA; active clamp	2.05	2.42	2.70	V
		I_i = –50 mA; active clamp	2.05	2.37	2.70	V
I_{sink}	input sink current	V_i = 2 V; passive clamp	0.5	1.6	3	µA
$\|I_{clamp}\|$	maximum absolute input clamping current	$V_i = V_{clamp}$ + 0.5 V; active clamp	200	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video outputs (pins 10 to 12)						
R_o	output resistance		–	–	50	Ω
R_{oZ}	output resistance	3-state output	0.1	–	–	MΩ
$C_{oZ(max)}$	maximum output capacitance	3-state output	–	3	–	pF
G_v	voltage gain	f_i = 1 MHz	−0.5	0	+0.5	dB
B	bandwidth	at ±0.5 dB	5	–	–	MHz
		at ±1 dB	10	–	–	MHz
		at ±3 dB	22	60	–	MHz
α_{ct}	crosstalk attenuation between two video channels	f_i = 5 MHz; note 2	−60	–	–	dB
		f_i = 10 MHz; note 2	−50	–	–	dB
		f_i = 22 MHz; note 2	−40	–	–	dB
α_{off}	isolation of the 3-state configuration	f_i = 5 MHz; note 2	−60	–	–	dB
		f_i = 10 MHz; note 2	−50	–	–	dB
		f_i = 22 MHz; note 2	−40	–	–	dB
SR	slew rate		100	120	–	V/μs
$\lvert\Delta G_m\rvert$	gain matching between two different signals of the same channel	f_i = 5 MHz	–	–	0.5	dB
$V_{o(bl)}$	output blanking level voltage		2.1	2.23	2.7	V
$V_{os(bl)}$	output blanking offset voltage	$V_{i(ch1)}$ = 0.7 V (p-p) (white); $V_{i(ch2)}$ = 0 V (p-p) (black); active clamp; note 3	–	–	5	mV
		$V_{i(ch1)}$ = 0.7 V (p-p) (white); $V_{i(ch2)}$ = 0 V (p-p) (black); active clamp; note 3	–	–	15	mV
$\Delta V_{os(bl)}$	matching of output blanking offset voltage	$V_{i(ch1)}$ = 0.7 V (p-p) (white); $V_{i(ch2)}$ = 0 V (p-p) (black); active clamp; note 3	–	–	5	mV
		$V_{i(ch1)}$ = 0.7 V (p-p) (white); $V_{i(ch2)}$ = 0 V (p-p) (black); active clamp; note 3	–	–	5	mV
Fast blanking inputs (pins 14 and 15)						
Z_i	input impedance		10	–	–	kΩ
Fast blanking output (pin 13)						
V_{OH}	HIGH level output voltage		2	2.35	3	V
V_{OL}	LOW level output voltage		0	0.15	0.3	V
Z_o	output impedance		–	–	50	Ω
SEL input (pin 5)						
Z_i	input impedance		10	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
$t_{dSEL;VID}$	delay time between SEL input and video output	note 4	–	12	20	ns
$t_{dSEL;FBO}$	delay time between SEL input and fast blanking output	note 5	–	15	40	ns
t_{SWVID}	switching time of video output	note 4	–	8.5	15	ns
t_{SWFBO}	switching time of fast blanking output	note 5	–	8.5	15	ns
t_{dFB}	fast blanking level delay between input and output	note 6	–	13	20	ns
t_{dVID}	video delay between input and output	note 7	–	4	20	ns
Δt_{dVID}	delay difference between two video signals at the output	note 7	–	5	10	ns
$\Delta t_{dFB;VID}$	delay difference between fast blanking level and video at the output	note 7	–	5	10	ns

Notes

1. The supply voltage rejection ratio is measured at the video outputs (pins 10 to 12) when a sine wave is applied on the power supply pin (pin 1); where: V_{DC} = 8 V; V_i = 100 mV (p-p). This additional sine wave on the power supply pin is guaranteed not to cause extraneous oscillations on the video control and fast blanking signals.
2. The 6 video inputs will contain the same signal. The source impedance is 50 Ω.
3. The blanking offset is the level difference between the two channels when they are selected separately and, also, on one video output. This value is measured on each video signal.
4. The delay between the SEL input and the video output together with the switching time of the video output is illustrated in Fig.3. The amplitude of the video signal is 1.9 V (p-p) when the clamp is active and 1.0 V (p-p) when the clamp is passive.
5. The delay between the SEL input and fast blanking output together with the switching time of fast blanking output is illustrated in Fig.4.
6. The fast blanking delay between input and output is illustrated in Fig.5.
7. The video delay between input and output and delay differences are illustrated in Fig.6. Inputs 1 and 2 are either fast blanking input plus a video signal or two video signals. The amplitude of the video signal is 0.5 V (p-p). The video signal levels (i1, i2, o1 and o2) are 50% of the video amplitude. The fast blanking signal levels (i1 and o1) are 0.9 V when the signal rises and 0.5 V when the signal falls.

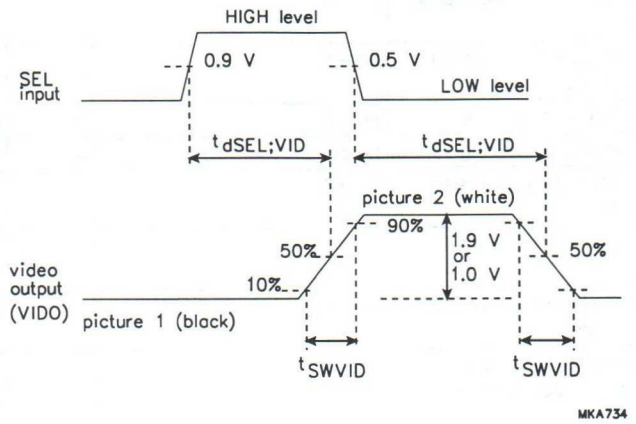


Fig.3 Timing definition: SEL and VIDO.

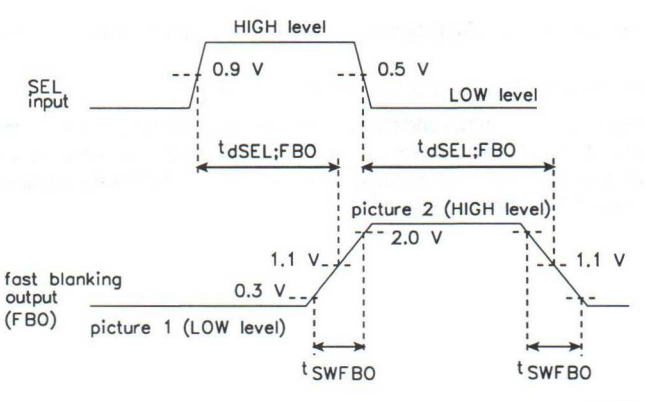


Fig.4 Timing definition: SEL and FBO.

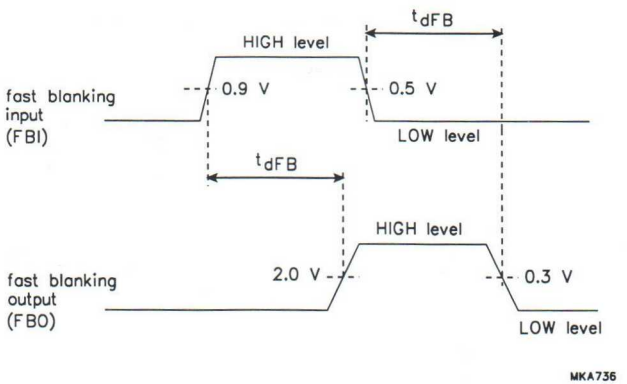


Fig.5 Timing definition: fast blanking delay.

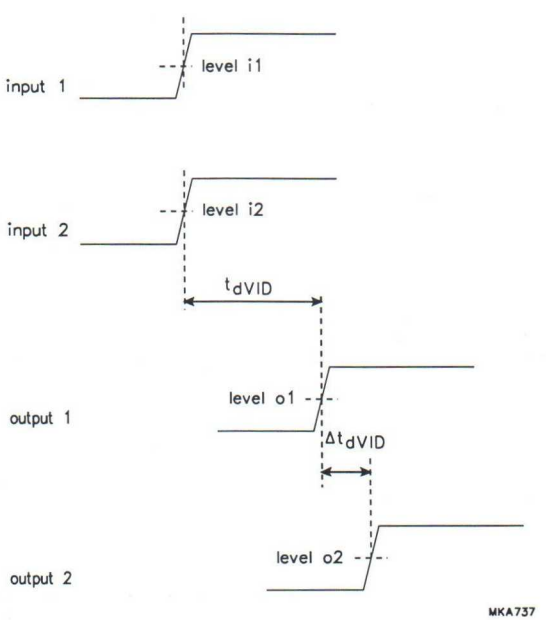


Fig.6 Timing definition: video delay.

INTERNAL PIN CONFIGURATION

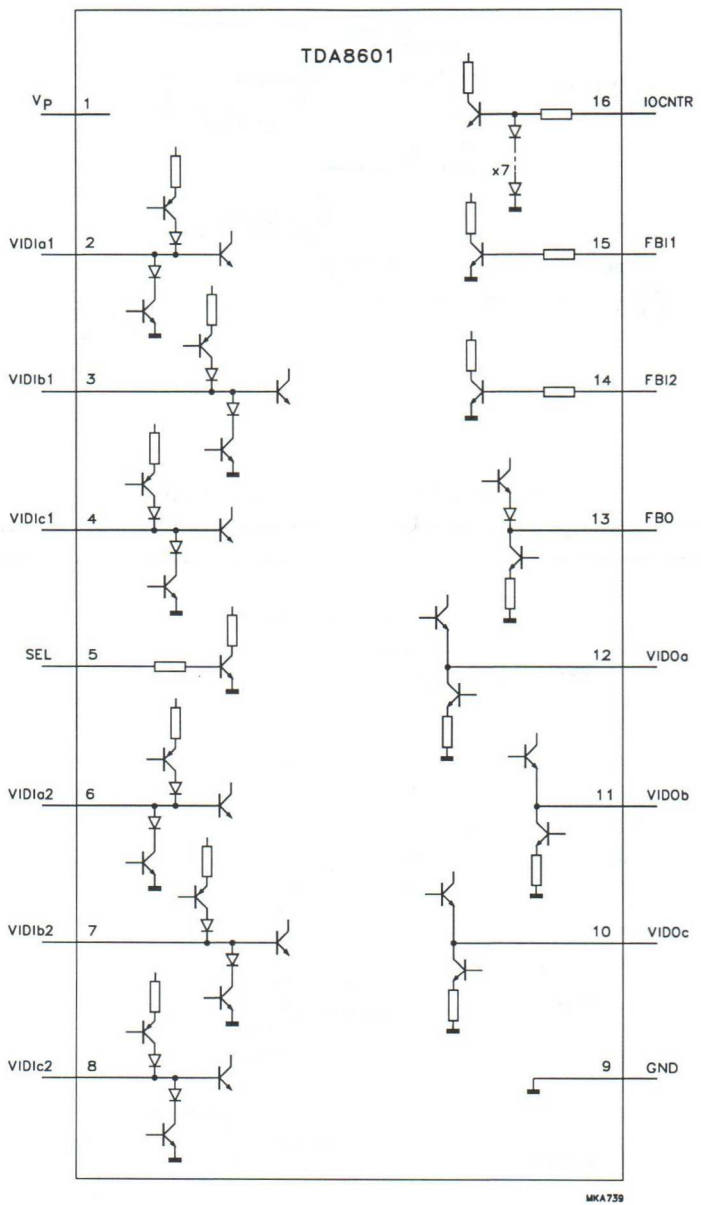


Fig.7 Internal pin configuration.

APPLICATION INFORMATION

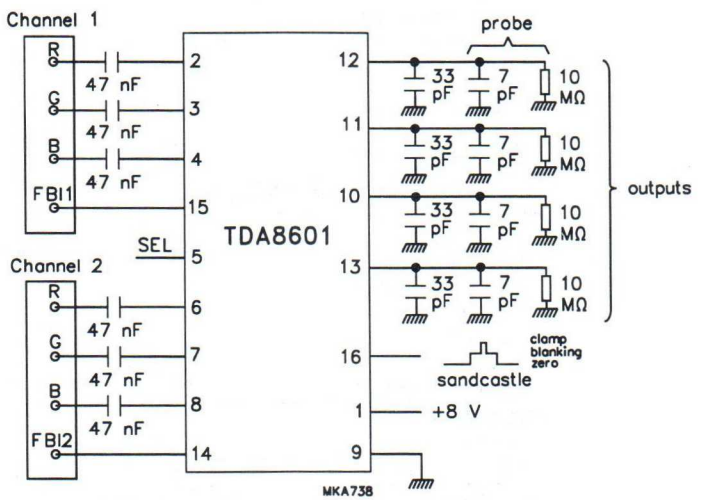


Fig.8 Application diagram.

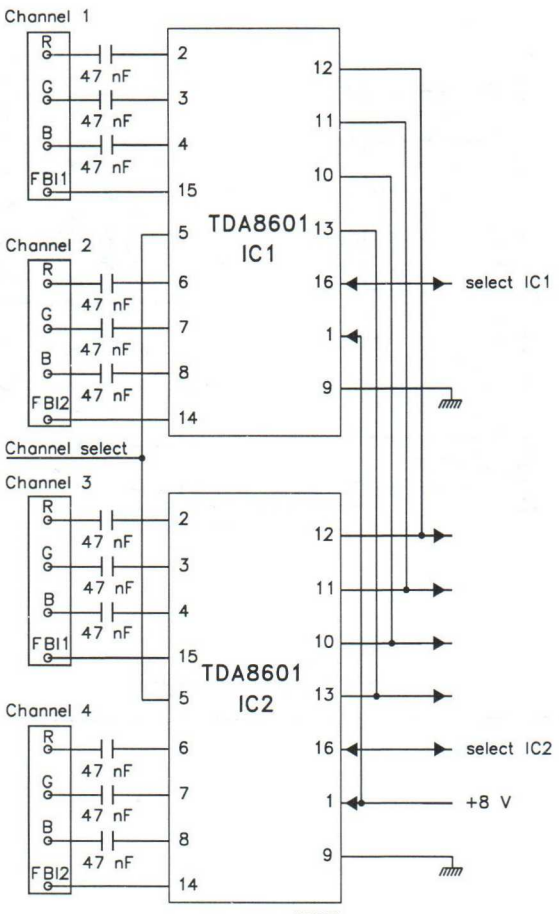


Fig.9 Schematic diagram of two TDA8601s operating four channels.

8-bit video digital-to-analog converter TDA8702

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is an 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 kΩ	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	30	MHz
B	–3 dB analog bandwidth	f_{CLK} = 30 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Notes

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38
TDA8702T	16	SO16	plastic	SOT162A

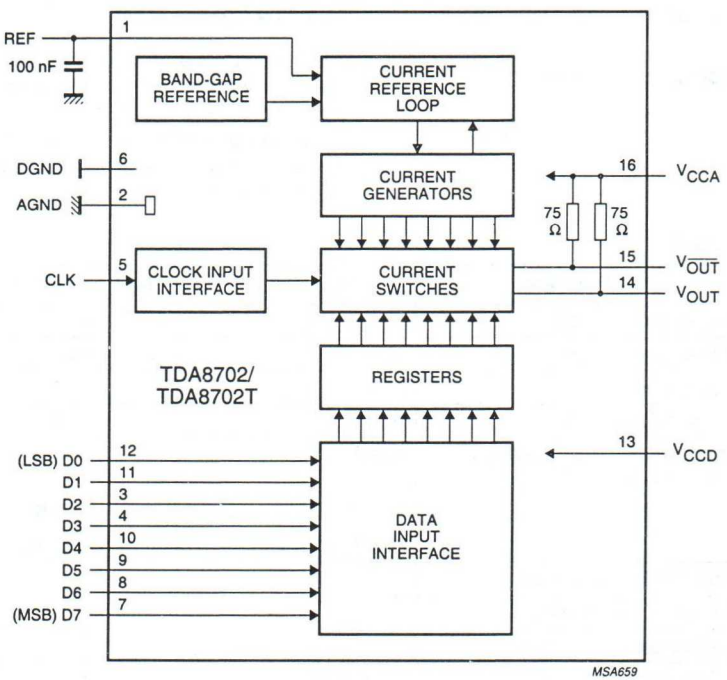


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

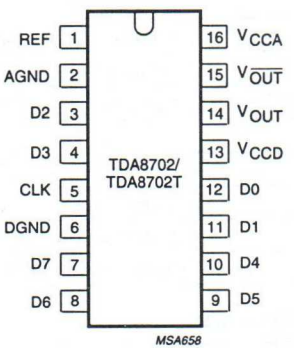


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+0.5	V
AGND − DGND	ground voltage differential	−0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
$I_{OUT}/\overline{I_{OUT}}$	total output current (pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambienttemperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT38	70 K/W
	SOT162A	90 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND – DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	0.01	20	µA
f_{CLK}	maximum clock frequency		–	–	30	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages (peak-to-peak value)	$Z_L = 10$ kΩ	−1.45	−1.60	−1.75	V
		$Z_L = 75$ Ω	−0.72	−0.80	−0.88	V
V_{OS}	analog offset output voltage	code = 0	–	−3	−25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	−3 dB analog bandwidth	note 3; $f_{CLK} = 30$ MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_O	output impedance		–	75	–	Ω
Transfer function ($f_{CLK} = 30$ MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB

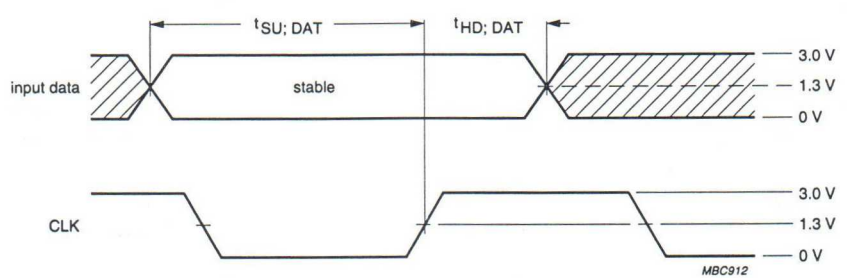
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB.ns

Notes

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V_{OUT}}$	V_{OUT}	$\overline{V_{OUT}}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	.....				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	.....				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

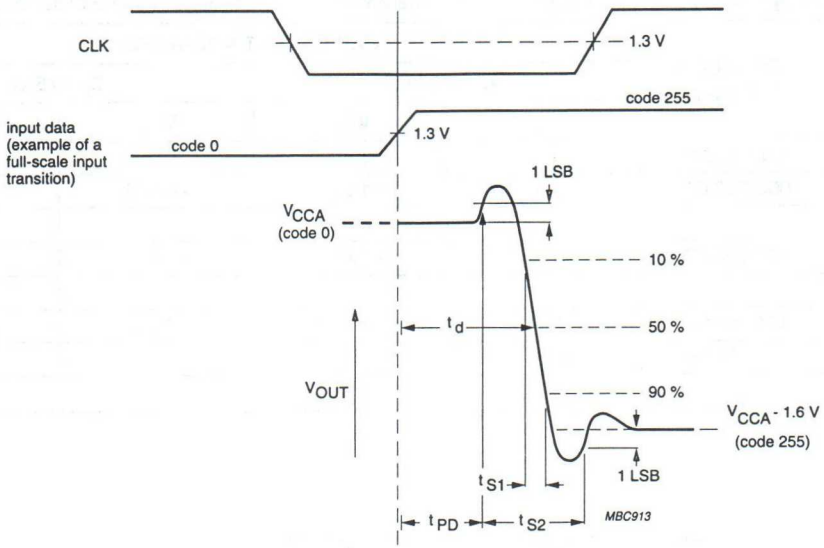
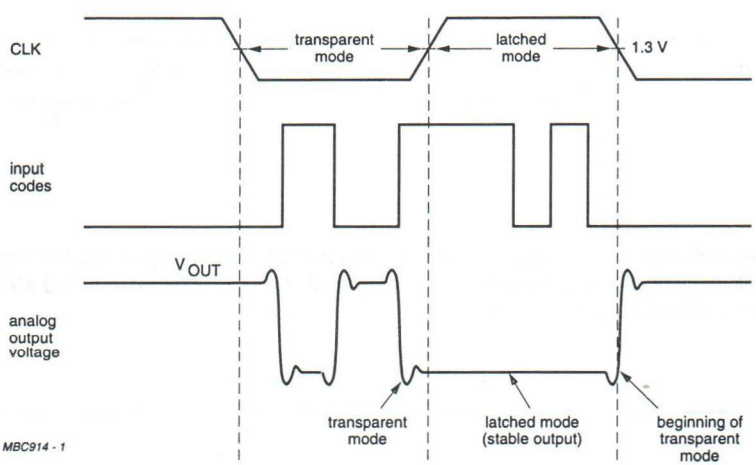
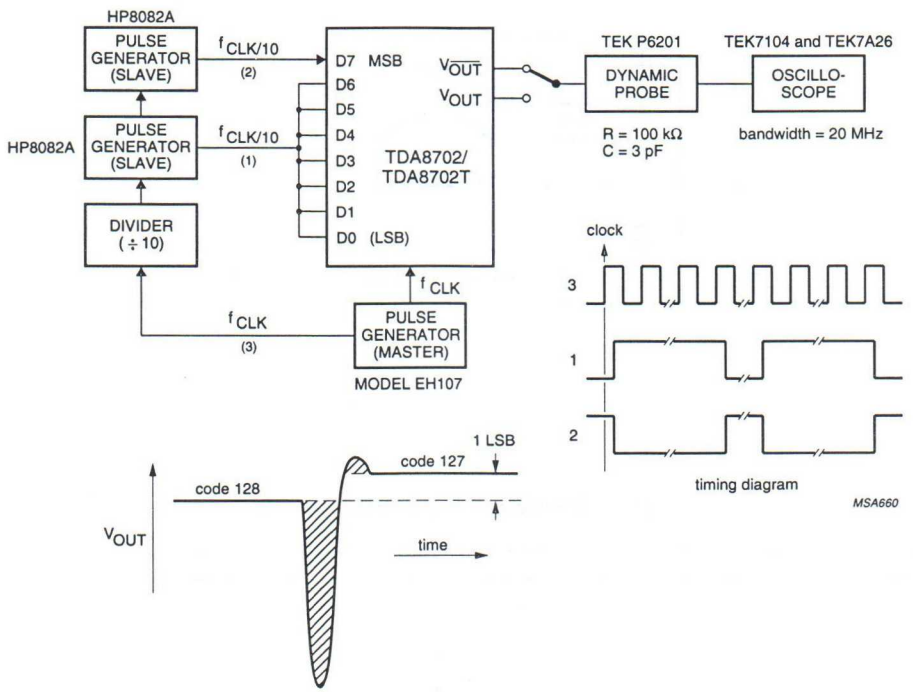


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

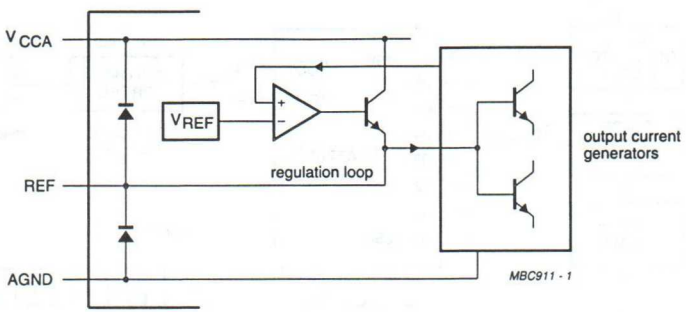


Fig.7 Reference voltage generator decoupling.

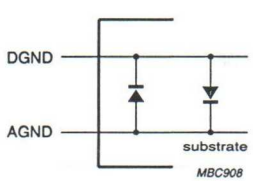


Fig.8 AGND and DGND.

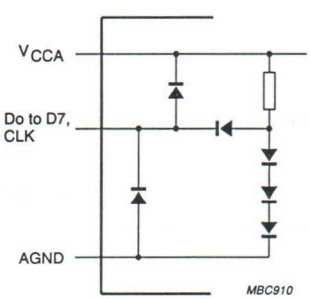


Fig.9 D7 to D0 and CLK.

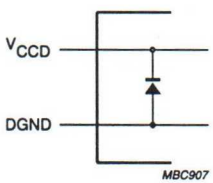


Fig.10 Digital supply.

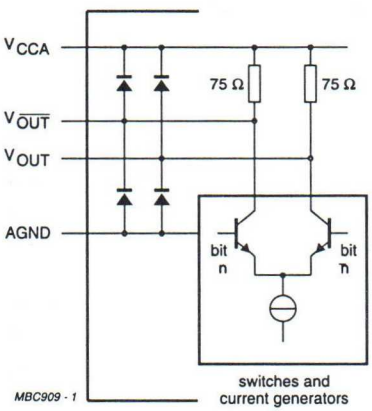


Fig.11 Analog outputs.

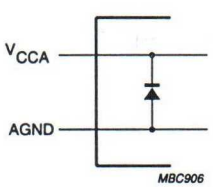
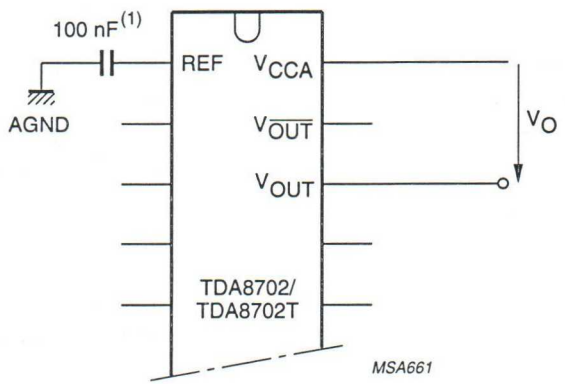


Fig.12 Analog supply.

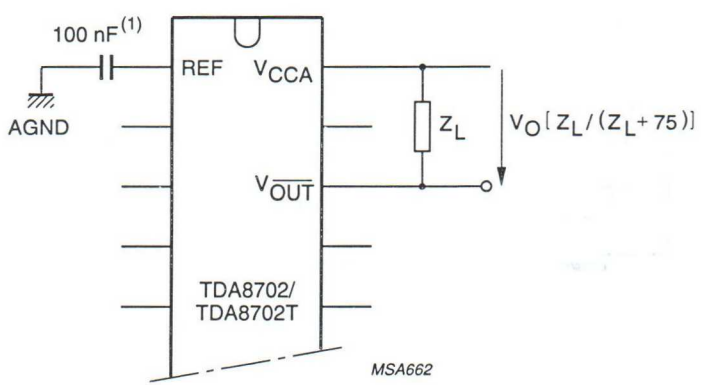
APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



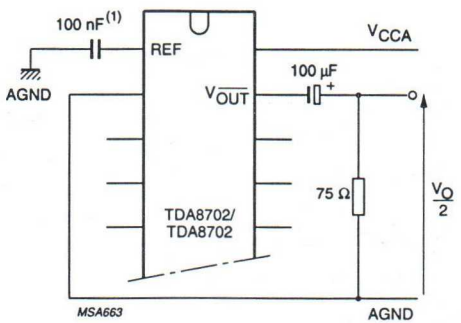
(1) This is a recommended value for decoupling pin 1.

Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).



(1) This is a recommended value for decoupling pin 1.

Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output with AGND as reference.

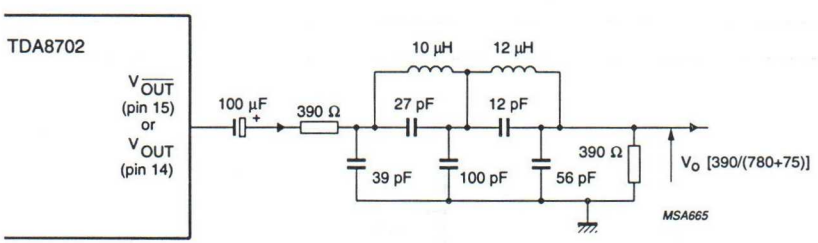
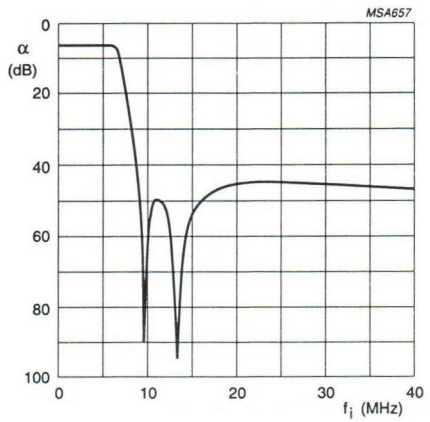


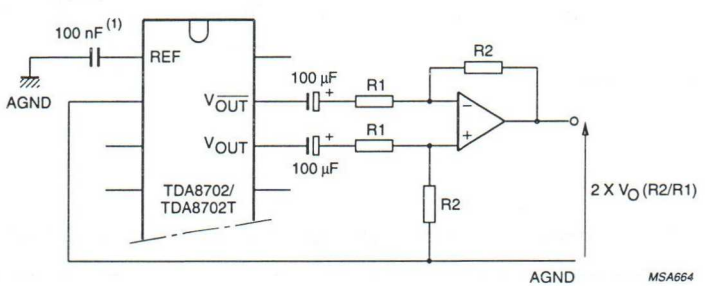
Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple at ≤ 0.1 dB
- $f_{(-3\ dB)}$ = 6.7 MHz
- $f_{(NOTCH)}$ = 9.7 MHz and 13.3 MHz

Fig.17 Frequency response for filter shown in Fig.16.



(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

8-bit high-speed analog-to-digital converter

TDA8703

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR.

GENERAL DESCRIPTION

The TDA8703 is an 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stages supply current		–	11	14	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	–	19.5	–	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	–	–	MHz
P_{tot}	total power dissipation		–	290	415	mW

Notes

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.
   - If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

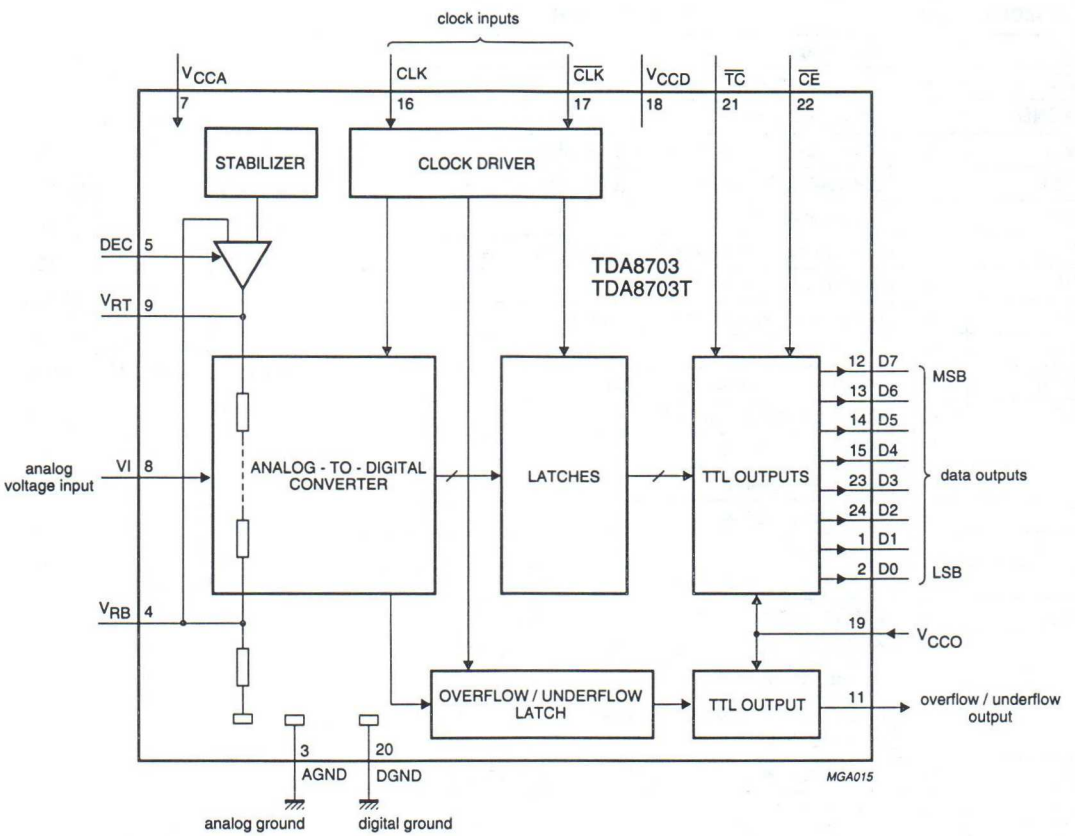


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output ($\overline{TTL}$ level input, active LOW)
$\overline{CE}$	22	chip enable input ($\overline{TTL}$ level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

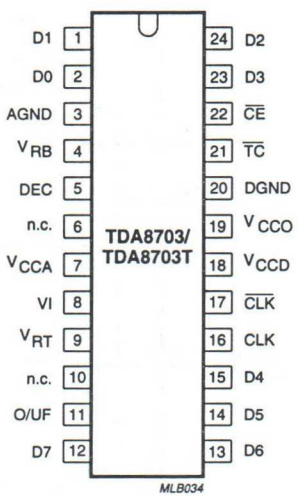


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK}/V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; referenced to DGND	–	2.0	V
I_O	output current		–	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+125	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition. If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT101	55 K/W
	SOT137A	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	–	11	14	mA
Inputs						
Clock input $\overline{CLK}$ and CLK (note 1; referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V $V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	– –	– –	100 300	µA µA
Z_i	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4	–	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4.5	–	pF
$V_{CLK} - V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	–	2.0	V
$\overline{TC}$ and $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	–	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	–	0.115	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_{VI} = 3.6$ V	60	120	180	µA
Z_i	input impedance	$f_i = 1$ MHz	–	10	–	kΩ
C_i	input capacitance	$f_i = 1$ MHz	–	14	–	pF

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
Digital outputs (D7 - D0) (referenced to DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency		40	–	–	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	−3 dB bandwidth	note 3	–	19.5	–	MHz
G_d	differential gain	note 4	–	0.6	–	%
ϕ_d	differential phase	note 4	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	−55	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	−28	−25	dB
SVRR2	supply voltage ripple rejection	note 5	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 6	–	–	±2	LSB
EB	effective bits	f_i = 4.43 MHz	–	7.1	–	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		–	–	2	ns
t_{HD}	output hold time		6	–	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	16	20	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	12	ns

Notes

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition. If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V:
   $SVRR1 = 20 \log (\Delta V_{VI(127)} / \Delta V_{CCA})$
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:
   $SVR2 = \{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} + \Delta V_{CCA}$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition:
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.

Table 1 Output coding and input voltage (referenced to AGND; typical values).

			BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection.

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

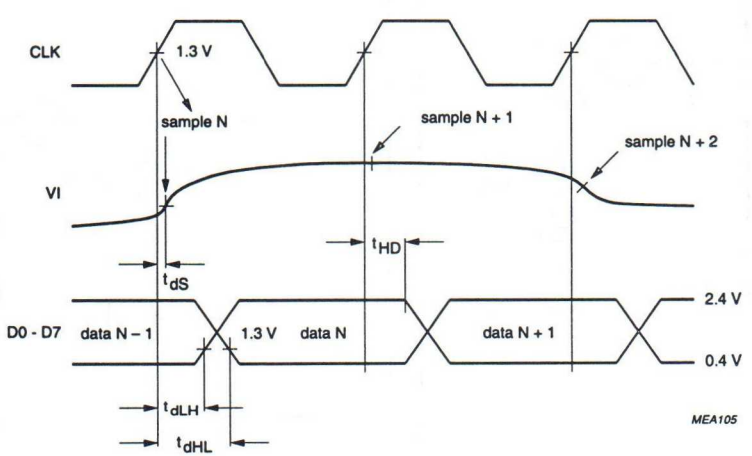


Fig.3 Timing diagram.

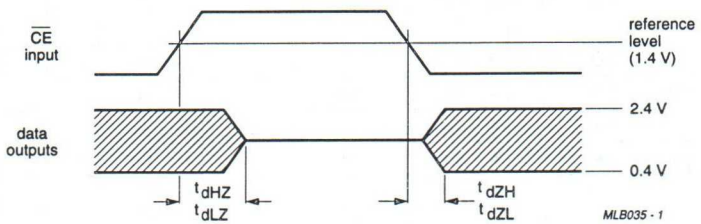


Fig.4 3-state delay timing diagram.

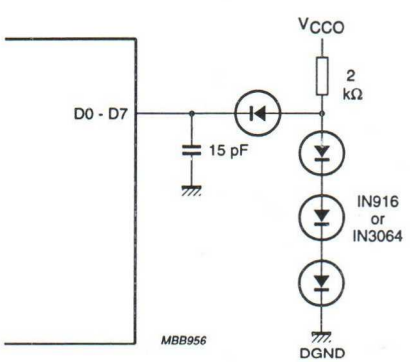


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

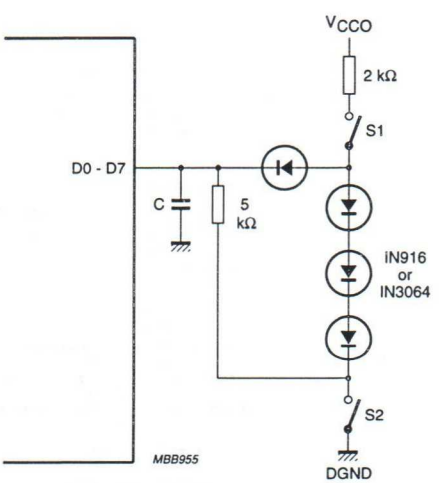


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit.

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

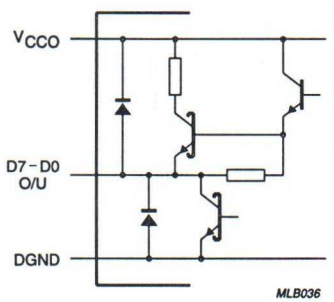


Fig.7 TTL data and overflow/underflow outputs.

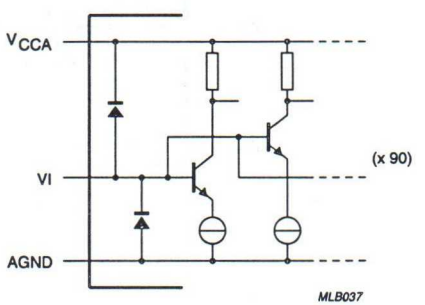


Fig.8 Analog inputs.

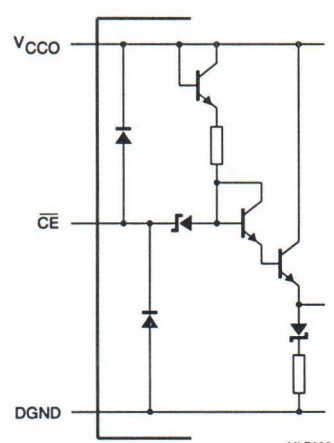


Fig.9 $\overline{CE}$ (3-state) input.

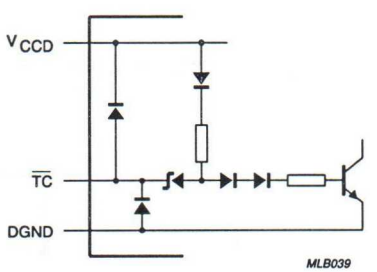


Fig.10 $\overline{TC}$ (two's complement) input.

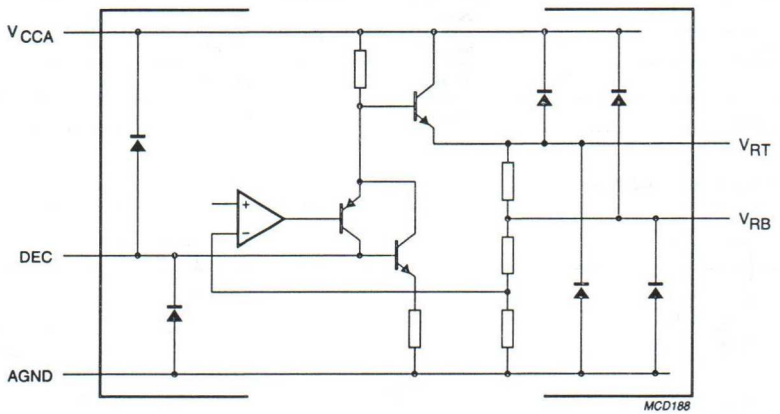


Fig.11 V_{RB}, V_{RT} and DEC.

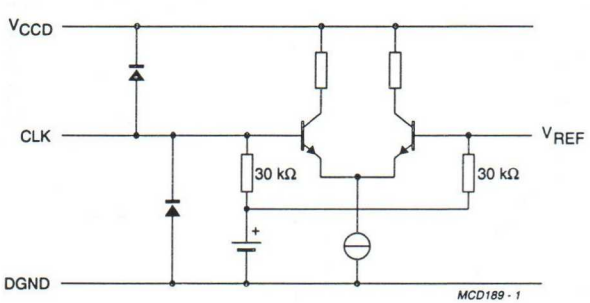


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

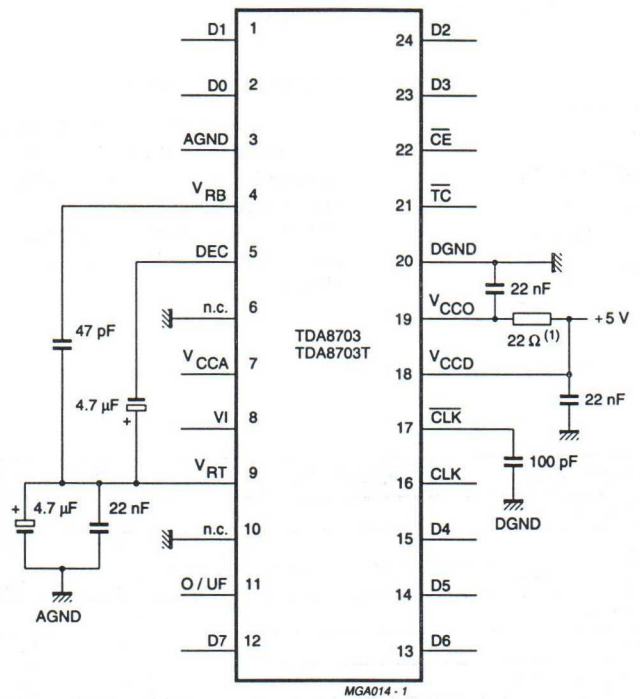


Fig.13 Application diagram.

Notes to Fig.13

1. It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of the TDA8703 interfaces with a capacitive CMOS load device.
2. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
3. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
4. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
5. If it is required to use the TDA8703 in a parallel system configuration, the references (V_{RB} and V_{RT}) of each TDA87803 can be connected together. Code 0 will be identical and code 255 will remain in the 1LSB variation for each TDA8703.
6. Analog and digital supplies should be separated and decoupled.
7. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

6-bit high-speed dual analog-to-digital converter

TDA8705

FEATURES

- 2 times 6-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (5.8 effective bits at 10 MHz full-scale input at f_{clk} = 40 MHz
- TTL output
- Two separated inputs (AC-coupling)
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference regulation possible)
- Power dissipation only 250 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- DBS (Digital Broadcast Satellite)
- QPSK (Quadrature Phase Shift Keying) demodulation
- Video.

GENERAL DESCRIPTION

The TDA8705 is a 6-bit high-speed dual analog-to-digital converter (ADC) for satellite video and other applications. It converts the two analog input signals into two 6-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	24	–	mA
I_{CCD}	digital supply current		–	14	–	mA
I_{CCO}	output stages supply current		–	10	–	mA
ILE	DC integral linear error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation		–	250	–	mW

Note

1. Full-scale sine wave (f_i = 10 MHz; f_{clk} = 40 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8705T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

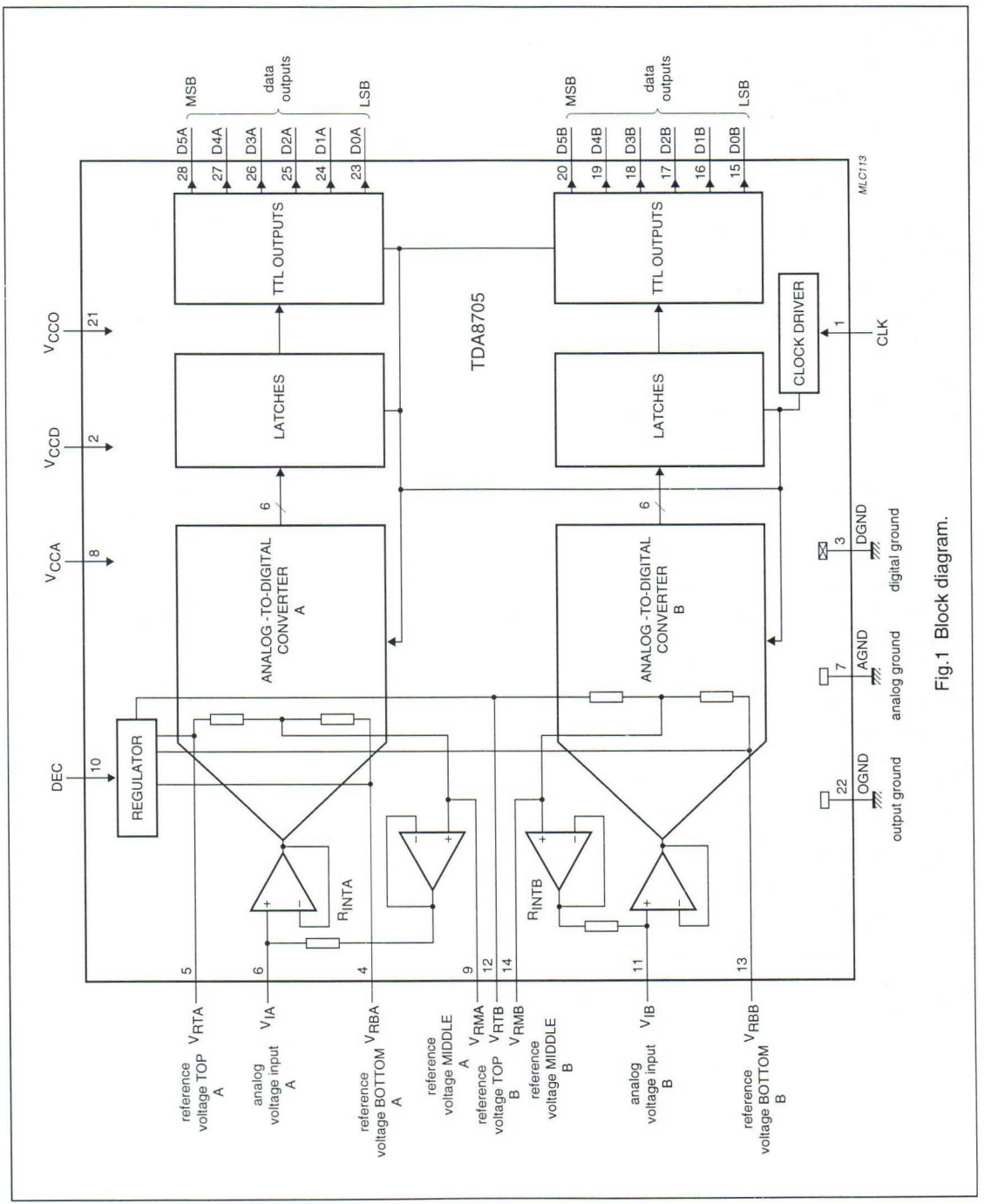


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
V_{CCD}	2	digital supply voltage (+5 V)
DGND	3	digital ground
V_{RBA}	4	reference voltage BOTTOM for ADC A (decoupling)
V_{RTA}	5	reference voltage TOP for ADC A (decoupling)
V_{IA}	6	analog input voltage for ADC A
AGND	7	analog ground
V_{CCA}	8	analog supply voltage (+5 V)
V_{RMA}	9	reference voltage MIDDLE for ADC A (decoupling)
DEC	10	decoupling input
V_{IB}	11	analog input voltage for ADC B
V_{RTB}	12	reference voltage TOP for ADC B (decoupling)
V_{RBB}	13	reference voltage BOTTOM for ADC B (decoupling)
V_{RMB}	14	reference voltage MIDDLE for ADC B (decoupling)
D0B	15	data output; bit 0 (LSB), ADC B
D1B	16	data output; bit 1, ADC B
D2B	17	data output; bit 2, ADC B
D3B	18	data output; bit 3, ADC B
D4B	19	data output; bit 4, ADC B
D5B	20	data output; bit 5 (MSB), ADC B
V_{CCO}	21	supply voltage for output stages (+5 V)
OGND	22	output ground
D0A	23	data output; bit 0 (LSB), ADC A
D1A	24	data output; bit 1, ADC A
D2A	25	data output; bit 2, ADC A
D3A	26	data output; bit 3, ADC A
D4A	27	data output; bit 4, ADC A
D5A	28	data output; bit 5 (MSB), ADC A

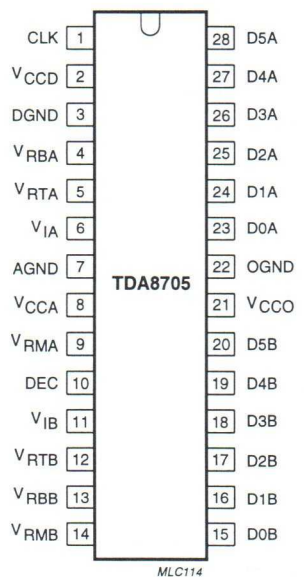


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCO} and V_{CCD} may have any value between −0.3 V and +7.0 V provided the difference between V_{CCA}, V_{CCO} and V_{CCD} is between −1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

V_{CCA} = V_8 to V_7 = 4.75 to 5.25 V; V_{CCD} = V_2 to V_3 = 4.75 to 5.25 V; V_{CCO} = V_{21} to V_{22} = 4.75 to 5.25 V; AGND, OGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.25 to +0.25 V; V_{CCO} to V_{CCD} = −0.25 to +0.25 V; V_{CCA} to V_{CCO} = −0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at V_{CCA} = V_{CCD} = V_{CCO} = 5 V and T_{amb} = 25 °C; C_L = 15 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	24	–	mA
I_{CCD}	digital supply current		–	14	–	mA
I_{CCO}	output stages supply current		–	10	–	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−1	–	+1	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	µA
Z_I	input impedance	f_{clk} = 40 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 40 MHz	–	2	–	pF
V_I ANALOG INPUT VOLTAGE FOR A AND B (REFERENCED TO AGND)						
R_I	DC parallel input resistance		20	–	–	kΩ
C_I	parallel input capacitance	f_i = 10 MHz	–	1.5	–	pF
α_{CT}	crosstalk between V_{IA} and V_{IB}	f_i = 10 MHz	40	–	–	dB
Reference voltages for the resistor ladder (A and B); see Table 1						
V_{RB}	reference voltage BOTTOM		tbf	2.0	tbf	V
V_{RT}	reference voltage TOP		tbf	2.9	tbf	V
V_{diff}	differential reference voltage V_{RT} − V_{RB}		0.85	0.90	0.95	V
I_{ref}	reference current		–	2	–	mA
R_{LAD}	resistor ladder		–	450	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	0.127	–	Ω/K
V_{osB}	offset voltage BOTTOM	note 2	–	200	–	mV
V_{osT}	offset voltage TOP	note 2	–	200	–	mV
$V_{i(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
Outputs (A and B)						
DIGITAL OUTPUTS D5 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −1 mA	2.4	–	V_{CCD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK INPUT CLK (note 1; see Fig.3)						
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		10	–	–	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.5	±1.0	LSB
OFE	offset error between A and B	middle code	–	–	±0.5	LSB
GE	gain error between A and B		–	–	±1.0	LSB
BANDWIDTH (f_{clk} = 40 MHz)						
B	–0.5 dB analog bandwidth	full-scale sine wave; note 4	–	50	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.4; note 5	–	tbf	–	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.4; note 5	–	tbf	–	ns
HARMONICS (f_{clk} = 40 MHz); see Fig.5						
h_1	fundamental harmonics (full scale)	f_i = 10 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 10 MHz				
	second harmonics		–	–49	–	dB
	third harmonics		–	–51	–	dB
THD	total harmonic distortion	f_i = 10 MHz	–	–46	–42	dB
SIGNAL-TO-NOISE RATIO (note 7; see Fig.5)						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 40 MHz; f_i = 10 MHz	36	37	–	dB
EFFECTIVE BITS (note 7; see Figs 5 and 6)						
EB	effective bits	f_{clk} = 40 MHz				
		f_i = 10 MHz	–	5.8	–	bits
		f_i = 20 MHz	–	5.6	–	bits
TWO-TONE (note 8)						
TTIR	two-tone intermodulation rejection	f_{clk} = 40 MHz	–	48	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 10 MHz; V_I = ±8 LSB at code 32	–	tbf	–	times/ samples

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIFFERENTIAL GAIN (note 6)						
G_{diff}	differential gain	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	tbf	–	%
DIFFERENTIAL PHASE (note 6)						
φ_{diff}	differential phase	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	tbf	–	deg
Timing (f_{clk} = 40 MHz; C_L = 15 pF); note 9; see Fig.3						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	–	14	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including 3F:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 3F at T_{amb} = 25 °C.
3. Full-scale sine wave (f_i = 10 MHz; f_{clk} = 40 MHz).
4. The –0.5 dB analog bandwidth is determined by the 0.5 dB reduction in the reconstructed output, the input being a full-scale sine wave. It is determined with a beat frequency method; no glitches occurrence.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Measurement carried out using video analyser VM700A.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 10.0 MHz and 10.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{I(p-p)}$ A OR B (V)	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
Underflow	<2.2	0	0	0	0	0	0
0	2.2	0	0	0	0	0	0
1	2.208	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
62	2.692	1	1	1	1	1	0
63	2.7	1	1	1	1	1	1
Overflow	>2.7	1	1	1	1	1	1

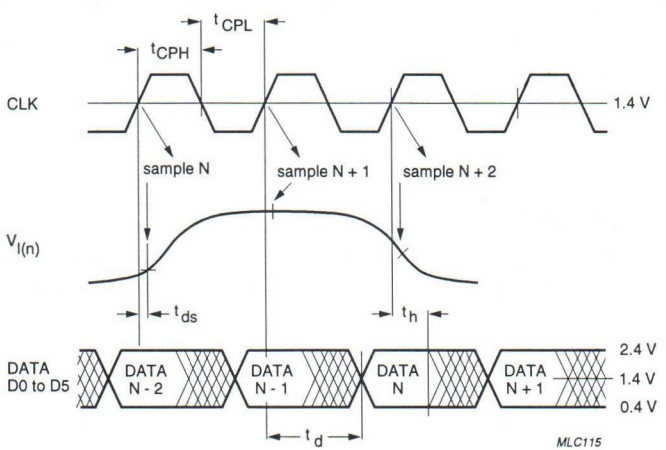


Fig.3 Timing diagram for data output.

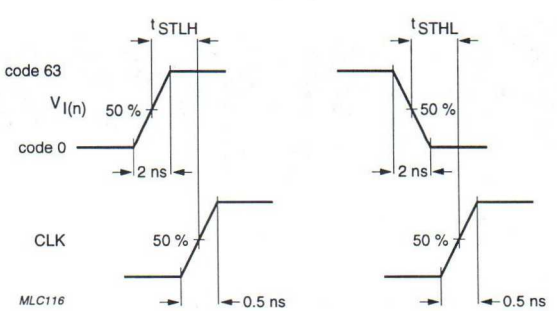
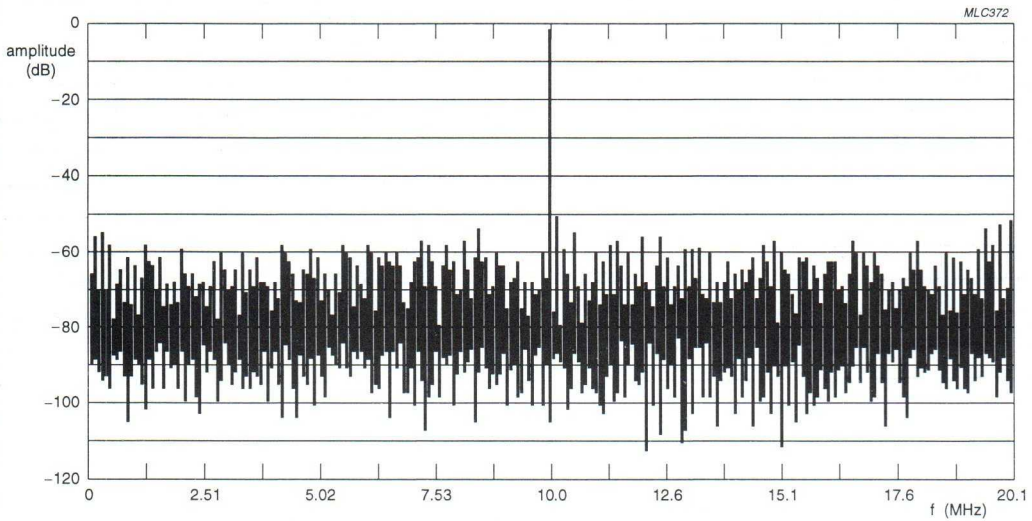
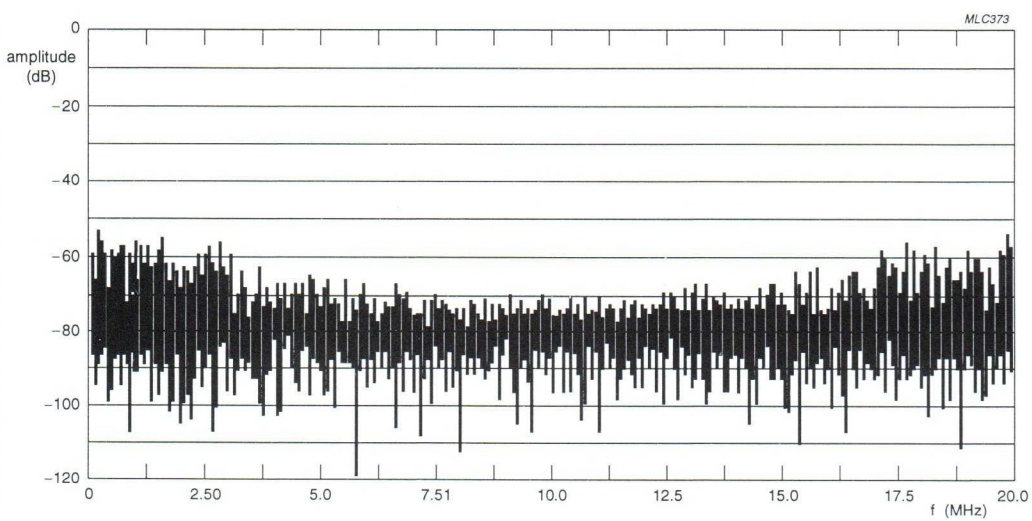


Fig.4 Analog input settling-time diagram.



Effective bits: 5.83; THD = −46.31 dB;
Harmonic levels (dB): 2nd = −51.85; 3rd = −51.11; 4th = −55.73; 5th = −59.89; 6th = −52.68.

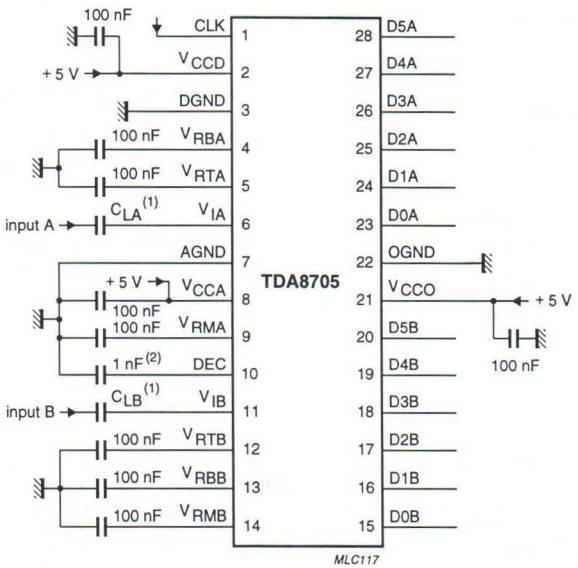
Fig.5 Typical Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 10 MHz).



Effective bits: 5.65; THD = −41.79 dB;
Harmonic levels (dB): 2nd = −51.73; 3rd = −42.51; 4th = −65.18; 5th = −57.48; 6th = −58.98.

Fig.6 Typical Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 20 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

$V_{RT(n)}$, $V_{RM(n)}$ and $V_{RB(n)}$ and DEC inputs are decoupled to AGND.

(1) In the event of AC-coupling, C_{LA} and C_{LB} values are chosen in accordance with the classical low frequencies cut-off formulae

$$f_{CL} = \frac{1}{2 \times \pi \times R_i \times C_L}$$ where input resistance R_i is the value measured under DC conditions.

In the event of DC-coupling, C_{LA} and C_{LB} capacitors are omitted. The DC biassing and AC modulation signal directly applied to inputs (pin 6 and 11), must be in the range of $V_{RT(n)} - V_{RB(n)}$.

(2) When pin 10 (DEC) is short-circuited to AGND, an external regulator can be connected to $V_{RT(n)}$ and $V_{RB(n)}$.

Fig.7 Application diagram.

6-bit high-speed dual analog-to-digital converter

TDA8705A

FEATURES

- 2 times 6-bit resolution
- Sampling rate up to 80 MHz
- High signal-to-noise ratio over a large analog input frequency range (5.5 effective bits at 20 MHz full-scale input at f_{clk} = 80 MHz)
- TTL output
- Two separated inputs (AC-coupling)
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference regulation possible)
- Power dissipation only 250 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- DBS (Digital Broadcast Satellite)
- QPSK (Quadrature Phase Shift Keying) demodulation
- Video.

GENERAL DESCRIPTION

The TDA8705A is a 6-bit high-speed dual analog-to-digital converter (ADC) for satellite video and other applications. It converts the two analog input signals into two 6-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	24	–	mA
I_{CCD}	digital supply current		–	14	–	mA
I_{CCO}	output stages supply current		–	10	–	mA
ILE	DC integral linear error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
P_{tot}	total power dissipation		–	250	–	mW

Note

1. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8705AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

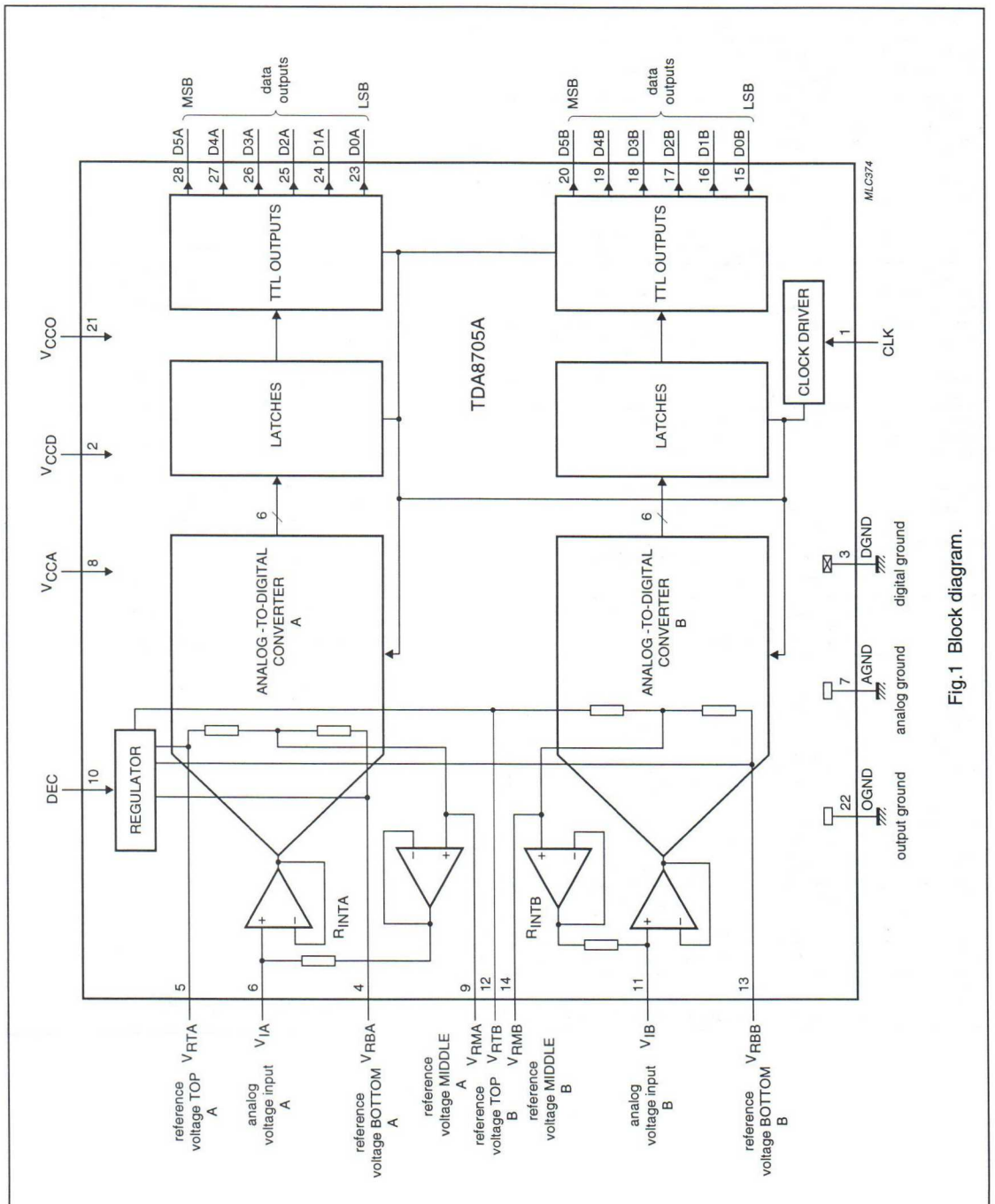


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
V_{CCD}	2	digital supply voltage (+5 V)
DGND	3	digital ground
V_{RBA}	4	reference voltage BOTTOM for ADC A (decoupling)
V_{RTA}	5	reference voltage TOP for ADC A (decoupling)
V_{IA}	6	analog input voltage for ADC A
AGND	7	analog ground
V_{CCA}	8	analog supply voltage (+5 V)
V_{RMA}	9	reference voltage MIDDLE for ADC A (decoupling)
DEC	10	decoupling input
V_{IB}	11	analog input voltage for ADC B
V_{RTB}	12	reference voltage TOP for ADC B (decoupling)
V_{RBB}	13	reference voltage BOTTOM for ADC B (decoupling)
V_{RMB}	14	reference voltage MIDDLE for ADC B (decoupling)
D0B	15	data output; bit 0 (LSB), ADC B
D1B	16	data output; bit 1, ADC B
D2B	17	data output; bit 2, ADC B
D3B	18	data output; bit 3, ADC B
D4B	19	data output; bit 4, ADC B
D5B	20	data output; bit 5 (MSB), ADC B
V_{CCO}	21	supply voltage for output stages (+5 V)
OGND	22	output ground
D0A	23	data output; bit 0 (LSB), ADC A
D1A	24	data output; bit 1, ADC A
D2A	25	data output; bit 2, ADC A
D3A	26	data output; bit 3, ADC A
D4A	27	data output; bit 4, ADC A
D5A	28	data output; bit 5 (MSB), ADC A

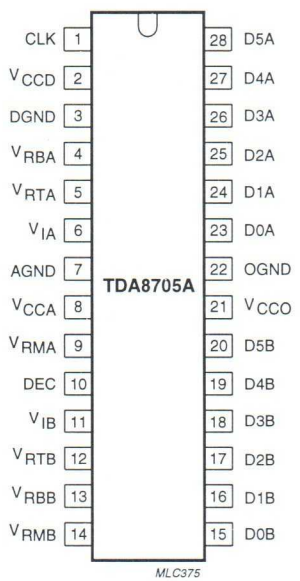


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCO} and V_{CCD} may have any value between −0.3 V and +7.0 V provided the difference between V_{CCA}, V_{CCO} and V_{CCD} is between −1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

$V_{CCA} = V_8$ to V_7 = 4.75 to 5.25 V; $V_{CCD} = V_2$ to V_3 = 4.75 to 5.25 V; $V_{CCO} = V_{21}$ to V_{22} = 4.75 to 5.25 V; AGND, OGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.25 to +0.25 V; V_{CCO} to V_{CCD} = −0.25 to +0.25 V; V_{CCA} to V_{CCO} = −0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; C_L = 15 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	24	–	mA
I_{CCD}	digital supply current		–	14	–	mA
I_{CCO}	output stages supply current		–	10	–	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−1	–	+1	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	µA
Z_I	input impedance	f_{clk} = 80 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 80 MHz	–	2	–	pF
V_I ANALOG INPUT VOLTAGE FOR A AND B (REFERENCED TO AGND)						
R_I	DC parallel input resistance		20	–	–	kΩ
C_I	parallel input capacitance	f_i = 20 MHz	–	1.5	–	pF
α_{CT}	crosstalk between V_{IA} and V_{IB}	f_i = 20 MHz	40	–	–	dB
Reference voltages for the resistor ladder (A and B); see Table 1						
V_{RB}	reference voltage BOTTOM		tbf	2.0	tbf	V
V_{RT}	reference voltage TOP		tbf	2.9	tbf	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		0.85	0.90	0.95	V
I_{ref}	reference current		–	2	–	mA
R_{LAD}	resistor ladder		–	450	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	0.127	–	Ω/K
V_{osB}	offset voltage BOTTOM	note 2	–	200	–	mV
V_{osT}	offset voltage TOP	note 2	–	200	–	mV
$V_{i(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
Outputs (A and B)						
DIGITAL OUTPUTS D5 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −1 mA	2.4	–	V_{CCD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK INPUT CLK (note 1; see Fig.3)						
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
t_{CPH}	clock pulse width HIGH		5.5	–	–	ns
t_{CPL}	clock pulse width LOW		5.5	–	–	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.5	±1.0	LSB
OFE	offset error between A and B	middle code	–	–	±0.5	LSB
GE	gain error between A and B		–	–	±1.0	LSB
BANDWIDTH (f_{clk} = 80 MHz)						
B	–0.5 dB analog bandwidth	full-scale sine wave; note 4	–	50	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.4; note 5	–	tbf	–	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.4; note 5	–	tbf	–	ns
HARMONICS (f_{clk} = 40 MHz); see Fig.5						
h_1	fundamental harmonics (full scale)	f_i = 20 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 20 MHz				
	second harmonics		–	–45	–	dB
	third harmonics		–	–41	–	dB
THD	total harmonic distortion	f_i = 20 MHz	–	–39	–37	dB
SIGNAL-TO-NOISE RATIO (note 7; see Fig.5)						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 80 MHz; f_i = 20 MHz	35	36	–	dB
EFFECTIVE BITS (note 7; see Fig.5)						
EB	effective bits	f_{clk} = 80 MHz				
		f_i = 10 MHz	–	5.7	–	bits
		f_i = 20 MHz	–	5.5	–	bits
		f_i = 30 MHz	–	5.1	–	bits
TWO-TONE (note 8)						
TTIR	two-tone intermodulation rejection	f_{clk} = 80 MHz	–	48	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 80 MHz; f_i = 20 MHz; V_I = ±8 LSB at code 32	–	tbf	–	times/ samples
DIFFERENTIAL GAIN (note 6)						
G_{diff}	differential gain	f_{clk} = 80 MHz; f_i = 4.43 MHz	–	tbf	–	%
DIFFERENTIAL PHASE (note 6)						
φ_{diff}	differential phase	f_{clk} = 80 MHz; f_i = 4.43 MHz	–	tbf	–	deg
Timing (f_{clk} = 80 MHz; C_L = 15 pF); note 9; see Fig.3						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	–	11	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including 3F:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 3F at T_{amb} = 25 °C.
3. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).
4. The –0.5 dB analog bandwidth is determined by the 0.5 dB reduction in the reconstructed output, the input being a full-scale sine wave. It is determined with a beat frequency method; no glitches occurrence.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Measurement carried out using video analyser VM700A.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 20.0 MHz and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND).

STEP	$V_{I(p-p)}$ A OR B (V)	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
Underflow	<2.2	0	0	0	0	0	0
0	2.2	0	0	0	0	0	0
1	2.208	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
62	2.692	1	1	1	1	1	0
63	2.7	1	1	1	1	1	1
Overflow	>2.7	1	1	1	1	1	1

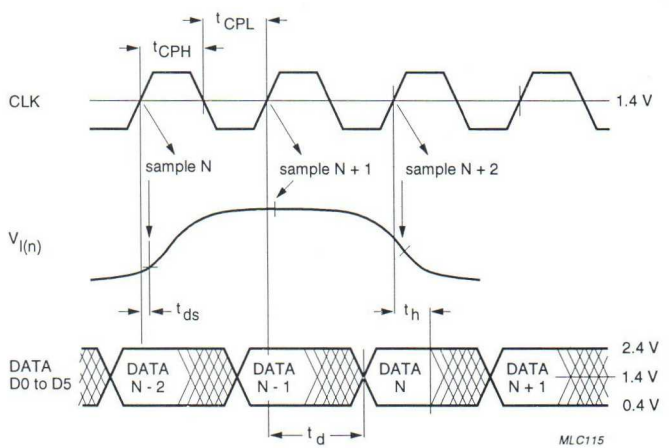


Fig.3 Timing diagram for data output.

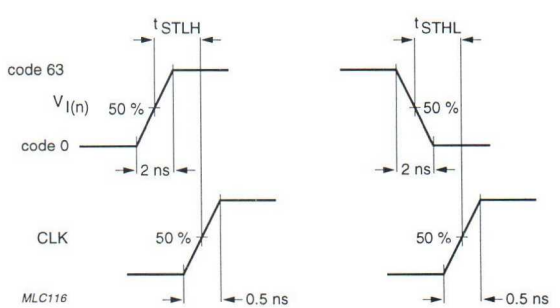
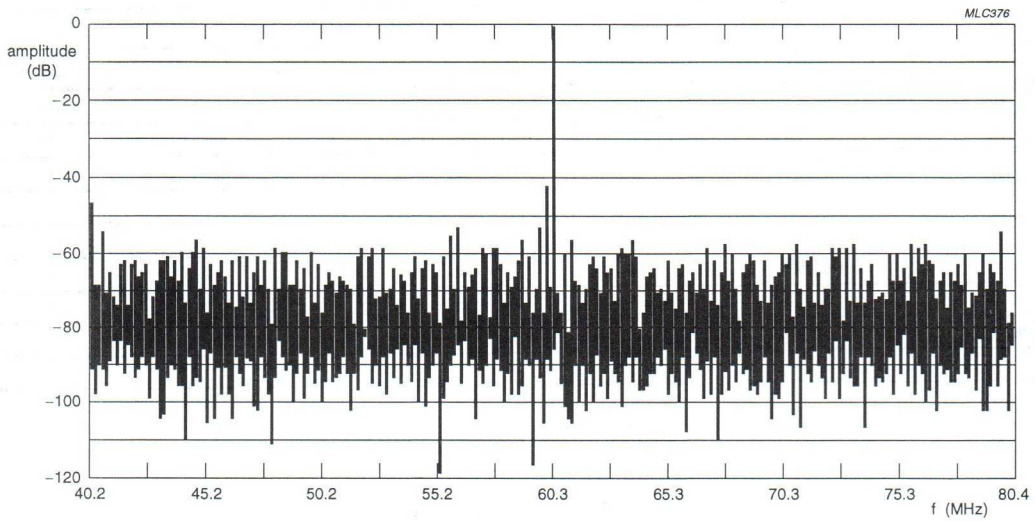


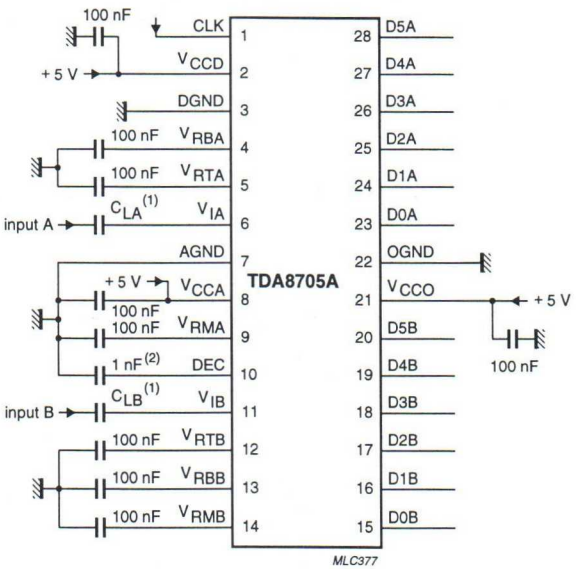
Fig.4 Analog input settling-time diagram.



Effective bits: 5.54; THD = −39.89 dB;
Harmonic levels (dB): 2nd = −46.51; 3rd = −41.21; 4th = −80.65; 5th = −60.16; 6th = −54.51.

Fig.5 Typical Fast Fourier Transform (f_{clk} = 80 MHz; f_i = 20 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

$V_{RT(n)}$, $V_{RM(n)}$ and $V_{RB(n)}$ and DEC inputs are decoupled to AGND.

(1) In the event of AC-coupling, C_{LA} and C_{LB} values are chosen in accordance with the classical low frequencies cut-off formulae

$$f_{CL} = \frac{1}{2 \times \pi \times R_i \times C_L}$$ where input resistance R_i is the value measured under DC conditions.

In the event of DC-coupling, C_{LA} and C_{LB} capacitors are omitted. The DC biassing and AC modulation signal directly applied to inputs (pin 6 and 11), must be in the range of $V_{RT(n)} - V_{RB(n)}$.

(2) When pin 10 (DEC) is short-circuited to AGND, an external regulator can be connected to $V_{RT(n)}$ and $V_{RB(n)}$.

Fig.6 Application diagram.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package

APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIPCO) for TV
- Videophone
- Frame grabber

GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit analog-to-digital converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

FUNCTIONAL DESCRIPTION

The TDA8706 is a "like-flash" converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH). Luminance clamping level is fitted with 00 hex. code (output 000000). Chrominance clamping level is fitted with 20 Hex. code (output 100000).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 20)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)		–	28	37	mA
ILE	integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
f_{CLK}	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	300	418	mW
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8706	20	DIL	plastic	SOT146EF4
TDA8706T	20	SO20L	plastic	SOT163AG7

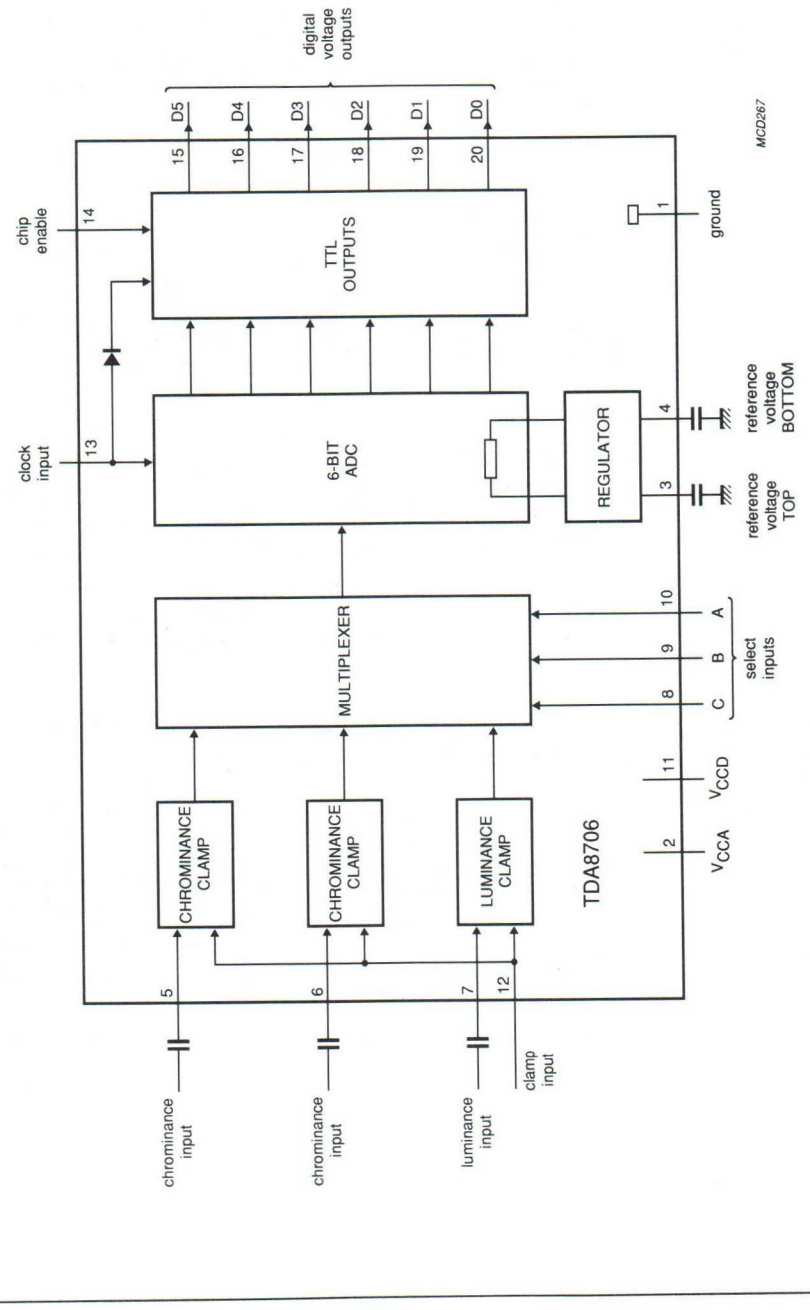


Fig.1 Block diagram.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

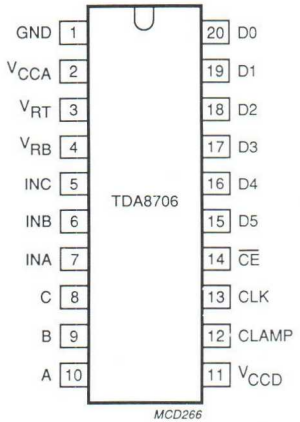


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CCA}	2	analog positive supply (+5 V)
V_{RT}	3	reference voltage TOP decoupling
V_{RB}	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V_{CCD}	11	digital positive supply voltage (+5 V)
CLAMP	12	clamp pulse input (positive pulse)
CLK	13	clock input
$\overline{CE}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage input: least significant bit (LSB)

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range (pin 2)	−0.3	7.0	V
V_{CCD}	digital supply voltage range (pin 10)	−0.3	7.0	V
V_{CCA}-V_{CCD}	supply voltage difference	1.0	–	V
V_I	input voltage range	−0.3	7.0	V
I_O	output current	–	10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS (see Tables 1 and 2)

V_{CCA} = 4.5 V to 5.5 V; V_{CCD} = 4.5 V to 5.5 V = V_{CCD}; T_{amb} = 0 °C to +70°C; C_{VRB} = C_{VR1} = 100 nF; Typical values measured at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 2)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
Inputs						
CLOCK INPUT (PIN 13)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{CLK} = 20 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 20 MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	20	µA
Reference voltage (pins 3 and 4)						
V_{RT}	reference voltage TOP decoupling		3.22	3.35	3.44	V
V_{RB}	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
Analog inputs INA, INB, INC (pins 7, 6 and 5)						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
Z_I	input impedance	f_i = 4.43 MHz	100	–	–	kΩ
C_{clamp}	coupling clamp capacitance		1	10	1000	nF
Analog signal processing (pins 5, 6 and 7) (f_{CLK} = 20 MHz)						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz	-	–45	-	dB
G_{diff}	differential gain	note 1	–	0.4	–	%
ϕ_{diff}	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB
Outputs						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (SEE TABLE 2)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level ouptut voltage	I_O = 0.5 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	20	µA
Switching characteristics						
CLOCK TIMING (SEE FIG.3)						
f_{CLK}	maximum clock frequency		20	–	–	MHz
f_{mux}	maximum multiplexing frequency		10	–	–	MHz
t_{CLK}	period		50	–	–	ns
	duty cycle	CLK = V_{IH}	45	50	66.6	%
t_{LOW}	LOW time	at 50%	16	–	–	ns
t_{HIGH}	HIGH time	at 50%	22.5	–	–	ns
t_{CLR}	rise time	at 10% to 90%	4	6	–	ns
t_{CLF}	fall time	at 90% to 10%	4	6	–	ns
Select signals, Clamp, Data (see Figs 4 and 5)						
t_S	set-up time select A, B and C		35	–	–	ns
t_r	rise time (A, B and C)	at 10% to 90%	4	6	–	ns
t_f	fall time (A, B and C)	at 90% to 10%	4	6	–	ns
t_{CLPS}	set-up time clamp asynchronous		0	–	–	
t_{CLPH}	hold time clamp asynchronous		0	–	–	
t_{CLPP}	clamp pulse	C_{CLP} = 10 nF	–	3	–	µs
t_d	data output delay time		–	15	24	ns
t_{DH}	data hold time		12	–	–	ns
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 3	–	–	±2	LSB
EB	effective bits	note 3	–	5.7	–	bits
Timing						
DIGITAL OUTPUTS						
T_{dt}	3-state delay time	see Fig.6	–	16	25	ns
T_{sto}	sampling time offset		–	2	–	ns

Notes to the characteristics

1. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V and f_i = 4.43 MHz) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

   $$SVRR = 20 \log \frac{\Delta V_{VI31)}}{\Delta V_{CCA}}$$

3. Full-scale sinewave; f_i = 4.43 MHz, f_{CLK} = 20 MHz.

Table 1 Output coding

STEP	V_I (note 1) (TYP. value)	BINARY OUTPUTS D5 to D0
Underflow	< 2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		.....
.		.....
.		.....
62	3.072 V	111110
63	3.086 V	111111
Overflow	> 3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 to D5
1	high impedance
0	active. Binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	$V_{in}A$
0	1	X	2.2
1	1	0	2.2

Note

X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	$V_{in}B/V_{in}C$
0	1	X	2.65
1	1	32	2.65

Note

X = don't care.

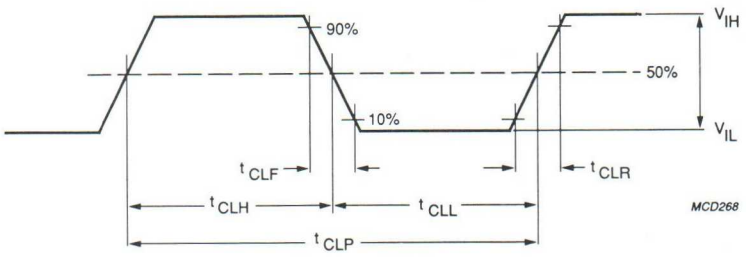


Fig.3 AC clock characteristics.

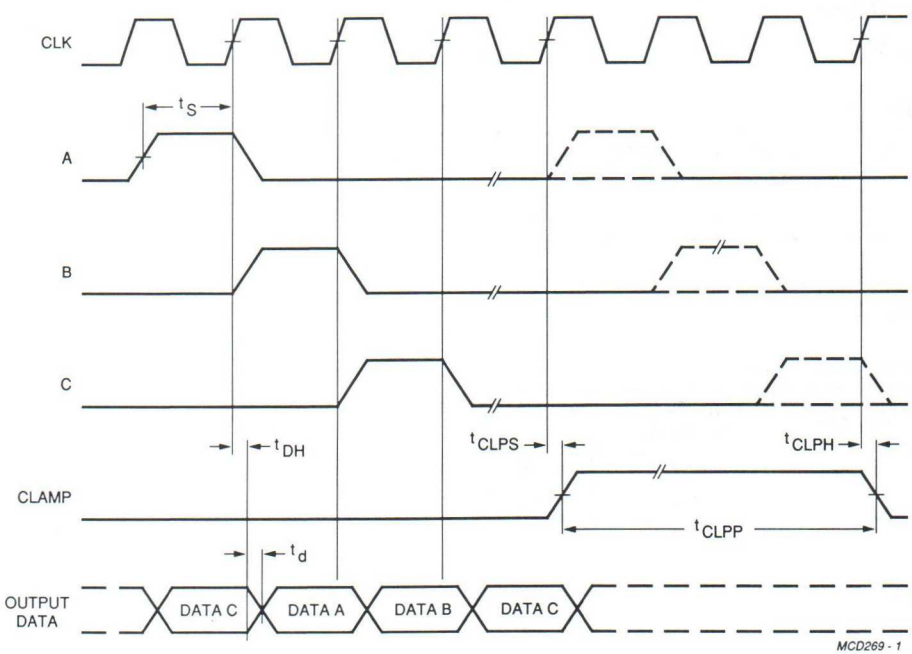


Fig.4 AC characteristics select signals; Clamp, Data.

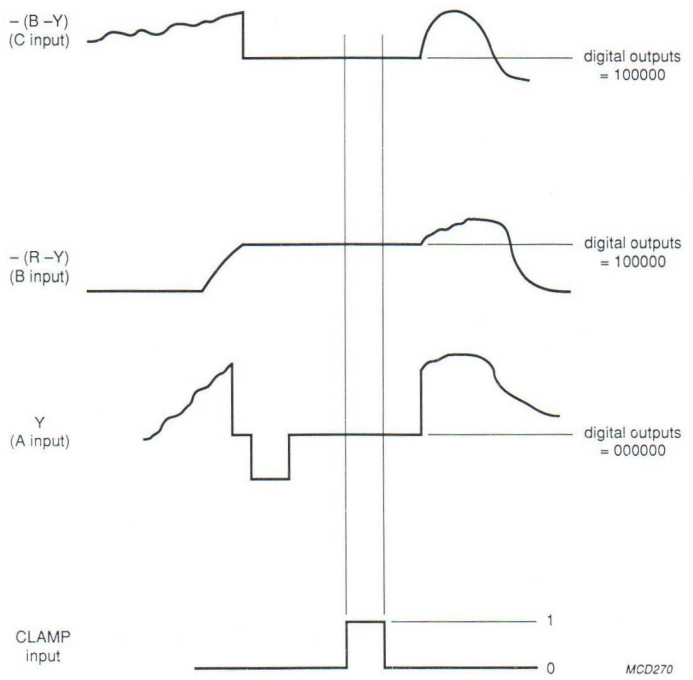


Fig.5 AC characteristics select signals; Clamp, Data.

Table 5 Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
clamping time per line (signal active)	2.2	3.0	3.3	µs
input signals clamped to correct level after	–	3	10	lines

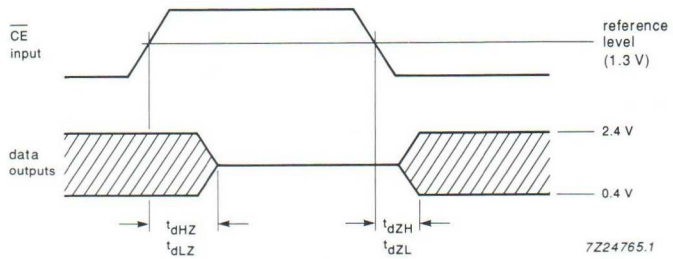


Fig.6 Timing diagram of 3-state delay.

Application information

Additional application information will be supplied on request (please quote reference number FTV/9112).

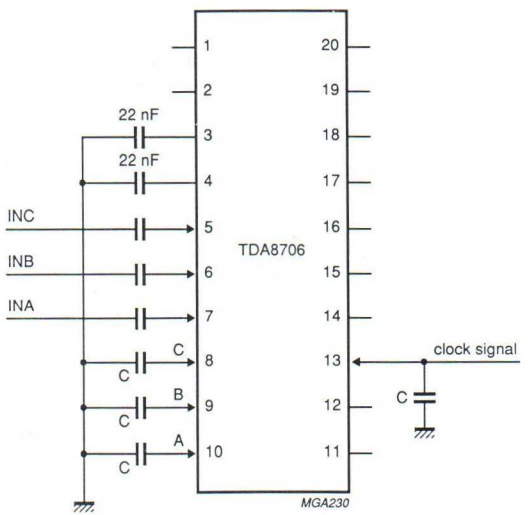


Fig.7 Application diagram.

Notes to figure 7

1. 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins
2. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity
3. Analog and digital supplies should be separated and decoupled.

Triple RGB 6-bit video analog-to-digital interface

TDA8707

FEATURES

- Triple analog-to-digital converter (ADC)
- 6-bit resolution
- Sampling rate up to 35 MHz
- Power dissipation of 300 mW (typical)
- Internal clamping function.

APPLICATIONS

- High-speed analog-to-digital conversion for video signals
- VGA signal treatment.

DESCRIPTION

The TDA8707 is a CMOS triple 6-bit video low-power analog-to-digital converter (ADC) for RGB signals. It converts the analog inputs into 6-bit binary coded digital words at a sampling rate of 35 MHz. All analog signal inputs are clamped.

Analog-to-digital converter

The TDA8707 implements 3 independent 6-bit analog-to-digital converters in CMOS process. These converters use a full-flash approach.

Clamping feature

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INR, ING and INB are switched, through series capacitors, to on-chip clamping levels during an active pulse on the clamp input CLP. Clamping level in the R, G and B channels is Code 0.

Input buffers

Internal buffers are provided to drive the analog-to-digital converter inputs. Their ratio can be adjusted externally at 1.5 or 2.0 with select input SLT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	60	77	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	5	8	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.35	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.35	±0.6	LSB
EB	effective bits	note 1	–	5.3	–	bits
f_{clk}	maximum clock conversion rate		35	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 35 MHz; note 2	–	335	450	mW

Notes

1. The number of effective bits is measured with a clock frequency of 35 MHz. This value is given for a 4.43 MHz frequency on the R, G and B channels.
2. The external resistor (value 15 kΩ) between V_{DDA} and CLREF, fixing internal static currents, influences P_{tot}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8707H	QFP44[1]	plastic quad flat package; 44 leads; lead length 1.3 mm; body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

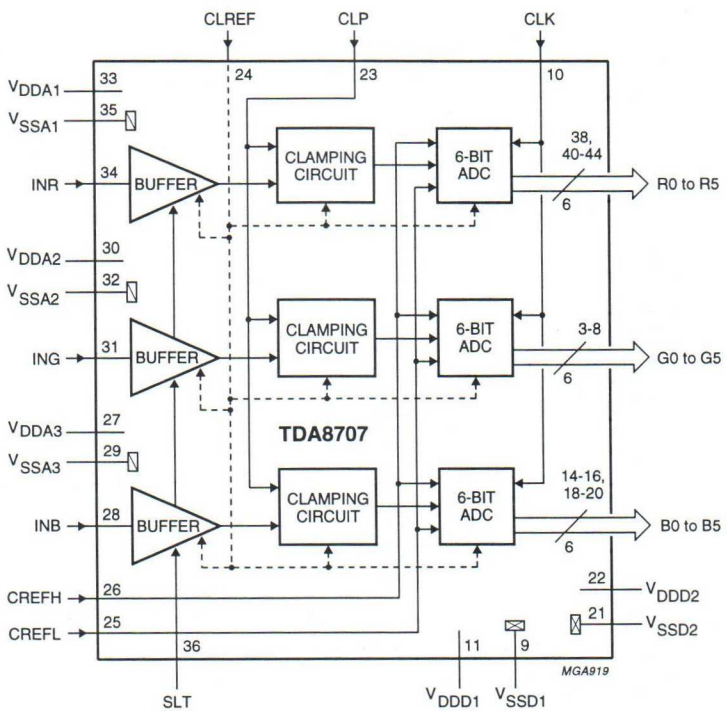


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
G0	3	GREEN data output; bit 0 (LSB)
G1	4	GREEN data output; bit 1
G2	5	GREEN data output; bit 2
G3	6	GREEN data output; bit 3
G4	7	GREEN data output; bit 4
G5	8	GREEN data output; bit 5 (MSB)
V_{SSD1}	9	digital supply ground 1
CLK	10	clock input
V_{DDD1}	11	digital supply voltage 1
n.c.	12	not connected
n.c.	13	not connected
B0	14	BLUE data output; bit 0 (LSB)
B1	15	BLUE data output; bit 1
B2	16	BLUE data output; bit 2
n.c.	17	not connected
B3	18	BLUE data output; bit 3
B4	19	BLUE data output; bit 4
B5	20	BLUE data output; bit 5 (MSB)
V_{SSD2}	21	digital supply ground 2
V_{DDD2}	22	digital supply voltage 2
CLP	23	clamping input
CLREF	24	current reference level input for ADCs
CREFL	25	converter reference LOW level input
CREFH	26	converter reference HIGH level input
V_{DDA3}	27	analog supply voltage 3
INB	28	BLUE analog input
V_{SSA3}	29	analog supply ground 3
V_{DDA2}	30	analog supply voltage 2
ING	31	GREEN analog input
V_{SSA2}	32	analog supply ground 2
V_{DDA1}	33	analog supply voltage 1
INR	34	RED analog input
V_{SSA1}	35	analog supply ground 1
SLT	36	select input buffer ratio
n.c.	37	not connected
R0	38	RED data output; bit 0 (LSB)
n.c.	39	not connected
R1	40	RED data output; bit 1

SYMBOL	PIN	DESCRIPTION
R2	41	RED data output; bit 2
R3	42	RED data output; bit 3
R4	43	RED data output; bit 4
R5	44	RED data output; bit 5 (MSB)

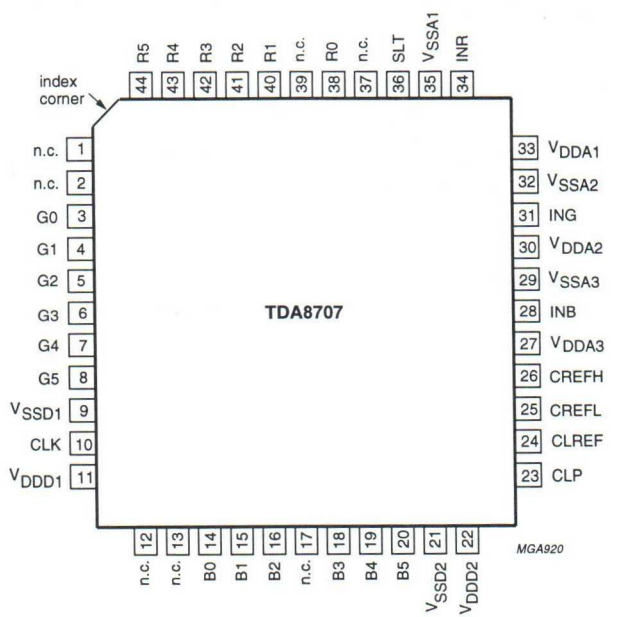


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pins 27, 30 and 33)		−0.3	+6.5	V
V_{DDD}	digital supply voltage (pins 11 and 22)		−0.3	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}		−0.5	+0.5	V
V_I	input voltage (pins 28, 31 and 34)	referenced to V_{SSA}	−	V_{DDA}	V
$V_{i(p-p)}$	AC input voltage for switching (pins 10 and 23; peak-to-peak value)	referenced to V_{SSD}	−	V_{DDD}	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} short-circuited together; $V_{DDA} - V_{DDD} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; SLT = 0 V; CREFH = 2.0 V, CREFL = 0.5 V; $C_L = 15$ pF; typical values measured at $V_{DDA} = V_{DDD} = 5$ V; $V_{SSA} = V_{SSD} = 0$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage	note 1	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	note 1	4.5	5.0	5.5	V
I_{DDA}	analog supply current	note 2	–	60	77	mA
I_{DDD}	digital supply current	$f_{clk} = 35$ MHz	–	5	8	mA
Inputs						
DIGITAL INPUTS (CLK: PIN 10 AND CLP: PIN 23)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{LI}	input leakage current		–10	–	+10	µA
C_I	input capacitance		–	7	–	pF
CLAMP AND REFERENCES (CLREF: PIN 24, CREFL: PIN 25 AND CREFH: PIN 26)						
A_{CL}	clamping accuracy		–	±0.5	–	LSB
I_{CL}	input clamping current		–200	–	+400	µA
C_{CL}	external series clamping capacitor		10	22	–	nF
R_{CLREF}	external resistor on CLREF pin for current reference of converter	note 2	12	15	–	kΩ
V_{REFH}	converter reference voltage HIGH level applied to CREFH pin	referenced to V_{SSA}	1.5	2.0	2.5	V
V_{REFL}	converter reference voltage LOW level applied to CREFL pin	referenced to V_{SSA}	0.25	0.5	0.75	V
ΔREF	reference voltage difference between V_{REFH} and V_{REFL}	note 3	–	1.5	–	V
Z_{CREF}	internal ladder impedance between pins CREFH and CREFL		–	300	–	Ω
ANALOG INPUTS (INR: PIN 34, ING: PIN 31 AND INB: PIN 28)						
$V_{I(p-p)}$	full-range input voltage (peak-to-peak value)	SLT = logic 0; gain = 1.5; note 4	–	1.0	–	V
		SLT = logic 1; gain = 2.0; note 4	–	0.75	–	V
I_I	input current	clamp off	–	5	100	nA
C_I	input capacitance		–	7	15	pF
INPUT ISOLATION						
α_{ct}	crosstalk between INR, ING and INB		–	–	–40	dB
Outputs (R0 to R5: pins 38 and 40 to 44; G0 to G5: pins 3 to 8; B0 to B5: pins 14 to 16 and 18 to 20)						
V_{OL}	LOW level output voltage		0	–	0.5	V
V_{OH}	HIGH level output voltage		4.0	–	V_{DDD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK INPUT CLK (see Fig.3)						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		11	–	–	ns
t_{CPL}	clock pulse width LOW		11	–	–	ns
Analog signal processing (50% clock duty cycle)						
LINEARITY						
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.35	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.35	±0.6	LSB
BANDWIDTH (f_{clk} = 35 MHz); see Fig.5 and note 7						
B	–3 dB analog bandwidth		–	9	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full scale square wave	–	13	16	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full scale square wave	–	11	14	ns
HARMONICS; note 6						
f_1	fundamental harmonic		–	–	0	dB
f_{all}	harmonics, all components		–	–38	–	dB
EFFECTIVE BITS; note 8						
EB	effective bits		–	5.3	–	bits
DIFFERENTIAL GAIN; note 5						
G_{diff}	differential gain	PAL modulated ramp	–	3	–	%
DIFFERENTIAL PHASE; note 5						
φ_{diff}	differential phase	PAL modulated ramp	–	2	–	deg
Timing (see Figs 3 and 4)						
t_{dS}	sampling delay time		–	3	–	ns
t_h	output hold time		6	–	–	ns
t_d	output delay time	note 9	–	–	16	ns
t_r	clock rise time		3	5	–	ns
t_f	clock fall time		3	5	–	ns
t_{CLP}	active clamping duration		3	4	–	µs

Notes to the "Characteristics"

1. V_{DDA} and V_{DDD} should be supplied from the same power supply and decoupled separately.
2. The analog supply current is directly proportional to the series resistance between V_{DDA} and CLREF.
3. CREFH and CREFL are connected respectively to the top and bottom reference ladders of the 3 analog-to-digital converters.
4. $V_{I(p-p)} = (V_{REFL} - V_{REFH})$/buffer gain factor. See Table 2 for gain factor selection. When clamping at code 0 is used, active video signal amplitude V_{ACT} should be: $V_{ACT} = \frac{(V_{REFH} - V_{REFL})}{\text{buffer gain factor}}$
5. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
6. $V_{I(p-p)} = \Delta REF$ with $f_i = 4.43$ MHz.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. The number of effective bits is measured with a clock frequency of 35 MHz. This value is given for a 4.43 MHz input frequency.
9. Output data acquisition: output data is available after the maximum delay time of t_d.

Table 1 Output coding (V_{REFH} = 2.0 V; V_{REFL} = 0.5 V referenced to V_{SSA}, SLT = logic 0; buffer ratio = 1.5)

STEP	$V_{I(p-p)}$	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
–	$<0.333 = \frac{V_{REFL}}{1.5}$	0	0	0	0	0	0
0	0.349	0	0	0	0	0	0
1	0.364	0	0	0	0	0	1
.	.	.		.	.	.	.
62	1.317	1	1	1	1	1	0
63	1.333	1	1	1	1	1	1
–	$>1.333 = \frac{V_{REFH}}{1.5}$	1	1	1	1	1	1

Table 2 Mode selection

SLT	BUFFER RATIO	$V_{I(p-p)}$ FULL SCALE
0	1.5	$\frac{V_{REFH} - V_{REFL}}{1.5}$
1	2.0	$\frac{V_{REFH} - V_{REFL}}{2.0}$

TIMING DIAGRAMS

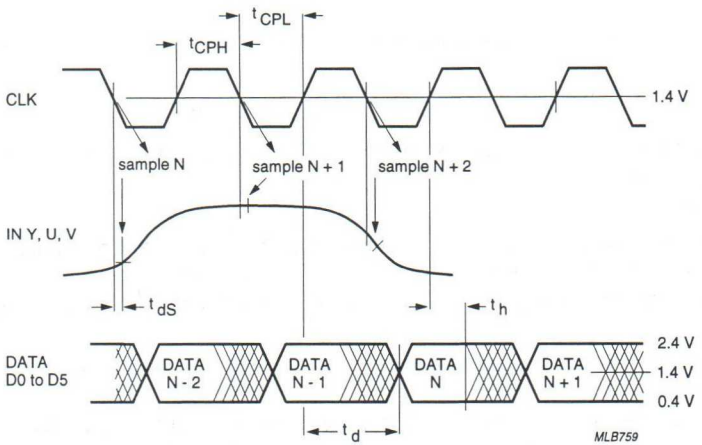


Fig.3 Input timing.

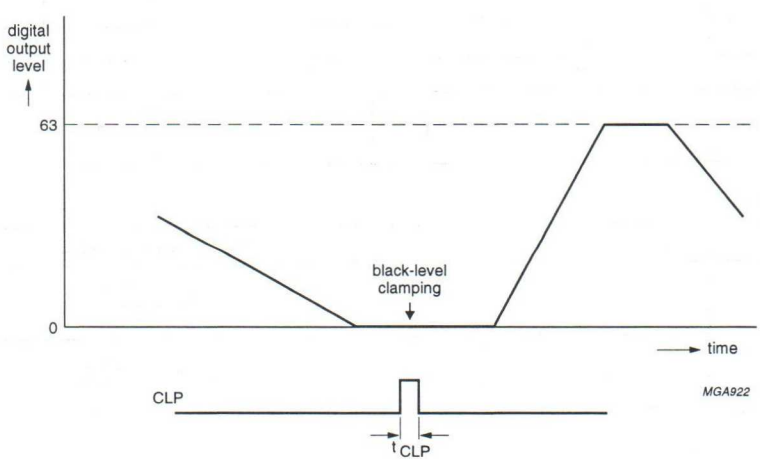


Fig.4 Clamp timing.

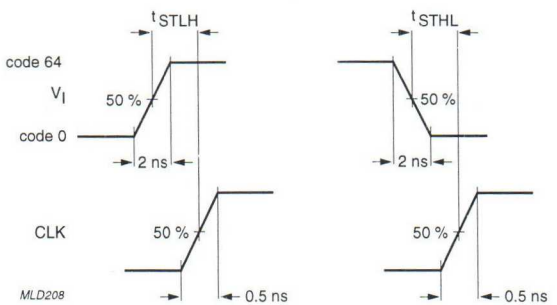
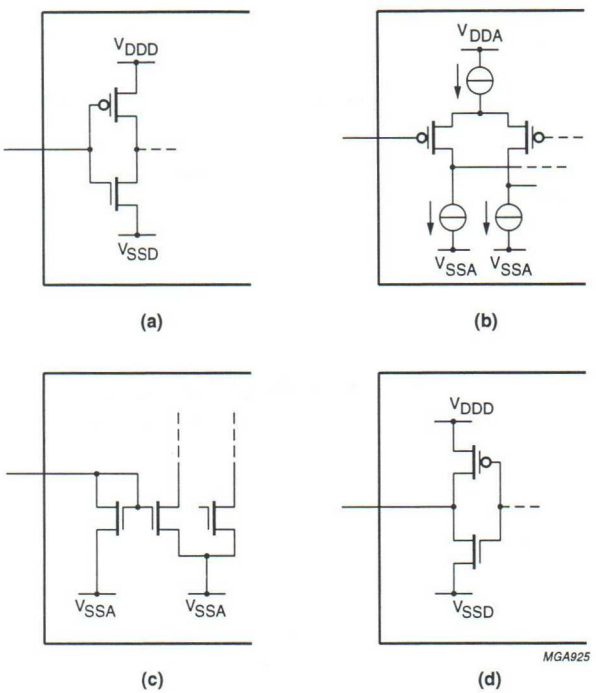


Fig.5 Analog input settling-time diagram.

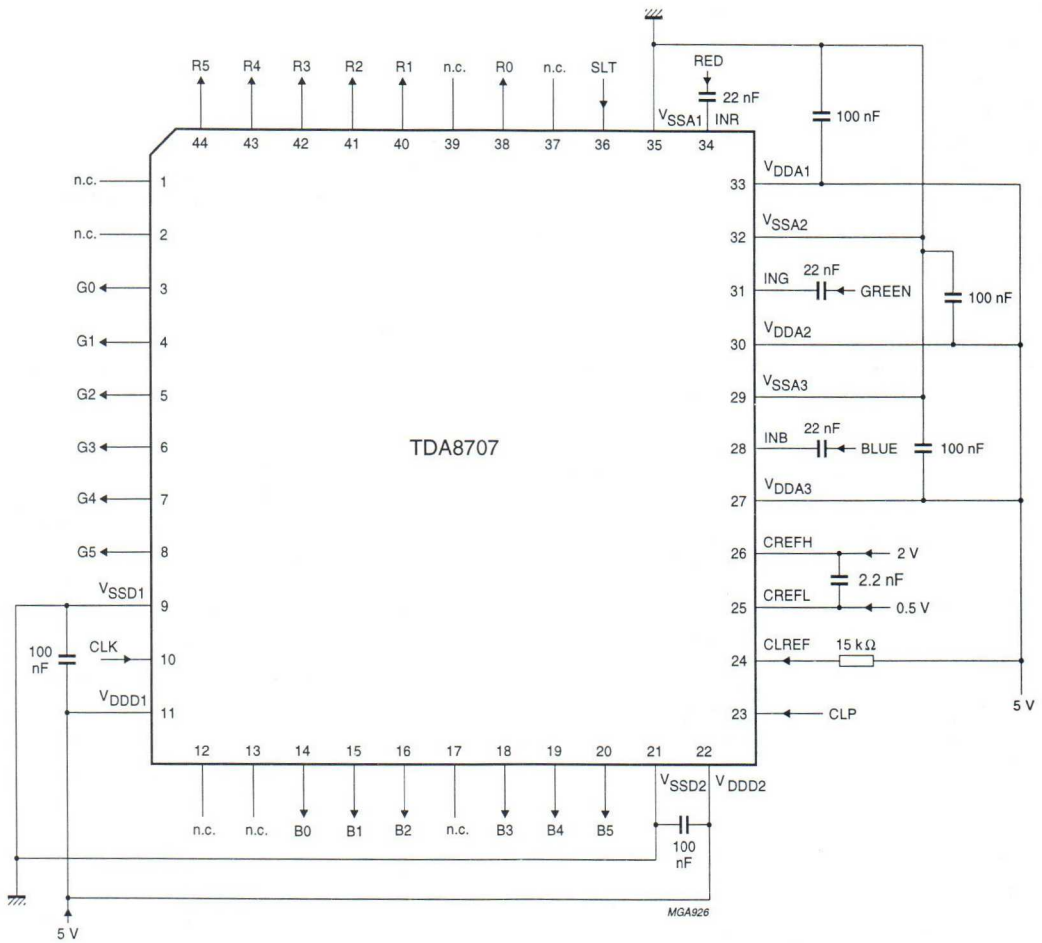
INTERNAL CIRCUITRY



(a) Digital inputs; pins 10, 23 and 36.
(b) Analog inputs; pins 28, 31 and 34.
(c) Current reference; pin 24.
(d) Digital outputs; pins 3 to 8, 14 to 16, 18 to 20 and 40 to 44.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.

Supplies are not connected internally; also applicable to grounds.

The internal reference currents are set by the series resistor between pin V_{DDA} and CLREF. The resistor value should be in the range of 12 kΩ and 15 kΩ.

It is recommended, if possible, to connect pins 1, 2, 12, 13, 17, 37 and 39 to V_{SSD}.

Fig.7 Application diagram.

Video analog input interface TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

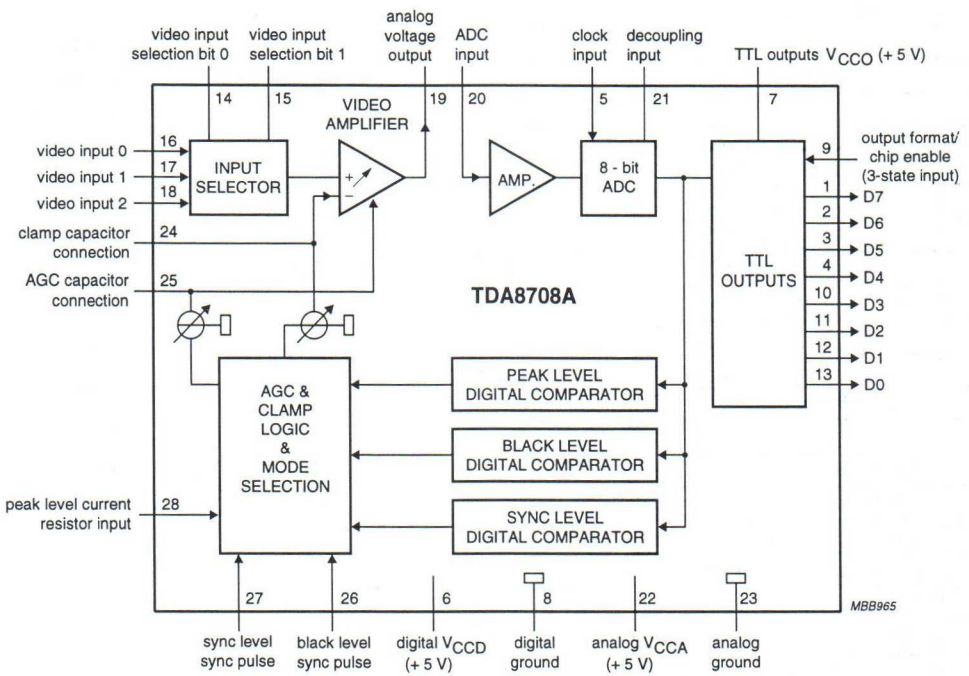


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

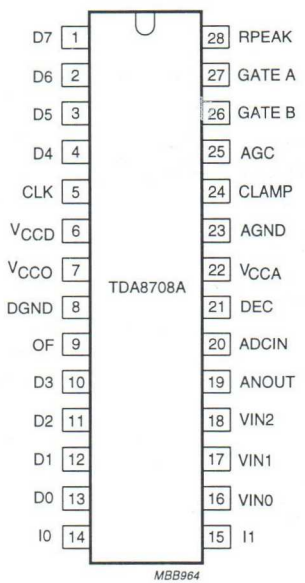


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0 TO 2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
t_W	pulse width	see Fig.5	2	–	–	μs
RPEAK INPUT (PIN 28)						
$I_{28(min)}$	minimum peak level current	R_{28} = 0 Ω	–	80	150	μA
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	note 3	–	V_{CCA} – 2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{clk}= 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	300	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 5)						
V_{20}	input voltage	digital output = 00	–	$V_{CCA} - 2.42$	–	V
V_{20}	input voltage	digital output = 255	–	$V_{CCA} - 1.41$	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = −0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	−20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.3; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.3; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	−55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	19	25	ns
t_{dDZ}	3-state delay time; output disable		–	14	20	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)} = 1.33$ V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUTC(p-p)}}{V_{ANOUTY\ (RMS\ noise)}} \text{ at } B = 5 \text{ MHz}.$$

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for $V_I = 1$ V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave ($f_i = 4.4$ MHz; $f_{clk} = 27$ MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE(2)
1	1	output < 255	–2.5 µA	1
		output > 255	I_{AGCM}	1
0	X(1)	output < 248	0 µA	2
		output > 248	I_{AGCM}	2
1	0	output < 0	+2.5 µA	2
		0 < output < 248	–2.5 µA	2
		output > 248	I_{AGCM}	2

Note

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0	I_{CLAMPM}	1
		output > 0	–2.5 µA	1
X(1)	0	X(1)	0 µA	2
0	1	output < 64	+50 µA	2
		64 < output	–50 µA	2

Note

1. X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit(1)	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} – 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} – 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

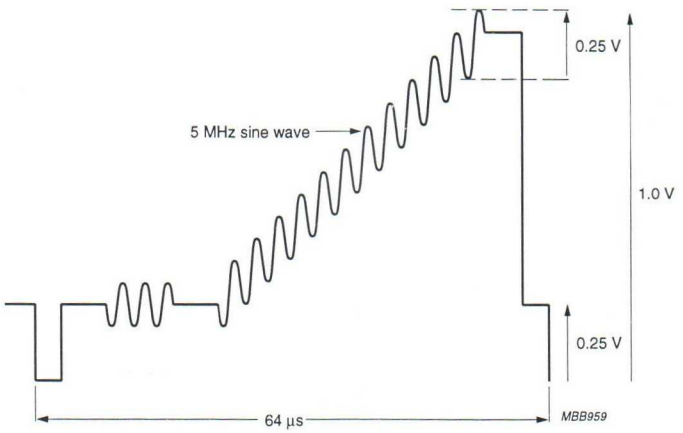


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

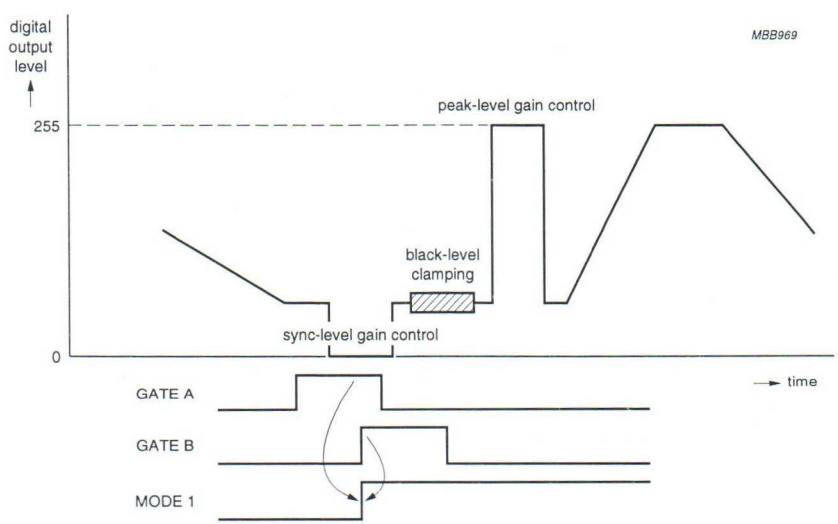


Fig.4 Control mode 1.

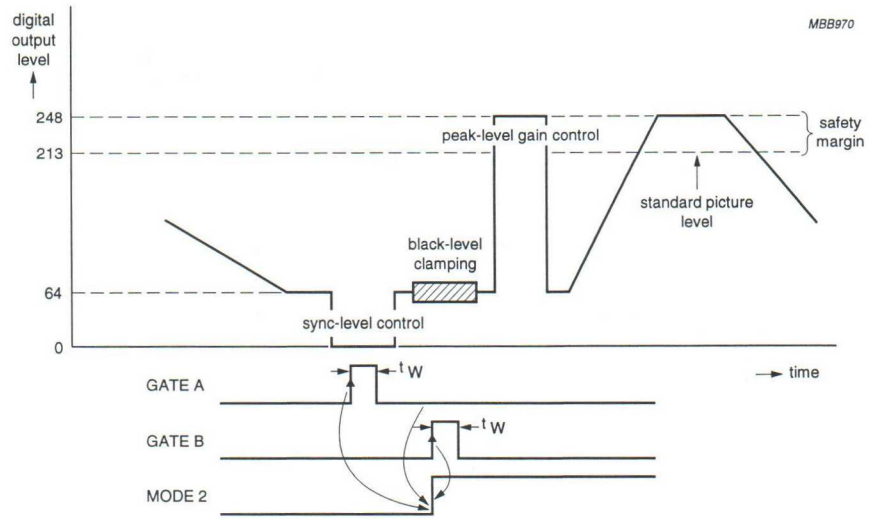


Fig.5 Control mode 2.

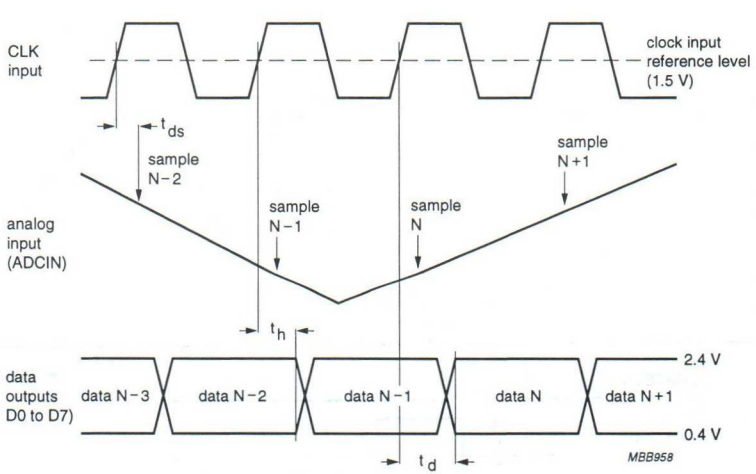


Fig.6 Timing diagram for data output.

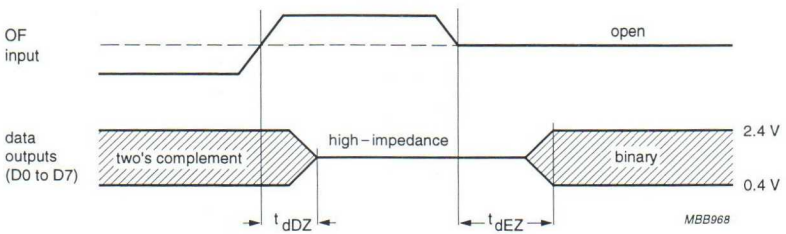


Fig.7 Output format timing diagram.

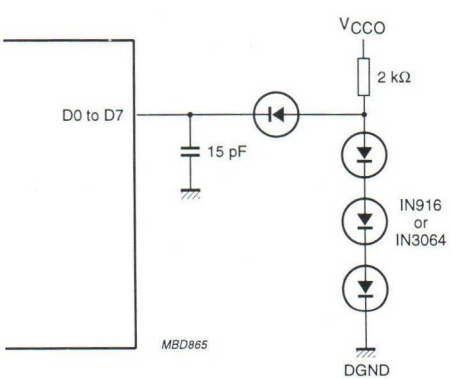


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

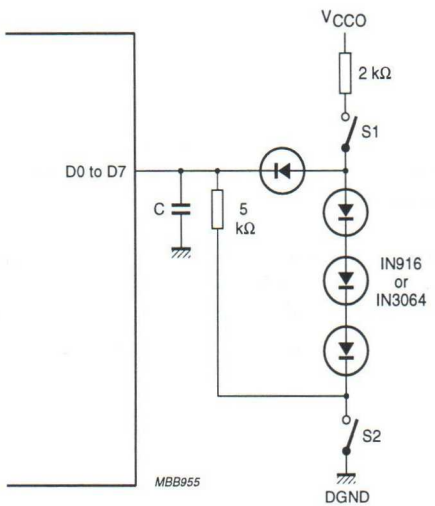
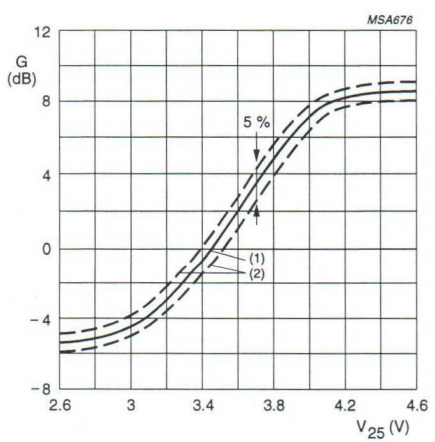


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

INTERNAL PIN CIRCUITRY

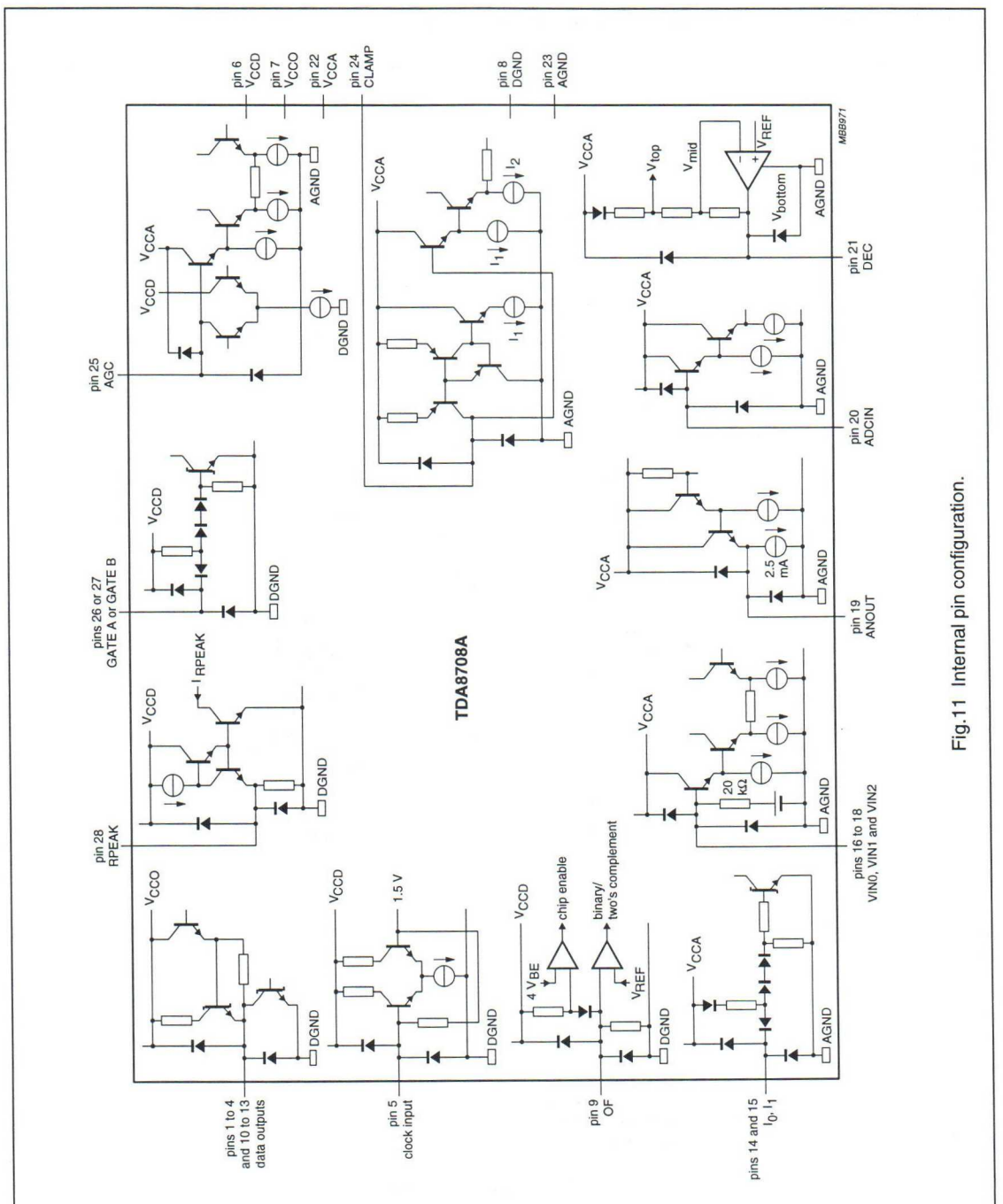
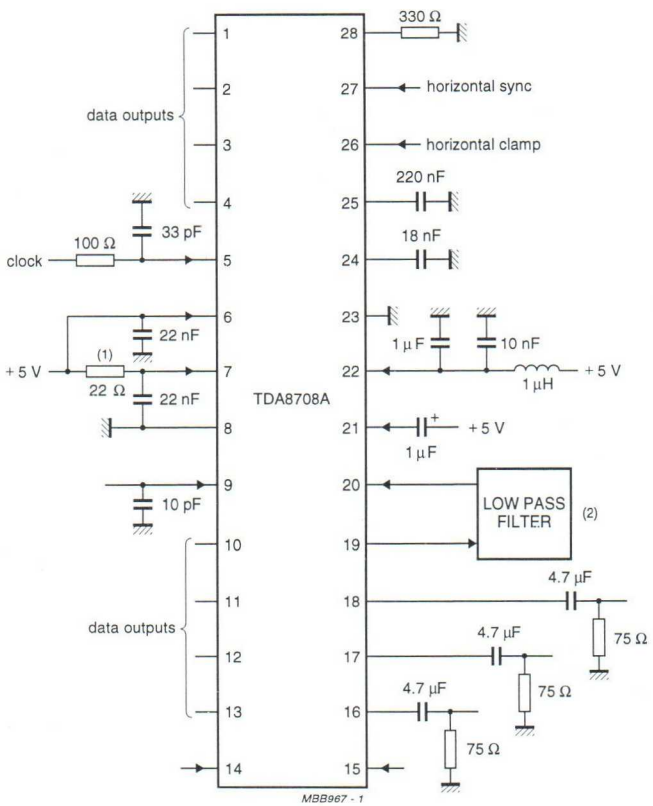


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

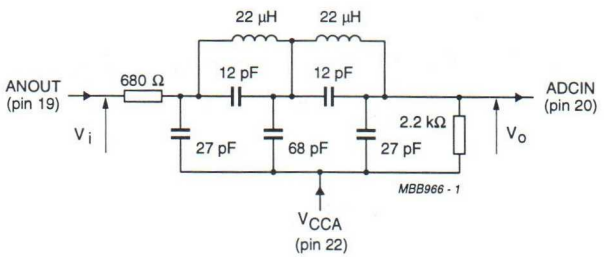
Additional information can be found in the laboratory report *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.

(2) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

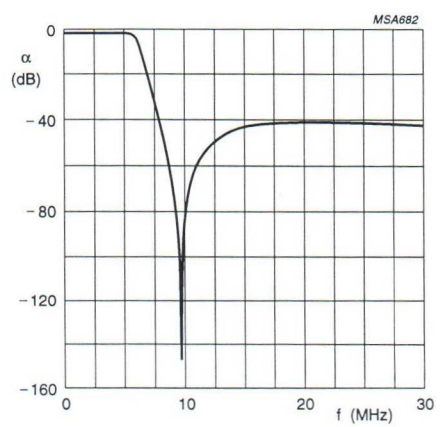
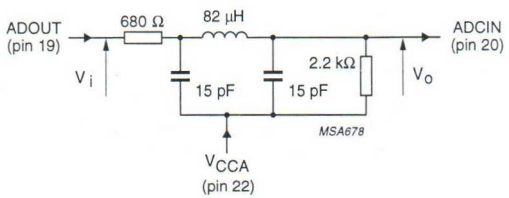


Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig. 13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.75 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

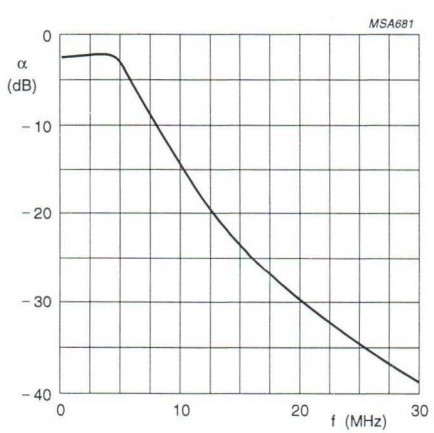


Fig.16 Frequency response for filter shown in Fig.15.

Characteristics of Fig. 15

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB.

Video analog input interface TDA8708B

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required
- The TDA8708B has no white peak control in mode 2 whereas the TDA8708A has control in modes 1 and 2.
- In-range output (not TTL levels).

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708B is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708B	28	DIP	plastic	SOT117-1
TDA8708BT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

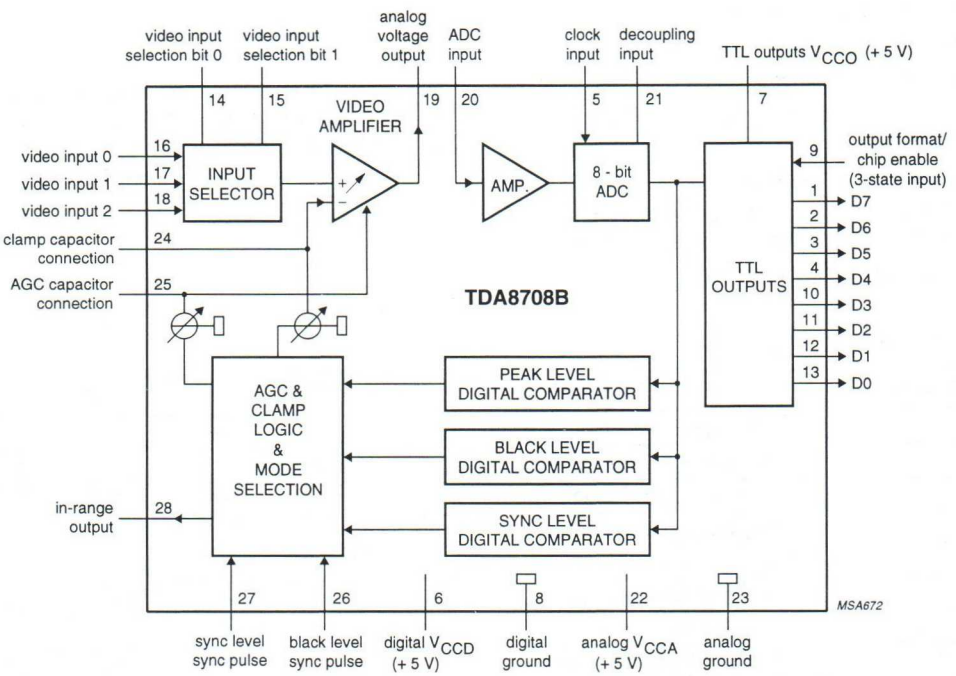


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
IR	28	in-range output

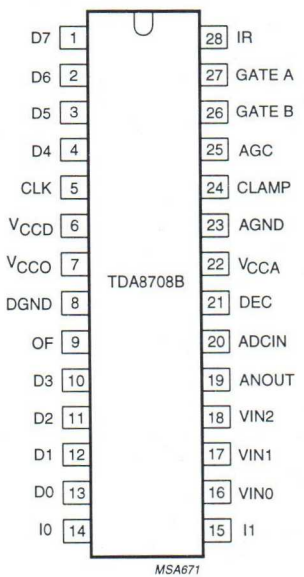


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708B provides a simple interface for decoding video signals.

The TDA8708B operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708B automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708B is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The voltage across the capacitor connected to the AGC pin controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The use of nominal signals will prevent the output from exceeding a digital code of 213.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	TTL output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
t_W	pulse width	see Fig.5	2	–	–	μs
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	note 3	–	V_{CCA} – 2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	300	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 5)						
V_{20}	input voltage	digital output = 00	–	$V_{CCA} - 2.42$	–	V
V_{20}	input voltage	digital output = 255	–	$V_{CCA} - 1.41$	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
IR OUTPUT (PIN 28)						
V_{OL}	LOW level output voltage		–	–	1.7	V
V_{OH}	HIGH level output voltage		1.9	–	–	V
I_O	output current		–500	–	–	μA
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.7; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.7; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	19	25	ns
t_{dDZ}	3-state delay time; output disable		–	14	20	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUTC\,(p-p)}}{V_{ANOUTY\,(RMS\ noise)}}$$ at B = 5 MHz.

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I\,(00)} - V_{I\,(FF)}) + (V_{I\,(00)} - V_{I\,(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE[2]
1	1	output < 255	–2.5 µA	1
		output > 255	130 µA	1
0	X[1]	–	0 µA	2
1	0	output < 0	+2.5 µA	2
		output > 0	–2.5 µA	2

Notes

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0	130 µA	1
		output > 0	–2.5 µA	1
X[1]	0	X	0 µA	2
0	1	output < 64	+50 µA	2
		64 < output	–50 µA	2

Note

1. X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit[1]	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} – 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} – 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

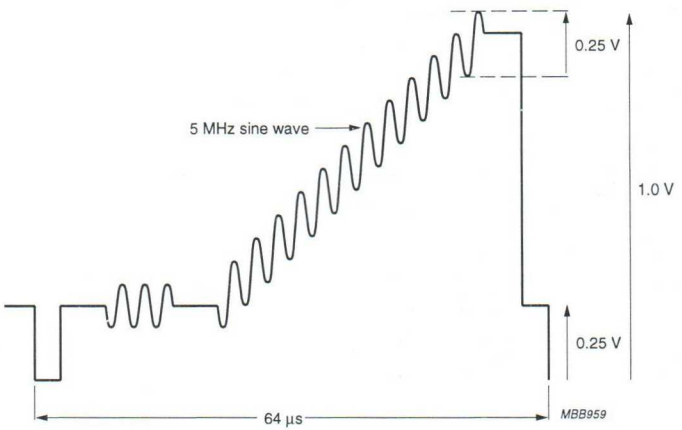


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

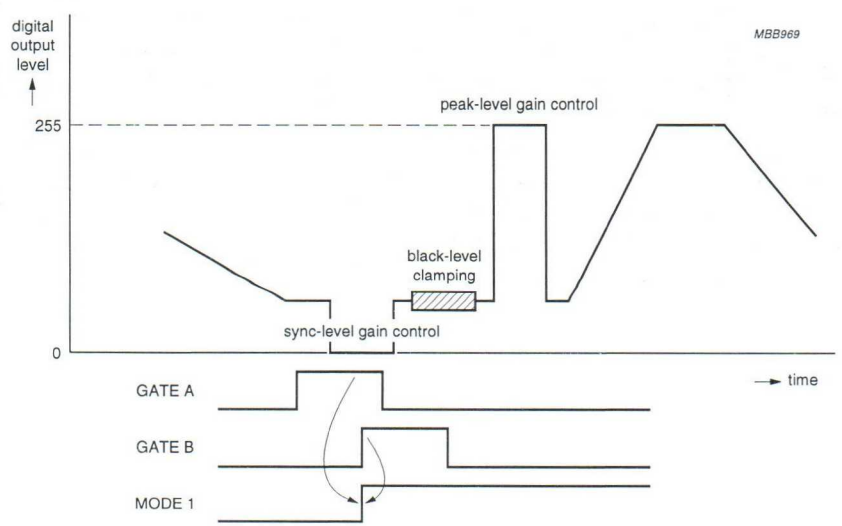


Fig.4 Control mode 1.

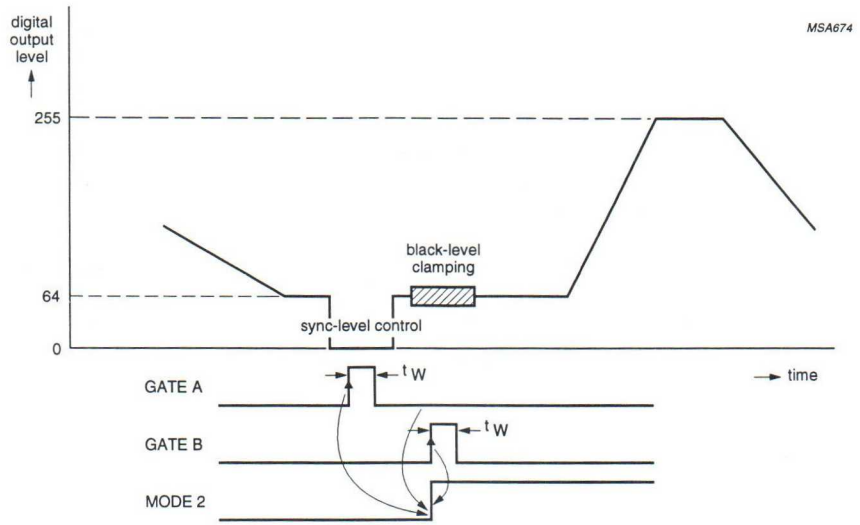


Fig.5 Control mode 2.

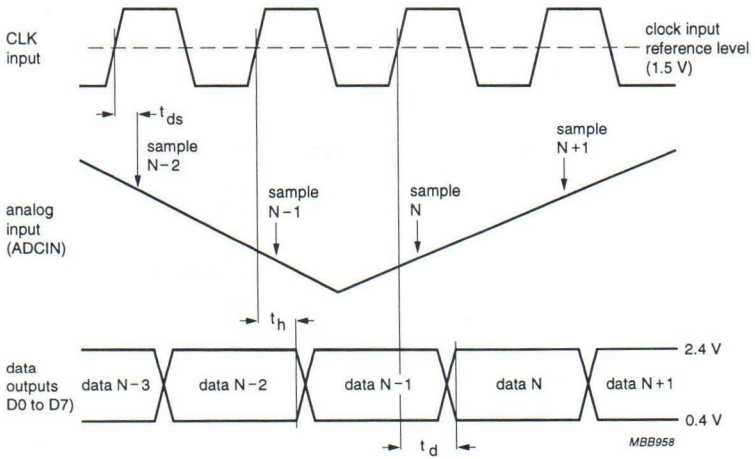


Fig.6 Timing diagram for data output.

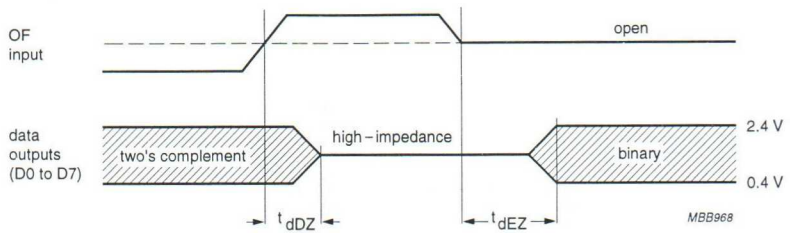


Fig.7 Output format timing diagram.

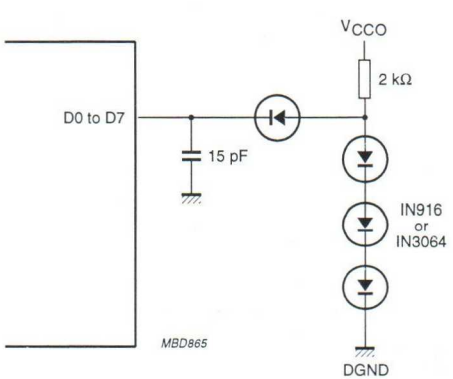


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

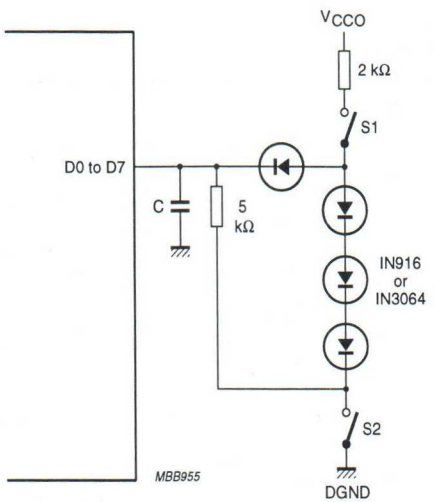
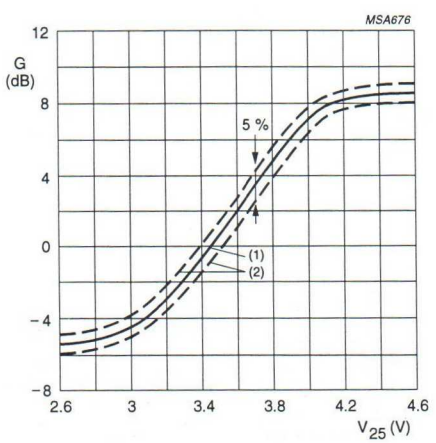


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

INTERNAL PIN CIRCUITRY

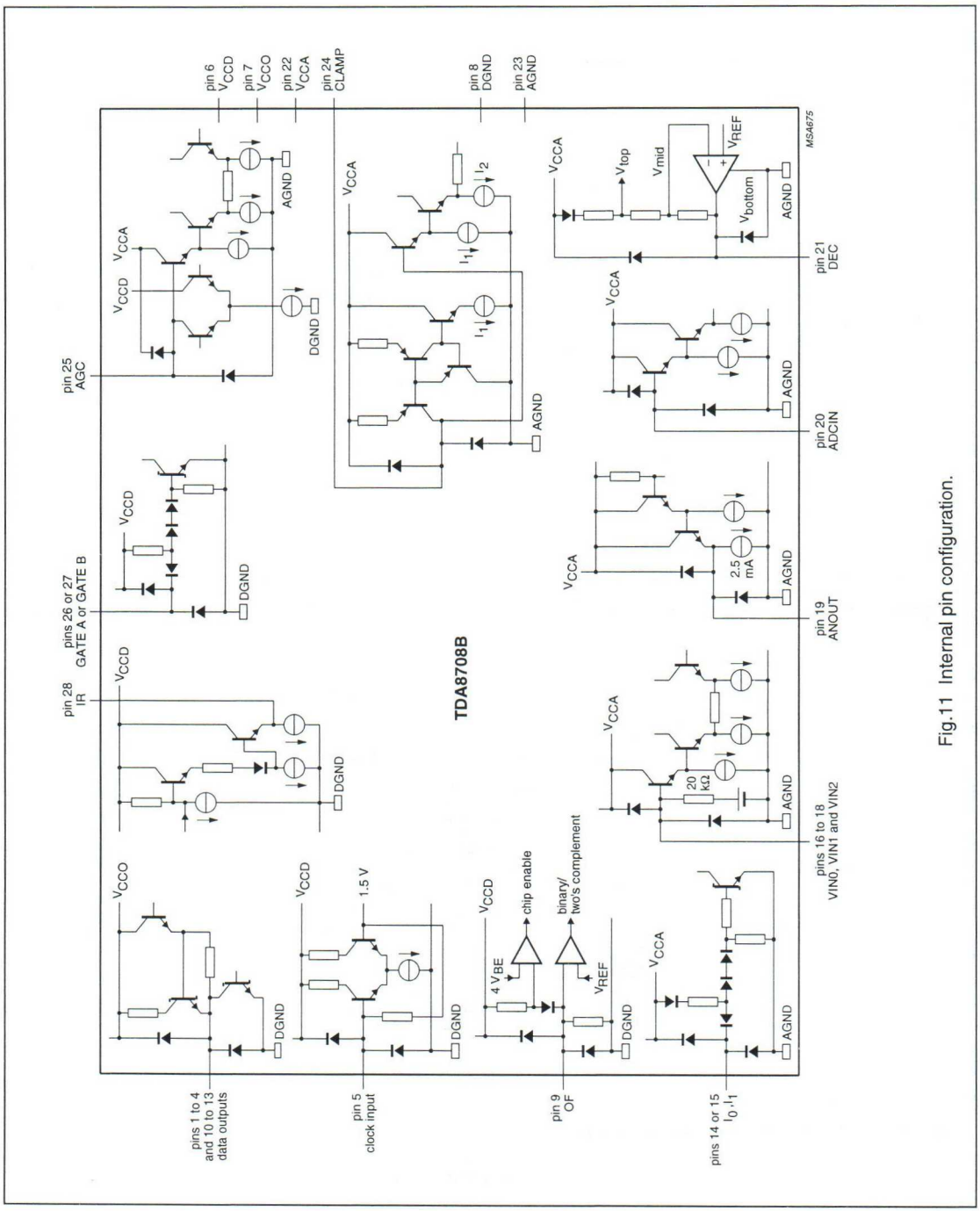
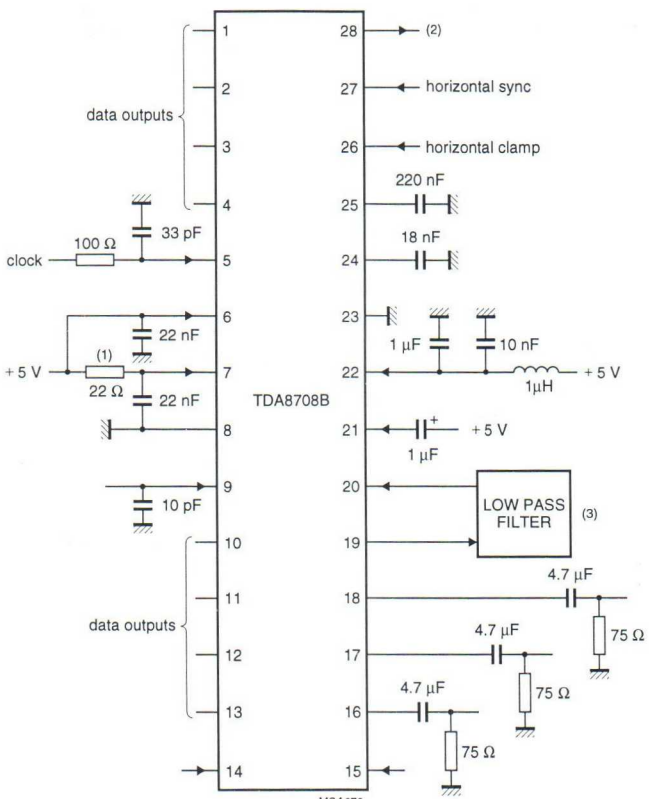


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report of TDA8708A *"FBL/AN9308"*.

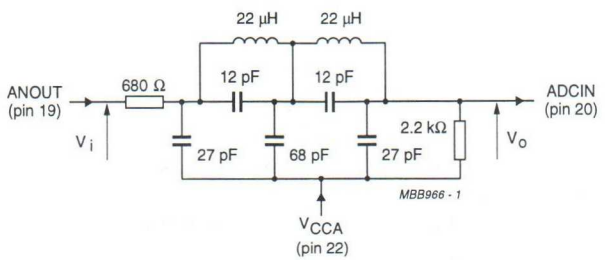


(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708B interfaces with a capacitive CMOS load device.

(2) When IR is not used, it must be connected to ground via a 47 pF capacitor.

(3) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

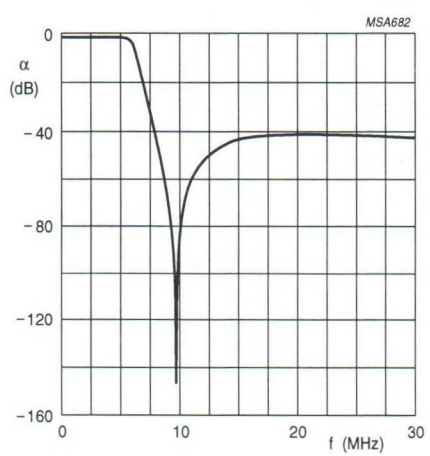
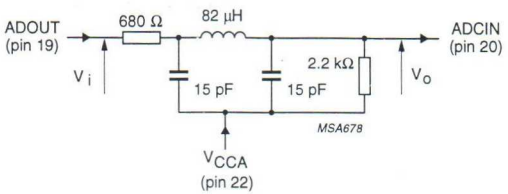


Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig.14

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.75 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

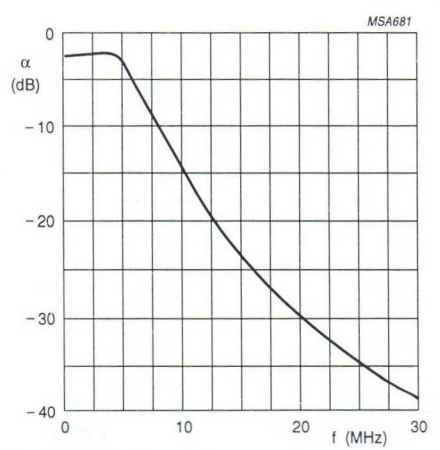


Fig.16 Frequency response for filter shown in Fig.15.

Characteristics of Fig.16

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB.

Video analog input interface TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

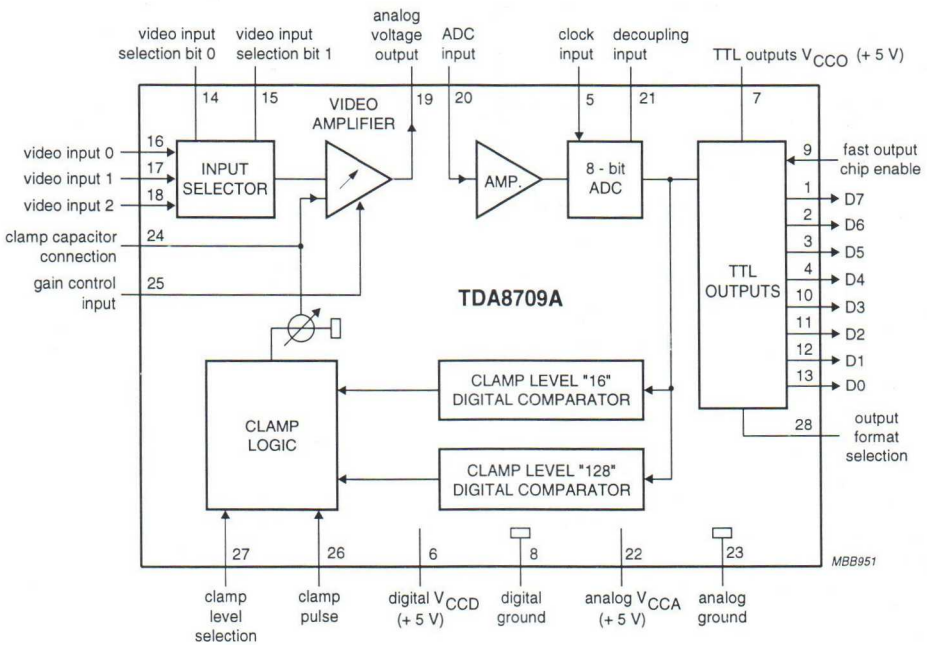


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

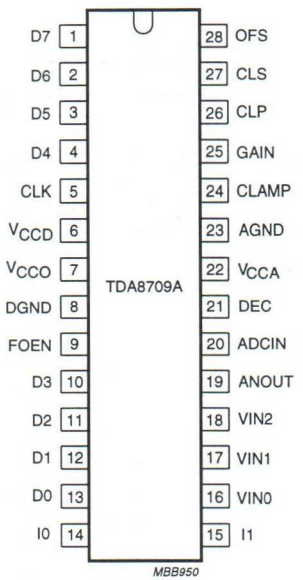


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	TTL output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	–	12	16	mA
Preamplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
CLS, OFS AND CLP TTL INPUTS (SEE FIG.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
t_{CLP}	clamp pulse width		2	–	–	µs
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	–	1.8	–	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	–	3.8	–	V
I_I	input current		–	1.0	–	µA
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 2			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3.0 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	–	V_{CCA} – 2.02	–	V
V_{19}	DC output voltage for black level	CLS = logic 0	–	V_{CCA} – 2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V; note 3	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.9	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\lvert Z_i \rvert$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V_{20}	input voltage	digital output = 00	–	$V_{CCA} - 2.52$	–	V
V_{20}	input voltage	digital output = 255	–	$V_{CCA} - 1.52$	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.5; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.7)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.6; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.6; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	16	25	ns
t_{dDZ}	3-state delay time; output disable		–	12	25	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

$$\frac{S}{N} = 20 \log \frac{V_{ANOUT\,(p-p)}}{V_{ANOUT\,(RMS\ noise)}} \text{ at } B = 5 \text{ MHz}.$$

5. The voltage ratio is expressed as:

$$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G} \text{ for } V_I = 1 \text{ V (p-p)}, \text{ gain at 100 kHz} = 1 \text{ and 1 V supply variation.}$$

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I\,(00)} - V_{I\,(FF)}) + (V_{I\,(00)} - V_{I\,(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128	+50 μA
		output > 128	−50 μA
X[1]	0	X	0 μA
0	1	output < 16	+50 μA
		16 < output	−50 μA

Note

1. X = don't care.

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 4 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} – 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} – 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

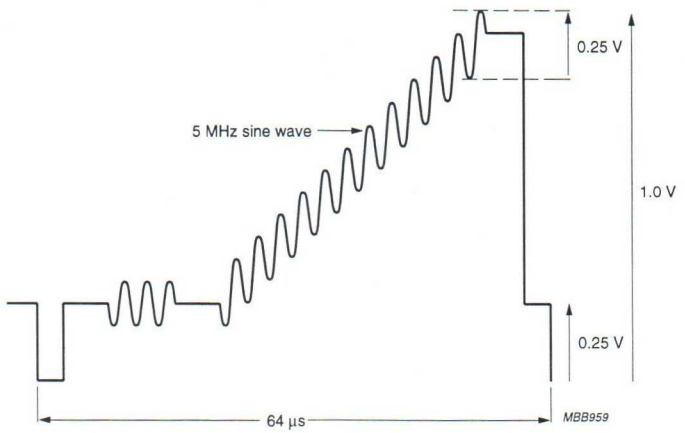


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

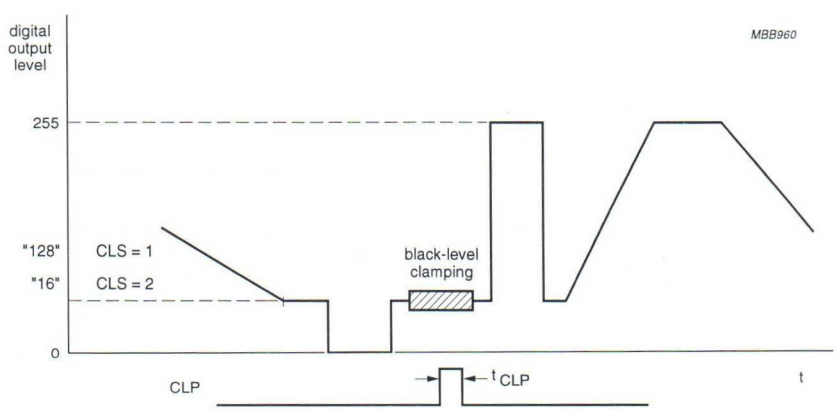


Fig.4 Control mode selection.

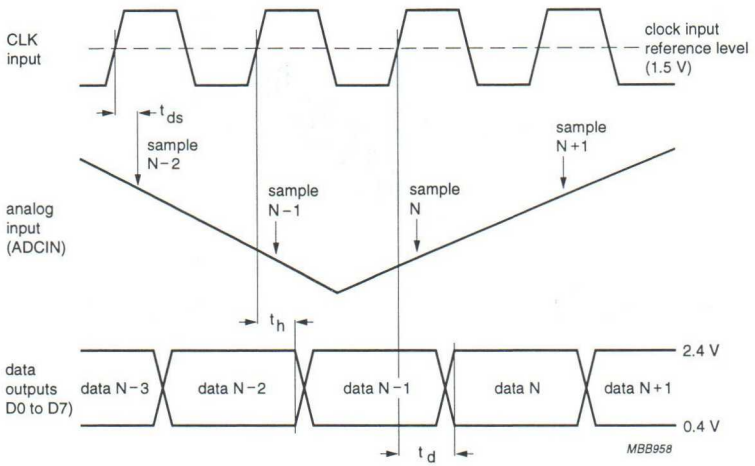


Fig.5 Timing diagram.

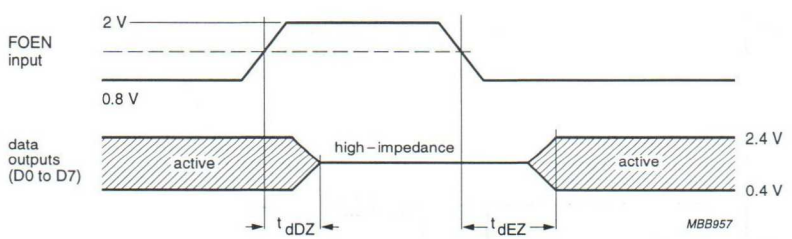


Fig.6 Output format timing diagram.

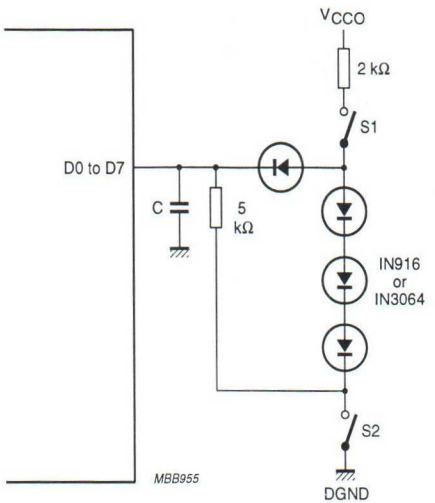


Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

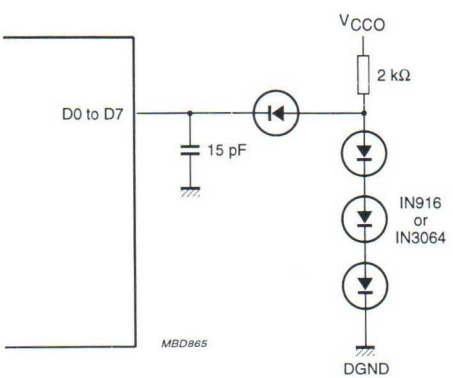
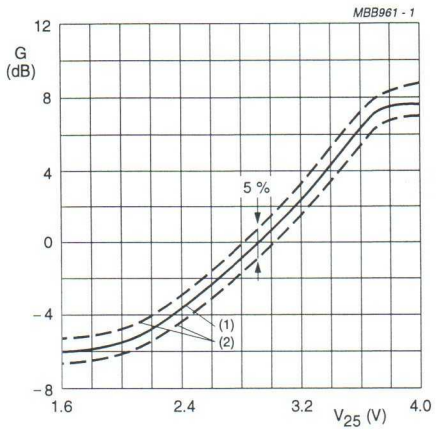


Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).



(1) Typical value ($V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C).
(2) Minimum and maximum values (temperature and supply).

Fig.9 Typical gain control curve as a function of gain voltage.

INTERNAL PIN CIRCUITRY

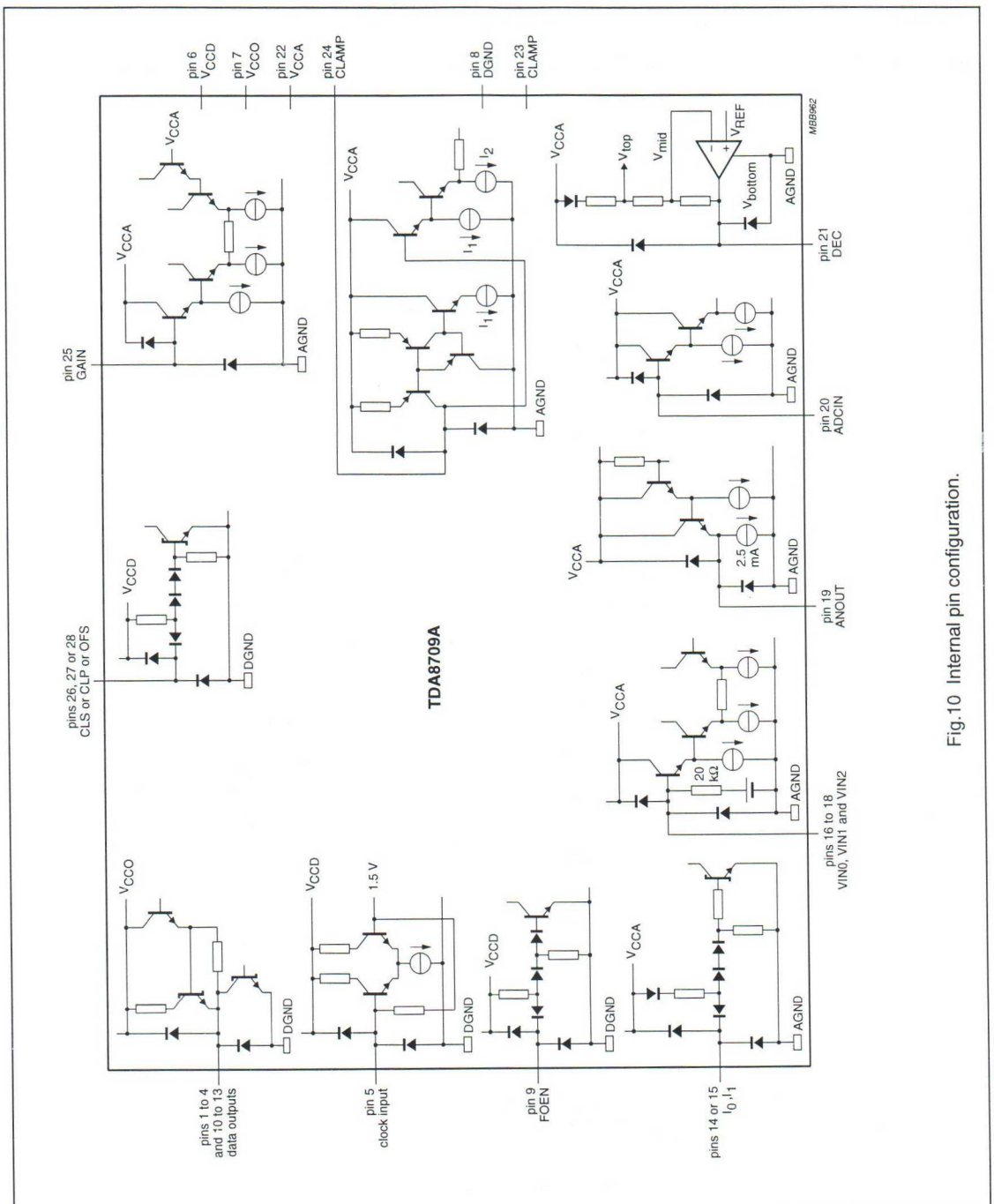
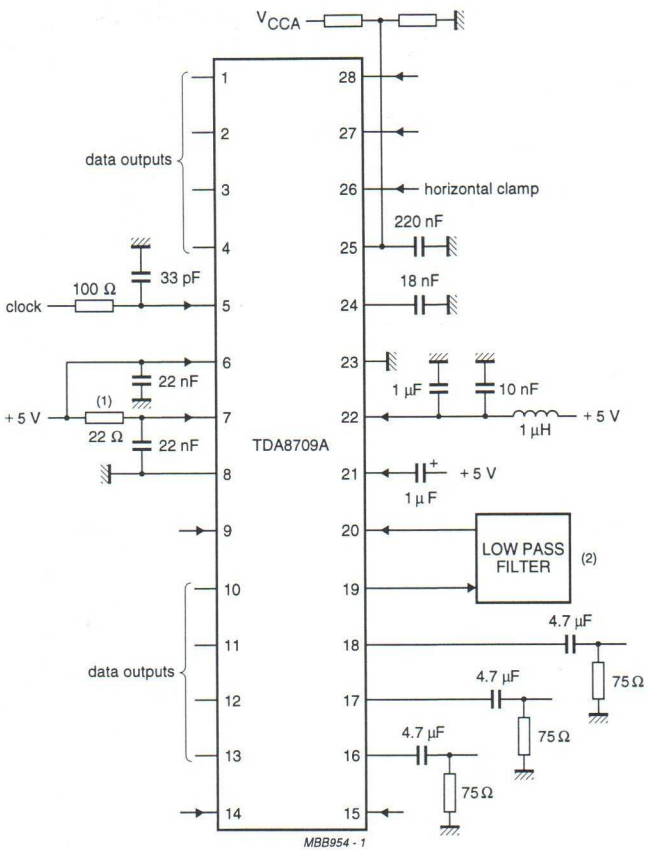


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

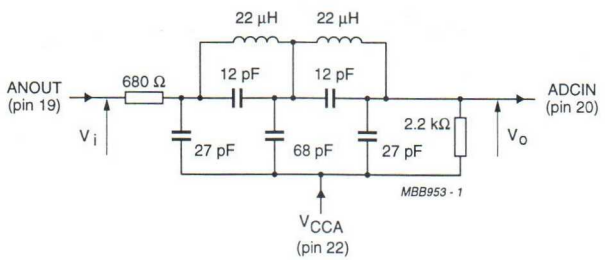
Additional information can be found in the laboratory report of TDA8708A *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.

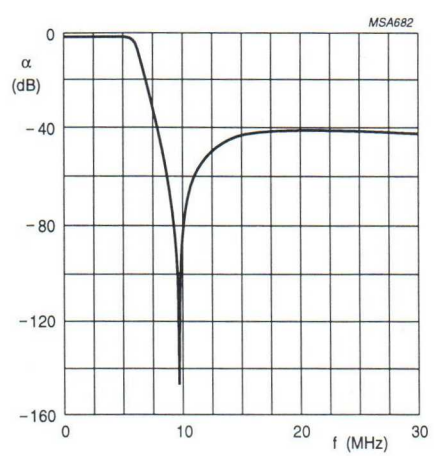
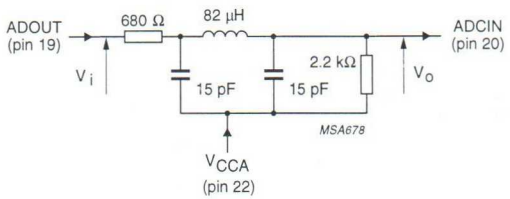


Fig.13 Frequency response for filter shown in Fig.12.

Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB
- f_{notch} = 9.65 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

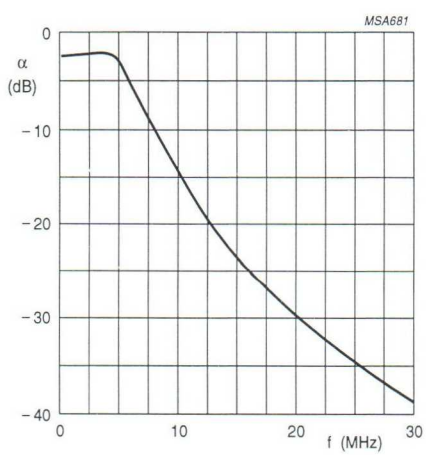
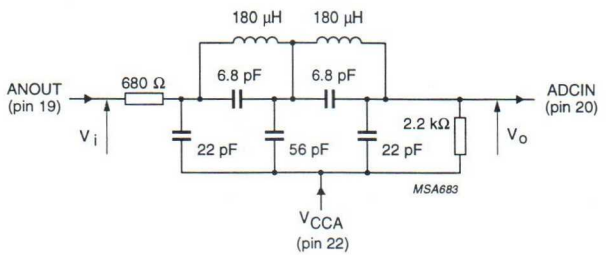


Fig.15 Frequency response for filter shown in Fig.14.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

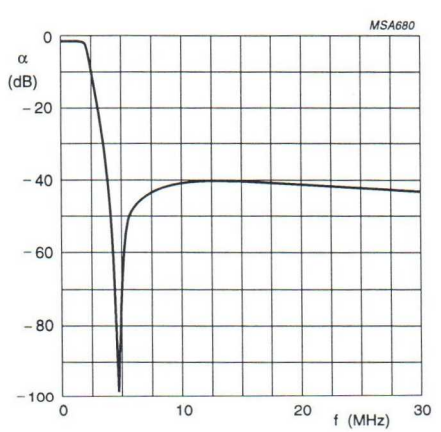
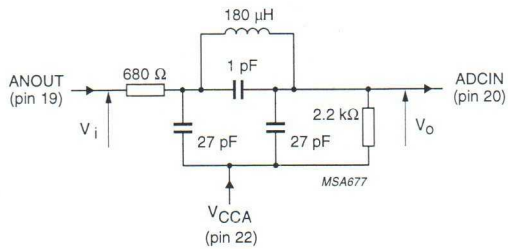


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 2.3 MHz at −3 dB
- f_{notch} = 4.5 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

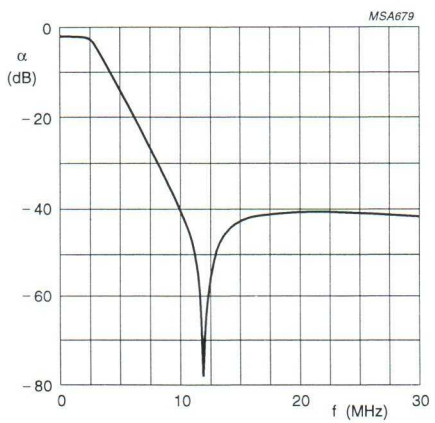


Fig.19 Frequency response for filter shown in Fig.18.

Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.3$ dB
- f = 2.8 MHz at –3 dB
- f_{notch} = 11.9 MHz.

8-bit digital-to-analog converters TDA8712; TDF8712

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required
- Temperature range
  - TDA8712: 0 to 70 °C
  - TDF8712: –40 to +85 °C.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs
- Industrial and automotive.

GENERAL DESCRIPTION

The TDA8712 and TDF8712 are 8-bit digital-to-analog converters (DACs) for video and other applications. They convert the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8712	16	DIP	plastic	SOT38-1
TDF8712	16	DIP	plastic	SOT38-1
TDA8712T	16	SO16L	plastic	SOT162-1
TDF8712T	16	SO16L	plastic	SOT162-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
$\Delta V_{OUT(p-p)}$	full-scale analog output voltage differences between V_{OUT} and $\overline{V}_{OUT}$ (peak-to-peak value)	Z_L = 10 kΩ; note 2	−1.45	−1.60	−1.75	V
		Z_L = 75 Ω; note 2	−0.72	0.80	−0.88	V
ILE	DC integral linear error		–	±0.3	±0.5	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
$f_{clk(max)}$	maximum conversion rate		50	–	–	MHz
B	−3 dB analog bandwidth	f_{clk} = 50 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation					
	TDA8712		160	250	340	mW
	TDF8712		170	250	325	mW

Notes

1. D0 to D7 are connected to V_{CCD} and CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V}_{OUT}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

BLOCK DIAGRAM

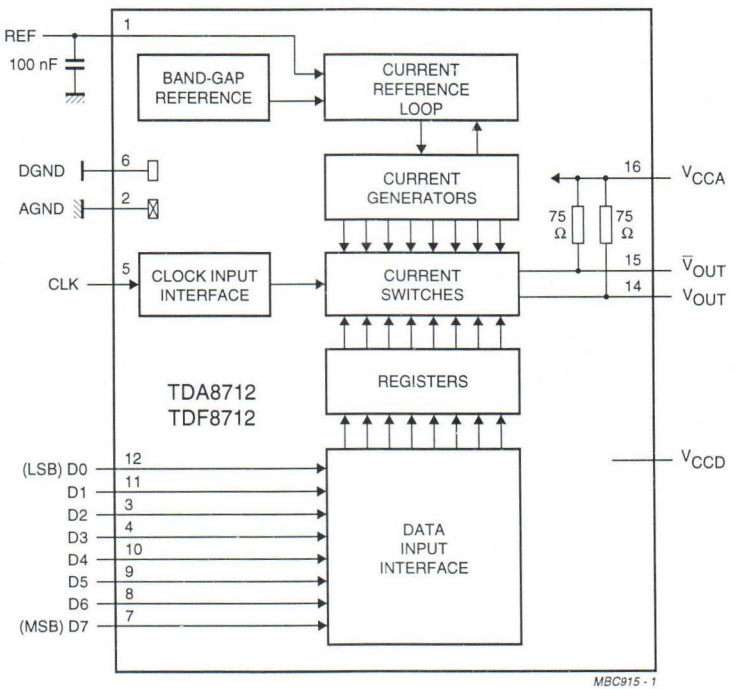


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7 (MSB)
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0 (LSB)
V_{CCD}	13	digital supply voltage (+5 V)
V_{OUT}	14	analog output voltage
$\overline{V}_{OUT}$	15	complimentary analog output voltage
V_{CCA}	16	analog supply voltage (+5 V)

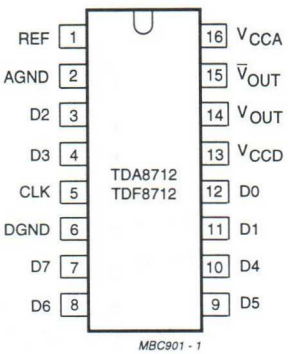


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}	−0.5	+0.5	V
ΔV_{GND}	ground voltage differences between V_{AGND} and V_{DGND}	−0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{tot}	total output current ($I_{OUT} + \bar{I}_{OUT}$; pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature			
	TDA8712	0	+70	°C
	TDF8712	−40	+85	°C
T_j	junction temperature	−	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT38-1	70	K/W
	SOT162-1	90	K/W

CHARACTERISTICS

$V_{CCA} = V_{16}$ to V_2 = 4.5 to 5.5 V (TDA8712) = 4.75 to 5.25 V (TDF8712); $V_{CCD} = V_{13}$ to V_6 = 4.5 to 5.5 V (TDA8712) = 4.75 to 5.25 V (TDF8712); V_{CCA} to V_{CCD} = −0.5 to +0.5 V (TDA8712) = −0.25 to +0.25 V (TDF8712); REF decoupled to AGND via a 100 nF capacitor; T_{amb} = −40 to +85 °C; AGND and DGND shorted together; typical readings taken at $V_{CCA} = V_{CCD}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage					
	TDA8712		4.5	5.0	5.5	V
	TDF8712		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
ΔV_{GND}	ground voltage differences between V_{AGND} and V_{DGND}		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT CLK						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	0.01	20	µA
$f_{clk(max)}$	maximum clock frequency		50	–	–	MHz
Outputs (referenced to V_{CCA})						
$\Delta V_{OUT(p-p)}$	full-scale analog output voltage differences between V_{OUT} and $\overline{V}_{OUT}$ (peak-to-peak value)	Z_L = 10 kΩ; note 2	−1.45	−1.60	−1.75	V
		Z_L = 75 Ω; note 2	−0.72	0.80	−0.88	V
V_{os}	analog offset output voltage	code = 0	–	−3	−25	mV
TC_{VOUT}	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
TC_{Vos}	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	−3 dB analog bandwidth	f_{clk} = 50 MHz; note 3	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
φ_{diff}	differential phase		–	1	–	deg
Z_o	output impedance		–	75	–	Ω
Transfer function (f_{clk} = 50 MHz)						
ILE	DC integral linear error		–	±0.3	±0.5	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB

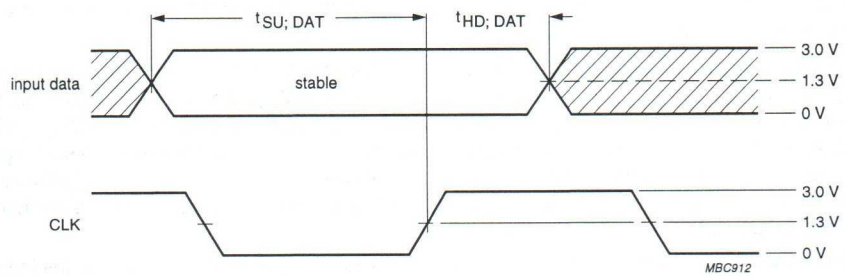
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{clk} = 50 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time 1	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time 2	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; f_{clk} = 50 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB·ns

Notes

1. D0 to D7 are connected to V_{CCD} and CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V}_{OUT}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V}_{OUT}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages; see Fig.5.
5. The data set-up time ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 and 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES (V)			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V}_{OUT}$	V_{OUT}	$\overline{V}_{OUT}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	.	.	.	.	.
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	.	.	.	.	.
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

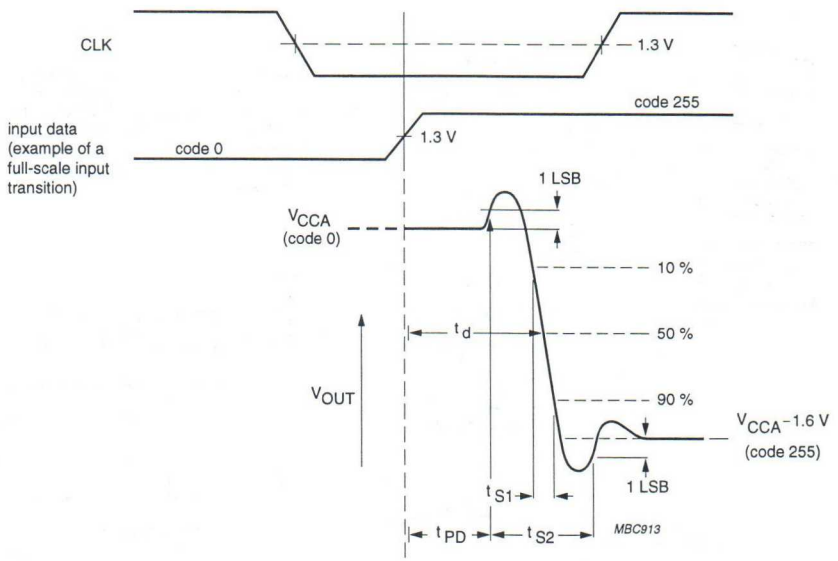
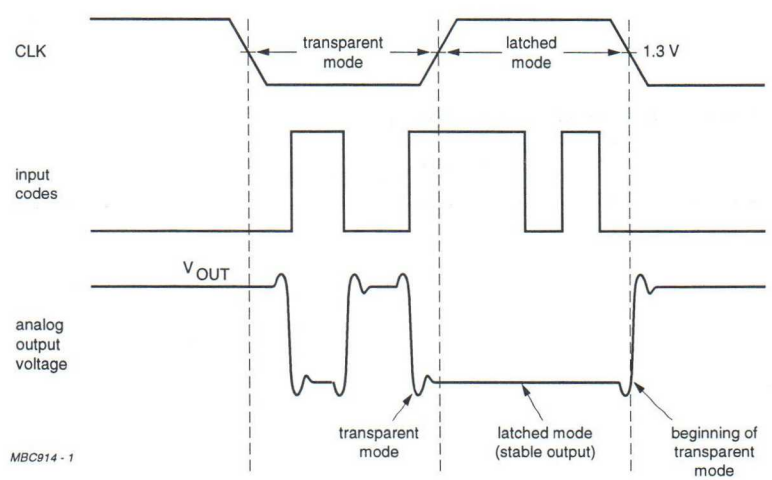
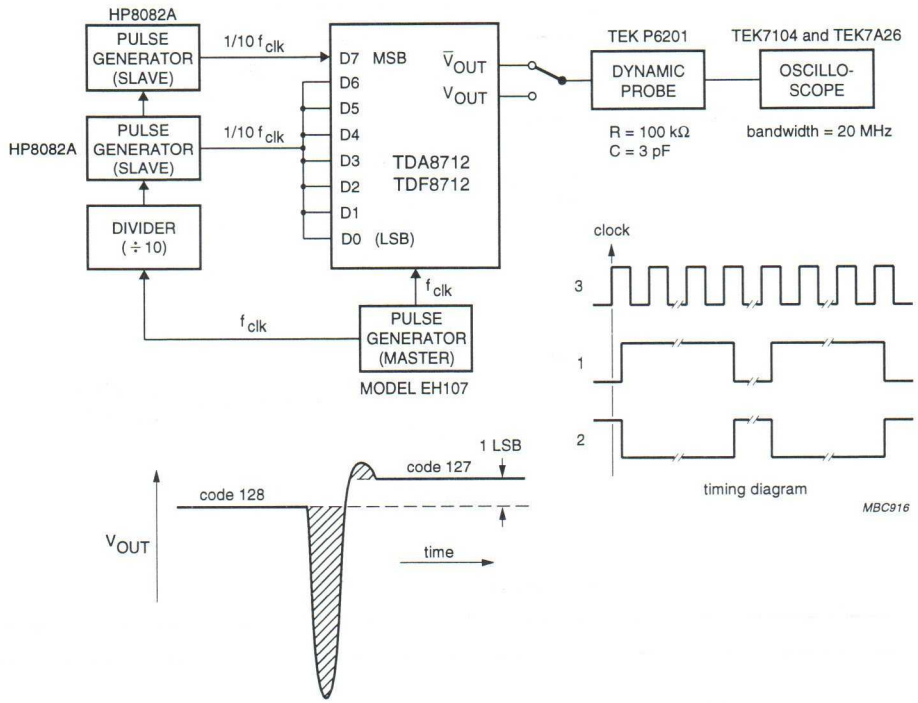


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB·ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

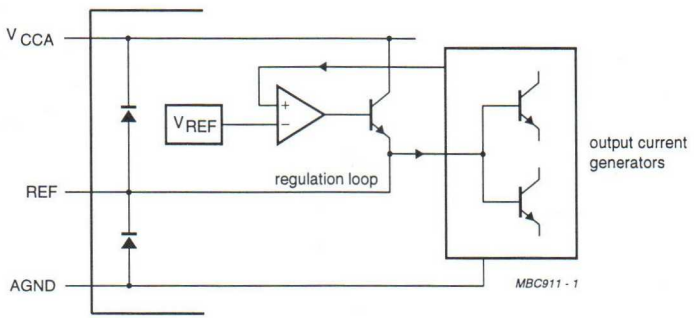


Fig.7 Reference voltage generator decoupling.

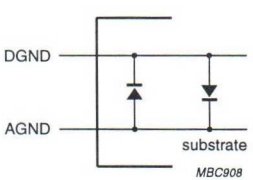


Fig.8 AGND and DGND.

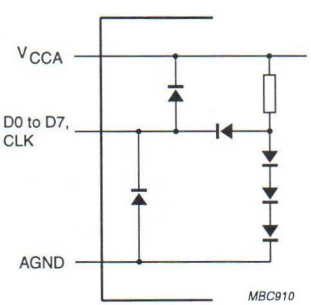


Fig.9 D7 to D0 and CLK.

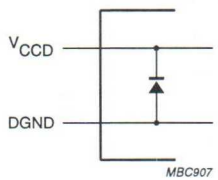


Fig.10 Digital supply.

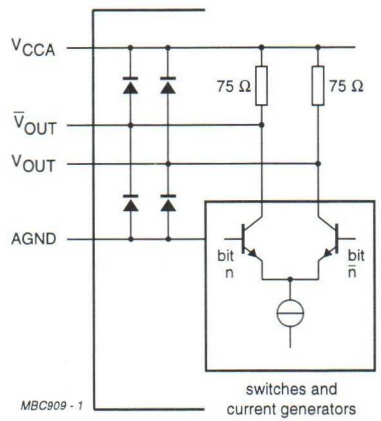


Fig.11 Analog outputs.

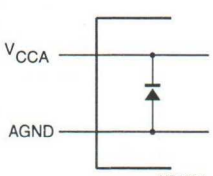
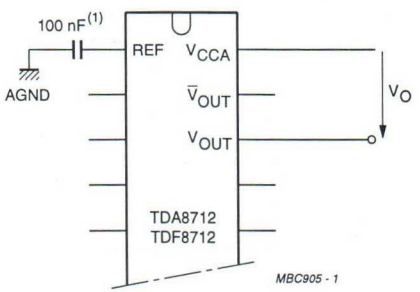


Fig.12 Analog supply.

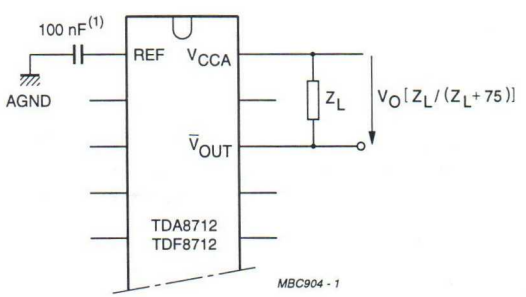
APPLICATION INFORMATION

Additional application information can be supplied on request (please quote *"FTV/8901"*).



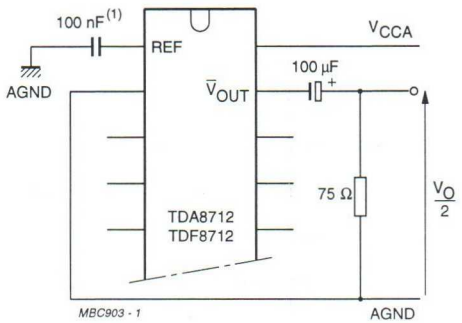
(1) This is a recommended value for decoupling pin 1.
$V_O = -\overline{V}_{OUT}$; see Table 1; Z_L = 10 kΩ.

Fig.13 Analog output voltage without external load.



(1) This is a recommended value for decoupling pin 1.
External load Z_L = 75 Ω to ∞.

Fig.14 Analog output voltage with external load.



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output voltage with AGND as reference.

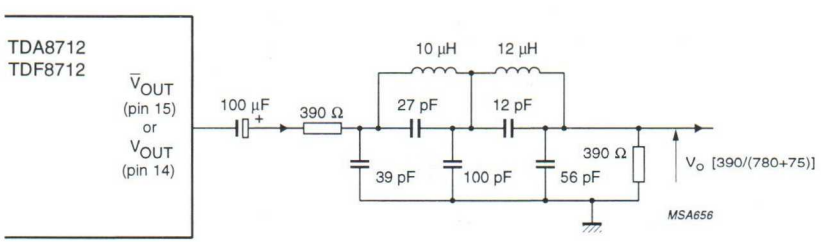


Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).

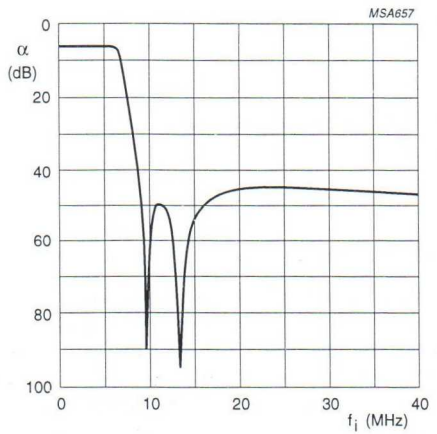
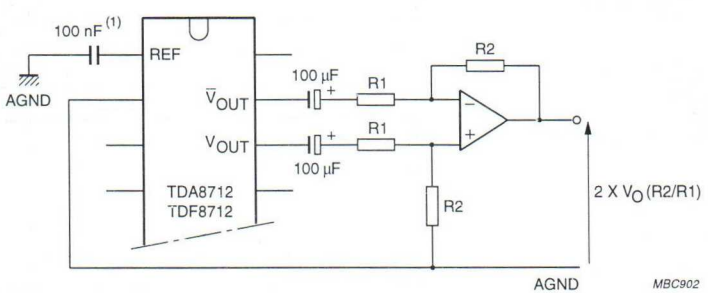


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig. 17

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.1$ dB
- f = 6.7 MHz at −3 dB
- f_{notch} = 9.7 MHz and 13.3 MHz.



(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

8-bit high-speed analog-to-digital converter TDA8714

FEATURES

- 8-bit resolution
- Sampling rate up to 75 MHz
- No missing codes guaranteed
- High signal-to-noise ratio over a large analog input frequency range (7.7 effective bits at 4.43 MHz full-scale input at f_{clk} = 75 MHz)
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 340 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- video data digitizing
- radar pulse analysis
- transient signal analysis
- high energy physics research
- ΣΔ modulators
- medical imaging.

GENERAL DESCRIPTION

The TDA8714 is an 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 75 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	25	30	mA
I_{CCD}	digital supply current		–	27	33	mA
I_{CCO}	output stages supply current		–	16	20	mA
INL	DC integral non-linearity		–	±0.4	±0.5	LSB
DNL	DC differential non-linearity		–	±0.2	±0.35	LSB
AINL	AC integral non-linearity	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8714/7		75	–	–	MHz
	TDA8714/6		60	–	–	MHz
	TDA8714/4		40	–	–	MHz
P_{tot}	total power dissipation		–	340	435	mW

Note

1. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 75 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8714T/4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	40
TDA8714T/6	SO24		SOT137-1	60
TDA8714T/7	SO24		SOT137-1	75
TDA8714T/4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	40
TDA8714T/6	SSOP24		SOT340-1	60
TDA8714T/7	SSOP24		SOT340-1	75

BLOCK DIAGRAM

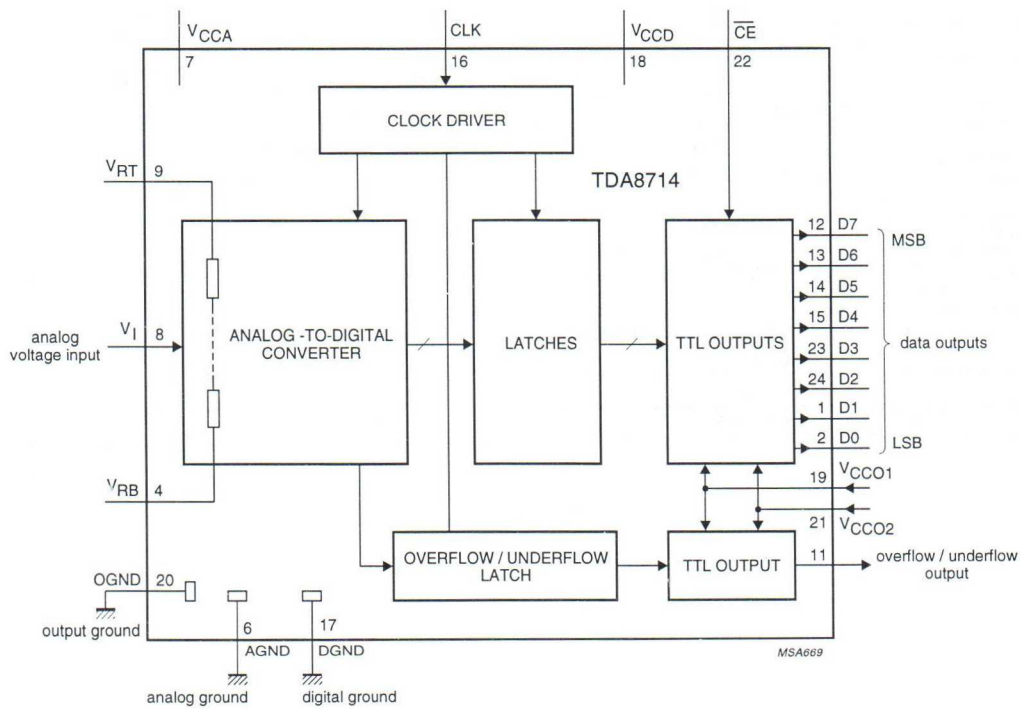


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage BOTTOM input
n.c.	5	not connected
AGND	6	analog ground
V_{CCA}	7	analog supply voltage (+5 V)
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	digital supply voltage (+5 V)
V_{CCO1}	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

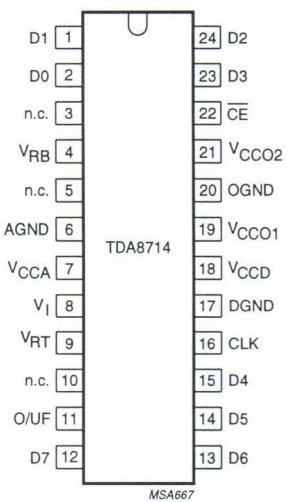


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 V and +7.0 V provided the difference between V_{CCA} and V_{CCD} is between −1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT137-1	75	K/W
	SOT340-1	119	K/W

CHARACTERISTICS

$V_{CCA} = V_7$ to $V_6 = 4.75$ to 5.25 V; $V_{CCD} = V_{18}$ to $V_{17} = 4.75$ to 5.25 V; $V_{CCO} = V_{19}$ and V_{21} to $V_{20} = 4.75$ to 5.25 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCO} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCA} to $V_{CCO} = -0.25$ to +0.25 V; $V_{i(p-p)} = 1.75$ V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	25	30	mA
I_{CCD}	digital supply current		–	27	33	mA
I_{CCO}	output stages supply current		–	16	20	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{clk} = 2.7$ V	–	–	300	µA
Z_I	input impedance	$f_{clk} = 75$ MHz	–	2	–	kΩ
C_I	input capacitance	$f_{clk} = 75$ MHz	–	4.5	–	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND) see Table 2						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	$V_I = 1.2$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_I = 3.5$ V	60	130	280	µA
Z_I	input impedance	$f_i = 4.43$ MHz	–	10	–	kΩ
C_I	input capacitance	$f_i = 4.43$ MHz	–	14	–	pF
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	1.6	V
V_{RT}	reference voltage TOP		3.5	3.6	3.9	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.9	2.3	2.7	V
I_{ref}	reference current		–	11.5	–	mA
R_{LAD}	resistor ladder		–	200	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	0.24	–	ppm
V_{osB}	offset voltage BOTTOM	note 2	–	255	–	mV
V_{osT}	offset voltage TOP	note 2	–	300	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)		1.45	1.75	2.15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
		I_O = −1 mA	2.4	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics						
CLOCK INPUT CLK (note 1; see Fig.3)						
$f_{clk(max)}$	maximum clock frequency					
	TDA8714/4		40	–	–	MHz
	TDA8714/6		60	–	–	MHz
	TDA8714/7		75	–	–	MHz
t_{CPH}	clock pulse width HIGH		6	–	–	ns
t_{CPL}	clock pulse width LOW		6	–	–	ns
Analog signal processing						
LINEARITY						
INL	DC integral non-linearity		–	±0.4	±0.5	LSB
DNL	DC differential non-linearity		–	±0.2	±0.35	LSB
AINL	AC integral non-linearity	note 3	–	±0.5	±1.0	LSB
BANDWIDTH (f_{clk} = 40 MHz); note 4						
B	analog bandwidth	full-scale sine wave	–	13	–	MHz
		75% full-scale sine wave; small signal at V_i = ±5 LSB, code 128	–	20	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.6; note 5	–	2.5	3.5	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.6; note 5	–	3.0	4.0	ns
HARMONICS (f_{clk} = 40 MHz)						
h_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	−64	−60	dB
	third harmonics		–	−58	−55	dB
THD	total harmonic distortion	f_i = 4.43 MHz	–	−56	–	dB
SIGNAL-TO-NOISE RATIO (note 6; see Fig.7 and Fig.13)						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	46	48	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS (note 6; see Figs.7 and 13)						
EB	effective bits					
	TDA8714/4	f_{clk} = 40 MHz				
		f_i = 4.43 MHz	–	7.75	–	bits
		f_i = 7.5 MHz	–	7.6	–	bits
	effective bits					
	TDA8714/6	f_{clk} = 60 MHz				
		f_i = 4.43 MHz	–	7.7	–	bits
		f_i = 7.5 MHz	–	7.55	–	bits
		f_i = 10 MHz	–	7.4	–	bits
	effective bits					
	TDA8714/7	f_{clk} = 75 MHz				
		f_i = 4.43 MHz	–	7.7	–	bits
		f_i = 7.5 MHz	–	7.5	–	bits
		f_i = 10 MHz	–	7.2	–	bits
		f_i = 15 MHz	–	6.3	–	bits
TWO-TONE (note 7)						
TTIR	two-tone intermodulation rejection	f_{clk} = 40 MHz	–	–56	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 128	–	10^{-11}	–	times/ samples
DIFFERENTIAL GAIN (note 8)						
G_{diff}	differential gain	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	0.6	–	%
DIFFERENTIAL PHASE (NOTE 8)						
φ_{diff}	differential phase	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	0.8	–	deg
Timing (note 9; see Figs 3 and 5; f_{clk} = 75 MHz)						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	10	11	ns
3-state output delay times (see Fig.4)						
t_{dZH}	enable HIGH		–	6	10	ns
t_{dZL}	enable LOW		–	12	16	ns
t_{dHZ}	disable HIGH		–	50	54	ns
t_{dLZ}	disable LOW		–	10	14	ns

Notes to the Characteristics

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including FF:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to FF at T_{amb} = 25 °C.
3. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 75 MHz).
4. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
7. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
8. Measurement carried out using video analyser VM700A where the video analog signal is reconstructed through a digital-to-analog converter.
9. Output data acquisition: the output data is available after the maximum delay time of t_d; in the event of 75 MHz clock operation, the hardware design must take into account the t_d and t_h limits with respect to the input characteristics of the acquisition circuit.

Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{I(p-p)}$	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.555	1	0	0	0	0	0	0	0	0
0	1.555	0	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1
.	.	.	.		.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	3.30	0	1	1	1	1	1	1	1	1
Overflow	>3.30	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{CE}$	D7 TO D0	O/UF
1	high impedance	high impedance
0	active; binary	active

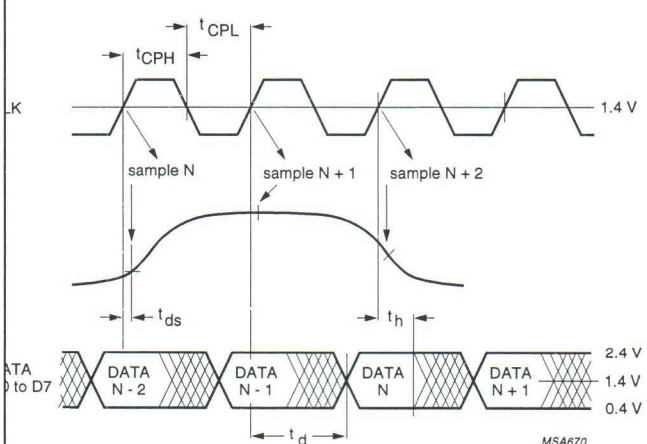
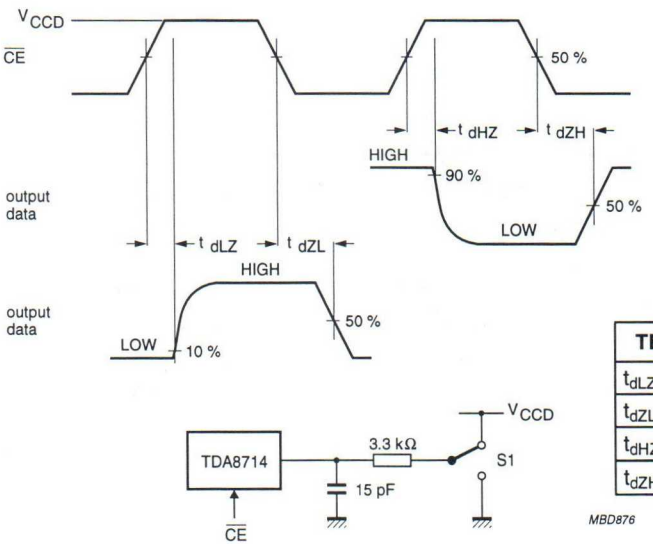


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

f_{CE} = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

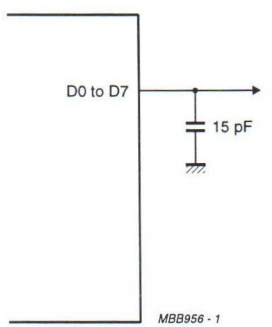


Fig.5 Load circuit for timing measurement.

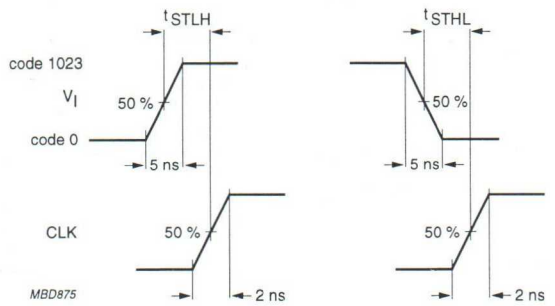
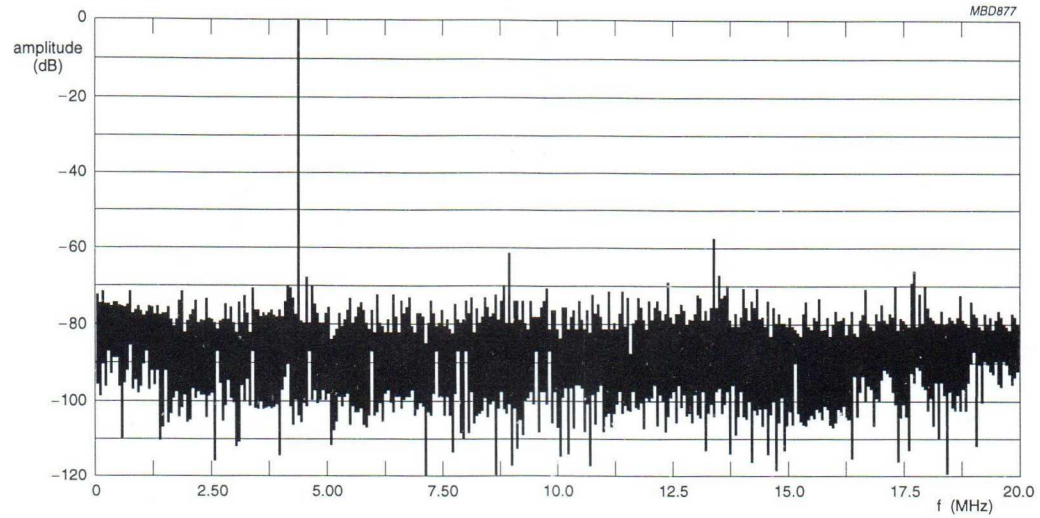
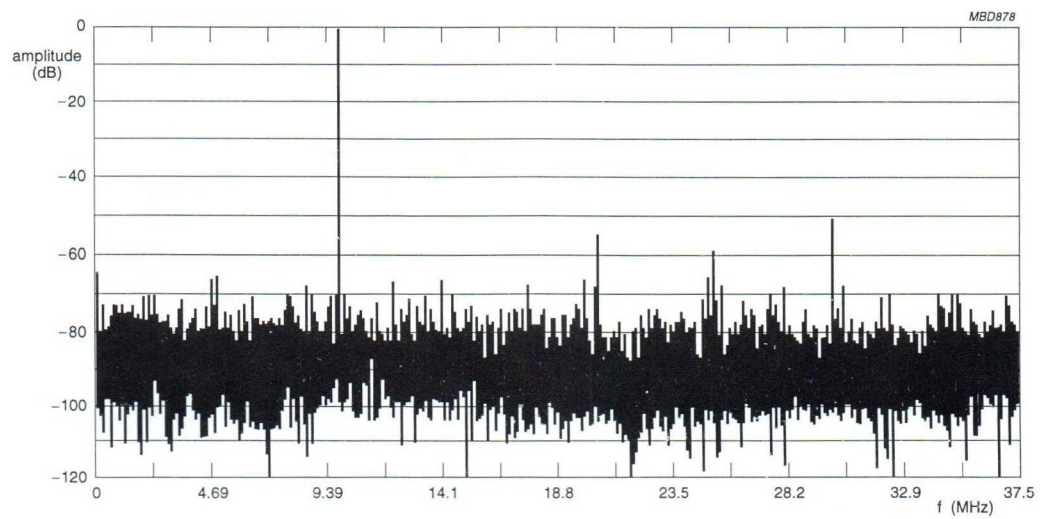


Fig.6 Analog input settling-time diagram.



Effective bits: 7.80; THD = −57.82 dB;
Harmonic levels (dB): 2nd = −68.00; 3rd = −61.54; 4th = −72.46; 5th = −65.80; 6th = −68.88.

Fig.7 Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 4.43 MHz).



Effective bits: 7.27; THD = −49.23 dB;
Harmonic levels (dB): 2nd = −56.16; 3rd = −51.01; 4th = −69.84; 5th = −59.10; 6th = −65.34.

Fig.8 Fast Fourier Transform (f_{clk} = 75 MHz; f_i = 10 MHz).

INTERNAL PIN CONFIGURATIONS

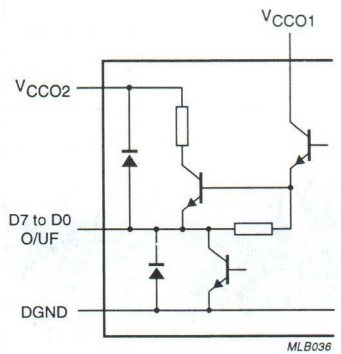


Fig.9 TTL data and overflow/underflow outputs.

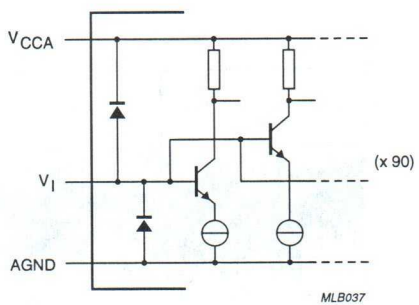


Fig.10 Analog inputs.

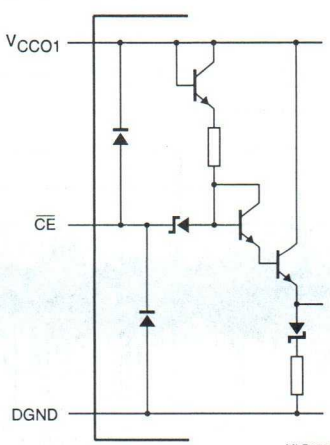


Fig.11 $\overline{CE}$ (3-state) input.

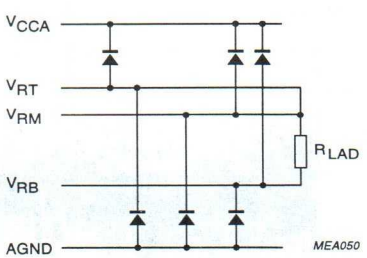


Fig.12 V_{RB} and V_{RT}.

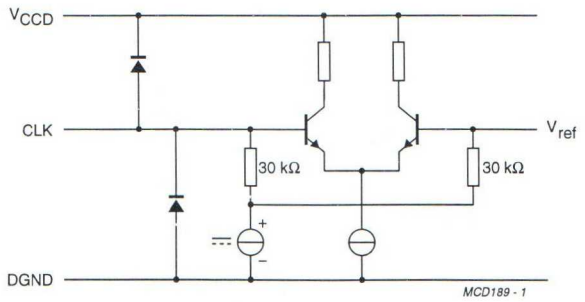
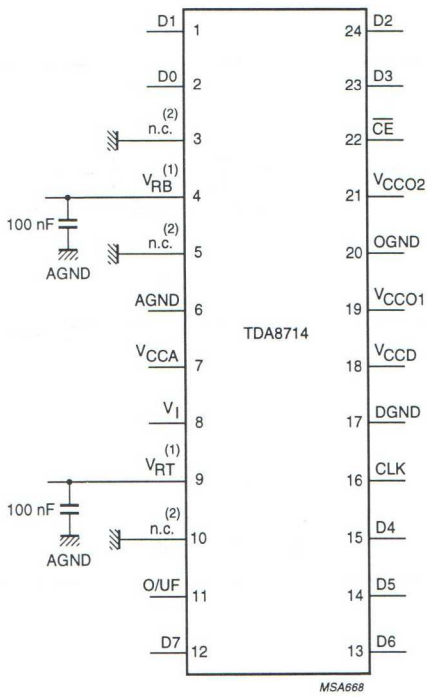


Fig.13 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value.

(1) V_{RB} and V_{RT} are decoupled to AGND.

(2) Pin 5 should be connected to AGND; pins 3 and 10 to DGND in order to prevent noise influence.

Fig.14 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8716

FEATURES

- 8-bit resolution
- Sampling rate up to 120 MHz
- ECL (10 K family) compatible digital inputs and outputs
- Overflow/Underflow output
- Low power dissipation
- Low input capacitance (13 pF typ.).

APPLICATIONS

- High speed analog-to-digital convertion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- Medical systems
- Industrial instrumentation.

GENERAL DESCRIPTION

The TDA8716 is an 8-bit high-speed analog-to-digital converter (ADC) designed for HDTV and professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 120 MHz. All digital outputs are ECL compatible.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–5.45	–5.2	–4.95	V
V_{EED}	digital supply voltage		–5.45	–5.2	–4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED}	digital supply current		–	100	110	mA
I_{EEO}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{RB}	reference voltage BOTTOM		–	–3.130	–	V
V_{RT}	reference voltage TOP		–	–1.870	–	V
ILE	DC integral linearity error	see Fig.8	–	±0.5	±1	LSB
DLE	DC differential linearity error	see Fig.9	–	±0.25	±0.45	LSB
EB	effective bit	f_i = 20 MHz; f_{CLK} = 100 MHz	–	7	–	bits
f_{CLK}	maximum clock frequency		120	–	–	MHz
P_{tot}	total power dissipation	excluding load	–	780	900	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8716	24	DIL	plastic	SOT101
TDA8716T	32	SO32L	plastic	SOT287

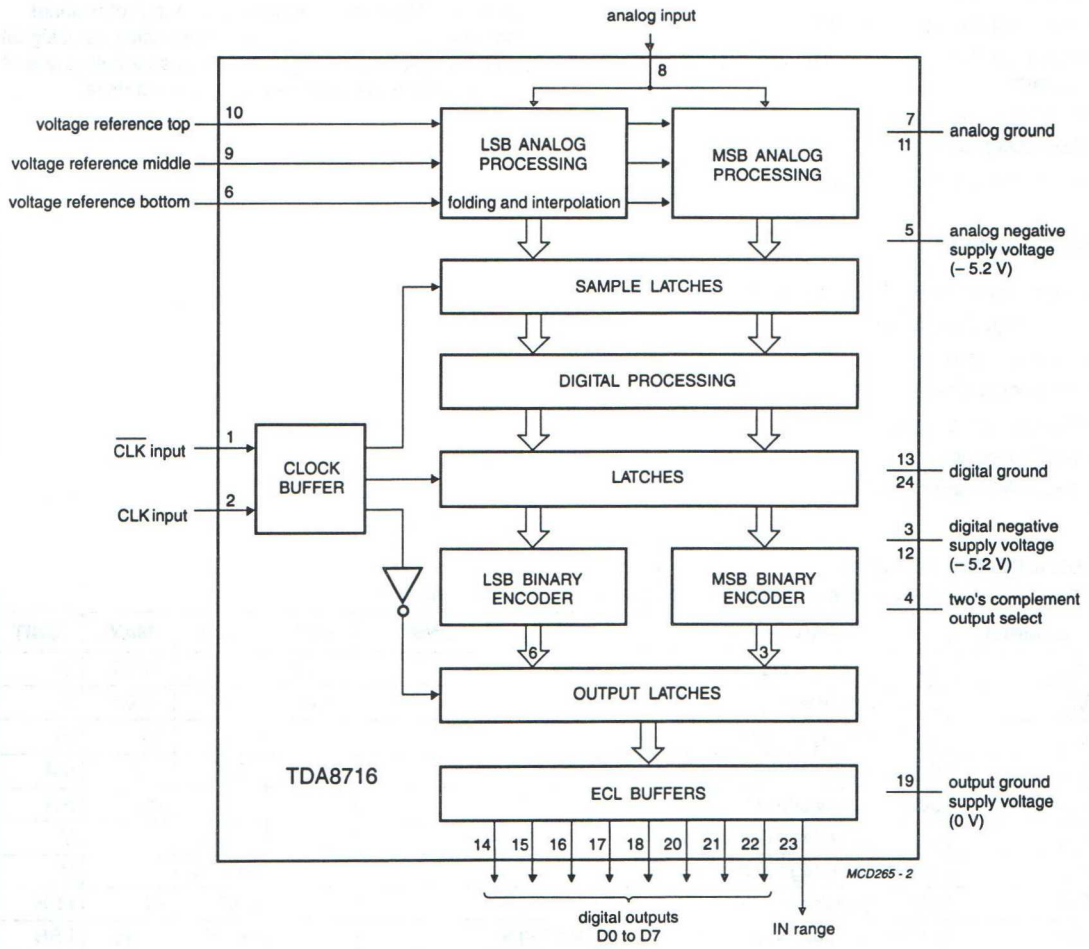


Fig.1 Block diagram; TDA8716.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (−5.2 V)
C_{PLT2}	4	two's complement output select (active HIGH)
V_{EEA}	5	analog negative supply voltage (−5.2 V)
V_{RB}	6	reference voltage BOTTOM
AGND1	7	analog ground 1
V_I	8	analog input
V_{RM}	9	reference voltage MIDDLE decoupling
V_{RT}	10	reference voltage TOP
AGND2	11	analog ground 2
V_{EED2}	12	digital negative supply voltage (−5.2 V)
DGND1	13	digital ground 1
D0	14	digital output (LSB)
D1	15	digital output
D2	16	digital output
D3	17	digital output
D4	18	digital output
OGND	19	output ground supply voltage (0 V)
D5	20	digital output
D6	21	digital output
D7	22	digital output (MSB)
IR	23	IN range
DGND2	24	digital ground 2

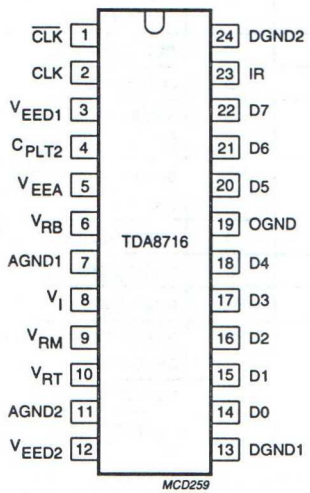


Fig.2 Pin configuration; TDA8716.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (−5.2 V)
n.c.	4	not connected
n.c.	5	not connected
C_{PLT2}	6	two's complement output select (active HIGH)
V_{EEA}	7	analog negative supply voltage (−5.2 V)
V_{RB}	8	reference voltage BOTTOM
AGND1	9	analog ground 1
V_I	10	analog input
V_{RM}	11	reference voltage MIDDLE decoupling
n.c.	12	not connected
n.c.	13	not connected
V_{RT}	14	reference voltage TOP
AGND2	15	analog ground 2
V_{EED2}	16	digital negative supply voltage (−5.2 V)
DGND1	17	digital ground 1
D0	18	digital output (LSB)
D1	19	digital output
n.c.	20	not connected
n.c.	21	not connected
D2	22	digital output
D3	23	digital output
D4	24	digital output
OGND	25	output ground supply voltage (0 V)
D5	26	digital output
D6	27	digital output
n.c.	28	not connected
n.c.	29	not connected
D7	30	digital output (MSB)
IR	31	IN range
DGND2	32	digital ground 2

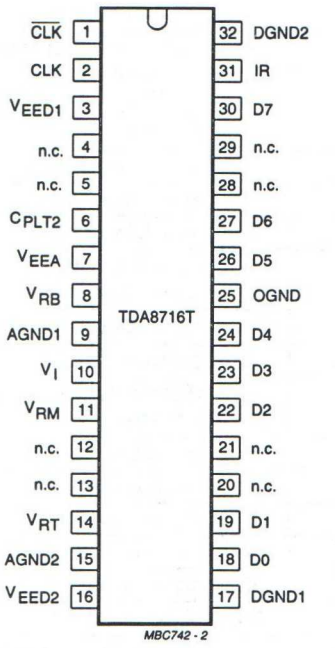


Fig.3 Pin configuration; TDA8716T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7.0	+0.3	V
V_{EED1}, V_{EED2}	digital supply voltage		−7.0	+0.3	V
$V_{EEA}-V_{EED1}$; $V_{EEA}-V_{EED2}$	supply voltage differences		−1	+1	V
V_I	input voltage	referenced to AGND	V_{EEA}	0	V
$V_{CLK;\ \overline{CLK}(p\text{-}p)}$	input voltage for differential clock drive (peak-to-peak value)	note 1	−	2.0	V
I_O	output current (each output stage)		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the rising edge of the clock input signal: CLK and $\overline{CLK}$ are two's complementary ECL signals.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT101	35 K/W
	SOT287 (see Fig.4)	65 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{EEA} = −4.95 V to −5.45 V; V_{EED1}, V_{EED2} = −4.95 V to −5.45 V; AGND, DGND and OGND shorted together; T_{amb} = 0 °C to +70°C; unless otherwise specified. (Typical values taken at V_{EEA} = −5.2 V; V_{EED1}, V_{EED2} = −5.2 V; T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−5.45	−5.2	−4.95	V
V_{EED1}, V_{EED2}	digital supply voltage		−5.45	−5.2	−4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED1}, I_{EED2}	digital supply current		–	100	110	mA
I_{EE}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{diff}	supply voltage differential	$V_{EEA} - V_{EED1}$; $V_{EEA} - V_{EED2}$	−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage BOTTOM		−3.5	−3.13	–	V
V_{RT}	reference voltage TOP		–	−1.87	−1.5	V
V_{ref}	reference voltage differential	$V_{RT} - V_{RB}$	–	1.26	–	V
V_{OB}	voltage offset BOTTOM	note 1	–	130	–	mV
V_{OT}	voltage offset TOP	note 1	–	130	–	mV
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		0.95	1.0	1.5	V
I_{ref}	reference current		–	15	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RL}	temperature coefficient of the resistor ladder		–	0.18	–	Ω/K
Inputs						
CLK and $\overline{CLK}$ input						
V_{IL}	LOW level input voltage		−1850	−1770	−1650	mV
V_{IH}	HIGH level input voltage		−960	−880	−810	mV
I_{IL}	LOW level input current	V_{CLK} = −1.77 V	–	1	–	μA
I_{IH}	HIGH level input current	V_{CLK} = −0.88 V	–	10	–	μA
R_I	input resistance		–	20	–	kΩ
C_I	input capacitance		–	2	–	pF
$V_{CLK(p-p)}$	differential clock input V_{CLK} − $V_{\overline{CLK}}$ (peak-to-peak value)		–	900	–	mV
Analog input; note 2						
I_{IB}	input current BOTTOM	V_{RB} = −3.13 V	–	0	–	μA
I_{IT}	input current TOP	V_{RT} = −1.87 V	–	170	–	μA
R_I	input resistance		–	7	–	kΩ
C_I	input capacitance		–	13	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 2.2 kΩ)						
Digital 10K ECL outputs (D0 to D7; IR)						
V_{OL}	LOW level output voltage		−1850	−1770	−1600	mV
V_{OH}	HIGH level output voltage		−960	−880	−810	mV
I_{OL}	LOW level output current		−	1.8	4.0	mA
I_{OH}	HIGH level output current		−	2.0	4.0	mA
Timing (f_{CLK} = 100 MHz; R_L = 2.2 kΩ; see Fig.5)						
t_{ds}	sampling delay		−	1	3	ns
t_{HD}	output hold time		4	−	−	ns
t_d	output delay time	note 3				
		C_L = 3.3 pF	−	−	7.5	ns
		C_L = 7.5 pF	−	−	9	ns
t_{aj}	aperture jitter		−	15	−	ps
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		120	−	−	MHz
Analog signal processing (f_{CLK} = 100 MHz)						
G_{diff}	differential gain	note 4	−	0.3	−	%
ϕ_{diff}	differential phase	note 4	−	0.4	−	°C
Harmonics (full scale); f_i = 10 MHz; f_{CLK} = 100 MHz						
f1	fundamental		−	0	−	dB
f2	even harmonics		−	−60	−	dB
f3	odd harmonics		−	−50	−	dB
Transfer function						
ILE	DC integral linearity error		−	±0.5	±1	LSB
DLE	DC differential linearity error		−	±0.25	±0.45	LSB
AILE	AC integral linearity error	note 4	−	±1	±1.5	LSB
EB	effective bits	Figs 13 and 14; note 5; f_{CLK} = 100 MHz				
	f_i = 4.43 MHz	Fig.10	-	7.7	−	bits
	f_i = 10 MHz	Fig.11	-	7.5	−	bits
	f_i = 20 MHz	Fig.12	-	7.0	−	bits
	f_i = 30 MHz		-	6.5	−	bits
BER	bit error rate	f_{CLK} = 100 MHz; f_i = 10 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	−	10^{-11}	−	times/ samples

Notes

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RB} and V_{RT} levels.
3. The TDA8716 can only withstand one or two 10K or 100K ECL loads in order to work-out timings at the maximum sampling frequency. It is therefore recommended to minimize the printed-circuit board load by implementing the load device as close as possible to the TDA8716.
4. Full-scale sinewave; f_i = 4.43 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 100 MHz.
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4 K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR = EB (dB) x 6.02 + 1.76.

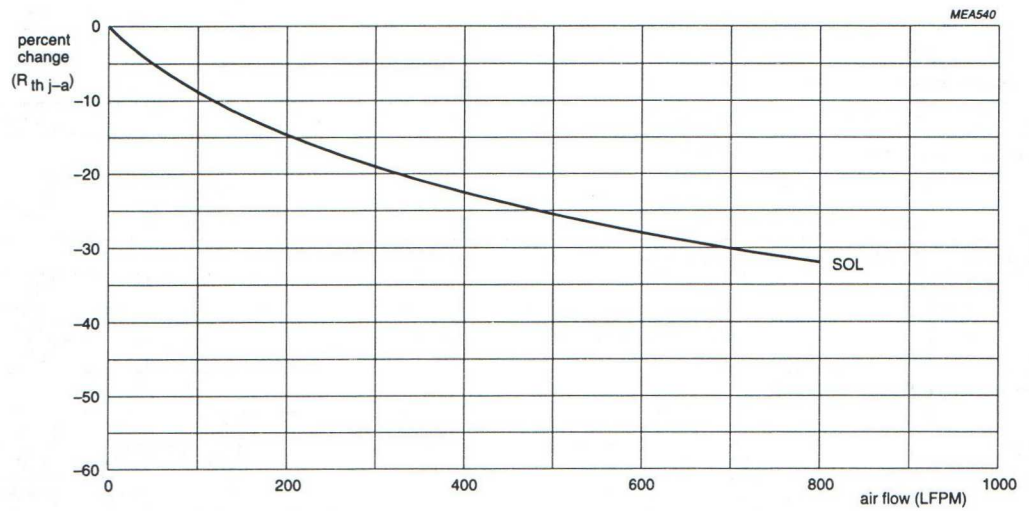


Fig.4 Average effect of air flow on thermal resistance.

Table 1 Output coding (CPLT2 HIGH).

STEP	V_I (TYP.)	BINARY OUTPUTS D7 to D0	IR
Underflow	< –3 V	00000000	0
0	–3 V	00000000	1
1	.	00000001	1
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	11111110	1
255	–2 V	11111111	1
Overflow	> –2 V	11111111	0

Table 2 Two's complement coding.

C_{PLT2}	D7 (MSB)
1 (V_{IH})	non inverted
0 (V_{IL})	inverted

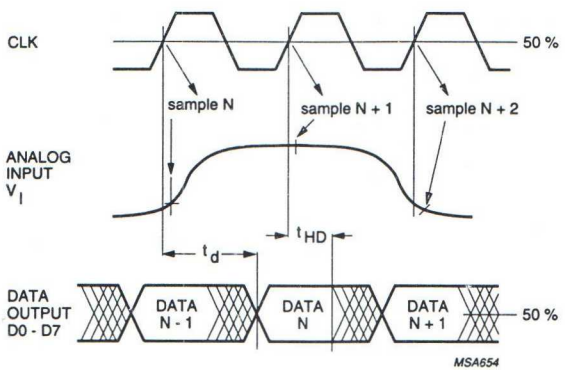


Fig.5 Timing diagram.

APPLICATION INFORMATION

Additional application information will be supplied upon request, please quote reference number FTV/AN 9109.

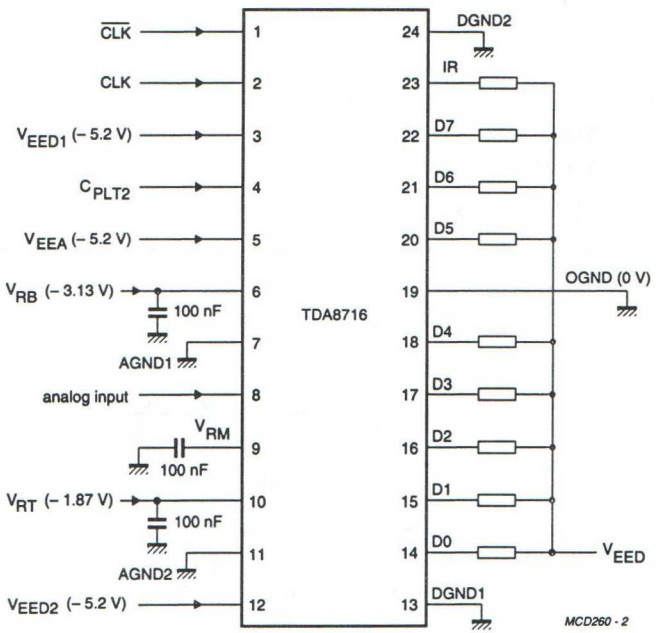


Fig.6 Application diagram; TDA8716.

Notes to Fig.6

1. Typical value for resistors = 2.2 kΩ.
2. Lower resistor values can be used down to 500 Ω to obtain higher sampling frequencies in the 150 MSPS range (limited by t_d and t_{HD} timings). In this configuration a DC shift of the ECL output levels V_{OL} and V_{OH} will occur.
3. V_{RB}, V_{RT} and V_M are decoupled to AGND.
4. Analog, digital and output supplies should be separated and decoupled.
5. The external voltage regulator must be constructed in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

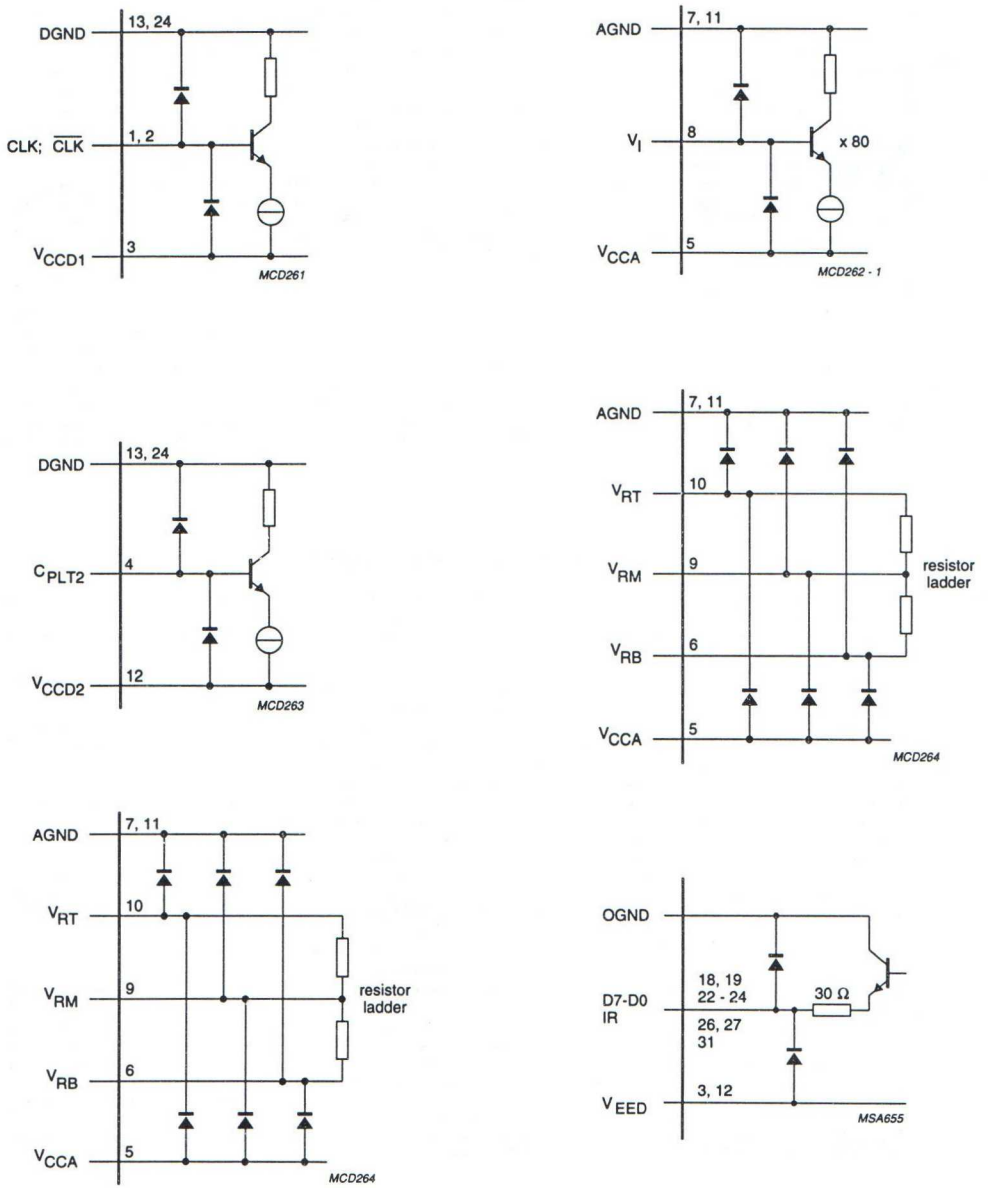


Fig.7 Internal pin configuration diagram.

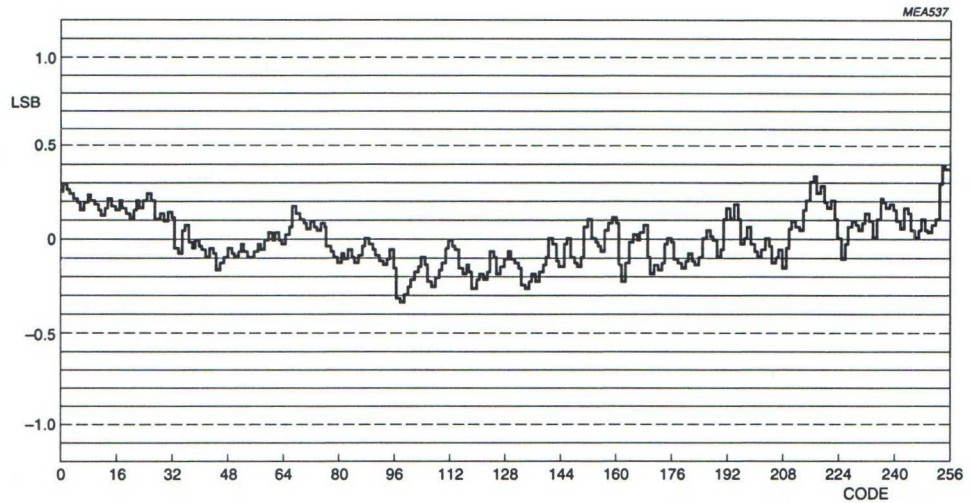


Fig.8 DC Integral linearity error (ILE).

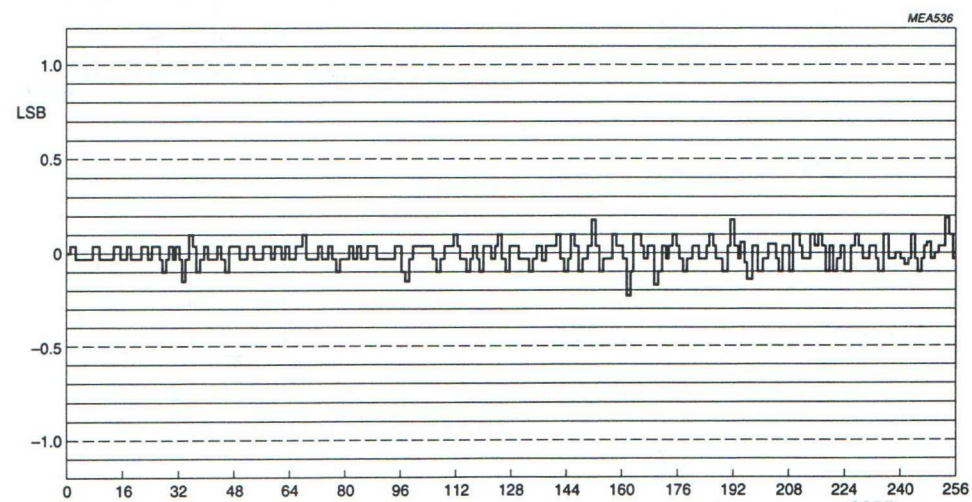
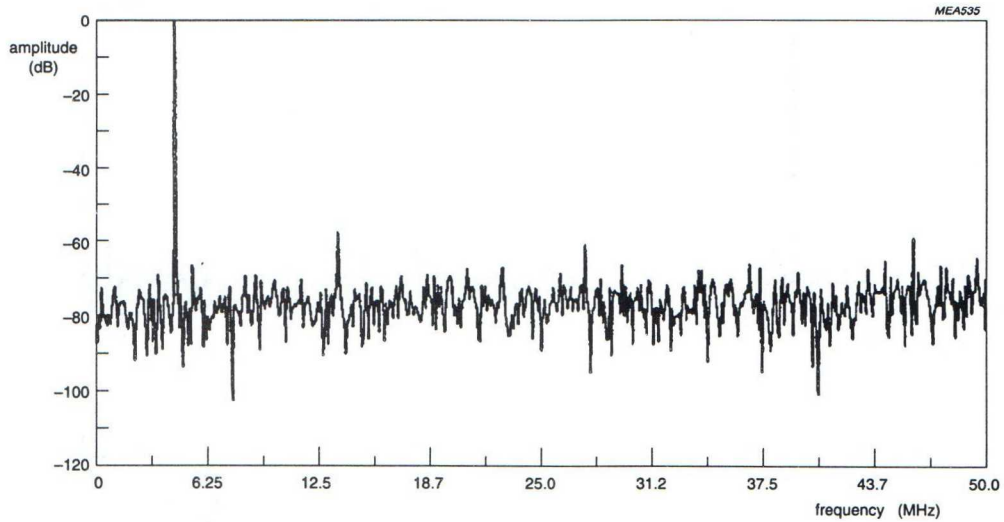
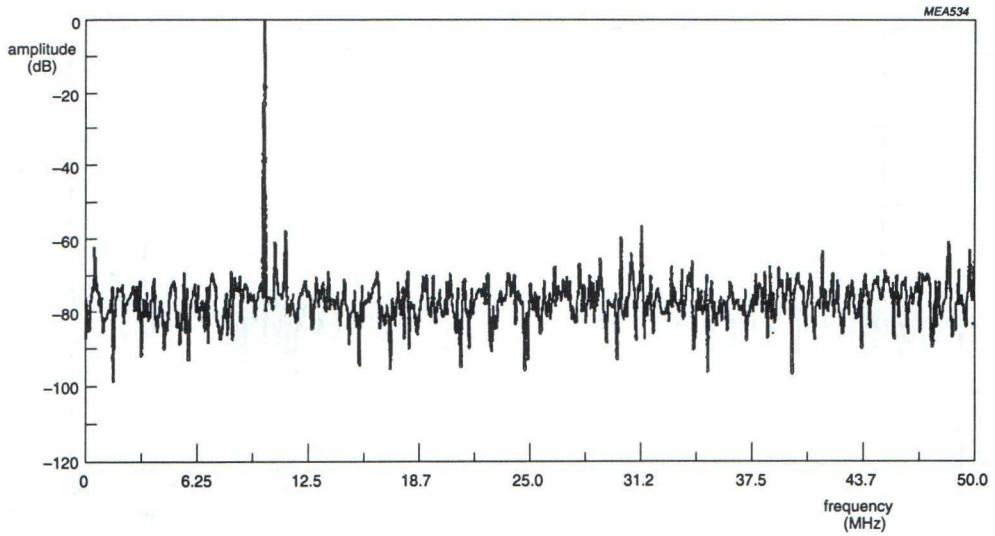


Fig.9 DC differential linearity error (DLE).



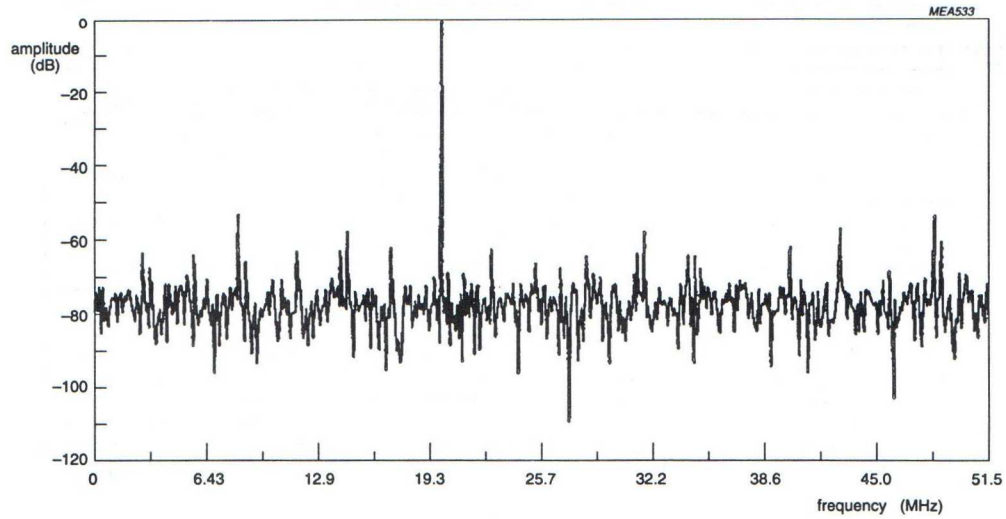
Effective bits: 7.74; Harmonic levels (in dB): 2nd = −69.34; 3rd = −58.85; 4th = −82.55; 5th = −68.16 and 6th = −63.01

Fig.10 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 7.57; Harmonic levels (in dB): 2nd = −82.07; 3rd = −61.90; 4th = −75.70; 5th = −65.61 and 6th = −72.50

Fig.11 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 10 MHz).



Effective bits: 7.04; Harmonic levels (in dB): 2nd = −61.36; 3rd = −56.66; 4th = −61.97; 5th = −62.79 and 6th = −61.52

Fig.12 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 20 MHz).

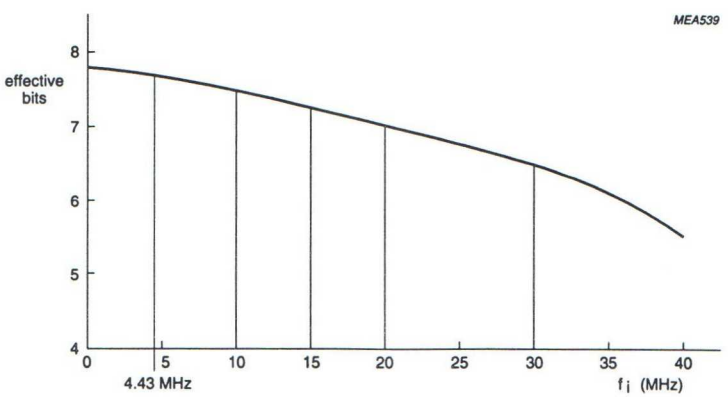


Fig.13 Typical effective bit as a function of input signal at f_{CLK} = 100 MHz.

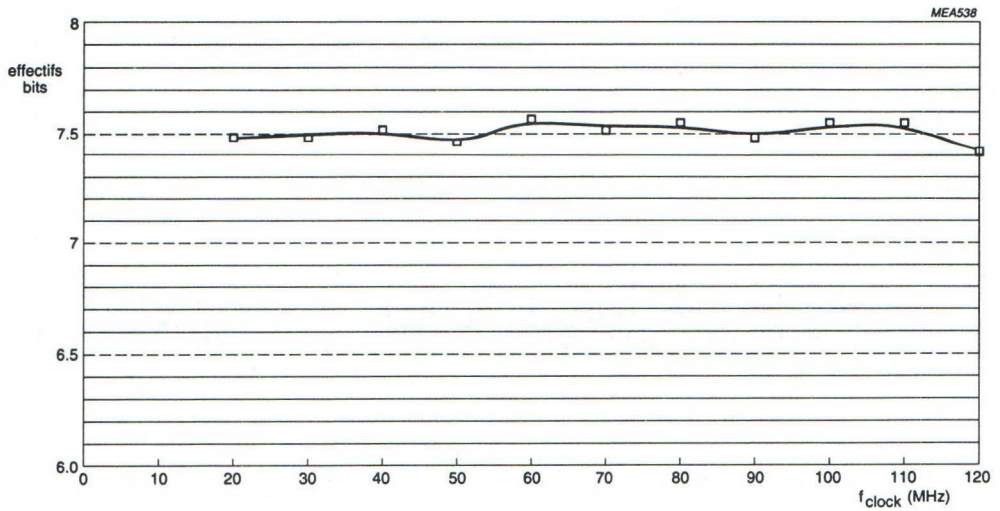


Fig.14 Typical effective bits as a function of clock frequency at f_i = 10 MHz.

8-bit high-speed analog-to-digital converter TDA8718

FEATURES

- 8-bit resolution
- Sampling rate up to 600 MHz
- ECL (100K family) compatible for digital inputs and outputs
- Overflow/Underflow output
- 50 Ω load drive capability
- Low input capacitance (5 pF typ.).

GENERAL DESCRIPTION

The TDA8718 is an 8-bit analog-to-digital converter (ADC) designed for professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 600 MHz. It has an effective bandwidth capability up to 150 MHz full-scale sine wave. All digital outputs are ECL compatible.

APPLICATIONS

- High speed analog-to-digital conversion
- Industrial instrumentation
- Data communication
- RF communication.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.2	−4.5	−4.8	V
V_{EED}	digital supply voltage		−4.2	−4.5	−4.8	V
I_{ref}	resistive ladder current	R = 48 Ω	30	45	60	mA
I_{EEA}	analog supply current		30	42	54	mA
I_{EED}	digital supply current		100	120	150	mA
$I_{EEO(L)}$	LOW level output supply current	R_L = 50 Ω	40	70	90	mA
$I_{EEO(H)}$	HIGH level output supply current	R_L = 50 Ω	155	170	185	mA
ILE	DC integral linearity error		–	±0.7	±1.0	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
EB	effective bits	f_i = 4.43 MHz; I_{ref} = 45 mA; f_{clk} = 100 MHz	–	7.5	–	bits
		f_i = 4.43 MHz; I_{ref} = 45 mA; f_{clk} = 100 MHz	–	6.5	–	bits
$f_{clk(max)}$	maximum clock frequency		600	–	–	MHz
P_{tot}	total power dissipation		–	990	1250	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8718K	28	PLCC28	plastic	SOT261-2

BLOCK DIAGRAM

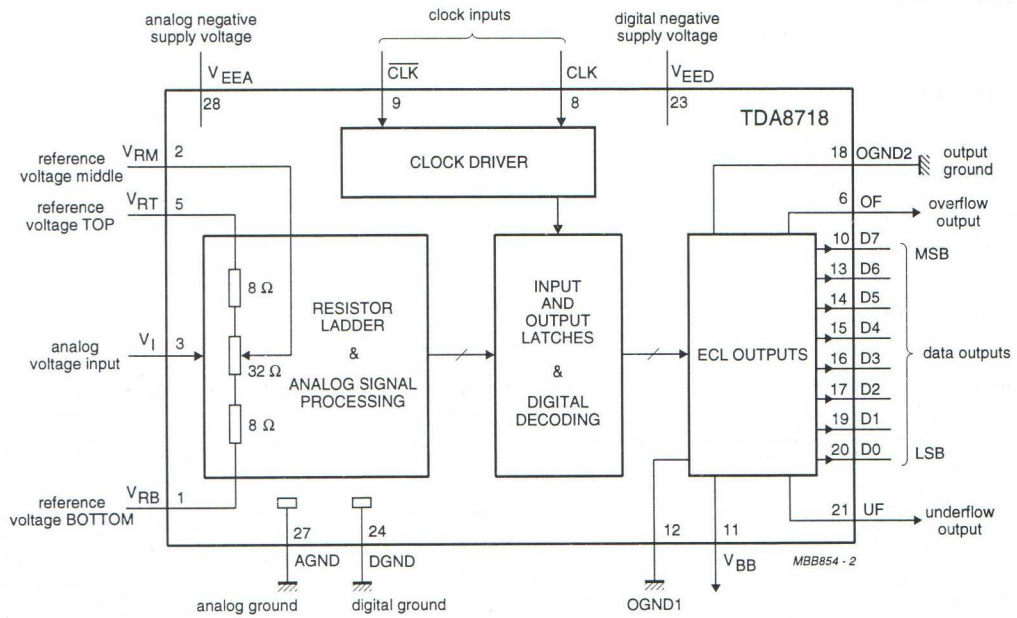


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{RB}	1	reference voltage BOTTOM
V_{RM}	2	reference voltage MIDDLE decoupling
V_I	3	analog input voltage
n.c.	4	not connected
V_{RT}	5	reference voltage TOP
OF	6	overflow digital output
n.c.	7	not connected
CLK	8	clock input
$\overline{CLK}$	9	complementary clock input
D7	10	digital output; bit 7 (MSB)
V_{BB}	11	ECL reference voltage
OGND1	12	output ground 1 (0 V)
D6	13	digital output; bit 6
D5	14	digital output; bit 5
D4	15	digital output; bit 4
D3	16	digital output; bit 3
D2	17	digital output; bit 2
OGND2	18	output ground 2 (0 V)
D1	19	digital output; bit 1
D0	20	digital output; bit 0 (LSB)
UF	21	underflow digital output
n.c.	22	not connected
V_{EED}	23	digital supply voltage (–4.5 V)
DGND	24	digital ground
n.c.	25	not connected
n.c.	26	not connected
AGND	27	analog ground
V_{EEA}	28	analog supply voltage (–4.5 V)

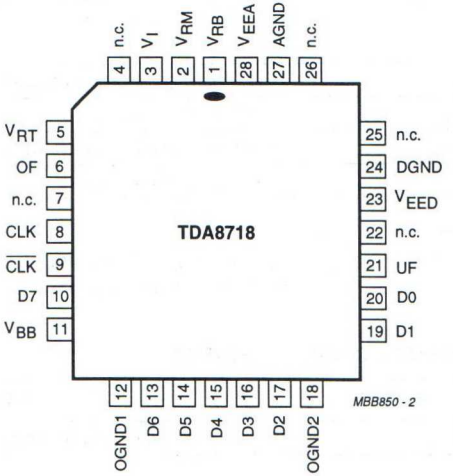


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

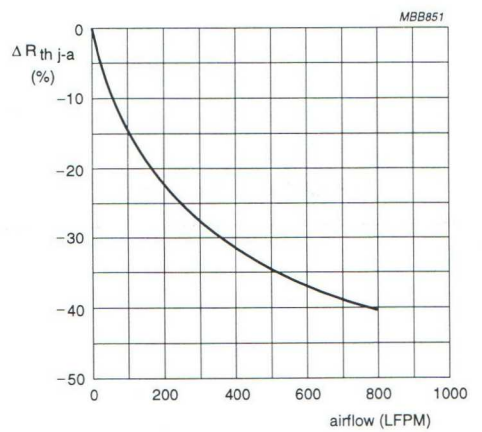
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage (pin 28)		−7.0	+0.3	V
V_{EED}	digital supply voltage (pin 23)		−7.0	+0.3	V
ΔV_{EE}	supply voltage difference between V_{EEA} and V_{EED}		−1.00	+1.0	V
V_I	input voltage (pin 3)	referenced to AGND	V_{EEA}	0	V
$\Delta V_{clk(p-p)}$	clock input voltage difference between CLK and $\overline{CLK}$ pin 8 to pin 9 (peak-to-peak value)	referenced to V_{EED}; note 1	–	2.0	V
I_O	output current for each digital output		–	30	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. Sampling takes place on the falling edge of the clock input signal; CLK and $\overline{CLK}$ are two complementary signals.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W



Test conditions: PCB (2.24 × 2.24 × 0.062 inches).
LFPM = Linear Foot Per Minute.

Fig.3 Average effect of air flow on $R_{th\ j\text{-}a}$.

CHARACTERISTICS

V_{EEA} = −4.2 to −4.8 V; V_{EED} = −4.2 to −4.8 V; V_{EEA} to V_{EED} = −0.1 to +0.1 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at V_{EEA} = −4.5 V, V_{EED} = −4.5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage (pin 28)		−4.2	−4.5	−4.8	V
V_{EED}	digital supply voltage (pin 23)		−4.2	−4.5	−4.8	V
I_{EEA}	analog supply current (pin 28)		30	42	54	mA
I_{EED}	digital supply current (pin 23)		100	120	150	mA
$I_{EEO(L)}$	LOW level output supply current	R_L = 50 Ω	40	70	90	mA
$I_{EEO(H)}$	HIGH level output supply current	R_L = 50 Ω	155	170	185	mA
Reference voltages for the resistor ladder (see Table 1)						
I_{RT}	reference current (pin 5)	R = 48 Ω	30	45	60	mA
V_{RB}	reference voltage BOTTOM (pin 1)		–	48 Ω × I_{RT}	–	V
V_{RT}	reference voltage TOP (pin 5)		–	0	–	V
R_{LAD}	resistor ladder		–	48	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	175	–	MΩ/K
V_{osB}	voltage offset BOTTOM	note 1	–	8 Ω × I_{RT}	–	mV
V_{osT}	voltage offset TOP	note 1	–	8 Ω × I_{RT}	–	mV
Inputs						
CLK INPUT (PIN 8); $\overline{\text{CLK}}$ INPUT (PIN 9)						
V_{IL}	LOW level input voltage		–	−1.8	–	V
V_{IH}	HIGH level input voltage		–	−0.8	–	V
I_{IL}	LOW level input current	V_{clk} = −1.8 V	–	0	–	µA
I_{IH}	HIGH level input current	V_{clk} = −0.8 V	–	120	–	µA
R_I	input resistance	f_{clk} = 100 MHz	–	1.5	–	kΩ
C_I	input capacitance	f_{clk} = 100 MHz	–	3.5	–	pF
$\Delta V_{clk(p-p)}$	clock input voltage difference between CLK and $\overline{\text{CLK}}$ pin 8 to pin 9 (peak-to-peak value)		–	900	–	mV
ANALOG INPUT (PIN 3); NOTE 2						
I_{IL}	LOW level input current	data output = 00	20	40	80	µA
I_{IH}	HIGH level input current	data output = FF	100	200	400	µA
R_I	input resistance		–	10	–	kΩ
C_I	input capacitance		–	5	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 50 Ω)						
DIGITAL 100K ECL OUTPUTS (D0 TO D7; OF; UF)						
V_{OL}	LOW level output voltage	Tamb = 25 °C	–	–1770	–1650	mV
V_{OH}	HIGH level output voltage	Tamb = 25 °C	–1300	–1150	–	mV
V_{ECL}	ECL reference voltage		–1550	–1450	–1350	mV
I_{OL}	LOW level output current		4	6	8	mA
I_{OH}	HIGH level output current		10	20	25	mA
Switching characteristics						
$f_{clk(max)}$	maximum clock frequency (pins 8 and 9)		600	–	–	MHz
t_r; t_f	rise and fall times	f_i = 100 MHz	–	–	750	ps
Analog signal processing (f_{clk} = 500 MHz)						
HARMONICS (FULL SCALE)						
h_1	fundamental harmonics	f_i = 100 MHz	–	0	–	dB
h_2	second harmonics	f_i = 100 MHz	–	–54	–	dB
h_3	third harmonics	f_i = 100 MHz	–	–50	–	dB
Transfer function						
ILE	DC integral linearity error		–	±0.7	±1.0	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.9	±1.5	LSB
EB	effective bits	f_i = 4.43 MHz, full scale; I_{ref} = 45 mA; note 4; f_{clk} = 100 MHz; Fig.5	–	7.5	–	bits
		f_i = 100 MHz, full scale; I_{ref} = 45 mA; note 4; f_{clk} = 500 MHz; Fig.6	–	6.5	–	bits
BER	bit error rate	f_{clk} = 500 MHz; f_i = 100 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	–	10^{-11}	–	times/ samples
Timing (f_{clk} = 500 MHz; R_L = 50 Ω; C_L = 5 pF) note 5						
t_{ds}	sampling delay		–	–	300	ps
t_h	output hold time		400	700	–	ps
t_d	output delay time		–	1300	1500	ps

Notes to the "Characteristics"

1. Voltage offset BOTTOM (V_{osB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C. Voltage offset TOP (V_{osT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RT} and V_{RB} levels.
3. Full-scale sine wave; f_i = 4.43 MHz; f_{clk} = 100 MHz.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).

   Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
5. TDA8718 can only withstand one or two 100K ECL loads in order to work out timings at the maximum sampling frequency. It is recommended to minimize the printed circuit-board load by implementing the load device as close as possible to the TDA8718.

Table 1 Output coding and input voltage (typical values; referenced to AGND.

STEP	V_I	O/UF	BINARY OUTPUT BITS					
			D5	D4	D3	D2	D1	D0
Underflow	$< -40\ \Omega \times I_{RT}$	1	0	0	0	0	0	0
0	$-40\ \Omega \times I_{RT}$	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	1
.	.	.	.		.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	0
255	$-8\ \Omega \times I_{RT}$	0	1	1	1	1	1	1
Overflow	$> -8\ \Omega \times I_{RT}$	1	1	1	1	1	1	1

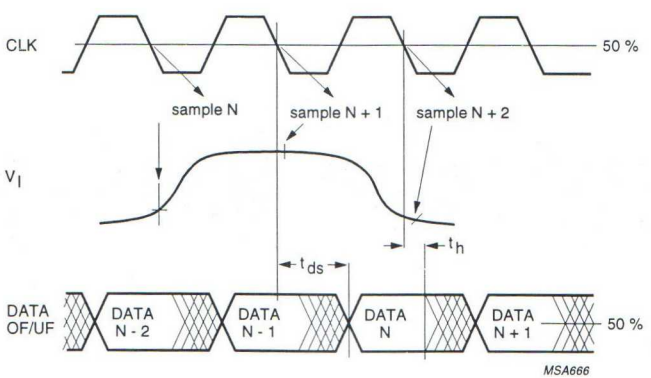
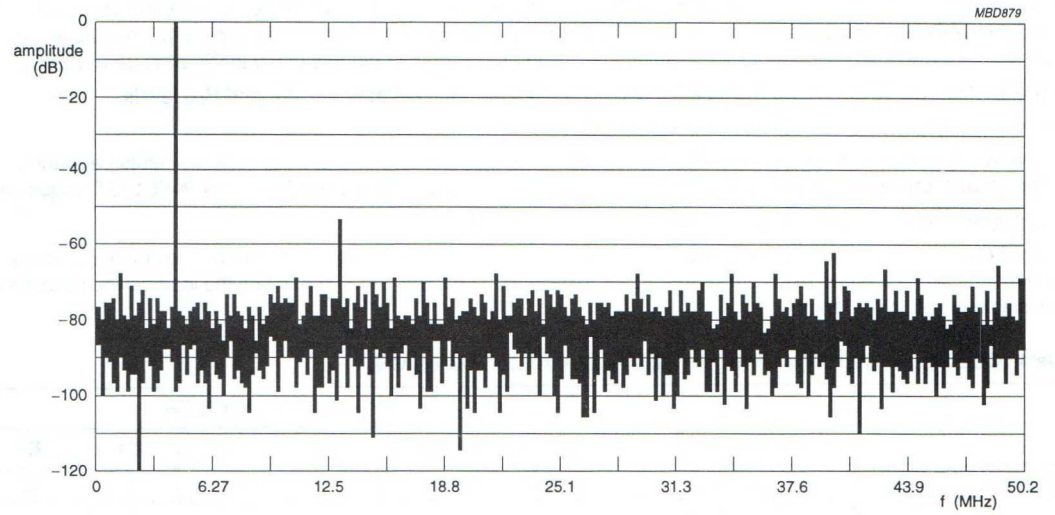
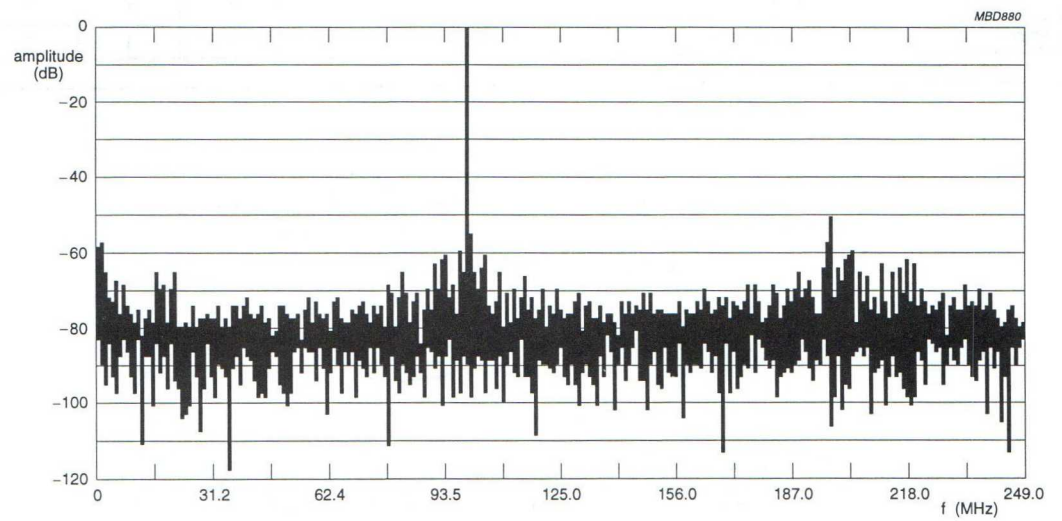


Fig.4 Timing diagram.



Effective bits: 7.53; THD = −54.56 dB.
Harmonic levels (dB): 2nd = −77.28; 3rd = −54.76; 4th = −71.43; 5th = −71.85; 6th = −105.50.

Fig.5 Fast Fourier Transform (f_{clk} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 6.60; THD = −48.60 dB.
Harmonic levels (dB): 2nd = −64.81; 3rd = −51.10; 4th = −65.05; 5th = −58.33; 6th = −54.07.

Fig.6 Fast Fourier Transform (f_{clk} = 500 MHz; f_i = 100 MHz).

APPLICATION INFORMATION

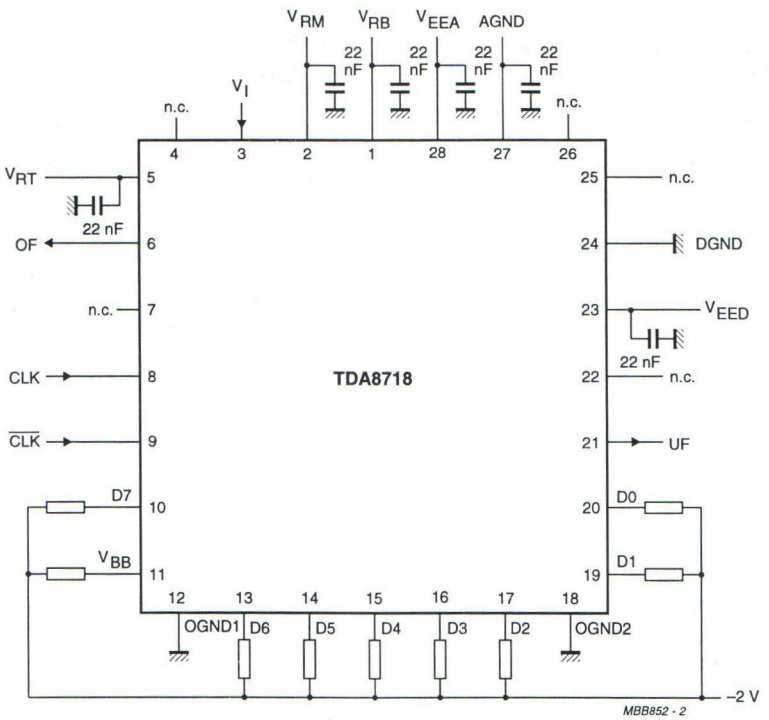


Fig.7 Application diagram.

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

FEATURES

- Video amplifier with clamp and white clip circuits
- FM sound modulator
- Asymmetrical and symmetrical RF outputs available
- Symmetrical RF oscillator using only a few external components
- External adjusting of modulation depth and level of the sound subcarrier
- I²C-bus receiver for frequency setting and test-mode selection
- One I²C programmable output port
- On-chip Phase-Locked Loop (PLL) frequency synthesizer
- On-chip power supply regulator
- Bus switchable oscillator
- On-chip Test Pattern Signal Generator (TPSG).

GENERAL DESCRIPTION

The TDA8722 is a programmable modulator which generates an RF TV channel from a baseband video signal and a baseband audio signal in the event of negative video and FM sound standards (PAL B/G, I, D/K and NTSC).

It is especially suited for satellite receivers, video recorders and cable converters. The video carrier frequency is set exactly to the correct channel frequency by a PLL synthesizer which is programmed in accordance with the I²C-bus format.

APPLICATIONS

- Video recorders
- Cable converters
- Satellite receivers.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8722T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA8722M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

I²C-bus programmable modulator for negative video modulation and FM sound

QUICK REFERENCE DATA

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C after the IC has reached thermal equilibrium; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DD}	total supply current	normal mode	41	52	63	mA
Δm	typical modulation depth range	video level (pin 19) = 0.5 V (p-p); note 1; see Fig.10	65	–	90	%
$\Delta P/S$	typical picture-to-sound level range	note 2; see Fig.11	−18	–	−10	dB
V_{RF}	RF output voltage level asymmetrical on a 75 Ω load	frequency between 471.25 and 855.25 MHz	77	80	83	dBμV
δf	FM deviation on audio subcarrier	$f_i = 400$ Hz; $V_1 = 0.5$ V (RMS); before pre-emphasis filter	20	25	30	kHz

Notes

1. Value depends on value of resistor R17 (see Fig.7).
2. Value depends on value of capacitor C17 (see Fig.7).

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

BLOCK DIAGRAM

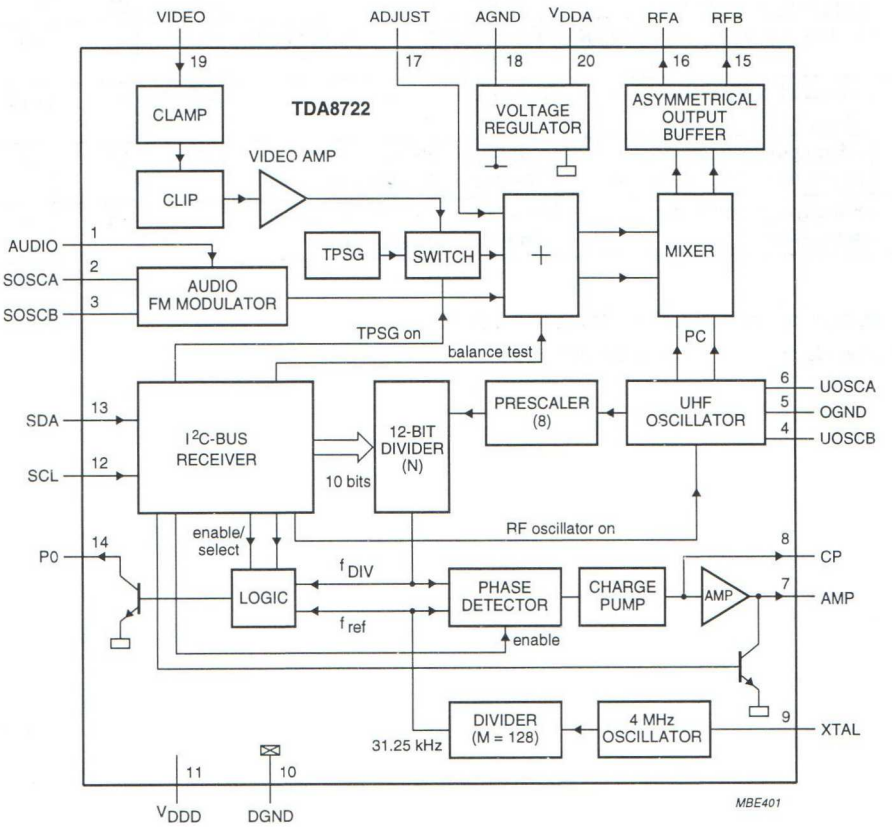


Fig.1 Block diagram.

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

PINNING

SYMBOL	PIN	DESCRIPTION
AUDIO	1	audio input
SOSCA	2	sound oscillator A
SOSCB	3	sound oscillator B
UOSCB	4	UHF oscillator B
OGND	5	RF oscillator ground
UOSCA	6	UHF oscillator A
AMP	7	tuning amplifier output
CP	8	charge pump output
XTAL	9	crystal oscillator
DGND	10	digital ground
V_{DDD}	11	digital supply voltage
SCL	12	serial clock input (I²C-bus)
SDA	13	serial data input (I²C-bus)
P0	14	NPN open-collector output Port
RFB	15	asymmetrical RF output B
RFA	16	asymmetrical RF output A
ADJUST	17	modulation depth and picture-to-sound distance adjustment pin
AGND	18	analog ground
VIDEO	19	video input
V_{DDA}	20	analog supply voltage

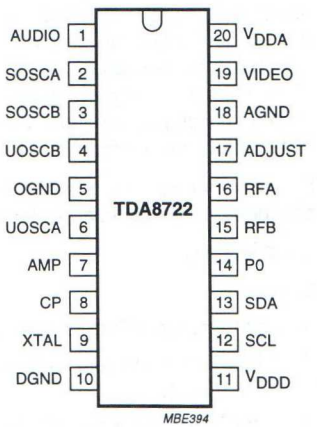


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8722 is a programmable modulator which can be divided into two main blocks:

- A modulator for negative video modulation and FM sound TV standards
- A programmable PLL frequency synthesizer.

The video part of the modulator consists of a clamping circuit which sets the internal reference voltage to the bottom of the synchronizing pulse, followed by a white clip which avoids over modulation in case the video signal is too strong. Typically, the IC starts to clip the video signal when the voltage at the video input (pin 19) is >560 mV (p-p) while the normal voltage at the video input is 500 mV (p-p). This clipping function ensures that the video modulation depth is not too high. The modulation depth is adjusted in the application between at least 65 and 90% by changing the resistor value between pin 17 and ground (R17). The value can change between 47 kΩ and infinite (R17 removed); see Fig.10.

The video part also contains a test pattern signal generator to simplify the adjustment of the receiving channel of the TV set to the required channel of the modulator. The pattern consists of a synchronization pulse and two vertical white bars on screen (see Fig.3).

The audio part of the modulator contains an FM sound modulator. The frequency of the sound subcarrier is set in the application by external components (C3, L3 and R3). The difference between the video carrier level and the sound subcarrier level is adjusted in the application by changing the value of the capacitor between pin 17 and ground (C17). The value can change between 0 and 47 pF. The distance between the video carrier and the sound subcarrier can be adjusted between at least −10 and −18 dB (see Fig.11).

To bias the audio input it is necessary to put a resistor in the application between pin 1 and ground. The resistor has a typical value of 12 kΩ.

The RF part of the oscillator consists of:

- An oscillator which operates at the required video carrier frequency. The range of the oscillator is determined in the application by C5, C6, L5 and D5.
- An RF mixer. It first combines the video signal and the sound subcarrier to build a baseband TV channel. Then the baseband signal is mixed with the oscillator signal to get the RF TV channel. The mixer has two outputs which can be used as two independent asymmetrical outputs, or as one symmetrical output. In the event of asymmetrical use, the unused output must be loaded with a 75 Ω resistor (see Fig.7).

The oscillator frequency is set by a programmable PLL frequency synthesizer in accordance with equation:

$$f_{osc} = 8 \times N \times f_{ref}$$

Where:

f_{osc} is the local oscillator frequency.

N is a 12-bit dividing number (10 bits are programmable by the I²C-bus).

f_{ref} is the crystal frequency (4 MHz) divided by 128 (31.25 kHz).

The circuit allows a step of 250 kHz but because only 10 bits are programmable, the programming steps are 1 MHz.

When the PLL loop is locked, both inputs of the phase comparator are equal, which gives equation:

$$f_{DIV} = \frac{f_{osc}}{8 \times N} = \frac{f_{xtal}}{128} = f_{ref}$$

During the test mode operation, f_{DIV} and f_{ref} can be monitored on the output Port pin (pin 14).

Software information

The synthesizer is controlled via a two-wire I²C-bus receiver. For programming, the address byte (C8 HEX) has to be sent first. Then one or two data bytes are used to set the 10 programmable bits of the dividing number N, the test bits (see Table 1) and the output Port state. Note that after power-up of the IC, the two data bytes must be sent.

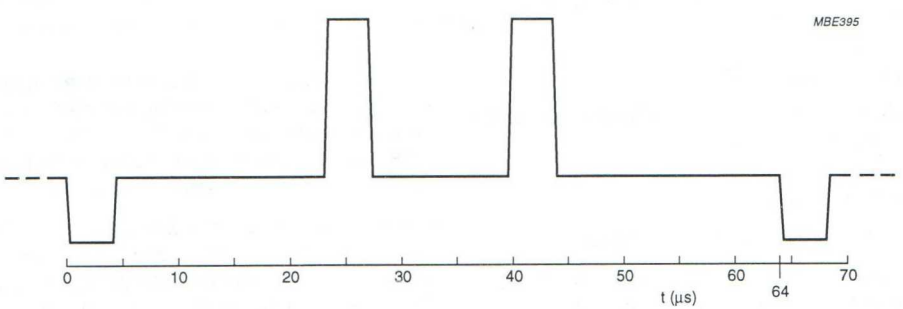


Fig.3 Test pattern signal.

Table 1 Data format; notes 1 and 2

BYTE	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	ACKNOWLEDGE BIT
Address byte C8	1	1	0	0	1	0	0	0	ACK
Data byte 1	0	b11	b10	b9	b8	b7	b6	b5	ACK
Data byte 2	1	T0(3)	T1(3)	T2(3)	P0(4)	b4	b3	b2	ACK

Notes

1. The 10 programmable bits of N are: b2 to b11.
2. Internal hardware sets: b1 = 0 and b0 = 1.
3. T0, T1 and T2 are bits used for test purposes (see Table 5).
4. P0 is a bit used for controlling the state of the output Port (see Table 6).

Table 2 Structure of the dividing number N

RESULT	BITS(1)											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1(2)	b0(2)
Frequency (MHz)(3)	512	256	128	64	32	16	8	4	2	1	0.5	0.25

Notes

1. Bits b2 to b11 are programmable and represent the integer part of the frequency in MHz. Bits b1 and b0 are fixed internally to b1 = 0 and b0 = 1 to get the added 0.25 MHz, common for most TV channels.
2. Bits b1 and b0 are not programmable.
3. f_{osc} = 512b11 + 256b10 + 128b9 + 64b8 + 32b7 + 16b6 + 8b5 + 4b4 + 2b3 + b2 + 0.25 (MHz).

Table 3 Dividing number N for programming channel 21 (471.25 MHz)

RESULT	BITS											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1(1)	b0(1)
Value	0	1	1	1	0	1	0	1	1	1	0	1
Frequency (MHz)(2)	0	256	128	64	0	16	0	4	2	1	0	0.25

Notes

1. Bits b1 and b0 are not programmable.
2. f_{osc} = 0 + 256 + 128 + 64 + 0 + 16 + 0 + 4 + 2 + 1 + 0.25 (MHz) = 471.25 MHz.

Table 4 Content of the data bytes to program channel 21 (471.25 MHz)

BYTE	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	ACKNOWLEDGE BIT
Address byte C8	1	1	0	0	1	0	0	0	ACK
Data byte 1	0	0	1	1	1	0	1	0	ACK
Data byte 2	1	0	0	0	0	1	1	1	ACK

It is possible to change only one data byte. The circuit will recognize which one is received with the value of MSB (0 for data byte 1 and 1 for data byte 2). It is possible to change the frequency by 1 MHz with data byte 2. It is easy to increment the channel frequency when its frequency width is 8 MHz by simply incrementing data byte 1.

The bits T0 to T2 are available for test purposes and the possibilities are shown in Table 5.

Table 5 Test modes

T0	T1	T2	OPERATIONAL MODE
0	0	0	normal operation
0	0	1	Test Pattern Signal Generator (TPSG) on; note 1
0	1	0	RF oscillator off; note 2
0	1	1	balance test; note 3
1	0	0	f_{ref} out (if p0 = 0); note 4
1	0	1	high-impedance test; note 5
1	1	0	f_{DIV} out (if p0 = 0); note 4
1	1	1	phase detector disabled; baseband signals on RF outputs; note 6

Notes

1. In 'TPSG on' mode the video carrier is modulated by the test signal consisting of a synchronization pulse and two vertical white bars on a black screen. This mode should be selected to adjust the TV set receiving the modulated signal to the right frequency.
2. In 'RF oscillator off' mode, the RF oscillator and the RF mixer are switched-off and there is no RF carrier coming out of the device. This mode can be selected to avoid RF radiation to other parts when the modulator output is not used.
3. In 'balance test', the video carrier is over modulated. This simplifies residual carrier measurements.
4. In 'f_{ref}' and 'f_{DIV}' modes, the reference frequency f_{ref} in the phase comparator or the divided RF oscillator frequency f_{DIV} is available on the output Port pin. This mode requires that bit P0 = 0.
5. The 'high-impedance test' mode may be used to inject an external tuning voltage to the RF tank circuit, to test the oscillator. In this mode, the phase detector is disabled and the external transistor of the tuning amplifier is switched-off. The AMP output (pin 7) is LOW (<200 mV).
6. In the 'phase detector disabled' mode, it is possible to measure the leakage current at the input of the tuning amplifier, on the CP pin. In this mode the RF oscillator is off, and the baseband TV channel signal is present on the RF outputs for testing the audio and video parts.

The possibilities of bit P0, which controls the output Port (pin 14) are given in Table 6.

The Port is an NPN open-collector type. For monitoring the f_{ref} or f_{DIV} frequency on the output Port, the P0 bit must be logic 0 to let the output Port free.

Table 6 Output Port programming

P0	OUTPUT PORT STATE
0	off; high impedance
1	on; sinking current

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.3	+6	V
V_{DDD}	digital supply voltage	−0.3	+6	V
V_{DD}	operating supply voltage	4.5	5.5	V
V_{max}	maximum voltage on all pins	−0.3	V_{DD}	V
T_{stg}	IC storage temperature	−40	+125	°C
T_{amb}	operating ambient temperature	−20	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits. Every pin withstands the ESD test in accordance with *"MIL-STD-883C category B"* (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model (MM) 0 Ω, 200 pF (200 V).

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO20; SOT163-1	85	K/W
	SSOP20; SOT266-1	120	K/W

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; valid over the whole UHF band; measured in circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	supply current	normal mode	41	52	63	mA
		RF off test mode	30	38	46	mA
Video characteristics						
I_{19}	input current (AC)	$V_{19} = 3.2$ V	–	0.5	2.0	μA
z_{19}	video input impedance	$V_{19} = 3.2$ V	30	–	–	kΩ
m	modulation depth	$V_{19} = 500$ mV (p-p) EBU colour bars; R17 = 120 kΩ; see Fig.7	77	82	87	%
		during clipping condition; note 1	85	–	98	%
		TPSG mode; R17 = 120 kΩ	72	82	92	%
		balance test mode; R17 = 120 kΩ	110	–	–	%
Δm	modulation depth range	$V_{19} = 500$ mV (p-p) EBU colour bars; 47 kΩ ≤ R17 ≤ ∞	65	–	90	%
Δm_{APL}	variation of modulation depth with change of APL between 10 and 90%	referenced to the value for APL = 50%; $V_{19} = 500$ mV (p-p)	–2	–	+2	%
$V_{clip(p-p)}$	video input level where clipping starts (peak-to-peak value)	video level on pin 19; note 2	–	0.56	–	V
S/N video	video signal-to-noise ratio	$f_{RF} < 700$ MHz; note 3	48	52	–	dB
		$f_{RF} > 700$ MHz; note 3	46	50	–	dB
G_{diff}	differential gain	note 4	–8	–	+8	%
ϕ_{diff}	differential phase	note 4	–8	–	+8	deg
V/S	video-to-sync ratio	$V_{19} = 500$ mV (p-p); V/S = 7/3	6.9/3.1	7/3	7.1/2.9	
f_{video}	frequency response for the video signal	note 5	–1	–	+1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio characteristics (for PAL G standard; audio subcarrier at 5.5 MHz)						
Z_I	audio input impedance		30	–	–	kΩ
δm	modulation deviation	f_I = 400 Hz; V_I = 0.5 V (RMS) before pre-emphasis filter	20	25	30	kHz
$δm_{max}$	maximum modulation deviation	f_I = 400 Hz; V_I = 2.0 V (RMS) before pre-emphasis filter	60	85	–	kHz
THD	total harmonic distortion	f_I = 1 kHz; V_I = 0.5 V (RMS) before pre-emphasis filter	–	0.4	1.5	%
S/N audio	audio signal-to-noise ratio	note 6	45	50	–	dB
f_{audio}	frequency response of the audio signal	note 7	−1	–	+1	dB
P/S	picture-to-sound ratio	no audio signal; FM = 5.5 MHz; C17 = 15 pF	−16	−13	−10	dB
ΔP/S	picture-to-sound ratio range	no audio signal; FM = 5.5 MHz; 0 pF ≤ C17 ≤ 39 pF	−18	–	−10	dB
Channel characteristics						
f_{RF}	RF frequency range	using tank circuit of Fig.7	471.25	–	855.25	MHz
V_{RF}	output level on RFA and RFB	asymmetrical output loaded with 75 Ω; f = 471.25 to 855.25 MHz	77	80	83	dBμV
$ΔV_{RF}$	difference between the level of modulated carrier and the level of the unmodulated carrier	measurement is made during synchronization pulse for the modulated carrier	0	1	2	dB
SPO	spurious outside channel	note 8	–	−62	–	dBc
RF_{sh}	RF second harmonic level on asymmetrical output	f_{RF} = 471.25 MHz	–	−30	−25	dBc
		f_{RF} = 855.25 MHz	–	−20	−15	dBc
SC_{sh}	sound carrier second harmonic level	f_s = 5.5 MHz; C17 = 15 pF; f_{RF} < 700 MHz	–	−65	−60	dBc
		f_s = 5.5 MHz; C17 = 15 pF; f_{RF} > 700 MHz	–	−63	−58	dBc
SC_{th}	sound carrier third harmonic level	f_s = 5.5 MHz; C17 = 15 pF	–	−65	−60	dBc
	video signal harmonics	note 9	–	−60	−55	dBc
f_{ref}	reference frequency spurious	f_p + 31.25 kHz	–	−65	−60	dBc
IM	chrominance beat	note 10	–	−65	−60	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump output (CP)						
I_8	output current		–	±100	–	µA
V_7	output voltage	in lock	1.5	–	2.5	V
I_{OZ}	OFF-state leakage current	V_{CP} = 2 V; T0 = 1; T1 = 1; T2 = 1	–	–	10	nA
Amplifier output (AMP)						
G	amplifier current gain	V_{CP} = 2 V; I_{AMP} = 10 µA	–	4000	–	
V_{7sat}	output saturation voltage	V_{CP} = 0 V; T0 = 1; T1 = 0; T2 = 1	–	140	200	mV
Crystal oscillator characteristics (XTAL)						
Z_9	oscillator input impedance		–	–	–500	Ω
Output Port characteristics (P0)						
V_{OL}	LOW level output voltage	P0 = 1; I_{14} = 5 mA	–	150	400	mV
I_{OZ}	OFF-state leakage current	P0 = 0; V_{DD} = 5.5 V	–	–	10	µA
$I_{14(max)}$	maximum Port current	P0 = 1	–	–	10	mA
I²C-bus receiver characteristics (SDA and SCL)						
V_{IH}	HIGH level input voltage		3	–	5.5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{DD} = 0 or 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{DD} = 0 or 5 V	–10	–	–	µA
V_o	output voltage on SDA	during acknowledge pulse; I_{IL} = 3 mA	–	–	0.4	V

Notes

1. Modulation depth when the video signal is between 560 and 1000 mV (peak-to-peak value) at pin 19. R17 = 120 kΩ in the application.
2. For application information only.
3. Ratio between the CCIR 17 line bar amplitude (corresponding to the level difference between black and white; see Fig.4 and the RMS value of the noise on a black line (line 22 or 335) measured on the video signal after demodulation for PAL G standard. Measurement is unweighted, done between 200 kHz and 5 MHz.
4. Measured for PAL G standard on 4 first steps of CCIR 330 line, corresponding to a 5 step staircase with 300 mV (peak-to-peak value) chrominance carrier when the level between synchronization pulse and white is 1 V; see Fig.5.
5. Measured with a spectrum analyzer with 'peak hold' function, applying a 500 mV (peak-to-peak value) sine wave at the video input of the IC, with a frequency of 0.5, 2.0, 4.0 and 4.8 MHz. The reference is the value measured for 1.0 MHz.
6. Measured using CCIR 468-3 weighting filter and quasi-peak detection, with an audio frequency of 1 kHz and a deviation of 50 kHz. Video signal is EBU colour bars of 500 mV (peak-to-peak value) on pin 19.
7. Measured in PAL G standard with no pre-emphasis on the audio input and no de-emphasis in the receiver. Audio input level is adjusted for having a deviation of 25 kHz at 1 kHz audio frequency. Measurement is done for frequencies between 50 Hz and 15 kHz, reference is the level measured for 1 kHz.

8. Except for the harmonics of the RF oscillator frequency and for the combinations between the RF oscillator frequency and the sound oscillator frequency ($f_{RF} + 2f_s$, $2f_{RF} + f_s$, etc.). This measurement includes the spurious at the $\frac{1}{4}f_{RF}$, $\frac{1}{2}f_{RF}$ and $\frac{3}{4}f_{RF}$.
9. Corresponding to the harmonics of the video signal. Measured by putting a 1 MHz sine wave of 500 mV (peak-to-peak value) at the video input (pin 19) and checking the level at $f_{RF} + 2$ MHz, $f_{RF} + 3$ MHz, etc.
10. Measured with a 4.43 MHz sine wave of 350 mV (peak-to-peak value) at the video input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 1.07 MHz. C17 = 15 pF in the application diagram of Fig.7.

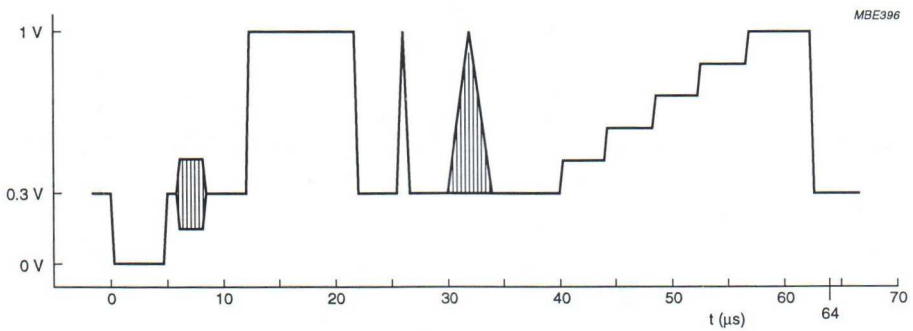


Fig.4 CCIR insertion line N.17.

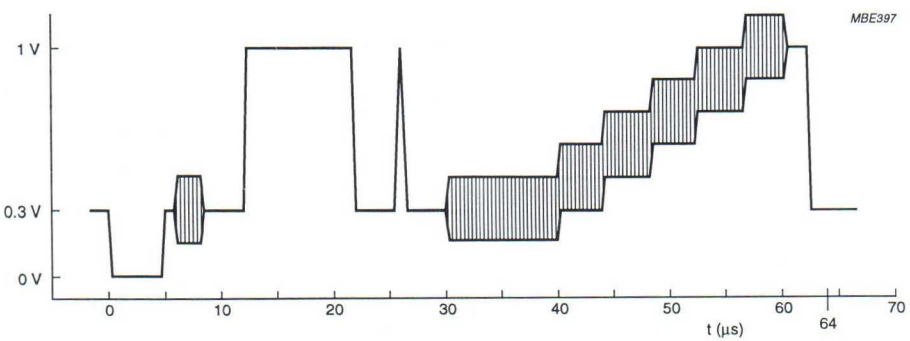
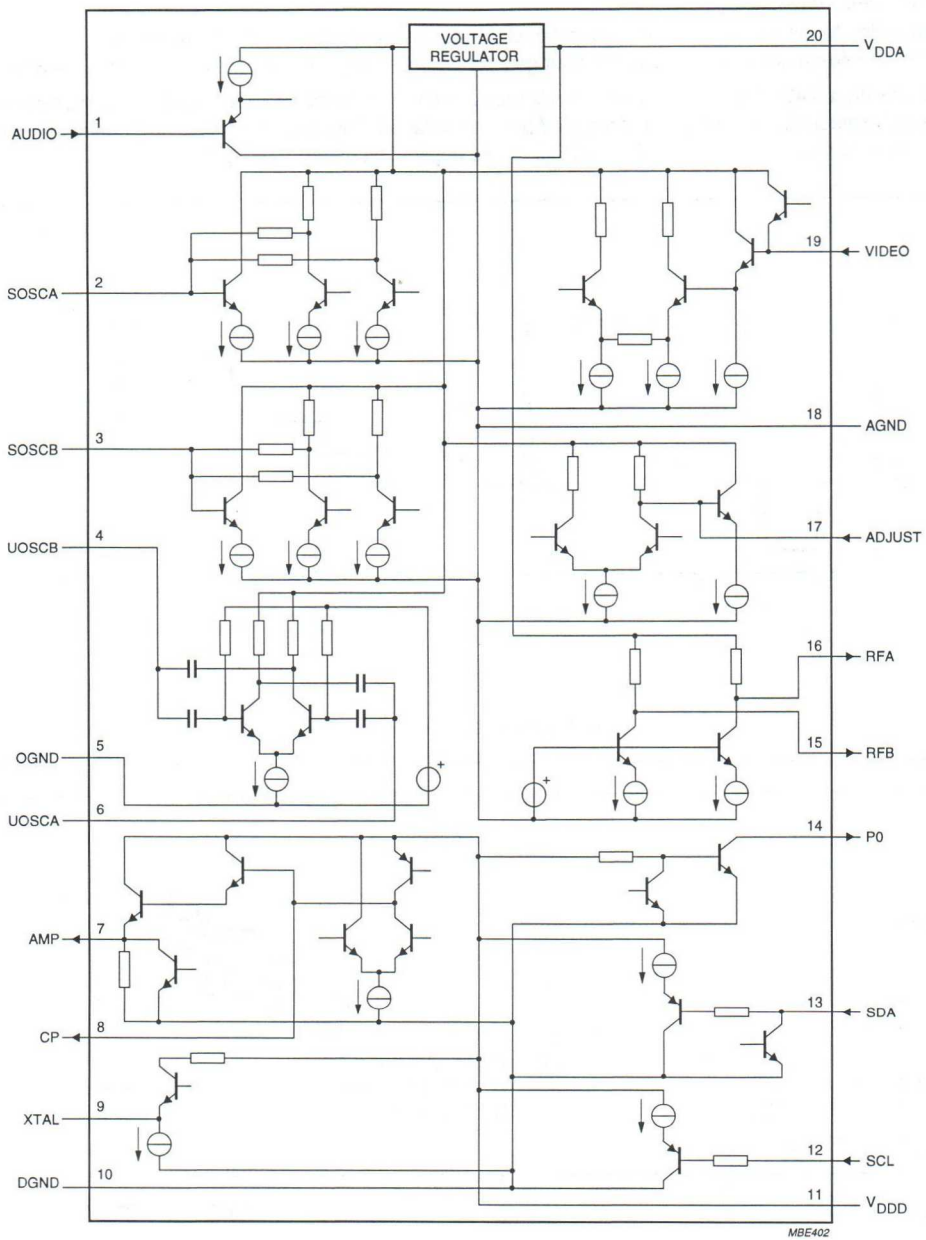


Fig.5 CCIR insertion line N.330.

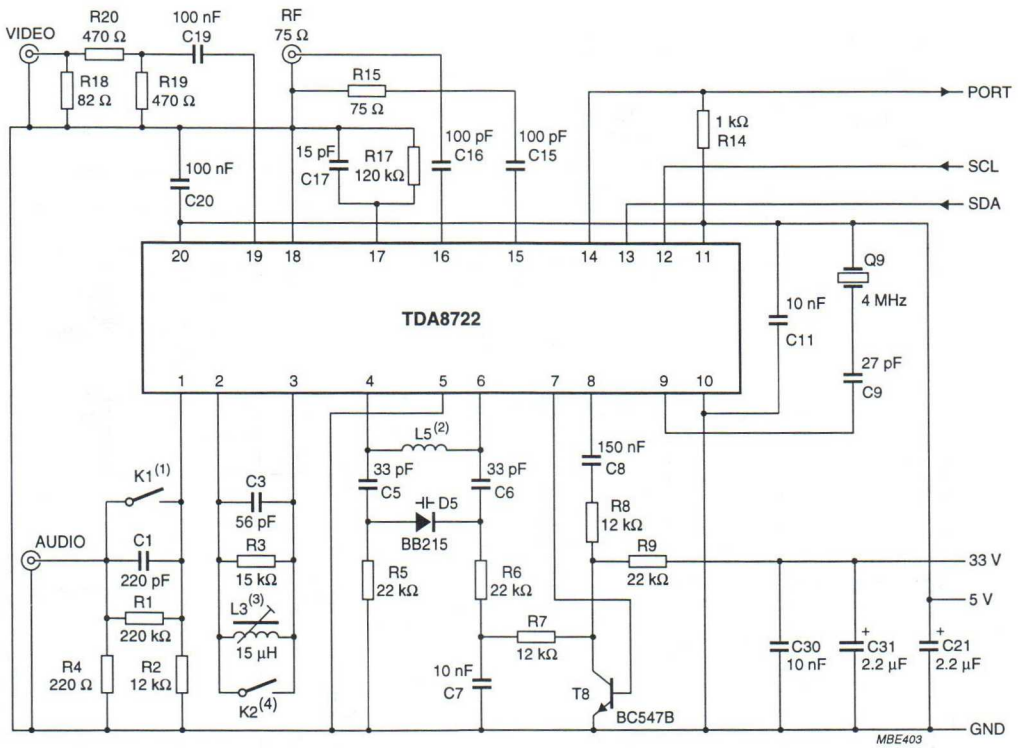
INTERNAL PIN CONFIGURATION



ESD protection components are not shown in the diagram.

Fig.6 Pin equivalent circuit for each pin.

APPLICATION INFORMATION



(1) K1: switches the pre-emphasis filter on or off.

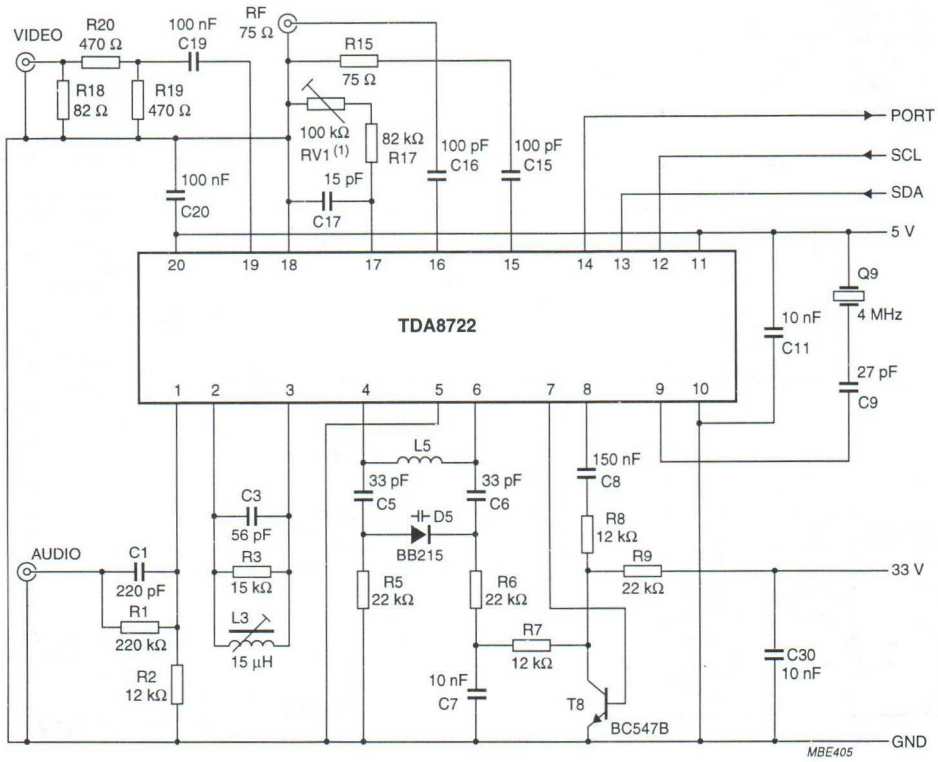
(2) L5: air coil; 1.5 turns; diameter of 2 mm.

(3) L3: to adjust the application to the right sound carrier frequency (5.5 MHz for PAL G).

(4) K2: Switches the FM sound oscillator on or off.

Fig.7 Reference measuring set-up.

Application design



(1) RV1 allows fine adjustment of the modulation depth between 70 and 90%.

Fig.8 Application using an asymmetrical output.

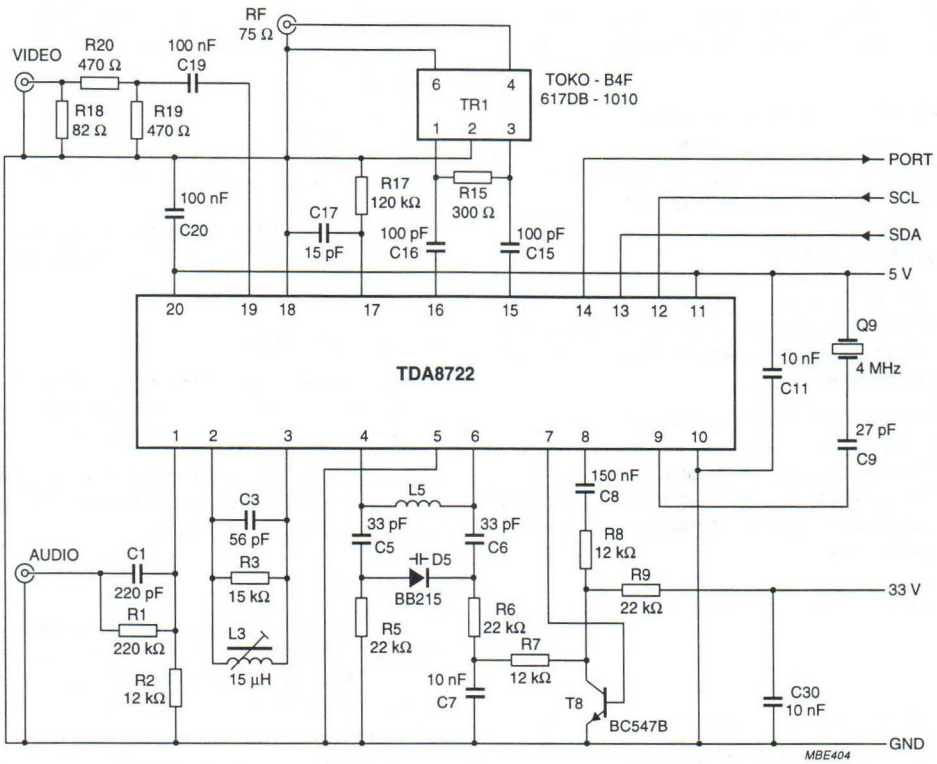


Fig.9 Application using a symmetrical output with a balun transformer.

In the design of the application, it is highly recommended to separate the part of the RF oscillator as much as possible from the part of the RF outputs in order to avoid parasitic coupling between these two parts.

A good solution is shielding the RF oscillator part to avoid radiation from and to this part. The pin 5 (OGND) must be connected to the shielding box and to ground.

RF outputs

For inexpensive applications, it is possible to use the IC with an asymmetrical output (pins 15 or 16). In this event, the unused output pin must be loaded with a load as similar as possible to the load connected to the used pin, see Fig.8.

A good improvement in performance is obtained using a 1 : 4 symmetrical to asymmetrical transformer (balun; balance-to-unbalance) connected between the two outputs. In this event both outputs have their loads matched. The level of the RF second harmonic, and the spurious outside channel is decreasing. The parasitic coupling between RF outputs and RF oscillator is also reduced (see Fig.9).

Modulation depth

With 500 mV (peak-to-peak value) video input signal, the wanted modulation depth must be set by the value of R17 (resistor between pin 17 and ground) as shown Fig.10. For a good accuracy, it is recommended to use a 1% type resistor.

It is also possible to use an adjustable resistor, see Fig.8.

Depending on the layout of the PCB, it may be necessary to slightly change the value of R17 from the one given in Fig.10 to get the wanted modulation depth.

Sound oscillator design

The frequency of the sound subcarrier is fixed by the tank circuit connected between pins 2 and 3. This frequency can be adjusted between 4.5 and 6.5 MHz covering all existing standards in the world.

The damping resistor R3 between pins 2 and 3 is necessary to decrease the quality factor of the tank circuit allowing the frequency to be modulated by the audio signal. The value of this resistor is calculated for several Q factor ranges of the coil for a sound frequency of 5.5 MHz (see Table 7).

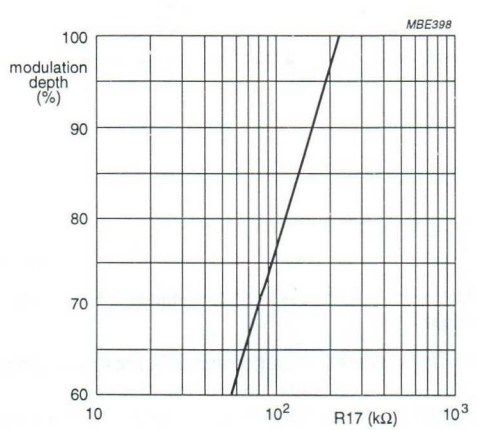


Fig.10 Typical modulation depth as a function of the value of R17.

Table 7 Value of resistor for several Q factor ranges

COIL QUALITY FACTOR	PROPOSED VALUE FOR R3 (kΩ)
30 to 40	82 to 33
40 to 50	33 to 27
50 to 60	27 to 22
60 to 80	22 to 18
80 to >100	18 to 15

The use of a coil with a quality factor <30 may result in a non operating oscillator. For safety, it is recommended to use a coil with a quality factor ≥50.

Picture-to-sound ratio

The picture-to-sound ratio can be adjusted in the application by changing the value of C17 (capacitor between pin 17 and ground); see Fig.11.

Figure 11 shows us that the picture-to-sound ratio will change for a constant value of C17 when the sound subcarrier frequency will change.

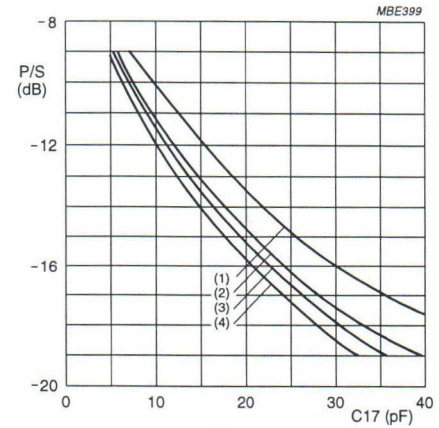
RF harmonics

This IC has been designed to have the lowest level of unwanted RF harmonics at the frequencies where these are the hardest to be filtered out, especially for the second harmonic of the RF carrier at the lowest frequencies of the UHF band.

The level of the second and third RF harmonic is shown in Fig.12 for an asymmetrical application. This chart gives a typical value while the level of these harmonics can vary depending on the design of the application.

It is possible to reduce the level of the second harmonic by using a wide band transformer at the output of the IC and create a symmetrical application (see Fig.9).

To reduce the out-of-band harmonics and especially the third one, it is necessary to use a low-pass filter at the output of the IC.



R17 = 120 kΩ.
(1) 4.5 MHz.
(2) 5.5 MHz.
(3) 6.0 MHz.
(4) 6.5 MHz.

Fig.11 Typical picture-to-sound ratio as a function of the value of C17.

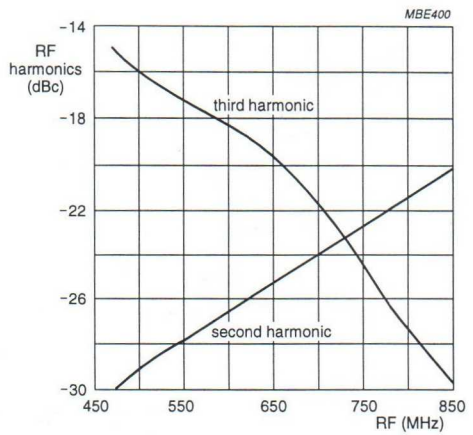


Fig.12 Typical level of RF harmonics for an asymmetrical application.

VHF operation

This IC can operate on frequencies as low as 200 MHz (and especially for VHF 3 band) provided the impedance of the tuned circuit between pins 4 and 6 is >1 kΩ.

NICAM and stereo

Because of the fact that the ADJUST pin (pin 17) is an access point to the RF mixer, it is possible to use this pin to inject an external modulated subcarrier into the IC.

This is especially interesting when it is necessary to transmit a second frequency modulated audio subcarrier for stereo sound (f = 5.72 MHz) or a NICAM QPSK modulated carrier for digital audio transmission (f = 5.85 or 6.552 MHz).

The incoming signal must be externally modulated either in FM with the desired signal corresponding to PAL B/G specification for stereo sound transmission, or in QPSK in accordance with the NICAM transmission system.

The input impedance on pin 17 is approximately 3500 Ω, the incoming signal must be capacitive coupled, the resistor R17 between pin 17 and ground must remain to adjust the modulation depth, the capacitor C17 between pin 17 and ground may be changed depending on the capacitance brought on by the incoming network. If this capacitance is large, it is possible to remove C17. Figure 13 shows a possible application for injecting such kind of signal into the modulator IC.

Following this application, to get a picture-to-second sound carrier ratio of –20 dB, it is necessary to apply a level of approximately 800 mV (peak-to-peak value) at the second carrier input, when the picture-to-first sound carrier ratio is approximately –13 dB.

In addition, the internal FM sound modulator can be switched off by short-circuiting pins 2 and 3.

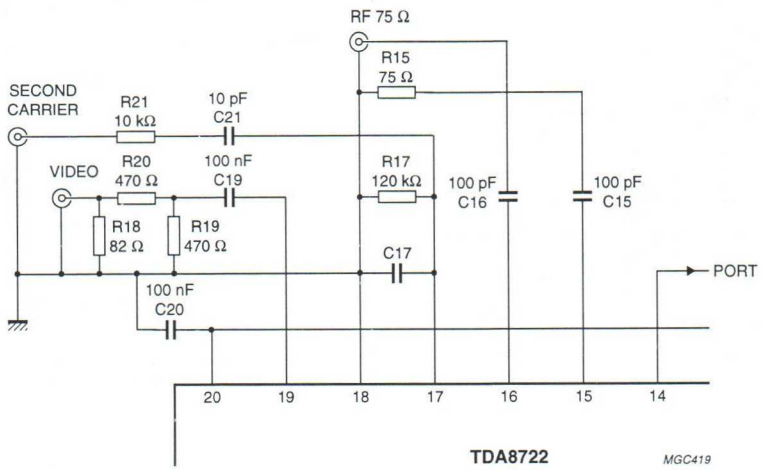


Fig.13 Possible application for a second sound subcarrier.

Antenna signal processor TDA8725T

FEATURES

- 75 Ω antenna input stage
- 75 Ω VCR RF input stage
- 75 Ω VCR tuner output
- 75 Ω TV tuner output.

GENERAL DESCRIPTION

The TDA8725T has been designed to split and combine RF signals for Picture-In-Picture (PIP) and VCR applications.

For PIP applications, the antenna input signal is split and fed to the main TV tuner and the PIP tuner. Good signal suppression between the two outputs enables good quality of the main picture when the PIP tuner is in use.

For VCR applications, the antenna input signal is split and then fed directly to the VCR tuner and the TV tuner after being combined with the VCR - RF signal. Good signal suppression between the two outputs enables good quality pictures when the TV and VCR tuners are both operating. Good signal suppression between the VCR input and the antenna input reduces the amount of unwanted signal on the antenna.

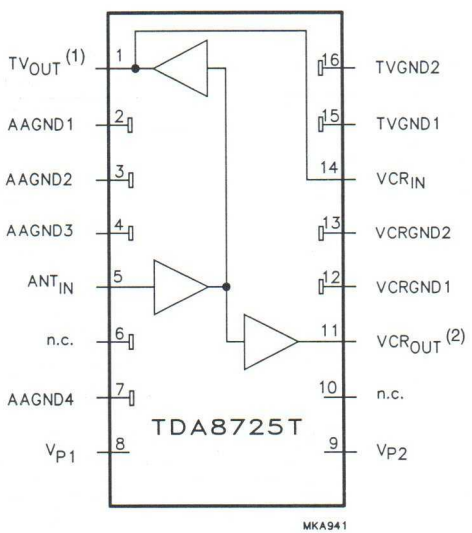
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 8 and 9)		4.75	5.0	5.25	V
I_P	supply current (pins 8 and 9)		–	65	–	mA
f_i	input frequency		40	–	860	MHz
G_p	power gain					
	from antenna to VCR		3.5	5.0	6.5	dB
	from antenna to TV		4	5.5	7	dB
	from VCR		–	0	–	dB
F	noise figure		6.5	9.0	10	dB
IP2	antenna linearity 2nd order intercept point	at 40 MHz	137	140	–	dBμV
		at 860 MHz	119	124	–	dBμV
IP3	antenna linearity 3rd order intercept point	at 40 MHz	121	124	–	dBμV
		at 860 MHz	108	111	–	dBμV
s_{sup}	signal suppression					
	VCR input to antenna	0 to 1 GHz	32	37	–	dB
		1 to 3 GHz	25	30	–	dB
	VCR output to TV output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
	TV output to VCR output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
VSWR	voltage standing wave ratio					
	at the antenna input		–	2.5	4	
	at the outputs		–	1.5	3	
$P_{i(max)}$	maximum input power on antenna for 1 dB gain compression		–	–10	–	dBm

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8725T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) TV tuner or main tuner.
(2) VCR tuner or PIP tuner.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TV_{OUT}	1	output to TV tuner (VCR+TV) and to main tuner (PIP)
AAGND1	2	antenna amplifier ground 1
AAGND2	3	antenna amplifier ground 2
AAGND3	4	antenna amplifier ground 3
ANT_{IN}	5	antenna input
n.c.	6	not connected
AAGND4	7	antenna amplifier ground 4
V_{P1}	8	power supply for the antenna amplifier
V_{P2}	9	power supply for the VCR output amplifier
n.c.	10	not connected
VCR_{OUT}	11	output to VCR and PIP tuner
VCRGND1	12	VCR amplifier ground 1
VCRGND2	13	VCR amplifier ground 2
VCR_{IN}	14	VCR RF input
TVGND1	15	TV amplifier ground 1
TVGND2	16	TV amplifier ground 2

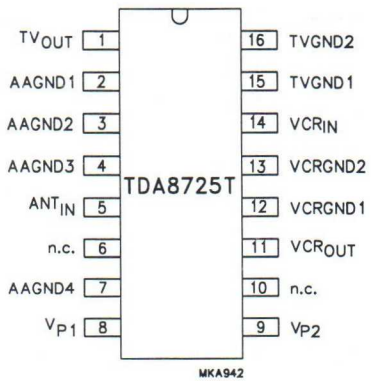


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		−0.3	6	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−10	+80	°C
T_j	junction temperature		−	+150	°C
V_{es}	electrostatic handling	note 1	−2000	+2000	V
		note 2	−200	+200	V

Notes

1. Human Body Model: UZW-BO/FQ-A302 (R = 1500 Ω, C = 100 pF). The IC withstands the ESD test class 2 (2000 V).
2. Machine Model: UZW-BO/FQ-B302 (R = 0 Ω, C = 200 pF). All pins withstand 200 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	115	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 8 and 9)		4.75	5.0	5.25	V
I_P	supply current (pins 8 and 9)		55	65	75	mA
f_i	input frequency		40	–	860	MHz
G_p	power gain	40 to 860 MHz				
	from antenna to VCR		3.5	5.0	6.5	dB
	from antenna to TV		4	5.5	7	dB
	from VCR		–	0	–	dB
F	noise figure		6.5	9.0	10	dB
IP2	antenna linearity 2nd order intercept point	at 40 MHz	137	140	–	dBµV
		at 860 MHz	119	124	–	dBµV
IP3	antenna linearity 3rd order intercept point	at 40 MHz	121	124	–	dBµV
		at 860 MHz	108	111	–	dBµV
s_{sup}	signal suppression					
	VCR input to antenna	0 to 1 GHz	32	37	–	dB
		1 to 3 GHz	25	30	–	dB
	VCR output to TV output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
	TV output to VCR output	0 to 300 MHz	35	40	–	dB
		300 to 860 MHz	22	27	–	dB
VSWR	voltage standing wave ratio					
	at the antenna input		–	2.5	4	
	at the outputs		–	1.5	3	
$P_{i(max)}$	maximum input power on antenna for 1 dB gain compression		–	–10	–	dBm

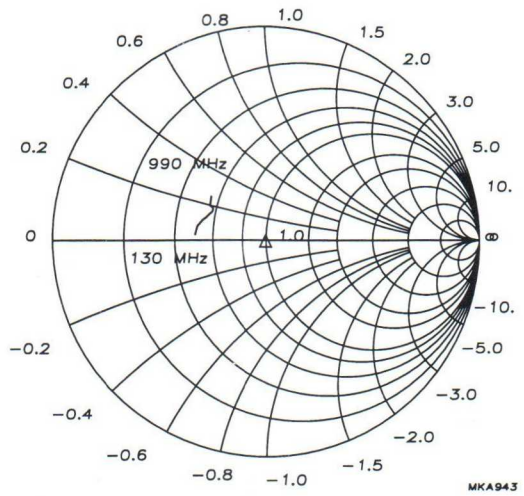


Fig.3 Reflection coefficient (S11) antenna input.

APPLICATION INFORMATION

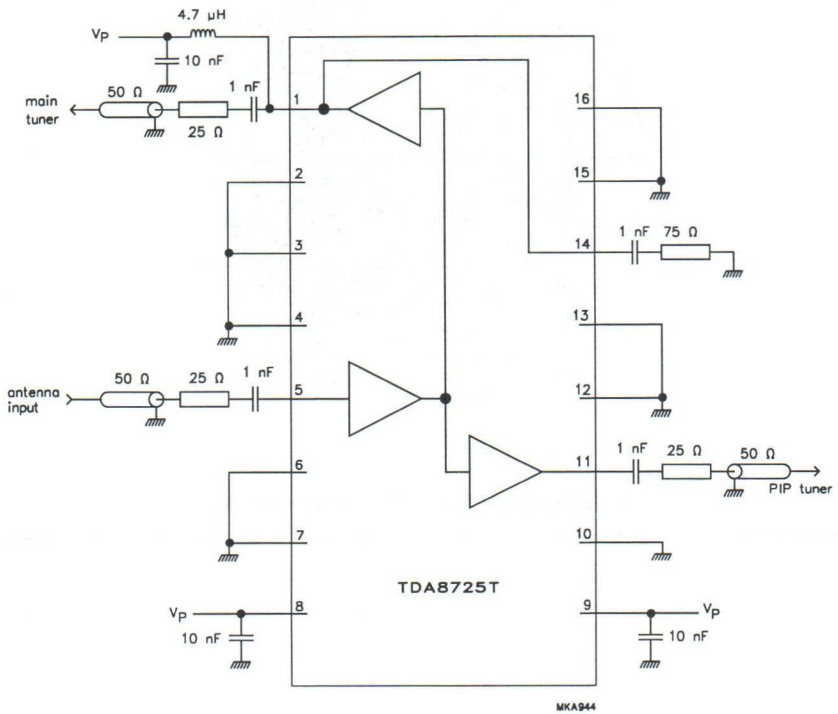


Fig.4 Picture-in-picture (PIP) application.

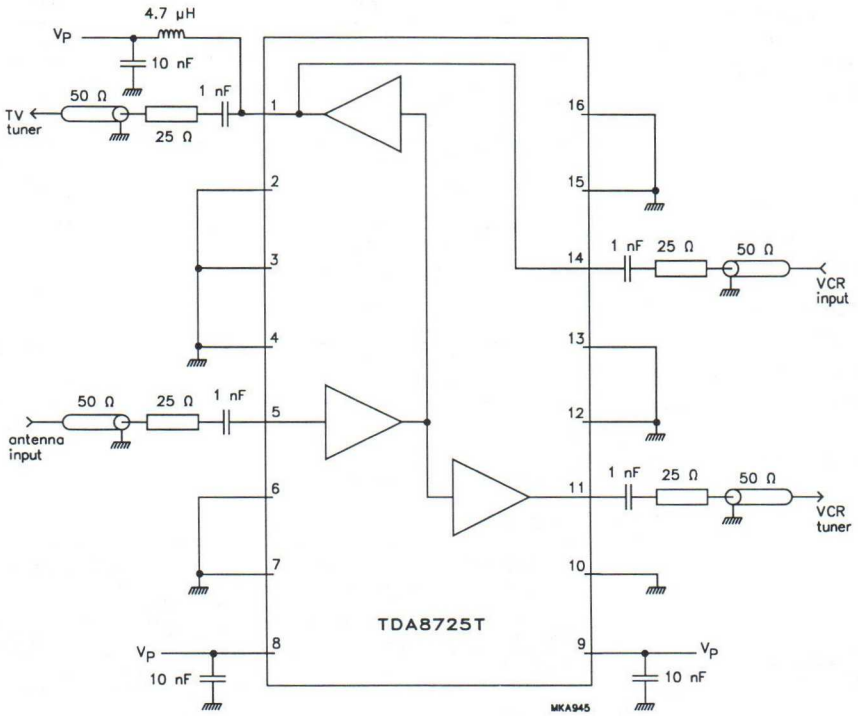


Fig.5 VCR and TV application.

PLL FM demodulator for DBS signals

TDA8730

GENERAL DESCRIPTION

The TDA8730 is a sensitive PLL demodulator for the second IF and direct broadcasting satellite (DBS) receivers. It provides AGC output and threshold adjustment for optimal signal level at the input of the demodulator.

FEATURES

- Broadband IF amplifier
- PLL demodulator, consisting of:
  - a multiplier
  - a voltage controlled oscillator
  - a loop amplifier
- AGC detector and DC amplifier
- LOW impedance video and data output
- Power supply voltage stabilizer

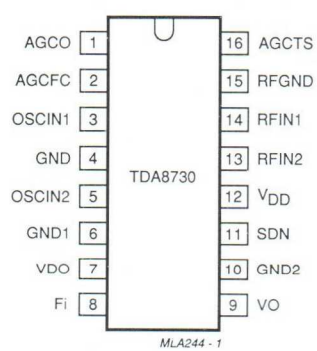


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		-	9	-	V
I_{DD}	supply current		-	75	-	mA
V_I	input voltage level		-	70	-	dBμV
f_{osc}	minimum oscillator frequency		-	130	-	MHz
f_{osc}	maximum oscillator frequency		-	720	-	MHz
V_O	video output signal amplitude (peak-to-peak value)	note 1	-	1.1	-	V
V_{AGC}	AGC output voltage		1.8	-	V_{DD}	V

Note

1. Δf = 13.5 MHz(peak-to-peak value)

PINNING

SYMBOL	PIN	DESCRIPTION
AGCO	1	AGC output
AGCFC	2	AGC frequency compensation
OSCIN1	3	oscillator input 1
GND	4	GND
OSCIN2	5	oscillator input 2
GND1	6	ground 1
VDO	7	variable capacitor drive output
FI	8	feedback input
VO	9	video output
GND2	10	ground 2
SDN	11	stabilizer decoupling node
V_{DD}	12	supply voltage +9 V
RFIN2	13	RF input 2
RFIN1	14	RF input 1
RFGND	15	RF ground
AGCTS	16	AGC threshold setting

APPLICATIONS

Direct broadcasting satellite (DBS) receivers.

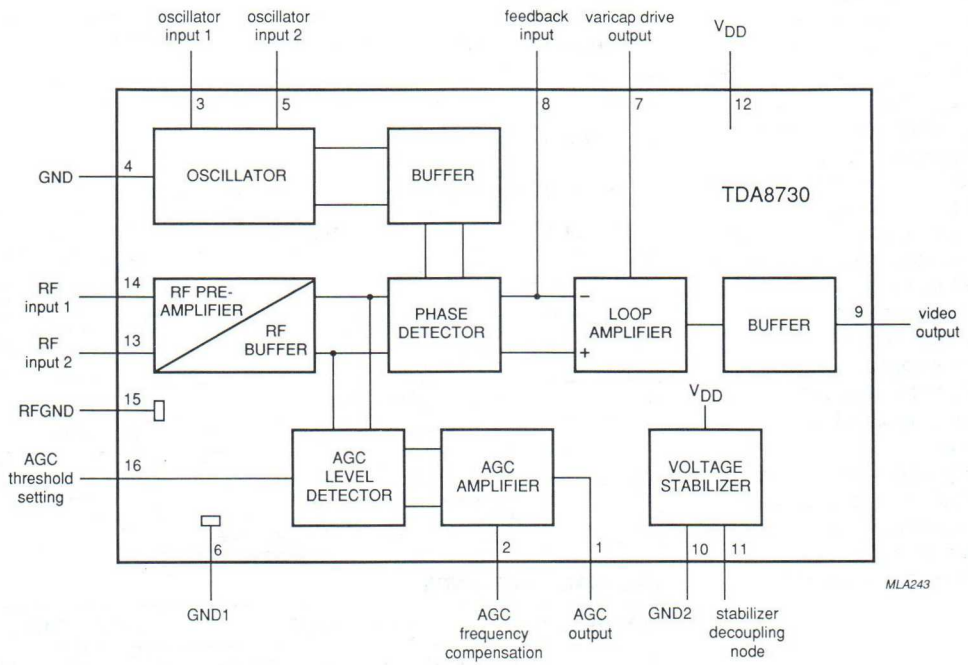


Fig.2 Block diagram.

PLL FM demodulator for DBS signals

TDA8730

FUNCTIONAL DESCRIPTION

The TDA8730 is a PLL FM demodulator intended for use in satellite tuners. It can demodulate frequency deviations ranging from 13.5 $MHz_{(p-p)}$ (DBS services) up to 25 $MHz_{(p-p)}$ (FSS services) and offers a high demodulation linearity. The circuit is optimized for operation at 479.5 MHz (the European IF for satellite tuners) and can handle the various broadcasting standards that are in use (including MAC).
Due to the PLL principle, demodulation noise threshold extension is possible. The high sensitivity of the balanced IF input reduces the additional gain, required in the tuner.
An on-chip AGC circuit delivers a gain control signal for use by the tuner IF amplifier, and a voltage regulator makes the circuit insensitive to supply voltage changes.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8730	16	DIL	plastic	SOT38GE

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	11	V
I_{DD}	input voltage	−0.3	V_{DD}	V
$I_{O(source)}$	output source current	-	10	mA
V_{AGC}	AGC output voltage	-	11	V
t_{sc}	max short circuit time of outputs	10	-	s
$V_{AGC(adj)}$	AGC threshold adjustment voltage	−0.3	V_{DD}	V
T_{stg}	storage temperature	−55	150	°C
T_j	junction temperature	-	150	°C
T_{amb}	operating ambient temperature	−25	85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j-a}$	from-junction-to-ambient in free air	55	-	K/W

CHARACTERISTICS

V_{DD} = 9 V; T_{amb} = 25 °C; f = 480 MHz; Input level 70 dBμV; measured in circuit of Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{pin\ 12}$ to pin 10 or pin15	8.1	9.0	9.9	V
I_{DD}	supply current	$I_{pin\ 12}$; note 1	-	75	90	mA
Frequency demodulator						
f_{osc}	minimum oscillator frequency	-	-	130	-	MHz
f_{osc}	maximum oscillator frequency	-	-	720	-	MHz
V_i	operating input level	pin 13; note 2	-	70	74	DBμV
S11	input reflection coefficient |S11| unbalanced; pin 14 decoupled (50 Ω reference)	pin 13; note 3	-	0.07	-	
	balanced; 100 Ω reference	pin 13 to pin 14	-	0.11	-	
Kd	phase detector constant	(level at pin 13 is 70 dBμV)	-	0.45	-	V/rad.
Ko	VCO constant		-	12	-	MHz/V
Ao	open loop gain of loop amplifier	pin 7 to pin 8	-	40	-	dB
f-3 dB	open loop bandwidth of loop amplifier		-	2.8	-	MHz
Z_{in}	input impedance of feedback input	pin 8	-	930	-	Ω
Z_{out}	output impedance of loop amplifier	pin 7	-	30	50	Ω
le	VCO linearity error over $\Delta f = \pm 10$ MHz	note 4	-	1	-	%
	shift of DC level at video output for $\Delta V_{DD} = \pm 10\%$ with unmodulated 480 MHz input signal	pin 9	-	-	±50	mV
	drift of DC level at video output for T_{amb} = 25 to 50 °C with unmodulated 480 MHz input signal	pin 9	-	-	+50	mV
V_{VCO}	VCO capture range		±14	-	-	MHz
G_d	differential gain	note 5	-	-	±4	%
ϕ_d	differential phase	note 5	-	-	±2	deg.
MOD	intermodulation	note 6	-	–70	-	dB
AGC						
V_{IAGC}	AGC threshold (IAGC = 0 mA) as a function of voltage applied to pin 16 V_{pin16} = 0.8 V	pin 13	-	-	67	dBμV
	$V_{pin\ 16}$ = 9.0 V	note 7	73	-	-	dBμV
	AGC steepness	pin 1; note 8	-	18	-	mA/dB
	AGC output saturation voltage HIGH at I = –0.2 mA	$V_{pin\ 1}$ to pin 10 or pin 15	V_{DD}-0.5	-	V_{DD}	V
	AGC output saturation voltage LOW at I = 0.2 mA		-	1.8	2.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output						
V_O	video output signal amplitude (Δf = 13.5 MHz p-p)	pin 9 to pin 10 or pin 15	-	1.1	-	V
$V_{O(DC)}$	DC level of video output	pin 9 to pin 10 or pin 15; note 9	3.1	3.5	3.9	V
Z_O	output impedance	pin 9	-	30	50	Ω
Z_L	AC load impedance	pin 9; note 10	600	-	-	Ω
Voltage regulator						
V_{ref}	reference voltage for |I loadI ≤ 1 mA	pin 11; note 11	-	7	-	V
V_{reg}	line regulation 8.1 V ≤ VIN ≤ 9.9 V	pin 11	-	70	-	mV
I_{load}	allowable load current	pin 11	–1	-	0	mA

Notes

1. The supply current is the consumption of the circuit only.
   The current consumption of this application is given by the addition of the supply current of the circuit plus the current consumption of external components in the application given. In this event (Fig.4) the typical current is 80 mA.
2. The circuit of Fig.4 is designed for an input level of 70 dBμV.
   The maximum allowable input level for PLL design is 74 dBμV.
   However, for levels other than 70 dBμV the optimum loop filter values will be different from those given in Fig.4.
3. In the application circuit of Fig.4 the RF input is asymmetrically driven.
   In order to reduce the influence of oscillator signal coupling to the RF inputs, it is recommended to use a symmetrical drive at both inputs.
4. The linearity is specified as the maximum difference between the slope df/dV at the channel centre frequency (480 MHz) and the slope at 480 MHz ± 10 MHz.
5. Measurements with test signals in accordance with CCIR Rec. 473-3; Fm signal with DBS parameters: pre-and de-emphasis in accordance with CCIR Rec. 405-1, 625 lines PAL TV system. Modulator sensitive 13.5 MHz/V at pre-emphasis cross over frequency 1 V(p-p) video signal at pre-emphasis filter input.
6. For the intermodulation measurement, an FM test signal is applied having the following modulating components: 1.5 MHz reference sinewave with a deviation of 9.45 MHz(p-p), 5.5 and 5.75 MHz sinewaves with deviation 5.6 MHz(p-p) (so 4.5 dB below the reference, see Fig. 3). At the demodulator output the 2nd order intermodulation is defined according to Fig. 3. The video output is loaded with 500 Ω resistor + DC blocking capacitor.
7. The voltage applied at pin 16 is allowed to be higher than the minimum supply voltage (8.1 V).
8. The voltage at the AGC output (pin 1) decreases when the RF input level at pin 13 increases above the adjusted AGC threshold.
9. The DC level at the video output decreases when the RF input frequency increases.
   The DC level at the video output (pin 9) is measured with the VCO switched off because when the oscillator is operating, the DC level is dependent on the application (oscillator into the input).
10. The load impedance must have at least the minimum value for a frequency range from DC to the bandwidth of the i.f. filter (usually 27 MHz) since wide-band noise components will also appear at the video output.
11. It is possible to use the regulator output voltage (pin 11). The maximum current allowed is 1 mA.
    Possible application as voltage reference source for AFC circuit.

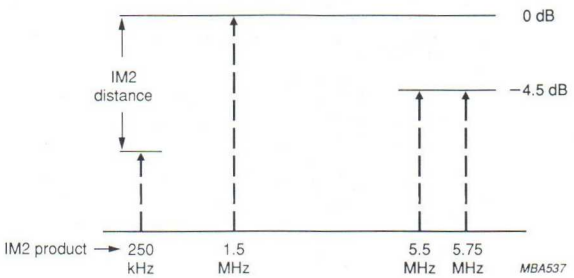


Fig.3 IM2 product.

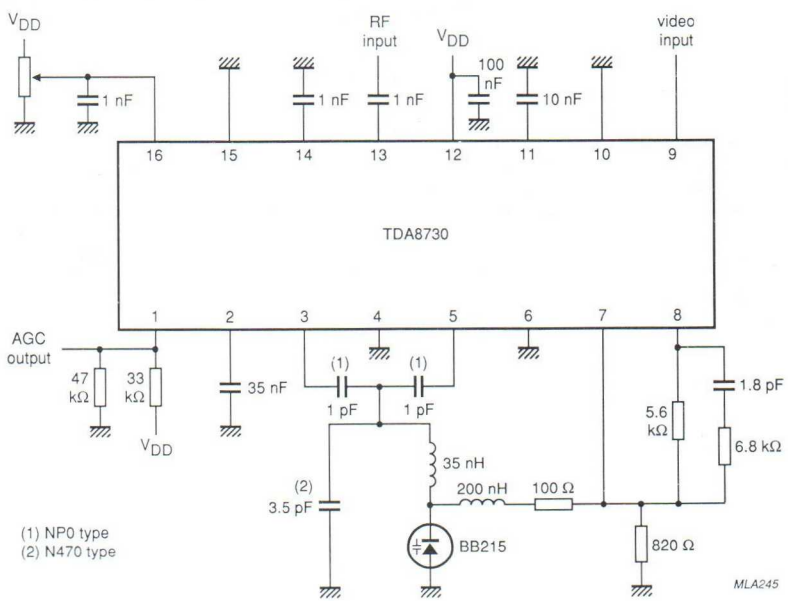


Fig.4 Application information.

NICAM-728 demodulator (NIDEM) TDA8732

FEATURES

- 5 V supplies for analog and digital circuitry
- Low cost application
- Improved noise behaviour
- Limiting amplifier for QPSK input
- Suitable with PAL B, G and I NICAM-728 systems.

APPLICATIONS

- NICAM-728 systems.

GENERAL DESCRIPTION

The NIDEM is a dedicated device providing a DQPSK (Differential Quadrature Phase Shift Keying) demodulator for a NICAM-728 system.
The device interfaces with NICAM-728 decoders and provides data synchronized to a 728 kHz clock (either supplied externally or by the on-board clock).
The device consists of a costas loop quadrature demodulator, a bit-rate clock recovery and differential decoder with parallel-to-serial conversion.
The Voltage Controlled Oscillator (VCO) used in the costas loop is achieved with a single-pin crystal oscillator.
A second single-pin crystal oscillator with a divider chain provides signals at 5.824 MHz and at 728 kHz.
The NIDEM is suitable for PAL B and G (carrier oscillator crystal at 11.7 MHz) and PAL I (carrier oscillator crystal at 13.104 MHz).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5	5.5	V
V_{CCD}	digital supply voltage	4.5	5	5.5	V
V_{CCA}	analog supply voltage	4.5	5	5.5	V
$V_{CCA}-V_{CCD}$	differential supply voltage	−0.5	–	0.5	V
I_{CCA}	analog supply current	–	12.5	–	mA
I_{CCD}	digital supply current	–	14.5	–	mA
V_3	QPSK input level (peak-to-peak value)	30	100	300	mV
R_I	input resistance	1.75	2.5	3.25	kΩ
C_I	input capacitance	–	2	–	pF
f_{CAROSC}	carrier oscillator frequency	11.5	–	13.5	MHz
f_{XTAL}	crystal frequency				
	PAL B, G	–	11.7	–	MHz
	PAL I	–	13.104	–	MHz
f_{CLKOSC}	clock oscillator frequency	–	11.648	–	MHz
f_{C5M}	C5M output frequency	–	5.824	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8732	20	DIL	plastic	SOT146

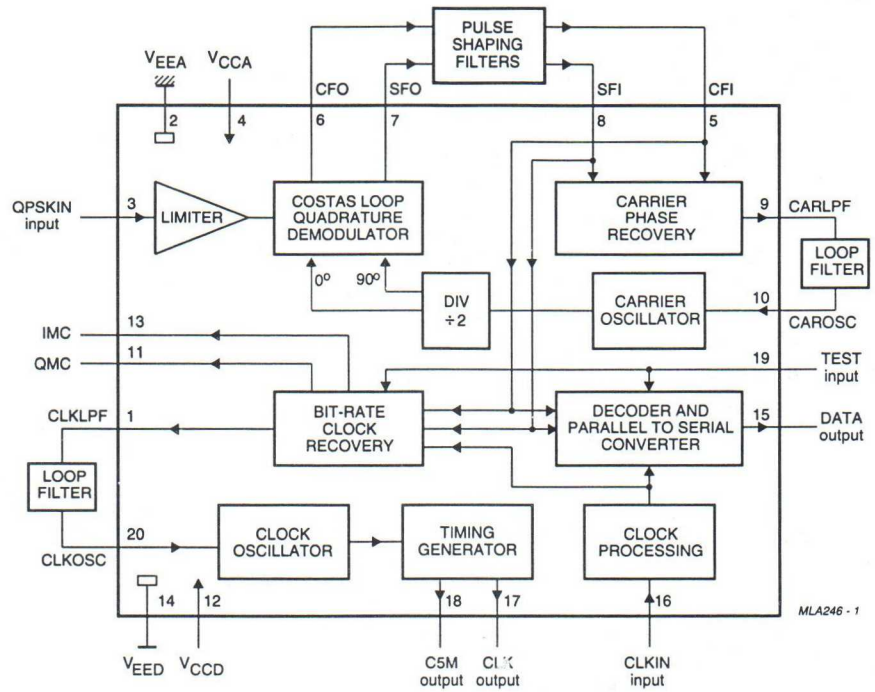


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLKLPF	1	transconductance output for bit-rate loop low-pass filter
V_{EEA}	2	ground for analog circuitry
QPSKIN	3	QPSK modulated data input
V_{CCA}	4	power supply for analog circuitry
CFI	5	baseband cosine channel input after filtering
CFO	6	demodulated cosine channel output to low-pass filter
SFO	7	demodulated sine channel output to low-pass filter
SFI	8	baseband sine channel input after filtering
CARLPF	9	transconductance output for carrier loop low-pass filter
CAROSC	10	crystal input for carrier oscillator (frequency is 11.7 MHz or 13.104 MHz)
QMC	11	monostable components connection for quadrature data transition detector
V_{CCD}	12	power supply for digital circuitry
IMC	13	monostable components connection for in-phase data transition detector
V_{EED}	14	ground for digital circuitry
DATA	15	728 kbit/s demodulated and differentially decoded serial data output
CLKIN	16	bit-rate clock input at 728 kHz, phase-locked to the data
CLK	17	output clock frequency at 728 kHz
C5M	18	reference frequency output at 5.824 MHz (8 x CLK)
TEST	19	input for test purpose (grounded for normal operation)
CLKOS	20	crystal input for clock oscillator (frequency is 11.648 MHz)

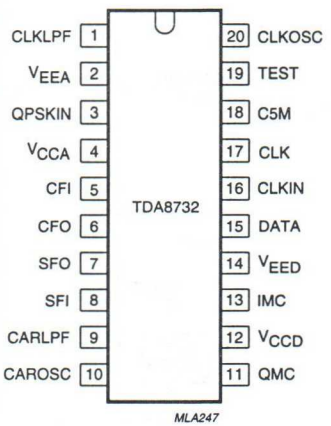


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

QPSK demodulator

The DQPSK signal input to the demodulator (QPSKIN) is limited and fed into the costas loop demodulator. A single-pin carrier oscillator (CAROSC), at twice the carrier frequency, supplies a differential signal to the divider circuitry, which drives the demodulators with both 0° and 90° phase shift. This produces cosine and sine signals which are required for the carrier recovery. Cosine (in-phase) and sine (in Quadrature) channel baseband filters are then provided externally between pins CFO and CFI, and SFO and SFI respectively. The two filtered baseband signals are then processed to provide an error signal, the magnitude and which of which bear a fixed relationship to the phase error of the carrier, regardless of which of the four rest-states the signal occupies. The carrier recovery loop is closed with the aid of a single pin loop filter connection at CARLPF, which filters the error voltage signal to control the 728 kHz as shown in application diagrams Fig.4 and 5.

Bit-rate clock recovery loop

The CFI and SFI channels are processed using edge detectors and monostables, with externally derived time constants (see Fig.3), to generate a signal with a coherent component at the data bit symbol rate. This signal is compared with the clock derived from CLKIN and used to produce an error signal at the transconductance output CLKLPF. This error signal is loop-filtered and used to control the clock generator (at CLKOSC if the on-board clock is used; see Fig.5).

Clock oscillator and timing generator

A voltage-controlled oscillator on-board the NIDEM operates at 11.648 MHz and is divided down to produce a 728 kHz (bit-rate) clock output (CLK) which is phase locked to the pulse stream and may be used as an alternative clock input for NIDEM. A reference clock at 5.824 MHz is provided at pin C5M (TTL levels).

Differential decoder and parallel-to-serial converter

The recovered symbol-rate clocking-signal (364 kHz) produced internally is passed to the demodulator where it samples the sliced raised cosine pulse stream. The recovered bit-rate clocking-signal is passed to the decoder and is used to differentially decode the demodulated data signal and reform it into a serial bit-stream.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	6	V
V_{CCD}	digital supply voltage	−0.3	6	V
QPSKIN	modulated data input voltage	−0.3	5.5	V
CFI	baseband cosine channel input voltage	−0.3	V_{CCA}	V
SFI	baseband sine channel input voltage	−0.3	V_{CCA}	V
CFO	demodulated cosine channel output voltage	−0.3	5.5	V
SFO	demodulated sine channel output voltage	−0.3	5.5	V
CAROSC	crystal input voltage for carrier oscillator	−0.3	5.5	V
CLKOSC	crystal input voltage for clock oscillator	−0.3	5.5	V
QMC,IMC	monostable output voltage	−0.3	V_{CCD}	V
DATA	data output voltage	−0.3	5.5	V
CLK	clock output voltage	−0.3	5.5	V
C5M	reference frequency output voltage	−0.3	5.5	V
CLKIN	bit-rate clock input voltage	−0.3	6	V
TEST	input voltage for test purpose	−0.3	6	V
CLKLPF	bit-rate loop output voltage	−0.3	5.5	V
CARLPF	carrier loop output voltage	−0.3	5.5	V
T_{amb}	operating ambient temperature	0	70	°C
T_{stg}	storage temperature	−40	+125	°C
T_j	maximum junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

V_{CCA} = 5 V ± 10%; V_{CCD} = 5 V ± 10%; −0.5 V < V_{CCA} − V_{CCD} < 0.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5	5.5	V
V_{CCD}	digital supply voltage		4.5	5	5.5	V
V_{CCA}–V_{CCD}	differential supply voltage		−0.5	−	0.5	V
I_{CCA}	analog supply current		−	13	17	mA
I_{CCD}	digital supply current		−	13	17	mA
P_{tot}	total power dissipation		−	130	187	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
CLKIN						
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
V_{IL}	LOW level input voltage		–	–	0.8	V
I_{IH}	HIGH level input current	V_I = 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_I = 0 V	–400	–	–	µA
QPSKIN						
f_{QPSKIN}	input frequency		5	–	7	MHz
R_I	input resistance	f = 6 MHz	1.75	2.5	3.25	kΩ
C_I	input capacitance	f = 6 MHz	–	2	–	pF
SFI, CFI						
I_b	input bias current	V_{SFI} = 4.3 V; V_{CFI} = 4.3 V	–	–	5	µA
R_I	input resistance	f = 364 kHz	70	100	130	kΩ
C_I	input capacitance	f = 364 kHz	–	2	–	pF
CAROSC						
f_{car}	oscillator frequency		11.5	–	13.5	MHz
CARRIER OSCILLATOR CRYSTAL						
	holder			RW 43		
	nominal frequency with specified load	C_L = 15 pF				
$f_{PAL\ I}$	PAL I		–	13.104	–	MHz
$f_{PAL\ B,\ G}$	PAL B, G		–	11.7	–	MHz
	vibration mode	fundamental				
	circuit condition	series resonance				
	adjustment tolerance on frequency at 25 °C		–30	–	+30	10^{-6}
	temperature		0	–	70	°C
	frequency stability over temperature		–30	–	+30	10^{-6}
C_L	load capacitance		–	15	–	pF
R_s	resonance resistance	note 1	15	–	40	Ω
C_m	motional capacitance		–	21	–	fF
C_p	parallel capacitance		–	–	5	pF
	drive power level		–	–	0.5	mW
CLKOSC						
f_{clk}	oscillator frequency	C_l = 15 pF	–	11.648	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BIT-RATE OSCILLATOR CRYSTAL						
	holder			RW 43		
	nominal frequency with specified load	C_L = 15 pF				
$f_{PAL\ I}$	PAL I		–	11.648	–	MHz
$f_{PAL\ B,\ G}$	PAL B, G		–	11.648	–	MHz
	vibration mode	fundamental				
	circuit condition	series resonance				
	adjustment tolerance on frequency at 25 °C		−30	–	+30	10^{-6}
	temperature		0	–	70	°C
	frequency stability over temperature		−30	–	+30	10^{-6}
C_L	load capacitance		–	15	–	pF
R_s	resonance resistance	note 1	15	–	40	kΩ
C_m	motional capacitance		–	21	–	fF
C_p	parallel capacitance		–	–	5	pF
	drive level		–	–	0.5	mW
Outputs						
CFO, SFO						
R_O	output impedance	f = 364 kHz	–	110	200	Ω
V_{amp}	signal amplitude (peak-to-peak value)		0.8	1	–	V
CARLPF						
V_{OL}	LOW level output voltage	I_{OL} = 100 μA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 μA	V_{CCD}−1 V	–	–	V
gm ϕ1	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD} − 1 V	100	125	–	μA/rd
I_{LO}	output leakage current for π/4 phase shift		−5	–	5	μA
CLKLPF						
V_{OL}	LOW level output voltage	I_{OL} = 100 μA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 μA	V_{CCD}−1 V	–	–	V
gm ϕ2	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD}−1 V	50	65	–	μA/rd
I_{LO}	off-state output leakage current		−5	–	5	μA
IMC, QMC (TYPICAL RC NETWORK; R = 22 kΩ; C = 150 pF)						
t_{REC}	monostable recovery time		–	–	600	ns
t_{on}	monostable time		–	1.37	–	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK, C5M						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 µA	2.4	–	V_{CCD}	V
t_r	rise time	C_L = 15 pF; see Fig.3	–	20	–	ns
t_f	fall time	C_L = 15 pF; see Fig.3	–	20	–	ns
f_{C5M}	C5M reference frequency		–	5.824	–	MHz
DATA						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 µA	2.4	–	V_{CCD}	V
t_r	rise time	C_L = 15 pF; see Fig.3	–	30	–	ns
t_f	fall time	C_L = 15 pF; see Fig.3	–	30	–	ns
CLOCK TIMING						
t_d	CLK to C5M delay (pin 17 to 18)		–	15	–	ns
t_d	CLKIN to DATA delay (pin 16 to 15)	V_{CCD} = 4.5 V	–	520	585	ns

Note

1. Only the maximum value is relevant with a 15 Ω resistor in series with the crystal (due to the application requirements).

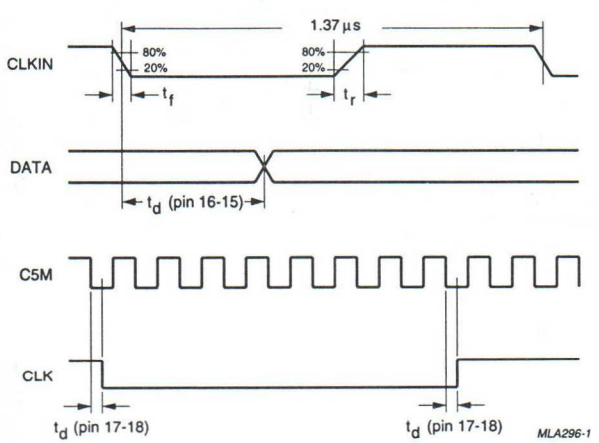
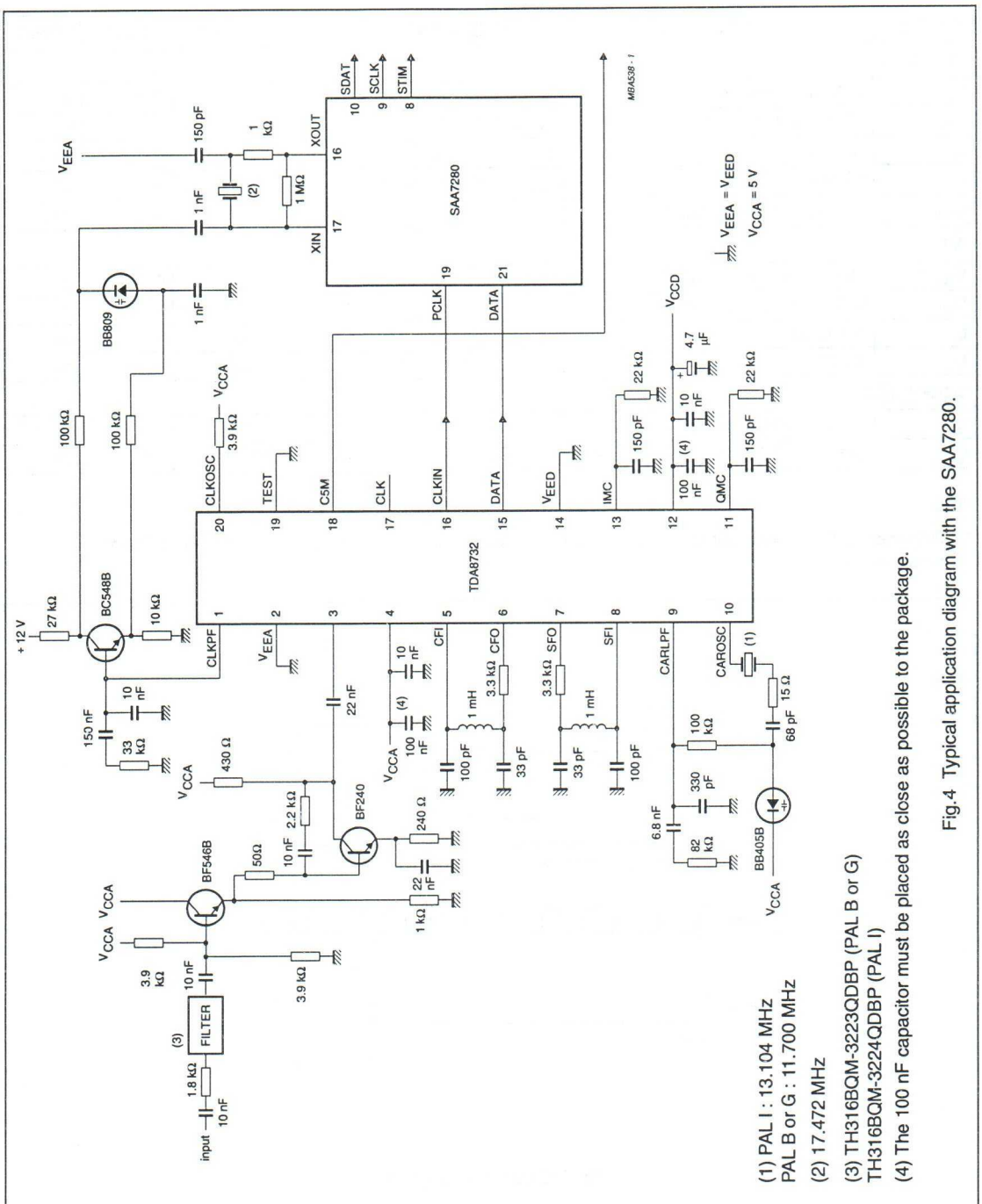


Fig.3 Data timing diagram.



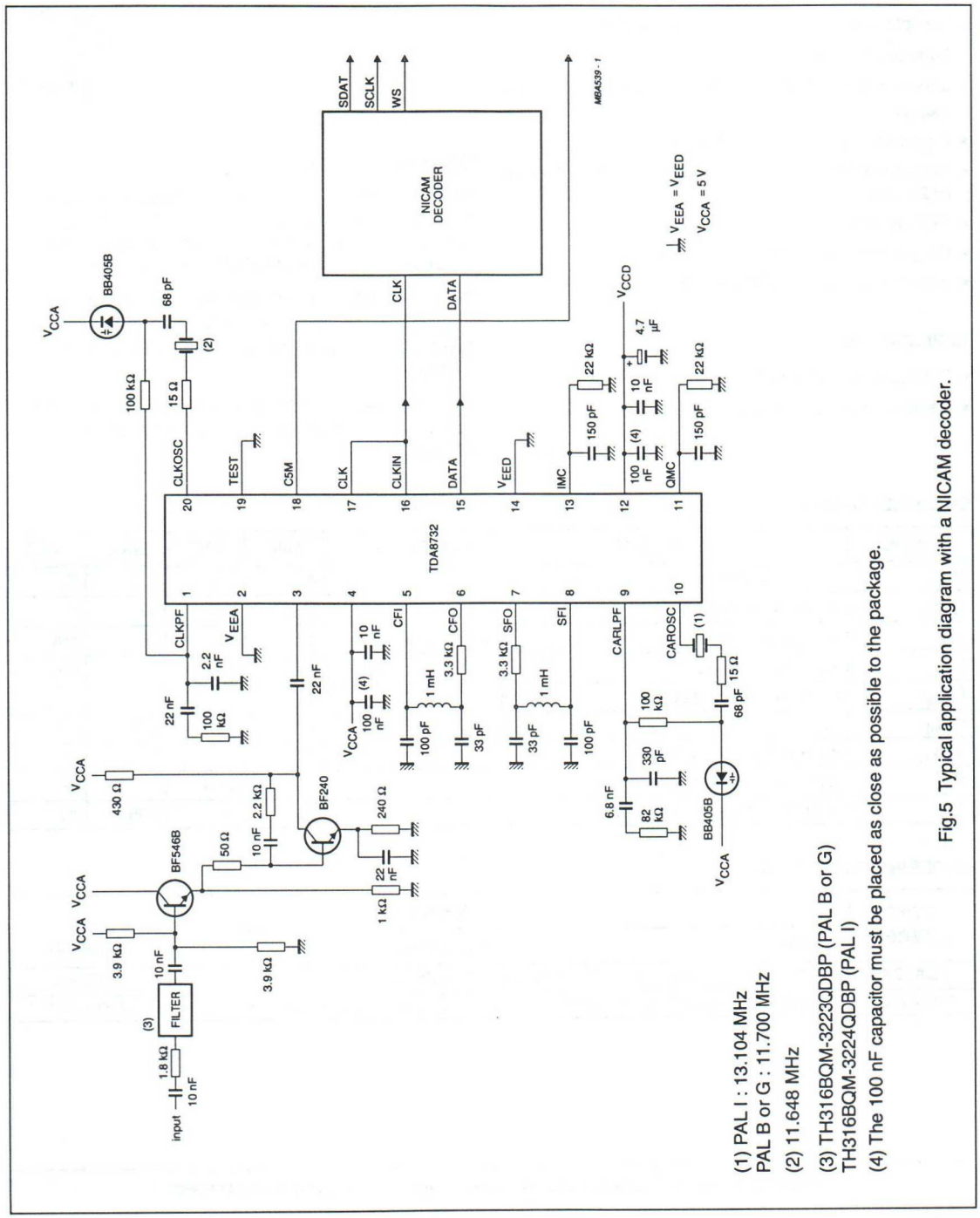
(1) PAL I : 13.104 MHz
PAL B or G : 11.700 MHz

(2) 17.472 MHz

(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.4 Typical application diagram with the SAA7280.



(1) PAL I : 13.104 MHz
PAL B or G : 11.700 MHz

(2) 11.648 MHz

(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.5 Typical application diagram with a NICAM decoder.

PLL frequency synthesizer | TDA8735

FEATURES

- Complete 30 MHz single-chip tuning system
- Loop amplifier included
- 2-level current amplifier (charge pump) for adjusting the loop gain
- A powerful digital memory phase detector
- Programmable reference frequencies of 1 kHz, 10 kHz or 25 kHz
- I²C-bus interface
- Programmable address select input
- Software controlled switch output.

APPLICATIONS

- Satellite sound receiver
- Radio receiver: LW, MW and SW.

GENERAL DESCRIPTION

The TDA8735 is a single-chip PLL synthesizer designed for satellite receivers. The device can be set to two different addresses which can be used in applications where independently tuned VCOs are required.

To adapt to different frequency accuracy, 3 reference frequencies are selectable via the I²C-bus. The charge pump current can be set to 2 values with a ratio of 1 : 100 via the I²C-bus.

A programmable switch (open collector) is integrated to enable mode or normal switching, or other types of application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	outputs unloaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	outputs unloaded	0.2	0.5	1	mA
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)		30	–	500	mV
P_{tot}	total power dissipation		–	0.14	–	W
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8735	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TDA8735T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

BLOCK DIAGRAM

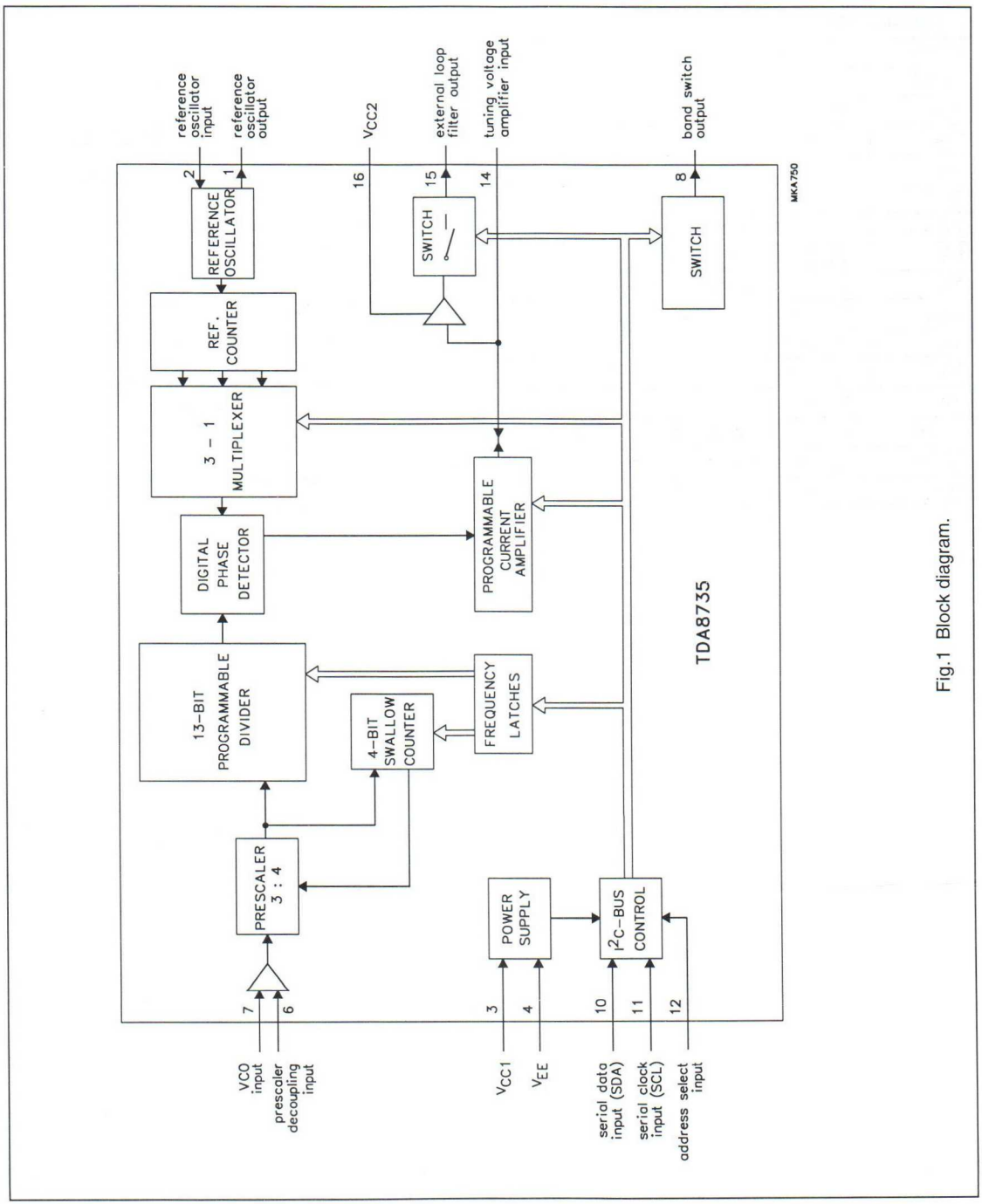


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL1	1	reference oscillator output
XTAL2	2	reference oscillator input
V_{CC1}	3	supply voltage 1
V_{EE}	4	ground
n.c.	5	not connected
DEC	6	prescaler decoupling
VCOFI	7	VCO input frequency
BS	8	band switch output
n.c.	9	not connected
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
n.c.	13	not connected
$LOOP_I$	14	tuning voltage amplifier input
$LOOP_O$	15	external loop filter output
V_{CC2}	16	supply voltage 2

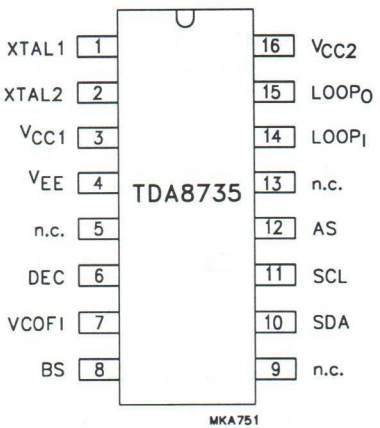


Fig.2 Pin configuration.

Satellite sound circuit with noise reduction TDA8740; TDA8740H

FEATURES

- Demodulation of main audio signal using wide band PLL (lock range selectable)
- Demodulation of secondary audio signals using wide band PLL
- HF input selection: two-out-of-eight secondary audio signals can be selected
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio and external
- Mute control
- Line outputs (SCART level).

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8740; TDA8740H is a multi-function sound IC for use in satellite receivers, television sets and video recorders. The pin numbers given in parenthesis throughout this document refer to the QFP44 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8	12	13.2	V
Main channel						
$V_{IN3(rms)}$	input sensitivity pin 18 (14) (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator					
	either		5.5	–	7.5	MHz
	or		10.0	–	11.5	MHz
V_{OM}	output voltage pin 23 (19)		–9	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	–	dB
Secondary channels						
$V_{IN1,IN2}$	input sensitivity pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$\Delta f_{OS1,2}$	lock range PLL demodulators		6.0	–	8.5	MHz
$V_{OR,OL}$	output voltage pins 24 and 25 (20 and 21)		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	–	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		–	74	–	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		–	74	–	dB
$\alpha_{S/S}$	crosstalk between secondary channels		–	74	–	dB

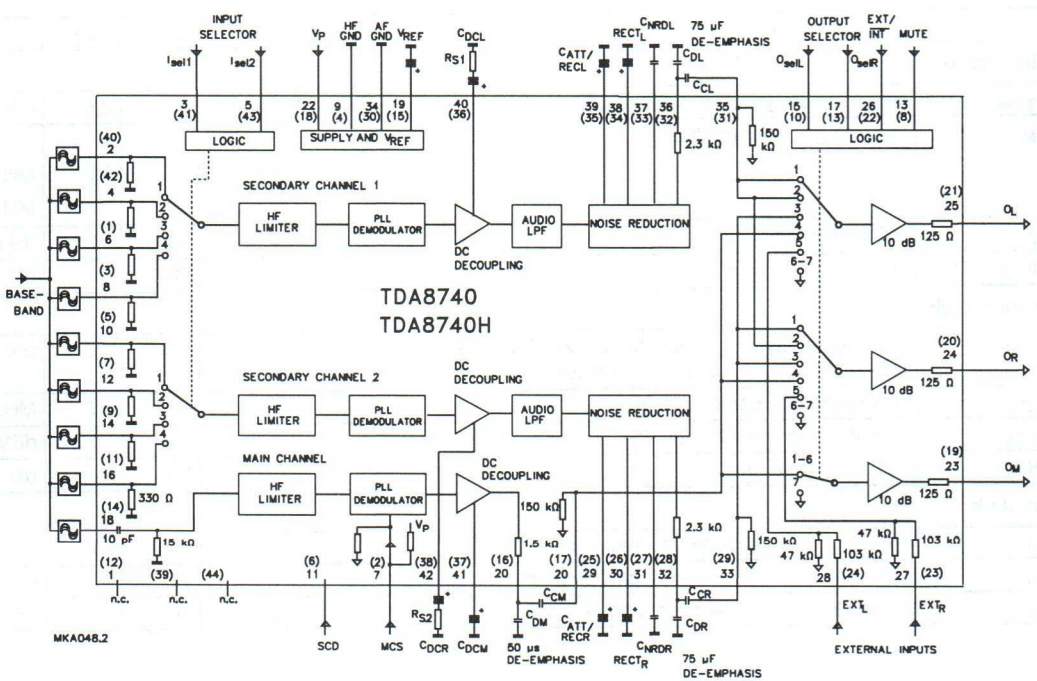
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8740	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8740H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM



The pin numbers in parenthesis refer to the QFP44 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
n.c.	1	39	not connected
IN-1A	2	40	intercarrier input A for Channel 1 (left)
$I_{sel\ 1}$	3	41	input select switch bit 1
IN-1B	4	42	intercarrier input B for Channel 1 (left)
$I_{sel\ 2}$	5	43	input select switch bit 2
IN-1C	6	1	intercarrier input C for Channel 1 (left)
MCS	7	2	main channel PLL lock-in range select/disable
IN-1D	8	3	intercarrier input D for Channel 1 (left)
HFGND	9	4	ground for HF section
IN-2A	10	5	intercarrier input A for Channel 2 (right)
SCD	11	6	secondary channels PLLs disable
IN-2B	12	7	intercarrier input B for Channel 2 (right)
MUTE	13	8	mute switch
IN-2C	14	9	intercarrier input C for Channel 2 (right)
$O_{sel\ L}$	15	10	output select switch bit 1 (left)
IN-2D	16	11	intercarrier input D for Channel 2 (right)
$O_{sel\ R}$	17	13	output select switch bit 2 (right)
IN-3	18	14	intercarrier input for main channel
V_{REF}	19	15	decoupling capacitor for reference voltage
$C_{D\ M}$	20	16	de-emphasis capacitor for main channel
$C_{C\ M}$	21	17	audio pass-through capacitor input for main channel
V_P	22	18	positive supply voltage
O_M	23	19	main channel output
O_R	24	20	right channel output
O_L	25	21	left channel output
EXT/$\overline{INT}$	26	22	output switch bit 3 (external/internal)
EXT_R	27	23	external audio input (right)
EXT_L	28	24	external audio input (left)
$C_{ATT/REC\ R}$	29	25	attack/recovery capacitor (right)
$RECT_R$	30	26	rectifier DC decoupling (right)
$C_{NR\ D\ R}$	31	27	noise reduction de-emphasis capacitor (right)
$C_{D\ R}$	32	28	fixed de-emphasis capacitor (right)
$C_{C\ R}$	33	29	audio pass-through capacitor input for right channel
AFGND	34	30	ground for AF section
$C_{C\ L}$	35	31	audio pass-through capacitor input for left channel
$C_{D\ L}$	36	32	fixed de-emphasis capacitor (left)
$C_{NR\ D\ L}$	37	33	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	34	rectifier DC decoupling (left)
$C_{ATT/REC\ L}$	39	35	attack/recovery capacitor (left)

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
$C_{DC\,L}$	40	36	DC decoupling capacitor (left)
$C_{DC\,M}$	41	37	DC decoupling capacitor (main)
$C_{DC\,R}$	42	38	DC decoupling capacitor (right)
n.c.	–	12	not connected
n.c.	–	44	not connected

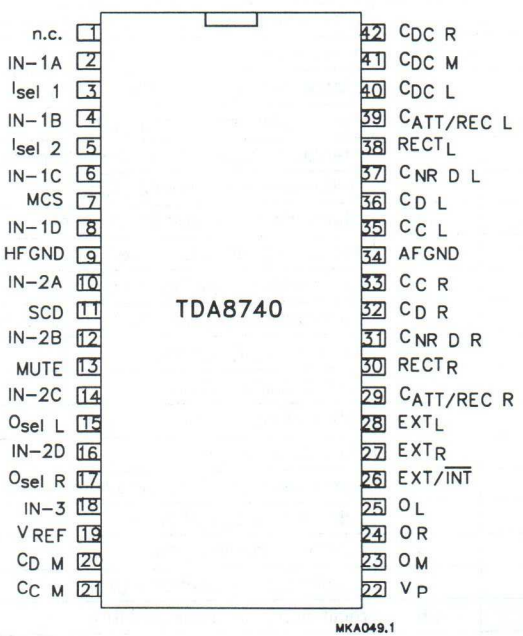


Fig.2 Pin configuration (SDIP42).

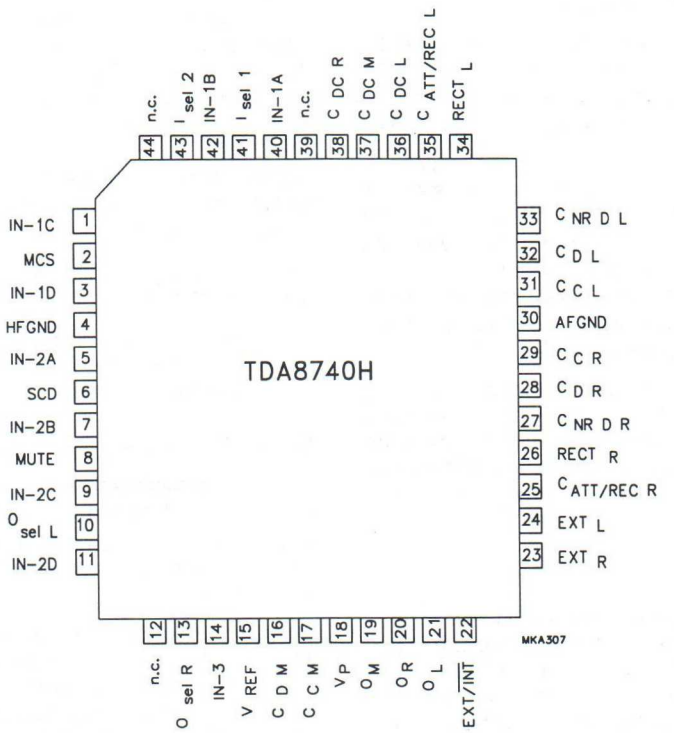


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner contains the demodulated video signal plus a number of sound carriers to facilitate reception of a PAL/NTSC/SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the single channel sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present which can be used for stereo or multi-language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz. The TDA8740; H contains all circuitry for processing the main channel and for two secondary channels, from baseband signal to line (SCART) output drivers. The desired frequencies can be routed to the TDA8740; H via bandpass filters.

Main channel (see Fig.1)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz, PLL off and 10.0 to 11.5 MHz using the MCS signal at pin 7 (2) [when pin 7 (2) is at logic 0, being a voltage from 0 to 1.2 V, the lock-in range = 5.5 to 7.5 MHz; when pin 7 (2) is at logic 1, being a voltage from 3.5 V until V_P, the lock-in range = 10.0 to 11.5 MHz; when pin 7 (2) is in the mid voltage position, being a voltage from 1.8 to 2.8 V, the main channel PLL is switched off]. The mid voltage position of the MCS pin can also be obtained by a floating MCS pin if the circuit supply voltage V_P is 10.8 to 13.2 V. The voltage on the MCS pin is then determined by the resistor divider at this pin between V_P and ground.

If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 (14) via a 6.5 MHz ceramic bandpass filter. Alternatively, if there is a requirement to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In this event the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 (14) via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment-free. High gain and DC error signals from the PLL, which are superimposed on the demodulator output, require DC decoupling. A buffer amplifier is used to amplify the signal to the same level as the secondary channels and decouples DC using an electrolytic capacitor connected to pin 41 (37). The demodulator output signal is fed to pin 20 (16) via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor connected to ground.

Capacitor value = de-emphasis time constant per 1500 (for 50 µs: 33 nF).

From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. –6 dBV) in the output amplifiers.

Secondary channels

Up to eight secondary channel inputs are available at pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42). External ceramic bandpass filters tuned to the required secondary sound carrier frequencies route these signals to the inputs.

For stereo applications the TDA8740; TDA8740H contains two identical secondary sound processing channels. For each channel it is possible to select from four inputs (IN-A, IN-B, IN-C and IN-D) using the input selector (see Logic Table 1). With the input switch several stereo signals or languages can be selected for demodulation. It should be noted that the inputs are identical and can be freely interchanged. Secondary Channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary Channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2'.

From the input selector switch the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled using electrolytic capacitors connected to pins 40 (36) (left) and 42 (38) (right). The output level is set with a 220 Ω resistor connected in series with the capacitor.

High frequency components in the amplified PLL output signal are filtered out in the audio LPF block (4th order Butterworth low-pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The noise reduction can be regarded as an input level-dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (0 dB) the frequency response of the first part (i.e. without the fixed de-emphasis) is virtually flat. As the input level is lowered by x-dB, the higher output frequencies will be reduced an extra x-dB with respect to the lower frequencies (1 : 2 expansion).

The NR output signal is fed to pin 36 (32) (left) and pin 32 (28) (right) via internal resistors.

Fixed de-emphasis is achieved by these resistors and external capacitors connected to ground. The signals are DC decoupled via pins 36/35 (32/31) and 32/33 (28/29) and then routed to the output selectors.

OUTPUT SELECTION

With the output selector (see Table 2) the outputs at pins 25 and 24 (21 and 20) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs at pin 28 and 27 (24 and 23) for IC chaining purposes.

Pin 23 (19) is a separate output which delivers the main channel only, thereby creating the possibility of having three different output channels simultaneously e.g. for use in hi-fi VCRs.

The outputs at pins 25 and 24 (21 and 20) can be muted by setting the MUTE signal at pin 13 (8) to logic 1 (switch positions 6 and 7).

The output at pin 23 (19) can be muted by setting the MUTE signal and the EXT/$\overline{\text{INT}}$ signal at pin 26 (22) both logic 1 (switch position 7).

All outputs at pins 23, 24 and 25 (19, 20 and 21) are line drivers with SCART level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels = –6 dBV typical when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54 × 85 kHz = 46 kHz for the main channel and 0.54 × 50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

LPF = Low-Pass Filter.

NR = Noise Reduction.

PLL = Phase-Locked-Loop

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	note 1	0	13.2	V
V_n	voltage on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	note 2	0	1	V
V_n	voltage on pins 3, 5, 11, 13, 15, 17, 20, 21, 23 to 26, 31, 33, 35, 37, 40, 41, and 42 (6, 8, 10, 13, 16, 17, 19, 20 to 22, 27, 29, 31, 33, 36, 37, 38, 41 and 43)	note 2	0	9	V
V_n	voltage on pins 7, 18, 19, 27 to 30, 32, 36, 38 and 39 (2, 14, 15, 23 to 26, 28, 32, 34 and 35)	note 1	0	V_P	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C

Notes

1. All voltages referenced to ground pins 9 and 34 (4 and 30).
2. All voltages referenced to ground pins 9 and 34 (4 and 30). These voltages must not exceed V_P or maximum value at any time.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	53	K/W
	QFP44	69	K/W

DC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 7.02 MHz; f_{OS2} = 7.20 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	8.0	12	13.2	V
I_P	supply current	–	38	45	mA
P_{tot}	total power dissipation	–	–	600	mW
V_n	voltage on pins 20, 21, 23, 24, 25, 27, 28, 30, 32, 33, 35, 36 and 38 (16, 17, 19, 20, 21, 23, 24, 26, 28, 29, 31, 32 and 34)	–	3.8	–	V
V_{REF}	input reference voltage on pin 19 (15)	3.7	3.8	3.9	V
V_n	voltage on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	–	0	–	V
$V_{CDCL,CDCR}$	voltage on pins 40 and 42 (36 and 38)	–	2.7	–	V
V_{CDCM}	voltage on pin 41 (37)	–	2.8	–	V
I_{IN3}	input current at pin 18 (14)	–	–	1	µA

AC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 7.02 MHz; f_{OS2} = 7.20 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input pin 18 (14) and limiter						
$V_{IN3(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
$V_{IN3(rms)}$	input signal level (RMS value)		–	–	200	mV
R_{IN3}	input resistance		–	15	–	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		–	6.5	–	MHz
		MCS = logic 1	–	10.7	–	MHz
Δf_{OM}	lock range of PLL	note 1	5.5	–	7.5	MHz
		MCS = logic 1; note 1	10.0	–	11.5	MHz
R_{CDM}	output resistance for 50 µs de-emphasis pin 20 (16)		1.24	1.5	1.7	kΩ
V_{CDM}	output voltage pin 20 (16)		−18.5	−16.0	−14.5	dBV
ΔV_{CDM}	spread of PLL output voltage over lock range pin 20 (16)		–	–	±1	dB
R_{CCM}	input resistance of output amplifier pin 21 (17)		95	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{OM,OR,OL}$	output voltage pins 23, 24 and 25 (19, 20 and 21)	all PLLs locked	−9	−6	−4	dBV
UBM	output voltage unbalance pins 23, 24, 25 (19, 20, 21)	output selector in position 4	−0.5	–	+0.5	dB
THD	total harmonic distortion	all PLLs locked	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	–	dB
$\frac{V_{OM\,(15\,kHz)}}{V_{OM\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz pin 23 (19)	no de-emphasis connected	−0.5	0	+0.5	dB
$R_{OM,OR,OL}$	output resistance pins 23, 24 and 25 (19, 20 and 21)		92	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	–	74	–	dB
$MUTE_{att}$	mute attenuation	output selector in position 7	74	–	–	dB
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	35	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - HF inputs pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) and limiters						
$V_{IN1,IN2}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$V_{I(rms)}$	input signal level (RMS value)		–	–	200	mV
R_i	input resistance		260	330	380	Ω
Secondary channels 1 and 2 - PLL FM demodulators (input selector in position 1)						
f_{CCO1}	free running frequency PLL1		–	7.0	–	MHz
f_{CCO2}	free running frequency PLL2		–	7.2	–	MHz
$\Delta f_{OS1/2}$	lock range of PLLs	note 3	6.0	–	8.5	MHz
$R_{S1,S2}$	series resistance for optimum frequency response adjustment		0	0.22	1.0	kΩ
$V_{CDCL,CDCR\ (rms)}$	PLL output voltage pins 40 and 42 (36 and 38) (RMS value)	pins to be left open-circuit	–	7	–	mV
$\Delta V_{CDCL,CDCR}$	spread of PLL output voltage over lock range		–	–	±1	dB
Secondary channels - overall performance of LPF and NR (input and output selectors in position 1)						
R_o	output resistance for 75 µs de-emphasis pins 36 and 32 (32 and 28)		1.9	2.3	2.6	kΩ
R_i	input resistance of output amplifiers pins 35 and 33 (31 and 29)		95	150	200	kΩ
$V_{OL,OR}$	output voltage level pins 25 and 24 (21 and 20)	note 4	–8	–6	–4	dBV
UBS	unbalance voltage outputs pins 25 and 24 (21 and 20)	note 4	–1	–	+1	dBV
THD	total harmonic distortion	note 4	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	–	dB
R_o	output resistance pins 25 and 24 (21 and 20)	note 4	92	125	150	Ω
$MUTE_{att}$	mute attenuation	output selector in position 6; note 4	74	–	–	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	–	74	–	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	–	74	–	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors pins 29, 39 (25, 35)	all PLLs locked; $\Delta f = 0$	14	16	20	mV
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - low-pass filter pins 38 and 30 (34 and 26)						
$\frac{V_{RECTL,\,RECTR\,(50\,kHz)}}{V_{RECTL,\,RECTR\,(1\,kHz)}}$	50 kHz frequency response with respect to 1 kHz	note 7	–25	–16	–9	dB
Secondary channels - noise reduction pins 25 and 24 (21 and 20); note 4						
$V_{OL,OR}$	output voltage at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–1	+1	+3	dBV
$\frac{V_{OL,\,OR\,(15\,kHz)}}{V_{OL,\,OR\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–2	0	+2	dB
$V_{OL,OR}$	output voltage at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–29	–26	–23	dBV
$\frac{V_{OL,\,OR\,(15\,kHz)}}{V_{OL,\,OR\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–13	–11.5	–10	dB
External inputs - pin 28 (24) (left) and pin 27 (23) (right) - overall performance (output selector in position 5)						
$V_{EXTR,EXTL}$	input signal level		–	–	6	dBV
R_i	input resistance		95	150	200	kΩ
$V_{OL,OR}$	output level pins 25 and 24 (21 and 20)	$V_{EXTR,\,EXTL} = -6$ dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{EXTR,\,EXTL} = -6$ dBV; $f_i = 1$ kHz	–	–	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{EXTR,\,EXTL} = -6$ dBV	80	–	–	dB
$\alpha_{L/R}, \alpha_{R/L}$	crosstalk	$f_i = 1$ kHz	–	80	–	dB
Input selector control circuit pins 3 and 5 (41 and 43) (see also Table 1) and secondary channels PLLs disable [SCD pin 11 (6)]; pins 3, 5 and 11 (41, 43 and 6) left open-circuit = logic HIGH						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		3.5	–	9	V
R_i	input resistance	connected to V_P	65	100	130	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output selector control circuit (see also Table 2) and main channel PLL lock-in select [MCS pin 7 (2)]; pins 15, 17, 26 and 13 (10, 13, 22 and 8) are MOS inputs and should not be left open-circuit						
V_{IL}	LOW level input voltage limits		0	–	1.2	V
V_{IM}	MID level input voltage limits for MCS pin only		1.8	–	2.8	V
V_{IMF}	MID level input voltage on MCS pin if MCS pin is floating	V_P must be 10.8 to 13.2 V	17	19	21	$\%V_P$
V_{IH}	HIGH level input voltage limits		3.5	–	V_P	V
R_{IL}	low input resistance MCS pin to ground		12	19	26	kΩ
R_{IH}	high input resistance MCS pin to V_P		52	80	108	kΩ
I_{IL}	LOW level input current (not MCS pin)	V_{IL} = 0 V	–	<–1	–	μA
I_{IH}	HIGH level input current (not MCS pin)	V_{IH} = 5 V	–	<1	–	μA

Notes

1. At pin 20 (16) the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (–16 dBV), and THD of maximum 0.5%; V_P = 8 to 13.2 V; T_{amb} = –20 to +70 °C.
2. Modulation of main channel is OFF; modulation of secondary channels is ON.
3. The electrolytic capacitors at pins 40 and 42 (36 and 38) are removed and 1500 pF capacitors between pin 40 (36) and ground and between pin 42 (38) and ground are connected. At pins 40 and 42 (36 and 38) the demodulated 1 kHz signals should be present with typical levels of 7 mV (RMS) and THD of maximum 0.5%; V_P = 8 to 13.2 V; T_{amb} = –20 to +70 °C.
4. All PLLs locked; $R_{S1} = R_{S2}$ = 220 kΩ.
5. Modulation of secondary channel being measured and main channel is OFF; modulation of other secondary channel is ON.
6. Modulation of main channel is ON; modulation of secondary channels is OFF.
7. Measured at pins 38 (34) (left) and 30 (26) (right) and no electrolytic capacitors connected to these pins.

Table 1 Truth table for input selection.

SWITCH POSITION	STATE	PIN 15 (10)	PIN 17 (13)
1	pins 2 and 10 (IN-A) (40 and 5)	0	0
2	pins 4 and 12 (IN-B) (42 and 7)	0	1
3	pins 6 and 14 (IN-C) (1 and 9)	1	0
4	pins 8 and 16 (N-D) (3 and 12)	1	1

Table 2 Truth table for output selection (note 1).

SWITCH POSITION	STATE	PIN 15 (10)	PIN 17 (13)	PIN 26 (22)	PIN 13 (8)
		OUTSEL L	OUTSEL R	EXT/$\overline{\text{INT}}$	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

Note

1. X = don't care.

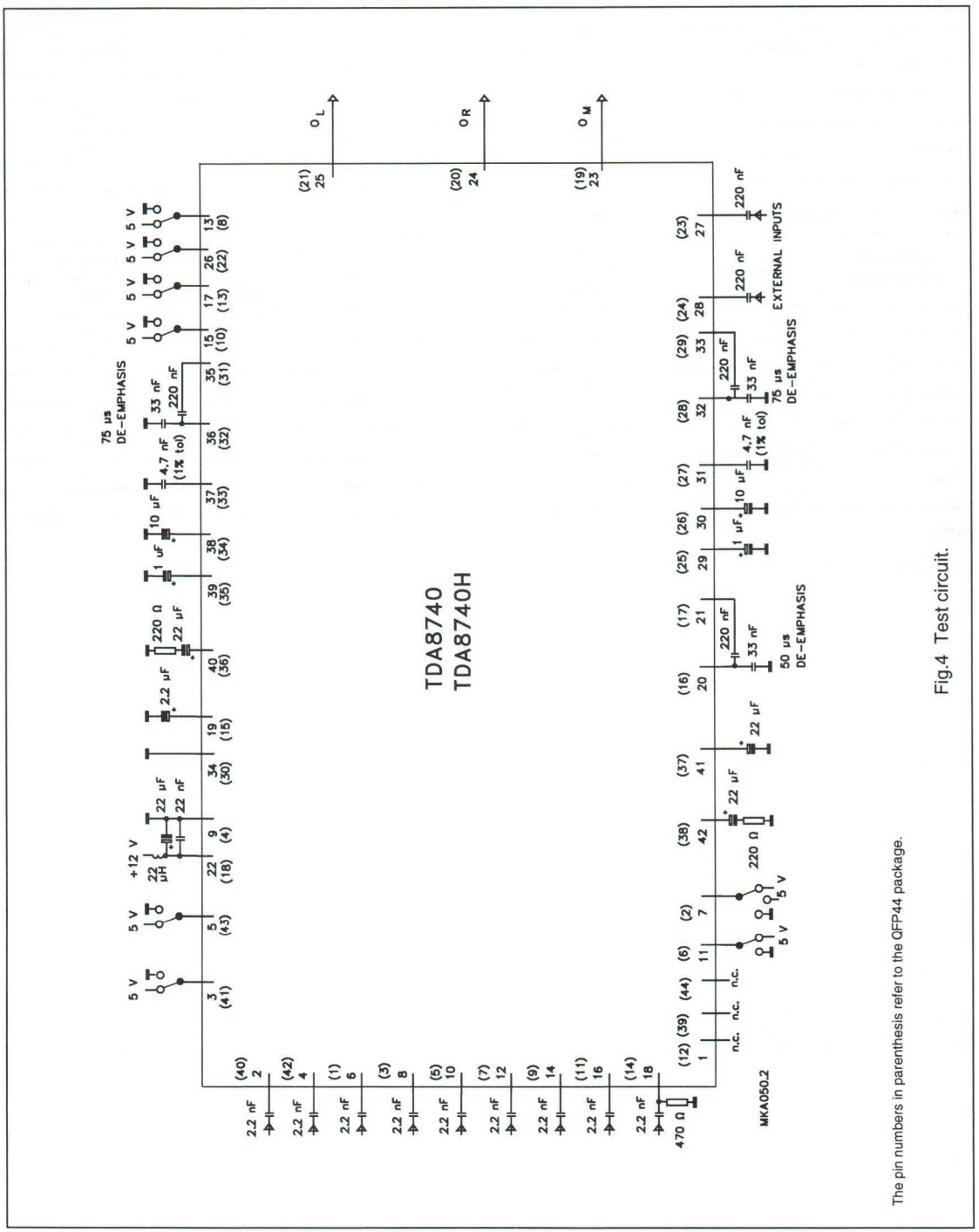


Fig.4 Test circuit.

APPLICATION INFORMATION

MCS pin 7 (2) = logic 0; (see Fig.5)

The lock-in range of the main channel PLL is 5.5 to 7.5 MHz. The satellite baseband signal is routed to nine bandpass filters, eight for the secondary channels and one for the main channel. For the secondary channels the bandpass filter terminating resistors are integrated on-chip (330 Ω typically) so no external resistors are required. For the main channel this is not the case therefore filters with different characteristics can be used.

MCS pin 7 (2) = logic 1; (see Fig.6)

The lock-in range of the main channel PLL is now 10.0 to 11.5 MHz. The carrier frequency for the main channel is transposed to 10.7 MHz by an external frequency synthesizer and mixer; e.g., if a 6.65 MHz carrier is to be demodulated this frequency is mixed to 10.7 MHz by tuning the frequency synthesizer to 17.35 MHz. If the synthesizer is tuned 17.20 MHz a 6.5 MHz carrier can be demodulated. In this event the audio output level should be adjusted to –6 dBV by inserting a 470 Ω resistor in series with the electrolytic capacitor to pin 41 (37).

MCS pin 7 (2) = MID position

The main channel PLL is off if the voltage is between 1.8 and 2.8 V on pin 7 (2). This situation can be obtained by a floating MCS pin if V_P is between 10.8 and 13.2 V or by forcing this MCS pin to the desired voltage by an external voltage source. In that event V_P can be in the full range of 8 to 13.2 V. This feature can be used to slightly improve the signal-to-noise ratio of the secondary channels if the main channel is not used.

For the main channel the baseband signal is routed to the mixer, and to eight ceramic bandpass filters for the secondary channels. For high-end applications the input level of the NR can be adjusted to give optimal performance. 0 dB is the maximum input level which corresponds to the maximum frequency deviation of the incoming FM signal (50 kHz for secondary channels). If the NR input signal is too low (HIGH) the NR will attenuate (favour) the higher audio frequencies too much due to the expansion character. In general a 1 dB error in the NR input level will give a 1 dB difference between LOW (50 Hz) and HIGH (15 kHz) audio frequencies. With R_{S1} (R_{S2}) the input level and so the frequency response of the NR can be adjusted: at 0 dB input level (which corresponds to a frequency deviation of 50 kHz) the output level of a 15 kHz modulated signal should be 0.25 dB lower than that of a 50 Hz modulated signal.

If the main channel only is to be demodulated the PLLs of the secondary channels can be disabled by setting SCD pin 11 (6) to logic 1.

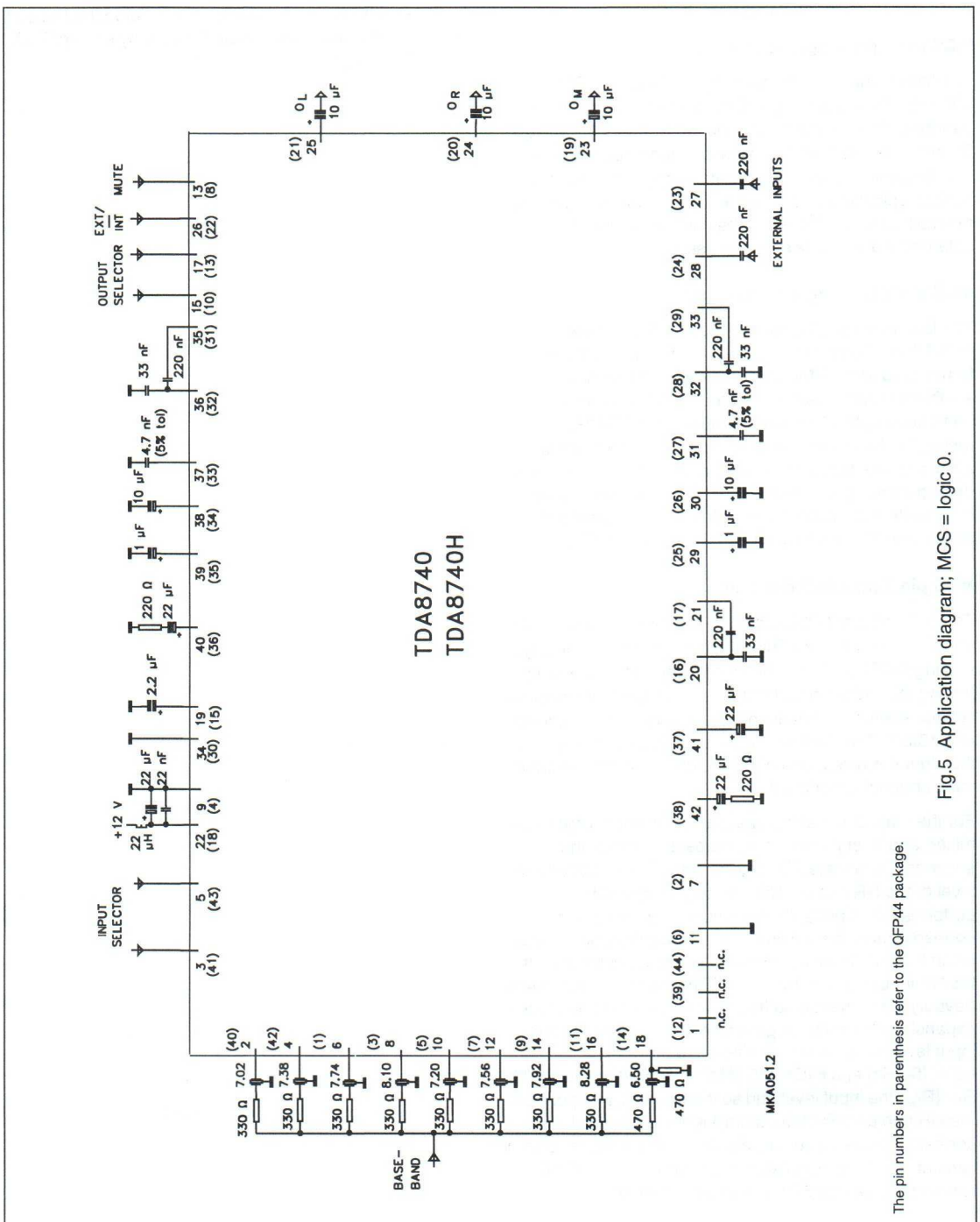


Fig.5 Application diagram; MCS = logic 0.

The pin numbers in parenthesis refer to the QFP44 package.

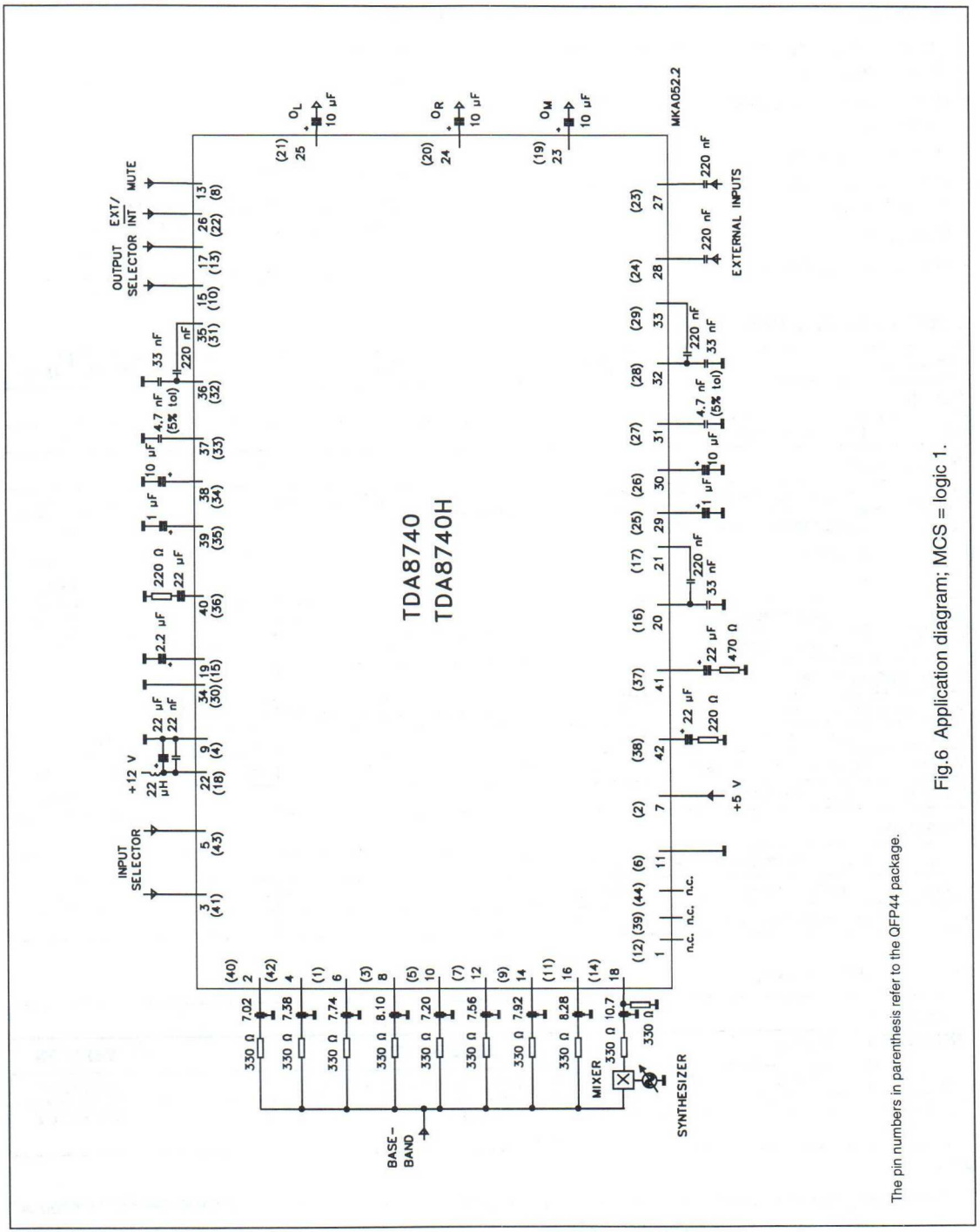


Fig.6 Application diagram; MCS = logic 1.

The pin numbers in parenthesis refer to the QFP44 package.

Satellite sound circuit with noise reduction TDA8741; TDA8741H

FEATURES

- Demodulation of main audio signal using wide band PLL (lock range selectable)
- Demodulation of secondary audio signals using wide band PLL
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio and external
- Mute control
- Line outputs (SCART level).

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8741; TDA8741H is a multi-function sound IC for use in satellite receivers, television sets and video recorders. The pin numbers given in parenthesis throughout this document refer to the QFP44 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8	12	13.2	V
Main channel						
$V_{IN3(rms)}$	input sensitivity pin 18 (14) (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator					
	either		5.5	–	7.5	MHz
	or		10.0	–	11.5	MHz
V_{OM}	output voltage pin 23 (19)		–9	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	–	dB
Secondary channels						
$V_{IN1,IN2(rms)}$	input sensitivity pins 8 and 16 (3 and 11) (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$\Delta f_{OS1,2}$	lock range PLL demodulators		10.0	–	11.5	MHz
$V_{OR,OL}$	output voltage pins 24 and 25 (20 and 21)		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	–	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		–	74	–	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		–	74	–	dB
$\alpha_{S/S}$	crosstalk between secondary channels		–	74	–	dB

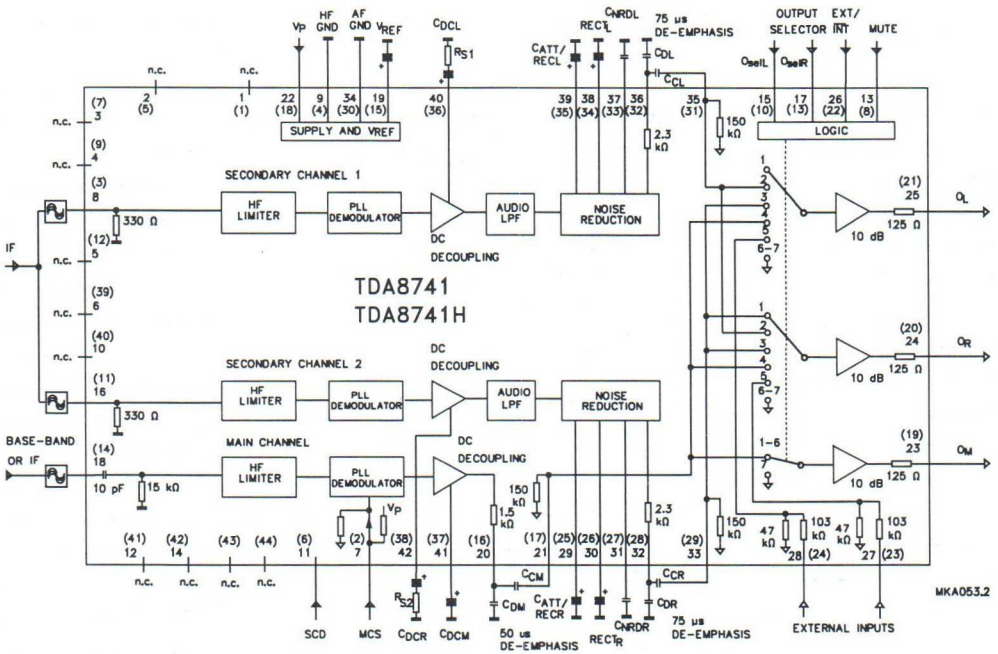
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8741	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8741H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM



The pin numbers in parenthesis refer to the QFP44 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
n.c.	1	1	not connected
n.c.	2	5	not connected
n.c.	3	7	not connected
n.c.	4	9	not connected
n.c.	5	12	not connected
n.c.	6	39	not connected
MCS	7	2	main channel PLL lock-in range select/disable
IN-1	8	3	intercarrier input for secondary Channel 1 (left)
HFGND	9	4	ground for HF section
n.c.	10	40	not connected
SCD	11	6	secondary channels PLLs disable
n.c.	12	41	not connected
MUTE	13	8	mute switch
n.c.	14	42	not connected
$O_{sel\,L}$	15	10	output select switch bit 1 (left)
IN-2	16	11	intercarrier input for secondary Channel 2 (right)
$O_{sel\,R}$	17	13	output select switch bit 2 (right)
IN-3	18	14	intercarrier input for main channel
V_{REF}	19	15	decoupling capacitor for reference voltage
$C_{D\,M}$	20	16	de-emphasis capacitor for main channel
$C_{C\,M}$	21	17	audio pass-through capacitor input for main channel
V_P	22	18	positive supply voltage
O_M	23	19	main channel output
O_R	24	20	right channel output
O_L	25	21	left channel output
EXT/$\overline{INT}$	26	22	output switch bit 3 (external/internal)
EXT_R	27	23	external audio input (right)
EXT_L	28	24	external audio input (left)
$C_{ATT/REC\,R}$	29	25	attack/recovery capacitor (right)
$RECT_R$	30	26	rectifier DC decoupling (right)
$C_{NR\,D\,R}$	31	27	noise reduction de-emphasis capacitor (right)
$C_{D\,R}$	32	28	fixed de-emphasis capacitor (right)
$C_{C\,R}$	33	29	audio pass-through capacitor input for right channel
AFGND	34	30	ground for AF section
$C_{C\,L}$	35	31	audio pass-through capacitor input for left channel
$C_{D\,L}$	36	32	fixed de-emphasis capacitor (left)
$C_{NR\,D\,L}$	37	33	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	34	rectifier DC decoupling (left)
$C_{ATT/REC\,L}$	39	35	attack/recovery capacitor (left)

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
$C_{DC\,L}$	40	36	DC decoupling capacitor (left)
$C_{DC\,M}$	41	37	DC decoupling capacitor (main)
$C_{DC\,R}$	42	38	DC decoupling capacitor (right)
n.c.	–	43	not connected
n.c.	–	44	not connected

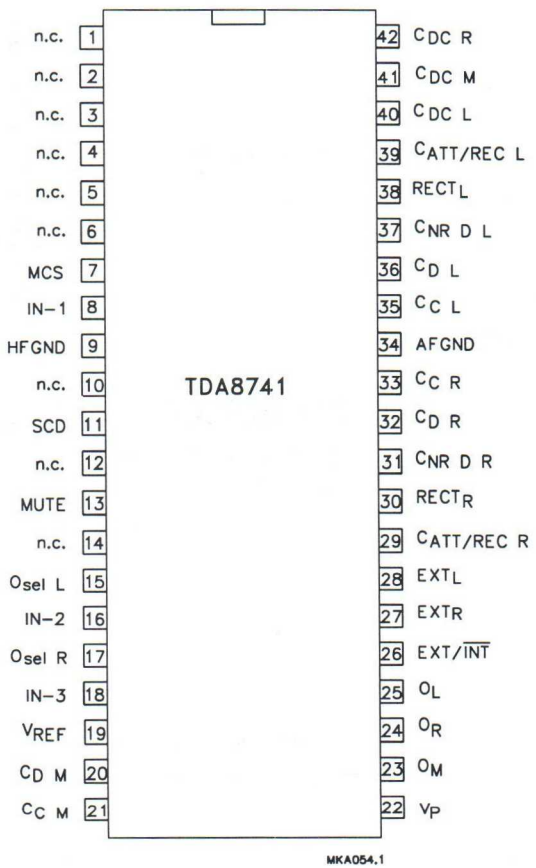


Fig.2 Pin configuration (SDIP42).

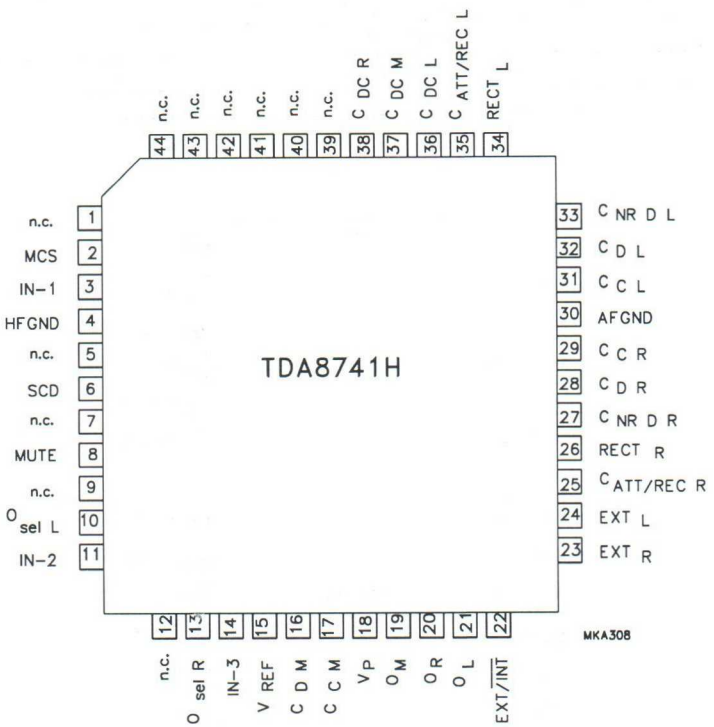


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner contains the demodulated video signal plus a number of sound carriers to facilitate reception of a PAL/NTSC/SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the single channel sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present which can be used for stereo or multi-language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz. For accurate tuning to the many sound carriers an external frequency synthesizer and mixer is used to transpose the sound carriers to intermediate frequencies of 10.7 and 10.52 MHz.

The TDA8741; H contains all circuitry for processing the main channel and for two secondary channels, from IF signal to line (SCART) output drivers. The desired frequencies can be routed to the TDA8741; H via bandpass filters.

Main channel (see Fig.1)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz, PLL off and 10.0 to 11.5 MHz using the MCS signal at pin 7 (2) [when pin 7 (2) is at logic 0, being a voltage from 0 to 1.2 V, the lock-in range = 5.5 to 7.5 MHz; when pin 7 (2) is at logic 1, being a voltage from 3.5 V until V_P, the lock-in range = 10.0 to 11.5 MHz; when pin 7 (2) is in the mid voltage position, being a voltage from 1.8 to 2.8 V, the main channel PLL is switched off]. The voltage is then determined by the resistor divider at this pin between V_P and ground.

If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 (14) via a 6.5 MHz ceramic bandpass filter. Alternatively, if there is a requirement to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In this event the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 (14) via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment-free. High gain and DC error signals from the PLL, which are superimposed on the demodulator output, require DC decoupling. A buffer amplifier is used to amplify the signal to the same level as the secondary channels and decouples DC using an electrolytic capacitor connected to pin 41 (37). The demodulator output signal is fed to pin 20 (16) via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor connected to ground.

Capacitor value = de-emphasis time constant per 1500 (for 50 μs: 33 nF).

From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. –6 dBV) in the output amplifiers.

Secondary channels

An external mixer and oscillator frequency synthesizer transfers the secondary sound carriers to fixed intermediate frequencies e.g. 10.7 and 10.52 MHz. Two secondary channel inputs are available at pins 8 and 16 (3 and 11). The signals are routed to the inputs via external ceramic bandpass filters which are tuned to the required intermediate frequencies.

For stereo applications the TDA8741; TDA8741H contains two identical secondary sound processing channels. Secondary Channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary Channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2'.

From the inputs the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled using electrolytic capacitors connected to pins 40 (36) (left) and 42 (38) (right). The output level is set with a resistor connected in series with the capacitor.

High frequency components in the amplified PLL output signal are filtered out in the audio LPF block (4th order Butterworth low-pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The noise reduction can be regarded as an input level-dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (0 dB) the frequency response of the first part (i.e. without the fixed de-emphasis) is virtually flat. As the input level is lowered by x-dB, the higher output frequencies will be reduced an extra x-dB with respect to the lower frequencies (1 : 2 expansion).

The NR output signal is fed to pin 36 (32) (left) and pin 32 (28) (right) via an internal resistor.

Fixed de-emphasis is achieved by these resistors and external capacitors connected to ground. The signals are DC decoupled via pins 36/35 (32/31) and 32/33 (28/29) and then routed to the output selectors.

OUTPUT SELECTION

With the output selector (see Table 1) the outputs at pins 25 and 24 (21 and 20) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs at pin 28 and 27 (24 and 23) for IC chaining purposes.

Pin 23 (19) is a separate output which delivers the main channel only, thereby creating the possibility of having three different output channels simultaneously e.g. for use in hi-fi VCRs.

The outputs at pins 25 and 24 (21 and 20) can be muted by setting the MUTE signal at pin 13 (8) to logic 1 (switch positions 6 and 7).

The output at pin 23 (19) can be muted by setting the MUTE signal and the EXT/INT signal at pin 26 (22) both logic 1 (switch position 7).

All outputs at pins 23, 24 and 25 (19, 20 and 21) are line drivers with SCART level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels = −6 dBV typical when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54 × 85 kHz = 46 kHz for the main channel and 0.54 × 50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

LPF = Low-Pass Filter.

NR = Noise Reduction.

PLL = Phase-Locked-Loop.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	note 1	0	13.2	V
V_I	input voltage level on pins 8 and 16 (3 and 11)	note 2	0	1	V
V_n	voltage on pins 11, 13, 15, 17, 20, 21, 23 to 26, 31, 33, 35, 37, 40, 41, and 42 (6, 8, 10, 13, 16, 17, 19, 20 to 22, 27, 29, 31, 33, 36, 37 and 38)	note 2	0	9	V
V_n	voltage on pins 7, 18, 19, 27 to 30, 32, 36, 38 and 39 (2, 14, 15, 23 to 26, 28, 32, 34 and 35)	note 1	0	V_P	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C

Notes

1. All voltages referenced to ground pins 9 and 34 (4 and 30).
2. All voltages referenced to ground pins 9 and 34 (4 and 30). These voltages must not exceed V_P or maximum value at any time.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	53	K/W
	QFP44	69	K/W

DC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 10.7 MHz; f_{OS2} = 10.52 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at pins 8 and 16 (3 and 11): 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	8.0	12	13.2	V
I_P	supply current	–	38	45	mA
P_{tot}	total power dissipation	–	–	600	mW
V_n	voltage on pins 20, 21, 23, 24, 25, 27, 28, 30, 32, 33, 35, 36 and 38 (16, 17, 19, 20, 21, 23, 24, 26, 28, 29, 31, 32 and 34)	–	3.8	–	V
V_{REF}	input reference voltage on pin 19 (15)	3.7	3.8	3.9	V
$V_{IN1,IN2}$	voltage on pins 8 and 16 (3 and 11)	–	0	–	V
$V_{CDCL,CDCR}$	voltage on pins 40 and 42 (36 and 38)	–	3.0	–	V
V_{CDCM}	voltage on pin 41 (37)	–	2.8	–	V
I_{IN3}	input current at pin 18 (14)	–	–	1	µA

AC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 10.7 MHz; f_{OS2} = 10.52 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at pins 8 and 16 (3 and 11): 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input pin 18 (14) and limiter						
$V_{IN3(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
$V_{IN3(rms)}$	input signal level (RMS value)		–	–	200	mV
R_{IN3}	input resistance		–	15	–	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		–	6.5	–	MHz
		MCS = logic 1	–	10.7	–	MHz
Δf_{OM}	lock range of PLL	note 1	5.5	–	7.5	MHz
		MCS = logic 1; note 1	10.0	–	11.5	MHz
R_{CDM}	output resistance for 50 µs de-emphasis pin 20 (16)		1.24	1.5	1.7	kΩ
V_{CDM}	output voltage pin 20 (16)		−18.5	−16.0	−14.5	dBV
ΔV_{CDM}	spread of PLL output voltage over lock range pin 20 (16)		–	–	±1	dB
R_{CCM}	input resistance of output amplifier pin 21 (17)		95	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{OM,OR,OL}$	output voltage pins 23, 24 and 25 (19, 20 and 21)	all PLLs locked	−9	−6	−4	dBV
THD	total harmonic distortion	all PLLs locked	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	–	dB
$\frac{V_{OM\,(15\,kHz)}}{V_{OM\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz pin 23 (19)	no de-emphasis connected	−0.5	0	+0.5	dB
$R_{OM,OR,OL}$	output resistance pins 23, 24 and 25 (19, 20 and 21)		92	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	–	74	–	dB
$MUTE_{att}$	mute attenuation	output selector in position 7	74	–	–	dB
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	35	–	dB
Secondary channels 1 and 2 - HF inputs pins 8 and 16 (3 and 11) and limiters						
$V_{IN1,IN2(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$V_{i(rms)}$	input signal level (RMS value)		–	–	200	mV
$R_{IN1,IN2}$	input resistance		280	330	380	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - PLL FM demodulators						
f_{CCO1}	free running frequency PLL1		–	10.7	–	MHz
f_{CCO2}	free running frequency PLL2		–	10.52	–	MHz
$\Delta f_{OS1/2}$	lock range of PLLs	note 3	10	–	11.5	MHz
$R_{S1,S2}$	series resistance for optimum frequency response adjustment		0	0.68	2.2	kΩ
$V_{CDCL,CDCR(rms)}$	PLL output voltage pins 40 and 42 (36 and 38) (RMS value)	pins to be left open-circuit	–	9	–	mV
$\Delta V_{CDCL,CDCR}$	spread of PLL output voltage over lock range		–	–	±1	dB
Secondary channels - overall performance of LPF and NR (output selectors in position 1)						
R_O	output resistance for 75 µs de-emphasis pins 36 and 32 (32 and 28)		1.9	2.3	2.6	kΩ
R_i	input resistance of output amplifiers pins 35 and 33 (31 and 29)		95	150	200	kΩ
$V_{OL,OR}$	output voltage level pins 25 and 24 (21 and 20)	note 4	–8	–6	–4	dBV
UBS	unbalance voltage outputs pins 25 and 24 (21 and 20)	note 4	–1	–	+1	dB
THD	total harmonic distortion	note 4	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	–	dB
R_o	output resistance pins 25 and 24 (21 and 20)	note 4	92	125	150	Ω
$MUTE_{att}$	mute attenuation	output selector in position 6; note 4	74	–	–	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	–	74	–	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	–	74	–	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors pins 29, 39 (25, 35)	all PLLs locked; $\Delta f = 0$	14	16	20	mV
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	25	–	dB
Secondary channels - low-pass filter pins 38 and 30 (34 and 26)						
$\frac{V_{RECTL,RECTR(50\ kHz)}}{V_{RECTL,RECTR(1\ kHz)}}$	50 kHz frequency response with respect to 1 kHz	note 7	–25	–16	–9	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - noise reduction pins 25 and 24 (21 and 20); note 4						
$V_{OL,OR}$	output voltage at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–1	+1	+3	dBV
$\frac{V_{OL,OR\,(15\,kHz)}}{V_{OL,OR\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–2	0	+2	dB
$V_{OL,OR}$	output voltage at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–29	–26	–23	dBV
$\frac{V_{OL,OR\,(15\,kHz)}}{V_{OL,OR\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–13	–11.5	–10	dB
External inputs - pin 28 (24) (left) and pin 27 (23) (right) - overall performance (output selector in position 5)						
$V_{EXTR,EXTL}$	input signal level		–	–	6	dBV
R_i	input resistance		95	150	200	kΩ
$V_{OL,OR}$	output level	$V_{EXTR,\,EXTL} = -6$ dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{EXTR,\,EXTL} = -6$ dBV; $f_i = 1$ kHz	–	–	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{EXTR,\,EXTL} = -6$ dBV	80	–	–	dB
$\alpha_{L/R}, \alpha_{R/L}$	crosstalk	$f_i = 1$ kHz	–	80	–	dB
Secondary channels PLLs disable [SCD pin 11 (6)]; pin 11 (6) left open-circuit = logic HIGH						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		3.5	–	9	V
R_i	input resistance	connected to V_P	65	100	130	kΩ
Output selector control circuit (see also Table 1) and main channel PLL lock-in select [MCS pin 7 (2)]; pins 15, 17, 26, 13 and 7 (10, 13, 22, 8 and 2) MOS inputs and should not be left open-circuit						
V_{IL}	LOW level input voltage limits		0	–	1.2	V
V_{IM}	MID level input voltage limits for MCS pin only		1.8	–	2.8	V
V_{IMF}	MID level input voltage on MCS pin if MCS pin is floating	V_P must be 1.8 to 13.2 V	17	19	21	$\%V_P$
V_{IH}	HIGH level input voltage limits		3.5	–	V_P	V
R_{IL}	low input resistance MCS pin to ground		12	19	26	kΩ
R_{IH}	high input resistance MCS pin to V_P		52	80	108	kΩ
I_{IL}	LOW level input current (not MCS pin)	$V_{IL} = 0$ V	–	<–1	–	μA
I_{IH}	HIGH level input current (not MCS pin)	$V_{IH} = 5$ V	–	<1	–	μA

Notes to the AC characteristics

1. At pin 20 (16) the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (−16 dBV), and THD of maximum 0.5%; V_P = 8 to 13.2 V; T_{amb} = −20 to +70 °C.
2. Modulation of main channel is OFF; modulation of secondary channels is ON.
3. The electrolytic capacitors at pins 40 and 42 (36 and 38) are removed and 1500 pF capacitors between pin 40 (36) and ground and between pin 42 (38) and ground are connected. At pins 40 and 42 (36 and 38) the demodulated 1 kHz signals should be present with typical levels of 9 mV (RMS) and THD of maximum 0.5%; V_P = 8 to 3.2 V; T_{amb} = −20 to +70 °C.
4. All PLLs locked; $R_{S1} = R_{S2} = 0.68\ k\Omega$.
5. Modulation of secondary channel being measured and main channel is OFF; modulation of other secondary channel is ON.
6. Modulation of main channel is ON; modulation of secondary channels is OFF.
7. Measured at pins 38 (34) (left) and 30 (26) (right) and no electrolytic capacitors connected to these pins.

Table 1 Truth table for output selection (note 1)

SWITCH POSITION	STATE	PIN 15 (10)	PIN 17 (13)	PIN 26 (22)	PIN 13 (8)
		OUTSEL L	OUTSEL R	EXT/$\overline{\text{INT}}$	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

Note

1. X = don't care.

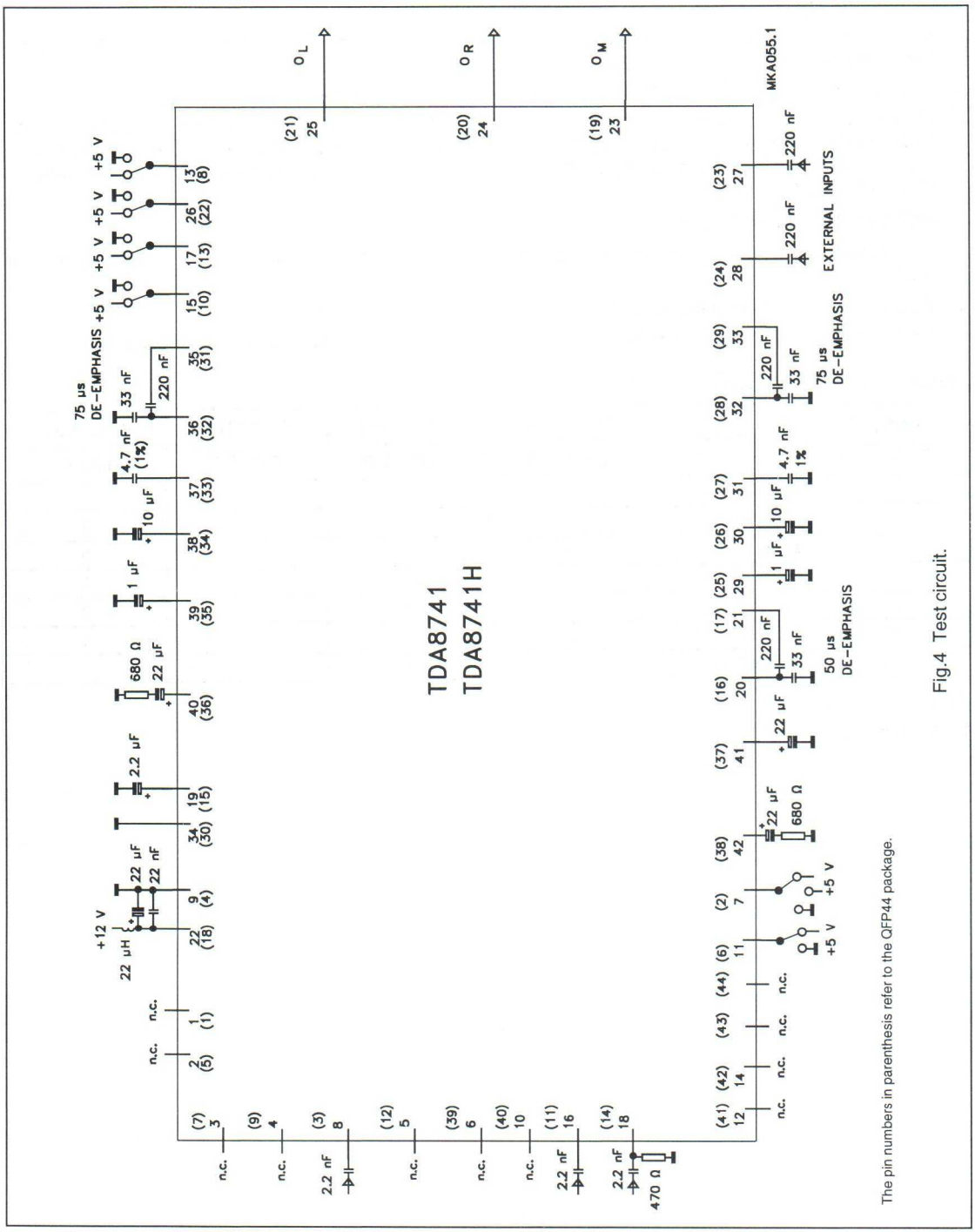


Fig.4 Test circuit.

The pin numbers in parenthesis refer to the QFP44 package.

APPLICATION INFORMATION

General

The satellite baseband signal is routed to a mixer to transfer the various secondary channels to fixed intermediate frequencies of 10.7 and 10.52 MHz. Tuning to the required carrier frequencies can be achieved by varying the oscillator frequency e.g. tuning to 7.02 and 7.20 MHz carrier frequencies requires an oscillator frequency of 17.72 MHz and tuning to 7.38 and 7.56 MHz requires an oscillator frequency of 18.08 MHz. The IF signals are routed to the inputs pin 8 and 16 (3 and 11) via 10.7 and 10.52 MHz ceramic bandpass filters. For the secondary channels the bandpass filter terminating resistor is integrated on-chip (330 Ω typical) thus no external resistors are required.

MCS pin 7 (2) = logic 0; (see Fig.5)

The lock-in range of the main channel PLL is 5.5 to 7.5 MHz. For the main channel a ceramic bandpass filter (e.g. 6.5 MHz) is used to filter out the main sound carrier directly from the baseband signal. Simultaneous demodulation of one main channel and various secondary channels is now possible with a minimum of external components. As no bandpass filter terminating resistor for the main channel pin 18 (14) is integrated on-chip, an external resistor is required.

MCS pin 7 (2) = logic 1; (see Fig.6)

The lock-in range of the main channel PLL is now 10.0 to 11.5 MHz. The carrier frequency of the main channel is also transferred to a fixed intermediate frequency. In this event the main audio output level should be adjusted to −6 dBV by inserting a 470 Ω resistor in series with the electrolytic capacitor on pin 41 (37).

MCS pin 7 (2) = MID position

The main channel PLL is off if the voltage is between 1.8 and 2.8 V on pin 7 (2). This situation can be obtained by a floating MCS pin if V_P is between 10.8 and 13.2 V or by forcing this MCS pin to the desired voltage by an external voltage source. In that event V_P can be in the full range of 8 to 13.2 V. This feature can be used to slightly improve the signal-to-noise ratio of the secondary channels if the main channel is not used.

If simultaneous demodulation of main- and secondary sound carriers is not required, a low cost solution as given in Fig.6 can be considered. One mixer and frequency synthesizer are used to transfer all sound carriers to intermediate frequencies of 10.7 and 10.52 MHz. When the bandwidth of the main channel is larger than the secondary channel bandwidth, a separate (e.g. 10.7 MHz) ceramic filter plus resistors are required for the main channel.

The secondary sound carriers can be demodulated as described above. If e.g. a 6.65 MHz main sound carrier is to be demodulated, this frequency is mixed to 10.7 MHz by tuning the frequency synthesizer to 17.35 MHz. If the synthesizer is tuned to 17.20 MHz a 6.5 MHz main sound carrier can be demodulated. When main sound is to be demodulated and this IF signal is also available on the secondary Channel 1 input the PLLs of the secondary channels can be disabled by making SCD pin 11 (6) HIGH. The output selector should be in position 4 (main sound on all outputs) if output pins 25 and 24 (21 and 20) are used.

For high-end applications the input level of the NR can be adjusted to give optimum performance. 0 dB is the maximum input level which corresponds to the maximum frequency deviation of the incoming FM signal (50 kHz for secondary channels). If the NR input signal is too low (HIGH) the NR will attenuate (favour) the higher audio frequencies too much due to the expansion character. In general: 1 dB error in NR input level will give a 1 dB difference between low (50 Hz) and high (15 kHz) audio frequencies. With R_{S1} (R_{S2}) the input level and so the frequency response of the NR can be adjusted: at **0 dB input level** (which corresponds to a frequency deviation of 50 kHz) the output level of a 15 kHz modulated signal should be 0.25 dB lower than that of an 50 Hz modulated signal.

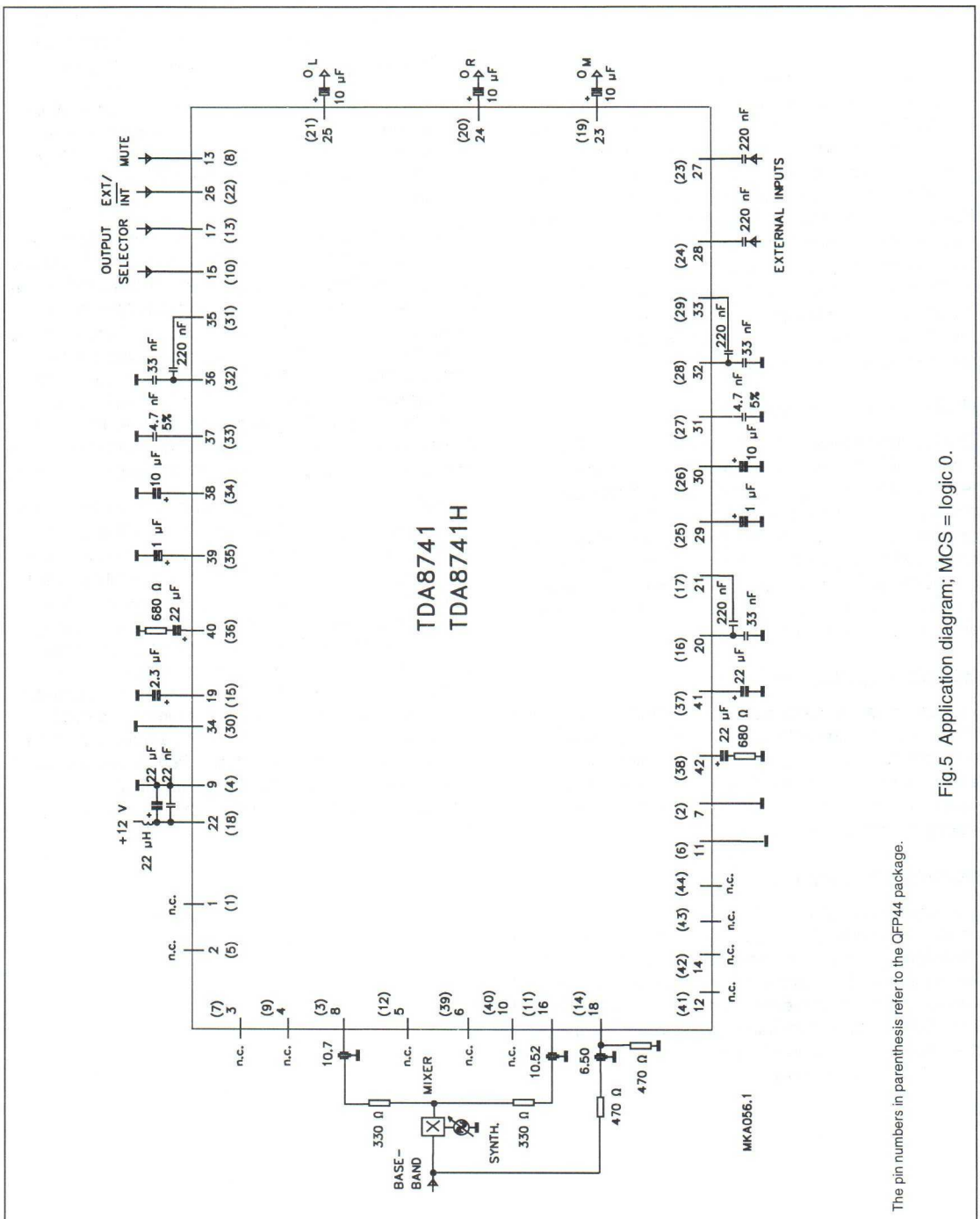


Fig.5 Application diagram; MCS = logic 0.

The pin numbers in parenthesis refer to the QFP44 package.

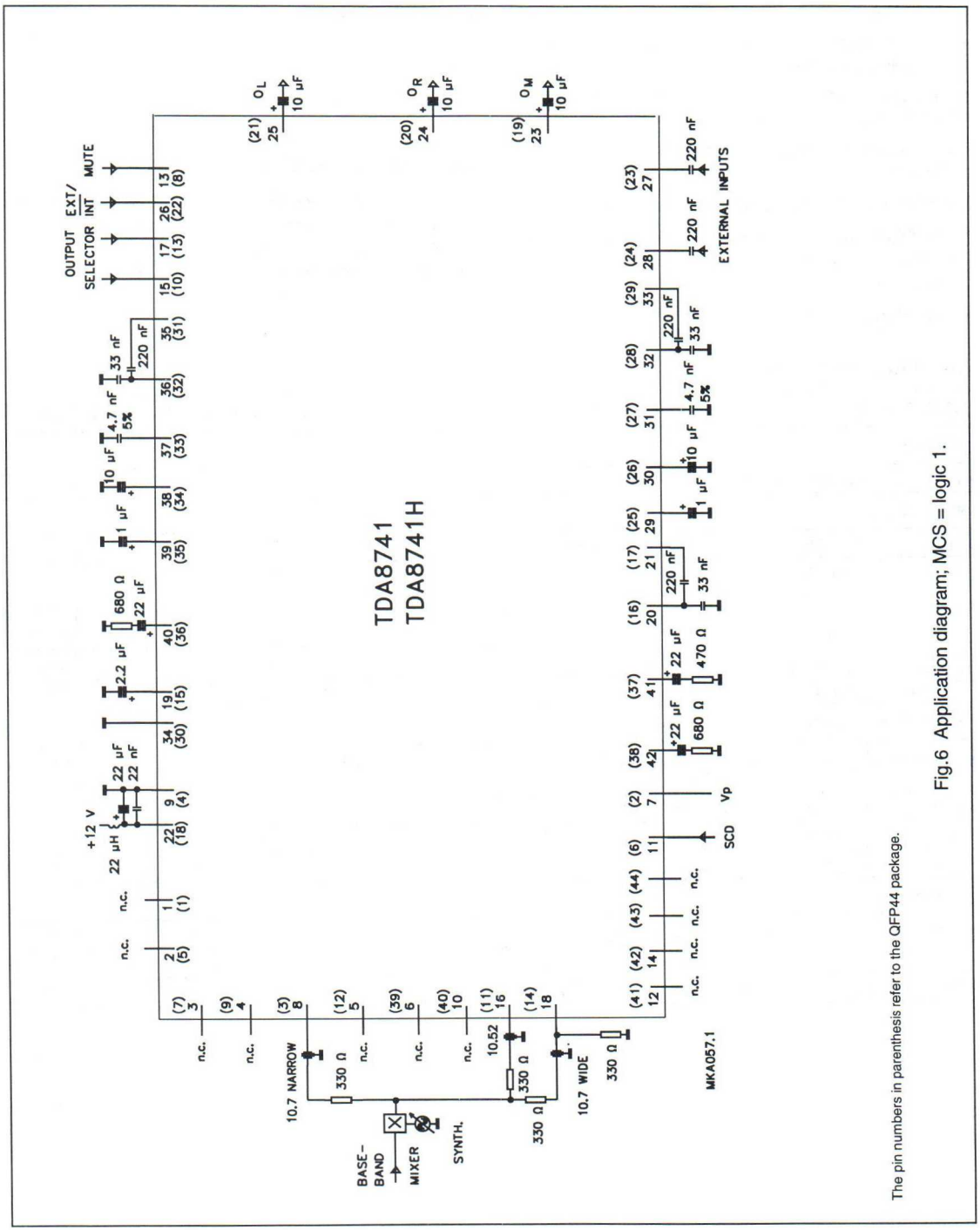


Fig.6 Application diagram; MCS = logic 1.

The pin numbers in parenthesis refer to the QFP44 package.

Satellite sound circuit with noise reduction TDA8742; TDA8742H

FEATURES

- Demodulation of main audio signal using wide band PLL (lock range selectable)
- HF input selection: two-out-of-eight secondary audio signals can be selected
- Demodulation of secondary audio signals using wide band PLL
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio and external
- Mute control
- Line outputs (SCART level).

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8742; TDA8742H is a multi-function sound IC for use in satellite receivers, television sets and video recorders. The pin numbers given in parenthesis throughout this document refer to the QFP44 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8	12	13.2	V
Main channel						
$V_{IN3(rms)}$	input sensitivity pin 18 (14) (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator					
	either		5.5	–	7.5	MHz
	or		10.0	–	11.5	MHz
V_{OM}	output voltage pin 23 (19)		–9	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	–	dB
Secondary channels						
$V_{IN1,IN2(rms)}$	input sensitivity pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$\Delta f_{OS1,2}$	lock range PLL demodulators		10.0	–	11.5	MHz
$V_{OR,OL}$	output voltage pins 24 and 25 (20 and 21)		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	–	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		–	74	–	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		–	74	–	dB
$\alpha_{S/S}$	crosstalk between secondary channels		–	74	–	dB

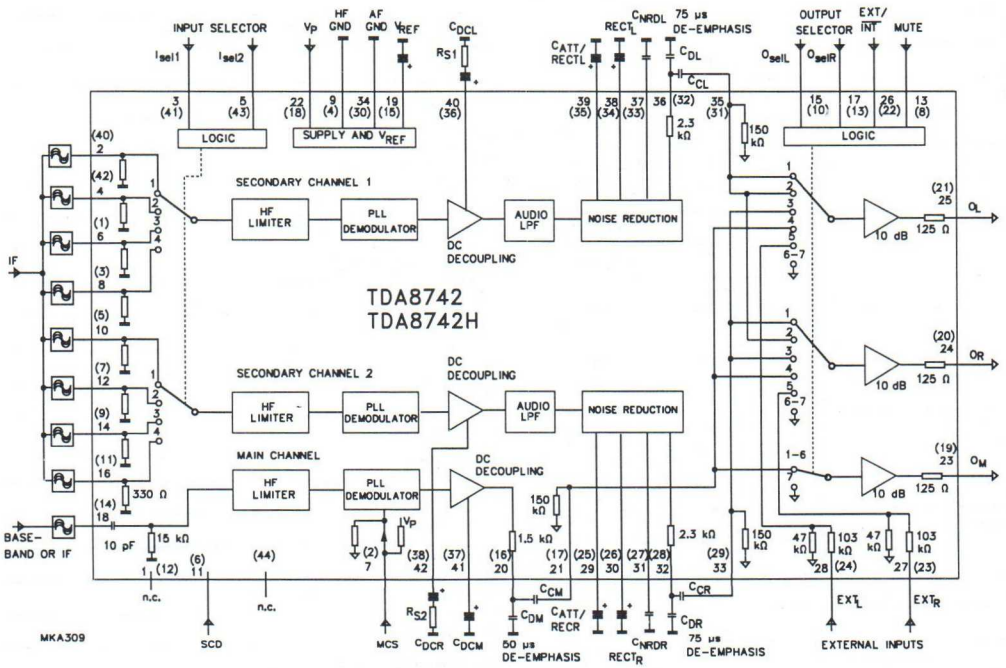
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8742	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8742H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM



The pin numbers in parenthesis refer to the QFP44 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
n.c.	1	39	not connected
IN-1A	2	40	intercarrier input A for Channel 1 (left)
$I_{sel\ 1}$	3	41	input select switch bit 1
IN-1B	4	42	intercarrier input B for Channel 1 (left)
$I_{sel\ 2}$	5	43	input select switch bit 2
IN-1C	6	1	intercarrier input C for Channel 1 (left)
MCS	7	2	main channel PLL lock-in range select/disable
IN-1D	8	3	intercarrier input D for Channel 1 (left)
HFGND	9	4	ground for HF section
IN-2A	10	5	intercarrier input A for Channel 2 (right)
SCD	11	6	secondary channels PLLs disable
IN-2B	12	7	intercarrier input B for Channel 2 (right)
MUTE	13	8	mute switch
IN-2C	14	9	intercarrier input C for Channel 2 (right)
$O_{sel\ L}$	15	10	output select switch bit 1 (left)
IN-2D	16	11	intercarrier input D for Channel 2 (right)
$O_{sel\ R}$	17	13	output select switch bit 2 (right)
IN-3	18	14	intercarrier input for main channel
V_{REF}	19	15	decoupling capacitor for reference voltage
$C_{D\ M}$	20	16	de-emphasis capacitor for main channel
$C_{C\ M}$	21	17	audio pass-through capacitor input for main channel
V_P	22	18	positive supply voltage
O_M	23	19	main channel output
O_R	24	20	right channel output
O_L	25	21	left channel output
EXT/$\overline{INT}$	26	22	output switch bit 3 (external/internal)
EXT_R	27	23	external audio input (right)
EXT_L	28	24	external audio input (left)
$C_{ATT/REC\ R}$	29	25	attack/recovery capacitor (right)
$RECT_R$	30	26	rectifier DC decoupling (right)
$C_{NR\ D\ R}$	31	27	noise reduction de-emphasis capacitor (right)
$C_{D\ R}$	32	28	fixed de-emphasis capacitor (right)
$C_{C\ R}$	33	29	audio pass-through capacitor input for right channel
AFGND	34	30	ground for AF section
$C_{C\ L}$	35	31	audio pass-through capacitor input for left channel
$C_{D\ L}$	36	32	fixed de-emphasis capacitor (left)
$C_{NR\ D\ L}$	37	33	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	34	rectifier DC decoupling (left)
$C_{ATT/REC\ L}$	39	35	attack/recovery capacitor (left)

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
$C_{DC\,L}$	40	36	DC decoupling capacitor (left)
$C_{DC\,M}$	41	37	DC decoupling capacitor (main)
$C_{DC\,R}$	42	38	DC decoupling capacitor (right)
n.c.	–	12	not connected
n.c.	–	44	not connected

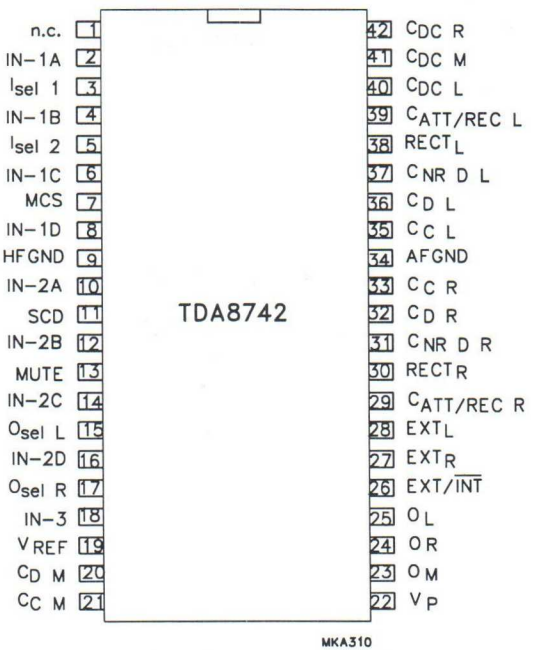


Fig.2 Pin configuration (SDIP42).

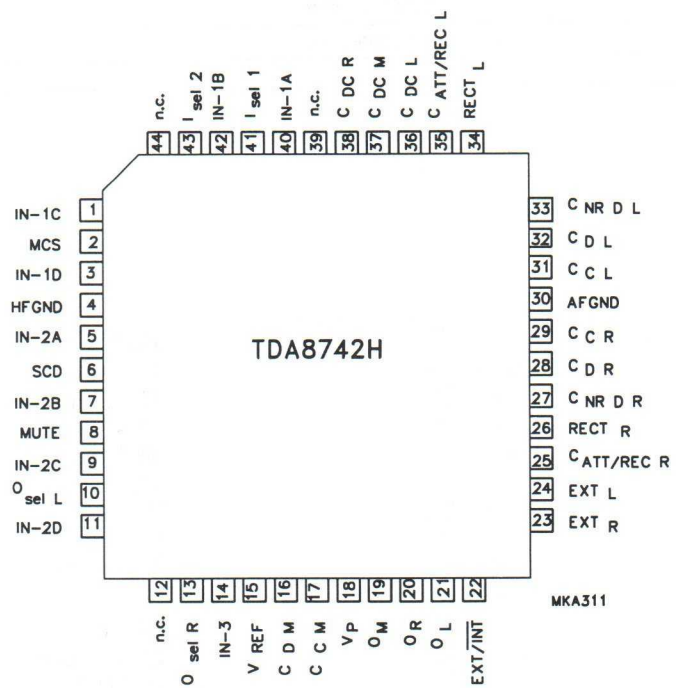


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner contains the demodulated video signal plus a number of sound carriers to facilitate reception of a PAL/NTSC/SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the single channel sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present which can be used for stereo or multi-language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz.

The TDA8742; H contains ali circuitry for processing the main channel and for two secondary channels, from baseband signal to line (SCART) output drivers. The desired frequencies can be routed to the device via bandpass filters.

Main channel (see Fig.1)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz, PLL off and 10.0 to 11.5 MHz using the MCS signal at pin 7 (2) [when pin 7 (2) is at logic 0, being a voltage from 0 to 1.2 V, the lock-in range = 5.5 to 7.5 MHz; when pin 7 (2) is at logic 1, being a voltage from 3.5 V until V_P, the lock-in range = 10.0 to 11.5 MHz; when pin 7 (2) is in the mid voltage position, being a voltage from 1.8 to 2.8 V, the main channel PLL is switched off]. The voltage is then determined by the resistor divider at this pin between V_P and ground.

If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 (14) via a 6.5 MHz ceramic bandpass filter. Alternatively, if there is a requirement to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In this event the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 (14) via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment-free. High gain and DC error signals from the PLL, which are superimposed on the demodulator output, require DC decoupling. A buffer amplifier is used to amplify the signal to the same level as the secondary channels and decouples DC using an electrolytic capacitor connected to pin 41 (37). The demodulator output signal is fed to pin 20 (16) via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor connected to ground.

Capacitor value = de-emphasis time constant per1500 (for 50 µs: 33 nF).

From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. −6 dBV) in the output amplifiers.

Secondary channels

Up to eight secondary channels are available at pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42). External ceramic bandpass filters, tuned to the required secondary sound carrier frequencies, route these signals to the inputs. This enables the demodulation of eight different channel; frequencies, which are derived from the baseband, by using an external mixer and oscillator frequency synthesizer.

For stereo applications the TDA8742; TDA8742H contains two identical secondary sound processing channels. For each channel it is possible to select from four inputs (IN-A, IN-B, IN-C and IN-D) using the input selector (see Table 1). With the input switch several stereo signals or languages can be selected for demodulation. It should be noted that the inputs are identical and can be freely interchanged Secondary Channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary Channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2'.

From the input selector switch the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled using electrolytic capacitors connected to pins 40 (36) (left) and 42 (38) (right). The output level is set with a 220 Ω resistor connected in series with the capacitor.

High frequency components in the amplified PLL output signal are filtered out in the audio LPF block (4th order Butterworth low-pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The noise reduction can be regarded as an input level-dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (0 dB) the frequency response of the first part (i.e. without the fixed de-emphasis) is virtually flat. As the input level is lowered by x-dB, the higher output frequencies will be reduced an extra x-dB with respect to the lower frequencies (1 : 2 expansion).

The NR output signal is fed to pin 36 (32) (left) and pin 32 (28) (right) via an internal resistor.

Fixed de-emphasis is achieved by these resistors and external capacitors connected to ground. The signals are DC decoupled via pins 36/35 (32/31) and 32/33 (28/29) and then routed to the output selectors.

OUTPUT SELECTION

With the output selector (see Table 2) the outputs at pins 25 and 24 (21 and 20) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs at pin 28 and 27 (24 and 23) for IC chaining purposes.

Pin 23 (19) is a separate output which delivers the main channel only, thereby creating the possibility of having three different output channels simultaneously e.g. for use in hi-fi VCRs.

The outputs at pins 25 and 24 (21 and 20) can be muted by setting the MUTE signal at pin 13 (8) to logic 1 (switch positions 6 and 7).

The output at pin 23(19) can be muted by setting the MUTE signal and the EXT/$\overline{\text{INT}}$ signal at pin 26 (22) both logic 1 (switch position 7).

All outputs at pins 23, 24 and 25 (19, 20 and 21) are line drivers with SCART level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels = –6 dBV typical when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54 × 85 kHz = 46 kHz for the main channel and 0.54 × 50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

LPF = Low-Pass Filter.

NR = Noise Reduction.

PLL = Phase-Locked-Loop.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	note 1	0	13.2	V
V_n	voltage level on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	note 2	0	1	V
V_n	voltage on pins 3, 5, 11, 13, 15, 17, 20, 21, 23 to 26, 31, 33, 35, 37, 40, 41, and 42 (6, 8, 10, 13, 16, 17, 19, 20 to 22, 27, 29, 31, 33, 36, 37, 38, 41 and 43)	note 2	0	9	V
V_n	voltage on pins 7, 18, 19, 27 to 30, 32, 36, 38 and 39 (2, 14, 15, 23 to 26, 28, 32, 34 and 35)	note 1	0	V_P	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C

Notes

1. All voltages referenced to ground pins 9 and 34 (4 and 30).
2. All voltages referenced to ground pins 9 and 34 (4 and 30). These voltages must not exceed V_P or maximum value at any time.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	53	K/W
	QFP44	69	K/W

DC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 10.52 MHz; f_{OS2} = 10.7 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	8.0	12	13.2	V
I_P	supply current	–	38	45	mA
P_{tot}	total power dissipation	–	–	600	mW
V_n	voltage on pins 20, 21, 23, 24, 25, 27, 28, 30, 32, 33, 35, 36 and 38 (16, 17, 19, 20, 21, 23, 24, 26, 28, 29, 31, 32 and 34)	–	3.8	–	V
V_{REF}	input reference voltage on pin 19 (15)	3.7	3.8	3.9	V
V_n	voltage on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	–	0	–	V
$V_{CDCL,CDCR}$	voltage on pins 40 and 42 (36 and 38)	–	2.7	–	V
V_{CDCM}	voltage on pin 41 (37)	–	2.8	–	V
I_{IN3}	input current at pin 18 (14)	–	–	1	µA

AC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 10.52 MHz; f_{OS2} = 10.7 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input pin 18 (14) and limiter						
$V_{IN3(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
$V_{IN3(rms)}$	input signal level (RMS value)		–	–	200	mV
R_{IN3}	input resistance		–	15	–	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		–	6.5	–	MHz
		MCS = logic 1	–	10.7	–	MHz
Δf_{OM}	lock range of PLL	note 1	5.5	–	7.5	MHz
		MCS = logic 1; note 1	10.0	–	11.5	MHz
R_{CDM}	output resistance for 50 µs de-emphasis pin 20 (16)		1.24	1.5	1.7	kΩ
V_{CDM}	output voltage pin 20 (16)		–18.5	–16.0	–14.5	dBV
ΔV_{CDM}	spread of PLL output voltage over lock range pin 20 (16)		–	–	±1	dB
R_{CCM}	input resistance of output amplifier pin 21 (17)		95	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{OM,OR,OL}$	output voltage pins 23, 24 and 25 (19, 20 and 21)	all PLLs locked	–9	–6	–4	dBV
UBM	unbalance voltage outputs pins 23 to 25 (19 to 21)	output selector in position 4	–0.5	–	+0.5	dB
THD	total harmonic distortion	all PLLs locked	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	–	dB
$\frac{V_{OM\,(15\,kHz)}}{V_{OM\,(1\,kHz)}}$	15 kHz frequency response with respect to 1 kHz pin 23 (19)	no de-emphasis connected	–0.5	0	+0.5	dB
$R_{OM,OR,OL}$	output resistance pins 23, 24 and 25 (19, 20 and 21)		92	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	–	74	–	dB
$MUTE_{att}$	mute attenuation	output selector in position 7	74	–	–	dB
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	35	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - HF inputs pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) and limiters						
$V_{IN1,IN2(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$V_{i(rms)}$	input signal level (RMS value)		–	–	200	mV
R_i	input resistance		260	330	380	Ω
Secondary channels 1 and 2 - PLL FM demodulators (input selector in position 1)						
f_{CCO1}	free running frequency PLL1		–	10.7	–	MHz
f_{CCO2}	free running frequency PLL2		–	10.52	–	MHz
$\Delta f_{OS1/2}$	lock range of PLLs	note 3	10	–	11.5	MHz
$R_{S1, S2}$	series resistance for optimum frequency response adjustment		0	0.68	2.2	kΩ
$V_{CDCL,CDCR(rms)}$	PLL output voltage pins 40 and 42 (36 and 38) (RMS value)	pins to be left open-circuit	–	9	–	mV
$\Delta V_{CDCL,CDCR}$	spread of PLL output voltage over lock range		–	–	±1	dB
Secondary channels - overall performance of LPF and NR (output selectors in position 1)						
R_o	output resistance for 75 µs de-emphasis pins 36 and 32 (32 and 28)		1.9	2.3	2.6	kΩ
R_i	input resistance of output amplifiers pins 35 and 33 (31 and 29)		95	150	200	kΩ
$V_{OL,OR}$	output voltage level pins 25 and 24 (21 and 20)	note 4	–8	–6	–4	dBV
UBS	unbalance voltage outputs pins 25 and 24 (21 and 20)	note 4	–1	–	+1	dB
THD	total harmonic distortion	note 4	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	–	dB
R_o	output resistance pins 25 and 24 (21 and 20)	note 4	92	125	150	Ω
$MUTE_{att}$	mute attenuation	output selector in position 6; note 4	74	–	–	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	–	74	–	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	–	74	–	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors pins 29, 39 (25, 35)	all PLLs locked; $\Delta f = 0$	14	16	20	mV
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - low-pass filter pins 38 and 30 (34 and 26)						
$\frac{V_{RECTL, RECTR (50 kHz)}}{V_{RECTL, RECTR (1 kHz)}}$	50 kHz frequency response with respect to 1 kHz	note 7	–25	–16	–9	dB
Secondary channels - noise reduction pins 25 and 24 (21 and 20); note 4						
$V_{OL, OR}$	output voltage at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–1	+1	+3	dBV
$\frac{V_{OL, OR (15 kHz)}}{V_{OL, OR (1 kHz)}}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–2	0	+2	dB
$V_{OL,OR}$	output voltage at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–29	–26	–23	dBV
$\frac{V_{OL, OR (15 kHz)}}{V_{OL, OR (1 kHz)}}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–13	–11.5	–10	dB
External inputs - pin 28 (24) (left) and pin 27 (23) (right) - overall performance (output selector in position 5)						
$V_{EXTR,EXTL}$	input signal level		–	–	6	dBV
R_i	input resistance		95	150	200	kΩ
$V_{OL,OR}$	output level	$V_{EXTR, EXTL} = –6$ dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{EXTR, EXTL} = –6$ dBV; $f_i = 1$ kHz	–	–	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{EXTR, EXTL} = –6$ dBV	80	–	–	dB
$\alpha_{L/R}, \alpha_{R/L}$	crosstalk	$f_i = 1$ kHz	–	80	–	dB
Input selector control circuit pins 3 and 5 (41 and 43) (see also Table 1) and secondary channels PLLs disable [SCD pin 11 (6)]; pin 11 (6); pins left open-circuit = logic HIGH						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		3.5	–	9	V
R_i	input resistance	connected to V_P	65	100	130	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output selector control circuit (see also Table 2) and main channel PLL lock-in select [MCS pin 7 (2)]; pins 15, 17, 26, 13 and 7 (10, 13, 22, 8 and 2) MOS inputs and should not be left open-circuit						
V_{IL}	LOW level input voltage limits		0	–	1.2	V
V_{IM}	MID level input voltage limits for MCS pin only		1.8	–	2.8	V
V_{IMF}	MID level input voltage on MCS pin if MCS pin is floating	V_P must be 1.8 to 13.2 V	17	19	21	$\%V_P$
V_{IH}	HIGH level input voltage limits		3.5	–	V_P	V
R_{IL}	low input resistance MCS pin to ground		12	19	26	kΩ
R_{IH}	high input resistance MCS pin to V_P		52	80	108	kΩ
I_{IL}	LOW level input current (not MCS pin)	V_{IL} = 0 V	–	<–1	–	µA
I_{IH}	HIGH level input current (not MCS pin)	V_{IH} = 5 V	–	<1	–	µA

Notes

1. At pin 20 (16) the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (–16 dBV), and THD of maximum 0.5%; V_P = 8 to 3.2 V; T_{amb} = –20 to +70 °C.
2. Modulation of main channel is OFF; modulation of secondary channels is ON.
3. The electrolytic capacitors at pins 40 and 42 (36 and 38) are removed and 1500 pF capacitors between pin 40 (36) and ground and between pin 42 (38) and ground are connected. At pins 40 and 42 (36 and 38) the demodulated 1 kHz signals should be present with typical levels of 9 mV (RMS) and THD of maximum 0.5%; V_P = 8 to 3.2 V; T_{amb} = –20 to +70 °C.
4. All PLLs locked; $R_{S1} = R_{S2}$ = 0.68 kΩ.
5. Modulation of secondary channel being measured and main channel is OFF; modulation of other secondary channel is ON.
6. Modulation of main channel is ON; modulation of secondary channels is OFF.
7. Measured at pins 38 (34) (left) and 30 (26) (right) and no electrolytic capacitors connected to these pins.

Table 1 Truth table for input selection

SWITCH POSITION	STATE	PIN 3 (41)	PIN 5 (43)
1	pins 2 and 10; IN-A (pins 40 and 5)	0	0
2	pins 4 and 12; IN-B (pins 42 and 7)	0	1
3	pins 6 and 14; IN-C (pins 1 and 9)	1	0
4	pins 8 and 16; IN-D (pins 3 and 12	1	1

Table 2 Truth table for output selection (note 1)

SWITCH POSITION	STATE	PIN 15 (10)	PIN 17 (13)	PIN 26 (22)	PIN 13 (8)
		OUTSEL L	OUTSEL R	EXT/$\overline{\text{INT}}$	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

Note

1. X = don't care.

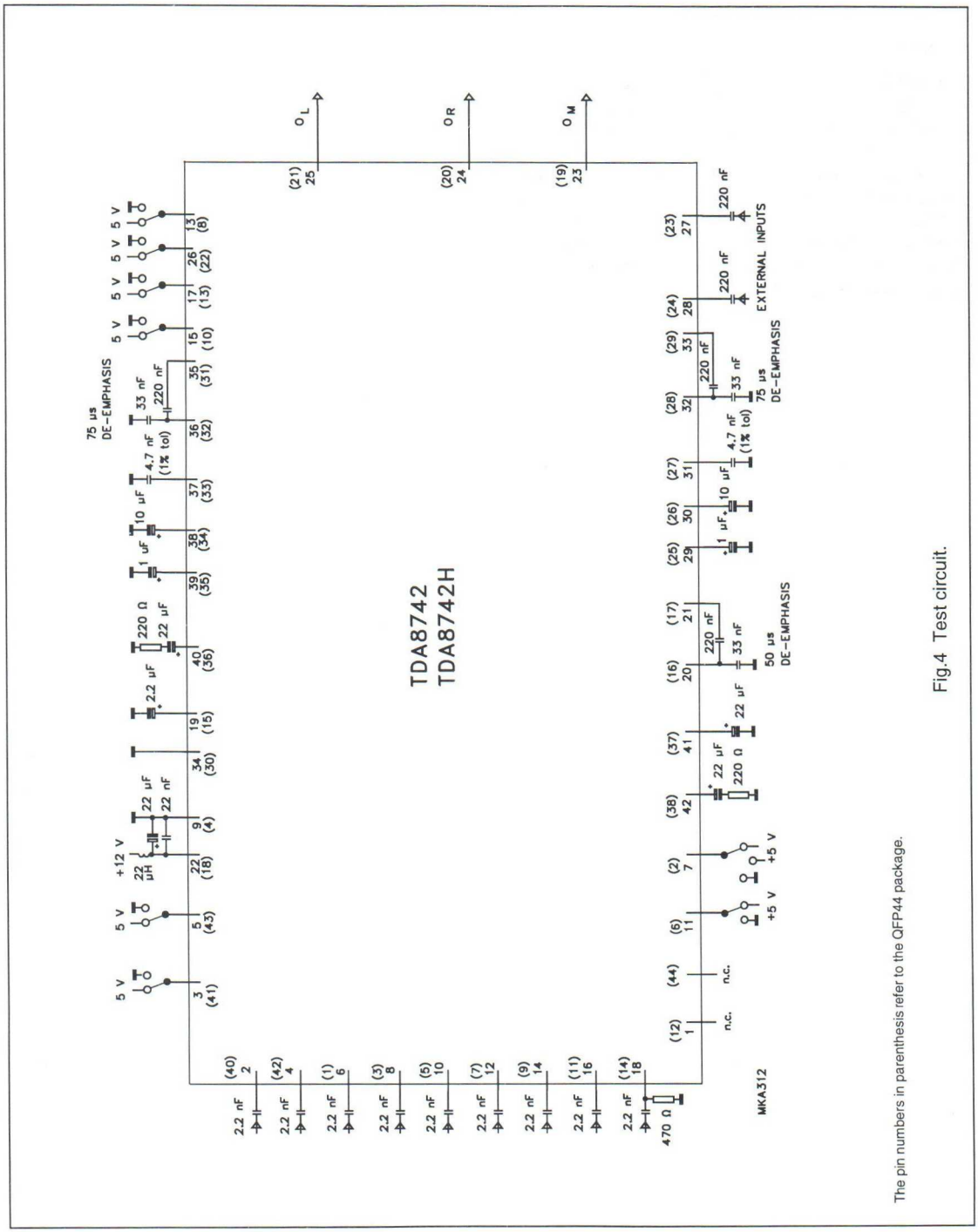


Fig.4 Test circuit.

The pin numbers in parenthesis refer to the QFP44 package.

APPLICATION INFORMATION

General

This application is mainly intended to have more than two inputs for secondary channel available. In this event a choice between the same frequency sets e.g. 10.7 and 10.52 MHz but with different bandwidths is possible. A narrow bandwidth can be chosen in the event of a weak signal, however this produces slightly more distortion. A normal signal will be processed using 150 kHz filters thus resulting in a signal with normal distortion. For the main channel either baseband or synthesized signal can be selected. The circuit is illustrated in Fig.5.

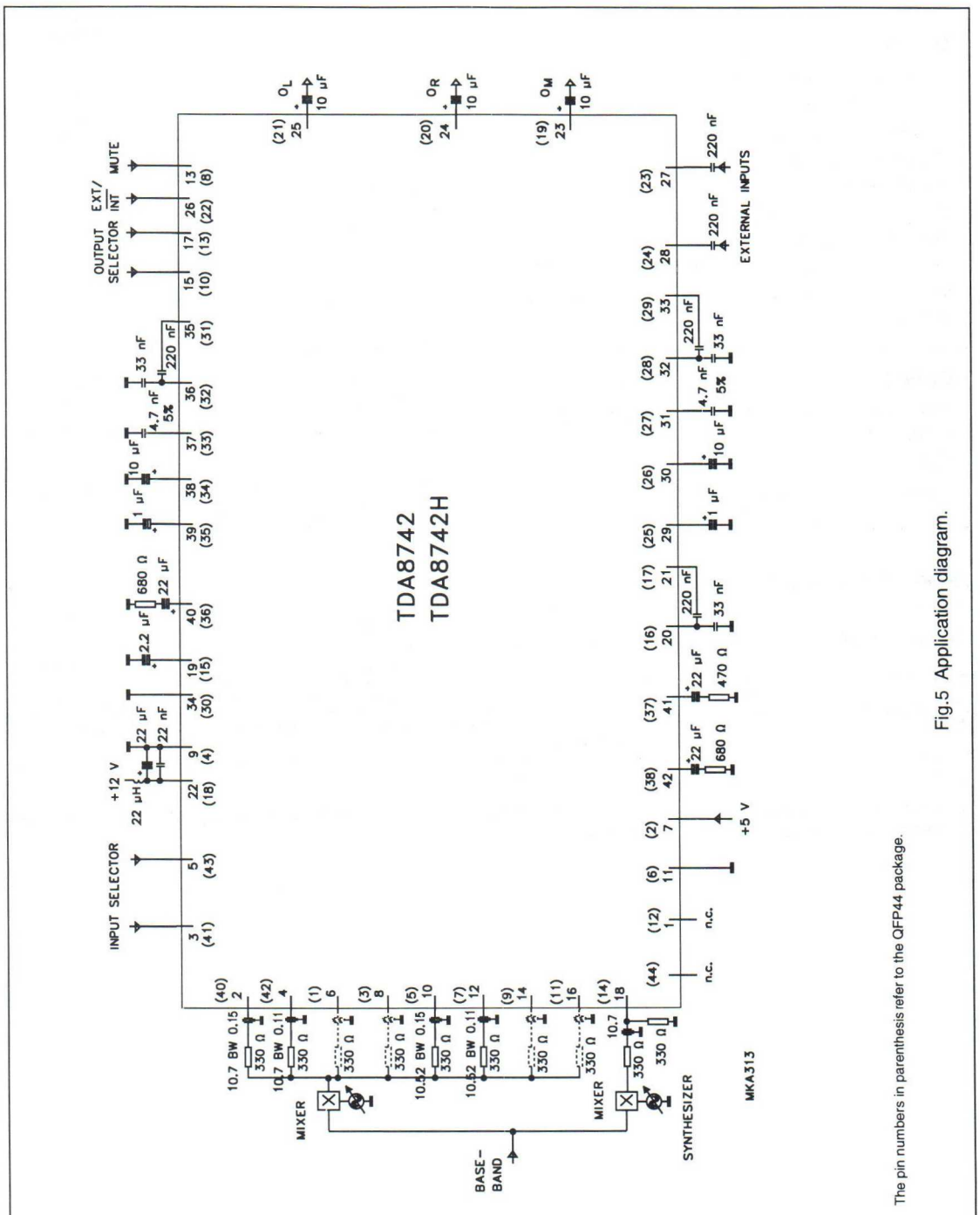


Fig.5 Application diagram.

The pin numbers in parenthesis refer to the QFP44 package.

Satellite sound receiver with I²C-bus control

TDA8745

FEATURES

- On-chip frequency synthesizer and mixer:
  - tuning range 4 to 9.77 MHz
  - reference oscillator 4 MHz (using a crystal or 4 MHz frequency source)
- IF input switches allowing selection of various IF bandwidths (wide or narrow)
- Demodulation of two audio signals by wide band Phase-Locked Loops (PLLs)
- Audio level control after PLL (modulation depth setting)
- Noise Reduction (NR) bypass for use with main audio signals
- Left, right and mono output [½(l + r)] on SCART level
- External audio inputs (for decoder connection)
- Selectable de-emphasis (DEEM) 50 μs, 75 μs, J17 and flat response
- I²C-bus control of all functions
- Two selectable addresses
- Carrier presence detector with automatic mute option.

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8745 is the successor of the TDA8740 and TDA8741. The device contains the functionality of the TDA8740 and TDA8741 together with a synthesizer, mixer and I²C-bus control.

The pin numbers mentioned in this publication refer to the SDIP42 package; unless otherwise indicated.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8745	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8745H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	synthesizer and mixer supply voltage		4.5	5.0	5.5	V
V_{P2}	I²C-bus supply voltage		4.5	5.0	5.5	V
V_{P3}	general supply voltage		8.0	12.0	13.2	V
I_{P1}	synthesizer and mixer supply current		–	37	48	mA
I_{P2}	I²C-bus supply current		–	0.6	–	mA
I_{P3}	general supply current		–	35	46	mA
S/N(A)	signal-to-noise ratio secondary channel	A-weighted; NR = on; DEEM = 75 µs	68	77	–	dB
$V_{i(rms)}$	input sensitivity (RMS value) baseband input to mixer	S/N(A) = 40 dB; NR = on; DEEM = 75 µs	–	0.5	1.5	mV
$V_{i(rms)}$	baseband input voltage (RMS value)	THD ≤ 0.5%			200	mV
V_o	output voltage		–8	–6	–4	dBV
P_{tot}	total power dissipation		–	610	800	mW
T_{stg}	storage temperature		–65	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+70	°C

BLOCK DIAGRAM

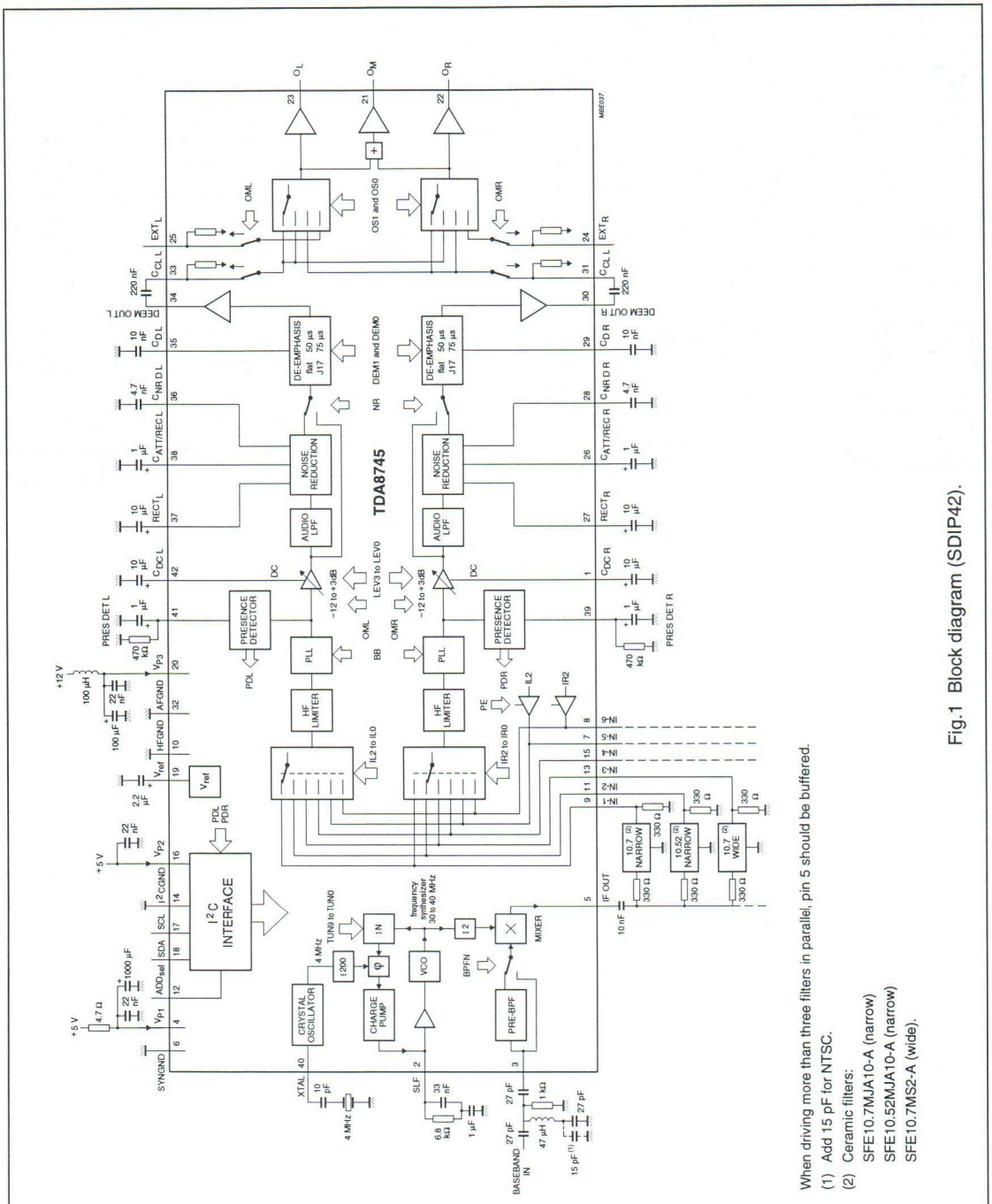


Fig.1 Block diagram (SDIP42).

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
$C_{DC\,R}$	1	39	DC decoupling capacitor (right channel)
SLF	2	41	synthesizer loop-filter
BASEBAND IN	3	42	baseband input to mixer
V_{P1}	4	43	synthesizer and mixer supply voltage (+5 V)
IF OUT	5	44	intercarrier output from mixer
SYNGND	6	1	synthesizer and mixer ground
IN-5	7	2	intercarrier input 5/port expansion output 1
IN-6	8	3	intercarrier input 6/port expansion output 2
IN-1	9	4	Intercarrier input 1
HFGND	10	5	HF ground
IN-2	11	6	intercarrier input 2
ADD_{sel}	12	7	I²C-bus address selection
IN-3	13	8	Intercarrier input 3
I²CGND	14	9	I²C-bus ground
IN-4	15	10	intercarrier input 4
V_{P2}	16	11	I²C-bus supply voltage (+5 V)
SCL	17	12	I²C-bus serial clock input
SDA	18	13	I²C-bus serial data input/output
V_{ref}	19	14	decoupling capacitor for reference voltage
V_{P3}	20	15	general supply voltage (+12 V)
O_M	21	17	mono channel output [½(l + r)]
O_R	22	18	right channel output
O_L	23	19	left channel output
EXT_R	24	20	external audio input (right channel)
EXT_L	25	21	external audio input (left channel)
$C_{ATT/REC\,R}$	26	22	attack/recovery capacitor (right channel)
$RECT_R$	27	23	rectifier DC decoupling (right channel)
$C_{NR\,D\,R}$	28	24	noise reduction de-emphasis capacitor (right channel)
$C_{D\,R}$	29	25	de-emphasis capacitor (right channel)
DEEM OUT R	30	26	de-emphasis output (right channel)
$C_{CL\,R}$	31	27	audio pass-through input (right channel)
AFGND	32	28	AF ground
$C_{CL\,L}$	33	29	audio pass-through input (left channel)
DEEM OUT L	34	30	de-emphasis output (left channel)
$C_{D\,L}$	35	31	de-emphasis capacitor (left channel)
$C_{NR\,D\,L}$	36	32	noise reduction de-emphasis capacitor (left channel)
$RECT_L$	37	33	rectifier DC decoupling (left channel)
$C_{ATT/REC\,L}$	38	34	attack/recovery capacitor (left channel)

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
PRES DET R	39	35	presence detector timing (right channel)
XTAL	40	36	crystal input for 4 MHz oscillator
PRES DET L	41	37	presence detector timing (left channel)
$C_{DC\,L}$	42	38	DC decoupling capacitor (left channel)
n.c.	–	16	not connected
n.c.	–	40	not connected

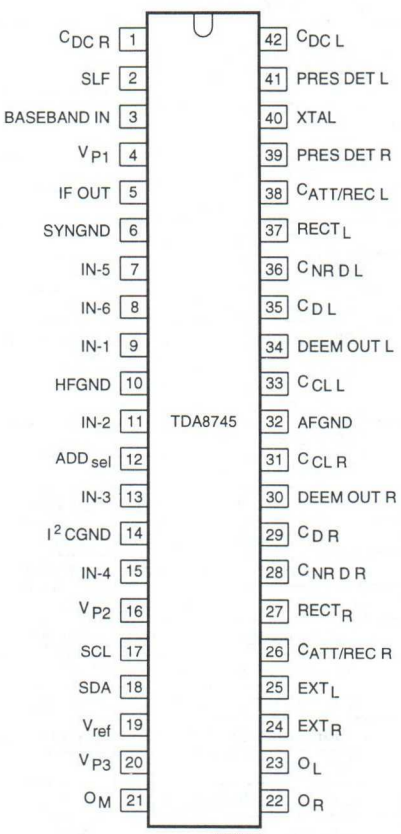


Fig.2 Pin configuration (SDIP42).

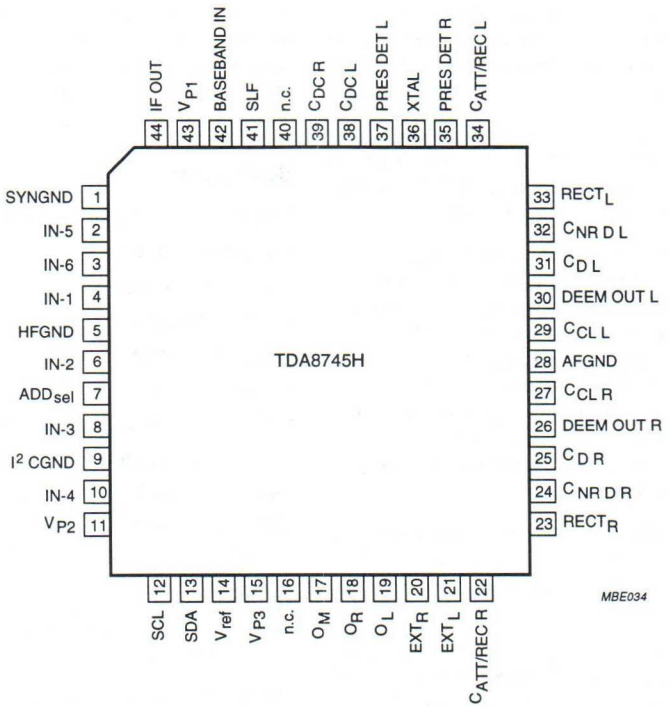


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner comprises the demodulated video signal plus a number of sound carriers in the event of reception of a PAL, NTSC or SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the mono sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present. These can be used for stereo or multi-language sound related to the video signal, or for unrelated radio sound. These carriers are also FM modulated, and for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis). These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz.

For accurate tuning to the many sound carriers, an internal frequency synthesizer and mixer are used to transfer the sound carriers to intermediate frequencies of 10.7 and 10.52 MHz.

The TDA8745 contains all circuitry for the processing of the main channel and secondary channels, from baseband signal to line (SCART) output drivers. By means of external band-pass filters the desired frequencies coming from the synthesizer/mixer are routed to the IF limiter/demodulator inputs.

Band-pass filter and mixer

Before the incoming baseband signal is applied to the mixer, the signal is filtered. Related to the sound carriers, the level of the video part of the baseband signal can be much higher, so to avoid overload it is desirable to attenuate the latter, this is also to avoid interference (additional unwanted mix of signals after mixing).

The internal band-pass filter (pass band from approximately 4 to 10 MHz) is completed by a simple external notch filter. The external filter provides substantial attenuation of the video colour carrier. The notch filter is chosen to be external because the required notch frequency is TV standard dependent and also because an accurate on-chip notch filter requires a tuning mechanism (consuming additional chip area).

The mixer is a double-balanced mixer with degeneration, this to accommodate the level of the filter output signal.

The mixer transfers the different sound carrier frequencies to fixed intermediate frequencies of 10.7 and 10.52 MHz. These frequencies are fed via an internal buffer stage to external ceramic band-pass filters before they are routed to the two demodulator inputs. The buffer stage can drive up to three external ceramic band-pass filters (assuming 330 Ω filter terminations) but this can be increased to four or more by adding an external buffer.

Synthesizer

The synthesizer consists of the following parts:

- Reference oscillator
- Reference divider
- A 10-bit programmable divider
- Phase detector
- Charge pump
- Voltage Controlled Oscillator (VCO)
- Divide-by-two circuit.

The reference frequency circuit consists of a 4 MHz crystal oscillator and a divider (by 200). The resulting reference frequency of 20 kHz is fed to the phase detector. The programmable divider consists of a series of cells (divide by 2 or 3) connected as a ripple counter. The minimum division ratio is 2^n and the maximum division ratio is $2^{n+1} - 1$.

The programmable divider output signal is also fed to the phase detector. The charge pump provides output current pulses in accordance with the signals from the phase detector. The final tuning voltage for the VCO is provided by the loop filter and a buffer amplifier.

The oscillator frequency range is from 29.04 to 40.94 MHz, depending on the setting of the programmable divider (by the TUN signal). The tuning voltage is clipped to limit the VCO frequency range. The frequency of the oscillator is divided-by-two before it is applied to the mixer (to obtain the desired 10 kHz resolution).

Left and right channel inputs

A maximum of six inputs are available (pins 9, 11, 13, 15, 7 and 8). External ceramic band-pass filters, which are tuned to the desired intermediate frequencies, rout the signals to the inputs.

For stereo purposes the TDA8745 contains two identical secondary sound processing channels (secondary channel 1 will also be referred to as 'left' or 'language 1' and secondary channel 2 as 'right' or 'language 2').

With the input selection every input pin of the left and/or right channel can be independently selected. Input selection for the left channel is controlled by the IL signal and for the right channel by the IR signal.

From the inputs, the signals are coupled to the limiter/amplifier and to the PLL demodulator of each channel. The output signal from the PLL is routed to both the presence detector and audio level control.

The inputs of pins 7 and 8 can be changed into digital outputs for external switching purposes, set by the so called Port Extension bit (PE). Not used inputs should be connected to ground. Note that the inputs of pins 7 and 8 are also floating when not in Port Extension mode.

Presence detector

The presence detector is used to determine if a carrier is present on the channel of interest. It does so by measuring the amount of high frequency noise (>20 kHz) in the audio signal, which is directly related to the C/N (carrier-to-noise ratio) at the IF input. If a carrier is present, these high frequencies are fairly moderate, if no carrier is present, strong noise components are present.

The audio signal, first high-pass filtered and then rectified, is filtered by the components at pins 41 and 39 (PRES DET L and PRES DET R). The DC level at this pin is then compared with an internal reference voltage. If the level at pins 41 and 39 exceeds this voltage level, the presence detector output goes HIGH (no carrier).

This output signal can be used to drive the output mute (if bit PDM = 1; see Section "Output selection") and can be monitored by reading bits PDL and PDR. The detection level can be modified by changing the leakage resistor at pins 41 and 39, a higher resistor value gives a 'no carrier' response ant C/N levels detected as 'carrier present' with a lower resistor value.

Audio level control

Each demodulator output signal is amplified in a buffer amplifier and DC decoupled by means of electrolytic capacitors connected to pin 42 (left) and pin 1 (right).

The output level of all channels is –6 dBV typical at a frequency deviation of the FM signal of 54% of the maximum deviation (i.e 0.54×85 kHz = 46 kHz for the main channel and 0.54×50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

To adjust for different (main channel) modulation depths used at some satellites the audio level is made adjustable, the signal can be controlled in steps of 1 dB from –12 dB to +3 dB by the LEV signal.

Noise Reduction (NR)

To improve the quality of the secondary channels, the audio signal is processed at the transmitter side before modulation. For an overall flat audio response the inverse processing must take place after demodulation. This is achieved in the NR.

The NR can be regarded as an input level dependent Low-Pass Filter (LPF) [adaptive de-emphasis system] followed by a fixed de-emphasis. Figure 3 shows the transfer characteristics as function of the input level (normalized to input level, and without the fixed de-emphasis).

At maximum input level (50 kHz frequency deviation, referred to as 0 dB) the frequency response of the first part (i.e. without fixed de-emphasis) is nearly flat (note the small dip around 3 kHz in Fig.3; this is a system attribute). As the input level is X dB lowered, the higher output frequencies will be reduced an extra X dB with respect to the lower frequencies15 (1 : 2 expansion).

If a main carrier signal is received, the NR can be bypassed at which the signal is fed directly to the de-emphasis circuit. The noise reduction is active when the NR signal (via I²C-bus) is logic 1.

De-emphasis

De-emphasis is realized by means of several internal resistors and an external capacitor to ground. Via the I²C-bus, the DEM signal can be switched between 50 µs, 75 µs, J17 and no de-emphasis. Figure 4 shows these four different possibilities.

Output selection

With the output selector the output pins 23 and 22 can be switched to the left and right satellite channels (pins 33 and 31) or to the external inputs (pins 25 and 24) for an other signal source or for connection of a decoder box. the OS1 and OS0 bits determine this selection.

Pin 21 is a separate output which delivers the mono channel. The mono signal is the sum of pin 23 (left) and pin 22 (right) output signal [½(l + r)].

Output pins 23 and 22 can be muted by setting the OML and OMR signals to logic 1. In addition, automatic muting is also possible, the presence detector (as described in Section "Presence detector") sets the PDL bit (PDR for other channel). Absence of a carrier at the selected frequency results in automatic muting. This mechanism is enabled or inhibited by the PDM bit (Presence Detector auto Mute).

All outputs (pins 21, 22 and 23) are line drivers with SCART level capability and are short-circuit protected by means of 125 Ω output resistors. Pins 34 and 30 are also line drivers at SCART level and can be used as signal outputs before the IC's output selection (i.e. for decoder box use).

ABBREVIATIONS

BPF = Band-Pass Filter.

f_{mod} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

IF = Intermediate Frequency.

IL = Input Left.

IR = Input Right.

LPF = Low-Pass Filter.

NR = Noise Reduction.

OML = Output Mute Left.

OMR = Output Mute Right.

OS = Output Select.

PDM = Presence Detector auto Mute.

PE = Port Extension.

PLL = Phase-Locked Loop.

POR = Power-On Reset.

S/N = Signal-to-Noise ratio.

VCO = Voltage Controlled Oscillator.

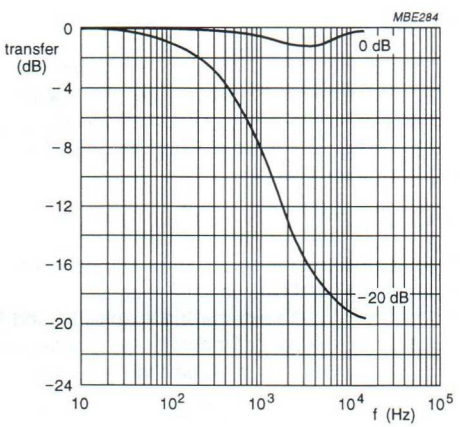


Fig.4 Noise reduction transfer as function of input level.

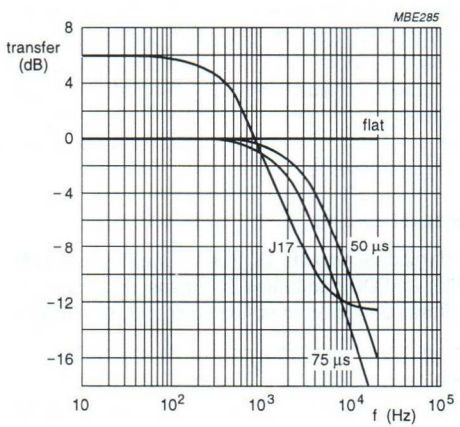


Fig.5 LF de-emphasis curves.

I²C-BUS PROTOCOL

Table 1 Slave receiver/transmitter address: D4 or D6 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	0	1	0	1	AS(1)	R/$\overline{W}$(2)

Notes

1. AS bit defined by level at address select (pin 12); 0 V = logic 0; 5 V = logic 1.
2. R/$\overline{W}$ = 0; TDA8745 is receiver (microcontroller is master transmitter).
   R/$\overline{W}$ = 1; TDA8745 is transmitter (microcontroller is master receiver).

TDA8745 receiver use

In the receiver mode the device has four subaddresses with auto-increment, as shown in Tables 2 to 5.

Table 2 Input byte SA: 00; situation after POR

IL2 i7	IL1 i6	IL0 i5	IR2 i4	IR1 i3	IR0 i2	TUN9 i1	TUN8 i0
0	0	0	0	0	1	1	0

Table 3 Tuning byte SA: 01; situation after POR

TUN7 t7	TUN6 t6	TUN5 t5	TUN4 t4	TUN3 t3	TUN2 t2	TUN1 t1	TUN0 t0
1	1	1	0	1	1	0	0

Table 4 Select byte SA: 02; situation after POR

TEST s7	BB s6	OS1 s5	OS0 s4	PDM s3	PE s2	OML s1	OMR s0
0	0	0	0	0	0	1	1

Table 5 Audio byte SA: 03; situation after POR

LEV3 a7	LEV2 a6	LEV1 a5	LEV0 a4	NR a3	DEM1 a2	DEM0 a1	BPFN a0
1	1	0	0	1	1	1	0

TDA8745 transmitter use

No subaddress.

Table 6 Read byte

PDL r7	PDR r6	– r5	– r4	– r3	– r2	– r1	POR r0
0 or 1	0 or 1	1	1	1	1	1	0 or 1

Slave receiver mode (bits transmitted from microcontroller to TDA8745)

Different IF inputs can be selected for the PLLs, for switching between different external BPFs and/or channels; see Tables 7 and 8.

Table 7 IL2 to IL0; Input Left; note 1

IL2 i7	IL1 i6	IL0 i5	PE[2] s2	MODE
0	0	0	0	IF input IN-1 selected for left PLL [por].
0	0	1	0	IF input IN-2 selected for left PLL.
0	1	0	0	IF input IN-3 selected for left PLL.
0	1	1	0	IF input IN-4 selected for left PLL.
1	0	0	0	IF input IN-5 selected for left PLL.
1	0	1	0	IF input IN-6 selected for left PLL.
1	1	0	0	No selection.
1	1	1	0	No selection.
X	0	0	1	IF input IN-1 selected for left PLL.
X	0	1	1	IF input IN-2 selected for left PLL.
X	1	0	1	IF input IN-3 selected for left PLL.
X	1	1	1	IF input IN-4 selected for left PLL.
0	X	X	1	IF input IN-5 used as output; 0 = 0 V.
1	X	X	1	IF input IN-5 used as output; 1 = 5 V.

Notes

1. X = don't care.
2. Bit PE (s2) can be set to logic 1 to change IF input 5 into digital output for external switching purposes.

Table 8 IR2 to IR0; input right; note 1

IR2 i4	IR1 i3	IR0 i2	PE[2] s2	MODE
0	0	0	0	IF input IN-1 selected for right PLL.
0	0	1	0	IF input IN-2 selected for right PLL [por].
0	1	0	0	IF input IN-3 selected for right PLL.
0	1	1	0	IF input IN-4 selected for right PLL.
1	0	0	0	IF input IN-5 selected for right PLL.
1	0	1	0	IF input IN-6 selected for right PLL.
1	1	0	0	No selection.
1	1	1	0	No selection.
X	0	0	1	IF input IN-1 selected for right PLL.
X	0	1	1	IF input IN-2 selected for right PLL.
X	1	0	1	IF input IN-3 selected for right PLL.
X	1	1	1	IF input IN-4 selected for right PLL.
0	X	X	1	IF input IN-6 used as output; 0 = 0 V.
1	X	X	1	IF input IN-6 used as output; 1 = 5 V.

Notes

1. X = don't care.
2. Bit PE (s2) can be set to logic 1 to change IF input 6 into digital output for external switching purposes.

Table 9 TUN9 to TUN0; tuning

TUN9 i1	TUN8 i0	TUN7 t7	TUN6 t6	TUN5 t5	TUN4 t4	TUN3 t3	TUN2 t2	TUN1 t1	TUN0 t0	10.7 IF (MHz)	10.52 IF (MHz)
0	1	1	0	1	0	1	1	0	0	3.82	4.00
0	1	1	0	1	0	1	1	0	1	3.83	4.01
0	1	1	0	1	0	1	1	1	0	3.84	4.02
0110101111 to 1001010011										3.85 to 5.49	4.03 to 5.67
1	0	0	1	0	1	0	1	0	0	5.50	5.68
1001010101 to 1010000101										5.51 to 5.99	5.69 to 6.17
1	0	1	0	0	0	0	1	1	0	6.00	6.18
1010000111 to 1010110111										6.01 to 6.49	6.19 to 6.67
1	0	1	0	1	1	1	0	0	0	6.50	6.68
1010111001 to 1011101011										6.51 to 7.01	6.69 to 7.19
1	0	1	1	1	0	1	1	0	0	7.02[1]	7.20[1]
1011101101 to 1100001111										7.03 to 7.37	7.21 to 7.55
1	1	0	0	0	1	0	0	0	0	7.38	7.56
1100010001 to 1100110011										7.39 to 7.73	7.57 to 7.91
1	1	0	0	1	1	0	1	0	0	7.74	7.92
1100110101 to 1111111100										7.75 to 9.74	7.93 to 9.92
1	1	1	1	1	1	1	1	0	1	9.75	9.93
1	1	1	1	1	1	1	1	1	0	9.76	9.94
1	1	1	1	1	1	1	1	1	1	9.77	9.95

Note

1. This is the situation after POR.

The frequency range of synthesizer is shown in Table 10.

Table 10 Frequency range of synthesizer

PARAMETER	RANGE (MHz)
Synthesizer frequency range	29.04 to 40.94 (in 20 kHz grid); note 1
Mixer input frequency range	14.52 to 20.47 (in 10 kHz grid); note 2
Tuning range	3.82 to 9.77 (in 10 kHz grid; 10.7 MHz IF); note 3

Notes

1. Tuning the synthesizer below 29.04 MHz may be possible, but is not guaranteed.
2. The mixing frequency (f_{mix}) can be calculated with equation:
   f_{mix} = (1024 + 512[TUN9] + 256[TUN8] + 128[TUN7] + 64[TUN6] + 32[TUN5] + 16[TUN4] + 8[TUN3] + 4[TUN2] + 2[TUN1] + [TUN0]) × 10 kHz.
3. Tuning frequency = mixer input frequency – 10.7 MHz.

Table 11 Bit TEST

TEST s7	MODE	DESCRIPTION
0	– [por]	In applications this bit should always be logic 0, to avoid conflicts with other settings.
1	test	Setting TEST enables some special modes used for factory testing.

Table 12 Bit BB; baseband; note 1

BB s6	MODE	DESCRIPTION
0	synthesizer	Synthesizer use (PLLs central frequency approximately 10.7 MHz) [por].
1	baseband	Baseband use (PLLs central frequency approximately 6 MHz).

Note

1. The PLL demodulators can also be used for demodulating FM carriers (e.g. terrestrial TV sound) at baseband frequencies, by changing the lock range of the PLLs.

Table 13 Bits OS1 and OS0; output select; note 1

OS1 s5	OS0 s4	MODE	DESCRIPTION
0	0	stereo [por]	Left channel audio (pin 33) at O_L; right channel audio (pin 31) at O_R.
0	1	left	Left channel audio (pin 33) at both O_L and O_R.
1	0	right	Right channel audio (pin 31) at both O_L and O_R.
1	1	external	External left at (pin 25) at O_L; external right (pin 24) at O_R.

Note

1. The signal at both line outputs O_L and O_R (pins 23 and 22) can be selected with bits OS1 and OS0.

Table 14 Bit PDM; Presence Detector auto Mute; note 1

PDM s3	MODE	DESCRIPTION
0	– [por]	–
1	PDM	If this bit is set to logic 1, a channel for which no incoming carrier is found will be muted.

Note

1. In both situations the status of the presence detector can be monitored by reading the bits PDL (r7) and PDR (r6) back from the IC. Appropriate action (e.g. muting, channel selection or tuning) can then be taken by the microcontroller. Note that this function also mutes the signal from the external inputs (pins 25 and 24). This may be desirable when using these inputs for connecting a satellite descrambler box. If not, reset PDM (s3) to logic 0 when selecting external [e.g. together with bits OS1 (s5) and OS0 (s4)].

Table 15 Bit PE; Port Extension; note 1

PE s2	DESCRIPTION
0	6 IF inputs; no digital output [por]
1	4 IF inputs; 2 digital outputs

Note

1. Two IF inputs (IN-5 and IN-6; pins 7 and 8) can be used as digital output instead. If no more than four IF inputs are needed, two external functions can be controlled via the I²C-bus this way. The level at these pins is controlled by bits IL2 (i7) and IR2 (i4); see Tables 7 and 8.

Table 16 Bits OML and OMR; Output Mute Left and Output Mute Right; note 1

BIT	LEVEL	MODE	DESCRIPTION
OML (s1)	0	–	–
	1	mute	Left audio channel is muted.
OMR (s0)	0	–	–
	1	mute	Right audio channel is muted.

Note

1. Left and right audio can be muted independently. Note that also the external input signals (pins 25 and 24) can be muted this way.

Table 17 Bits LEV3 to LEV0; level adjust; note 1

LEV3 a7	LEV2 a6	LEV1 a5	LEV0 a4	MODE	SECONDARY CHANNELS[2] (kHz)	MAIN CHANNEL[2] (kHz)
0	0	0	0	−12 dB	199	338
0	0	0	1	−11 dB	177	302
0	0	1	0	−10 dB	158	269
0	0	1	1	−9 dB	141	240
0	1	0	0	−8 dB	126	214
0	1	0	1	−7 dB	112	190
0	1	1	0	−6 dB	100	170
0	1	1	1	−5 dB	89	151
1	0	0	0	−4 dB	79	135
1	0	0	1	−3 dB	71	120
1	0	1	0	−2 dB	63	107
1	0	1	1	−1 dB	56	95
1	1	0	0	0 dB	50[3]	85[3]
1	1	0	1	+1 dB	45	76
1	1	1	0	+2 dB	40	68
1	1	1	1	+3 dB	35	60

Notes

1. The audio level can be adjustment in steps of 1 dB, to adjust for different FM deviations used in main channel audio carriers and/or spread in PLL output amplitude. With secondary carriers the Noise Reduction (NR) is to be used with the 0 dB setting (note that the NR audio frequency response is level dependent, therefore another setting than 0 dB is only to be used when making a fine-adjustment (+2 dB/−2 dB) for PLL spread. Typical setting for main channel carriers is in most cases 85 kHz (0 dB) or 76 kHz (+1 dB).
2. Maximum deviation.
3. Situation after POR.

Table 18 Bit NR; Noise Reduction; note 1

NR a3	MODE	DESCRIPTION
0	NR bypassed	Noise Reduction bypassed (main channel).
1	NR active	Noise Reduction active (secondary channels) [por].

Note

1. For reception of main channel carriers the NR circuit can be bypassed.

Table 19 Bits DEM1 and DEM0; De-emphasis; note 1; see Fig.5

DEM1 a2	DEM0 a1	DE-EMPHASIS
0	0	no de-emphasis (flat)
0	1	J17
1	0	50 µs(2)
1	1	75 µs [por](3)

Notes

1. Different de-emphasis characteristics can be selected, to adjust for different main channel audio carriers.
2. In most cases the de-emphasis needed for main channel carriers is 50 µs.
3. The NR is to be used with the 75 µs setting for standard secondary channels.

Table 20 Bit BPFN; Band-Pass Filter Not; note 1

BPFN a0	DESCRIPTION
0	Mixer input signal filtered by BPF [por].
1	Mixer input signal is not filtered.

Note

1. To avoid interference by the video signal, the incoming baseband signal is filtered. If this filtering is not required the filter can be switched off.

Slave transmitter mode (bits transmitted from TDA8745 to microcontroller)

Table 21 Bit PDL; Presence Detector Left; note 1

PDL r7	DESCRIPTION
0	carrier detected at left channel
1	no carrier detected at left channel

Note

1. Bit PDL (r7) transmits the current status of the left channel presence detector. When PDL = 1, no carrier is found at the currently selected frequency. If bit PDM (s3) = 0 the left channel audio is muted.

Table 22 Bit PDR; Presence Detector Right; note 1

PDR r6	DESCRIPTION
0	carrier detected at right channel
1	no carrier detected at right channel

Note

1. Bit PDR (r6) transmits the current status of the right channel presence detector. When PDR = 1, no carrier is found at the currently selected frequency. If bit PDM (s3) = 0 the right channel audio is muted.

Table 23 Bit POR; Power-On Reset; note 1

POR r0	DESCRIPTION
0	normal operation
1	POR generated; power dip detected since last read of POR bit.

Note

1. At switching on, or after a power dip on the I²C-bus supply voltage (V_{P2}), an internal signal is generated which resets the I²C-bus registers to a pre-defined state. If bit POR (r0) = 1, such a situation has occurred since the last time the read byte was read. After reading, the bit is reset to logic 0.

Table 24 Bits r5 to r1

– r5	– r4	– r3	– r2	– r1	DESCRIPTION
1	1	1	1	1	These bits have no function. Although their state is fixed, the microcontroller should not rely on this because of eventual future use.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	synthesizer and mixer supply voltage	note 1	0	5.5	V
V_{P2}	I²C-bus supply voltage	note 1	0	5.5	V
V_{P3}	general supply voltage	note 1	0	13.2	V
V_n	voltage on pins 2, 3, 5 and 40	note 1	0	5.5	V
	voltage on pins 7 and 8	note 2	0	V_{P2}	V
	voltage on pins 1 and 42	note 1	0	7.7	V
V_i	input voltage on pins 7, 8, 9, 11, 13 and 15	notes 1 and 3	0	1	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C

Notes

1. All voltages referenced to ground at pins 6, 10, 14 and 32.
2. Port Extension enabled (PE = 1; see Table 15).
3. IN-5 and IN-6 (pins 7 and 8) **not** being in the Port Extension mode.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	50	K/W
	QFP44	60	K/W

DC CHARACTERISTICS

All voltages referenced to ground (pins 6, 10, 14 and 32). In accordance with the block diagram (see Fig.1); $V_{P1} = V_{P2} = 5$ V; $V_{P3} = 12$ V; $T_{amb} = 25$ °C; $f_{OS1} = 10.7$ MHz; $f_{OS2} = 10.52$ MHz (no modulation; see note 1); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	synthesizer and mixer supply voltage		4.5	5.0	5.5	V
V_{P2}	I²C-bus supply voltage		4.5	5.0	5.5	V
V_{P3}	general supply voltage		8.0	12	13.2	V
I_{P1}	synthesizer and mixer supply current		–	37	48	mA
I_{P2}	I²C-bus supply current		–	0.6	–	mA
I_{P3}	general supply current		–	35	46	mA
P_{tot}	total power dissipation		–	610	800	mW
Pins						
$V_{21,22,23}$	voltage on pins 21, 22 and 23		–	3.8	–	V
$V_{24,25,31,33}$	voltage on pins 24, 25, 31 and 33		–	3.8	–	V
$V_{31,33}$	voltage on pins 31 and 33		–	3.8	–	V
$V_{30,34}$	voltage on pins 30 and 34		–	3.8	–	V
$V_{27,37}$	voltage on pins 27 and 37		–	3.8	–	V
V_{19}	voltage on pin 19		3.7	3.8	3.9	V
$V_{9,11,13,15}$	voltage on pins 9, 11, 13 and 15	note 2	–	0	–	V
$V_{42,1}$	voltage on pins 42 and 1		–	3.4	–	V
$V_{41,39}$	voltage on pins 41 and 39		–	2.6	–	V
V_5	voltage on pin 5		–	1.8	–	V
V_3	voltage on pin 3		–	2.4	–	V
V_2	voltage on pin 2		–	2.6	–	V
V_{40}	voltage on pin 40		–	1.3	–	V
Port extensions (pins 7 and 8; bit PE = 1)						
V_{OH}	HIGH level output voltage	$I_{OH} = 0.5$ mA	4.5	–	5	V
V_{OL}	LOW level output voltage	$I_{OL} = -0.5$ mA	0	–	0.5	V

Notes

1. Presence of both carriers is required to achieve lock of the PLLs; otherwise not all pins will have a stable DC voltage.
2. Pin 7 and 8 functioning as normal inputs (bit PE = 0).

AC CHARACTERISTICS

All voltages referenced to ground (pins 6, 10, 14 and 32); in accordance with the block diagram (see Fig.1); $V_{P1} = V_{P2} = 5$ V; $V_{P3} = 12$ V; $T_{amb} = 25$ °C; $f_{mod} = 1$ kHz; $\Delta f_M = 46$ kHz; $\Delta f_{S1} = \Delta f_{S2} = 27$ kHz (reference levels); $f_{OM} = 10.7$ MHz; $f_{OS1} = 10.7$ MHz; $f_{OS2} = 10.52$ MHz; IF level at pins 9, 11, 13, 15, 7 and 8 = 20 mV (RMS value) and SFE 10.7MJA (narrow), SFE 10.52MJA (narrow) and SFE 10.7MS3 (wide) ceramic filters; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band-pass filter, mixer and buffer						
R_i	input resistance		10	12.5	15	kΩ
$V_{i(rms)}$	baseband input voltage (RMS value)	note 1	–	–	200	mV
V_3	1 dB compression point (RMS value)	$\Delta V_3 - \Delta V_5 = 1$ dB; note 2	–	180	–	mV
H_l/H_h	filter transfer at 200 kHz with respect to 7.3 MHz		–	–	–60	dB
H_{lm}/H_h	filter transfer at 2 MHz with respect to 7.3 MHz		–	–28	–20	dB
H_{mh}/H_h	filter transfer at 5.3 MHz with respect to 7.3 MHz		–2	+2	+4	dB
H_h*A	filter transfer at 7.3 MHz and mixer amplification		16	17.5	19	dB
H_h*C	filter transfer at 7.3 MHz and mixer conversion gain	note 3	13	14.5	16	dB
$I_{o(p)}$	mixer output current (peak)		5	7	–	mA
R_o	mixer output resistance	f = 10.7 MHz; note 4	–	12	30	Ω
Charge pump, buffer amplifier and VCO						
t	repetition time of charge pump pulses		–	50	–	µs
S_{VCO}	VCO sensitivity	note 5	–	–9	–	MHz/V
f_{VCO}	VCO frequency	$V_{loopf} = 2.6$ V	–	35.4	–	MHz
Crystal oscillator (4 MHz)						
f_{xtal}	crystal oscillator frequency		–	4	–	MHz
R_{xtal}	resonance resistance of crystal		–	–	60	Ω
C_{xtal}	parallel capacitance of crystal		–	4.5	10	pF
$I_{i(p)}$	input current from external 4 MHz source (peak)	note 6	50	–	–	µA
IF inputs (pins 9, 11, 13, 15, 7 and 8) and limiters						
$V_{IN-1\ to\ IN-6(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB; $\Delta f_S = 27$ kHz; NR = on; de-emphasis = 75 µs	–	0.3	1	mV
		S/N(A) = 40 dB; $\Delta f_M = 46$ kHz; NR = off; de-emphasis = 50 µs	–	0.8	2	mV
V_{i1} to V_{i6}	input signal	THD ≤ 0.5%	–	–	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulators						
f_{CCO}	free-running frequency	PLL left; BB = 0	–	10.6	–	MHz
		PLL right; BB = 0	–	10.6	–	MHz
		PLL left; BB = 1	–	6.9	–	MHz
		PLL right; BB = 1	–	6.9	–	MHz
Δf_{CCO}	lock range of PLLs	BB = 0; note 7	10	–	11.5	MHz
		BB = 1; note 7	5.50	–	8.50	MHz
V_{OL}; V_{OR}	PLL output voltage (pins 23 and 22)	NR = off; DEEM = flat; BB = 0	–	–5.6	–	dBV
		NR = off; DEEM = flat; BB = 1; note 8	–	–7.3	–	dBV
ΔV_{OL}; ΔV_{OR}	spread off PLL output voltage over lock range (pins 23 and 22)	NR = off; DEEM = flat; BB = 1; note 8	–	–	±1.5	dB
Noise reduction						
$\frac{V_{37,27\ (50\ kHz)}}{V_{37,27\ (1\ kHz)}}$	low-pass filter 50 kHz response with respect to 1 kHz	note 9	–21	–16	–11	dB
$V_{o\ 23,22}$	output voltage (pins 23 and 22)	at 0 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; DEEM = flat; note 10	–1	+1	+3	dBV
		at –20 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; DEEM = flat	–29	–26	–23	dBV
$\frac{V_{23,22\ (15\ kHz)}}{V_{23,22\ (1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz	at 0 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; DEEM = flat	–2	0	+2	dB
		at –20 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; DEEM = flat	–13	–11.5	–10	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors (pins 38 and 26)	$\Delta f = 0$ kHz; all PLLs locked	14	–	22	mV
De-emphasis						
$\frac{V_{23,22\ (15\ kHz)}}{V_{23,22\ (1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz flat	NR = off; DEEM = flat	–0.5	0	+0.5	dB
		NR = off; DEEM = J17; note 11	–14.3	–12.8	–11.3	dB
		NR = off; DEEM = 50 µs	–16	–14.5	–13	dB
		NR = off; DEEM = 75 µs	–19.4	–17.9	–16.4	dB
R_o	output resistance (pins 34 and 30)		100	125	150	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall performance						
$V_{i\ 3(rms)}$	baseband input sensitivity main sound carrier (RMS value)	S/N(A) = 40 dB; Δf_S = 27 kHz; NR = on; DEEM = 75 µs	–	0.5	1.5	mV
		S/N(A) = 40 dB; Δf_M = 46 kHz; NR = off; DEEM = 50 µs	–	1.5	3	mV
$V_{o\ 23,22}$	output voltage	secondary channels; Δf_S = 27 kHz; NR = on; DEEM = 75 µs	–8	–6	–4	dBV
		main channel; Δf_S = 46 kHz; NR = off; DEEM = 50 µs	–8	–6	–4	dBV
UBS	unbalance output voltage	secondary channels; NR = on; DEEM = 75 µs	–1	–	+1	dBV
		main channel; NR = off; DEEM = 50 µs	–1	–	+1	dBV
THD	total harmonic distortion	secondary channels; NR = on; DEEM = 75 µs; note 12	–	0.1	0.5	%
		main channel; NR = off; DEEM = 50 µs; note 12	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; secondary channels (synthesizer included); NR = on; DEEM = 75 µs; note 12	69	77	–	dB
		A-weighted; main channel (synthesizer excluded); NR = on; DEEM = 75 µs; note 12	72	80	–	dB
		A-weighted; secondary channels (synthesizer included); NR = off; DEEM = 50 µs; note 12	54	62	–	dB
		A-weighted; main channel (synthesizer excluded); NR = on; DEEM = 50 µs; note 12	62	70	–	dB
$MUTE_{att}$	mute attenuation	output select left and right muted	74	90	–	dB
$\alpha_{ct\ S/S}$	crosstalk attenuation between secondary channels		–	74	–	dB
$SVRR_{P3}$	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	14.3	–	dB
		V_{RR} = 100 mV; f_i = 1 kHz	–	15.6	–	dB
$SVRR_{P1-P2}$	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	25	–	dB
		V_{RR} = 100 mV; f_i = 1 kHz	–	4	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output select						
$V_{i\ 25,24}$	input voltage (pins 25 and 24)		–	–	8	dBV
$R_{i\ 25,24,33,31}$	input resistance at pins 25, 24, 33 and 31		100	150	200	kΩ
$V_{o\ 23,22}$	output voltage at pins 23 and 22	$V_{24,25}$ = –6 dBV; OS = external	–6.5	–6	–5.5	dBV
$R_{o\ 23,22,21}$	output resistance at pins 23, 22 and 21		100	125	150	Ω
THD	total harmonic distortion	$V_{24,25}$ = –6 dBV; OS = external; f = 1 kHz	–	0.01	0.3	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{24,25}$ = –6 dBV; OS = external	80	–	–	dB
$\alpha_{ct\ L/R}$; $\alpha_{ct\ R/L}$	crosstalk between channels	f = 1 kHz	–	80	–	dB
I²C-bus						
C_i	input capacitance		–	4	–	pF
I_{sink}	SDA sink current		3	–	–	mA
V_{IH}	HIGH level input voltage		3	–	5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
Address D4H	address D4H	ADD_{sel} = LOW	0	–	1	V
Address D6H	address D6H	ADD_{sel} = HIGH	3	–	5	V
f_{SCL}	SCL frequency		–	–	100	kHz

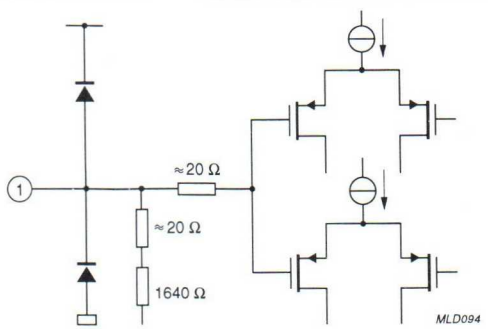
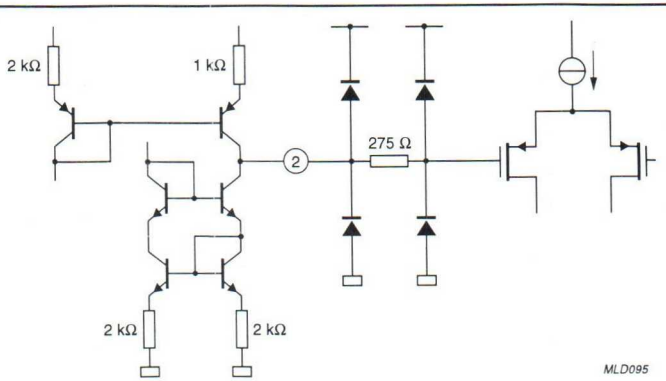
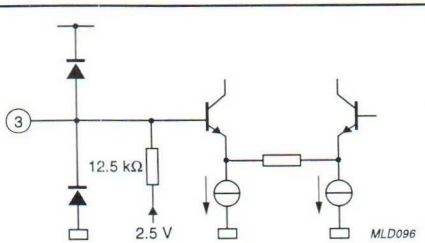
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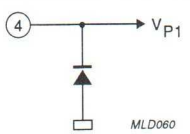
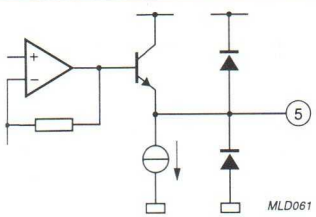
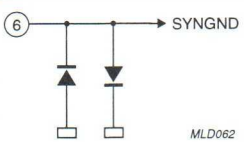
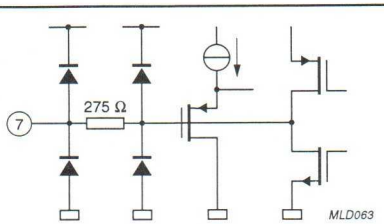
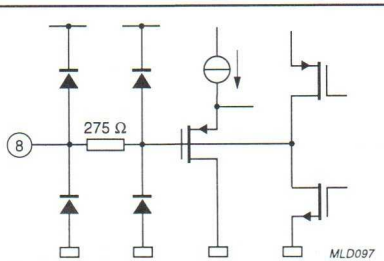
1. Maximum of 0.5% THD at LF outputs.
2. When the increase of the output signal (pin 5 at 10.7 MHz) lags 1 dB behind the increase of the input signal (pin 3; 7.02 MHz carrier), the so called 1 dB compression point is reached. For complex signals (more than one sound carrier), this point will shift to a higher value.
3. The mixer performs both a mixing and amplifying action (normal operation). The synthesizer is tuned to the 7.3 MHz incoming carrier.
4. The buffer output is sensitive to capacitive loading, therefore (capacitive) loads other than those present in the block diagram (see Fig.1) should be avoided.
5. As present at the mixer output (pin 5) in 'BPFTILT' test mode the actual VCO sensitivity is two times the given value because of the divide-by-two circuit between VCO output and mixer.
6. The required 4 MHz crystal can be omitted if this frequency is already available in the application. This signal source should be connected to pin 40, via a capacitor in series with a resistor R_{ext}. The minimum required AC current is 50 µA, determined by the resistors R_{int} and R_{ext} and the level of the 4 MHz AC voltage. The value of R_{int} is 700 Ω and the signal shape of the signal is not important.
7. Maximum THD of 0.5%; 8 V < V_{P3} < 13.2 V; 0 °C < T_{amb} < 70 °C. Measured at pins 34 and 30; NR = off; DEEM = flat.
8. Correction of output voltage is possible by correcting the volume level.
9. Measured at pins 37 and 27 with no electrolytic capacitors connected to these pins.

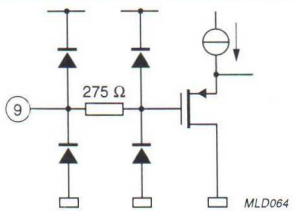
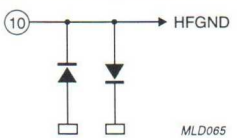
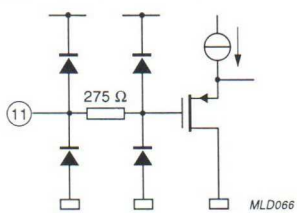
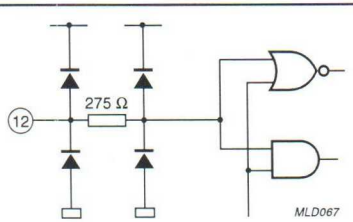
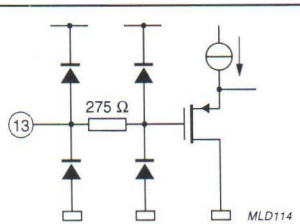
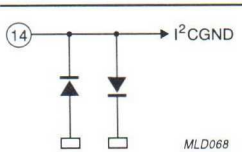
10. Input level of 0 dB; signal level in accordance with $\Delta f_{S1} = \Delta f_{S2} = 50$ kHz. At this input level, the NR response is equal for high and low frequencies (see Fig.4).
11. J17 de-emphasis includes +6 dB amplification (see Fig.5).
12. Both PLLs locked.

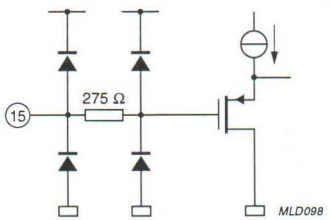
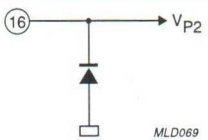
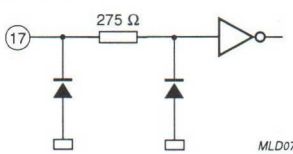
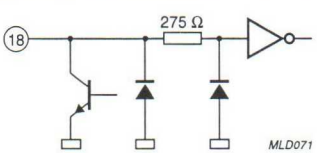
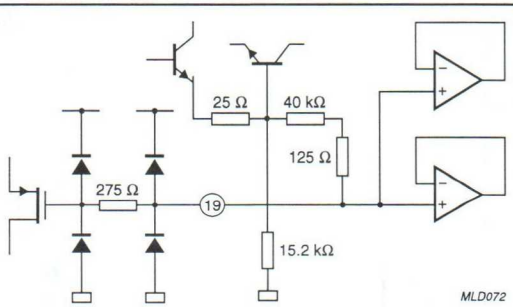
INTERNAL CIRCUITRY

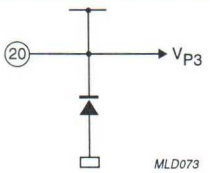
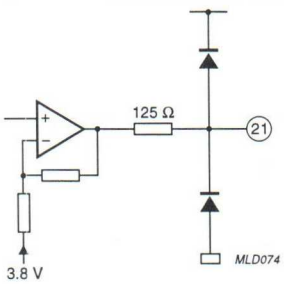
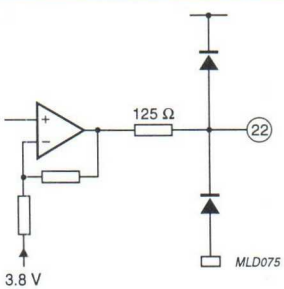
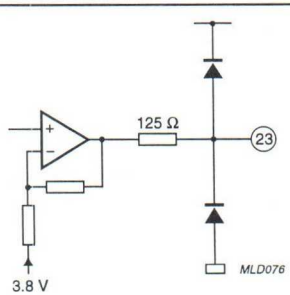
For description see Chapter "Pinning".

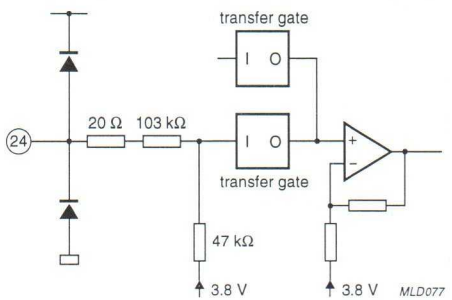
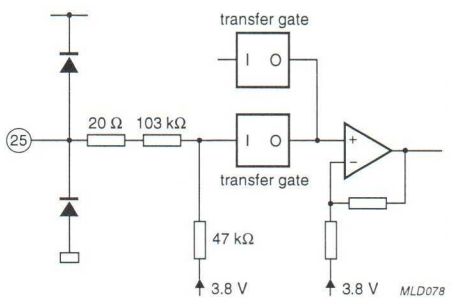
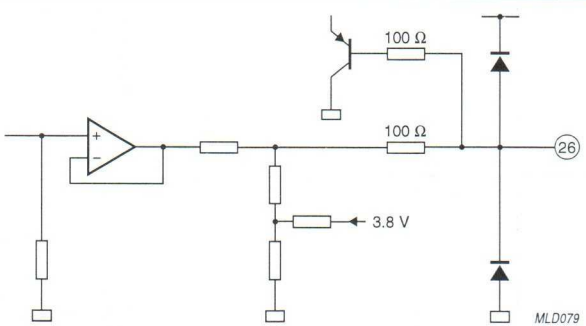
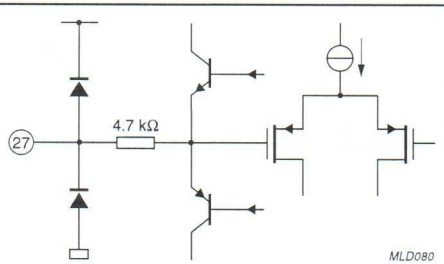
SYMBOL	PIN	EQUIVALENT CIRCUIT
$C_{DC\ R}$	1	
SLF	2	
BASEBAND IN	3	

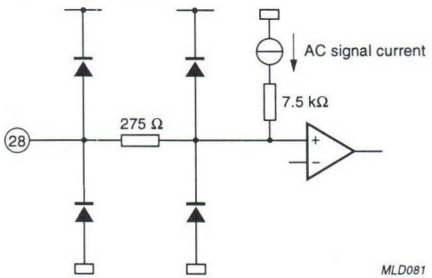
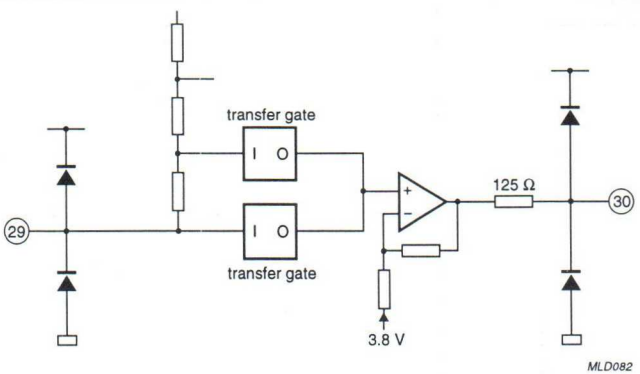
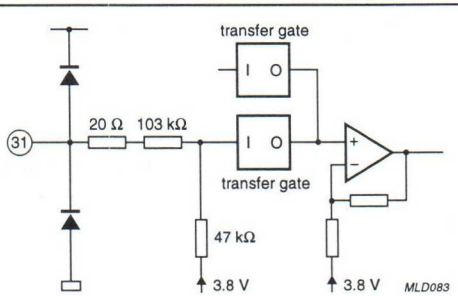
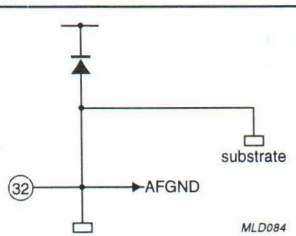
SYMBOL	PIN	EQUIVALENT CIRCUIT
V_{P1}	4	
IF OUT	5	
SYNGND	6	
IN-5	7	
IN-6	8	

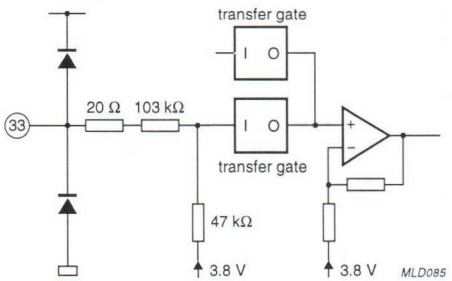
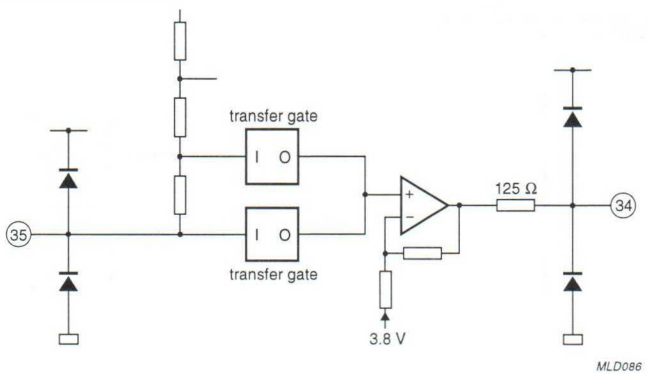
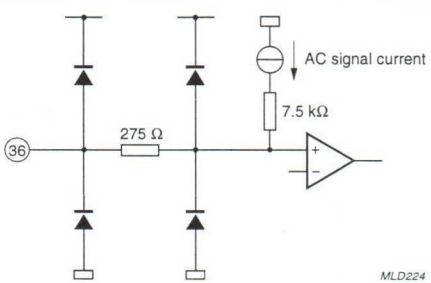
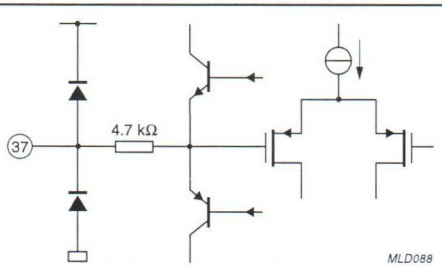
SYMBOL	PIN	EQUIVALENT CIRCUIT
IN-1	9	
HFGND	10	
IN-2	11	
ADD_{sel}	12	
IN-3	13	
I²CGND	14	

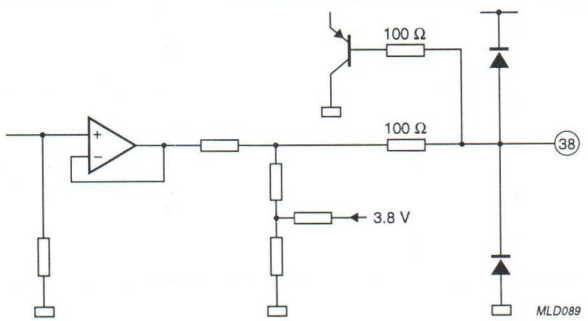
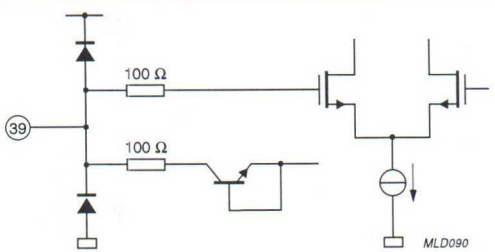
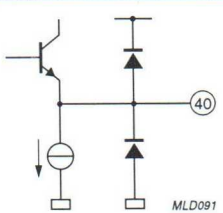
SYMBOL	PIN	EQUIVALENT CIRCUIT
IN-4	15	
V_{P2}	16	
SCL	17	
SDA	18	
V_{ref}	19	

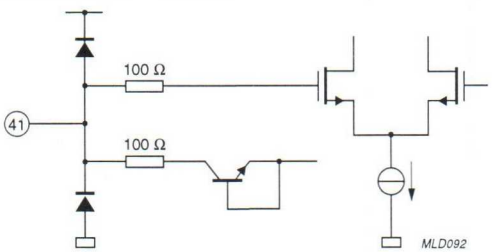
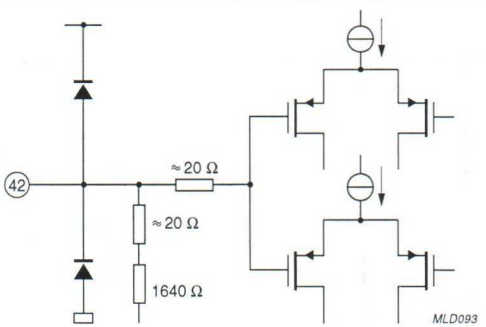
SYMBOL	PIN	EQUIVALENT CIRCUIT
V_{P3}	20	
O_M	21	
O_R	22	
O_L	23	

SYMBOL	PIN	EQUIVALENT CIRCUIT
EXT_R	24	
EXT_L	25	
$C_{ATT/REC\ R}$	26	
$RECT_R$	27	

SYMBOL	PIN	EQUIVALENT CIRCUIT
$C_{NR\,D\,R}$	28	
$C_{D\,R}$	29	
DEEM OUT R	30	
$C_{CL\,R}$	31	
AFGND	32	

SYMBOL	PIN	EQUIVALENT CIRCUIT
$C_{CL\,L}$	33	
DEEM OUT L	34	
$C_{D\,L}$	35	
$C_{NR\,D\,L}$	36	
$RECT_L$	37	

SYMBOL	PIN	EQUIVALENT CIRCUIT
$C_{ATT/REC\ L}$	38	
PRES DET R	39	
XTAL	40	

SYMBOL	PIN	EQUIVALENT CIRCUIT
PRES DET L	41	
$C_{DC\ L}$	42	

YUV 8-bit analog-to-digital interface TDA8753A

FEATURES

- Triple analog-to-digital converter
- 8-bit resolution
- Sampling rate up to 20 MHz
- Power dissipation of 500 mW (typical)
- Internal clamp functions
- 4 : 1 : 1 output data encoder
- Y binary output
- U, V two's complement outputs
- Sample rate converter permits programmable horizontal compression factors from 1 to 2
- Serial microcontroller interface
- TTL compatible inputs.

APPLICATIONS

- High-speed analog-to-digital conversion for video signal digitizing in 4 : 1 : 1 format
- 100 Hz improved definition TV for all formats (4/3, 16/9, 14/9 etc.).

GENERAL DESCRIPTION

The TDA8753A is a monolithic CMOS 8-bit video low-power analog-to-digital conversion interface for YUV signals. It converts the YUV analog input signal into 8-bit binary coded digital words in format 4 : 1 : 1 at a sampling rate of 20 MHz. All analog signal inputs are clamped. The device includes a digital sample rate converter for variable compression with a factor 1 to 2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
I_{DDA}	analog supply current		–	55	63	mA
I_{DDD}	digital supply current		–	45	55	mA
INL	integral non-linearity	f_{clk} = 16 MHz; ramp input	–	±0.75	–	LSB
DLE	differential non-linearity	f_{clk} = 16 MHz; ramp input; Y	–	±0.5	0.75	LSB
		f_{clk} = 16 MHz; ramp input; U and V	–	±0.6	±0.9	LSB
SNR	signal-to-noise ratio without harmonics	note 1	43	–	–	dB
f_{clk}	maximum conversion rate		20	–	–	MHz
P_{tot}	total power dissipation	note 2	–	500	650	mW

Notes

1. The signal-to-noise ratio without harmonics is measured using a 16 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels).
2. The external resistor (between V_{DDA} and I_{ref}) fixing internal static currents influences P_{tot}. The value of the resistor should be 5.6 kΩ (5%).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8753A	SDIP42	plastic shrink dual in-line package; 42 leads; (600 mil)	SOT270-1

BLOCK DIAGRAM

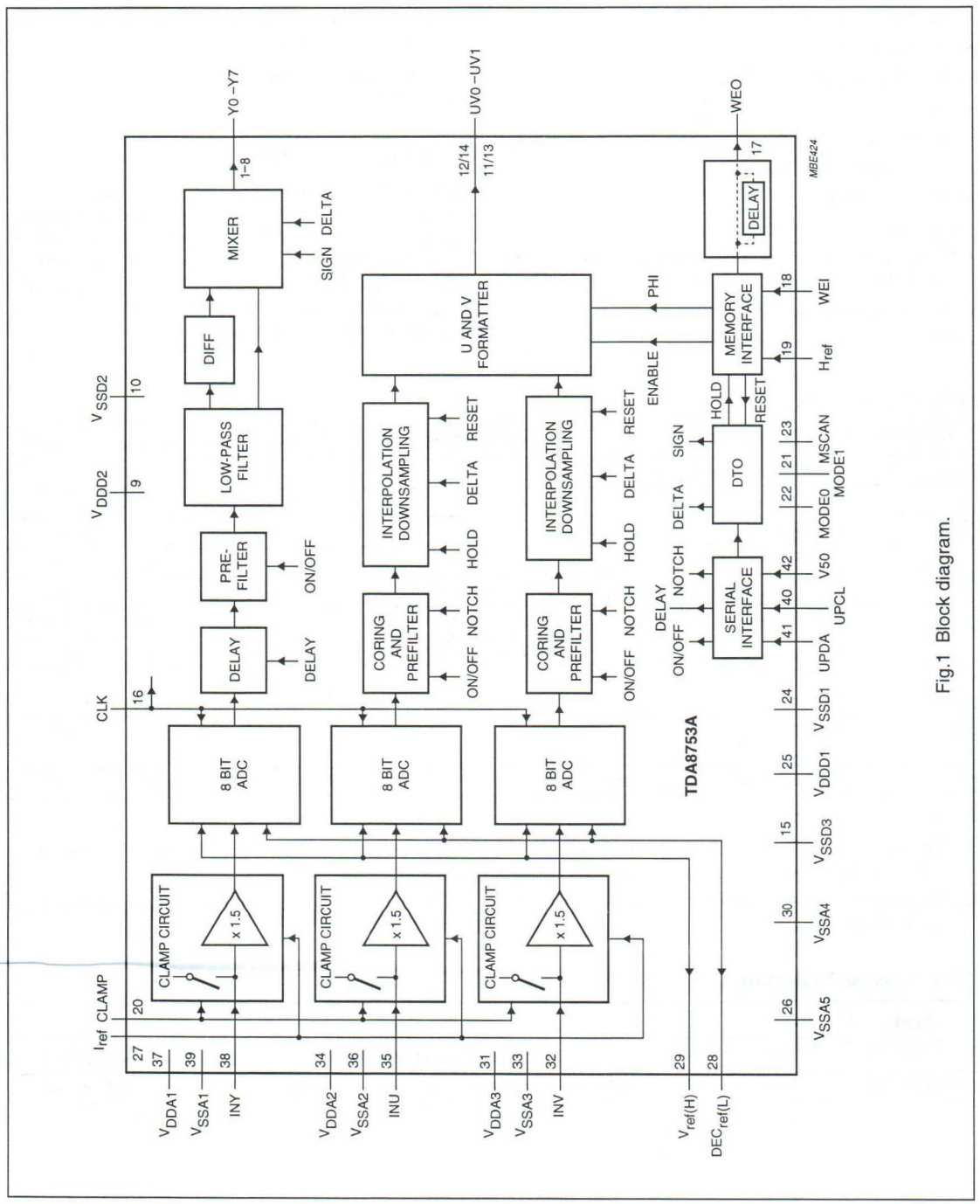


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
Y7	1	Y data output, bit 7 (MSB)
Y6	2	Y data output, bit 6
Y5	3	Y data output, bit 5
Y4	4	Y data output, bit 4
Y3	5	Y data output, bit 3
Y2	6	Y data output, bit 2
Y1	7	Y data output, bit 1
Y0	8	Y data output, bit 0 (LSB)
V_{DDD2}	9	digital supply voltage 2, (+5 V)
V_{SSD2}	10	digital ground 2
U1	11	U data output, bit 1 (n)
U0	12	U data output, bit 0 (n – 1)
V1	13	V data output, bit 1 (n)
V0	14	V data output, bit 0 (n – 1)
V_{SSD3}	15	digital ground 3
CLK	16	clock input
WEO	17	write enable output
WEI	18	write enable input
H_{ref}	19	horizontal reference signal input
CLAMP	20	clamp control input
MODE1	21	test mode select
MODE0	22	test mode select
MSCAN	23	test pin
V_{SSD1}	24	digital ground 1
V_{DDD1}	25	digital supply voltage 1 (+5 V)
V_{SSA5}	26	analog ground 5
I_{ref}	27	current level reference
$DEC_{ref(L)}$	28	decoupling output from reference LOW
$V_{ref(H)}$	29	reference voltage input (HIGH)
V_{SSA4}	30	analog ground 4
V_{DDD3}	31	analog supply voltage 3, (+5 V)
INV	32	V analog voltage input
V_{SSA3}	33	analog ground 3
V_{DDA2}	34	analog supply voltage 2 (+5 V)
INU	35	U analog voltage input
V_{SSA2}	36	analog ground 2
V_{DDA1}	37	analog supply voltage 1 (+5 V)
INY	38	Y analog voltage input
V_{SSA1}	39	analog ground 1
UPCL	40	control clock input
UPDA	41	serial interface data input
V50	42	data execution input

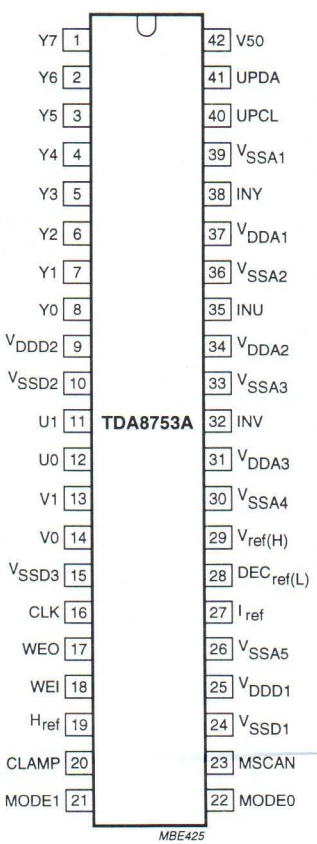


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog-to-digital converter

The TDA8753 implements 3 independent CMOS 8-bit analog-to-digital converters. The converters use a multi-step approach with offset compensated comparators.

Clamping

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INY, INV and INU are switched to on-chip clamping levels during an active pulse on the clamp input CLP.The clamping level in the Y channel is code level 16. The clamping level in the U/V channel is code level 128 (output code 0 in the 2's complement description) see Tables 3 and 4.

Sample rate converter

A sample rate converter is integrated in the TDA8753A to facilitate programming of the horizontal aspect ratio which can be varied from a factor 1 to 2. This includes conversion from 16/9 to 14/9 and 4/3. In the U/V channel a linear interpolation is sufficient because of the four times oversampling.

Discrete time oscillator (DTO)

A discrete time oscillator is used to calculate for every sample of the phase delay that is needed for a given compression factor.

Serial interface (SIO)

All controls are sent to the TDA8753A via a serial microprocessor interface. Data from this interface will be made active at the vertical input pulse V50.

The TDA8753A has three addressable control registers which can be loaded via the signals UPDA and UPCL. The format of this bus is fixed according to mode 0 of the 8051 family UART at 1 Mbaud (8 bits are transmitted, LSB first).

Serial interface protocol

POWER-ON STATE

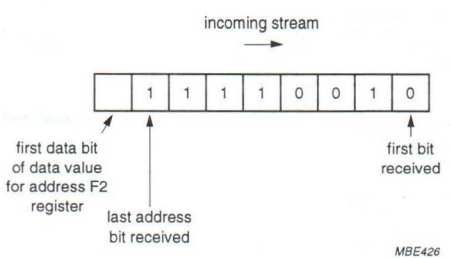
When powered up the SIO is in an unknown state and all data in the registers is random. When signals are applied to UPCL and UPDA in this state, the behaviour is unpredictable. The only way to exit from this state to a known state is apply a V50 signal to the TDA8753A.

INITIALIZATION STATE

From power-on or any other state, the INIT state is entered (at the latest) one TDA8753A clock period after the end of the V50 HIGH state. In this state the F0, F1 and F2 TDA8753A registers are loaded with the values that are in the corresponding line buffers BF0, BF1 and BF2.The first time V50 is issued after power-on, this data is unknown. After a rising UPCL edge has been detected, the address reception state is entered.

ADDRESS RECEPTION STATE

Bits are counted at each rising UPCL edge. The next 8 bits received on UPDA line are considered as address bits. The address reception is illustrated in Fig.3.



(in this example address received is F2 hex)

Fig.3 Address reception.

The TDA8753A registers have address F0, F1 and F2 hexadecimal notation. Whenever the received address (decoded on the first 8 bits received) is one of these, the event is recorded in such a way that the next data received by the TDA8753A will be captured in the line buffer BF0, BF1 and BF2 respectively.

When 8 bits have been received, the data reception state is entered. The address reception state can also be exited at any time when V50 goes HIGH. The F0, F1 and F2 registers may not be loaded properly if there is some activity in progress on the incoming line.

DATA RECEPTION STATE

The next 8 bits are considered as data bits according to the format of Fig.4.

When 8 data bits have been received, the data is recorded in the BF0, BF1 or BF2 line buffers if the previous address recorded was F0 hex, F1 hex or F2 hex respectively. The bit count is then reset to zero and the address reception state is entered. This state may be ended any time when V50 goes HIGH but in that condition F0, F1 and F2 registers may not be loaded properly.

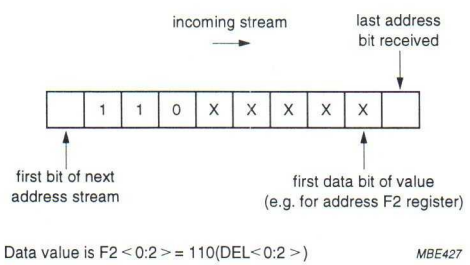


Fig.4 Data reception.

Table 1 Data allocation

ADDRESS	PARAMETER	FUNCTION	NUMBER OF BITS	BIT POSITION
F0 Hex	CF	compression factor value will be (1 + cf/255) which results in a range from 1 to 2	8	7:0
F1 Hex	UV_CORING	coring definition in U and V channels; see Table 5	2	1:0
	UV_FILTER_TYPE	notch filter selection in U and V channels (0 = 4 MHz; 1 = 2 MHz)	1	2
	PRE_ON	luminance prefilter active	1	3
	NOTCH_ON	notch prefilter active	1	4
	DTO_ON	DTO control	1	5
	SEL_DTO_RES	select DTO reset (0 = WE; 1 = Href)	1	6
	WEO_DEL_SEL	select delay in WEO		
F2 Hex	Y_VAR_DELAY	luminance delay compression (see Table 5)		
		not used; load 0	5	7:2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		−0.3	6.5	V
V_{DDA}	analog supply voltage		−0.3	6.5	V
$V_{DDA} - V_{DDD}$	supply voltage difference		−0.5	+0.5	V
V_I	input voltage	referenced to AGND	–	V_{DDA}	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	V_{DDD}	V
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	45	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.75$ to 5.25 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.1$ to +0.1 V (see note 1); $V_{ref(H)} = 2.38$ V; $f_{clk} = 20$ MHz with 50% duty cycle; 5.6 kΩ (5%) connected between I_{ref} and V_{DDA}; CL = 15 pF; $T_{amb} = 0$ to 70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
I_{DDA}	analog supply current		–	55	63	mA
I_{DDD}	digital supply current		–	45	55	mA
Digital inputs and clock input (WE, H_{ref}, CLAMP, MODE1, MODE0, SCCL, UPCL, UPDA and V50)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
C_I	input capacitance		–	7	15	pF
$\lvert I_{LI} \rvert$	input leakage current	$V_I = 0$ V; $V_{DDD} = 5$ V	−10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp and references [I_{ref}, $DEC_{ref(L)}$ and $V_{ref(H)}$]						
A_{CL}	clamping accuracy	Y	−4	−	+1	LSB
		U and V	−1	−	+1	LSB
C_{clamp}	serial clamp capacitor		10	22	−	nF
Z_{ADC}	internal impedance between pin 29 and V_{SSA}		−	420	−	Ω
$V_{ref(H)}$	converter reference HIGH, applied to pin 29		−	2.38	−	V
$V_{DECref(L)}$	converter reference voltage LOW, applied to pin 28	$V_{ref(H)}$ = 2.38 V	−	0.39	−	V
Y analog input (INY); $V_{ref(H)}$ = 2.38 V, $V_{ref(L)}$ = 0.39 V; see Table 4						
$V_{i(p-p)}$	input voltage, full range (peak-to-peak value)	ramp input	−	1.26	−	V
I_i	input current	clamp non-active	−	5	100	μA
C_I	input capacitance		−	−	15	pF
U,V analog inputs (INU and INV); $V_{ref(H)}$ = 2.38 V, $V_{ref(L)}$ = 0.39 V; see Table 4						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	ramp input	−	1.26	−	V
I_i	input current	clamp non-active	−	5	100	μA
C_I	input capacitance		−	−	15	pF
Inputs isolation						
α_{act}	crosstalk between INY, INU and INV		−	−	−50	dB
Digital outputs (Y0 to Y7, U1, U0, V1 and V0); see Table 3						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	−	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = 0.4 mA	2.4	−	V_{DDD}	V
Analog signal processing (f_{CLK} = 20 MHz)						
G_{diff}	differential gain	note 2	−	1.5	−	%
Φ_{diff}	differential phase	note 2	−	1.0	−	deg
f_{all}	harmonics (full scale) all components	note 3	−	−50	−	dB
SVR	supply voltage ripple rejection	note 4	−	2	−	%/V
B	bandwidth	−1 dB; note 5	−	tbf	−	MHz
		−3 dB; note 5	−	tbf	−	MHz
Transfer function (f_{clk} = 16 MHz)						
INL	integral non-linearity	ramp input	−	±0.75	-	LSB
DNL	differential non-linearity	ramp input; Y	−	±0.5	±0.75	LSB
		ramp input; U and V	−	±0.6	±0.9	LSB
SNR	signal-to-noise ratio without harmonics	note 6	45	−	−	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 20 MHz; C_L = 15 pF); see Figs 7 and 10; note 7						
f_{clk}	maximum input clock frequency		20	–	–	MHz
$t_{CP(H)}$	clock pulse width HIGH		22	–	–	ns
$t_{CP(L)}$	clock pulse width LOW		22	–	–	ns
t_{ds}	sampling delay		–	4	–	ns
t_{hd}	output hold time		7	–	–	ns
t_d	output delay time		–	–	32	ns
t_{CLKr}	clock rise time		3	5	–	ns
t_{CLKf}	clock fall time		3	5	–	ns
$t_{su;Href}$	HREF set-up time		7	–	–	ns
$t_{hd;Href}$	HREF hold time		3	–	–	ns
t_r	data output rise time		–	10	–	ns
t_f	data output fall time		–	10	–	ns
t_{CLP}	minimum time for active clamp pulse width		2.3	2.5	–	µs
$t_{su;WE}$	WE set-up time		7	–	–	ns
$t_{hd;WE}$	WE hold time		3	–	–	ns
t_{XLXL}	serial port clock cycle time	f_{xtal} = 12 MHz	1	–	–	µs
t_{QVXH}	output data set-up to rising edge of clock		700	–	–	ns
t_{XHQH}	output data hold time after rising edge of clock		50	–	–	ns
t_W	V50 pulse duration		2	–	–	ms
t_{VC}	V50 to clock time		2	–	–	ms
Sample rate converter (f_{clk} = 20 MHz)						
ΦY	Y phase accuracy	f_{iY} = 0 to 5 MHz	–	±1	–	ns
FUV	UV phase accuracy	f_{iUV} = 0 to 1.5 MHz	–	±4	–	ns
Y_{fr}	Y frequency response	f_{iY} = 0 to 5 MHz	–	±0.5	–	dB
UV_{fr}	UV frequency response	f_{iUV} = 0 to 1.5 MHz	–	±0.5	–	dB
Y_{step}	Y step size		–	1	–	ns
UV_{step}	UV step size		–	4	–	ns

Notes to the Characteristics

1. V_{DDA} and V_{DDD} should be supplied from the same power supply and decoupled separately.
2. Measurement carried out using video amplifier type VM700A, where the video analog signal (Y channel) is reconstructed via the DAC.
3. The input conditions are related as follows:
   Y – $V_{i(p-p)}$ = 1.26 V, f_i = 4.43 MHz
   U and V – $V_{i(p-p)}$ = 1.26 V, f_i = 1.5 MHz.
4. Supply voltage ripple rejection: SVR; relative variation of the full-scale range of analog input for a supply voltage variation of 0.5 V. SVR = $[\Delta (V_{I(0)} - V_{I(255)}] / [V_{I(o)} - V_{I(255)}] / \Delta V_{DDA}$.
5. The –1 dB bandwidth is the frequency value for which the analog reconstructed (glitch-free) output signal is compressed in term of number of codes, by –1 dB (respectively for –3 dB bandwidth).
6. The signal-to-noise ratio without harmonics is measured under a 20 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels).
7. Output data acquisition: Output data is available after the maximum delay of t_d.

Table 2 Mode selection.

MODE1	MODE0	MODE
0	0	normal configuration

Table 3 Output data coding.

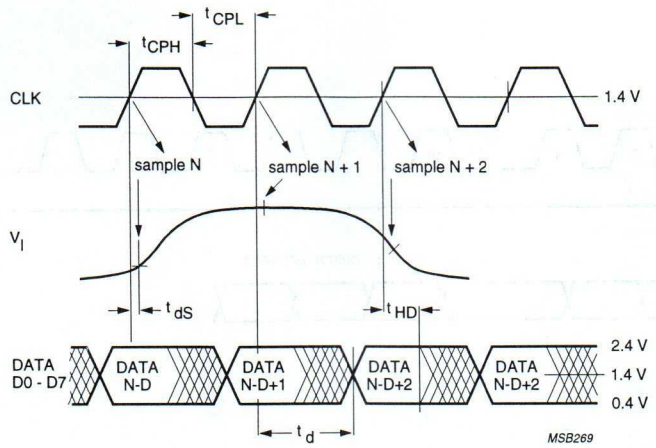
OUTPUT PORT	BIT	OUTPUT DATA			
Y	Y7	Y_07	Y_17	Y_27	Y_37
	Y6	Y_06	Y_16	Y_26	Y_36
	Y5	Y_05	Y_15	Y_25	Y_35
	Y4	Y_04	Y_14	Y_24	Y_34
	Y3	Y_03	Y_13	Y_23	Y_33
	Y2	Y_02	Y_12	Y_22	Y_32
	Y1	Y_01	Y_11	Y_21	Y_31
	Y0	Y_00	Y_10	Y_20	Y_30
U	U1	$\overline{U}_07$	U_05	U_03	U_01
	U0	U_06	U_04	U_02	U_00
V	V1	$\overline{V}_07$	V_05	V_03	V_01
	V0	V_06	V_04	V_02	V_00

Table 4 Internal ADC data coding as a function of the analog input

STEP	INPUT VOLTAGE	INTERNAL BINARY OUTPUTS	REMARKS
Underflow	<0.26	00000000	
0	0.26	00000000	$V_{DECref(L)}$ /1.5
1	-	00000001	
....	....	.....	
16	0.34	00010000	clamp level of Y channel
....	....	.....	
128	0.89	10000000	clamp level of U and V channels
....	....	.....	
254	–	11111110	
255	1.52	11111111	$V_{ref(H)}$ – 0.1 V/1.5
Overflow	> 1.52	11111111	

Table 5 Coring and luminance delay

UV_CORING		INTERNAL CORING CORRECTION IN U AND V CHANNELS (AROUND CODE 128 LEVEL)	Y_VAR_DELAY		INTERNAL DELAY FOR Y PATH AT PREFILTER INPUT (CLOCK PULSE)
F1:1	F1:0		F2:1	F2:0	
0	0	coring off	0	0	0
0	1	+1/–1	0	1	1
1	0	+1/–0	1	0	2
1	1	+2/–1	1	1	3



The value D is equal to 15.

Fig.5 Timing diagram.

TIMING

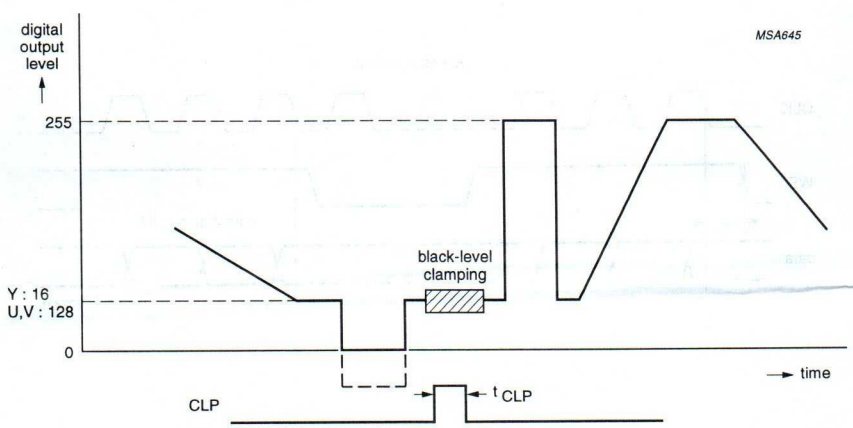
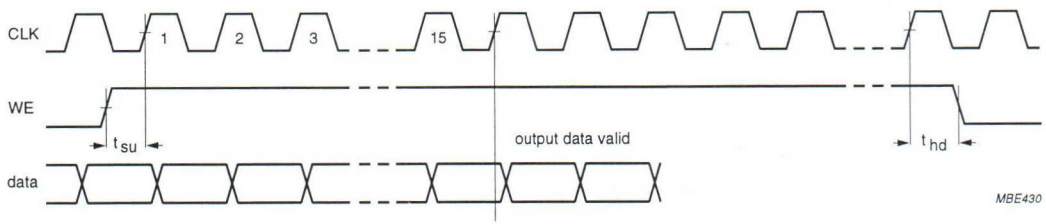
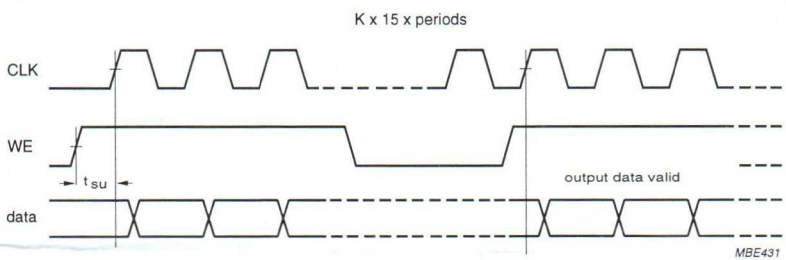


Fig.6 Clamp control timing.



The output data is valid 15 clock periods after WE goes HIGH.

Fig.7 Set-up and hold time definition; WE signal.



When the WE period is a whole multiple of 15 clock periods, the output data is valid without any clock delay.
The internal circuit always gives an internal 15 clock period as illustrated in Fig.7.

Fig.8 Timing diagram; WE signal.

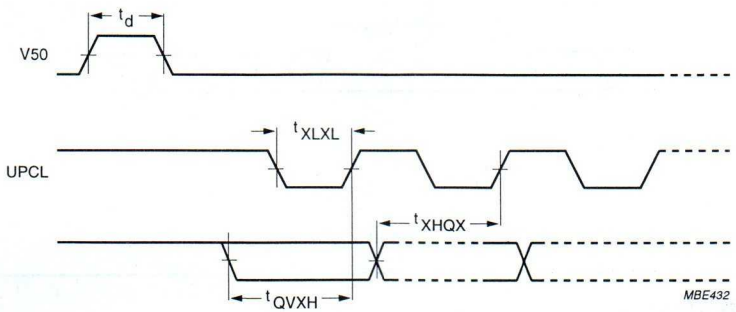


Fig.9 Timing of the asynchronous interface.

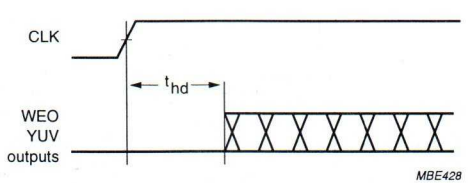


Fig.10 Outputs hold time.

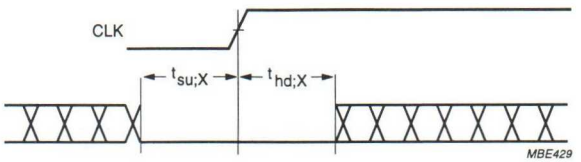


Fig.11 Digital inputs WE and H_{REF}; set-up and hold time.

INTERNAL PIN CONFIGURATION

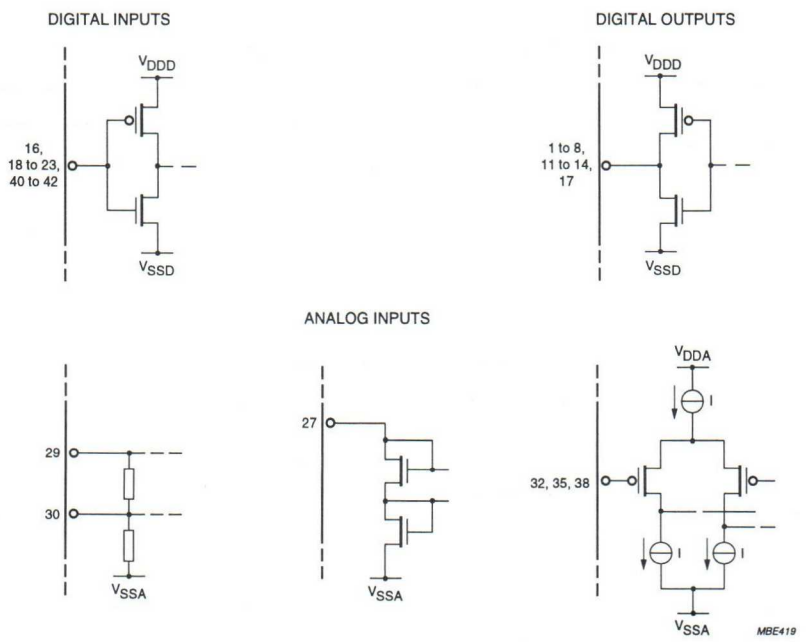
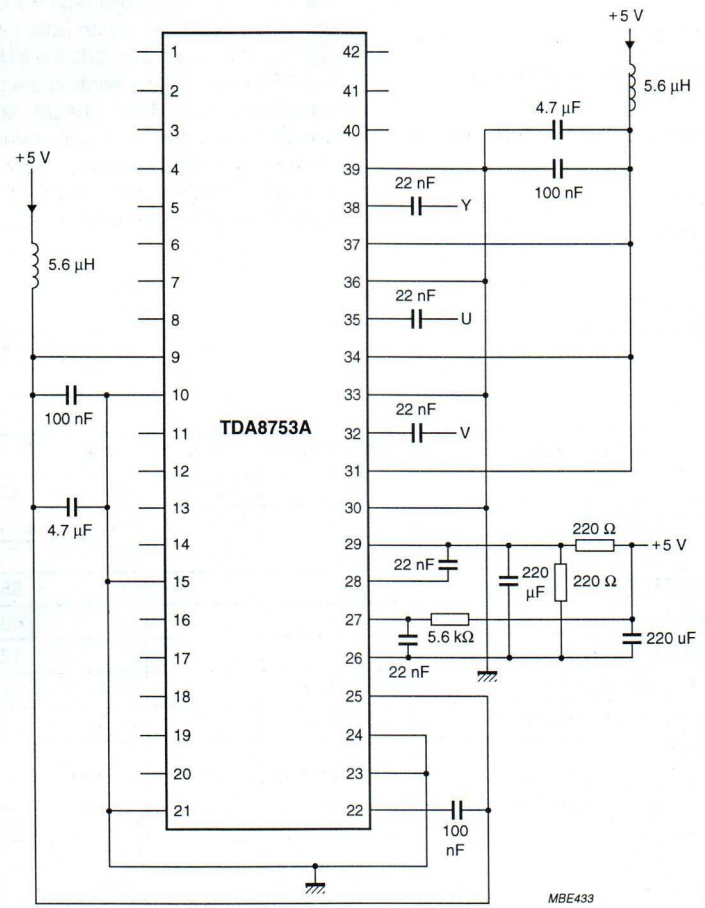


Fig.12 Internal pin configuration.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled. Test pins MODE1, MODE0 and MSCAN must be connected to digital ground.

Fig.13 Application diagram.

YUV 8-bit video low-power analog-to-digital interface

TDA8755

FEATURES

- 8-bit resolution
- Sampling rate up to 20 MHz
- TTL compatible digital inputs
- 3-state TTL outputs
- U, V two's complement outputs
- Y binary output
- Power dissipation of 550 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- High signal-to-noise ratio over a large analog input frequency range
- Track-and-hold included
- Clamp functions included
- UV multiplexed ADC
- 4 : 1 : 1 output data encoder
- Stable voltage regulator included.

APPLICATIONS

- High speed analog-to-digital conversion for video signal digitizing
- 100 Hz improved definition TV (IDTV).

GENERAL DESCRIPTION

The TDA8755 is a bipolar 8-bit video low-power analog-to-digital conversion (ADC) interface for YUV signals. The device converts the YUV analog input signal into 8-bit coded digital words in a 4 : 1 : 1 format at a sampling rate of 20 MHz. The U/V signals are converted in a multiplexed manner. All analog signal inputs are digitally clamped and a fast precharge is provided for start-up. All digital inputs and outputs are TTL compatible. Frame synchronization is supported in a multiplexed manner.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	46	55	mA
I_{CCD}	digital supply current		–	55	66	mA
I_{CCO}	output stages supply current		–	9	12	mA
INL	DC integral non-linearity	f_{clk} = 2 MHz	–	±0.4	±1	LSB
DNL	DC differential non-linearity	f_{clk} = 2 MHz	–	±0.3	±0.5	LSB
EB	effective bits		–	7.1	–	bits
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	550	700	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8755T	32	SO32L	plastic	SOT287-1

BLOCK DIAGRAM

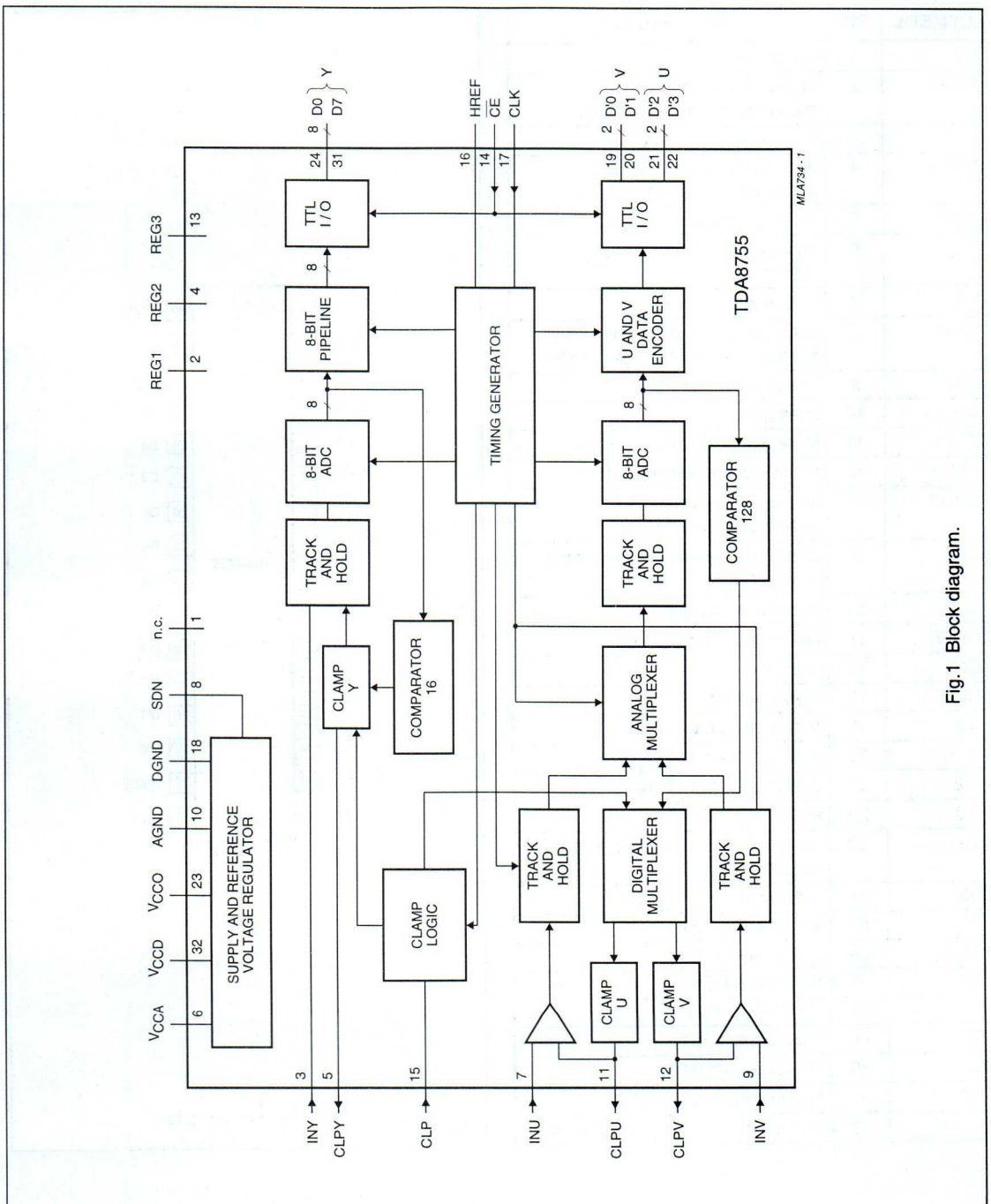


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REG1	2	decoupling input (internal stabilization loop decoupling)
INY	3	Y analog voltage input
REG2	4	decoupling input (internal stabilization loop decoupling)
CLPY	5	Y clamp capacitor connection
V_{CCA}	6	analog positive supply voltage (+5 V)
INU	7	U analog voltage input
SDN	8	stabilizer decoupling node and analog reference voltage (+3.35 V)
INV	9	V analog voltage input
AGND	10	analog ground
CLPU	11	U clamp capacitor connection
CLPV	12	V clamp capacitor connection
REG3	13	decoupling input (internal stabilization loop decoupling)
$\overline{CE}$	14	chip enable input (TTL level input active LOW)
CLP	15	clamp control input
HREF	16	horizontal reference signal
CLK	17	clock input
DGND	18	digital ground
D'0	19	V data output; bit 0 (n–1)
D'1	20	V data output; bit 1 (n)
D'2	21	U data output; bit 0 (n–1)
D'3	22	U data output; bit 1 (n)
V_{CCO}	23	positive supply voltage for output stages (+5 V)
D0	24	Y data output; bit 0 (LSB)
D1	25	Y data output; bit 1
D2	26	Y data output; bit 2
D3	27	Y data output; bit 3
D4	28	Y data output; bit 4
D5	29	Y data output; bit 5
D6	30	Y data output; bit 6
D7	31	Y data output; bit 7 (MSB)
V_{CCD}	32	digital positive supply voltage (+5 V)

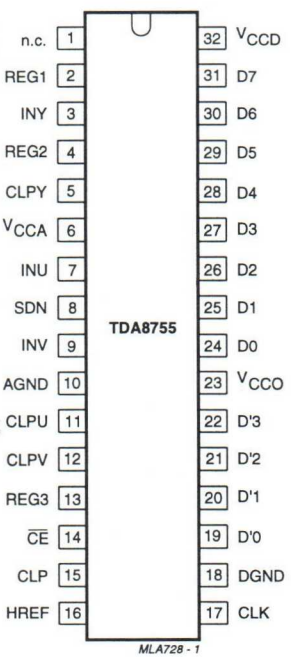


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{CCO}	output stages supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−	+5.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	+6	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

$V_{CCA} = V_6$ to V_{10} = 4.75 to 5.25 V; $V_{CCD} = V_{32}$ to V_{18} = 4.75 to 5.25 V; $V_{CCO} = V_{23}$ to V_{18} = 4.75 to 5.25 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.25 to +0.25 V; V_{CCO} to V_{CCD} = −0.25 to +0.25 V; V_{CCA} to V_{CCO} = −0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	46	55	mA
I_{CCD}	digital supply current		–	55	66	mA
I_{CCO}	output stages supply current		–	9	12	mA
Inputs						
CLK (PIN 17)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{clk} = 20 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 20 MHz	–	4.5	–	pF
$\overline{CE}$, CLP AND HREF (PINS 14 TO 16)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
CLPY (PIN 5)						
V_5	clamp voltage for 16 output code		–	3.725	–	V
I_5	clamp output current		–	±50	–	µA
CLPU AND CLPV (PINS 11 AND 12)						
$V_{11, 12}$	clamp voltage for 128 output code		–	3.30	–	V
$I_{11, 12}$	clamp output current		–	±50	–	µA
INY (PIN 3)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 4.43 MHz	0.93	1.0	1.07	V
Z_I	input impedance	f_i = 6 MHz	–	30	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INU AND INV (PINS 7 AND 9)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 1.5 MHz	0.93	1.03	1.13	V
Z_I	input impedance	f_i = 2 MHz	–	30	–	kΩ
C_I	input capacitance	f_i = 2 MHz	–	1	–	pF
INPUTS ISOLATION						
α_{ct}	crosstalk between Y, U and V		–	–55	–50	dB
Outputs						
SDN (PIN 8)						
V_{ref}	reference voltage		–	3.32	–	V
V_{REG}	line regulation	4.75 V ≤ V_{CCA} ≤ 5.25 V	–	4.0	–	mV
I_L	load current		–2	–	–	mA
DIGITAL OUTPUTS D0 TO D7 AND D'0 TO D'3 (PINS 24 TO 31 AND 19 TO 22)						
V_{OL}	LOW level output voltage	I_O = 0.4 mA	0	–	0.4	V
		I_O = 1.5 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
$f_{clk(min)}$	minimum clock frequency		–	–	2.0	MHz
t_{CPH}	clock pulse width HIGH		20	–	–	ns
t_{CPL}	clock pulse width LOW		20	–	–	ns
Analog signal processing (f_{clk} = 20 MHz; 50% clock duty factor)						
G_{diff}	differential gain	note 1; see Fig.8	–	2	–	%
φ_{diff}	differential phase	note 1; see Fig.8	–	3	–	deg
f_1	fundamental harmonics (full-scale)	note 2	–	–	0	dB
f_{all}	harmonics (full-scale), all components	note 2; see Fig.10	–	–54	–	dB
SVRR1	supply voltage ripple rejection 1	note 3	–	–40	–	dB
SVRR2	supply voltage ripple rejection 2	note 3	–	1.0	–	%/V
Transfer function (50% clock duty factor)						
INL	DC integral non-linearity	f_{clk} = 2 MHz	–	±0.4	±1.0	LSB
DNL	DC differential non-linearity	f_{clk} = 2 MHz	–	±0.3	±0.5	LSB
AILE	AC integral non-linearity	note 4	–	±1.0	±2.0	LSB
EB	effective bits	note 5; Fig.10	–	7.1	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 20 MHz); note 6; see Figs 3 to 7						
t_{ds}	sampling delay time		–	1	–	ns
t_h	output hold time		7	–	–	ns
t_d	output delay time		–	33	42	ns
t_{dZH}	3-state output delay time	enable-to-HIGH	–	10	14	ns
t_{dZL}	3-state output delay time	enable-to-LOW	–	10	14	ns
t_{dHZ}	3-state output delay time	disable-to-HIGH	–	8	11	ns
t_{dLZ}	3-state output delay time	disable-to-LOW	–	4	6	ns
t_r	clock rise time		3	5	–	ns
t_f	clock fall time		3	5	–	ns
t_{su}	HREF set-up time		7	–	–	ns
t_h	HREF hold time		3	–	–	ns
t_r	data output rise time		–	12	–	ns
t_f	data output fall time		–	16	–	ns
t_{CLP}	minimum time for active clamp	note 7; see Fig.9	3	–	–	µs

Notes

1. Low frequency ramp signal ($V_{I(p-p)}$ = full-scale and 64 µs period) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.25 full-scale, f_i = maximum permitted frequency) at the input.
2. The input conditions are related as follows:
   a) Y channel: $V_{I(p-p)}$ = 1.0 V; f_i = 4.43 MHz
   b) U/V channel: $V_{I(p-p)}$ = 1.0 V; f_i = 1.5 MHz.
3. Supply voltage ripple rejection:
   a) SVRR1 is the variation of the input voltage producing output code 127 (code 15) for supply voltage variation of 0.5 V:

$$SVRR1 = 20 \log \frac{\Delta V_{I(127)}}{\Delta V_{CCA}}$$

   b) SVRR2 is the relative variation of the full-scale range of analog input for a supply voltage variation of 0.5 V:

$$SVVR2 = \frac{\Delta (V_{I(0)} - V_{I(255)})}{V_{I(0)} - V_{I(255)}} \times \frac{1}{\Delta V_{CCA}}$$

4. Full-scale sinewave (f_i = 4.43 MHz for Y and f_i = 1.5 MHz for U and V; f_{clk} = 20 MHz).
5. The number of effective bits is measured using a 20 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels). This value is obtained via a Fast Fourier Transform (FFT) treatment taking 4 × T_{clk} (clock periods) acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).

   Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
6. Output data acquisition is available after the maximum delay time of t_d.
7. U and V output data is not valid during t_{CLP}.

Table 1 Mode selection

$\overline{CE}$	D7 TO D0; D'3 TO D'0
1	high impedance
0	active; binary

Table 2 Output data coding

OUTPUT PORT	BIT	OUTPUT DATA			
Y	D7	Y_07	Y_17	Y_27	Y_37
	D6	Y_06	Y_16	Y_26	Y_36
	D5	Y_05	Y_15	Y_25	Y_35
	D4	Y_04	Y_14	Y_24	Y_34
	D3	Y_03	Y_13	Y_23	Y_33
	D2	Y_02	Y_12	Y_22	Y_32
	D1	Y_01	Y_11	Y_21	Y_31
	D0	Y_00	Y_10	Y_20	Y_30
U	D'3	$\overline{U}_07$	U_05	U_03	U_01
	D'2	U_06	U_04	U_02	U_00
V	D'1	$\overline{V}_07$	V_05	V_03	V_01
	D'0	V_06	V_04	V_02	V_00

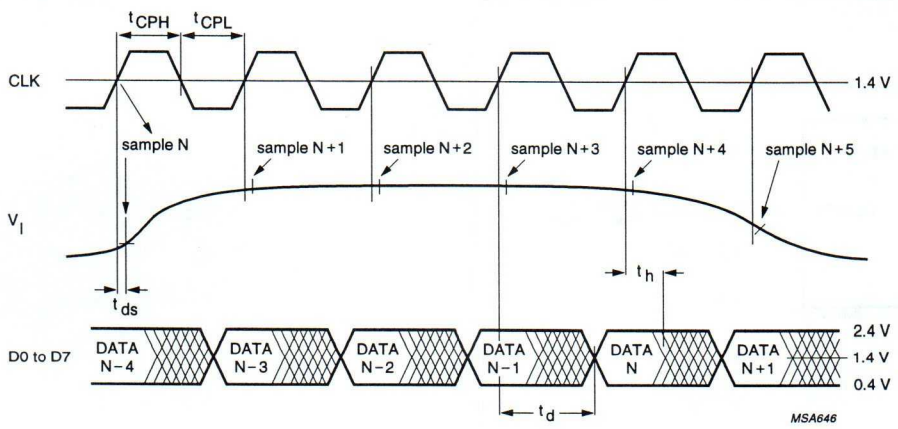
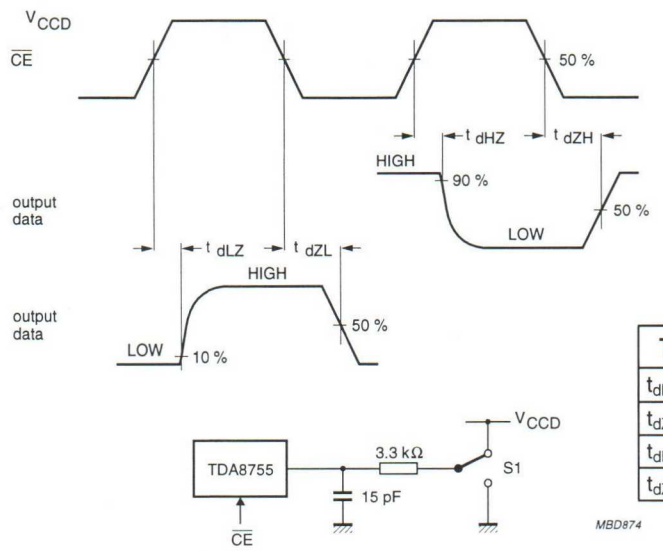


Fig.3 Timing diagram (INY signal).



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

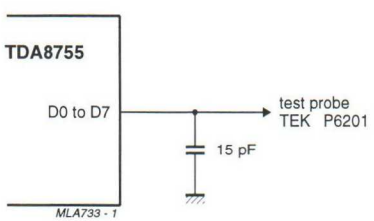
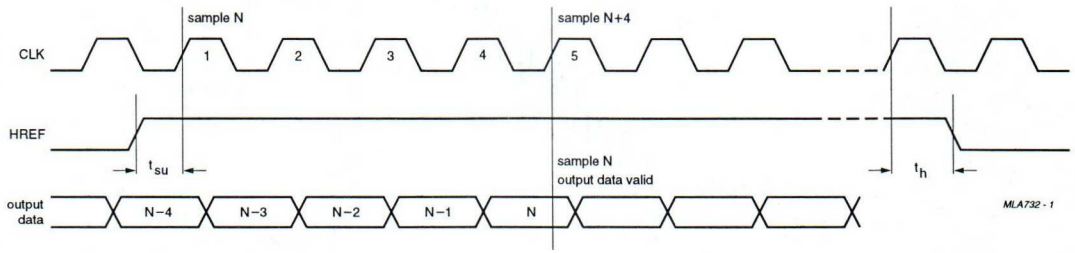
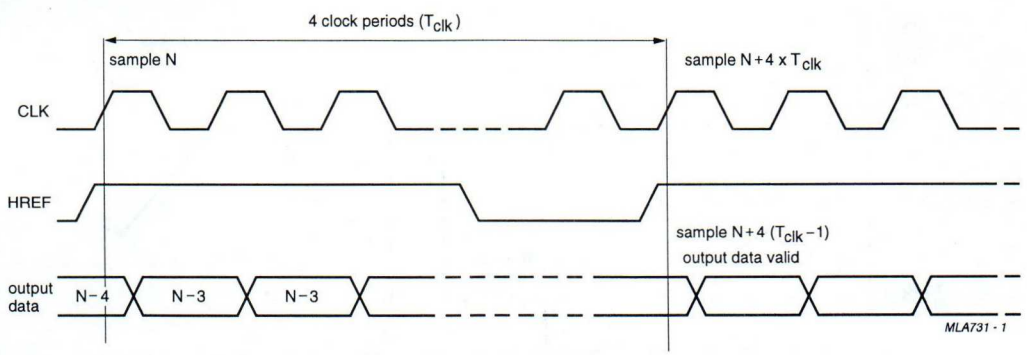


Fig.5 Load circuit for the 3-state output timing measurement.



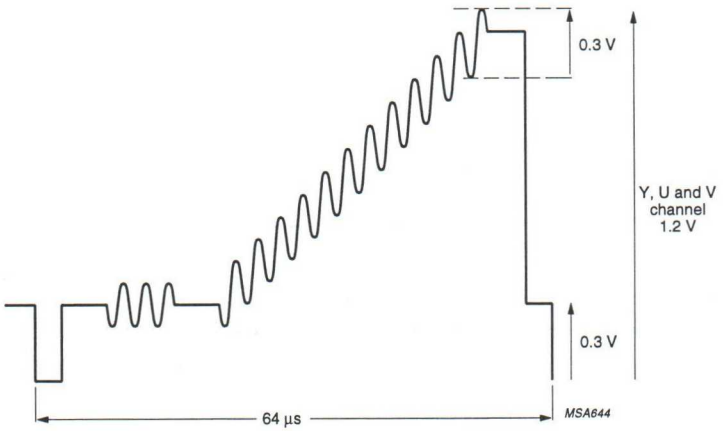
The output data is valid 4 clock periods after HREF goes HIGH.

Fig.6 Timing definition for set-up and hold times (HREF signal).



When the HREF period is a multiple of 4 clock periods, the output data is valid without any clock delay. The internal circuit always gives an internal delay of 4 clock periods as illustrated in Fig.6.

Fig.7 Timing diagram (HREF signal).



Y channel = 4.43 MHz sinewave.
U, V channel = 1.5 MHz sinewave.

Fig.8 Input test signal for differential gain and phase measurements.

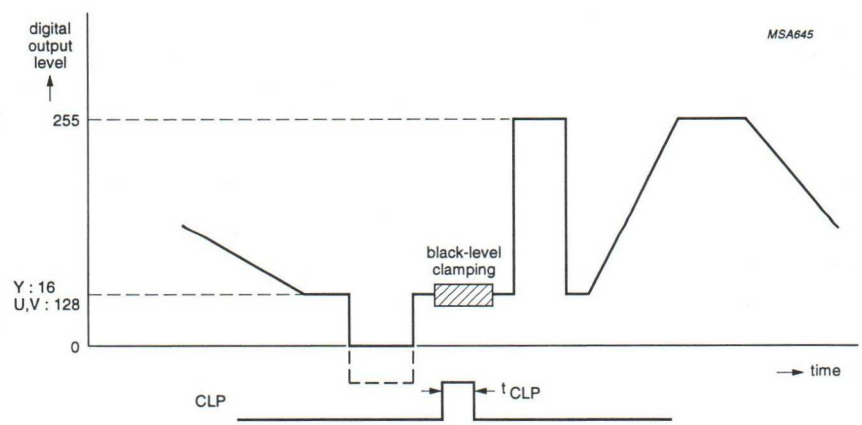
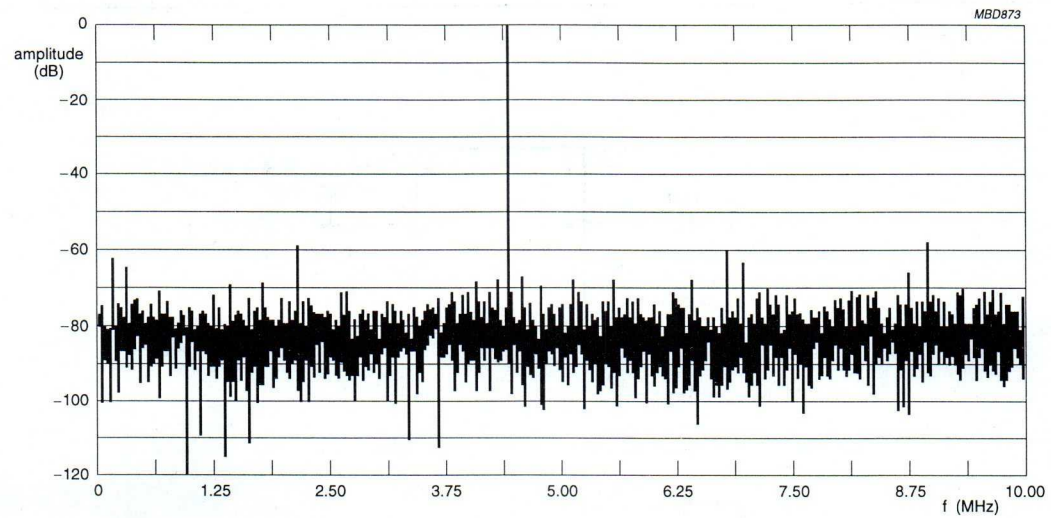


Fig.9 Clamping control timing.

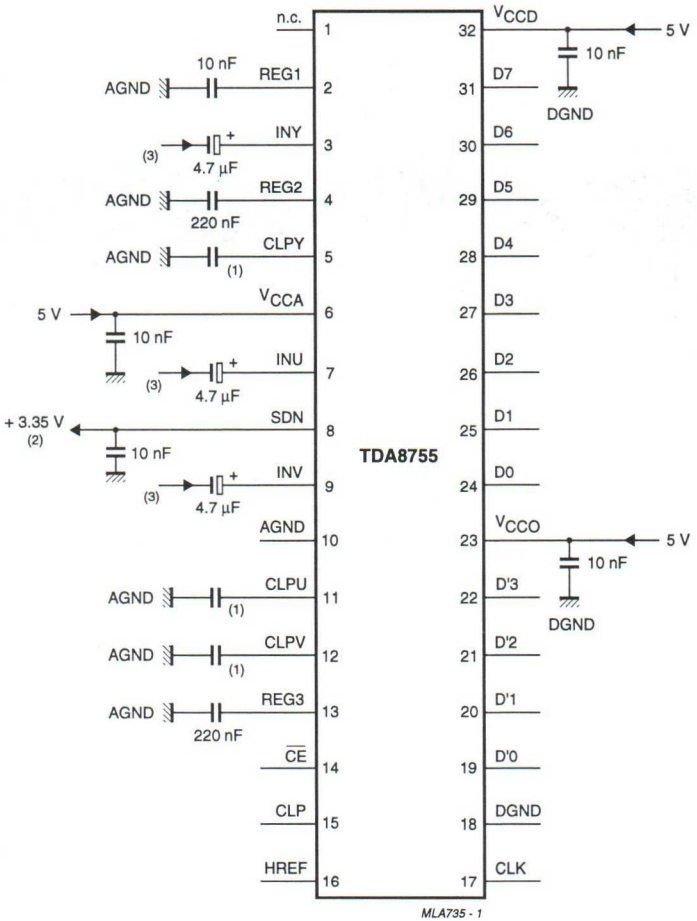


Effective bits: 7.30; THD = −53.35 dB.

Harmonic levels (dB): 2nd = −58.38; 3rd = −60.03; 4th = −57.30; 5th = −69.38; 6th = −67.09.

Fig.10 Fast Fourier Transform (f_{clk} = 20 MHz; f_i = 4.43 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

(1) Clamp capacitors must be determined in accordance with the application; recommended values are CLPY = 18 nF, CLPU and CLPV = 33 nF.

(2) It is possible to use the reference output voltage pin SDN to drive other analog circuits under the limits indicated in Chapter "Characteristics".

(3) Input signal pins have a high bandwidth. It is necessary to take special care on PCB layout to avoid any interaction from other signals (digital clocks for example).

Fig.11 Application diagram.

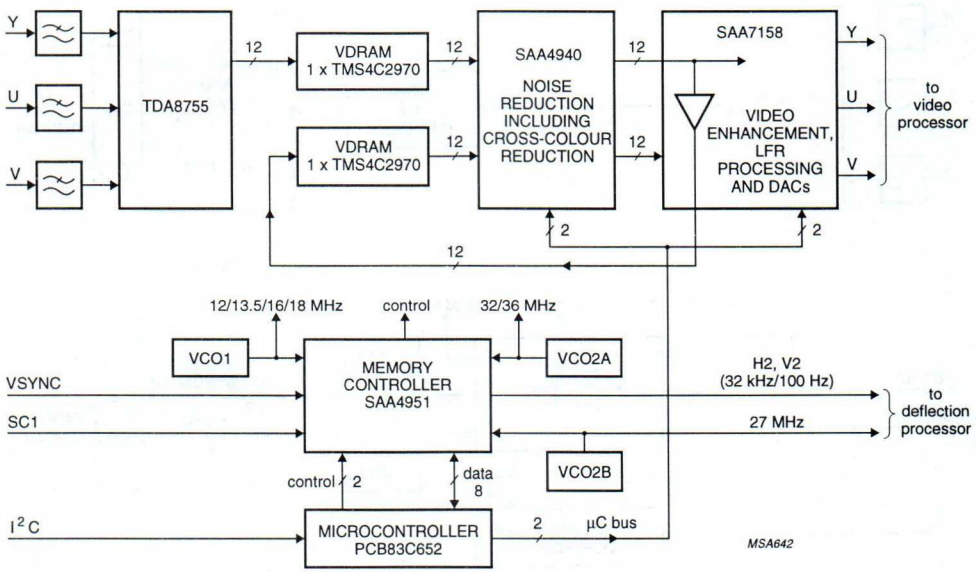


Fig.12 Block diagram of a full-options Improved Picture Quality (IPQ) module.

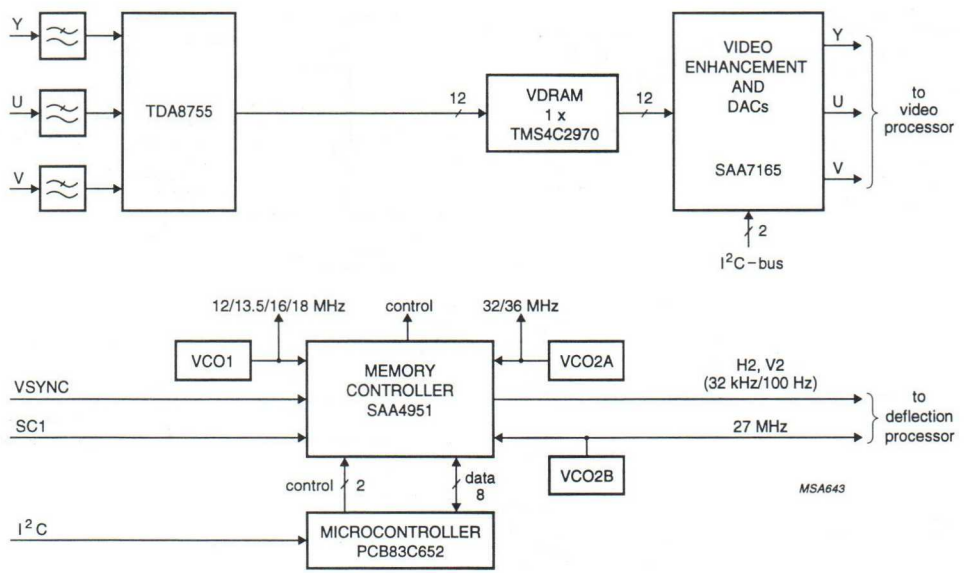


Fig.13 Block diagram of an economic Improved Picture Quality (IPQ) module.

YC 8-bit low-power analog-to-digital video interface

TDA8758

FEATURES

- Two 8-bit ADCs:
  - one Luminance or CVBS channel
  - one Chrominance channel
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs for each channel
- Internal reference voltage regulator
- TTL-compatible digital inputs and outputs
- Power dissipation of 530 mW (typical)
- Input selector circuit (five selectable video inputs for CVBS or YC processing)
- Peak white enable input
- Clamp and Automatic Gain Control (AGC) functions for Y/CVBS channel (clamping on code 64 and Peak White level control at code 255)
- Clamp function for C channel (code 128)
- No sample-and-hold circuit required.

APPLICATIONS

- Video signal decoding
- Digital picture processing
- Frame grabbing
- Multimedia with the Philips Desktop Video chip set (SAA7151B, SAA7191B, SAA7194, SAA7196 and SAA9051).

GENERAL DESCRIPTION

The TDA8758 is an 8-bit video high-speed low-power analog-to-digital conversion (ADC) interface for YC and CVBS signal processing. It converts 1-of-3 CVBS input signals or 1-of-2 YC input signals into binary or two's complement words at a sampling rate of 32 MHz. All analog signal inputs are digitally clamped and an ADC interface is provided on the Y/CVBS channel. A fast precharge on clamp and AGC is provided for start-up. All digital inputs and outputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	59	70	mA
I_{CCD}	digital supply current		–	28	40	mA
I_{CCO}	output supply current	C_L = 15 pF	–	19	28	mA
ILE	DC integral linearity error		–	±0.75	±1.5	LSB
DLE	DC differential linearity error		–	±0.4	±1.0	LSB
EB	effective bits (from video input to digital outputs)	f_{clk} = 32 MHz; f_i = 4.43 MHz	–	7.1	–	bits
$f_{clk(max)}$	maximum clock frequency		30	32	–	MHz
B	maximum –3 dB bandwidth (input preamplifier)	full-scale; 0 dB gain	–	15	–	MHz
α_{ct}	crosstalk between Y and C channels and each video input		–	–63	–55	dB
P_{tot}	total power dissipation		–	530	724	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8758G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

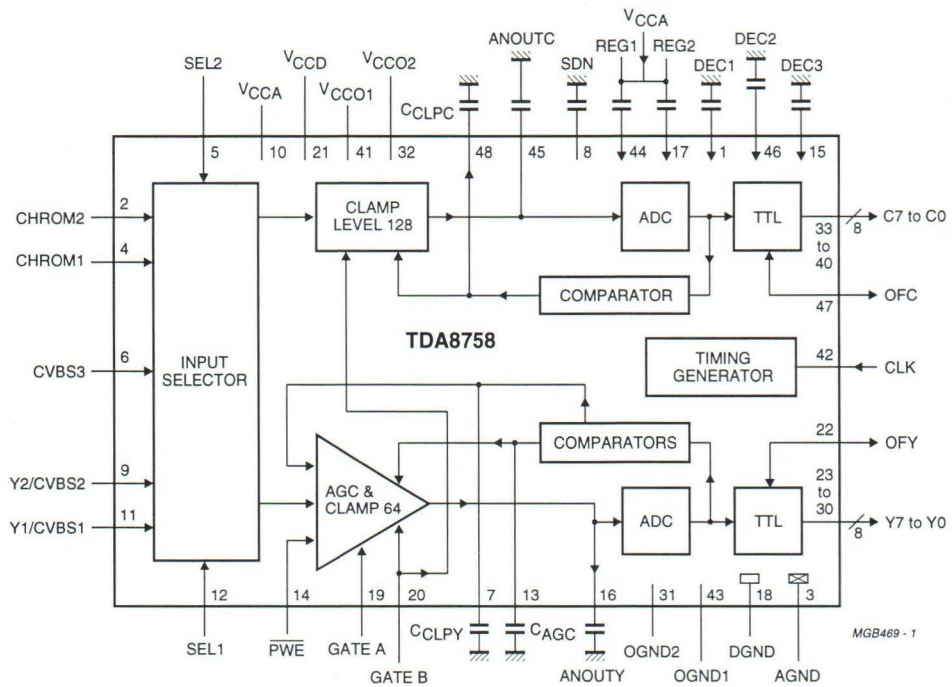


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DEC1	1	decoupling input 1
CHROM2	2	chrominance analog voltage input 2
AGND	3	analog ground
CHROM1	4	chrominance analog voltage input 1
SEL2	5	selection control input 2
CVBS3	6	luminance analog voltage input 3
C_{CLPY}	7	Y channel clamping capacitor
SDN	8	stabilizer decoupling node
Y2/CVBS2	9	luminance analog voltage input 2
V_{CCA}	10	analog supply voltage (+5 V)
Y1/CVBS1	11	luminance analog voltage input 1
SEL1	12	selection control input 1
C_{AGC}	13	AGC capacitor
$\overline{PWE}$	14	peak white enable input (active LOW)
DEC3	15	decoupling input 3
ANOUTY	16	analog output for Y channel
REG2	17	decoupling input 2 (internal stabilization loop decoupling)
DGND	18	digital ground
GATE A	19	AGC control input
GATE B	20	clamp control input
V_{CCD}	21	digital supply voltage (+5 V)
OFY	22	Y channel output format/chip enable (3-state input)
Y7	23	Y channel data output; bit 7 (MSB)
Y6	24	Y channel data output; bit 6
Y5	25	Y channel data output; bit 5
Y4	26	Y channel data output; bit 4
Y3	27	Y channel data output; bit 3
Y2	28	Y channel data output; bit 2
Y1	29	Y channel data output; bit 1
Y0	30	Y channel data output; bit 0 (LSB)
OGND2	31	output ground 2
V_{CCO2}	32	output supply voltage 2 (+5 V)
C7	33	C channel data output; bit 7 (MSB)
C6	34	C channel data output; bit 6
C5	35	C channel data output; bit 5
C4	36	C channel data output; bit 4
C3	37	C channel data output; bit 3
C2	38	C channel data output; bit 2
C1	39	C channel data output; bit 1
C0	40	C channel data output; bit 0 (LSB)

SYMBOL	PIN	DESCRIPTION
V_{CCO1}	41	output supply voltage 1 (+5 V)
CLK	42	clock input
OGND1	43	output ground 1
REG1	44	decoupling input 1 (internal stabilization loop decoupling)
ANOUTC	45	analog output for C channel
DEC2	46	decoupling input 2
OFC	47	C channel output format/chip enable (3-state input)
C_{CLPC}	48	C channel clamping capacitor

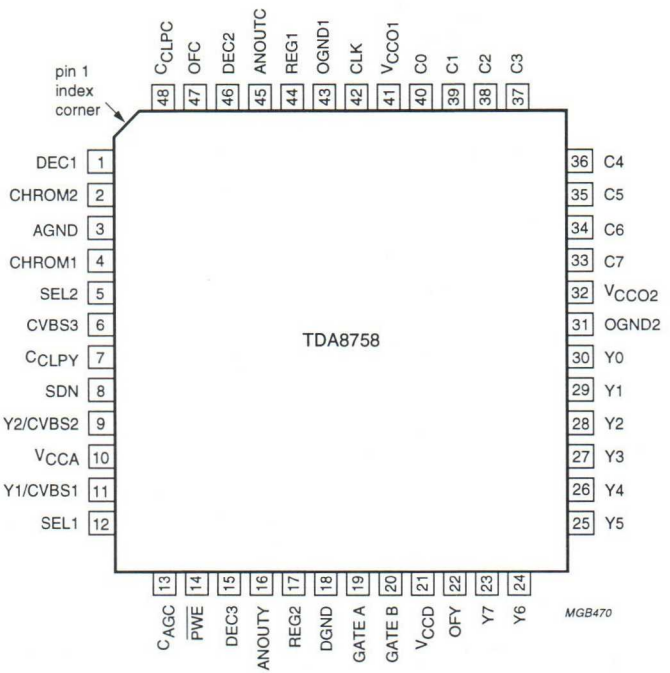


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8758 provides a simple interface between CVBS or Y/C analog signals and a digital colour decoder.

Video inputs selection

The input selector allows a choice from different video sources, and has one of the following configurations:

A: Two Y/C and one CVBS signals

B: One Y/C and two CVBS signals

C: Three CVBS signals (only the Y channel is used).

The wiring of the five video inputs (pins 2, 4, 6, 9 and 11) and the control of the two selection inputs (pins 5 and 12) will depend on the available video sources.

- In configuration A, connect as follows:
  - Y1 to pin 11
  - C1 to pin 4
  - Y2 to pin 9
  - C2 to pin 2
  - CVBS3 to pin 6.

  Keep SEL2 (pin 5) LOW and select Y1/C1 or Y2/C2 by switching SEL1 (pin 12).

  CVBS3 is selected with SEL1 and SEL2 HIGH.
- In configuration B, replace Y1 (or Y2) by a CVBS input (no more C1 or C2). The selection mode is the same.
- In configuration C, connect as follows:
  - CVBS1 to pin 11
  - CVBS2 to pin 9
  - CVBS3 to pin 6.

  Use both SEL1 and SEL2 to select inputs.

Remark: the video inputs selection is a static selection.

Synchronization pulses

GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively. They should be distinct.

On the Y channel, the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the C_{AGC} pin. The voltage across this capacitor controls the gain of the video amplifier. This is the control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 1 at the converter Y output. As the black level is digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The Peak White control loop is active when the selection pin $\overline{PWE}$ is LOW. Then, if the Y video signal exceeds the digital code of 255, it will be limited to avoid any over-range of the converter.

The clamp level control is accomplished by using the same techniques as used for the gain control. On both Y and C channels, the black level digital comparators are active during a positive-going pulse at the GATE B input. On the Y channel, the clamping capacitor connected to the C_{CLPY} pin will be charged or discharged to adjust the digital output to code 64. On the C channel, the clamping capacitor connected to the C_{CLPC} pin will be charged or discharged to adjust the digital output to code 128.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{CCO}	output supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−	5.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCO}	V
I_O	output current		−	+6	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	72	K/W

CHARACTERISTICS

$V_{CCA} = V_{10}$ to $V_3 = 4.75$ t 5.25 V; $V_{CCD} = V_{21}$ to $V_{18} = 4.75$ to 5.25 V; $V_{CCO1} = V_{41}$ to $V_{43} = 4.75$ to 5.25 V; $V_{CCO2} = V_{32}$ to $V_{31} = 4.75$ to 5.25 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCO} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCA} to $V_{CCO} = -0.25$ to +0.25 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		−	59	70	mA
I_{CCD}	digital supply current		−	28	40	mA
I_{CCOtot}	total output supply current	$C_L = 15$ pF	−	19	28	mA
Video amplifier inputs						
Y1/CVBS1, Y2/CVBS2, CVBS3, CHROM1 AND CHROM2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1				
	Y channel		0.7	−	1.4	V
	C channel		−	1.0	−	V
$\|Z_i\|$	input impedance	$f_i = 6$ MHz	−	25	−	kΩ
C_I	input capacitance	$f_i = 6$ MHz	−	2	−	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SEL1 AND SEL2 TTL INPUTS (see Table 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (see Figs 5 and 6)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
AGC INPUT (PIN 13) see Fig.8						
$V_{13(min)}$	AGC voltage for minimum gain at –3 dB		–	3.3	–	V
$V_{13(max)}$	AGC voltage for maximum gain at +3 dB		–	3.75	–	V
I_{12}	AGC output current		see Table 2			
C-CHANNEL CLAMP INPUT (PIN 48)						
V_{48}	CLAMP voltage for code 128 output		–	3.45	–	V
I_{48}	CLAMP output current		see Table 3			
Y-CHANNEL CLAMP INPUT (PIN 7)						
V_7	CLAMP voltage for code 64 output		–	3.70	–	V
I_7	CLAMP output current		see Table 3			
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between video inputs (pins 2, 4, 6, 9 and 11)	V_{CCA} = 4.75 to 5.25 V	–	–63	–55	dB
B	–3 dB bandwidth		–	15	–	MHz
ΔG	gain range		–3	–	+3	dB
G_{stab}	gain stability as a function of:					
	supply voltage	f_i = 4.43 MHz	–	–	0.5	%
	supply voltage and temperature		–	–	6	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 42)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	µA
C_I	input capacitance	f_{clk} = 32 MHz	–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OFY AND OFC INPUTS; 3-STATE (see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_I	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	µA
I_{IH}	HIGH level input current		–	500	700	µA
Analog-to-digital converter outputs						
ANOUTY AND ANOUTC OUTPUTS (PINS 16 AND 45) see Table 5						
V_{ANOUT}	output voltage	digital output = 00	–	2.6	–	V
V_{ANOUT}	output voltage	digital output = 255	–	3.6	–	V
$V_{ANOUT(p-p)}$	output voltage amplitude (peak-to-peak value)		–	1.0	–	V
DIGITAL OUTPUTS Y0 TO Y7, C0 TO C7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
Switching characteristics; see Fig.9						
$f_{clk(max)}$	CLK input maximum frequency	note 2	30	32	–	MHz
t_{CPH}	clock pulse width HIGH		12	–	–	ns
t_{CPL}	clock pulse with LOW		12	–	–	ns
Analog signal processing from video input to digital output on both channels; 0 dB gain (f_{clk} = 32 MHz)						
INL	DC integral non-linearity		–	±0.75	±1.5	LSB
DNL	DC differential non-linearity		–	±0.4	±1.0	LSB
AINL	AC integral non linearity	f_i = 4.43 MHz	–	±1.5	–	LSB
ADNL	AC differential non-linearity	f_i = 4.43 MHz	–	±0.5	–	LSB
THD	total harmonic distortion	note 3	–	–52	–	dB
EB	effective bits	f_i = 4.43 MHz; note 4	–	7.1	–	bits
G_{diff}	differential gain	$V_{16,45}$ = 1.0 V (p-p); see Fig.4; PAL modulated ramp; note 5	–	1.5	3.0	%
φ_{diff}	differential phase	see Fig.5; PAL modulated ramp; note 5	–	0.6	1.5	deg
SVRR2	supply voltage ripple rejection	note 6	–	–	5	%/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 32 MHz) see Fig.9						
DIGITAL OUTPUTS (C_L = 15 pF)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		10	–	–	ns
t_d	output delay time		–	15	18	ns
t_W	clamp pulse width	see Figs 6 and 7	2	3	–	µs
3-state output delay times; see Fig.10						
t_{dZH}	enable HIGH		–	12	14	ns
t_{dZL}	enable LOW		–	10	12	ns
t_{dHZ}	disable HIGH		–	58	62	ns
t_{dLZ}	disable LOW		–	70	74	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{I(p-p)}$ = 1.0 V on Y channel.
2. It is recommended that the rise and fall times of the clock are ≥1 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
3. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   a) F being the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
5. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a digital-to-analog converter.
6. The supply voltage ripple rejection is the relative variation of the analog signal (full-scale signal at input) for 0.5 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) \times (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

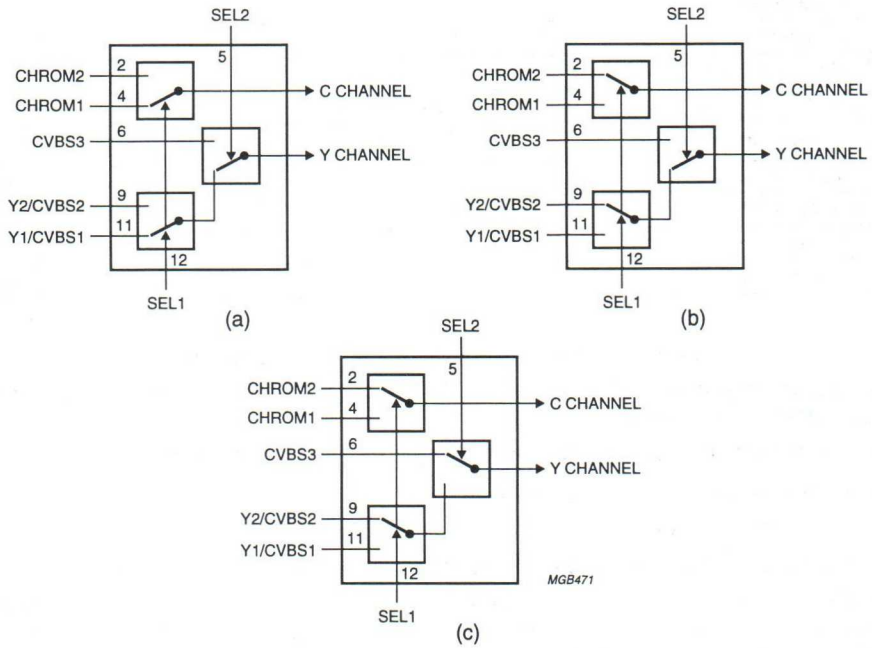


Fig.3 Video inputs selector.

Table 1 Video input selection

SEL1	SEL2	Y-CHANNEL	C-CHANNEL	FIGURE 3
0	X[1]	Y1/CVBS1	CHROM1	(a)
1	0	Y2/CVBS2	CHROM2	(b)
1	1	CVBS3	CHROM2	(c)

Note

1. X = don't care.

Table 2 AGC output current

$\overline{PWE}$	GATE A	DIGITAL OUTPUT	I_{AGC}
0	0	output < 255	0 μA
		output > 255	+540 μA
0	1	output < 0	+8 μA
		0 < output < 255	−8 μA
		output > 255	+540 μA
1	0	X[1]	0 μA
1	1	output < 0	+8 μA
		0 < output < 255	−8 μA

Note

1. X = don't care.

Table 3 CLAMP output current

CLAMP	GATE B	DIGITAL OUTPUT	I_{CLAMP}
C	1	output < 128	+54 μA
		output > 128	−54 μA
X[1]	0	X[1]	0 μA
Y	1	output < 64	+54 μA
		64 < output	−54 μA

Note

1. X = don't care.

Table 4 OFY and OFC input coding

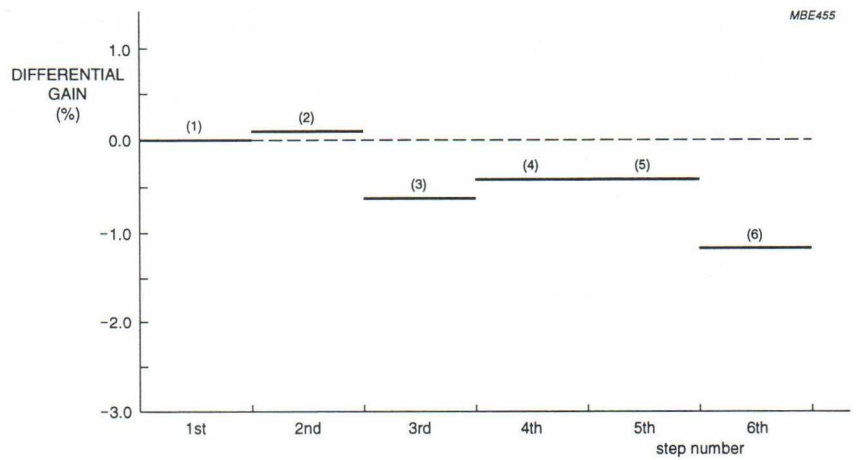
OFY (OR OFC)	Y0 TO Y7 (OR C0 TO C7)
0	active, two's complement
1	high impedance
open circuit[1]	active, binary

Note

1. Use C ≥ 10 pF to DGND.

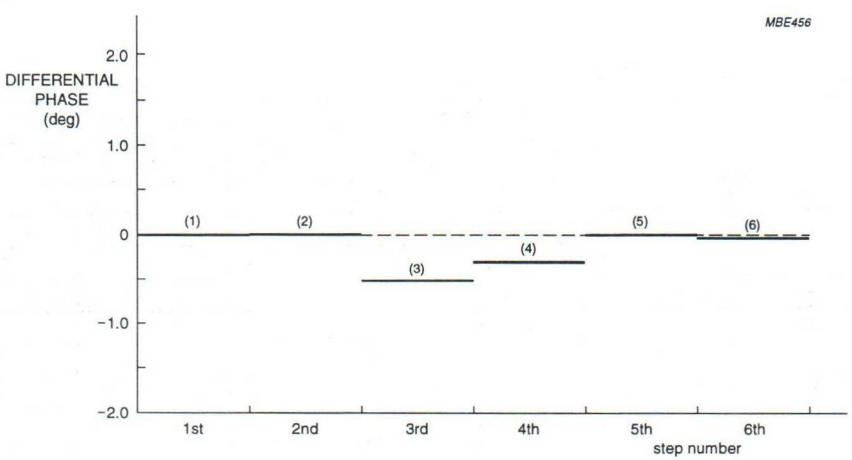
Table 5 Output coding and ANOUTY (or ANOUTC) voltage (typical values)

STEP	V_I	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	2.6	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.6	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1



(1) = 0.00; (2) = 0.09; (3) = −0.63; (4) = −0.45; (5) = −0.45; (6) = −1.23.
Differential gain = max. (2) − min. (6) = 1.32%.

Fig.4 Typical differential gain result on VM700A.



(1) = 0.00; (2) = 0.03; (3) = −0.53; (4) = −0.32; (5) = 0.01; (6) = −0.08.
Differential phase = max. (2) − min. (3) = 0.56 deg.

Fig.5 Typical differential phase result on VM700A.

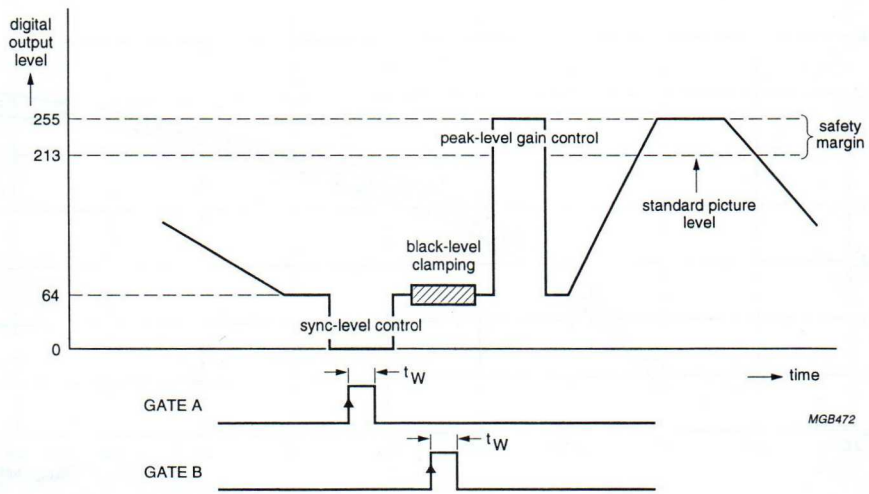


Fig.6 Control mode Y channel.

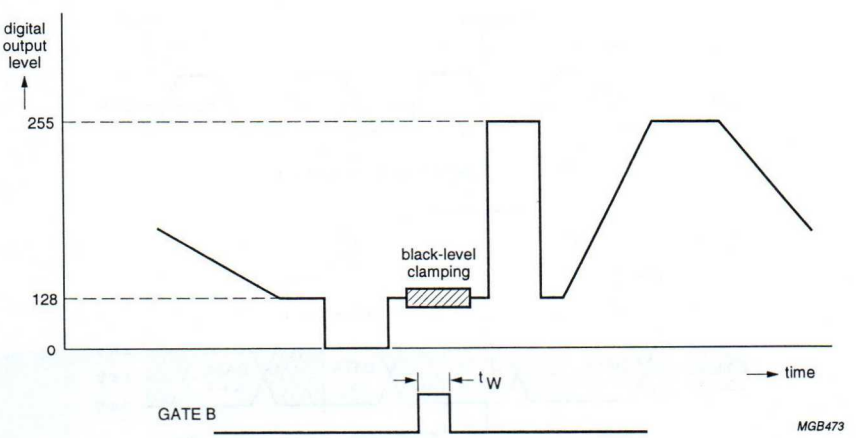
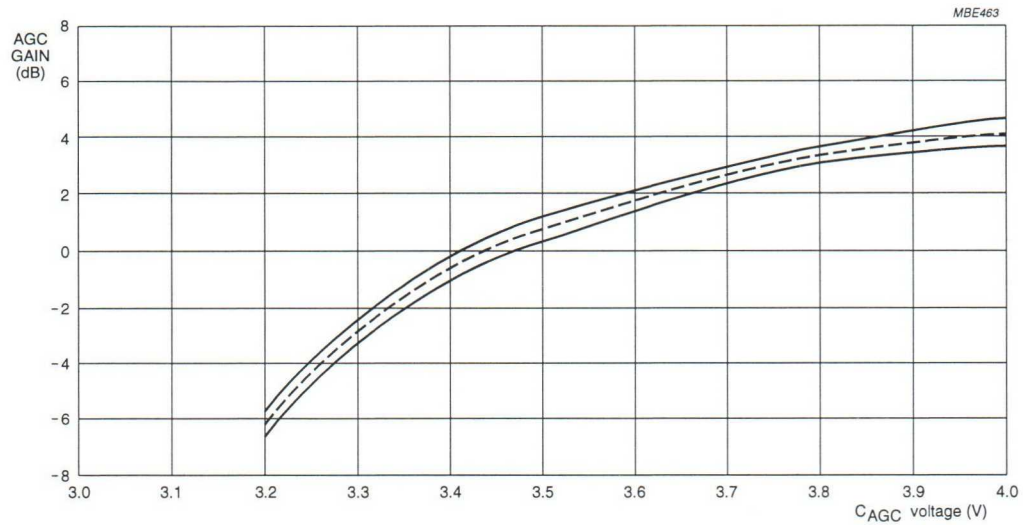


Fig.7 Control mode C-channel.



Dotted line: Typical curve (T_{amb} = 25 °C; V_{CC} = 5 V).
Full line: Maximum envelope (T_{amb} = 0 to 70 °C; V_{CC} = 4.75 to 5.25 V).

Fig.8 AGC behaviour as a function temperature and supply voltage for ANOUTY output; f_i = 4.43 MHz, V_i = 0 dB.

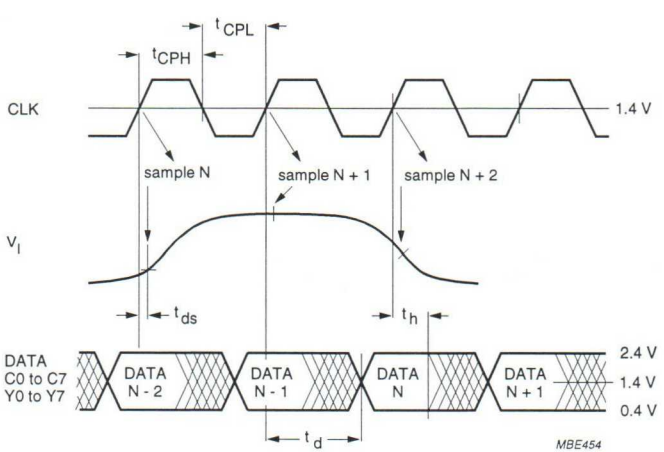
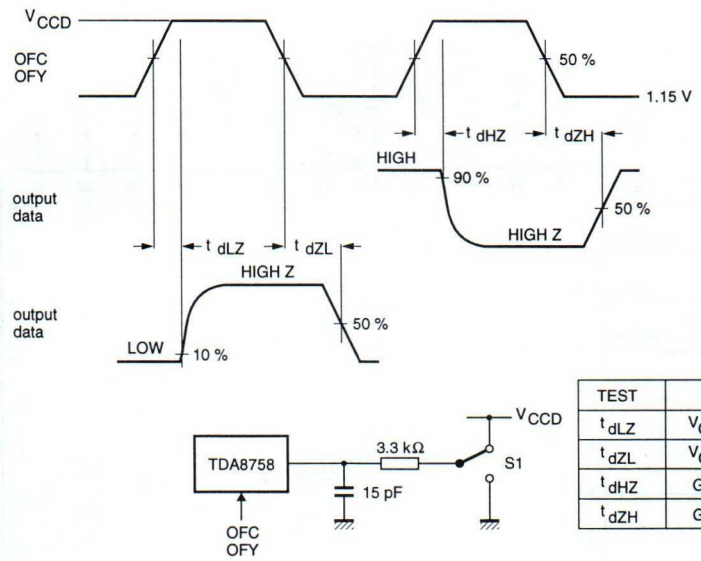


Fig.9 Timing diagram.

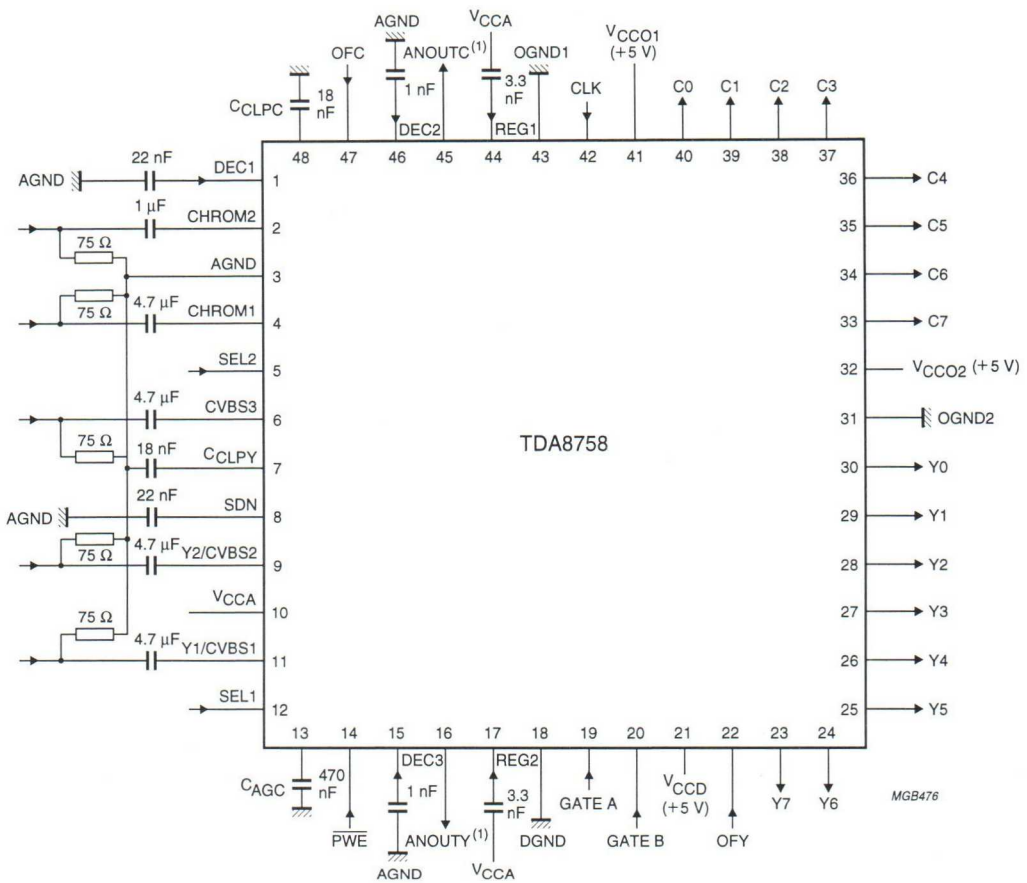


TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{OFC} = f_{OFY} = 100$ kHz.

Fig.10 Timing diagram and test conditions of 3-state output delay time.

APPLICATION INFORMATION



(1) It is recommended that pin 16 and pin 45 are not loaded in order to avoid any distortion.

Fig.11 Application diagram.

10-bit high-speed analog-to-digital converter

TDA8760

FEATURES

- 10-bit resolution
- Sampling rate up to 50 MHz
- Total harmonic distortion (THD): –65 dB at 4.43 MHz full scale and a 40 MHz clock frequency
- High signal-to-noise ratio over a large analog input frequency range (8.8 effective bits at 10 MHz full-scale input at a 40 MHz clock frequency)
- +5 V power supplies
- Binary or two's complement 3-state TTL outputs
- In-range 3-state TTL output
- TTL compatible digital inputs
- LOW-level AC clock input signal allowed
- Power dissipation 850 mW (typical)
- Low analog input capacitance (typ. 4.5 pF), no buffer amplifier required
- No external sample-and-hold circuit required
- Analog Input; single or differential
- External amplitude range control
- Voltage controlled regulator included.

APPLICATIONS

- High-speed analog-to-digital conversion for
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Digital video broadcasting (satellite and cable)
  - Transient signal analysis
  - High energy physics research
  - Sigma-delta (SD) modulators
  - Medical imaging
  - Radar pulse digitizing.

GENERAL DESCRIPTION

The TDA8760 is a monolithic bipolar 10-bit analog-to-digital converter (ADC) for video or other applications. It converts the analog input signal into 10-bit binary coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible. However, a sine-wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	95	100	mA
I_{CCD}	digital supply current		–	40	45	mA
I_{CCO}	output supply current		–	35	40	mA
ILE	DC integral linearity error	f_{clk} = 4 MHz	–	±1.0	±2.0	LSB
DLE	DC differential linearity error	f_{clk} = 4 MHz	–	±0.6	±1.0	LSB
AILE	AC integral linearity error	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	±1.2	±2.0	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8760K/2		20	–	–	MHz
	TDA8760K/4		40	–	–	MHz
	TDA8760K/5		50	–	–	MHz
P_{tot}	total power dissipation		–	850	970	mW
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				
	PINS	PIN POSITION	MATERIAL	CODE	SAMPLING FREQUENCY (MHz)
TDA8760K/2	44	PLCC	plastic	SOT187	20
TDA8760K/4	44	PLCC	plastic	SOT187	40
TDA8760K/5	44	PLCC	plastic	SOT187	50

BLOCK DIAGRAM

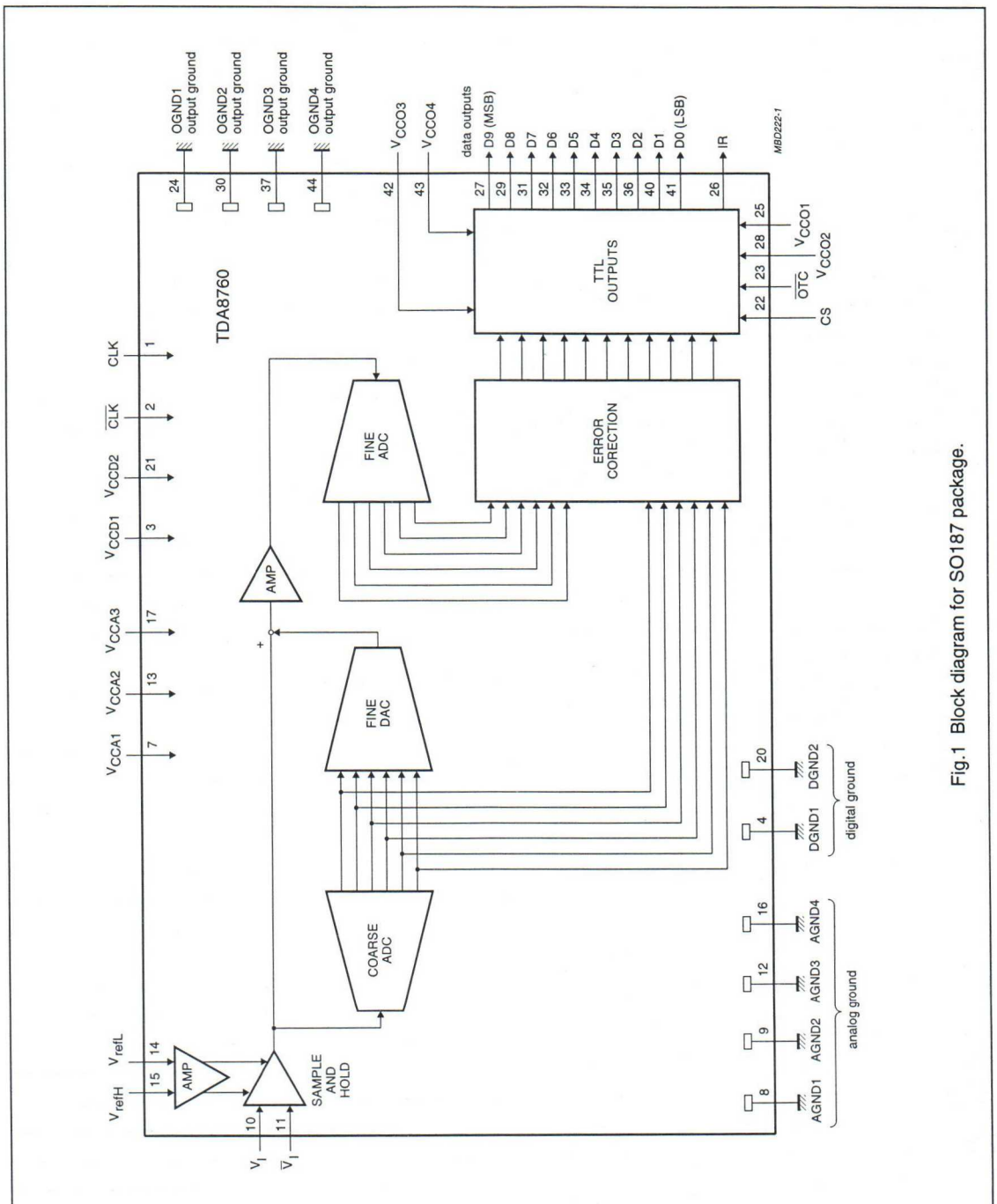


Fig.1 Block diagram for SO187 package.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{CLK}$	2	complementary clock input
V_{CCD1}	3	digital supply voltage (+5 V)
DGND1	4	digital ground
n.c.	5	not connected
n.c.	6	not connected
V_{CCA1}	7	analog supply voltage (+5 V)
AGND1	8	analog ground
AGND2	9	analog ground
V_I	10	analog input voltage
$\overline{V_I}$	11	complementary analog input voltage
AGND3	12	analog ground
V_{CCA2}	13	analog supply voltage (+5 V)
V_{refL}	14	reference voltage LOW
V_{refH}	15	reference voltage HIGH
AGND4	16	analog ground
V_{CCA3}	17	analog supply voltage (+5 V)
n.c.	18	not connected
n.c.	19	not connected
DGND2	20	digital ground
V_{CCD2}	21	digital supply voltage (+5 V)
CS	22	chip select input (TTL level input; active HIGH)
$\overline{OTC}$	23	output two's complement
OGND1	24	output ground
V_{CCO1}	25	output supply voltage (+5 V)
IR	26	in-range output
D9	27	data output, bit 9 (MSB)
V_{CCO2}	28	output supply voltage (+5 V)
D8	29	data output, bit 8
OGND2	30	output ground
D7	31	data output, bit 7
D6	32	data output, bit 6
D5	33	data output, bit 5
D4	34	data output, bit 4
D3	35	data output, bit 3
D2	36	data output, bit 2
OGND3	37	output ground
n.c.	38	not connected
n.c.	39	not connected
D1	40	data output, bit 1

SYMBOL	PIN	DESCRIPTION
D0	41	data output, bit 0 (LSB)
V_{CCO3}	42	output supply voltage (+5 V)
V_{CCO4}	43	output supply voltage (+5 V)
OGND4	44	output ground

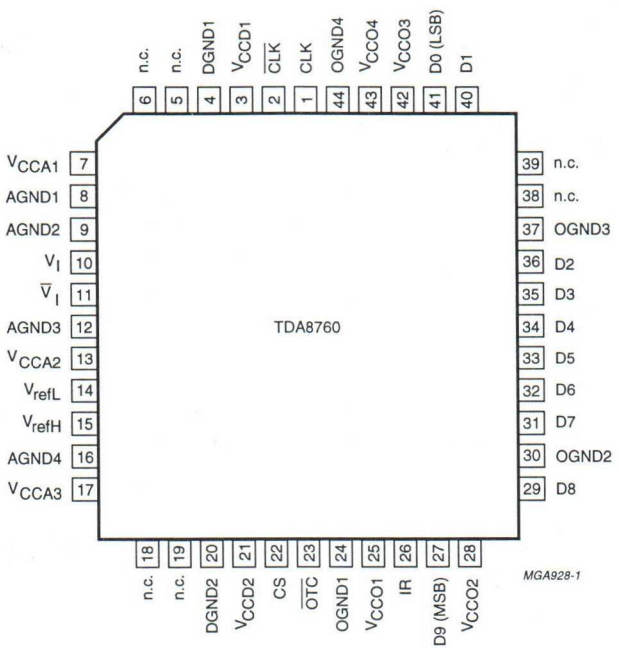


Fig.2 Pin configuration for SOT187.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		–0.3	+7.0	V
V_{CCD}	digital supply voltage		–0.3	+7.0	V
V_{CCO}	output supply voltage		–0.3	+7.0	V
ΔV_{CC1}	supply voltage difference between V_{CCA} and V_{CCD}		–0.5	+0.5	V
ΔV_{CC2}	supply voltage difference between V_{CCO} and V_{CCD}		–0.5	+0.5	V
ΔV_{CC3}	supply voltage difference between V_{CCA} and V_{CCO}		–0.5	0.5	V
V_I	input voltage	referenced to AGND	0.3	V_{CCA}	V
$V_{I(p-p)}$	input voltage for differential clock drive (peak-to-peak value)		–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	TDA8760K/5; TDA8760K/4	35 K/W
	TDA8760K/2	46 K/W

CHARACTERISTICS

$V_{CCA} = V_{CCD} = V_{CCO} = 4.75$ to 5.25 V; AGND and DGND shorted together;
$V_{CCA} - V_{CCD} = V_{CCO} - V_{CCD} = V_{CCA} - V_{CCO} = -0.25$ to +0.25 V; $T_{amb} = 0$ to +70 °C; unless otherwise specified.
Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	95	100	mA
I_{CCD}	digital supply current		–	40	45	mA
I_{CCO}	output supply current	all outputs LOW	–	35	40	mA
Inputs						
CLK AND $\overline{CLK}$ (REFERENCED TO DGND); NOTE 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} or $V_{\overline{clk}} = 0.4$ V	–400	–	–	mA
I_{IH}	HIGH level input current	V_{clk} or $V_{\overline{clk}} = 2.0$ V	–	–	100	mA
		V_{clk} or $V_{\overline{clk}} = V_{CCD}$	–	–	300	mA
Z_I	input impedance	$f_{clk} = 40$ MHz	–	2	–	kΩ
C_I	input capacitance	$f_{clk} = 40$ MHz	–	4.5	–	pF
ΔV_{clk}	AC input voltage for switching ($V_{clk} - V_{\overline{clk}}$)	DC level = 1.5 V	0.5	–	2.0	V
		DC level = 2.5 V	1.5	–	5.0	V
$\overline{OTC}$ AND CS (REFERENCED TO DGND); SEE TABLE 3						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.8$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.0$ V	–	–	20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_I AND $\overline{V}_I$ (REFERENCED TO AGND; SEE ALSO TABLES 1 AND 2)						
I_{IL}	LOW level input current	$V_{refH} - V_{refL}$ = 1.5 V	–	7	–	μA
I_{IH}	HIGH level input current	$V_{refH} - V_{refL}$ = 1.5 V	–	22	–	μA
Z_I	input impedance	f_i = 4.43 MHz	–	2	–	kΩ
C_I	input capacitance	f_i = 4.43 MHz	–	4.5	–	pF
$V_{Ioffset(d)}$	input offset voltage	differential mode; $V_I = \overline{V}_I$; output code 511; Table 1				
		V_{CCA} = 5 V	3.3	3.4	3.6	V
		V_{CCA} = 4.75 V	3.2	–	3.45	V
		V_{CCA} = 5.25 V	3.3	–	3.8	V
$V_{Ioffset(s)}$	input offset voltage	single mode; $V_I = V_{Ioffset(s)}$; output code 511; Table 2				
		V_{CCA} = 5 V	3.6	3.7	3.8	V
		V_{CCA} = 4.75 V	tbf	–	tbf	V
		V_{CCA} = 5.25 V	tbf	–	tbf	V
Voltage controlled regulator inputs V_{refH} and V_{refL} (referenced to AGND); differential input						
V_{refH}	reference voltage HIGH		4.0	4.5	V_{CCA}	V
V_{refL}	reference voltage LOW		2.5	3.0	3.5	V
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		1.4	1.5	1.6	V
I_{refH}	input current at V_{refH}		–	10	–	μA
I_{refL}	input current at V_{refL}		–	10	–	μA
Voltage controlled regulator inputs V_{refH} and V_{refL} (referenced to AGND); single input						
V_{refH}	reference voltage HIGH		4.0	4.4	V_{CCA}	V
V_{refL}	reference voltage LOW		2.5	3.0	3.5	V
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		1.3	1.4	1.5	V
I_{refH}	input current at V_{refH}		–	10	–	μA
I_{refL}	input current at V_{refL}		–	10	–	μA
Outputs (referenced to DGND)						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_O	output current in 3-state mode	0.4 V < V_O < V_{CCO}	–20	–	+20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK FREQUENCY f_{clk} (NOTE 1; SEE FIG.3)						
$f_{clk(min)}$	minimum clock frequency		–	–	1	MHz
$f_{clk(max)}$	maximum clock frequency					
	TDA8760K/5		50	–	–	MHz
	TDA8760K/4		40	–	–	MHz
	TDA8760K/2		20	–	–	MHz
t_{CPH}	clock pulse width HIGH	note 7	10	–	–	ns
t_{CPL}	clock pulse width LOW		8	–	–	ns
Analog signal processing in differential input mode; see Table 1; 50% clock duty factor; $V_{I(p-p)} = V_{refH} - V_{refL} = 1.5$ V						
LINEARITY						
ILE	DC integral linearity error	f_{clk} = 4 MHz	–	±1.0	±2.0	LSB
DLE	DC differential linearity error	f_{clk}= 4 MHz	–	±0.6	±1.0	LSB
AILE	AC integral linearity error	note 3	–	±1.2	±2.0	LSB
BANDWIDTH (f_{clk} = 50 MHz); NOTE 9						
B	Analog bandwidth	-1 dB	–	140	–	MHz
		-3 dB	–	220	–	MHz
HARMONICS (f_{clk} = 40 MHz); SEE FIGS 6, 8, 9 AND 10						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	–70	–63	dB
	third harmonics		–	–70	–63	dB
THD_d	total harmonic distortion	f_i = 4.43 MHz; note 2	–	–65	–60	dB
SIGNAL-TO-NOISE RATIO; NOTES 4 AND 5; SEE FIGS 6, 8, 9 AND 10						
SNR	signal-to-noise ratio	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	54	56	–	dB
EFFECTIVE BITS; NOTES 4 AND 5; SEE FIGS 6, 8, 9 AND 10						
EB	effective bits TDA8760K/2 (f_{clk} = 20 MHz)	f_i = 4.43 MHz	–	8.90	–	bits
		f_i = 7.5 MHz	–	8.70	–	bits
	effective bits TDA8760K/4 (f_{clk} = 40 MHz)	f_i = 4.43 MHz	–	8.80	–	bits
		f_i = 10 MHz	–	8.80	–	bits
		f_i = 15 MHz	–	8.70	–	bits
	effective bits TDA8760K/5 (f_{clk} = 50 MHz)	f_i = 4.43 MHz	–	8.70	–	bits
		f_i = 10 MHz	–	8.65	–	bits
		f_i = 15 MHz	–	8.60	–	bits
		f_i = 20 MHz	–	8.20	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TWO-TONE						
Two-tone	two-tone intermodulation rejection	f_{clk} = 40 MHz; note 8	–	–65	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 512	–	2×10^{-12}	–	times/ samples
DIFFERENTIAL GAIN; SEE FIG.5						
G_{diff}	differential gain	f_{clk} = 20 MHz; f_i = 4.43 MHz	–	0.5	tbf	%
		f_{clk} = 40 MHz; f_i = 4.43 MHz	–	1.0	tbf	%
DIFFERENTIAL PHASE						
Φ_{diff}	differential phase	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	0.1	0.2	deg
Analog signal processing in single input mode; see Table 2; 50% clock duty factor; $V_{I(p-p)} = V_{refH} - V_{refL}$ = 1.4 V						
LINEARITY						
ILE	DC integral linearity error	f_{clk} = 4 MHz	–	±1.0	±2.0	LSB
DLE	DC differential linearity error	f_{clk}= 4 MHz	–	±0.6	±1.0	LSB
AILE	AC integral linearity error	note 3	–	±1.2	±2.0	LSB
BANDWIDTH (f_{clk} = 50 MHz); NOTE 9						
B	Analog bandwidth	-1 dB	–	140	–	MHz
		-3 dB	–	220	–	MHz
HARMONICS (f_{clk} = 40 MHz); SEE FIG.7						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	–61	–	dB
	third harmonics		–	–62	–	dB
THD_s	total harmonic distortion	f_i = 4.43 MHz; note 2	–	–59	–	dB
SIGNAL-TO-NOISE RATIO; NOTES 4 AND 5; SEE FIG.7						
SNR	signal-to-noise ratio	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	54	56	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS; NOTES 4 AND 5; SEE FIG.7						
EB	effective bits TDA8760K/2 (f_{clk} = 20 MHz)	f_i = 4.43 MHz	–	8.70	–	bits
		f_i = 7.5 MHz	–	8.50	–	bits
	effective bits TDA8760K/4 (f_{clk} = 40 MHz)	f_i = 4.43 MHz	–	8.50	–	bits
		f_i = 10 MHz	–	8.20	–	bits
	effective bits TDA8760K/5 (f_{clk} = 50 MHz)	f_i = 4.43 MHz	–	8.25	–	bits
		f_i = 10 MHz	–	8.00	–	bits
TWO-TONE						
Two-tone	two-tone intermodulation rejection	f_{clk} = 40 MHz; note 8	–	–60	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 512	–	2×10^{-12}	–	times/ samples
DIFFERENTIAL GAIN; SEE FIG.5						
G_{diff}	differential gain	f_{clk} = 20 MHz; f_i = 4.43 MHz	–	0.5	tbf	%
		f_{clk} = 40 MHz; f_i = 4.43 MHz	–	1.0	tbf	%
DIFFERENTIAL PHASE						
Φ_{diff}	differential phase	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	0.1	0.2	deg
Timing (note 6; see Fig.3; C_L = 15 pF)						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		8	–	–	ns
t_d	output delay time		–	12	16	ns
3-state output delay times (see Fig.4)						
t_{dZH}	enable HIGH		–	12	16	ns
t_{dZL}	enable LOW		–	12	16	ns
t_{dHZ}	disable HIGH		–	8	12	ns
t_{dLZ}	disable LOW		–	16	20	ns

Notes

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. There are three modes of operation:

   TTL mode 1:
   CLK input is at TTL level with a threshold voltage of 1.5 V and sampling is taken on the falling edge of the clock input signal. $\overline{CLK}$ decoupled to DGND via a 100 nF capacitor.

   TTL mode 2:
   $\overline{CLK}$ input is at TTL level with threshold voltage of 1.5 V and sampling is taken on the rising edge of the clock input signal. CLK decoupled to DGND via a 100 nF capacitor.

   TTL mode3:
   CLK and $\overline{CLK}$ inputs are at differential TTL levels.

   AC driving modes:
   When driving the CLK input directly and with any AC signal of minimum 0.5 V (p-p) and with a DC level of 1.5 V, the sampling takes place at the falling edge of the clock signal.
   When driving the $\overline{CLK}$ input with the same signal, sampling takes place at the rising edge of the clock signal.It is recommended to decouple the $\overline{CLK}$ or CLK input to DGND via a 100 nF capacitor.

2. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   F being the fundamental harmonic referenced at 0 dB for a full-scale sinewave input.

3. AC linearity: full-scale differential sinewave (f_i = 4.43 MHz; f_{clk} = 40 MHz).
4. Effective bits with differential input and single input are respectively executed with full scale differential input and full scale single sinewave.
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR = EB x 6.02 + 1.76 dB.
6. Output data acquisition: the output data is available after the maximum delay of t_d.
7. t_{CPH} of 9 ns (minimum) can be applied at the penalty of 0.5 effective bit drop compared to typical values.
8. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. The –3 dB (or –1 dB) analog bandwidth is determined by the 3 dB (or 1 dB) reduction in the reconstructed output, the input being a full-scale sine wave.

Table 1 Output coding with differential inputs (typical values to AGND); $V_{I(p-p)} = V_{refH} - V_{refL} = 1.5$ V.

CODE	$V_{I(p-p)}$	$\overline{V}_{I(p-p)}$	IR	BINARY OUTPUTS	TWO'S COMPLEMENT OUTPUTS
				D9 TO D0	D9 TO D0
underflow	<3.025	>3.775	0	0000000000	1000000000
0	3.025	3.775	1	0000000000	1000000000
1	–	–	1	0000000001	1000000001
•	–	–	•	••••••••••	••••••••••
511	3.40	3.40	1	0111111111	1111111111
•	–	–	•	••••••••••	••••••••••
1022	–	–	1	1111111110	0111111110
1023	3.775	3.025	1	1111111111	0111111111
overflow	>3.775	<3.025	0	1111111111	0111111111

Table 2 Output coding with single inputs (typical values to AGND); $V_{I(p-p)} = V_{refH} - V_{refL} = 1.4$ V; $\overline{V}_{I(p-p)} = 3.7$ V.

CODE	$V_{I(p-p)}$	IR	BINARY OUTPUTS	TWO'S COMPLEMENT OUTPUTS
			D9 TO D0	D9 TO D0
underflow	<3.0	0	0000000000	1000000000
0	3.0	1	0000000000	1000000000
1	–	1	0000000001	1000000001
•	–	•	••••••••••	••••••••••
511	3.7	1	0111111111	1111111111
•	–	•	••••••••••	••••••••••
1022	–	1	1111111110	0111111110
1023	4.4	1	1111111111	0111111111
overflow	>4.4	0	1111111111	0111111111

Table 3 Mode selection.

$\overline{OTC}$	CS	D0 TO D9 AND IR
1	1	binary; active
0	1	two's complement; active
X[1]	0	high impedance

Note

1. Where: X = don't care.

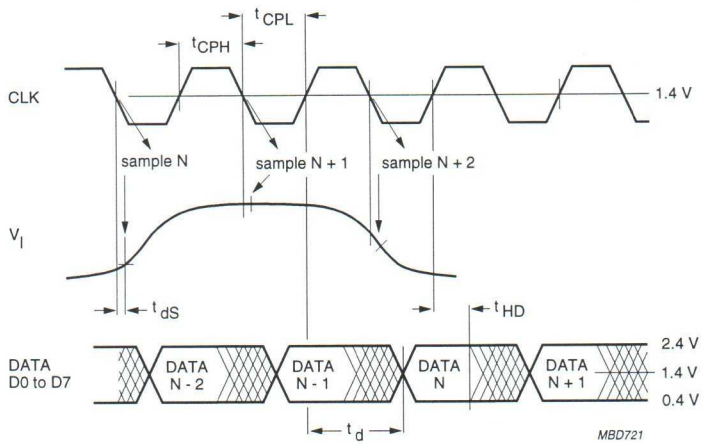
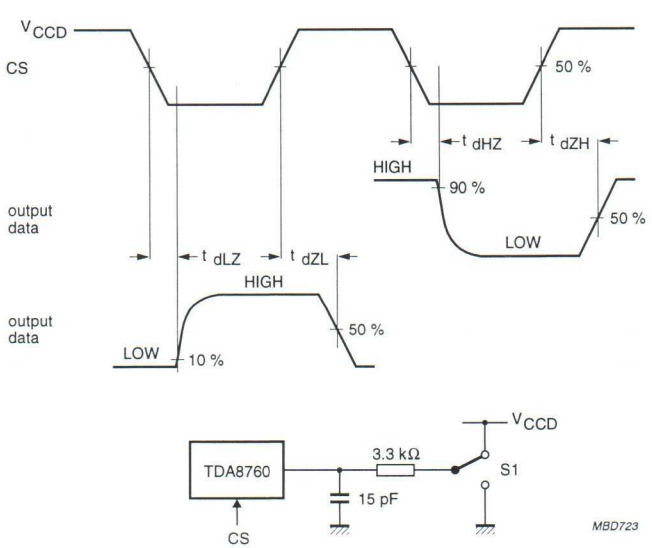


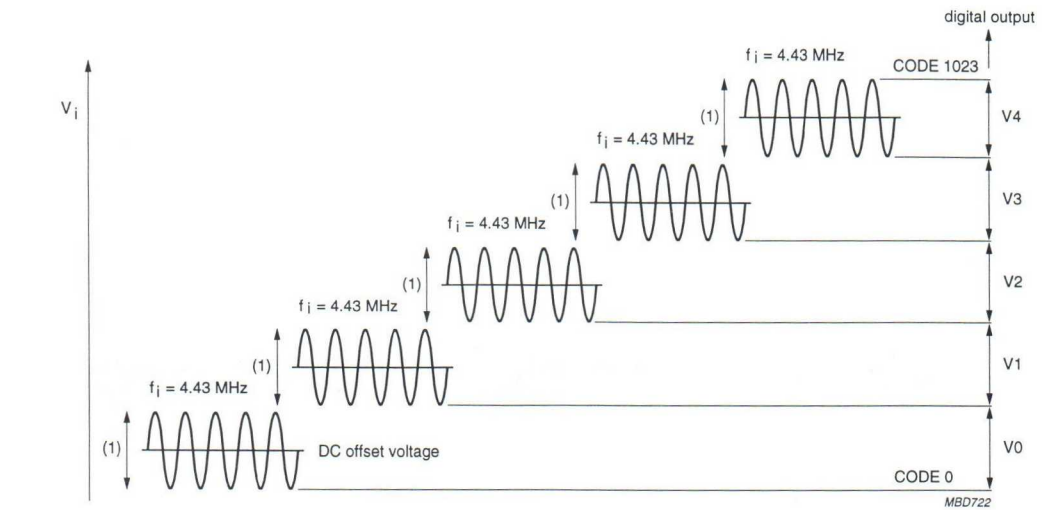
Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

CS = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.



(1) Full-scale divided by 5.

$$G_{diff} = \text{maximum of } \left(\frac{V_n(1 \text{ to } 4) - V0}{V0}\right) \times 100\%$$

Fig.5 Differential gain measurement conditions.

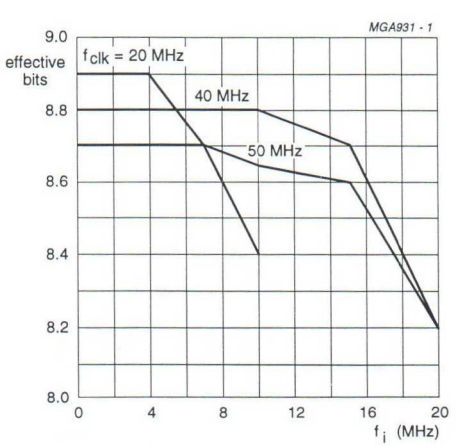


Fig.6 Typical effective bits under differential input mode as a function of input signal frequency.

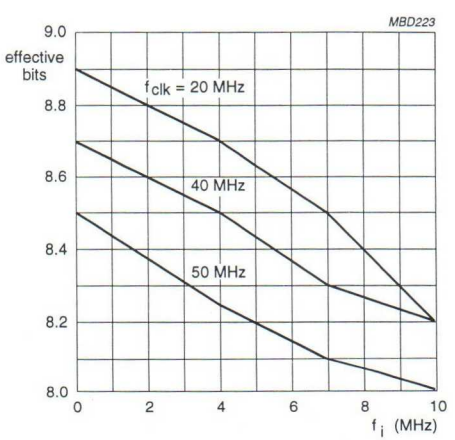
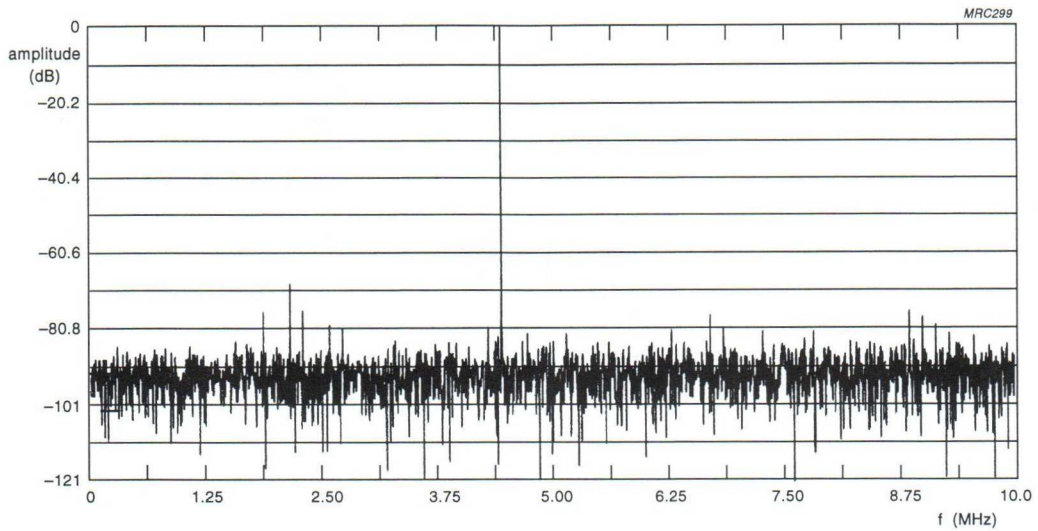
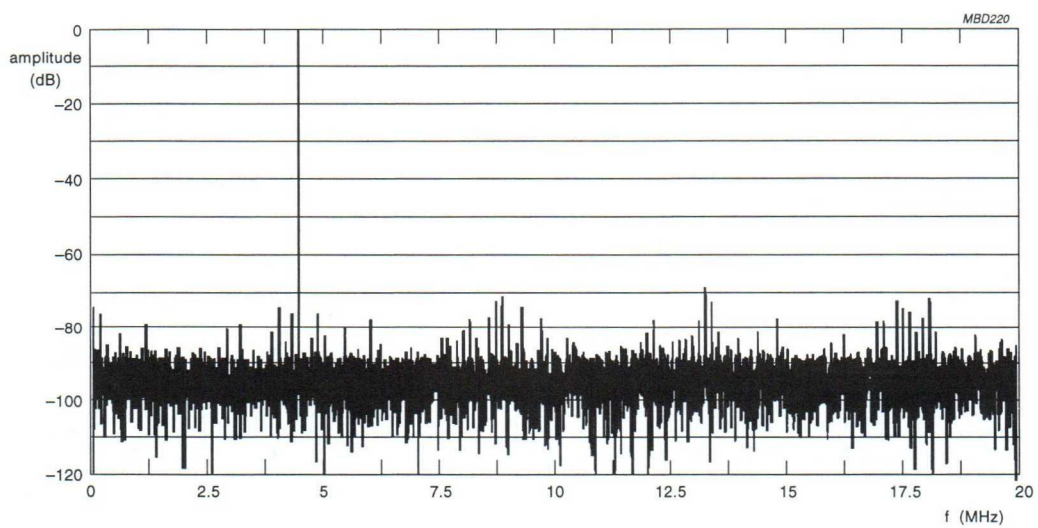


Fig.7 Typical effective bits under single input mode as a function of input signal frequency.



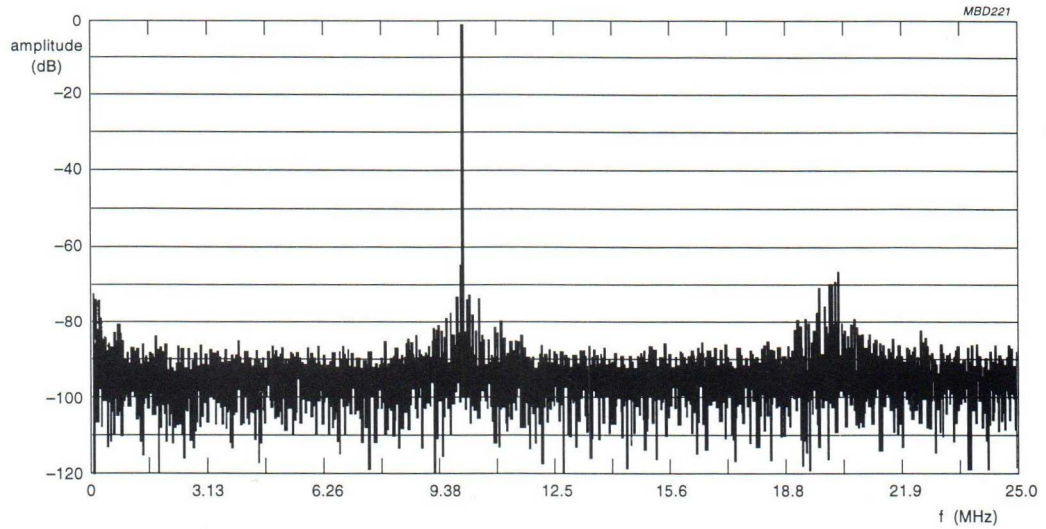
Effective bits: 9.1; THD = −65.81 dB;
Harmonic levels (dB): 2nd = −75.54; 3rd = −76.29; 4th = −74.90; 5th = −67.50; 6th = −90.87.

Fig.8 Fast Fourier Transformer (f_{clk} = 20 MHz; f_i = 4.43 MHz); for differential input mode.



Effective bits: 8.92; THD = −65.86 dB;
Harmonic levels (dB): 2nd = −70.92; 3rd = −68.48; 4th = −75.32; 5th = − 81.40; 6th = −72.69.

Fig.9 Fast Fourier Transformer (f_{clk} = 40 MHz; f_i = 4.43 MHz); for differential input mode.



Effective bits: 8.73; THD = −66.03 dB;
Harmonic levels (dB): 2nd = −69.50; 3rd = −70.57; 4th = −82.71; 5th = − 73.54; 6th = −71.83.

Fig.10 Fast Fourier Transformer (f_{clk} = 50 MHz; f_i = 10 MHz); for differential input mode.

INTERNAL PIN CONFIGURATION

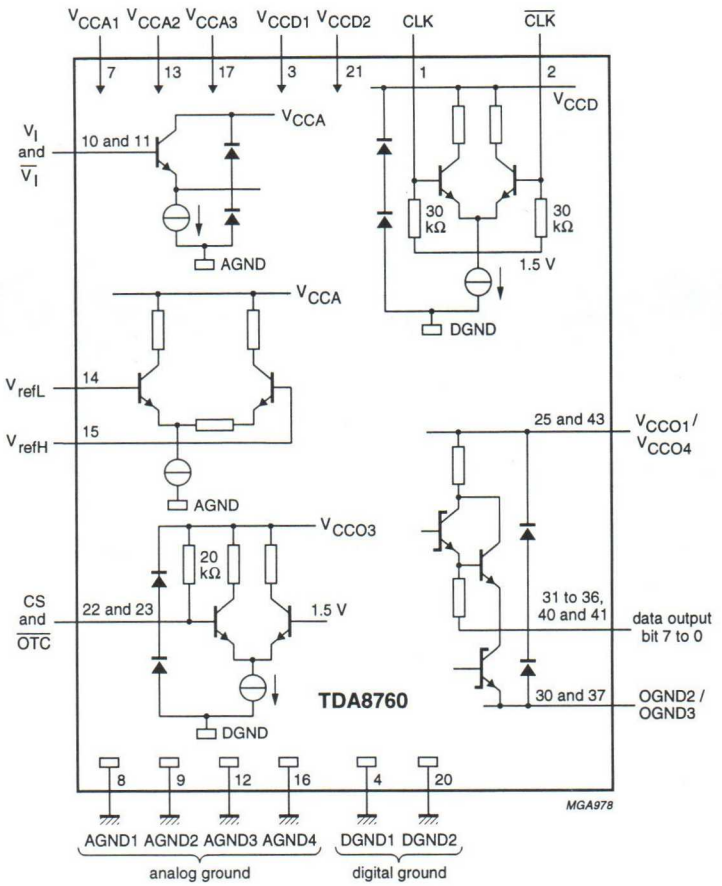
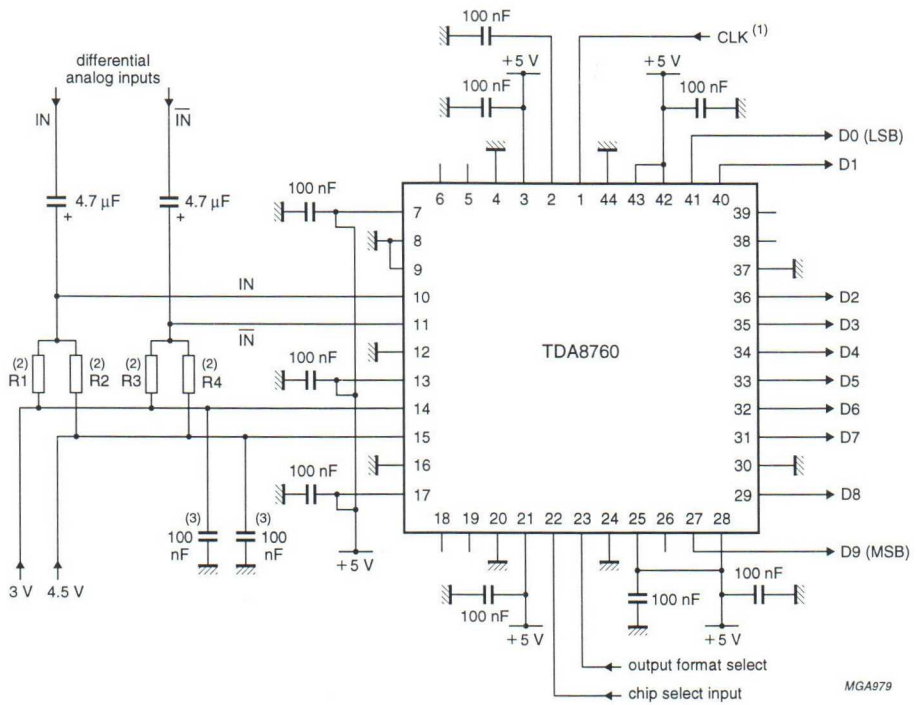


Fig.11 Description of input and output circuitry.

APPLICATION INFORMATION



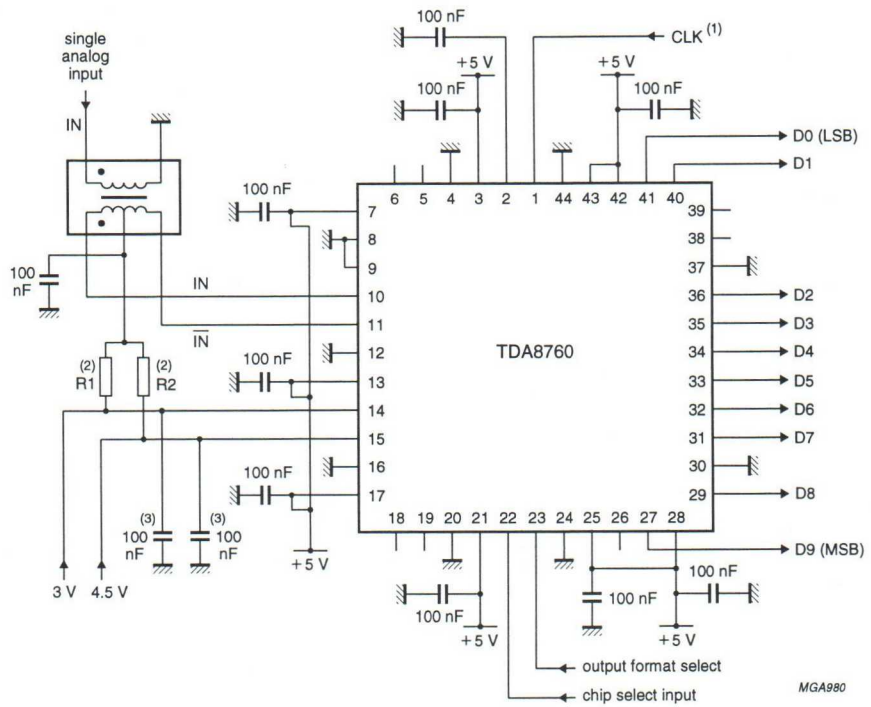
The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

(2) R1 and R2 must be determined in order to obtain a middle voltage of 3.4 V; see Table 1.

(3) V_{refH} and V_{refL} must be decoupled to AGND.

Fig.12 Application diagram for differential input mode.



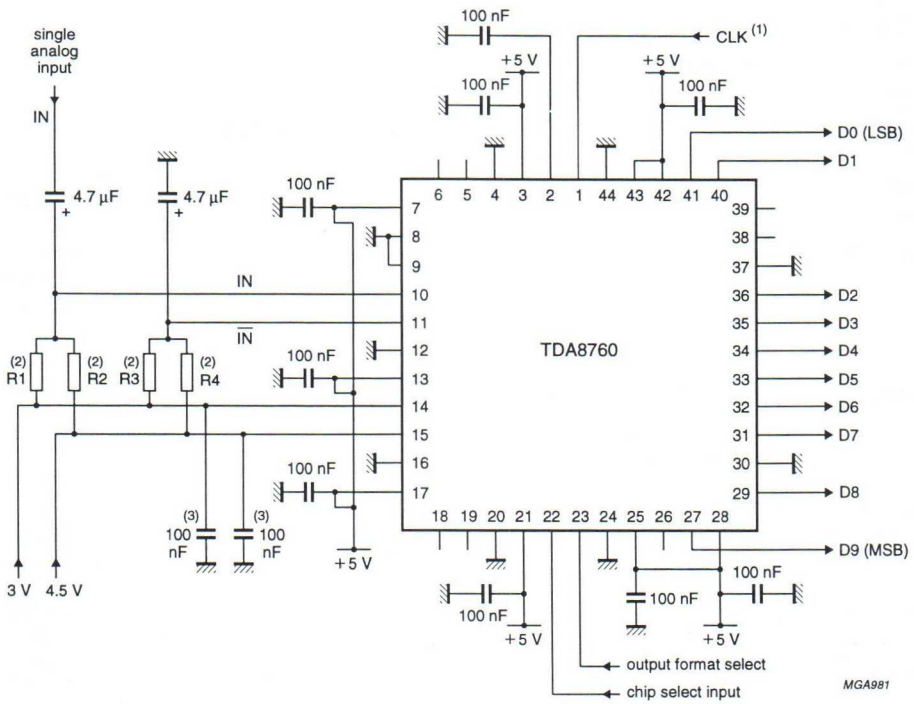
The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

(2) R1 and R2 must be determined in order to obtain 3.4 V at the transformer; see Table 1. Adaptation with the single input signal impedance must be taken care of.

(3) V_{refH} and V_{refL} must be decoupled to AGND.

Fig.13 Application diagram for differential input mode using an input transformer.



The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

(2) R1 = R3; R2 = R4. R1, R2, R3 and R4 must be determined in order to obtain a middle voltage of 3.7 V; see Table 2.

(3) V_{refH} and V_{refL} must be decoupled to AGND.

Fig.14 Application diagram for single input mode.

9-bit analog-to-digital converter for digital video

TDA8761

FEATURES

- 9-bit resolution
- Sampling rate up to 30 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (8.5 effective bits at 10 MHz full-scale input at f_{clk} = 30 MHz
- No missing codes guaranteed
- In range (IR) 3-state TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 360 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

Analog-to-digital conversion for:

- Video data digitizing
- Digital Video Broadcasting (DVB)
- Cable TV.

GENERAL DESCRIPTION

The TDA8761 is a 9-bit analog-to-digital converter (ADC) for professional video and digital video set box applications. It converts the analog input signal into 9-bit binary-coded digital words at a maximum sampling rate of 30 MHz. Its linearity performance ensures the required conversion accuracy in case of 256QAM demodulator concept and for all symbol frequencies. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output stages supply current		–	22	tbf	mA
AINL	AC integral non-linearity	note 1; full scale input sine wave	–	±0.75	tbf	LSB
		note 1; 50% full scale input sine wave	–	±0.5	tbf	LSB
ADNL	AC differential non-linearity	note 1; full scale input sine wave	–	±0.5	tbf	LSB
		note 1; 50% full scale input sine wave	–	±0.3	tbf	LSB
$f_{clk(max)}$	maximum clock frequency		30	–	–	MHz
P_{tot}	total power dissipation		–	360	tbf	mW

Note

1. f_i = 11 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8761M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM

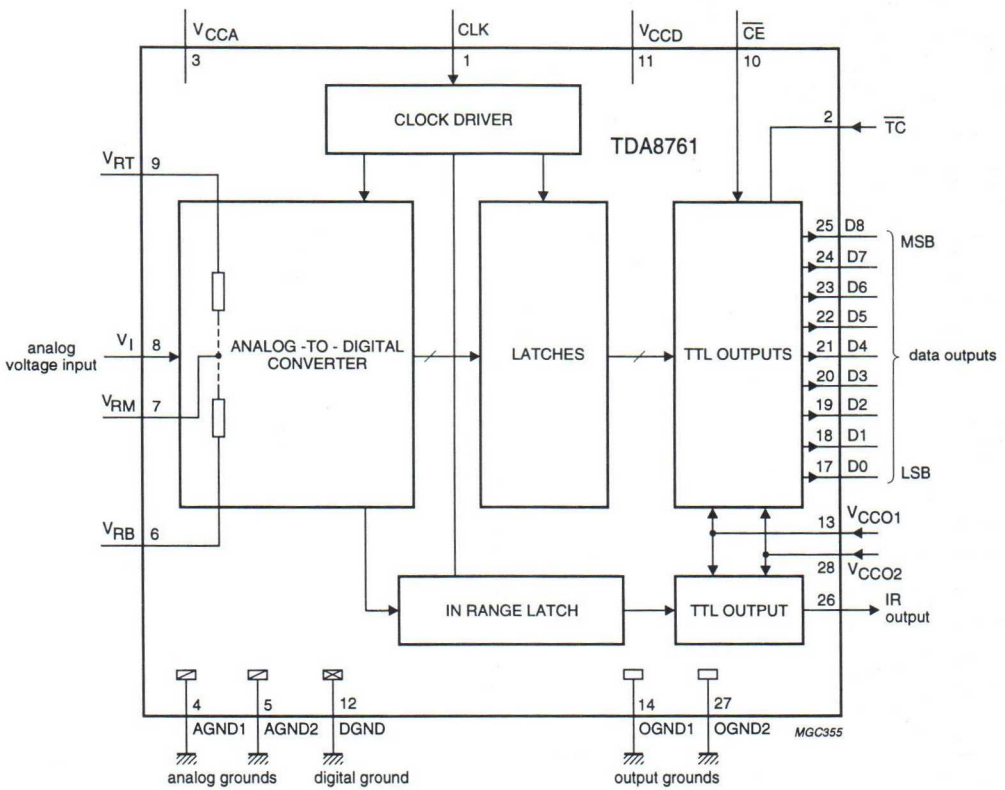


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (+5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{CE}$	10	chip enable input (TTL level input, active LOW)
V_{CCD}	11	digital supply voltage (+5 V)
DGND	12	digital ground
V_{CCO1}	13	supply voltage for output stages 1 (+5 V)
OGND1	14	output ground 1
n.c.	15	not connected
n.c.	16	not connected
D0	17	data output; bit 0 (LSB)
D1	18	data output; bit 1
D2	19	data output; bit 2
D3	20	data output; bit 3
D4	21	data output; bit 4
D5	22	data output; bit 5
D6	23	data output; bit 6
D7	24	data output; bit 7
D8	25	data output; bit 8 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
V_{CCO2}	28	supply voltage for output stages 2 (+5 V)

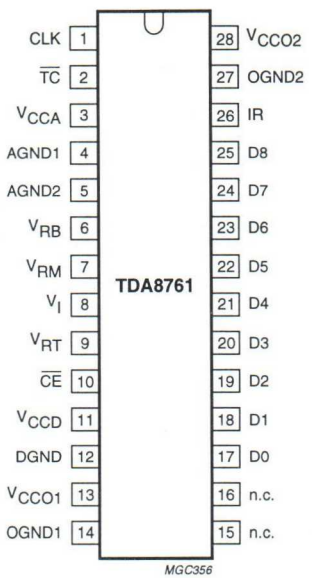


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between				
	V_{CCA} and V_{CCD}		−1.0	+1.0	V
	V_{CCO} and V_{CCD}		−1.0	+1.0	V
	V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{i(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided the difference between V_{CCA}, V_{CCD} and V_{CCO} is between −1 and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	110	K/W

CHARACTERISTICS

$V_{CCA} = V_3$ to V_4 and V_5 = 4.75 to 5.25 V; $V_{CCD} = V_{11}$ to V_{12} = 4.75 to 5.25 V; $V_{CCO} = V_{13}$ and V_{28} to V_{14} and V_{27} = 4.4 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; $V_{i(p-p)}$ = 1.5 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
ΔV_{CC}	supply voltage differences between					
	V_{CCA} and V_{CCD}		−0.25	–	+0.25	V
	V_{CCA} and V_{CCO}		−0.4	–	+0.4	V
	V_{CCD} and V_{CCO}		−0.4	–	+0.4	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output stages supply current		–	22	tbf	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−1	0	+1	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	µA
Z_I	input impedance	f_{clk} = 30 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 30 MHz	–	2	–	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	V_I = 1.3 V	–	0	–	µA
I_{IH}	HIGH level input current	V_I = 3.8 V	–	70	–	µA
Z_I	input impedance	f_i = 10 MHz	–	5	–	kΩ
C_I	input capacitance	f_i = 10 MHz	–	8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	–	V
V_{RT}	reference voltage TOP		–	3.3	V_{CCA} – 0.8 V	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.0	3.0	V
I_{ref}	reference current		–	30	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1.86	–	ppm
V_{osB}	offset voltage BOTTOM	note 2	–	250	–	mV
V_{osT}	offset voltage TOP	note 2	–	250	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.3	1.5	2.5	V
Outputs						
DIGITAL OUTPUTS D8 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
		I_O = 0 mA	2.7	–	V_{CCO} – 0.5	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.7	–	V_{CCO} – 1.3	V
		I_O = –1 mA	2.4	–	V_{CCO} – 1.4	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{clk(max)}$	maximum clock frequency		30	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		10	–	–	ns
Analog signal processing						
LINEARITY						
AINL	AC integral non-linearity	note 5; full scale input sine wave	–	±0.75	tbf	LSB
		note 5; 50% full scale input sine wave	–	±0.5	tbf	LSB
ADNL	AC differential non-linearity	note 5; full scale input sine wave	–	±0.5	tbf	LSB
		note 5; 50% full scale input sine wave	–	±0.3	tbf	LSB
OFER	offset error	middle code; V_{RB} = 1.3 V; V_{RT} = 3.3 V	–	±1	–	LSB
GER	gain error (from device to device)	V_{RB} = 1.3 V; V_{RT} = 3.3 V; note 4	–	±0.1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH (f_{clk} = 30 MHz)						
B	analog bandwidth	full-scale sine wave; note 6	–	40	–	MHz
		75% full-scale sine wave; note 6	–	55	–	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 256; note 6	–	700	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.5; note 7	–	2.0	tbf	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.5; note 7	–	2.5	tbf	ns
HARMONICS (f_{clk} = 30 MHz)						
THD	total harmonic distortion	f_i = 10 MHz	–	–64	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.7; note 8						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 30 MHz; f_i = 10 MHz	53	55	–	dB
EFFECTIVE BITS; see Fig 6; note 8						
EB	effective bits	f_{clk} = 30 MHz; f_i = 10 MHz	–	8.5	–	bits
TWO-TONE; note 9						
TTIR	two-tone intermodulation rejection	f_{clk} = 30 MHz	–	–64	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 30 MHz; f_i = 10 MHz; V_I = ±16 LSB at code 256	–	10^{-11}	–	times/ sample
DIFFERENTIAL GAIN; note 10						
G_{diff}	differential gain	f_{clk} = 30 MHz; PAL modulated ramp	–	tbf	–	%
DIFFERENTIAL PHASE; note 10						
φ_{diff}	differential phase	f_{clk} = 30 MHz; PAL modulated ramp	–	tbf	–	deg
Timing (f_{clk} = 30 MHz; C_L = 15 pF); see Fig.3; note 11						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	10	14	ns
C_L	digital output load		–	15	40	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	tbf	tbf	ns
t_{dZL}	enable LOW		–	tbf	tbf	ns
t_{dHZ}	disable HIGH		–	tbf	tbf	ns
t_{dLZ}	disable LOW		–	tbf	tbf	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
2. Analog input voltages producing code 0 up to and including code 511:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 511 at T_{amb} = 25 °C.
3. Analog input voltage range can be derived from $V_{RT} - V_{RB}$ difference. It is $\frac{(V_{RT} - V_{RB}) \times 8}{9}$
4. $GER = \frac{(V_{511} - V_0) - 1.5\ V}{1.5\ V} \times 100$
5. f_i = 11 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
9. Intermodulation measured relative to either tone with analog input frequencies of 10.0 MHz and 10.10 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
10. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
11. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.3 V)

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS									TWO'S COMPLEMENT OUTPUT BITS								
			D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.55	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
510	.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
511	3.05	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
O/F	>3.05	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D8 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

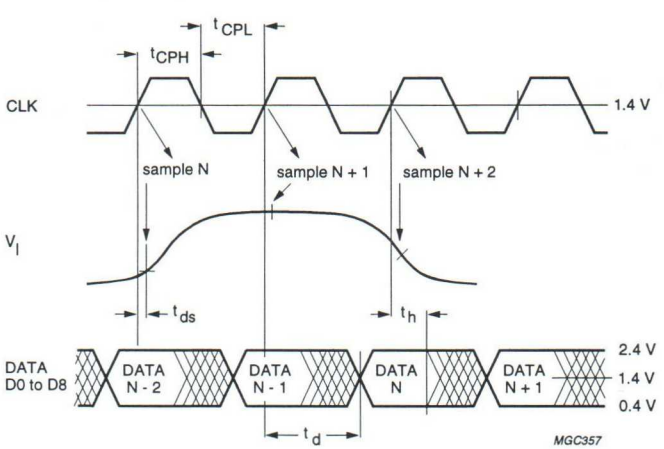
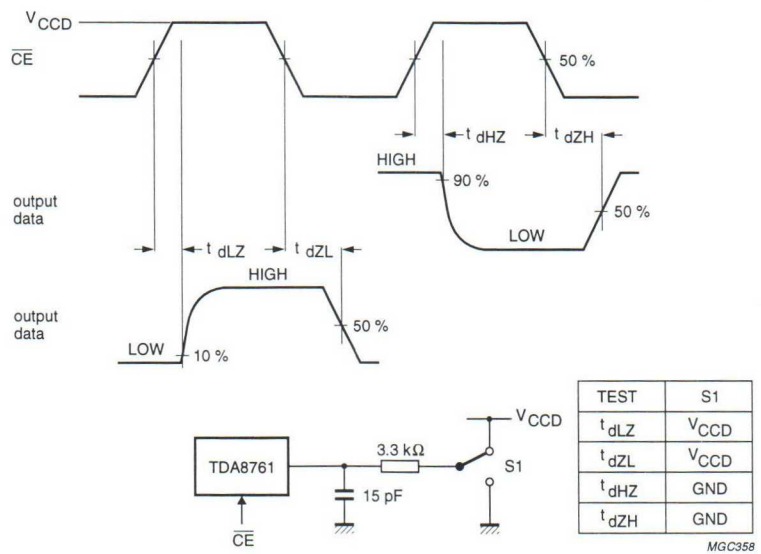


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

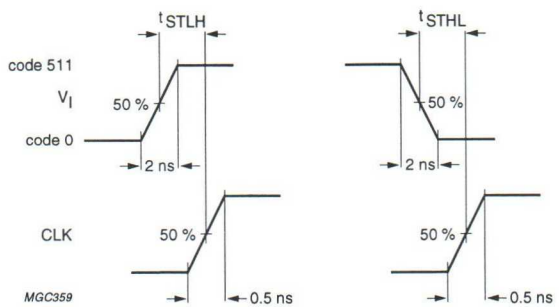
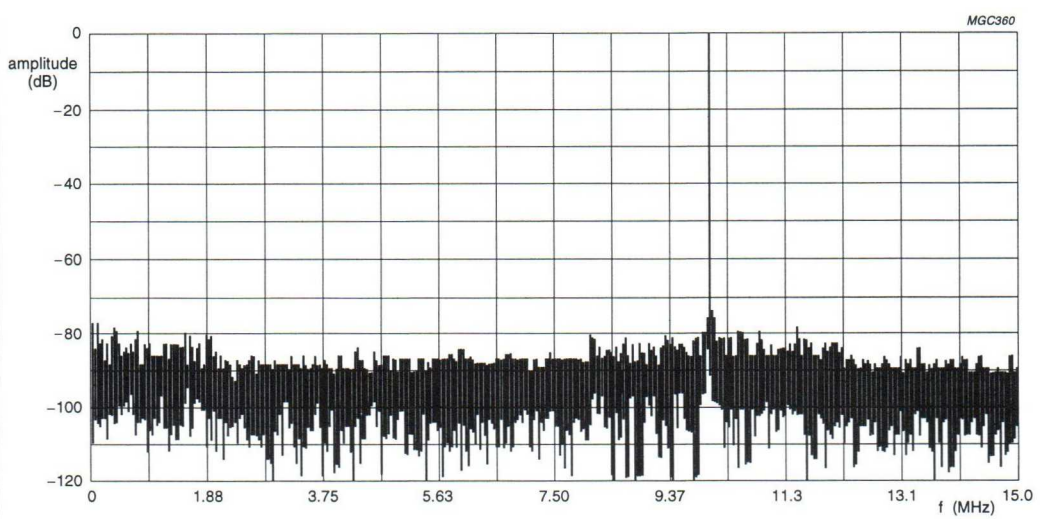


Fig.5 Analog input settling-time diagram.



Effective bits: 8.58; THD = −61.80 dB;
Harmonic levels (dB): 2nd = −64.77; 3rd = −79.30; 4th = −71.90; 5th = −66.12; 6th = −82.29.

Fig.6 Fast Fourier Transform (f_{clk} = 30 MHz; f_i = 10 MHz).

INTERNAL PIN CONFIGURATIONS

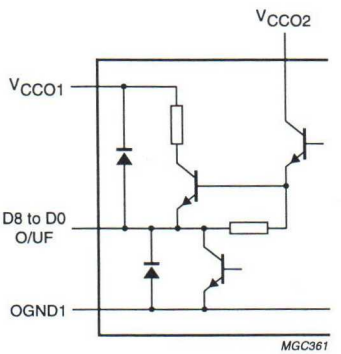


Fig.7 TTL data and in-range outputs.

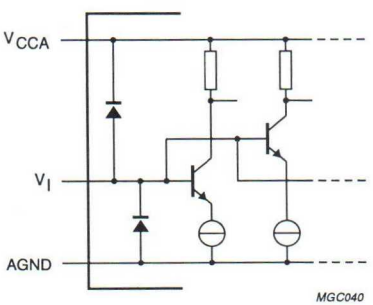


Fig.8 Analog inputs.

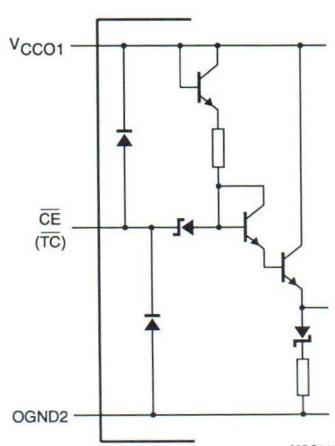


Fig.9 $\overline{CE}$ ($\overline{TC}$) 3-state input.

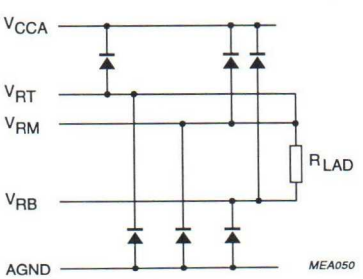


Fig.10 V_{RB}, V_{RM} and V_{RT}.

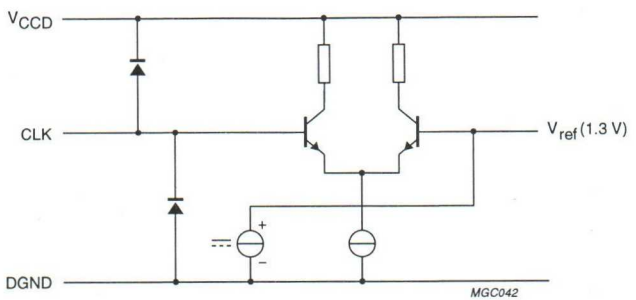
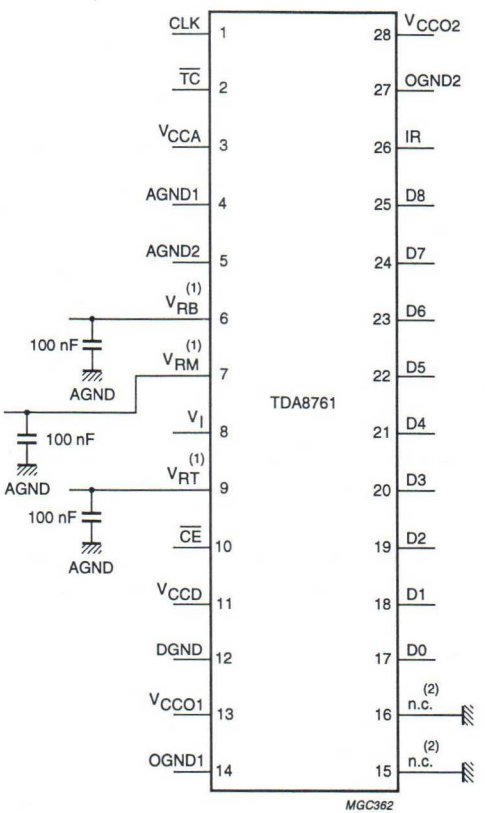


Fig.11 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{CCA} supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale, V_{RM} must be decoupled and connected to analog input signal (pin 8) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g. R = 5 kΩ and C = 100 nF).

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

(2) Pins 15 and 16 should be connected to DGND in order to prevent noise influence.

Fig.12 Application diagram.

10-bit high-speed low-power analog-to-digital converter

TDA8762

FEATURES

- 10-bit resolution
- Sampling rate up to 40 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.4 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz
- No missing codes guaranteed
- In range (IR) 3-state TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- ΣΔ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8762 is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	24	tbf	mA
I_{CCO}	output stages supply current		–	24	tbf	mA
INL	DC integral non-linearity		–	±0.8	tbf	LSB
DNL	DC differential non-linearity		–	±0.5	±0.9	LSB
AINL	AC integral non-linearity	note 1	–	±1.0	±2.0	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8762M/4		40	–	–	MHz
	TDA8762M/2		20	–	–	MHz
P_{tot}	total power dissipation		–	380	tbf	mW

Note

1. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 40 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8762M/4	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	40
TDA8762M/2	SSOP28		SOT341-1	20

BLOCK DIAGRAM

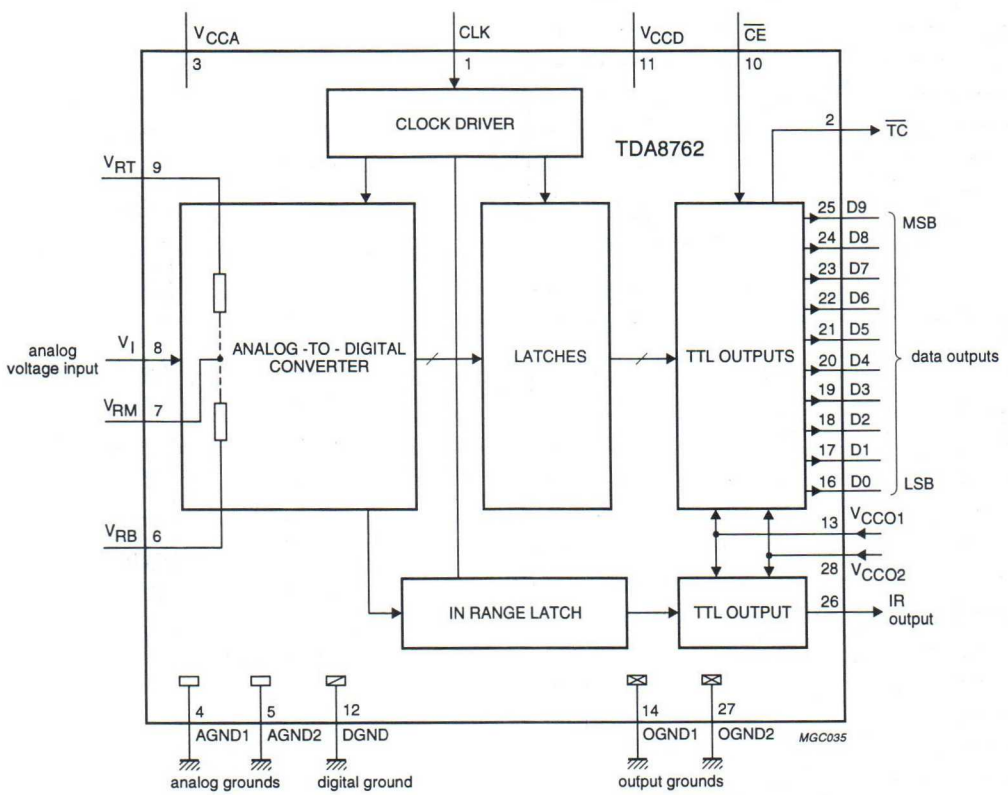


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (+5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{CE}$	10	chip enable input (TTL level input, active LOW)
V_{CCD}	11	digital supply voltage (+5 V)
DGND	12	digital ground
V_{CCO1}	13	supply voltage for output stages 1 (+5 V)
OGND1	14	output ground 1
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
V_{CCO2}	28	supply voltage for output stages 2 (+5 V)

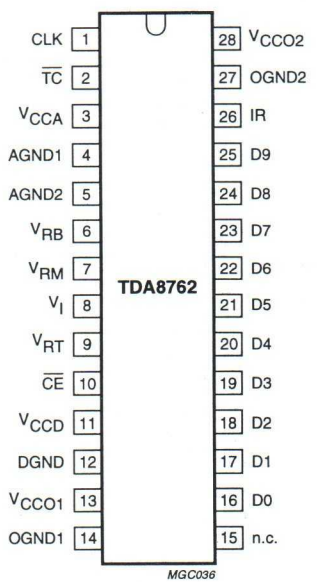


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided the difference between V_{CCA}, V_{CCD} and V_{CCO} is between −1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	110	K/W

CHARACTERISTICS

$V_{CCA} = V_3$ to V_4 and V_5 = 4.75 to 5.25 V; $V_{CCD} = V_{11}$ to V_{12} = 4.75 to 5.25 V; $V_{CCO} = V_{13}$ and V_{28} to V_{14} and V_{27} = 4.4 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; $V_{I(p-p)}$ = 2.0 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
ΔV_{CC}	voltage difference					
	$V_{CCA} - V_{CCD}$		−0.25	–	+0.25	V
	$V_{CCA} - V_{CCO}$		−0.4	–	+0.4	V
	$V_{CCD} - V_{CCO}$		−0.4	–	+0.4	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	24	tbf	mA
I_{CCO}	output stages supply current		–	24	tbf	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	−1	0	+1	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	μA
Z_I	input impedance	f_{clk} = 40 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 40 MHz	–	2	–	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	μA
V_i (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	V_i = 1.3 V	–	0	–	μA
I_{IH}	HIGH level input current	V_i = 3.8 V	–	70	–	μA
Z_I	input impedance	f_i = 4.43 MHz	–	5	–	kΩ
C_I	input capacitance	f_i = 4.43 MHz	–	8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	–	V
V_{RT}	reference voltage TOP		–	3.8	V_{CCA} – 0.8 V	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.5	3.0	V
I_{ref}	reference current		–	30	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1.86	–	mΩ/K
V_{osB}	offset voltage BOTTOM	note 2	–	250	–	mV
V_{osT}	offset voltage TOP	note 2	–	250	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.5	2.0	2.5	V
Outputs						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW level output voltage	I_O = 0 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.7	–	V_{CCO} – 0.5	V
		I_O = –0.4 mA	2.7	–	V_{CCO} – 1.3	V
		I_O = –1 mA	2.4	–	V_{CCO} – 1.4	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{clk(max)}$	maximum clock frequency					
	TDA8762/2		20	–	–	MHz
	TDA8762/4		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		8	–	–	ns
t_{CPL}	clock pulse width LOW		8	–	–	ns
Analog signal processing						
LINEARITY						
OFER	offset error	middle code; V_{RB} = 1.3 V; V_{RT} = 3.8 V	–	±1	–	LSB
GER	gain error (from device to device)	V_{RB} = 6.3 V; V_{RT} = 3.8 V; note 4	–	±0.1	–	%
INL	DC integral non-linearity		–	±0.8	tbf	LSB
DNL	DC differential non-linearity		–	±0.5	±0.9	LSB
AINL	AC integral non-linearity	note 5	–	±1.0	±2.0	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH (f_{clk} = 40 MHz)						
B	analog bandwidth	full-scale sine wave; note 6	–	40	–	MHz
		75% full-scale sine wave; note 6	–	55	–	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 512; note 6	–	700	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.5; note 7	–	2.0	tbf	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.5; note 7	–	2.5	tbf	ns
HARMONICS (f_{clk} = 40 MHz)						
h_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	–75	tbf	dB
	third harmonics		–	–72	tbf	dB
THD	total harmonic distortion	f_i = 4.43 MHz	–	–70	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.7; note 8						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	57	59	–	dB
EFFECTIVE BITS; see Figs 6, 7 and 8; note 8						
EB	effective bits TDA8762M/2	f_{clk} = 20 MHz				
		f_i = 4.43 MHz	–	9.5	–	bits
		f_i = 7.5 MHz	–	9.3	–	bits
	effective bits TDA8762M/4	f_{clk} = 40 MHz				
		f_i = 4.43 MHz	–	9.4	–	bits
		f_i = 7.5 MHz	–	9.2	–	bits
		f_i = 10 MHz	–	9.0	–	bits
		f_i = 15 MHz	–	8.7	–	bits
TWO-TONE; note 9						
TTIR	two-tone intermodulation rejection	f_{clk} = 40 MHz	–	–70	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 512	–	10^{-11}	–	times/ sample

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIFFERENTIAL GAIN; note 10						
G_{diff}	differential gain	f_{clk} = 40 MHz; PAL modulated ramp	–	tbf	–	%
DIFFERENTIAL PHASE; note 10						
φ_{diff}	differential phase	f_{clk} = 40 MHz; PAL modulated ramp	–	tbf	–	deg
Timing (f_{clk} = 40 MHz; C_L = 15 pF); see Fig.3; note 11						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	10	14	ns
C_L	digital output load		–	15	40	pF
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	tbf	tbf	ns
t_{dZL}	enable LOW		–	tbf	tbf	ns
t_{dHZ}	disable HIGH		–	tbf	tbf	ns
t_{dLZ}	disable LOW		–	tbf	tbf	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
2. Analog input voltages producing code 0 up to and including code 1023:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 1023 at T_{amb} = 25 °C.
3. Analog input voltage range can be derived from $V_{RT} - V_{RB}$ difference. It is $\frac{(V_{RT} - V_{RB}) \times 8}{9}$
4. $GER = \frac{(V_{1023} - V_0) - 2\ V}{2\ V} \times 100$
5. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 40 MHz).
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
9. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
10. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
11. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.8 V)

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS										TWO'S COMPLEMENT OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.55	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1.55	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1022	.	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
1023	3.55	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
O/F	>3.55	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D9 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

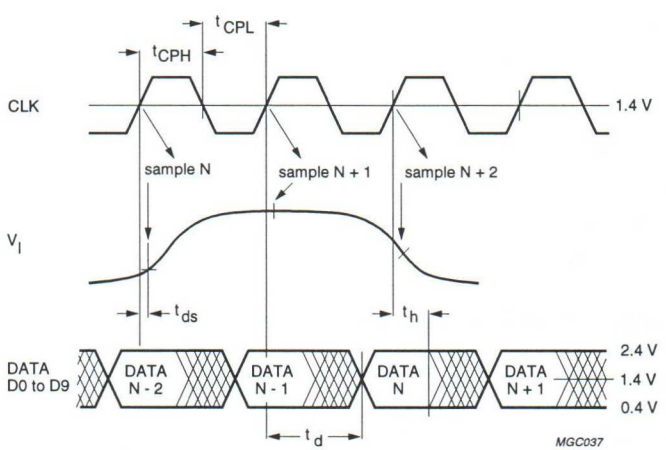
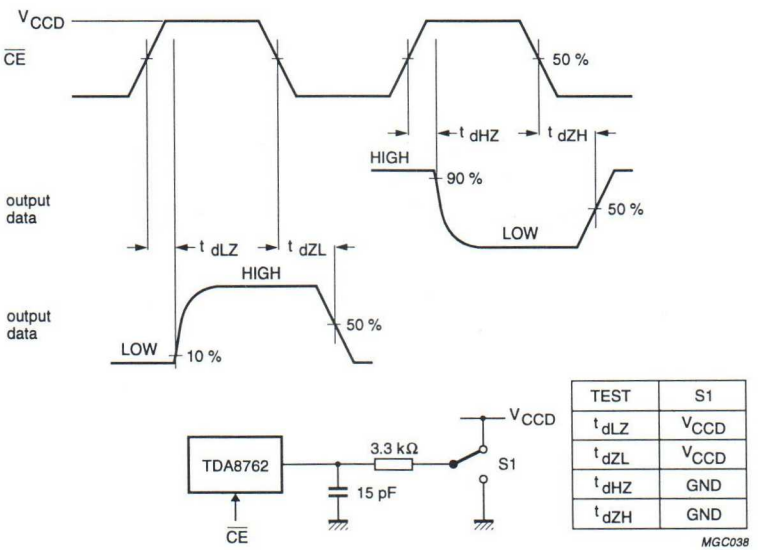


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

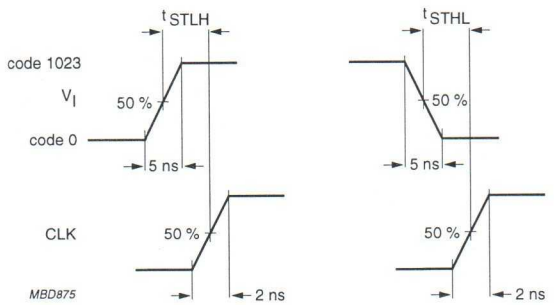
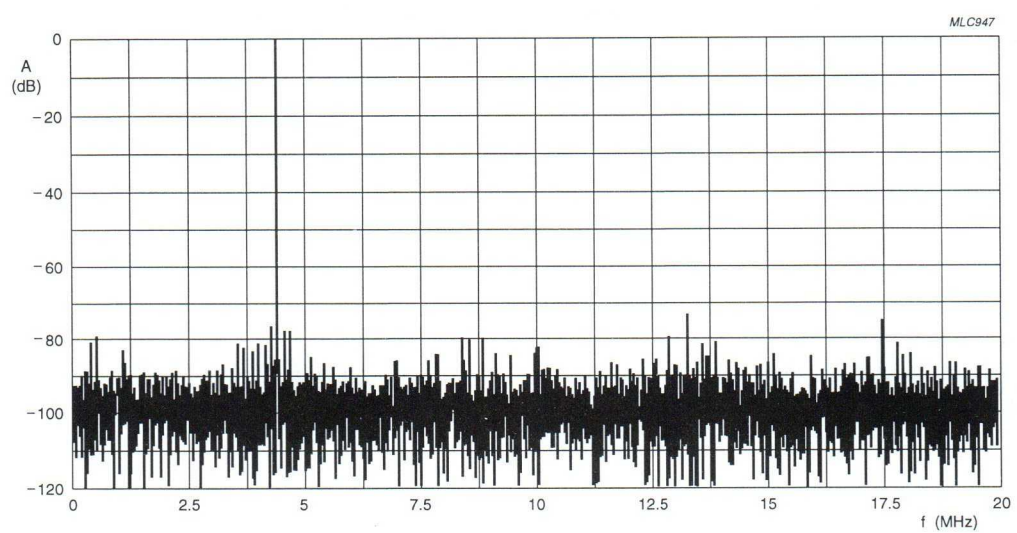
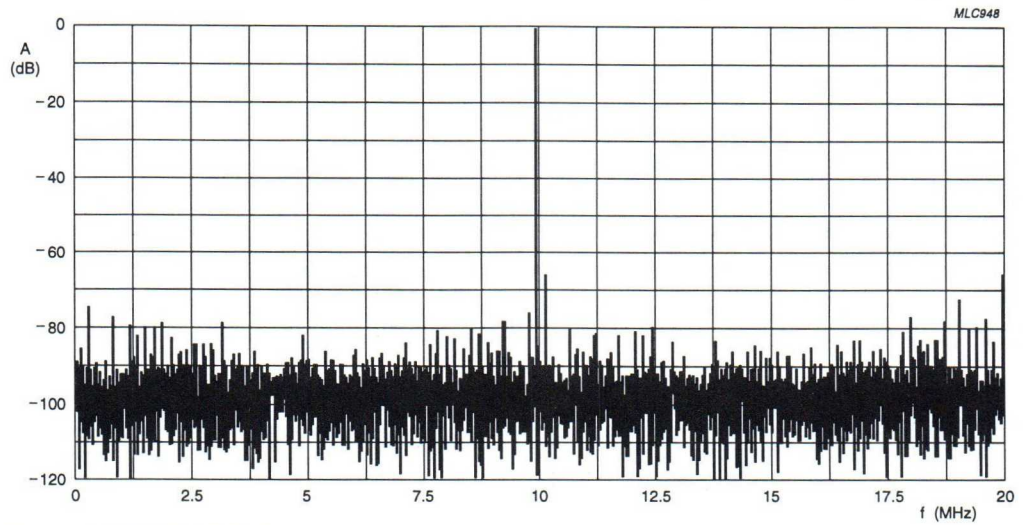


Fig.5 Analog input settling-time diagram.



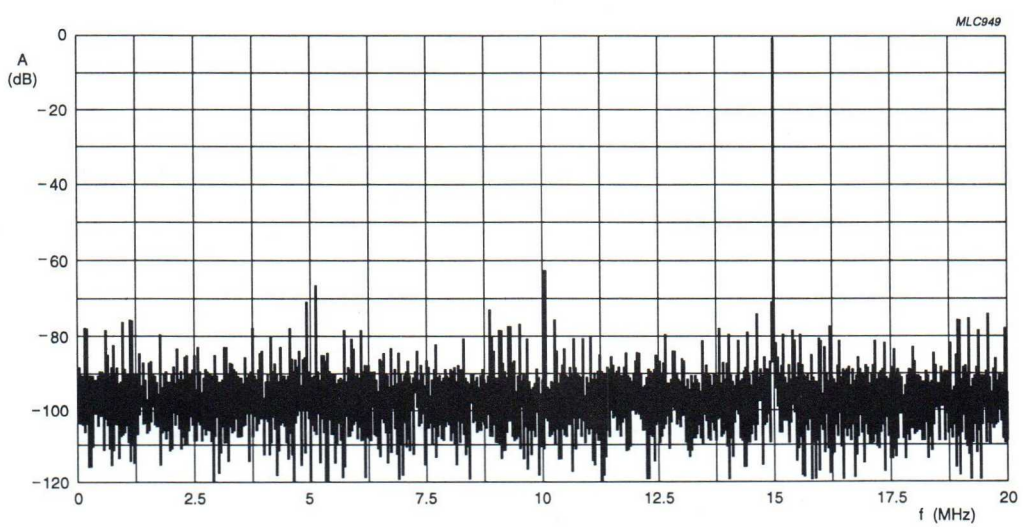
Effective bits: 9.46; THD = −71.19 dB;
Harmonic levels (dB): 2nd = −79.70; 3rd = −72.84; 4th = −81.54; 5th = −83.93; 6th = −86.47.

Fig.6 Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 4.43 MHz).



Effective bits: 9.11; THD = −63.18 dB;
Harmonic levels (dB): 2nd = −66.49; 3rd = −66.52; 4th = −85.15; 5th = −75.95; 6th = −83.47.

Fig.7 Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 10 MHz).



Effective bits: 8.70; THD = −60.18 dB;
Harmonic levels (dB): 2nd = −62.24; 3rd = −70.44; 4th = −77.29; 5th = −65.99; 6th = −89.67.

Fig.8 Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 15 MHz).

INTERNAL PIN CONFIGURATIONS

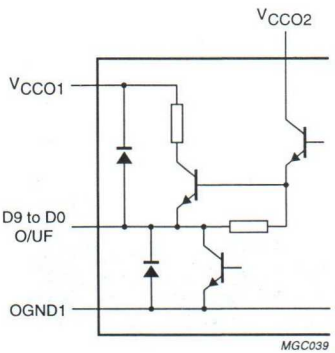


Fig.9 TTL data and in-range outputs.

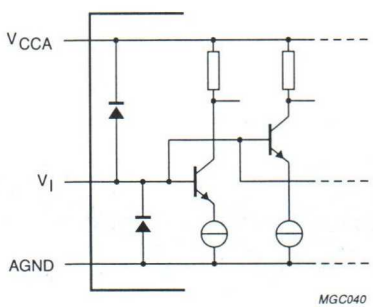


Fig.10 Analog inputs.

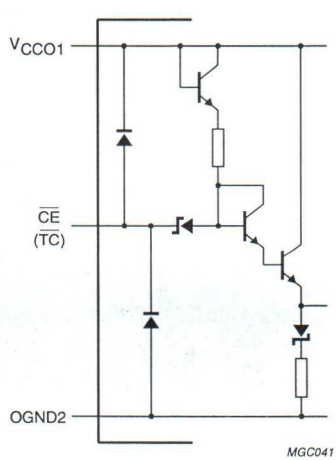


Fig.11 $\overline{CE}$ ($\overline{TC}$) 3-state input.

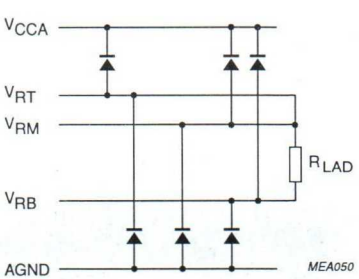


Fig.12 V_{RB}, V_{RM} and V_{RT}.

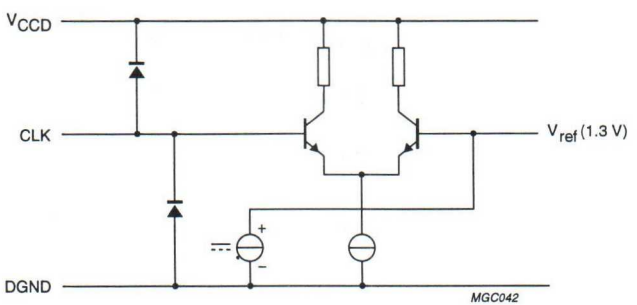
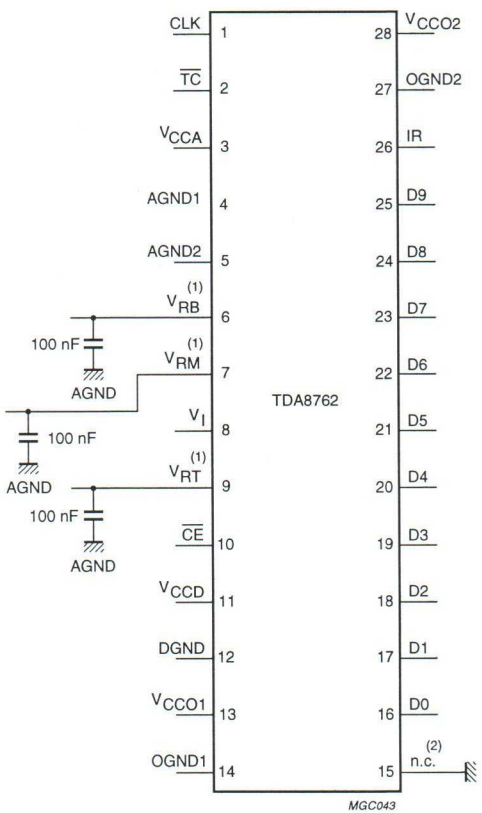


Fig.13 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{CCA} supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale, V_{RM} must be decoupled and connected to analog input signal (pin 8) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g. R = 5 kΩ and C = 100 nF).

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

(2) Pin 15 should be connected to DGND in order to prevent noise influence.

Fig.14 Application diagram.

10-bit high-speed 3 V analog-to-digital converter

TDA8766

FEATURES

- 10-bit resolution
- 3 V operation
- Sampling rate up to 20 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 1.0 MHz full-scale input at f_{clk} = 20 MHz)
- In range (IR) 3-state CMOS output
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 66 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Standby mode
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

GENERAL DESCRIPTION

The TDA8766 is a 10-bit high-speed 3 V analog-to-digital converter (ADC) for professional video and other applications. It converts at 3 V operation the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 20 MHz. All digital inputs and outputs are CMOS compatible. A standby mode allows reduction of the device power consumption down to 4 mW.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.3	5.25	V
V_{DDD1}	digital supply voltage 1		2.7	3.3	5.25	V
V_{DDD2}	digital supply voltage 2		2.7	3.3	5.25	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.25	V
I_{DDA}	analog supply current		–	9	tbf	mA
I_{DDD}	digital supply current		–	8	tbf	mA
I_{DDO}	output stages supply current	f_{clk} = 20 MHz; C_L = 20 pF; ramp input	–	3	tbf	mA
INL	integral non-linearity	f_{clk} = 20 MHz; ramp input	–	±1	±2	LSB
DNL	differential non-linearity		–	±0.5	±0.9	LSB
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	–	66	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8766G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

BLOCK DIAGRAM

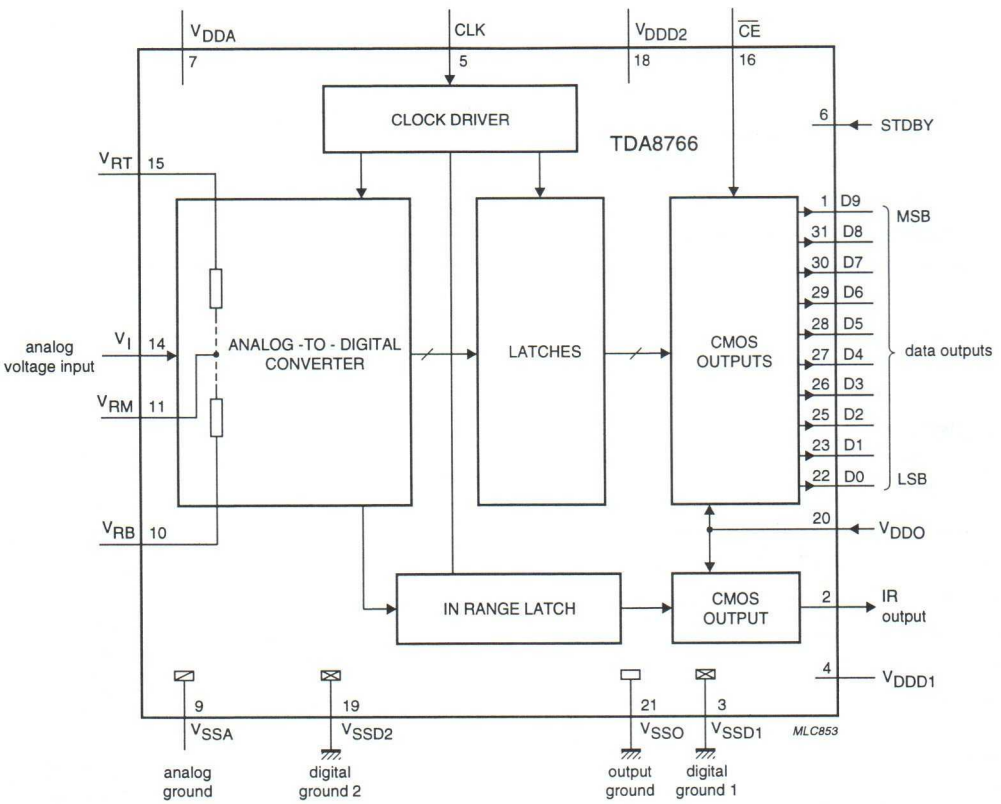


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D9	1	data output; bit 9 (MSB)
IR	2	in range data output
V_{SSD1}	3	digital ground 1
V_{DDD1}	4	digital supply voltage 1 (+3.3 V)
CLK	5	clock input
STDBY	6	standby mode input
V_{DDA}	7	analog supply voltage (+3.3 V)
n.c.	8	not connected
V_{SSA}	9	analog ground
V_{RB}	10	reference voltage BOTTOM input
V_{RM}	11	reference voltage MIDDLE
n.c.	12	not connected
n.c.	13	not connected
V_I	14	analog input voltage
V_{RT}	15	reference voltage TOP input
$\overline{CE}$	16	chip enable input
n.c.	17	not connected

SYMBOL	PIN	DESCRIPTION
V_{DDD2}	18	digital supply voltage 2 (+3.3 V)
V_{SSD2}	19	digital ground 2
V_{DDO}	20	positive supply voltage for output stage (+3.3 V)
V_{SSO}	21	digital output ground
D0	22	data output; bit 0 (LSB)
D1	23	data output; bit 1
n.c.	24	not connected
D2	25	data output; bit 2
D3	26	data output; bit 3
D4	27	data output; bit 4
D5	28	data output; bit 5
D6	29	data output; bit 6
D7	30	data output; bit 7
D8	31	data output; bit 8
n.c.	32	not connected

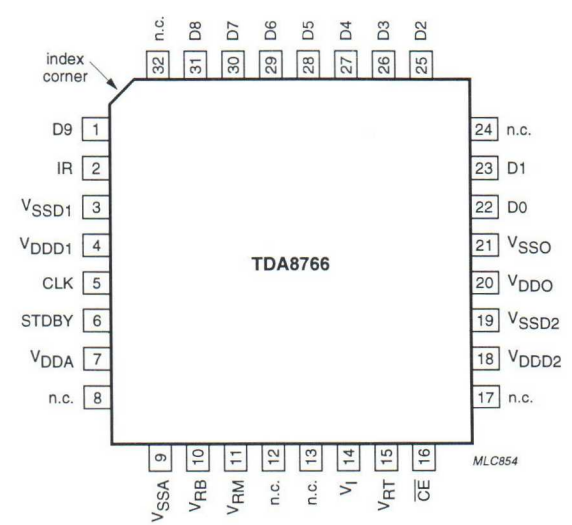


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{DDD1}, V_{DDD2}	digital supply voltages	note 1	−0.3	+7.0	V
V_{DDO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{DD1}	supply voltage differences between $\Delta V_{DD1} = V_{DDA} - V_{DDD}$		−1.0	+4.0	V
ΔV_{DD2}	supply voltage differences between $\Delta V_{DD2} = V_{DDD} - V_{DDO}$		−1.0	+4.0	V
ΔV_{DD3}	supply voltage differences between $\Delta V_{DD3} = V_{DDA} - V_{DDO}$		−1.0	+4.0	V
V_I	input voltage	referenced to V_{SSA}	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to V_{SSD}	−	V_{DDD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−20	+75	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{DDA}, V_{DDD} and V_{DDO} may have any value between −0.3 V and +7.0 V provided the difference between V_{DDA}, V_{DDD} and V_{DDO} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

CHARACTERISTICS

$V_{DDA} = V_7$ to $V_9 = 3.3$ V; $V_{DDD} = V_4$ to $V_3 = V_{18}$ to $V_{19} = 3.3$ V; $V_{DDO} = V_{20}$ to $V_{21} = 3.3$ V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(p-p)} = 1.84$ V; $C_L = 20$ pF; $T_{amb} = 0$ to +70 °C; typical values measured at $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		2.7	3.3	5.25	V
V_{DDD1}	digital supply voltage 1		2.7	3.3	5.25	V
V_{DDD2}	digital supply voltage 2		2.7	3.3	5.25	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.25	V
ΔV_{DD}	voltage difference					
	$V_{DDA} - V_{DDD}$		−0.2	–	+0.2	V
	$V_{DDA} - V_{DDO}$		−0.2	–	+3.0	V
	$V_{DDD} - V_{DDO}$		−0.2	–	+3.0	V
I_{DDA}	analog supply current		–	9	tbf	mA
I_{DDD}	digital supply current		–	8	tbf	mA
I_{DDO}	output stages supply current	$f_{clk} = 20$ MHz; ramp input; $C_L = 20$ pF	–	3	tbf	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO V_{SSD}); see note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4$ V	−1	0	+1	µA
I_{IH}	HIGH level input current	$V_{clk} = 2.7$ V	–	–	5	µA
Z_I	input impedance	$f_{clk} = 20$ MHz	–	4	–	kΩ
C_I	input capacitance	$f_{clk} = 20$ MHz	–	3	–	pF
INPUTS $\overline{CE}$ AND STDBY (REFERENCED TO V_{SSD}); see Table 3						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	−1	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	+1	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO V_{SSA})						
I_{IL}	LOW level input current	$V_I = V_{RB}$	–	0	–	µA
I_{IH}	HIGH level input current	$V_I = V_{RT}$	–	35	–	µA
Z_I	input impedance	$f_i = 1$ MHz	–	5	–	kΩ
C_I	input capacitance	$f_i = 1$ MHz	–	8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.1	1.2	–	V
V_{RT}	reference voltage TOP	$V_{TOP} \leq V_{DDA}$	2.7	3.3	3.8	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.5	2.1	2.7	V
I_{ref}	reference current		–	7.2	–	mA
R_{LAD}	resistor ladder		–	290	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1.86	–	ppm
V_{osB}	offset voltage BOTTOM	note 2	–	130	–	mV
V_{osT}	offset voltage TOP	note 2	–	130	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.4	1.84	2.4	V
Outputs						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO V_{SSD})						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{DDO}	V
		I_O = –0.4 mA; V_{DDO} > 4 V	3.5	–	V_{DDO}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{DDO}	–20	–	+20	µA
Switching characteristics						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
t_{CPH}	clock pulse width HIGH		15	–	–	ns
t_{CPL}	clock pulse width LOW		15	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	f_{clk} = 20 MHz; ramp input; see Fig.5	–	±1	±2	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; ramp input; see Fig.6	–	±0.5	±0.9	LSB
INPUT SET RESPONSE (f_{clk} = 20 MHz; see Fig.7; note 4)						
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave	–	4	6	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave	–	4	6	ns
HARMONICS; (f_{clk} = 20 MHz; see Fig.8; note 5)						
THD	total harmonic distortion	f_i = 1 MHz	–	–63	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.8; note 5						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 20 MHz; f_i = 1 MHz	–	60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS; see Fig.8; note 5						
EB	effective bits	f_{clk} = 20 MHz				
		f_i = 300 kHz	–	9.5	–	bits
		f_i = 1 MHz	–	9.3	–	bits
		f_i = 3.58 MHz	–	8.5	–	bits
DIFFERENTIAL GAIN; see note 6						
G_{diff}	differential gain	f_{clk} = 20 MHz; PAL modulated ramp	–	tbf	–	%
DIFFERENTIAL PHASE; see note 6						
φ_{diff}	differential phase	f_{clk} = 20 MHz; PAL modulated ramp	–	tbf	–	deg
Timing (f_{clk} = 20 MHz; C_L = 20 pF); see Fig.3; note 7						
t_{ds}	sampling delay time		–	–	5	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		8	12	16	ns
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	tbf	tbf	ns
t_{dZL}	enable LOW		–	tbf	tbf	ns
t_{dHZ}	disable HIGH		–	tbf	tbf	ns
t_{dLZ}	disable LOW		–	tbf	tbf	ns
Standby mode output delay times						
t_{dSTBLH}	standby (LOW-to-HIGH transition)		–	–	200	ns
t_{dSTBHL}	start-up (HIGH-to-LOW transition)		–	–	500	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 0 up to and including 1023:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 1023 at T_{amb} = 25 °C.
3. Analog input voltage range can be derived from $V_{RT} - V_{RB}$ difference. It is $\frac{(V_{RT} - V_{RB}) \times 8}{9}$
4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
5. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
6. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a DAC.
7. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to V_{SSA})

STEP	$V_{I(p-p)}$ (V)	IR	BINARY OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.33	0	0	0	0	0	0	0	0	0	0	0
0	1.33	1	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1022	.	1	1	1	1	1	1	1	1	1	1	0
1023	3.17	1	1	1	1	1	1	1	1	1	1	1
Overflow	>3.17	0	1	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{CE}$	D9 TO D0	IR
1	high impedance	high impedance
0	active; binary	active

Table 3 Standby selection

STDBY	D9 TO D0	$I_{DDA} + I_{DDD}$ (typ.)
1	last logic state	1.2 mA
0	active	17 mA

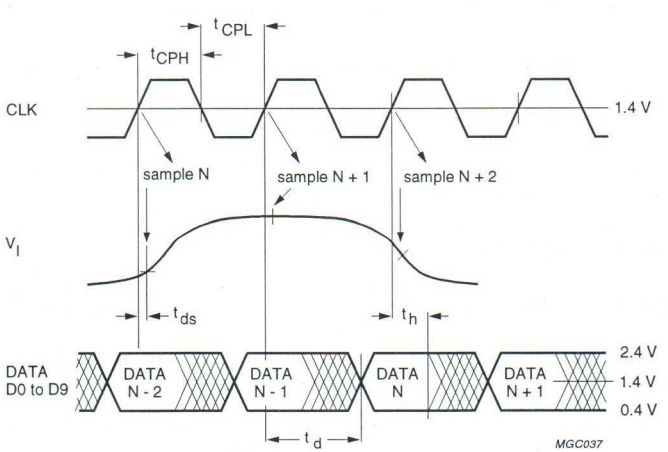
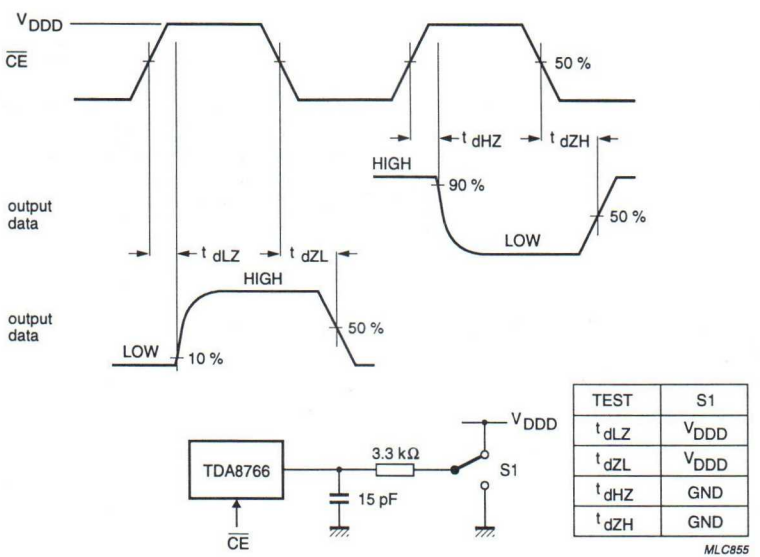


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{DDD}
t_{dZL}	V_{DDD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

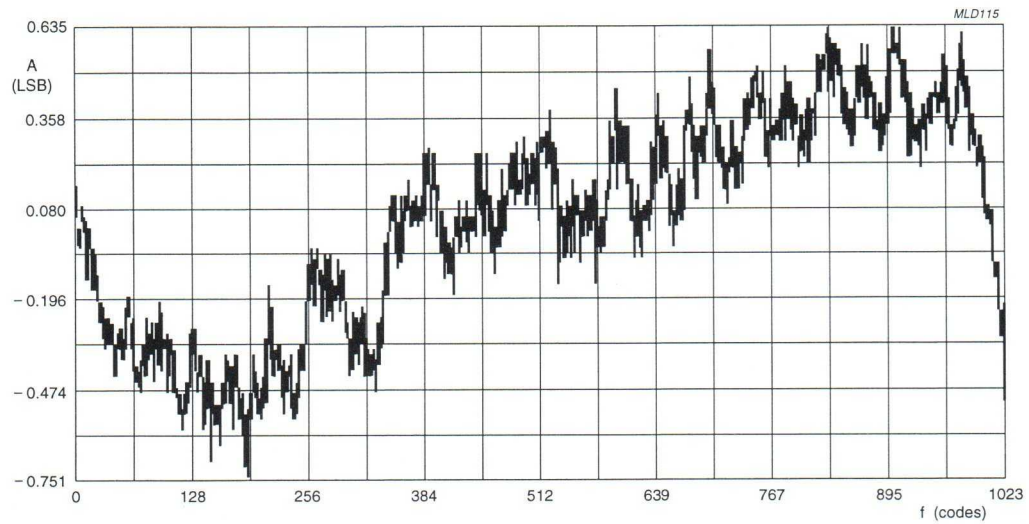


Fig.5 Typical integral non-linearity (INL) performance.

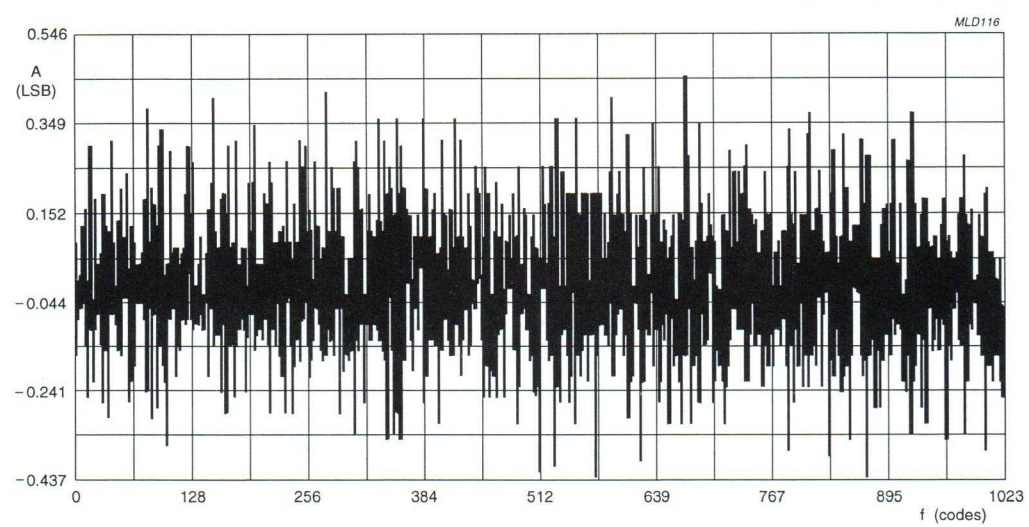


Fig.6 Typical differential non-linearity (DNL) performance.

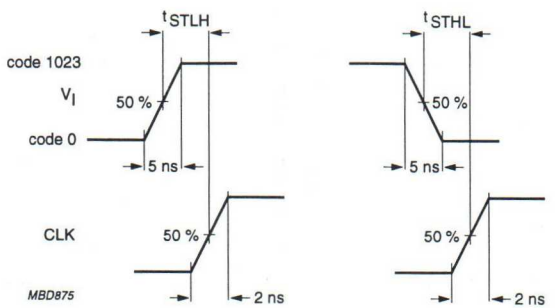
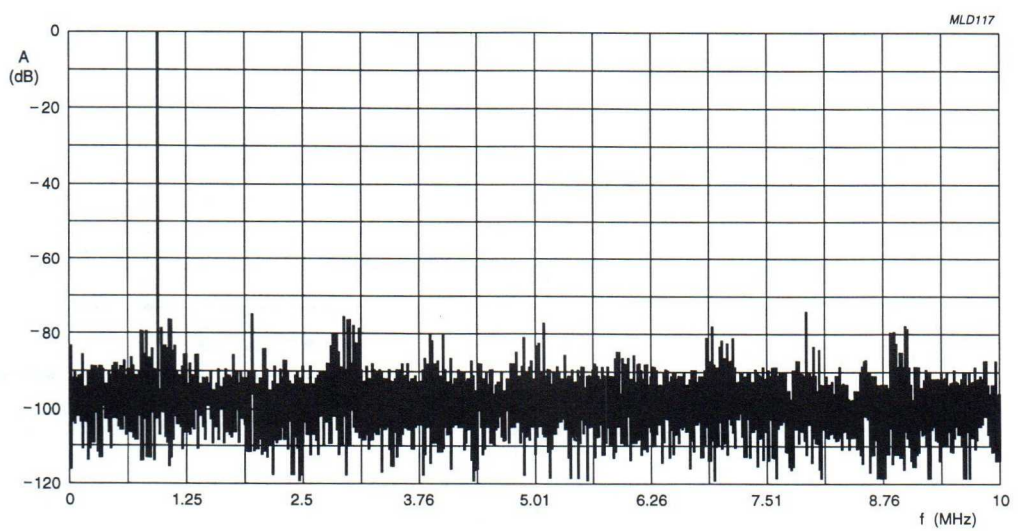


Fig.7 Analog input settling-time diagram.



Effective bits: 9.59; THD = 76.60 dB;
Harmonic levels (dB): 2nd = −81.85; 3rd = −87.56; 4th = −88.81; 5th = −88.96; 6th = −79.58.

Fig.8 Typical Fast Fourier Transform (f_{clk} = 20 MHz; f_i = 1 MHz).

INTERNAL PIN CONFIGURATIONS

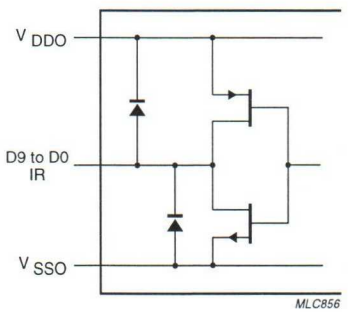


Fig.9 CMOS data and overflow/underflow outputs.

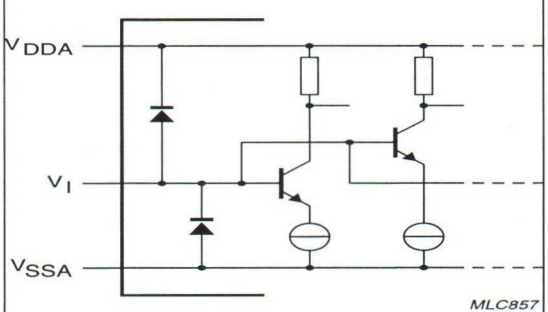


Fig.10 Analog inputs.

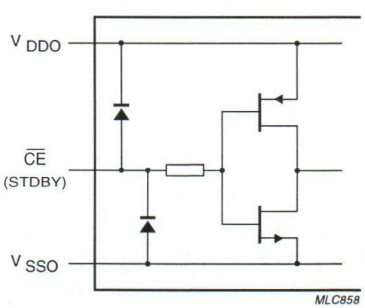


Fig.11 $\overline{CE}$ (STDBY) 3-state input.

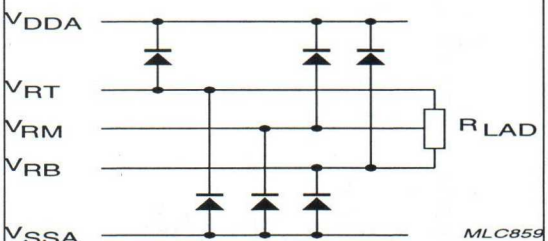


Fig.12 V_{RB}, V_{RM} and V_{RT}.

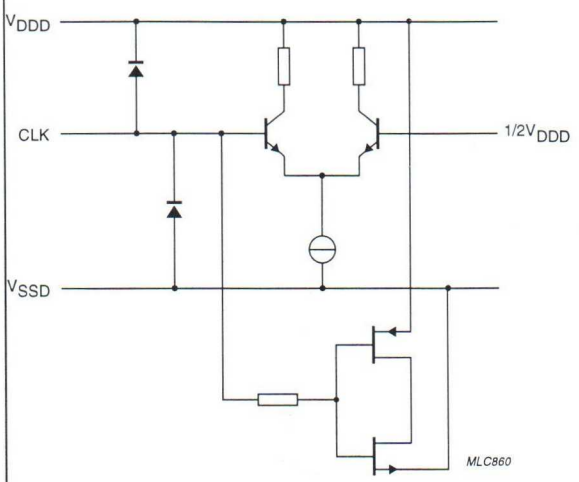
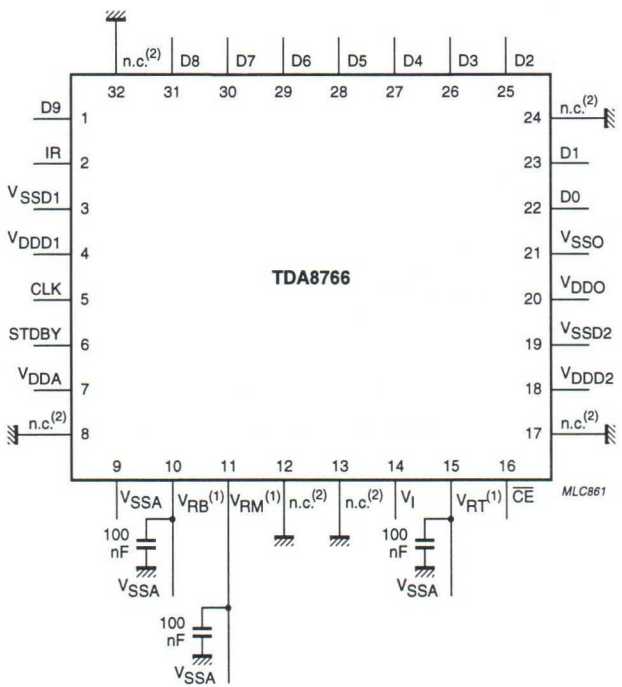


Fig.13 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{DDA} supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale, V_{RM} must be decoupled and connected to analog input signal (pin 14) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g. R = 5 kΩ and C = 100 nF).

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to V_{SSA}.

(2) Pins 8, 12, 13, 17, 24 and 32 should be connected to the closest ground pin in order to prevent noise influence.

Fig.14 Application diagram.

Triple 8-bit video digital-to-analog converter

TDA8771

FEATURES

- 8-bit resolution
- Sampling rate up to 35 MHz
- Internal reference voltage regulator
- No deglitching circuit required
- Large output voltage range
- 1 kΩ output load
- Power dissipation only 200 mW
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8771 is a triple 8-bit video digital-to-analog converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz.

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The device is fabricated in a 5 V, CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 1 kΩ; note 1	10	33	45	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	7	20	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
P_{tot}	total power dissipation	R_L = 1 kΩ; f_{clk} = 35 MHz; note 1	45	200	360	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8771H	44	QFP	plastic	SOT307-2

BLOCK DIAGRAM

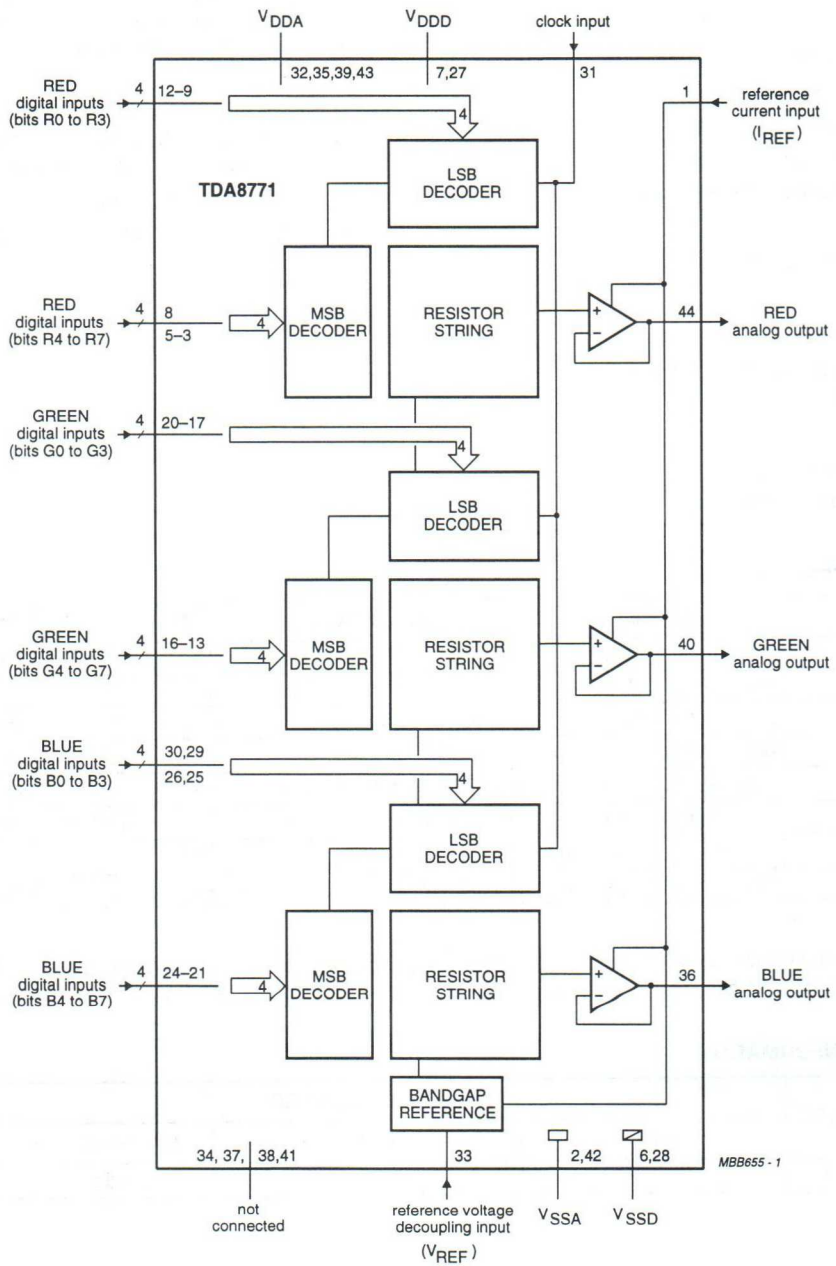


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I_{REF}	1	reference current input for output buffers
V_{SSA1}	2	analog supply ground 1
R7	3	RED digital input data; bit 7 (MSB)
R6	4	RED digital input data; bit 6
R5	5	RED digital input data; bit 5
V_{SSD1}	6	digital supply ground 1
V_{DDD1}	7	digital supply voltage 1
R4	8	RED digital input data; bit 4
R3	9	RED digital input data; bit 3
R2	10	RED digital input data; bit 2
R1	11	RED digital input data; bit 1
R0	12	RED digital input data; bit 0 (LSB)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
B7	21	BLUE digital input data; bit 7 (MSB)
B6	22	BLUE digital input data; bit 6
B5	23	BLUE digital input data; bit 5
B4	24	BLUE digital input data; bit 4
B3	25	BLUE digital input data; bit 3
B2	26	BLUE digital input data; bit 2
V_{DDD2}	27	digital supply voltage 2
V_{SSD2}	28	digital supply ground 2
B1	29	BLUE digital input data; bit 1
B0	30	BLUE digital input data; bit 0 (LSB)
CLK	31	clock input
V_{DDA1}	32	analog supply voltage 1
V_{REF}	33	decoupling input for reference voltage
n.c.	34	not connected
V_{DDA2}	35	analog supply voltage 2
OUTB	36	BLUE analog output
n.c.	37	not connected
n.c.	38	not connected
V_{DDA3}	39	analog supply voltage 3
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
V_{SSA2}	42	analog supply ground 2
V_{DDA4}	43	analog supply voltage 4
OUTR	44	RED analog output

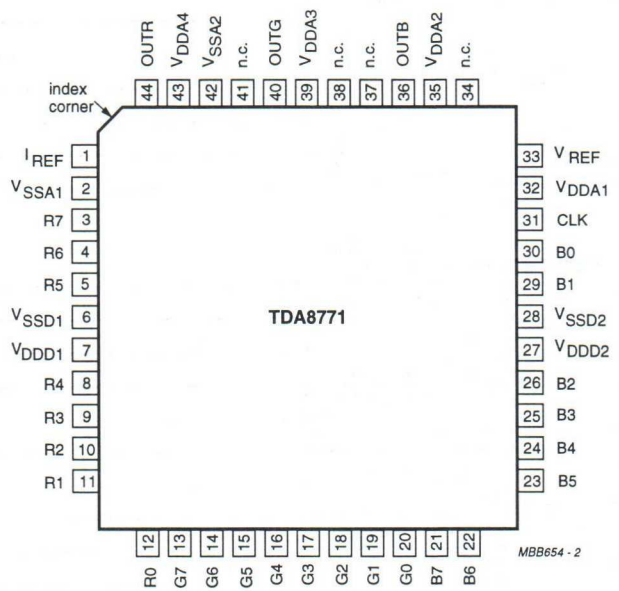


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 1$ kΩ; note 1	10	33	45	mA
I_{DDD}	digital supply current	$f_{clk} = 35$ MHz	–	7	20	mA
Inputs						
CLOCK INPUT (PIN 31)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
R, G, B DIGITAL INPUTS (PINS 12 TO 8, 5 TO 3, 20 TO 13, 30, 29 AND 26 TO 21)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{REF} REFERENCE CURRENT INPUT FOR OUTPUT BUFFERS (PIN 1)						
I_I	input current		–	0.6	0.7	mA
Timing; see Fig.3						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		8	–	–	ns
t_{CPL}	clock pulse width LOW		8	–	–	ns
t_r	clock rise time		–	–	5	ns
t_f	clock fall time		–	–	6	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		4	–	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{REF}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) FOR 1 kΩ LOAD; see Table 1						
FSR	full-scale output voltage range		2.80	2.95	3.10	V
V_{os}	offset of analog voltage output		–	0.25	–	V
V_{Omax}	maximum output voltage	data inputs = logic 1; note 2	2.95	3.20	3.45	V
V_{Omin}	minimum output voltage	data inputs = logic 0; note 2	0.05	0.25	0.45	V
THD	total harmonic distortion	$f_i = 4.43$ MHz; $f_{clk} = 35$ MHz	–	–44	–	dB
Z_L	output load impedance		0.9	1.0	1.1	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{clk} = 35 MHz)						
INL	integral non-linearity	ramp input	–	0.5	±1	LSB
DNL	differential non-linearity	ramp input	–	0.25	±0.5	LSB
α_{CT}	crosstalk DAC to DAC		–50	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (for 1 kΩ output load); see Fig.4						
t_d	input to 50% output delay time	full-scale change	–	12	–	ns
t_{s1}	settling time	10% to 90% of full-scale change	–	15	–	ns
t_{s2}	settling time	to ±1 LSB	–	50	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB·ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V_O is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 1 kΩ
0000 0000	0	0.262
0000 0001	1	0.273
....	.	.
1000 0000	128	1.731
....	.	.
1111 1110	254	3.188
1111 1111	255	3.200

TIMING

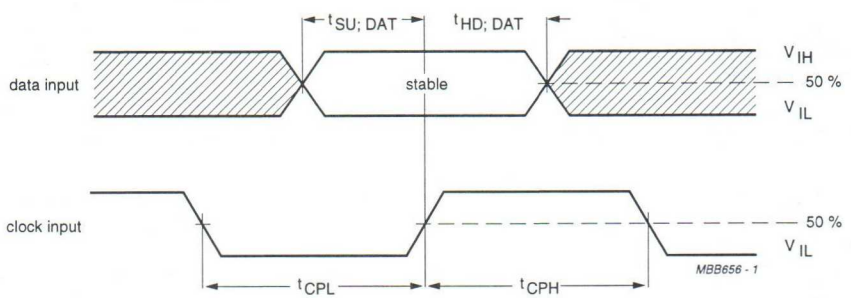


Fig.3 Input timing.

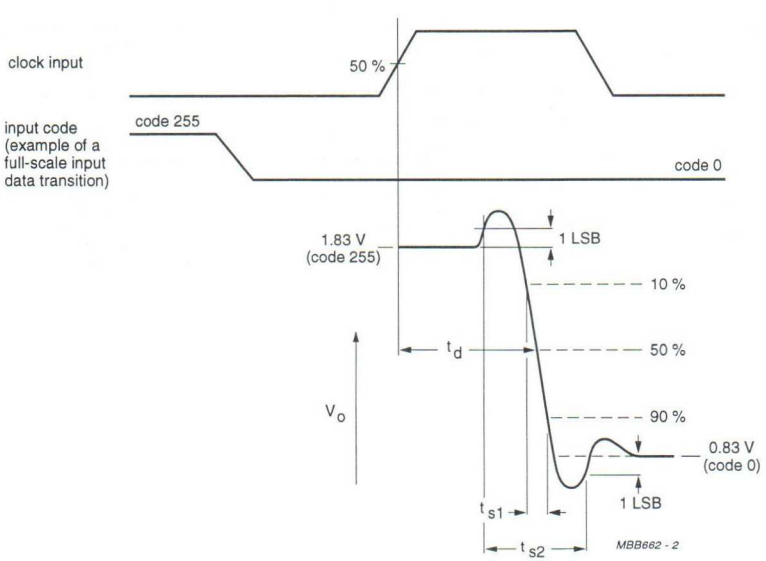
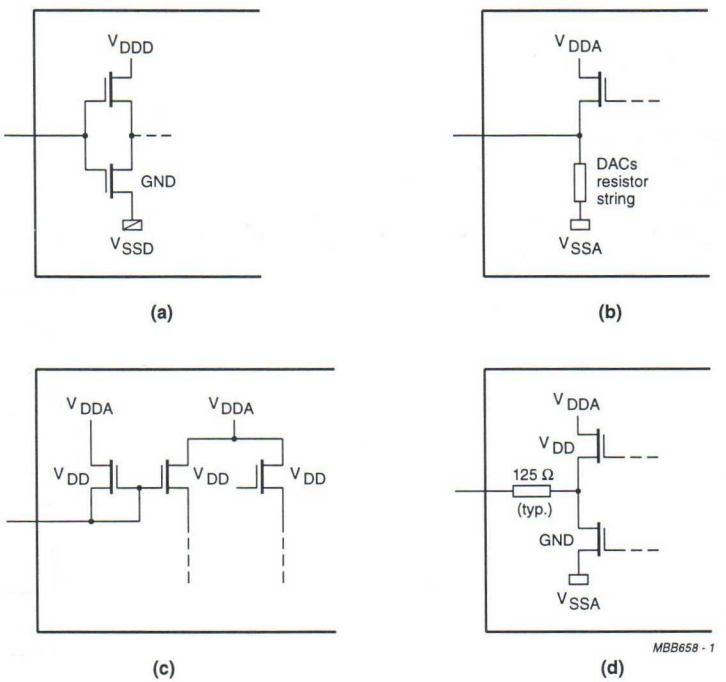


Fig.4 Switching timing.

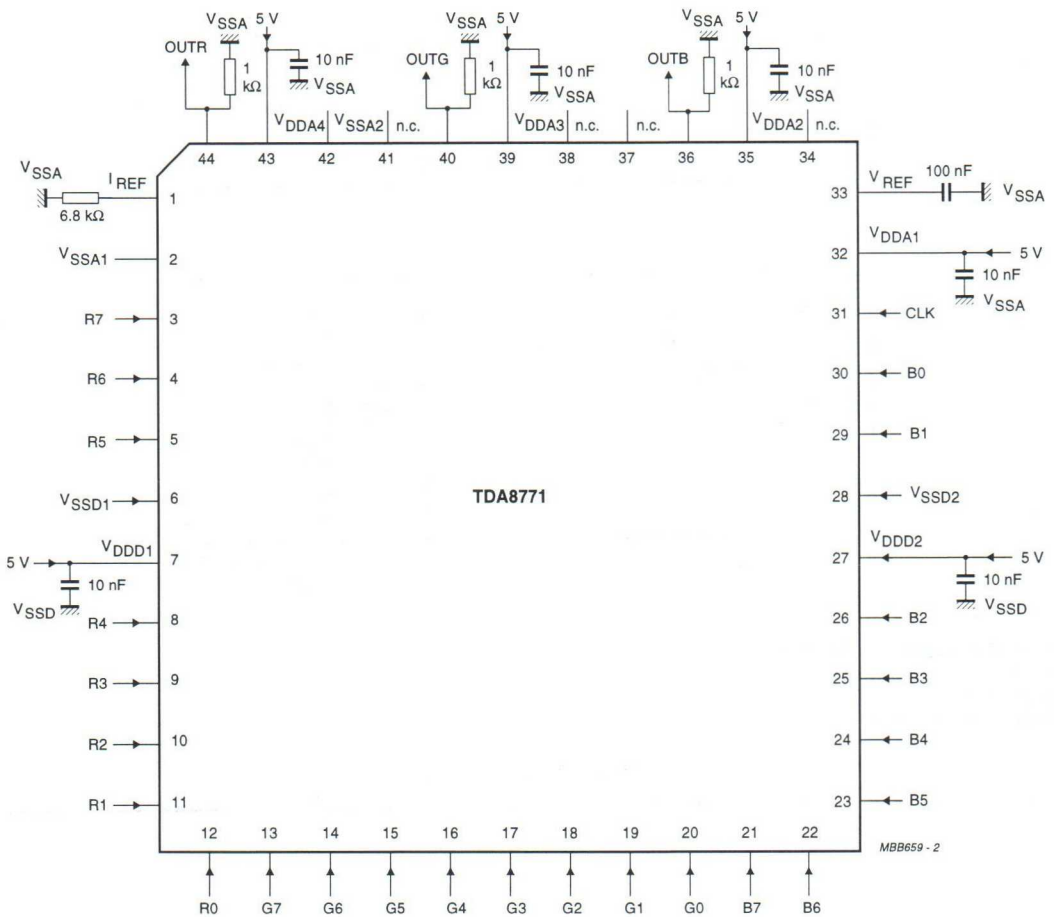
INTERNAL CIRCUITRY



(a) Digital inputs; pins 3 to 5, 8 to 26 and 29 to 31.
(b) V_{REF}; pin 33.
(c) I_{REF}; pin 1.
(d) OUTR, G, B; pins 44, 40 and 36.

Fig.5 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on application.
See Figs 7 and 9 for example of anti-aliasing filter.

Fig.6 Application diagram.

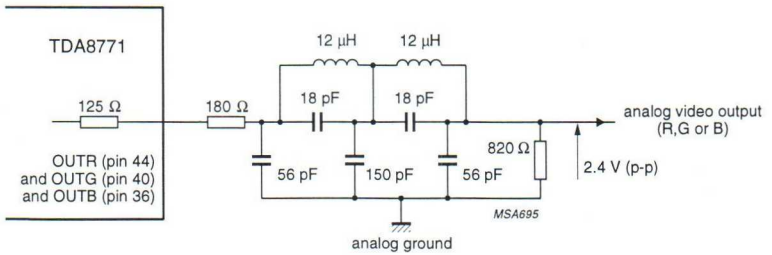


Fig.7 Example of anti-aliasing filter for 2.4 V output swing.

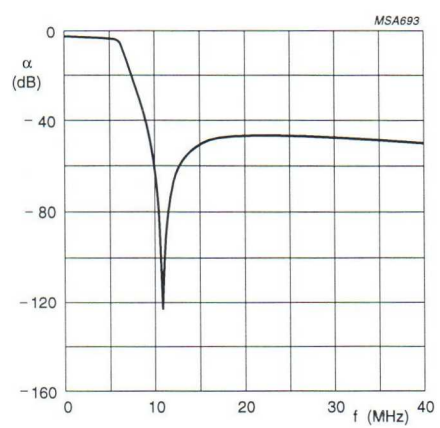


Fig.8 Frequency response for filter shown in Fig.7.

Characteristics of Fig.8

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.7$ dB
- f at −3 dB = 6.2 MHz
- f_{NOTCH} = 10.8 MHz.

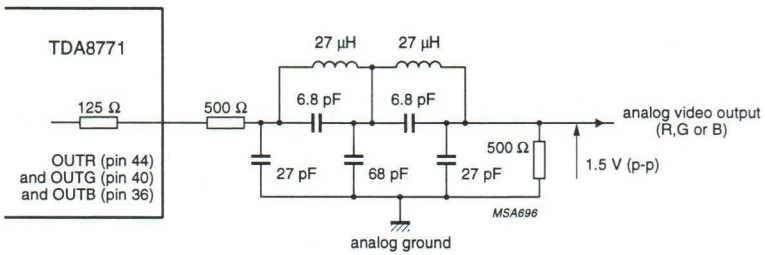


Fig.9 Example of anti-aliasing filter for 1.5 V output swing.

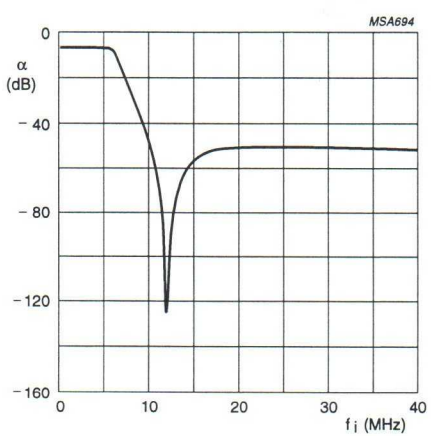


Fig.10 Frequency response for filter shown in Fig.9.

Characteristics of Fig.10

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.25$ dB
- f at −3 dB = 5.6 MHz
- f_{NOTCH} = 11.7 MHz.

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

FEATURES

- 8-bit resolution
- Sampling rate up to
  35 MHz for TDA8772H/3, TDA8772AH/3
  85 MHz for TDA8772H/8, TDA8772AH/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75 Ω output load
- TDA8772A has $\overline{\text{BLANK}}$ control input on the GREEN channel only while TDA8772 has it on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772, TDA8772A are triple 8-bit video digital-to-analog converters (DACs). They convert the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3, TDA8772AH/3) and 85 MHz (TDA8772H/8, TDA8772AH/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772AH/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772H/8	44	QFP44	plastic	SOT307B	85 MHz
TDA8772AH/8	44	QFP44	plastic	SOT307B	85 MHz

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 75 Ω; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
INL	integral non-linearity2	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
		f_{clk} = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	±0.5	±0.75	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
P_{tot}	total power dissipation	note 1				
	TDA8772H/3, TDA8772AH/3	R_L = 75 Ω; f_{clk} = 35 MHz	180	360	640	mW
	TDA8772H/8, TDA8772AH/8	R_L = 75 Ω; f_{clk} = 85 MHz	180	405	700	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

BLOCK DIAGRAMS

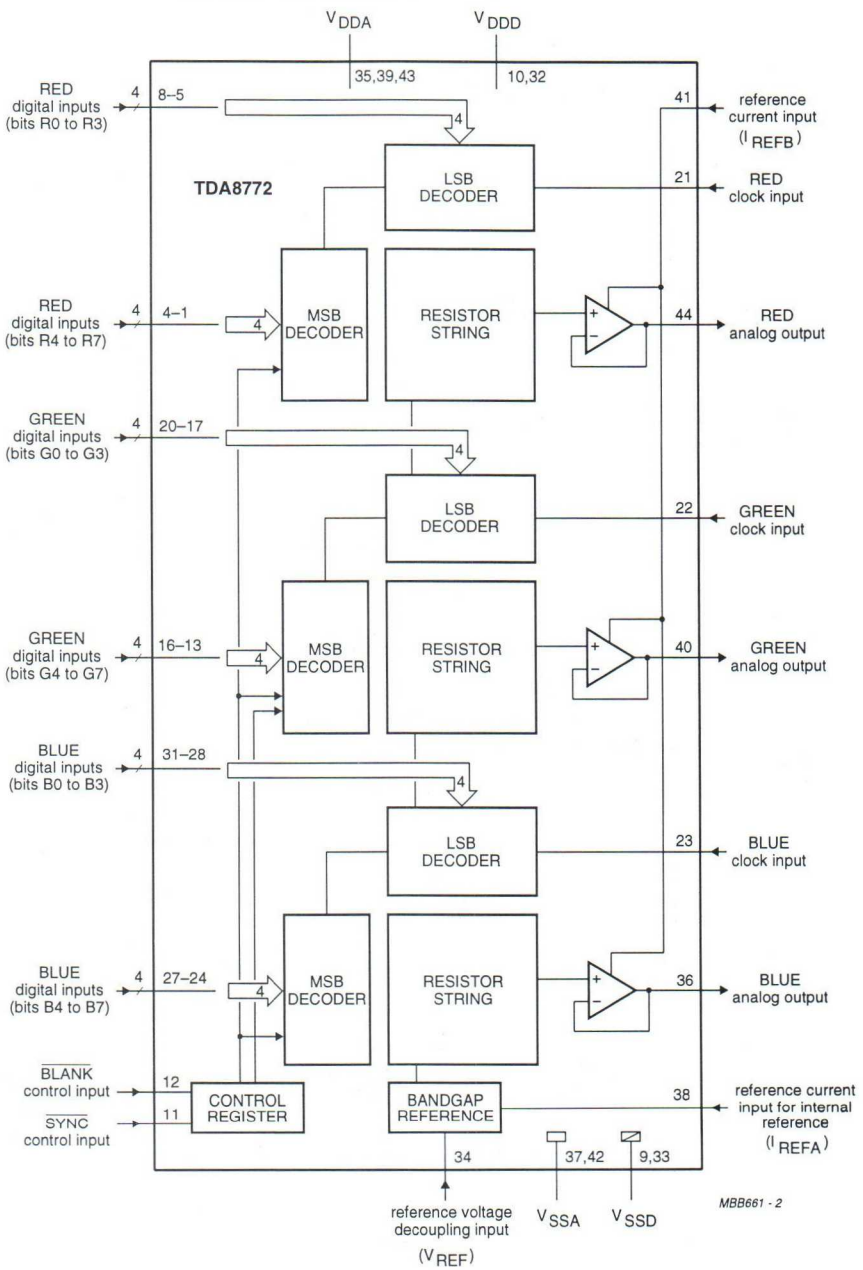


Fig.1 Block diagram for TDA8772.

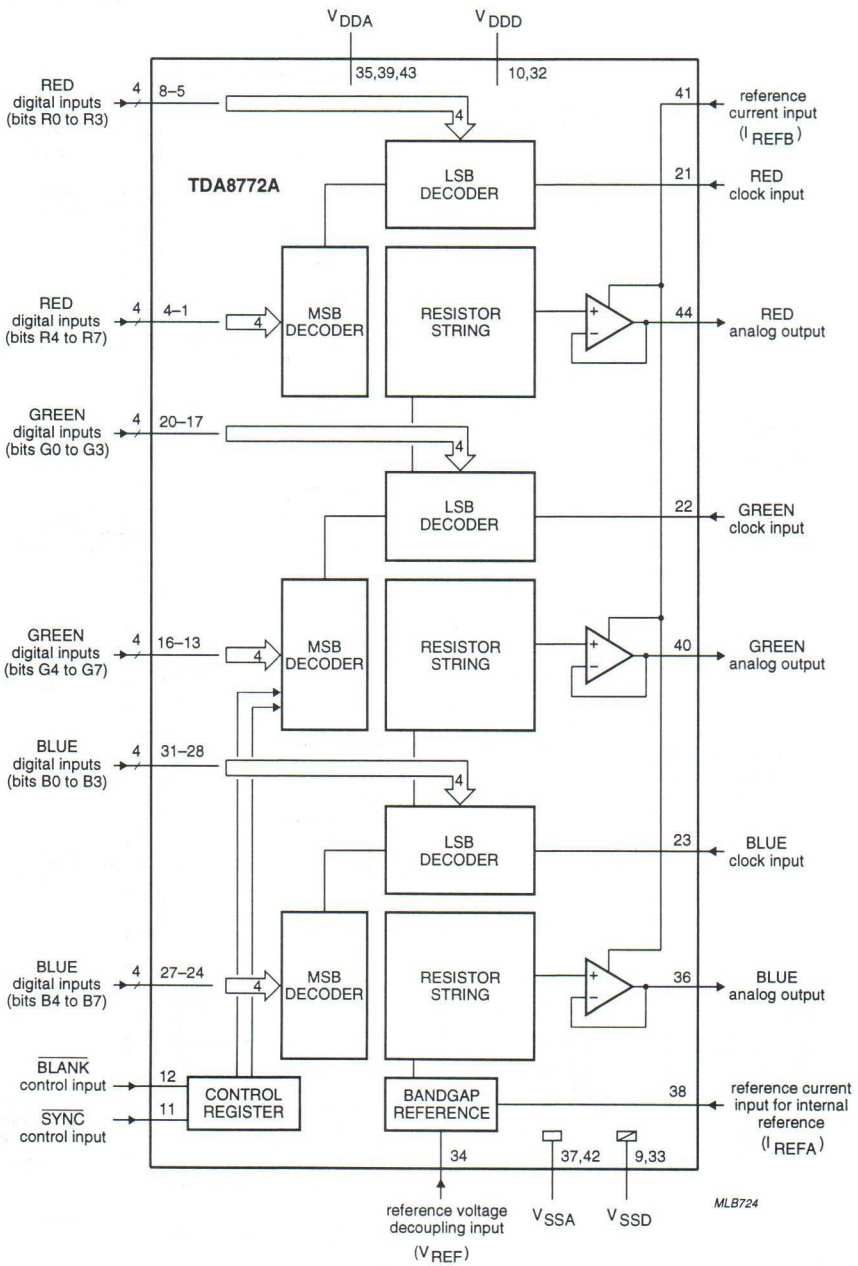


Fig.2 Block diagram for TDA8772A.

PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

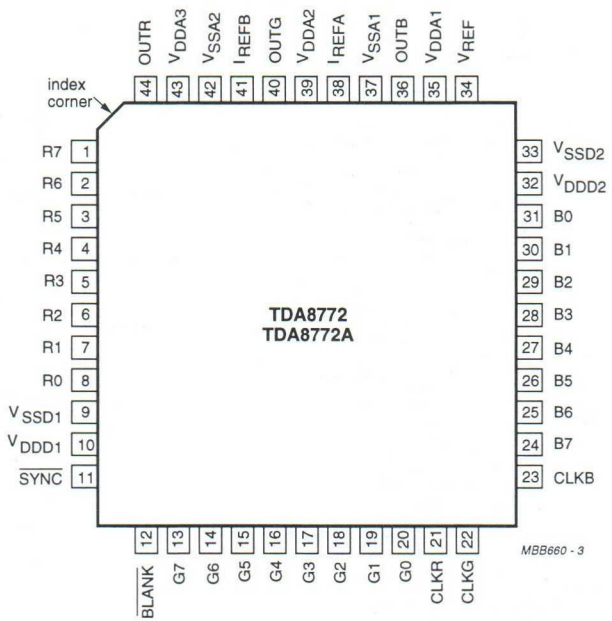


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.5	+6.5	V
V_{DDD}	digital supply voltage	–0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	–1.0	+1.0	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8772H/3, TDA8772AH/3 operating at 35 MHz and TDA8772H/8, TDA8772AH/8 operating at 85 MHz unless otherwise specified.

$V_{DDA} = V_{DDD} = 4.5$ V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 75\ \Omega$; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
Inputs						
CLOCK INPUTS (PINS 21, 22 AND 23)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
$\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ INPUTS (PINS 12 AND 11; ACTIVE LOW)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
R, G, B DIGITAL INPUTS (PINS 1 TO 8, 13 TO 20 AND 24 TO 31)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
I_{REFA} INTERNAL REFERENCE SUPPLY CURRENT (PIN 38)						
I_I	input current		–	0.17	0.25	mA
I_{REFB} OUTPUT BUFFER SUPPLY CURRENT (PIN 41)						
I_I	input current		–	0.5	0.7	mA
Timing ($C_L = 25$ pF; $R_L = 75\ \Omega$); see Fig.4						
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
t_{CPH}	clock pulse width HIGH		5	–	–	ns
t_{CPL}	clock pulse width LOW		5	–	–	ns
t_r	clock rise time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
t_f	clock fall time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage reference (pin 34, referenced to V_{SSA})						
V_{REF}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) FOR 75 Ω LOAD; see Tables 1 and 2						
FSR	full-scale output voltage range		0.9	1.0	1.1	V
V_{os}	offset of analog voltage output		0.75	0.83	0.95	V
V_{OUTmax}	maximum output voltage	data inputs = logic 1; note 2	1.65	1.83	2.05	V
V_{OUTmin}	minimum output voltage	data inputs = logic 0; note 2	0.75	0.83	0.95	V
THD	total harmonic distortion	f_i = 4.43 MHz; f_{clk} = 35 MHz	–	–45	–	dB
		f_i = 4.43 MHz; f_{clk} = 85 MHz	–	–43	–	dB
Z_L	output load impedance		60	75	90	Ω
Transfer function						
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
		f_{clk} = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	±0.5	±0.75	LSB
α_{CT}	crosstalk DAC to DAC		–45	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (for 75 Ω output load); see Fig.5						
t_d	input to 50% output delay time	full-scale change	–	10	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	6	–	ns
t_{s2}	settling time	to ±1 LSB	–	30	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB.ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V_{OUT} is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 75 Ω
0000 0000	0	0.830
0000 0001	1	0.834
....	.	.
1000 0000	128	1.330
....	.	.
1111 1110	254	1.826
1111 1111	255	1.830

Table 2 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (PIN 11)	$\overline{\text{BLANK}}$ (PIN 12)	DAC OUTPUT VOLTAGES (V)		
			OUTG (PIN 40)	OUTR/B (PINS 44, 46) TDA8772	OUTR/B (PINS 44, 46) TDA8772A
....	x	1	see Table 1	see Table 1	see Table 1
....	1	0	0.830	0.830	
....	0	0	0.440		

TIMING

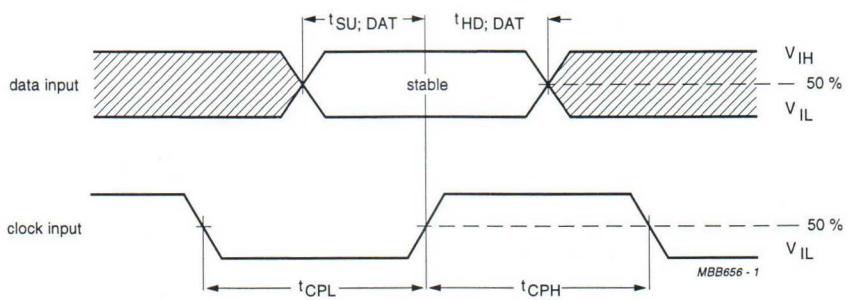


Fig.4 Input timing.

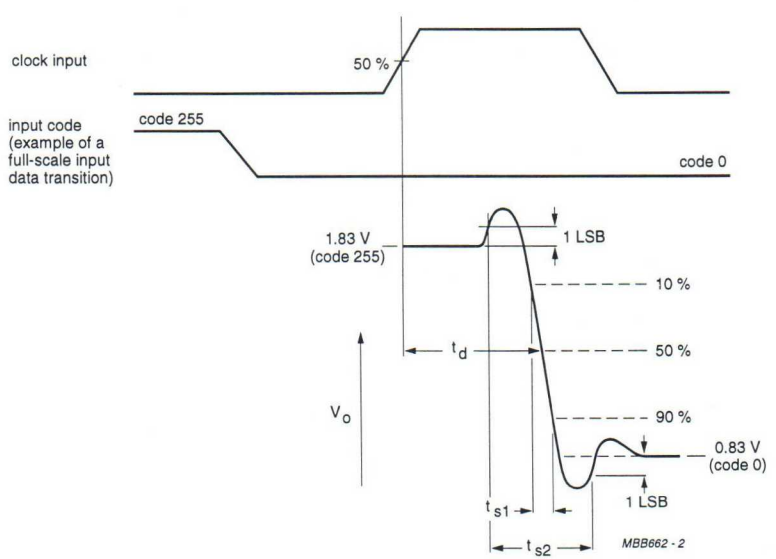
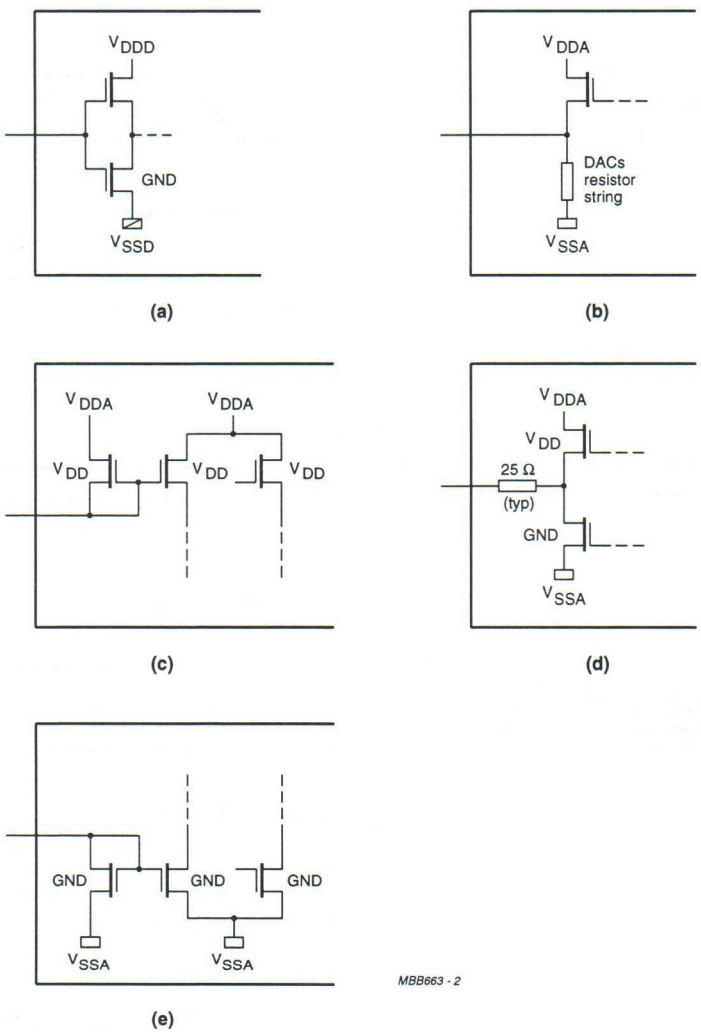


Fig.5 Switching timing.

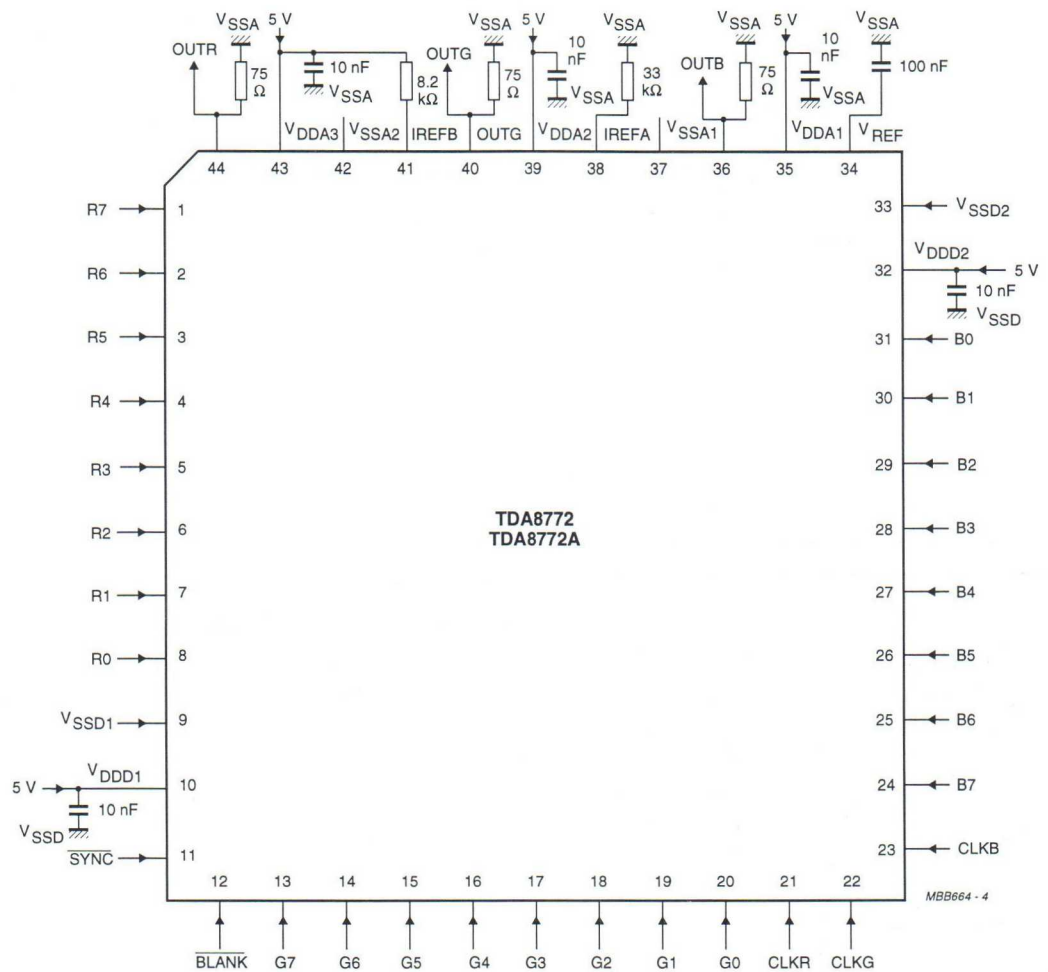
INTERNAL CIRCUITRY



(a) Digital inputs; pins 1 to 8 and 11 to 31.
(b) VREF; pin 34.
(c) IREFA; pin 38.
(d) OUTR, G, B; pins 44, 40 and 36.
(e) IREFB; pin 41.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on the application.
See Fig.8 for example of anti-aliasing filter.

Fig.7 Application diagram.

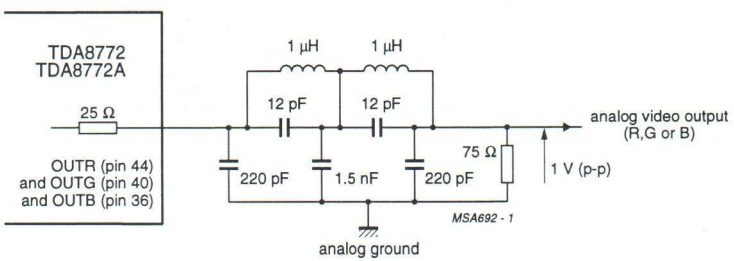


Fig.8 Example of anti-aliasing filter for 1 V output swing.

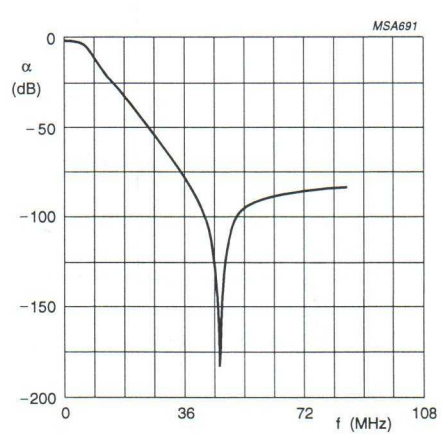


Fig.9 Frequency response for filter shown in Fig.8.

Characteristics of Fig.9

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.6$ dB
- f at −3 dB = 6.5 MHz
- f_{NOTCH} = 46 MHz.

10-bit, 500 MSPS digital-to-analog converter TDA8776

FEATURES

- 10-bit resolution
- Conversion rate up to 500 MHz
- 100K ECL input levels
- Internal reference voltage generator
- No deglitching circuit required
- Internal input register
- Power dissipation only 780 mW (typical)
- Internal 50 Ω output load (connected to the analog ground)
- Very few external components required.

APPLICATIONS

High-speed digital-to-analog conversion for:

- High resolution video and graphics
- Direct digital synthesis (DDS)
- Telecommunication
- High-speed modems.

GENERAL DESCRIPTION

The TDA8776 is a 10-bit digital-to-analog converter (DAC) for high resolution video and other high frequency applications. It converts the digital input signal into an analog output voltage at a maximum conversion rate of 500 MSPS. No external reference voltage is required and all digital inputs are 100K-ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−5.46	−5.20	−4.94	V
V_{EED}	digital supply voltage		−5.46	−5.20	−4.94	V
V_{EEI}	input stages digital supply voltage	note 1	−5.46	−5.20	−4.94	V
I_{EEA}	analog supply current	note 1	–	60	tbf	mA
I_{EED}	digital supply current	note 1	–	60	tbf	mA
I_{EEI}	input stages digital supply current	note 1	–	30	tbf	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2; Z_L = 50 Ω	–	2.0	–	V
INL	DC integral non-linearity		–	±0.25	tbf	LSB
DNL	DC differential non-linearity		–	±0.35	tbf	LSB
$f_{clk(max)}$	maximum clock frequency		500	–	–	MHz
t_{S1}	settling time (differential)	10% to 90% full scale; Fig.9	–	0.5	tbf	ns
P_{tot}	total power dissipation		–	780	tbf	mW

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{CLK}$ is LOW.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8776K	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2

BLOCK DIAGRAM

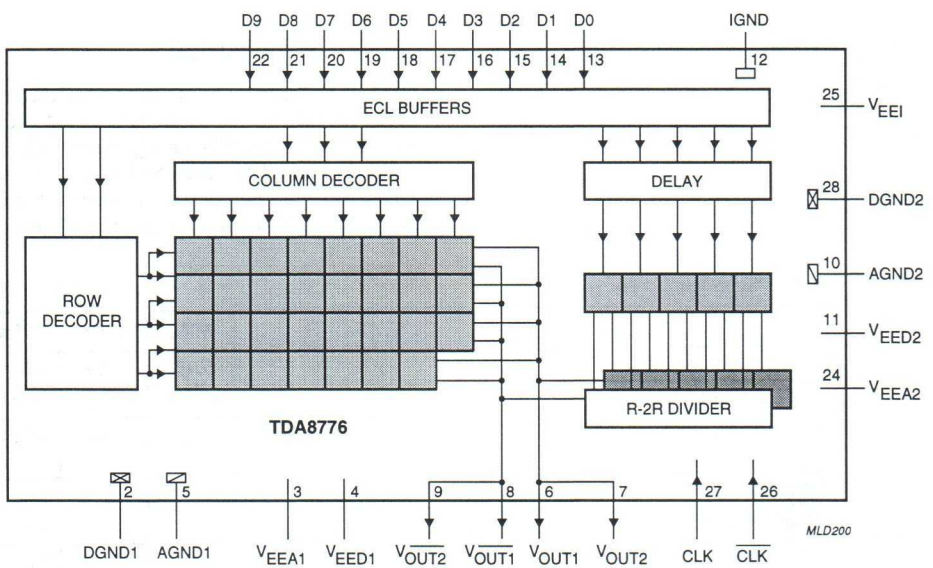


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DGND1	2	digital ground 1
V_{EEA1}	3	analog supply voltage 1 (–5.2 V)
V_{EED1}	4	digital supply voltage 1 (–5.2 V)
AGND1	5	analog ground 1
V_{OUT1}	6	analog voltage output 1
V_{OUT2}	7	analog voltage output 2
$V_{\overline{OUT1}}$	8	complementary analog voltage output 1
$V_{\overline{OUT2}}$	9	complementary analog voltage output 2
AGND2	10	analog ground 2
V_{EED2}	11	digital supply voltage 2 (–5.2 V)
IGND	12	input ground for ECL input buffers
D0	13	data input; bit 0 (LSB)
D1	14	data output; bit 1

SYMBOL	PIN	DESCRIPTION
D2	15	data input; bit 2
D3	16	data input; bit 3
D4	17	data input; bit 4
D5	18	data input; bit 5
D6	19	data input; bit 6
D7	20	data input; bit 7
D8	21	data input; bit 8
D9	22	data input; bit 9 (MSB)
n.c.	23	not connected
V_{EEA2}	24	analog supply voltage 2 (–5.2 V)
V_{EEI}	25	input supply voltage for ECL input buffers (–5.2 V)
$\overline{CLK}$	26	complementary clock input
CLK	27	clock input
DGND2	28	digital ground 2

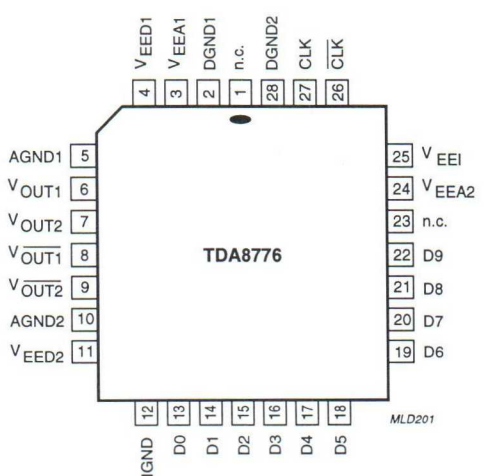


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7.0	±0.3	V
V_{EED}	digital supply voltage		−7.0	±0.3	V
V_{EEI}	input stages digital supply voltage		−7.0	±0.3	V
$V_{EEA} - V_{EED}$	supply voltage differential		−0.5	+0.5	V
AGND − DGND	ground voltage differential		−0.1	+0.1	V
V_I	input voltage		V_{EEI}	±0.3	V
$I_{OUT}/I_{\overline{OUT}}$	total output current	$Z_L = 50\ \Omega$	−5	+50	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W

CHARACTERISTICS

$V_{EEA} = V_3$ and V_{24} to V_5 and $V_{10} = -5.46$ to -4.94 V; $V_{EED} = V_4$ and V_{11} to V_2 and $V_{28} = -5.46$ to -4.94 V; $V_{EEI} = V_{25}$ to $V_{12} = -5.46$ to -4.94 V; $V_{EED} - V_{EEI} = -0.25$ to $+0.25$ V; reference voltage decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ to $+70$ °C; AGND, DGND and IGND shorted together; $V_{OUT} - V_{\overline{OUT}} = 2$ V (p-p); $Z_L = 50\ \Omega$; unless otherwise specified (typical values measured at $V_{EEA} = V_{EED} = -5.2$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−5.46	−5.20	−4.94	V
V_{EED}	digital supply voltage		−5.46	−5.20	−4.94	V
V_{EEI}	input stages digital supply voltage	note 1	−5.46	−5.20	−4.94	V
I_{EEA}	analog supply current	note 1	–	60	tbf	mA
I_{EED}	digital supply current	note 1	–	60	tbf	mA
I_{EEI}	input stages digital supply current	note 1	–	30	tbf	mA
AGND − DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D9 TO D0) AND CLOCK INPUTS (CLK AND $\overline{CLK}$)						
V_{IL}	LOW level input voltage		tbf	−1.8	tbf	V
V_{IH}	HIGH level input voltage		tbf	−0.9	tbf	V
I_{IL}	LOW level input current	$V_I = -1.8$ V	–	−0.01	–	mA
I_{IH}	HIGH level input current	$V_I = -0.9$ V	–	−0.01	–	μA
$f_{clk(max)}$	maximum clock frequency		500	–	–	MHz
Outputs (referenced to AGND); note 2						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	$Z_L = 50\ \Omega$	–	2.0	–	V
Z_O	output impedance		–	50	–	Ω
Transfer function (f_{clk} = 500 MHz)						
INL	DC integral non-linearity		–	±0.25	tbf	LSB
DNL	DC differential non-linearity		–	±0.35	tbf	LSB
Spurious free dynamic range (f_{clk} = 500 MHz); see Fig.3						
SFDR	spurious free dynamic range					
	f_{OUT} = 10.132 MHz	see Fig.4	–	71	–	dB
	f_{OUT} = 50.147 MHz	see Fig.5	–	66	–	dB
	f_{OUT} = 80.444 MHz	see Fig.6	–	63	–	dB
	f_{OUT} = 100.220 MHz	see Fig.7	–	61	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{clk} = 500 MHz); notes 3 and 4; see Figs 8 and 9						
$t_{SU;DAT}$	data set-up time		tbf	–	–	ns
$t_{HD;DAT}$	data hold time		tbf	–	–	ns
t_{PD}	propagation delay time		–	–	tbf	ns
t_{S1}	settling time (differential)	10% to 90% full scale	–	0.5	tbf	ns
t_{S2}	settling time (differential)	change to ±1 LSB	–	2.0	tbf	ns
t_d	input to 50% output delay time		–	tbf	tbf	ns
Output transients; glitches (f_{clk} = 500 MHz); note 5; see Fig.10						
E_g	differential glitch energy from code	transition 511 to 512	–	1	tbf	pV.s

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{CLK}$ is LOW.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω.
3. The worst case characteristics are obtained at the transition from input code 0 to 1023 and if an external load impedance greater than 50 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and AGND in parallel with the external 50 Ω load. The specified values have been measured with an active probe (15 pF) between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock.
4. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
5. The definition of glitch energy and the measurement set-up are shown in Fig.10. The glitch energy is measured at the input transition between code 511 to 512.

Table 1 Input coding and DAC output voltages (typical values; referenced to AGND regardless of the offset voltage)

CODE	BINARY INPUT DATA										DAC OUTPUT VOLTAGES (V) Z_L = 50 Ω	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	V_{OUT}	$V_{\overline{OUT}}$
0	0	0	0	0	0	0	0	0	0	0	0	−1.0
1	0	0	0	0	0	0	0	0	0	1	−0.0010	−0.9990
.	.	.	.	.	.	.	.	.	.	.	.	.
512	1	0	0	0	0	0	0	0	0	0	−0.5	−0.5
.	.	.	.	.	.	.	.	.	.	.	.	.
1022	1	1	1	1	1	1	1	1	1	0	−0.9990	−0.0010
1023	1	1	1	1	1	1	1	1	1	1	−1.0	0

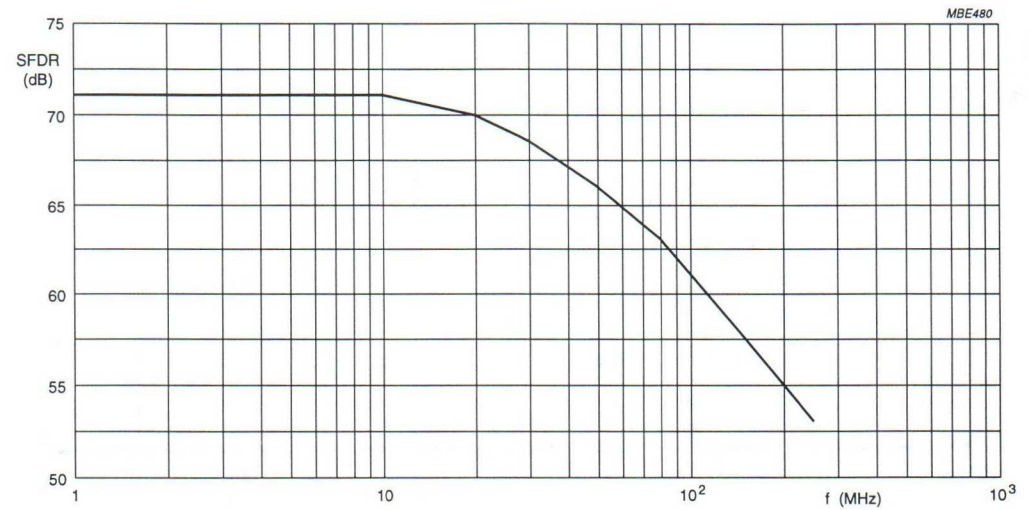


Fig.3 Typical spurious free dynamic range (SFDR) as a function of output frequency.

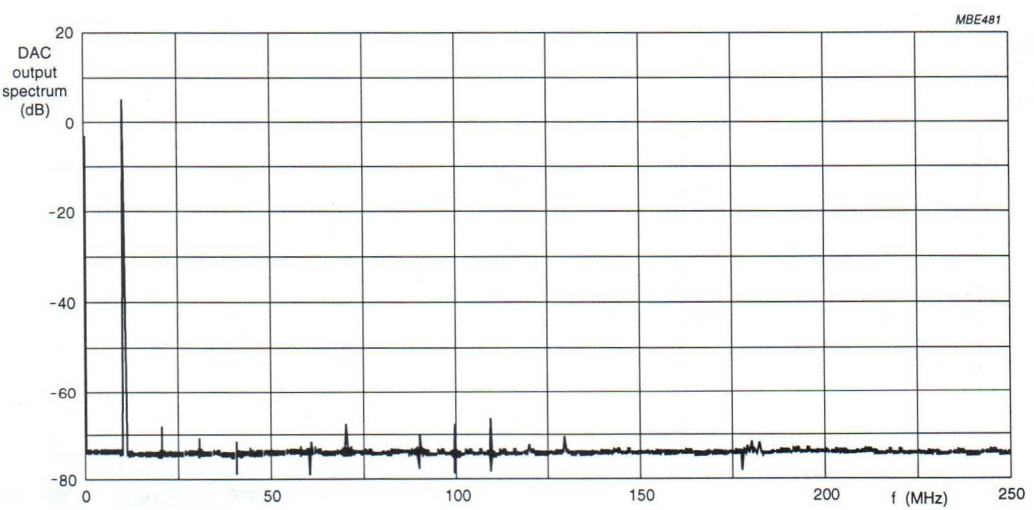


Fig.4 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 10.132 MHz.

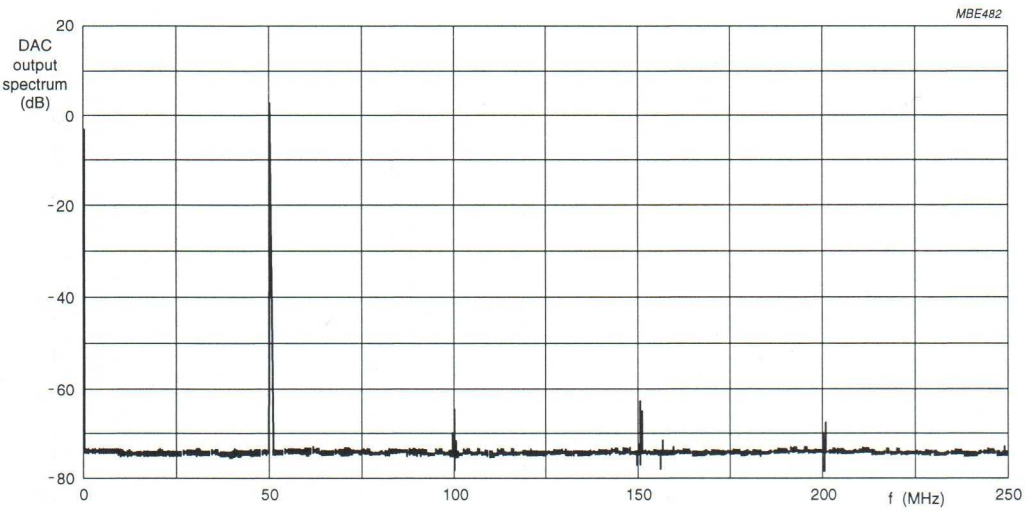


Fig.5 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 51.147 MHz.

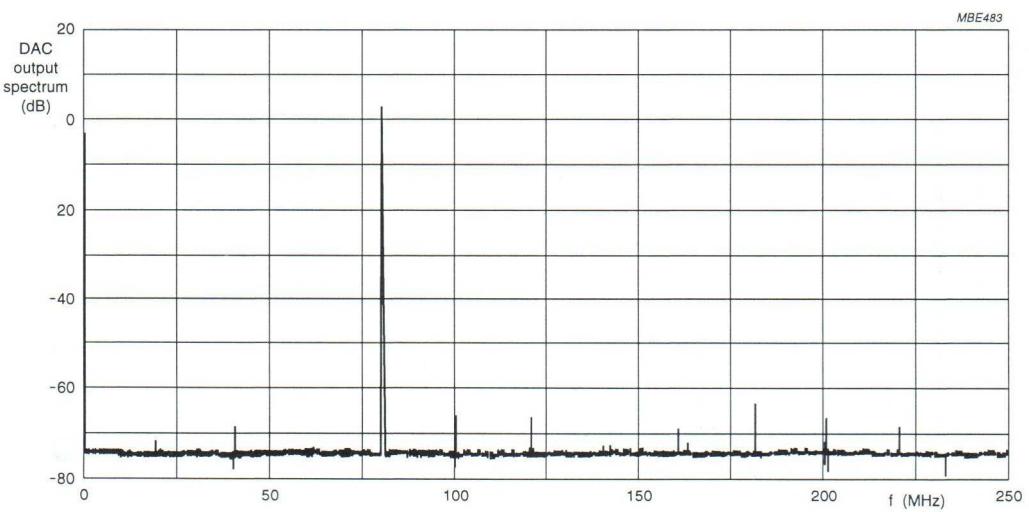


Fig.6 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 80.444 MHz.

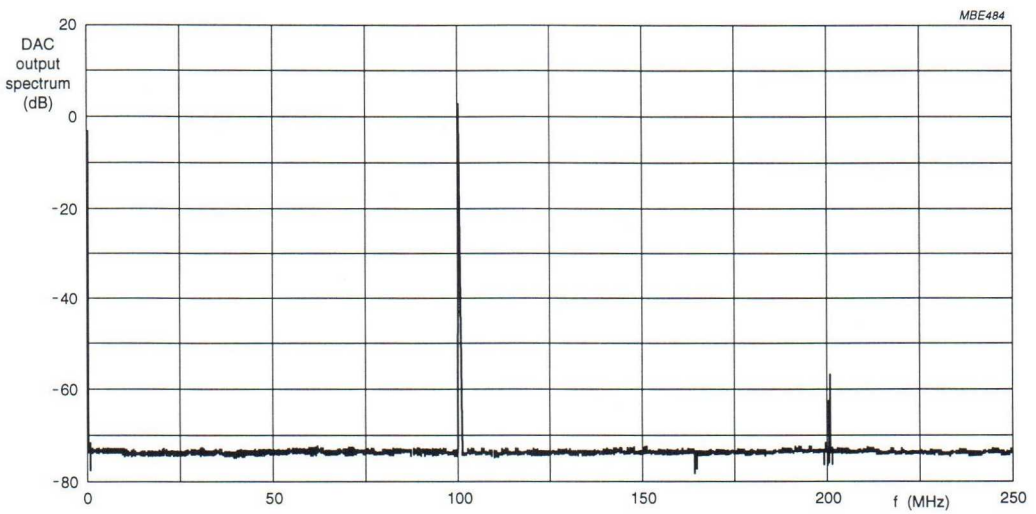
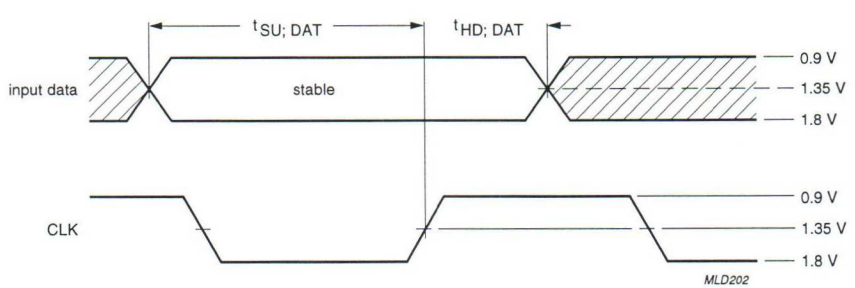


Fig.7 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 100.220 MHz.



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within tbf ns after the rising edge of the clock ($t_{SU;DAT}$ is negative; tbf ns). Data must be held at least tbf ns after the rising edge ($t_{HD;DAT}$ = tbf ns).

Fig.8 Data set-up and hold times.

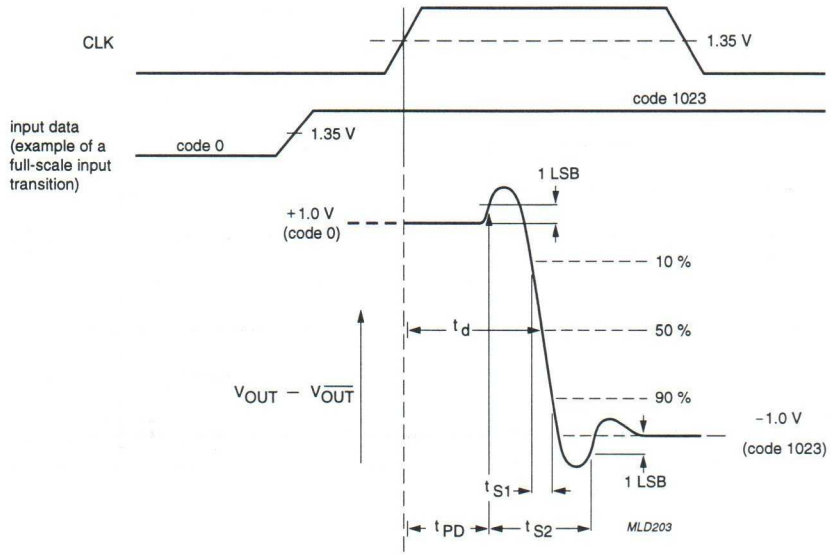
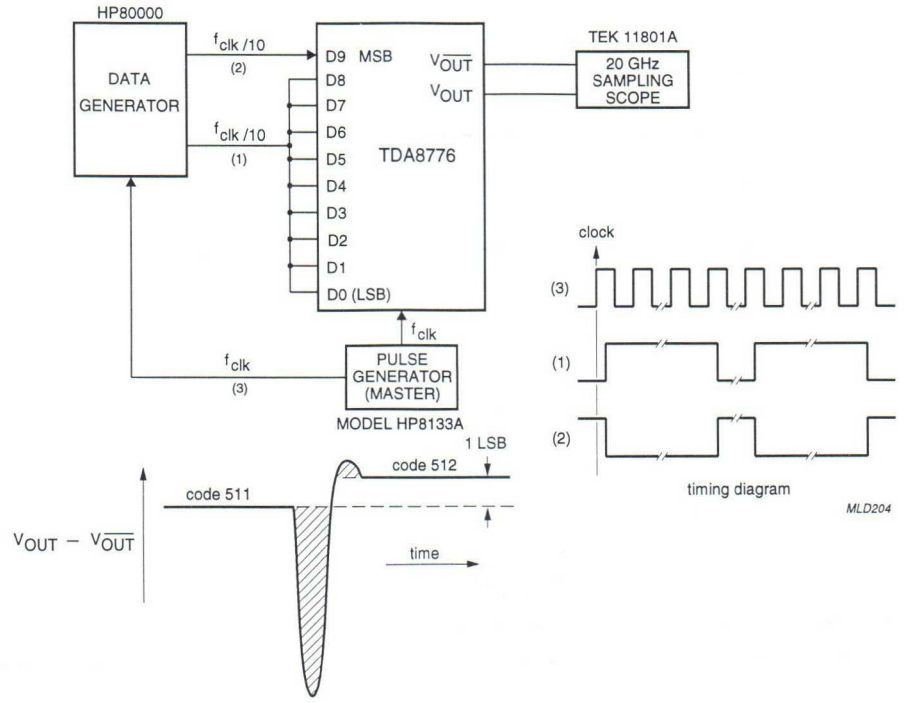


Fig.9 Differential switching characteristics.



The value of the glitch energy is the sum of the shaded areas measured in pV.s.

Fig.10 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

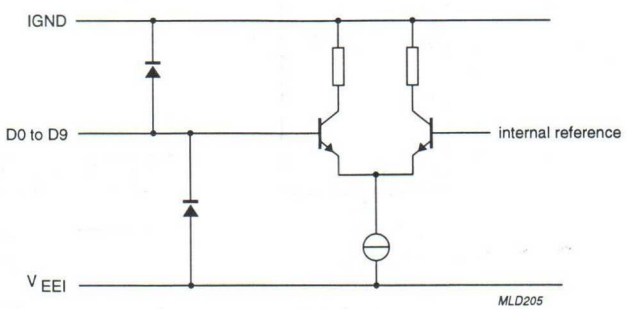


Fig.11 D9 to D0.

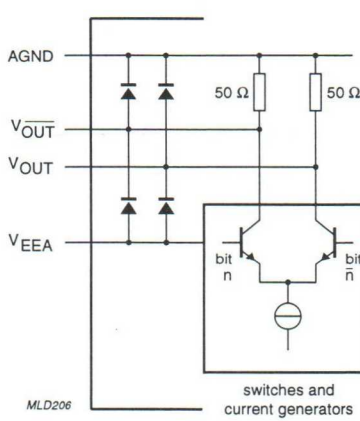


Fig.12 Analog outputs.

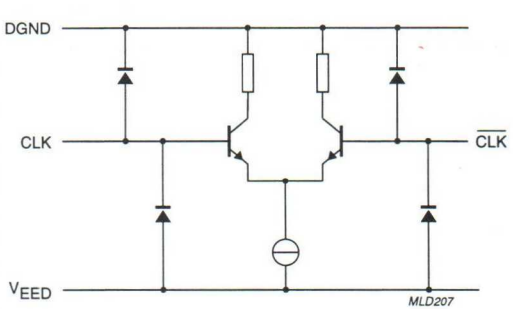
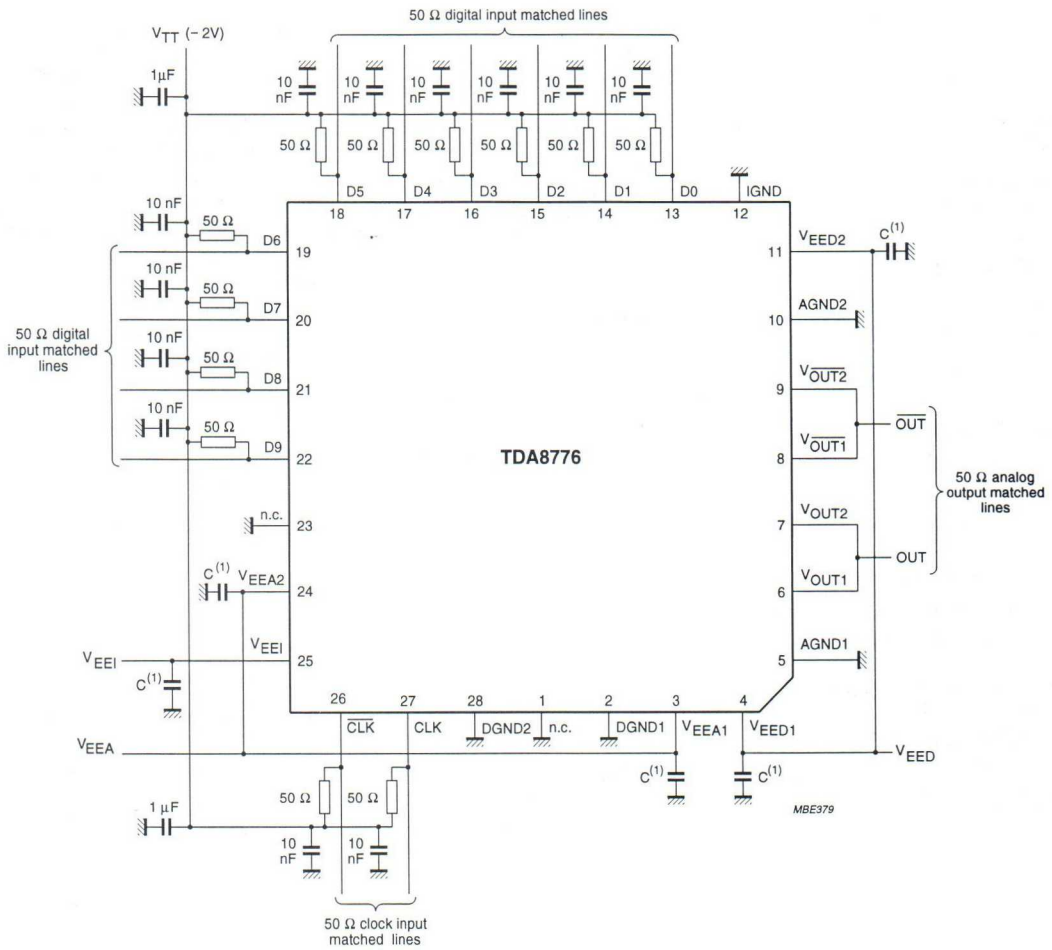


Fig.13 CLK and $\overline{CLK}$.

APPLICATION INFORMATION



(1) C = 1 μF in parallel with 10 nF in parallel with 1 nF; all three mounted close to the supply pin of the DAC with 1 nF the nearest.

Fig.14 Application diagram.

PAL/NTSC/SECAM decoder/sync processor

TDA9141

FEATURES

- Multistandard PAL, NTSC and SECAM
- I²C-bus controlled
- I²C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- CVBS or YC input with automatic detection
- CVBS output
- Vertical divider system
- Two-level sandcastle signal
- V_A synchronization pulse (3-state)
- H_A synchronization pulse or clamping pulse CLP input/output
- Line-locked clock output or stand-alone I²C-bus output port
- Stand-alone I²C-bus input/output port
- Colour matrix and fast YUV switch
- Comb filter enable input/output with subcarrier frequency.

GENERAL DESCRIPTION

The TDA9141 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor. The TDA9141 has been designed for use with baseband chrominance delay lines, and has a combined subcarrier frequency/comb filter enable signal for communication with a PAL comb filter.

The IC can process CVBS signals and Y/C input signals. The input signal is available on an output pin, in the event of a Y/C signal, it is added into a CVBS signal.

The sync processor provides a two-level sandcastle, a horizontal pulse (CLP or H_A pulse, bus selectable) and a vertical (V_A) pulse. When the H_A pulse is selected a line-locked clock (LLC) signal is available at the output port pin.

A fast switch can select either the internal Y signal with the UV input signals, or YUV signals made of the RGB input signals. The RGB input signals can be clamped with either the internal or an external clamping signal (search tuning mode).

Two pins with an input/output port and an output port of the I²C-bus are available.

The I²C-bus address of the TDA9141 is hardware programmable.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9141	32	SDIL	plastic	SOT232

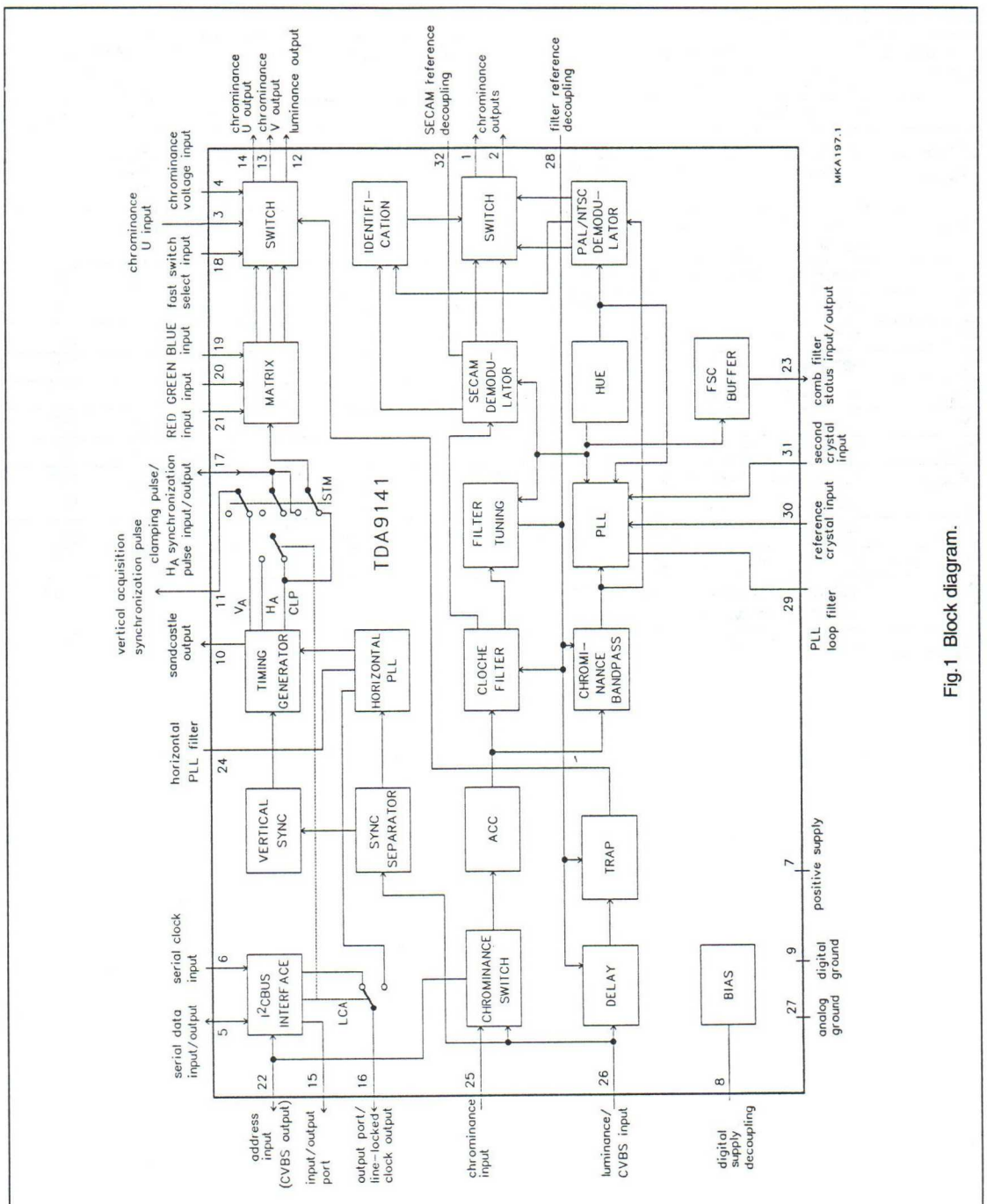


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	45	–	mA
$V_{26(p-p)}$	CVBS input voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
$V_{26(p-p)}$	luminance input voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
$V_{22(p-p)}$	chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
V_{12}	luminance black-white output voltage		–	1.0	–	V
$V_{14(p-p)}$	U output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	V
$V_{13(p-p)}$	V output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	V
V_{10}	sandcastle blanking voltage level		–	2.5	–	V
V_{10}	sandcastle clamping voltage level		–	4.5	–	V
V_{11}	V_A output voltage		–	5.0	–	V
V_{17}	H_A output voltage		–	5.0	–	V
$V_{16(p-p)}$	LLC output voltage amplitude (peak-to-peak value)		–	500	–	mV
$V_{21,20\ 19(p-p)}$	RGB input voltage (peak-to-peak value)	0 to 100% saturation	–	0.7	–	V
$V_{clamp\ I/O}$	clamping pulse input/output voltage		–	5.0	–	V
V_{sub}	subcarrier output voltage amplitude (peak-to-peak value)		–	200	–	mV
$V_{15,16}$	O port output voltage		–	5.0	–	V

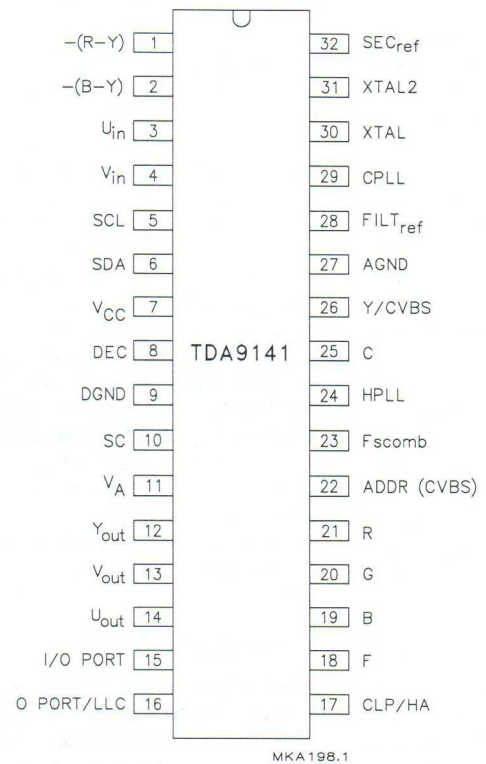


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−(R−Y)	1	chrominance output
−(B−Y)	2	chrominance output
U_{in}	3	chrominance U input
V_{in}	4	chrominance voltage input
SCL	5	serial clock input
SDA	6	serial data input/output
V_{CC}	7	positive supply input
DEC	8	digital supply decoupling
DGND	9	digital ground
SC	10	sandcastle output
V_A	11	vertical acquisition synchronization pulse
Y_{out}	12	luminance output
V_{out}	13	chrominance V output
U_{out}	14	chrominance U output
I/O PORT	15	input/output port
O PORT/LLC	16	output port/line-locked clock output
CLP/HA	17	clamping pulse/H_A synchronization pulse input/output
F	18	fast switch select input
B	19	BLUE input
G	20	GREEN input
R	21	RED input
ADDR (CVBS)	22	I²C-bus address input (CVBS output)
Fscomb	23	comb filter status input/output
HPLL	24	horizontal PLL filter
C	25	chrominance input
Y/CVBS	26	luminance/CVBS input
AGND	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
CPLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

FUNCTIONAL DESCRIPTION

General

The TDA9141 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM colour decoder/sync processor which has been designed for use with baseband chrominance delay lines. In the standard operating mode the I²C-bus address is 8A. If the address input is connected to the positive rail the address will change to 8E.

Input switch

WARNING: THE VOLTAGE ON THE CHROMINANCE PIN MUST NEVER EXCEED 5.5 V. IF IT DOES THE IC ENTERS A TEST MODE.

The TDA9141 has a two pin input for CVBS or YC signals which can be selected via the I²C-bus. The input selector also has a position in which it automatically detects whether a CVBS or YC signal is on the input. In this input selector position, standard identification first takes place on an added Y/CVBS and C input signal. After that, both chrominance signal input amplitudes are checked once and the input with the strongest chrominance burst signal is selected. The input switch status is read out by the I²C-bus via output bit YC.

CVBS output

In the standard operating mode with the I²C-bus address 8A, a CVBS output signal is available on the address pin, which represents either the CVBS input signal or the Y/C input signal, added into a CVBS signal

RGB colour matrix

WARNING: THE VOLTAGE ON THE UIN PIN MUST NEVER EXCEED 5.5 V. IF IT DOES THE IC ENTERS A TEST MODE.

The TDA9141 has a colour matrix to convert RGB input signals into YUV signals. A fast switch, controlled by the signal on pin F and enabled by the I²C-bus via EFS (enable fast switch), can select between these YUV signals and the YUV signals of the decoder. The Y signal is internally connected to the switch. The –(R–Y) and –(B–Y) output signals of the decoder have to first be delayed in external baseband chrominance delay lines. The outputs of the delay lines must be connected to the UV input pins. If the RGB signals are not synchronous with the selected decoder input signal, clamping of the RGB input signals is possible by I²C-bus selection of STM (search tuning mode), EFS and by feeding an external clamping signal to the CLP pin.
Also in search tuning mode the VA output will be in a high impedance OFF-state.

Standard identification

The standards which the TDA9141 can decode are dependent on the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded. Which 3.6 MHz standards can be decoded is dependent on the exact frequencies of the 3.6 MHz crystals. In an application where not all standards are required only one crystal is sufficient (in this instance the crystal must be connected to the reference crystal input (pin 30)). If a 4.4 MHz crystal is used it must always be connected to pin 30. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator.
To enable the calibrating circuits to be adjusted exactly two bits from I²C-bus subaddress 00 are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components; the search loop is illustrated in Fig.3.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information concerning which standard and which crystal have been selected and whether the colour killer is ON or OFF is provided by the read out. Using the forced-mode does not affect the search loop, it does, however, prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. is forced mode). To reduce the risk of wrong identification PAL has priority over SECAM (only line identification is used for SECAM).

Integrated filters

All filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the luminance delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.28 MHz or 3.58 MHz irrespective of the frequency of the active crystal. The switching is controlled by the identification circuit.
In YC mode the chrominance notch filter is bypassed, to preserve full

signal bandwidth.
For a CVBS signal the chrominance notch filter can be bypassed by I²C-bus selection of TB (trap bypass).
The luminance delay line delivers the Y signal to the output 60 ns after the –(R–Y) and –(B–Y) signals have arrived at their outputs. This compensates for the delay of the external chrominance delay lines.

Colour decoder

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected it will always connect to the crystal on the reference crystal input (pin 30).

The Hue signal, which is adjustable via the I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search mode or SECAM mode. If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals.

The frequency of the active crystal is fed to the Fscomb output, which can be connected to an external comb filter IC. The DC value on this pin contains the comb enable information. Comb enable is true when bus bit ECMB is HIGH. If ECMB is LOW, the subcarrier frequency is suppressed. The external comb filter can force the DC value of Fscomb LOW, as pin Fscomb also acts as input pin. In this event the subcarrier frequency is still present. If the DC value of Fscomb is HIGH, the input switch is always forced in Y/C mode, indicated by bus bit YC.

Sync processor (φ1 loop)

The main part of the sync circuit is a 432 x f_H (6.75 MHz) oscillator the frequency of which is divided by 432 to lock the Phase 1 loop to the incoming signal. The time constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time constant, depending on the noise content of the input signal and whether the loop is phase-locked or not (medium or slow). The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal.

When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency greater than 6.75 MHz to protect the horizontal output transistor. The oscillator frequency is reset to 6.75 MHz when the crystal indication bits have been loaded into the IC. To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits and when subaddress 01 is received the line oscillator calibration will be initiated (for the start-up procedure after power-on reset detection see the I²C-bus protocol. The calibration is terminated when the oscillator frequency reaches 6.75 MHz. The oscillator is again calibrated when an out-of-lock condition with the input signal is detected by the coincidence detector. Again the calibration will be terminated when the oscillator frequency reaches 6.75 MHz.
The Phase 1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal the phase 1 loop can be opened to provide a stable line frequency and thus a stable picture.

The sync part also delivers a two-level sandcastle signal, which provides a combined horizontal and vertical blanking signal and a clamping pulse for the display section of the TV.

Vertical divider system

The vertical divider system has a fully integrated vertical sync separator. The divider can accommodate both 50 and 60 Hz systems; it can either locate the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in Fig.4. The divider system operates at twice the horizontal line frequency. The line counter receives enable pulses at this line frequency, thereby counting two pulses per line. A state diagram of the controller is illustrated in Fig.5. Because it is symmetrical only the right hand part will be described.

Depending on the previously found field frequency, the controller will be in one of the COUNT states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal) the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR_NORM or NO_NORM depending on the position of the vertical sync pulse in the previous fields. When the controller is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse

of the double line frequency signal and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal.
When the controller is in the NEAR_NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR_NORM window (i.e. $622 < LC < 628$). If no vertical sync pulse is detected, the controller will move back to the COUNT state when the line counter reaches $LC = 628$. The line counter will then be reset.
When the controller is in the NO_NORM state it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a vertical sync pulse is not detected before $LC = 722$ (if the Phase 1 loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the Phase 1 loop is not locked the controller will move back to the COUNT state when $LC = 628$. The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the norm counter which is an up/down counter that counts up if it finds a vertical sync pulse within the selected window. In the NEAR_NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR_NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field. If no vertical sync pulse is found in the selected window this will always result in a down pulse for the norm counter.

Output port and input/output port

Two stand-alone ports are available for external use. These ports are I²C-bus controlled, the output port by bus bit OPB and the input/output port by bus bit OPA. Bus bit OPA is an open-drain output, to enable input port functioning. The pin status is read out by bus via output bit IP.

Sandcastle

Figure 7 illustrates the timing of the acquisition sandcastle (ASC) and the V_A pulse with respect to the input signal. The sandcastle signal is in accordance with the 2-level 5 V sandcastle format. An external vertical guard current can overrule the sink current to enable blanking purposes.

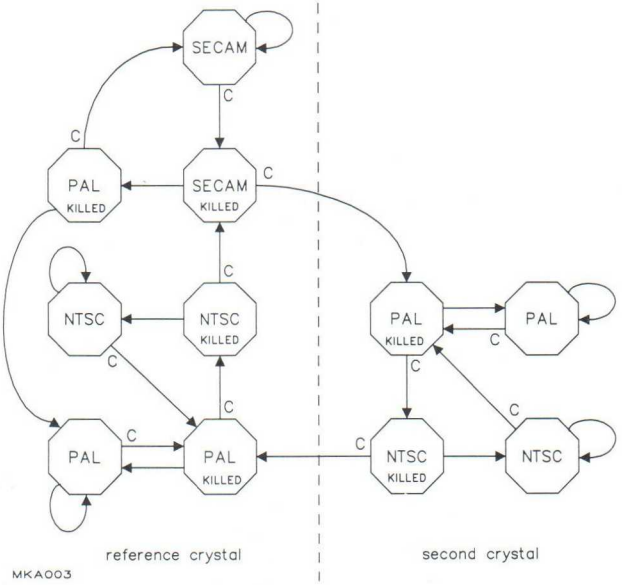


Fig.3 Search loop of the identification circuit.

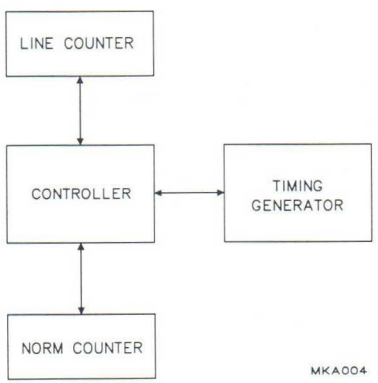


Fig.4 Block diagram of the vertical divider system.

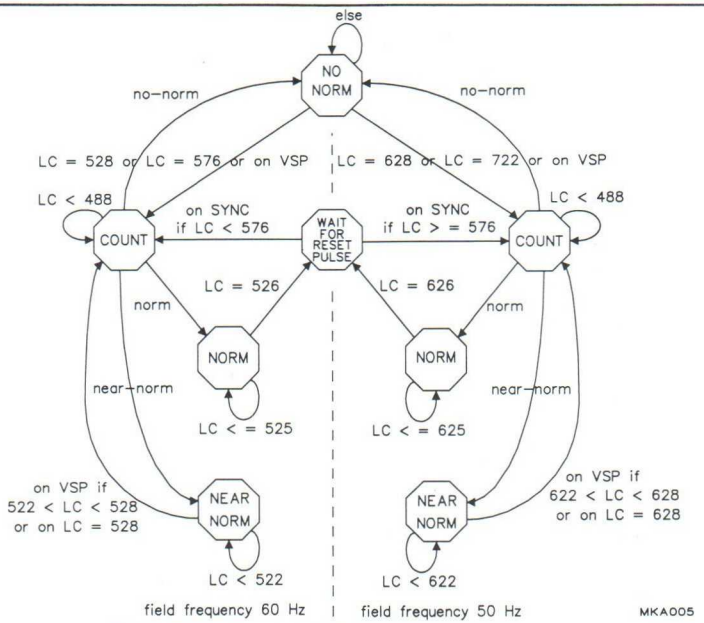


Fig.5 State diagram of the vertical divider system.

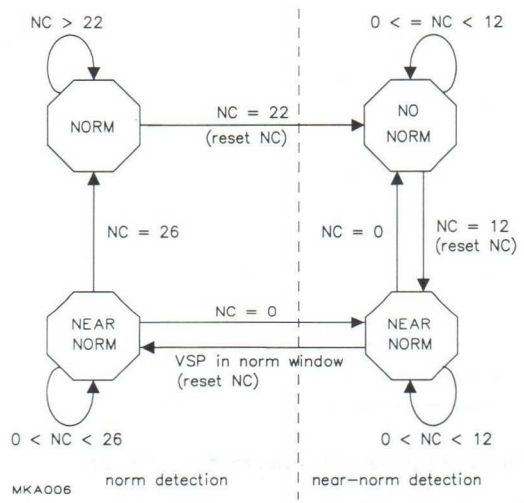


Fig.6 State diagram of the norm counter.

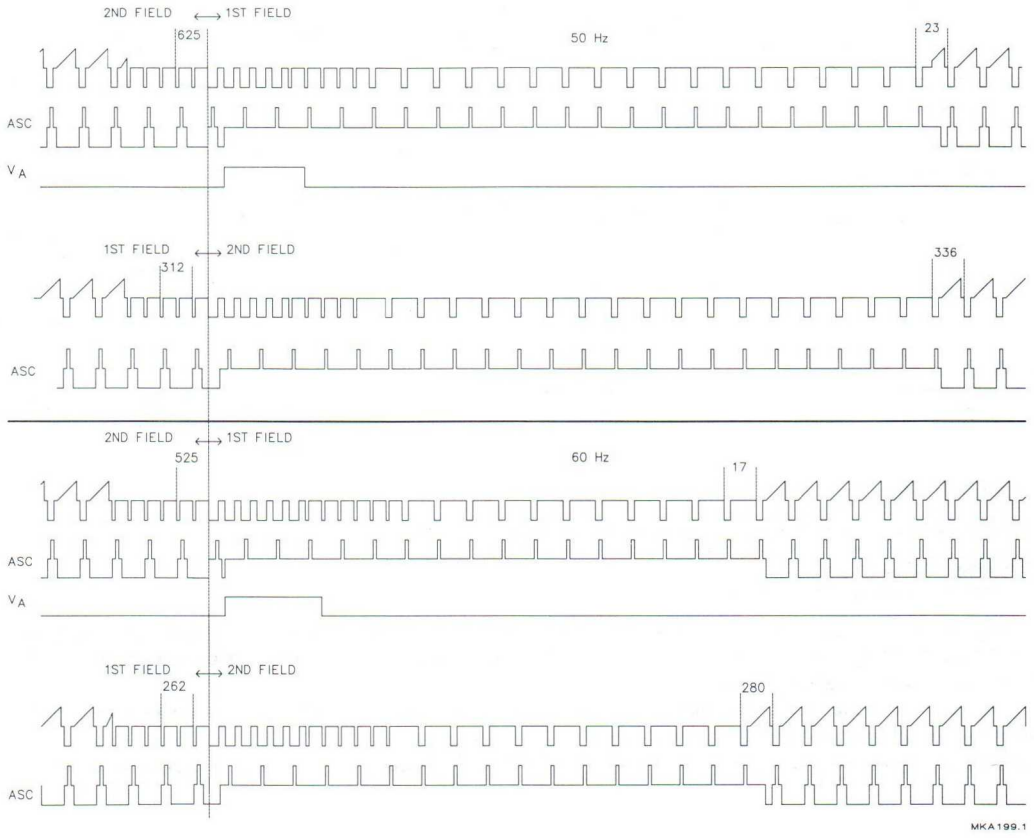


Fig.7 Acquisition sandcastle signal and V_A pulse timing diagram.

Table 1 Slave address (8A).

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	X	1	X

Table 2 Inputs.

SUBADDRESS	MSB							LSB
00	INA	INB	TB	ECMB	FOA	FOB	XA	XB
01	FORF	FORS	OPA	OPB	POC	FM	SAF	FRQF
02	EFS	STM	HU5	HU4	HU3	HU2	HU1	HU0
03	LCA	–	–	–	–	–	–	–

Table 3 Outputs.

ADDRESS	POR	FSI	YC	SL	IP	SAK	SBK	FRQ

I²C-bus protocol

If the address input is connected to the positive supply the address will change from 8A to 8E.

Valid subaddresses = 00 to 0F
Auto-increment mode available for subaddresses.

Start-up procedure: read the status byte until POR = 0; send subaddress 00 with the crystal indicator bits (XA and XB) indicating that only one crystal is connected to the IC; wait for 250 ms; send subaddress 01; wait for at least 100 ms; set XA, XB to the actual crystal configuration.
Each time before the data in the IC is refreshed , the staus byte must be read. If POR = 1, then the above procedure must be carried out to restart the IC.
Failure to stick to the above procedure may result in an incorrect line frequency after power-up or a power-dip.

INPUT SIGNALS

Table 4 Source select.

INA	INB	SOURCE
0	0	CVBS
0	1	YC
1	–	auto CVBS/YC

Table 5 Trap bypass.

TB	CONDITION
0	trap not bypassed
1	trap bypassed

Table 6 Comb filter enable.

ECMB	CONDITION
0	comb filter disabled
1	comb filter enabled

Table 7 Phase 1 time constant.

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 8 Crystal indication.

XA	XB	CRYSTAL
0	0	2 x 3.6 MHz
0	1	1 x 3.6 MHz
1	0	1 x 4.4 MHz
1	1	3.6 and 4.4 MHz

Table 9 Forced field frequency.

FORF	FORS	FIELD FREQUENCY
0	0	auto; 60 Hz if no lock
0	1	60 Hz
1	0	50 Hz
1	1	auto; 50 Hz if no lock

Table 10 Output value I/O port.

OPA	CONDITION
0	LOW
1	HIGH

Table 11 Output value O port.

OPB	CONDITION
0	LOW
1	HIGH

Table 12 Phase 1 loop control.

POC	CONDITION
0	phase one loop closed
1	phase one loop open

Table 13 Forced standard.

FM	SAF	FRQF	STANDARD
0	–	–	auto search
1	0	0	PAL/NTSC second crystal
1	0	1	PAL/NTSC reference crystal
1	1	0	illegal
1	1	1	SECAM reference crystal

Note to Table 13

If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal the colour will be switched off.

Table 14 Fast switch enable.

EFS	CONDITION
0	fast switch disabled
1	fast switch enabled

Table 15 Search tuning mode.

STM	CONDITION
0	search tuning mode off
1	search tuning mode on

Table 16 Hue.

FUNCTION	ADDRESS	DIGITAL NUMBER
hue	HU5 to HU0	000000 = −45 ° 111111 = +45 °

Table 17 Line-locked clock active.

LCA	CONDITION
0	OPB/CLP mode
1	LLC/HA mode

OUTPUT SIGNALS

Table 18 Power-on reset.

POR	CONDITION
0	normal mode
1	power-down mode

Table 19 Field frequency indication.

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 20 Input switch mode.

YC	CONDITION
0	CVBS mode
1	YC mode

Table 21 Phase 1 lock indication.

SL	CONDITION
0	not locked
1	locked

Table 22 Input value I/O port.

IP	CONDITION
0	LOW
1	HIGH

Table 23 Standard read-out.

SAK	SBK	FRQ	STANDARD
0	0	0	PAL second crystal
0	0	1	PAL reference crystal
0	1	0	NTSC second crystal
0	1	1	NTSC reference crystal
1	0	0	illegal forced mode
1	0	1	SECAM reference crystal
1	1	–	colour off

LIMITING VALUES

In accordance with the Absolute Maximum Rating System. (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		–	8.8	V
I_{CC}	supply current		–	60	mA
P_{tot}	total power dissipation		–	530	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−10	+65	°C
ESD	electrostatic discharge (on all pins)				
	Human body model	note 1	−2000	+2000	V
	Machine model	note 2	−200	+200	V

Notes to the limiting values

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	48 K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	45	–	mA
P_{tot}	total power dissipation		–	360	–	mW
Input switch						
Y/CVBS INPUT (PIN 26)						
$V_{26(p-p)}$	input voltage (peak-to-peak value)	top sync - white	–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
C INPUT (PIN 25)						
$V_{25(p-p)}$	input burst voltage (peak-to-peak value)		–	0.3	0.43	V
Z_I	input impedance		60	–	–	kΩ
CVBS OUTPUT (PIN 22) ONLY ADDRESS 8A						
$V_{22(p-p)}$	output voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
Z_O	output impedance		–	–	500	Ω
V_{tsl}	top sync voltage level		–	2.8	–	V
Bias generator (pin 8)						
V_8	digital supply voltage		–	5.0	–	V
Subcarrier regeneration						
GENERAL						
CR	catching range	note 1				
	reference crystal 4.4 MHz		±400	–	–	Hz
	reference crystal 3.6 MHz		tbf	–	–	Hz
	second crystal 3.6 MHz		±300	–	–	Hz
φ	phase shift					
	for 400 Hz deviation	4.4 MHz	–	–	5	deg
	for 300 Hz deviation	3.6 MHz	–	–	5	deg
TC	temperature coefficient of oscillator		–	tbf	–	Hz/K
Z_I	input impedance					
	reference crystal input		–	1.0	–	kΩ
	second crystal input		–	1.5	–	kΩ
V_{dep}	supply voltage dependency		–	tbf	–	V
FSCOMB OUTPUT (PIN 23)						
$V_{sub(p-p)}$	subcarrier output amplitude (peak-to-peak value)	C_L = 15 pF	150	200	300	mV
V_{cen}	comb enable voltage level		4.0	4.2	–	V
V_{cdis}	comb disable voltage level		–	0.8	1.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{sink}	minimum sink current to force output to comb disable level		0.4	–	2.0	mA
R_{GND}	value of grounded resistor to force output to comb disable level		0.4	–	2.0	kΩ
ACC						
	ACC control range		–20	–	+5	dB
	change of –(R–Y) and –(B–Y) signals over ACC range		–	–	1	dB
	colour killer threshold					
	PAL/NTSC		–	–25	–	dB
	SECAM		–	–23	–	dB
	kill - unkill hysteresis		–	3	–	dB
Demodulators –(R–Y) and –(B–Y) outputs (pins 1 and 2)						
	ratio of –(R–Y) and –(B–Y) signals	standard colour bar	1.20	1.27	1.34	
TC	temperature coefficient of –(R–Y) and –(B–Y) amplitude		–	tbf	–	Hz/K
	spread of –(R–Y) and –(B–Y) ratio between standards		–1	–	+1	dB
V_1	output level of –(R–Y) during blanking		–	2.0	–	V
V_2	output level of –(B–Y) during blanking		–	2.0	–	V
B	–3 dB bandwidth		–	1	–	MHz
Z_O	output impedance		–	–	500	Ω
V_{dep}	supply voltage dependency		–	tbf	–	V
PAL/NTSC DEMODULATOR						
$V_{1(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	standard colour bar	470	525	585	mV
$V_{2(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	standard colour bar	595	665	740	mV
α	crosstalk between –(R–Y) and –(B–Y)		–	tbf	–	dB
$V_{1,2(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{1,2(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
PAL DEMODULATOR						
$V_{R(p-p)}$	H/2 ripple (peak-to-peak value)		–	–	50	mV
S/N	signal-to-noise ratio		46	–	–	dB
NTSC DEMODULATOR						
φ	hue phase shift		–	±45	–	deg
SECAM DEMODULATOR						
$V_{1(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	standard colour bar	0.94	1.05	1.17	V
$V_{2(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	standard colour bar	1.19	1.33	1.48	V
f_{os}	black level offset		–	–	7	kHz
S/N	signal-to-noise ratio		–	43	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{res(p-p)}$	7.8 to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of deemphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3	4	5	V
NL	non linearity		–	–	3	%
Filters						
TUNING						
V_{tune}	tuning voltage		1.5	3.0	6.0	V
LUMINANCE DELAY						
t_d	delay time					
	PAL/NTSC		–	480	–	ns
	SECAM		–	480	–	ns
	B/W		–	220	–	ns
CHROMINANCE TRAP						
f_o	notch frequency					
		f_{SC} = 3.6 MHz	3.53	3.58	3.63	MHz
		f_{SC} = 4.4 MHz	4.37	4.43	4.49	MHz
		SECAM	4.23	4.29	4.35	MHz
		YC mode; not active				
B	bandwidth at –3 dB					
		f_{SC} = 3.6 MHz	–	2.5	–	MHz
		f_{SC} = 4.4 MHz	–	3.1	–	MHz
		SECAM	–	3.0	–	MHz
SUPP	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency					
		f_{SC} = 3.6 MHz	–	3.58	–	MHz
		f_{SC} = 4.4 MHz	–	4.43	–	MHz
B	bandwidth at –3 dB					
		f_{SC} = 3.6 MHz	–	1.4	–	MHz
		f_{SC} = 4.4 MHz	–	1.7	–	MHz
CLOCHE FILTER						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth at –3 dB	SECAM	241	268	295	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sync input						
VIDEO INPUT						
V_{26}	sync pulse amplitude	Y/CVBS input	50	300	600	mV
	slicing level		–	50	–	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
S/N	noise detector threshold level		–	20	–	dB
H	hysteresis		–	3	–	dB
t_d	delay between video signal and internally separated vertical sync pulse		12	18.5	27	µs
Horizontal section						
CLP OUTPUT (OPB/CLP MODE); H_A OUTPUT (LLC/HA MODE)						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	H_A pulse width (32 LLC pulses)		–	4.7	–	µs
t_d	delay between middle of horizontal sync pulse and middle of H_A	note 2	0.3	0.45	0.6	µs
t_d	delay between negative edge LLC pulse and positive edge H_A pulse	C_L = 15 pF	10	20	40	ns
t_W	CLP pulse width	21 LLC pulses	–	3.1	–	µs
t_d	delay between middle of horizontal sync pulse and start of CLP pulse	note 2	3.5	3.7	3.9	µs
FIRST LOOP						
Δf	frequency deviation when not locked		–	–	1.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	V
TC	temperature coefficient		–	tbf	–	Hz/°C
f_{CR}	catching range		±625	–	–	Hz
f_{HR}	holding range		–	–	±1.4	kHz
ϕ	static phase shift		–	–	0.1	µs/kHz
LLC OUTPUT (LLC/H_A MODE)						
f_O	output frequency					
	$432f_H$	50 Hz standard	–	6.75	–	MHz
	$432f_H$	60 Hz standard	–	6.80	–	MHz
$V_{O(p-p)}$	output amplitude (peak-to-peak value)	C_L = 15 pF	0.25	–	–	V
V_O	DC output voltage level		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical section						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency	FORF = 1; divider ratio 628	–	50	–	Hz
		FORF = 0; divider ratio 528	–	60	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
V_A output						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	V_A pulse width	50 Hz standard	–	160	–	µs
		60 Hz standard	–	192	–	µs
t_d	delay between start of vertical sync pulse and positive edge of V_A pulse		–	32	–	µs
Z_O	output impedance	STM = 1	3	–	–	MΩ
Sandcastle output (pin 10)						
V_{10}	zero level output voltage		0	0.5	1.0	V
I_{sink}	sink current		0.5	–	–	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.0	2.5	3.0	V
I_{source}	source current		0.5	–	–	mA
I_{ext}	external current required to force the output to the blanking level		1.0	–	3.0	mA
t_W	horizontal blanking pulse width	69 LLC pulses	–	10.2	–	µs
t_d	delay between start of horizontal blanking and start of clamping pulse	45 LLC pulses	–	6.7	–	µs
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.0	4.5	5.0	V
I_{source}	source current		0.5	–	–	mA
t_W	pulse width	21 LLC pulses	–	3.1	–	µs
t_d	delay between middle sync of input and start of clamping pulse	note 2	3.5	3.7	3.9	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour matrix						
G_v	gain					
	from R to Y		–	0.43	–	
	from G to Y		–	0.84	–	
	from B to Y		–	0.16	–	
	from R to U_{out}		–	0.43	–	
	from G to U_{out}		–	0.84	–	
	from B to U_{out}		–	1.27	–	
	from R to V_{out}		–	1.00	–	
	from G to V_{out}		–	0.84	–	
	from B to V_{out}		–	0.16	–	
Output and input/output port						
O PORT (OPB/CLP MODE)						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		100	–	–	µA
I_{source}	source current		100	–	–	µA
I/O PORT (OPB/CLP MODE)						
V_{OH}	HIGH level output voltage		–	–	V_{SUP}	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
V_{IH}	HIGH level input voltage		2.0	–	–	V
V_{IL}	LOW level input voltage		–	–	0.6	V
YUV switches (note 3)						
RGB INPUTS (NOTE 3)						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 4	–	0.7	1.0	V
Z_I	input impedance		3	–	–	MΩ
UV INPUTS (NOTE 3)						
$V_{I(p-p)}$	U input voltage (peak-to-peak value)	note 3	–	1.33	1.90	V
$V_{I(p-p)}$	V input voltage (peak-to-peak value)		–	1.05	1.50	V
Z_I	input impedance (both inputs)		3	–	–	MΩ
Y OUTPUT						
$V_{O(p-p)}$	U output voltage (peak-to-peak value)	note 4; top sync-to-white	–	1.43	–	V
Z_O	output impedance		–	–	250	Ω
V_O	DC output voltage level	top sync	–	2.5	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV switches (note 3)						
RGB INPUTS (NOTE 3)						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 4	–	0.7	1.0	V
Z_I	input impedance		3	–	–	MΩ
UV INPUTS (NOTE 3)						
$V_{I(p-p)}$	U input voltage (peak-to-peak value)	note 3	–	1.33	1.90	V
$V_{I(p-p)}$	V input voltage (peak-to-peak value)		–	1.05	1.50	V
Z_I	input impedance (both inputs)		3	–	–	MΩ
Y OUTPUT						
$V_{O(p-p)}$	U output voltage (peak-to-peak value)	note 4; top sync-to-white	–	1.43	–	V
Z_O	output impedance		–	–	250	Ω
V_O	DC output voltage level	top sync	–	2.5	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB
UV OUTPUTS (NOTE 3)						
$V_{O(p-p)}$	U output voltage (peak-to-peak value)		–	1.33	1.90	V
$V_{O(p-p)}$	V output voltage (peak-to-peak value)		–	1.05	1.50	V
Z_O	output impedance (both outputs)		–	–	250	Ω
V_O	DC output voltage level		–	2.7	–	V
GENERAL						
V_{diff}	difference between black levels of YUV outputs in RGB mode and YUV mode	sync locked	–	–	10	mV
NL	non-linearity	any input to any output	–	–	5	%
B	bandwidth	any input to any output	–	7	–	MHz
CT	crosstalk between RGB and UV_{in} signals on UV_{out}	f = 0 to 5 MHz	–	–	–50	dB
FAST SWITCH SELECT INPUT (PIN 18)						
V_{IH}	HIGH level input voltage	RGB switched on	0.9	–	3.0	V
V_{IL}	LOW level input voltage	UV switched on	0	–	0.5	V
G_v	gain from U_{in} to U_{out} from V_{in} to V_{out}		 – –	 1 1	 – –	
t_d	switching delay	between pin 18 and YUV	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT CLAMP (PIN 17)						
V_{IH}	HIGH level input voltage	clamping	2.4	–	5.5	V
V_{IL}	LOW level input voltage	no clamping	0	–	0.6	V
t_W	clamping pulse width		1.8	3.5	–	µs
V_{os}	clamping offset voltage on UV outputs		–	–	10	mV
Z_I	input impedance	STM = 1	3	–	–	MΩ

Notes to the characteristics

1. All oscillator specifications are measured with the Philips crystal series 4322 143/144. If the spurious response of the reference crystal is less than –3 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequenct is guaranteed. The spurious response of the second crystal must be less than –3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.

   The catching and detuning range are measured for nominal crystal parameters. These are:

   load resonance frequency f_0 (C_L = 20 pF) = 4.433619 MHz, (second crystal: 3.579545 MHz)

   motional capacitance C_M = 20.6 fF, (second crystal: 14.7 fF)

   parallel capacitance C_0 = 5.5 pF, (second crystal: 4.5 pF).

   The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.
2. This delay is caused by the low pass filter at the sync separator input.
3. The output signals of the demodulator are called –(R–Y) and –(B–Y). The colour difference input and output signals of the YUV switch are called UV signals. However, these signals do not have the amplitude correction factor of real UV signals. They are called UV signals and not –(R–Y) and –(B–Y) to prevent confusion between the colour difference signals of the demodulator and the colour difference signals of the YUV switch.
4. This value refers to signals including a sync pulse. For Y signals composed ot the RGB inputs this output voltage is 30% lower, as there is no sync pulse on such signals.

QUALITY SPECIFICATION

Quality level in accordance with URV 4-2-59/601.

TEST AND APPLICATION INFORMATION

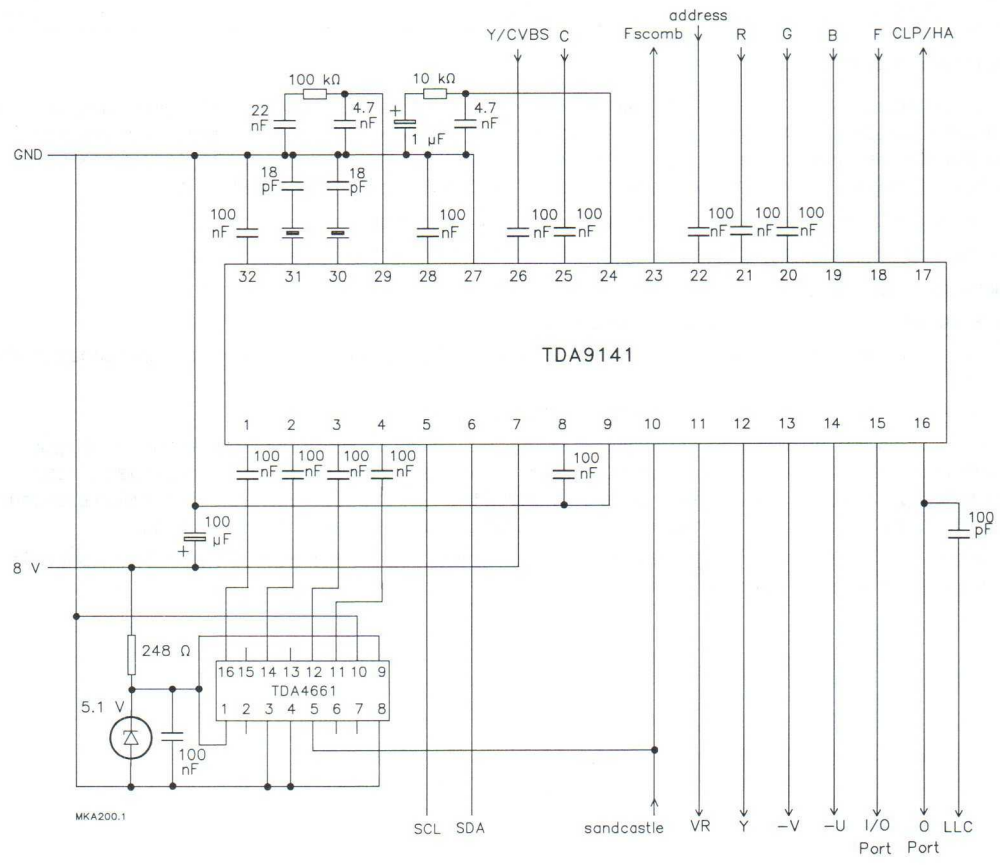


Fig.8 Application diagram.

Notes to figure 8

1. Pins 28 and 32 are sensitive to leakage current.
2. The analog and digital ground currents should be completely separated.
3. The decoupling capacitor connected between pins 8 and 9 must be placed as close to the IC as possible.

Programmable deflection controller TDA9150B

FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Flash detection with restart
- Two-level sandcastle pulse.

Vertical deflection

- Self adaptive 16-bit precision vertical scan
- DC coupled deflection to prevent picture bounce
- Programmable fixed compression to 75%
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity
- Programmable de-interlace phase.

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity.

Horizontal deflection

- Phase 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Over voltage protection/detection with selection and status bit.

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter.

GENERAL DESCRIPTION

The TDA9150B is a programmable deflection controller contained in a 20-pin DIP package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9150B uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device is self-adaptive for a number of functions and is fully programmable via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9150B	20	DIP	plastic	SOT146-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
T_{amb}	operating ambient temperature		–25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	
V_{12}	vertical sync (V_A) logic level		–	TTL	–	
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	
V_{17}	serial data input (SDA) logic level		–	CMOS 5 V	–	
V_{PSL}	horizontal flyback (HFB) phase slicing level	FBL = logic 0	–	3.9	–	V
		FBL = logic 1	–	1.3	–	V
V_1	horizontal flyback (HFB) blanking slicing level		–	100	–	mV
V_3	over voltage protection (PROT) level		–	3.9	–	V
V_9	EHT flash detection level		–	1.5	–	V
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
I_{11}–$I_{10(M)}$	vertical differential ($VOUT_{A, B}$) output current (peak value)	vertical amplitude = 100%; I_8 = –120 µA; note 2	440	475	510	µA
$V_{10,11}$	vertical output voltage		0	–	3.9	V
$I_{6(M)}$	EW (EWOUT) total output current (peak value)	I_8 = –120 µA	–	–	930	µA
V_6	EW (EWOUT) output voltage		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_2	base voltage level		–	0.5	–	V
V_2	horizontal and vertical blanking voltage level		–	2.5	–	V
V_2	video clamping voltage level		–	4.5	–	V
HORIZONTAL OFF-CENTRE SHIFT (OFCS)						
V_{19}	output voltage	I_{19} = 2 mA	0	–	V_{CC}	V

Notes

1. Hard wired to ground or V_{CC} is highly recommended.
2. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.

BLOCK DIAGRAM

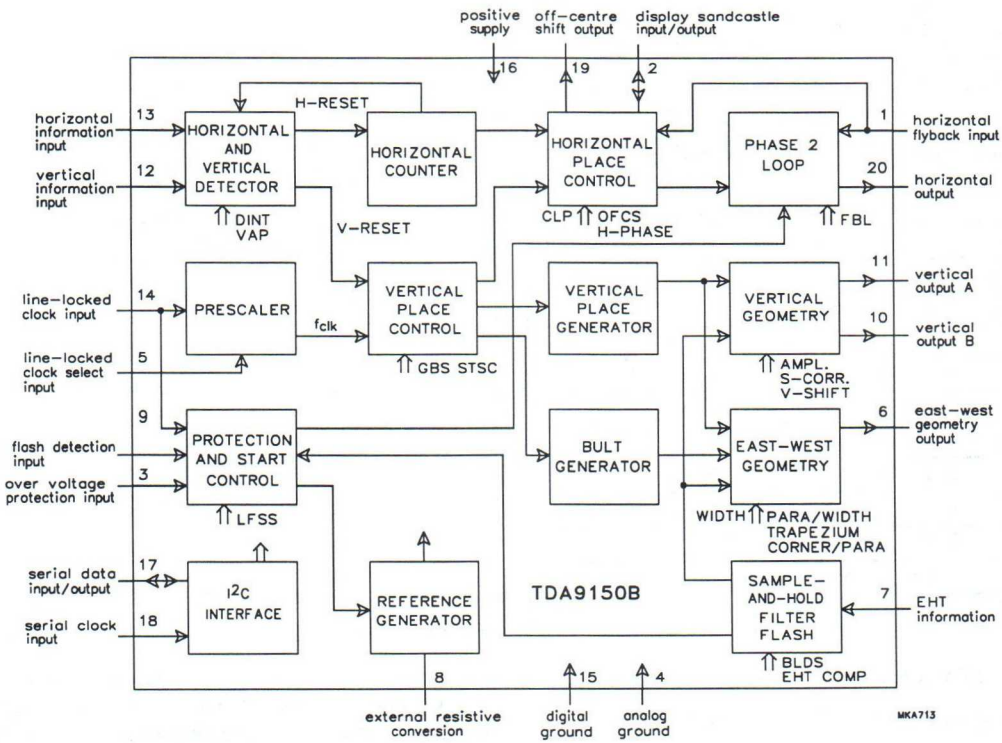


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over voltage protection input
AGND	4	analog ground
LLCS	5	line-locked clock selection input
EWOUT	6	east-west geometry output
EHT	7	EHT compensation
R_{CONV}	8	external resistive conversion
FLASH	9	flash detection input
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
DGND	15	digital ground
V_{CC}	16	supply input (+8 V)
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

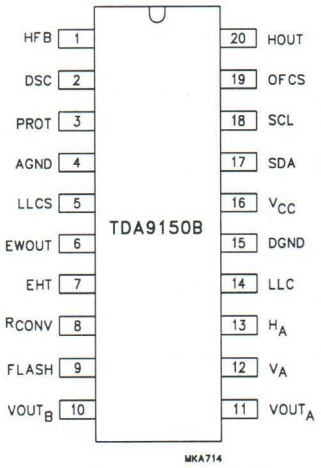


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9150B requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I^2C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.

I^2C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and/or V_A inputs for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs, the EW output current will drop to zero and the vertical output current will drop to 20% of the adjusted value within 100 µs). The SDA and SCL inputs meet the I^2C-bus specification, the other three inputs are TTL compatible.

The LLC frequency can be divided-by-two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.

The LLC timing is given in the Chapter "Characteristics".

I²C-bus commands

Slave address: **8C HEX = 1000110X BIN**

READ MODE

The format of the status byte is: PON PROT 0 0 0 0 0 0

Where:

PON is the status bit for power-on reset (POR) and after power failure:

- Logic 1:
  - after the first POR and after power failure; also set to 1 after a severe voltage dip that may have disturbed the various settings
  - POR 1 to 0 transition, V_{CC} = 6.25 V (typ.)
  - POR 0 to 1 transition, V_{CC} = 5.75 V (typ.)
- Logic 0:
  - after a successful read of the status byte.

PROT is the over voltage detection for the scaled EHT input:

- Logic 1:
  - if the scaled EHT rises above the reference value of 3.9 V
- Logic 0:
  - after a successful read of the status byte and EHT <3.9 V.

Remark: a read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode with auto increment; subaddress and data byte format.

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Vertical amplitude	00	X[1]	X	A5	A4	A3	A2	A1	A0
Vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
Vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
Vertical off-centre shift	03	X	note 2	note 2	note 2	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	note 2	note 2	note 2
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
Horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
Horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
Clamp shift	0A	X	X	X	X	X	A2	A1	A0
Control 1	0B	MS	WS	FBL	VAP	BLDS	LFSS	DINT	GBS
Control 2	0F	X	X	X	VPR	CPR	DIP	PRD	CSU

Notes

1. X = don't care.
2. Data bit used in another function.

Table 2 Control bits.

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	Line stop: EW output current becomes zero and the vertical output current is reduced to 20% of the adjusted value. LFSS becomes logic 0 after a HIGH on PON.
	1	Line start enabled: the soft start mechanism is now activated.
DINT	0	De-interlace on: the V_A pulse is sampled at a position selected with control bit DIP.
	1	De-interlace off: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset.
BLDS	0	Aquadag selected.
	1	Bleeder selected.
GBS	0	Becomes logic 0 after power-on.
	1	Guard band 48/12 lines.
VAP	0	Positive V_A edge detection.
	1	Negative V_A edge detection.
FBL	0	Horizontal flyback slicing level = 3.9 V.
	1	Horizontal flyback slicing level = 1.3 V.
CSU	0	No clamping suppression, standard mode of operation.
	1	Clamping suppression in wait, stop and protection modes (used in systems with e.g. TDA4680/81).
PRD	0	No defeat of HOUT, the over voltage information is only written in the PROT status bit.
	1	HOUT is defeated and status bit PROT is set when over voltage is detected.
DIP	0	V_A is sampled 42 clock pulses after the leading edge of H_A.
	1	V_A is sampled 258 clock pulses after the leading edge of H_A.
CPR	0	Nominal amplitude.
	1	Compression to 75% of adjusted amplitude, used for display of 16 : 9 standard pictures on 4 : 3 displays.
VPR	0	Nominal amplitude (100%) during wait, stop and clipping.
	1	Amplitude reduced to 20% during wait, stop and clipping.

Table 3 Explanation of control bits shown in Table 2.

CONTROL BITS	DESCRIPTION
LFSS	line frame start/stop
DINT	de-interlace
BLDS	bleeder mode selection
GBS	guard band selection
VAP	polarity of V_A edge detection
FBL	flyback slicing level
CSU	clamping suppression mode
PRD	protection/detection mode
DIP	de-interlace phase
CPR	compression on/off
VPR	vertical power reduction mode

Table 4 Clock frequency control bit (pin 5; note 1).

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler on: the internal clock frequency $f_{clk} = \frac{1}{2}f_{LLC}$
	1	prescaler off (default by internal pull-up resistor): the internal clock frequency $f_{clk} = f_{LLC}$

Note

1. Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to ground or V_{CC}. Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and large flyback pulses. The permitted combinations of LLC and the prescaler are shown in Table 5.

Table 5 Line duration with prescaler.

LLC (MHz)	ON (μs)	OFF (μs)
6.75	note 1	64
13.5	64	32
27	32	note 1

Note

1. Combination not allowed.

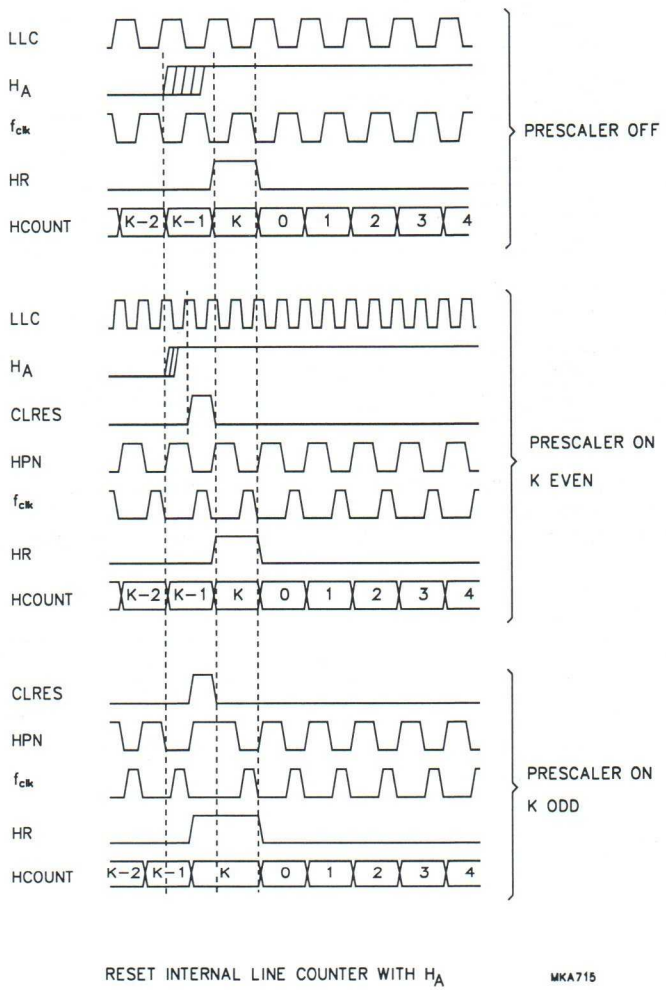


Fig.3 Timing relations between LLC, H_A and line counter.

Horizontal part (pins 1, 2, 13, 19 and 20)

SYNCHRONIZATION PULSE

The H_A input (pin 13) is a TTL-compatible CMOS input. Pulses on this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW periods is 2 internal clock periods.

FLYBACK INPUT PULSE

The HFB input (pin 1) is a CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08), as illustrated in Fig.7. The resolution is 6-bit.

OUTPUT PULSE

The HOUT pulse (pin 20) is an open-drain NMOS output. The duty factor for this output is typically $^{52}/_{48}$ (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 5 to 52% over a minimum period of 2000 lines in 2000 steps.

OFF-CENTRE SHIFT

The OFCS output (pin 19) is a push-pull CMOS output which is driven by a pulse-width modulated DAC.

By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 × 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.8.

SANDCASTLE

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamping. As an input it acts as a current sensor during the vertical blanking interval for guard detection.

CLAMPING PULSE

The clamping pulse width is 21 internal clock periods. The shift, with respect to H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.9. It is possible to suppress the clamping pulse during wait, stop and protection modes with control bit CSU. This will avoid unwanted reset of the TDA4680/81 (only used in those circuits).

HORIZONTAL BLANKING

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{clk}/f_H ratio K in accordance with 41 – (432 – K).

Stop of the horizontal blanking pulse is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level crossing as illustrated in Fig.10.

VERTICAL BLANKING

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Section "Vertical guard").

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02 (see Figs 11 and 12).

VERTICAL GUARD

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 800 μA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in the event of missing or malfunctioning vertical deflection (see Figs 11 and 12).

Vertical part (pins 6, 8, 10, 11 and 12)

SYNCHRONIZATION PULSE

The V_A input (pin 12) is a TTL-compatible CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods. For further requirements on minimum pulse width see also Section "De-interlace".

VERTICAL PLACE GENERATOR

With control bit CPR a compress to 75% of the adjusted values is possible in all modes of operation. This control bit is used to display 16 : 9 standard pictures on 4 : 3 displays. No new adjustment of other corrections, such as corner and S-correction, is required.

With control bit VPR a reduction of the current during clipping, wait and stop modes to 20% of the nominal value can be selected, which will reduce the dissipation in the vertical drive circuits.

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 × 432 clock periods in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.

The minimum number of synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15 625 or 31250 Hz respectively.

If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.

Amplitude control is automatic, with a settling time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit.

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

DE-INTERLACE

With de-interlace on (DINT = logic 0), the V_A pulse is sampled with LLC at a position supplied by control bit DIP (de-interlace phase).

When DIP = logic 0 sampling takes place 42 clock pulses after the leading edge of H_A ($T = T_{line} \times 42/432$).

When DIP = logic 1 sampling takes place 258 clock pulses after the leading edge of H_A ($T = T_{line} \times 258/432$).

The distance between the two selectable sampling points is ($T_{line} \times (258 - 42)/432$) which is exactly half a line, thus de-interlace is possible in two directions.

The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to caught, in this event an active time of minimum of half a line (see Fig.13 which has an integration time of $T_{line} \times 1/4$ for the V_A pulse).

With de-interlace off, the V_A pulse is sampled with the system clock. The leading edge is detected and used as the vertical reset. Selection of the positive or negative leading edge is achieved by the control bit VAP.

VERTICAL GEOMETRY PROCESSING

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The external resistive conversion (R_{CONV}) at pin 8 sets the reference current for both the vertical and EW geometry processing. A useful range is 100 to 150 µA, the recommended value is 120 µA.

VERTICAL OUTPUTS

The vertical outputs $VOUT_A$ and $VOUT_B$ on pins 10 and 11 together form a differential current output. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with a 6-bit resolution.

The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is –1.5 to +1.5% ($\pm 1/8 \times I_8$) in 7 steps set by the least significant nibble at subaddress 03.

EW GEOMETRY PROCESSING

The EW geometry processing is DC coupled and therefore independent of field frequency. R_{CONV} sets the reference current for both the vertical and EW geometry processing.

The EW output is an ESD-protected single-ended current output.

The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of –40 to 0% in 63 steps via subaddress 06.

The EW trapezium correction can be set from –1.5 to +1.5% in 7 steps via the most significant nibble at subaddress 03.

BULT GENERATOR

The Bult generator makes the EW waveform continuous (see Fig.20).

Protection input (pin 3)

The protection input (PROT) is a CMOS input.

The input voltage must be EHT scaled and has the following characteristics:

Two modes of protection are available with the aid of control bit PRD.

- With PRD = logic 1 the protection mode is selected, HOUT will be defeated and the PROT bit in the status word is set if the input voltage is above 3.9 V. Thus the deflection stops and EW output current is zero, while the vertical output current is reduced to 20% of the adjusted value. A new start of the circuit is I²C-bus controlled with the user software.
- With PRD = logic 0 the detection mode is selected, HOUT will not be defeated and the over voltage information is only written in the PROT status bit and can be read by the I²C-bus.

All further actions, such as a write of the LFSS bit, are achieved by the I²C-bus. They depend on the configuration used and are defined by user software.

Flash detection/protection input (pin 9)

The FLASH input is a CMOS input with an internal pull-up current of approximately 8 μA.

When a negative-going edge crosses the 0.75 V level a restart will be executed with a soft start of approximately 2000 lines, such as in the soft-start mode. When the function is not used pin 9 can be connected to ground, V_{CC} or left open-circuit, the internal pull-up current source will prevent any problems. However a hard wired connection to V_{CC} or ground is recommended when the function is not used.

EHT compensation (pin 7)

The EHT input is a CMOS input.

The EHT compensation input permits scan amplitude modulation should the EHT supply not be perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, provided by the ratio $R_{CONV\text{-}EW}/R_{CONV}$, must be $^1/_{16}V_{scan} \times V_{ref}$ (see Fig.14).

The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS).

EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from –10 to +9.7%.

INTERNAL CIRCUITRY

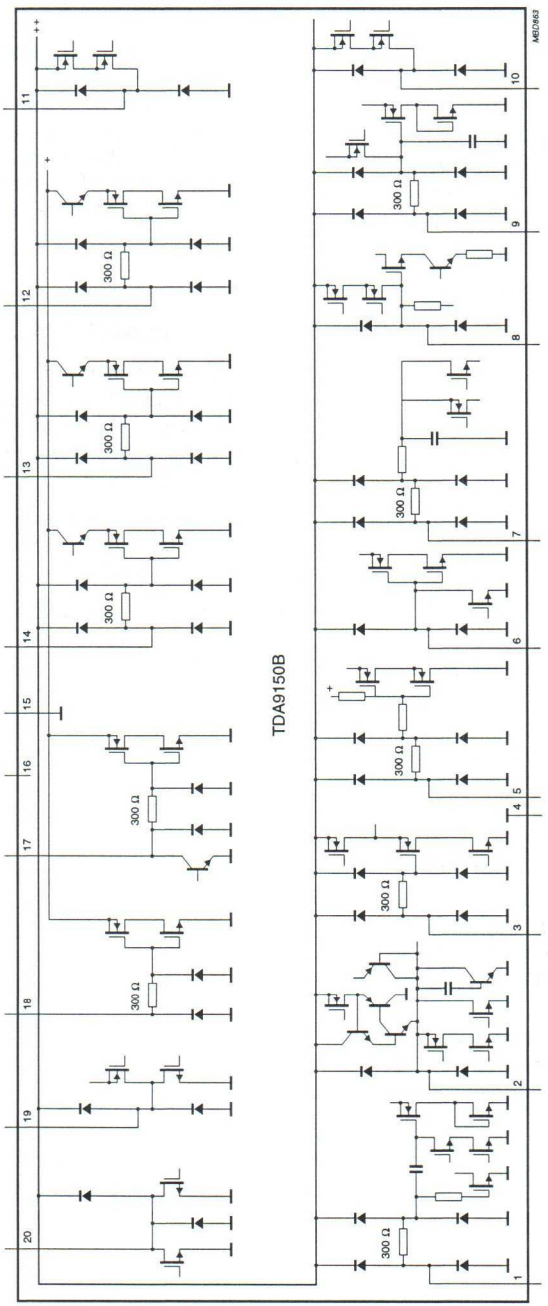


Fig.4 Internal circuitry.

APPLICATION INFORMATION

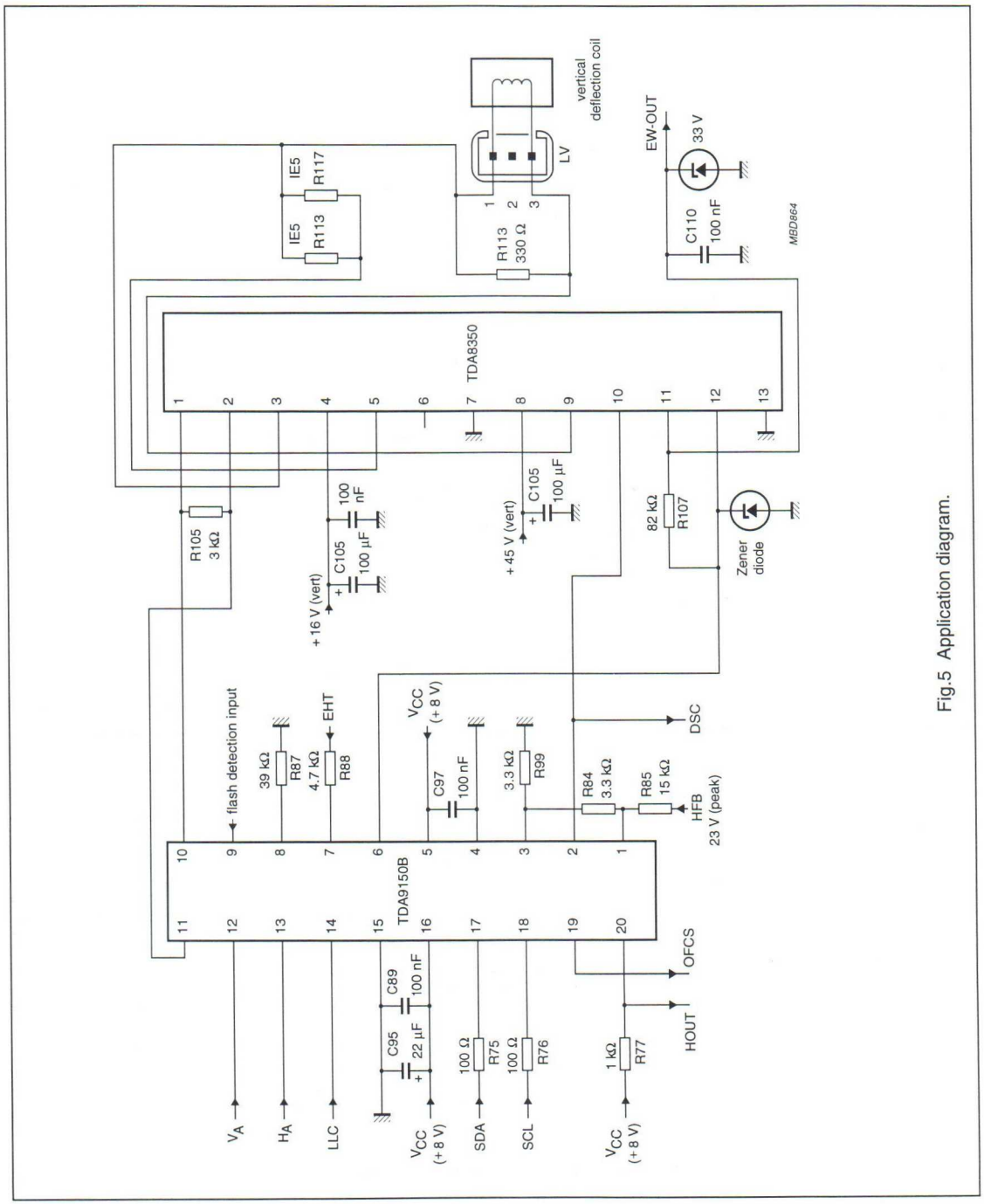


Fig.5 Application diagram.

TIMING DIAGRAMS

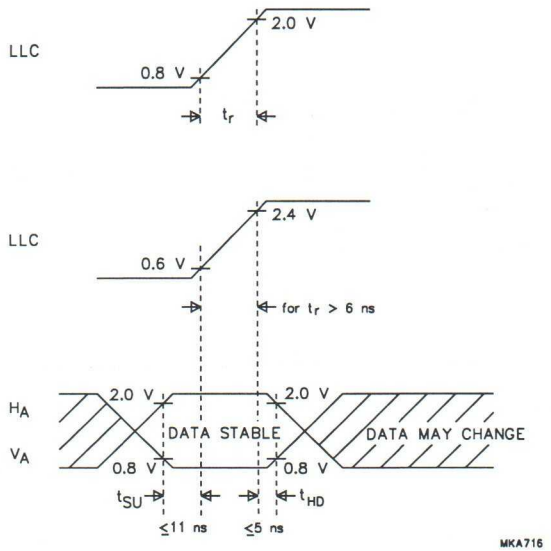


Fig.6 Timing requirements for LLC, H_A and V_A.

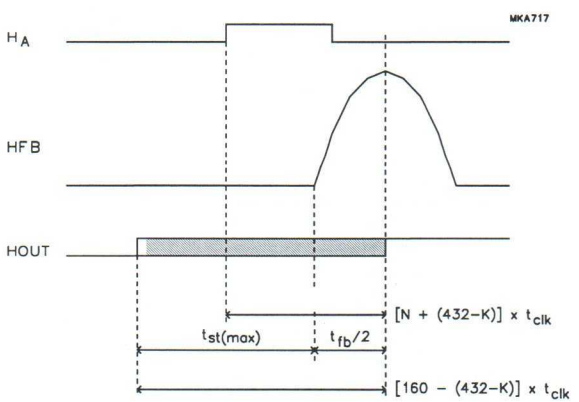


Fig.7 Horizontal phase and HOUT control range.

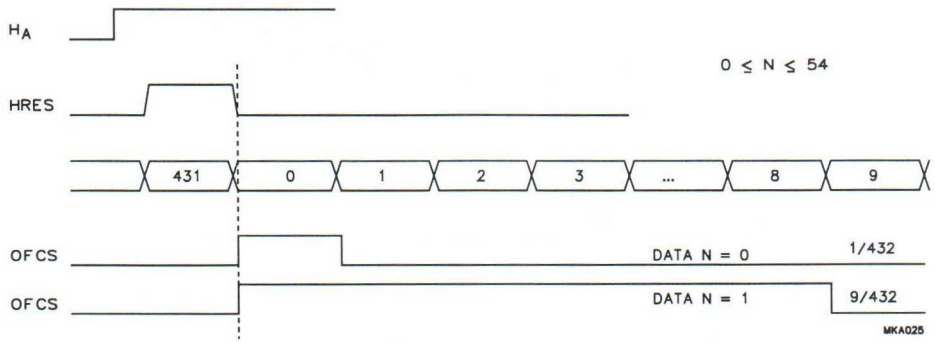


Fig.8 OFCS duty factor.

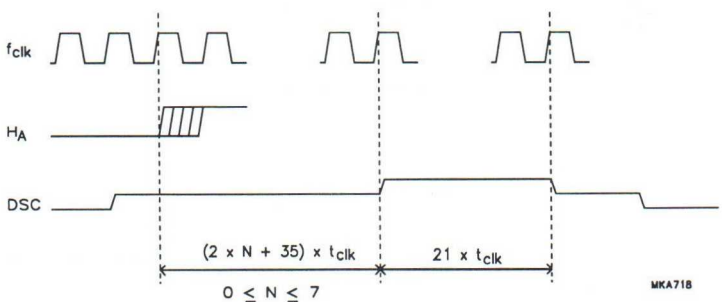


Fig.9 DSC clamping pulse.

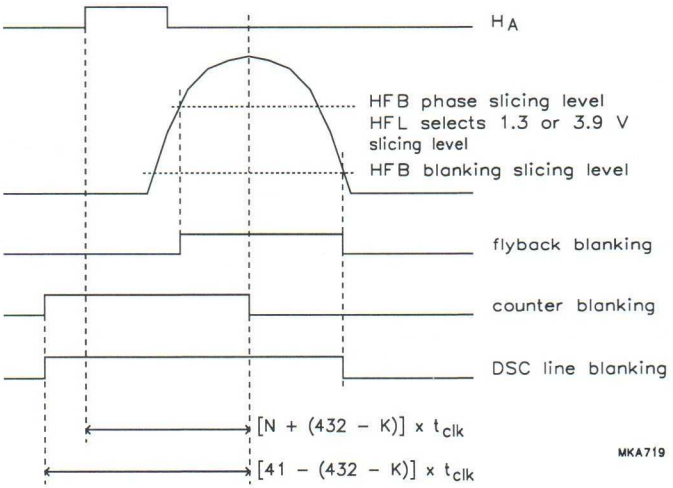


Fig.10 DSC line blanking.

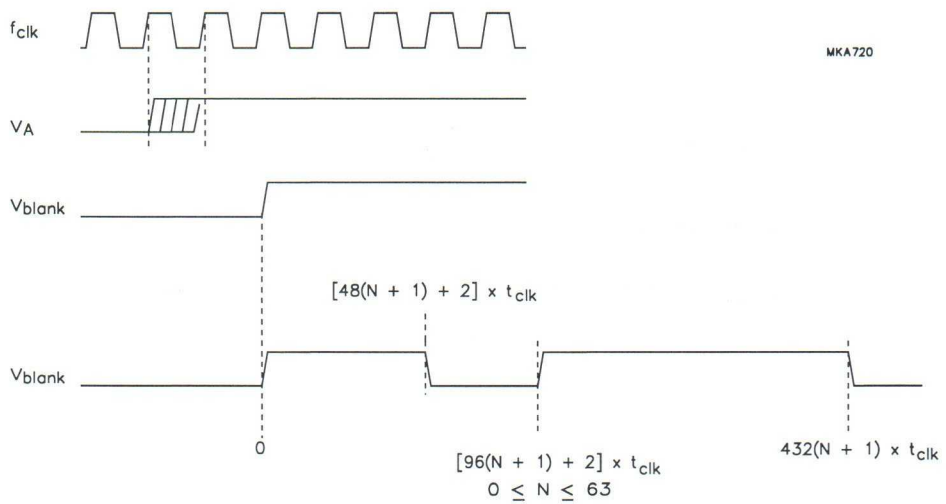
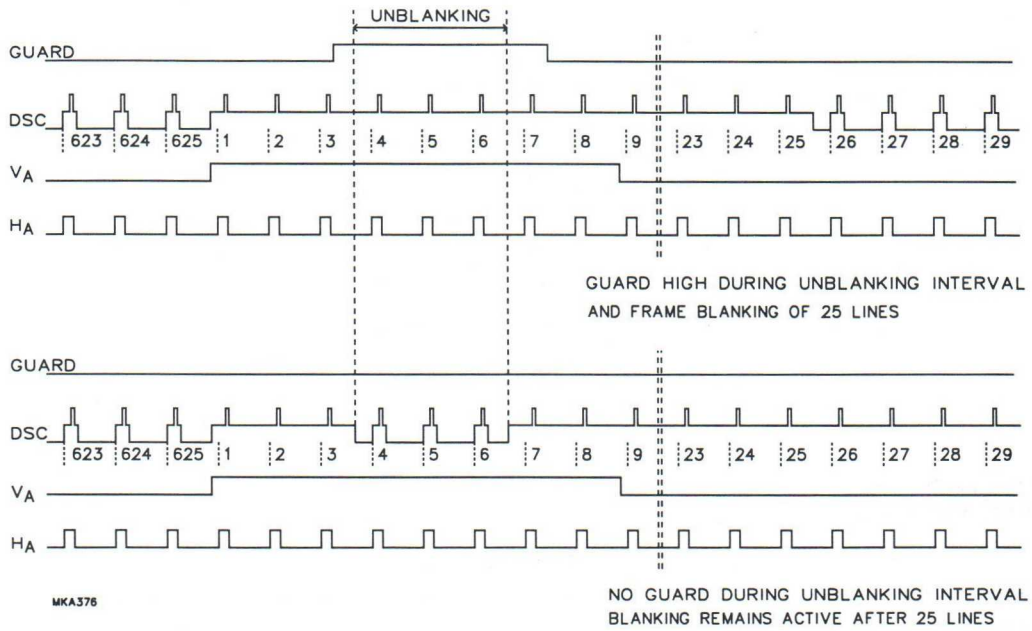
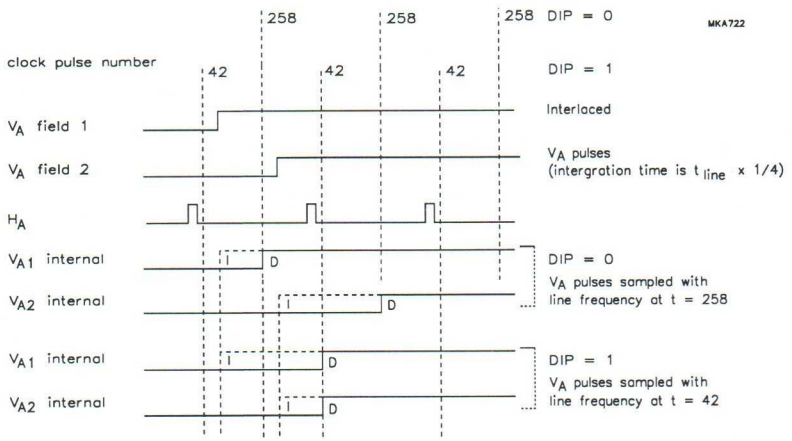


Fig.11 DCS vertical blanking with unblanking.



Vertical blanking LOW period: during scan, during unblanking.
Vertical blanking HIGH period (2.5 V): during STSC.
Vertical blanking continuously HIGH: POR = logic 1, LFSS = logic 0, no guard detected.

Fig.12 DSC with guard interval; start scan = 24.



I = start V_A for DINT = logic 1.
D = start V_A for DINT = logic 0.

Fig.13 De-interlace timing.

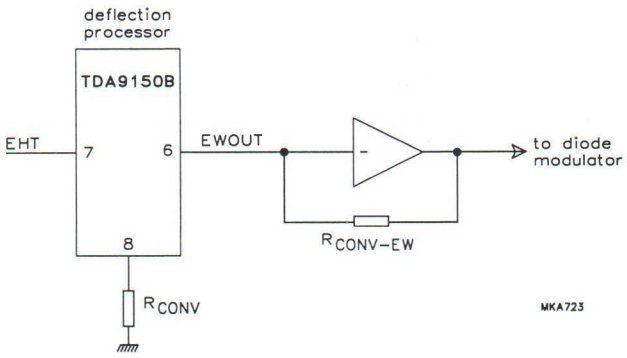


Fig.14 Explanation of $R_{CONV-EW}/R_{CONV}$ ratio.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	8.8	V
I_{CC}	supply current	−10	+50	mA
P_{tot}	total power dissipation	−	500	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 14 and 17 to 20	−0.5	V_{CC} + 0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16	−20	+20	mA
V_{ESD}	electrostatic handling for all pins (note 1)	−	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; DGND = AGND = 0 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
V_{por}	power-on reset	POR 1-to-0 transition	–	6.25	7.0	V
		POR 0-to-1 transition	5.0	5.75	–	V
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 17)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	–	–	V
I_{IL}	LOW level input current (pin 17)	$V_{17} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 17)	$V_{17} = V_{CC}$	–	–	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	–	–	0.4	V
V_{18}	SCL input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 18)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	–	–	V
I_{IL}	LOW level input current (pin 18)	$V_{18} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 18)	$V_{18} = V_{CC}$	–	–	10	µA
Line-locked clock and line-locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		–	–	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	–	–	V
I_{14}	input current	V_{14} = <5.5 V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	
δ_0	duty factor	LLCS = logic 0; at 1.4 V; note 2	40	50	60	%
δ_1	duty factor	LLCS = logic 1; at 1.4 V; note 2	25	50	75	%
TIMING (PRESCALER ON; $f_{clk} = \frac{1}{2}f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	856	864	865	
		H unlocked	–	866	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432.5	
		H unlocked	–	433	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TIMING (PRESCALER OFF; $f_{clk} = f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		6.2	–	15.5	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SSD}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{13}	input current	$V_{13} = 5.5$ V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
HFB (pin 1)						
V_{PSL}	phase slicing level	FBL = logic 0	3.7	3.9	4.1	V
		FBL = logic 1	1.1	1.3	1.5	V
V_{blank}	blanking slicing level		0	0.1	0.2	V
I_1	input current		–10	–	+10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	$N \times t_{clk}$	$N + (432 - K) \times t_{clk}$	
	number of steps		–	63	–	
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	$I_{20} = 0$	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{20} = 10$ mA	–	–	0.5	V
I_{20}	input current	output off	–10	–	+10	µA
δ	duty factor	normal operation	51	52	53	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	5	%
CR	control range		5	–	53	%
t_{ss}	soft start time		1500	–	3000	lines
Switch-off time to the centre of the flyback pulse						
CR	control range	note 3	0	–	160 – (432 – K) × t_{clk}	
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
k	correction factor	note 4	–	0.5	–	
σ	sigma value of phase jitter	note 5	–	750	–	ps
PSRR	power supply rejection ratio		–	–	10	ns/V
Horizontal off-centre shift (pin 19; N = off-centre shift data)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{19} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{19} = –2 mA	V_{CC} –0.5	–	–	V
$\delta_{(max)}$	maximum duty factor	N <54	1/K	(8N + 1)/K	425/K	%
δ	duty factor	N ≥54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamping voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking voltage level		2.0	2.5	3.0	V
V_{base}	base voltage level		0	0.5	1.0	V
I_2	output current	guard not detected	–1.0	–	+0.35	mA
		guard detected	0.8	–	2.5	mA
t_r	rise time		–	60	–	ns
t_f	fall time		–	60	–	ns
Clamping pulse (N = clamp pulse shift data)						
t_W	clamping pulse width		–	21 × t_{clk}	–	
t_{clamp}	clamp pulse shift w.r.t H_A		35	(2N + 35) × t_{clk}	49	
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41 – (432 – K) × t_{clk}	41	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start-scan data)						
t_{start}	start interval w.r.t V_A	no wait	$\{48(N+1) +2\} \times t_{clk}$	–	–	
t_{stop}	stop interval w.r.t V_A	no wait	$\{96(N+1) +2\} \times t_{clk}$	–	–	
Vertical section						
INPUT SIGNALS (PIN 12; V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} <5.5 V	−10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
t_{WH}	pulse width HIGH	de-interlace mode	$0.5 \times t_{line}$	–	–	
t_{WL}	pulse width LOW	de-interlace mode	$0.5 \times t_{line}$	–	–	
Vertical place generator (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
L_{max}	maximum number of synchronized lines per scan		–	910	–	lines/ scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
L_{min}	minimum number of synchronized lines per scan		–	200	–	lines/ scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = logic 0	–	16/12	–	lines
		GBS = logic 1	–	48/12	–	lines
	settling time		1	1.5	2	new fields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical geometry processing						
$\Delta I_{(M)}$	vertical differential output current between $VOUT_A$ and $VOUT_B$ (peak value)	V_A = 100%; note 6; I_8 = −120 µA	440	475	510	µA
D/ΔT	drift over temperature range		–	–	10^{-4}	K^{-1}
	amplitude error due to S-correction setting		–	–	2	%
$½(I_{10}+I_{11})$	vertical output signal bias current	I_8 = −120 µA	275	325	375	µA
I_{os}	vertical output offset current	note 7	–	–	1	%
OS/ΔT	offset over temperature range		–	–	10^{-4}	K^{-1}
V_{10}	vertical output voltage (pin 10)		0	–	3.9	V
V_{11}	vertical output voltage (pin 11)		0	–	3.9	V
CMRR	common mode rejection ratio		–	–	1	%/V
LE	linearity error	adjacent blocks; note 8	–	–	2.0	%
		non-adjacent blocks; note 8	–	–	3.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range	note 9	81	–	119	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range	note 9	0	–	15	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		$-⅛I_8$	–	$+⅛I_8$	µA
	number of steps		–	7	–	
EW output (pin 6)						
V_6	output voltage	note 10	1.0	–	5.5	V
I_6	output current	I_8 = −120 µA; note 11	15	–	930	µA
RR	output ripple rejection		–	0.15	1	%/V
D/ΔT	output drift over temperature range		–	–	5.10^{-4}	K^{-1}
EW WIDTH/WIDTH RATIO						
CR	control range	note 9	100	–	81	%
I_{eq}	equivalent output current		15	–	440	µA
	number of steps		–	63	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW PARABOLA/WIDTH RATIO						
CR	control range	note 9	1	–	19	%
I_{eq}	equivalent output current	width = 100%	10	–	430	µA
		width = 80%	10	–	345	µA
	number of steps		–	63	–	
EW CORNER/EW PARABOLA RATIO						
CR	control range	notes 9 and 12	40	–	0	%
I_{eq}	equivalent output current	width = 100%	0	–	200	µA
		width = 80%	0	–	160	µA
	number of steps		–	63	–	
EW TRAPEZIUM CORRECTION						
	EW trapezium/width ratio	note 9	−1.5	–	+1.5	%
	number of steps		–	7	–	
EHT input (pin 7)						
V_{ref}	reference voltage	BLDS = logic 1	–	3.9	–	V
		BLDS = logic 0	–	V_{CC}	–	V
V_I	input voltage w.r.t V_{ref}	BLDS = logic 1	−20	0	+20	%
V_I	input voltage w.r.t V_{CC}	BLDS = logic 0	0	–	$-2V_{ref}$	V
m_{scan}	scan modulation		−10	0	+9.7	%
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
I_I	input current		−100	–	+100	nA
R_{CONV} input (pin 8)						
V_O	output voltage	I_8 = −120 µA	3.7	3.9	4.1	V
I_8	current range		−100	−120	−150	µA
PROT input (pin 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.7	3.9	4.1	V
I_I	input current		−10	–	+10	µA
FLASH detection input (pin 9)						
V_I	input voltage		0	–	V_{CC}	V
V_9	voltage detection level	falling edge	0.5	0.75	1.0	V
H	detection level hysteresis		0.3	0.5	0.8	V
I_9	detection pull-up current		−4	−8	−16	µA

Notes to the characteristics

1. For all other frequencies the expected supply current will be as shown in Table 6 (f_{clk} is the internal clock frequency, f_{LLC} is the internal clock frequency applied to pin 14).
2. When the prescaler is on, one in two LLC HIGH periods is omitted.
3. For 16 kHz operation the minimum value of the control range is 5.7 µs. With $\frac{1}{2}t_{FB} = 5.7$ µs the minimum storage time is 0 and the maximum is 18 µs.

   For 32 kHz operation the minimum value of the control range is 0 µs. With $\frac{1}{2}t_{FB} = 2.85$ µs the minimum storage time is 0 and the maximum is 9 µs.
4. The k factor is defined as the amount of correction of a phase step. Thus with k = 0.5 a 50% correction of the error takes place each line. The resulting step response now becomes k^n, with n the line number after the step.
5. The sigma value (σ) of the jitter with respect to LLC at $f_H = 32$ kHz and a storage time of 5 µs.

   Measurement of σ is carried out during 200 lines in the active scan, the resulting peak-to-peak value is approximately 6σ. The visible jitter on the screen will be higher than the peak-to-peak jitter, depending on the deflection stage.
6. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.
7. Value is a percentage of $I_{10} - I_{11}$.
8. The linearity error is measured without S-correction and based on the same measurement principle as used for the screen. Measuring method: divide the output signal $I_{10} - I_{11}$ into 22 equal parts, ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused.

   Linearity error for adjacent blocks = $\frac{a_k - a_{(k+1)}}{a_{avg}}$

   Linearity error for non-adjacent blocks = $\frac{a_{max} - a_{min}}{a_{avg}}$

   Where a = amplitude, a_k = amplitude block k and a_{avg} = average amplitude.
9. Minimum available range.
10. Selection of test mode.

    When the EW output is pulled above $V_{CC} - 0.5$ V a special test mode is entered in which the prescaler and the clock detector are disabled.
11. DAC values: vertical amplitude = 31; EHT = 0; WIDTH = 0.
12. The value of –40% (typically 46%) corresponds with data 3F (hexadecimal) and implies maximum 4th order compensation.

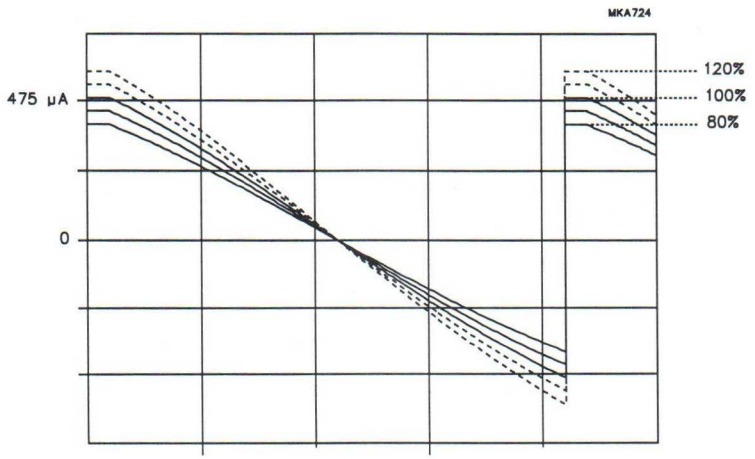
Table 6 Supply current with prescaler on/off.

LLC (MHz)	ON (mA)	OFF (mA)
6.75	note 1	27
13.5	27	38
27	42	note 1

Note

1. Combination not allowed.

TEST AND APPLICATION INFORMATION



$I_{11} - I_{10}$.

Fig.15 Control range amplitude.

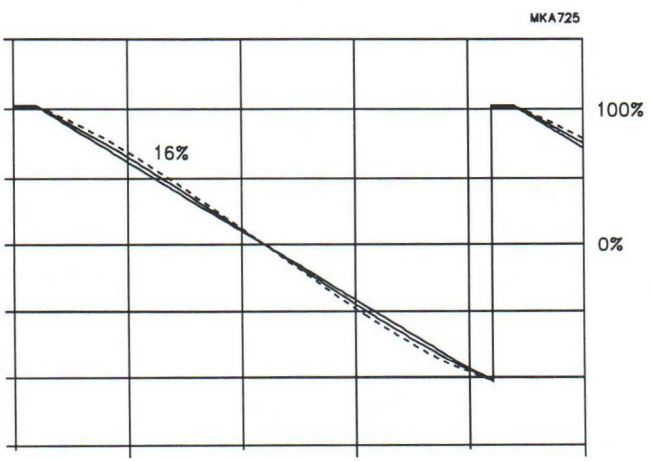


Fig.16 Control range S-correction.

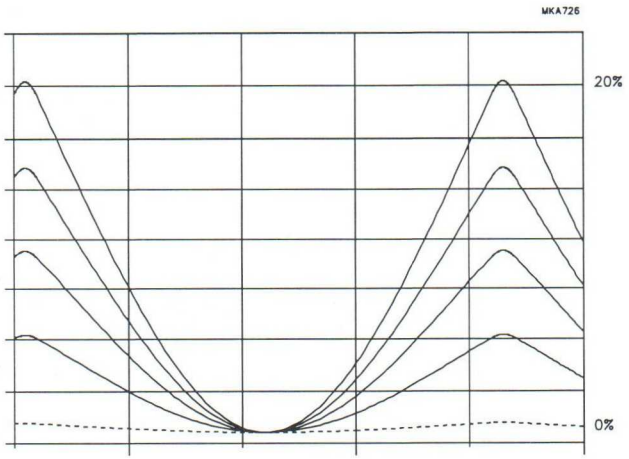


Fig.17 Control range EW parabola/width ratio.

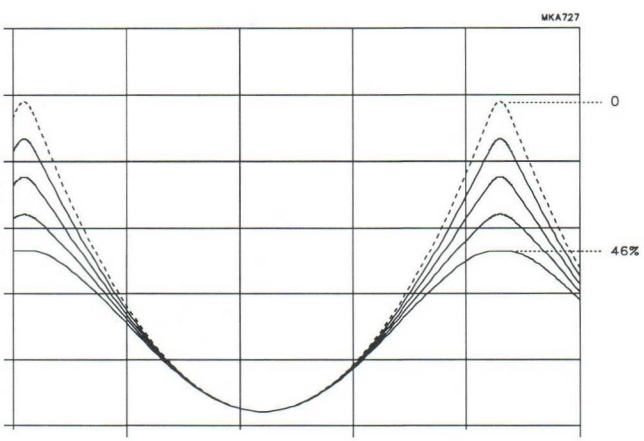


Fig.18 Control range EW corner/EW parabola ratio.

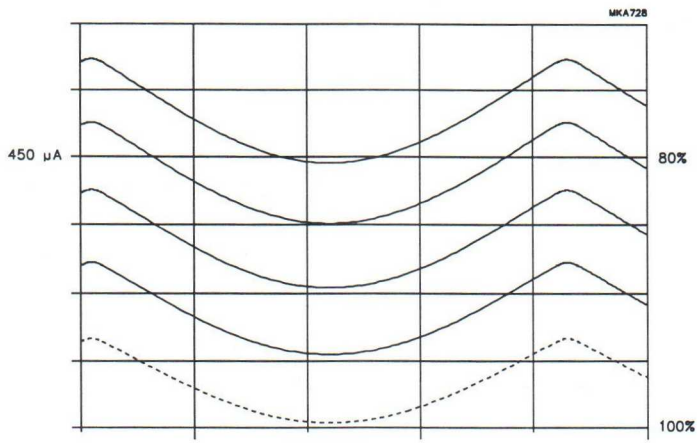


Fig.19 Control range EW width.

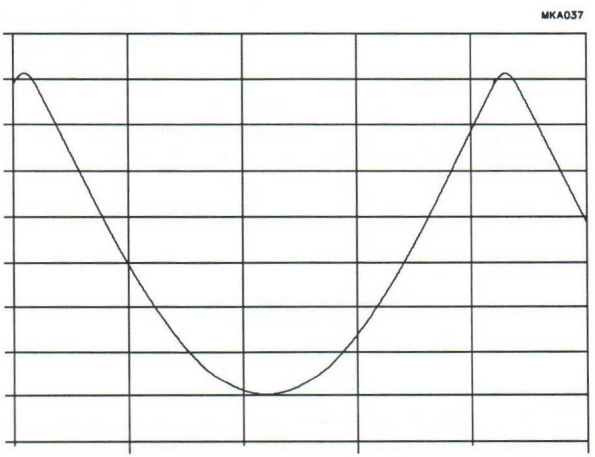


Fig.20 The BULT makes the EW waveform continuous.

Programmable deflection controller TDA9151B

FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Flash detection with restart
- Two-level sandcastle pulse.

Vertical deflection

- 16-bit precision vertical scan
- Self adaptive or programmable fixed slope mode
- DC coupled deflection to prevent picture bounce
- Programmable fixed compression to 75%
- Programmable vertical expansion in the fixed slope mode
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity
- Programmable de-interlace phase.

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity.

Horizontal deflection

- Phase 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Over voltage protection/detection with selection and status bit.

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter.

GENERAL DESCRIPTION

The TDA9151B is a programmable deflection controller contained in a 20-pin DIP package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9151B uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device can be programmed in a self-adaptive mode or in a programmable fixed slope mode. Selection of these modes and a large number of other functions is fully programmable via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9151B	20	DIP	plastic	SOT146-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
T_{amb}	operating ambient temperature		−25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	
V_{12}	vertical sync (V_A) logic level		–	TTL	–	
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	
V_{17}	serial data input (SDA) logic level		–	CMOS 5 V	–	
V_1	horizontal flyback (HFB) phase slicing level	FBL = logic 0	–	3.9	–	V
		FBL = logic 1	–	1.3	–	V
V_1	horizontal flyback (HFB) blanking slicing level		–	100	–	mV
V_3	over voltage protection (PROT) level		–	3.9	–	V
V_9	EHT flash detection level		–	1.5	–	V
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
$I_{11}-I_{10(M)}$	vertical differential ($VOUT_{A, B}$) output current (peak value)	vertical amplitude = 100%; I_8 = −120 µA; note 2	440	475	510	µA
$V_{10,11}$	vertical output voltage		0	–	3.9	V
$I_{6(M)}$	EW (EWOUT) total output current (peak value)	I_8 = −120 µA	–	–	930	µA
V_6	EW (EWOUT) output voltage		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_2	base voltage level		–	0.5	–	V
V_2	horizontal and vertical blanking voltage level		–	2.5	–	V
V_2	video clamping voltage level		–	4.5	–	V
HORIZONTAL OFF-CENTRE SHIFT (OFCS)						
V_{19}	output voltage	I_{19} = 2 mA	0	–	V_{CC}	V

Notes

1. Hard wired to ground or V_{CC} is highly recommended.
2. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.

BLOCK DIAGRAM

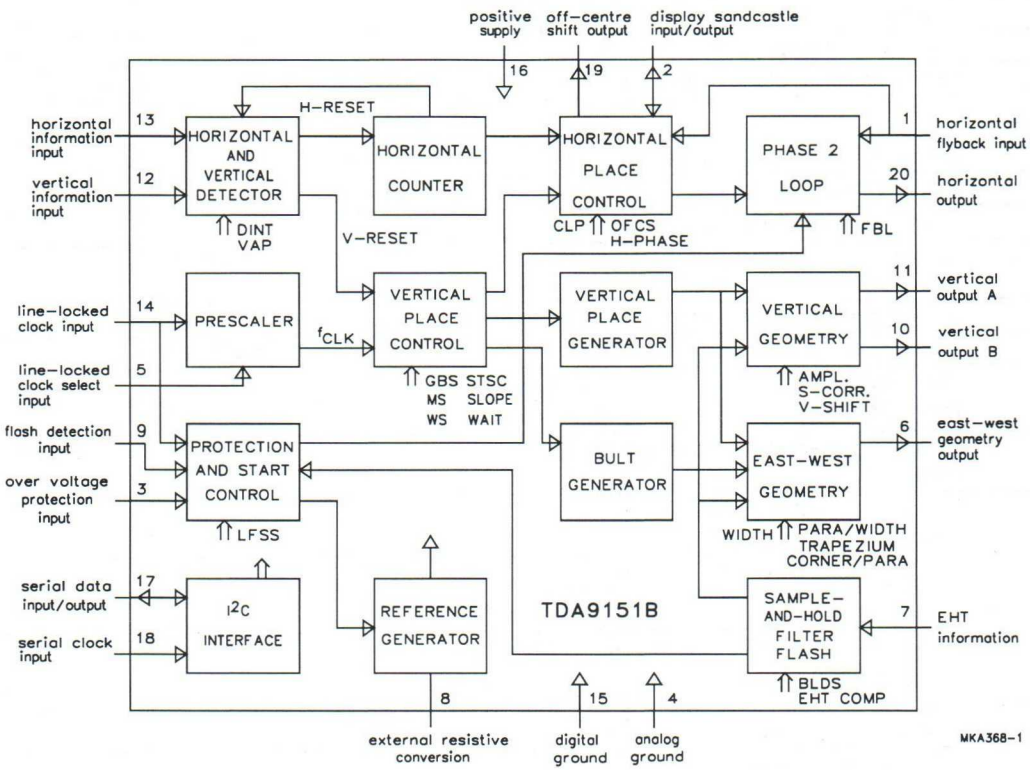


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over voltage protection input
AGND	4	analog ground
LLCS	5	line-locked clock selection input
EWOUT	6	east-west geometry output
EHT	7	EHT compensation
R_{CONV}	8	external resistive conversion
FLASH	9	flash detection input
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
DGND	15	digital ground
V_{CC}	16	supply input (+8 V)
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

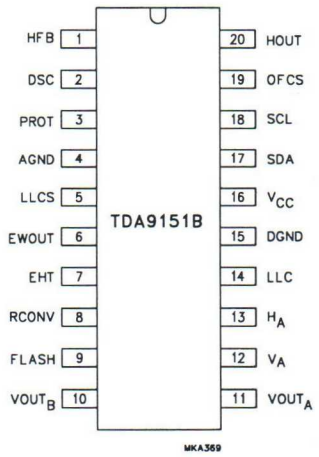


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9151B requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.

I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and/or V_A inputs for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs, the EW output current will drop to zero and the vertical output current will drop to 20% of the adjusted value within 100 µs). The SDA and SCL inputs meet the I²C-bus specification, the other three inputs are TTL compatible.

The LLC frequency can be divided-by-two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.

The LLC timing is given in the Chapter "Characteristics".

I²C-bus commands

Slave address: **8C HEX = 1000110X BIN**

READ MODE

The format of the status byte is: PON PROT 0 0 0 0 0 0

Where:

PON is the status bit for power-on reset (POR) and after power failure:

- Logic 1:
  - after the first POR and after power failure; also set to 1 after a severe voltage dip that may have disturbed the various settings
  - POR 1 to 0 transition, V_{CC} = 6.25 V (typ.)
  - POR 0 to 1 transition, V_{CC} = 5.75 V (typ.)
- Logic 0:
  - after a successful read of the status byte.

PROT is the over voltage detection for the scaled EHT input:

- Logic 1:
  - if the scaled EHT rises above the reference value of 3.9 V
- Logic 0:
  - after a successful read of the status byte and EHT <3.9 V.

Remark: a read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode with auto increment; subaddress and data byte format.

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Vertical amplitude	00	X[1]	X	A5	A4	A3	A2	A1	A0
Vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
Vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
Vertical off-centre shift	03	X	note 2	note 2	note 2	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	note 2	note 2	note 2
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
Horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
Horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
Clamp shift	0A	X	X	X	X	X	A2	A1	A0
Control 1	0B	MS	WS	FBL	VAP	BLDS	LFSS	DINT	GBS
Vertical slope MSB	0C	A7	A6	A5	A4	A3	A2	A1	A0
Vertical slope LSB	0D	A7	A6	A5	A4	A3	A2	A1	A0
Vertical wait	0E	A7	A6	A5	A4	A3	A2	A1	A0
Control 2	0F	X	X	X	VPR	CPR	DIP	PRD	CSU

Notes

1. X = don't care.
2. Data bit used in another function.

Table 2 Control bits.

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	Line stop: EW output current becomes zero and the vertical output current is reduced to 20% of the adjusted value. LFSS becomes logic 0 after a HIGH on PON.
	1	Line start enabled: the soft start mechanism is now activated.
DINT	0	De-interlace on: the V_A pulse is sampled at a position selected with control bit DIP.
	1	De-interlace off: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset.
BLDS	0	Aquadag selected.
	1	Bleeder selected.
GBS	0	Becomes logic 0 after power-on.
	1	Guard band 48/12 lines.
VAP	0	Positive V_A edge detection.
	1	Negative V_A edge detection.
FBL	0	Horizontal flyback slicing level = 3.9 V.
	1	Horizontal flyback slicing level = 1.3 V.
WS	0	No wait state.
	1	Programmable wait state (only in constant slope mode; MS = logic 1).
MS	0	Adaptive mode with guardband amplitude control.
	1	Constant slope mode (programmable).
CSU	0	No clamping suppression, standard mode of operation.
	1	Clamping suppression in wait, stop and protection modes (used in systems with e.g. TDA4680/81).
PRD	0	No defeat of HOUT, the over voltage information is only written in the PROT status bit.
	1	HOUT is defeated and status bit PROT is set when over voltage is detected.
DIP	0	V_A is sampled 42 clock pulses after the leading edge of H_A.
	1	V_A is sampled 258 clock pulses after the leading edge of H_A.
CPR	0	Nominal amplitude.
	1	Compression to 75% of adjusted amplitude, used for display of 16 : 9 standard pictures on 4 : 3 displays.
VPR	0	Nominal amplitude (100%) during wait, stop and clipping.
	1	Amplitude reduced to 20% during wait, stop and clipping.

Table 3 Explanation of control bits shown in Table 2.

CONTROL BITS	DESCRIPTION
LFSS	line frame start/stop
DINT	de-interlace
BLDS	bleeder mode selection
GBS	guard band selection
VAP	polarity of V_A edge detection
FBL	flyback slicing level
WS	wait state on/off
MS	mode select
CSU	clamping suppression mode
PRD	protection/detection mode
DIP	de-interlace phase
CPR	compression on/off
VPR	vertical power reduction mode

Table 4 Clock frequency control bit (pin 5; note 1).

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler on: the internal clock frequency $f_{clk} = \frac{1}{2}f_{LLC}$
	1	prescaler off (default by internal pull-up resistor): the internal clock frequency $f_{clk} = f_{LLC}$

Note

1. Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to ground or V_{CC}. Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and large flyback pulses. The permitted combinations of LLC and the prescaler are shown in Table 5.

Table 5 Line duration with prescaler.

LLC (MHz)	ON (µs)	OFF (µs)
6.75	note 1	64
13.5	64	32
27	32	note 1

Note

1. Combination not allowed.

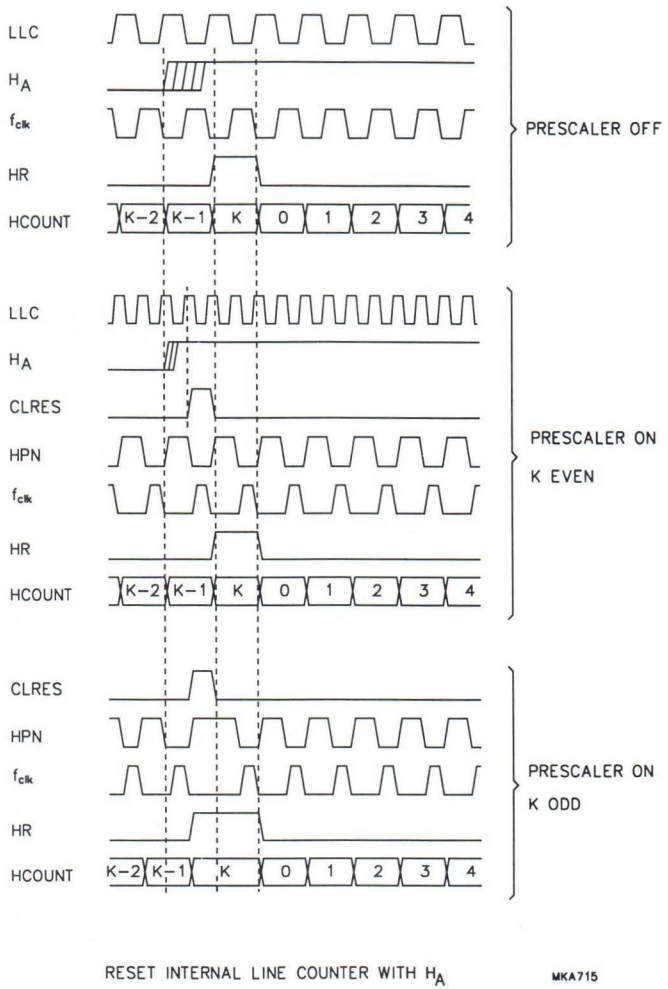


Fig.3 Timing relations between LLC, H_A and line counter.

Horizontal part (pins 1, 2, 13, 19 and 20

Synchronization pulse

The H_A input (pin 13) is a TTL-compatible CMOS input. Pulses on this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW periods is 2 internal clock periods.

Flyback input pulse

The HFB input (pin 1) is a CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08), as illustrated in Fig.7.
The resolution is 6-bit.

Output pulse

The HOUT pulse (pin 20) is an open-drain NMOS output. The duty factor for this output is typically $^{52}/_{48}$ (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 5 to 52% over a minimum period of 2000 lines in 2000 steps.

Off-centre shift

The OFCS output (pin 19) is a push-pull CMOS output which is driven by a pulse-width modulated DAC.

By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 × 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.8.

Sandcastle

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamping. As an input it acts as a current sensor during the vertical blanking interval for guard detection.

Clamping pulse

The clamping pulse width is 21 internal clock periods. The shift, with respect to H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.9. It is possible to suppress the clamping pulse during wait, stop and protection modes with control bit CSU. This will avoid unwanted reset of the TDA4680/81 (only used in those circuits).

Horizontal blanking

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{clk}/f_H ratio K in accordance with 41 – (432 – K).

Stop of the horizontal blanking pulse is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level crossing as illustrated in Fig.10.

Vertical blanking

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Section "Vertical guard").

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02 (see Figs 11, 12 and 13).

Vertical guard

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 800 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in the event of missing or malfunctioning vertical deflection (see Figs 11, 12 and 13).

Vertical part (pins 6, 8, 10, 11 and 12)

SYNCHRONIZATION PULSE

The V_A input (pin 12) is a TTL-compatible CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods. For further requirements on minimum pulse width see also Section "De-interlace".

VERTICAL PLACE GENERATOR

An overview of the various modes of operation of the vertical place generator is illustrated in Fig.13.

With control bit CPR a compress to 75% of the adjusted values is possible in all modes of operation. This control bit is used to display 16 : 9 standard pictures on 4 : 3 displays. No new adjustment of other corrections, such as corner and S-correction, is required.

With control bit VPR a reduction of the current during clipping, wait and stop modes to 20% of the nominal value can be selected, which will reduce the dissipation in the vertical drive circuits.

Vertical place generator in adaptive mode (MS = logic 0)

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 × 432 clock periods in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.

The minimum number of synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15 625 or 31250 Hz respectively.

If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.

Amplitude control is automatic, with a settling time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit.

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

Vertical place generator in constant slope mode (MS = logic 1)

In this mode the slope can be programmed directly with a two byte value on subaddress 0C (MSB) and 0D (LSB). When the actual number of lines is greater than the programmed number of lines, the circuit will enter the stop state in which the differential vertical output current remains 100% or drops to 20% (programmable with control bit VPR). The programmed value for the slope is the required number of lines multiplied by 72. The programming limits are; minimum 200 × 72 and maximum 910 × 72.

A vertical expansion is obtained with a combination of slope data and a programmable wait status, at subaddress 0E. The wait status is selected with control bit MS and can only be activated in the constant slope mode. The wait state is an 8-bit value, programmable from 0 to 255. The actual wait state is one line longer than the programmed value. If blanking is applied during stop and wait status the differential output current will be the same with VPR selected value (20 or 100%).

DE-INTERLACE

With de-interlace on (DINT = logic 0), the V_A pulse is sampled with LLC at a position supplied by control bit DIP (de-interlace phase).

When DIP = logic 0 sampling takes place 42 clock pulses after the leading edge of H_A ($T = T_{line} \times 42/432$).

When DIP = logic 1 sampling takes place 258 clock pulses after the leading edge of H_A ($T = T_{line} \times 258/432$).

The distance between the two selectable sampling points is ($T_{line} \times (258 - 42)/432$) which is exactly half a line, thus de-interlace is possible in two directions.

The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to caught, in this event an active time of minimum of half a line (see Fig.14 which has an integration time of $T_{line} \times 1/4$ for the V_A pulse).

With de-interlace off, the V_A pulse is sampled with the system clock. The leading edge is detected and used as the vertical reset. Selection of the positive or negative leading edge is achieved by the control bit VAP.

VERTICAL GEOMETRY PROCESSING

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The external resistive conversion (R_{CONV}) at pin 8 sets the reference current for both the vertical and EW geometry processing. A useful range is 100 to 150 μA, the recommended value is 120 μA.

VERTICAL OUTPUTS

The vertical outputs $VOUT_A$ and $VOUT_B$ on pins 10 and 11 together form a differential current output. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with a 6-bit resolution.

The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is −1.5 to +1.5% ($\pm 1/8 \times I_8$) in 7 steps set by the least significant nibble at subaddress 03.

EW GEOMETRY PROCESSING

The EW geometry processing is DC coupled and therefore independent of field frequency. R_{CONV} sets the reference current for both the vertical and EW geometry processing.

The EW output is an ESD-protected single-ended current output.

The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of −40 to 0% in 63 steps via subaddress 06.

The EW trapezium correction can be set from −1.5 to +1.5% in 7 steps via the most significant nibble at subaddress 03.

BULT GENERATOR

The Bult generator makes the EW waveform continuous (see Fig.21).

Protection input (pin 3)

The protection input (PROT) is a CMOS input.

The input voltage must be EHT scaled and has the following characteristics:

Two modes of protection are available with the aid of control bit PRD.

- With PRD = logic 1 the protection mode is selected, HOUT will be defeated and the PROT bit in the status word is set if the input voltage is above 3.9 V. Thus the deflection stops and EW output current is zero, while the vertical output current is reduced to 20% of the adjusted value. A new start of the circuit is I²C-bus controlled with the user software.
- With PRD = logic 0 the detection mode is selected, HOUT will not be defeated and the over voltage information is only written in the PROT status bit and can be read by the I²C-bus.

All further actions, such as a write of the LFSS bit, are achieved by the I²C-bus. They depend on the configuration used and are defined by user software.

Flash detection/protection input (pin 9)

The FLASH input is a CMOS input with an internal pull-up current of approximately 8 μA.

When a negative-going edge crosses the 0.75 V level a restart will be executed with a soft start of approximately 2000 lines, such as in the soft-start mode. When the function is not used pin 9 can be connected to ground, V_{CC} or left open-circuit, the internal pull-up current source will prevent any problems. However a hard wired connection to V_{CC} or ground is recommended when the function is not used.

EHT compensation (pin 7)

The EHT input is a CMOS input.

The EHT compensation input permits scan amplitude modulation should the EHT supply not be perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, provided by the ratio $R_{CONV\text{-}EW}/R_{CONV}$, must be $1/16 V_{scan} \times V_{ref}$ (see Fig.15).

The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS).

EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from −10 to +9.7%.

INTERNAL CIRCUITRY

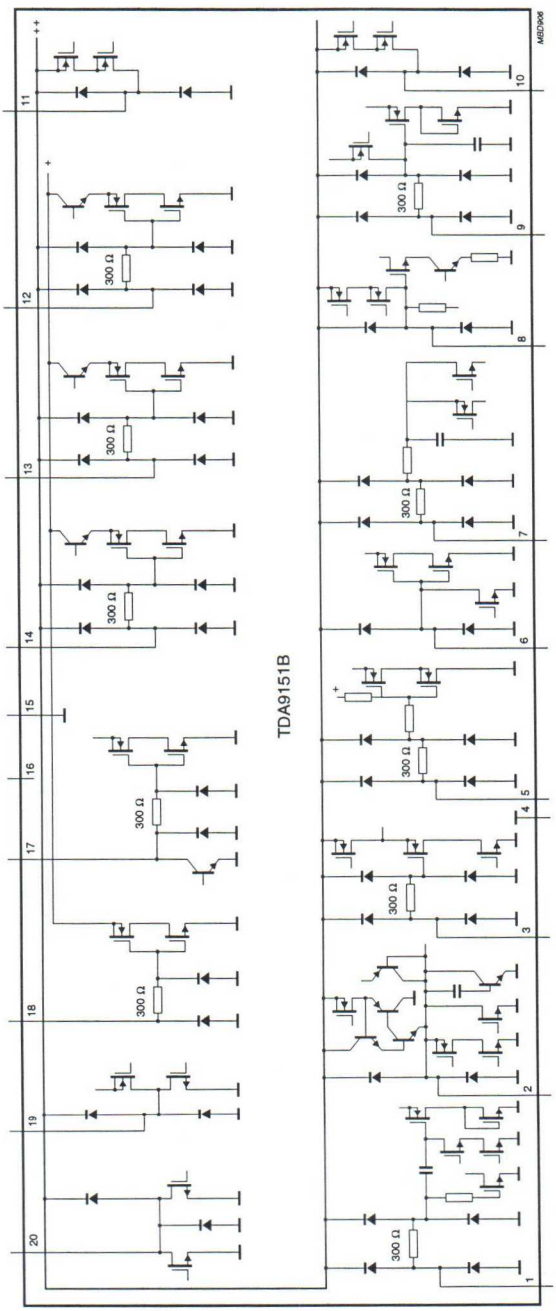


Fig.4 Internal circuitry.

APPLICATION INFORMATION

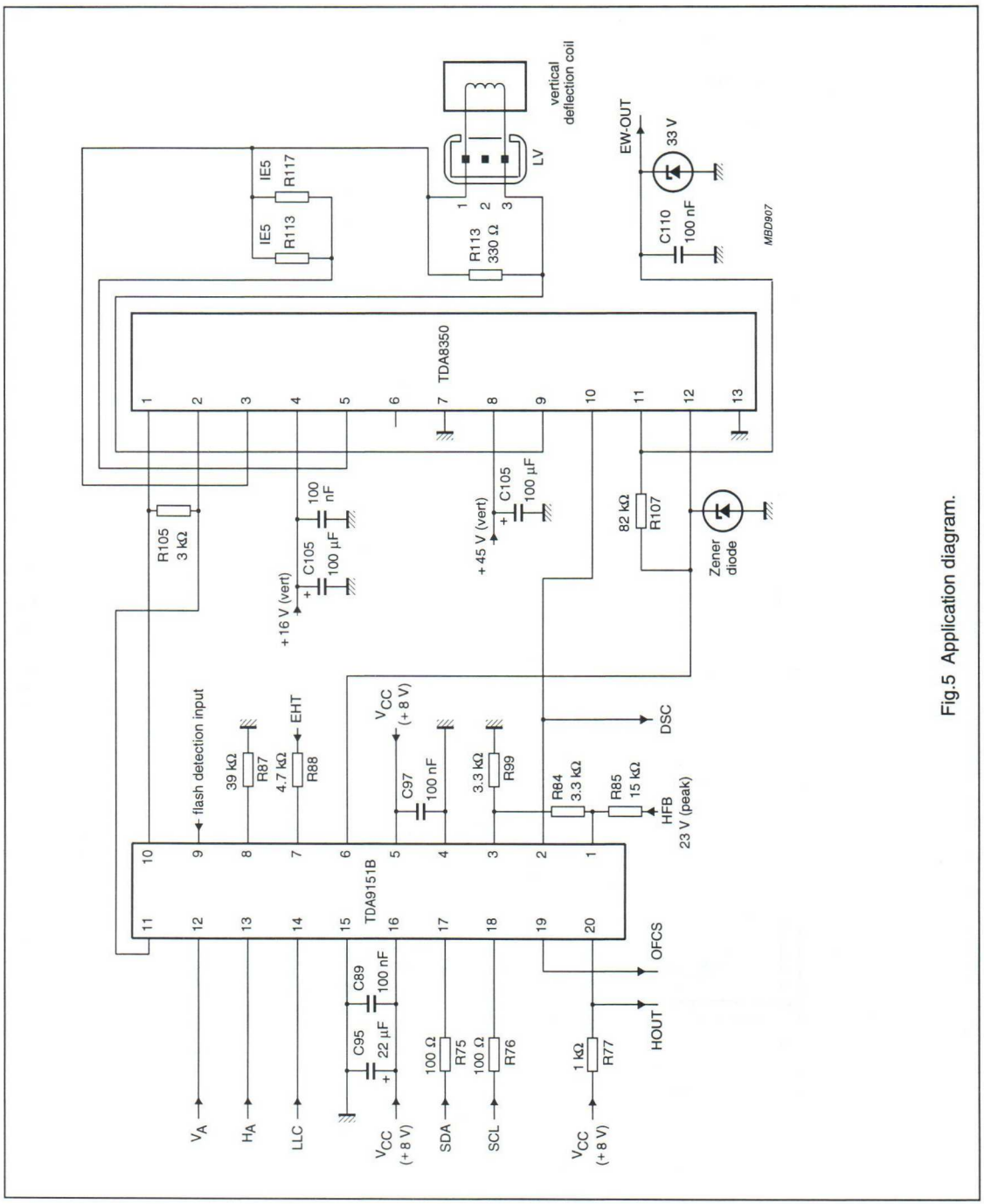


Fig.5 Application diagram.

TIMING DIAGRAMS

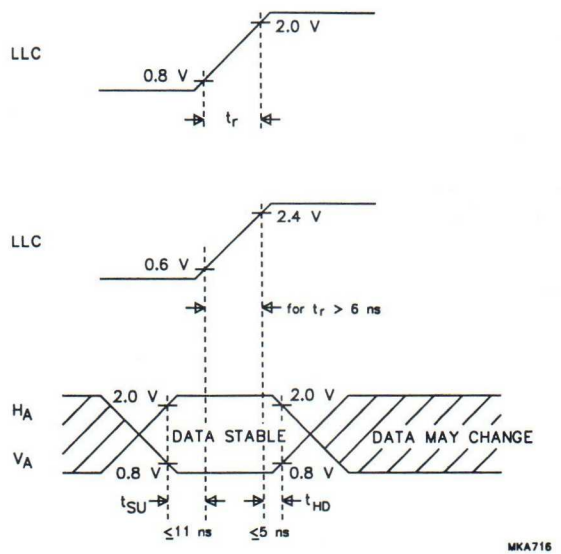


Fig.6 Timing requirements for LLC, H_A and V_A.

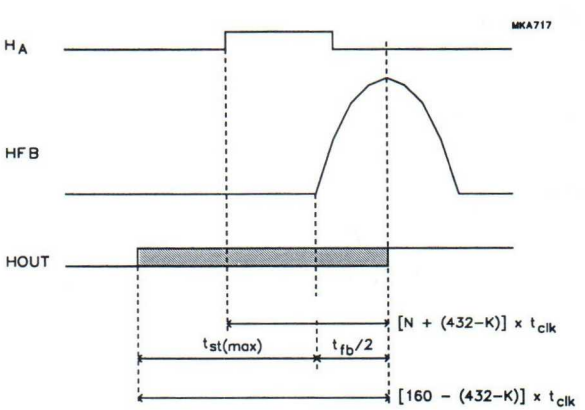


Fig.7 Horizontal phase and HOUT control range.

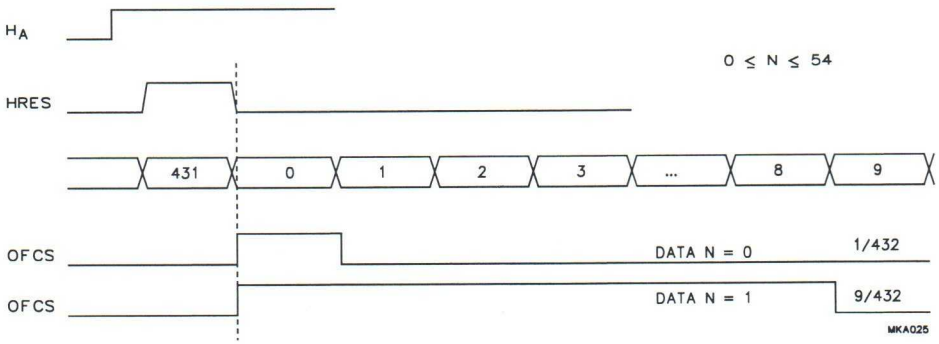


Fig.8 OFCS duty factor.

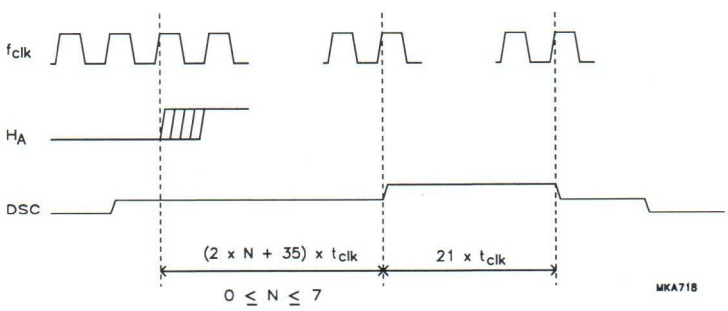


Fig.9 DSC clamping pulse.

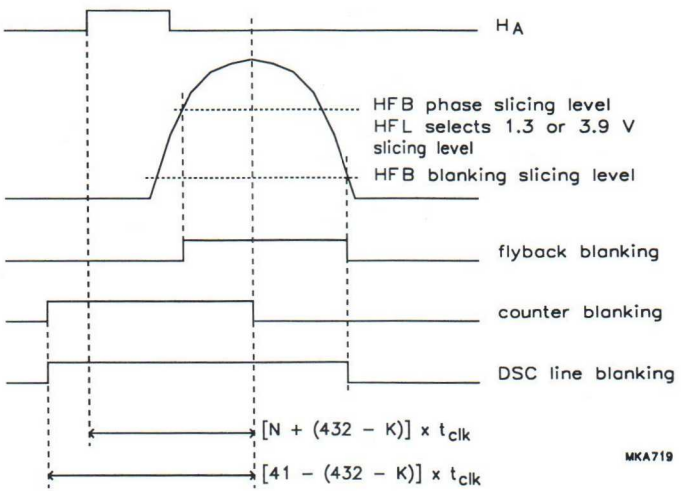


Fig.10 DSC line blanking.

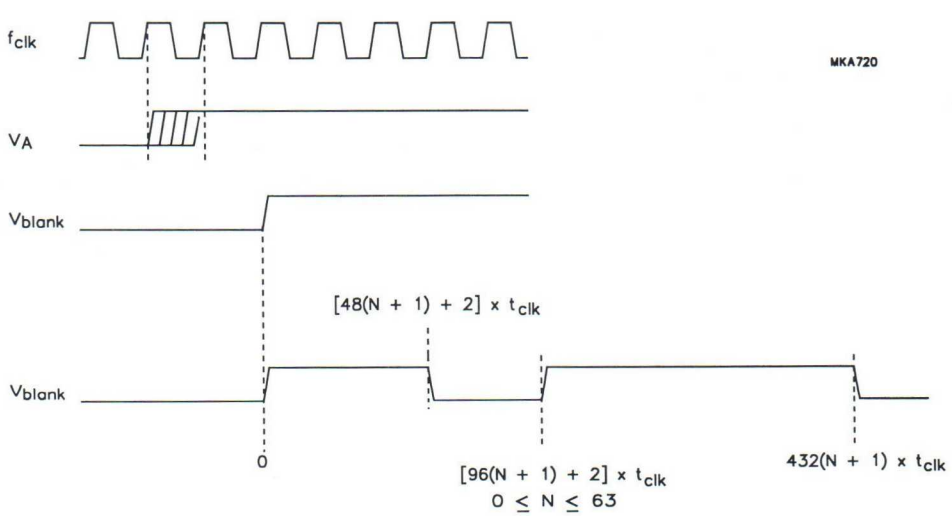
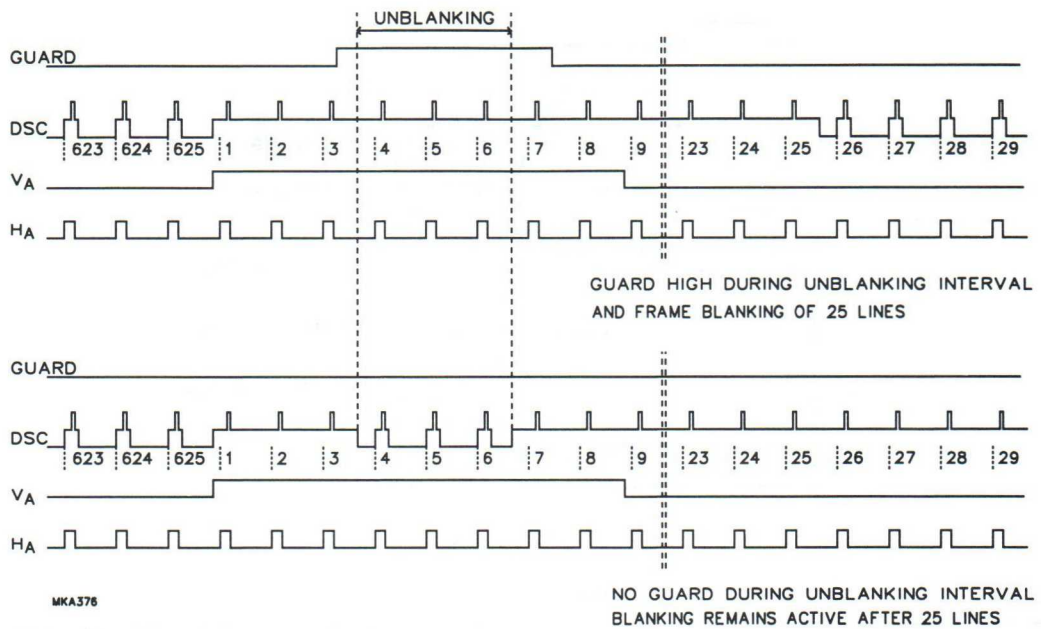


Fig.11 DCS vertical blanking with unblanking.



Vertical blanking LOW period: during scan, during unblanking.
Vertical blanking HIGH period (2.5 V): during STSC, stop and wait.
Vertical blanking continuously HIGH: POR = logic 1, LFSS = logic 0, no guard detected.

Fig.12 DSC with guard interval; start scan = 24.

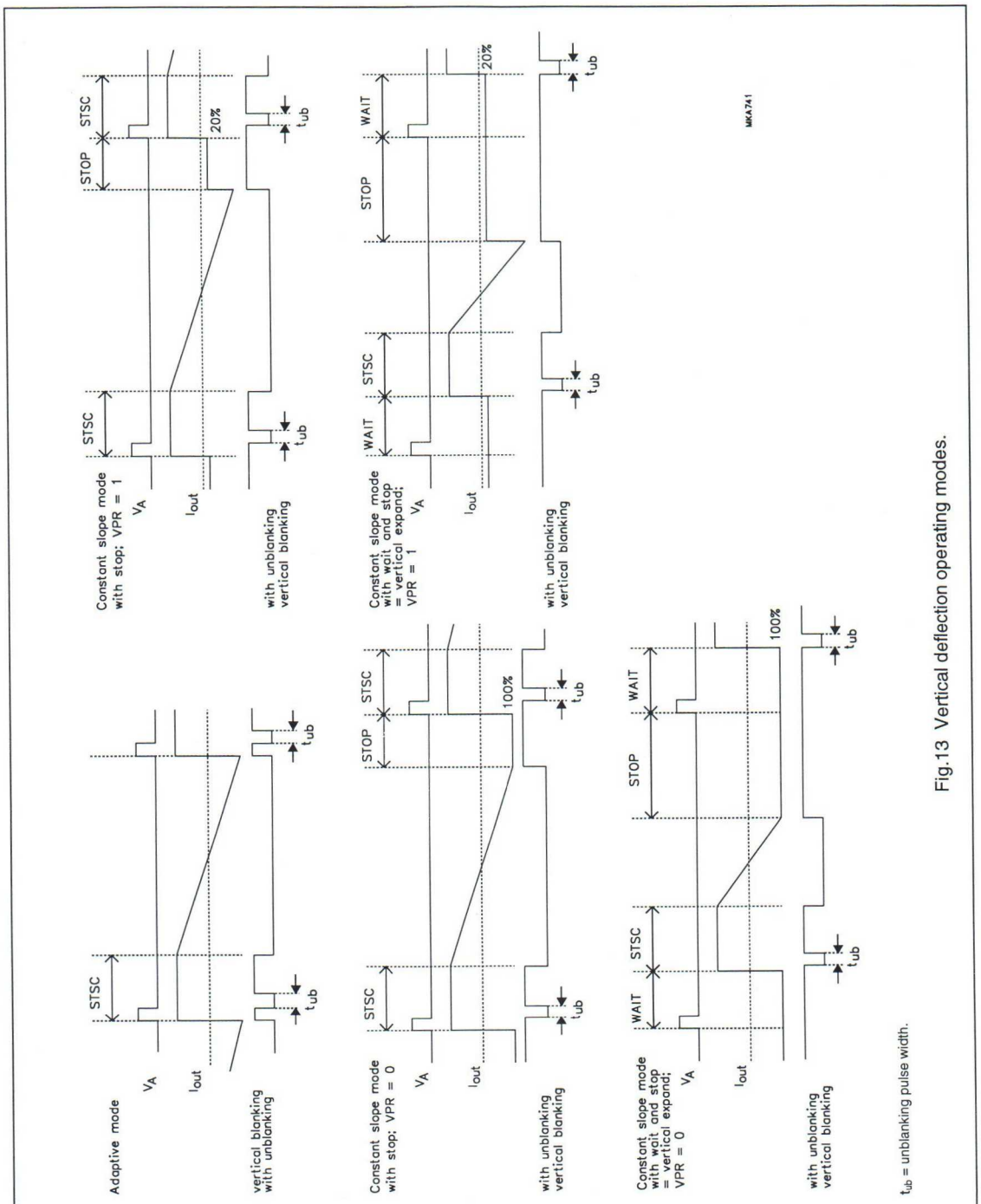
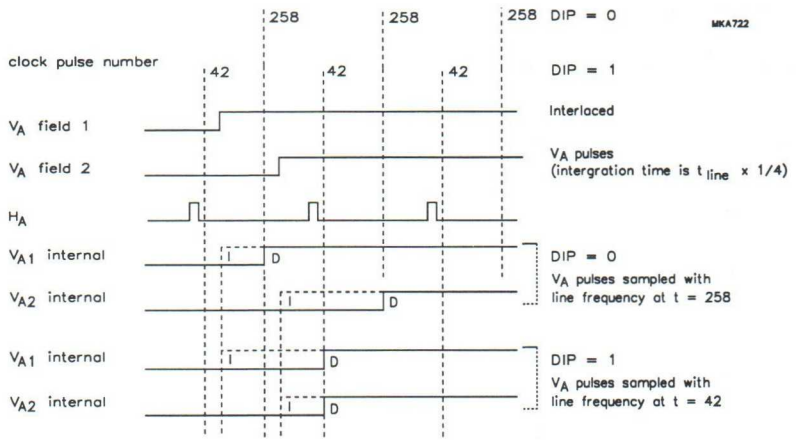


Fig.13 Vertical deflection operating modes.



I = start V_A for DINT = logic 1.
D = start V_A for DINT = logic 0.

Fig.14 De-interlace timing.

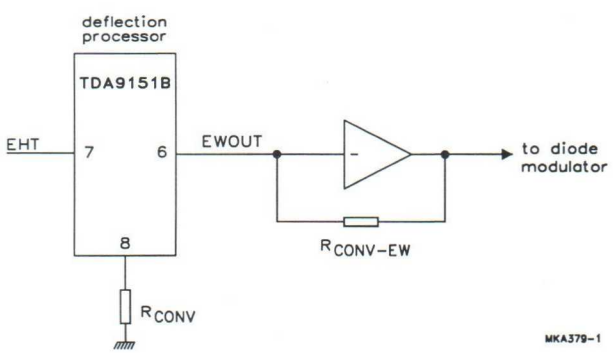


Fig.15 Explanation of $R_{CONV-EW}/R_{CONV}$ ratio.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	8.8	V
I_{CC}	supply current	−10	+50	mA
P_{tot}	total power dissipation	−	500	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 14 and 17 to 20	−0.5	V_{CC} + 0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16	−20	+20	mA
V_{ESD}	electrostatic handling for all pins (note 1)	−	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; DGND = AGND = 0 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
V_{por}	power-on reset	POR 1-to-0 transition	–	6.25	7.0	V
		POR 0-to-1 transition	5.0	5.75	–	V
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 17)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	–	–	V
I_{IL}	LOW level input current (pin 17)	$V_{17} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 17)	$V_{17} = V_{CC}$	–	–	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	–	–	0.4	V
V_{18}	SCL input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 18)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	–	–	V
I_{IL}	LOW level input current (pin 18)	$V_{18} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 18)	$V_{18} = V_{CC}$	–	–	10	µA
Line-locked clock and line-locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		–	–	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	–	–	V
I_{14}	input current	V_{14} = <5.5 V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	
δ_0	duty factor	LLCS = logic 0; at 1.4 V; note 2	40	50	60	%
δ_1	duty factor	LLCS = logic 1; at 1.4 V; note 2	25	50	75	%
TIMING (PRESCALER ON; $f_{clk} = \frac{1}{2}f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	856	864	865	
		H unlocked	–	866	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432.5	
		H unlocked	–	433	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TIMING (PRESCALER OFF; $f_{clk} = f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		6.2	–	15.5	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SSD}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{13}	input current	$V_{13} = 5.5$ V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
HFB (pin 1)						
V_{PSL}	phase slicing level;	FBL = logic 0	3.7	3.9	4.1	V
		FBL = logic 1	1.1	1.3	1.5	V
V_{blank}	blanking slicing level		0	0.1	0.2	V
I_1	input current		–10	–	+10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	$N \times t_{clk}$	$N + (432 - K) \times t_{clk}$	
	number of steps		–	63	–	
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	$I_{20} = 0$	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{20} = 10$ mA	–	–	0.5	V
I_{20}	input current	output off	–10	–	+10	µA
δ	duty factor	normal operation	51	52	53	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	5	%
CR	control range		5	–	53	%
t_{ss}	soft start time		1500	–	3000	lines
Switch-off time to the centre of the flyback pulse						
CR	control range	note 3	0	–	160 – (432 – K) × t_{clk}	
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
k	correction factor	note 4	–	0.5	–	
σ	sigma value of phase jitter	note 5	–	750	–	ps
PSRR	power supply rejection ratio		–	–	10	ns/V
Horizontal off-centre shift (pin 19; N = off-centre shift data)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{19} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{19} = –2 mA	V_{CC} – 0.5	–	–	V
$\delta_{(max)}$	maximum duty factor	N <54	1/K	(8N+1)/K	425/K	%
δ	duty factor	N ≥54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamping voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking voltage level		2.0	2.5	3.0	V
V_{base}	base voltage level		0	0.5	1.0	V
I_2	output current	guard not detected	–1.0	–	+0.35	mA
		guard detected	0.8	–	2.5	mA
t_r	rise time		–	60	–	ns
t_f	fall time		–	60	–	ns
Clamping pulse (N = clamp pulse shift data)						
t_W	clamping pulse width		–	21 × t_{clk}	–	
t_{clamp}	clamp pulse shift w.r.t H_A		35	(2N + 35) × t_{clk}	49	
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41 – (432 – K) × t_{clk}	41	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start-scan data)						
t_{start}	start interval w.r.t V_A	no wait	$\{48(N+1) +2\} \times t_{clk}$	–	–	
t_{stop}	stop interval w.r.t V_A	no wait	$\{96(N+1) +2\} \times t_{clk}$	–	–	
Vertical section						
INPUT SIGNALS (PIN 12; V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} <5.5 V	−10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
t_{WH}	pulse width HIGH	de-interlace mode	$0.5 \times t_{line}$	–	–	
t_{WL}	pulse width LOW	de-interlace mode	$0.5 \times t_{line}$	–	–	
Vertical place generator in adaptive mode (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
L_{max}	maximum number of synchronized lines per scan		–	910	–	lines/ scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
L_{min}	minimum number of synchronized lines per scan		–	200	–	lines/ scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = logic 0	–	16/12	–	lines
		GBS = logic 1	–	48/12	–	lines
	settling time		1	1.5	2	new fields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical place generator in constant slope mode (N = vertical wait data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	255	–	
	programmable slope		200	–	910	lines/scan
	programmable slope data (number of lines × 72)	2-byte instruction;	200 × 72	–	910 × 72	lines
Vertical geometry processing						
$\Delta I_{(M)}$	vertical differential output current between $VOUT_A$ and $VOUT_B$ (peak value)	V_A = 100%; note 6; I_8 = −120 µA	440	475	510	µA
D/ΔT	drift over temperature range		–	–	10^{-4}	K^{-1}
	amplitude error due to S-correction setting		–	–	2	%
$\frac{1}{2}(I_{10}+I_{11})$	vertical output signal bias current	I_8 = −120 µA	275	325	375	µA
I_{os}	vertical output offset current	note 7	–	–	1	%
OS/ΔT	offset over temperature range		–	–	10^{-4}	K^{-1}
V_{10}	vertical output voltage (pin 10)		0	–	3.9	V
V_{11}	vertical output voltage (pin 11)		0	–	3.9	V
CMRR	common mode rejection ratio		–	–	1	%/V
LE	linearity error	adjacent blocks; note 8	–	–	2.0	%
		non-adjacent blocks; note 8	–	–	3.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range	note 9	81	–	119	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range	note 9	0	–	15	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		$-\frac{1}{8}I_8$	–	$+\frac{1}{8}I_8$	µA
	number of steps		–	7	–	
EW output (pin 6)						
V_6	output voltage	note 10	1.0	–	5.5	V
I_6	output current	I_8 = −120 µA; note 11	15	–	930	µA
RR	output ripple rejection		–	0.15	1	%/V
D/ΔT	output drift over temperature range		–	–	5.10^{-4}	K^{-1}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW WIDTH/WIDTH RATIO						
CR	control range	note 9	100	–	81	%
$I_{eq(typ)}$	typical equivalent output current	V_6 = 3 V	15	–	440	µA
	number of steps		–	63	–	
EW PARABOLA/WIDTH RATIO						
CR	control range	note 9	1	–	19	%
$I_{eq(typ)}$	typical equivalent output current	width = 100%	10	–	430	µA
		width = 80%	10	–	345	µA
	number of steps		–	63	–	
EW CORNER/EW PARABOLA RATIO						
CR	control range	notes 9 and 12	40	–	0	%
$I_{eq(typ)}$	typical equivalent output current	width = 100%	0	–	200	µA
		width = 80%	0	–	160	µA
	number of steps		–	63	–	
EW TRAPEZIUM CORRECTION						
	EW trapezium/width ratio	note 9	–1.5	–	+1.5	%
	number of steps		–	7	–	
EHT input (pin 7)						
V_{ref}	reference voltage	BLDS = logic 1	–	3.9	–	V
		BLDS = logic 0	–	V_{CC}	–	V
V_I	input voltage w.r.t V_{ref}	BLDS = logic 1	–20	0	+20	%
V_I	input voltage w.r.t V_{CC}	BLDS = logic 0	0	–	$-2V_{ref}$	V
m_{scan}	scan modulation		–10	0	+9.7	%
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
I_I	input current		–100	–	+100	nA
R_{CONV} input (pin 8)						
V_O	output voltage	I_8 = –120 µA	3.7	3.9	4.1	V
I_8	current range		–100	–120	–150	µA
PROT input (pin 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.7	3.9	4.1	V
I_I	input current		–10	–	+10	µA
FLASH detection input (pin 9)						
V_I	input voltage		0	–	V_{CC}	V
V_9	voltage detection level	falling edge	0.5	0.75	1.0	V
H	detection level hysteresis		0.3	0.5	0.8	V
I_9	detection pull-up current		–4	–8	–16	µA

Notes to the characteristics

1. For all other frequencies the expected supply current will be as shown in Table 6 (f_{clk} is the internal clock frequency, f_{LLC} is the internal clock frequency applied to pin 14).
2. When the prescaler is on, one in two LLC HIGH periods is omitted.
3. For 16 kHz operation the minimum value of the control range is 5.7 µs. With $\frac{1}{2}t_{FB}$ = 5.7 µs the minimum storage time is 0 and the maximum is 18 µs.

   For 32 kHz operation the minimum value of the control range is 0 µs. With $\frac{1}{2}t_{FB}$ = 2.85 µs the minimum storage time is 0 and the maximum is 9 µs.
4. The k factor is defined as the amount of correction of a phase step. Thus with k = 0.5 a 50% correction of the error takes place each line. The resulting step response now becomes k^n, with n the line number after the step.
5. The sigma value (σ) of the jitter with respect to LLC (H_A) at f_H = 32 kHz and a storage time of 5 µs.

   Measurement of σ is carried out during 200 lines in the active scan, the resulting peak-to-peak value is approximately 6σ. The visible jitter on the screen will be higher than the peak-to-peak jitter, depending on the deflection stage.
6. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.
7. Value is a percentage of $I_{10} - I_{11}$.
8. The linearity error is measured without S-correction and based on the same measurement principle as used for the screen. Measuring method: divide the output signal $I_{10} - I_{11}$ into 22 equal parts, ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused.

   Linearity error for adjacent blocks = $\frac{a_k - a_{(k+1)}}{a_{avg}}$

   Linearity error for non-adjacent blocks = $\frac{a_{max} - a_{min}}{a_{avg}}$

   Where a = amplitude, a_k = amplitude block k and a_{avg} = average amplitude.
9. Minimum available range.
10. Selection of test mode.

    When the EW output is pulled above V_{CC} – 0.5 V a special test mode is entered in which the prescaler and the clock detector are disabled.
11. DAC values: vertical amplitude = 31; EHT = 0.
12. The value of –40% (typically 46%) corresponds with data 3F (hexadecimal) and implies maximum 4th order compensation.

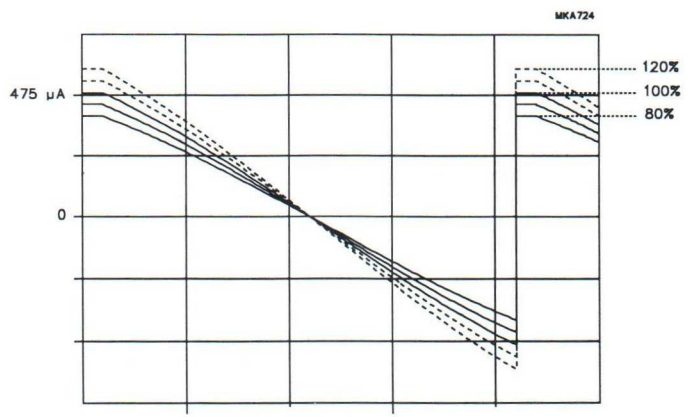
Table 6 Supply current with prescaler on/off.

LLC (MHz)	ON (mA)	OFF (mA)
6.75	note 1	27
13.5	27	38
27	42	note 1

Note

1. Combination not allowed.

TEST AND APPLICATION INFORMATION



$I_{11} - I_{10}$.

Fig.16 Control range amplitude.

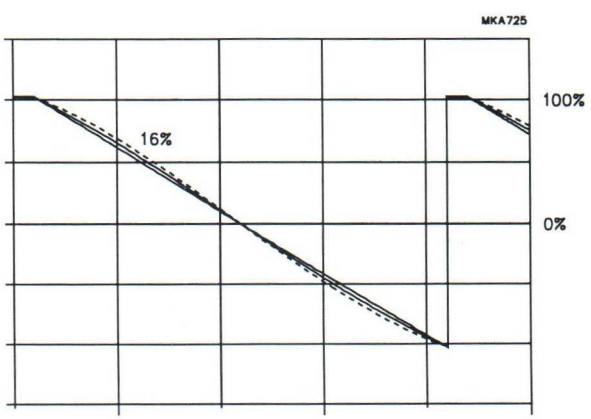


Fig.17 Control range S-correction.

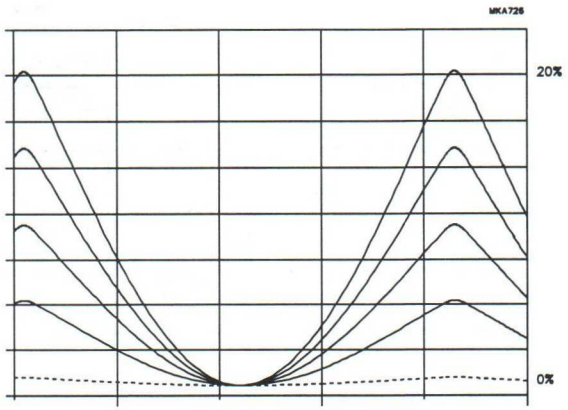


Fig.18 Control range EW parabola/width ratio.

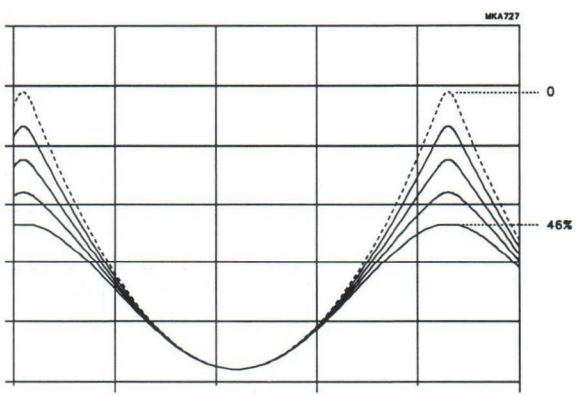


Fig.19 Control range EW corner/EW parabola ratio.

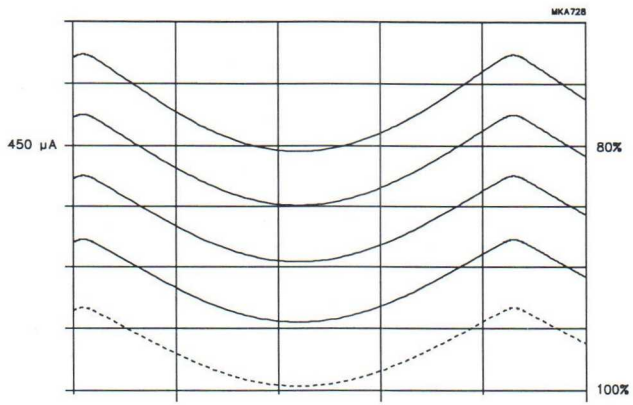


Fig.20 Control range EW width.

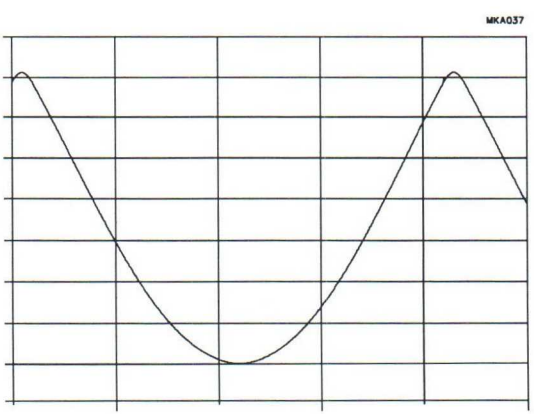


Fig.21 The BULT makes the EW waveform continuous.

PAL/NTSC/SECAM decoder/sync processor

TDA9160

FEATURES

- Multistandard PAL, NTSC and SECAM
- I²C-bus controlled
- I²C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Horizontal and vertical drive output
- East-West correction drive output
- Two CVBS inputs
- S-VHS input
- Vertical divider system
- H_A synchronization pulse
- Two level sandcastle pulse

GENERAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/processor. The device contains horizontal and vertical drive outputs and an east-west correction drive circuit. The TDA9160 has been designed for use with baseband chrominance delay lines and DC-coupled vertical and east-west output circuits.

The device has three inputs, two for CVBS and one for S-VHS. The main signal is available at the luminance and colour difference outputs and, also, at the TXT output (unprocessed). The signal at the PIP output can be selected independently from the main signal. The circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an east-west drive current for the EW output stage. These signals can be used to provide geometry correction of the picture. A two level sandcastle pulse and an H_A pulse are made available for synchronization purposes.

The I²C-bus address of the TDA9160 can be programmed by hardware.

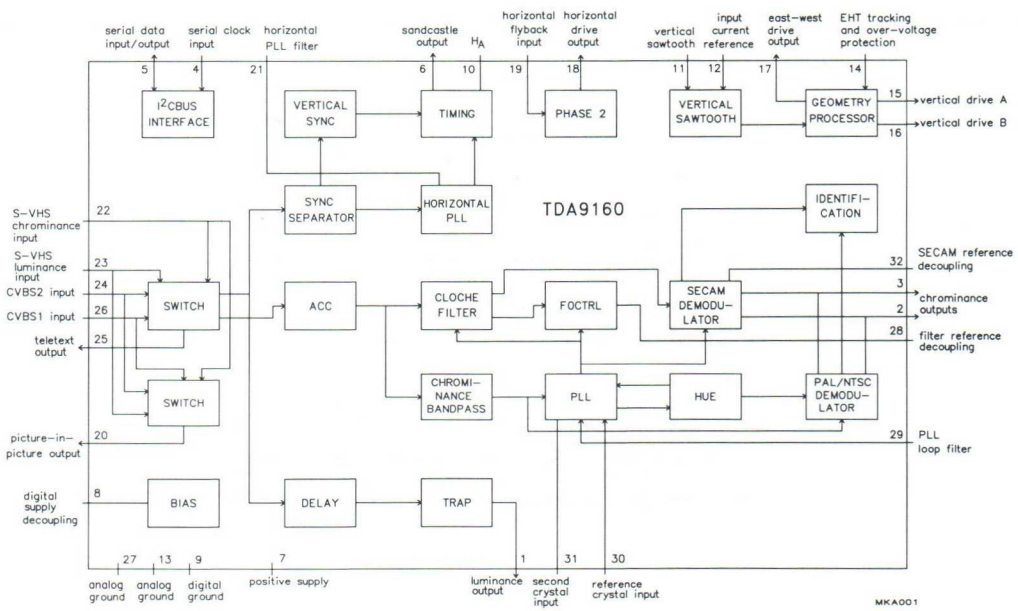


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
$V_{24.26(p-p)}$	CVBS input voltage (peak-to-peak value)		–	1.0	–	V
$V_{23(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)		–	1.0	–	V
$V_{22(p-p)}$	S-VHS chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
$V_{1(p-p)}$	luminance output voltage (peak-to-peak value)		–	0.45	–	V
$V_{25(p-p)}$	teletext output voltage (peak-to-peak value)		–	1.0	–	V
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	PAL/NTSC	–	525	–	mV
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	SECAM	–	1.05	–	V
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	PAL/NTSC	–	665	–	mV
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	SECAM	–	1.33	–	V
V_{10}	H_A output voltage		–	5.0	–	V
$I_{15.16(p-p)}$	vertical drive output current (peak-to-peak value)		–	1	–	mA
I_{18}	horizontal drive output current		–	–	10	mA
I_{17}	EW drive output current		–	–	0.9	mA
V_6	sandcastle clamping voltage level		–	4.5	–	V
V_6	sandcastle blanking voltage level		–	2.5	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9160	32	SDIL	plastic	SOT232

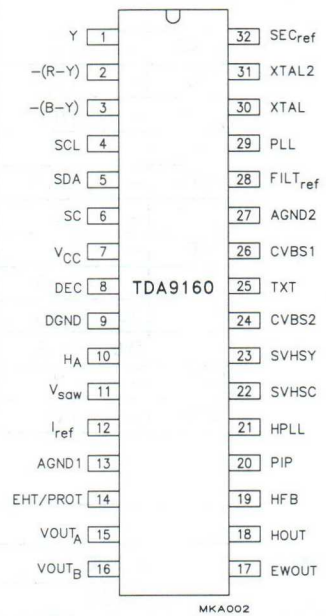


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
Y	1	luminance output
−(R-Y)	2	chrominance output
−(B-Y)	3	chrominance output
SCL	4	serial clock input
SDA	5	serial data input/output
SC	6	sandcastle output
V_{CC}	7	positive supply input
DEC	8	positive supply decoupling
DGND	9	digital ground
H_A	10	horizontal acquisition synchronization pulse
V_{saw}	11	vertical sawtooth
I_{ref}	12	input current reference
AGND1	13	analog ground
EHT/PROT	14	EHT tracking and over-voltage protection
$VOUT_A$	15	vertical drive output A
$VOUT_B$	16	vertical drive output B
EWOUT	17	east-west drive output
HOUT	18	horizontal drive output
HFB	19	horizontal flyback input
PIP	20	picture-in-picture output
HPLL	21	horizontal PLL filter
SVHSC	22	S-VHS chrominance input
SVHSY	23	S-VHS luminance input
CVBS2	24	CVBS2 input
TXT	25	teletext output
CVBS1	26	CVBS1 input
AGND2	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
PLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

FUNCTIONAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment free PAL/NTSC/SECAM colour decoder/sync processor/deflection controller which has been designed for use with baseband chrominance delay lines.
In the standard operating mode the I²C-bus address is 8A . If the TXT output is connected to the positive rail the address will change to 8E

The standards which the TDA9160 can decode are dependent on the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded. Which 3.6 MHz standards can be decoded is dependent on the exact frequencies of the crystal. In an application where not all standards are required only one crystal is sufficient (in this instance the crystal must be connected to the reference crystal input (pin 30)). If a 4.4 MHz crystal is used it must always be connected to pin 30. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator.
To enable the calibrating circuits to be adjusted exactly two bits from the I²C-bus address are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components; the search loop is illustrated in Fig.3.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information, concerning which standard and which crystal have been selected and whether the colour killer is ON or OFF is provided by the read out. Using the forced-mode does not affect the search loop, it does, however, prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. forced mode). To reduce the risk of wrong identification PAL has priority over SECAM (only line identification is used for SECAM).

The TDA9160 has two CVBS inputs and one S-VHS input which can be selected via the I²C-bus. The input selector can also be switched to enable CVBS2 to be processed, providing that there is no S-VHS signal present at the input. If the input selector is set to CVBS2 it will switch to S-VHS if an S-VHS sync pulse is detected at the luminance input. The S-VHS detector output can be read via the I²C-bus.
If the voltage at either the S-VHS luminance or the chrominance input (pins 22 and 23) exceeds +5.5 V the IC will revert to test mode.

The TDA9160 also provides outputs for picture-in-picture and teletext (PIP pin 20 and TXT pin 25). The decoder input signal can be switched directly to the TXT output. The PIP output signal can be selected independently from the TXT output. If S-VHS is selected at the TXT output only the luminance signal will be present; if S-VHS is selected at the PIP output then the luminance and chrominance signals will be added.

All filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.28 MHz or 3.58 MHz irrespective of the frequency of the active crystal. The switching is controlled by the identification circuit.

The S-VHS luminance signal does not pass through the notch filter to preserve bandwidth. The luminance delay line delivers the Y signal to the output 40 ns after the –(R-Y) and –(B-Y) signals. This compensates for the delay of the external chrominance delay lines.

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected it will always connect to the crystal at the reference input (pin 30).

The Hue signal, which is adjustable via the I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical flyback period, when the reference crystal is active. When the second crystal is active the VCO is not calibrated. During this time the frequency of the VCO is kept constant by applying a constant voltage to its control input. If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals.

The main part of the sync circuit is a 432 x f_H (6.75 MHz) oscillator the

frequency of which is divided by 432 to lock the phase 1 loop to the incoming signal. The time constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time constant, depending on the noise content of the input signal and whether the loop is phase locked or not (medium or slow). The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal.

When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency greater than 6.75 MHz to protect the horizontal output transistor. The oscillator frequency is reset to 6.75 MHz when the crystal indication bits have been loaded into the IC. To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits, when subaddress 01 is received the line oscillator calibration will be initiated. The calibration is terminated when the oscillator frequency reaches 6.75 MHz. The oscillator is again calibrated when an out-of-lock condition with the input signal is realised by the coincidence detector. Again the calibration will be terminated when the oscillator frequency reaches 6.75 MHz.
The phase 1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal the phase 1 loop can be opened to provide a stable line frequency and thus a stable picture.

The sync part provides an H_A pulse that is coupled to the processed CVBS signal.

The horizontal drive signal can be switched off via the I²C-bus (standby mode). The horizontal drive is also switched off when the over-voltage protection circuit trips or when a POR is detected. Should either of these two conditions occur the IC will return to the normal operating mode when the appropriate command is received via the I²C-bus. The duty cycle of the horizontal drive signal is increased from 2%, at start-up, to a constant value of 55% in approximately 300 lines. The two-level sandcastle pulse provides a combined horizontal and vertical blanking signal and a clamping pulse coupled to the display section of the TV.

The vertical sawtooth generator drives the geometry processing circuits which provide control for the horizontal shift, EW width, EW parabola/width ratio, EW corner/parabola ratio, trapezium correction, vertical slope, vertical shift, vertical amplitude and the S-correction. All of these control functions can be set via the I²C-bus. The geometry processor has a differential current output for the vertical drive signal and a single-ended output for the EW drive. Both the vertical drive and the EW drive outputs can be modulated for EHT compensation. The EHT compensation pin (pin 14) can also be used for over-voltage protection. De-interlace of the vertical output can be set via the I²C-bus.

The vertical divider system has a fully integrated vertical sync separator. The divider can accommodate both 50 and 60 Hz systems; it can either locate the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in Fig.4. The divider system operates at 432 times the horizontal line frequency. The line counter receives enable pulses at twice the line frequency, thereby counting two lines per pulse.
A state diagram of the controller is illustrated in Fig.5. Because it is symmetrical only the right hand part will be described.

Depending on the previously found field frequency, the controller will be in one of the 'count' states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal) the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR-NORM or NO-NORM depending on the position of the vertical sync pulse in the previous fields. When the counter is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal.
When the controller is in the NEAR-NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR-NORM window (i.e. $622 < LC < 628$). If no vertical sync pulse is detected, the controller will move back to the COUNT state when the line counter reaches LC = 628. The line counter will then be reset.
When the controller is in the NO-NORM state it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a sync pulse is not detected before LC = 722 (if the

phase loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the phase loop is not locked the controller will move back to the COUNT state when LC = 628. The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the 'norm' counter which is an up/down counter that counts up if it finds a vertical sync pulse within the selected window. In the NEAR-NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR-NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field. If no vertical sync pulse is found in the selected window this will always result in a down pulse for the 'norm' counter.

Figure 7 illustrates the timing of the display sandcastle (DSC) and the reset pulse of the vertical sawtooth with respect to the input signal.

I²C-bus protocol

If the TXT output is connected to the positive supply the address will change from 8A to 8E.

Valid subaddresses = 00 to 0F
Auto-increment mode available for subaddresses.

Subaddress 00 must always be sent before subaddress 01 in order to protect the horizontal output transistor.

Table 1 Slave address (8A)

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	X	1	X

Table 2 Inputs

SUBADDRESS	MSB							LSB
00	INA	INB	INC	IND	FOA	FOB	XA	XB
01	FORF	FORS	DL	STB	POC	FM	SAF	FRQF
02	–	–	HU5	HU4	HU3	HU2	HU1	HU0
03	–	–	HS5	HS4	HS3	HS2	HS1	HS0
04	–	–	EW5	EW4	EW3	EW2	EW1	EW0
05	–	–	PW5	PW4	PW3	PW2	PW1	PW0
06	–	–	CP5	CP4	CP3	CP2	CP1	CP0
07	–	–	TC5	TC4	TC3	TC2	TC1	TC0
08	–	–	VS5	CS4	VS3	VS2	VS1	VS0
09	–	–	VA5	VA4	VA3	VA2	VA1	VA0
0A	–	–	SC5	SC4	SC3	SC2	SC1	SC0
0B	SBL	–	VSH5	VSH4	VSH3	VSH2	VSH1	VSH0

Table 3 Outputs

ADDRESS	POR	FSI	STS	SL	PROT	SAK	SBK	FRQ

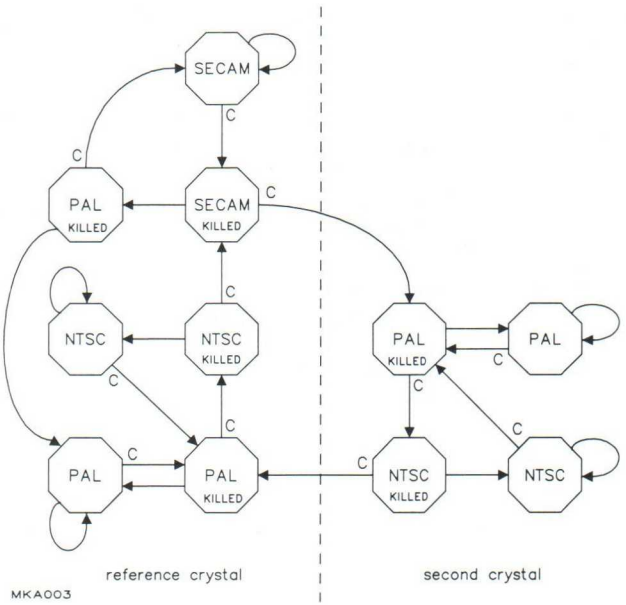


Fig.3 Search loop of the identification circuit.

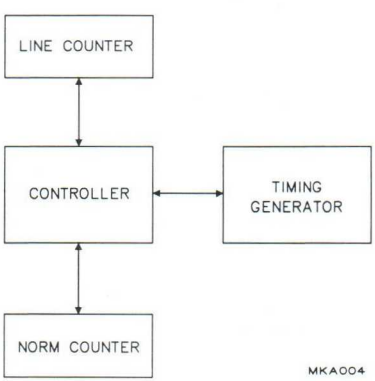


Fig.4 Block diagram of the vertical divider system.

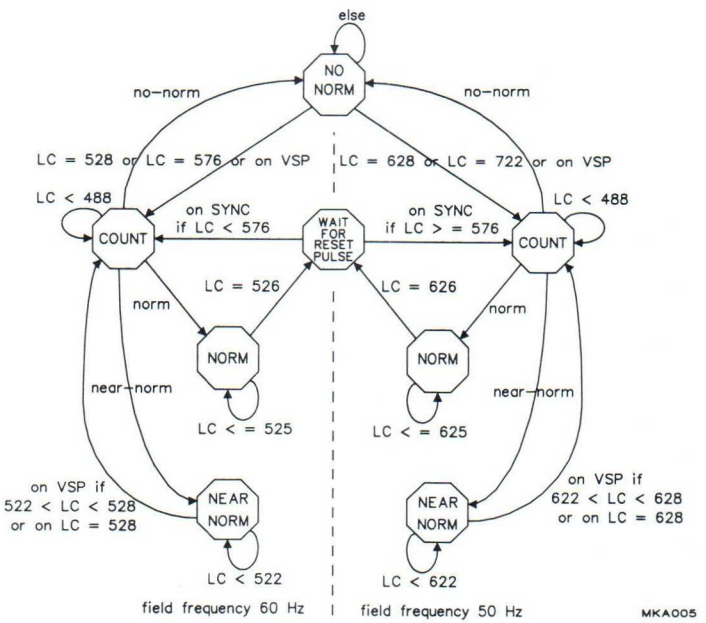


Fig.5 State diagram of the vertical divider system.

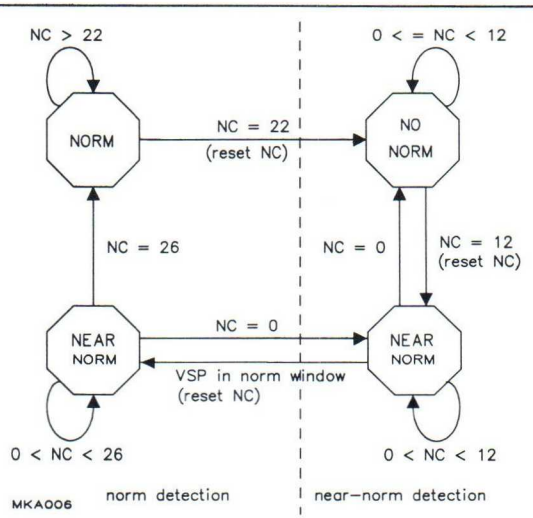


Fig.6 State diagram of the 'norm' counter.

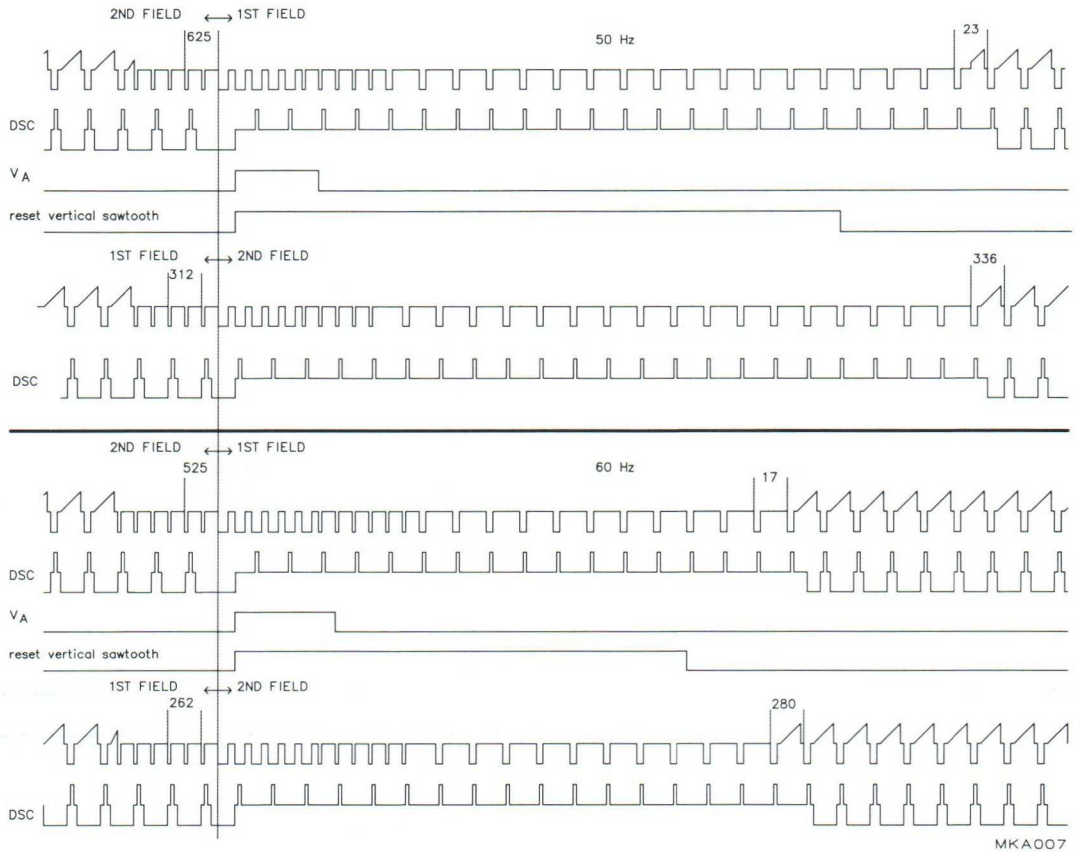


Fig.7 Field timing diagram.

INPUT SIGNALS

Table 4 Source select 1

INA	INB	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 5 Source select 2

INC	IND	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 6 Phase time constant

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 7 XTAL indication

XA	XB	CRYSTAL
0	0	2 x 3.6 MHz
0	1	1 x 3.6 MHz
1	0	1 x 4.4 MHz
1	1	3.6 and 4.4 MHz

Table 8 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto
0	1	60 Hz
1	0	50 Hz
1	1	auto

Table 9 Interlace

DL	CONDITION
0	interlace
1	de-interlace

Table 10 Standby

STB	CONDITION
0	standby
1	normal mode

Table 11 Phase loop control

POC	CONDITION
0	phi one loop closed
1	phi one loop open

Table 12 Forced standard

ADD	LOGIC	CONDITION
FM	0	auto search
	1	forced mode
SAF	0	PAL/NTSC
	1	SECAM
FRQF	0	second crystal
	1	reference crystal

Table 13 Service blanking

SBL	CONDITION
0	service blanking OFF
1	service blanking ON

Note to table 12

If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal the colour will be switched off.

Table 14 Other input signals

FUNCTION	ADDRESS	DIGITAL NUMBER
hue	HU5 to HU0	000000 = −45° 111111 = +45°
horizontal shift	HS5 to HS0	000000 = −2.2 µs 111111 = +2.2 µs
EW width	EW5 to EW0	000000 = 80% 111111 = 100%
EW parabola/width	PW5 to PW0	000000 = 0% 111111 = 24%
EW corner/parabola	CP5 to CP0	000000 = 0% 111111 = −44%
EW trapezium	TC5 to TC0	000000 = −4% 111111 = +4%
vertical slope	VS5 to VS0	000000 = −14% 111111 = +14%
vertical amplitude	VA5 to VA0	000000 = −80% 111111 = +120%
S correction	SC5 to SC0	000000 = 0% 111111 = 20%
vertical shift	VSH5 to VSH0	000000 = −4% 111111 = +4%

Table 15 Standard read-out

SAK	SBK	FRQ	STANDARD
0	0	0	PAL, second crystal
0	0	1	PAL, reference crystal
0	1	0	NTSC, second crystal
0	1	1	NTSC, reference crystal
1	0	0	not used
1	0	1	SECAM, reference crystal
1	1	0	colour off
1	1	1	clolour off

INPUT SIGNALS

Table 16 Power-on-reset

POR	CONDITION
0	normal mode
1	power-down mode

Table 17 Field frequency indication

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 18 S-VHS status

STS	CONDITION
0	no signal at input
1	signal at input

Table 19 Phase lock indication

SL	CONDITION
0	not locked
1	locked

Table 20 Over-voltage protection

PROT	CONDITION
0	no over-voltage detected
1	over-voltage detected

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		–	8.8	V
I_{CC}	supply current		–	70	mA
P_{tot}	total power dissipation		–	–	W
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–10	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	t.b.f.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
P_{tot}	total power dissipation		–	400	–	mW
Input switch						
CVBS1 AND CVBS2 INPUTS (PINS 26 AND 24)						
$V_{26,24(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS Y INPUT (PIN 23)						
$V_{23(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS CHROMINANCE INPUT (PIN 22)						
$V_{22(p\text{-}p)}$	input voltage (peak-to-peak value)	burst	–	0.3	1.43	V
Z_I	input impedance		60	–	–	kΩ
LUMINANCE OUTPUT (PIN 1)						
$V_{1(p\text{-}p)}$	output voltage (peak-to-peak value)		–	450	–	mV
Z_O	output impedance		–	–	500	Ω
V_O	top sync level		–	2.1	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPP	suppression of unselected inputs		50	–	–	dB
TXT AND PIP OUTPUTS (PINS 25 AND 20)						
$V_{20,25(p-p)}$	output voltage (peak-to-peak value)		–	1.0	–	V
Z_O	output impedance		–	–	500	Ω
V_O	top sync level	TXT output	–	1.8	–	V
		PIP output	–	2.8	–	V
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; PIP output	50	–	–	dB
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; TXT output	35	–	–	dB
Bias generator						
V_8	digital supply voltage		–	5.0	–	V
V_{12}	DC voltage		–	3.9	–	V
Subcarrier regeneration						
$V_{ACC(p-p)}$	burst amplitude within ACC range (peak-to-peak value)		25	–	500	mV
CR	catching range	note 1	500	–	–	Hz
φ	phase shift for 400 Hz deviation		–	–	5	deg
TC	temperature coefficient of oscillator		–	tbf	–	Hz/K
Z_I	input impedance	reference crystal input	–	1.0	–	kΩ
		second crystal input	–	1.5	–	kΩ
V_{dep}	supply voltage dependency		–	tbf	–	V
Demodulators						
Δ2/Δ3	change of –(R-Y) and –(B-Y) signals over the ACC range		–	–	1	dB
	ratio of –(R-Y) and –(B-Y) signals		–	1.27	–	
TC	temperature coefficient of –(R-Y) and –(B-Y) amplitude		–	tbf	–	Hz/K
	spread of –(R-Y) and –(B-Y) ratio between standards		–1	–	+1	dB
V_2	output level of –(R-Y) during blanking		–	2.0	–	V
V_3	output level of –(B-Y) during blanking		–	2.0	–	V
B	bandwidth	at –3 dB	–	1	–	MHz
Z_O	output impedance		–	–	500	Ω
V_{dep}	supply voltage dependency		–	tbf	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/NTSC DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	525	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	665	–	mV
α	crosstalk between –(R-Y) and –(B-Y)		–	tbf	–	dB
$V_{2.3(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{2.3(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
S/N	signal-to-noise ratio		46	–	–	dB
PAL DEMODULATOR						
$V_{R(p-p)}$	H/2 ripple (peak-to-peak value)		–	–	50	mV
S/N	signal-to-noise ratio		46	–	–	dB
NTSC DEMODULATOR						
φ	hue phase shift		–45	–	+45	deg
SECAM DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	mV
f_{OS}	black level offset		–	–	7	kHz
S/N	signal-to-noise ratio		–	43	–	dB
$V_{res(p-p)}$	7.8 to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of deemphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3.0	4.0	5.0	V
NL	non linearity		–	–	3	%
Filters						
V_{tune}	tuning voltage		1.5	3.0	6.0	V
Luminance delay						
t_d	delay time	PAL/NTSC/BW	–	430	–	ns
t_d	delay time	SECAM	–	480	–	ns
Luminance trap						
f_O	notch frequency	f_{SC} = 3.6 MHz f_{SC} = 4.4 MHz SECAM S-VHS/BW; not active	3.53 4.37 4.23	3.58 4.43 4.29	3.63 4.49 4.35	MHz MHz MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	2.8	–	MHz
		f_{SC} = 4.4 MHz	–	3.4	–	MHz
		SECAM	–	3.3	–	MHz
SUPP	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency	f_{SC} = 3.6 MHz	–	3.58	–	MHz
		f_{SC} = 4.4 MHz	–	4.43	–	MHz
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	1.6	–	MHz
		f_{SC} = 4.4 MHz	–	2	–	MHz
Cloche filter						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth	at –3 dB; SECAM	241	268	295	kHz
Sync input						
V_{22}	sync pulse amplitude	CVBS 1/2; S-VHS input	50	300	600	mV
	slicing level		–	50	–	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
S/N	noise detector threshold level		–	20	–	dB
H	hysteresis		–	3	–	dB
t_d	delay between video signal and internally separated vertical sync pulse		12	18.5	27	µs
Horizontal section						
H_A OUTPUT (PIN 10)						
V_{OH}	output voltage HIGH		2.4	5.0	5.5	V
V_{OL}	output voltage LOW		–	0.3	0.6	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	pulse width	32 clock cycles	–	4.7	–	µs
t_d	delay between middle of horizontal sync pulse and middle of H_A	note 2	0.3	0.45	0.6	µs
FIRST LOOP						
Δf	frequency deviation when not locked		–	–	1.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	V
TC	temperature coefficient		–	tbf	–	Hz/°C
f_{CR}	catching range		625	–	–	Hz
f_{HR}	holding range		–	–	1400	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ϕ	static phase shift		–	–	0.1	µs/kHz
SECOND LOOP						
φ	control sensitivity		300	–	–	µs/µs
t_{CR}	control range of the positive going edge of horizontal drive to flyback	HS = 00; note 4	13.5	–	–	µs
t_d	delay between second loop reference and mid-sync of processed video		–	3	–	µs
HORIZONTAL SHIFT						
SR	horizontal shift range	63 steps	–2.2	–	+2.2	µs
HORIZONTAL DRIVE OUTPUT (PIN 18)						
R_{18}	output resistance	on-state	–	–	50	Ω
I_{18}	output current		–	–	10	mA
	duty cycle of output current		–	55	–	%
HORIZONTAL FLYBACK INPUT (PIN 19)						
V_{HB}	switching level for horizontal blanking		–	0.3	–	V
$V_{\varphi 2}$	switching level for phase two loop		–	3.8	–	V
V_{19}	maximum input voltage		–	–	V_{CC}	V
Z_I	input impedance		10	–	–	MΩ
Soft start						
CR	duty cycle control range		2	–	55	%
	soft start time		200	300	500	lines
Vertical section (note 3)						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency	divider ratio 628	–	50	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
VERTICAL SAWTOOTH (PIN 11)						
$V_{11(p-p)}$	voltage amplitude level (peak-to-peak value)	VS = 1F; C = 100 nF; R = 39 kΩ	–	3.5	–	V
I_{dis}	discharge current		–	1	–	mA
I_{charge}	charge current set by external resistor	f = 50 Hz; VS = 1F	–	19	–	µA
CR	vertical slope control range	63 steps	–14	–	+14	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL DRIVE OUTPUTS (PINS 15 AND 16)						
$I_{diff(p-p)}$	differential output current (peak-to-peak value)	VA = 1F	–	1	–	mA
$I_{15,16}$	common mode current		–	400	–	µA
V_O	output voltage range		0	–	4.0	V
EHT TRACKING AND OVER-VOLTAGE PROTECTION (PIN 14)						
TR	tracking range		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
α	sensitivity		–	7.5	–	%/V
V_{14}	over-voltage protection detection level		–	3.9	–	V
DE-INTERLACE						
	first field delay		–	0.5H	–	
Sandcastle (pin 6)						
V_6	zero level		0	0.5	1.0	V
I_{sink}	sink current		0.5	–	–	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.0	2.5	3.0	V
I_{source}	source current		0.5	–	–	mA
I_{ext}	external current required to force the output to the blanking level		1	–	3	mA
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.0	4.5	5.0	V
I_{source}	source current		0.5	–	–	mA
t_W	pulse width	PAL (17 LLC pulses) SECAM (24 LLC pulses)	– –	2.5 3.6	– –	µs µs
t_d	delay between mid sync of input and start of clamping pulse		3.6	3.7	3.8	µs
Geometry processing (note 3)						
EW WIDTH						
CR	control range	63 steps	100	–	80	%
I_{eq}	equivalent EW output current		0	–	400	µA
V_O	EW output voltage range		1.0	–	8.0	V
I_O	EW output current range		0	–	900	µA
EW PARABOLA/WIDTH						
CR	control range	63 steps	0	–	24	%
I_{eq}	equivalent EW output current	EW = 3F	0	–	480	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW CORNER/PARABOLA						
CR	control range	63 steps	–44	–	0	%
I_{eq}	equivalent EW output current	EW = 3F; PW = 3F	–210	–	0	µA
EW TRAPEZIUM						
CR	control range	63 steps	–4	–	+4	%
I_{eq}	equivalent EW output current		–80	–	+80	µA
EW EHT TRACKING						
TR	tracking range		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
I_{eq}	equivalent output current		+120	–	–120	µA
φ	sensitivity		–	–7.5	–	%/V
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00 63 steps; SC = 3F	80 86	– –	120 112	% %
I_{eq}	equivalent differential vertical drive output current	SC = 00	800	–	1200	µA
VERTICAL SHIFT						
CR	control range	63 steps	–4	–	+4	%
I_{eq}	equivalent differential vertical drive output current		–40	–	+40	µA
S CORRECTION						
CR	control range	63 steps	0	–	20	%

Notes to the characteristics

1. All oscillator specifications are measured with the Philips crystal series 4322 143/144. The spurious response of the reference crystal must be less than –7 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ. The spurious response of the second crystal must be less than –7 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.
2. This delay is caused by the low pass filter at the sync separator input.
3. All values are valid for a reference current of 100 µA (R_C = 39 kΩ).
4. Valid for flyback pulse width of 12 µs at the switching level of the phase 2 loop.

QUALITY SPECIFICATION

Quality level according to URV 4-2-59/601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Test and application information

EW output stage

In order to obtain the correct tracking of the vertical and horizontal EHT correction, the EW output stage should be configured as illustrated in figure 8.

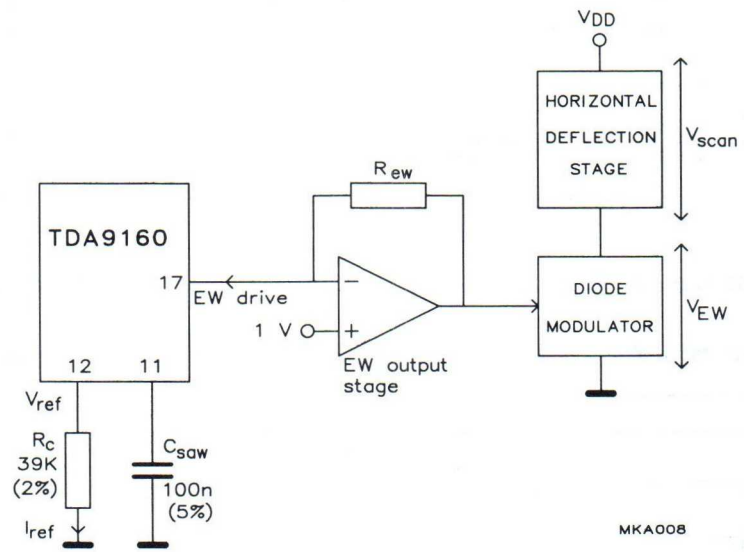


Fig.8 Configuration of the EW output stage.

Note to Fig.8

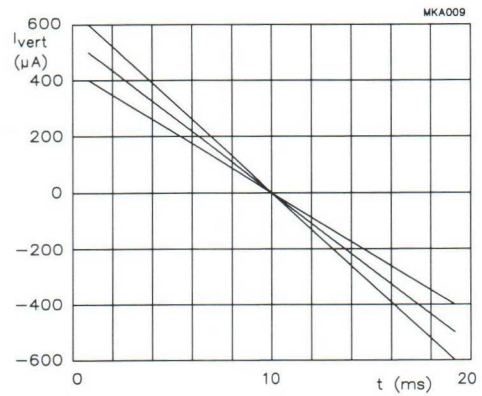
Resistor R_{ew} determines the gain of the EW output stage. Resistor R_c sets the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_c = 39 kΩ results in a reference current of 100 µA (V_{ref} = 3.9 V).
The value of R_{ew} is given in the following equation:

$$R_{ew} = R_c \times \frac{V_{scan}}{(18 \times V_{ref})}$$

Example: If V_{ref} = 3.9 kΩ, R_c = 39 kΩ and V_{scan} = 120 V then R_{ew} = 68 kΩ

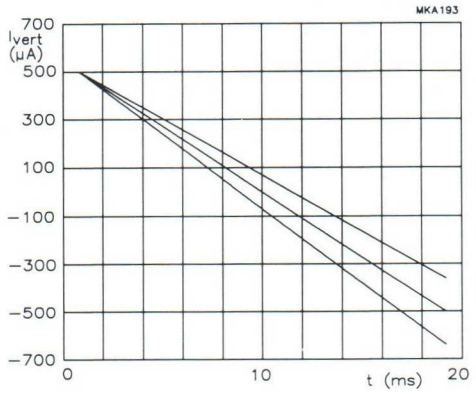
Control ranges of geometry control parameters

Typical case curves (R_C = 39 kΩ; C_{saw} = 100 nF)



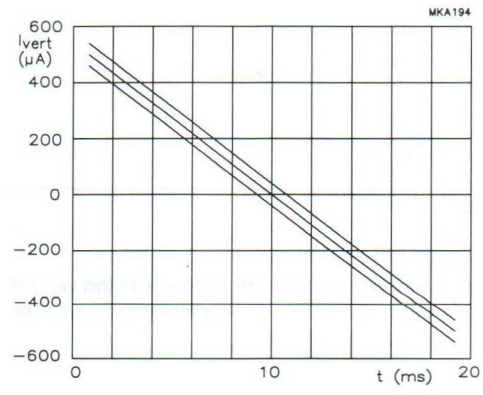
VA = 0, 31 and 63; VSH = 31; SC = 0

Fig.9 Control range of vertical amplitude.



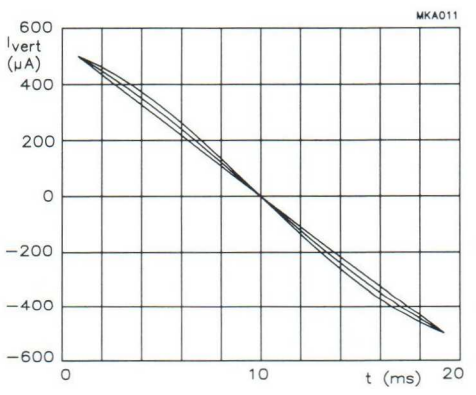
VA = 31; VS = 0, 31 and 63; VSH = 31; SC = 0

Fig.10 Control range of vertical slope.



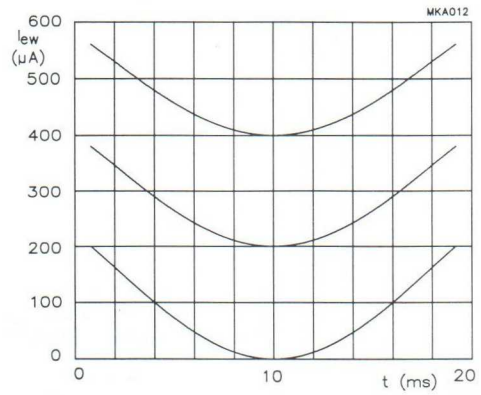
VA = 31; VSH = 0, 31 and 63; SC = 0

Fig.11 Control range of vertical shift.



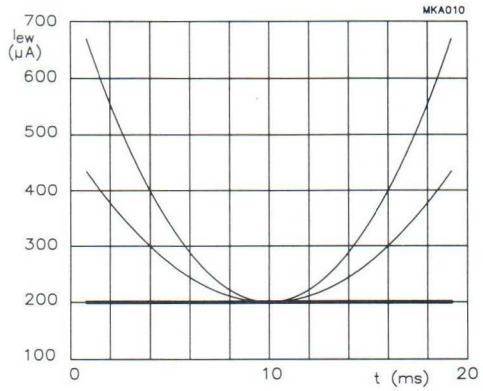
SC = 0, 31 and 63; VA = 31; VSH = 31. The picture height does not change with the setting of S correction for nominal setting of vertical amplitude (VA = 31).

Fig.12 Control range of S correction.



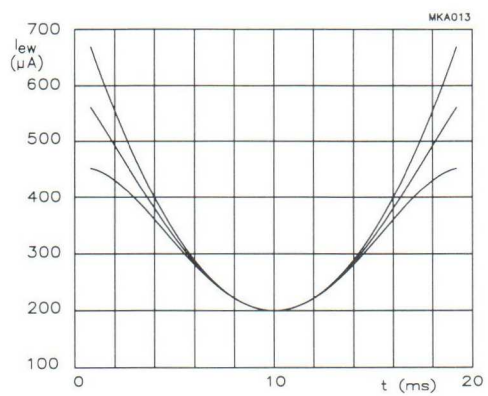
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.13 Control range of EW width.



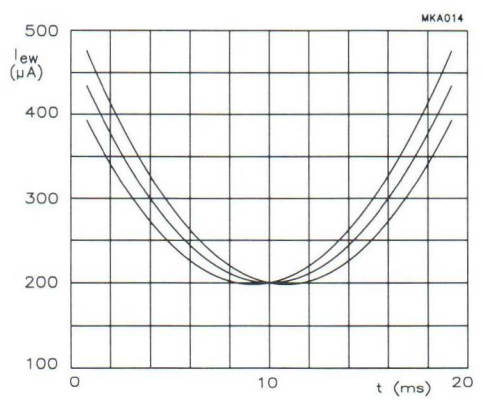
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.14 Control range of EW parabola/width ratio.



CP = 0, 31 and 63; EW = 31; PW = 63

Fig.15 Control range of EW corner/parabola ratio.



TC = 0, 31 and 63; EW = 31; PW = 31; CP = 0

Fig.16 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA9160 offers nine control parameters for picture alignment:

- S-correctiion, vertical amplitude, vertical slope and vertrical shift for the vertical picture alignment
- Horizontal shift, EW width, EW parabola/width, EW corner/parabola and EW trapezium correction for the horizontal picture alignment

The required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio are determined for a particular combination of picture tube type, vertical output stage and EW output stage. These parameters can be preset via the I²C-bus and do not require any additional adjustment. The remainder of the parameters are preset to the mid value of their control range (i.e. 1F), or to values that have obtained from previous TV set adjustments.
After the vertical S-correction has been preset the vertical picture alignment could, in theory, be completed by positioning the top of the picture using the vertical amplitude adjustment and the bottom of the picture using the vertical slope adjustment (see note). It can be shown, however, that without compensation offsets in the external vertical output stage or in the picture tube would result in a certain linearity error especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the offset and to the square of the required S-correction. A vertical shift control is available for offset compensation.
For adjustmen of the vertical shift, independent of the vertical slope, a special vertical shift alignment is provided. This mode is entered by setting the SBL bit HIGH. In this mode the –(R-Y) and –(B-Y) outputs are blanked during the second half of the picture. The first line in which the colours are blanked must be positioned in the middle of the screen.
The necessity to use the vertical shift alignment depends on the expected offsets in the vertical output stage and picture tube, on the required value of the S-correction and on the demands upon the vertical linearity. If the vertical shift alignment is not used VSH should be set to its mid value (i.e. VSH = 1F).
The actual factory adjustments of the picture consist of the following steps:

- The vertical shift is adjusted as previously described (if required).
- The top of the picture is positioned by adjusting the vertical amplitude and the bottom of the picture by adjusting the vertical slope
- The picture is positioned in the horizontal direction by adjusting the EW width and horizontal shift
- The left and right hand sides of the picture are aligned in parallel by adjusting the EW trapezium correction (if required).

Note

The value of the vertical slope determines the charge current of the vertical sawtooth capacitor (C_{saw} as shown in Fig.8) and thus the amplitude of the sawtooth voltage at pin 11. This voltage serves as the input voltage for the geometry processor. Consequently the setting of the vertical slope will affect both the vertical and EW output currents.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

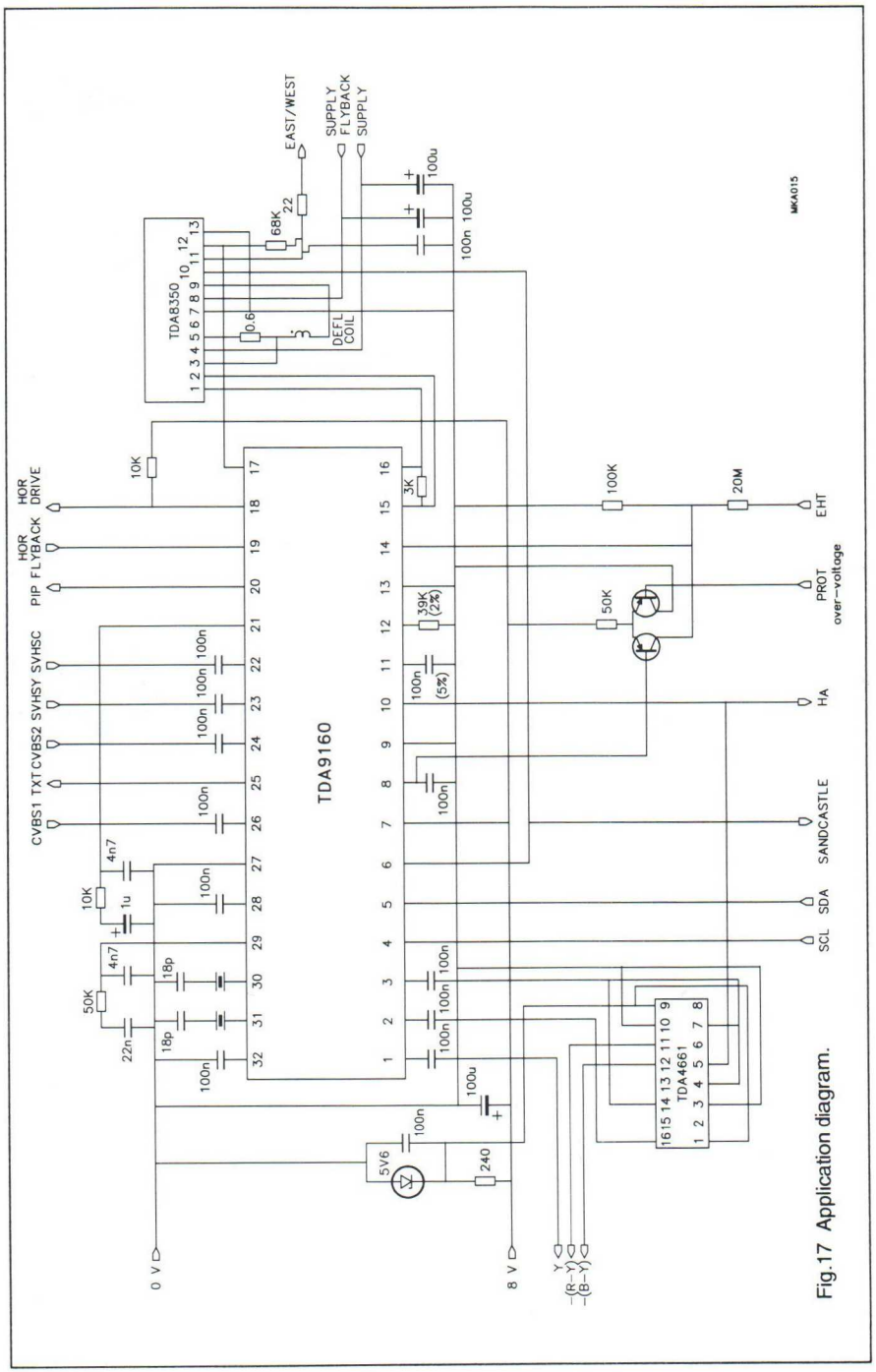


Fig.17 Application diagram.

Notes to figure 17

1. Pins 31 and 32 are sensitive to leakage current.
2. The analog and digital ground currents should be well separated.
3. The decoupling capacitor connected between pins 8 and 9 must be placed as close to the IC as possible.

YUV picture improvement processor based on histogram modification

TDA9170

FEATURES

- Picture content dependent non-linear Y and U, V processing by histogram analysis
- Adaptive and variable gamma correction controls
- Black and white stretch capabilities
- Transparent I²C-bus control
- On-chip window generator for valid histogram measurement and black detection.

GENERAL DESCRIPTION

The TDA9170 is a transparent analog video processor with a YUV interface. It offers three main luminance processing functions any combination of which can be selected.

The luminance transfer is controlled in a non-linear manner by the distribution (in 5 discrete histogram sections) of the luminance values measured in a picture. As a result, the contrast ratio of the most important parts of the picture will be improved.

Black restoration is available in the event of a set-up in the luminance signal. A variable gamma function, after the histogram conversion, offers the possibility of excellent brightness control.

To maintain a proper colour reproduction, the saturation of the U and V colour difference signals are controlled as a function of the actual non-linearity in the luminance channel.

The TDA9170 concept has maximum flexibility with the optional on-board I²C-bus (including hardwired address select) and window control. The supply voltage is 8 V. The device is mounted in a 32 pin SDIP envelope.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9170	SDIP32	plastic shrink in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

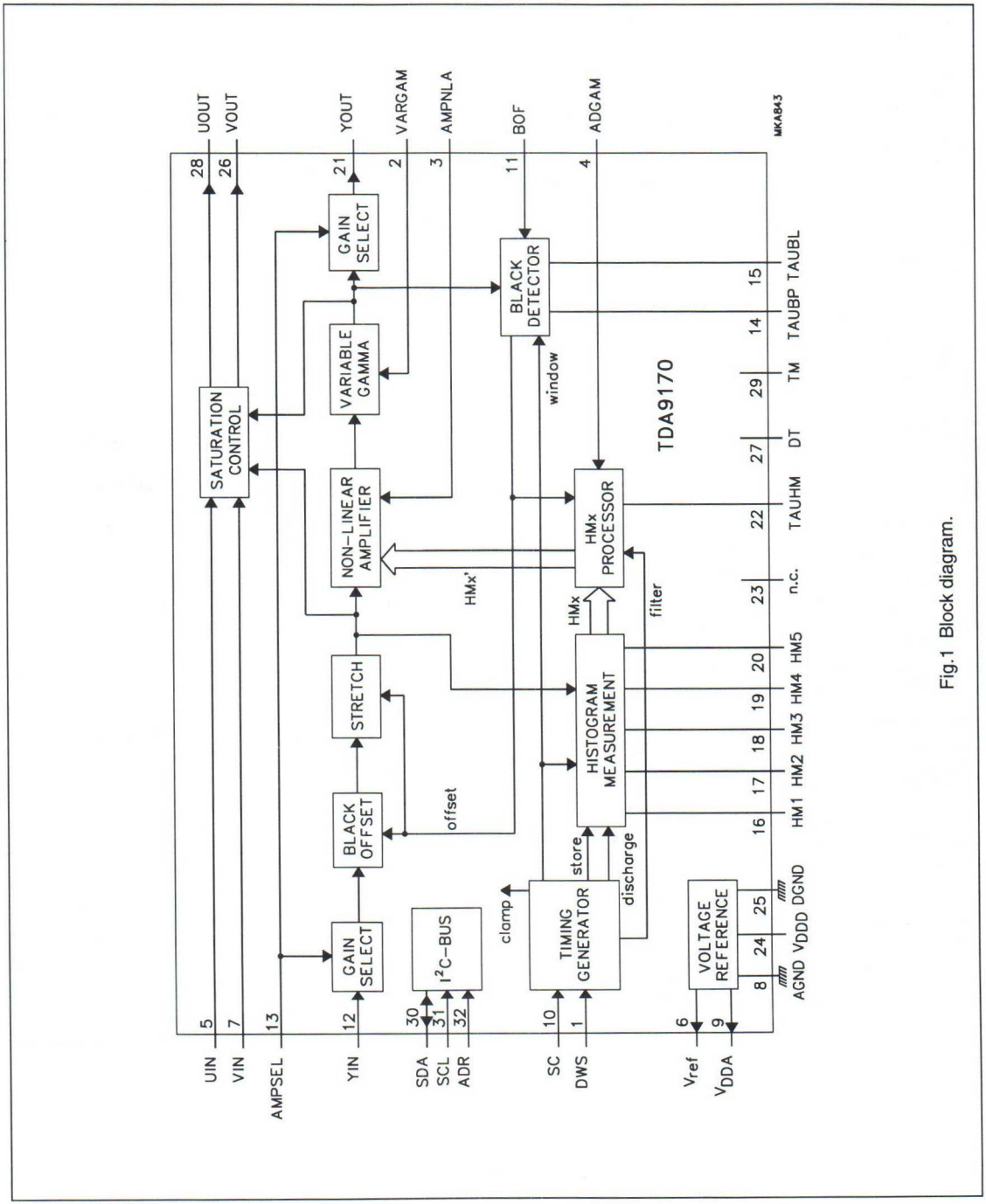


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DWS	1	default window select input
VARGAM	2	variable gamma input
AMPNLA	3	amplitude non-linearity input
ADGAM	4	adaptive gamma input
UIN	5	colour difference U input
V_{ref}	6	reference supply voltage output (+4 V)
VIN	7	colour difference V input
AGND	8	analog ground
V_{DDA}	9	analog supply voltage
SC	10	sandcastle input
BOF	11	black offset on/off input
YIN	12	luminance input
AMPSEL	13	amplitude select input
TAUBP	14	time constant black peak
TAUBL	15	time constant black loop
HM1	16	histogram segment memory 1
HM2	17	histogram segment memory 2
HM3	18	histogram segment memory 3
HM4	19	histogram segment memory 4
HM5	20	histogram segment memory 5
YOUT	21	luminance output
TAUHM	22	time constant histogram measurement loop
n.c.	23	not connected
V_{DDD}	24	digital supply voltage (+5 V)
DGND	25	digital ground
VOUT	26	colour difference V output
DT	27	test option
UOUT	28	colour difference U output
TM	29	test option
SDA	30	serial data input/output (I^2C-bus)
SCL	31	serial clock input (I^2C-bus)
ADR	32	address select input (I^2C-bus)

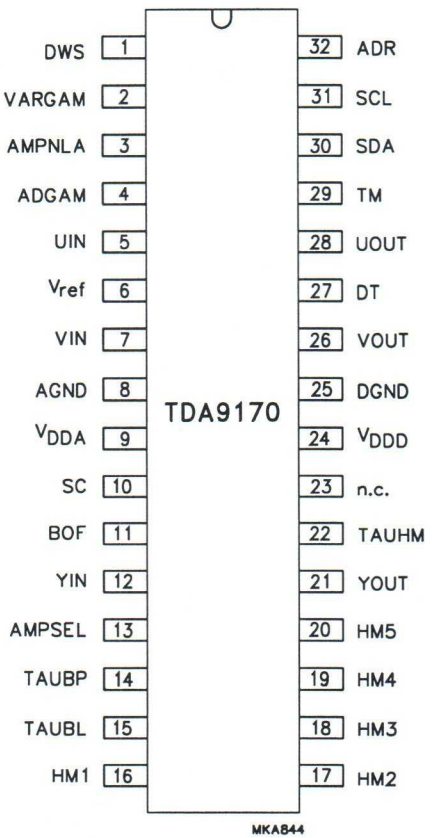


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Y input selection and amplification

The dynamic range of the luminance input amplifier can be switched between 0.3 and 1 V (excluding sync) either externally (pin AMPSEL) or by I²C-bus (AMPSEL bit). Amplitudes that exceed the corresponding specified range (e.g. the sync) will be clipped internally. The input is clamped during the logic HIGH period of the clamp which is defined by the sandcastle reference and should be DC-decoupled with an external capacitor.

Black offset detection and correction

The black detector measures and stores the blackest part of the picture within a defined window in each field. Any difference between this value and the value measured during the black clamp period is regarded as black offset. In a closed loop configuration, the black offset is held until a predefined value of the full scale (FS) value is fed back to the input stage where it is partly compensated for. Depending on the loop gain, 30% to 50% of the offset value is counteracted. The loop gain is also a function of the adaptive and variable gamma settings. The black offset correction mechanism can be switched on and off by the I²C-bus via the BON bit (see Table 6), or externally with the black offset on/off switch (BOF pin 11).

Two external time constants are required to ensure correct performance of the black detector; a loop filter time constant (TAUBL) for the loop dynamics and a time constant for memorizing the darkest parts of the picture (TAUBP) in just one field. During the field retrace the time constant TAUBP is first sampled and then preset to a value that corresponds to the maximum black offset.

The corrected black offset is related to the nominal signal amplitude which is reset to 100% FS via an amplitude stretch function. Luminance values beyond FS are not affected. Additionally, this offset is also used to set the adaptive gain (see Section "Adaptive gamma").

Histogram measurement

The histogram distribution is measured in real time over five segments (HM1 to HM5) within a defined window period of each field. During the window period, the video is in one segment, a corresponding external capacitor C_{HMx} is loaded via a current source. At the end of the field five segment voltages are stored from the external capacitors into on-board memories. The external capacitors are discharged and the measurements are restarted.

Any part of the picture that does not contribute to the information within the total picture should be omitted from the histogram measurement. The miscount detector disables measurements until it detects changing parts. Additionally, luminance values close to FS (or white) do not contribute sufficiently in order to maintain the absolute light output. This procedure is allowed because the eye is less sensitive to details in white.

As the miscount detector shortens the effective measurement period and, because of spreads of internal and external components, the current source is controlled within in a closed loop so as to maintain a constant average value of the sum of the segment voltages. The dominant time constant of the closed loop is external and can be tuned with an appropriate capacitor connected to TAUHM (pin 22).

Processing of the measured histogram values

Field averaging of histogram values

With very rapid picture changes, also related to the field interlace, flicker might result. The histogram values are averaged at the field rate to reduce these flicker effects. The time constant of the averaging process is adapted to the speed of the histogram changes.

Adaptive gamma

The output voltage of the first segment is fed to a variable gain amplifier with a gain between 1 and 3. In this way luminance values in the 'black' segment have a larger weight. In our perception black parts are expanded, as occurs with gamma control. However, the effective contribution to the non-linear gain is only relevant for moderate segment voltages and hence the term adaptive gamma.

The adaptive gamma gain is a **max**-function of a fixed gain part and a dynamic gain part. The fixed gain part can be set externally with the adaptive gamma gain control (ADGAM) or via the I²C-bus.

The dynamic part of the adaptive gamma gain is controlled by the measured black offset value from the black detector.

ADAPTIVE WHITE-POINT STRETCHING

For dominant HM4 and HM5 voltages or large white parts the histogram conversion procedure makes a transfer with large gain in the white parts. However, the amount of light being emitted from the picture is considerably reduced. The white stretcher introduces additional overall gain for increased light production and, as a result, violates the principle of having a full-scale reference.

STANDARD DEVIATION

For pictures in which segments of the histogram distribution are very dominant, with respect to the others, the non-linear amplification should be reduced to compensate for pictures with a flat histogram distribution. The standard deviation detector measures the spread of the histogram distribution in the segments HM1 to HM5 and modulates the user setting of the non-linear amplifier.

Non-linear amplifier

The stored segment voltages, relative to their average value and averaged over two fields, determine the individual gain of each segment in such a way that continuity is guaranteed for the complete range. The maximum and minimum gain of each segment is limited. Apart from the adaptive white-point stretching the black and white references are not affected by the non-linear processing. The amount of linearity can be controlled externally at AMPNLA (pin 3) or via the I²C-bus.

Variable gamma function

As well as the histogram conversion, a variable gamma function can be applied to ensure excellent brightness control. It is intended as an alternative to the DC-offset of the classic brightness user control; it maintains the black and white references. The gamma ranges from 0.5 to 1.5. The gamma can be set externally at VARGAM (pin 2) or via the I²C-bus.

Colour compensation

Non-linear luminance processing influences the colour reproduction, mainly the colour saturation. Therefore, U and V signals are also processed for saturation compensation. The U and V input signals are clamped during the logic HIGH period of the clamp which is defined by the sandcastle reference and should be DC decoupled with external capacitors.

Timing generator

The TDA9170 is equipped with a transparent internal timing generator for window purposes. As a timing reference the relevant sandcastle (SC) can be used. The window enables the black measurement and the histogram measurement circuitry. The internal timing generator is basically intended for system invariant operation. The default window handles all existing norms and disables measurement in subtitles or logos. This default window is preset at power-up and can be selected with a logic HIGH level at the default window select DWS (pin 1). If not selected the blanking of the sandcastle will define the window borders.

However, using the I²C-bus and setting the WD1 and WD2 control bits (see Table 3), the window format can also be user-programmed. The horizontal window generator synchronizes on the rising edge of the burst key/clamp key of the external sandcastle reference with an adjustable window start and stop delay. The vertical window generator synchronizes on the falling edge of the first burst key/clamp key after a field pulse recognition.

I²C-bus specification

The I²C-bus is designed for transparent use. At power-up all registers are preset for system invariant and external control. All pins related to the I²C-bus can be left open-circuit when the I²C-bus is in the standby mode. If the sleep mode bit in the control register is set all settings are left to bus control. For the relevant registers and addresses see Tables 2 to 8.

Table 1 Slave address.

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	ADR	X

Table 2 Control function.

CONTROL FUNCTION	TYPE	SUB-ADDRESS[1]	DATA BYTE							
			D7	D6	D5	D4	D3	D2	D1	D0
Control	REG	00	X	X	X	BON	WD2	WD1	AMS	SLP
User variable gamma	DAC	01	X	X	D5	D4	D3	D2	D1	D0
Adaptive gamma	DAC	02	X	X	D5	D4	D3	D2	D1	D0
Non-linear amplifier	DAC	03	X	X	D5	D4	D3	D2	D1	D0
Line start stop	REG	04	ST3	ST2	ST1	ST0	SP3	SP2	SP1	SP0
Field start stop	REG	05	ST3	ST2	ST1	ST0	SP3	SP2	SP1	SP0
Status	REG	–	X	X	X	X	X	X	X	POR

Note

1. Valid sub-addresses: 00 to 05 (HEX); auto-increment mode available for sub-addresses.

Table 3 Window select bits (WD1 and WD2).

WD1	WD2	FUNCTION
0	0	default window
0	1	window by sandcastle blanking
1	X	user window

Table 4 Amplitude select bit (AMS).

LOGIC LEVEL	FUNCTION
0	0.3 V luminance
1	1 V luminance

Table 5 Sleep mode bit (SLP).

LOGIC LEVEL	FUNCTION
0	sleep
1	I^2C-bus control

Table 6 Black offset compensation enable bit (BON).

LOGIC LEVEL	FUNCTION
0	disabled
1	enabled

Window formats

Table 7 Line frequency start stop format.

LINE WINDOW[1]	TIMING[2]	UNIT
Start (LWS)	$^{4.5}/_{64fh} + {}^{1}/_{64fh} \times$ DEC(ST3, ST2, ST1, ST0)	µs
Stop (LWP)	$^{26.5}/_{64fh} + {}^{2}/_{64fh} \times$ DEC(SP3, SP2, SP1, SP0)	µs
Default	DEC(ST3, ST2, ST1, ST0) = 2 DEC(SP3, SP2, SP1, SP0) = 14	

Notes

1. Start and stop events are relative to the leading edge of the BK/CLP pulse of the sandcastle.
2. fh is defined as the line frequency.

Table 8 Field frequency start stop format.

FIELD WINDOW[1]	TIMING	UNIT
Start (FWS)	10 + 6 × DEC(ST3, ST2, ST1, ST0)	lines
Stop (FWP)	121 + 10 × DEC(SP3, SP2, SP1, SP0)	lines
Default	DEC(ST3, ST2, ST1, ST0) = 9 DEC(SP3, SP2, SP1, SP0) = 4	

Note

1. The start event is relative to the trailing edge of the first BK/CLP pulse after a field pulse recognition. The stop event is relative to the actual start event.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		−0.5	+8.8	V
V_{DDD}	digital supply voltage		−0.5	+5.5	V
V_{ref}	reference supply voltage		−0.5	+5.5	V
V_n	voltage input/output on any other pin		−0.5	V_{DDA} + 0.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−10	+70	°C
V_{es}	electrostatic discharge	note 1	−2000	+2000	V
		note 2	−200	+200	V

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The Handbook can be ordered using the code 9398 510 63011. All pins are protected against electrostatic discharge by means of clamping diodes.

Latch-up

At T_{amb} = 70 °C all pins meet the specification as follows, except for pins 6 and 7 at positive trigger currents:

$I_{trigger} > 100$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

$I_{trigger} < -100$ mA or $V_{pin} < -0.5V_{DDA(max)}$.

pin 6, V_{ref}: $I_{trigger} > 40$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

pin 24, V_{DDD}: $I_{trigger} > 70$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	48	K/W

CHARACTERISTICS

V_{DDA} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins 6, 9 and 24)						
V_{DDA}	analog supply voltage		7.2	–	8.8	V
V_{DDD}	digital supply voltage		–	5.0	–	V
V_{ref}	reference supply voltage		–	4.0	–	V
I_{DDA}	analog supply current		–	40	–	mA
$Z_{o(24)}$	output impedance		–	–	250	Ω
$Z_{o(6)}$	output impedance		–	–	250	Ω
Luminance input/output selection						
LUMINANCE INPUT (PIN 12); note 1						
$V_{i(Y)}$	luminance input voltage	AMPSEL = 0	0.3	–	–	V
		AMPSEL = 1	1.0	–	–	V
$V_{i(Yclamp)}$	input voltage level during clamping		–	1.5	–	V
$I_{ib(Y)}$	input bias current		–	–	0.1	µA
LUMINANCE INPUT VOLTAGE RANGE SELECTION AMPSEL (PIN 13); note 2						
$V_{i(SEL)l}$	input voltage selection for lower range		–	–	1.5	V
$V_{i(SEL)h}$	input voltage selection for higher range		3.5	–	–	V
$I_{ib(SEL)}$	input bias current		–	–	0.1	µA
LUMINANCE OUTPUT (PIN 21)						
$V_{o(Y)}$	luminance output voltage	AMPSEL = 0	0.3	–	–	V
		AMPSEL = 1	1.0	–	–	V
$V_{oYclamp}$	output voltage level during clamping	AMPSEL = 0	–	2.9	–	V
		AMPSEL = 1	–	2.0	–	V
V_{no}	output noise voltage		52	–	–	dB
B_Y	luminance bandwidth	transparent	7	9	–	MHz
$B_{Y(nl)}$	non-linear processing luminance bandwidth		10	–	–	MHz
E_{bl}	black level error	no offset; transparent	–	–	1	%
$E_{G(n)}$	nominal gain error	no offset; transparent	–	–	8	%
Black detection and correction						
BLACK DETECTOR						
$BI_{osd(max)}$	maximum black offset detection at the input		23	25	27	%
$BI_{osc(max)}$	maximum black offset correction at the input		8	10	12	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PICTURE AMPLITUDE STRETCH						
$E_{G(s)}$	gain error after stretch	maximum offset	–	–	1	%
BLACK OFFSET CORRECTION ON/OFF SWITCH BOF (PIN 11); note 2						
$V_{i(blos)}$	input voltage level	correction off	–	–	1.5	V
		correction on	3.5	–	–	V
$I_{ib(blos)}$	input bias current		–	–	0.1	µA
TIME CONSTANT CONTROL TAUBP (PIN 4); see Fig.3						
$I_{BP(d)}$	discharge current		–	–	3.5	mA
I_{ibBP}	input bias current		–	–	0.1	µA
$V_{BP(l)}$	control voltage lower limit		–	1.0	–	V
$V_{BP(h)}$	control voltage upper limit		–	2.5	–	V
TIME CONSTANT CONTROL TAUBL (PIN 5); see Fig.4						
I_{ibBL}	input bias current		–	–	0.1	µA
$V_{BL(l)}$	control voltage lower limit		–	2.0	–	V
$V_{BL(h)}$	control voltage upper limit		–	3.5	–	V
Histogram measurement						
HISTOGRAM UPDATES AT HMx (PINS 16 TO 20)						
Q_{HMb}	segment bleeder accuracy		–	–	2	%
$V_{HM(av)}$	average voltage level for 5 segments		–	1.0	–	V
$V_{HM(min)}$	minimum segment voltage level		0	–	–	V
$V_{HM(max)}$	maximum segment voltage level		–	5.0	–	V
I_{ibHM}	input bias current		–	–	0.1	µA
TIME CONSTANT CONTROL TAUHM (PIN 22); see Figs 5, 6 and 7						
I_{ibTHM}	input bias current		–	–	0.1	µA
$V_{THM(l)}$	control voltage lower limit		–	1.0	–	V
$V_{THM(h)}$	control voltage upper limit		–	2.0	–	V
MISCOUNT DETECTION						
$Q_{mc(d)}$	miscount detection level		–	5	–	%
$t_{p(mc)}$	miscount propagation delay	20% step	–	25	–	ns
$t_{o(mc)}$	miscount detection on-time for each event		0.31	0.36	0.41	µs
$t_{Y(mc)}$	mismatch propagation and luminance delay		–	–	20	ns
$Q_{mc(aW)}$	miscount activation level at white	no miscount	–	90	–	%
$Q_{mc(dW)}$	miscount de-activation level at white	miscount	–	87	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Processing of measured histogram values						
ADAPTIVE GAMMA CONTROL RANGE						
$G_{adg(min)}$	minimum gain for HM1		–	1	–	
$G_{adg(max)}$	maximum gain for HM1		–	3	–	
ADAPTIVE GAMMA SETTING ADGAM (PIN 4); note 3; see Fig.8						
$V_{adg(l)}$	control voltage lower limit		–	1.75	–	V
$V_{adg(h)}$	control voltage upper limit		–	3.25	–	V
I_{ibADG}	input bias current		–	–	0.1	µA
$G_{adp(min)}$	minimum gain for HM1	no offset; $G_{VAR} = 1$	–	1	–	
$G_{adp(max)}$	maximum gain for HM1	no offset; $G_{VAR} = 1$	–	3	–	
ADAPTIVE GAMMA BY BLACK OFFSET						
$G_{adb(min)}$	minimum gain for HM1	no offset; $G_{VAR} = 1$	–	1	–	
$G_{adb(max)}$	maximum gain for HM1	maximum offset; $G_{VAR} = 1$	–	2.5	–	
WHITE-POINT STRETCH						
G_{wp}	maximum gain luminance for white stretch	HM-pattern = 01103: $G_{nl} = 1$	–	1.09	–	
Non-linear amplifier						
NON-LINEAR GAIN SET BY HMx (PINS 16 TO 20)						
$Q_{nl(b)}$	segment bleeder accuracy		–	–	2	%
$G_{nl(min)}$	minimum gain segment	HM-pattern = 31100: $G_{nl} = 1$	–	0.36	–	
$G_{nl(max)}$	maximum gain segment	HM-pattern = 31100: $G_{nl} = 1$	–	2.28	–	
NON-LINEARITY SETTING AMPNLA (PIN 3); note 3						
$V_{nl(l)}$	control voltage lower limit		–	1.75	–	V
$V_{nl(h)}$	control voltage upper limit		–	3.25	–	V
$I_{ib(nl)}$	input bias current		–	–	0.1	µA
DYNAMICS						
$t_{d(nl)}$	delay between linear and non-linear path		–	–	20	ns
Variable gamma						
VARIABLE GAMMA CONTROL RANGE						
$G_{VAR(min)}$	minimum variable gamma setting		–	0.5	–	
$G_{VAR(max)}$	maximum variable gamma setting		–	1.5	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VARIABLE GAMMA SETTING VARGAM (PIN 2); note 3						
$V_{VAR(l)}$	control voltage lower limit		–	1.75	–	V
$V_{VAR(h)}$	control voltage upper limit		–	3.25	–	V
$V_{VAR(lt)}$	control voltage for linear transfer		–	2.5	–	V
I_{ibVAR}	input bias current		–	–	0.1	µA
Colour difference processing						
COLOUR DIFFERENCE INPUTS UIN AND VIN (PINS 5 AND 7)						
$V_{i(UIN)}$	input voltage		1.8	–	–	V
$V_{i(VIN)}$	input voltage		1.8	–	–	V
I_{ib}	input bias current (pins 5 and 7)		–	–	0.1	µA
$V_{i(cl)}$	input voltage level during clamping		–	1.5	–	V
COLOUR DIFFERENCE OUTPUTS (PINS 28 AND 26)						
ΔV_{o28}	output voltage range with respect to the input (pin 28)		150	–	–	%
ΔV_{o26}	output voltage range with respect to the input (pin 26)		150	–	–	%
$V_{o(cl)}$	output voltage level during clamping		–	2.3	–	V
E_{off}	offset error	transparent	–	–	1	%
E_G	gain error	transparent	–	–	5	%
B	bandwidth	transparent	20	30	–	MHz
Timing						
HORIZONTAL WINDOW GENERATION						
fh	line frequency		15	–	16	kHz
Default window setting (with respect to start BK/CLP pulse)						
$t_{dh(ws)}$	default start window		–	$^{6.5}/_{64fh}$	–	
$t_{dhd(wp)}$	default window stop		–	$^{54.5}/_{64fh}$	–	
User window generation with I²C-bus (with respect to start BK/CLP pulse)						
$t_{hws(min)}$	minimum start window		–	$^{4.5}/_{64fh}$	–	
$t_{hws(max)}$	maximum start window		–	$^{19.5}/_{64fh}$	–	
$t_{hwp(min)}$	minimum window stop		–	$^{26.5}/_{64fh}$	–	
$t_{hwp(max)}$	maximum window stop		–	$^{56.5}/_{64fh}$	–	
VERTICAL WINDOW GENERATION						
fv	vertical frequency		45	–	65	Hz
Default window setting (start event with respect to start detected field blanking, stop event with respect to start event)						
t_{dvws}	default window start		–	64	–	lines
t_{dvdwp}	default window stop		–	161	–	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
User window generation with I²C-bus						
$t_{vsw(min)}$	minimum window start		–	10	–	lines
$t_{vsw(max)}$	maximum window start		–	100	–	lines
$t_{vwp(min)}$	minimum window stop		–	121	–	lines
$t_{vwp(max)}$	maximum window stop		–	271	–	lines
Default window select DWS; (pin 1): note 2						
$V_{isc(DWS)}$	voltage input level for window by SC blanking		–	–	1.5	V
$V_{id(DWS)}$	voltage input level for default window		3.5	–	5.5	V
I_{ibDWS}	input bias current	$V_{DWS} = V_{DDA}$	–	–	10	µA
Sandcastle input SC; (pin 10)						
$V_{i(SC)}$	voltage input level	no blanking; no clamp	–	0	1.0	V
		with blanking; no clamp	1.2	1.5	1.8	V
		with blanking and clamp	3.1	3.5	3.9	V
$t_{i(sw)}$	input sync width	no vertical sync	–	–	15	µs
		with vertical sync	35	–	–	µs
CLP PULSE WIDTH RESTORATION						
$t_{d(clp)}$	internal CLP pulse width difference		–	–100	–	ns
I²C-bus specification						
ADDRESS SELECT ADR (PIN 32)						
V_{iADR}	input voltage level	A0 = 0	–	–	1.5	V
		A1 = 1	3.5	–	5.5	V
I_{ibADR}	input bias current		–	–	0.1	µA
TEST PINS TM AND DT (PINS 29 AND 27)						
$V_{i(test)}$	input voltage level		–	–	0.5	V
Overall output performance						
$t_{d(YUV)}$	delay from input to output of YUV	transparent	–	50	100	ns
$t_{dm(YUV)}$	delay of matching YUV	transparent	–	10	20	ns
$\alpha_{w(YUV)}$	crosstalk from window	any channel	–	–	–60	dB

Notes

1. Input amplitude values greater than the minimum specified range are still processed. However, the gain will slowly saturate. Amplitudes up to +4 dB are permitted without significant clipping.
2. This select is valid provided the sleep mode bit is not set.
3. This control is valid provided the sleep mode bit is not set.

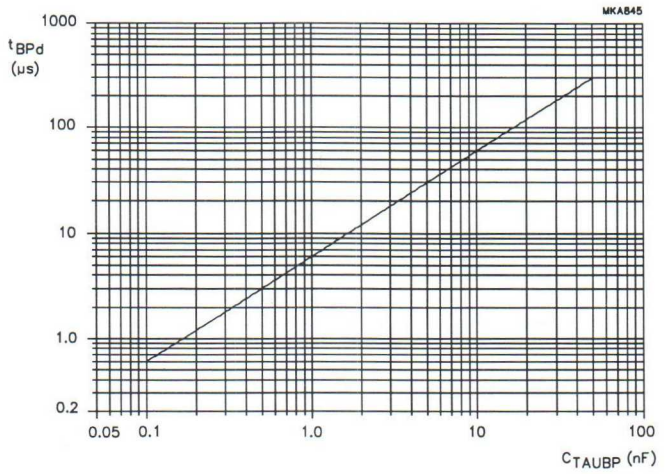
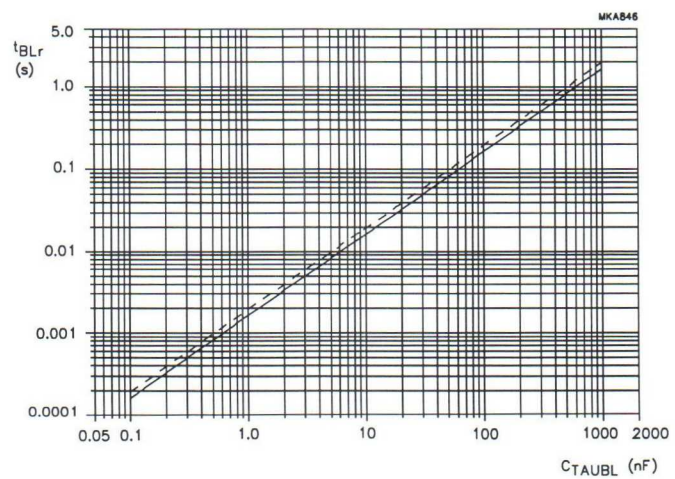
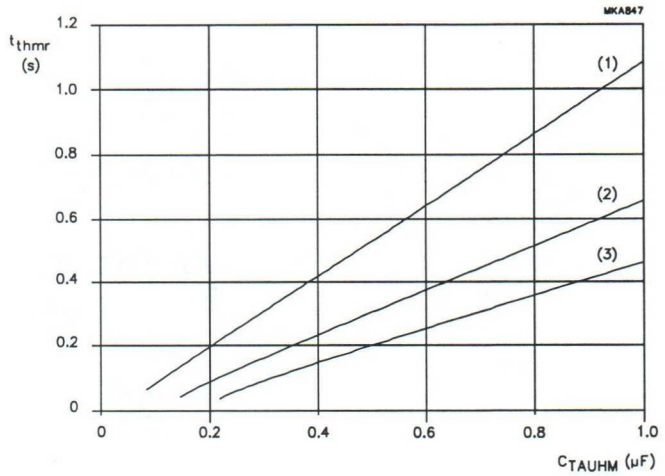


Fig.3 Black occurrence detection time constant as a function of C_{TAUBP}.



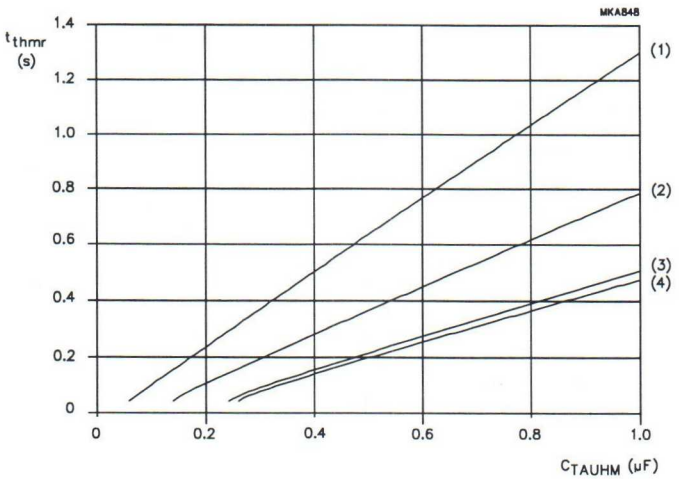
The dashed line = 625 lines/frame.
The full line = 525 lines/frame.

Fig.4 Response time constant black level loop as a function of C_{TAUBL}.



(1) Minimum user window.
(2) Default window.
(3) Maximum user window, window by sandcastle blanking.
$R_{mc} = 1$.
$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.
Where:
t_{hw} = horizontal window width (µs).
N_{vw} = vertical window height (lines).
R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.5 Response speed of average histogram amplitude control loop as a function of C_{TAUHM} at 60 Hz field-rate.



(1) Minimum user window.
(2) Default window.
(3) Maximum user window.
(4) window by sandcastle blanking.

$R_{mc} = 1$.

$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.

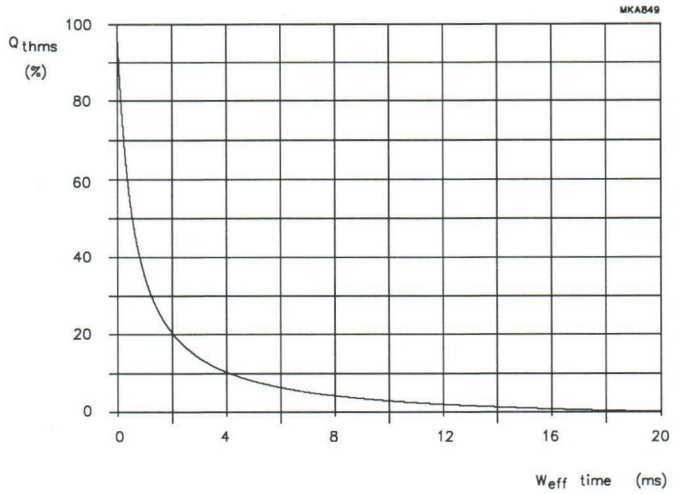
Where:

t_{hw} = horizontal window width (µs).

N_{vw} = vertical window height (lines).

R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.6 Response speed of average histogram amplitude control loop as a function of C_{TAUHM} at 50 Hz field-rate.



$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.

Where:

t_{hw} = horizontal window width (µs).

N_{vw} = vertical window height (lines).

R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.7 Static error on average histogram amplitude (pin TAUHM) as a function of effective histogram measuring time in a field.

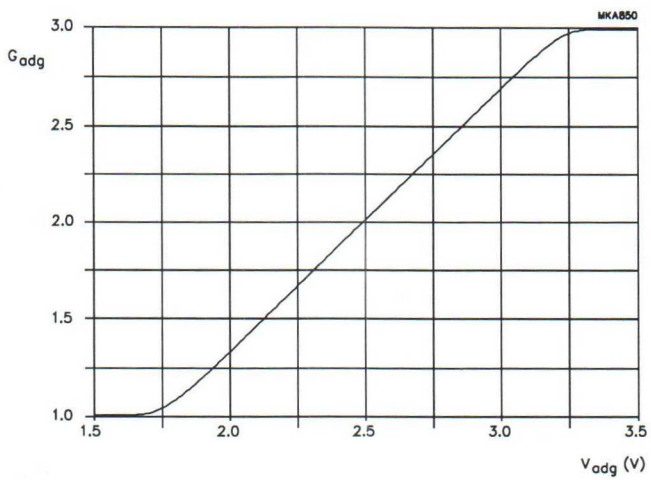


Fig.8 Adaptive gamma gain setting as a function of ADGAM setting in sleep mode.

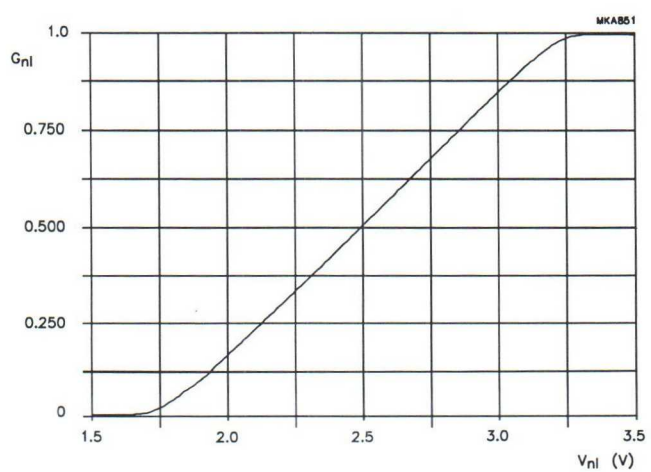


Fig.9 Non-linear amplifier non-linearity setting as a function of AMPNLA setting in sleep mode.

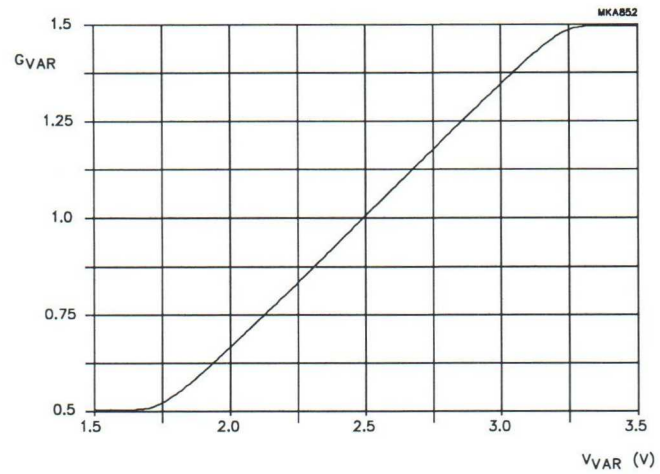


Fig.10 Variable gamma setting as a function of VARGAM setting in sleep mode.

APPLICATION INFORMATION (BUS-MODE)

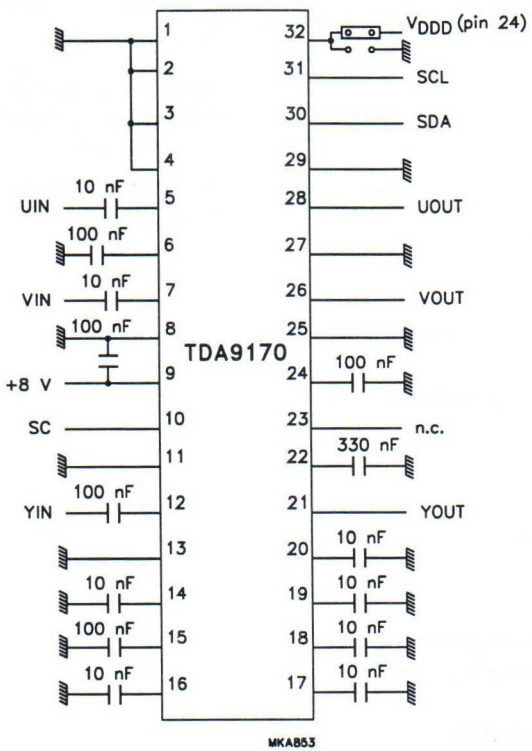


Fig.11 Application diagram.

Audio FM processor for VHS hi-fi audio TDA9610H

FEATURES

- Integrated High Frequency (HF) low-pass filter (LPF) and summator
- Low-noise Phase-Locked Loop (PLL) FM (de)modulator
- Low-distortion sample-and-hold switching noise suppressor
- Integrated audio low-pass filter
- 4 stereo input selectors (left [L] and right [R] channel):
  - EXT1L and EXT1R
  - EXT2L and EXT2R
  - CINL and CINR
  - TUNL and TUNR
- Additional mono inputs for linear audio: EXN1 and EXN2
- DC output for VU meter drive
- Direct headphone drive
- Linear input/linear output
- Modulator output with overload Automatic Gain Control (AGC)
- RAF (Record Audio FM) for head amplifier control
- Power-down mode facility
- I²C-bus control of:
  - line input volume
  - headphone output volume
  - input/output selector
  - PAL/NTSC mode
- E-E performance (record + playback):
  - Total Harmonic Distortion (THD): 0.05% (–8 dBV, 1 kHz)
  - linearity error: 0.1 dB (–88 dBV)
  - noise: –93 dBV (20 Hz to 20 kHz).

GENERAL DESCRIPTION

The TDA9610H is a dual audio FM processing IC for VHS hi-fi audio, digitally controlled via the I²C-bus. The FM (de)modulator and peak noise reduction functions are highly integrated, resulting in few external components and adjustments.

In addition special functions for audio editing, mixing and dubbing have been implemented.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9610H	QFP64[1]	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

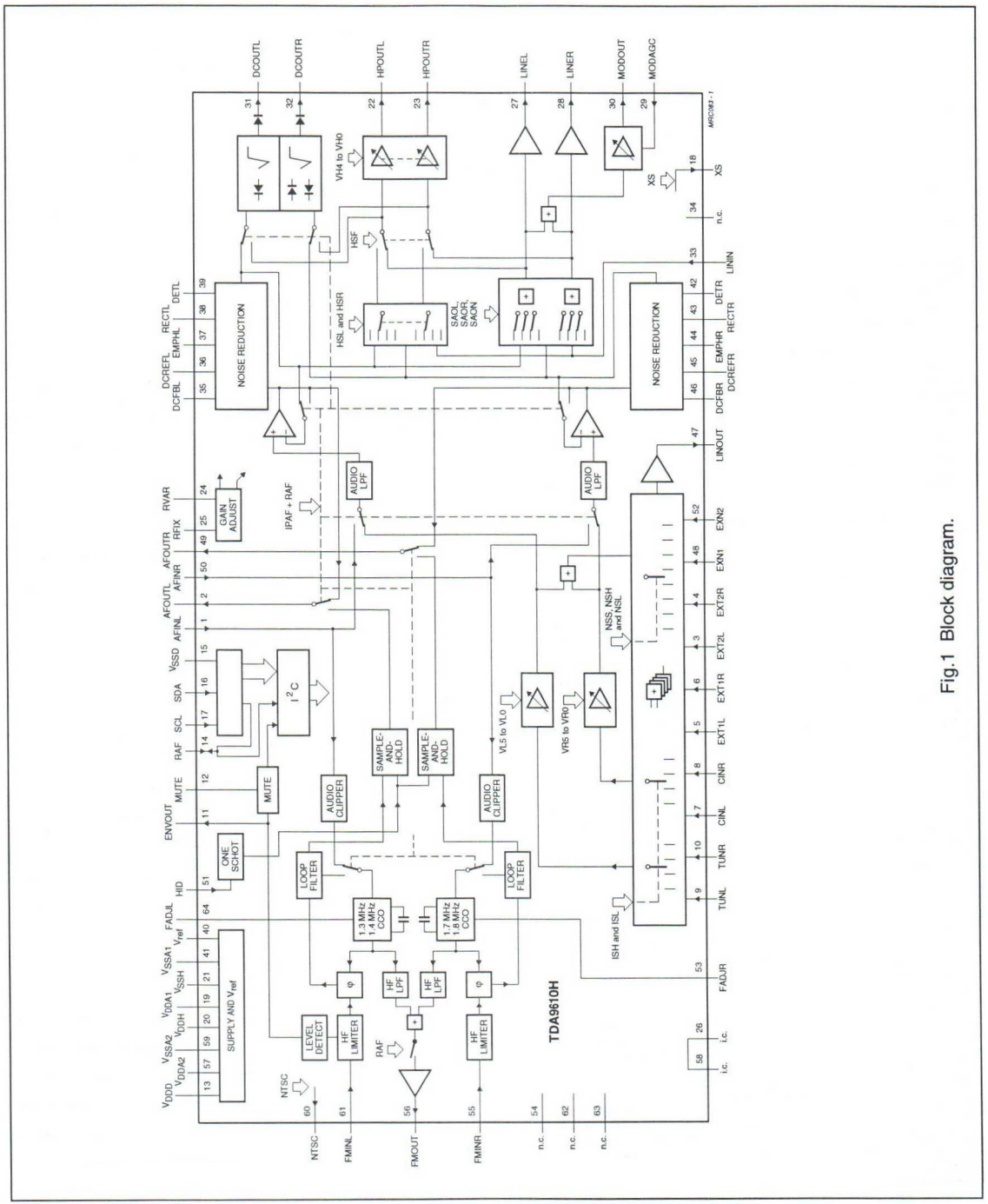


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AFINL	1	audio input for either audio clipper (record) or noise reduction (playback) of left channel
AFOUTL	2	audio output from either sample-and-hold (playback) or noise reduction (record and loop-through) of left channel
EXT2L	3	input selector for left channel
EXT2R	4	input selector for right channel
EXT1L	5	input selector for left channel
EXT1R	6	input selector for right channel
CINL	7	input selector for left channel
CINR	8	input selector for right channel
TUNL	9	input selector for left channel
TUNR	10	input selector for right channel
ENVOUT	11	level detector output; external capacitor required for filtering
MUTE	12	mute timing; external capacitor required for timing playback mute
V_{DDD}	13	digital supply voltage (+5 V)
RAF	14	overrule the I^2C-bit RAF input or record/playback switch drive output for head amplifier control
V_{SSD}	15	I^2C-bus digital ground
SDA	16	I^2C-bus data input
SCL	17	I^2C-bus clock input
XS	18	auxiliary switch; digital output controlled by I^2C-bit XS
V_{DDA1}	19	analog supply voltage 1 (+12 V)
V_{DDH}	20	headphone supply voltage (+12 V)
V_{SSH}	21	headphone ground
HPOUTL	22	headphone drive output left
HPOUTR	23	headphone drive output right
RVAR	24	gain adjustment of noise reduction by means of a resistor to ground
RFIX	25	fixed bias current generation circuit by using an external 100 kΩ resistor to ground
i.c.	26	pin internally connected to die pad; preferably connected to ground
LINEL	27	line output left
LINER	28	line output right
MODAGC	29	RF modulator AGC-time constant
MODOUT	30	RF modulator drive output
DCOUTL	31	VU meter drive output left
DCOUTR	32	VU meter drive output right
LININ	33	linear input
n.c.	34	not connected
DCFBL	35	DC feedback left
DCREFL	36	DC reference left
EMPHL	37	total emphasis left (20 to 240 μs)

SYMBOL	PIN	DESCRIPTION
RECTL	38	rectifier DC decoupling left
DETL	39	attack/recovery timing left
V_{ref}	40	noise filtering of 3.8 V reference voltage; external capacitor required for filtering
V_{SSA1}	41	analog ground for LF circuits
DETR	42	attack/recovery timing right
RECTR	43	rectifier DC decoupling right
EMPHR	44	total emphasis right (20 to 240 µs)
DCREFR	45	DC reference right
DCFBR	46	DC feedback left
LINOUT	47	linear output
EXN1	48	EXN input (external normal input); mono input selectable to linear output
AFOUTR	49	audio output from either sample-and-hold (playback) or noise reduction (record and loop-through) of right channel
AFINR	50	audio input for either audio clipper (record) or noise reduction (playback) of right channel
HID	51	head identification pulse input for sample-and-hold circuits
EXN2	52	EXN input (external normal input); mono input selectable to linear output
FADJR	53	frequency adjustment of right channel oscillator by means of a variable resistor
n.c.	54	not connected; preferably connected to ground
FMINR	55	1.7 to 1.8 MHz input for limiter
FMOUT	56	FM output
V_{DDA2}	57	analog supply voltage (+5 V)
i.c.	58	pin internally connected to die pad; preferably connected to ground
V_{SSA2}	59	analog ground for HF circuits
NTSC	60	digital output controlled by I^2C-bit NTSC
FMINL	61	1.3 to 1.4 MHz input for limiter
n.c.	62	not connected; preferably connected to ground
n.c.	63	not connected; preferably connected to ground
FADJL	64	frequency adjustment of left channel oscillator by means of a variable resistor

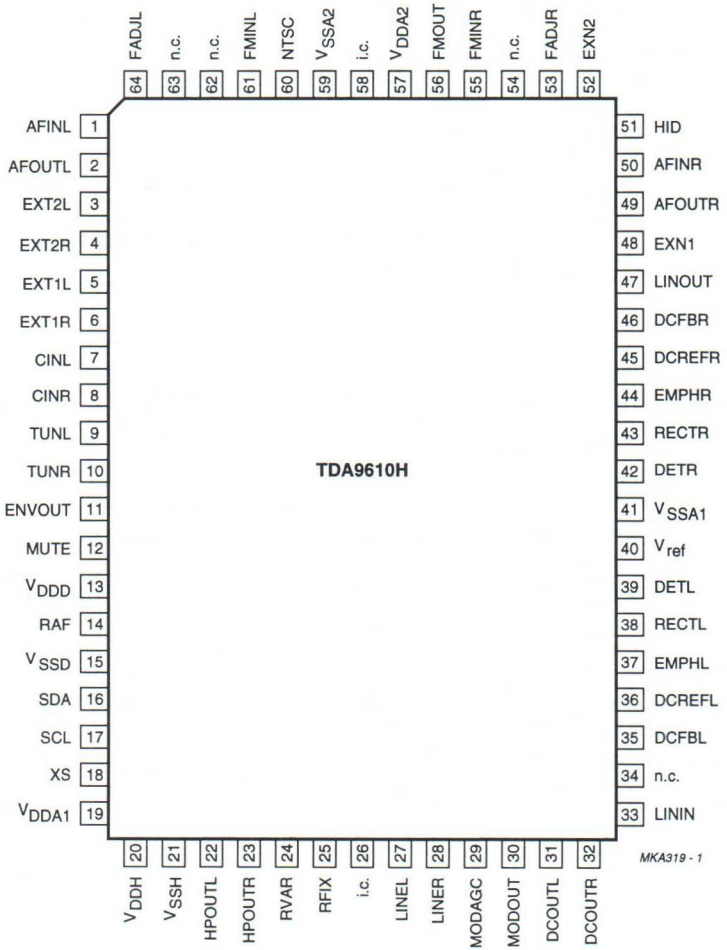


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The IC is intended for use within the audio FM system of VHS video recorders. Three modes of operation can be distinguished:

- Record mode
- Playback mode
- Loop-through mode.

Switching and control of the three modes is done by the I^2C-bus.

Record mode

The audio signal, selected from the four stereo audio inputs (EXT1L, EXT1R, EXT2L, EXT2R, CINL, CINR, TUNL and TUNR), is fed to the volume control stage (separate for left [L] and right [R]). The information for LINOUT is, after summing of L and R, derived from either one of the four stereo inputs or the volume control output or one of the mono inputs (EXN1 and EXN2). After the Low-Pass Filter (LPF) and signal compression in the noise reduction (NR) and filter block the audio signal is available at AFOUTL and AFOUTR. The compressed signal is now FM modulated on a RF carrier in the PLL block. After low-pass filtering and summation of both RF carriers (L and R) the signal is available at FMOUT.

The output select block offers the possibility to choose eight different audio signal modes:

1. Stereo.
2. Left.
3. Right.
4. Mono.
5. Normal.
6. Mixed stereo (stereo + LININ).
7. Mixed left (left + LININ).
8. Mixed right (right + LININ).

These audio signal modes are selectable for the output stages LINEL, LINER and MODOUT. The standard audio output is LINEL and LINER, e.g. for SCART output. MODOUT is a mono audio output, with an overload-protecting AGC, to drive an external RF modulator.

The headphone select block offers the possibility to choose either the output select signal or four independent audio signal modes (stereo, left, right and normal) for the output stages HPOUTL and HPOUTR.
HPOUTL and HPOUTR, with common volume control for L and R, is suitable for direct headphone drive.

DCOUTL and DCOUTR are intended for VU meter drive. It is connected to the selected stereo audio input after the volume control block. The output signal at DCOUTL and DCOUTR is proportional to the square root of the recorded audio signal (see Fig.3).

Playback mode

The two FM modulated RF carriers, present at the two FMINL and FMINR inputs after being band-pass filtered, are demodulated in the PLL block. The LF audio signal is fed through a sample-and-hold circuit to suppress head-switching noise. The demodulated audio signal is available at AFOUTL and AFOUTR. The audio signal is low-pass filtered and expanded in the noise reduction (NR) and filter block. The resulting audio signal is available after the output and headphone select blocks for all four output stages (LINEL, LINER, MODOUT, HPOUTL, HPOUTR, DCOUTL and DCOUTR). The functionality of the output and headphone select blocks is identical to the record mode. During playback DCOUTL and DCOUTR are connected to the headphone select block.

The functionality of the input and normal select blocks is also identical to record mode (see Fig.3), which offers the possibility to control (other) audio signals independently for LINOUT (see Fig.4).

Loop-through mode

This mode is similar to the record mode (see Fig.3), except for the FMOUT pin, which is inactive, and the RAF output which is active LOW (see Fig.5).

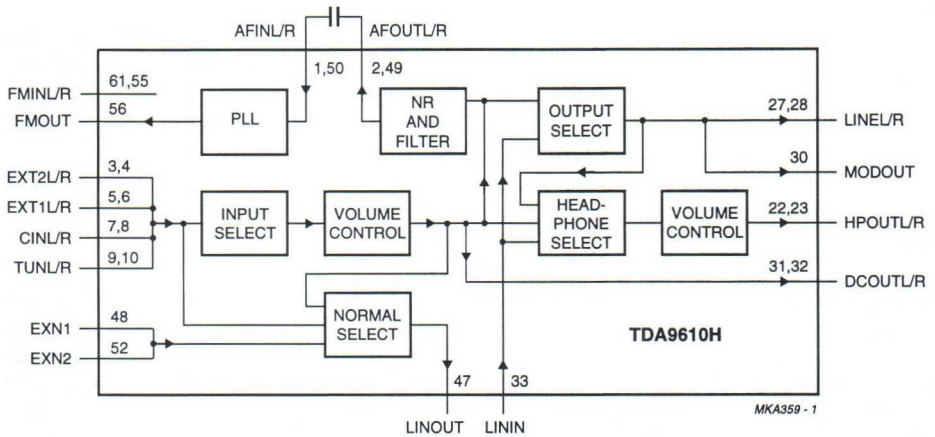


Fig.3 Record mode.

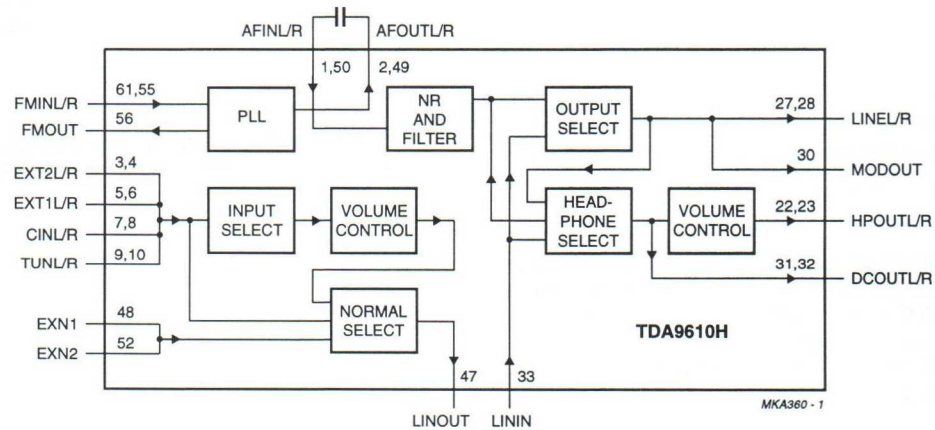


Fig.4 Playback mode.

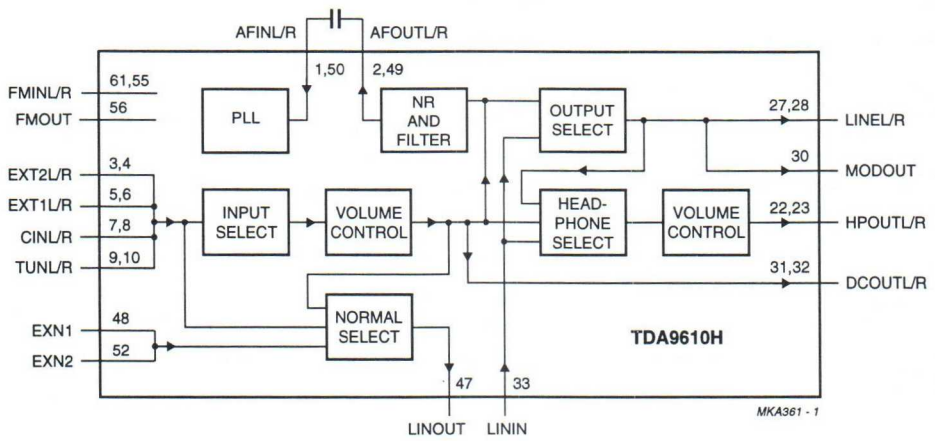


Fig.5 Loop-through mode.

I²C-bus

Bus specification in accordance with I²C-bus specification. Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

The address and data bytes of the TDA9610H are shown in Table 1.

Table 1 TDA9610H address and data bytes

NAME	ADDRESS							
Slave address (B8)	1	0	1	1	1	0	0	0
Control byte(1)	0	0	0	IPAF	RAF	NTSC	PAFM	MUTE
Select byte(2)	0	0	1	SAOL	SAOR	SAON	HSF	NSS
Input byte(3)	0	1	1	0	ISH	ISL	NSH	NSL
Function byte(4)	0	1	1	1	HSL	HSR	XS	TEST
Record volume left byte(5)	1	0	VL5	VL4	VL3	VL2	VL1	VL0
Record volume right byte(5)	1	1	VR5	VR4	VR3	VR2	VR1	VR0
Headphone volume byte(6)	0	1	0	VH4	VH3	VH2	VH1	VH0

Notes

1. See Section "Control byte".
2. See Section "Select byte".
3. See Section "Input byte".
4. See Section "Function byte".
5. See Section "Record volume left and right byte".
6. See Section "Headphone volume byte".

Power-On Reset (POR); derived from digital supply V_{DDD}

In the data byte descriptions [por] indicates the mode after POR.

The status of the data bytes after POR is shown in Table 2.

Table 2 TDA9610H address and data bytes after POR

NAME	ADDRESS							
Control byte(1)	0	0	0	1	0	0	0	1
Select byte(2)	0	0	1	1	1	0	0	0
Input byte(3)	0	1	1	0	0	0	0	0
Function byte(4)	0	1	1	1	0	0	0	0
Record volume left byte(5)	1	0	1	1	0	0	0	1
Record volume right byte(5)	1	1	1	1	0	0	0	1
Headphone volume byte(6)	0	1	0	1	0	1	1	1

Notes

1. See Section "Control byte".
2. See Section "Select byte".
3. See Section "Input byte".
4. See Section "Function byte".
5. See Section "Record volume left and right byte".
6. See Section "Headphone volume byte".

Control byte

Table 3 Bits of control byte

BIT	DESCRIPTION
IPAF	Inverse Playback Audio FM; see Table 4
RAF	Record Audio FM; see Table 4
NTSC	National Television Standards Committee; television standard; see Table 5
PAFM	Playback Audio FM Mute; see Table 6
MUTE	Mute; see Table 7

Table 4 Bits IPAF and RAF

IPAF	RAF[1]	MODE	DESCRIPTION
0	0	playback	NR and modem in playback mode
1	0	loop-through	NR in record mode; modem not active [por]
0	1	record[2]	NR and modem in record mode
1	1	record[2]	NR and modem in record mode

Notes

1. The RAF bit can be overruled externally by applying a low-ohmic voltage to the RAF I/O (pin 14) either logic 0 or logic 1 (0 or +5 V). The actual mode of the IC is determined by the level measured at this pin.
2. The two record modes are equal, only differing in their reaction to forcing RAF LOW at the RAF I/O pin; the status of the IPAF bit determines whether the IC is switched to the playback or loop-through mode.

Table 5 Bit NTSC

NTSC	MODE	DESCRIPTION
0	PAL	modem set to PAL carrier frequencies [por]
1	NTSC	modem set to NTSC carrier frequencies

Table 6 Bit PAFM

PAFM[1]	MODE	DESCRIPTION
0	–	
1	PB mute	the signal from the modem is muted in playback mode

Note

1. Bit PAFM has the same effect as the internally generated mute signal from the modem part when no FM carrier is detected during playback mode. If one (or both) of these signals is HIGH, the audio signal coming from the modem is muted.

Table 7 Bit MUTE

MUTE	MODE	DESCRIPTION
0	–	
1	full mute	all audio outputs are muted [por]

Select byte

Table 8 Bits of select byte

BIT	DESCRIPTION
SAOL	Select Audio Output Left; see Table 9
SAOR	Select Audio Output Right; see Table 9
SAON	Select Audio Output Normal; see Table 9
HSF	Headphone Select Function; see Table 10
NSS	Normal Special Select; see Table 11

Table 9 Bits SAOL, SAOR and SAON; note 1

SAOL	SAOR	SAON	MODE	DESCRIPTION
1	1	0	stereo	left at LINEL, right at LINER [por]
1	0	0	left	left at both LINEL and LINER
0	1	0	right	right at both LINEL and LINER
0	0	0	mono	left + right added at both LINEL and LINER (hi-fi mono)
1	1	1	mixed stereo	left + normal added at LINEL, right + normal added at LINER
1	0	1	mixed left	left + normal added at both LINEL and LINER
0	1	1	mixed right	right + normal added at both LINEL and LINER
0	0	1	normal	normal (is linear audio) at both LINEL and LINER

Note

1. The bits SAOL, SAOR and SAON provide eight output select functions, left and right are the left and right hi-fi channels, normal is the conventional audio channel, linear audio input (LININ; pin 33).

Table 10 Bit HSF; note 1

HSF	MODE	DESCRIPTION
0	–	headphone output signals identical to line outputs LINEL and LINER [por]
1	headphone select	headphone output signals independently selectable

Note

1. Normally the headphone outputs carry the same audio signal as present at the line outputs (LINEL and LINER), so the signal is selectable by means of the bits SAOL, SAOR and SAON. However when bit HSF is set HIGH, the headphone output has its own output select function switchable with bits HSL and HSR to stereo, left, right and normal (see Section "Function byte").

Table 11 Bit NSS; note 1

NSS	MODE	DESCRIPTION
0	–	signal at LINOUT is the mono version of selected stereo line input pair [por]
1	normal special select	special output signals selectable for LINOUT

Note

1. Normally the bits NSH and NSL select one of the four possible stereo line inputs (TUNL/R, CINL/R, EXT1L/R, EXT2L/R) as the source signal for linear out. Left and right channels of the selected input are added to give a mono signal as output.

   When bit NSS is set HIGH, four special input selects can be made in combination with the same bits NSH and NSL; volume controlled, tuner left (TUNL), EXN1 and EXN2 (see Section "Input byte").

Input byte

Table 12 Bits of input byte

BIT	DESCRIPTION
ISH	Input Select HIGH; see Table 13
ISL	Input Select LOW; see Table 13
NSH	Normal Select HIGH; see Table 14
NSL	Normal Select LOW; see Table 14

Table 13 Bits ISH and ISL; note 1

ISH	ISL	MODE	DESCRIPTION
0	0	Tuner	TUNL and TUNR selected (as hi-fi stereo input source) [por]
0	1	Cinch	CINL and CINR selected
1	0	Ext1	EXT1L and EXT1R (e.g. Scart input) selected
1	1	Ext2	EXT2L and EXT2R selected

Note

1. With bits ISH and ISL the stereo input signal is selected which is fed to the hi-fi processing. One out of four stereo sources can be selected. The terms: Tuner, Cinch, Ext1 and Ext2 are used for describing purposes only, technically all four inputs are equal (except for the fact that tuner left (TUNL, pin 6) is also selectable by Normal Select).

Table 14 Bits NSH, NSL and NSS; note 1

NSH	NSL	NSS[2]	MODE	DESCRIPTION
0	0	0	Tuner	TUNL and TUNR selected (as normal audio input source) [por]
0	1	0	Cinch	CINL and CINR selected
1	0	0	Ext1	EXT1L and EXT1R selected
1	1	0	Ext2	EXT2L and EXT2R selected
0	0	1	Volume	hi-fi input source selected; taken after record volume control
0	1	1	Exn1	additional mono input (EXN1, pin 48) selected
1	0	1	Tuner left	only TUNL selected (e.g. dual language)
1	1	1	Exn2	additional mono input (EXN2, pin 52) selected

Notes

1. With bits NSH and NSL in combination with bit NSS the input signal is selected which is fed out at pin 47 (LINOUT). With bit NSS set LOW a selection can be made between the four stereo line inputs (like the hi-fi input select). With bit NSS set HIGH, bits NSH and NSL make a selection between four special select functions.

   When a stereo input source is selected, both channels are added to obtain a mono output signal, then the output signal at LINOUT is equal to: $\frac{(L + R)}{2}$

   In the Volume mode the output signal is equal to: $\frac{(L \times \text{Volume Left} + R \times \text{Volume Right})}{2}$

   Note that for the Volume mode the hi-fi input select (ISH and ISL) determines the used input source.
2. NSS from select byte.

Function byte

Table 15 Bits of function byte

BIT	DESCRIPTION
HSL	Headphone Select Left; see Table 16
HSR	Headphone Select Right; see Table 16
XS	auxiliary Switch; see Table 17
TEST	Test; see Table 18

Table 16 Bits HSL, HSR and HSF; note 1

HSL	HSR	HSF(2)	MODE	DESCRIPTION
1	1	0	outsel	headphone output signal identical to LINEL and LINER
1	0	0	outsel	headphone output signal identical to LINEL and LINER
0	1	0	outsel	headphone output signal identical to LINEL and LINER
0	0	0	outsel	headphone output signal identical to LINEL and LINER [por]
1	1	1	stereo	left at HPOUTL, right at HPOUTR
1	0	1	left	left at both HPOUTL and HPOUTR
0	1	1	right	right at both HPOUTL and HPOUTR
0	0	1	normal	normal (is linear audio) at both HPOUTL and HPOUTR

Notes

1. Normally (bit HSF set LOW) the headphone outputs carry the same audio signal as present at the line outputs (LINEL and LINER), so the signal is selectable by means of the bits SAOL, SAOR and SAON. However, when bit HSF is set HIGH the headphone output has its own output select function switchable with bits HSL and HSR.
   a) These special headphone selections are also active for the VU meter drive during playback.
2. HSF from select byte.

Table 17 Bit XS

XS	MODE	DESCRIPTION
0	–	XS output LOW [por]
1	XS	XS output HIGH

Table 18 Bits TEST, HSL, HSR and XS; note 1

TEST[2]	HSL	HSR	XS	MODE	DESCRIPTION
0	0	0	0	–	[por]
0	X	X	X	–	
1	0	0	X	–	
1	1	0	0	VCO test L	in record mode; only 1.4 or 1.3 MHz at output
1	0	1	0	VCO test R	in record mode; only 1.8 or 1.7 MHz at output
1	1	1	0	Test	not for application
1	1	0	1	Test	not for application
1	0	1	1	Test	not for application
1	1	1	1	Test	not for application

Notes

1. X = don't care.
2. With TEST bit set HIGH, the IC can be switched between several special modes for testing and adjustment purposes, by means of bits HSL and HSR.

Record volume left and right byte

Table 19 Record volume left/right byte; note 1

VL5	VL4	VL3	VL2	VL1	VL0	MUTE[2]	MODE
VR5	VR4	VR3	VR2	VR1	VR0		
1	1	0	0	0	1	1	mute [por]
X	X	X	X	X	X	1	mute
0	0	0	0	0	0	0	mute
0	0	0	0	0	1	0	–48 dB
0	0	0	0	1	0	0	–47 dB
0	0	0	0	1	1	0	–46 dB
0	0	0	1	0	0	0	–45 dB
0	0	0	1	0	1	0	–44 dB
0	0	0	1	1	0	0	–43 dB
0	0	0	1	1	1	0	–42 dB
0	0	1	0	0	0	0	–41 dB
0	0	1	0	0	1	0	–40 dB
0	0	1	0	1	0	0	–39 dB
0	0	1	0	1	1	0	–38 dB
0	0	1	1	0	0	0	–37 dB
0	0	1	1	0	1	0	–36 dB
0	0	1	1	1	0	0	–35 dB
0	0	1	1	1	1	0	–34 dB
0	1	0	0	0	0	0	–33 dB
0	1	0	0	0	1	0	–32 dB
0	1	0	0	1	0	0	–31 dB

VL5	VL4	VL3	VL2	VL1	VL0	MUTE[2]	MODE
VR5	VR4	VR3	VR2	VR1	VR0		
0	1	0	0	1	1	0	−30 dB
0	1	0	1	0	0	0	−29 dB
0	1	0	1	0	1	0	−28 dB
0	1	0	1	1	0	0	−27 dB
0	1	0	1	1	1	0	−26 dB
0	1	1	0	0	0	0	−25 dB
0	1	1	0	0	1	0	−24 dB
0	1	1	0	1	0	0	−23 dB
0	1	1	0	1	1	0	−22 dB
0	1	1	1	0	0	0	−21 dB
0	1	1	1	0	1	0	−20 dB
0	1	1	1	1	0	0	−19 dB
0	1	1	1	1	1	0	−18 dB
1	0	0	0	0	0	0	−17 dB
1	0	0	0	0	1	0	−16 dB
1	0	0	0	1	0	0	−15 dB
1	0	0	0	1	1	0	−14 dB
1	0	0	1	0	0	0	−13 dB
1	0	0	1	0	1	0	−12 dB
1	0	0	1	1	0	0	−11 dB
1	0	0	1	1	1	0	−10 dB
1	0	1	0	0	0	0	−9 dB
1	0	1	0	0	1	0	−8 dB
1	0	1	0	1	0	0	−7 dB
1	0	1	0	1	1	0	−6 dB
1	0	1	1	0	0	0	−5 dB
1	0	1	1	0	1	0	−4 dB
1	0	1	1	1	0	0	−3 dB
1	0	1	1	1	1	0	−2 dB
1	1	0	0	0	0	0	−1 dB
1	1	0	0	0	1	0	0 dB
1	1	0	0	1	0	0	1 dB
1	1	0	0	1	1	0	2 dB
1	1	0	1	0	0	0	3 dB
1	1	0	1	0	1	0	4 dB
1	1	0	1	1	0	0	5 dB
1	1	0	1	1	1	0	6 dB
1	1	1	0	0	0	0	7 dB
1	1	1	0	0	1	0	8 dB

VL5	VL4	VL3	VL2	VL1	VL0	MUTE(2)	MODE
VR5	VR4	VR3	VR2	VR1	VR0		
1	1	1	0	1	0	0	9 dB
1	1	1	0	1	1	0	10 dB
1	1	1	1	0	0	0	11 dB
1	1	1	1	0	1	0	12 dB
1	1	1	1	1	0	0	13 dB
1	1	1	1	1	1	0	14 dB

Notes

1. X = don't care.
2. MUTE from control byte.

Headphone volume byte

Table 20 Headphone volume byte

VH4	VH3	VH2	VH1	VH0	MODE
0	0	0	0	0	mute
0	0	0	0	1	–44 dB
0	0	0	1	0	–42 dB
0	0	0	1	1	–40 dB
0	0	1	0	0	–38 dB
0	0	1	0	1	–36 dB
0	0	1	1	0	–34 dB
0	0	1	1	1	–32 dB
0	1	0	0	0	–30 dB
0	1	0	0	1	–28 dB
0	1	0	1	0	–26 dB
0	1	0	1	1	–24 dB
0	1	1	0	0	–22 dB
0	1	1	0	1	–20 dB
0	1	1	1	0	–18 dB
0	1	1	1	1	–16 dB
1	0	0	0	0	–14 dB
1	0	0	0	1	–12 dB
1	0	0	1	0	–10 dB
1	0	0	1	1	–8 dB
1	0	1	0	0	–6 dB
1	0	1	0	1	–4 dB
1	0	1	1	0	–2 dB
1	0	1	1	1	0 dB(1)
1	1	0	0	0	2 dB
1	1	0	0	1	4 dB

VH4	VH3	VH2	VH1	VH0	MODE
1	1	0	1	0	6 dB
1	1	0	1	1	8 dB
1	1	1	0	0	10 dB
1	1	1	0	1	12 dB
1	1	1	1	0	14 dB
1	1	1	1	1	16 dB

Note

1. This is the situation after Power-On Reset (POR).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage	0	13.2	V
V_{DDA2}	analog supply voltage	0	5.5	V
V_{DDH}	headphone supply voltage	0	13.2	V
V_{DDD}	digital supply voltage	0	5.5	V
V_n	voltage on pins:			
	1, 3, 4, 5, 6, 7, 8, 9, 10, 39, 42, 48, 50 and 52	0	7.7	V
	11, 12, 56 and 60	0	V_{DDA2}	V
	14 and 18	0	V_{DDD}	V
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C

HANDLING

All pins are meeting the ESD requirements.

Remark: Pin 1 showed a higher sensitivity during the latch-up test and was not fully meeting the test limits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W

DC CHARACTERISTICS

V_{DDA1} = 12 V; V_{DDA2} = 5 V; f_{OUTR} = 1.8 MHz; f_{OUTL} = 1.4 MHz; NTSC = 0; f_m = 1 kHz; T_{amb} = 25 °C; all volume control levels set to 0 dB; measured in test circuit (see Fig.12); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltages						
V_{DDA1}	analog supply voltage; pin 19		10.5	12	13.2	V
V_{DDA2}	analog supply voltage; pin 57		4.75	5	5.25	V
V_{DDH}	headphone supply voltage; pin 20		10.5	12	13.2	V
V_{DDD}	digital supply voltage; pin 13		4.75	5	5.25	V
Supply currents						
I_{DDA1}	analog supply current; pin 19		–	37	46	mA
I_{DDA2}	analog supply current; pin 57	record or loop-through	–	7	9	mA
		playback	–	10	13	mA
I_{DDH}	headphone supply current; pin 20		–	3.5	4.5	mA
I_{DDD}	digital supply current; pin 13		–	0.5	2	mA
Input voltages						
V_I	DC input voltage; pins 1, 3, 4, 5, 6, 8, 9, 10, 33, 48, 50, 52		–	3.8	–	V
$V_{55,61}$	DC input voltage internally generated; pins 55 and 61		–	0	–	V
Output voltages						
V_O	DC output voltage:					
	pins 27 and 28		–	6	–	V
	pins 22 and 23		–	5.5	–	V
	pins 2, 30, 40, 49, 53 and 64		–	3.8	–	V
	pin 47		–	6	–	V
	pin 24		–	0.5	–	V
	pin 25		–	2.0	–	V
	pin 56	record mode	–	1.2	–	V
Head identification pulse input (HID; pin 51)						
V_{IH}	HIGH level input voltage		2.75	–	5.25	V
V_{IL}	LOW level input voltage		0	–	2.25	V
Auxiliary switch output (XS; pin 18)						
V_{OH}	HIGH level output voltage	I_L = –500 µA	V_{DDD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_L = 500 µA	–	–	0.5	V
Digital output (NTSC; pin 60)						
V_{OH}	HIGH level output voltage	I_L = –500 µA	V_{DDA2} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_L = 500 µA	–	–	0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/O RAF (pin 14); used as output						
V_{OH}	HIGH level output voltage	RAF = 1; I_L = –35 µA	V_{DDD} – 0.25	–	V_{DDD}	V
V_{OL}	LOW level output voltage	RAF = 0; I_L = 185 µA	0	–	0.4	V
I_{OH}	HIGH level output current (drive capability)	RAF = 1	–35	–	–	µA
I_{OL}	LOW level output current (drive capability)	RAF = 0	185	–	–	µA
I/O RAF (pin 14); used as input (output overruled)						
V_{IH}	HIGH level input voltage		3.5	–	V_{DDD}	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current	at V_{IH}	–	–	345	µA
I_{IL}	LOW level input current	at V_{IL}	–	–	–65	µA

AC CHARACTERISTICS

Record mode

Audio input signal –8 dBV from TUNL and TUNR (pins 9 and 10).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio inputs (EXT1L, EXT1R, EXT2L, EXT2R, CINL, CINR, TUNL, TUNR, EXN1 and EXN2; pins 3, 4, 5, 6, 7, 8, 9, 10, 48 and 52)						
R_i	input resistance		100	130	–	kΩ
V_{iAF}	audio input voltage		–	–	8	dBV
Linear input (LININ; pin 33); select mode: linear						
R_i	input resistance	V_i = –8 dBV; f = 1 kHz	50	75	100	kΩ
V_o	line output voltage	V_i = –8 dBV; f = 1 kHz	–9	–8	–7	dBV
Line outputs (LINEL and LINER; pins 27 and 28)						
V_o	output voltage		–9	–8	–7	dBV
R_o	output resistance		–	200	275	Ω
THD	total harmonic distortion		–	0.01	0.1	%
V_o	output voltage	THD = 1%; R_L = 5 kΩ; C_L = 2.2 nF; TUNL ≤ –3 dBV; TUNR ≤ –3 dBV; note 1	10	11	–	dBV
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–92	–88	dBV
α_{cb}	channel balance		–1	–	+1	dB
V_m	volume mute level		–	–100	–80	dBV
α_{ct}	crosstalk between channels	one channel driven	–	–88	–80	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{res}	frequency response with respect to 1 kHz; low-pass filter transfer	f_i = 20 kHz	–0.5	–	+0.5	dB
		f_i = 60 kHz	–	–9	–5	dB
α_{ct}	maximum audio input crosstalk	–8 dBV at a not selected stereo audio input	–	–85	–	dBV
VU meter drive (DCOUTL and DCOUTR; pins 31 and 32); square root of output voltage (see Fig.8)						
V_o	output voltage		1.6	1.8	2.0	V
R_o	output resistance		–	100	–	Ω
V_o	output voltage at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	V_{DDD} – 0.5	–	V_{DDD}	V
V_{oz}	output voltage for zero-level input		–	–	300	mV
RF modulator drive output; mono MODOUT; pin 30 (see Fig.9)						
V_o	output voltage		–10	–8	–6	dBV
R_o	output resistance		–	100	–	Ω
THD	total harmonic distortion		–	0.04	–	%
V_o	output voltage at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–7	–4	–1	dBV
THD	total harmonic distortion at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–	1	–	%
Linear output (LINOUT; pin 47); NSS = 0						
V_o	output voltage		–9	–8	–7	dBV
R_o	output resistance		–	200	–	Ω
THD	total harmonic distortion		–	0.01	–	%
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–93	–	dBV
V_o	output voltage	THD = 1%; R_L = 10 kΩ; TUNL ≤ –3 dBV; TUNR ≤ –3 dBV; NSS = 1; note 1	9	10	–	dBV
Headphone output (HPOUTL and HPOUTR; pins 22 and 23); headphone volume set to 0 dB						
V_o	output voltage		–9	–8	–7	dBV
R_o	output resistance		–	3	–	Ω
THD	total harmonic distortion		–	0.06	0.1	%
V_o	output voltage	THD = 1%; TUNL ≤ –3 dBV; TUNR ≤ –3 dBV; R_L = 250 Ω; note 1	9.5	10.5	–	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_n	noise level	f_i = 300 Hz to 20 kHz; tuner AC short-circuited	–	–90	–80	dBV
α_{ct}	crosstalk between channels	one channel driven	–	–90	–70	dBV
V_{mute}	headphone volume mute level		–	–90	–70	dBV
α_{cb}	channel balance		–1	–	+1	dB
Audio outputs (AFOUTL and AFOUTR; pins 2 and 49); audio output from noise reduction						
V_{oAF}	audio output voltage		–13	–11.5	–10	dBV
THD	total harmonic distortion		–	0.15	0.3	%
V_{oAF}	audio output voltage at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–3.5	–2	–0.5	dBV
THD	total harmonic distortion at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–	0.4	3	%
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–55	–52	dBV
α_{cb}	channel balance		–1	–	+1	dB
L	linearity	V_i = –8 to –68 dBV	28.5	30	31.5	dB
α_{cc}	channel crosstalk	one channel driven	–	–65	–50	dBV
t_{att}	attack time according VHS		–	5	–	ms
t_{rec}	recovery time according VHS		–	70	–	ms
V_{mute}	mute level	MUTE = 1	–	–52	–	dBV
	frequency response with respect to 1 kHz; output level	f_i = 300 Hz	–0.9	–0.2	+0.5	dB
		f_i = 10 kHz	2.9	3.9	4.9	dB
FM modulator (audio input from AFINL and AFINR; pins 1 and 50)						
THD	total harmonic distortion	Δf = 50 kHz	–	0.1	0.2	%
Δf	FM frequency deviation	V_{iAF} = –11.5 dBV	45	50	55	kHz
Δf_{max}	maximum FM frequency deviation		140	150	160	kHz
TC	temperature coefficient		–	±50	–	10^{-6}/K
R_{fa}	frequency adjust resistor	left channel	22	28	35	kΩ
		right channel	17	22	28	kΩ
f_{oR}	FM centre frequency right	NTSC = 1	–	1700	–	kHz
f_{oL}	FM centre frequency left	NTSC = 1	–	1300	–	kHz
Δf	FM frequency deviation	NTSC = 1; V_{iAF} = –11.5 dBV	45	50	55	kHz
HF output stage (FMOUT; pin 56)						
$V_{oR(p-p)}$	right output voltage (peak-to-peak value)	f_{oR} = 1.8 MHz; 1st harmonic	455	510	572	mV
$V_{oL(p-p)}$	left output voltage (peak-to-peak value)	f_{oL} = 1.4 MHz; 1st harmonic	152	170	190	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\frac{V_{oR}}{V_{oL}}$	ratio of output voltages		2.7	3	3.3	
α_{3rd}	3rd harmonic suppression		20	30	–	dB
R_o	output resistance		–	100	130	Ω

Note

1. Record volume control for left and right channel set to maximum (+14 dB). Headphone volume control at 0 dB.

Playback mode

Audio output signal from the FM (de)modulator at AFOUTL and AFOUTR (pins 2 and 49).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulator and limiter						
α_{AM}	AM rejection	V_{iHF} = 1 to 100 mV; m = 30%	–	–80	–	dBV
$V_{i(rms)}$	sensitivity; PLL locked (RMS value)	Δf = 150 kHz	–	–	0.6	mV
$V_{i\,max(rms)}$	maximum signal level (RMS value)		–	–	200	mV
THD	total harmonic distortion	Δf = 50 kHz	–	0.03	0.3	%
		Δf = 150 kHz	–	0.2	1	%
S/N	signal-to-noise ratio	V_{iHF} = 30 mV; Δf = 50 kHz	55	60	–	dB
V_{oAF}	AF output voltage	Δf = 50 kHz	–12.5	–11.5	–10.5	dBV
α_{ct}	crosstalk between channels	L to R; R to L	–	–90	–	dBV
Sample-and-hold (see Fig.10)						
t_h	hold pulse width		5	6	7	µs
d_{AF}	audio distortion	note 1	–	–	–76	dB
t_d	delay from HID pulse to hold pulse		–	0.15	–	µs
Mute timing (MUTE; pin 12)						
$V_{i(rms)}$	mute activation level (RMS value)		1.1	2.0	3.5	mV
t_{off}	switch-off duration	signal to no signal	–	15	–	ms
t_{on}	switch-on duration	no signal to signal	–	400	–	ms
Level detector output ENVOUT; pin 11 (see Fig.11)						
V_o	output voltage level	$V_{iHF(rms)}$ = 1 mV	–	1.5	–	V
		$V_{iHF(rms)}$ = 10 mV	–	3.1	–	V
		$V_{iHF(rms)}$ = 100 mV	–	4.5	–	V
R_o	output resistance		–	20	–	kΩ
Line outputs (LINEL and LINER; pins 27 and 28); audio inputs at AFINL and AFINR (pins 1 and 50): –11.5 dBV						
V_o	output voltage		–11	–8	–5	dBV
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–93	–90	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion		–	0.06	0.2	%
L	linearity	V_{iAF} = –11.5 to –41.5 dBV	57	60	63	dB
α_{cb}	channel balance		–2	–	+2	dB
f_{res}	frequency response with respect to 1 kHz; output level	f_i = 300 Hz	–1	+0.4	+1.8	dB
		f_i = 10 kHz	–9.7	–7.7	–5.7	dB
DC outputs (DCOUTL and DCOUTR; pins 31 and 32); square root of output voltage (see Fig.8)						
V_{oz}	output voltage for zero input level	HSF = 1	–	–	300	mV
		HSF = 0	–	–	440	mV

Note

1. The audio distortion is measured with the HID pulse frequency set to 1 kHz (500 Hz input at pin 51). FM signal: f_m = 10 kHz; Δf = 50 kHz. The distortion is measured with a 3 kHz 4th-order low-pass filter. The measured value at 1 kHz HID-pulse frequency is corrected with 26 dB in order to calculate the equivalent distortion at 50 Hz HID-pulse frequency.

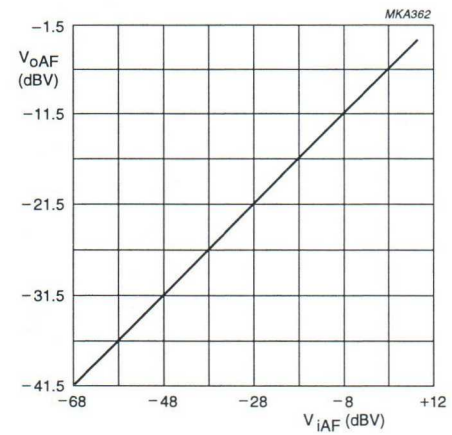


Fig.6 Compression curve of noise reduction at 1 kHz; record mode. The audio output voltage at AFOUTL and AFOUTR (pins 2 and 49) as a function of the audio input voltage at TUNL and TUNR (pins 9 and 10).

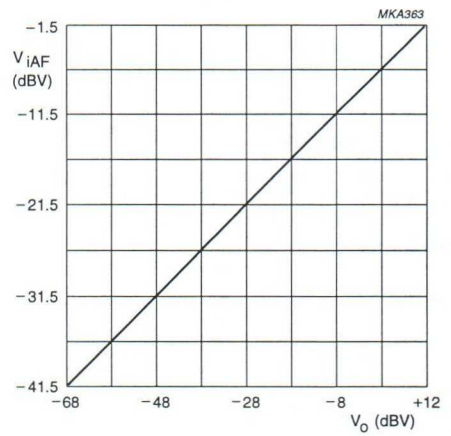


Fig.7 Expansion curve of noise reduction at 1 kHz; playback mode. The audio output voltage at LINEL and LINER (pins 27 and 28) as a function of the audio input voltage at AFINL and AFINR (pins 1 and 50).

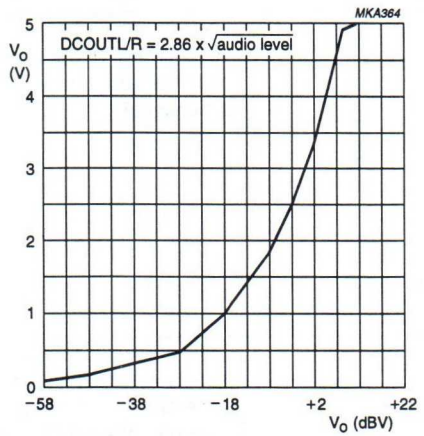


Fig.8 VU meter output voltage at DCOUTL and DCOUTR (pins 31 and 32) as a function of audio signal level.

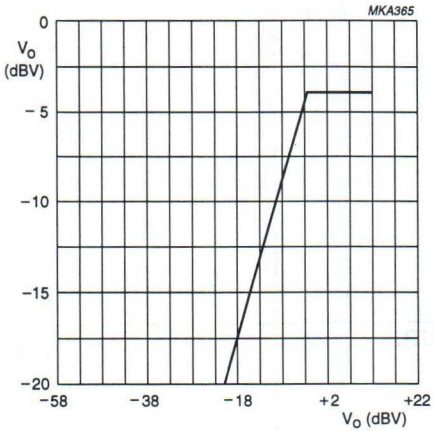


Fig.9 Modulator output voltage at MODOUT (pin 30) as a function of line output signal level at LINEL and LINER (pins 27 and 28).

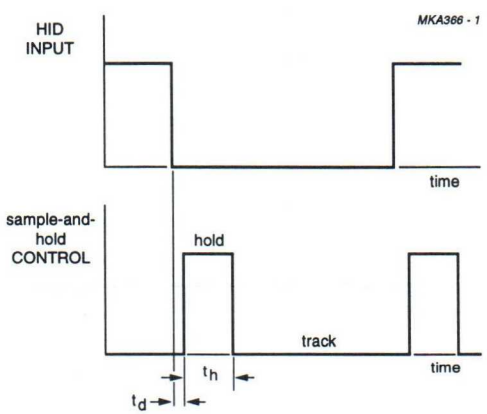


Fig.10 Sample-and-hold timing waveforms.

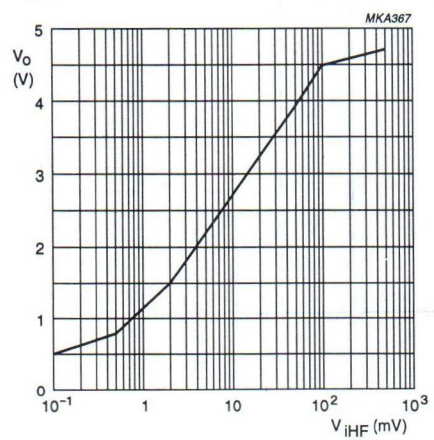
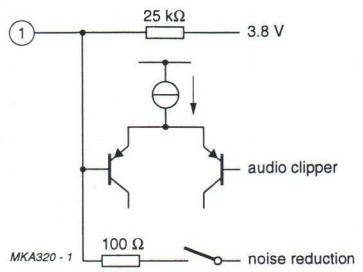
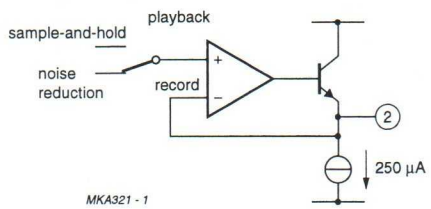
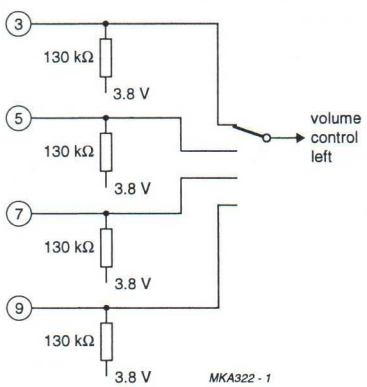
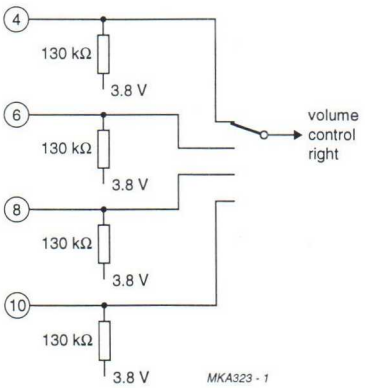
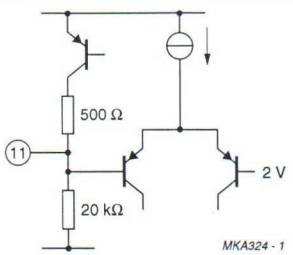
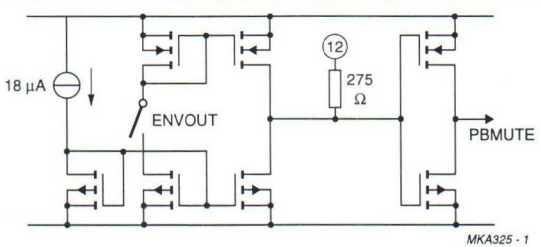
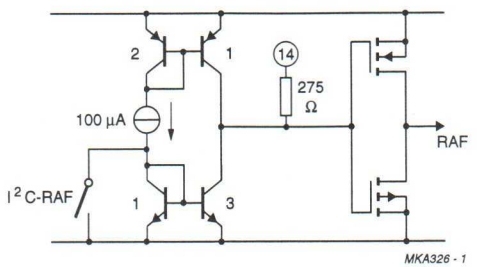
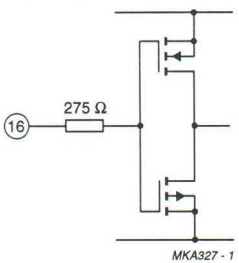
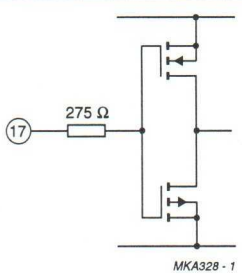
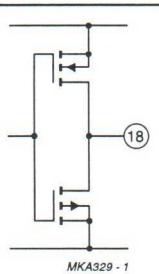


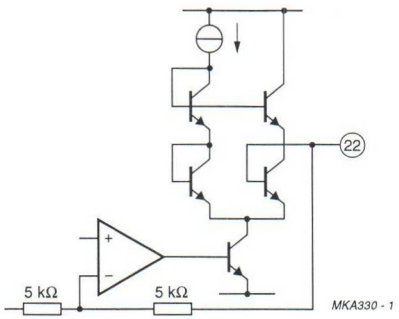
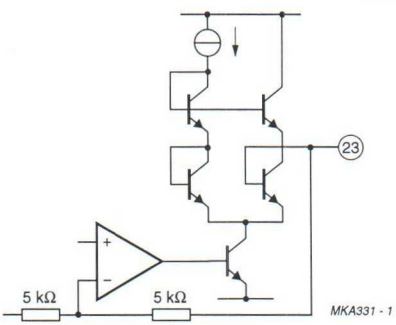
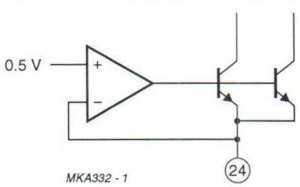
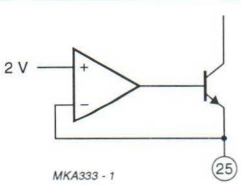
Fig.11 Level detector output voltage at ENVOUT (pin 11) as a function of the limiter input voltage level (RMS value) at FMINL (pin 61).

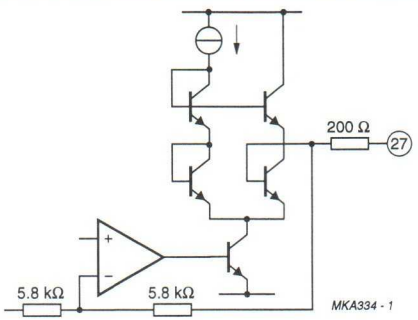
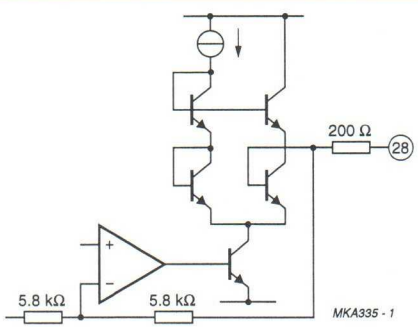
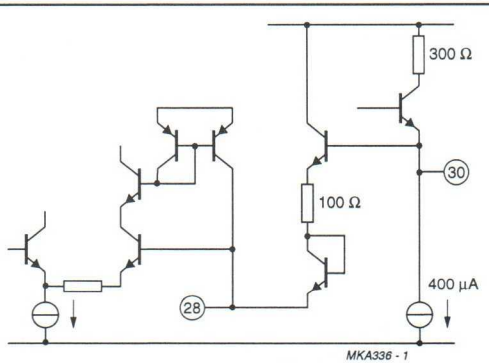
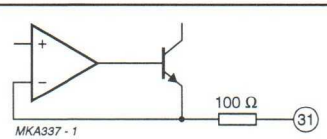
INTERNAL CIRCUITRY

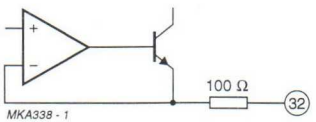
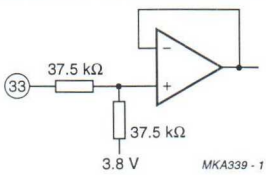
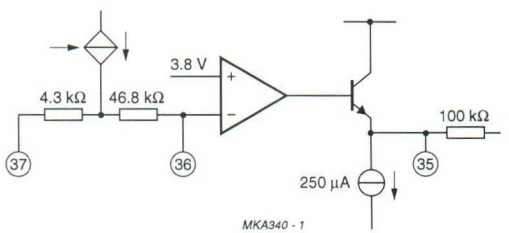
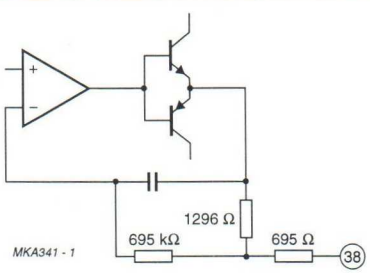
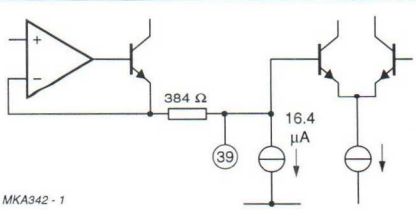
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
AFINL	1		audio input for either audio clipper (record) or noise reduction (playback) of left channel
AFOUTL	2		audio output from either sample-and-hold (playback) or noise reduction (record and loop-through) of left channel
EXT2L	3		input selector for left channel
EXT1L	5		
CINL	7		
TUNL	9		

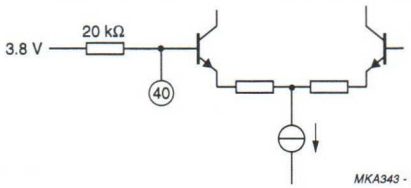
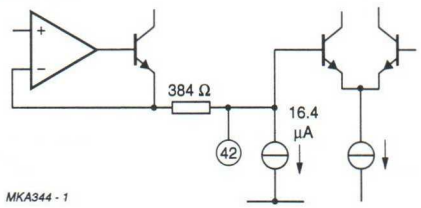
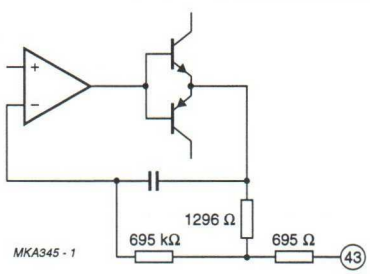
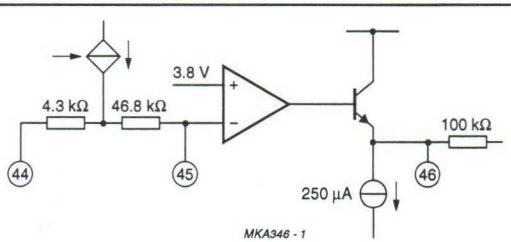
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
EXT2R	4		input selector for right channel
EXT1R	6		
CINR	8		
TUNR	10		
ENVOUT	11		level detector output; external capacitor required for filtering
MUTE	12		mute timing; external capacitor required for timing playback mute
V_{DDD}	13		digital supply voltage (+5 V)

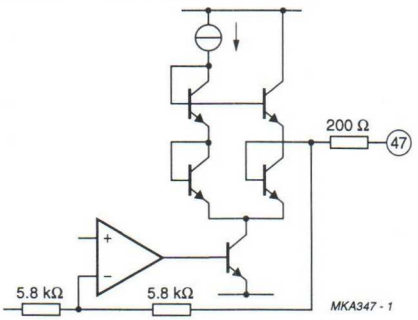
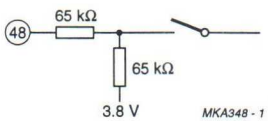
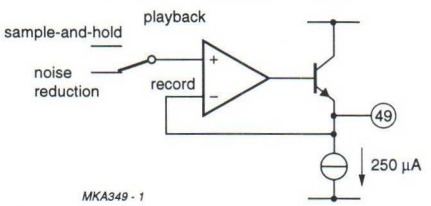
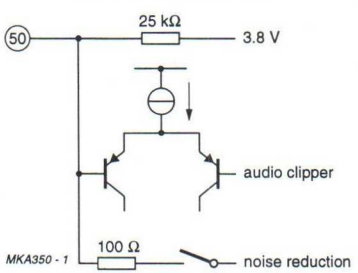
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
RAF	14		overrule the I²C-bit RAF input or record/playback switch drive output for head amplifier control
V_{SSD}	15		I²C-bus digital ground
SDA	16		I²C-bus data input
SCL	17		I²C-bus clock input
XS	18		auxiliary switch; digital output controlled by I²C-bit XS
V_{DDA1}	19		analog supply voltage (+12 V)
V_{DDH}	20		headphone supply voltage (+12 V)

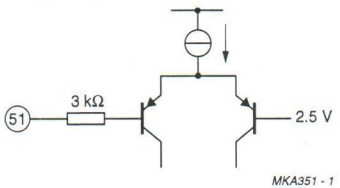
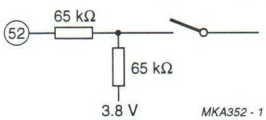
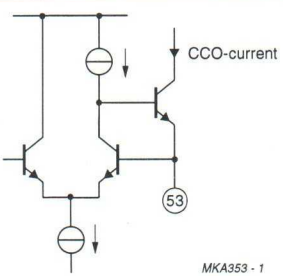
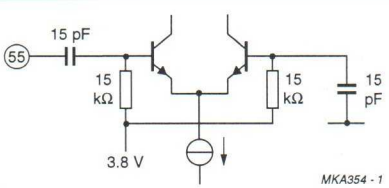
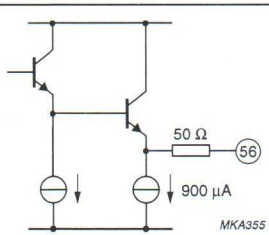
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
V_{SSH}	21		headphone ground
HPOUTL	22		headphone drive output left
HPOUTR	23		headphone drive output right
RVAR	24		gain adjustment of noise reduction by means of a resistor to ground
RFIX	25		fixed bias current generation circuit by using an external 100 kΩ resistor to ground
i.c.	26		pin internally connected to die pad; preferably connected to ground

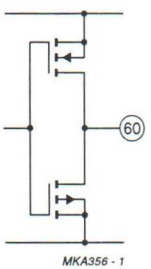
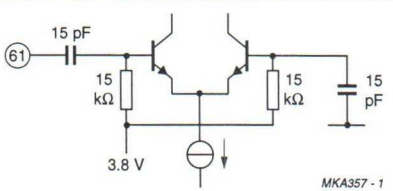
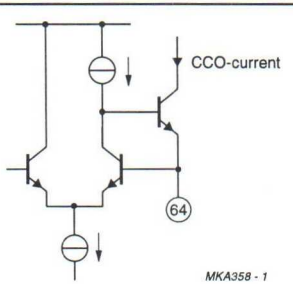
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
LINEL	27		line output left
LINER	28		line output right
MODAGC	29		RF modulator AGC time constant
MODOUT	30		RF modulator drive output
DCOUTL	31		VU meter drive output left

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
DCOUTR	32		VU meter drive output right
LININ	33		linear input
n.c.	34		not connected
DCFBL	35		DC feedback left
DCREFL	36		DC reference left
EMPHL	37		total emphasis left (20 to 240 µs)
RECTL	38		rectifier DC decoupling left
DETL	39		attack/recovery timing left

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
V_{ref}	40		noise filtering of 3.8 V reference voltage; external capacitor required for filtering
V_{SSA1}	41		analog ground for LF circuits
DETR	42		attack/recovery timing right
RECTR	43		rectifier DC decoupling right
EMPHR	44		total emphasis right (20 to 240 µs)
DCREFR	45		DC reference right
DCFBR	46		DC feedback right

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
LINOUT	47		linear output
EXN1	48		EXN input (External Normal Input); mono input selectable to linear output
AFOUTR	49		audio output from either sample-and-hold (playback) or noise reduction (record and loop-through) of right channel
AFINR	50		audio input for either audio clipper (record) or noise reduction (playback) of right channel

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
HID	51		Head Identification pulse input for sample-and-hold circuits
EXN2	52		EXN input (External Normal Input); mono input selectable to linear output
FADJR	53		frequency adjustment of right channel oscillator by means of a variable resistor
n.c.	54		not connected; preferably connected to ground
FMINR	55		1.7 or 1.8 MHz input for limiter
FMOUT	56		FM output
V_{DDA2}	57		analog supply voltage (+5 V)

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
i.c.	58		pin internally connected to die pad; preferably connected to ground
V_{SSA2}	59		analog ground for HF circuits
NTSC	60		digital output controlled by I²C-bit NTSC
FMINL	61		1.3 or 1.4 MHz input for limiter
n.c.	62		not connected; preferably connected to ground
n.c.	63		not connected; preferably connected to ground
FADJL	64		frequency adjustment of left channel oscillator by means of a variable resistor

TEST AND APPLICATION INFORMATION

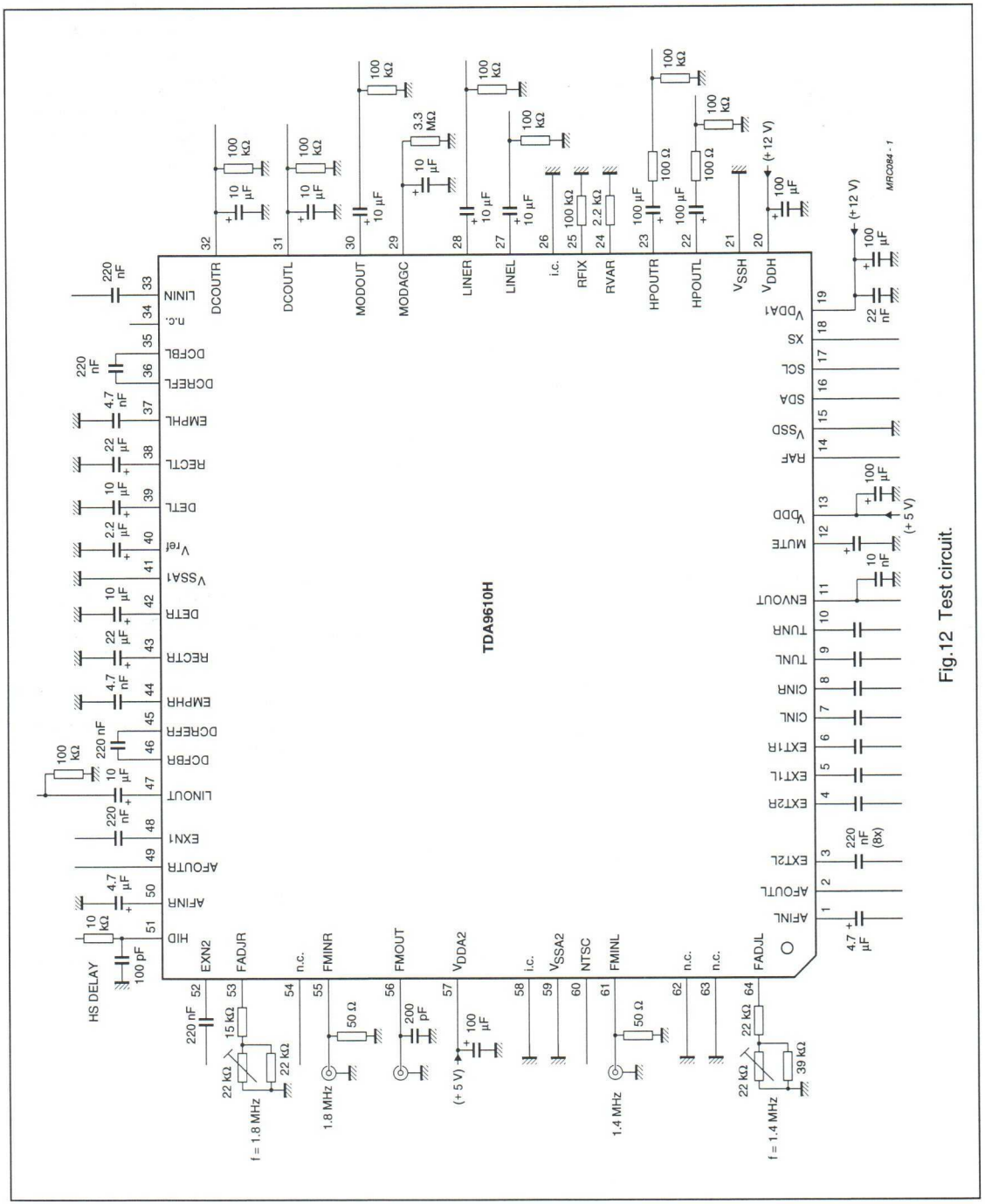


Fig.12 Test circuit.

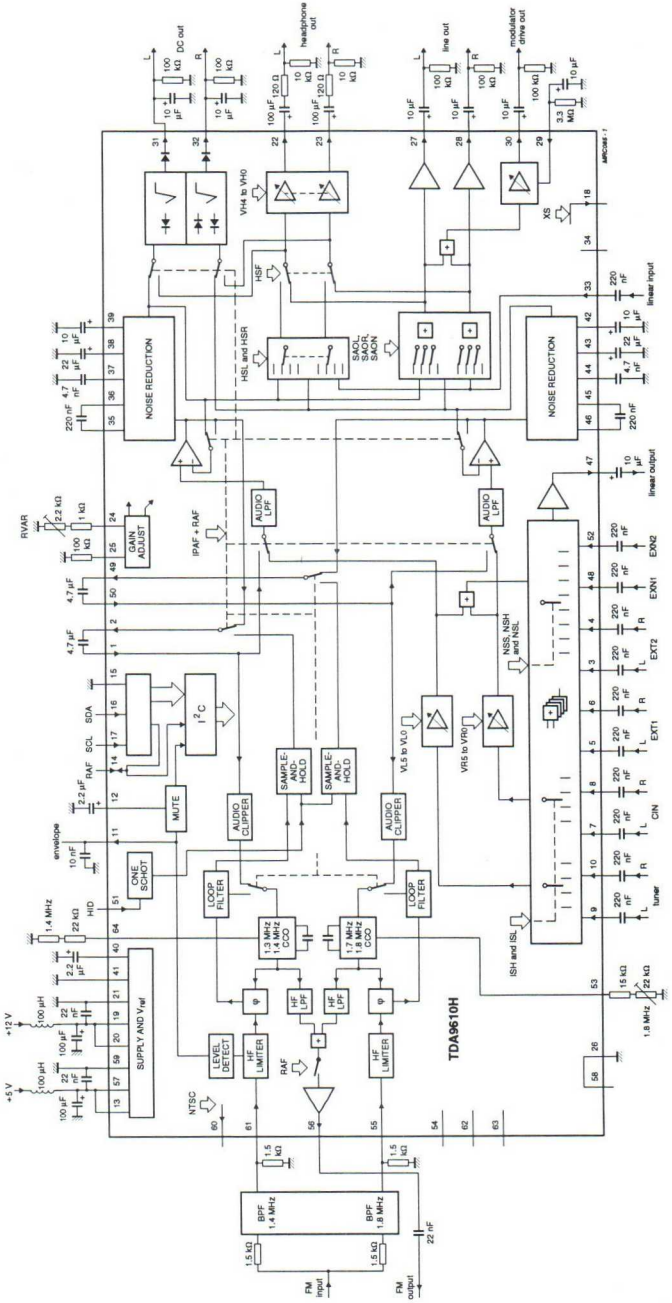


Fig.13 Application diagram.

Adjustment of VCO frequency

Set the TDA9610H in record mode (NTSC off), no audio input signal.

Measure the frequency at FMOUT (pin 56) with a frequency counter and use the VCO TEST modes (see Section "Function byte") to output only the channel of interest.

Adjust the VCO frequencies to 1.4 MHz ±10 kHz and 1.8 MHz ±10 kHz by means of the potentiometers at pin 64 (FADJL) and pin 53 (FADJR).

When NTSC is to be the main video standard, set NTSC on and adjust to 1.3 MHz and 1.7 MHz for optimum frequency accuracy.

Standard FM deviation and audio level

Reference levels of frequency deviation and audio output level are set by the resistor value at pin 24 (RVAR); simultaneous for left, right, playback and record. Typical resistor values can be calculated with equation:

$$R_{typ} = \frac{\left(\frac{\Delta f}{50\ kHz}\right)^2}{\left(\frac{A}{400\ mV\ (RMS)}\right)} \times 2.2\ k\Omega$$

Where:

Δf = reference FM deviation.

A = reference audio output level (1 kHz audio frequency).

If adjustment for overall tolerance is needed, R has to be made adjustable for the range $0.7R_{typ}$ to $1.4R_{typ}$.

Set the TDA9610H in playback. Use a HF test generator to make a carrier of 1.4 MHz with the desired modulation and input this signal at FMINL (pin 61) or before the band-pass filter and measure the audio output level at LINEL (pin 27).

Power-down mode

To lower the dissipation in a stand-by situation, the 12 V supply voltage at pin 19 (V_{DDA1}) and pin 20 (V_{DDH}) may be switched off, with pins 19 and 20 'floating'. No low-ohmic DC path to ground may be seen from pins 19 and 20, because this will drain extra current from the 5 V supply via these pins to ground.

Because of the fact that the I²C circuitry and the digital outputs RAF, NTSC and XS are supplied via the 5 V supply, no I²C settings will be lost and the output pins can still be used.

For instance, XS can be used to drive external mute transistors to mute the DC jump at the line outputs when switching the 12 V supply.

RAF I/O

The status of the I²C RAF bit is output at pin 14 (RAF = HIGH; record). This output can be used to switch the audio FM head amplifier to playback and record. If accurate fast switching of the TDA9610H is needed, this pin can also be used as input. Thereby overruling the I²C RAF bit. To make this possible the RAF output is current limited.

When using the RAF pin as output, no more than 35 µA (LOW) and 185 µA (HIGH) current may be drawn from this pin to assure the mode of the TDA9610H is not changed.

When using the RAF pin as input, the voltage source used must be capable of delivering at least 345 µA (forced HIGH; >3.5 V) or sinking at least 65 µA (forced LOW; <1.5 V).

Audio processor for VHS hi-fi and linear audio

TDA9614H

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING
6 FUNCTIONAL DESCRIPTION
6.1 Audio I/O switching
6.1.1 Input Select (InputSel)
6.1.2 Normal Select (NormSel)
6.1.3 Volume L/R; AGC
6.1.4 Audio FM Output Mute (AFOMute); Normal Output Mute (NOMute)
6.1.5 Output Select (OutSel)
6.1.6 RF Converter Mute (RFCMute)
6.1.7 Line Select (LineSel)
6.1.8 Decoder Select (DecodeSel)
6.1.9 Headphone Select (HPSel)
6.1.10 Headphone volume
6.1.11 DC Select (DCSel)
6.2 Linear audio circuits
6.2.1 Record/loop-through
6.2.2 Playback
6.3 Audio FM circuits
6.3.1 Record/loop-through
6.3.2 Playback
6.3.3 Automatic calibration
6.3.4 PAL/NTSC mode
6.4 I²C-bus
6.5 Power-On Reset (POR); derived from digital supply voltage V_{DDD}
6.6 Control byte
6.7 Main select byte
6.8 Secondary select byte
6.9 Left/Right (L/R) volume byte
6.10 Headphone volume byte
6.11 Install byte
6.12 Test byte
6.13 Read byte
7 LIMITING VALUES
8 THERMAL CHARACTERISTICS
9 DC CHARACTERISTICS
10 AC CHARACTERISTICS
10.1 Record audio FM mode
10.2 Record linear audio mode
10.3 Playback Audio FM mode
10.4 Playback linear audio
11 INTERNAL CIRCUITRY
12 TEST AND APPLICATION INFORMATION
12.1 RAF I/O (pin 12)
12.2 RCCOL, RCCOR, RBPF and RFIX (pins 59, 53, 55 and 49)
13 PACKAGE OUTLINE
14 SOLDERING
14.1 Plastic quad flat packages
14.1.1 By wave
14.1.2 By solder paste reflow
14.1.3 Repairing soldered joints (by hand-held soldering iron or pulse-heated solder tool)
15 DEFINITIONS
16 LIFE SUPPORT APPLICATIONS
17 PURCHASE OF PHILIPS I²C COMPONENTS

Audio processor for VHS hi-fi and linear audio

TDA9614H

1 FEATURES

- All functions controlled by I²C-bus
- No adjustments needed by use of auto-calibration circuit
- Integrated Bandpass Filters (BPFs)
- Low-noise Phase-Locked Loop (PLL) FM (de)modulator
- Low-distortion sample-and-hold switching noise suppressor
- Integrated HF Low-Pass Filter (LPF) and summator
- Integrated audio LPF
- 5 stereo inputs (left and right channel):
  - TUNL and TUNR
  - CINL and CINR
  - EXT1L and EXT1R
  - EXT2L and EXT2R
  - EXT3L and EXT3R
- Additional mono input: Second Audio Program (SAP)
- Independent Input/Output (I/O) selections and 2nd line output
- Linear audio
- DC output for VU meter drive
- Direct headphone drive
- RF converter output with overload Automatic Gain Control (AGC)
- Integrated standby mode for low current consumption
- E-E performance (record + playback):
  - Total Harmonic Distortion (THD): 0.05% (–8 dBV, 1 kHz)
  - linearity error: 0.1 dB (–88 dBV, 1 kHz)
  - noise: –93 dBV (20 Hz to 20 kHz).

2 GENERAL DESCRIPTION

The TDA9614H is an audio processing IC for VHS hi-fi and linear audio, digitally controlled via the I²C-bus. The FM (de)modulator and peak noise reduction functions are highly integrated, resulting in few external components and no external adjustments.

In addition special functions for audio mixing, dubbing and descrambling have been implemented.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9614H	QFP64[1]	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

4 BLOCK DIAGRAM

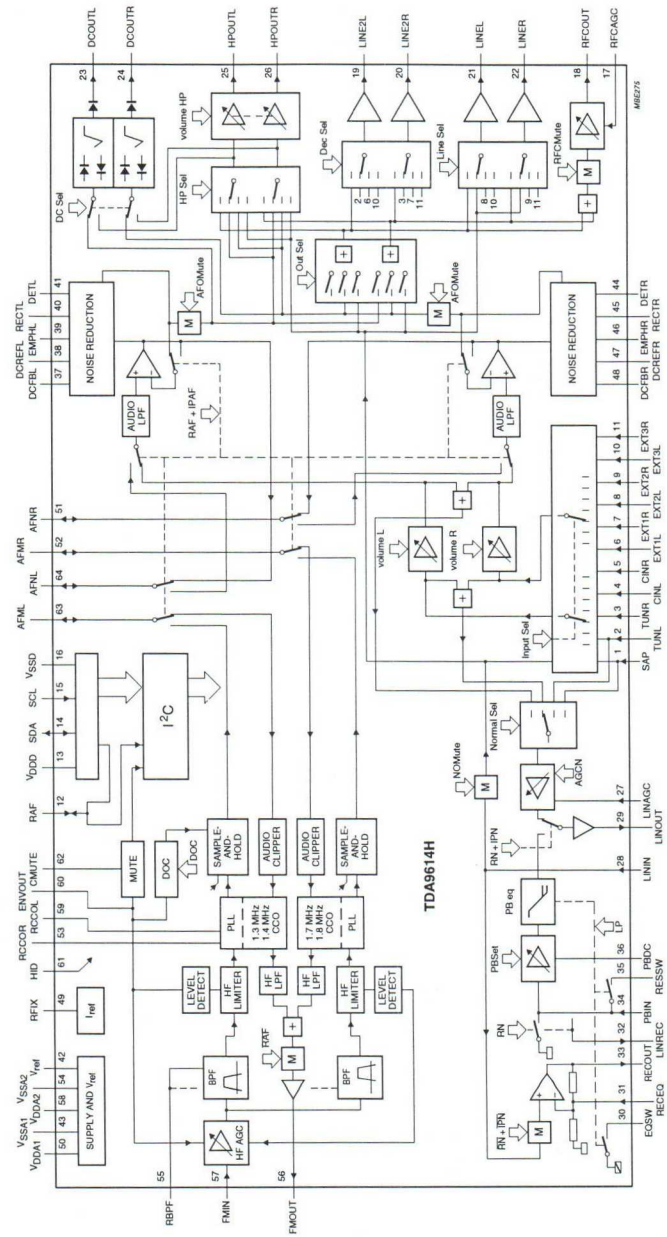


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
SAP	1	Second Audio Program (SAP) input.
TUNL	2	Left channel tuner input.
TUNR	3	Right channel tuner input.
CINL	4	Left channel cinch input.
CINR	5	Right channel cinch input.
EXT1L	6	Left channel external 1 input.
EXT1R	7	Right channel external 1 input.
EXT2L	8	Left channel external 2 input.
EXT2R	9	Right channel external 2 input.
EXT3L	10	Left channel external 3 input.
EXT3R	11	Right channel external 3 input.
RAF	12	Record/playback switch drive output for head amplifier control or input for overruling the I^2C-bit RAF.
V_{DDD}	13	Digital supply voltage for I^2C-bus (+5 V).
SDA	14	Data input/output for I^2C-bus.
SCL	15	Clock input for I^2C-bus.
V_{SSD}	16	Digital ground for I^2C-bus.
RFCAGC	17	RF converter AGC-time constant.
RFCOUT	18	RF converter drive output.
LINE2L	19	Line 2 left output (e.g. decoder output).
LINE2R	20	Line 2 right output (e.g. decoder output).
LINEL	21	Line output left.
LINER	22	Line output right.
DCOUTL	23	VU meter drive output left.
DCOUTR	24	VU meter drive output right.
HPOUTL	25	Headphone drive output left.
HPOUTR	26	Headphone drive output right.
LINAGC	27	Linear audio AGC-time constant.
LININ	28	Audio input for linear audio to REC equalizer and output select.
LINOUT	29	Audio output from AGC or PB equalizer.
EQSW	30	Long Play (LP) equalization switch; 15 Ω on resistance and 150 kΩ input impedance.
RECEQ	31	Linear audio recording amplifier negative feedback input for connecting a record equalization network.
LINREC	32	Digital output controlled by I^2C-bit RN; can be used to drive an external (high voltage) head switch and possibly the bias oscillator.
RECOUT	33	Linear audio recording amplifier output.
PBIN	34	Linear audio playback amplifier input; during playback the impedance is 100 kΩ; during record the impedance is 7 Ω.
RESSW	35	Long Play equalization switch 50 Ω on and 150 kΩ off impedance to PBIN.
PBDC	36	Linear audio playback amplifier DC decoupling.

SYMBOL	PIN	DESCRIPTION
DCFBL	37	DC feedback left.
DCREFL	38	DC reference left.
EMPHL	39	Total emphasis left (240 to 20 μs).
RECTL	40	Rectifier DC decoupling left.
DETL	41	Attack/recovery timing left.
V_{ref}	42	Noise filtering of 3.8 V reference voltage (external capacitor required for filtering).
V_{SSA1}	43	Analog ground 1 for LF circuits.
DETR	44	Attack/recovery timing right.
RECTR	45	Rectifier DC decoupling right.
EMPHR	46	Total emphasis right (240 to 20 μs).
DCREFR	47	DC reference right.
DCFBR	48	DC feedback right.
RFIX	49	Fixed bias current generation circuit by using an external 180 kΩ resistor to ground.
V_{DDA1}	50	Analog supply voltage 1 for LF circuits (+12 V).
AFNR	51	Audio output from noise reduction of right channel (record and loop-through) or audio input for noise reduction of right channel (playback).
AFMR	52	Audio input for audio clipper of right channel (record and loop-through) or audio output from sample-and-hold (playback).
RCCOR	53	Voltage-to-current transfer for right channel oscillator by means of an external resistor to ground.
V_{SSA2}	54	Analog ground 2 for HF circuits.
RBPF	55	Bias current generation for the internal band-pass filters by means of an external resistor to ground.
FMOUT	56	FM output.
FMIN	57	FM input.
V_{DDA2}	58	Analog supply voltage 2 for HF circuits (+5 V).
RCCOL	59	Voltage-to-current transfer for left channel oscillator by means of an external resistor to ground.
ENVOUT	60	Level detector output (external capacitor required for filtering).
HID	61	Head Identification Pulse (HID) input for sample-and-hold circuits.
CMUTE	62	Mute timing (external capacitor required for playback mute).
AFML	63	Audio input for audio clipper of left channel (record and loop-through) or audio output from sample-and-hold circuit of left channel (playback).
AFNL	64	Audio output from noise reduction of left channel (record and loop-through) or audio input for noise reduction of left channel (playback).

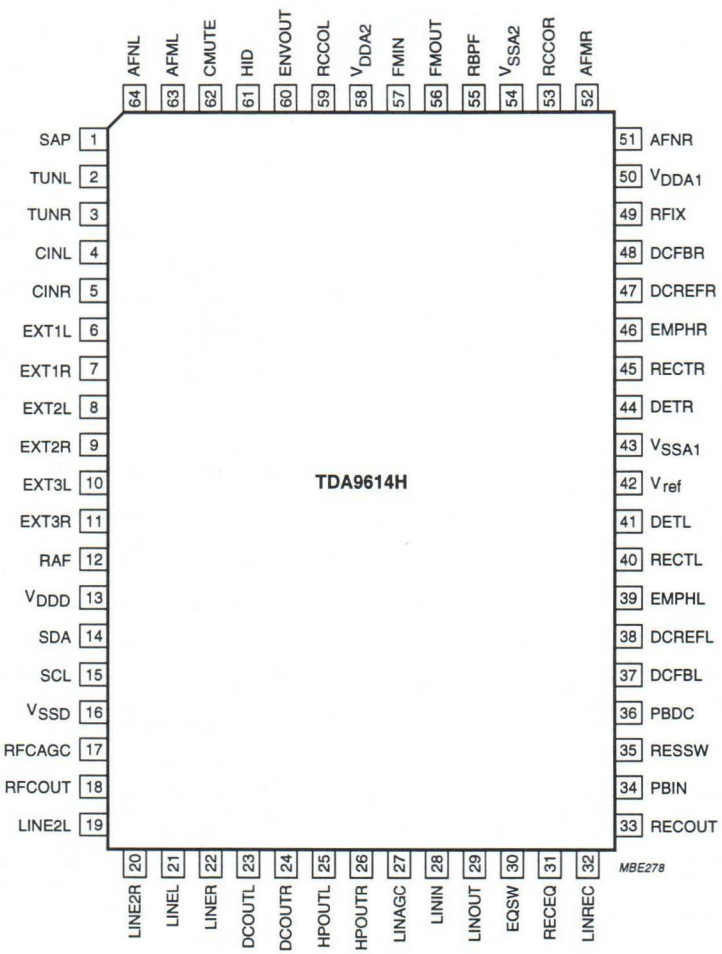


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

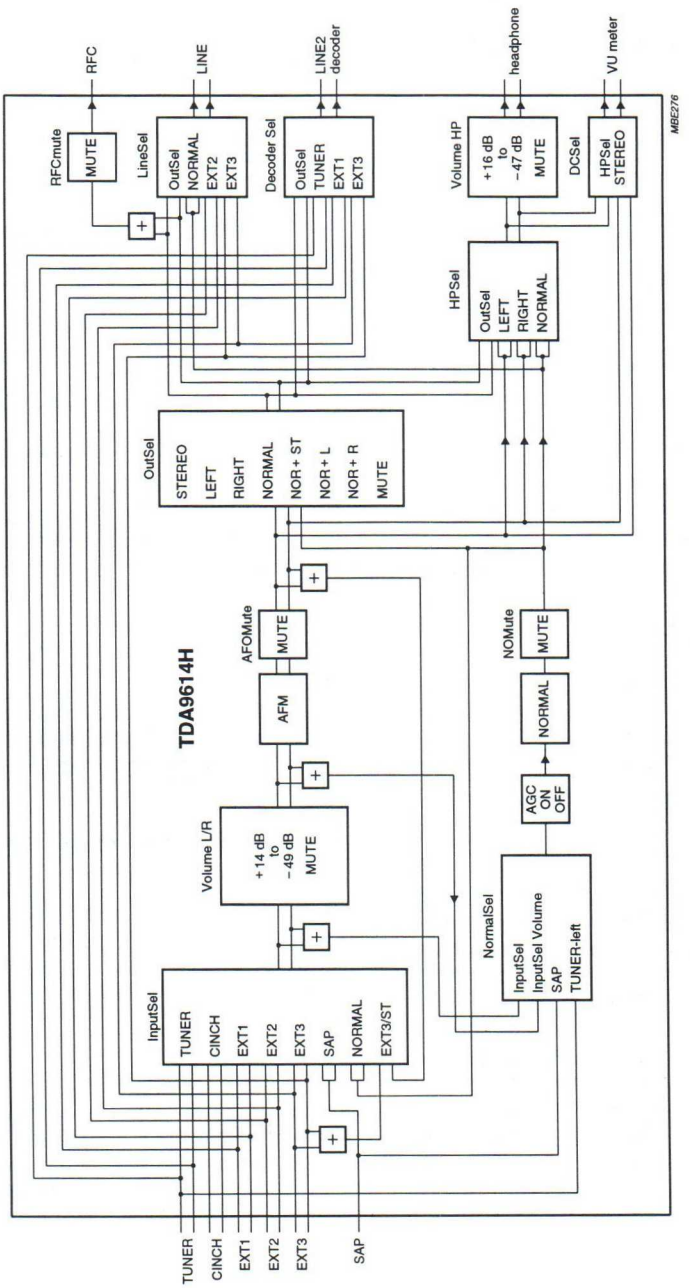


Fig.3 Audio input/output selections.

6.1 Audio I/O switching

6.1.1 Input Select (InputSel)

For the audio FM circuitry eight different audio signals can be selected. The selection made here for hi-fi is also available for the linear audio circuitry.

1. TUNER (stereo input; internal tuner of VCR).
2. CINCH (stereo input; connection to hi-fi set).
3. EXT1 (stereo input; TV SCART1).
4. EXT2 (stereo input; decoder, 2nd VCR SCART2).
5. EXT3 (stereo input; front CINCH for e.g. camcorder).
6. SAP (mono input; 'Second Audio Program' audio carrier for NTSC or conventional FM carrier with NICAM reception).
7. NORMAL (linear audio; [playback] signal of linear audio).

   When inserting a new video signal in an old audio/video recording the hi-fi audio track is erased. This setting can keep the current audio available on the hi-fi track by copying the (playback) linear audio signal to the hi-fi track during video insert.
8. EXT3/ST (input mix; mono EXT3 on left, mono hi-fi on right channel).

For linear audio use see Section 6.1.2.

6.1.2 Normal Select (NormSel)

For linear audio four settings can be selected:

1. INPUTSEL (mono signal from input select).

   This is the 'standard' setting. The signal source selected with the input select is led to the linear audio circuit. The linear audio AGC should be switched on.
2. VOLUME (mono signal from [hi-fi] volume control).

   The signal source selected with the input select has now volume control, the linear audio AGC should be switched off. This setting is for use with 'audio dubbing': inserting a new audio signal on the linear track in an old audio/video recording. A special audio dubbing feature is now possible by selecting 'input mix' EXT3/ST in the input select. This setting enables us to use the VCR as a mixer console: an audio source connected to EXT3 (front CINCH) can be adjusted and mixed together with the original hi-fi playback signal, using the left (EXT3) and right (hi-fi playback) volume controls.
3. SAP (SAP input).

   This setting enables simultaneous recording of the NTSC SAP signal on the linear track and TUNER stereo on the audio FM track. When receiving a NICAM audio signal, the linear audio can be used as a 'backup' track when received television signals are weak.
4. TUNER LEFT (left channel [language 1] of TUNER input).

   When receiving dual language transmissions the main language (language 1) can be recorded on linear audio. Note that if the SAP input is not used it can be connected to the right TUNER channel, enabling language selection for linear audio.

6.1.3 Volume L/R; AGC

The volume controls are mainly intended for level adjusting of the audio signals to be recorded on the hi-fi track, however using the 'VOLUME' setting in the Normal Select it can also be used to control linear audio. The volume controls have a control range of +14 dB to –49 dB in 1 dB steps and a full mute. Because the volume controls are I²C-bus controlled their actual behaviour is defined by the VCR's software. For instance user control can be 'volume only', 'left + right', 'volume + balance' or the setting can be defined by a 'digital AGC' software loop using the signals at the DC (VU meter) outputs.

The linear audio level can be controlled by an AGC circuit, which can be switched off when desired. In most cases the AGC should be used at all settings of the Normal Select except for 'VOLUME'.

6.1.4 Audio FM Output Mute (AFOMute); Normal Output Mute (NOMute)

The audio output signal of the audio FM circuit can be muted with AFOMute, the linear output signal can be muted using NOMute. If one of these signals is not used as an output (or input) signal it is best muted to further minimize crosstalk.

6.1.5 Output Select (OutSel)

This block is the 'main' output select function, possibly functional on all outputs. Each output however has some means to override this selection for its own output signal, to implement extra features. Eight selections are possible and they are shown in Table 1.

Table 1 Output select possibilities

SELECTION	REMARK	DESCRIPTION
STEREO[1]	hi-fi stereo	audio FM output signal left and right channel
LEFT	hi-fi left	audio FM output signal left channel (language 1)
RIGHT	hi-fi right	audio FM output signal right channel (language 2)
NORMAL	linear audio	linear audio
NOR + ST	linear and hi-fi	mix of audio FM stereo and linear audio
NOR + L	linear and left	mix of audio FM left channel and linear audio
NOR + R	linear and right	mix of audio FM right channel and linear audio
MUTE	mute	

Note

1. STEREO is the 'standard' setting, LEFT and RIGHT are for language selection. Using the tuner as input or output signal (record or loop-through of audio FM) the VCR can automatically switch from stereo to left (language 1) when a 'dual language' transmission is received. If the VCR is in playback mode and no hi-fi track is present (checking bit AFOM via the I²C-bus or using the level at pin 11) the VCR can switch the output select to NORMAL (or let the IC do this automatically by setting bit AUTN). If a hi-fi track is present the user may want to switch to LEFT and RIGHT if the recording made was a 'dual language' recording.

   Furthermore the user may want to switch from a hi-fi selection to NORMAL, e.g. when a complete audio remix has been created on the linear track using 'audio dubbing' (see Section 6.7). 'Audio dubbing' can also be used to re-record the linear track with e.g. only commentary. Combined playback of this commentary together with the original hi-fi sound is then possible by means of a mix mode.

6.1.6 RF Converter Mute (RFCMute)

The RFC output is a mono output derived from the output select, its output signal can be muted.

6.1.7 Line Select (LineSel)

The line output select is normally connected to both CINCH (hi-fi set) and television (SCART1). Normally the audio signal from the output select will be available at this output, but three extra selections are possible and they are shown in Table 2.

Table 2 Extra line select possibilities

SELECTION	DESCRIPTION
NORMAL	linear audio, useful for monitoring during 'audio dubbing'
EXT2[1]	audio from input EXT2
EXT3[2]	audio from input EXT3

Notes

1. A signal from a source at EXT2 (laser disc or second VCR) can be connected to a television set at line out. Because this is a direct connection from the input to the line output buffers it is fully independent of any mode setting of the IC. Connection of a 'Pay-TV' decoder box to EXT2 and using this selection together with selecting EXT1 in the decoder select enables combined use of the decoder box by both TV and VCR. In Europe, use of the SCART connector 'status line' can automatize this switching.
2. Direct audio connection from input EXT3. If the line 2 outputs and EXT3 inputs are not used for external connections a built-in karaoke unit or sound processor can be inserted between line 2 and EXT3.

6.1.8 Decoder Select (DecodeSel)

The line 2 output is normally connected to a decoder box or e.g. a second VCR (SCART2). Normally the audio signal from the output select will be available at this output, but three extra selections are shown in Table 3.

Table 3 Extra decoder select possibilities

SELECTION	DESCRIPTION
TUNER(1)	audio from input TUNER
EXT1(2)	audio from input EXT1
EXT3	audio from input EXT3

Notes

1. Enables the use of a decoder box (connected to line 2 [EXT2]) by the VCR.
2. Decoder box connection to television set (See Section 6.1.7).

6.1.9 Headphone Select (HPSel)

The headphone output will normally carry the output select signal, however three more selections are possible and shown in Table 4.

Table 4 Extra headphone select possibilities

SELECTION	DESCRIPTION
LEFT(1)	left hi-fi channel
RIGHT(1)	right hi-fi channel
NORMAL	linear audio, useful for monitoring the recording by 'audio dubbing'

Note

1. The selections LEFT and RIGHT make it possible to select a different language for the headphone as for the line outputs. A possible implementation is to invert always a language selection made at the output select.

6.1.10 Headphone volume

The headphone volume control has a control range of +16 dB to −47 dB in 1 dB steps and a full mute.

6.1.11 DC Select (DCSel)

The VU meter output is normally connected to the headphone select, but can also be switched to STEREO (hi-fi stereo, before the output select). When using the VU meter output signal to implement a 'digital AGC' (read the level at the DC output, and adjust the VOLUME L/R controls accordingly) it is necessary to have information of both hi-fi audio channels, independent from the setting of output or headphone select. For this mode the selection STEREO can be made.

6.2 Linear audio circuits

6.2.1 Record/loop-through

The signal selected with the normal select can be level controlled in the AGC block. If wanted this AGC can be switched off using bit AGCN. The audio signal is thereafter DC decoupled using a capacitor between pin 29 (LINOUT) and pin 28 (LININ).

From here on the signal goes to the output select and (in the event of record mode) to the record equalizer. The record equalizer is a non-inverting amplifier with a gain of +12 dB, consisting of an opamp with feedback resistors, and acts as a pre-correction filter for the tape and head characteristics. The inverting input of the opamp is connected to pin 31 (RECEQ), its output to pin 33 (RECOUT). The circuit externally connected between pin 31 and ground defines the transfer of the record equalizer with equation: $A = 3.98 \times \frac{(1200 + Z)}{Z}$

Where: Z is the complex impedance of the external circuit.

Two equalizings can be used, switching additional circuitry to ground with pin 30 (EQSW) in long play or extended play (I^2C-bus: LP = 1).

Instead of the hi-fi circuit, linear audio has two loop-through modes:

- Loop-through playback
- Loop-through record.

The only difference between Loop-through record and record is the RECOUT output, which is muted.

The LINREC output (pin 32) is used to drive the external high-voltage switch and possibly the bias oscillator. The LINREC voltage has a small internal delay to be non-overlapping with the internal switching to playback mode. This ensures that no bias voltage will appear at the PBIN input while the IC is in playback mode.

6.2.2 Playback

The signal coming from the head is amplified and can be level controlled in 16 steps of 1 dB. This setting can be used to adjust for spread or nominal difference in head output level. Afterwards, the signal is frequency corrected in the playback equalizer. This equalizer includes the two standard VHS equalizing settings of 3180 and 120 µs

(standard play: LP = 0) and 3180 and 170 µs (Long Play: LP = 1).

The signal is DC decoupled and routed to the output select via pins 29 and 28. When switching to or from playback the signal should be muted shortly using the Normal Output Mute (NOM) to prevent audible clicks caused by offset differences of the playback amplifier and AGC.

6.3 Audio FM circuits

6.3.1 Record/loop-through

After low-pass filtering and signal compression in the Noise Reduction (NR) the audio signal is available at AFNL and AFNR. Through a DC-decoupling capacitor the compressed audio signal is fed to an audio clipper at AFML and AFMR. Subsequently, the audio signal is FM-modulated on a RF-carrier using an integrated current-controlled oscillator (CCO). Each CCO (L and R) requires an external resistor (RCCOL/R) for temperature stability. Through automatic calibration both the oscillator centre frequency and FM-deviation are adjusted. After low-pass filtering and summation of the two RF-carriers, the FM signal is available at FMOUT during record. During loop-through the FMOUT pin is inactive.

The RAF pin reflects the status of the RAF-bit when it is used as output pin. In this case it is meant to switch the head amplifier between record and playback position. It can also be used as an input pin to overrule the RAF-bit thereby forcing the IC in record or playback/loop-through position.

6.3.2 Playback

The two FM modulated RF carriers, presented at FMIN, are fed to an AGC circuit. The AGC operates on the peak level of the added BPF output signals. As a result, the input signal of the BPFs is kept constant for FMIN voltages >30 mV (RMS value) both carriers added. In this way the dynamic range of the integrated BPFs is optimally used over a large input signal range. Subsequently, the RF carriers are bandpass filtered using two integrated BPFs. These bandpass filters are automatically calibrated as described in Section 6.3.3. An external resistor (RBPF) is required for temperature stability.

The filtered input signals are fed to a limiter. The limiter output signal is demodulated by means of a PLL demodulator. The LF audio signal is fed through a sample-and-hold circuit to suppress head-switching noise. The demodulated audio is available at AFML and AFMR. Through a decoupling capacitor the audio signal is applied to an audio low-pass filter at AFNL and AFNR. The low-pass filtered audio signal is expanded in the noise reduction.

If the left channel carrier at FMIN falls below the mute level of 4.2 mV (RMS value) the audio signal is muted in front of the low-pass filter. This is achieved by comparing the left channel level detector signal with an internal reference. The mute timing is fixed by a capacitor at the CMUTE pin. If the level at CMUTE rises above a certain threshold, the PBMUTE bit is set. This will mute the audio signal. If bit AUTN has been set, the output selection will automatically switch to NORMAL mode. The left channel level detector output is also available at pin ENVOUT. An AGC correction voltage is added at this pin, such that the ENVOUT voltage indicates the left channel FM-carrier level even within the AGC-range. The ENVOUT voltage can be used for auto-tracking of the FM-audio heads.

In the event of drop-outs in the incoming FM signal, the left channel level detector is also used to activate the sample-and-hold. This drop-out cancellation is only active if bit DOC has been set.

6.3.3 Automatic calibration

By means of bit CALS the two integrated oscillators and bandpass filters can be calibrated in Loop-Through (LT) or record (REC) mode. Normally this will be done after start-up of the VCR. After setting of bit CALS the calibration procedure is automatically executed as shown in Fig.4. The calibration starts at the first negative edge of HID after CALS has been set. During the LOW period of HID (20 ms for PAL) the number of oscillator cycles is compared to a certain value stored in a Read Only Memory (ROM).

Therefore, the final oscillator frequency is proportional to the inverse of the HID LOW-time. This means that an error of 1 µs in the HID LOW-time will result in an additional frequency error of approximately 100 Hz. The maximum number of required HID cycles for one complete oscillator calibration is six, which is equal to 240 ms.

After both oscillators have been calibrated the bandpass filters are calibrated using the right channel oscillator as reference frequency generator (1.6 MHz for PAL). This will take <10 ms.

Bit CALR is set to 1 if the calibration has been executed successfully. CALR is 0 if:

- A Power-On Reset (POR) has occurred.
- The calibration is running.
- The initial oscillator and bandpass frequencies are too low or too high for a successful calibration.

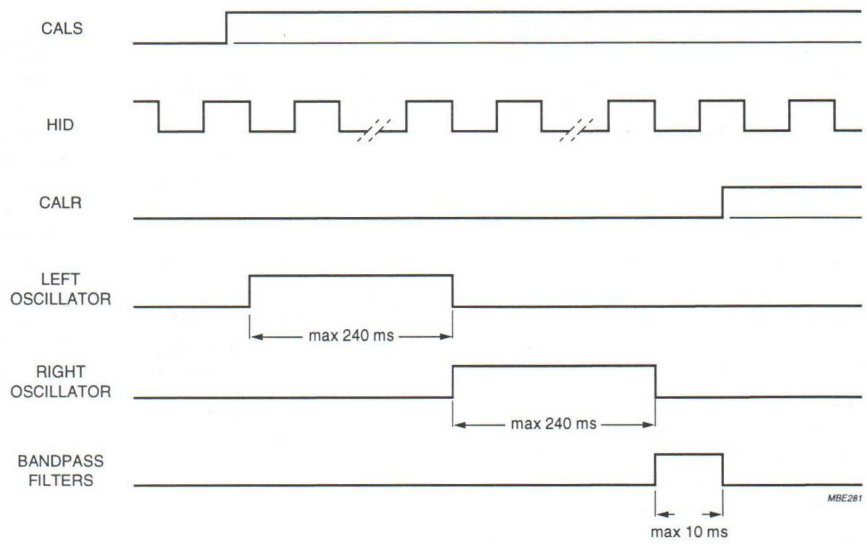


Fig.4 Timing diagram of automatic calibration.

If CALS is reset during CALR = 0, the calibration will be stopped if it was not finished yet. If required, a new calibration can be started using CALS.

WARNING: the IC should not be calibrated in a test or standby mode.

6.3.4 PAL/NTSC MODE

Depending on bit NTSC the IC is calibrated in PAL or NTSC mode using bit CALS. After an automatic calibration the oscillator frequencies can be switched between PAL and NTSC using bit NTSC. This centre frequency shift is done without automatic calibration. During playback (PB) or loop-through (LT) a change in bit NTSC will automatically calibrate the bandpass filters again. This will take <10 ms.

WARNING: A change of PB to REC, LT to REC and PAL to NTSC should not be combined in one transmitted byte. The PAL to NTSC transition should be preceded by the PB to REC or LT to REC transition.

6.4 I²C-bus

The TDA9614H is controlled via the 2-wire I²C-bus, in accordance with the I²C-bus specification. As slave receiver for programming there is one module address, with R/$\overline{W}$ bit = 0, a subaddress byte and eight data bytes. If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic address increment feature. As slave transmitter (R/$\overline{W}$ bit = 1) there is one read byte.

Table 5 TDA9614H addresses and data bytes

NAME	ADDRESS							
Slave address byte	1	0	1	1	1	0	0	R/$\overline{W}$
Subaddress bytes 00 to 07	0	0	0	0	0	X(1)	X(1)	X(1)
Control byte (subaddress 00)	RAF	IPAF	AFOM	NTSC	RN	IPN	NOM	LP
Main select byte (subaddress 01)	IS2	IS1	IS0	NS1	NS0	OSL	OSR	OSN
Secondary select byte (subaddress 02)	HSL	HSR	DCS	RFCM	LOS1	LOS0	DOS1	DOS0
Left volume byte (subaddress 03)	0	VLM	VL5	VL4	VL3	VL2	VL1	VL0
Right volume byte (subaddress 04)	0	VRM	VR5	VR4	VR3	VR2	VR1	VR0
Headphone volume byte (subaddress 05)	0	VHM	VH5	VH4	VH3	VH2	VH1	VH0
Install byte (subaddress 06)	DEV1	DEV0	NPL3	NPL2	NPL1	NPL0	AUTN	DOC
Test byte (subaddress 07)	STBY	CALS	AGCN	TST4	TST3	TST2	TST1	TST0
Read byte (address B9)	CALR	PAFM	1	POR	1	0	1	1

Note

1. These bits determine the subaddress.

6.5 Power-On Reset (POR); derived from digital supply voltage V_{DDD}

In the data byte descriptions [por] indicates the mode after POR. The status of the data bytes after POR is shown in Table 6.

Table 6 Status of data bytes after POR

DATA BYTE	ADDRESS							
Control byte	0	1	1	0	0	1	1	0
Main select byte	0	0	0	0	0	1	1	0
Secondary select byte	1	1	0	0	0	0	0	0
Left volume byte	0	0	1	1	0	0	0	1
Right volume byte	0	0	1	1	0	0	0	1
Headphone volume byte	0	0	1	0	1	1	1	1
Install byte	0	1	0	1	1	1	0	1
Test byte	0	0	0	0	0	0	0	0

A POR occurrence is signalled by bit POR in the read byte (see Table 39).

6.6 Control byte

Table 7 Bits of control byte

BIT	DESCRIPTION
RAF	Record Audio FM; see Table 8
IPAF	Inverse Playback Audio FM; see Table 8
AFOM	Audio FM Output Mute; see Table 9
NTSC	NTSC; television standard; see Table 10
RN	Record Normal; see Table 11
IPN	Inverse Playback Normal; see Table 11
NOM	Normal Output Mute; see Table 12
LP	Long Play mode; see Table 13

Table 8 Bits RAF and IPAF

RAF[1]	IPAF	MODE	DESCRIPTION
0	0	playback	NR and modem in playback mode
0	1	loop-through	NR in record mode; modem not active [por]
1	0	record[2]	NR and modem in record mode
1	1	record[2]	NR and modem in record mode

Notes

1. The RAF bit can be overruled externally by applying a low-ohmic voltage to the RAF I/O (pin 12) either logic 0 or logic 1 (0 or +5 V). The actual mode of the IC is determined by the level measured at this pin, enabling fast switching between record and playback/loop-through.
2. The two record modes are equal, only differing in their reaction to forcing RAF LOW at the RAF I/O pin; the status of the IPAF bit determines whether the IC is switched to the playback or loop-through mode.

Table 9 Bit AFOM

AFOM	MODE	DESCRIPTION
0	–	–
1	mute[1]	output from audio FM (NR) circuit is muted [por]

Note

1. Audio coming from the audio FM circuit is muted, either the signal from tape in playback or the loop-through signal in record or loop-through modes.

Table 10 Bit NTSC

NTSC	MODE	DESCRIPTION
0	PAL	modem and BPF set to PAL carrier frequencies [por]
1	NTSC	modem and BPF set to NTSC carrier frequencies

Table 11 Bits RN and IPN

RN[1]	IPN	MODE	DESCRIPTION
0	0	playback	linear audio circuit in playback mode
0	1	loop-through P	linear audio circuit in loop-through mode (playback ready) [por]
1	0	loop-through R[2]	linear audio circuit in loop-through mode (record ready)
1	1	record	linear audio circuit in record mode

Notes

1. Bit RN is output at LINREC (pin 32), which is used to drive an external (high voltage) head switch and possibly the bias oscillator. The two loop-through modes are equal in signal flow, however they differ in the state of the head switches (the internal switch at PBIN [pin 34] and the external head switch driven by pin LINREC).
2. Loop-through R is equal to record except for the RECOUT output (pin 33) which is muted.

Table 12 Bit NOM

NOM	MODE	DESCRIPTION
0	–	–
1	mute[1]	output from linear audio circuit is muted [por]

Note

1. Audio coming from the linear audio circuit is muted, either the signal from tape in playback or the loop-through signal in record or loop-through modes. To avoid clicks when changing the mode of the linear audio circuit to or from playback, the output should be muted shortly, using this bit.

Table 13 Bit LP

LP	MODE	DESCRIPTION
0	SP	Record and playback equalizing set for Standard Play [por]. Record equalization switch at EQSW (pin 30) and playback equalization switch at RESSW (pin 35) are open (high impedance). The internal playback equalizing is 3180 and 120 μs. It can be changed to 2544 and 96 μs by selecting test number 31 (see Section 6.12).
1	LP	Record and playback equalizing set for Long Play. Record equalization switch at EQSW (pin 30) and playback equalization switch at RESSW (pin 35) are closed. The internal playback equalizing is 3180 and 170 μs. It can be changed to 2731 and 146 μs by selecting test number 31 (see Section 6.12).

6.7 Main select byte

Table 14 Bits of main select byte

BIT	DESCRIPTION
IS2 to IS0	Input Select 2 to Input Select 0; see Table 15
NS1 and NS0	Normal Select 1 and Normal Select 0; see Table 16
OSL	Output Select Left; see Table 17
OSR	Output Select Right; see Table 17
OSN	Output Select Normal; see Table 17

Table 15 Bits IS2 to IS0; note 1

IS2	IS1	IS0	MODE	SELECTED INPUT SOURCE
0	0	0	Tuner	TUNL and TUNR [por]
0	0	1	Cinch	CINL and CINR
0	1	0	Ext1	EXT1L and EXT1R (e.g. SCART1; TV connector)
0	1	1	Ext2	EXT2L and EXT2R (e.g. SCART2; decoder connector)
1	0	0	Ext3	EXT3L and EXT3R (e.g. front cinch)
1	0	1	SAP	additional mono input (SAP; pin 1)
1	1	0	Normal[2]	output from linear audio (LININ; pin 28)
1	1	1	Dub Mix [2][3]	mixing of EXT3 input with hi-fi output signal

Notes

1. With bits IS2 to IS0, the stereo input signal is selected which is led to the hi-fi processing. One out of five stereo sources can be selected. The five stereo inputs differ in their connectivity; with bits NS1 and NS0 tuner left (TUNL; pin 2) can be selected as linear audio input source, with bits LOS1 and LOS0 Normal, Ext2 and Ext3 are directly connectable to Line out and to DOS1 and DOS0 Tuner, Ext1 and Ext3 are directly connectable to decoder out (2nd Line Out).
2. **Remark:** when using the selections Normal or Dub Mix be aware of signal loops (which should be avoided) because this can lead to large audio oscillations.
3. The selection Dub Mix is a special function in which a mono signal derived from the Ext3 inputs ($\frac{1}{2}$EXT3L + $\frac{1}{2}$EXT3R) is led to the left input and a mono signal derived from the audio FM output ($\frac{1}{2}$L + $\frac{1}{2}$R) is led to the right input channel. This function can be used for audio dubbing using the volume controls as a mixing desk.

Table 16 Bits NS1 and NS0; note 1

NS1	NS0	MODE	DESCRIPTION
0	0	Input	linear audio input source is equal to hi-fi input [por]
0	1	Volume	linear audio input source is equal to hi-fi input, inclusive volume control
1	0	SAP	additional mono input (SAP; pin 1) is selected
1	1	Tuner L	left channel of tuner input is selected

Note

1. With bits NS1 and NS0 the input signal is selected for the linear audio circuit. When a stereo input source is selected, a mono signal is made by adding the left and right channel. Furthermore two independent selections can be made (the mono input SAP or the left channel of tuner e.g. for dual language). If in the volume mode the built-in AGC circuit is switched off by using bit AGCN, the audio level can be controlled by the left and right volume controls (VLx and VRx).

Table 17 Bits OSL, OSR and OSN; note 1

OSL	OSR	OSN	MODE	DESCRIPTION
1	1	0	stereo	LEFT at left channel; RIGHT at right channel [por].
1	0	0	left	LEFT at both left and right channels.
0	1	0	right	RIGHT at both left and right channels.
0	0	0	mute	No selection.
1	1	1	mixed stereo	LEFT + NORMAL added at left channel; RIGHT + NORMAL added at right channel.
1	0	1	mixed left	LEFT + NORMAL added at both left and right channels.
0	1	1	mixed right	RIGHT + NORMAL added at both left and right channels.
0	0	1	normal	NORMAL (is linear audio) at both left and right channels.

Note

1. The bits OSL, OSR and OSN provide eight output select functions. LEFT and RIGHT are the left and right hi-fi channels; NORMAL is the linear audio channel (LININ; pin 28). This selection is normally output at line out (LINEL and LINER), RFCOUT (pin 18), decoder out (LINE2L and LINE2R), headphone out (HPOUTL and HPOUTR) and DC out (DCOUTL and DCOUTR). However line out can be overruled by bits LOS1 and LOS0; decoder out can be overruled by bits DOS1 and DOS0, headphone out (and DC out) can be overruled by bits HSL and HSR and DC out can be overruled by bit DCS.

Remark: if AUTN = 1 (see Section 6.11) the output select modes stereo, left and right will be forced to normal as long as the audio FM circuit is in playback mode and the internal PB mute signal is generated (no hi-fi track on tape). The status of this internal mute signal can be read by bit PAFM (see Section 6.13).

6.8 Secondary select byte

Table 18 Bits of secondary select byte

BIT	DESCRIPTION
HSL	Headphone Select Left; see Table 19
HSR	Headphone Select Right; see Table 19
DCS	DC Select; see Table 20
RFCM	RFC Mute; see Table 21
LOS1 and LOS0	Line Output Select 1 and Line Output Select 0; see Table 22
DOS1 and DOS0	Decoder Output Select 1 and Decoder Output Select 0; see Table 23

Table 19 Bits HSL and HSR

HSL	HSR	MODE	DESCRIPTION
1	1	outsel	Headphone signal set by the output selection [por].
1	0	left	LEFT at both headphone out left and right.
0	1	right	RIGHT at both headphone out left and right.
0	0	normal	NORMAL (is linear audio) at both headphone outputs.

Normally the headphone output signal is set by the output selection OSL, OSR and OSN (see Table 17). Furthermore three independent selections can be made: LEFT hi-fi channel, RIGHT hi-fi channel (language selection) and NORMAL (e.g. monitoring an audio dubbing recording). These headphone selections are also active for the VU meter output (DC out), unless bit DCS = 1.

Table 20 Bit DCS

DCS	MODE	DESCRIPTION[1]
0	headphone	DC output is set by Headphone Select [por].
1	stereo	DC output is hi-fi stereo.

Note

1. The signal at DC out (DCOUTL and DCOUTR; pins 23 and 24) is normally the signal which can be listened to by the headphone. For use in concepts with digital AGC (using the DC output signal to control the left and right volume settings), an independent selection to hi-fi stereo can be made.

Table 21 Bit RFCM

RFCM	MODE	DESCRIPTION[1]
0	–	[por]
1	mute[1]	RF converter output signal muted

Note

1. The audio signal at RF converter out (a mono version of the signal selected with the output select with overload AGC) can be independently muted.

Table 22 Bits LOS1 and LOS0; note 1

LOS1	LOS0	MODE	DESCRIPTION
0	0	Outsel	Line output selection is set by output select function [por].
0	1	Normal	Linear audio is connected to line output.
1	0	Ext2	Ext2 input is directly connected to line output.
1	1	Ext3	Ext3 input is directly connected to line output.

Note

1. With the line output select some special connections can be made overruling the output select (OSL, OSR and OSN), e.g. for connecting a decoder box (for a pay-TV channel) to a television set via the VCR.

Table 23 Bits DOS1 and DOS0; note 1

DOS1	DOS0	MODE	DESCRIPTION
0	0	Outsel	Decoder output selection is set by output select function [por].
0	1	Tuner	Tuner input is directly connected to decoder output.
1	0	Ext1	Ext1 input is directly connected to decoder output.
1	1	Ext3	Ext3 is directly connected to decoder output.

Note

1. With the decoder output select some special connections can be made overruling the output select (OSL, OSR and OSN), e.g. for connecting a decoder box to the VCR.

6.9 Left/Right (L/R) volume byte

Table 24 Bits of Left/Right volume byte

BIT	DESCRIPTION
VLM	Volume Left Mute; see Table 25
VL5 to VL0	Volume Left 5 to Volume Left 0; see Table 25
VRM	Volume Right Mute; see Table 25
VR5 to VR0	Volume Right 5 to Volume Right 0; see Table 25

Table 25 Left/Right volume byte; notes 1 and 2

VLM	VL5	VL4	VL3	VL2	VL1	VL0	MODE
VRM	VR5	VR4	VR3	VR2	VR1	VR0	
1	X	X	X	X	X	X	mute
0	0	0	0	0	0	0	–49 dB
0	0	0	0	0	0	1	–48 dB
0	0	0	0	0	1	0	–47 dB
0	0	0	0	0	1	1	–46 dB
0	0	0	0	1	0	0	–45 dB
0	0	0	0	1	0	1	–44 dB
0	0	0	0	1	1	0	–43 dB
0	0	0	0	1	1	1	–42 dB
0	0	0	1	0	0	0	–41 dB
0	0	0	1	0	0	1	–40 dB
0	0	0	1	0	1	0	–39 dB
0	0	0	1	0	1	1	–38 dB
0	0	0	1	1	0	0	–37 dB
0	0	0	1	1	0	1	–36 dB
0	0	0	1	1	1	0	–35 dB
0	0	0	1	1	1	1	–34 dB
0	0	1	0	0	0	0	–33 dB
0	0	1	0	0	0	1	–32 dB
0	0	1	0	0	1	0	–31 dB

VLM	VL5	VL4	VL3	VL2	VL1	VL0	MODE
VRM	VR5	VR4	VR3	VR2	VR1	VR0	
0	0	1	0	0	1	1	–30 dB
0	0	1	0	1	0	0	–29 dB
0	0	1	0	1	0	1	–28 dB
0	0	1	0	1	1	0	–27 dB
0	0	1	0	1	1	1	–26 dB
0	0	1	1	0	0	0	–25 dB
0	0	1	1	0	0	1	–24 dB
0	0	1	1	0	1	0	–23 dB
0	0	1	1	0	1	1	–22 dB
0	0	1	1	1	0	0	–21 dB
0	0	1	1	1	0	1	–20 dB
0	0	1	1	1	1	0	–19 dB
0	0	1	1	1	1	1	–18 dB
0	1	0	0	0	0	0	–17 dB
0	1	0	0	0	0	1	–16 dB
0	1	0	0	0	1	0	–15 dB
0	1	0	0	0	1	1	–14 dB
0	1	0	0	1	0	0	–13 dB
0	1	0	0	1	0	1	–12 dB
0	1	0	0	1	1	0	–11 dB
0	1	0	0	1	1	1	–10 dB
0	1	0	1	0	0	0	–9 dB
0	1	0	1	0	0	1	–8 dB
0	1	0	1	0	1	0	–7 dB
0	1	0	1	0	1	1	–6 dB
0	1	0	1	1	0	0	–5 dB
0	1	0	1	1	0	1	–4 dB
0	1	0	1	1	1	0	–3 dB
0	1	0	1	1	1	1	–2 dB
0	1	1	0	0	0	0	–1 dB
0	1	1	0	0	0	1	0 dB [por]
0	1	1	0	0	1	0	1 dB
0	1	1	0	0	1	1	2 dB
0	1	1	0	1	0	0	3 dB
0	1	1	0	1	0	1	4 dB
0	1	1	0	1	1	0	5 dB
0	1	1	0	1	1	1	6 dB
0	1	1	1	0	0	0	7 dB
0	1	1	1	0	0	1	8 dB

VLM	VL5	VL4	VL3	VL2	VL1	VL0	MODE
VRM	VR5	VR4	VR3	VR2	VR1	VR0	
0	1	1	1	0	1	0	9 dB
0	1	1	1	0	1	1	10 dB
0	1	1	1	1	0	0	11 dB
0	1	1	1	1	0	1	12 dB
0	1	1	1	1	1	0	13 dB
0	1	1	1	1	1	1	14 dB

Notes

1. X = don't care.
2. Optimum mute performance is achieved by combination of the mute bit (VLM and/or VRM) with the smallest volume setting (Vx5 to Vx0 = '000000').

6.10 Headphone volume byte

Table 26 Bits of Left/Right volume byte

BIT	DESCRIPTION
VHM	Volume Headphone Mute; see Table 27
VH5 to VH0	Volume Headphone 5 to Volume Headphone 0; see Table 27

Table 27 Headphone volume byte; notes 1 and 2

VHM	VH5	VH4	VH3	VH2	VH1	VH0	MODE
1	X	X	X	X	X	X	mute
0	0	0	0	0	0	0	–47 dB
0	0	0	0	0	0	1	–46 dB
0	0	0	0	0	1	0	–45 dB
0	0	0	0	0	1	1	–44 dB
0	0	0	0	1	0	0	–43 dB
0	0	0	0	1	0	1	–42 dB
0	0	0	0	1	1	0	–41 dB
0	0	0	0	1	1	1	–40 dB
0	0	0	1	0	0	0	–39 dB
0	0	0	1	0	0	1	–38 dB
0	0	0	1	0	1	0	–37 dB
0	0	0	1	0	1	1	–36 dB
0	0	0	1	1	0	0	–35 dB
0	0	0	1	1	0	1	–34 dB
0	0	0	1	1	1	0	–33 dB
0	0	0	1	1	1	1	–32 dB
0	0	1	0	0	0	0	–31 dB
0	0	1	0	0	0	1	–30 dB
0	0	1	0	0	1	0	–29 dB

VHM	VH5	VH4	VH3	VH2	VH1	VH0	MODE
0	0	1	0	0	1	1	−28 dB
0	0	1	0	1	0	0	−27 dB
0	0	1	0	1	0	1	−26 dB
0	0	1	0	1	1	0	−25 dB
0	0	1	0	1	1	1	−24 dB
0	0	1	1	0	0	0	−23 dB
0	0	1	1	0	0	1	−22 dB
0	0	1	1	0	1	0	−21 dB
0	0	1	1	0	1	1	−20 dB
0	0	1	1	1	0	0	−19 dB
0	0	1	1	1	0	1	−18 dB
0	0	1	1	1	1	0	−17 dB
0	0	1	1	1	1	1	−16 dB
0	1	0	0	0	0	0	−15 dB
0	1	0	0	0	0	1	−14 dB
0	1	0	0	0	1	0	−13 dB
0	1	0	0	0	1	1	−12 dB
0	1	0	0	1	0	0	−11 dB
0	1	0	0	1	0	1	−10 dB
0	1	0	0	1	1	0	−9 dB
0	1	0	0	1	1	1	−8 dB
0	1	0	1	0	0	0	−7 dB
0	1	0	1	0	0	1	−6 dB
0	1	0	1	0	1	0	−5 dB
0	1	0	1	0	1	1	−4 dB
0	1	0	1	1	0	0	−3 dB
0	1	0	1	1	0	1	−2 dB
0	1	0	1	1	1	0	−1 dB
0	1	0	1	1	1	1	0 dB [por]
0	1	1	0	0	0	0	1 dB
0	1	1	0	0	0	1	2 dB
0	1	1	0	0	1	0	3 dB
0	1	1	0	0	1	1	4 dB
0	1	1	0	1	0	0	5 dB
0	1	1	0	1	0	1	6 dB
0	1	1	0	1	1	0	7 dB
0	1	1	0	1	1	1	8 dB
0	1	1	1	0	0	0	9 dB
0	1	1	1	0	0	1	10 dB
0	1	1	1	0	1	0	11 dB
0	1	1	1	0	1	1	12 dB

VHM	VH5	VH4	VH3	VH2	VH1	VH0	MODE
0	1	1	1	1	0	0	13 dB
0	1	1	1	1	0	1	14 dB
0	1	1	1	1	1	0	15 dB
0	1	1	1	1	1	1	16 dB

Notes

1. X = don't care.
2. Optimum mute performance is achieved by combination of the mute bit (VHM) with the smallest volume setting (VH5 to VH0 = '000000').

6.11 Install byte

Table 28 Bits of install byte

BIT	DESCRIPTION
DEV1 and DEV0	Deviation 1 and Deviation 0; see Table 29
NPL3 to NPL0	Normal Playback Level 3 to Normal Playback Level 0; see Table 30
AUTN	Auto Normal; see Table 31
DOC	Drop-out Cancellation; see Table 32

Table 29 Bits DEV1 and DEV0; note 1

DEV1	DEV0	MODE	DESCRIPTION
0	0	56 kHz	deviation of modem set to 56 kHz (equals 50 kHz; –10 dBV); 1 kHz audio
0	1	50 kHz	deviation of modem set to 50 kHz (equals 50 kHz; –8 dBV); 1 kHz audio
1	0	45 kHz	deviation of modem set to 45 kHz (equals 50 kHz; –6 dBV); 1 kHz audio
1	1	40 kHz	deviation of modem set to 40 kHz (equals 50 kHz; –4 dBV); 1 kHz audio

Note

1. A selection of four different settings of FM deviation/audio level can be made for the audio FM circuit.

Table 30 Normal Playback Level bits; note 1

NPL3	NPL2	NPL1	NPL0	MODE
0	0	0	0	−7 dB
0	0	0	1	−6 dB
0	0	1	0	−5 dB
0	0	1	1	−4 dB
0	1	0	0	−3 dB
0	1	0	1	−2 dB
0	1	1	0	−1 dB
0	1	1	1	0 dB [por]
1	0	0	0	1 dB
1	0	0	1	2 dB
1	0	1	0	3 dB
1	0	1	1	4 dB
1	1	0	0	5 dB
1	1	0	1	6 dB
1	1	1	0	7 dB
1	1	1	1	8 dB

Note

1. A selection of 16 settings of amplification in the linear audio playback amplifier can be made. This can be used for adjustment purposes or as a fixed setting.

Table 31 Bit AUTN; note 1

AUTN	MODE	DESCRIPTION
0	–	Audio FM signal is muted, when no hi-fi tracks are found in playback [por].
1	auto normal	Output select is switched to normal, when no hi-fi tracks are found in playback.

Note

1. When the audio FM circuit is in playback and there is no FM input signal (playback of a conventional recording) the audio FM circuitry is muted. If this situation occurs and AUTN = 1 the selections stereo, left or right in the output select (OSR, OSL and OSN) are overridden and the selection normal is made. This means that linear audio is the output signal for as long as the internal playback mute is active. The status of this internal mute signal can be read by bit PAFM (see Section 6.13).

Table 32 Bit DOC

DOC	MODE	DESCRIPTION
0	–	–
1	drop-out cancel(1)	audibility of short drop-outs is minimized [por]

Note

1. When DOC = 1 an additional sample-and-hold circuit is activated during drop-outs in the FM input signal, minimizing their audibility.

6.12 Test byte

Table 33 Bits of test byte

BIT	DESCRIPTION
STBY	Standby; see Table 34
CALS	Calibration Start; see Table 35
AGCN	AGC Not; see Table 36
TST4 to TST0	Test 4 to Test 0; see Table 37

Table 34 Bit STBY

STBY	MODE	DESCRIPTION
0	–	normal operation [por]
1	standby(1)	standby mode (low power consumption)

Note

1. When STBY = 1 the IC is partly switched off to minimize its power consumption. The I^2C-bus and the direct connections between inputs and outputs (selectable with bits: LOS1, LOS0, DOS1 and DOS0) are still operable in standby mode.

Table 35 Bit CALS

CALS	MODE	DESCRIPTION
0	–	[por]
1	auto-calibrate(1)	oscillators and BPFs are automatically calibrated

Note

1. When CALS is made logic 1 after being logic 0 the IC performs an automatic frequency calibration of the modem CCOs and the built-in bandpass filters (BPFs). During calibration, the IC should be in record or loop-through mode. The calibration takes <500 ms and uses the HID input (25 Hz in PAL mode or 30 Hz in NTSC mode) as the reference frequency. The bit CALR (see Section 6.13) can be read to check if the calibration has been completed successfully.

Table 36 Bit AGCN; note 1

AGCN	MODE	DESCRIPTION
0	AGC on	linear audio record; AGC active [por]
1	AGC off	linear audio record; AGC inactive

Note

1. With bit AGCN the linear audio record AGC can be switched (off and on).

Table 37 Test bits TST4 to TST0; note 1

TST4	TST3	TST2	TST1	TST0	MODE	DESCRIPTION
0	0	0	0	0	–	[por]
0	0	0	0	1	VCO test L	in record mode: only 1.4 or 1.3 MHz at FMOUT
0	0	0	1	0	VCO test R	in record mode: only 1.8 or 1.7 MHz at FMOUT
0	0	0	1	1	BPF test L	in playback mode: only left BPF at FMOUT; HF AGC switched off
0	0	1	0	0	BPF test R	in playback mode: only right BPF at FMOUT; HF AGC switched off
0	0	1	0	1	Test	not for application
0	0	1	1	0	Test	not for application
0	0	1	1	1	Test	not for application
0	1	0	0	0	Test	not for application
0	1	0	0	1	Test	not for application
0	1	0	1	0	Test	not for application
0	1	0	1	1	Test	not for application
0	1	1	0	0	Test	not for application
0	1	1	0	1	Test	not for application
0	1	1	1	0	Test	not for application
0	1	1	1	1	Test	not for application
1	0	0	0	0	Test	not for application
1	0	0	0	1	Test	not for application
1	0	0	1	0	Test	not for application
1	0	0	1	1	Test	not for application
1	0	1	0	0	Test	not for application
1	0	1	0	1	Test	not for application
1	0	1	1	0	Test	not for application
1	0	1	1	1	Test	not for application
1	1	0	0	0	Test	not for application
1	1	0	0	1	Test	not for application
1	1	0	1	0	Test	not for application
1	1	0	1	1	Test	not for application
1	1	1	0	0	Test	not for application
1	1	1	0	1	Test	not for application
1	1	1	1	0	Test	not for application
1	1	1	1	1	EQ set[2]	linear audio playback equalization using non-standard settings

Notes

1. The bits TST4 to TST0 are used for testing and measurement purposes.
2. Test number 31 (TST4 to TST0 = 11111) is a special setting which can be used to change the internal linear audio playback equalization to non-standard settings as shown in Table 38.

Table 38 Linear audio playback equalization non-standard settings

SETTING	MODE	TEST NUMBER 31
Standard play (LP = 0)	3180 and 120 µs	not selected
	2544 and 96 µs	selected
Long play (LP = 1)	3180 and 170 µs	not selected
	2731 and 146 µs	selected

6.13 Read byte

Table 39 Bits of read byte

BIT	DESCRIPTION
CALR	Calibration ready; see Table 40
PAFM	Playback Audio FM Mute; see Table 41
POR	Power-On reset; see Table 42

Table 40 Bit CALR; note 1

CALR	MODE	DESCRIPTION
0	not calibrated	IC has not been auto-calibrated [por].
1	calibrated	IC has been calibrated successfully.

Note

1. If CALR = 0, bandpass filters and oscillators have not been calibrated successfully. When an automatic calibration is started by bit CALS, the end of the calibration cycle can be checked via this bit. If for some reason a successful calibration can not be made within the available adjustment range, e.g. if no HID signal is available, CALR will remain logic 0. After calibration the adjustment will be held for as long as the digital supply voltage (V_{DDD}) is available.

Table 41 Bit PAFM; note 1

PAFM	MODE	DESCRIPTION
0	AFM available	Audio FM signal is detected at FM input.
1	no AFM carrier	No audio FM signal detected; hi-fi processing is muted.

Note

1. When the hi-fi processing is in playback mode but no Audio FM input signal is found, the IC generates an internal mute signal which mutes the noise signal coming from the demodulators. The status of this mute signal can be read via bit PAFM. This signal however is only valid with the hi-fi circuit in playback (RAF = 0 and IPAF = 0).

Table 42 Bit POR; note 1

POR	MODE	DESCRIPTION
0	–	–
1	POR generated	POR pulse is generated since last read.

Note

1. When the IC is switched on, or a power dip occurs on the digital supply (V_{DDD}) line, a Power-on Reset signal is generated which resets the IC's I^2C-bus registers and the auto-calibration circuit. If such a situation has occurred after the last time the read byte has been read, bit POR = 1. After reading the read byte POR is reset to logic 0.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1		0	13.2	V
V_{DDA2}	analog supply voltage 2		0	5.5	V
V_{DDD}	digital supply voltage		0	5.5	V
V_n	voltage on pins:				
	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 28, 41, 44, 51, 52, 63 and 64		0	7.7	V
	56, 60 and 62		0	V_{DDA2}	V
	12 and 32		0	V_{DDD}	V
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{es}	electrostatic handling	MM; note 1	−150	+150	V
		HBM; note 2	−1500	+1500	V

Notes

1. Machine Model (MM).
2. Human Body Model (HBM).

8 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W

9 DC CHARACTERISTICS

V_{DDA1} = 12 V; V_{DDA2} = 5 V; V_{DDD} = 5 V; NTSC = 0; LP = 0; CALR = 1; T_{amb} = 25 °C;
all volume control levels set to 0 dB; measured in test circuit (see Fig.13); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Supply voltages						
V_{DDA1}	analog supply voltage 1; pin 50		10.5	12	13.2	V
V_{DDA2}	analog supply voltage 2; pin 58		4.75	5	5.5	V
V_{DDD}	digital supply voltage; pin 13		4.75	5	5.5	V
Supply currents						
I_{DDA1}	analog supply current 1; pin 50	operating	–	47	60	mA
		standby	–	28	35	mA
I_{DDA2}	analog supply current 2; pin 58	record[1]; LT[2]	–	7	9	mA
		playback[3]	–	18	23	mA
		standby; LT[2]	–	3	5	mA
I_{DDD}	digital supply current; pin 13	operating	–	1	3	mA
		standby	–	1	3	mA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Input voltages						
V_I	DC input voltage; pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 28, 31, 34, 35 and 36		–	3.8	–	V
V_{57}	DC input voltage internally generated; pin 57		–	1.9	–	V
V_{30}	DC input voltage internally generated; pin 30		–	0	–	V
$V_{51,64}$	DC input voltage internally generated; pins 51 and 64	playback(3)	–	3.8	–	V
$V_{52,63}$	DC input voltage internally generated; pins 52 and 63	record(1); LT(2)	–	3.8	–	V
Output voltages						
V_O	DC output voltage:					
	pins 19, 20, 21, 22 and 33		–	6	–	V
	pins 25 and 26		–	5.5	–	V
	pins 18, 29, 42, 53 and 59		–	3.8	–	V
	pin 56	record(1)	–	1.2	–	V
	pin 56	playback(3); LT(2)	–	1.2	–	V
	pin 55		–	0.6	–	V
	pins 51 and 64	record(1); LT(2)	–	4.3	–	V
	pins 52 and 63	playback(3)	–	3.3	–	V
Head identification pulse input (HID; pin 61)						
V_{IH}	HIGH level input voltage		2.75	–	5.50	V
V_{IL}	LOW level input voltage		0	–	2.25	V
Normal record pin (LINREC; pin 32)						
V_{OH}	HIGH level output voltage	I_L = –500 µA	V_{DDD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_L = 500 µA	–	–	0.5	V
I/O RAF (pin 12)						
USED AS OUTPUT						
V_{OH}	HIGH level output voltage	RAF = 1; I_L = –35 µA	V_{DDD} – 0.25	–	V_{DDD}	V
V_{OL}	LOW level output voltage	RAF = 0; I_L = 185 µA	0	–	0.4	V
I_{OH}	HIGH level output current (drive capability)	RAF = 1	–35	–	–	µA
I_{OL}	LOW level output current (drive capability)	RAF = 0	185	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
USED AS INPUT (OUTPUT OVERRULED)						
V_{IH}	HIGH level input voltage		3.5	–	V_{DDD}	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current	at V_{IH}	–	–	345	μA
I_{IL}	LOW level input current	at V_{IL}	–	–	−65	μA

Notes

1. Record: record audio FM and record linear audio.
2. Loop-through: loop-through audio FM and loop-through R linear audio.
3. Playback: playback audio FM and playback linear audio.

10 AC CHARACTERISTICS

10.1 Record audio FM mode

Audio input signal −8 dBV from TUNL and TUNR (pins 2 and 3); V_{DDA1} = 12 V; V_{DDA2} = 5 V; V_{DDD} = 5 V; NTSC = 0; LP = 0; CALR = 1; f = 1 kHz (audio test frequency); T_{amb} = 25 °C; all volume control levels set to 0 dB; measured in test circuit (see Fig.13); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Audio inputs (SAP, TUNL, TUNR, CINL, CINR, EXT1L, EXT1R, EXT2L, EXT2R, EXT3L and EXT3R; pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 and 11)						
R_i	input resistance		100	130	–	kΩ
V_{iAF}	audio input voltage		–	–	8	dBV
Line and decoder outputs (LINEL, LINER, LINE2L and LINE2R; pins 21, 22, 19 and 20)						
$V_{o(max)}$	maximum output voltage		−9	−8	−7	dBV
		THD = 1%; R_L = 5 kΩ; C_L = 2.2 nF; TUNL ≤ −3 dBV; TUNR ≤ −3 dBV; note 1	10	11	–	dBV
R_o	output resistance		–	200	275	Ω
THD	total harmonic distortion		–	0.01	0.1	%
V_n	noise level	f_i = 300 Hz to 20 kHz; TUNL and TUNR AC grounded	–	−91	−87	dBV
α_{cb}	channel balance		−1	0	+1	dB
V_{mute}	volume mute level		–	−100	−80	dBV
α_{ct}	crosstalk between channels	one channel driven	–	−83	−78	dBV
f_{res}	frequency response with respect to 1 kHz; low-pass filter transfer	f_i = 20 kHz	−0.5	−0.1	+0.5	dB
		f_i = 60 kHz	–	−12	−5	dB
$\alpha_{ct(max)}$	maximum audio input crosstalk	−8 dBV at a not selected stereo audio input	–	−90	–	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
VU meter drive (DCOUTL and DCOUTR; pins 23 and 24); square root of output voltage (see Fig.7)						
V_o	output voltage		1.69	1.8	1.91	V
R_o	output resistance		–	100	–	Ω
V_o	output voltage at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	V_{DDD} – 0.5	–	V_{DDD}	V
V_{oz}	output voltage for zero-level input		–	–	300	mV
α_{cb}	channel balance		–0.11	–	+0.11	dB
RF converter drive output; mono RFCOUT; pin 18 (see Fig.8)						
V_o	output voltage		–9	–8	–7	dBV
R_o	output resistance		–	100	–	Ω
THD	total harmonic distortion		–	0.01	–	%
V_o	output voltage at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–5	–3	–1	dBV
THD	total harmonic distortion at maximum record level	TUNL = –3 dBV; TUNR = –3 dBV; note 1	–	0.3	–	%
Headphone outputs (HPOUTL and HPOUTR; pins 25 and 26); headphone volume set to 0 dB						
V_o	output voltage		–9	–8	–7	dBV
R_o	output resistance		–	1	–	Ω
THD	total harmonic distortion		–	0.01	0.1	%
$V_{o(max)}$	maximum output voltage	THD = 1%; TUNL ≤ –3 dBV; TUNR ≤ –3 dBV; R_L = 250 Ω; note 1	9.0	9.5	–	dBV
V_n	noise level	f_i = 300 Hz to 20 kHz; tuner AC grounded	–	–90	–80	dBV
α_{ct}	crosstalk between channels	one channel driven	–	–83	–70	dBV
V_{mute}	headphone volume mute level		–	–90	–70	dBV
α_{cb}	channel balance		–1	–	+1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Audio outputs (AFNL and AFNR; pins 64 and 51); audio output from noise reduction						
V_{oAF}	audio output voltage		−12.5	−11.5	−10.5	dBV
THD	total harmonic distortion		–	0.12	0.3	%
V_{oAF}	audio output voltage at maximum record level	TUNL = −3 dBV; TUNR = −3 dBV; note 1	−3.5	−2	−0.5	dBV
THD	total harmonic distortion at maximum record level	TUNL = −3 dBV; TUNR = −3 dBV; note 1	–	0.2	3	%
V_n	noise level	f_i = 300 Hz to 20 kHz; tuner AC grounded	–	−54	−52	dBV
α_{cb}	channel balance		−1	–	+1	dB
L	linearity	V_i = −8 to −68 dBV	28.5	30	31.5	dB
α_{cc}	channel crosstalk	one channel driven	–	−58	−50	dBV
t_{att}	attack time according VHS		–	5	–	ms
t_{rec}	recovery time according VHS		–	70	–	ms
V_{mute}	mute level	MUTE = 1	–	−52	–	dBV
	frequency response with respect to 1 kHz; output level	f_i = 300 Hz	−0.9	−0.2	+0.5	dB
		f_i = 10 kHz	2.9	3.9	4.9	dB
FM modulator (audio input from AFML and AFMR; pins 63 and 52)						
THD	total harmonic distortion	Δf = 50 kHz	–	0.1	0.2	%
Δf	FM frequency deviation	V_{iAF} = −11.5 dBV; NTSC = 0	45	50	55	kHz
		V_{iAF} = −11.5 dBV; NTSC = 1	45	50	55	kHz
		audio input signal from NR outputs AFNL and AFNR; NTSC = 0	44.5	50	56.1	kHz
		audio input signal from NR outputs AFNL and AFNR; NTSC = 1	44.5	50	56.1	kHz
Δf_{max}	maximum FM frequency deviation		140	150	160	kHz
f_{oL}	FM centre frequency left	f = 1.4 MHz; NTSC = 0; calibrated in PAL mode	1395	1400	1405	kHz
		f = 1.3 MHz; NTSC = 1; calibrated in NTSC mode	1295	1300	1305	kHz
		NTSC = 1; calibrated in PAL mode	–	1300	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
f_{oR}	FM centre frequency right	f = 1.8 MHz; NTSC = 0; calibrated in PAL mode	1795	1800	1805	kHz
		f = 1.7 MHz; NTSC = 1; calibrated in NTSC mode	1695	1700	1705	kHz
		NTSC = 1; calibrated in PAL mode	–	1700	–	kHz
TC	temperature coefficient		–	±50	–	10^{-6}/K
HF output stage (FMOUT; pin 56)						
$V_{oR(p-p)}$	right output voltage (peak-to-peak value)	f_{oR} = 1.8 MHz; 1st harmonic	455	510	572	mV
		f_{oR} = 1.7 MHz; 1st harmonic	455	510	572	mV
$V_{oL(p-p)}$	left output voltage (peak-to-peak value)	f_{oL} = 1.4 MHz; 1st harmonic	152	170	190	mV
		f_{oL} = 1.3 MHz; 1st harmonic	152	170	190	mV
$\frac{V_{oR}}{V_{oL}}$	ratio of output voltages		2.7	3	3.3	
α_{3rd}	3rd harmonic suppression	NTSC = 0	20	30	–	dB
		NTSC = 1	18	28	–	dB
R_o	output resistance		–	100	130	Ω

Note

1. Record volume control for left and right channel set to maximum (+14 dB). Headphone volume control at 0 dB.

10.2 Record linear audio mode

Audio input signal –8 dBV from SAP, TUNL and TUNR (pins 1, 2 and 3); NormSel is input; OutSel is normal.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear audio playback input; PBIN (pin 34)						
Z_i	input impedance	I_L = ±1 mA	–	7	15	Ω
Linear audio EQSW input (pin 30)						
Z_i	input impedance	LP = 0	100	150	–	kΩ
		LP = 1	–	15	30	Ω
Line output (pins 21 and 22)						
V_o	output voltage	AGCN = 0; note 1	–8	–6	–4	dBV
		AGCN = 1; NormSel = volume; note 1	–10	–8	–6	dBv
α_{ct}	crosstalk (linear to stereo)	OutSel = stereo; NormSel = SAP; TUNL and TUNR AC grounded	–	–88	–80	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear audio record output RECOUT; pin 33 (see Fig.11)						
V_o	output voltage	AGCN = 0; note 1	−2	0	+2	dBV
		AGCN = 1; NormSel = volume; note 1	−4	−2	0	dBv
THD	total harmonic distortion	AGCN = 1; NormSel = volume	–	0.02	0.5	%
V_n	noise level	AGCN = 1; TUNL and TUNR AC grounded	–	−80	−70	dBV
Z_o	output impedance		–	100	200	Ω
V_{mute}	mute level	loop-through R; NOM = mute	–	−85	–	dBV
Linear audio RECEQ (pin 31)						
Z_t	transfer impedance	note 2	900	1200	1500	Ω

Notes

1. Using AGC on (AGCN = 0) and NormSel set to volume mode. The AGC gain is 1 dB higher for audio signals below the AGC clip level (specified value of AGC clip level does not change).

   Using AGC off (AGCN = 1) and NormSel not set to volume mode, the output signal is 1 dB lower (1 dB below the specified value).

2. The transfer A of the REC equalizer from LININ to RECOUT is: $A = \frac{(R+Z)}{Z} \times 3.98$

   where Z is the (complex) impedance at pin RECEQ to ground and R is the specified resistance of 1200 Ω.

10.3 Playback Audio FM mode

Audio output signal from the FM (de)modulator at AFML and AFMR (pins 63 and 52).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Bandpass filters (filter curves measured using test numbers 3 and 4 [HF AGC off])						
$V_{o(rms)}$	output voltage level at FMOUT (RMS value)	$V_{iHF(rms)}$ = 30 mV; 1.3 MHz BPF	105	150	215	mV
		$V_{iHF(rms)}$ = 30 mV; 1.4 MHz BPF	105	150	215	mV
		$V_{iHF(rms)}$ = 30 mV; 1.7 MHz BPF	105	150	215	mV
		$V_{iHF(rms)}$ = 30 mV; 1.8 MHz BPF	105	150	215	mV
	1.4 MHz BPF	1.0 MHz/1.4 MHz	–	−30	−20	dB
		1.25 MHz/1.4 MHz	−6	−3	–	dB
		1.55 MHz/1.4 MHz	−7	−3	–	dB
		1.65 MHz/1.4 MHz	–	−17	−12	dB
		1.55 MHz/1.65 MHz	10	15	–	dB
		1.8 MHz/1.4 MHz	–	–	−30	dB

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
	1.8 MHz BPF	1.4 MHz/1.8 MHz	–	–	–30	dB
		1.55 MHz/1.8 MHz	–	–17	–10	dB
		1.65 MHz/1.8 MHz	–7	–3	–	dB
		1.95 MHz/1.8 MHz	–3	0	–	dB
		2.2 MHz/1.8 MHz		–25	–15	dB
	1.3 MHz BPF	1.45 MHz/1.3 MHz	–7	–3	–	dB
		1.55 MHz/1.3 MHz	–	–17	–12	dB
		1.45 MHz/1.55 MHz	10	15	–	dB
	1.7 MHz BPF	1.45 MHz/1.7 MHz	–	–17	–10	dB
		1.55 MHz/1.7 MHz	–7	–3	–	dB
		1.55 MHz/1.45 MHz	10	15	–	dB
f_{shift}	frequency shift of BPF curve with temperature	T_{amb} = 0 to 70 °C	–	10	–	kHz
HF AGC						
$V_{i\ max(p-p)}$	maximum input signal level (peak-to-peak value)	1.4 and 1.8 MHz carrier added	–	–	1.25	V
$V_{oL(rms)}$	left BPF output voltage level (RMS value)	f_i = 1.4 MHz at FMIN; $V_{iHF(rms)}$ = 4 mV	13	19	28	mV
		f_i = 1.4 MHz at FMIN; $V_{iHF(rms)}$ = 25 mV	84	120	170	mV
		f_i = 1.4 MHz at FMIN; $V_{iHF(rms)}$ = 125 mV	84	120	170	mV
$V_{oR(rms)}$	right BPF output voltage level (RMS value)	f_i = 1.8 MHz at FMIN; $V_{iHF(rms)}$ = 4 mV	13	19	28	mV
		f_i = 1.8 MHz at FMIN; $V_{iHF(rms)}$ = 25 mV	84	120	170	mV
		f_i = 1.8 MHz at FMIN; $V_{iHF(rms)}$ = 125 mV	84	120	170	mV
B	–3 dB bandwidth	$V_{iHF(rms)}$ = 75 mV; 1.4 MHz carrier	–	10	–	kHz
PLL FM demodulator and limiter						
α_{AM}	AM rejection	$V_{iHF(rms)}$ = 2 to 200 mV; m = 30%	–	–70	–	dBV
$V_{i(rms)}$	sensitivity; PLL locked (RMS value)	Δf = 150 kHz; S/N = 35 dB (audio)	–	0.6	1.25	mV
THD	total harmonic distortion	Δf = 50 kHz	–	0.03	0.3	%
		Δf = 150 kHz	–	0.2	1.5	%
S/N	signal-to-noise ratio	V_{iHF} = 30 mV; Δf = 50 kHz	54	57	–	dB
V_{oAF}	AF output voltage	Δf = 50 kHz	–12.5	–11.5	–10.5	dBV
V_{step}	step response	note 1	–	–	–48	dBV
α_{ct}	crosstalk between channels	L to R; R to L	–	–90	–	dBV

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Sample-and-hold (see Fig.9)						
t_h	hold time pulse width		5	6	7	µs
d_{AF}	audio distortion	note 2	–	–	–75	dB
t_d	delay from HID pulse to hold pulse		–	0.4	–	µs
Drop-Out Cancellation (DOC)						
	DOC activation level w.r.t. mute activation level		–7	–4	–2	dB
$t_{d(off)}$	switch-off delay time	no signal to signal	5	9	14	µs
Mute timing (CMUTE; pin 62)						
$V_{i(rms)}$	mute activation level (RMS value) referenced to FMIN		2.2	4.2	7.1	mV
$t_{d(off)}$	switch-off delay time	signal to no signal	–	15	–	ms
$t_{d(on)}$	switch-on delay time	no signal to signal	–	400	–	ms
Level detector output ENVOUT; pin 60 (see Fig.10)						
V_o	output voltage level	f_i (FMIN) = 1.4 MHz; $V_{iHF(rms)}$ = 2 mV	0.6	0.9	1.2	V
		f_i (FMIN) = 1.4 MHz; $V_{iHF(rms)}$ = 20 mV	2.5	2.9	3.3	V
		f_i (FMIN) = 1.4 MHz; $V_{iHF(rms)}$ = 200 mV	4.1	4.5	4.8	V
R_o	output resistance		–	33	–	kΩ
Line outputs (LINEL and LINER; pins 27 and 28); audio inputs at AFNL and AFNR (pins 64 and 51): –11.5 dBV						
V_o	output voltage		–10	–8	–6	dBV
		input signal from modem to AFML and AFMR	–10	–8	–6	dBV
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–98	–90	dBV
THD	total harmonic distortion		–	0.05	0.2	%
L	linearity	V_{iAF} = –11.5 to –41.5 dBV	58	60	62	dB
α_{cb}	channel balance		–2	0	+2	dB
f_{res}	frequency response with respect to 1 kHz; output level	f_i = 300 Hz	–1	+0.4	+1.8	dB
		f_i = 10 kHz	–9.7	–7.7	–5.7	dB

Notes

1. HID pulse frequency set to 1 kHz. Unmodulated carrier at FMIN input with 135° phase step.
2. The audio distortion is measured with the HID pulse frequency set to 1 kHz (f_i = 500 Hz). FM signal: f_m = 10 kHz; Δf = 50 kHz. The distortion is measured with a 3 kHz 4th-order low-pass filter. The measured value at 1 kHz HID-pulse frequency is corrected with 26 dB in order to calculate the equivalent distortion at 50 Hz HID-pulse frequency.

10.4 Playback linear audio

Audio input signal –68 dBV from PBIN (pin 34).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
Linear audio playback input PBIN (pin 34)						
Z_i	input impedance		60	100	–	kΩ
V_o	output voltage at LINOUT		–14	–12	–10	dBV
Linear audio RESSW input (pin 35)						
Z	impedance between RESSW and PBIN	LP = 0	–	50	100	Ω
		LP = 1	100	150	–	kΩ
Line outputs LINEL and LINER (pins 21 and 22)						
V_o	output voltage	LP = 0	–8	–6	–4	dBV
		LP = 1	–6.7	–4.7	–2.7	dBV
f_{res}	frequency response with respect to 1 kHz; output level	f_i = 315 Hz; LP = 0	7.2	8.2	9.2	dB
		f_i = 10 kHz; LP = 0	–5.4	–4.4	–3.4	dB
		f_i = 315 Hz; LP = 1	5.9	6.9	7.9	dB
		f_i = 10 kHz; LP = 1	–3.7	–2.7	–1.7	dB
THD	total harmonic distortion		–	0.05	0.5	%
$V_{o(max)}$	maximum output voltage	THD = 1%	–	10	–	dBV
V_n	noise level	f_i = 300 Hz to 20 kHz	–	–58	–55	dBV
		referenced to PBIN	–	–120	–	dBV

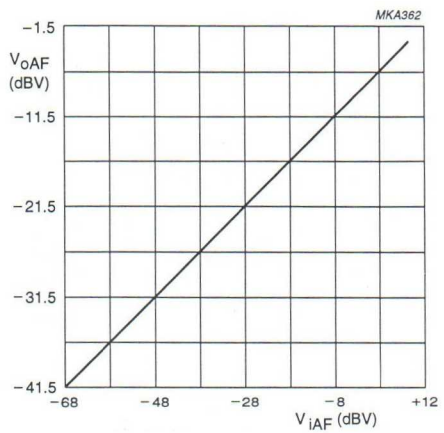


Fig.5 Compression curve of noise reduction at 1 kHz; record mode. The audio output voltage at AFNL and AFNR (pins 64 and 51) as a function of the audio input voltage at TUNL and TUNR (pins 2 and 3).

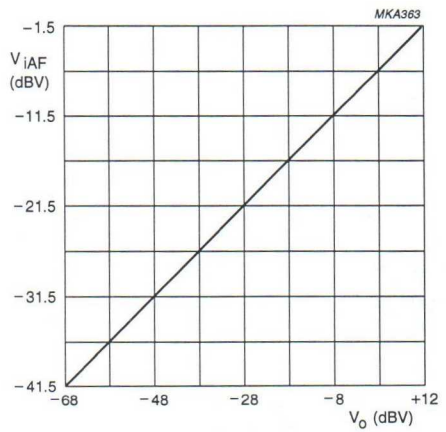


Fig.6 Expansion curve of noise reduction at 1 kHz; playback mode. The audio output voltage at LINEL and LINER (pins 21 and 22) as a function of the audio input voltage at AFNL and AFNR (pins 64 and 51).

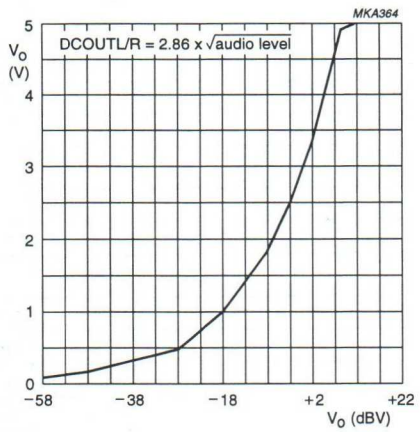


Fig.7 VU meter output voltage at DCOUTL and DCOUTR (pins 23 and 24) as a function of audio signal level.

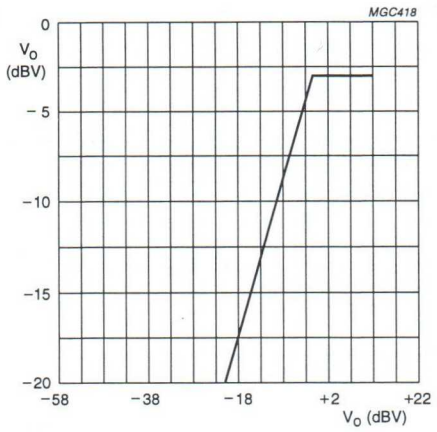


Fig.8 RF converter output voltage at RFCOUT (pin 18) as a function of line output signal level at LINEL and LINER (pins 21 and 22).

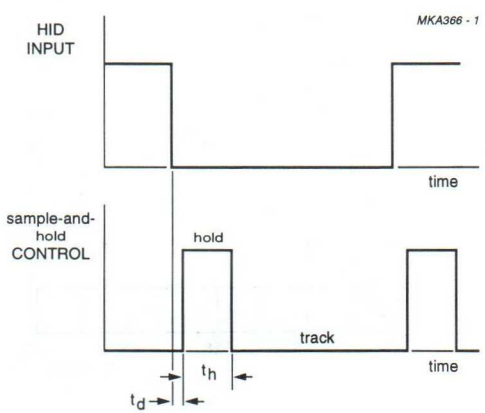


Fig.9 Sample-and-hold timing waveforms.

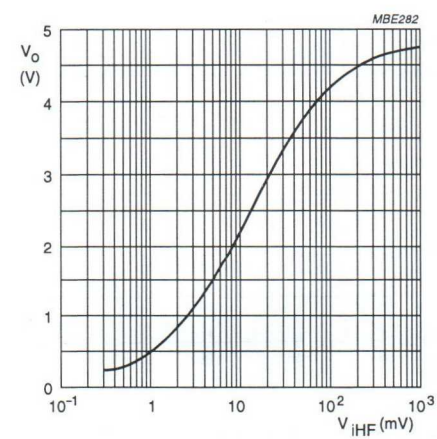
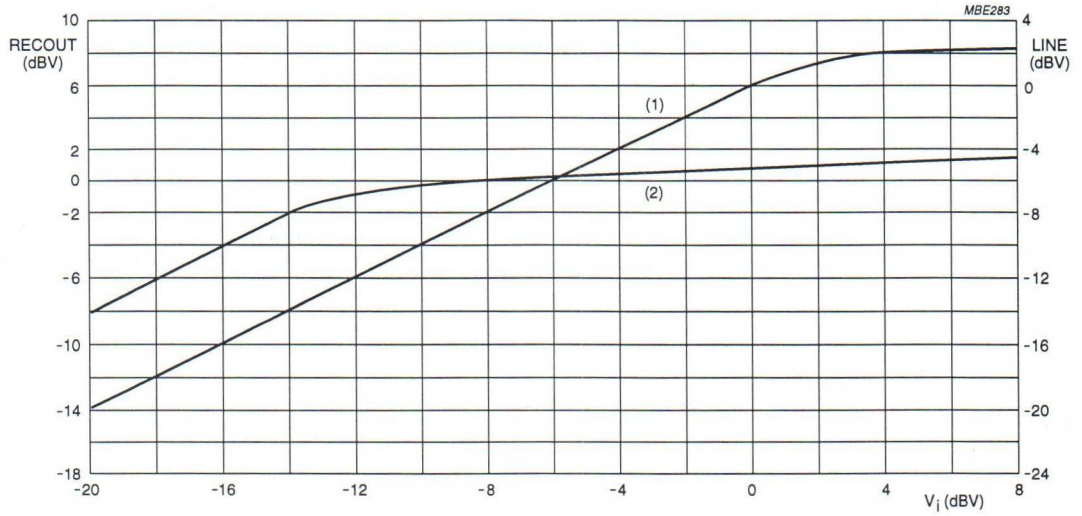


Fig.10 Level detector output voltage at ENVOUT (pin 60) as a function of the 1.4 MHz carrier input voltage level (RMS value) at FMIN (pin 57).



(1) Normsel = volume; AGCN = 1.
(2) Normsel ≠ volume; AGCN = 0.

Fig.11 RECOUT/LINE output as a function of audio signal level (hi-fi inputs).

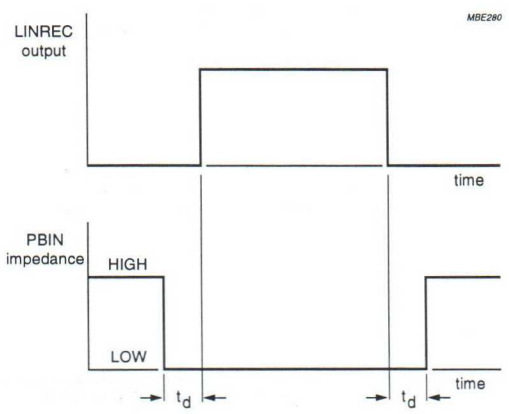
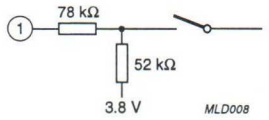
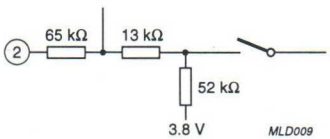
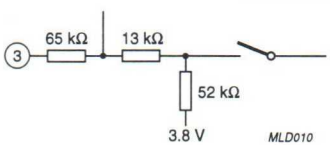
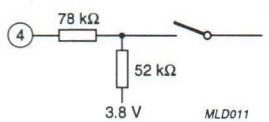
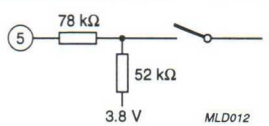
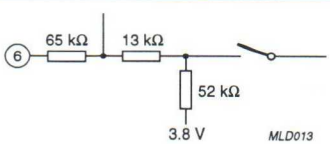
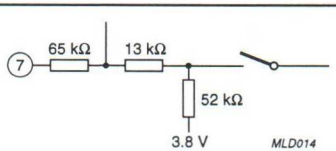
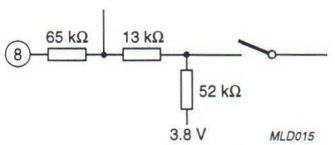
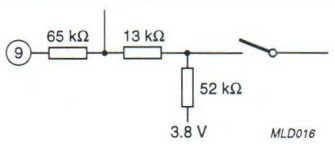
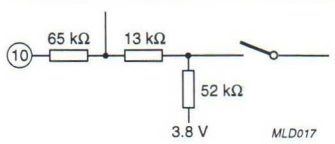
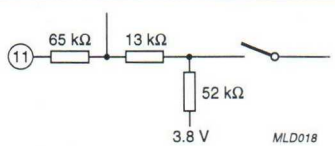
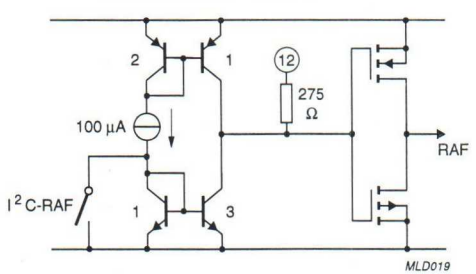
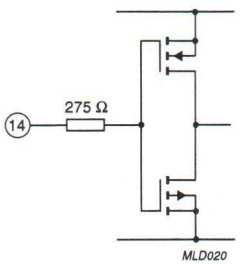
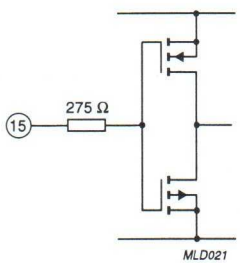
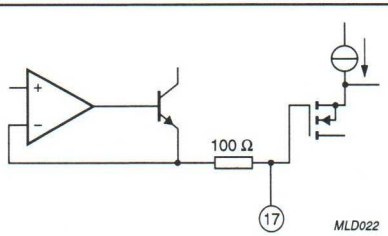
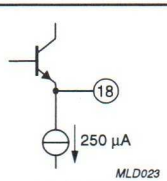


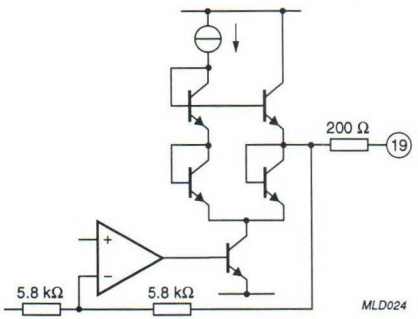
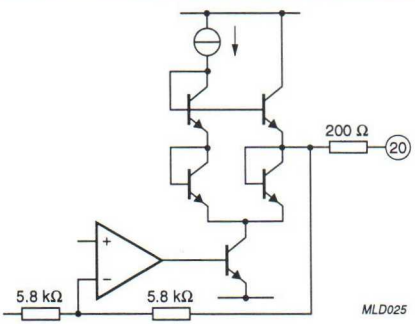
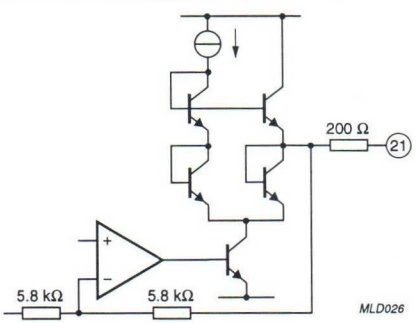
Fig.12 Timing of LINREC output versus PBIN impedance.

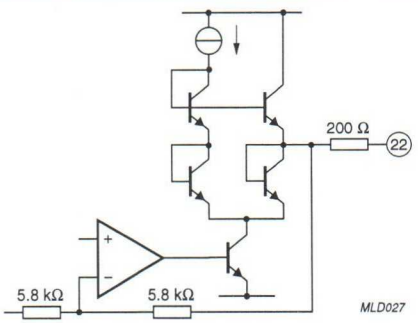
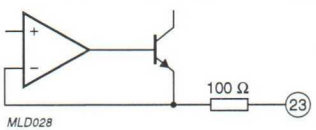
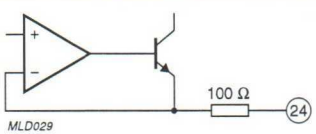
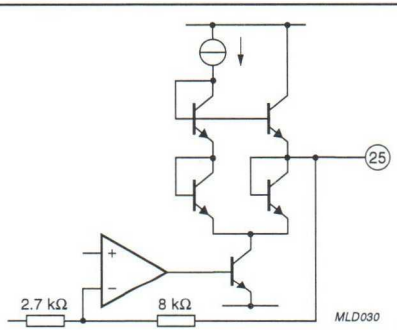
11 INTERNAL CIRCUITRY

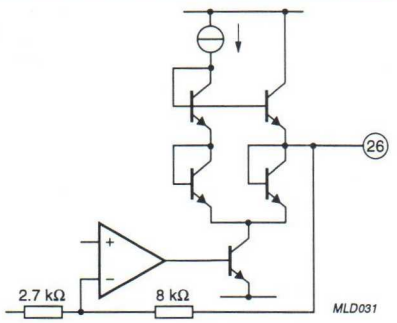
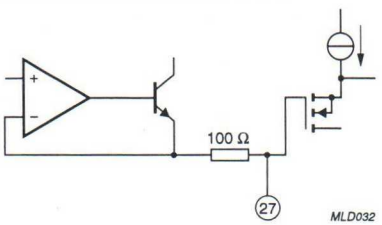
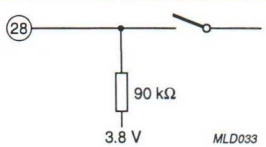
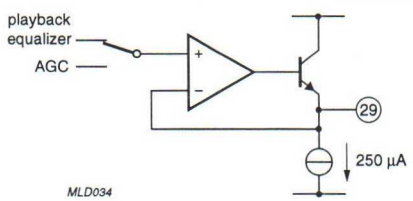
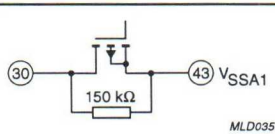
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
SAP	1		Second Audio Program (SAP) input.
TUNL	2		Left channel tuner input.
TUNR	3		Right channel tuner input.
CINL	4		Left channel cinch input.
CINR	5		Right channel cinch input.
EXT1L	6		Left channel external 1 input.
EXT1R	7		Right channel external 1 input.

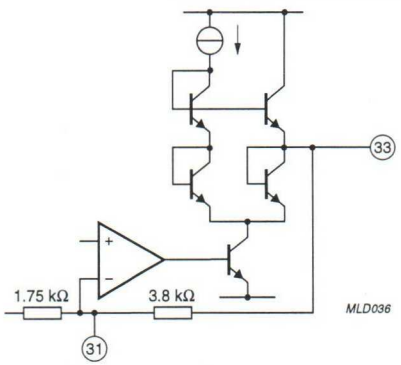
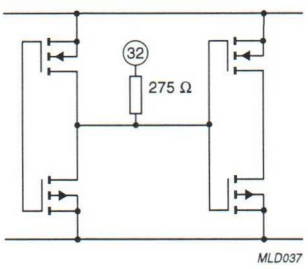
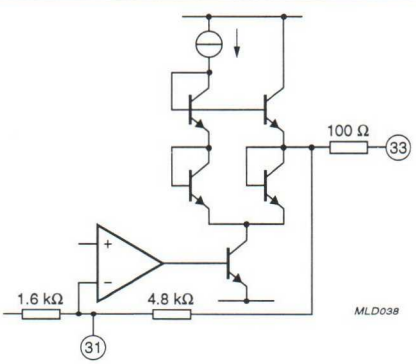
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
EXT2L	8		Left channel external 2 input.
EXT2R	9		Right channel external 2 input.
EXT3L	10		Left channel external 3 input.
EXT3R	11		Right channel external 3 input.
RAF	12		Record/playback switch drive output for head amplifier control or input for overruling the I²C-bit RAF.
V_{DDD}	13		Digital supply voltage for I²C-bus (+5 V).

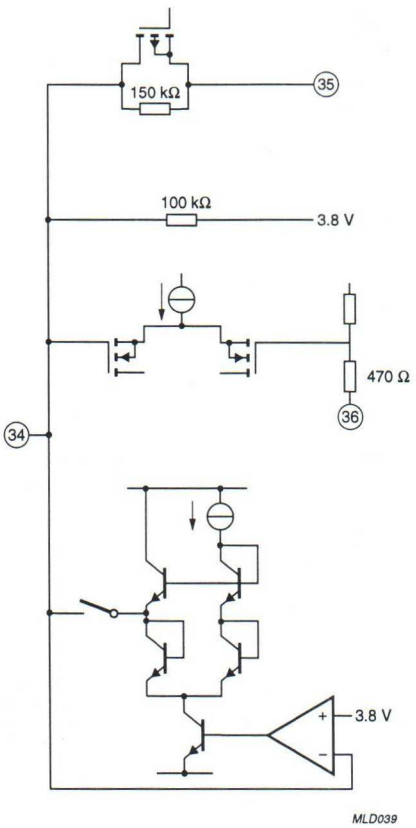
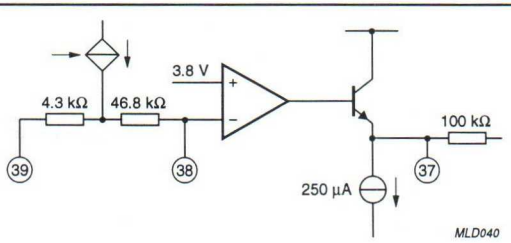
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
SDA	14		Data input/output for I²C-bus.
SCL	15		Clock input for I²C-bus.
V_{SSD}	16		Digital ground for I²C-bus.
RFCAGC	17		RF converter AGC-time constant.
RFCOUT	18		RF converter drive output.

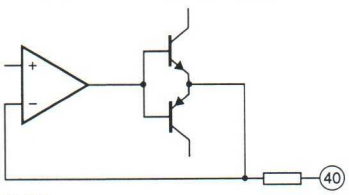
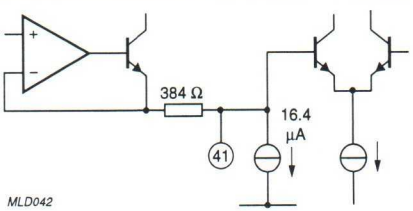
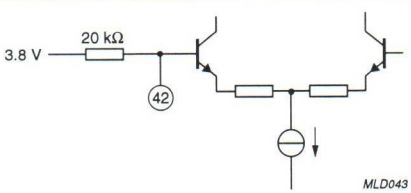
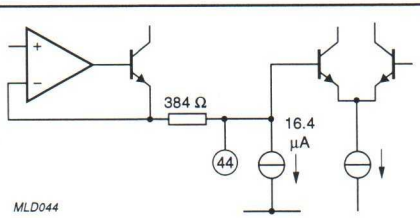
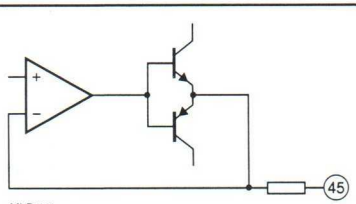
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
LINE2L	19		Line 2 left output (e.g. decoder output).
LINE2R	20		Line 2 right output (e.g. decoder output).
LINEL	21		Line output left.

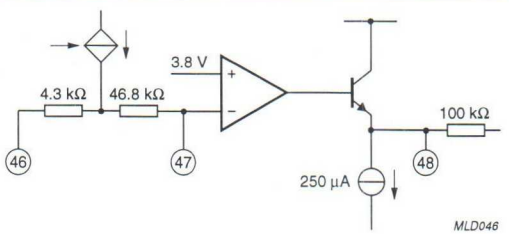
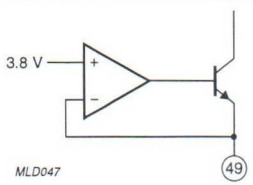
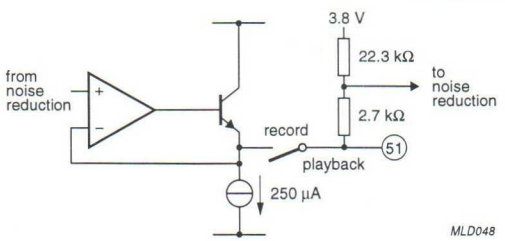
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
LINER	22		Line output right.
DCOUTL	23		VU meter drive output left.
DCOUTR	24		VU meter drive output right.
HPOUTL	25		Headphone drive output left.

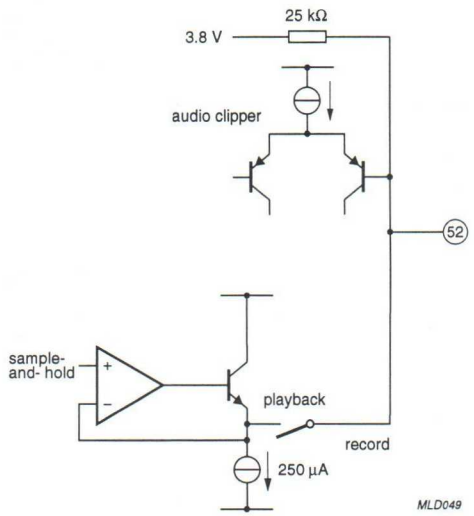
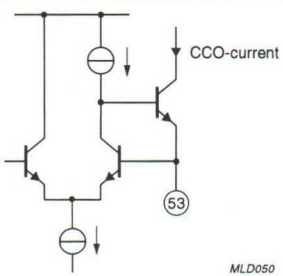
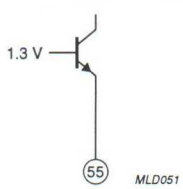
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
HPOUTR	26		Headphone drive output right.
LINAGC	27		Linear audio AGC-time constant.
LININ	28		Audio input for linear audio to REC equalizer and output select.
LINOUT	29		Audio output from AGC or PB equalizer.
EQSW	30		Long Play (LP) equalization switch; 15 Ω on resistance and 150 kΩ input impedance.

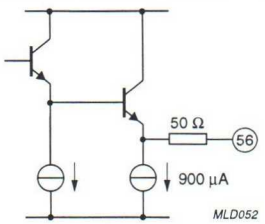
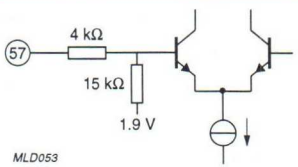
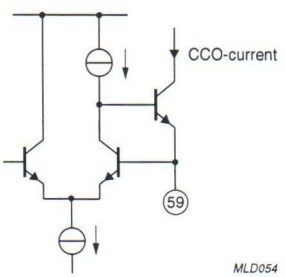
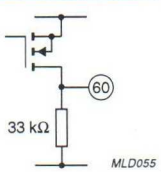
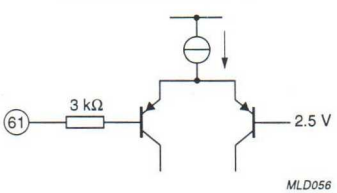
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
RECEQ	31		Linear audio recording amplifier negative feedback input for connecting a record equalization network.
LINREC	32		Digital output controlled by I²C-bit RN; can be used to drive an external (high voltage) head switch and possibly the bias oscillator.
RECOUT	33		Linear audio recording amplifier output.

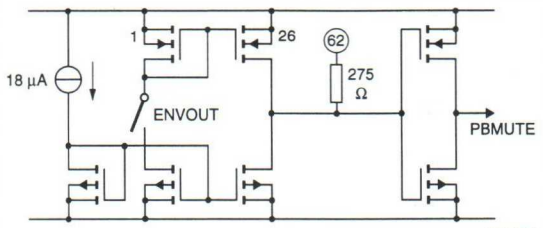
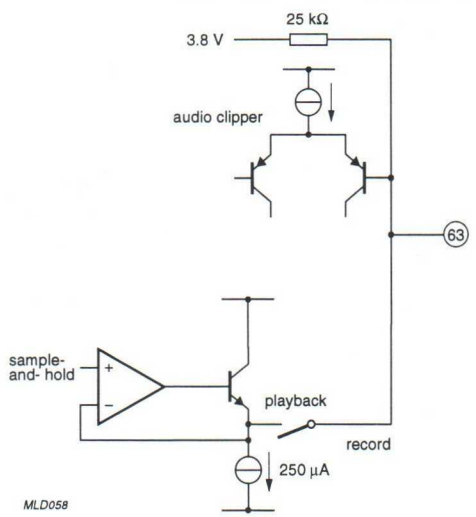
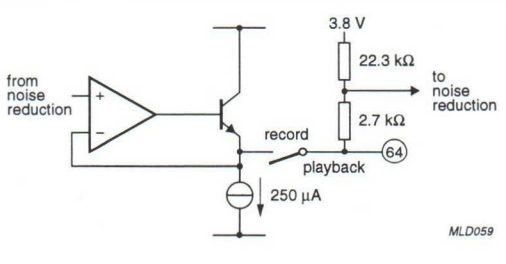
SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
PBIN	34		Linear audio playback amplifier input; during playback the impedance is 100 kΩ; during record the impedance is 7 Ω.
RESSW	35		Long Play equalization switch 50 Ω on and 150 kΩ off impedance to PBIN.
PBDC	36		Linear audio playback amplifier DC decoupling.
DCFBL	37		DC feedback left.
DCREFL	38		DC reference left.
EMPHL	39		Total emphasis left (240 to 20 µs).

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
RECTL	40		Rectifier DC decoupling left.
DETL	41		Attack/recovery timing left.
V_{ref}	42		Noise filtering of 3.8 V reference voltage (external capacitor required for filtering).
V_{SSA1}	43		Analog ground 1 for LF circuits.
DETR	44		Attack/recovery timing right.
RECTR	45		Rectifier DC decoupling right.

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
EMPHR	46		Total emphasis right (240 to 20 µs).
DCREFR	47		DC reference right.
DCFBR	48		DC feedback right.
RFIX	49		Fixed bias current generation circuit by using an external 180 kΩ resistor to ground.
V_{DDA1}	50		Analog supply voltage 1 for LF circuits (+12 V).
AFNR	51		Audio output from noise reduction of right channel (record and loop-through) or audio input for noise reduction of right channel (playback).

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
AFMR	52		Audio input for audio clipper of right channel (record and loop-through) or audio output from sample-and-hold (playback).
RCCOR	53		Voltage-to-current transfer for right channel oscillator by means of an external resistor to ground.
V_{SSA2}	54		Analog ground 2 for HF circuits.
RBPF	55		Bias current generation for the internal band-pass filters by means of an external resistor to ground.

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
FMOUT	56		FM output.
FMIN	57		FM input.
V_{DDA2}	58		Analog supply voltage 2 for HF circuits (+5 V).
RCCOL	59		Voltage-to-current transfer for left channel oscillator by means of an external resistor to ground.
ENVOUT	60		Level detector output (external capacitor required for filtering).
HID	61		Head Identification Pulse (HID) input for sample-and-hold circuits.

SYMBOL	PIN	EQUIVALENT CIRCUIT	DESCRIPTION
CMUTE	62		Mute timing (external capacitor required for playback mute).
AFML	63		Audio input for audio clipper of left channel (record and loop-through) or audio output from sample-and-hold circuit of left channel (playback).
AFNL	64		Audio output from noise reduction of left channel (record and loop-through) or audio input for noise reduction of left channel (playback).

12 TEST AND APPLICATION INFORMATION

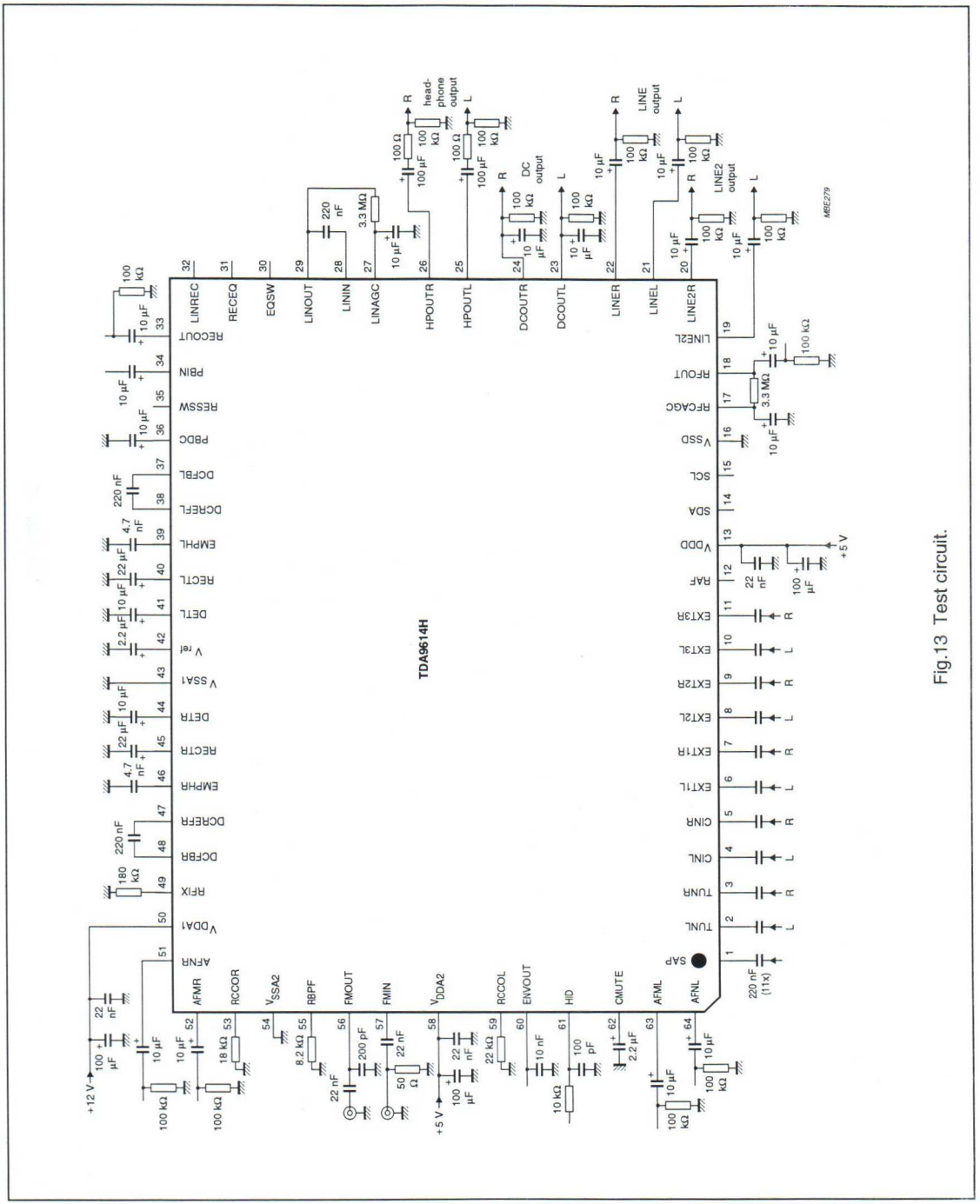


Fig.13 Test circuit.

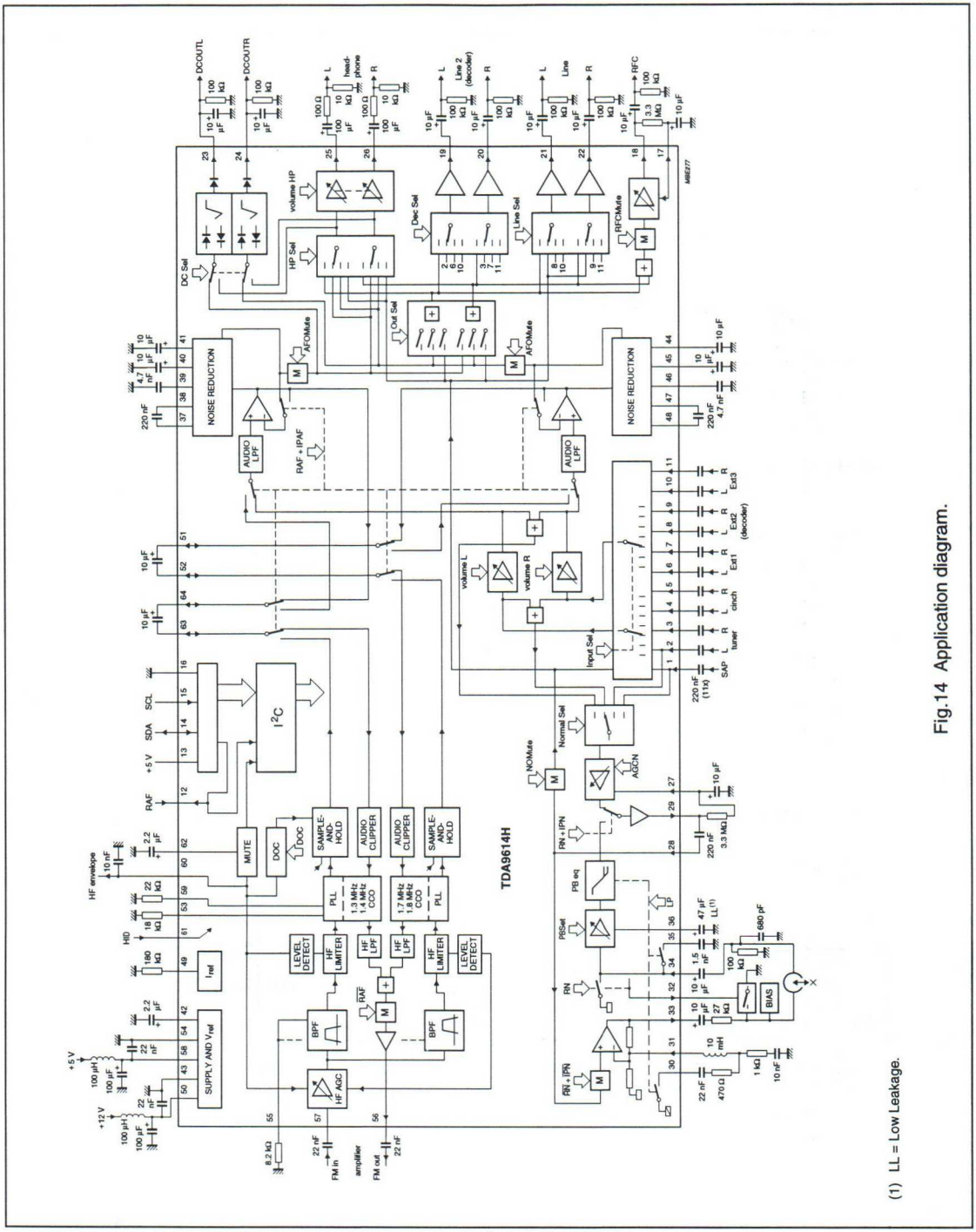


Fig.14 Application diagram.

(1) LL = Low Leakage.

12.1 RAF I/O (pin 12)

The status of the I²C RAF bit is output (RAF = HIGH; record). This output can be used to switch the audio FM head amplifier to playback and record. If accurate fast switching of the TDA9614H is needed, this pin can also be used as input. Thereby overruling the I²C RAF bit. To make this possible the RAF output is current limited.

When using the RAF pin as output, no more than 35 μA (LOW) and 185 μA (HIGH) current may be drawn from this pin to assure that the mode of the TDA9614H is not changed.

When using the RAF pin as input, the voltage source used must be capable of delivering at least 345 μA (forced HIGH; >3.5 V) or sinking at least 65 μA (forced LOW; <1.5 V).

12.2 RCCOL, RCCOR, RBPF and RFIX (pins 59, 53, 55 and 49)

The external resistors to ground at pins RCCOL, RCCOR, RBPF and RFIX must have a tolerance of 5%. This is necessary to guarantee correct functioning of the IC. The temperature coefficient of the external resistors at RCCOL, RCCOR and RBPF have a direct influence on the related frequencies of the on-chip oscillators and bandpass filters.

Y/C one-chip processor (VHS standard) — TDA9715H/A

FEATURES

- Luminance noise reduction (YNR)
- Chrominance noise reduction (CNR)
- Saturation dependent writing current control (CACC)
- Integrated filter
- Simple SVHS playback
- Skew output for longplay TRICK mode.

GENERAL DESCRIPTION

The TDA9715H/A is an integrated circuit for chrominance and luminance processing (record and playback) in VHS tape recorders for the TV standard PAL, NTSC, SECAM/ME (4.43 MHz chrominance systems).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		4.5	5.5	V
I_{CC}	supply current	V_{CC} = 5 V	–	200	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–25	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9715H/A	80	QFP80REC	plastic	SOT310

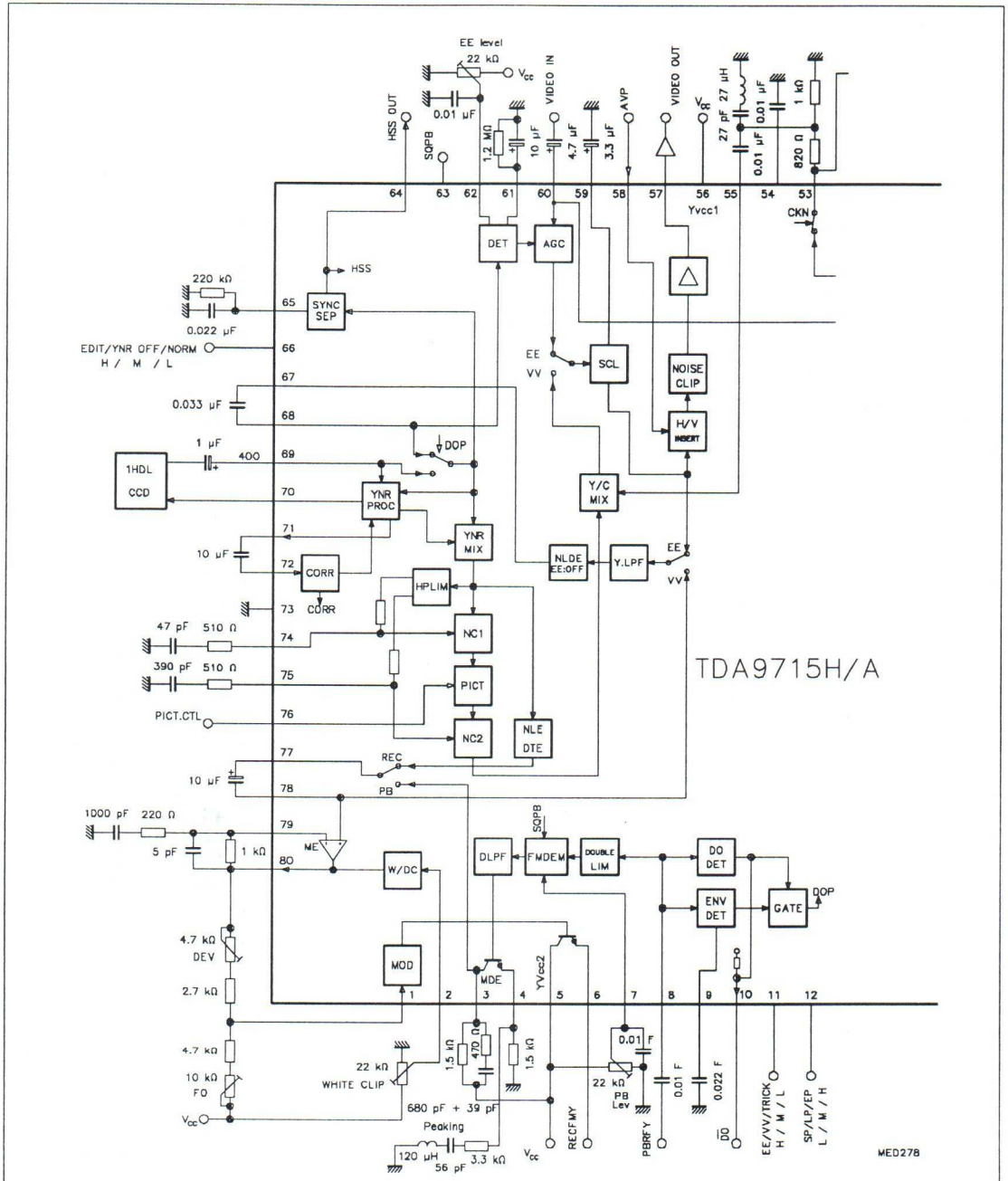


Fig.1 Block diagram (continued in Fig.2).

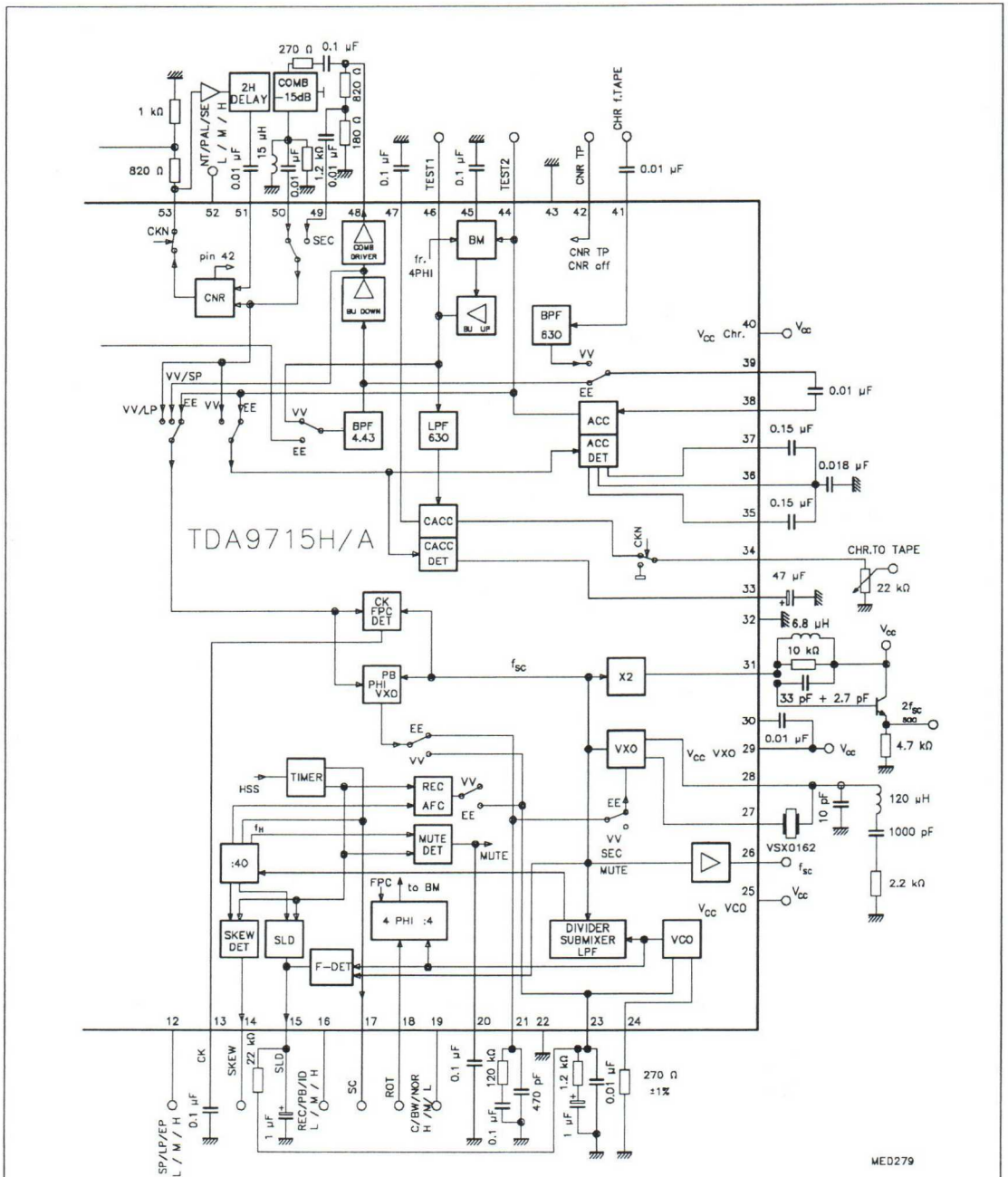


Fig.2 Block diagram (continued from Fig.1).

FUNCTIONAL DESCRIPTION

REC/EE - MODE

Luminance

The CVBS signal appears at the output pin 57 and at the internal Y low-pass filter (YLPF) via pin 60 and AGC stage. Exempt from chrominance the luminance signal is fed first to the sync separator stage to obtain the separated sync pulse at pin 64 and secondly via non linear emphasis (NLE), main emphasis, white/dark clip and FM modulator to the FM output pin 6.

Chrominance

Exempt from the luminance signal in the internal 4.43 MHz band-pass filter (BPF 4.43 MHz) and controlled by the ACC stage the chrominance signal is mixed in the band mixer with a 4-phase shifted 5.06 MHz signal, produced by the internal adjustment free oscillator. The formed N x f_H signal is fed via an internal low-pass filter and CACC to the output at pin 34.

PB/VV - MODE

Luminance

The FM signal is fed to the FM demodulator stage and the internal sub low-pass filter (DLPF) via input pin 8 and the double limiter. After passing main de-emphasis, non linear de-emphasis (NLDE) and the luminance noise reduction (YNR) the signal is fed first to the sync separator stage and then (via picture control stage) mixed with the chrominance signal. This CVBS signal is output at pin 57.

Chrominance

The internal N x f_H band-pass filter (BPF 627 kHz) and the ACC stage the signal is mixed in the band mixer with a 4-phase shifted 5.06 MHz signal, produced by the internal adjustment free oscillator via input pin 41. The formed f_{SC}-chrominance signal is fed via internal BPF 4.43 MHz, external comb filter and internal chrominance noise reduction (CNR) to the internal Y/C mixer.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		–	–	5.5	V
V_{65}	voltage V_{65} (with respect to GND)		–	–	4.5	V
V_I	input voltage V_{68}, V_{69}, V_{78} (with respect to GND)		–	–	4.1	V
V_I	input voltage at all other pins		0	–	V_{CC}	V
I_O	output currents $-I_4$, $-I_6$, $+I_{24}$, $-I_{39}$, $-I_{57}$, $-I_{67}$, $-I_{71}$, $-I_{77}$, $-I_{80}$		–	–	10	mA
P_{tot}	total power dissipation	see Fig.3	–	1887	–	mW
T_{stg}	storage temperature		–25	–	+150	°C
T_{amb}	operating ambient temperature	see Fig.3	–20	–	+70	°C
V_{ESD}	electrostatic handling for all pins	note 1	–	–	±300	V

Note to the limiting values

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

QUALITY SPECIFICATION

URV-4-2-59/601

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = +25 °C and typical application (see Fig.1).
Luminance part: All amplitudes are VBS peak-to-peak values, unless otherwise specified.
Chrominance part: All amplitudes for PAL and NTSC are red values with 75% saturation and chrominance-to-burst ratio of 2.2, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	4.95	5.5	V
I_P	current consumption ($I_5 + I_{25} + I_{29} + I_{40} + I_{56}$) at PB/VV		140	165	200	mA
I_R	current consumption ($I_5 + I_{25} + I_{29} + I_{40} + I_{56}$) at REC/EE		130	150	180	mA
Modulator input (pin 1)						
φ	sensitivity		10	12.5	15	kHz/µA
White clip control (pin 2)		open base				
CTL_φ	control sensitivity		60	80	100	%/V
Main de-emphasis output (pin3)		open collector				
V_3	DC voltage	FM input = 3.8 MHz; V_7 = 1.7 V	2.5	3.0	3.5	V
V_{s3}	video signal (peak-to-peak value)	V_7 = 1.7 V	230	300	370	mV
DEM_φ	demodulator sensitivity	normal VHS mode; V_7 = 1.7 V	0.23	0.3	0.37	V/MHz
		SQPB mode	0.14	0.19	0.24	V/MHz
LIN_3	demodulator linearity $\frac{V_0\ (5\ MHz) - V_0\ (4\ MHz)}{V_0\ (4\ MHz) - V_0\ (3\ MHz)}$	VHS mode	0.95	0.98	1.01	
	demodulator linearity $\frac{V_0\ (9\ MHz) - V_0\ (7\ MHz)}{V_0\ (7\ MHz) - V_0\ (5\ MHz)}$	SVHS mode	0.9	0.98	1.05	
α	suppression of demodulator carrier $\frac{V\ (4\ MHz)}{V\ (2\ MHz)}$	measured with FM input = 2 MHz	40	–	–	dB
f_b	boundary frequency for demodulating	V_7 = 1.2 V	10	–	–	MHz
Main de-emphasis and peaking (pin 4)		open emitter				
V_4	DC voltage	FM input = 3.8 MHz; V_7 = 1.7 V	1.7	2.0	2.3	V
V_{s4}	video signal (reverse) (peak-to-peak value)	V_7 = 1.7 V	230	300	370	mV
Supply voltage (pin 5)						
I_{SP}	DC current PB		13	–	19	mA
I_{5R}	DC current REC		8	–	14	mA
FM output (pin 6)						
V_{o6}	output mean value of DC	R_L = 1 kΩ	3.0	3.3	3.6	V
V_s	output signal (peak-to-peak value)	R_L = 1 kΩ	0.7	0.9	1.1	V
f_o	output frequency	I_1 = 304 µA	3.4	3.8	4.2	MHz
α	second distortion	f = 4 MHz	–	–50	–42	dB
Δf	carrier down	NTSC mode	320	400	480	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN_6	modulator linearity $\frac{I_1\ (6\ MHz) - I_1\ (4\ MHz)}{I_1\ (4\ MHz) - I_1\ (2\ MHz)}$		0.98	1.00	1.02	
f_{mod}	modulator frequency range		1.5	–	10	MHz
Demodulator gain control (pin 7)		open base				
V_7	active range of gain control		1.2	1.7	2.2	V
CTL_φ	control sensitivity	SYNC-white = 100%	65	80	95	%/V
PB FM input (pin 8)						
V_8	DC voltage		2.7	3.0	3.3	V
V_{s8}	input signal (peak-to-peak value)		–	350	–	mV
V_b	boundary input range (peak-to-peak value)		10	–	1000	mV
Envelope detector (pin 9)						
V_{D9}	DC range of normal mode		3.0	–	5.0	V
V_{D0}	DC range of DOC off mode		0	–	2.0	V
V_9	DC level at no signal		1.8	2.3	2.8	V
G_{ENV}	envelope detector switch on level (DO active)	0 dB = V_{s8} = 350 $mV_{(p-p)}$; f = 3.8 MHz	–13	–10	–7	dB
t_{ENV}	envelope detector operating time	C = 0.022 µF	480	600	720	µs
Drop-out pulse output (pin 10)						
V_{10L}	DC voltage low level	V_{s8} = 0 V	0	–	500	mV
V_{10H}	DC voltage high level	V_{s8} = 350 $mV_{(p-p)}$; R_L = 15 kΩ to GND	2.0	2.5	3.0	V
G_{DOC}	DOC on level	0 dB = V_8 = 350 $mV_{(p-p)}$; f = 3.8 MHz	–18	–15	–12	dB
G_{DOF}	DOC off level (hysteresis)		1	3	5	dB
V_{th}	threshold voltage for forced DO on		0.2	0.7	1.2	V
Switch (EE/VV/TRICK) (pin 11)						
V_{EE}	voltage range for active EE		3.5	–	5	V
V_{VV}	voltage range for active VV		1.75	–	3	V
V_{TR}	voltage range for active TRICK		0	–	1.25	V
V_{11}	DC level	pin open-circuit	4.8	–	5	V
Switch (SP/LP/EP) (pin12)		open pnp base				
V_{SP}	voltage range for active SP		0	–	1.25	V
V_{LP}	voltage range for active LP		1.75	–	3	V
V_{EP}	voltage range for active EP		3.5	–	5	V
Colour killer (pin 13)						
V_{13}	DC at no chrominance input		1.6	1.8	2.0	V
V_{CON}	threshold voltage colour on		2.0	2.2	2.4	V
G_{CKON}	colour killer active	relative to nominal input signal V_{s38} = 110 $mV_{(p-p)}$	–27	–30	–33	dB
G_{HY}	colour killer hysteresis		1	2	3	dB
Skew output (pin 14)		npn collector with 25 kΩ to V_{CC}				
V_{SL}	output voltage skew LOW		–	–	0.8	V
V_{SH}	output voltage skew HIGH		4	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency correction output (pin 15)						
I_{SLD}	output current SLD	VV mode; sidelock detector	±12	±17	±22	µA
t_{SLD}	pulse duration	VV mode; sidelock detector; f_H = 15.625 kHz	–	64	–	µs
f_{SLH}	start of detection at positive frequency deviation (referred to f_{SC} + N x f_H at pin 46; $-I_{15}$)	VV mode; sidelock detector; PAL	1.0	2.0	3.0	kHz
		VV mode; sidelock detector; NTSC	2.0	4.0	5.0	kHz
f_{SLL}	start of detection at negative frequency deviation (referred to f_{SC} + N x f_H at pin 46; $+I_{15}$)	VV mode; sidelock detector; PAL	–3.0	–2.0	–1.0	kHz
		VV mode; sidelock detector; NTSC	–5.0	–4.0	–2.0	kHz
V_{SLO}	operating range	EE and VV mode; frequency detector	0.8	–	4.2	V
I_{FD}	output current of frequency detector		±12	±17	±22	µA
t_{FD}	pulse duration		70	75	80	µs
f_{FDH}	start of detection at positive frequency deviation (referred to f_{SC} + N x f_H at pin 46; $-I_{15}$)	EE mode	40	70	100	kHz
f_{FDL}	start of detection at negative frequency deviation (referred to f_{SC} + N x f_H at pin 46; $+I_{15}$)		–100	–70	–40	kHz
Switch (REC/PB/ID) (pin 16)						
V_{REC}	voltage range for active REC mode		0	–	1.25	V
V_{PB}	voltage range for active PB mode and FPC on		1.75	2.5	3	V
V_{ID}	voltage range for active PB mode and FPC off (ID mode)		3.5	–	5	V
V_{16}	DC level	pin open-circuit	4.8	–	5	V
Sandcastle, BGP output (LOW active) (pin 17)		SC with external 20 kΩ resistance to GND				
t_{BGP}	duration of BGP		4.2	4.45	4.7	µs
t_{BGS}	start of BGP beyond sync start at pin 64		3.25	3.5	3.75	µs
V_{BGI}	DC voltage low (BGP)	I_{17} = 1 mA	–	–	0.5	V
V_{med}	DC voltage medium (horizontal blanking)	I_{17} = –0.2 mA	1.8	2.2	2.6	V
V_{HI}	DC voltage HIGH (inactive)	I_{17} = –0.4 mA	4.0	4.4	–	V
V_{BGPO}	voltage for BGP not active	BGP with external 20 kΩ resistance to V_{CC}	4.6	–	–	V
V_{BGPA}	voltage for BGP active		–	–	0.6	V
Rotary pulse (pin 18)		open pnp base				
V_{C2}	voltage for –90° phase rotation (Channel 2)		0	–	2.25	V
V_{C1}	voltage for non rotation (PAL) or +90° rotation (NTSC) (Channel 1)		2.75	–	5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switch (C/BW/NORM) (pin 19)		open pnp base				
V_{fCON}	voltage for forced colour on (C)		3.5	–	5	V
V_{fCOF}	voltage for forced colour off (BW)		1.75	–	3	V
V_{NORM}	voltage for NORM mode		0	–	1.25	V
Mute detector (pin 20)						
V_C	voltage at coincidence		3.5	–	–	V
V_{NC}	voltage at no coincidence (mute)		–	–	1.5	V
V_{MUTE}	threshold voltage to switch VXO to VV mode		2.2	–	2.8	V
Loop filter (EE) VXO (pin 21)						
V_{21}	DC level		1	2.4	3.6	V
β	VXO sensitivity		1.0	1.6	2.2	Hz/mV
f_{PRU}	pull in range upper		0.8	1.3	1.8	kHz
f_{PRL}	pull in range lower		–1.8	–1.3	–0.8	kHz
Loop filter VCO (pin 23)						
V_{23}	DC level	EE mode	1.3	2.1	2.9	V
β	VCO sensitivity (f_H related)		17	19	21	kHz/V
	VCO sensitivity (f_{SC} related)	VV mode	680	760	840	kHz/V
VCO bias current (pin 24)						
V_{24}	DC level		0.5	V_{BE}	0.8	V
R_{24}	external resistance to ground		267	270	273	Ω
Supply voltage VCO (pin 25)						
I_{25}	DC current		4.5	–	6.5	mA
f_{SC} output (pin 26)						
V_{26}	DC level		1.8	2.3	2.8	V
V_{s26}	output signal (peak-to-peak value)		500	600	700	mV
α_2	second distortion		–	–	–25	dB
α_3	third distortion		–	–	–20	dB
Δf_i	deviation of oscillator frequency (due to internal spread)	VV	–	–	±50	Hz
Δf_B	deviation of oscillator frequency (video signal without burst applied)	EE	–	–	±1.4	kHz
Δf_C	deviation of oscillator frequency (no video signal applied)	EE/MUTE/blueback option	–	–	±100	Hz
Δf_{VT}	deviation of frequency due to supply voltage from 4.5 V to 5.5 V and T_{amb} from –20 °C to +70 °C	VV	–	–	±100	Hz
VXO (crystal output) (pin 27)						
V_{27}	DC level		3.1	3.5	3.9	V
VXO (crystal input) (pin 28)						
V_{28}	DC level		2.6	3.0	3.4	V
Supply voltage VXO (pin 29)						
I_{29}	DC current		10	–	17	mA
Filter reference terminal (chrominance filter) (pin 30)						
V_{30}	active range of DC when controlling		2.5	3.0	3.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
2 x fsc output (pin 31)		open npn collector				
V_{31}	DC level		4.5	5.0	–	V
V_{s31}	output signal (peak-to-peak value)	R = 1 kΩ to V_{CC}; EF	40	55	70	mV
α	second distortion	tuned LC circuit (Q > 20); EF	–	–	–30	dB
Loop filter CACC (pin 33)		loading via EF; see Fig.6				
V_{C-B}	DC level	chrominance/burst = 2.2	2.0	2.5	3.0	V
V_{CTR}	control range		1.0	–	3.0	V
CACC output (pin 34)		see Figs 6 and 7				
V_{COF}	DC level at colour on		2.1	2.4	2.7	V
V_{CON}	DC level at active colour killer	EE or VV mode	–	0.1	0.3	V
V_{s34}	chrominance output signal (N x f_H) (peak-to-peak value)		467	660	932	mV
ΔG_{34}	maximum CACC gain $\Delta V_{34}/V_{46}$ (N x f_H)		–	2.7	–	dB
$\alpha_{2,3}$	second, third distortion	V_{s46} = 0 dB	–	–	–40	dB
		V_{s46} = +6 dB	–	–	–35	dB
α_{ck}	colour killer suppression		40	–	–	dB
$G_{1.5}$	1.5 dB up gain	see Fig.8	1	1.5	2	dB
α_{cr}	crosstalk CVBS signal		–	–	–40	dB
ACC loop filter switch (Channel 2) (pin 35)		open npn collector; non-conducting during VV TRICK				
R_{35}	in VV and EE switched to ground while ROT (pin 18) HIGH; output resistance		–	–	200	Ω
$t_{att/rec}$	attack and recover time	input signal 0 dB to 6 dB	50	–	100	lines
		–6 dB to 0 dB	50	–	100	lines
		–12 dB to –6 dB	50	–	100	lines
ACC loop filter (pin 36)						
t	attack time (TRICK mode)	0 dB to 6 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
	attack time (TRICK mode)	–6 dB to 0 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
	attack time (TRICK mode)	–12 dB to –6 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
ACC loop filter switch (Channel 1) (pin 37)		open npn collector; non-conducting during VV TRICK				
R_{37}	in VV and EE switched to ground while ROT (pin 18) LOW; output resistance		–	–	200	Ω
$t_{att/rec}$	attack and recover time	input signal 0 dB to 6 dB	50	–	100	lines
		–6 dB to 0 dB	50	–	100	lines
		–12 dB to –6 dB	50	–	100	lines
ACC input (pin 38)		see Fig.9				
V_{38}	DC level		1.1	1.6	2.1	V
V_{s38}	input signal (peak-to-peak value)		11	110	310	mV
f_B	bandwidth (–3 dB) upper cut-off frequency		10	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BPF switch output (pin 39)		EE mode: from BPF 4.43; VV mode: from BPF 630				
V_{39}	DC level	EE	1.9	2.4	2.9	V
		VV	2.5	3.0	3.5	V
G	gain $\frac{V_{39}}{V_{41}}$	VV; f = 630 kHz	−1	0	1	dB
V_{s39V}	output signal (peak-to-peak value)	VV	–	110	310	mV
V_{s40E}	output signal (peak-to-peak value)	EE	121	135	149	mV
α_{cr}	switch crosstalk EE → VV or VV → EE		–	–	−45	dB
$\alpha_{2,3}$	second, third distortion	0 dB input signal	–	–	−40	dB
		6 dB input signal	–	–	−35	dB
Supply voltage (pin 40)						
I_{40E}	DC current	EE mode	60	–	85	mA
I_{40V}	DC current	VV mode	60	–	85	mA
PB chrominance from tape (pin 41)						
V_{41}	DC level		1.7	2.2	2.7	V
V_{s41}	input signal (chrominance) (peak-to-peak value)		–	110	310	mV
CNR TEST PIN (pin 42)		npn EF with internal current source of 50 μA				
V_{42}	DC level		2.4	3.0	3.6	V
α	second distortion	external resistor 10 kΩ to GND	–	–	−35	dB
V_{OUs}	limited output signal (peak-to-peak value)	CNR on	225	275	350	mV
V_{CNRO}	CNR off mode		4.8	–	V_{CC}	V
TEST PIN 2 (pin 44)						
V_{44}	DC level		1.75	2.25	2.75	V
V_{OUs}	controlled output signal (peak-to-peak value)		340	440	540	mV
G_{o44}	deviation of output signal	V_{IN} −10 dB/+3 dB	−0.3	–	+0.3	dB
		V_{IN} −15 dB/+6 dB	−0.5	–	+0.5	dB
f_B	bandwidth (−3 dB)		10	–	–	MHz
$\alpha_{2,3}$	distortion of second, third harmonic with +6 dB signal amplitude at pin 38 or pin 44		–	–	−35	dB
	distortion of second, third harmonic with nominal signal at pin 38 and pin 44		–	–	−40	dB
Mixer balance (pin 45)						
V_{45}	DC voltage		1.75	2.25	2.75	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TEST PIN 1 (pin 46)						
V_{SL46}	output signal N x f_H (peak-to-peak value)	EE mode	80	110	140	mV
V_{SH46}	output signal 2 x f_{SC} + N x f_H (peak-to-peak value)		80	110	140	mV
α_{EESP}	suppression of f_{SC} + N x f_H		38	–	–	dB
	suppression of f_{SC}		38	–	–	dB
$BURST_{up}$	burst up at NTSC SP or NTSC EP mode		5.0	6.0	7.0	dB
V_{fsc}	output signal f_{SC} (peak-to-peak value)	VV mode	80	110	140	mV
V_{fsc+}	output signal f_{SC} + 2N x f_H (peak-to-peak value)		80	110	140	mV
α_{VVSP}	suppression of f_{SC} + N x f_H		38	–	–	dB
	suppression of N x f_H		38	–	–	dB
V_{46}	DC level	EE and VV mode	1.8	2.2	2.6	V
$\alpha_{2,3}$	second, third distortion	EE and VV mode; input 0 dB	–	–	–40	dB
		EE and VV mode; input 6 dB	–	–	–35	dB
f_B	bandwidth (–3 dB)	EE and VV mode	10	–	–	MHz
AC coupling (pin 47)						
V_{47}	DC voltage		1.85	2.2	2.55	V
Output COMB driver (VV) (pin 48)						
V_{48}	DC level		2.0	2.5	3.0	V
V_{s48N}	output signal (peak-to-peak value)	NTSC	290	350	420	mV
V_{s48P}	output signal (peak-to-peak value)	PAL, SECAM	520	620	740	mV
f_B	bandwidth (–3 dB)		10	–	–	MHz
$\alpha_{2,3}$	distortion of second, third harmonic with input signal at pin 46 = 110 $mV_{(p-p)}$		–	–	–40	dB
	distortion of second, third harmonic with input signal at pin 46 = 220 $mV_{(p-p)}$		–	–	–35	dB
$BURST_{down}$	burst down	NTSC SP mode	–6.0	–5.0	–4.0	dB
		NTSC EP mode	–5.0	–4.0	–3.0	dB
Through side chrominance input (pin 49)						
V_{49}	DC level		2.2	2.7	3.2	V
V_{s49}	chrominance input signal (peak-to-peak value)		–	110	–	mV
COMB side chrominance input (pin 50)						
V_{50}	DC level		2.2	2.7	3.2	V
V_{s50}	input signal (peak-to-peak value)		–	110	–	mV
CNR limiter input (pin 51)						
V_{51}	DC level		0.6	0.8	1.0	V
V_{s51}	input signal (peak-to-peak value)		–	39	100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switch (PAL/SECAM/NTSC) (pin 52)						
V_{PAL}	voltage range for active PAL mode		1.75	–	3	V
V_{SEC}	voltage range for active SECAM mode		3.5	–	5	V
V_{NT}	voltage range for active NTSC mode		0	–	1.25	V
V_{52}	DC level	pin open-circuit	4.8	–	5.0	V
Chrominance output (pin 53)						
V_{53}	DC level		2.5	3.0	3.5	V
V_{sout}	output signal	input signal pin 49 or pin 50 = 110 $mV_{(p-p)}$	700	880	1060	mV
α_{ck}	colour killer suppression		40	–	–	dB
α_{SEC}	crosstalk from inactive combside	V_{s50} = 110 $mV_{(p-p)}$	–	–40	–30	dB
K	CNR K factor	input signal pin 50 = 4 $mV_{(p-p)}$ CNR on/off	0.55	0.65	0.75	–
G_{51-53}	amplification –20lgK	input signal pin 51 = 1.4 $mV_{(p-p)}$	24	27	30	dB
α_{CNR}	CNR second distortion	input signal pin 51 = 39 $mV_{(p-p)}$	–	–35	–25	dB
Filter reference terminal (luminance filter) (pin 54)		open base and collector				
V_{54}	active range of DC when controlling		1.8	2.5	3.2	V
PB chrominance input (pin 55)						
V_{55}	DC voltage		1.7	2.0	2.3	V
V_{s55}	input signal (peak-to-peak value)		–	400	–	mV
V_{th}	threshold level of AGCKP1		2.6	3.0	3.4	V
Supply voltage Y (pin 56)						
I_{56R}	DC current	REC mode	40	–	60	mA
I_{56P}		PB mode	45	–	65	mA
Video output (pin 57)						
V_{SYT}	DC (sync tip)		0.95	1.1	1.25	V
V_{57}	EE output level (standard output level) (peak-to-peak value)	adjusted at pin 62	–	2.05	–	V
	EE output level (200 IRE) (peak-to-peak value)		2.12	2.22	2.32	V
	VV output level (peak-to-peak value)	V_{68} = 400 $mV_{(p-p)}$	1.80	2.05	2.30	V
WCSL	white clip suppression level	black to white = 100% and TRICK mode	115	135	–	%
V_{sout}	chrominance output level (peak-to-peak value)	V_{s55} = 0.4 $V_{(p-p)}$	1.3	1.55	1.8	V
ΔG_{55-57}	chrominance frequency response	V_{s55} = 400 $mV_{(p-p)}$ 5 MHz / 100 kHz	–1	–	+0.5	dB
V_{STL}	artificial sync tip level offset		–30	0	40	mV
V_{GL}	artificial grey level offset		0.85	1.0	1.15	V
α_{MU}	suppression at mute		40	–	–	dB
α_{ASP}	suppression of artificial sync pulse	REC mode	50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{do}	drop-out switch crosstalk	V_{68} = 400 $mV_{(p-p)}$ f_{68} = 1 MHz	–	–	–40	dB
t_{8-57}	drop-out switch delay on	f_8 = 4 MHz	–	0.45	1	µs
	drop-out switch delay off		3.0	4.0	5.0	µs
ΔV_{57}	drop-out switch DC offset		–25	0	+25	mV
ΔG	EE frequency response (5 MHz, referred to 100 kHz, $V_I = V_{60}$)		–1.0	–	0	dB
Noise canceller		PB				
$NC1_1$	response $NC1_1$	–30 dB; 1 MHz; NORM; note 2	–10	–8	–6	dB
$NC1_2$	response $NC1_2$	–30 dB; 2 MHz; NORM; note 2	–21	–15	–11	dB
$NC1_3$	response $NC1_3$	0 dB; 2 MHz; NORM; note 2	–1.5	–0.5	+0.5	dB
$NC1_{ED}$	response $NC1_{ED}$	–30 dB; 2 MHz; EDIT; note 2	–5.5	–4.0	–2.5	dB
$NC2_1$	response $NC2_1$	–30 dB; 1 MHz; NORM; note 3	–1.0	–0.5	+0.2	dB
$NC2_2$	response $NC2_2$	–30 dB; 2 MHz; NORM; note 3	–4.0	–2.5	–1.0	dB
$NC2_3$	response $NC2_3$	–30 dB; 3 MHz; NORM; note 3	–8.8	–6.8	–4.8	dB
$NC2_4$	response $NC2_4$	0 dB; 3 MHz; NORM; note 3	–1.25	–0.5	+0.25	dB
EDIT noise canceller		PB				
ED_1	depth 1	–30 dB recursive; note 4	–8.5	–7	–6	dB
ED_2	depth 2	–20 dB recursive; note 4	–5.2	–4.2	–3.2	dB
ED_3	depth 3	0 dB recursive; note 4	–1	–0.2	0	dB
Vertical noise canceller						
VNC_1	depth 1	–30 dB recursive; note 4	–10.2	–8.7	–7.7	dB
VNC_2	depth 2	–20 dB recursive; note 4	–9.2	–8.2	–7.2	dB
VNC_3	depth 3	0 dB recursive; note 4	–1.8	–0.4	0	dB
L1	limiter output level 1	V_{72} = 857 $mV_{(p-p)}$; f = 100 kHz; note 5	40	60	80	mV
L2	limiter output level 2	V_{72} = 285 $mV_{(p-p)}$; f = 100 kHz; note 5	40	60	80	mV
L3	limiter output level 3	V_{72} = 85 $mV_{(p-p)}$; f = 100 kHz; note 5	90	120	150	mV
L4	limiter output level 4	V_{72} = 285 $mV_{(p-p)}$; f = 1 MHz; note 5	150	200	250	mV
G_{AGC}	control characteristic of AGC	V_{s60} = 2.0 $V_{(p-p)}$/0.5 $V_{(p-p)}$	0	0.5	1.0	dB
COL_{AGC}	peak/keyed changeover level of AGC (black to white = 100%)	V_{s68} = 400 $mV_{(p-p)}$	107	112	117	%
P_{AGC}	peak AGC characteristic (window signal → 2 µs white over 20 lines, 100% = 2.05 $V_{(p-p)}$)	video/sync = 5.0	110	–	130	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	S/N (RMS value related to black/white amplitude)	100 kHz to 5 MHz; EE mode	60	–	–	dB
α_{cr}	FM carrier crosstalk suppression	0 dB = 2.05 $V_{(p-p)}$; f_{FM} = 5 MHz	60	–	–	dB
t_A	attack time of AGC	V_{s60}: 0.5 $V_{(p-p)} \rightarrow$ 1.0 $V_{(p-p)}$	–	–	0.1	s
t_R	recovery time of AGC	V_{s60}: 2.0 $V_{(p-p)} \rightarrow$ 1.0 $V_{(p-p)}$	–	–	0.5	s
VHS_{cg}	VHS standard (signal amplitude in case of copy guard)	100% = 2.05 $V_{(p-p)}$	35	–	48	%
Artificial sync control (pin 58)						
V_{58}	DC level	pin open-circuit	–	0.5	1.0	V
V_{thr}	voltage range of through mode		0	–	1.25	V
V_{arts}	voltage range of artificial H SYNC mode (inserts grey level and artificial H SYNC)		1.75	–	3.0	V
V_{artV}	voltage range of artificial V SYNC mode (inserts sync level)		3.5	–	5.0	V
Sub clamp detector (pin 59)		open base and collector				
V_{59}	detecting voltage		1.75	–	2.75	V
Video input (pin 60)						
V_{60}	DC level		2.35	2.75	3.15	V
V_{s60}	input level (CVBS signal) (peak-to-peak value)		0.3	1.0	2.0	V
AGC detector (pin 61)						
V_{61}	detecting voltage	V_{s60} = 1 $V_{(p-p)}$	1.8	–	2.6	V
EE adjust control (pin 62)		open base				
V_{ctrl}	active range of control	V_{s57} = 2.05 $V_{(p-p)}$; V_{s60} = 1 $V_{(p-p)}$	2.0	2.5	3.0	V
Simple SVHS mode control (pin 63)						
V_{63}	DC level	pin open-circuit	–	–	0.5	V
V_{VHS}	normal VHS mode		0	–	2.0	V
V_{SVHS}	simple SVHS mode		2.5	–	5	V
Sync separator output (pin 64)		push/pull output				
V_H	high level	R_L = 2 kΩ to GND	4.5	–	–	V
V_L	low level	R_L = 10 kΩ to V_{CC}	–	–	0.3	V
SEN	input sensitivity (slicing level for SYNC level = 100% at pin 68 = 120 mV)		26	33	40	%
t_{68-64}	front edge delay		600	750	900	ns
Sync separator detector (pin 65)						
V_{65}	detecting voltage		2.3	–	3.3	V
EDIT control (pin 66)						
V_{66}	DC level	pin open-circuit	–	–	0.5	V
V_{YNRO}	voltage range of YNR ON mode		0	–	1.25	V
V_{YNRF}	voltage range of YNR OFF mode		1.75	–	3.0	V
V_{EDIT}	voltage range of EDIT mode		3.5	–	5.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Y-LPF output (pin 67)						
V_{SYT}	output sync tip level		1.0	1.3	1.6	V
V_{67}	output signal (peak-to-peak value)	EE and VV mode; V_{57} = 2.05 V	350	400	450	mV
NL de-emphasis		VV mode; note 6				
S1	response S1	–20 dB; 500 kHz; SP	–2.9	–1.9	–0.9	dB
S2	response S2	–20 dB; 2 MHz; SP	–7.3	–5.8	–4.5	dB
L1	response L1	–20 dB; 500 kHz; LP	–5.8	–4.3	–3.0	dB
L2	response L2	–20 dB; 2 MHz; LP	–10.3	–8.8	–7.3	dB
L3	response L3	0 dB; 2 MHz; LP	–4.5	–3.2	–2.0	dB
Clamp 1 input (pin 68)		open base for clamp off				
V_{s68}	input signal (peak-to-peak value)		–	400	–	mV
V_{CLON}	DC level, when clamp is on (no signal)		2.0	2.1	2.2	V
Clamp 2 input (pin 69)		open base for clamp off				
V_{s69}	input signal (peak-to-peak value)		–	400	–	mV
V_{CLON}	DC level, when clamp is on (no signal)		2.0	2.1	2.2	V
To CCD drive (pin 70)						
V_{SYT}	output sync tip level		0.9	1.4	1.9	V
V_{70}	output signal (peak-to-peak value)		350	400	450	mV
Delta Y output (pin 71)						
V_{s71}	output signal (peak-to-peak value)	V_{s68} = 400 $mV_{(p-p)}$; 100 kHz; pin 69 capacitively to GND EDNC mode VNC mode	 4.8 2.7	 6.3 4.2	 7.8 5.7	 dB dB
V_{71}	DC level		1.4	2.1	2.8	V
Correlation input (pin 72)						
V_{72}	DC level		2.0	2.45	3.0	V
L_{COR}	threshold level of correlation 1 (for chrominance non correlation switch, related to maximum output level at pin 71)		4	5	6	%
NC1 LPF (pin 74)						
V_{74}	DC level		1.1	1.3	1.5	V
NC2 LPF (pin 75)						
V_{75}	DC level		1.1	1.3	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Picture control (pin 76)						
V_{76}	DC level	pin open-circuit	2.3	2.5	2.7	V
V_{SHA}	DC range of 'picture sharp'		0	–	2.3	V
V_{SOF}	DC range of 'picture soft'		2.7	–	5	V
R1	response 1	V_{s76} = 0 V; 0.5 MHz; note 7	0	0.5	1.0	dB
R2	response 2	V_{s76} = 0 V; 2 MHz; note 7	3.0	4.5	6.0	dB
R3	response 3	V_{s76} = 5 V; 0.5 MHz; note 7	−2.0	−1.0	−0.5	dB
R4	response 4	V_{s76} = 5 V; 2 MHz; note 7	−6.7	−5.2	−3.7	dB
R5	response 5	V_{s76} = 2.5 V; 2 MHz; note 7	−0.3	+0.2	+0.7	dB
t_{DL}	delay time (pin 57 to pin 68)	V_{s76} = 2.5 V; 0.1 MHz	185	210	235	ns
NLE output (REC) / MDE output (PB) (pin 77)						
V_{SYT}	sync tip DC level	REC	1.6	1.9	2.2	V
		PB; V_7 = 1.7 V	1.2	1.6	2.0	V
V_{s77R}	output signal (peak-to-peak value)	REC	–	400	–	mV
V_{s77P}		PB	–	300	–	mV
REC: Non linear emphasis (NLE) / detail enhancer (DTE); note 8						
R_{D1}	response D1	−20 dB; 500 kHz; SP; NORM	1.7	2.7	3.7	dB
R_{D2}	response D2	−20 dB; 2 MHz; SP; NORM	4.25	5.75	7.25	dB
R_{S1}	response S1	−20 dB; 500 kHz; SP; EDIT	1.0	1.7	2.4	dB
R_{S2}	response S2	−20 dB; 2 MHz; SP; EDIT	3.0	4.0	5.0	dB
R_{L1}	response L1	−20 dB; 500 kHz; LP	3.1	4.4	5.7	dB
R_{L2}	response L2	−20 dB; 2 MHz; LP	5.5	7.5	9.5	dB
R_{L3}	response L3	0 dB; 2 MHz; LP	0.9	1.6	2.3	dB
REC: Vertical emphasis; note 9						
P_{L1}	peak level 1	−30 dB recursive	3.0	4.0	5.0	dB
P_{L2}	peak level 2	−20 dB recursive	2.5	3.0	3.5	dB
P_{L3}	peak level 3	0 dB recursive	0	0.2	1.0	dB
ΔG_{77}	white level expansion	V_{68} = 100 $mV_{(p-p)}$; f_{68} = 10 kHz; V_{68DC} = 2.0/2.4 V	0	3	5	%
Clamp 3 input (pin 78)		open base for clamp off				
V_{s78R}	input signal (peak-to-peak value)	REC	–	400	–	mV
V_{s78P}		PB	–	300	–	mV
V_{78CO}	DC level, when clamp is on		1.3	1.5	1.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Negative feedback input of main emphasis (pin 79)		open base				
Main emphasis output (pin 80)						
V_{SYT}	DC level (sync tip)	feedback closed	1.9	2.1	2.3	V
V_{s80}	output signal (peak-to-peak value)	V_{s57} = 2.05 $V_{(p-p)}$; V_{60} = 1 $V_{(p-p)}$	350	400	450	mV
DCL	dark clip level	$V_I = V_{s78}$ = 400 $mV_{(p-p)}$	45	55	65	%
WCL	white clip level	$V_I = V_{s78}$ = 400 $mV_{(p-p)}$; V_2 = 2.35 V	150	190	230	%
G_{78-80}	flat amplifier gain	f = 100 kHz; note 10	12	14	16	dB
ΔG_{78-80}	flat amplifier frequency characteristics	f = 3 MHz/100 kHz; note 10	−1	–	0.5	dB
ΔV_{80}	DC offset between rotary HIGH and LOW		2.8	3.2	3.6	mV

Notes to the characteristics

1. The blanking of BGP starts at first equalizing pulse and stops 24 lines after rotary transition.
2. All values referred to 100 kHz, V_{76} = 2.5 V
   Input: 0 dB = V_{68} = 400 $mV_{(p-p)}$
   Output: 0 dB = V_{57} at 100 kHz and given input level
   pin 74: R = 2.2 kΩ, C = 68 pF
   pin 75: C = 22 µF
3. All values referred to 100 kHz, V_{76} = 2.5 V
   Input: 0 dB = V_{68} = 400 $mV_{(p-p)}$
   Output: 0 dB = V_{57} at 100 kHz and given input level
   pin 74: C = 22 µF
   pin 75: R = 1.2 kΩ, C = 3.3 nF
4. V_{76} = 2.5 V
   Input: 0 dB = V_{68} = 400 $mV_{(p-p)}$
   Output: 0 dB = V_{57} at 1, 2, 3, ... x f_H and given input level
5. All measurements with sinusoidal input signal; output signal at pin 57 measured between $\frac{\pi}{4}$ and $\frac{3\pi}{4}$
6. All values referred to 10 kHz
   Input: 0 dB = V_{78} = 300 $mV_{(p-p)}$
   Output: 0 dB = V_{67} at 10 kHz and given input level
7. All values referred to 100 kHz
   Input: V_{s68} = 40 $mV_{(p-p)}$ (−20 dB)
   Output: 0 dB = V_{57} at 100 kHz and given input level
8. All values referred to 10 kHz
   Input: 0 dB = V_{s68} = 400 $mV_{(p-p)}$
   Output: 0 dB = V_{77} at 10 kHz and given input level
9. Input: 0 dB = V_{s68} = 400 $mV_{(p-p)}$
   Output: 0 dB = V_{77} at 1, 2, 3, ... x f_H and given input level
10. Input: V_{78} = 75 $mV_{(p-p)}$
    R(pin 78/80) = 1 kΩ
    R/C(pin 79) = 220 Ω/0.1 µF

CHROMINANCE FILTER

Table 1 Low-pass filter 630 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LPF 630		PAL/EE				
Frequency response pin 46 to pin 34						
ΔG1	frequency response (1)	1 MHz/0.2 MHz	–4	–3	–2	dB
ΔG2	frequency response (2)	1.5 MHz/0.2 MHz	–9	–7	–5	dB
ΔG3	frequency response (3)	2 MHz/0.2 MHz	–10	–14	–18	dB
ΔG4	frequency response (4)	3 MHz/0.2 MHz	–	–	–25	dB
ΔG5	frequency response (5)	4.43 MHz/0.2 MHz	–	–	–40	dB
ΔG7	frequency response (7)	9.5 MHz/0.2 MHz	–	–	–35	dB
t_d	group delay (1)	0.2 MHz	245	285	325	ns
		SECAM/EE				
ΔG2	frequency response (2)	1.5 MHz/0.2 MHz	–5	–3	–1	dB

Table 2 Band-pass filter 4.43 MHz at EE mode.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BPF 4.43		PAL/EE				
Frequency response pin 60 to pin 39						
ΔG1	frequency response (1)	< 2.7 MHz/4.43 MHz	–	–	–22	dB
ΔG2	frequency response (2)	2.7 MHz/4.43 MHz	–	–	–30	dB
ΔG3	frequency response (3)	3.93 MHz/4.43 MHz	–2	–1	0	dB
ΔG4	frequency response (4)	4.93 MHz/4.43 MHz	–3	–2	–1	dB
ΔG6	frequency response (5)	6.2 MHz/4.43 MHz	–	–	–30	dB
ΔG7	frequency response (6)	> 6.2 MHz/4.43 MHz	–	–	–15	dB
t_d	group delay (1)	4.43 MHz	380	420	460	ns
		SECAM/EE				
ΔG7	frequency response (6)	6.0 MHz/4.43 MHz	–	–	–30	dB

Table 3 Band-pass filter 4.43 MHz at VV mode.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BPF 4.43		PAL/VV				
Frequency response pin 46 to pin 48						
ΔG1	frequency response (1)	< 2.7 MHz/4.43 MHz	–	–	–20	dB
ΔG2	frequency response (2)	2.9 MHz/4.43 MHz	–	–	–30	dB
ΔG3	frequency response (3)	3.9 MHz/4.43 MHz	–3	–2	–1	dB
ΔG4	frequency response (4)	4.93 MHz/4.43 MHz	–3.5	–2.5	–1.5	dB
ΔG5	frequency response (5)	5.7 MHz/4.43 MHz	–	–21	–15	dB
ΔG6	frequency response (6)	6 MHz/4.43 MHz	–	–	–30	dB
ΔG7	frequency response (7)	> 6 MHz/4.43 MHz	–	–26	–15	dB
t_d	group delay (1)	4.43 MHz	420	460	500	ns
		SECAM/VV				
ΔG2	frequency response (2)	2.7 MHz/4.43 MHz	–	–	–30	dB

Table 4 Band-pass filter 630 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BPF 630		VV				
Frequency response pin 41 to pin 39						
ΔG1	frequency response (1)	< 100 Hz/630 kHz	–	–	–20	dB
ΔG2	frequency response (2)	100 kHz/630 kHz	–7	–5	–3	dB
ΔG3	frequency response (3)	930 kHz/630 kHz	–3	–2	–1	dB
ΔG4	frequency response (4)	1.5 MHz/630 kHz	–	–15	–10	dB
ΔG5	frequency response (5)	2.3 MHz/630 kHz	–	–	–40	dB
ΔG6	frequency response (6)	> 2.4 MHz/630 kHz	–	–	–35	dB
t_d	group delay (1)	630 kHz	710	750	790	ns
Δt_d	delta group delay	SVHS / VHS	–200	–160	–120	ns

LUMINANCE FILTER

Table 5 Luminance main low-pass filter.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YLPF		EE				
Frequency response pin 60 to pin 67						
ΔG1	frequency response (1)	2 MHz/0.2 MHz	–2.5	–1.0	0	dB
ΔG2	frequency response (2)	3 MHz/0.2 MHz	–4.5	–3.0	–1.5	dB
ΔG3	frequency response (3)	4.43 MHz/0.2 MHz	–	–40	–30	dB
t_d	group delay (1)	0.2 MHz	660	700	740	ns

Table 6 Demodulator low-pass filter.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DLPF		VV				
Frequency response from demodulator output to pin 4						
ΔG1	frequency response (1)	3 MHz/0.2 MHz	–4.5	–	0	dB
ΔG2	frequency response (2)	6 MHz/0.2 MHz	–	–25	–15	dB

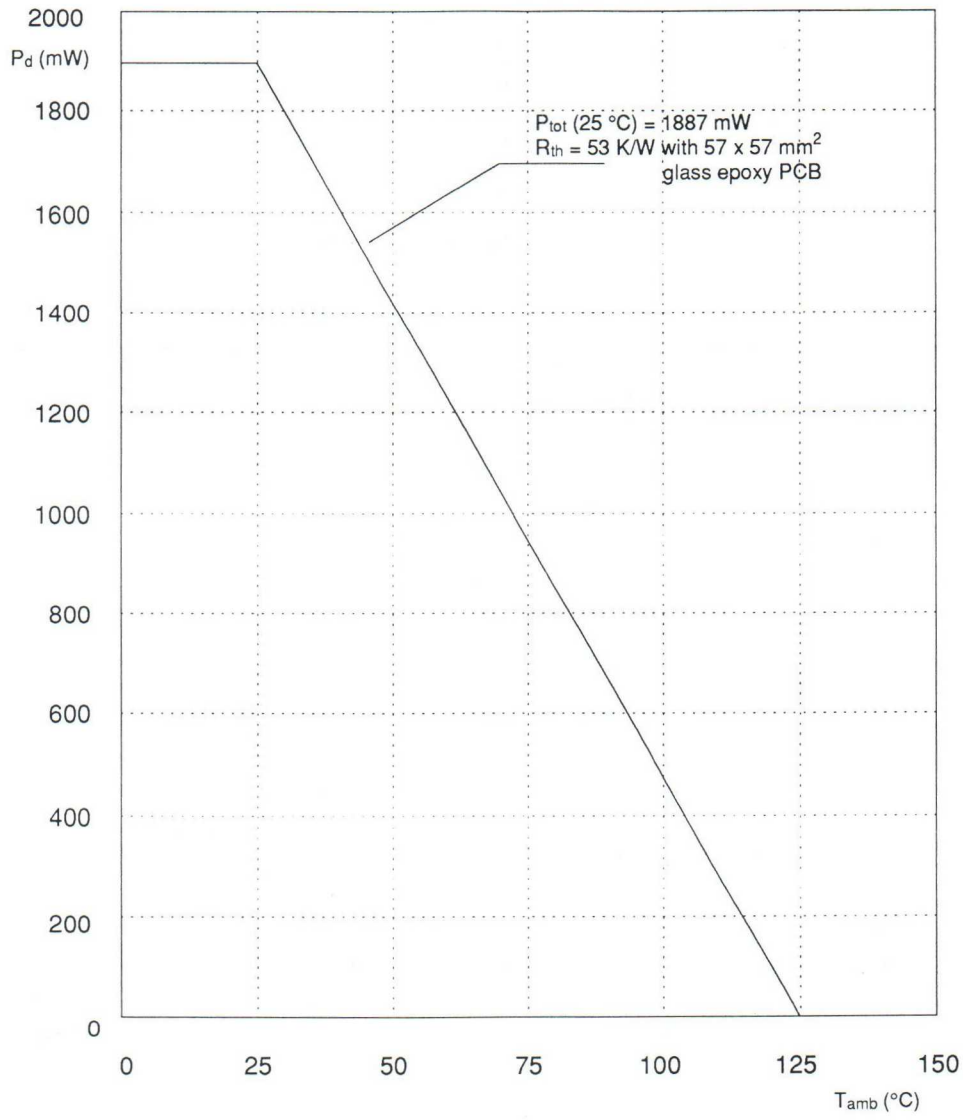


Fig.3 Power dissipation; ambient temperature.

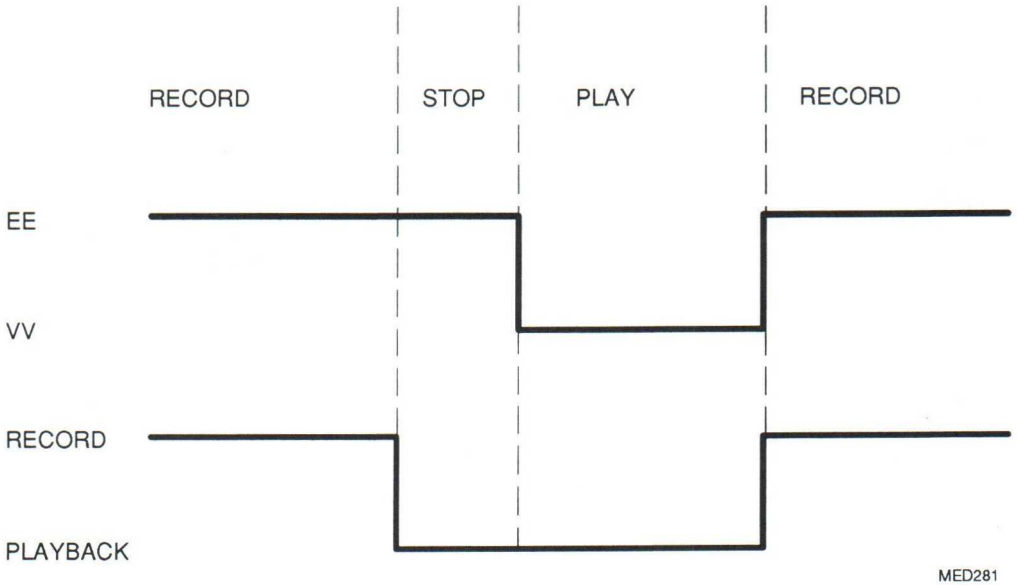


Fig.4 VCR/IC modes.

	PAL		NTSC		
	SP	LP	SP	LP	EP
NORM	2	1	4	2	2
TRICK	2	1	2	2	2

MED282

Fig.5 Sensitivity of PB APC (multiplication factor for phase detector sensitivity).

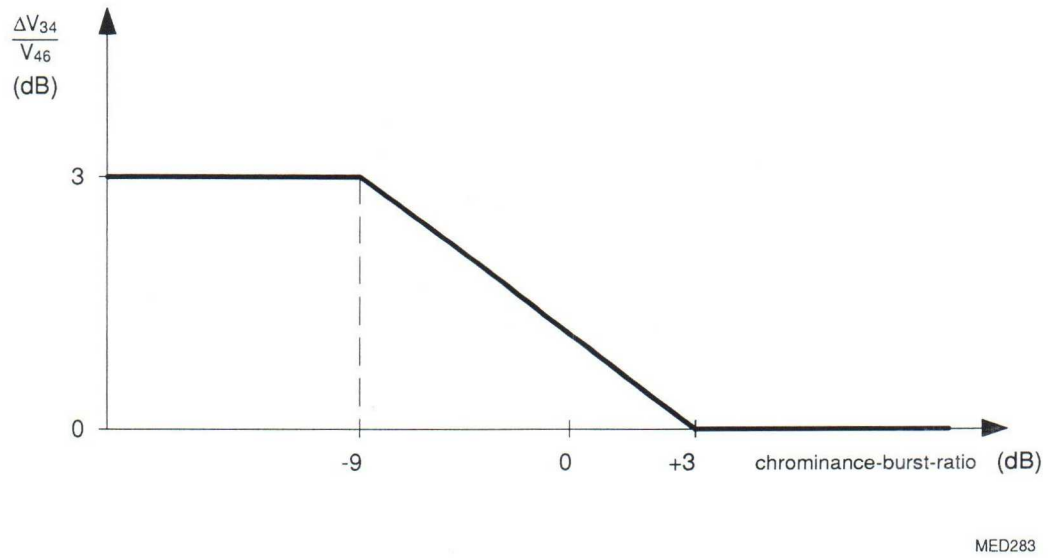


Fig.6 CACC control characteristics.

		CACC
NTSC	SP	ON
	LP	OFF
	EP	ON
PAL	SP	ON
	LP	OFF
SECAM	SP	OFF
	LP	

MED284

Fig.7 CACC logic.

		1.5 dB up
NTSC	SP	OFF
	LP	ON
	EP	
PAL	SP	OFF
	LP	ON
SECAM	SP	ON
	LP	

MED285

Fig.8 1.5 dB up gain logic.

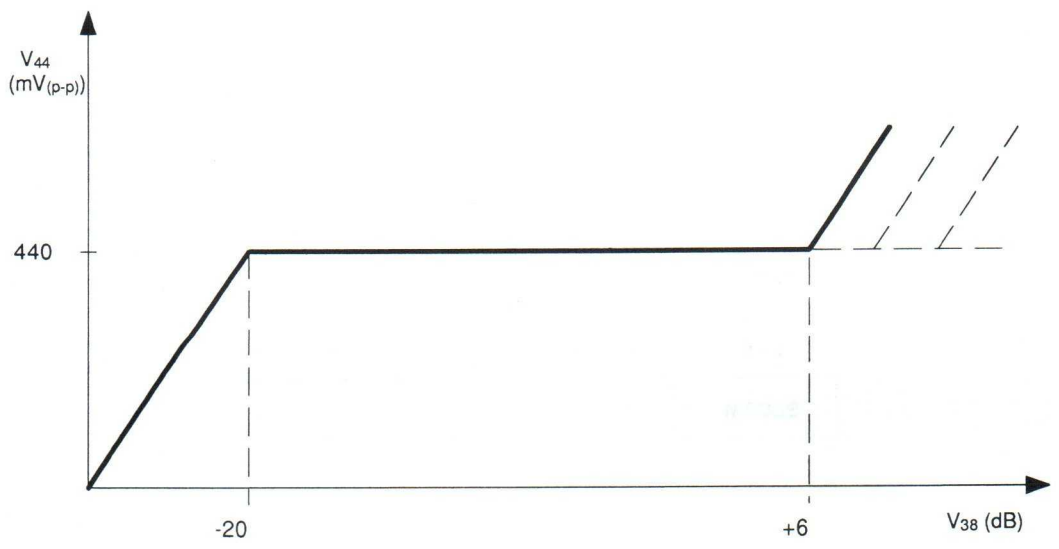


Fig.9 ACC characteristics.

		CNR
NTSC	NORM	OFF
	EDIT	
	pin 42 to V_{CC}	
	NCorr	
PAL	NORM	ON
	EDIT	OFF
	pin 42 to V_{CC}	
	NCorr	
SECAM	NORM	OFF
	EDIT	
	pin 42 to V_{CC}	
	NCorr	

MED287

Fig.10 CNR logic (NCorr: non correlation of luminance signal).

			BURST DOWN
EE	any mode		OFF
VV	NTSC	SP	ON (–5.0 dB)
		LP	OFF
		EP	ON (–4.0 dB)
	PAL		OFF
	SECAM		OFF

MED288

Fig.11 Burst down logic.

			SP	LP
FILTER	Y MAIN LPF		$f_c \approx 3$ MHz; 4.43 MHz Trap	
	Y SUB LPF (demodulation output)		$f_c \approx 3$ MHz	
YNR	REC	EDIT; pin 66 = H	OFF	
		YNR OFF; pin 66 = M	OFF	
		YNR ON; pin 66 = L	OFF	vertical emphasis
	PB	EDIT; pin 66 = H	OFF	EDNC
		YNR OFF; pin 66 = M	OFF	
		YNR ON; pin 66 = L	EDNC	VNC
NLE NLDE	REC	EDIT; pin 66 = H	NLE(C)	NLE(D)
		YNR OFF; pin 66 = M	NLE(C) + DTE	
		YNR ON; pin 66 = L		
	PB		NLDE(C)	NLDE(D)
FM Carrier Interleave			ON	

Fig.12 Operation mode diagram (Y-block) - part 1.

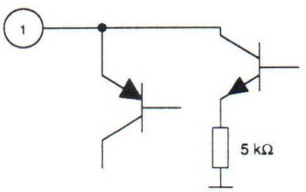
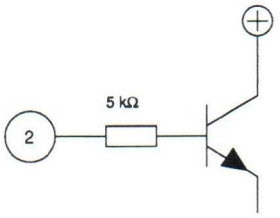
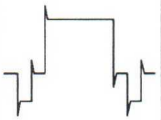
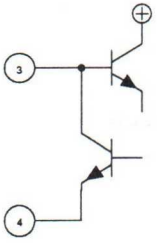
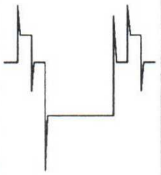
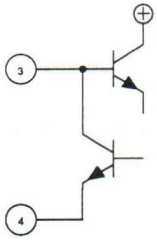
FUNCTION	CONDITION		OPERATION
main clamp pin 68	REC		ON
	PB	NORM	
		dropout; see note	OFF
emergency clamp	REC		ON
	PB	NORM	
		TRICK; pin 11 = L	OFF
noise canceller	REC		OFF
	PB	EDIT; pin 66 = H	ON (–6 dB)
		YNR ON; pin 66 = L	ON
		YNR OFF; pin 66 = M	
picture control	REC		OFF
	PB	EDIT; pin 66 = H	
		YNR ON; pin 66 = L	ON
		YNR OFF; pin 66 = M	
artificial H/V switch	REC		through
	PB	VIDEO; pin 58 = L	
		GREY; pin 58 = M	grey level (30%)
		SYNC; pin 58 = H	sync tip level
search noise clip	REC		OFF
	PB	NORM	
		TRICK; pin 11 = L	ON
SVHS PB	PB	VHS; pin 63 = L	VHS
		SQPB; pin 63 = M/H	SVHS

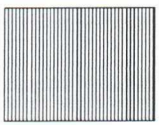
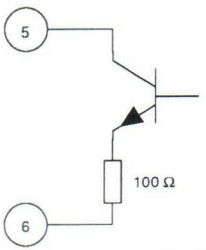
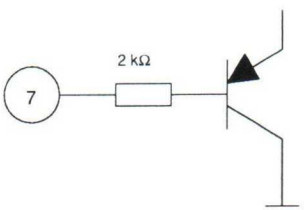
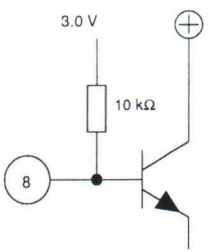
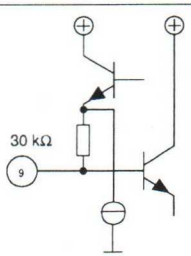
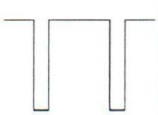
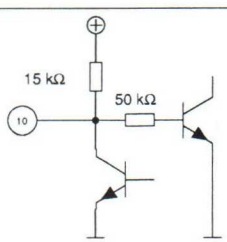
Note to Fig.13

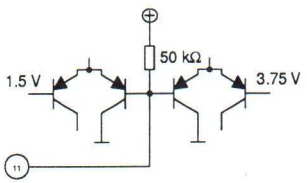
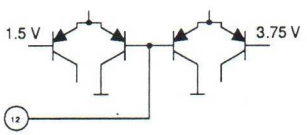
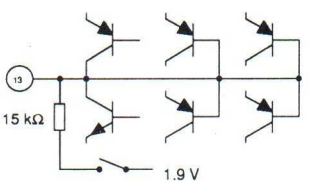
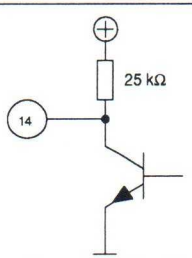
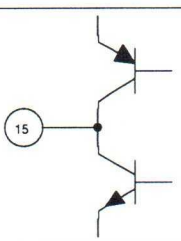
Same timing as DOC SW.

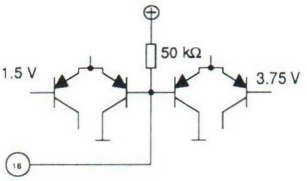
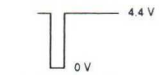
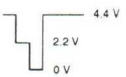
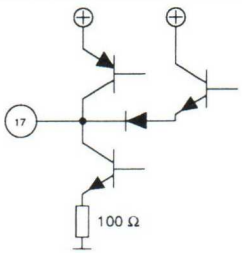
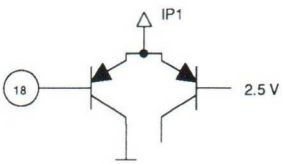
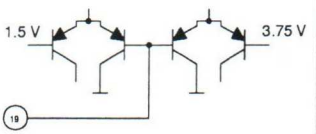
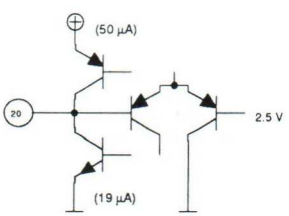
Fig.13 Operation mode diagram (Y-block) - part 2.

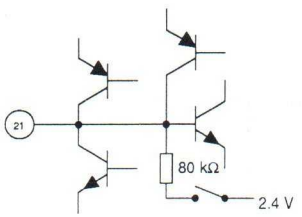
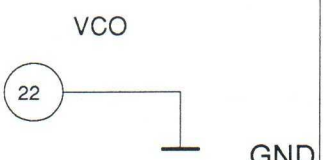
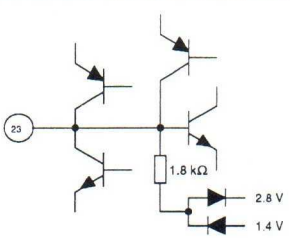
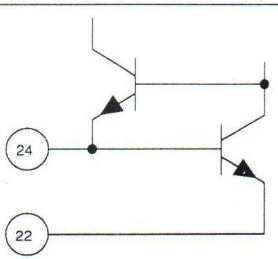
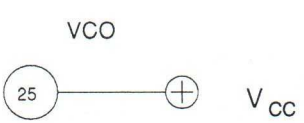
Table 7 Internal circuitry.

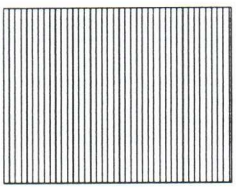
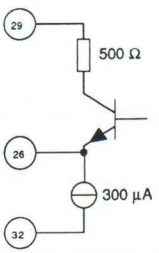
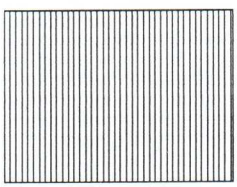
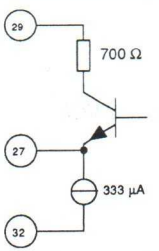
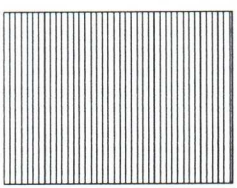
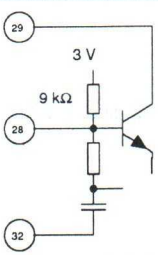
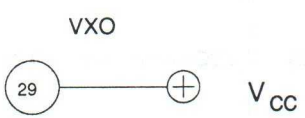
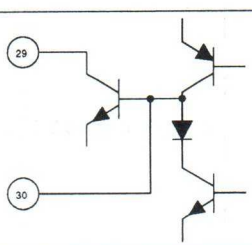
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
1	modulator input		2.1 V		V_T / I_E	
2	white clip control		2.35 V		OB	
3	main de-emphasis output	3.0 (sync)		 300 $mV_{sync/white}$	OC	
4	main de-emphasis and peaking	2.0 (sync)		 300 $mV_{sync/white}$	V_T / I_E	
5	supply voltage modulator	5.0				Modulator 

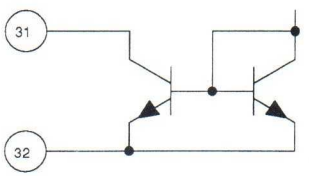
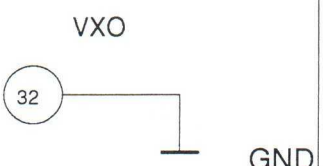
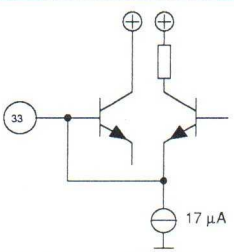
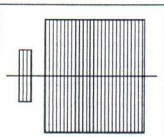
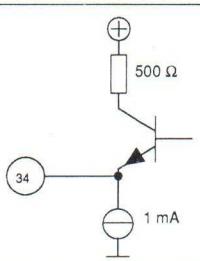
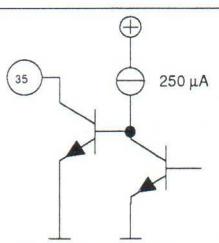
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
6	FM output	3.3	 900 $mV_{(p-p)}$		V_T / I_E + 100 Ω	
7	demodulator gain control	1.7 (typ)			OB	
8	PB FM input	3.0			10 kΩ	
9	envelope detector		(4.7 V)	(3.7 V) 2.3 V (no signal)	30 kΩ	
10	drop out pulse output		4.15 V	 HIGH 4.15 V LOW 0 V	15 kΩ	

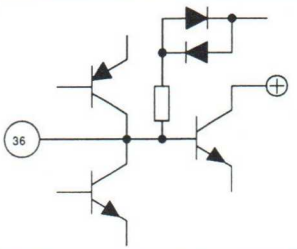
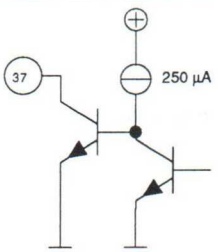
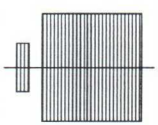
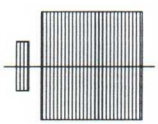
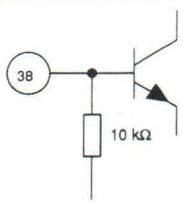
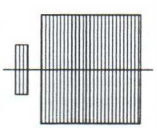
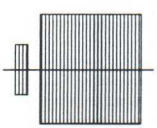
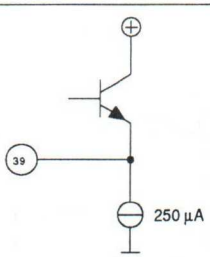
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
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12	switch (SP/LP/EP)		0 V ... 1.25 V (SP) 1.75 V ... 3 V (LP) 3.5 V ... 5 V (EP)		OB	
13	colour killer pin		1.8 V without chrominance signal colour on > 2.2 V colour off < 2.0 V			
14	skew output		HIGH (4.95 V) or LOW (0.2 V)		25 kΩ	
15	frequency correction output	(2.1)	current ± 17 μA if active			

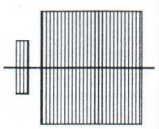
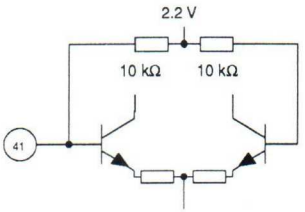
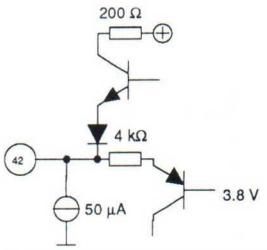
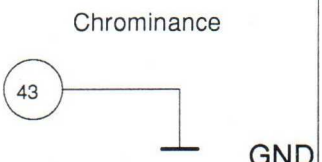
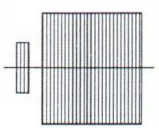
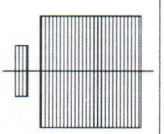
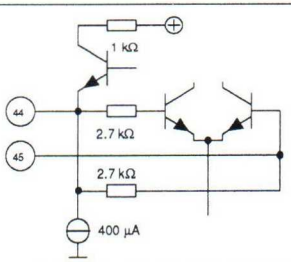
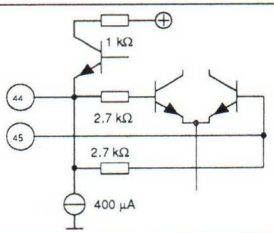
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
16	switch (REC/PB/ID)		0 V ... 1.25 V	1.75 V ... 3 V (PB) 3.5 V ... 5 V (ID)	50 kΩ	
17	sandcastle, BGP output (LOW active)		 with 20 kΩ to GND  with 20 kΩ to Vcc			
18	rotary pulse		Channel 1: 3 V ... 5 V Channel 2: 0 V ... 2 V		OB	
19	switch (C/BW/NORM)		0 V ... 1.25 V (NORM) 1.75 V ... 3 V (BW) 3.5 V ... 5 V (C)		OB	
20	mute detector		4.8 V at coincidence 0 V at no coincidence V_{th} = 2.5 V			

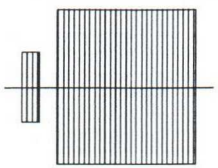
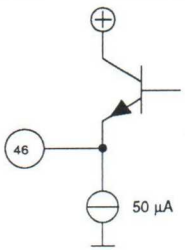
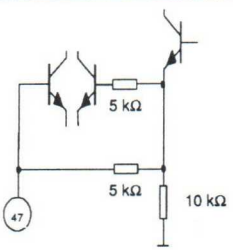
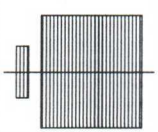
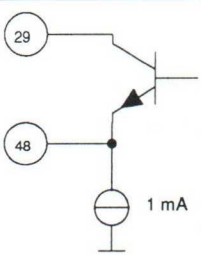
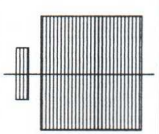
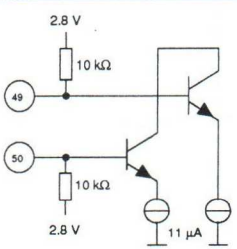
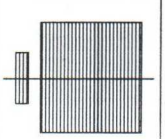
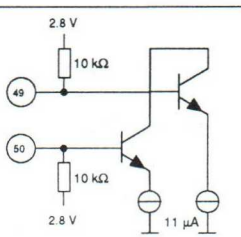
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
21	loop filter (EE) VXO	2.4				
22	ground VCO	0				
23	loop filter VCO	2.1				
24	VCO bias current	0.65				
25	supply voltage VCO	5.0				

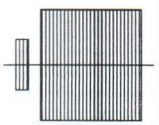
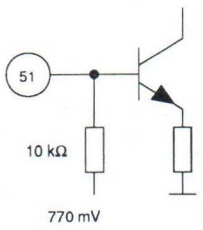
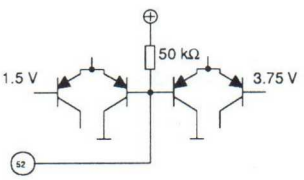
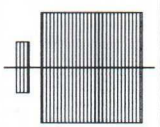
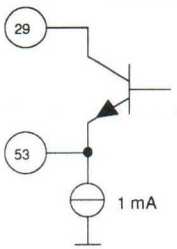
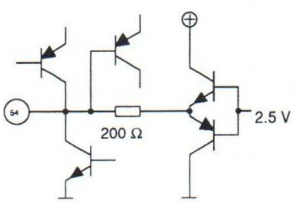
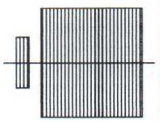
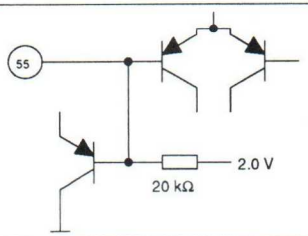
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
26	f_{SC} output	2.3	 600 $mV_{(p-p)}$		V_T / I_E	
27	VXO (crystal output)		 260 $mV_{(p-p)}$ EE → 3.4 V / VV → 3.55 V		V_T / I_E	
28	VXO (crystal input)	3.0	 260 $mV_{(p-p)}$		9 kΩ	
29	supply voltage VXO	5.0				
30	filter reference terminal (chrominance filter)	3.0				

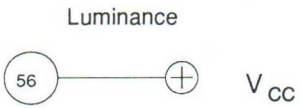
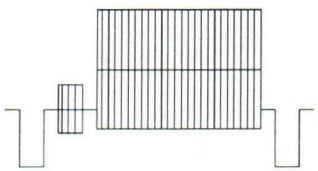
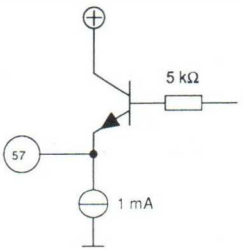
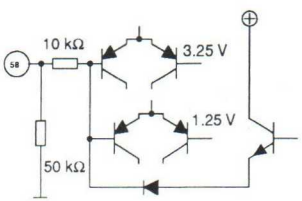
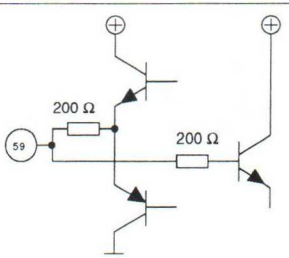
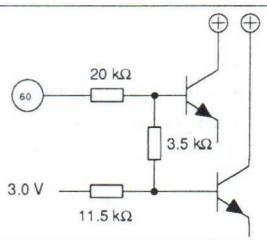
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
31	2fsc output	5.0	60 $mV_{(p-p)}$ with R_L = 1 kΩ		OC	
32	ground VXO	0				
33	loop filter CACC	(2.5)				
34	CACC output	2.5	 660 $mV_{(p-p)}$ at SP 2.5 V colour on 0 V colour off	2.5 V colour on 0 V colour off	V_T / I_E	
35	ACC loop filter switch (Channel 2)		non conductive during Channel 1 or TRICK		OC	

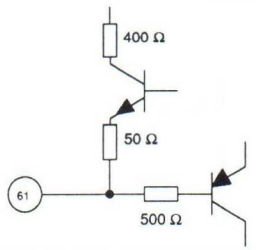
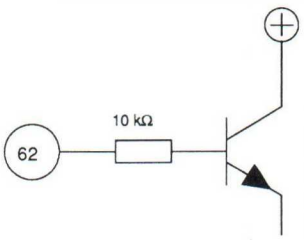
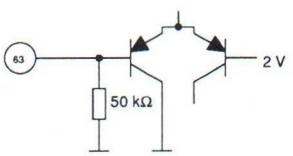
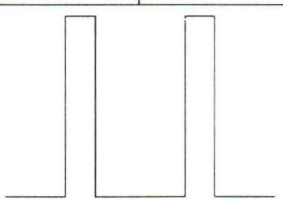
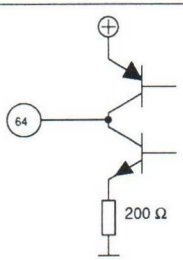
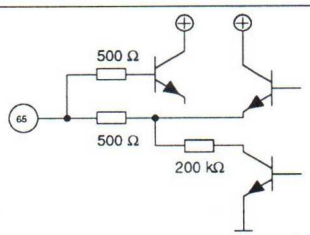
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
36	ACC loop filter	(3.4)				
37	ACC loop filter switch (Channel 1)	0.3	non conductive during Channel 2 or TRICK		OC	
38	ACC input	1.6	 135 $mV_{(p-p)}$	 110 $mV_{(p-p)}$	10 kΩ	
39	BPF switch output		 135 $mV_{(p-p)}$ 2.4 V	 110 $mV_{(p-p)}$ 3.0 V	V_T / I_E	
40	supply voltage chrominance part	5.0				Chrominance 

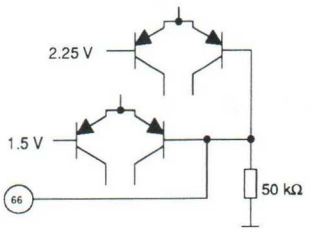
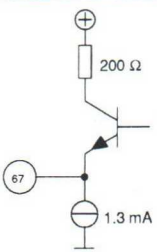
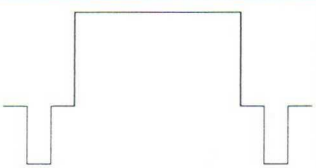
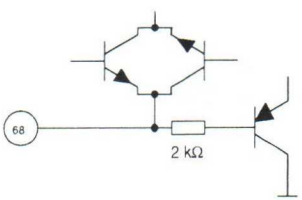
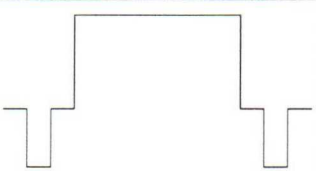
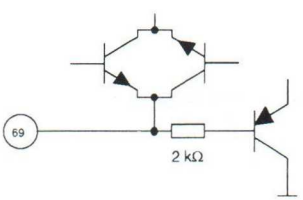
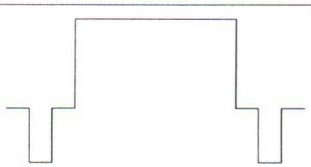
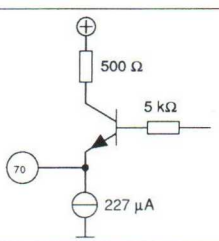
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
41	PB chrominance from tape	2.2		 110 $mV_{(p-p)}$ (FM + CHR → 330 $mV_{(p-p)}$)	10 kΩ	
42	CNR test pin	3.0		 noise > 4.8 V: CNR OFF		
43	ground chrominance part	0				
44	test pin 2	2.25	 440 $mV_{(p-p)}$	 440 $mV_{(p-p)}$		
45	mixer balance	2.25				

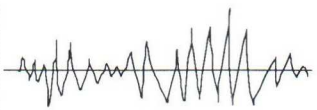
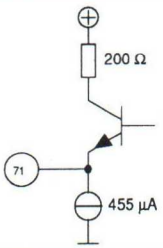
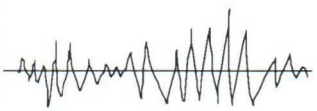
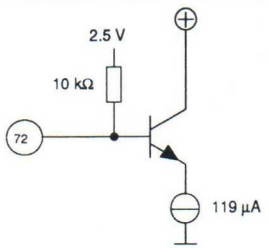
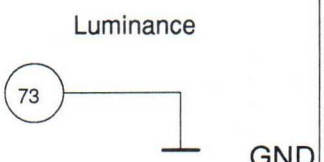
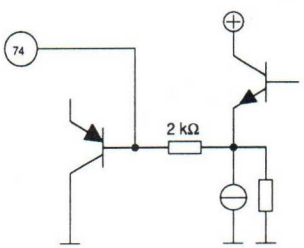
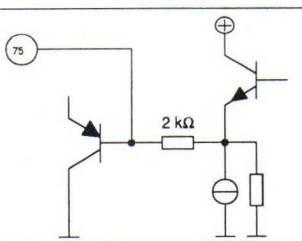
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
46	test pin 1	2.2	 110 $mV_{(p-p)}$ lower sideband (selectively measured)			
47	AC coupling	2.2				
48	output comb driver (VV)	2.5		 620 $mV_{(p-p)}$ (PAL) 350 $mV_{(p-p)}$ (NTSC)	V_T / I_E	
49	through side chrominance input	2.7		 110 $mV_{(p-p)}$	10 kΩ	
50	comb side chrominance input	2.7		 110 $mV_{(p-p)}$	10 kΩ	

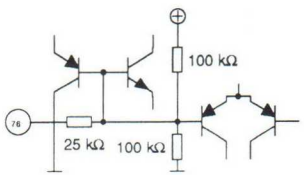
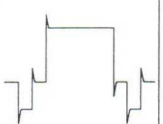
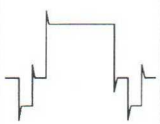
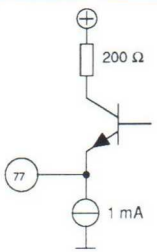
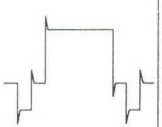
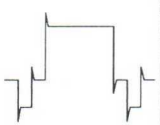
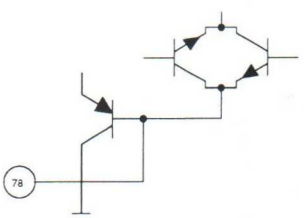
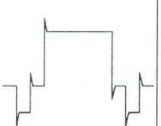
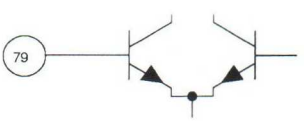
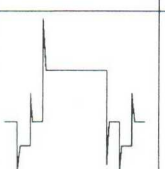
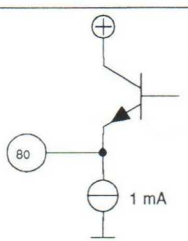
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
51	CNR limiter input	0.77		 39 $mV_{(p-p)}$		
52	switch (PAL / SECAM / NTSC)		0 V ... 1.25 V (NTSC) 1.75 V ... 3 V (PAL) 3.5 V ... 5 V (SECAM)		50 kΩ	
53	chrominance output	3.0		 880 $mV_{(p-p)}$	V_T / I_E	
54	filter reference terminal (luminance filter)	2.5			OB OC	
55	PB chrominance input		0 V HIGH: no reaction on copyguard LOW: AGC reacts on copyguard V_{th} = 3.0 V	 400 $mV_{(p-p)}$ 2.0 V	20 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
56	supply voltage luminance part	5.0				
57	video output	1.1 (sync)	 2.05 $V_{sync/white}$		V_T / I_E	
58	artificial sync control			0 V ... 1.25 V (VIDEO) 1.75 V ... 3 V (GREY + H_{sync}) 3.5 V ... 5 V (SYNC)	50 kΩ	
59	sub clamp detector	2.3				
60	video input		 1.0 $V_{(p-p)}$ 2.75 V	3.0 V	35 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
61	AGC detector		2.2 V	1.85 V	V_T / I_E + 450 Ω	
62	EE adjust control	2.5 (typ)			OB	
63	simple SVHS mode control			0 V ... 2 V (VHS) 2.5 V ... 5 V (SVHS)	50 kΩ	
64	sync separator output		 HIGH: 5 V LOW: 0 V			
65	sync separator detector	2.8			V_T / I_E + 500 Ω	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
66	EDIT control		0 V ... 1.25 V (YNR ON) 1.75 V ... 3 V (YNR OFF) 3.5 V ... 5 V (EDIT)		50 kΩ	
67	Y-LPF output		 400 $mV_{sync/white}$ EE → 1.2 V (sync) / VV → 1.4 V (sync)		V_T / I_E	
68	clamp 1 input	2.1 (sync)	 400 $mV_{sync/white}$			
69	clamp 2 input	2.1 (sync)	 400 $mV_{sync/white}$			
70	to CCD drive	1.4 (sync)	 400 $mV_{sync/white}$		V_T / I_E	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
71	delta Y output	2.1	 noise		V_T / I_E	
72	correlation input	2.45	 noise		10 kΩ	
73	ground luminance part	0				
74	NC1 LPF		0 V	 noise 1.3 V	2 kΩ	
75	NC2 LPF		0 V	 noise 1.3 V	2 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVE FORM EE	WAVE FORM VV	Z	INTERNAL CIRCUIT
76	picture control	2.5				
77	NLE output (REC) / MDE output (PB)		 400 $mV_{sync/white}$ 1.9 V (sync)	 300 $mV_{sync/white}$ 1.6 V (sync)	V_T / I_E	
78	clamp 3 input	1.5 (sync)	 400 $mV_{sync/white}$	 300 $mV_{sync/white}$		
79	negative feedback input of main emphasis	2.1 (sync)	 400 $mV_{sync/white}$		OB	
80	main emphasis output	2.1 (sync)	 400 $mV_{sync/white}$		V_T / I_E	

VIF-PLL demodulator and FM-PLL detector TDA9800

FEATURES

- Suitable for negative vision modulation
- Applicable for IF frequencies of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band VIF amplifier (AC coupled)
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Alignment-free FM-PLL detector with high linearity
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (300 mW at +5 V supply voltage).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	51	60	69	mA
$V_{i\,IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control	64	70	73	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{0.92/1.1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{2.76/3.3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{o\,AF}$	maximum AF output signal for THD < 1.5% (RMS value, pin 9)	0.8	–	–	V
T_{amb}	operating ambient temperature	–20	–	+70	°C

GENERAL DESCRIPTION

The TDA9800 is a monolithic integrated circuit for vision and sound IF signal processing in TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9800	20	DIL	plastic	SOT146
TDA9800T	20	mini-pack	plastic	SOT163A

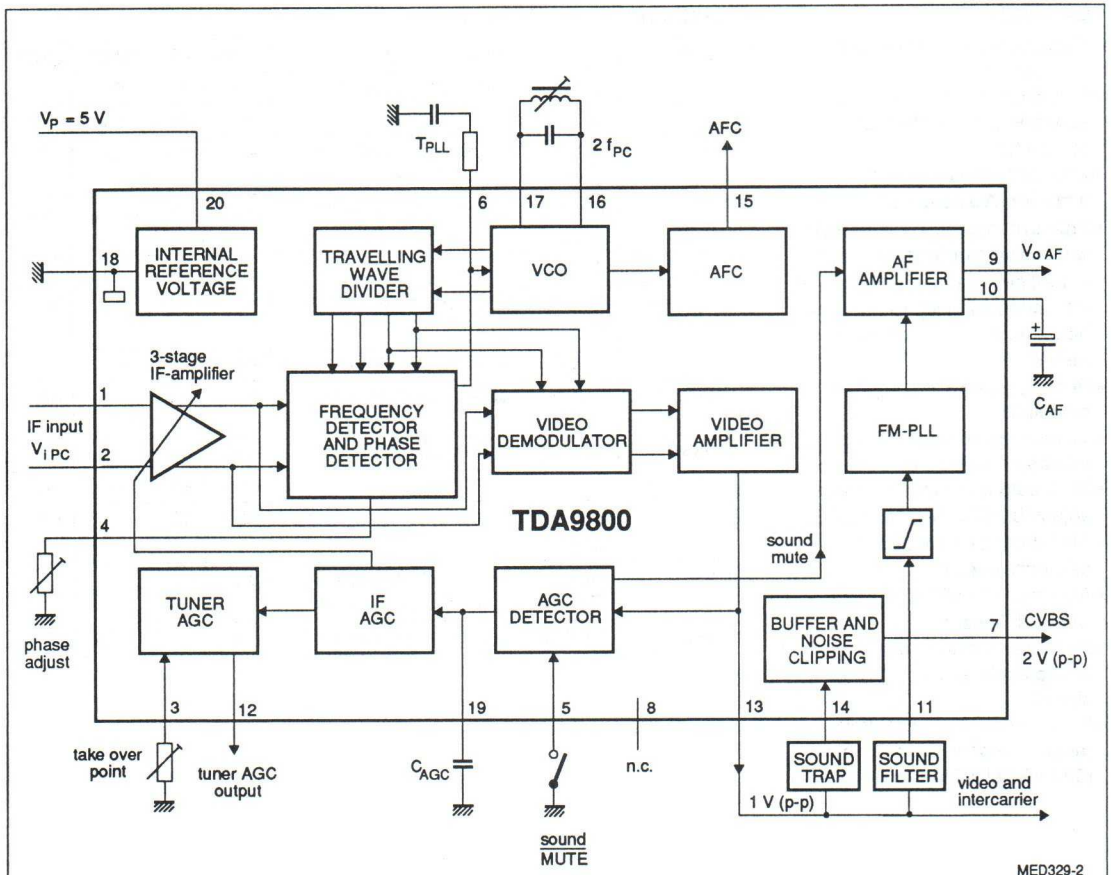


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ϕADJ	4	phase detector adjust
MUTE	5	sound mute switch
T_{PLL}	6	PLL time constant of phase detector
$V_{o\,CVBS}$	7	CVBS (positive) output signal
n.c.	8	not connected
$V_{o\,AF}$	9	audio frequency output signal
C_{AF}	10	decoupling capacitor of audio frequency amplifier
$V_{i\,IC}$	11	sound intercarrier input signal
TAGC	12	tuner AGC output
$V_{o\,VID}$	13	video and sound intercarrier output signal
$V_{i\,VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor
V_P	20	positive supply voltage

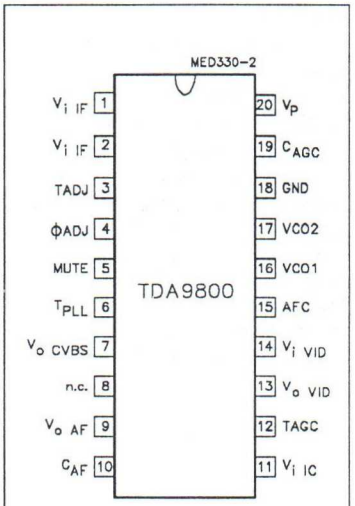


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. Since the TDA9800 is suitable for negative modulation only the peak-sync level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. During acquisition the frequency detector produces a DC current which is proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. Via the loop filter the DC current of either frequency detector or phase detector is converted into a DC voltage, which controls the VCO frequency.
The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.
The VCO signal is divided-by-two in a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13). The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters.
The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

Sound demodulation

The FM sound intercarrier signal is fed to pin 11 and through a limiter amplifier before it is demodulated. This achieves high sensitivity and high AM suppression. The limiter amplifier consists of seven internal AC-coupled stages, minimizing the DC offset.
The FM-PLL demodulator consists of an RC-oscillator, loop filter and phase detector. The oscillator frequency is locked on the FM intercarrier signal from the limiter amplifier. As a result of this locking, the RC-oscillator is frequency-modulated.

The modulating signal voltage (AF signal) is used to control the oscillator frequency. By this, the FM-PLL operates as an FM demodulator.
The audio frequency amplifier with internal feedback is designed for high gain and high common mode rejection. The low-level AF signal output from the FM-PLL demodulator is amplified and buffered in a low-ohmic audio signal output stage (pin 9). An external decoupling capacitor on pin 10 removes the DC voltage from the audio amplifier input.
By using the sound mute switch (pin 5) the AF amplifier is set to mute state.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	0	8.8	V
	SOT163A at +100 °C	0	5.5	V
V_I	voltage on pins 1, 2, 7, 11, 13, 14, 15 and 19	0	V_P	V
$t_{s\ max}$	short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes to the Limiting Values

1. Supply current I_P = 69 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	73 K/W
	SOT163A	85 K/W

CHARACTERISTICS

The following characteristics apply for V_P = 5 V; T_{amb} = +25 °C; see Table 1 for input frequencies and picture to sound ratios; V_{iIF} = 10 mV RMS value (sync level); video modulation DSB; residual carrier: 10%; video signal in accordance with CCIR line 17 or NTC-7 Composite; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 20)	note 1	4.5	5	8.8	V
I_P	supply current		51	60	69	mA
Vision IF input (pins 1 and 2)						
V_i	input sensitivity (RMS value) at 38.9 MHz and 45.75 MHz	–1 dB video at output	–	50	90	µV
	input sensitivity (RMS value) at 58.75 MHz		–	60	100	µV
	maximum input signal (RMS value) at 38.9 MHz and 45.75 MHz	+1 dB video at output	70	150	–	mV
	maximum input signal (RMS value) at 58.75 MHz		80	160	–	mV
$\Delta V_{o\,int.}$	internal IF amplitude difference between picture and sound carrier	within AGC range; B/G: Δf = 5.5 MHz; M/N: Δf = 4.5 MHz	–	0.7	1	dB
G_{IF}	IF gain control	see Fig.4				
		38.9 MHz and 45.75 MHz	64	70	–	dB
		58.75 MHz	62	68	–	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance (differential)		1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{1,2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		note 2				
f_{VCO}	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	I_{AFC} = 0; note 3	–	–	±20	ppm/K
$V_{o\,ref}$	oscillator swing at pins 16 and 17 (RMS value)	f_{PC} = 38.9 MHz	–	120	–	mV
		f_{PC} = 45.75 MHz	–	100	–	mV
		f_{PC} = 58.75 MHz	–	80	–	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	BL = 60 kHz; note 4	–	–	30	ms
$V_{i\,IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	maximum IF gain; note 5	–	50	90	µV
	for C/N = 10 dB	note 6	–	100	140	µV
I_{loop}	FPLL loop offset current at pin 6	note 7	–	–	±4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 13)		sound carrier off				
$V_{o\,vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level		1.4	1.5	1.6	V
	zero carrier level		–	2.6	–	V
	upper video clipping level		$V_P - 1.1$	$V_P - 1.0$	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{o\,FM}$	IF intercarrier level (RMS value)	sound carrier on; note 8	–	170	–	mV
R_{13}	output resistance		–	–	10	Ω
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.0	–	–	mA
B	–3 dB video bandwidth	$C_{13} < 50$ pF; $R_L > 1$ kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	$C_{13} < 50$ pF; $R_L > 1$ kΩ; note 9	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input	pin 14 not connected	1.5	1.8	2.1	V
G_v	voltage gain	note 10	6	7	7.5	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	3.9	4.0	–	V
		lower video clipping	–	1.0	1.1	V
		sync level	–	1.35	–	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.4	–	–	mA
B	–3 dB video bandwidth	$C_7 < 20$ pF; $R_L > 1$ kΩ	8	11	–	MHz
Measurements from IF input to CVBS output (pin 7)		330 Ω between pins 13 and 14, sound carrier off				
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	note 11	–	–	1	%
ΔG	differential gain	CCIR line 330 or NTC-7 Composite	–	2	5	%
Δφ	differential phase		–	1	3	deg
B	–3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 12	56	59	–	dB
$\alpha_{0.92/1.1}$	intermodulation at 'blue'	f = 0.92 or 1.1 MHz; see Fig.6 and note 13	56	62	–	dB
	intermodulation at 'yellow'		58	64	–	dB
$\alpha_{2.76/3.3}$	intermodulation at 'blue'	f = 2.76 or 3.3 MHz; see Fig.6 and note 13	56	62	–	dB
	intermodulation at 'yellow'		57	63	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	note 9	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal		–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		–	50	100	ms
I_{19}	charging current	note 11	0.85	1.1	1.35	mA
	discharging current		17	22	27	μA
V_{19}	AGC voltage	maximum gain	0	see Fig.4	–	V
		minimum gain	–	see Fig.4	$V_P - 0.7$	V
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	I_{12} = 0.4 mA	–	0.02	0.06	dB/K
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	μA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 14				
S	control steepness $\Delta I_{15}/\Delta f$	note 15				
		38.9 MHz	–0.6	–0.72	–0.84	μA/kHz
		45.75 MHz	–0.45	–0.6	–0.75	μA/kHz
		58.75 MHz	–0.38	–0.5	–0.62	μA/kHz
Δf_{IF}	frequency variation by temperature	I_{AFC} = 0; note 3	–	–	±20	ppm/K
V_{15}	output voltage upper limit	see Fig.8	$V_P - 0.5$	$V_P - 0.3$	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	μA
	output current sink		160	200	240	μA
ΔI_{15}	residual video modulation current (peak-to-peak value)		–	20	30	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound mute switch (pin 5)		note 16				
V_{IL}	input voltage for MUTE-ON		0	–	0.8	V
V_{IH}	input voltage for MUTE-OFF		1.5	–	V_P	V
I_{IL}	LOW level input current	V_5 = 0 V	–	–300	–360	μA
α_{mute}	audio attenuation	V_5 = 0 V	70	80	–	dB
ΔV_5	DC offset voltage at switching (plop)	switching to MUTE-ON	–	100	500	mV
FM sound limiter amplifier (pin 11)		note 17				
$V_{i\ FM}$	input signal (RMS value, pin 11) for S/N = 40 dB for AM suppression α_{AM} = 40 dB	CCIR468-4 see Fig.11 AM: f = 1 kHz; m = 0.3	 – –	 200 1	 300 –	 μV mV
	maximum input signal handling (RMS value)		200	–	–	mV
α_{AM}	AM suppression	see Fig.10; AM: f = 1 kHz; m = 0.3	46	50	–	dB
R_{11}	input resistance		480	600	720	Ω
B	–3 dB IF frequency response of sound IF	lower and upper cut-off frequency	3.5	–	10	MHz
V_{11}	DC voltage		2.3	2.6	2.9	V
FM-PLL sound demodulator and AF output (pin 9)		note 17				
$f_{i\ FM}$	catching range of PLL		4	–	7	MHz
	holding range of PLL		3.5	–	8	MHz
t_{acqu}	acquisition time		–	–	4	μs
$V_{o\ AF}$	AF output signal (RMS value, pin 9)	Δf_{AF} = ±27 kHz; see Fig.11	280	350	420	mV
	maximum output signal handling	THD < 1.5%	0.8	–	–	V
ΔV_o	temperature drift of AF output signal		–	3	7	10^{-3} dB/K
Δf_{AF}	frequency deviation	THD < 1.5%; note 18	–	–	±50	kHz
V_{10}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 19	1.2	–	2.2	V
R_9	output resistance		–	100	–	Ω
R_L	load resistance (pin 9)		2.2	–	–	kΩ
V_9	DC voltage		1.6	2.0	2.4	V
B	–3 dB audio frequency bandwidth		95	120	–	kHz
THD	total harmonic distortion	without ceramic filter	–	0.1	0.5	%
S/N (W)	signal-to-noise ratio, weighted	CCIR468-4; see Fig.11	50	55	–	dB
V_{SC}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
RR	ripple rejection on pin 9	see Fig.9	26	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to audio output (pin 9) 560 Ω between pins 13 and 11; note 20						
S/N (W)	weighted signal-to-noise ratio	27 kHz FM deviation; CCIR468-4; 50 µs (75 µs at standard M) de-emphasis; with offset alignment on pin 4				
	6 kHz sinusoidal waveform	black-to-white	39	46	–	dB
	black picture	sync only	40	48	–	dB
	white picture		39	46	–	dB
	colour bar		39	46	–	dB

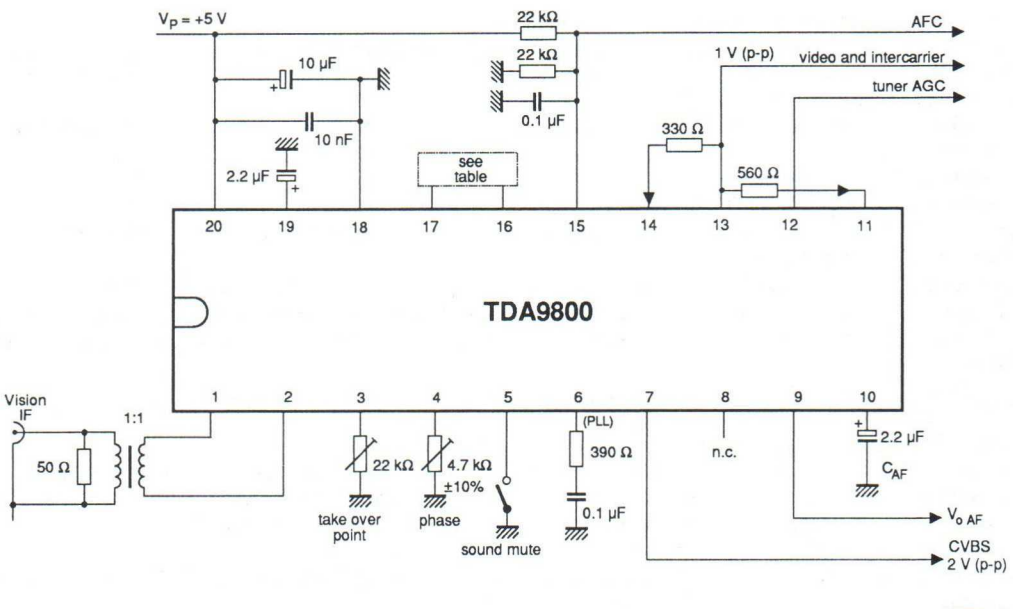
Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2 calculated with grey level and FPLL input signal level). Resonance circuit of VCO: $Q_o > 50$; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF (loop voltage about 2.7 V).
3. Temperature coefficient of external LC-circuit is equal to zero.
4. $V_{i\,IF}$ = 10 mV (RMS value); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
5. $V_{i\,IF}$ signal for nominal video signal.
6. Transformer at IF input (Fig.3). The C/N ratio at IF input for 'lock-in' is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band-limited white noise signal (RMS value); video modulation: white picture.
7. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open-circuit.
8. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula:

   $$20 \log\left(\frac{V_{13\,\text{interc.}\,(p-p)}}{1\,V\,(p-p)}\right) = \frac{V_{iSC}}{V_{iPC}}\,dB + 6.9\,dB \pm 2\,dB$$ with $\frac{V_{iSC}}{V_{iPC}}$ dB = sound to picture carrier ratio at IF input (pins 1 and 2) in dB and ±2 dB = tolerance of intercarrier output amplitude $V_{o\,FM}$.
9. Measurements taken with SAW filter G1962; modulation: VSB, $f_{video} > 0.5$ MHz, loop bandwidth BL = 60 kHz.
10. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
11. The leakage current of the AGC capacitor has to be < 1 µA to avoid larger tilt.
12. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
13. $\alpha_{0.92/1.1}$ = 20 log (V_o at 4.4 (3.58) MHz / V_o at 0.92 (1.1) MHz) + 3.6 dB; $\alpha_{0.92/1.1}$ value at 0.92 (1.1) MHz related to black/white signal.
    $\alpha_{2.76/3.3}$ = 20 log (V_o at 4.4 (3.58) MHz / V_o at 2.76 (3.3) MHz); $\alpha_{2.76/3.3}$ value at 2.76 (3.3) MHz related to colour carrier.
14. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
15. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO ($Q_o > 50$; $C_o = C_{int} + C_{ext}$; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF).
16. No mute state is also valid for pin not connected.
17. Input level for second IF from an external generator with 50 Ω source impedance, AC coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio reference. A VIF/SIF input signal is not permitted. Pin 19 has to be connected to positive supply voltage. S/N and THD measurements are taken at 50 µs (75 µs at standard M) de-emphasis.
18. To allow higher frequency deviation, the resistor R_x on pin 10 (see Fig.12) has to be increased to a value which does not exceed the AF output signal of nominally 0.35 V for THD = 0.1% (R_x = 4.7 kΩ provides –6 dB amplification).
19. The leakage current of the 2.2 µF capacitor is < 100 nA.
20. For all S/N measurements the used vision IF modulator has to meet the following specification:
    - Incidental phase modulation for black-to-white jump less than 0.5 degree.

Table 1 Input frequencies and carrier ratios.

		B/G STANDARD	M/N STANDARD	M STANDARD	UNIT
picture carrier	f_{PC}	38.9	45.75	58.75	MHz
sound carrier	f_{SC}	33.4	41.25	54.25	MHz
picture to sound carrier ratio	SC	13	7	7	dB



MED331-2

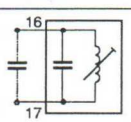
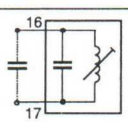
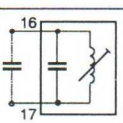
PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	 C(VCO) C L 8.5 pF 8.2 pF 251 nH	 C(VCO) C L 8.5 pF 10 pF 163 nH	 C(VCO) C L 8.5 pF 12 pF 90 nH
e.g. TOKO coil Philips ceramic capacitor	5KM 369SNS-2010Z 222263251828	5KMC V369SCS-2370Z (inside of coil)	MC139 NE545SNAS100108 12 pF SMD size = 0805

Fig.3 Test circuit.

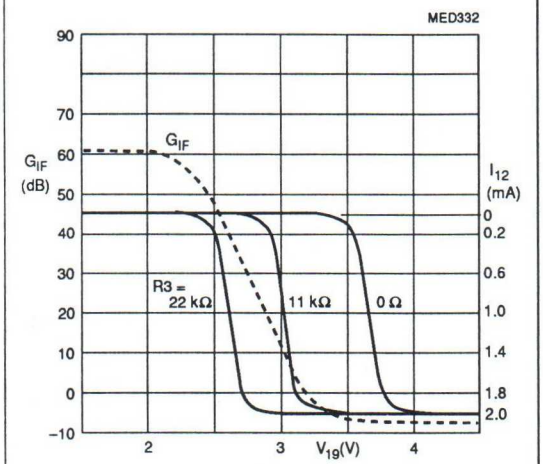


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

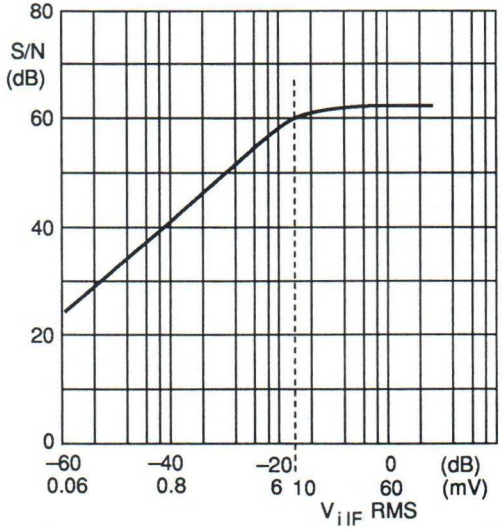
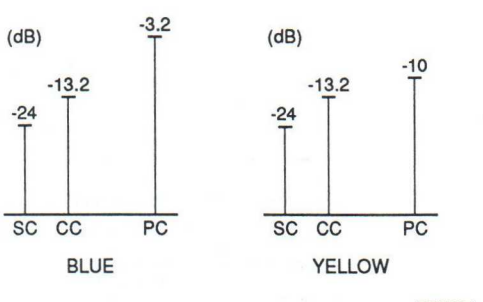


Fig.5 Typical signal-to-noise ratio as a function of IF input signal.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

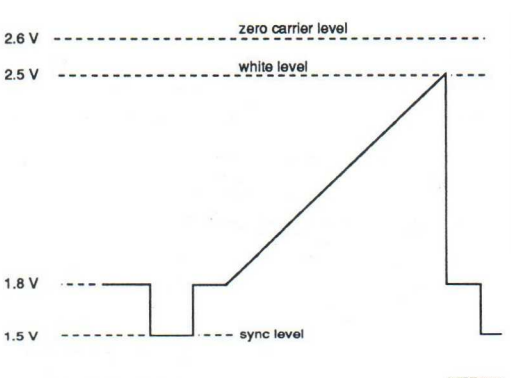


Fig.7 Video signal levels on output pin 13.

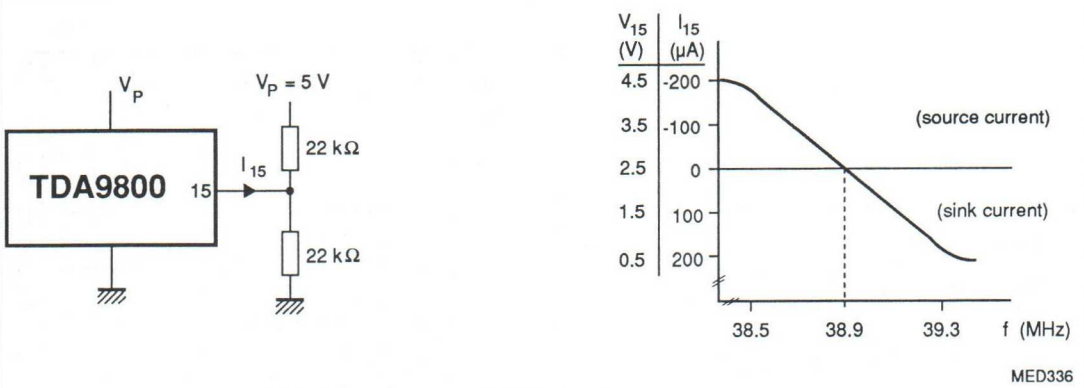


Fig.8 Measurement conditions and typical AFC characteristic.

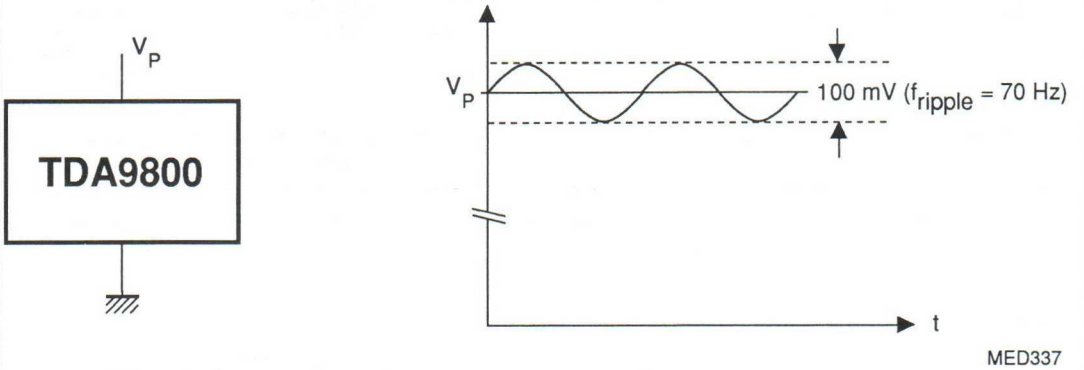


Fig.9 Ripple rejection condition.

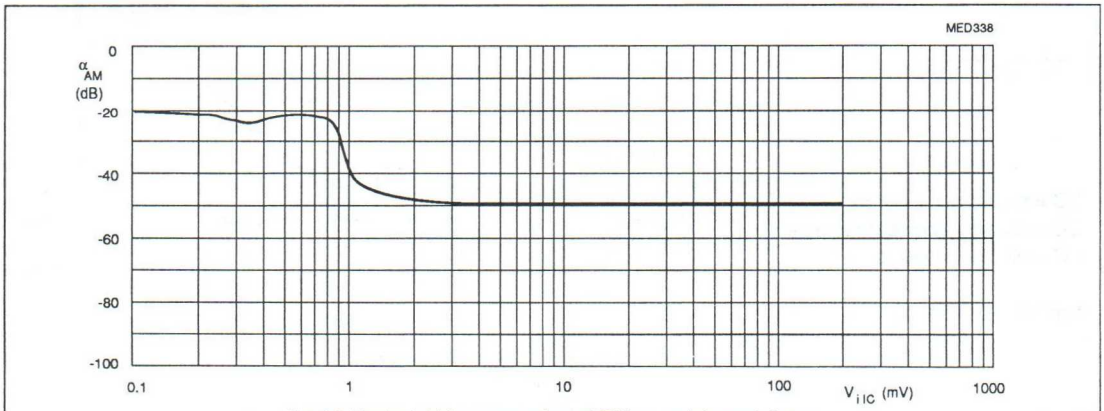


Fig.10 Typical AM suppression of FM sound demodulator.

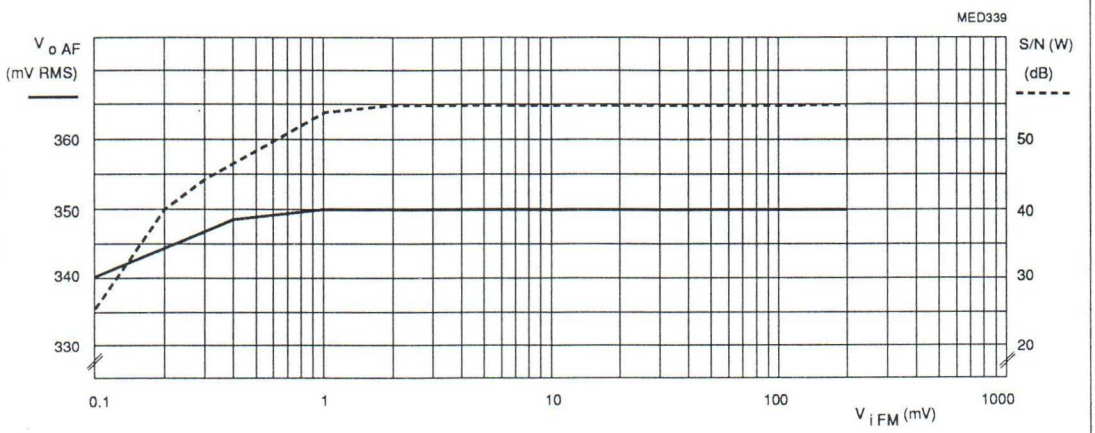
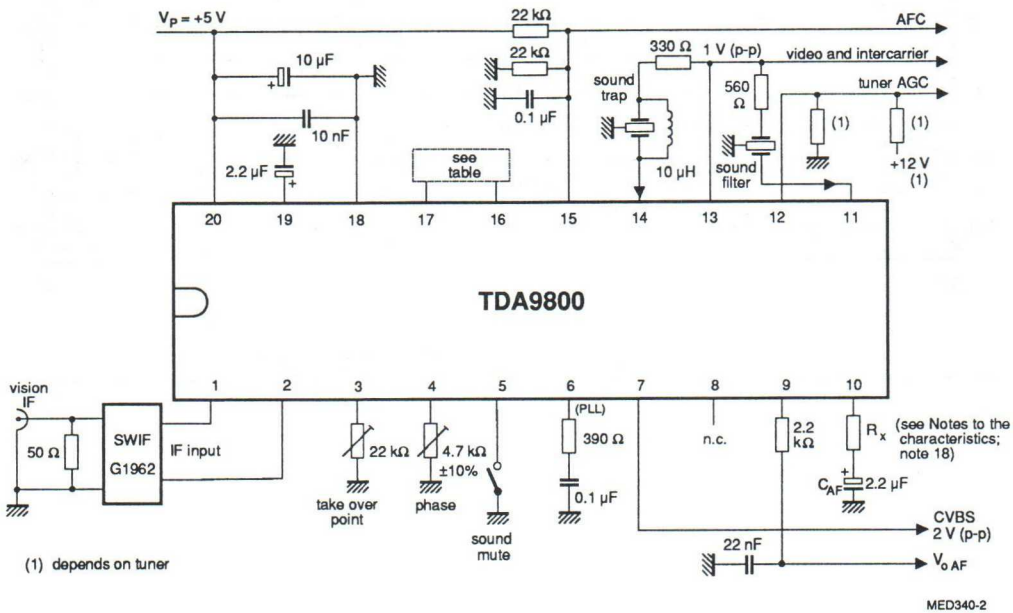


Fig.11 Typical AF output signal and signal-to-noise ratio.



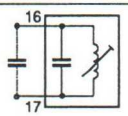
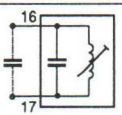
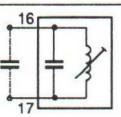
PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	 C(VCO) C L 8.5 pF 8.2 pF 251 nH	 C(VCO) C L 8.5 pF 10 pF 163 nH	 C(VCO) C L 8.5 pF 12 pF 90 nH
e.g. TOKO coil Philips ceramic capacitor	5KM 369SNS-2010Z 222263251828	5KMC V369SCS-2370Z (inside of coil)	MC139 NE545SNAS100108 12 pF SMD size = 0805

Fig.12 Application circuit.

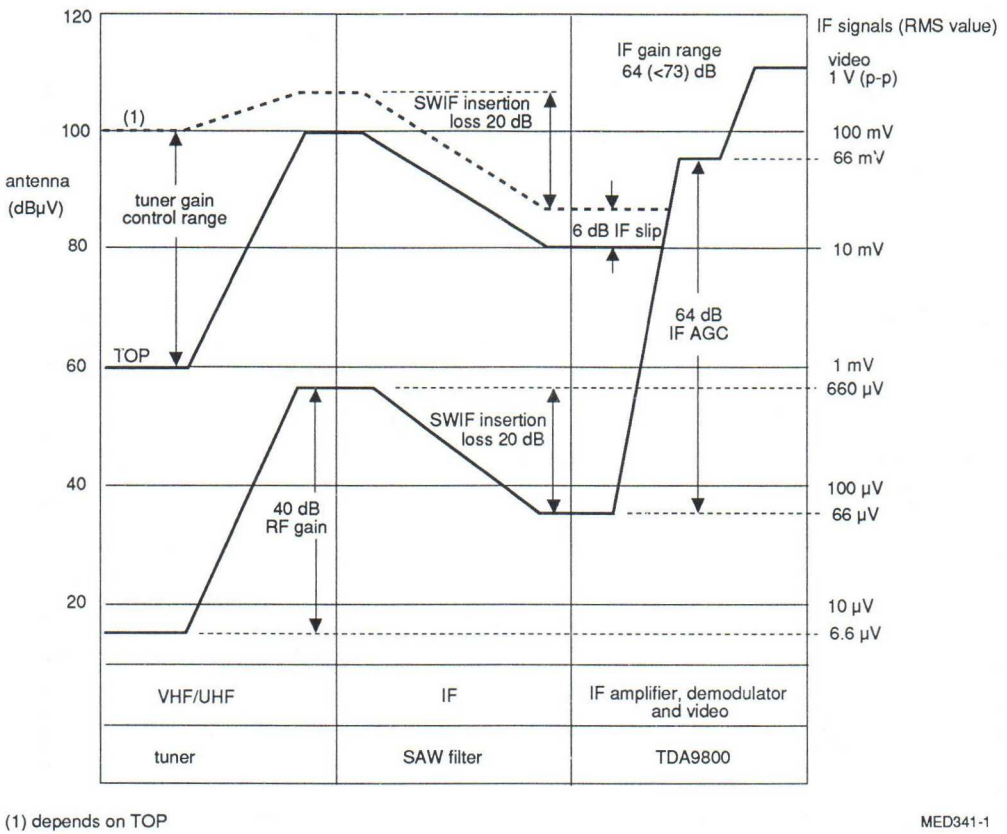


Fig.13 Front end level diagram.

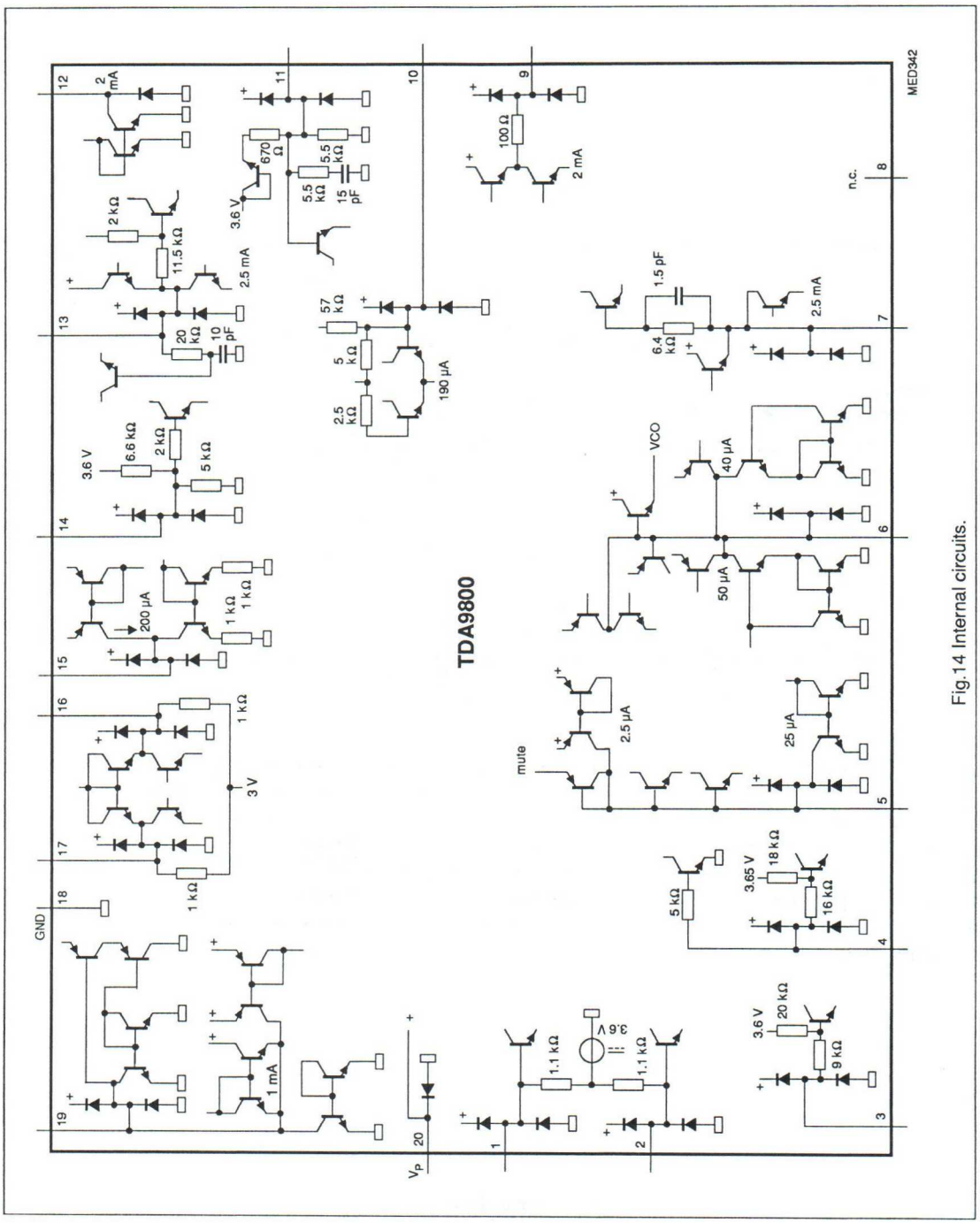


Fig.14 Internal circuits.

Multistandard VIF-PLL demodulator and FM-PLL detector

TDA9802

FEATURES

- Suitable for negative and positive vision modulation
- Gain controlled 3-stage IF amplifier; suitable for VIF frequencies up to 60 MHz
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation, e.g. B/G standard
- Peak white AGC for positive modulation, e.g. L standard
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Alignment-free FM-PLL detector with high linearity
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (300 mW at +5 V supply voltage)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	51	60	69	mA
$V_{i\,IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control range	64	70	73	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{1,1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{3,3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{o\,AF}$	maximum AF output signal for THD < 1.5% (RMS value, pin 9)	0.8	–	–	V
T_{amb}	operating ambient temperature range	0	–	+70	°C

GENERAL DESCRIPTION

The TDA9802 is a monolithic integrated circuit for vision and sound IF signal processing in multistandard TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9802	20	DIL	plastic	SOT146
TDA9802T	20	mini-pack	plastic	SOT163A

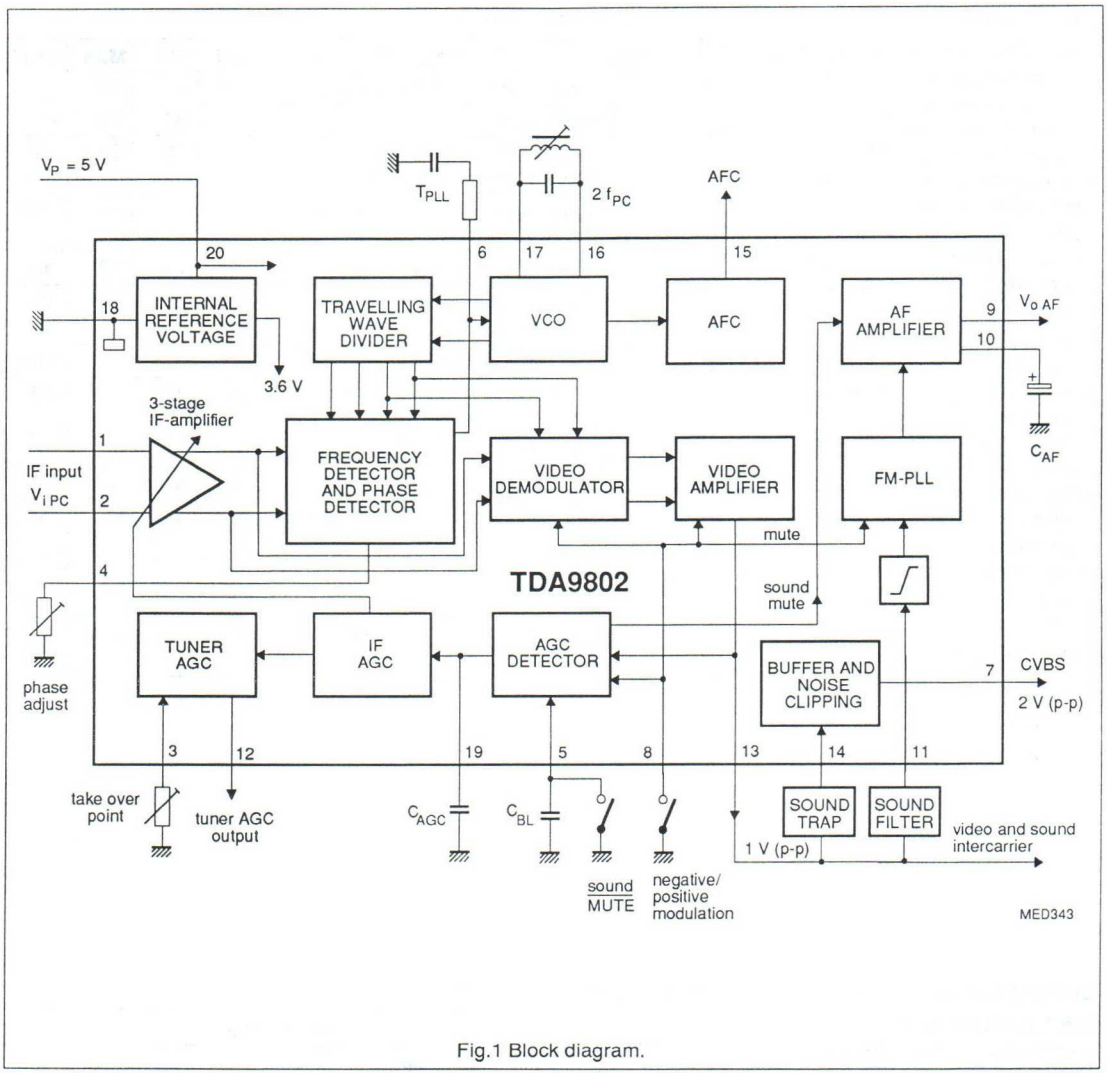


Fig.1 Block diagram.

Multistandard VIF-PLL demodulator and FM-PLL detector

TDA9802

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ϕADJ	4	phase detector adjust
C_{BL}	5	black level capacitor, mute switch input
T_{PLL}	6	PLL time constant of phase detector
$V_{o\ CVBS}$	7	CVBS (positive) output signal
STD	8	standard switch (negative = HIGH, positive = LOW)
$V_{o\ AF}$	9	audio frequency output signal
C_{AF}	10	decoupling capacitor of audio frequency amplifier
$V_{i\ IC}$	11	sound intercarrier input signal
TAGC	12	tuner AGC output
$V_{o\ VID}$	13	video and sound intercarrier output signal
$V_{i\ VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor
V_P	20	positive supply voltage

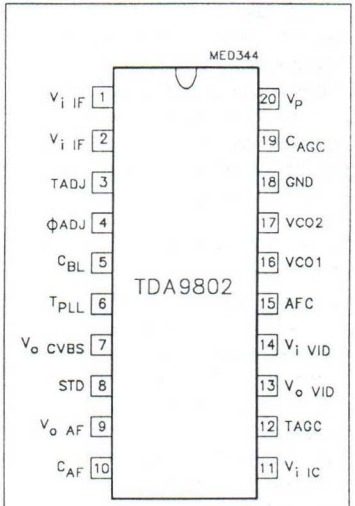


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. For negative modulation the peak-sync level is detected, for positive modulation the peak white level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. The standard is switched by the voltage on pin 8. To reduce the response time for positive modulation (which needs a very long time constant) a black level detector (C_{BL}) increases the AGC capacitor discharge current for low-level video signals.

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. The frequency detector is operational before lock-in. A DC current is generated which is proportional to the frequency difference between the input frequency and the VCO frequency. After lock-in, the frequency detector and the phase detector generate a DC current proportional to the phase difference between VCO and input signals. The control signal for the VCO is provided by the phase detector.

The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics. The polarity of the video signal is switched in the demodulator stage according to the TV standard.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO

frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.
The VCO signal is divided-by-two in a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. Dependent on transmission standard, a level shifter provides the same sync level for positive as for negative modulation. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13).

The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters.
The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

Sound demodulation

The FM sound intercarrier signal is fed to pin 11 and through a limiter amplifier before it is demodulated. This achieves high sensitivity and high AM suppression. The limiter amplifier consists of seven internal AC-coupled stages, minimizing the DC offset.
The FM-PLL demodulator consists of an RC-oscillator, loop filter and phase detector. The oscillator frequency is locked on the FM intercarrier signal from the limiter amplifier.

As a result of this locking, the RC-oscillator is frequency-modulated. The modulating signal voltage (AF signal) is used to control the oscillator frequency. By this, the FM-PLL operates as an FM demodulator.
The audio frequency amplifier with internal feedback is designed for high gain and high common mode rejection. The low-level AF signal output from the FM-PLL demodulator is amplified and buffered in a low-ohmic audio signal output stage (pin 9). An external decoupling capacitor on pin 10 removes the DC voltage from the audio amplifier input.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	0	8.8	V
	SO163A at +100 °C	0	5.5	V
V_I	voltage on pins 1, 2, 7, 8, 11, 13, 14, 15 and 19	0	V_P	V
$t_{s\,max}$	short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes to the Limiting Values

1. Supply current I_P = 69 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j\text{-}a}$	from junction to ambient in free air	
	SOT146	73 K/W
	SOT163A	85 K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz with V_{PC}/V_{SC} = 13 dB (B/G); V_{iIF} = 10 mV RMS value (sync level at B/G; peak-white level at L); video modulation DSB; residual carrier: B/G = 10%, L = 3%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 20)	see note 1	4.5	5	8.8	V
I_P	supply current		51	60	69	mA
Standard switch input (pin 8)						
V_{IH}	input voltage for negative modulation	see note 2	1.5	–	V_P	V
V_{IL}	input voltage for positive modulation		0	–	0.8	V
I_{IL}	LOW level input current	V_8 = 0 V	–	–300	–360	µA
Vision IF input (pins 1 and 2)		B/G standard				
V_i	input signal sensitivity (RMS value)	–1 dB video at output	–	50	90	µV
	maximum input signal (RMS value)	+1 dB video at output	70	150	–	mV
ΔV_i	IF amplitude difference between picture and sound carrier	within AGC range	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4	64	70	73	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance		1.7	2.2	2.7	kΩ
C_i	input capacitance		1.2	1.7	2.5	pF
$V_{1,2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		see note 3				
f_{VCO}	maximum oscillator frequency for carrier regeneration	f = $2f_{PC}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	see note 4; ΔT = 0 to +70 °C	–	–	±1300	10^{-6}
$V_{o\ ref}$	oscillator swing at pins 16 and 17 (RMS value)		tbn	120	tbn	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	see note 5; BL = 60 kHz	–	–	30	ms
$V_{i\ IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	see note 6; maximum IF gain	–	70	100	µV
	for C/N = 10 dB	see note 7	–	100	140	µV
I_{loop}	FPLL loop offset current at pin 6	see note 8	–	–	±4.5	µA
Composite video amplifier (pin 13)		sound carrier off				
$V_{o\ vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level	B/G and L	1.4	1.5	1.6	V
	zero carrier level	B/G	2.5	2.6	2.7	V
		L	1.37	1.47	1.57	V
	upper video clipping level		V_P – 1.1	V_P – 1.0	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{o\ FM}$	IF intercarrier level (RMS value)	sound carrier on; see note 9	tbn	140	tbn	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{13}	output resistance		–	–	10	Ω
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.0	tbn	–	mA
B	–3 dB video bandwidth	$C_{13} < 50$ pF; $R_L > 1$ kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	see note 10; $C_{13} < 50$ pF; $R_L > 1$ kΩ	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input	pin 14 not connected	1.5	1.8	2.1	V
G_v	voltage gain	see note 11	6	7	7.5	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	tbn	4.0	–	V
		lower video clipping	–	1.0	tbn	V
		sync level	1.25	1.35	1.45	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.4	tbn	–	mA
B	–3 dB video bandwidth	$C_7 < 20$ pF; $R_L > 1$ kΩ	8	11	–	MHz
Measurements from IF input to CVBS output (pin 7)		330 Ω between pins 13 and 14, sound carrier off				
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	B/G standard; see note 12	–	–	1	%
	vertical tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; see note 12	–	–	1.5	%
ΔG	differential gain		–	2	5	%
$\Delta\varphi$	differential phase		–	1	3	deg
B	–3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 13	56	59	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 1.1 MHz	56	62	–	dB
	intermodulation at 'yellow'		58	64	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 3.3 MHz	56	62	–	dB
	intermodulation at 'yellow'		57	63	–	dB
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	see note 10	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal	B/G and L	–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal	B/G	–	50	100	ms
		L	–	100	150	ms
I_{19}	charging current	B/G and L; see note 12	0.85	1.1	1.35	mA
	additional charging current	L in case of missing VITS pulses and no white video content	2.0	2.7	3.5	µA
	discharging current	B/G	17	22	27	µA
		normal mode L	0.24	0.33	0.42	µA
		fast mode L	31	44	57	µA
V_{19}	AGC voltage	see Fig.4				
		maximum gain	0	tbn	–	V
		minimum gain	–	tbn	$V_P - 0.7$	V
V_{13}	threshold voltage level	see Fig.7				
	for additional charging current	L	1.9	1.95	2.0	V
	for fast L mode	L	1.6	1.65	1.7	V
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	ΔT = 0 to +50 °C	–	1	3	dB
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	µA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 15				
S	control steepness $\Delta I_{15}/\Delta f$	see note 16	0.6	0.72	0.84	µA/kHz
Δf_{IF}	frequency variation by temperature	ΔT = 0 to +70 °C; see note 4	–	–	±1300	10^{-6}
V_{15}	output voltage upper limit	see Fig.8	$V_P - 0.5$	$V_P - 0.3$	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	µA
	output current sink		160	200	240	µA
ΔI_{15}	residual video modulation current (peak-to-peak value)	B/G and L	–	20	30	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound mute switch (pin 5)		see note 17				
V_{IL}	input voltage for MUTE-ON		0	–	0.8	V
V_{IH}	input voltage for MUTE-OFF		1.5	–	V_P	V
I_{IL}	LOW level input current	V_5 = 0 V	–	–300	–360	μA
α_{mute}	audio attenuation	V_5 = 0 V	70	80	–	dB
ΔV_5	DC offset voltage at switching (plop)	switching to MUTE-ON	–	100	500	mV
FM sound limiter amplifier (pin 11)		FM 5.5 MHz				
$V_{i\,FM}$	input signal (RMS value, pin 11)	CCIR468-4				
	for S/N = 40 dB	see Fig.11	–	200	300	μV
	for AM suppression α_{AM} = 40 dB	AM: f = 1 kHz; m = 0.3	–	1	–	mV
	maximum input signal handling (RMS value)		200	–	–	mV
R_{11}	input resistance		480	600	720	Ω
B	–3 dB IF frequency response of sound IF	lower and upper cut-off frequency	3.5	–	10	MHz
V_{11}	DC voltage		2.3	2.6	2.9	V
FM-PLL sound demodulator and AF output (pin 9)		see note 18				
$f_{i\,FM}$	catching range of PLL		4	–	7	MHz
	holding range of PLL		3.5	–	8	MHz
t_{acqu}	acquisition time		–	–	4	μs
Δf_{AF}	frequency deviation	THD < 1.5%; see note 19	–	–	±50	kHz
V_{10}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; see note 20	1.2	–	2.2	V
$V_{o\,AF}$	AF output signal (RMS value, pin 9)	Δf_{AF} = ±27 kHz; see Fig.11	280	350	420	mV
	maximum output signal handling	THD < 1.5%	0.8	–	–	V
ΔV_o	temperature drift of AF output signal	ΔT = 0 to +70 °C	–	0.2	0.5	dB
R_9	output resistance		–	100	–	Ω
R_L	load resistance (pin 9)		2.2	–	–	kΩ
V_9	DC voltage		1.6	2.0	2.4	V
B	–3 dB audio frequency bandwidth		95	120	–	kHz
THD	total harmonic distortion		–	0.1	0.5	%
S/N (W)	signal-to-noise ratio, weighted	CCIR468-4; see Fig.11	50	55	–	dB
V_{SC}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
α_{AM}	AM suppression	see Fig.10; AM: f = 1 kHz; m = 0.3	46	50	–	dB
RR	ripple rejection on pin 9	see Fig.9	26	30	–	dB
Measurements from IF input to audio output (pin 9)		560 Ω between pins 13 and 11				
S/N (W)	weighted signal-to-noise ratio referred to 54% FM modulation	CCIR468-4; with offset alignment on pin 4				
	6 kHz sinusoidal waveform	black-to-white	39	46	–	dB
	black level	sync only	39	48	–	dB
	white picture		39	46	–	dB

Notes to the characteristics

1. Typical values of video and sound parameters are decreased at V_P = 4.5 V.
2. The input voltage for negative modulation has to be V_8 > 1.5 V, or pin 8 open-circuit.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2 calculated with grey level and FPLL input signal level).
   Resonance circuit of VCO: Q_o > 50; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF (loop voltage about 2.7 V).
4. The oscillator drift is related to the picture carrier frequency (at external temperature-compensated LC-circuit).
5. $V_{i\,IF}$ = 10 mV (RMS value); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ for 0.9 V CVBS (peak-to-peak value) at composite video output pin 13; PLL is still locked.
7. Transformer at IF input (Fig.3). The C/N ratio at IF input for 'lock-in' is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band-limited white noise signal (RMS value); video modulation: white picture.
8. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF-amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open-circuit.
9. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula:

   $$20 \log \left(\frac{V_{13\,\text{interc. (p–p)}}}{1\ \text{V (p–p)}} \right) = \frac{V_{iSC}}{V_{iPC}}\ \text{dB} + 6.9\ \text{dB} \pm 2\ \text{dB}$$

   with

   $\frac{V_{iSC}}{V_{iPC}}$ dB = sound to picture carrier ratio at IF input (pins 1 and 2) in dB

   and

   ±2 dB = tolerance of intercarrier output amplitude $V_{o\,FM}$.
10. Measurements taken with SAW filter G1956; modulation: VSB, f_{video} > 0.5 MHz, loop bandwidth BL = 60 kHz.
11. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
12. The leakage current of the AGC capacitor has to be < 1 µA in B/G mode (< 30 nA in L mode) to avoid larger tilt.
13. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
14. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal
    $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
15. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
16. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO
    (Q_o > 50; $C_o = C_{int} + C_{ext}$; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF).
17. No mute state is also valid for pin not connected. For switching on the L-standard no external load is allowed at pin 5 except capacitor C_{BL}.
18. A 5.5 MHz signal for second IF with 10 mV (RMS value) input level, f_{mod} = 1 kHz and frequency deviation with 54% FM modulation of audio reference is fed directly to pin 11. Audio measurements are taken at 50 µs de-emphasis.
19. To allow higher frequency deviation, the resistor R_x on pin 10 (see Fig.12) has to be increased to a value which does not exceed the AF output signal of nominally 0.35 V for THD = 0.1% (R_x = 4.7 kΩ provides –6 dB amplification).
20. The leakage current of the 2.2 µF capacitor is < 100 nA.

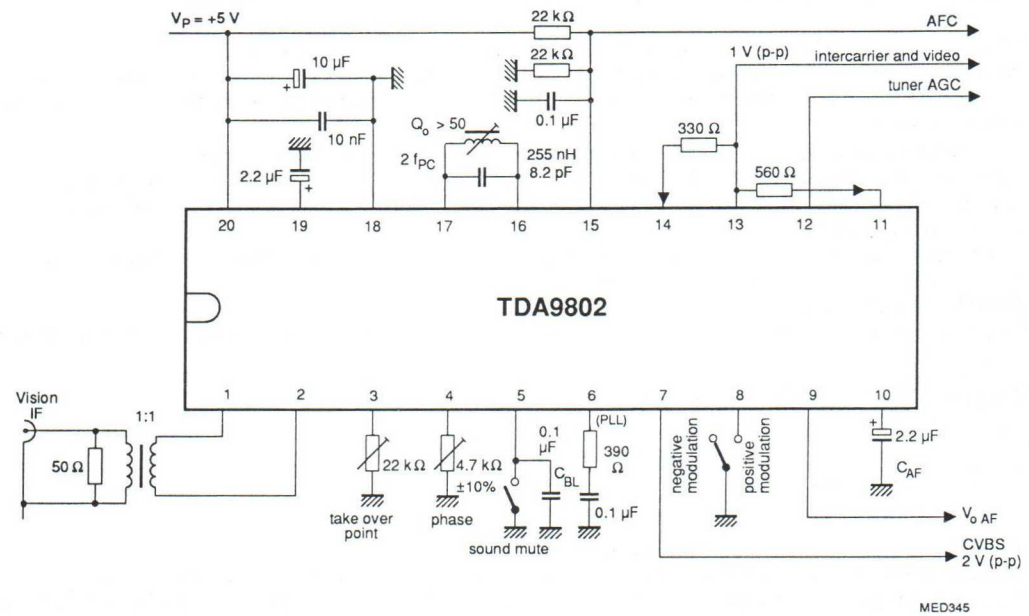


Fig.3 Test circuit.

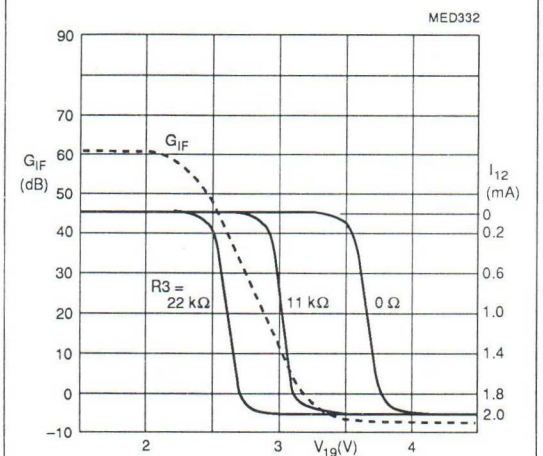


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

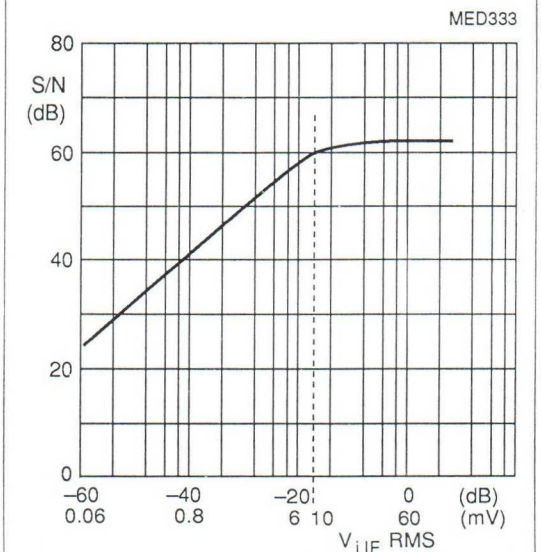
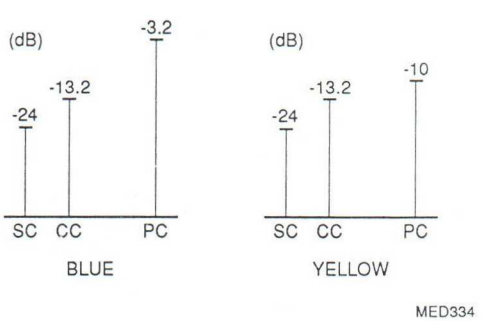


Fig.5 Typical signal-to-noise ratio as a function of IF input signal.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

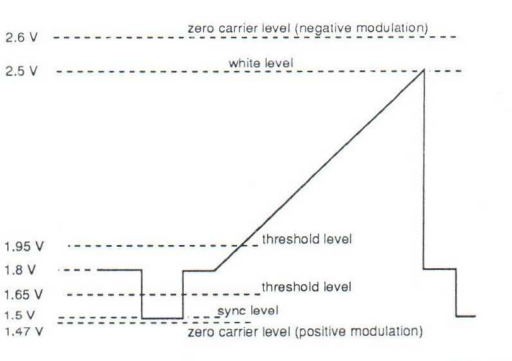


Fig.7 Video signal levels on output pin 13.

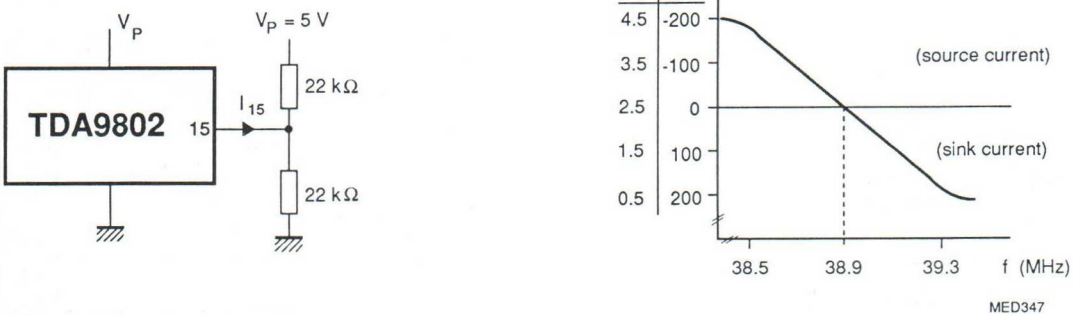


Fig.8 Measurement conditions and typical AFC characteristic.

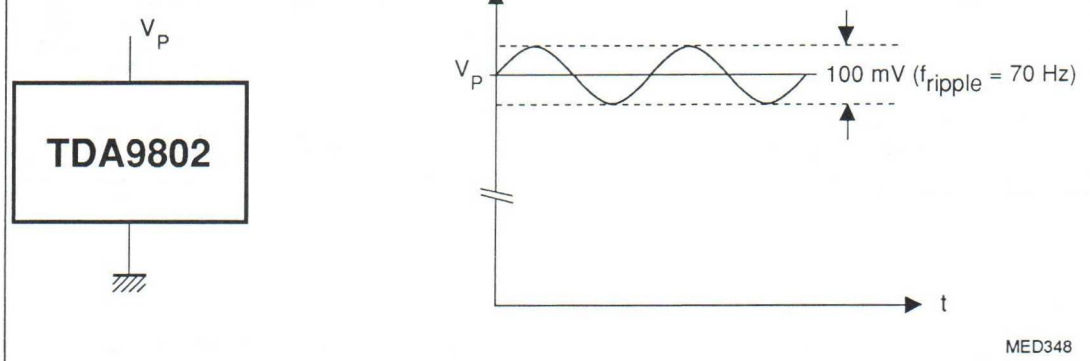


Fig.9 Ripple rejection condition.

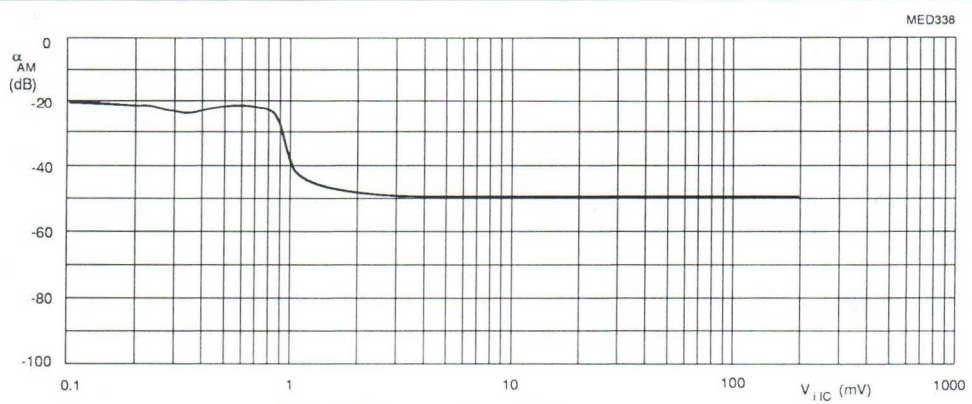


Fig.10 Typical AM suppression of FM sound demodulator.

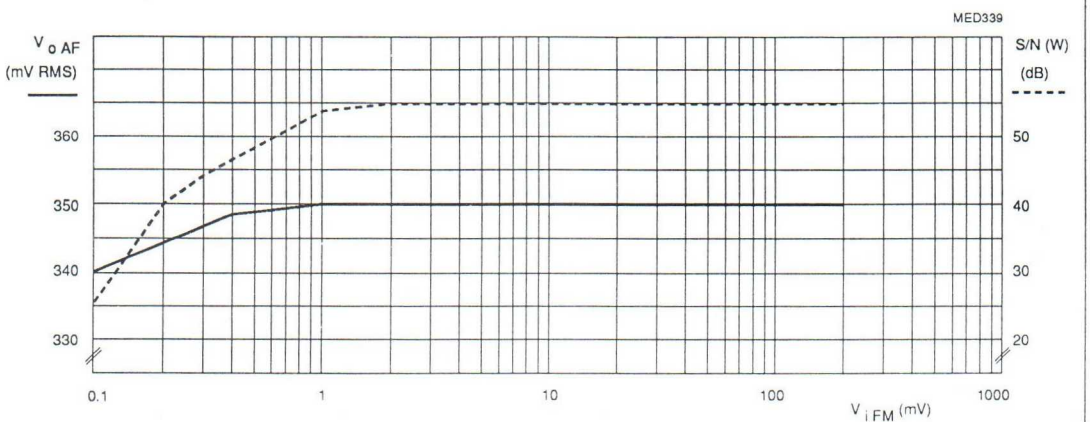


Fig.11 Typical AF output signal and signal-to-noise ratio.

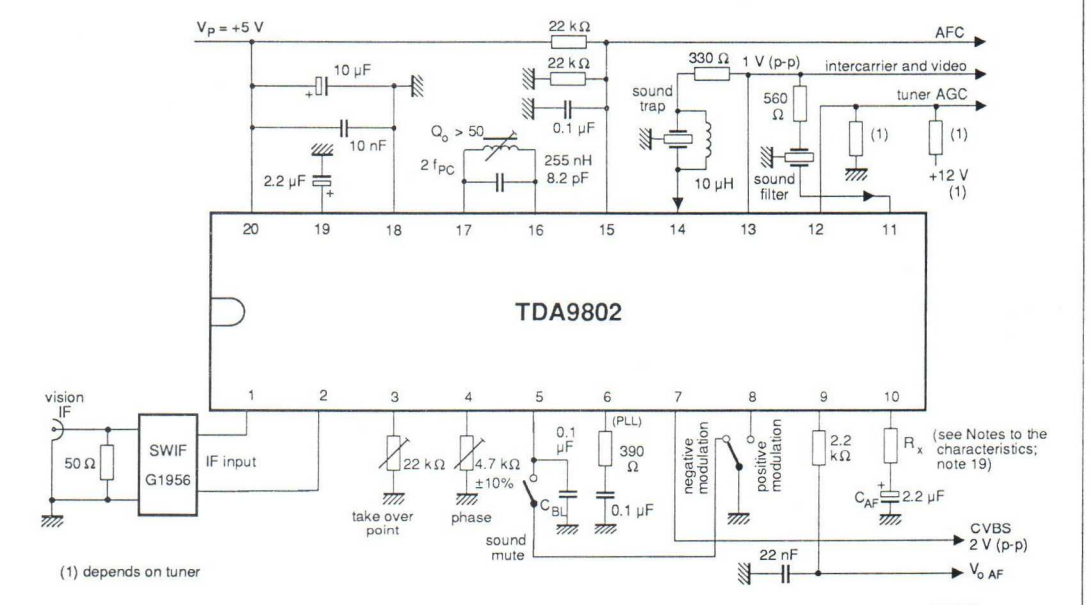


Fig.12 Application circuit.

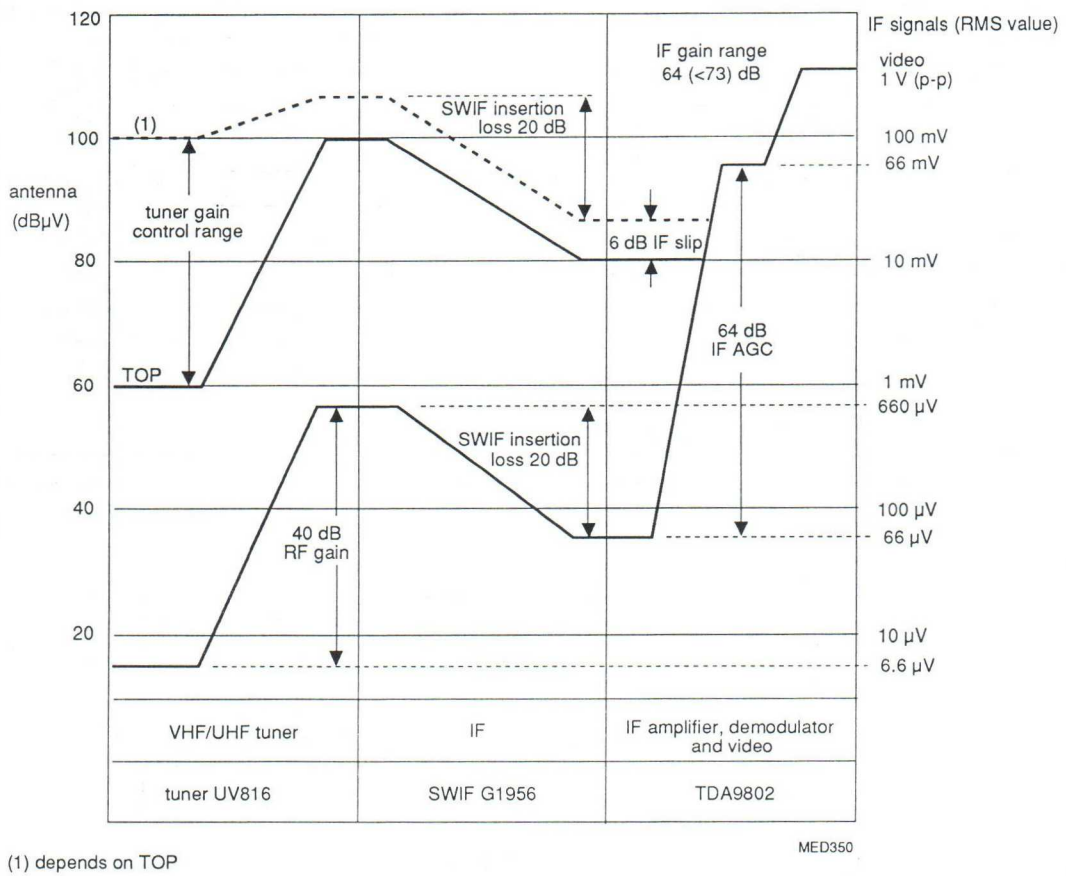


Fig.13 Front end level diagram.

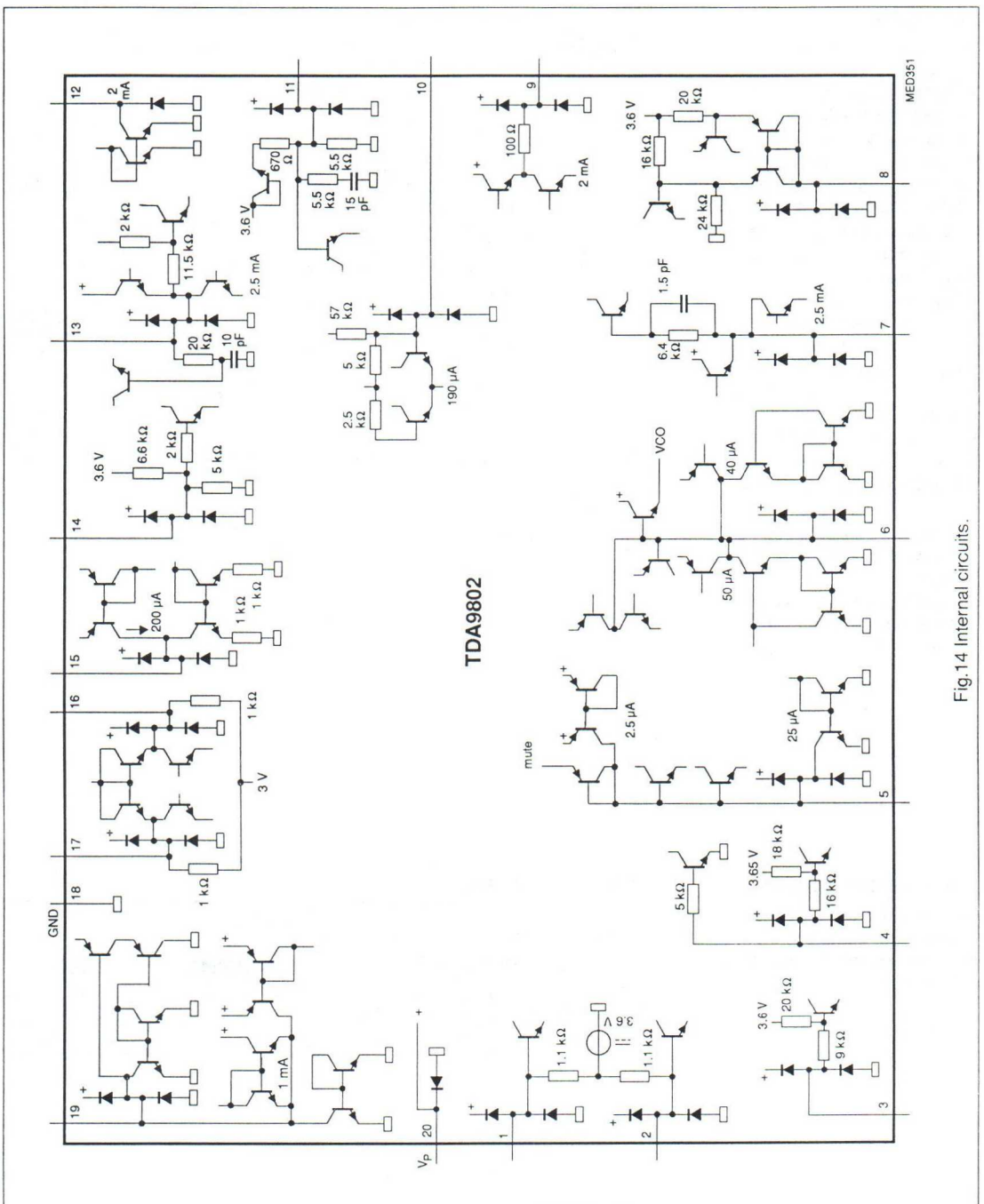


Fig.14 Internal circuits.

Multistandard VIF-PLL demodulator TDA9803

FEATURES

- Suitable for negative and positive vision modulation
- Gain controlled 3-stage IF amplifier; suitable for VIF frequencies up to 60 MHz
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation, e.g. B/G standard
- Peak white AGC for positive modulation, e.g. L standard
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (230 mW at +5 V supply)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	39	46	53	mA
$V_{i\ IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control range	64	70	73	dB
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{1.1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{3.3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
T_{amb}	operating ambient temperature range	0	–	+70	°C

GENERAL DESCRIPTION

The TDA9803 is a monolithic integrated circuit for vision IF signal processing in multistandard TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9803	20	DIL	plastic	SOT146
TDA9803T	20	mini-pack	plastic	SOT163A

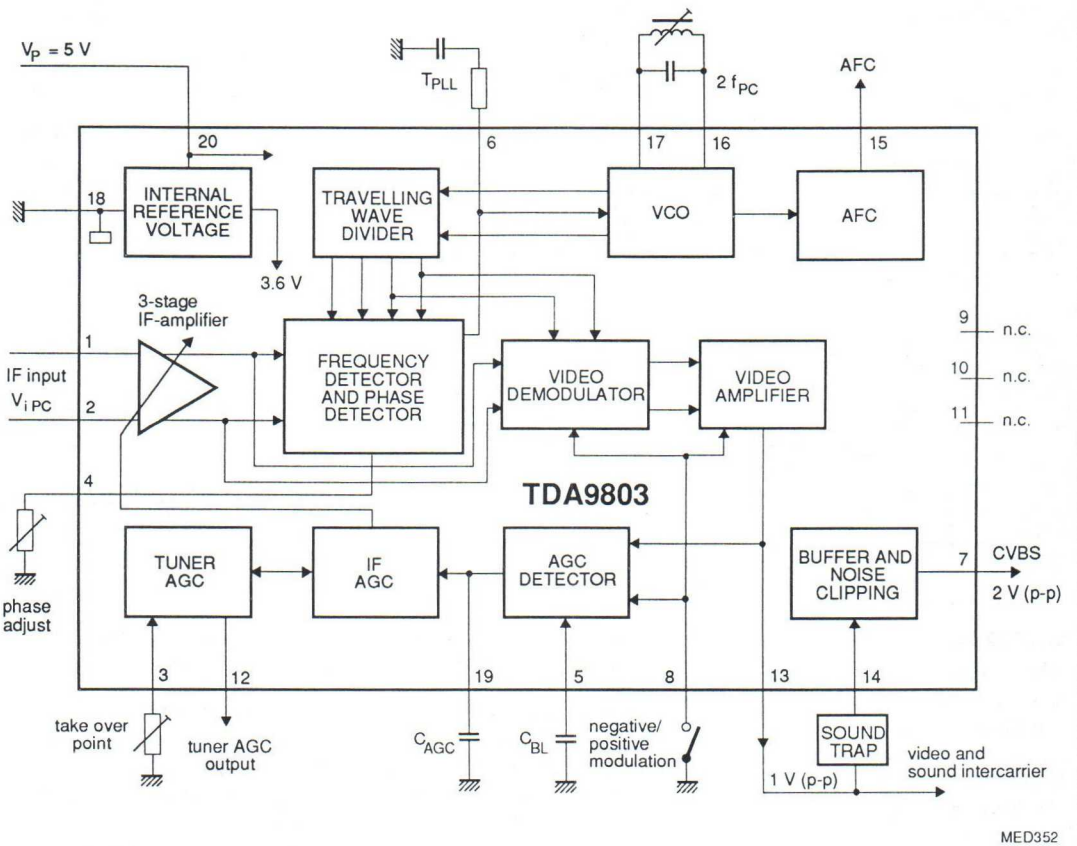


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ϕADJ	4	phase detector adjust
C_{BL}	5	black level capacitor, mute switch input
T_{PLL}	6	PLL time constant of phase detector
$V_{o\ CVBS}$	7	CVBS (positive) output signal
STD	8	standard switch (negative = HIGH, positive = LOW)
n.c.	9	not connected
	10	
	11	
TAGC	12	tuner AGC output
$V_{o\ VID}$	13	video and sound intercarrier output signal
$V_{i\ VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor
V_P	20	positive supply voltage

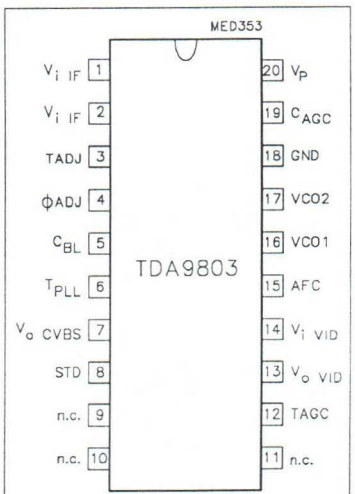


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. For negative modulation the peak-sync level is detected, for positive modulation the peak white level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. The standard is switched by the voltage on pin 8. To reduce the response time for positive modulation (which needs a very long time constant) a black level detector (C_{BL}) increases the AGC capacitor discharge current for low-level video signals.

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. The frequency detector is operational before lock-in. A DC current is generated which is proportional to the frequency difference between the input frequency and the VCO frequency. After lock-in, the frequency detector and the phase detector generate a DC current proportional to the phase difference between VCO and input signals. The control signal for the VCO is provided by the phase detector. The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics. The polarity of the video signal is switched in the demodulator stage according to the TV standard.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO

frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.
The VCO signal is divided-by-two in a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. Dependent on transmission standard, a level shifter provides the same sync level for positive as for negative modulation. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13).

The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters.
The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	0	8.8	V
	SOT163A at +100 °C	0	5.5	V
V_I	voltage on pins 1, 2, 7, 8, 13, 14, 15 and 19	0	V_P	V
$t_{s\ max}$	short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes to the Limiting Values

1. Supply current I_P = 53 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	73 K/W
	SOT163A	85 K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz with V_{PC}/V_{SC} = 13 dB (B/G); V_{iIF} = 10 mV RMS value (sync level at B/G; peak-white level at L); video modulation DSB; residual carrier: B/G = 10%, L = 3%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 20)	see note 1	4.5	5	8.8	V
I_P	supply current		39	46	53	mA
Standard switch (pin 8)						
V_{IH}	input voltage for negative modulation	see note 2	1.5	–	V_P	V
V_{IL}	input voltage for positive modulation		0	–	0.8	V
I_{IL}	LOW level input current	V_8 = 0 V	–	–300	–360	µA
Vision IF input (pins 1 and 2)		B/G standard				
V_i	input signal sensitivity (RMS value)	–1 dB video at output	–	50	90	µV
	maximum input signal (RMS value)	+1 dB video at output	70	150	–	mV
ΔV_i	IF amplitude difference between picture and sound carrier	within AGC range	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4	64	70	73	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance		1.7	2.2	2.7	kΩ
C_i	input capacitance		1.2	1.7	2.5	pF
$V_{1,2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		see note 3				
f_{VCO}	maximum oscillator frequency for carrier regeneration	f = 2f_{PC}	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	see note 4; ΔT = 0 to +70 °C	–	–	±1300	10^{-6}
$V_{o\,ref}$	oscillator swing at pins 16 and 17 (RMS value)		tbn	120	tbn	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	see note 5; BL = 60 kHz	–	–	30	ms
$V_{i\,IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	see note 6; maximum IF gain	–	70	100	µV
	for C/N = 10 dB	see note 7	–	100	140	µV
I_{loop}	FPLL loop offset current at pin 6	see note 8	–	–	±4.5	µA
Composite video amplifier (pin 13)		sound carrier off				
$V_{o\,vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level	B/G and L	1.4	1.5	1.6	V
	zero carrier level	B/G	2.5	2.6	2.7	V
		L	1.37	1.47	1.57	V
	upper video clipping level		V_P – 1.1	V_P – 1.0	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{o\,FM}$	IF intercarrier level (RMS value)	sound carrier on; see note 9	tbn	140	tbn	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{13}	output resistance		–	–	10	Ω
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.0	tbn	–	mA
B	–3 dB video bandwidth	$C_{13} < 50$ pF; $R_L > 1$ kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	see note 10; $C_{13} < 50$ pF; $R_L > 1$ kΩ	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input		1.5	1.8	2.1	V
G_v	voltage gain	see note 11	6	7	7.5	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	tbn	4.0	–	V
		lower video clipping	–	1.0	tbn	V
		sync level	1.25	1.35	1.45	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.4	tbn	–	mA
B	–3 dB video bandwidth	$C_7 < 20$ pF; $R_L > 1$ kΩ	8	11	–	MHz
Measurements from IF input to CVBS output (pin 7) 330 Ω between pins 13 and 14, sound carrier off						
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	B/G standard; see note 12	–	–	1	%
	vertical tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; see note 12	–	–	1.5	%
ΔG	differential gain		–	2	5	%
Δφ	differential phase		–	1	3	deg
B	–3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 13	56	59	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 1.1 MHz	56	62	–	dB
	intermodulation at 'yellow'		58	64	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	f = 3.3 MHz	56	62	–	dB
	intermodulation at 'yellow'		57	63	–	dB
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	see note 10	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal	B/G and L	–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal	B/G	–	50	100	ms
		L	–	100	150	ms
I_{19}	charging current	B/G and L; see note 12	0.85	1.1	1.35	mA
	additional charging current	L in case of missing VITS pulses and no white video content	2.2	2.7	3.2	μA
	discharging current	B/G	17	22	27	μA
		normal mode L	0.24	0.33	0.42	μA
		fast mode L	31	44	57	μA
V_{19}	AGC voltage	see Fig.4				
		maximum gain	0	tbn	–	V
		minimum gain	–	tbn	$V_P - 0.7$	V
V_{13}	threshold voltage level	see Fig.7				
	for additional charging current	L	1.9	1.95	2.0	V
	for fast L mode	L	1.6	1.65	1.7	V
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	ΔT = 0 to +50 °C	–	1	3	dB
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	μA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 15				
S	control steepness $\Delta I_{15}/\Delta f$	see note 16	0.6	0.72	0.84	μA/kHz
Δf_{IF}	frequency variation by temperature	ΔT = 0 to +70 °C; see note 4	–	–	±1300	10^{-6}
V_{15}	output voltage upper limit	see Fig.8	$V_P - 0.5$	$V_P - 0.3$	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	μA
	output current sink		160	200	240	μA
ΔI_{15}	residual video modulation current (peak-to-peak value)	B/G and L	–	20	30	μA

Notes to the characteristics

1. Typical values of video and sound parameters are decreased at $V_P = 4.5$ V.
2. The input voltage for negative modulation has to be $V_8 > 1.5$ V, or pin 8 open-circuit.
3. Loop bandwidth BL = 60 kHz (natural frequency $f_n = 15$ kHz; damping factor d = 2 calculated with grey level and FPLL input signal level).
   Resonance circuit of VCO: $Q_o > 50$; $C_{ext} = 8.2$ pF; $C_{int} \approx 8.5$ pF (loop voltage about 2.7 V).
4. The oscillator drift is related to the picture carrier frequency (at external temperature-compensated LC-circuit).
5. $V_{i\,IF} = 10$ mV (RMS value); $\Delta f = 1$ MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ for 0.9 V CVBS (peak-to-peak value) at composite video output pin 13; PLL is still locked.
7. Transformer at IF input (Fig.3). The C/N ratio at IF input for 'lock-in' is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band-limited white noise signal (RMS value); video modulation: white picture.
8. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF-amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open-circuit.
9. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula:

   $$20 \log \left(\frac{V_{13\,\text{interc. (p–p)}}}{1\ \text{V (p–p)}} \right) = \frac{V_{iSC}}{V_{iPC}}\ \text{dB} + 6.9\ \text{dB} \pm 2\ \text{dB}$$

   with

   $\frac{V_{iSC}}{V_{iPC}}$ dB = sound to picture carrier ratio at IF input (pins 1 and 2) in dB

   and

   ±2 dB = tolerance of intercarrier output amplitude $V_{o\,FM}$.
10. Measurements taken with SAW filter G1956; modulation: VSB, $f_{video} > 0.5$ MHz, loop bandwidth BL = 60 kHz.
11. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
12. The leakage current of the AGC capacitor has to be < 1 µA in B/G mode (< 30 nA in L mode) to avoid larger tilt.
13. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
14. $\alpha_{1.1} = 20 \log (V_o$ at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal
    $\alpha_{3.3} = 20 \log (V_o$ at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
15. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
16. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO
    ($Q_o > 50$; $C_o = C_{int} + C_{ext}$; $C_{ext} = 8.2$ pF; $C_{int} \approx 8.5$ pF).

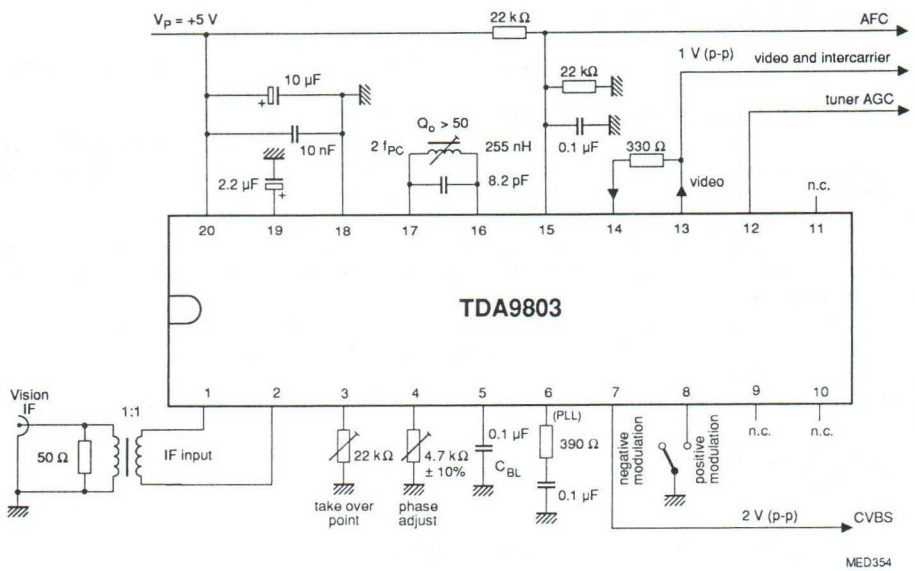


Fig.3 Test circuit.

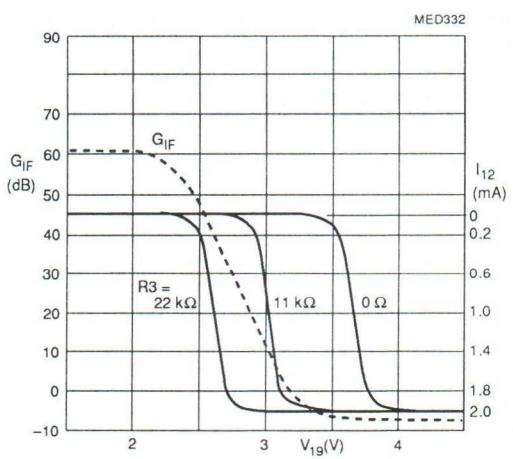


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

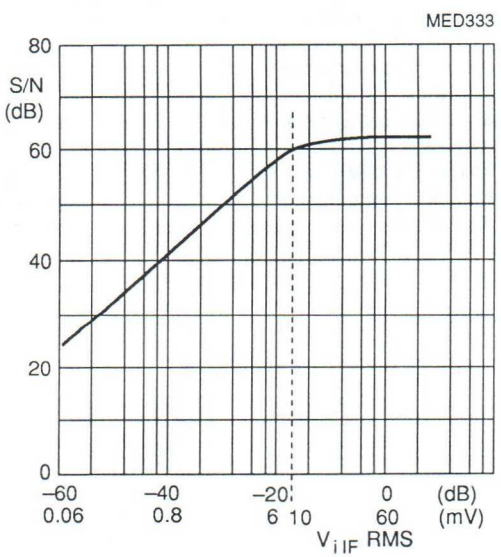
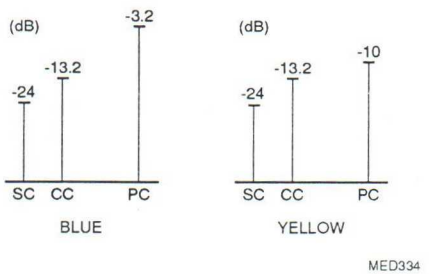


Fig.5 Typical signal-to-noise ratio as a function of the IF input signal.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

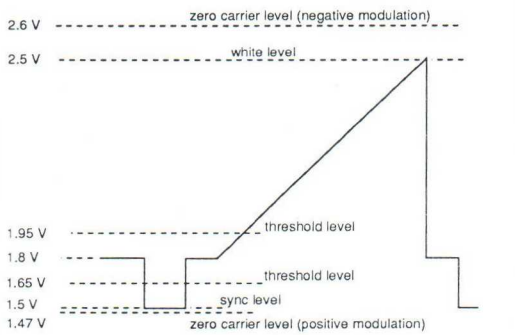
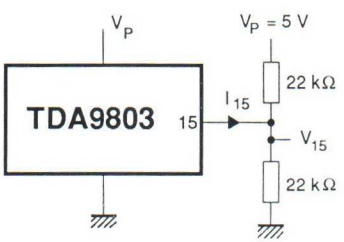


Fig.7 Video signal levels on output pin 13.



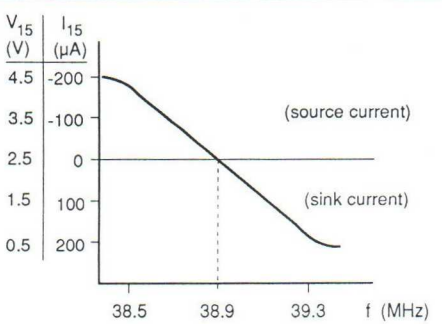
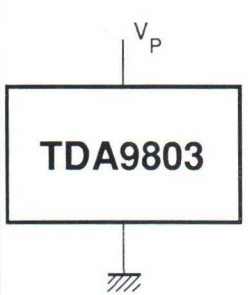


Fig.8 Measurement conditions and typical AFC characteristic.



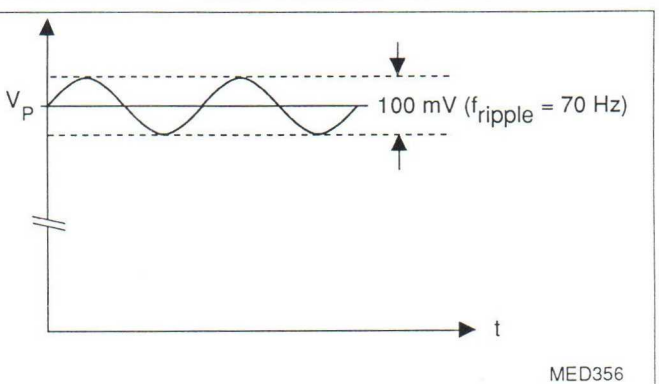


Fig.9 Ripple rejection condition.

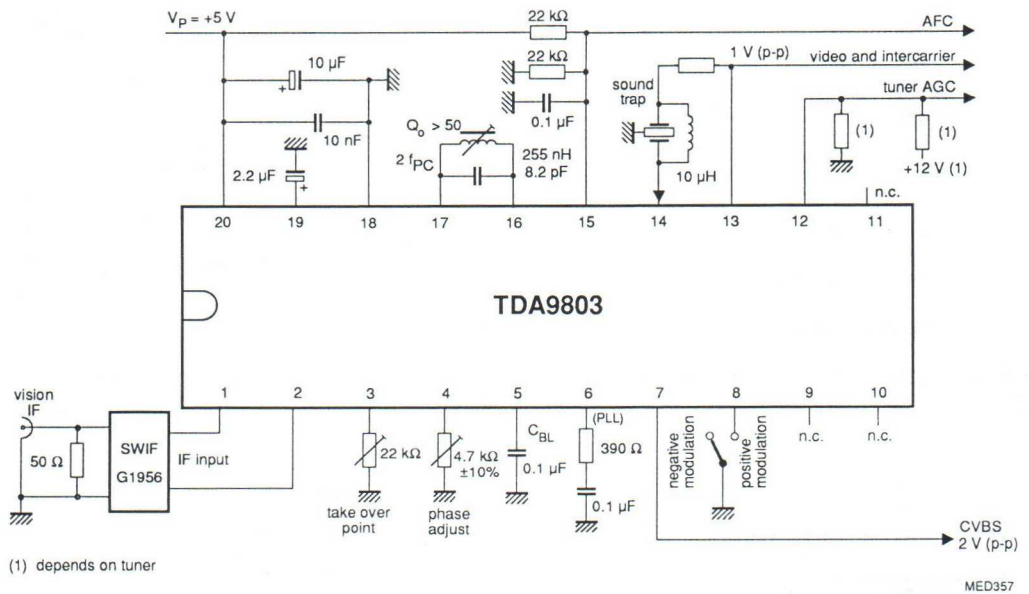


Fig.10 Application circuit.

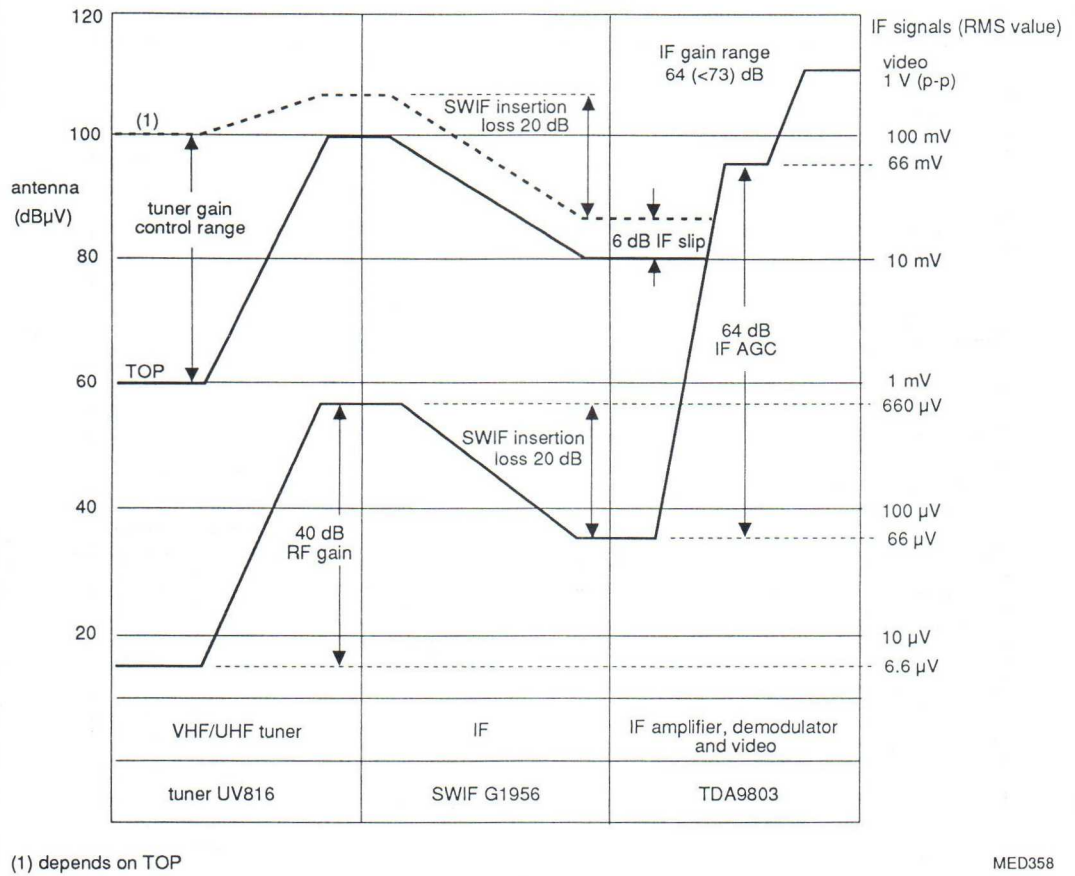


Fig.11 Front end level diagram.

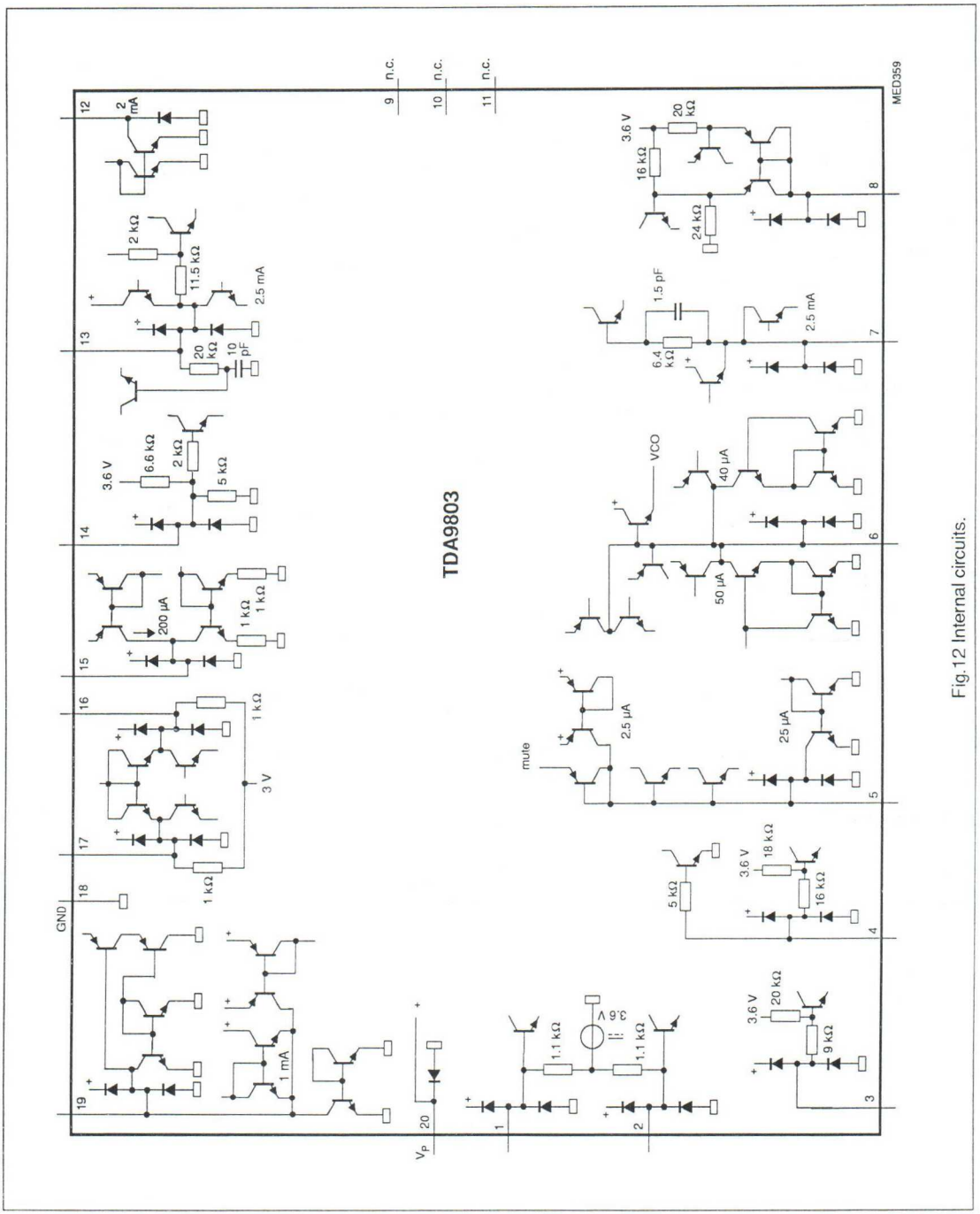


Fig.12 Internal circuits.

VIF-PLL demodulator with internal or external AGC and FM-PLL detector

TDA9804

FEATURES

- Suitable for negative vision modulation controlled by internal or external AGC
- Gain controlled 3-stage IF amplifier; suitable for VIF frequencies up to 60 MHz
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation, e.g. B/G standard
- Voltage controlled external AGC enabled by switching pin
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Alignment-free FM-PLL detector with high linearity
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (300 mW at +5 V supply voltage)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	51	60	69	mA
$V_{i\ IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control range	64	70	73	dB
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{1.1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{3.3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{o\ AF}$	maximum AF output signal for THD < 1.5% (RMS value, pin 9)	0.8	–	–	V
T_{amb}	operating ambient temperature range	0	–	+70	°C

GENERAL DESCRIPTION

The TDA9804 is a monolithic integrated circuit for vision and sound IF signal processing in TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9804	20	DIL	plastic	SOT146

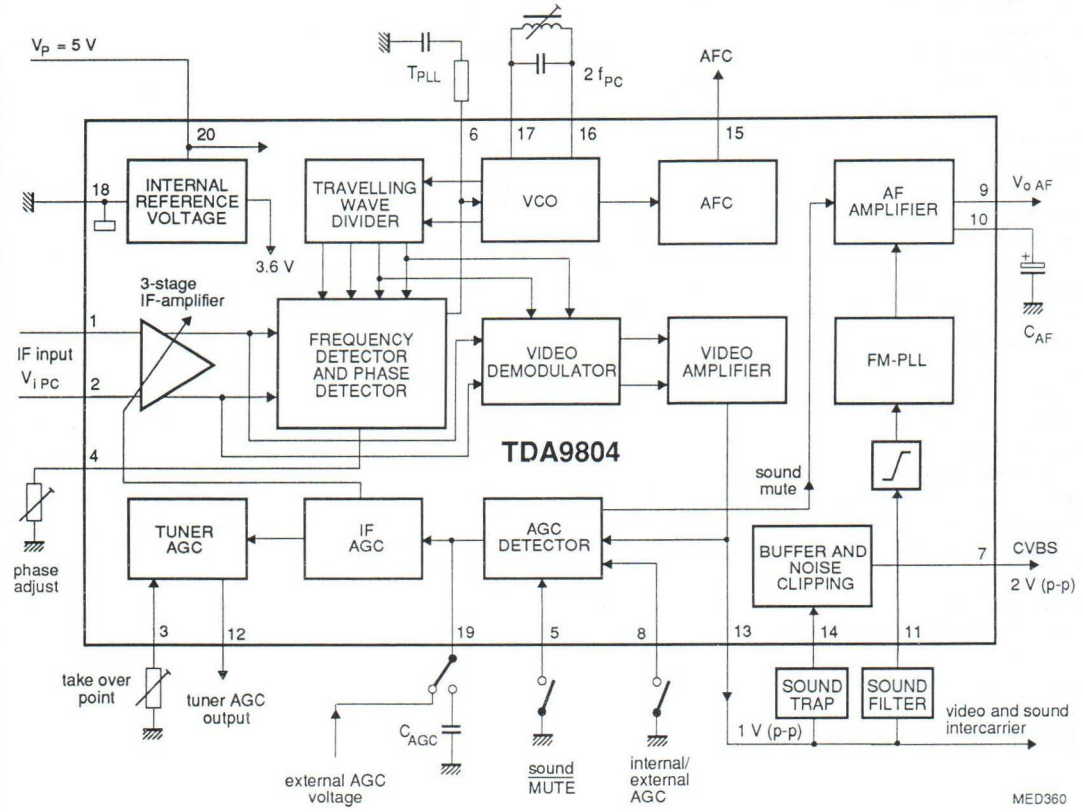


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ϕADJ	4	phase detector adjust
$Mute_{SWI}$	5	mute switch input
T_{PLL}	6	PLL time constant of phase detector
$V_{o\,CVBS}$	7	CVBS (positive) output signal
AGC_{SWI}	8	internal/external AGC switch
$V_{o\,AF}$	9	audio frequency output signal
C_{AF}	10	decoupling capacitor of audio frequency amplifier
$V_{i\,IC}$	11	sound intercarrier input signal
TAGC	12	tuner AGC output
$V_{o\,VID}$	13	video and sound intercarrier output signal
$V_{i\,VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor and external AGC voltage
V_P	20	positive supply voltage

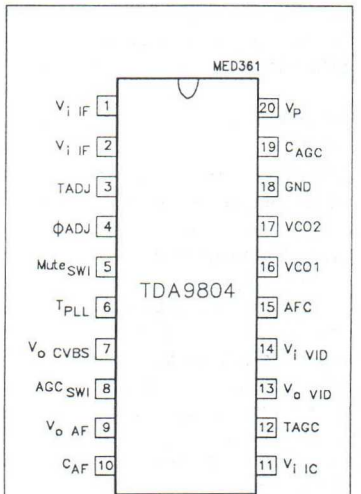


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. Since the TDA9804 is suitable for negative modulation only the peak-sync level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. In case of an external AGC (depending on the input voltage at pin 8) the internal charging and discharging currents are switched off and an external AGC voltage has to be applied to pin 19.

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. The frequency detector is operational before lock-in. A DC current is generated which is proportional to the frequency difference between the input frequency and the VCO frequency. After lock-in, the frequency detector and the phase detector generate a DC current proportional to the phase difference between VCO and input signals. The control signal for the VCO is provided by the phase detector.

The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.

The VCO signal is divided-by-two in

a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13). The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters. The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

Sound demodulation

The FM sound intercarrier signal is fed to pin 11 and through a limiter amplifier before it is demodulated. This achieves high sensitivity and high AM suppression. The limiter amplifier consists of seven internal AC-coupled stages, minimizing the DC offset.

The FM-PLL demodulator consists of an RC-oscillator, loop filter and phase detector. The oscillator frequency is locked on the FM intercarrier signal from the limiter amplifier. As a result of this locking, the RC-oscillator is frequency-modulated.

The modulating signal voltage (AF signal) is used to control the oscillator frequency. By this, the FM-PLL works as an FM demodulator.

The audio frequency amplifier with internal feedback is designed for high gain and high common mode rejection. The low-level AF signal coming out of the FM-PLL demodulator is amplified and buffered in a low-ohmic audio signal output stage (pin 9). An external decoupling capacitor on pin 10 removes the DC voltage from the audio amplifier input.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1) SOT146 at +120 °C	0	8.8	V
V_I	voltage on pins 1, 2, 7, 11, 13, 14, 15 and 19	0	V_P	V
$t_{s\ max}$	short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	−25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes to the Limiting Values

1. Supply current I_P = 69 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air SOT146	73 K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz with V_{PC}/V_{SC} = 13 dB (B/G); V_{iIF} = 10 mV RMS value (sync level at B/G); video modulation DSB; residual carrier: B/G = 10%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 20)	see note 1	4.5	5	8.8	V
I_P	supply current		51	60	69	mA
AGC switch input (pin 8)						
V_{IH}	input voltage for internal AGC	see note 2	1.5	–	V_P	V
V_{IL}	input voltage for external AGC		0	–	0.8	V
I_{IL}	LOW level input current	V_8 = 0 V	–	–300	–360	μA
Vision IF input (pins 1 and 2)		B/G standard				
V_i	input signal sensitivity (RMS value)	–1 dB video at output	–	50	90	μV
	maximum input signal (RMS value)	+1 dB video at output	70	150	–	mV
ΔV_i	IF amplitude difference between picture and sound carrier	within AGC range	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4	64	70	73	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance		1.7	2.2	2.7	kΩ
C_i	input capacitance		1.2	1.7	2.5	pF
$V_{1,2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		see note 3				
f_{VCO}	maximum oscillator frequency for carrier regeneration	f = $2f_{PC}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	see note 4; ΔT = 0 to +70 °C	–	–	±1300	10^{-6}
$V_{o\ ref}$	oscillator swing at pins 16 and 17 (RMS value)		tbn	120	tbn	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	see note 5; BL = 60 kHz	–	–	30	ms
$V_{i\ IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	see note 6; maximum IF gain	–	70	100	μV
	for C/N = 10 dB	see note 7	–	100	140	μV
I_{loop}	FPLL loop offset current at pin 6	see note 8	–	–	±4.5	μA
Composite video amplifier (pin 13)		sound carrier off				
$V_{o\ vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level		1.4	1.5	1.6	V
	zero carrier level		2.5	2.6	2.7	V
	upper video clipping level		V_P – 1.1	V_P – 1.0	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{o\ FM}$	IF intercarrier level (RMS value)	sound carrier on; see note 9	tbn	140	tbn	mV
R_{13}	output resistance		–	–	10	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.0	tbn	–	mA
B	–3 dB video bandwidth	$C_{13} < 50$ pF; $R_L > 1$ kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	see note 10; $C_{13} < 50$ pF; $R_L > 1$ kΩ	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input	pin 14 not connected	1.5	1.8	2.1	V
G_v	voltage gain	see note 11	6	7	7.5	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	tbn	4.0	–	V
		lower video clipping	–	1.0	tbn	V
		sync level	1.25	1.35	1.45	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.4	tbn	–	mA
B	–3 dB video bandwidth	$C_7 < 20$ pF; $R_L > 1$ kΩ	8	11	–	MHz
Measurements from IF input to CVBS output (pin 7) 330 Ω between pins 13 and 14, sound carrier off						
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	B/G standard; see note 12	–	–	1	%
ΔG	differential gain		–	2	5	%
Δφ	differential phase		–	1	3	deg
B	–3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 13	56	59	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 1.1 MHz	56	62	–	dB
	intermodulation at 'yellow'		58	64	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 3.3 MHz	56	62	–	dB
	intermodulation at 'yellow'		57	63	–	dB
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	see note 10	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal		–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		–	50	100	ms
I_{19}	charging current	see note 12	0.85	1.1	1.35	mA
	discharging current		17	22	27	μA
V_{19}	AGC voltage	see Fig.4				
		maximum gain	0	tbn	–	V
		minimum gain	–	tbn	$V_P - 0.7$	V
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	ΔT = 0 to +50 °C	–	1	3	dB
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	μA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 15				
S	control steepness $\Delta I_{15}/\Delta f$	see note 16	0.6	0.72	0.84	μA/kHz
Δf_{IF}	frequency variation by temperature	ΔT = 0 to +70 °C; see note 4	–	–	±1300	10^{-6}
V_{15}	output voltage upper limit	see Fig.8	$V_P - 0.5$	$V_P - 0.3$	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	μA
	output current sink		160	200	240	μA
ΔI_{15}	residual video modulation current (peak-to-peak value)		–	20	30	μA
Sound mute switch (pin 5)		see note 17				
V_{IL}	input voltage for MUTE-ON		0	–	0.8	V
V_{IH}	input voltage for MUTE-OFF		1.5	–	V_P	V
I_{IL}	LOW level input current	V_5 = 0 V	–	–300	–360	μA
α_{mute}	audio attenuation	V_5 = 0 V	70	80	–	dB
ΔV_5	DC offset voltage at switching (plop)	switching to MUTE-ON	–	100	500	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM sound limiter amplifier (pin 11)		FM 5.5 MHz				
$V_{i\,FM}$	input signal (RMS value, pin 11)	CCIR468-4				
	for S/N = 40 dB	see Fig.11	–	200	300	μV
	for AM suppression α_{AM} = 40 dB	AM: f = 1 kHz; m = 0.3	–	1	–	mV
	maximum input signal handling (RMS value)		200	–	–	mV
R_{11}	input resistance		480	600	720	Ω
B	–3 dB IF frequency response of sound IF	lower and upper cut-off frequency	3.5	–	10	MHz
V_{11}	DC voltage		2.3	2.6	2.9	V
FM-PLL sound demodulator and AF output (pin 9)		see note 18				
$f_{i\,FM}$	catching range of PLL		4	–	7	MHz
	holding range of PLL		3.5	–	8	MHz
t_{acqu}	acquisition time		–	–	4	μs
Δf_{AF}	frequency deviation	THD < 1.5%; see note 19	–	–	±50	kHz
V_{10}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; see note 20	1.2	–	2.2	V
$V_{o\,AF}$	AF output signal (RMS value, pin 9)	Δf_{AF} = ±27 kHz; see Fig.11	280	350	420	mV
	maximum output signal handling	THD < 1.5%	0.8	–	–	V
ΔV_o	temperature drift of AF output signal	ΔT = 0 to +70 °C	–	0.2	0.5	dB
R_9	output resistance		–	100	–	Ω
R_L	load resistance (pin 9)		2.2	–	–	kΩ
V_9	DC voltage		1.6	2.0	2.4	V
B	–3 dB audio frequency bandwidth		95	120	–	kHz
THD	total harmonic distortion		–	0.1	0.5	%
S/N (W)	signal-to-noise ratio, weighted	CCIR468-4; see Fig.11	50	55	–	dB
V_{SC}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
α_{AM}	AM suppression	see Fig.10; AM: f = 1 kHz; m = 0.3	46	50	–	dB
RR	ripple rejection on pin 9	see Fig.9	26	30	–	dB
Measurements from IF input to audio output (pin 9)		560 Ω between pins 13 and 11				
S/N (W)	weighted signal-to-noise ratio referred to 54% FM modulation	CCIR468-4; with offset alignment on pin 4				
	6 kHz sinusoidal waveform	black-to-white	39	46	–	dB
	black level	sync only	39	48	–	dB
	white picture		39	46	–	dB

Notes to the characteristics

1. Typical values of video and sound parameters are decreased at V_P = 4.5 V.
2. The input voltage for internal AGC has to be V_8 > 1.5 V, or pin 8 open-circuit.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2 calculated with grey level and FPLL input signal level).
   Resonance circuit of VCO: Q_o > 50; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF (loop voltage about 2.7 V).
4. The oscillator drift is related to the picture carrier frequency (at external temperature-compensated LC-circuit).
5. $V_{i\,IF}$ = 10 mV (RMS value); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ for 0.9 V CVBS (peak-to-peak value) at composite video output pin 13; PLL is still locked.
7. Transformer at IF input (Fig.3). The C/N ratio at IF input for 'lock-in' is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band-limited white noise signal (RMS value); video modulation: white picture.
8. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF-amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open-circuit.
9. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula:

   $$20 \log \left(\frac{V_{13\,\text{interc.}\,(p-p)}}{1\ V\ (p-p)} \right) = \frac{V_{iSC}}{V_{iPC}}\ dB + 6.9\ dB \pm 2\ dB$$

   with

   $\frac{V_{iSC}}{V_{iPC}}$ dB = sound to picture carrier ratio at IF input (pins 1 and 2) in dB

   and

   ±2 dB = tolerance of intercarrier output amplitude $V_{o\,FM}$.
10. Measurements taken with SAW filter G1956; modulation: VSB, f_{video} > 0.5 MHz, loop bandwidth BL = 60 kHz.
11. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
12. The leakage current of the AGC capacitor has to be < 1 µA to avoid larger tilt.
13. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
14. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal
    $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
15. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
16. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO
    (Q_o > 50; $C_o = C_{int} + C_{ext}$; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF).
17. No mute state is also valid for pin not connected.
18. A 5.5 MHz signal for second IF with 10 mV (RMS value) input level, f_{mod} = 1 kHz and frequency deviation with 54% FM modulation of audio reference is fed directly to pin 11. Audio measurements are taken at 50 µs de-emphasis.
19. To allow higher frequency deviation, the resistor R_x on pin 10 (see Fig.12) has to be increased to a value which does not exceed the AF output signal of nominally 0.35 V for THD = 0.1% (R_x = 4.7 kΩ provides –6 dB amplification).
20. The leakage current of the 2.2 µF capacitor is < 100 nA.

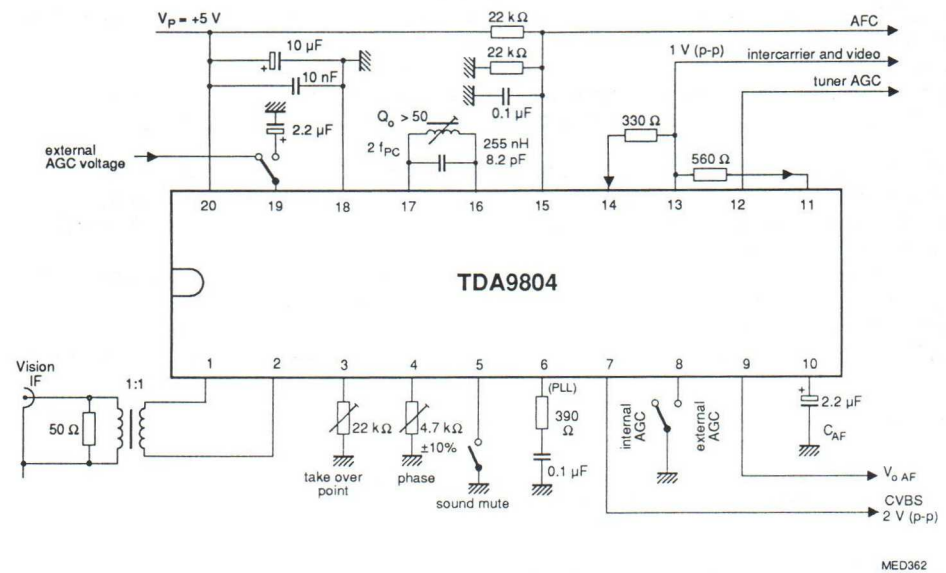


Fig.3 Test circuit.

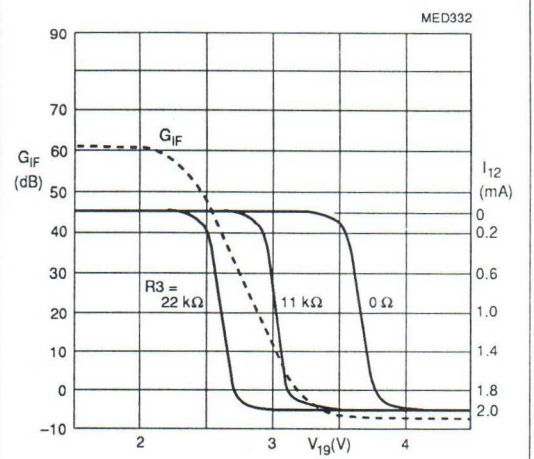


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

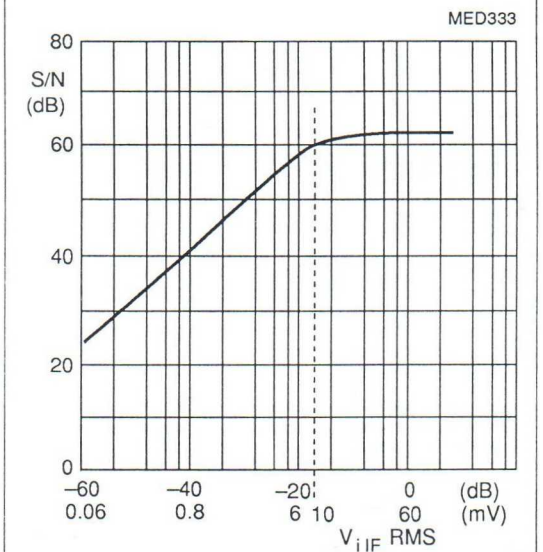
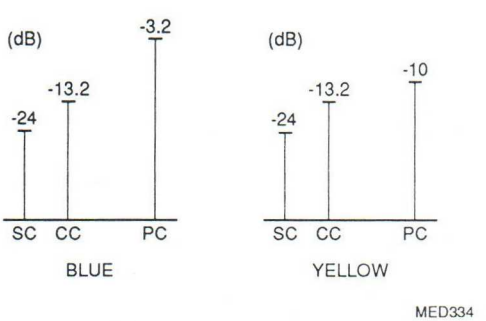


Fig.5 Typical signal-to-noise ratio as a function of IF input signal.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

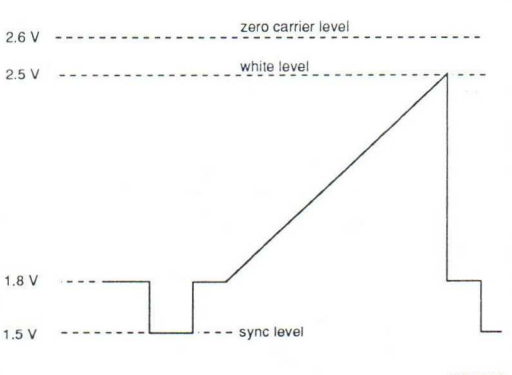
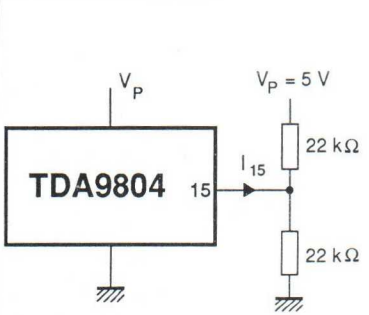


Fig.7 Video signal levels on output pin 13.



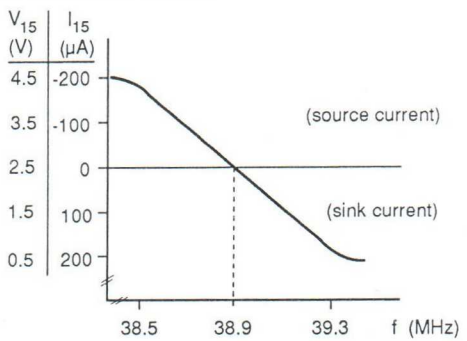


Fig.8 Measurement conditions and typical AFC characteristic.

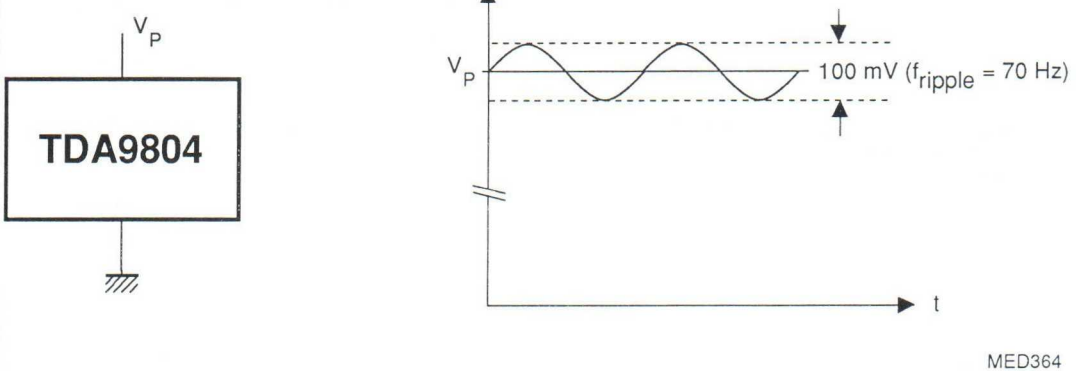


Fig.9 Ripple rejection condition.

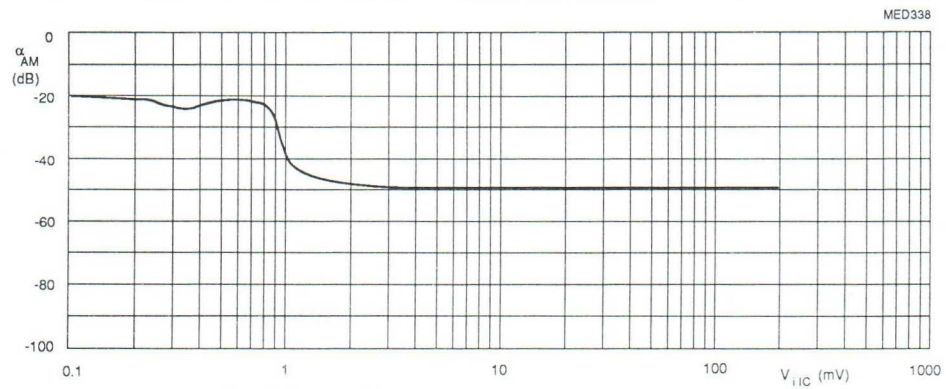


Fig.10 Typical AM suppression of FM sound demodulator.

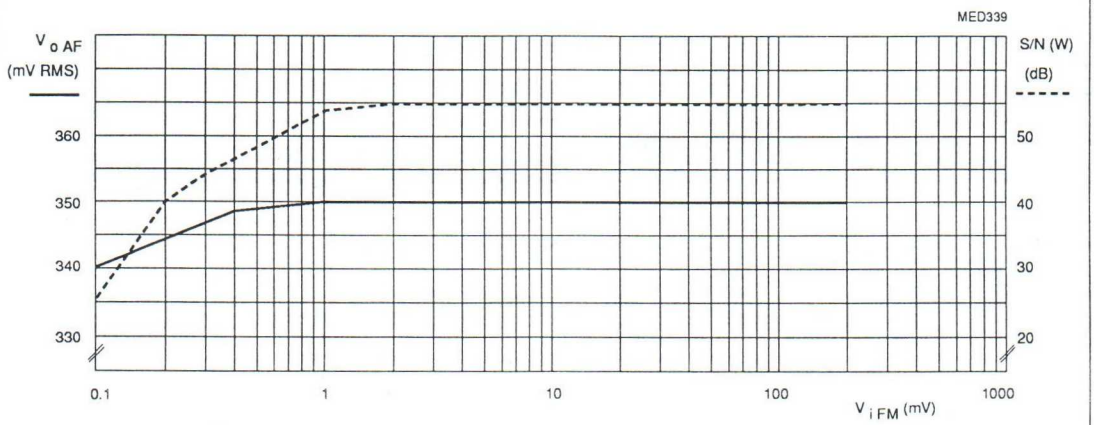


Fig.11 Typical AF output signal and signal-to-noise ratio.

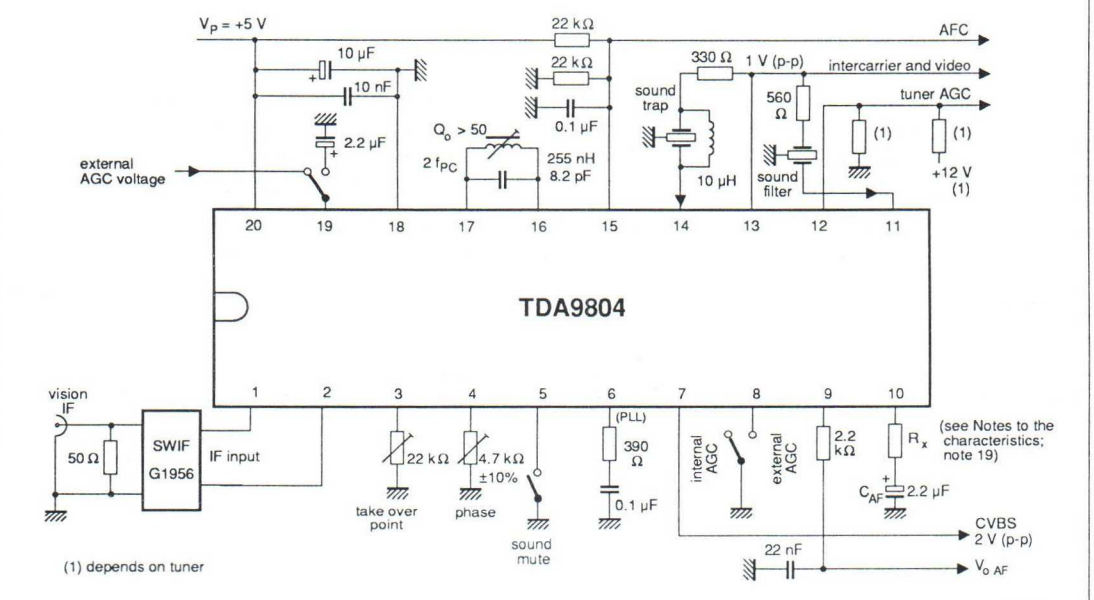


Fig.12 Application circuit.

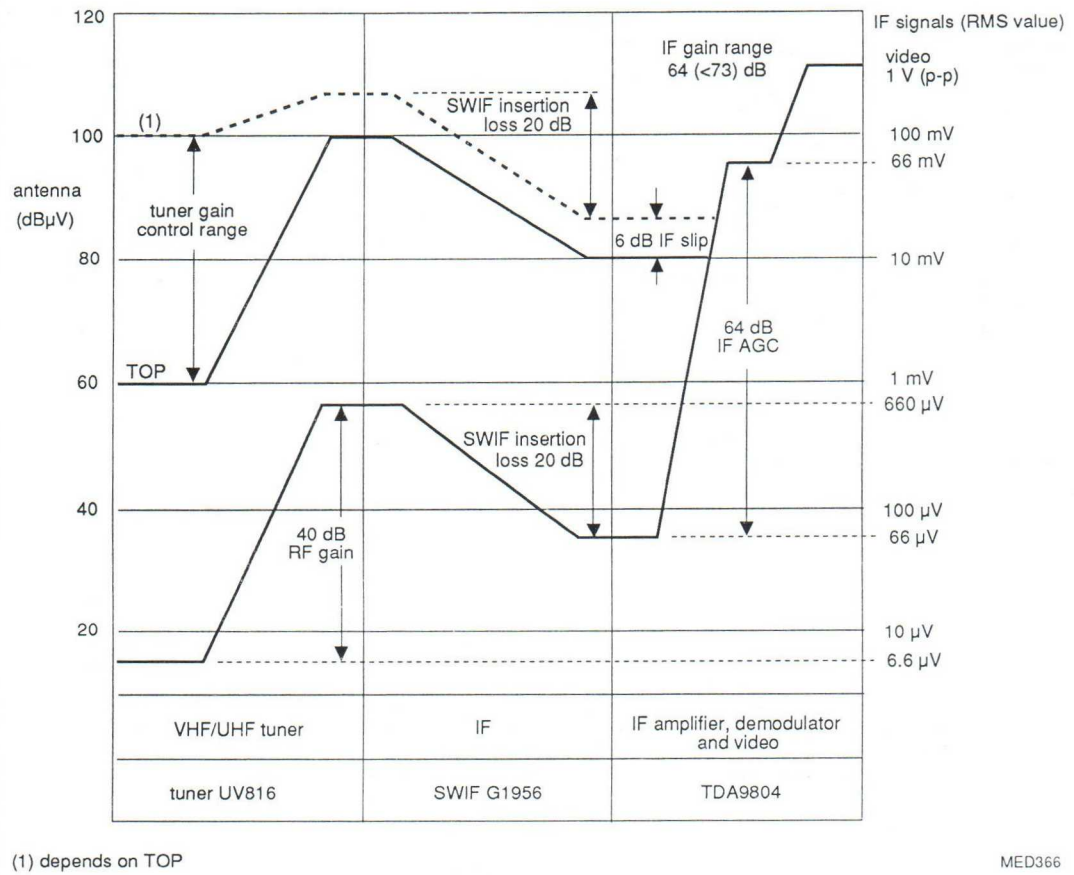


Fig.13 Front end level diagram.

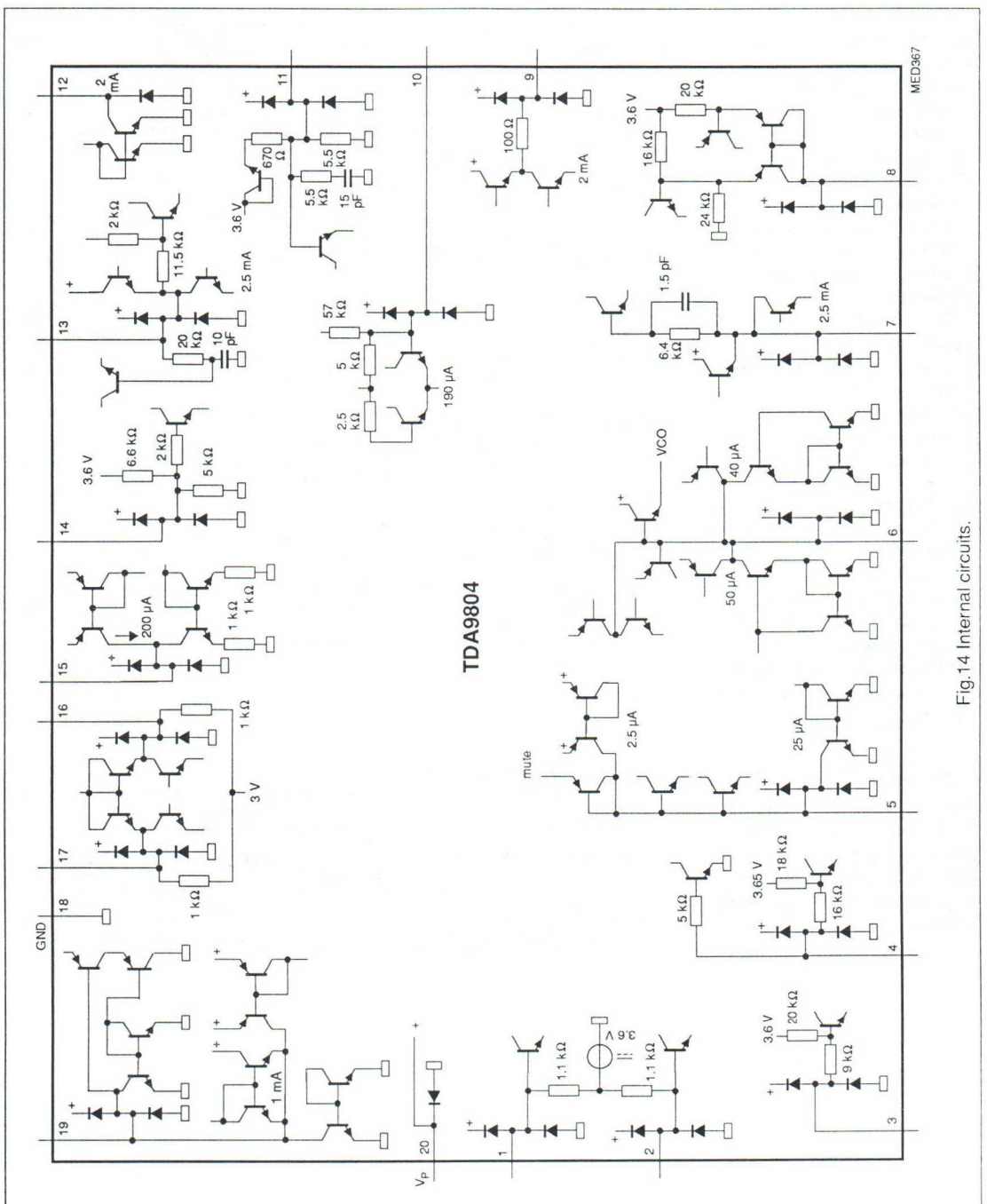


Fig.14 Internal circuits.

Single standard VIF-PLL with QSS-IF and FM-PLL demodulator

TDA9808

FEATURES

- 5 V positive supply voltage
- Applicable for IF frequencies of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- VIF AGC detector for gain control, operating as peak sync detector
- Tuner AGC with adjustable take over point (TOP)
- AFC detector without extra reference circuit
- SIF input for Single Reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; Single Reference QSS for high performance
- AC coupled limiter amplifier for sound intercarrier signal
- PLL-FM demodulator with high linearity, alignment-free
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 18)	4.5	5	5.5	V
I_P	supply current	72	85	98	mA
$V_{i\ VIF}$	vision IF input signal sensitivity (RMS value; pins 1 and 2)	–	60	100	μV
$V_{o\ CVBS}$	CVBS output signal on pin 9 (peak-to-peak value)	1.2	1.35	1.5	V
B	–3 dB video bandwidth on pin 9	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio for video	56	60	–	dB
$\alpha_{0.92}$	intermodulation attenuation	58	64	–	dB
$\alpha_{2.76}$		58	64	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{i\ SIF}$	sound IF input signal sensitivity (RMS value; pins 19 and 20)	–	50	100	μV
V_o	audio output signal for FM standard M, N (RMS value; 25 kHz modulation)	–	0.5	–	V
THD	total harmonic distortion; 25 kHz modulation for FM	–	0.15	–	%
S/N (W)	weighted signal-to-noise ratio; 25 kHz modulation for FM	–	60	–	dB

GENERAL DESCRIPTION

The TDA9808 is an integrated circuit for singlestandard (negative modulated) vision IF signal processing and FM demodulation, with single reference QSS-IF in TV and VTR sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9808	20	DIL	plastic	SOT146
TDA9808T	20	SO	plastic	SOT163A

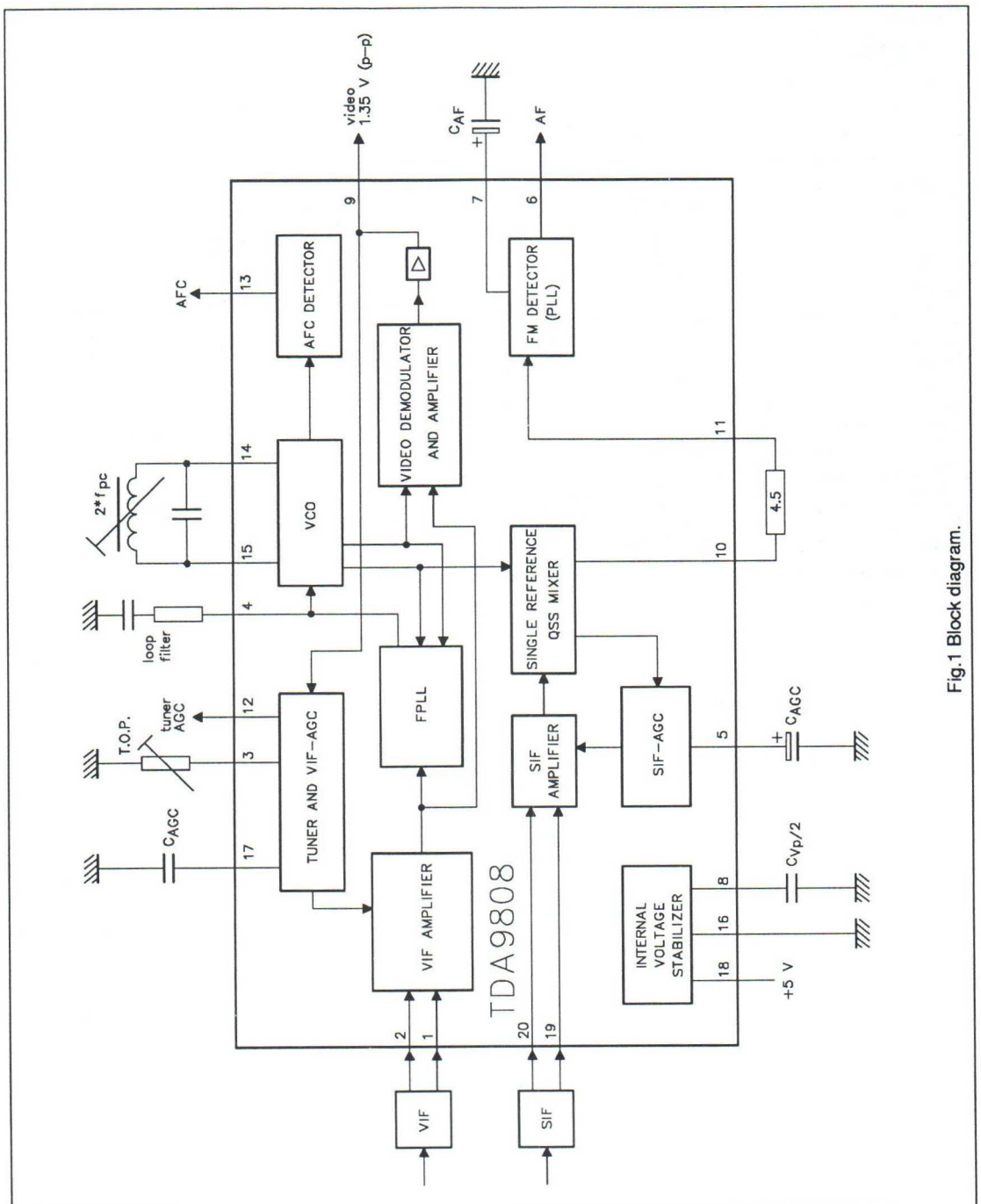


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF}$	1	VIF differential input signal
	2	
TADJ	3	tuner AGC takeover adjust (TOP)
T_{PLL}	4	PLL loop filter
C_{SAGC}	5	SIF AGC capacitor
$V_{o\ AF}$	6	audio frequency output
C_{AF}	7	decoupling capacitor
$C_{Vp/2}$	8	$V_P/2$ reference capacitor
$V_{o\ CVBS}$	9	CVBS output signal
$V_{o\ QSS}$	10	single reference QSS output
$V_{i\ FM}$	11	sound intercarrier input
TAGC	12	tuner AGC output
AFC	13	AFC output
VCO1	14	VCO reference circuit for $2f_{PC}$
VCO2	15	
GND	16	ground
C_{VAGC}	17	VIF AGC capacitor
V_P	18	positive supply voltage
$V_{i\ SIF}$	19	SIF differential input signal
	20	

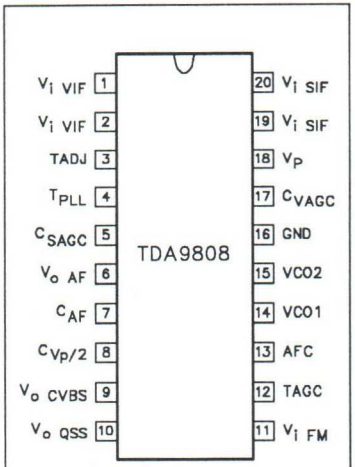


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network by means of emitter degeneration.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, to control the vision IF amplifier. Additionally it is fed into the tuner AGC amplifier to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC take over point can be adjusted at pin 3. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.
The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore the sync level of the video signal is detected.

Frequency-Phase detector (FPLL)

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current which is proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. Via the loop filter the DC current of either frequency detector or phase detector is converted into a DC voltage, which controls the VCO frequency.

VCO and AFC

The VCO operates with a symmetrically connected resonance circuit (with L and C in parallel). It is tuned to the double VIF picture carrier frequency. The VCO is controlled by two integrated varicaps. The control voltage required to tune the VCO from its free running frequency to actual double the PC frequency is generated by the frequency-phase detector and fed via the loop filter to the first varicap (FPLL). This control voltage is amplified, and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.
The oscillator signal is divided-by-two. Two differential output signals were generated with 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' VCO output signal.
The demodulator output signal is fed via an integrated low-pass for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video output signal at pin 9 is 1.35 V (p-p) for nominal vision IF modulation.

SIF amplifier and AGC

The sound IF amplifier consists of two AC coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.
The SIF AGC detector is related to the SIF signals (average level of FM carriers) at pin 19 and pin 20 (SIF input) and controls the SIF amplifier to provide a constant SIF signal at the SIF amplifier output.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 10. With this system a high performance Hi-Fi stereo sound processing can be achieved.

FM detector

The FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC coupled in order to minimize the DC offset and to save pins for DC decoupling.

The FM-PLL consists of an integrated RC oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the limited FM intercarrier signal. As a result of locking, the oscillator tracks with the frequency modulation of the input signal. The oscillator control voltage is superimposed by the AF voltage. By this way the FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

1) The AF pre-amplifier is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF output voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of this pre-amplifier reduces the harmonics of the intercarrier signal at the sound output terminal.

An additional DC control circuit is implemented to keep the DC level constant, independent of process spreadings.

2) The AF output amplifier (10 dB) provides the required output level by means of a rail-to-rail output stage.

Internal voltage stabilizer and $V_P/2$-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals this constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $V_P/2$ voltage has to be filtered via a low-pass by using an external capacitor at pin 8 together with an integrated resistor ($f_g \approx 5$ Hz). For a fast setting to $V_P/2$ an internal start-up circuit is added.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	–	7.6	V
	SOT163A at +120 °C	–	5.9	V
V_i	voltage at pins 1 to 8, 11 to 13, 16 to 20	0	5.5	V
$t_{s\ max}$	maximum short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	0	13.2	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes to the Limiting Values

1. I_{18} = 98 mA; T_{amb} = +70 °C.
2. Charge device model class B: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	65 K/W
	SOT163A	85 K/W

CHARACTERISTICS

The following characteristics apply for T_{amb} = +25 °C, V_P = 5 V, f_{pc} = 45.75 MHz (M), f_{pc} = 58.75 MHz (M), f_{SC} = 41.25 MHz (M), f_{SC} = 54.25 MHz (M); input level $V_{i\ IF1,2}$ = 10 mV RMS value (sync-level); $V_{i\ IF19,20}$ = 4.5 mV RMS value (SC), IF input from 50 Ω via broadband transformer 1:1; video modulation DSB; residual carrier M: 10%; video signal: NTC-7 composite; test circuit according to Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 18)						
V_{18}	supply voltage	note 1	4.5	5	5.5	V
I_{18}	supply current		72	85	98	mA
Vision IF amplifier (pins 1 and 2)						
$V_{i\ VIF}$	input sensitivity (RMS value) at 45.75 MHz	–1 dB video at output	–	60	90	µV
	input sensitivity (RMS value) at 58.75 MHz		–	70	100	µV
	maximum input signal (RMS value) at 45.75 MHz	+1 dB video at output	140	200	–	mV
	maximum input signal (RMS value) at 58.75 MHz		200	300	–	mV
$\Delta V_{o\ int.}$	internal IF amplitude difference between picture and sound carrier	within AGC range; M standard; Δf = 4.5 MHz	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4				
		45.75 MHz	65	70	–	dB
		58.75 MHz	68	73	–	dB
R_i	input resistance (differential)	note 2	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{1/2}$	DC voltage		–	3.4	–	V
True synchronous video demodulator (note 3)						
f_{VCO}	maximum oscillator frequency for carrier regeneration	f = 2f_{pc}	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	note 4	–	–	±750	Hz/K
$V_{o\ ref}$	oscillator swing at pins 14 and 15 (RMS value)	f_{pc} = 45.75 MHz	–	100	–	mV
		f_{pc} = 58.75 MHz	–	80	–	mV
Δf_{pc}	vision carrier capture range	M standard	±1.5	±2	–	MHz
t_{acqu}	acquisition time	note 5; BL = 60 kHz	–	–	30	ms
$V_{i\ VIF}$	VIF input signal sensitivity for PLL to be locked (RMS value; pins 1 and 2)	note 6; maximum IF gain	–	60	90	µV
I_{Loop}	FPLL loop offset current at pin 4	note 7	–	–	±4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 9; sound carrier off)						
$V_{o\ video}$	output signal (peak-to-peak value)	see Fig.9	1.2	1.35	1.5	V
V_9	sync level		–	1.5	–	V
	upper video clipping level		$V_P - 1.1$	$V_P - 1$	–	V
	lower video clipping level		–	0.3	0.4	V
R_9	output resistance	note 2	–	–	10	Ω
$I_{int\ 9}$	internal bias current for emitter-follower	DC	1.6	2.0	–	mA
I_9	maximum output sink current	DC and AC	1.0	–	–	mA
	maximum output source current		2.0	–	–	mA
ΔV_o	deviation of output signal	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	note 8	–	–	1	%
ΔG	differential gain	NTC-7 Composite	–	2	5	%
Δφ	differential phase		–	2	4	deg
B	–1 dB video bandwidth	M standard; $C_9 < 30$ pF; $R_L > 1.5$ kΩ; AC load	5	6	–	MHz
	–3 dB video bandwidth		7	8	–	MHz
S/N (W)	signal-to-noise ratio; weighted	see Fig.6 and note 9	56	60	–	dB
S/N	signal-to-noise ratio; unweighted		49	53	–	dB
$\alpha_{0.92}$	intermodulation at 'blue'	see Fig.7 and note 10; f = 0.92 MHz	58	64	–	dB
	intermodulation at 'yellow'		60	66	–	dB
$\alpha_{2.76}$	intermodulation at 'blue'	see Fig.7 and note 10; f = 2.76 MHz	58	64	–	dB
	intermodulation at 'yellow'		59	65	–	dB
α_c	residual vision carrier (RMS value)	fundamental wave and harmonics	–	2	10	mV
α_H	suppression of video signal harmonics	note 11; $C_9 < 30$ pF; $R_L > 1.5$ kΩ; AC load	35	40	–	dB
α_{sp}	spurious elements	note 12	40	–	–	dB
RR	ripple rejection at pin 9	see Fig.10; video signal: grey level	25	30	–	dB
VIF-AGC detector (pin 17)						
t_{resp}	response to an increasing amplitude step of 50 dB in the IF-input signal	+3 dB at video output pin 9	–	1	10	ms
	response to a decreasing amplitude step of 50 dB in the IF-input signal	–3 dB at video output pin 9	–	150	300	ms
I_{17}	charging current		55	75	95	μA
	discharging current	note 8	1.0	1.4	1.8	μA

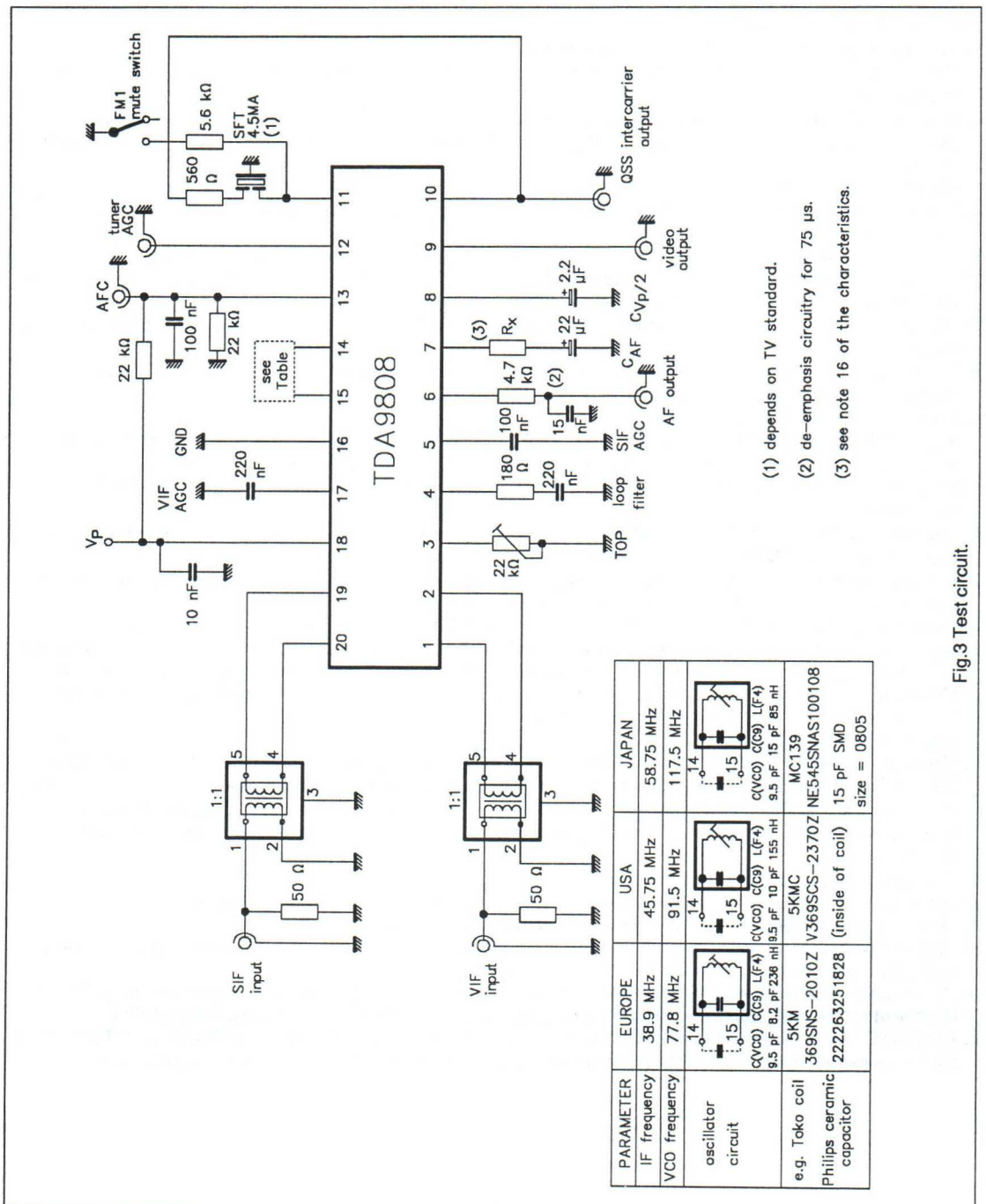
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1/2; R_{TOP} = 22 kΩ, I_{12} = 0.4 mA	–	2	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1/2; R_{TOP} = 0 Ω, I_{12} = 0.4 mA	50	100	–	mV
V_{12}	permissible output voltage	note 2; from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	I_{12} = 0.4 mA	–	0.03	0.07	dB/K
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	–	5	µA
		maximum tuner gain reduction	1.7	2.2	2.8	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 13; see Fig.8 and note 13)						
S	control steepness $\Delta I_{13} / \Delta f$	note 14				
		45.75 MHz	0.45	0.65	0.85	µA/kHz
		58.75 MHz	0.38	0.55	0.72	µA/kHz
f_{IF}	frequency variation by temperature	note 4	–	–	±750	Hz/K
V_{13}	output voltage upper limit	see Fig.8	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.6	V
I_{13}	output current source		150	200	250	µA
	output current sink		150	200	250	µA
ΔV_{13}	residual video modulation current (peak-to-peak value)		–	20	30	µA
Sound IF amplifier (pins 19 and 20)						
$V_{i\,SIF}$	input sensitivity (RMS value) at 41.25 MHz	–1 dB at intercarrier output pin 10	–	50	80	µV
	input sensitivity (RMS value) at 54.25 MHz		–	70	100	µV
	maximum input signal (RMS value) at 41.25 MHz	+1 dB at intercarrier output pin 10	40	80	–	mV
	maximum input signal (RMS value) at 54.25 MHz		80	110	–	mV
G_{SIF}	SIF gain control range	see Fig.5				
		41.25 MHz	59	64	–	dB
		54.25 MHz	59	64	–	dB
R_i	input resistance (differential)	note 2	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{19/20}$	DC voltage		–	3.4	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIF AGC detector (pin 5)						
I_5	charging current		3.5	5	6.5	µA
	discharging current		4.5	6	7.5	µA
Single reference QSS intercarrier mixer (pin 10)						
V_o	IF intercarrier level (RMS value)	SC_1	75	100	125	mV
B	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
α_H	residual sound carrier (RMS value)	fundamental wave	–	2	–	mV
		harmonics	–	0.75	–	mV
R_{10}	output resistance	note 2	–	–	10	Ω
V_{10}	DC voltage		–	2.0	–	V
I_{int10}	internal bias current for emitter-follower	DC	1.5	1.9	–	mA
I_{10}	output current (RMS value)	AC; $R_L > 1$ kΩ; $C_{10} < 50$ pF	–	–	1.2	mA
	output current	DC; $R_L > 1$ kΩ	2.0	2.5	–	mA
Limiter amplifier (pin 11)						
$V_{i\,FM}$	input signal for lock-in		–	–	100	µV
	input signal (RMS value)	(S+N)/N = 40 dB	–	300	400	µV
	permitted input signal (RMS value)		200	–	–	mV
R_{11}	input resistance	note 2	480	600	720	Ω
V_{11}	DC voltage		–	1.8	–	V
FM-PLL demodulator						
$f_{i\,FM}$	catching range of PLL		4.0	–	7	MHz
	holding range of PLL		3.5	–	8	MHz
t_{acqu}	acquisition time		–	–	4	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM operation (standard M, N) (pin 6; notes 15 and 15a)						
$V_{o\,AF}$	AF output signal (RMS value)	25 kHz FM deviation; see Fig.3 and note 16; $R_x = 0\ \Omega$	400	500	600	mV
	clipping level (RMS value)	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%				
		$R_x = 0\ \Omega$; see Fig.3	–	–	±53	kHz
		$R_x = 470\ \Omega$; see Fig.3	–	–	±106	kHz
ΔV_o	temperature drift of AF output signal		–	3	7	10^{-3}dB/K
V_7	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 17	1.2	–	3.0	V
R_6	output resistance	note 2	–	–	100	Ω
V_6	DC voltage	tracked with supply voltage	–	$V_P/2$	–	V
I_6	output sink and source current	DC and AC	–	–	1.1	mA
B	–3 dB audio frequency bandwidth		100	125	–	kHz
THD	total harmonic distortion	without ceramic filter; Δf = 25 kHz	–	0.15	0.5	%
S/N(W)	signal-to-noise ratio; weighted	FM-PLL only; with 75 µs de-emphasis; 25 kHz FM deviation; CCIR468-4	55	60	–	dB
V_{sc}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
α_{AM}	AM suppression	with 75 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 25 kHz FM deviation	46	50	–	dB
α_6	mute attenuation of AF signal	pin 6	70	75	–	dB
ΔV_6	DC jump of AF output terminal for switching from FM to mute state and vice versa	FM PLL has to be in locked mode	–	±50	±150	mV
RR	ripple rejection at pin 6	$R_x = 470\ \Omega$; see Fig.10	22	28	–	dB
Single reference QSS AF performance for FM operation (standard M) notes 18 and 19 picture to sound carrier ratio: PC/SC = 7 dB sound attenuation of VIF SAW filter: minimum 33 dB						
measurement condition: PC/SC ratio at pins 1 and 2; note 20			40	–	–	dB
S/N(W)	signal-to-noise ratio; weighted	25 kHz FM deviation; CCIR 468-4; 75 µs de-emphasis				
	black picture		50	56	–	dB
	white picture		47	53	–	dB
	colour bar		45	51	–	dB

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as an application information for designing the television receiver.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with sync level within gain control range). Resonance circuit of VCO: $Q_0 > 50$; C_{ext} see Fig.11; $C_{int} \approx 10$ pF (loop voltage approximately 2.7 V).
4. The oscillator drift is related to the picture carrier frequency (at external temperature-compensated LC-circuit).
5. $V_{i\,IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ for 1.2 V (peak-to-peak value) output signal at composite video output pin 9; PLL is still locked.
7. Offset current between pin 4 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at VIF input (pins 1 and 2) and VIF amplifier gain at minimum ($V_{17} = V_P$).
8. The leakage current of the AGC capacitor should not exceed 100 nA at M, N standard. Larger currents will increase the tilt.
9. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 9). B = 4.2 MHz weighted in accordance with CCIR 567 at a source impedance of 50 Ω.
10. The intermodulation figures are defined:
    $\alpha_{0.92}$ = 20 log (V_0 at 3.58 MHz / V_0 at 0.92 MHz) + 3.6 dB; $\alpha_{0.92}$ value at 0.92 MHz related to black/white signal
    $\alpha_{2.76}$ = 20 log (V_0 at 3.58 MHz / V_0 at 2.76 MHz); $\alpha_{2.76}$ value at 2.76 MHz related to colour carrier.
11. Measurements taken with SAW filter M3951M (Siemens, M standard); modulation: VSB, $f_{video} > 0.5$ MHz, loop bandwidth BL = 60 kHz.
12. Measurements taken with SAW filter M3951M and M9352M (Siemens, M standard); loop bandwidth BL = 60 kHz, frequency range = 10 kHz to 5 MHz. Sound carrier on, PC/SC ratio 7 dB (transmitter).
13. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.8. The AFC-steepness can be changed by the resistors R11 and R12.
14. Depending on the ratio $\Delta C / C_0$ of the LC resonant circuit of VCO ($Q > 50$; see note 3; $C_0 = C_{int} + C_{ext}$).
15. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 400 Hz, 25 kHz (50% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pins 5 and 17 have to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 75 µs de-emphasis. The FM demodulator steepness $\Delta V_{o\,AF}/\Delta f_{AF}$ is positive.
    a) Second IF input level 10 mV RMS.
16. Measured at de-emphasis circuitry with an FM deviation of 25 kHz (f_{mod} = 400 Hz) the typical AF output signal is 500 mV RMS (R_x = 0 Ω; see Fig.3). By using R_x = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS). For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with R_x = 470 Ω.
17. The leakage current of the decoupling capacitor (2.2 µF) should not exceed 1 µA.
18. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    - Incidental phase modulation for black-to-white jump less than 0.5 degree.
    - QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB for 6 kHz sinewave black-to-white video modulation.
19. Measurements are taken with SAW filter M3951M (Siemens) for vision IF (supressed sound carrier) and M9352M (Siemens) for sound IF (supressed picture carrier). Input level $V_{i\,SIF}$ = 10 mV RMS, 25 kHz FM deviation.
20. The PC/SC ratio is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC ratio will change these values.



PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	C(VCO) 9.5 pF, C(C9) 8.2 pF, L(F4) 236 nH	C(VCO) 9.5 pF, C(C9) 10 pF, L(F4) 155 nH	C(VCO) 9.5 pF, C(C9) 15 pF, L(F4) 85 nH
e.g. Toko coil	5KM 369SNS–2010Z	5KMC V369SCS–2370Z	MC139 NE545SNAS100108
Philips ceramic capacitor	2222632518 28	(inside of coil)	15 pF SMD size = 0805

Fig.3 Test circuit.

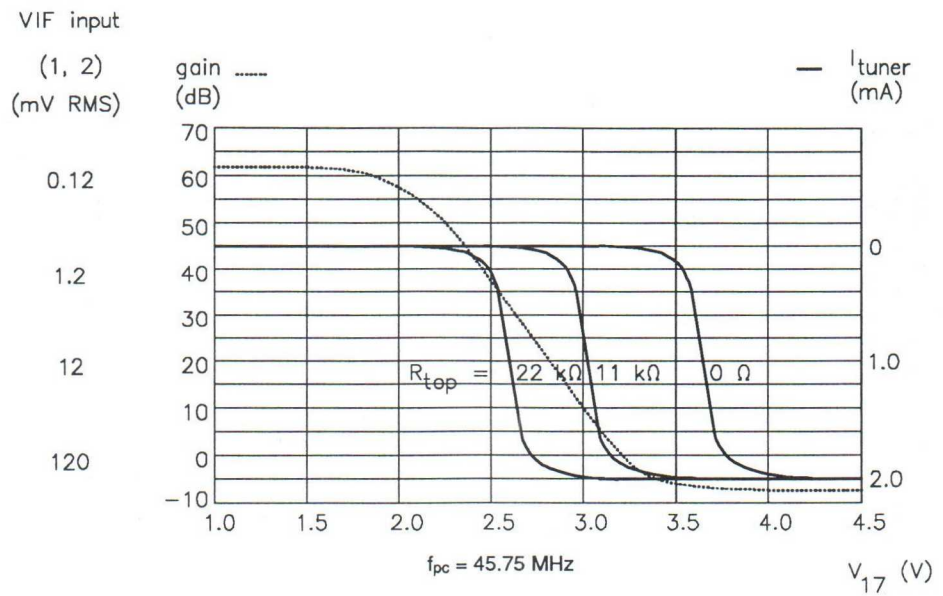


Fig.4 Typical VIF and tuner AGC characteristic.

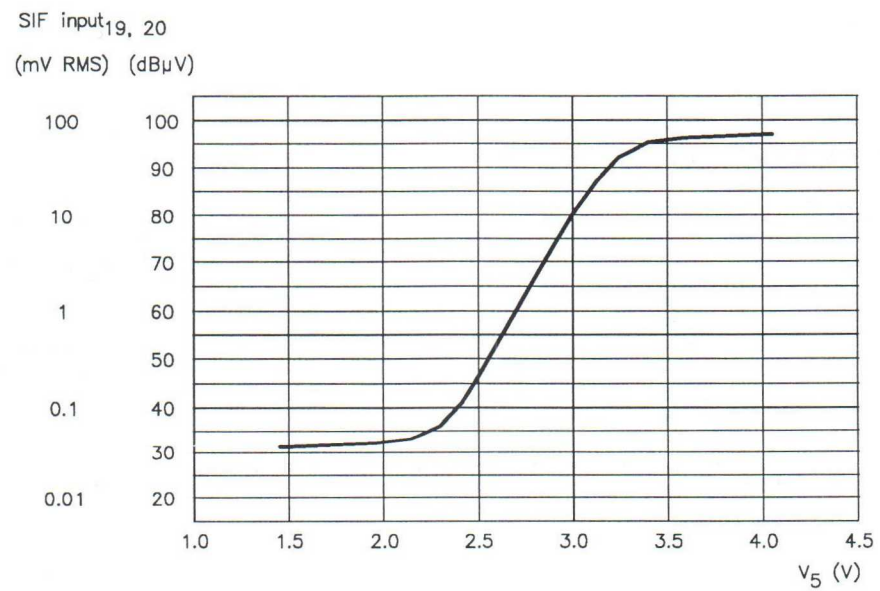


Fig.5 Typical SIF AGC characteristic.

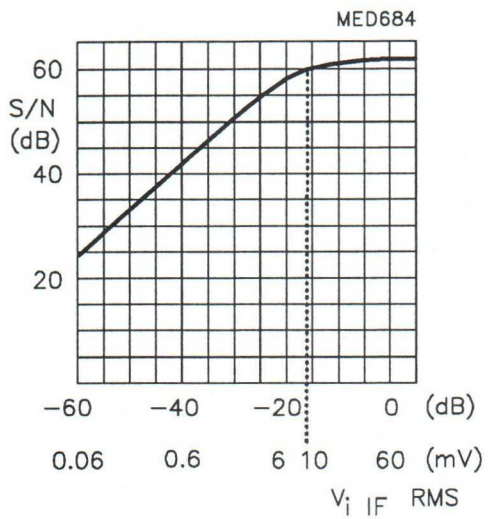
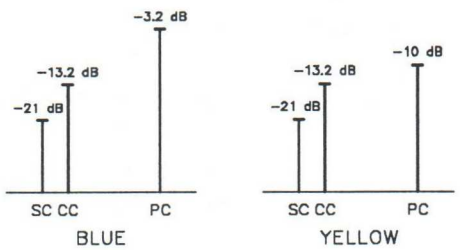


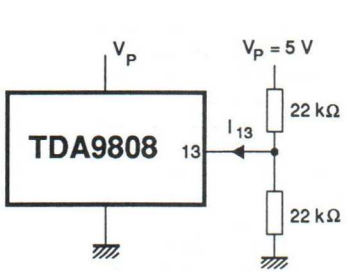
Fig.6 Typical S/N as a function of IF input voltage.



SC = sound carrier
CC = chrominance carrier
PC = picture carrier
all with respect to sync level

The sound carrier levels are taking into account a sound shelf attenuation of 20 dB.

Fig.7 Input signal conditions.



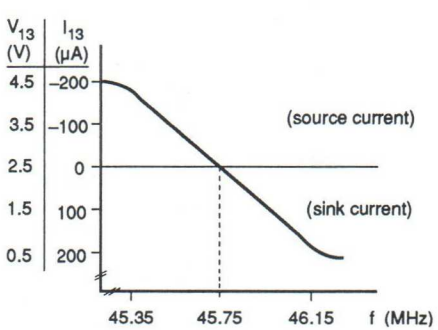


Fig.8 Measurement conditions and typical AFC characteristic.

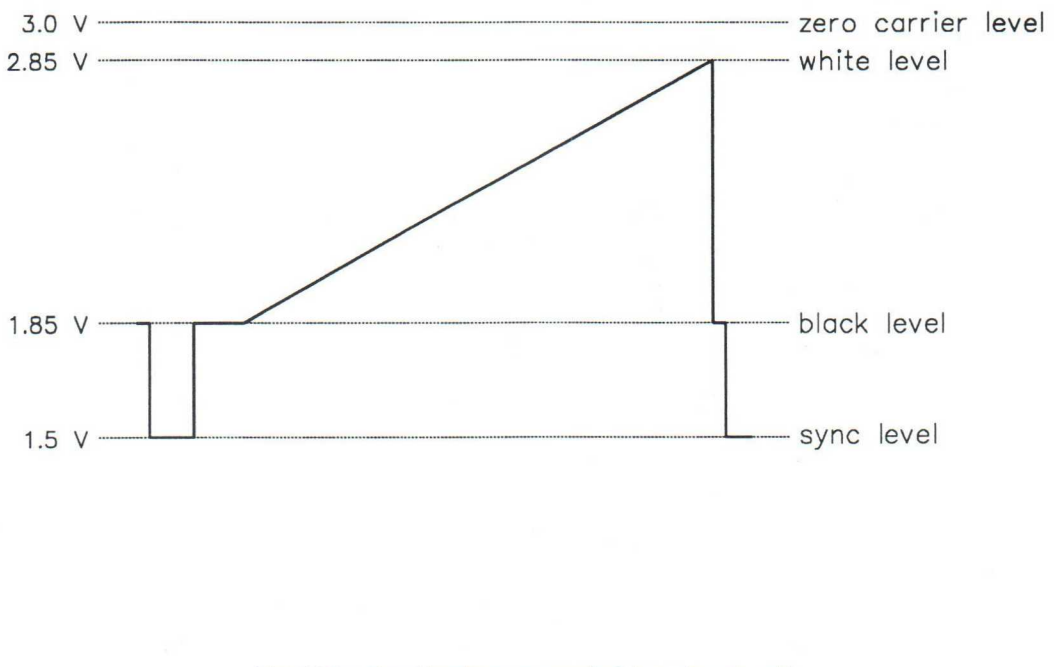


Fig.9 Video signal levels on output pin 9 (sound carrier off).

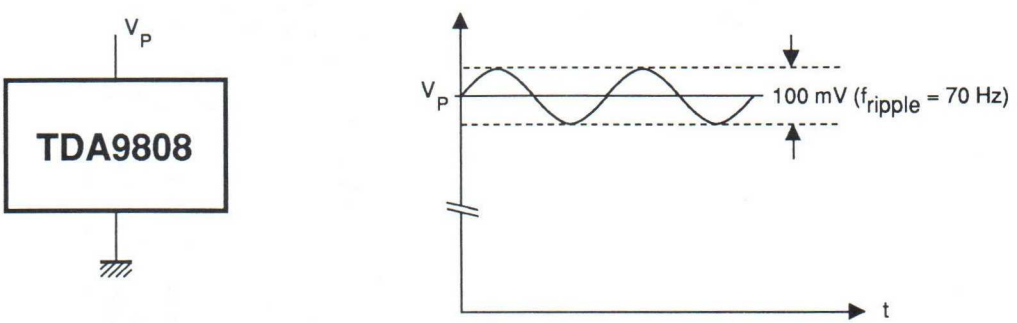
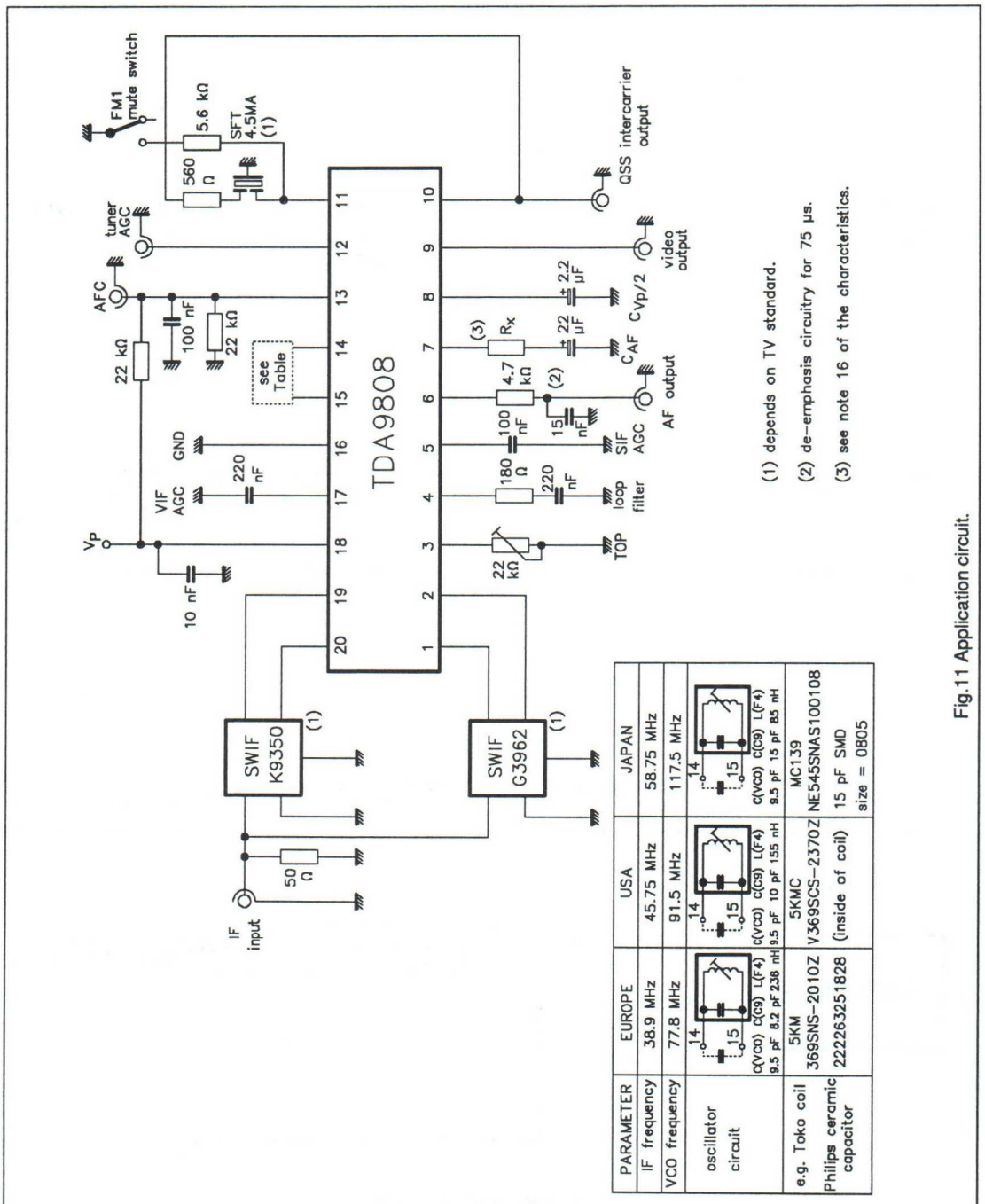


Fig.10 Ripple rejection condition.



PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	C(VCO) 9.5 pF C(G) 8.2 pF L(F4) 238 nH	C(VCO) 9.5 pF C(G) 10 pF L(F4) 155 nH	C(VCO) 9.5 pF C(G) 15 pF L(F4) 85 nH
e.g. Toko coil	5KM	5KMC	MC139
Philips ceramic capacitor	369SNS–2010Z 222263251828	V369SCS–2370Z (inside of coil)	NE545SNAS100108 15 pF SMD size = 0805

Fig.11 Application circuit.

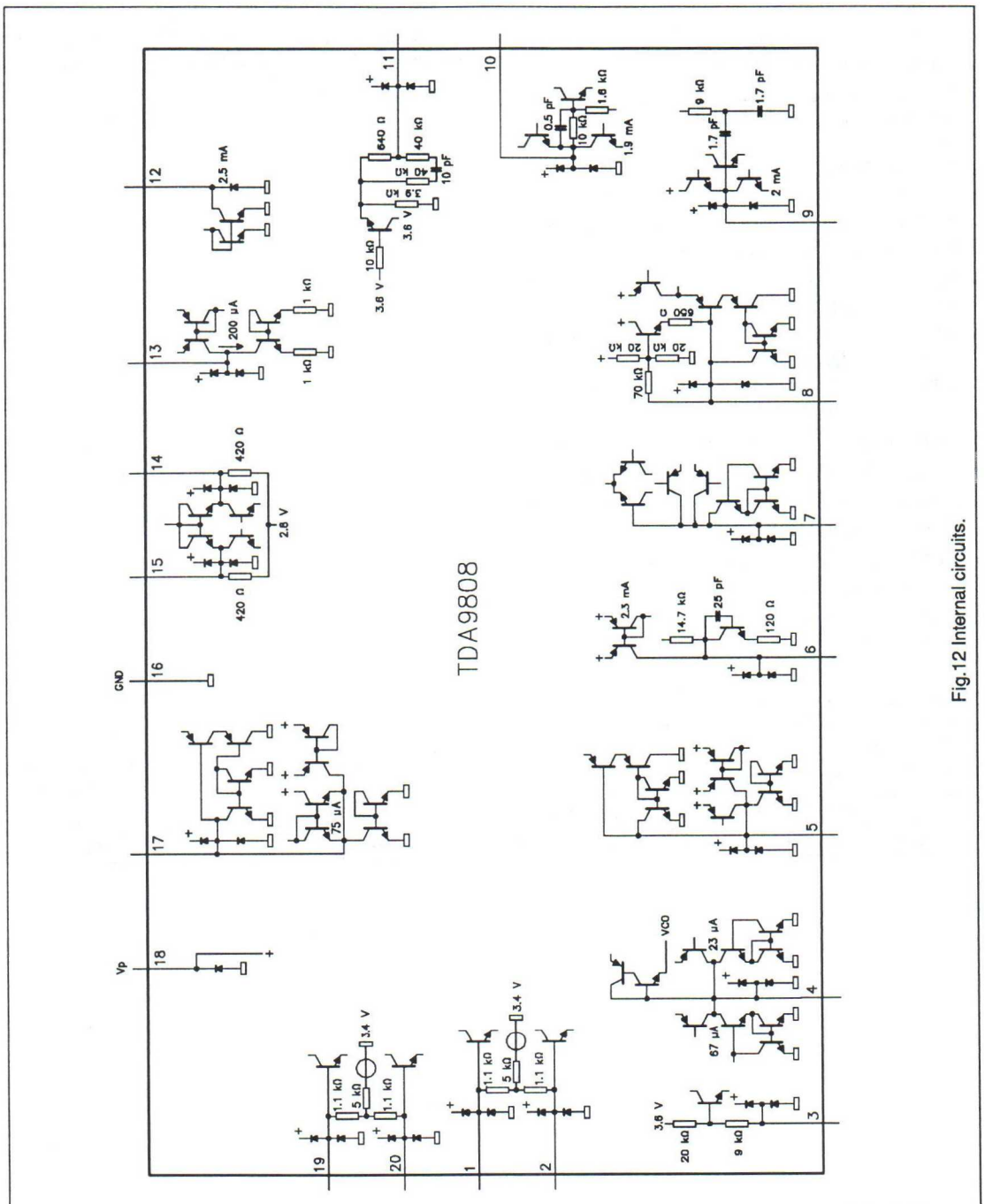


Fig.12 Internal circuits.

Multistandard VIF-PLL and FM-PLL/AM demodulator

TDA9812

FEATURES

- 5 V positive supply voltage
- Gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L/L accent standard
- VCO frequency switchable between L and L accent (alignment external) picture carrier frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for B/G (optional external AGC) and peak white detector for L; signal controlled reaction time for L
- Tuner AGC with adjustable Take Over Point (TOP)
- AFC detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM-PLL demodulator with high linearity, switchable de-emphasis for FM
- AM-SIF AGC detector for gain controlled SIF amplifier
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9812/T is an integrated circuit for multistandard vision IF signal processing and AM and FM sound demodulation in TV and VTR sets.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9812	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TDA9812T	SO28	plastic small outline package; 28 leads body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	5	5.5	V
I_P	supply current		82	96	110	mA
$V_{i\ VIF(rms)}$	vision IF input signal voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$V_{o\ CVBS\ (p-p)}$	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B_{-3}	−3 dB video bandwidth on pin CVBS	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio for video		56	60	–	dB
$IM_{\alpha 1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz	58	64	–	dB
$IM_{\alpha 3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz	58	64	–	dB
$\alpha_{H(sup)}$	suppression of harmonics in video signal		35	40	–	dB
$V_{i\ SIF(rms)}$	sound IF input signal voltage sensitivity (RMS value)	−3 dB video at AF output	–	70	100	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	B/G standard; 54% modulation	–	0.5	–	V
	audio output signal voltage for AM (RMS value)	L standard; 54% modulation	–	0.5	–	V
THD	total harmonic distortion	54% modulation				
	FM		–	0.15	0.5	%
	AM		–	0.5	1.0	%
S/N (W)	weighted signal-to-noise ratio	54% modulation				
	FM		–	60	–	dB
	AM		47	53	–	dB

BLOCK DIAGRAM

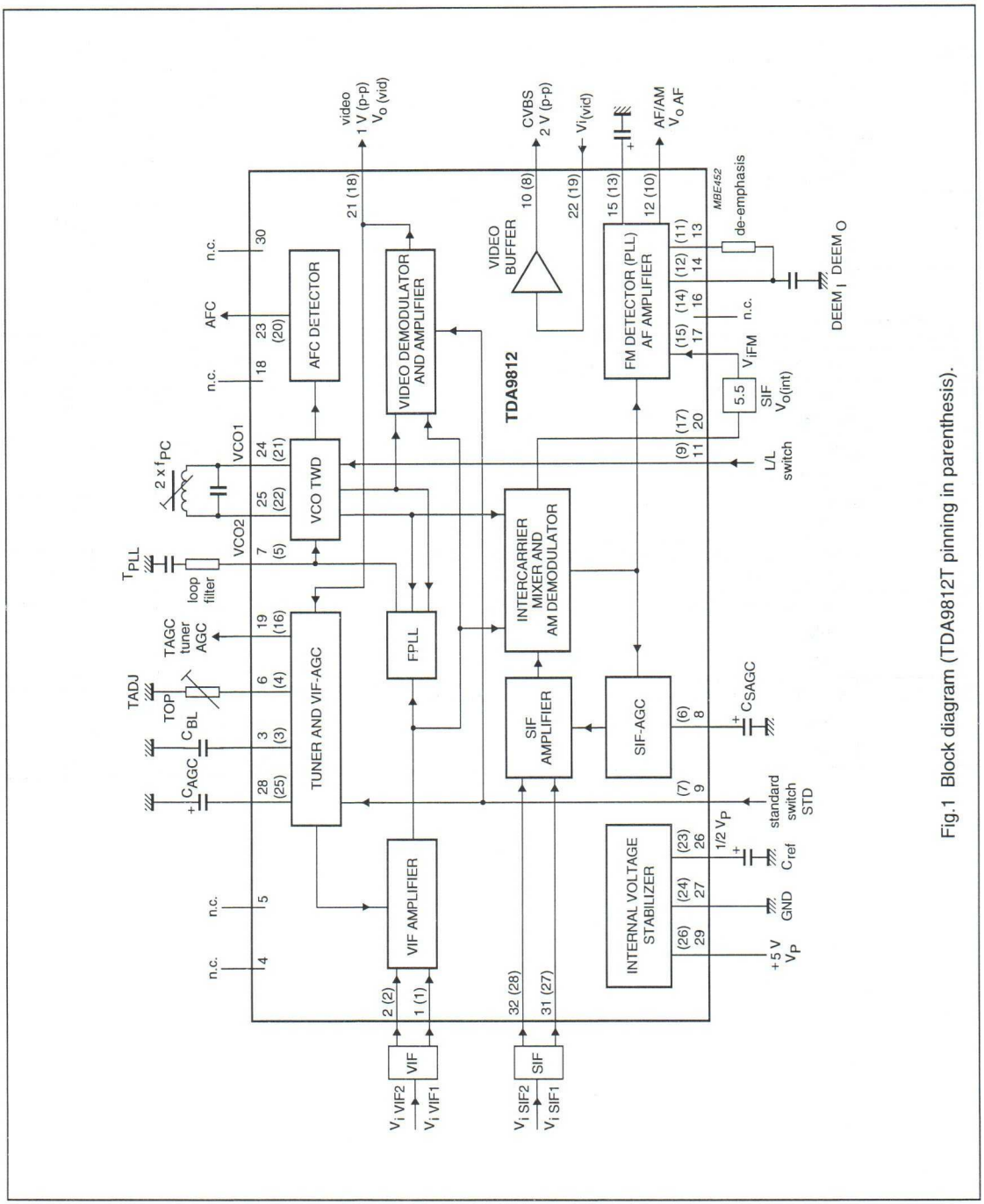


Fig.1 Block diagram (TDA9812T pinning in parenthesis).

PINNING

SYMBOL	PIN SDIP32	PIN SO28	DESCRIPTION
$V_{i\ VIF1}$	1	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	2	VIF differential input signal voltage 2
C_{BL}	3	3	black level detector
n.c.	4	–	not connected
n.c.	5	–	not connected
TADJ	6	4	tuner AGC take-over adjust (TOP)
T_{PLL}	7	5	PLL loop filter
C_{SAGC}	8	6	SIF AGC capacitor
STD	9	7	standard switch
$V_{o\ CVBS}$	10	8	CVBS output signal voltage
LSWI	11	9	L/L accent switch
$V_{o\ AF}$	12	10	audio voltage frequency output
$DEEM_I$	13	11	de-emphasis input
$DEEM_O$	14	12	de-emphasis output
C_{DEC}	15	13	decoupling capacitor
n.c.	16	14	not connected
$V_{i\ FM}$	17	15	sound intercarrier input voltage
n.c.	18	–	not connected
TAGC	19	16	tuner AGC output
$V_{o(int)}$	20	17	sound intercarrier output voltage
$V_{o(vid)}$	21	18	composite video output voltage
$V_{i(vid)}$	22	19	video buffer input voltage
AFC	23	20	AFC output
VCO1	24	21	VCO1 reference circuit for $2f_{PC}$
VCO2	25	22	VCO2 reference circuit for $2f_{PC}$
C_{ref}	26	23	$\frac{1}{2}V_P$ reference capacitor
GND	27	24	ground
C_{VAGC}	28	25	VIF AGC capacitor
V_P	29	26	supply voltage
n.c.	30	–	not connected
$V_{i\ SIF1}$	31	27	SIF differential input signal voltage 1
$V_{i\ SIF2}$	32	28	SIF differential input signal voltage 2

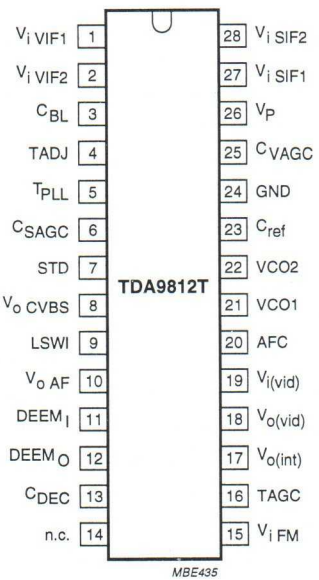


Fig.2 Pin configuration (SO28).

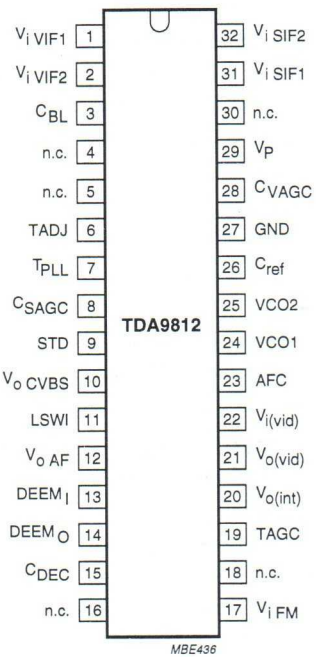


Fig.3 Pin configuration (SDIP32).

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output). The tuner AGC take-over point can be adjusted. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black-level detector voltage.

Frequency-Phase detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, travelling wave divider and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the Frequency-Phase detector and fed via the loop filter to the first variable capacitor (FPLL). This control voltage is amplified and additionally converted into a current which represents the AFC output signal. The VCO centre frequency can be decreased (required for L/L accent standard) by activating an additional internal capacitor. This is achieved by using the L/L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L/L accent switch for setting the VCO centre frequency to the required L/L accent value. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a Travelling Wave Divider (TWD) which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

SIF amplifier and AGC for AM sound

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signals (average level of AM carrier) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator. The SIF AGC reaction time is set to 'slow' for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector.

Intercarrier mixer

The intercarrier mixer is realized by a multiplier. The VIF amplifier output signal is fed to the intercarrier mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM detector

The FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset and to save pins for DC decoupling.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM-demodulator

The AF amplifier consists of two parts:

- The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal, at which the de-emphasis network for FM sound is applied. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
- The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM, FM de-emphasis or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer and $\frac{1}{2}V_P$-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $\frac{1}{2}V_P$ voltage has to be filtered via a low-pass filter by using an external capacitor together with an integrated resistor (f_g = 5 Hz). For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added.

LIMITING VALUES (SDIP32)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 29)	maximum chip temperature of +120 °C; note 1	0	5.5	V
V_i	voltage at pins 1 to 9, 11 to 19, 22, 23 and 28 to 32		0	V_P	V
$t_{s(max)}$	maximum short-circuit time		–	10	s
V_{19}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{esd}	electrostatic handling voltage	note 2	–300	+300	V

Notes

1. I_P = 110 mA; T_{amb} = +70 °C; $R_{th\ j\text{-}a}$ = 60 K/W for SDIP32 and $R_{th\ j\text{-}a}$ = 80 K/W for SO28.
2. Charge device model class B: equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP32	60	K/W
	SO28	80	K/W

CHARACTERISTICS (SDIP32 pinning)

V_P = 5 V; T_{amb} = +25 °C; see Table 1 for input frequencies and level; input level $V_{i\ IF\ 1,\ 2}$ = 10 mV RMS value (sync-level for B/G, peak white level for L); video modulation DSB; residual carrier B/G: 10%; L = 3%; video signal in accordance with "*CCIR, line 17*"; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 29)						
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		82	96	110	mA
Vision IF amplifier (pins 1 and 2)						
$V_{i(VIF)(rms)}$	input signal voltage sensitivity (RMS value)	B/G standard; –1 dB video at output	–	60	100	µV
$V_{i(max)(rms)}$	maximum input signal voltage (RMS value)	B/G standard; +1 dB video at output	120	200	–	mV
$\Delta V_{o(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; B/G standard; Δf = 5.5 MHz	–	0.7	1	dB
G_{IF}	IF gain control range	see Figs 5 and 6	65	70	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{1/2}$	DC input voltage		–	3.4	–	V
True synchronous video demodulator; see note 3						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{pc}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free-running) as a function of temperature	I_{AFC} = 0; note 4	–20	–	+20	ppm/K
$V_{0\ ref(rms)}$	oscillator voltage swing at pins 24 and 25 (RMS value)	B/G and L standard	70	100	130	mV
		L/L accent standard	45	65	85	mV
$\Delta f_{pc(capt)}$	vision carrier capture frequency range	B/G and L standard	±1.5	±2.0	–	MHz
		L/L accent standard; f_{pc} = 33.9 MHz; R_{11} = 5.6 kΩ	±1.0	±1.3	–	MHz
$\Delta f_{pc(ff)}$	vision carrier frequency (free-running) accuracy	L/L accent standard; f_{pc} = 33.9 MHz; R_{11} = 5.6 kΩ	–	±200	±400	kHz
$\Delta f_{pc(alg)}$	L/L accent alignment frequency range	I_{AFC} = 0	±400	±600	–	kHz
t_{acqu}	acquisition time	BL = 60 kHz; note 5	–	–	30	ms
$V_{i\ (VIF)(rms)}$	VIF input signal voltage sensitivity for PLL to be locked (RMS value; pins 1 and 2)	maximum IF gain; note 6	–	30	70	µV
$I_{PLL(os)}$	FPLL offset current at pin 7	note 7	–	–	±4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 21; sound carrier OFF)						
$V_{o\ video(p-p)}$	output signal voltage (peak-to-peak value)	see Fig.13	0.88	1.0	1.12	V
$V_{21(sync)}$	sync voltage level	B/G and L standard	–	1.5	–	V
$V_{21(clu)}$	upper video clipping voltage level		$V_P - 1.1$	$V_P - 1$	–	V
$V_{21(cll)}$	lower video clipping voltage level		–	0.3	0.4	V
R_{21}	output resistance	note 2	–	–	10	Ω
$I_{int\ 21}$	internal DC bias current for emitter-follower		1.6	2.0	–	mA
$I_{21(max)(sink)}$	maximum AC and DC output sink current		1.0	–	–	mA
$I_{21(max)(source)}$	maximum AC and DC output source current		2.0	–	–	mA
B_{-1}	–1 dB video bandwidth	B/G and L standard; $C_L < 50$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	B/G and L standard; $C_L < 50$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
α_H	suppression of video signal harmonics	$C_L < 50$ pF; $R_L > 1$ kΩ; AC load; note 8a	35	40	–	dB
PSRR	power supply ripple rejection at pin 21	video signal; grey level; see Fig.16				
		B/G standard	32	35	–	dB
		L standard	26	30	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 10 and 22)						
R_{22}	input resistance	note 2	2.6	3.3	4.0	kΩ
C_{22}	input capacitance	note 2	1.4	2	3.0	pF
V_{22}	DC input voltage		1.5	1.8	2.1	V
G_v	voltage gain	B/G and L standard; note 9	6.5	7	7.5	dB
$V_{10(clu)}$	upper video clipping voltage level		3.9	4.0	–	V
$V_{10(cll)}$	lower video clipping voltage level		–	1.0	1.1	V
R_{10}	output resistance	note 2	–	–	10	Ω
$I_{int\ 10}$	DC internal bias current for emitter-follower		2.0	2.5	–	mA
$I_{10(max)(sink)}$	maximum AC and DC output sink current		1.4	–	–	mA
$I_{10(max)(source)}$	maximum AC and DC output source current		2.4	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B_{-1}	–1 dB video bandwidth	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	8.4	11	–	MHz
B_{-3}	–3 dB video bandwidth	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	11	14	–	MHz
Measurements from IF input to CVBS output (pin 10; 330 Ω between pins 21 and 22, sound carrier OFF)						
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage on pin 10 (peak-to-peak value)	note 9	1.7	2.0	2.3	V
$V_{o\ CVBS(sync)}$	sync voltage level	B/G standard	–	1.35	–	V
		L standard	–	1.35	–	V
ΔV_o	deviation of CVBS output signal voltage at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(blBG)}$	black level tilt in B/G standard	gain variation; note 10	–	–	1	%
$\Delta V_{o(blL)}$	black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; gain variation; note 10	–	–	1.9	%
ΔG_{diff}	differential gain	*"CCIR, line 330"*	–	2	5	%
$\Delta\varphi_{diff}$	differential phase	*"CCIR, line 330"*	–	1	2	deg
B_{-1}	–1 dB video bandwidth	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio	see Figs 9 and 10; note 11	56	60	–	dB
S/N	unweighted signal-to-noise ratio	see Figs 9 and 10; note 11	49	53	–	dB
$IM\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz; see Fig.11 and note 12	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 1.1 MHz; see Fig.11; note 12	60	66	–	dB
$IM\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz; see Fig.11; note 12	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 3.3 MHz; see Fig.11; note 12	59	65	–	dB
$\alpha_{c(rms)}$	residual vision carrier (RMS value)	B/G and L standard; fundamental wave and harmonics	–	2	5	mV
$\alpha_{H(sup)}$	suppression of video signal harmonics	note 8a	35	40	–	dB
$\alpha_{H(spur)}$	spurious elements	note 8b	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PSRR	power supply ripple rejection at pin 10	video signal; grey level; see Fig.16				
		B/G standard	25	28	–	dB
		L standard	20	23	–	dB
VIF-AFC detector (pin 28)						
I_{28}	charging current	B/G and L standard; note 10	0.75	1	1.25	mA
	additional charging current	L standard in event of missing VITS pulses and no white video content	1.9	2.5	3.1	µA
	discharging current	B/G standard	15	20	25	µA
		normal mode L	225	300	375	nA
		fast mode L	30	40	50	µA
t_{resp}	AGC response to an increasing VIF step	B/G and L standard; note 13	–	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step	B/G standard	–	2.2	3.5	ms/dB
		fast mode L	–	1.1	1.8	ms/dB
		normal mode L; note 13	–	150	240	ms/dB
ΔIF	VIF amplitude step for activating fast AGC mode	L standard	–2	–6	–10	dB
V_3	threshold voltage level additional charging current	see Fig.13				
		L standard	–	1.95	–	V
		L standard; fast mode L	–	1.65	–	V
Tuner AGC (pin 19)						
$V_{i(rms)}$	IF input signal voltage for minimum starting point of tuner take-over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ; I_{19} = 0.4 mA	–	2	5	mV
	IF input signal voltage for maximum starting point of tuner take-over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω; I_{19} = 0.4 mA	50	100	5	mV
V_{19}	permissible output voltage	from external source; note 2	–	–	13.2	V
	saturation voltage	I_{19} = 1.5 mA	–	–	0.2	V
ΔV_{19}	variation of take-over point by temperature	I_{19} = 0.4 mA	–	0.03	0.07	dB/K
$I_{19(sink)}$	sink current	no tuner gain reduction; see Figs 5 and 6				
		V_{19} = 12 V	–	–	2.5	µA
		V_{19} = 13.2 V	–	–	5	µA
		maximum tuner gain reduction	1.5	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC circuit (pin 23); see Fig.12 and note 14						
S	control steepness $\Delta I_{23}/\Delta f$	note 15	0.5	0.72	1.0	µA/kHz
Δf_{IF}	frequency variation by temperature	I_{AFC} = 0; note 5	–20	–	+20	ppm/K
V_{23}	output voltage upper limit	see Fig.12	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit	see Fig.12	–	0.3	0.6	V
$I_{23(source)}$	output source current		150	200	250	µA
$I_{23(sink)}$	output sink current		150	200	250	µA
$\Delta I_{23(p-p)}$	residual video modulation current (peak-to-peak value)	B/G and L standard	–	20	30	µA
Sound IF amplifier (pins 31 and 32)						
$V_{i(SIF)(rms)}$	input signal voltage sensitivity (RMS value)	–3 dB video at AF output; pin 12	–	70	100	µV
$V_{i(max)(rms)}$	maximum input signal voltage (RMS value)	+1 dB video at AF output; pin 12	80	140	–	mV
G_{SIF}	SIF gain control range	see Figs 7 and 8	60	66	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{31/32}$	DC input voltage		–	3.4	–	V
$\alpha_{SIF/VIF}$	crosstalk attenuation between SIF and VIF input	between pins 1 and 2 and pins 31 and 32; note 16	50	–	–	dB
SIF-AFC detector (pin 8)						
I_8	charging current		0.8	1.2	1.6	mA
	discharging current	normal mode AM	1	1.4	1.8	µA
		fast mode AM	60	85	110	µA
Intercarrier mixer (B/G standard) (pin 20)						
$V_{o(rms)}$	IF intercarrier level (RMS value)	SC; note 17	–	see formula	–	mV
B_{-3}	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
$\alpha_{c(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	2	–	mV
R_{20}	output resistance	note 2	–	–	25	Ω
V_{20}	DC output voltage		–	2.0	–	V
I_{int20}	DC internal bias current for emitter-follower		1.5	1.9	–	mA
$I_{20(max)(sink)}$	maximum AC and DC output sink current		1.1	1.5	–	mA
$I_{20(max)(source)}$	maximum AC and DC output source current		3.0	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiter amplifier (pin 17); see note 18						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\left(\frac{S+N}{N}\right)$ = 40 dB	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
R_{17}	input resistance	note 2	480	600	720	Ω
V_{17}	DC input voltage		–	2.8	–	V
FM-PLL detector						
$f_{i\ FM(catch)}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
$f_{i\ FM(hold)}$	holding range of PLL	upper limit	9.0	–	–	MHz
		lower limit	–	–	3.5	MHz
t_{acqu}	acquisition time		–	–	4	μs
FM operation (B/G standard) (pin 12); see notes 18 and 18a						
$V_{o\ AF12(rms)}$	AF output signal voltage (RMS value)	without de-emphasis; short-circuit from pin 13 to pin 14; 27 kHz (54% FM deviation); see Fig.4 and note 19				
		R_x = 470 Ω	200	250	300	mV
		R_x = 0 Ω	400	500	600	mV
$V_{o\ AF12(cl)}$	AF output clipping signal voltage level	THD <1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD <1.5%; note 19	–	–	53	kHz
ΔV_o	temperature drift of AF output signal voltage		–	3	7	10^{-3} dB/K
V_{15}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 20	1.2	–	3.0	V
R_{12}	output resistance	note 2	–	–	100	Ω
V_{12}	DC output voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
$I_{12(max)(sink)}$	maximum AC and DC output sink current		–	–	1.1	mA
$I_{12(max)(source)}$	maximum AC and DC output source current		–	–	1.1	mA
B_{-3}	–3 dB video bandwidth	without de-emphasis; short-circuit from pin 13 to pin 14	100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N (W)	weighted signal-to-noise ratio	FM-PLL only; with 50 µs de-emphasis; 27 kHz (54% FM deviation); *"CCIR 468-4"*	55	60	–	dB
$\alpha_{c(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	–	75	mV
α_{AM}	AM suppression	50 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (54% FM deviation)	46	50	–	dB
α_{12}	mute attenuation of AF signal	B/G and L standard	70	75	–	dB
ΔV_{12}	DC jump voltage of AF output terminal for switching AF output to mute state and vice versa	FM-PLL in lock mode	–	±50	±150	mV
PSRR	power supply ripple rejection at pin 12	R_x = 470 Ω; see Fig.16	26	30	–	dB
AF performance for FM operation (B/G standard); see notes 21, 22 and 23; Table 1						
S/N (W)	weighted signal-to-noise ratio	PC/SC ratio at pins 1 and 2; 27 kHz (54% FM deviation); *"CCIR 468-4"*	27	–	–	dB
		black picture	45	51	–	dB
		white picture	45	51	–	dB
		6 kHz sine wave (black to white modulation)	40	46	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	35	40	–	dB
AM operation (L standard) (pin 12) see note 24						
$V_{o\ AF12(rms)}$	AF output signal voltage (RMS value)	54% modulation	400	500	600	mV
THD	total harmonic distortion	54% modulation; see Fig.15	–	0.5	1.0	%
B_{-3}	–3 dB AF bandwidth		100	125	–	kHz
S/N (W)	weighted signal-to-noise ratio	*"CCIR 468-4"*; see Fig.14	47	53	–	dB
V_{12}	DC potential voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
PSRR	power supply ripple rejection	see Fig.16	22	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Standard switch (pin 9); see also Table 2						
V_9	DC potential voltage for preferred settings					
	input voltage for negative standard	B/G standard; note 25	2.8	–	V_P	V
	input voltage for negative standard	negative AGC OFF	1.3	–	2.3	V
	input voltage for positive standard	L standard	0	–	0.8	V
I_{IL}	LOW level input current	V_9 = 0 V	190	250	310	µA
L/L accent switch (pin 11)						
V_{11}	DC potential voltage for L standard VCO frequency switching					
	L standard	note 25	2.8	–	V_P	V
	L/L accent standard and alignment		–	–	2.0	V
I_{IL}	LOW level input current	V_{11} = 0 V	150	200	250	µA

Notes

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with sync level within gain control range). Resonance circuit of VCO: Q_0 > 50; C_{ext} = 8.2 pF ±0.25 pF; C_{int} ≈ 8.5 pF (loop voltage approximately 2.7 V).
4. Temperature coefficient of external LC-circuit is equal to zero.
5. $V_{i\,IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ signal for nominal video signal.
7. Offset current measured between pin 7 and half of supply voltage (V_P = 2.5 V) under the following conditions: no input signal at VIF input (pins 1 and 2) and VIF amplifier gain at minimum (V_{28} = V_P). Due to sample-and-hold mode of the FPLL in L standard, the leakage current of the loop filter capacitor (C = 220 nF) should not exceed 500 nA.
8. Measurements taken with SAW filter G1962 (sound shelf: 20 dB); loop bandwidth BL = 60 kHz.
   a) modulation VSB; sound carrier OFF; f_{video} >0.5 MHz.
   b) sound carrier ON; SIF SAW filter L9453; f_{video} = 10 kHz to 10 MHz.
9. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 21 to pin 22).
10. The leakage current of the AGC capacitor should not exceed 1 µA at B/G standard respectively 10 nA current at L standard. Larger currents will increase the tilt.
11. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 10). B = 5 MHz weighted in accordance with *"CCIR 567"*.

12. The intermodulation figures are defined: $\alpha_{1.1}$ = 20 log (V_0 at 4.4 MHz/V_0 at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz referenced to black/white signal; $\alpha_{3.3}$ = 20 log (V_0 at 4.4 MHz/V_0 at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz referenced to colour carrier.
13. Response speed valid for a VIF input level range of 200 µV up to 70 mV.
14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.12. The AFC-steepness can be changed by the resistors at pin 23.
15. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO (Q > 50; see note 3; $C_0 = C_{int} + C_{ext}$).
16. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 38.9 MHz.
17. The intercarrier output signal at pin 20 can be calculated by the following formula taking into account the video output signal at pin 21 ($V_{o\ video(p-p)}$ = 1 V typical) as a reference:

$$V_{o(rms)} = 1V_{(p-p)} \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{iSC}}{V_{iPC}}(dB) + 6\ dB \pm 3\ dB}{20}}$$

with $\frac{1}{2\sqrt{2}}$ = correction term for RMS value,

$\frac{V_{iSC}}{V_{iPC}}(dB)$ = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB,

6 dB = correction term of internal circuitry

and ±3 dB = tolerance of video output and intercarrier output amplitude $V_{o(rms)}$.

Example: SAW filter G1962 (sound shelf: 20 dB) $\Rightarrow \frac{V_{iSC}}{V_{iPC}}$ = −27 dB $\Rightarrow V_{o(rms)}$ = 32 mV typical.

18. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pins 8 and 28 have to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 50 µs de-emphasis.

    a) Second IF input level 10 mV RMS.

19. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV RMS (R_x = 0 Ω; see Fig.4). By using R_x = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS). For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD <1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with R_x = 470 Ω.
20. The leakage current of the decoupling capacitor (2.2 µF) should not exceed 1 µA.
21. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    Incidental phase modulation for black-to-white jump less than 0.5 degrees
    Picture-to-sound carrier ratio; PC/SC = 13 dB; (transmitter)
    Sound shelf of VIF SAW filter: minimum 20 dB.
22. Measurements taken with SAW filter K6256 (Siemens) for vision and sound IF (sound shelf: 20 dB). Input level $V_{i\ SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
23. The PC/SC ratio at pins 1 and 2 is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC ratio will change these values.
24. Measurements taken with SAW filter L9453 (Siemens) for AM sound IF (suppressed picture carrier).
25. The input voltage has to be V >2.8 V, or open-circuit.

Table 1 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	L STANDARD	L/L ACCENT STANDARD	UNIT
Picture carrier	f_{pc}	38.9	38.9	33.9	MHz
Sound carrier	f_{sc}	33.4	32.4	40.4	MHz
Picture-to-sound carrier ratio	SC	13	10	10	dB

Table 2 Switch logic

STANDARD SWITCH	SELECTED STANDARD	VIDEO POLARITY	FM-PLL	AF-AMPLIFIER
2.8 V to V_P	B/G	negative	ON	FM
1.3 to 2.3 V	B/G, with external VIF AGC	negative	ON	FM
0 to 0.8 V	L	positive	OFF	AM

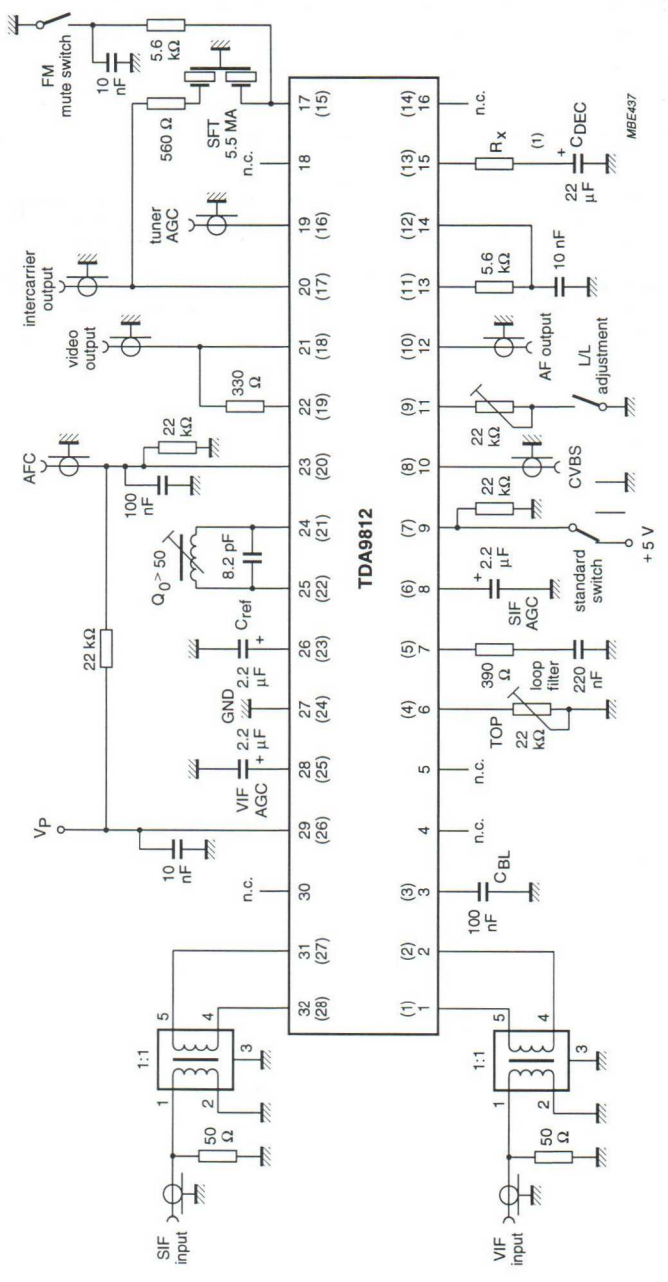


Fig.4 Test circuit (SO28 pinning in parenthesis).

(1) See note 19 of the characteristics.

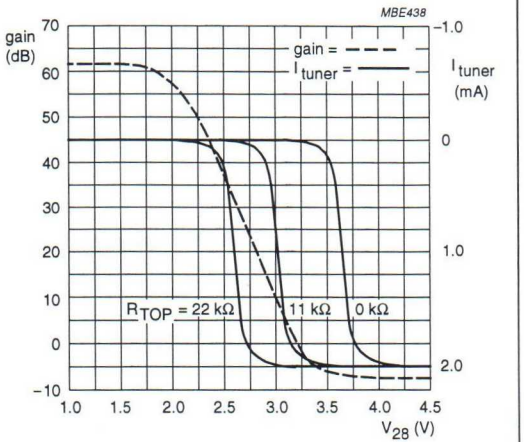


Fig.5 Typical tuner AGC characteristic.

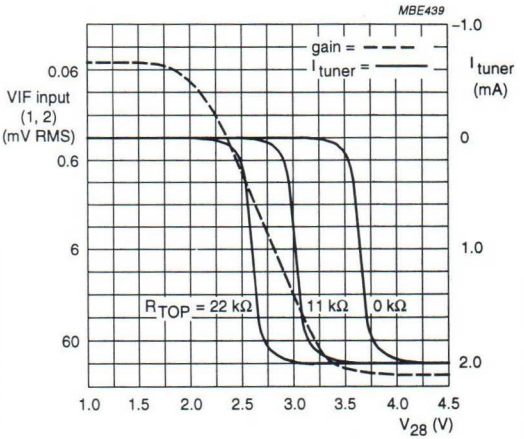


Fig.6 Typical tuner VIF characteristic.

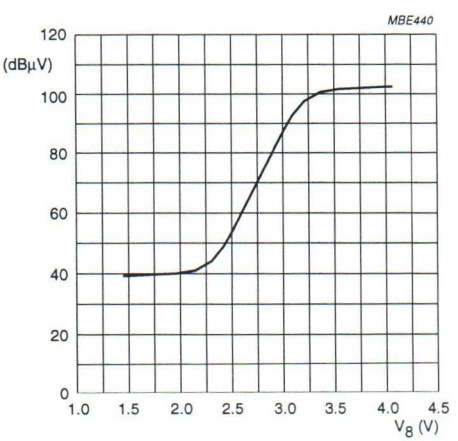


Fig.7 Typical AGC characteristic.

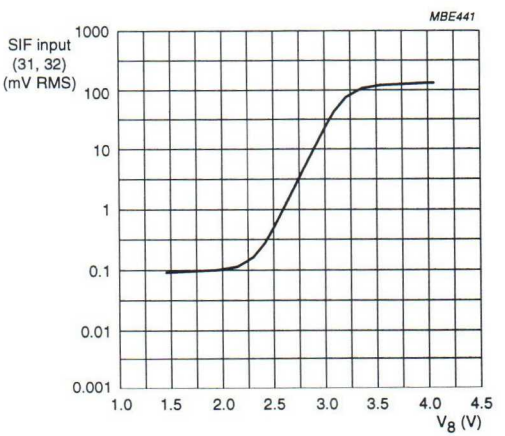


Fig.8 Typical SIF AGC characteristic.

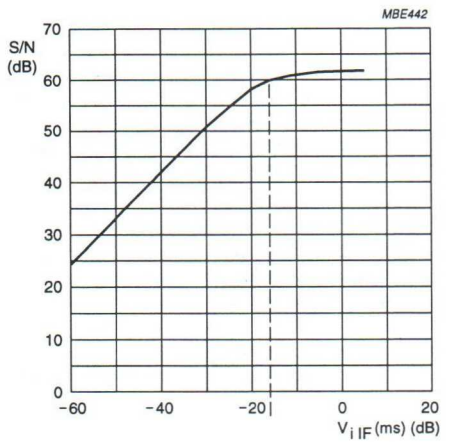


Fig.9 Typical signal-to-noise ratio as a function of IF input voltage (dB).

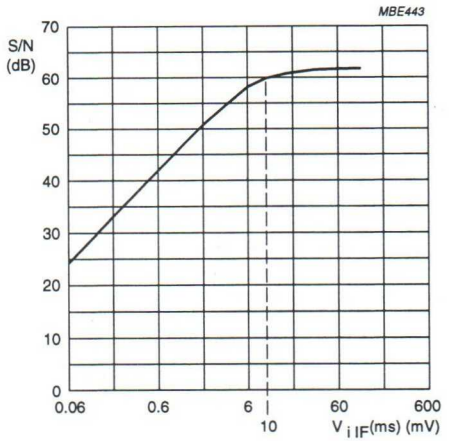
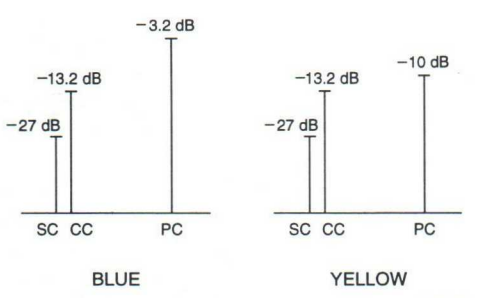


Fig.10 Typical signal-to-noise ratio as a function of IF input voltage (mV).



SC = Sound Carrier
CC = Chrominance Carrier
PC = Picture Carrier
all with respect to sync level.

The sound carrier levels take into account a sound shelf attenuation of 20 dB (SWIF G1962).

Fig.11 Input signal conditions.

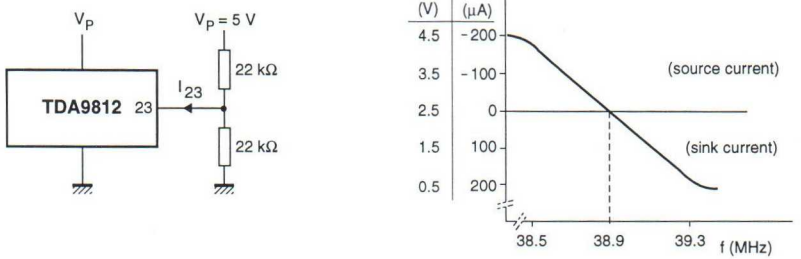


Fig.12 Measurement conditions and typical AFC characteristic.

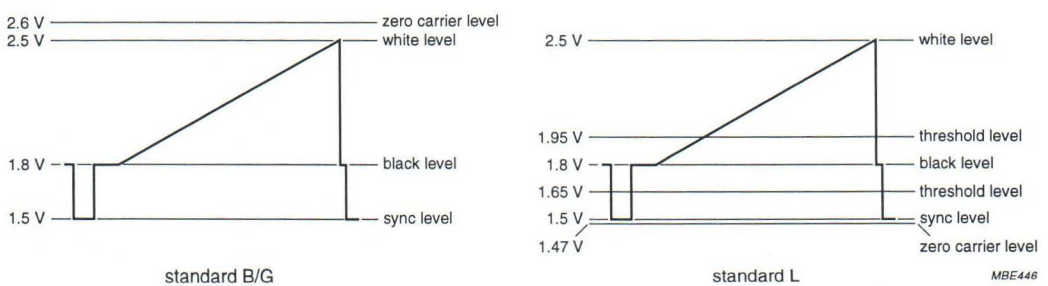


Fig.13 Typical video signal levels on output composite video (sound carrier OFF).

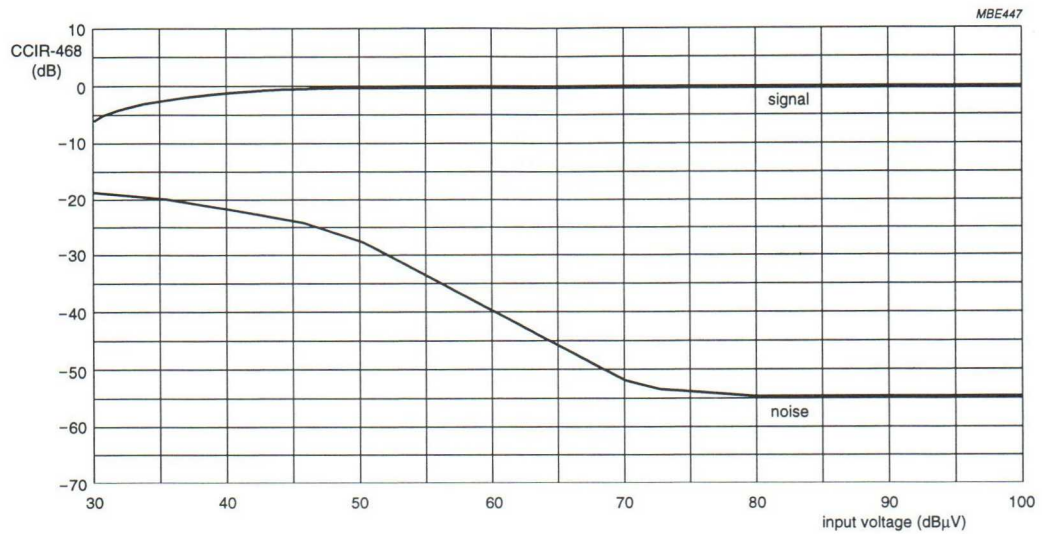


Fig.14 Typical audio sound-to-noise ratio as a function of input signal at AM standard.

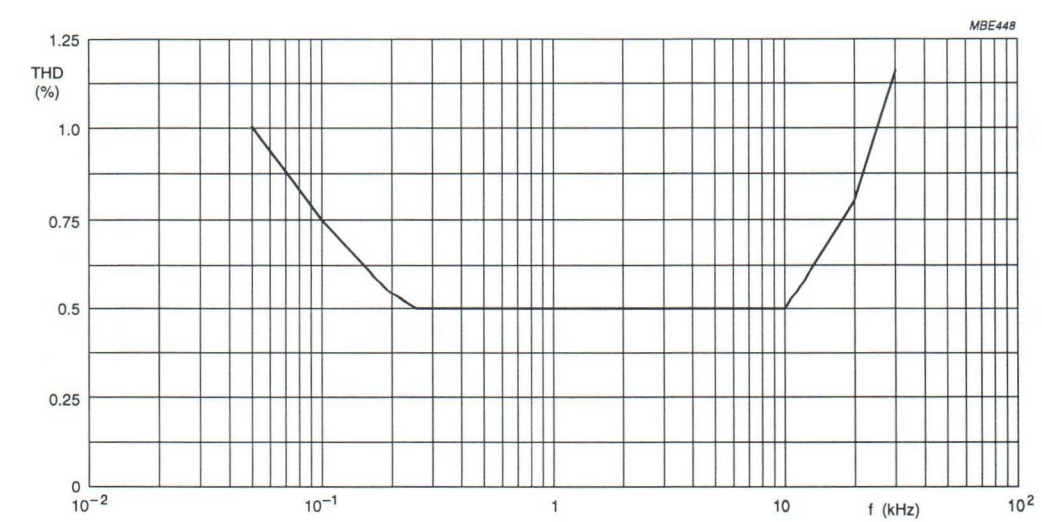


Fig.15 Typical total harmonic distortion as a function of input signal at AM standard.

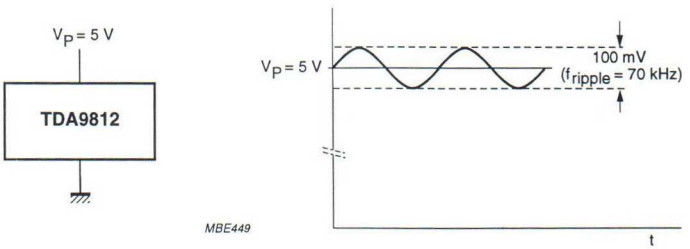


Fig.16 Ripple rejection condition.

INTERNAL CIRCUITRY

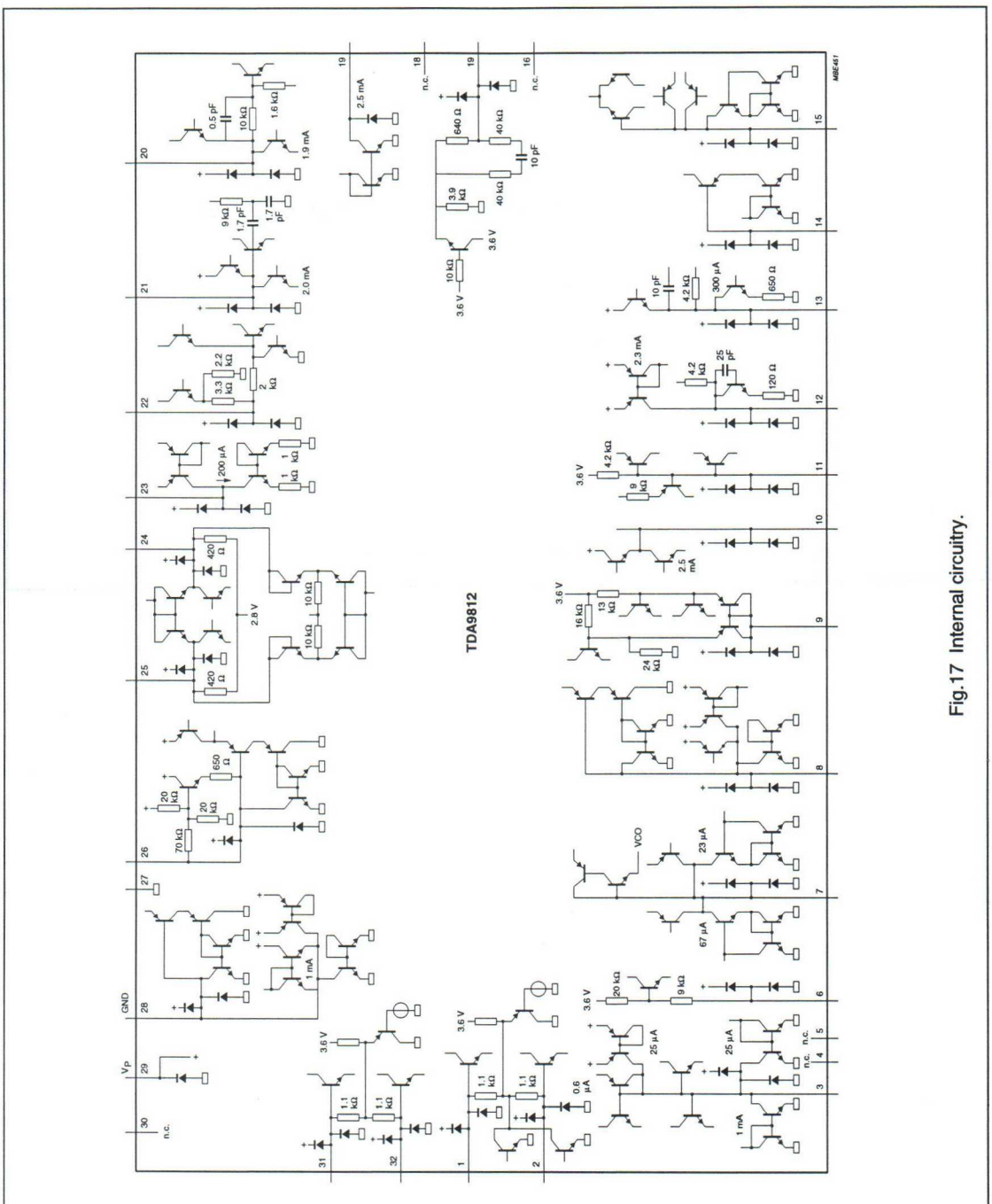


Fig.17 Internal circuitry.

APPLICATION INFORMATION

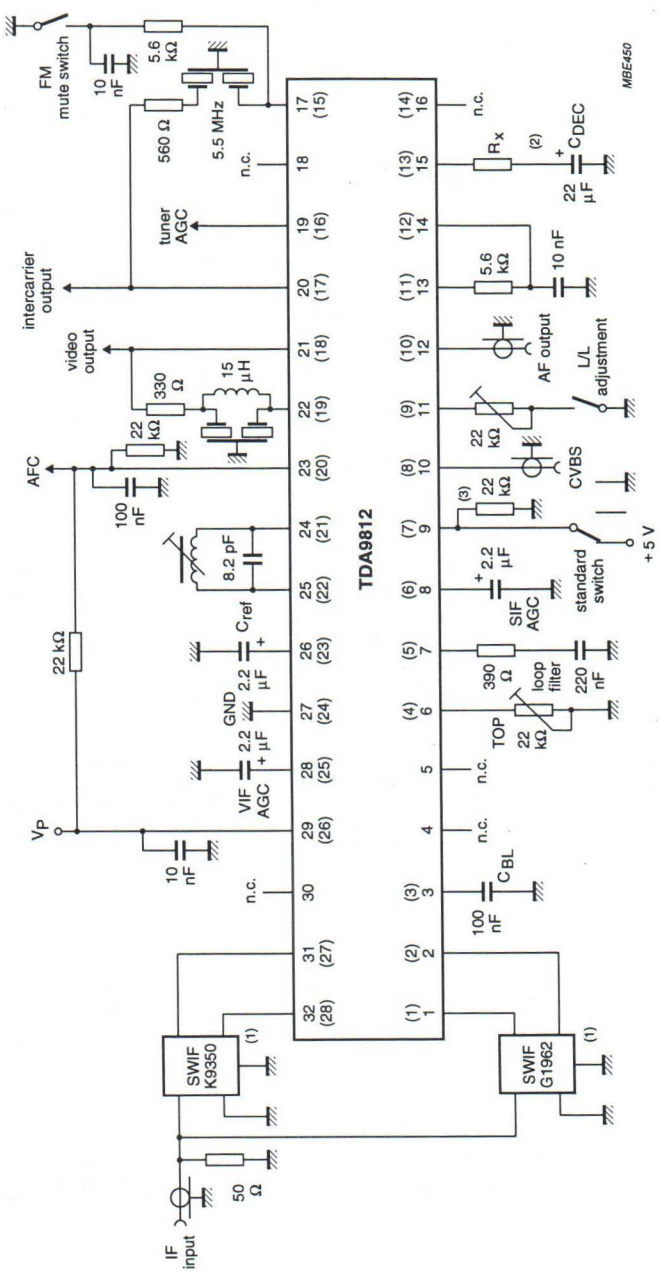


Fig.18 Application circuit (SO28 pinning in parenthesis).

(1) Depends on standard.
(2) See note 19 of the characteristics.
(3) Only required for external AGC mode.

Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator

TDA9814T

FEATURES

- 5 V positive supply voltage
- Gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L / L accent standard
- VCO frequency switchable between L and L accent (alignment externally) picture carrier frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for B/G and peak white detector for L (optional external AGC). Controlled reaction time for L
- Tuner AGC with adjustable take over point (TOP)
- AFC detector without extra reference circuit
- AC coupled limiter amplifier for sound intercarrier signal
- Two PLL-FM demodulators with high linearity, alignment-free
- SIF input for Single Reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; Single Reference QSS mode for high performance
- AM-demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9814T is an integrated circuit for multistandard vision IF signal processing and sound AM- and Dual-FM demodulation, with single reference QSS-IF in TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 26)	4.5	5	5.5	V
I_P	supply current	93	109	125	mA
$V_{i\,VIF}$	vision IF input signal sensitivity (RMS value; pins 1 and 2)	–	60	100	μV
$V_{o\,CVBS}$	CVBS output signal on pin 8 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 8	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio for video	56	60	–	dB
$\alpha_{1.1}$	intermodulation attenuation	58	64	–	dB
$\alpha_{3.3}$		58	64	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{i\,SIF}$	sound IF input signal sensitivity (RMS value; pins 27 and 28)	–	30	70	μV
V_o	audio output signal for FM standard B/G (RMS value; 54% modulation)	–	0.5	–	V
	audio output signal for AM standard L (RMS value; 54% modulation)	–	0.5	–	V
THD	total harmonic distortion; 54% modulation				
	for FM	–	0.15	–	%
	for AM	–	0.5	–	%
S/N (W)	weighted signal-to-noise ratio; 54% modulation				
	for FM	–	60	–	dB
	for AM	–	53	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9814T	28	SO	plastic	SOT136

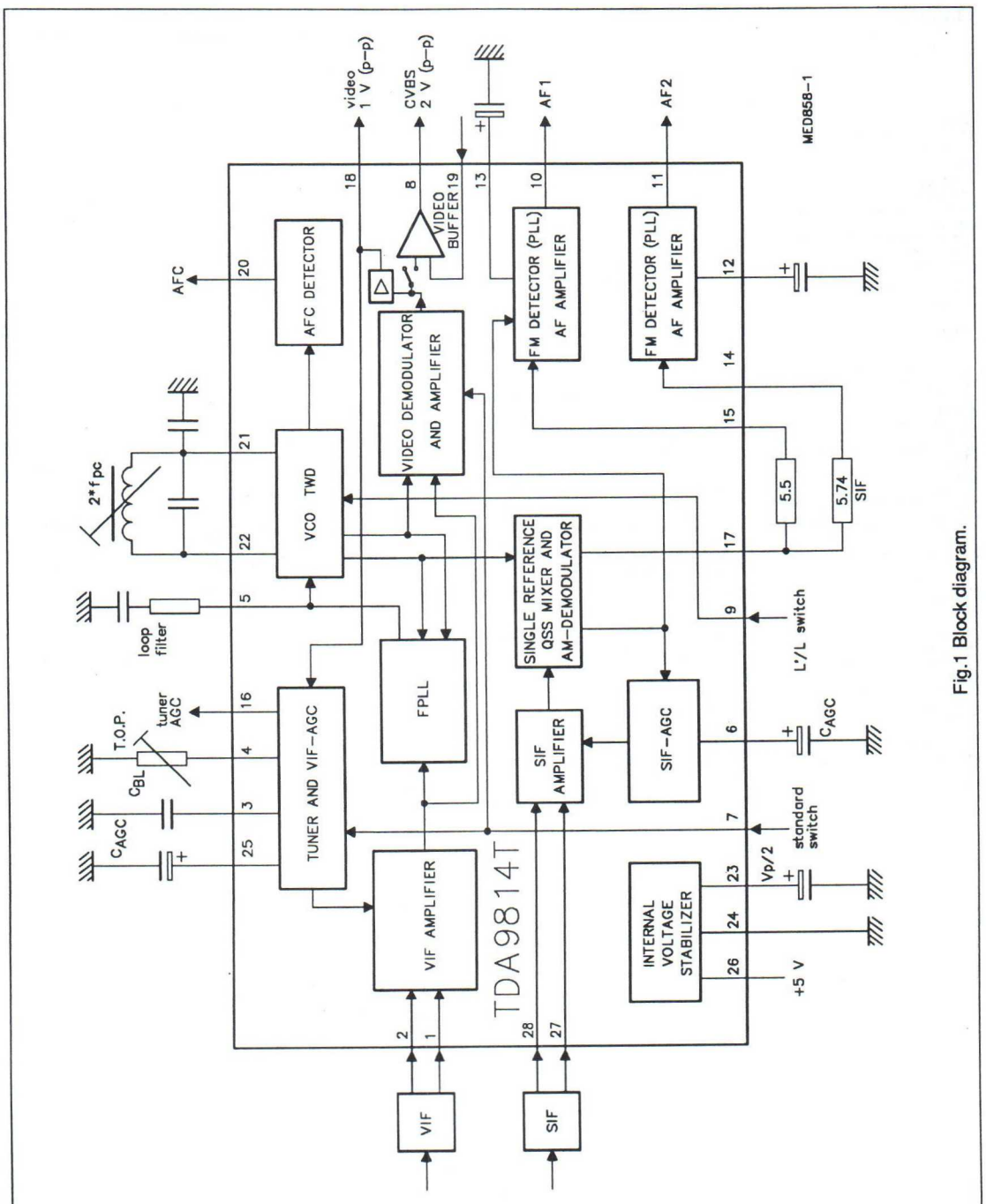


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF}$	1	VIF differential input signal
	2	
C_{BL}	3	black level detector
TADJ	4	tuner AGC takeover adjust (TOP)
T_{PLL}	5	PLL loop filter
C_{SAGC}	6	SIF AGC capacitor
STD	7	standard switch
$V_{o\ CVBS}$	8	CVBS output signal
LSWI	9	L / L accent switch
$V_{o\ AF1}$	10	audio frequency output 1
$V_{o\ AF2}$	11	audio frequency output 2
C_{AF2}	12	decoupling capacitor 2
C_{AF1}	13	decoupling capacitor 1
$V_{i\ FM2}$	14	sound intercarrier input 2
$V_{i\ FM1}$	15	sound intercarrier input 1
TAGC	16	tuner AGC output
$V_{o\ QSS}$	17	single reference QSS output
$V_{o\ vid}$	18	composite video output
$V_{i\ vid}$	19	video buffer input
AFC	20	AFC output
VCO1	21	VCO reference circuit for $2f_{PC}$
VCO2	22	
$C_{Vp/2}$	23	$V_P/2$ reference capacitor
GND	24	ground
C_{VAGC}	25	VIF AGC capacitor
V_P	26	positive supply voltage
$V_{i\ SIF}$	27	SIF differential input signal
	28	

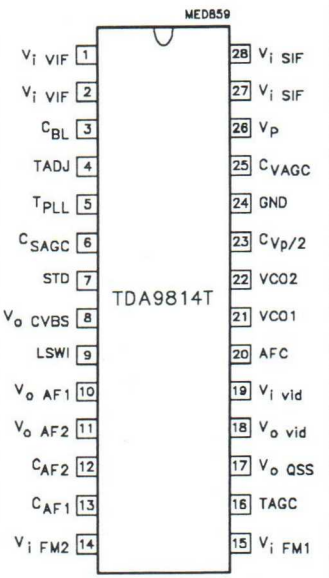


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network by means of emitter degeneration.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 16 (open-collector output). The tuner AGC take over point can be adjusted at pin 4. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.
The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black level detector voltage.

Frequency-Phase detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. Via the loop filter the DC current of either frequency detector or phase detector is converted into a DC voltage, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, travelling wave divider and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated varicaps. The control voltage required to tune the VCO from its free running frequency to actual double the PC frequency is generated by the frequency-phase detector and fed via the loop filter to the first varicap (FPLL). This control voltage is amplified and additionally converted into a current which represents the AFC output signal. Furthermore the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch pin 9. In this event the second varicap can be controlled by a variable resistor at pin 9 for setting the VCO centre frequency to the required L accent value. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a travelling wave divider (TWD) which generates two differential output signals with 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard. The demodulator output signal is fed via an integrated low pass for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal at pin 18 is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage (pin 8) delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

SIF amplifier and AGC

The sound IF amplifier consists of two AC coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF signals (average level of AM or FM carriers) at pin 27 and pin 28 and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. The SIF AGC reaction time is set to 'slow' in event of AM mode. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is also set to 'fast' controlled by the standard switch.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 17. With this system a high performance Hi-Fi stereo sound processing can be achieved.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low pass for attenuation of the carrier harmonics to the AF amplifier.

FM detectors

Each FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC coupled in order to minimize the DC offset and to save pins for DC decoupling.

The second limiter is extended with an additional level detector consisting of a rectifier and a comparator. By means of this the AF 2 signal is set to mute and the PLL VCO is switched off, if the intercarrier signal at pin 14 is below 1 mV RMS in order to avoid false identification of a stereo decoder. Note that noise at pin 14 disables the mute state (at low SIF input signal), but this will not lead to false identification. This 'auto-mute' function can be disabled by connecting a 5.6 kΩ resistor from pin 14 to $+V_P$ (see Fig.3).

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. By this way the FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

1) The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal.

An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.

2) The AF output amplifier (10 dB) provides the required output level by means of a rail-to-rail output stage. Furthermore this amplifier makes use of an input selector for switching to AM/FM or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer and $V_P/2$-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $V_P/2$ voltage has to be filtered via a low pass by using an external capacitor at pin 23 together with an integrated resistor ($f_g \sim 5$ Hz). For a fast setting to $V_P/2$ an internal start-up circuit is added.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 26) for a maximum chip temperature of +125 °C (note 1)	0	5.5	V
V_i	voltage at pins 1, 2, 6 to 11, 14, 15, 27 and 28	0	V_P	V
$t_{s\ max}$	maximum short-circuit time	–	10	s
V_{16}	tuner AGC output voltage	0	13.2	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
V_{ESD}	electrostatic handling (note 2)	–	±300	V

Notes to the Limiting Values

1. I_{26} = 125 mA; T_{amb} = +70 °C; $R_{th\ j\text{-}a}$ = 80 K/W.
2. Charge device model class B: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

The following characteristics apply for T_{amb} = +25 °C, V_P = 5 V, see Table 1 for input frequencies and level; input level $V_{i\ IF1,2}$ = 10 mV RMS value (sync-level for B/G, peak white level for L); video modulation DSB; residual carrier B/G: 10%; L = 3%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 26)						
V_{26}	supply voltage	note 1	4.5	5	5.5	V
I_{26}	supply current		93	109	125	mA
Vision IF amplifier (pins 1 and 2)		B/G standard				
$V_{i\ VIF}$	input sensitivity (RMS value)	−1 dB video at output	–	60	100	µV
	maximum input signal (RMS value)	+1 dB video at output	140	200	–	mV
$\Delta V_{o\ int.}$	internal IF amplitude difference between picture and sound carrier	within AGC range				
		B/G standard Δf = 5.5 MHz	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4	65	70	–	dB
R_i	input resistance (differential)	note 2	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{1/2}$	DC voltage		–	3.4	–	V
True synchronous video demodulator (note 3)						
f_{VCO}	maximum oscillator frequency for carrier regeneration	$f = 2f_{pc}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	note 4; I_{AFC} = 0	–	–	±20	ppm/K
$V_{o\ ref}$	oscillator swing at pins 21 and 22 (RMS value)	B/G and L standard	70	100	130	mV
		L accent standard	45	65	85	mV
Δf_{pc}	vision carrier capture range	B/G and L standard	±1.5	±2	–	MHz
		L accent standard;	±1.0	±1.3	–	MHz
	vision carrier (free running) accuracy	f_{pc} = 33.9 MHz; R_9 = 5.6 kΩ	–	±200	±400	kHz
	L accent alignment range	I_{AFC} = 0	±400	±600	–	kHz
t_{acqu}	acquisition time	note 5; BL = 60 kHz	–	–	30	ms
$V_{i\ VIF}$	VIF input signal sensitivity for PLL to be locked (RMS value; pins 1 and 2)	note 6; maximum IF gain	–	30	70	µV
I_{loop}	FPLL offset current at pin 5	note 7	–	–	±4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 18; sound carrier off)						
$V_{o\ video}$	output signal (peak-to-peak value)	see Fig.9	0.88	1.0	1.12	V
V_{18}	sync level	B/G and L	–	1.5	–	V
	zero carrier level	B/G	–	2.6	–	V
		L	–	1.47	–	V
	upper video clipping level		$V_P - 1.1$	$V_P - 1$	–	V
	lower video clipping level		–	0.3	0.4	V
R_{18}	output resistance	note 2	–	–	10	Ω
$I_{int\ 18}$	internal bias current for emitter-follower	DC	1.6	2.0	–	mA
I_{18}	maximum output sink current	DC and AC	1.0	–	–	mA
	maximum output source current		2.0	–	–	mA
B	–1 dB video bandwidth	B/G and L standard; $C_{18} < 50$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
	–3 dB video bandwidth		7	8	–	MHz
α_H	suppression of video signal harmonics	note 8a; $C_{18} < 50$ pF; $R_L > 1$ kΩ; AC load	35	40	–	dB
RR	ripple rejection at pin 18	see Fig.12; video signal: grey level;				
		B/G	32	35	–	dB
		L	26	30	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 8 and 19)						
R_{19}	input resistance	note 2	2.6	3.3	4.0	kΩ
C_{19}	input capacitance		1.4	2	3.0	pF
V_{19}	DC voltage at input		1.5	1.8	2.1	V
G_v	voltage gain	note 9; B/G and L	6.5	7	7.5	dB
V_{o8}	upper video clipping		3.9	4.0	–	V
	lower video clipping		–	1.0	1.1	V
R_8	output resistance	note 2	–	–	10	Ω
$I_{int\ 8}$	internal bias current for emitter-follower	DC	2.0	2.5	–	mA
I_{10}	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.4	–	–	mA
B	–1 dB video bandwidth	B/G, L; $C_8 < 20$ pF; $R_L > 1$ kΩ; AC load	8.4	11	–	MHz
	–3 dB video bandwidth		11	14	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to CVBS output (pin 8; 330 Ω between pins 18 and 19, sound carrier off)						
$V_{o\,CVBS}$	CVBS output signal on pin 8 (peak-to-peak value)	note 9	1.7	2.0	2.3	V
	CVBS output level	sync level (B/G)	–	1.35	–	V
		sync level (L)	–	1.35	–	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt in B/G standard	note 10; gain variation	–	–	1	%
	black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; note 10; gain variation	–	–	1.9	%
ΔG	differential gain	CCIR line 330	–	2	5	%
$\Delta\varphi$	differential phase		–	1	2	deg
B	–1 dB video bandwidth	B/G, L; $C_8 < 20$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
	–3 dB video bandwidth		7	8	–	MHz
S/N (W)	signal-to-noise ratio; weighted	see Fig.6 and note 11	56	60	–	dB
S/N	signal-to-noise ratio; unweighted		49	53	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.7 and note 12; f = 1.1 MHz	58	64	–	dB
	intermodulation at 'yellow'		60	66	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	see Fig.7 and note 12; f = 3.3 MHz	58	64	–	dB
	intermodulation at 'yellow'		59	65	–	dB
α_c	residual vision carrier (RMS value)	B/G and L standard; fundamental wave and harmonics	–	2	10	mV
α_H	suppression of video signal harmonics	note 8a	35	40	–	dB
	spurious elements	note 8b	40	–	–	dB
RR	ripple rejection at pin 8	see Fig.12; video signal: grey level; B/G	25	28	–	dB
VIF-AGC detector (pin 25)						
I_{25}	charging current	B/G and L; note 10	0.8	1	1.2	mA
	additional charging current	L in event of missing VITS pulses and no white video content	2.0	2.5	3.0	µA
	discharging current	B/G	16	20	24	µA
		normal mode L	240	300	360	nA
		fast mode L	32	40	48	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{resp}	AGC response to an increasing VIF step	B/G and L; note 13	–	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step	B/G	–	2.2	3.5	ms/dB
		fast mode L	–	1.1	1.8	ms/dB
		normal mode L; note 13	–	150	240	ms/dB
ΔIF	VIF amplitude step for activating fast AGC mode	L	–2	–6	–12	dB
V_3	threshold voltage level	see Fig.9				
	for additional charging current	L	–	1.95	–	V
	for fast mode L	L	–	1.65	–	V
Tuner AGC (pin 16)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1/2; R_{TOP} = 22 kΩ, I_{16} = 0.4 mA	–	2	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1/2; R_{TOP} = 0 Ω, I_{16} = 0.4 mA	50	100	–	mV
V_{16}	permissible output voltage	note 2; from external source	–	–	13.2	V
	saturation voltage	I_{16} = 1.7 mA	–	–	0.2	V
ΔV_{16}	variation of take over point by temperature	I_{16} = 0.4 mA	–	0.03	0.07	dB/K
I_{16}	sink current	see Fig.4				
		no tuner gain reduction; V_{16} = 12 V	–	–	2.5	µA
		V_{16} = 13.2 V	–	–	5	µA
		maximum tuner gain reduction	1.7	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 20; see Fig.8 and note 14)						
S	control steepness $\Delta I_{20} / \Delta f$	note 15; B/G and L	–0.5	–0.72	–1.0	µA/kHz
Δf_{IF}	frequency variation by temperature	note 5; I_{AFC} = 0	–	–	±20	ppm/K
V_{20}	output voltage upper limit	see Fig.8	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.6	V
I_{20}	output current source		160	200	240	µA
	output current sink		160	200	240	µA
$\Delta I_{20residual}$	residual video modulation current (peak-to-peak value)	B/G and L	–	20	30	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound IF amplifier (pins 27 and 28)						
$V_{i\,SIF}$	input sensitivity (RMS value)	FM-mode; –3 dB at intercarrier output pin 17	–	30	70	µV
		AM-mode; –3 dB at AF output pin 10	–	70	100	µV
	maximum input signal (RMS value)	FM-mode; +1 dB at intercarrier output pin 17	30	70	–	mV
		AM-mode; +1 dB at AF output pin 10	100	140	–	mV
G_{SIF}	SIF gain control range	see Fig.5, FM	60	67	–	dB
		see Fig.5, AM	60	67	–	dB
R_i	input resistance (differential)	note 2	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{27/28}$	DC voltage		–	3.4	–	V
$\alpha_{SIF/VIF}$	crosstalk attenuation between SIF and VIF input	pins 1/2 - 27/28; note 16	50	–	–	dB
SIF AGC detector (pin 6)						
I_6	charging current	FM mode	8	12	16	µA
		AM mode	0.8	1.2	1.6	µA
	discharging current	FM mode	8	12	16	µA
		normal mode AM	1	1.4	1.8	µA
		fast mode AM	60	85	110	µA
Single reference QSS intercarrier mixer (pin 17)		B/G				
V_o	IF intercarrier level (RMS value)	SC_1; sound carrier 2 off	75	100	125	mV
B	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
α_H	residual sound carrier (RMS value)	fundamental wave	–	2	–	mV
		harmonics	–	0.75	–	mV
R_{17}	output resistance	note 2	–	–	25	Ω
V_{17}	DC voltage		–	2.0	–	V
I_{int17}	internal bias current for emitter-follower	DC	1.5	1.9	–	mA
I_{17}	maximum output sink current	DC and AC	1.1	1.5	–	mA
	maximum output source current		3.0	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiter amplifier 1 (pin 15; note 17)						
$V_{i\,FM}$	input signal for lock-in		–	–	100	μV
	input signal (RMS value)	(S+N)/N = 40 dB	–	300	400	μV
	allowed input signal (RMS value)		200	–	–	mV
R_{15}	input resistance	note 2	480	600	720	Ω
V_{15}	DC voltage		–	2.8	–	V
Limiter amplifier 2 (pin 14; note 17)						
$V_{i\,FM}$	input signal for lock-in		–	–	100	μV
	input signal (RMS value)	(S+N)/N = 40 dB; PLL1 has to be in locked mode; auto mute off	–	300	400	μV
	allowed input signal (RMS value)		200	–	–	mV
	input signal for no auto mute; PLL enabled (RMS value)		0.7	1	1.5	mV
ΔV_{14}	hysteresis of level detector for auto mute		–3	–6	–8	dB
R_{14}	input resistance	note 2	480	600	720	Ω
V_{14}	DC voltage		–	2.0	–	V
FM-PLL demodulators						
$f_{i\,FM}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
	holding range of PLL	upper limit	9.0	–	–	MHz
		lower limit	–	–	3.5	MHz
t_{acqu}	acquisition time		–	–	4	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM operation (standard B/G) (pins 10 and 11; note 17a)						
$V_{o\ AF10,11}$	AF output signal (RMS value)	27 kHz (= 54% FM deviation); see Fig.3 and note 18				
		$R_{x,y}$ = 470 Ω	200	250	300	mV
		$R_{x,y}$ = 0 Ω	400	500	600	mV
	clipping level	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 18	–	–	±53	kHz
ΔV_o	temperature drift of AF output signal		–	3	7	10^{-3}dB/K
ΔV_o	difference between both AF output signals		–	–	±1.0	dB
$V_{12,13}$	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 19	1.2	–	3.0	V
$R_{10,11}$	output resistance	note 2	–	–	100	Ω
$V_{10,11}$	DC voltage	tracked with supply voltage	–	$V_P/2$	–	V
$I_{10,11}$	maximum sink and source current	DC and AC	–	–	1.1	mA
B	–3 dB audio frequency bandwidth		100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%
S/N(W)	signal-to-noise ratio; weighted	FM-PLL only; with 50 µs de-emphasis; 27 kHz (= 54% FM deviation); CCIR468-4	55	60	–	dB
V_{sc}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
α_{AM}	AM suppression	with 50 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (= 54% FM deviation)	46	50	–	dB
$\alpha_{10/11}$	crosstalk attenuation between AF outputs	f = 50 Hz to 12.5 kHz; $R_L \geq 10$ kΩ; C_L = 1 nF	66	70	–	dB
$\alpha_{10,11}$	mute attenuation of AF1 and AF2 signal	pins 10 and 11; B/G and L standard	70	80	–	dB
$\Delta V_{10,11}$	DC jump of AF output terminals for switching AF output to mute state and vice versa	both FM PLLs have to be in locked mode; note 20	–	±50	±150	mV
RR	ripple rejection at pins 10 and 11	see Fig.12; $R_x = R_y$ = 0 Ω	26	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single reference QSS AF performance for FM operation (standard B/G) notes 21 and 22 picture to sound carrier ratio: PC/SC_1 = 13 dB; PC/SC_2 = 20 dB; (transmitter) sound attenuation of VIF SAW filter: minimum 33 dB						
measurement condition: PC/SC_1 ratio at pins 1 and 2; note 23			40	–	–	dB
S/N(W)	signal-to-noise ratio; weighted	27 kHz (= 54% FM deviation) CCIR 468-4				
	black picture	SC_1 / SC_2	53/48	58/55	–	dB
	white picture	SC_1 / SC_2	52/47	55/53	–	dB
	6 kHz sine wave (black to white modulation)	SC_1 / SC_2	44/42	48/46	–	dB
	250 kHz square wave (black to white modulation)	SC_1 / SC_2; note 24	48/40	53/45	–	dB
	sound carrier subharmonics	SC_1 / SC_2: 2.75 MHz ± 3 kHz	45/44	51/50	–	dB
		SC_1 / SC_2: 2.87 MHz ± 3 kHz	46/45	52/51	–	dB
AM operation (standard L) pin 10; note 25						
$V_{o\,AF}$	AF output signal (RMS value)	m = 54%	400	500	600	mV
THD	total harmonic distortion	m = 54%; see Fig.11	–	0.5	1.0	%
B	–3 dB AF bandwidth		100	125	–	kHz
S/N(W)	signal-to-noise ratio; weighted	CCIR 468-4; see Fig.10	47	53	–	dB
V_{10}	DC potential	tracked with supply voltage	–	$V_P/2$	–	V
RR	ripple rejection at pin 10	see Fig.12	22	25	–	dB
Standard switch (pin 7)						
V_7	DC potential for preferred settings; for other settings see Table 2					
V_{IH}	input voltage for negative standard	note 26; B/G	2.8	–	V_P	V
V_{IT}	input voltage for negative standard	negative AGC OFF	1.3	–	2.3	V
V_{IL}	input voltage for positive standard	L	0	–	0.8	V
I_{IL}	LOW level input current	V_7 = 0 V	200	250	300	µA
L accent switch (pin 9)						
V_9	DC potential for standard L VCO frequency switching					
	for L standard	note 26	2.8	–	V_P	V
	for L accent standard and alignment		–	–	2.0	V
I_{IL}	LOW level input current	V_9 = 0 V	160	200	240	µA

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as an application information for designing the television receiver.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with sync level within gain control range). Resonance circuit of VCO: $Q_0 > 50$; C_{ext} = 6.8 pF; $C_{int} \approx 9$ pF (loop voltage approximately 2.7 V).
4. Temperature coefficient of external LC-circuit is equal to zero.
5. $V_{i\,IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ signal for nominal video signal.

7. Offset current measured between pin 5 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at VIF input (pins 1 and 2) and VIF amplifier gain at minimum ($V_{25} = V_P$). Due to sample and hold mode of the FPLL in L standard, the leakage current of the loop filter capacitor (C = 220 nF) should not exceed 500 nA.
8. Measurements taken with SAW filter G3962 (sound carrier suppression: 40 dB); loop bandwidth BL = 60 kHz; a. modulation VSB, $f_{video} > 0.5$ MHz; b. f_{video} = 10 kHz to 10 MHz.
9. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 18 to pin 19).
10. The leakage current of the AGC capacitor should not exceed 1 μA at B/G standard respectively 10 nA current at L standard. Larger currents will increase the tilt.
11. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 8). B = 5 MHz weighted in accordance with CCIR 567.
12. The intermodulation figures are defined:
    $\alpha_{1.1}$ = 20 log (V_0 at 4.4 MHz / V_0 at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal
    $\alpha_{3.3}$ = 20 log (V_0 at 4.4 MHz / V_0 at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
13. Response speed valid for a VIF input level range of 200 μV up to 70 mV.
14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.8. The AFC-steepness can be changed by the resistors at pin 20.
15. Depending on the ratio $\Delta C / C_0$ of the LC resonant circuit of VCO (Q > 50; see note 3; $C_0 = C_{int} + C_{ext}$).
16. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 38.9 MHz.
17. Input level for second IF from an external generator with 50 Ω source impedance. AC coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pin 6 and pin 25 has to be connected to positive supply voltage. S/N and THD measurements are taken at 50 μs de-emphasis. The not tested FM-PLL has to be locked to an unmodulated carrier.
    a. second IF input level 10 mV RMS.
18. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV RMS ($R_x = R_y = 0$ Ω; see Fig.3). By using $R_x = R_y$ = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS) and adapted to the stereo decoder family TDA9840. For handling an FM deviation of more than 53 kHz the AF output signals have to be reduced by using R_x and R_y in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended ($R_x = R_y$ = 470 Ω).
19. The leakage current of the decoupling capacitor (2.2 μF) should not exceed 1 μA.
20. In the event of activated auto mute state the second FM-PLL oscillator is switched off, if the input signal at pin 14 is missing or too weak (see Fig.3). In the event of switching the second FM-PLL oscillator on by the auto mute stage an increased DC jump is the consequence. Note, that noise at pin 14 disables the mute state (at low SIF input signal), but this will not lead to false identification of the used stereo decoder family TDA9840.
21. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    - Incidental phase modulation for black-to-white jump less than 0.5 degree.
    - QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sinewave black-to-white video modulation.
22. Measurements are taken with SAW filter G3962 (Siemens) for vision IF (supressed sound carrier) and G9350 (Siemens) for sound IF (supressed picture carrier). Input level $V_{i\,SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
23. The PC/SC_1 ratio is calculated as the addition of TV transmitter PC/SC_1 ratio and SAW filter PC/SC_1 ratio. This PC/SC_1 ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC_1 ratio will change these values.
24. The used loop filter is related to Fig.3 but with an additional capacitor of 6.8 nF in parallel. Without this capacitor the S/N value will decrease by typically 5 dB.
25. Measurements are taken with SAW filter K9350 (Siemens) for sound IF (supressed picture carrier).
26. The input voltage has to be V > 2.8 V, or open-circuit.

Table 1 Input frequencies and carrier ratios.

		B/G STANDARD	L STANDARD	L ACCENT STANDARD	UNIT
picture carrier	f_{pc}	38.9	38.9	33.9	MHz
sound carrier	f_{sc1}	33.4	32.4	40.4	MHz
	f_{sc2}	33.158	–	–	MHz
picture to sound carrier ratio	SC_1	13	10	10	dB
	SC_2	20	–	–	dB

Table 2 Switch logic.

STANDARD SWITCH (pin 7)	SELECTED STANDARD	VIDEO POLARITY	FM-PLL		AF-AMPLIFIER	
			1	2	1	2
2.8 V to V_P	B/G	negative	on	on	FM	FM
1.3 V to 2.3 V	B/G, with external VIF AGC	negative	on	on	FM	FM
0 to 0.8 V	L	positive	off	off	AM	mute

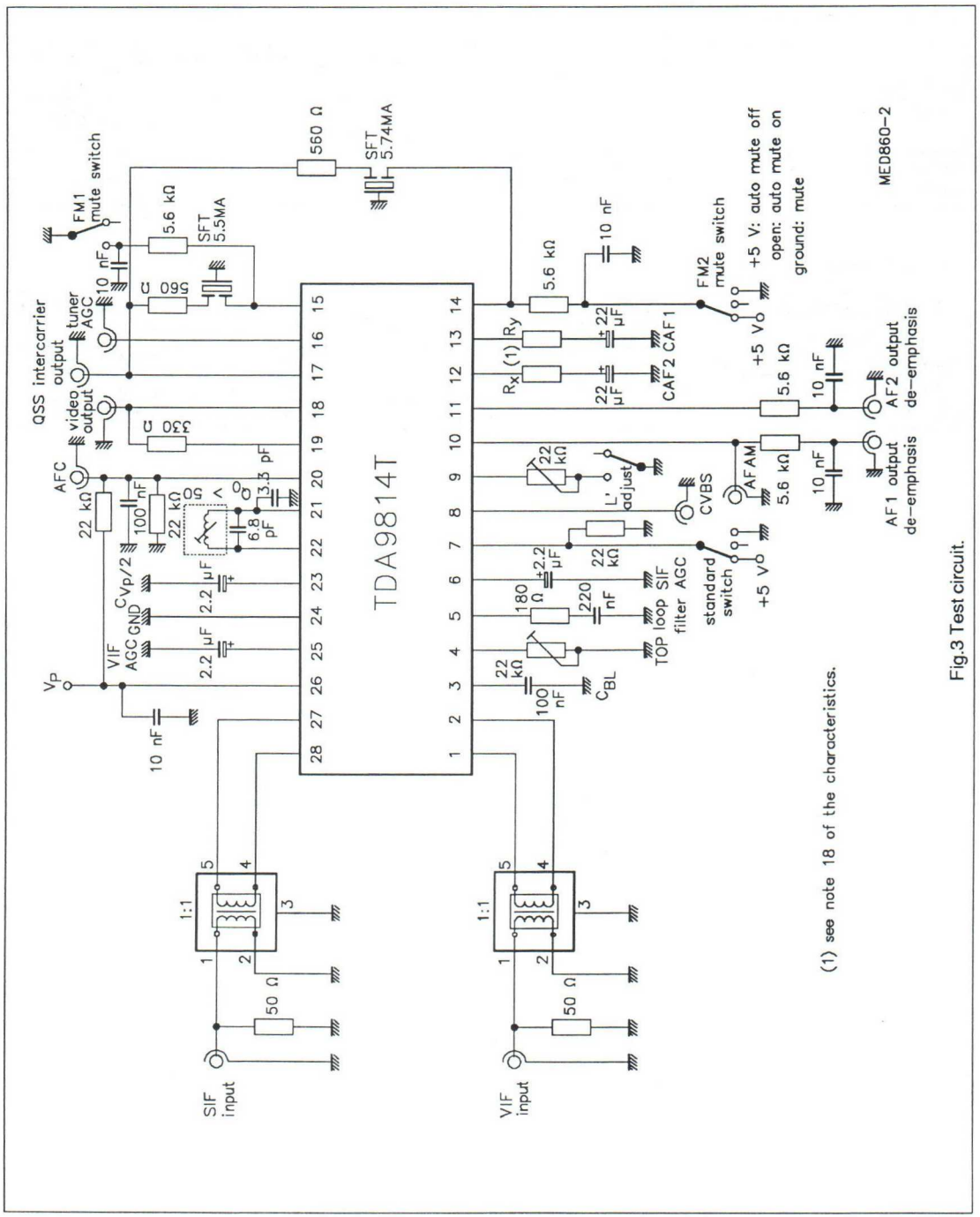


Fig.3 Test circuit.

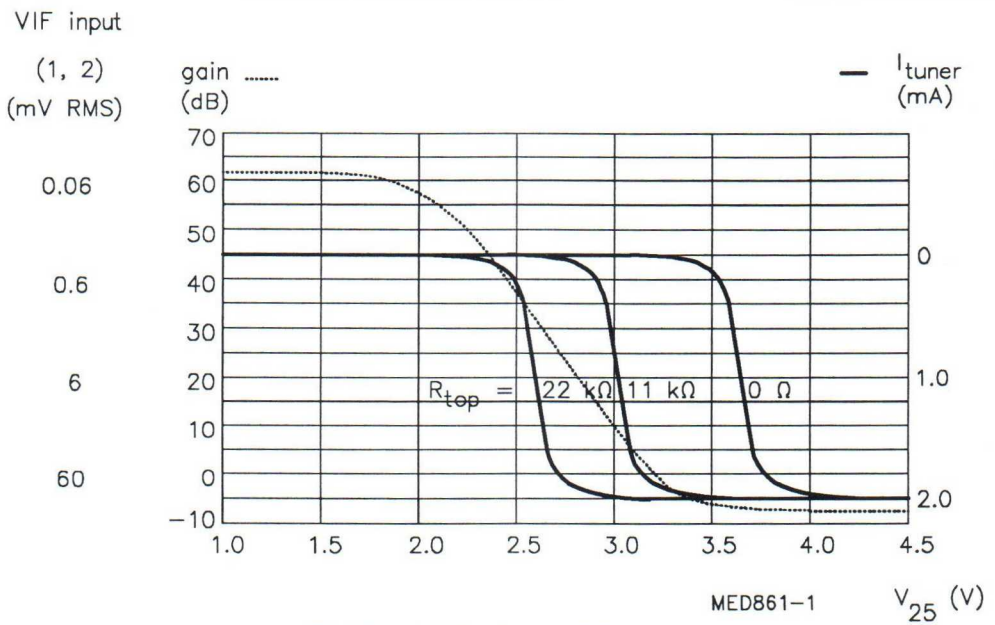


Fig.4 Typical VIF and tuner AGC characteristic.

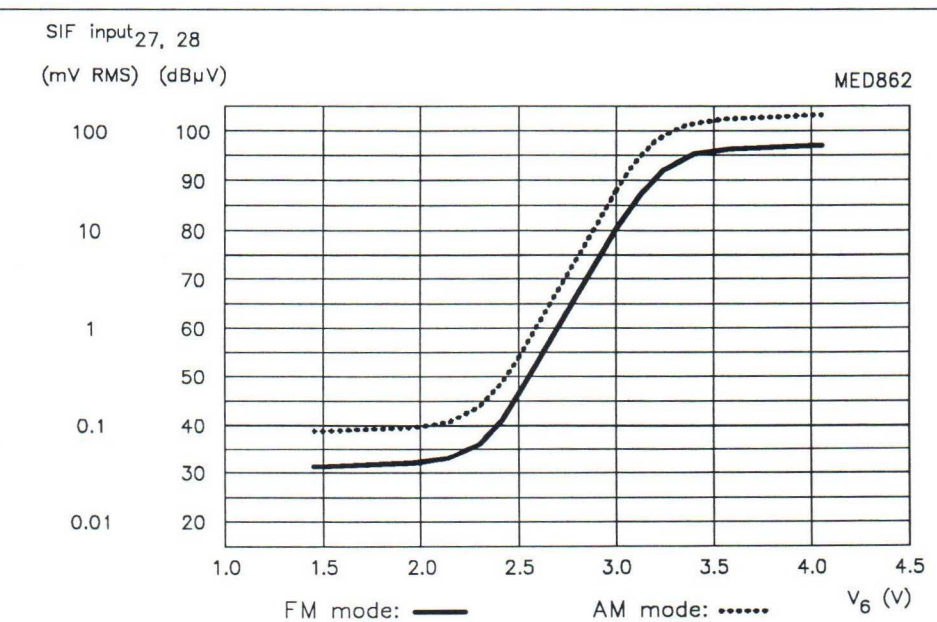


Fig.5 Typical SIF AGC characteristic.

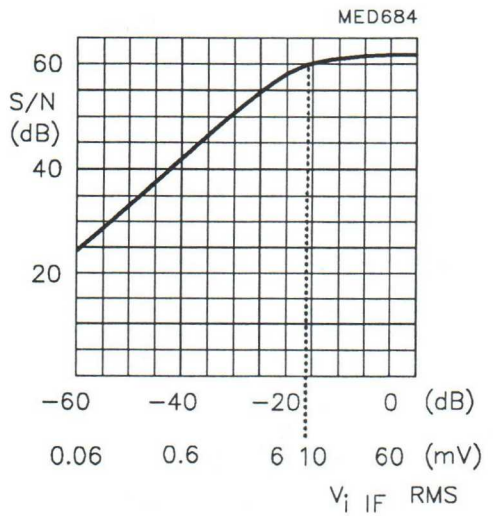
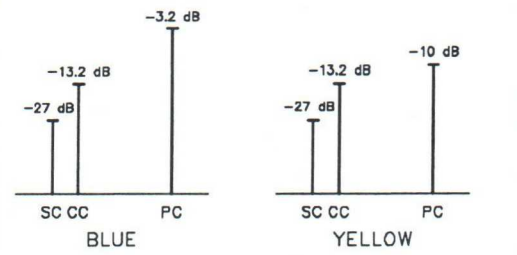


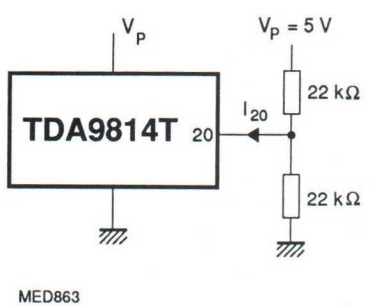
Fig.6 Typical S/N as a function of IF input voltage.



SC = sound carrier
CC = chrominance carrier
PC = picture carrier
all with respect to sync level

The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SWIF G1956).

Fig.7 Input signal conditions.



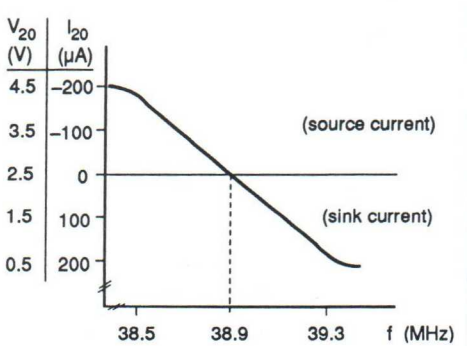


Fig.8 Measurement conditions and typical AFC characteristic.

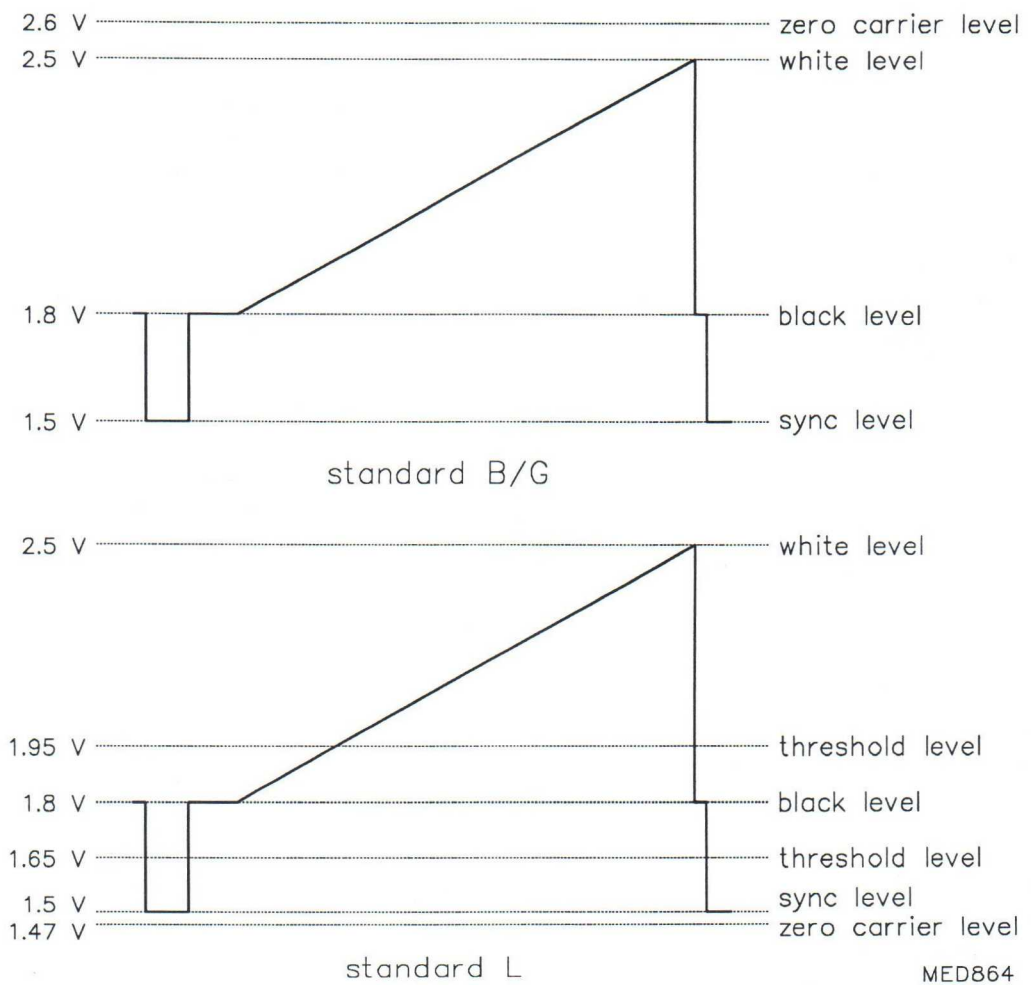


Fig.9 Typical video signal levels on output pin 18 (sound carrier off).

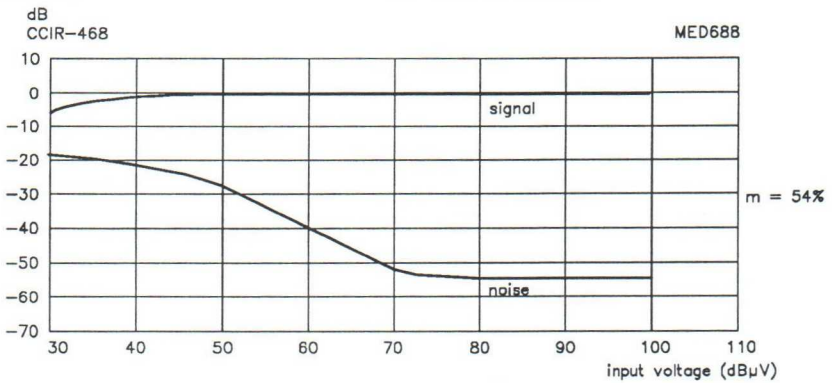


Fig.10 Typical audio S/N as a function of input signal at AM standard.

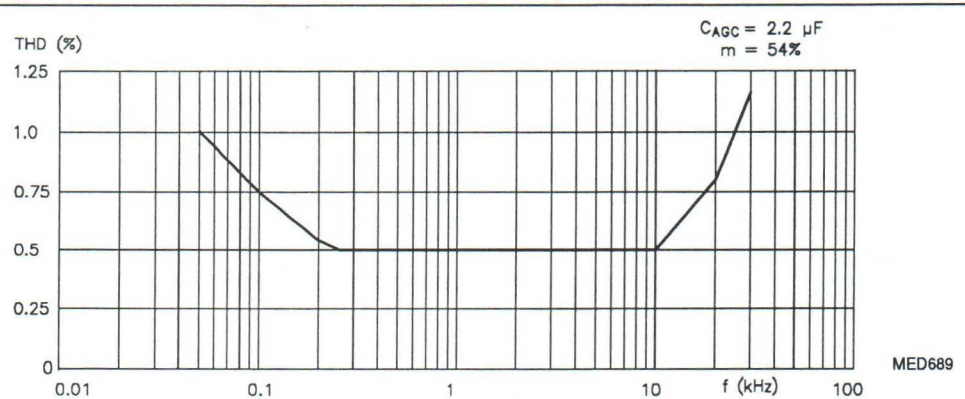


Fig.11 Typical THD as a function of audio frequency at AM standard.

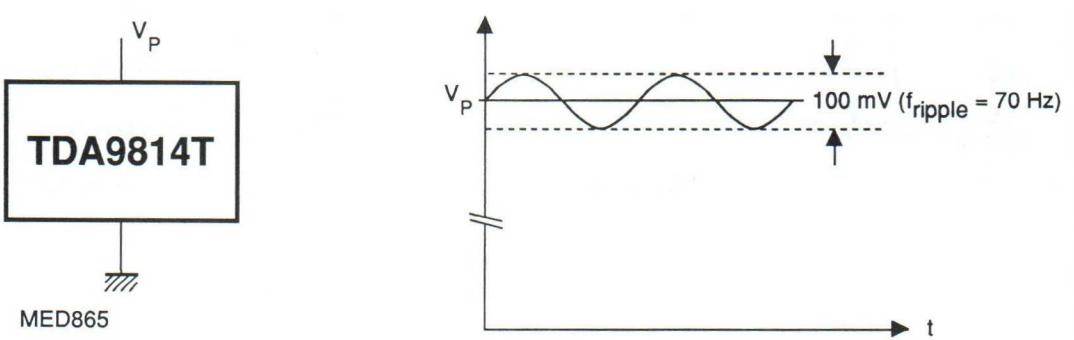
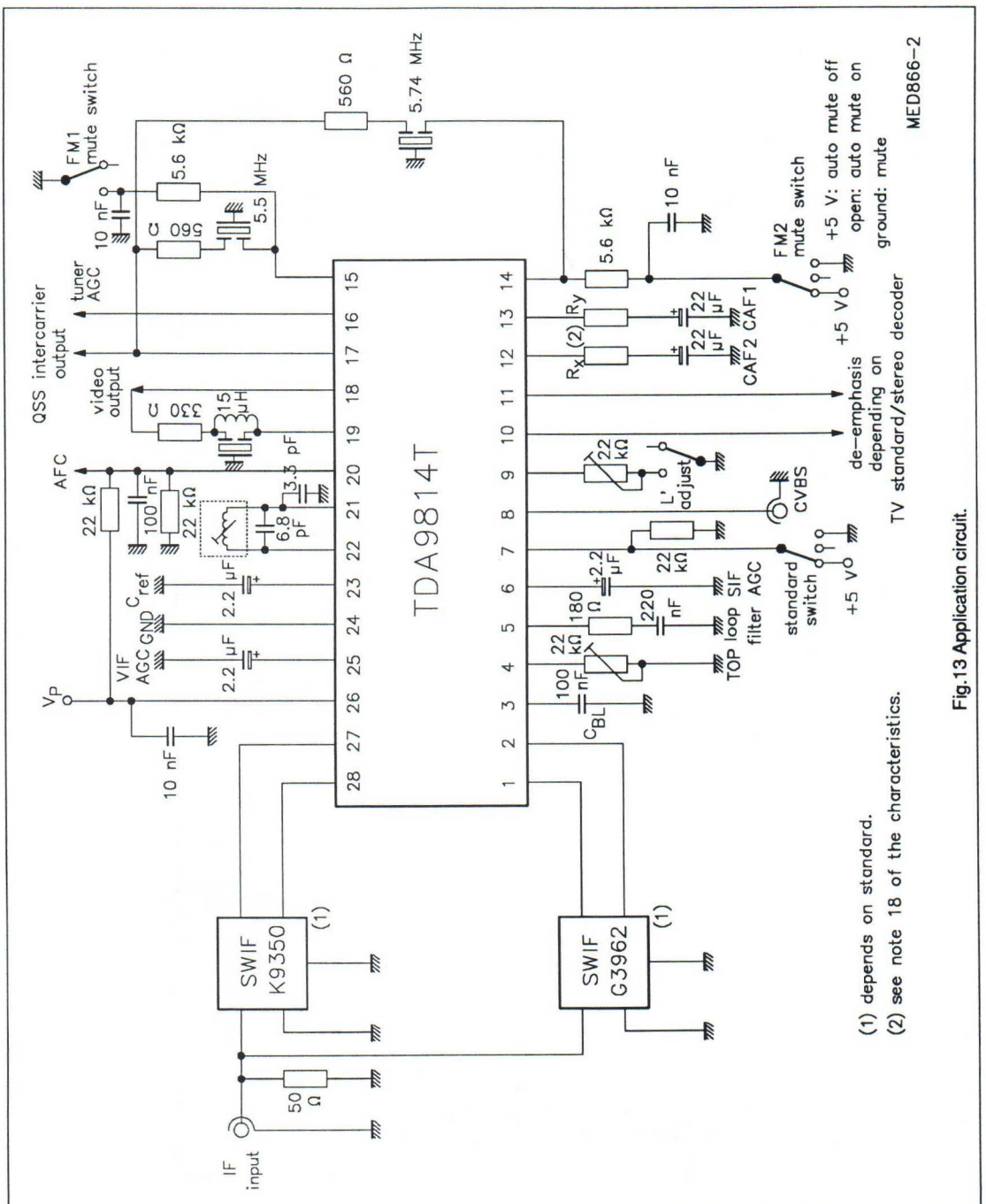


Fig.12 Ripple rejection condition.



(1) depends on standard.
(2) see note 18 of the characteristics.

Fig.13 Application circuit.

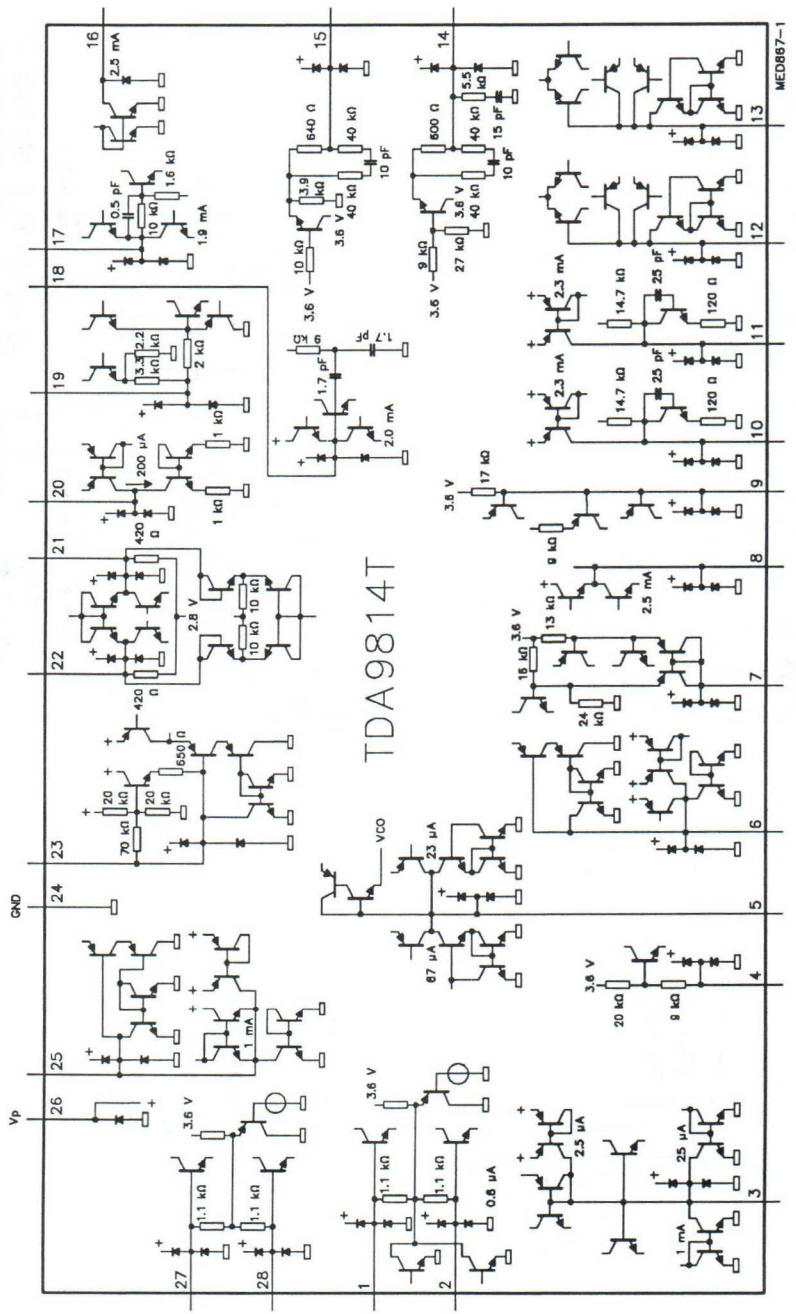


Fig.14 Internal circuits.

Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator

TDA9815

FEATURES

- 5 V positive supply voltage
- Two switched VIF inputs, gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L / L accent standard
- VCO frequency switchable between L and L accent (alignment externally) picture carrier frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for B/G, peak white detector for L and peak level for MAC (optional external AGC). Controlled reaction time for L and MAC
- Tuner AGC with adjustable take over point (TOP)
- AFC detector without extra reference circuit
- AC coupled limiter amplifier for sound intercarrier signal with input switch for additional FM signal
- Two PLL-FM demodulators with high linearity, alignment-free
- SIF input for Single Reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; Single Reference QSS mixer able to operate in high performance Single Reference QSS mode
- AM-demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9815 is an integrated circuit for multistandard vision IF signal processing (inclusive MAC) and sound AM- and Dual-FM demodulation, with single reference QSS-IF in TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 29)	4.5	5	5.5	V
I_P	supply current	93	109	125	mA
$V_{i\,VIF}$	vision IF input signal sensitivity (RMS value; pins 1, 2, 4 and 5)	–	60	100	μV
$V_{o\,CVBS}$	CVBS output signal on pin 10 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 10	7	8	–	MHz
B_{MAC}	–3 dB video bandwidth on pin 10	11	14	–	MHz
S/N (W)	weighted signal-to-noise ratio for video	56	60	–	dB
$\alpha_{1.1}$	intermodulation attenuation	58	64	–	dB
$\alpha_{3.3}$		58	64	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{i\,SIF}$	sound IF input signal sensitivity (RMS value; pins 31 and 32)	–	30	70	μV
V_o	audio output signal for FM standard B/G (RMS value; 54% modulation)	–	0.5	–	V
	audio output signal for AM standard L (RMS value; 54% modulation)	–	0.5	–	V
THD	total harmonic distortion; 54% modulation				
	for FM	–	0.15	–	%
	for AM	–	0.5	–	%
S/N (W)	weighted signal-to-noise ratio; 54% modulation				
	for FM	–	60	–	dB
	for AM	–	53	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9815	32	SDIL	plastic	SOT232

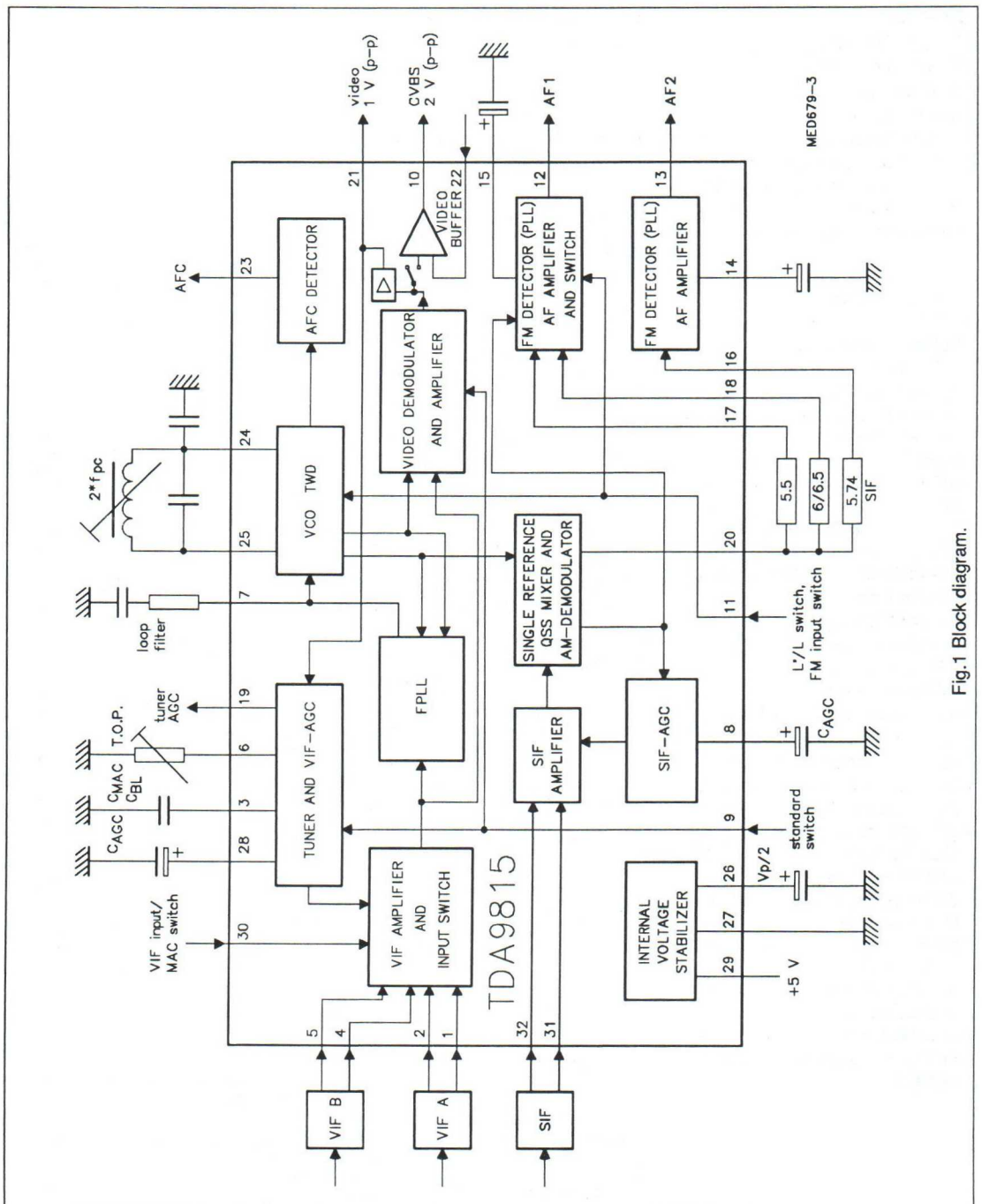


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF}$	1	VIF differential input signal A
	2	
$C_{BL/MAC}$	3	black level detector / MAC capacitor
$V_{i\ VIF}$	4	VIF differential input signal B
	5	
TADJ	6	tuner AGC takeover adjust (TOP)
T_{PLL}	7	PLL loop filter
C_{SAGC}	8	SIF AGC capacitor
STD	9	standard switch
$V_{o\ CVBS}$	10	CVBS output signal
FMLSWI	11	FM input select and L / L accent switch
$V_{o\ AF1}$	12	audio frequency output 1
$V_{o\ AF2}$	13	audio frequency output 2
C_{AF2}	14	decoupling capacitor 2
C_{AF1}	15	decoupling capacitor 1
$V_{i\ FM2}$	16	sound intercarrier input 2
$V_{i\ FM1}$	17	sound intercarrier input 1
$V_{i\ FM3}$	18	sound intercarrier input 3
TAGC	19	tuner AGC output
$V_{o\ QSS}$	20	single reference QSS output
$V_{o\ vid}$	21	composite video output
$V_{i\ vid}$	22	video buffer input
AFC	23	AFC output
VCO1	24	VCO reference circuit for $2f_{PC}$
VCO2	25	
$C_{Vp/2}$	26	$V_P/2$ reference capacitor
GND	27	ground
C_{VAGC}	28	VIF AGC capacitor
V_P	29	positive supply voltage
INSWI	30	VIF input switch
$V_{i\ SIF}$	31	SIF differential input signal
	32	

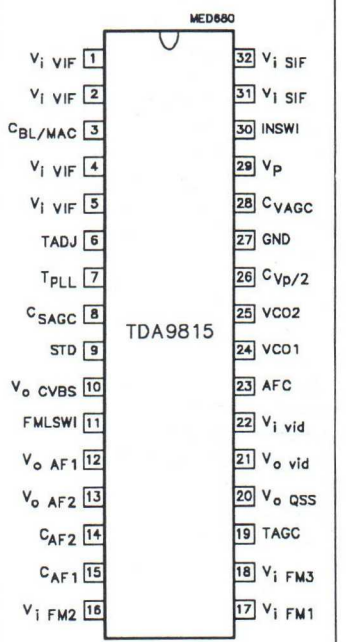


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier and input switch

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network by means of emitter degeneration. The first differential stage is extended by two pairs of emitter followers to provide two IF input channels. The VIF input can be selected by pin 30.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 19 (open-collector output). The tuner AGC take over point can be adjusted at pin 6. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.
The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive (or MAC) modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black level detector voltage.

Frequency-Phase detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. Via the loop filter the DC current of either frequency detector or phase detector is converted into a DC voltage, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, travelling wave divider and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated varicaps. The control voltage required to tune the VCO from its free running frequency to actual double the PC frequency is generated by the frequency-phase detector and fed via the loop filter to the first varicap (FPLL). This control voltage is amplified and additionally converted into a current which represents the AFC output signal. Furthermore the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the FM input and L accent switch pin 11. In this event the second varicap can be controlled by a variable resistor at pin 11 for setting the VCO centre frequency to the required L accent value. At centre frequency the AFC output current is equal to zero.
The oscillator signal is divided-by-two with a travelling wave divider (TWD) which generates two differential output signals with 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard. The demodulator output signal is fed via an integrated low pass for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal at pin 21 is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage (pin 10) delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.
For MAC standard a second buffer amplifier with 6 dB gain is used. This buffer amplifier is selected by the standard switch (pin 9).

SIF amplifier and AGC

The sound IF amplifier consists of two AC coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF signals (average level of AM or FM carriers) at pin 31 and pin 32 and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. The SIF AGC reaction time is set to 'slow' in event of AM mode. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is also set to 'fast' controlled by the standard switch.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high pass for attenuation of the video signal components to the output pin 20. With this system a high performance Hi-Fi stereo sound processing can be achieved.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low pass for attenuation of the carrier harmonics to the AF amplifier.

FM detectors

Each FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC coupled in order to minimize the DC offset and to save pins for DC decoupling.

At the input of one limiter a signal switch is available for selecting one of the two intercarrier signals. Controlled by the voltage at pin 11, either the input pin 17 or pin 18 is active for handling different intercarrier frequencies.

The other limiter is extended with an additional level detector consisting of a rectifier and a comparator. By means of this the AF 2 signal is set to mute and the PLL VCO is switched off, if the intercarrier signal at pin 16 is below 1 mV RMS in order to avoid false identification of a stereo decoder. Note that noise at pin 16 disables the mute state (at low SIF input signal), but this will not lead to false identification. This 'auto-mute' function can be disabled by connecting a 5.6 kΩ resistor from pin 16 to +V_P (see Fig.3).

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. By this way the FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

1) The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal.

An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.

2) The AF output amplifier (10 dB) provides the required output level by means of a rail-to-rail output stage. Furthermore this amplifier makes use of an input selector for switching to AM/FM or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer and $V_P/2$-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $V_P/2$ voltage has to be filtered via a low pass by using an external capacitor at pin 26 together with an integrated resistor ($f_g \approx 5$ Hz). For a fast setting to $V_P/2$ an internal start-up circuit is added.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 29) for a maximum chip temperature of +120 °C (note 1)	0	6.5	V
V_i	voltage at pins 1, 2, 4, 5, 8 to 13, 16 to 18, 31 and 32	0	V_P	V
$t_{s\ max}$	maximum short-circuit time	–	10	s
V_{19}	tuner AGC output voltage	0	13.2	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–20	+70	°C
V_{ESD}	electrostatic handling (note 2)	–	±300	V

Notes to the Limiting Values

1. I_{29} = 125 mA; T_{amb} = +70 °C; $R_{th\ j\text{-}a}$ = 60 K/W.
2. Charge device model class B: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	60 K/W

CHARACTERISTICS

The following characteristics apply for T_{amb} = +25 °C, V_P = 5 V, see Table 1 for input frequencies and picture to sound carrier ratios; input level $V_{i\ IF1,2/4,5}$ = 10 mV RMS value (sync-level for B/G, peak white level for L, peak level for MAC); video modulation DSB; residual carrier B/G and MAC: 10%; L = 3%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 29)						
V_{29}	supply voltage	note 1	4.5	5	5.5	V
I_{29}	supply current		93	109	125	mA
Vision IF amplifier (pins 1, 2, 4 and 5)		B/G standard				
$V_{i\ VIF}$	input sensitivity (RMS value)	−1 dB video at output	–	60	100	µV
	maximum input signal (RMS value)	+1 dB video at output	140	200	–	mV
$\Delta V_{o\ int.}$	internal IF amplitude difference between picture and sound carrier; MAC: bandedge	within AGC range				
		B/G-standard Δf = 5.5 MHz	–	0.7	1	dB
		MAC-standard Δf = 8.4 MHz	–	1.0	1.3	dB
G_{IF}	IF gain control range	see Fig.4	65	70	–	dB
R_i	input resistance (differential)	note 2; activated input	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{1/2,4/5}$	DC voltage		–	3.4	–	V
R_i	input resistance to ground	note 2; not activated input	–	1.1	–	kΩ
$V_{1/2,4/5}$	DC voltage		–	0.2	–	V
$\alpha_{i\ IF}$	crosstalk attenuation of IF input switch at pins 1, 2, 4 and 5	notes 2 and 3	55	60	–	dB
True synchronous video demodulator (note 4)						
f_{VCO}	maximum oscillator frequency for carrier regeneration	$f = 2f_{pc}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	note 5; I_{AFC} = 0	–	–	±20	ppm/K
$V_{0\ ref}$	oscillator swing at pins 24 and 25 (RMS value)	B/G, L, MAC standard	70	100	130	mV
		L accent standard	45	65	85	mV
Δf_{pc}	vision carrier capture range	B/G, L, MAC standard	±1.5	±2	–	MHz
		L accent standard	±1.0	±1.3	–	MHz
	vision carrier (free running) accuracy	f_{pc} = 33.9 MHz; R_{11} = 5.6 kΩ	–	±200	±400	kHz
	L accent alignment range	I_{AFC} = 0	±400	±600	–	kHz
t_{acqu}	acquisition time	note 6; BL = 60 kHz	–	–	30	ms
$V_{i\ VIF}$	VIF input signal sensitivity for PLL to be locked (RMS value; pins 1, 2, 4 and 5)	note 7; maximum IF gain	–	30	70	µV
I_{loop}	FPLL offset current at pin 7	note 8	–	–	±4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 21; sound carrier off)						
$V_{o\ video}$	output signal (peak-to-peak value)	see Fig.9	0.88	1.0	1.12	V
V_{21}	sync level	B/G and L	–	1.5	–	V
	zero carrier level	B/G	–	2.6	–	V
		L	–	1.47	–	V
	upper video clipping level		$V_P - 1.1$	$V_P - 1$	–	V
	lower video clipping level		–	0.3	0.4	V
R_{21}	output resistance	note 2	–	–	10	Ω
$I_{int\ 21}$	internal bias current for emitter-follower	DC	1.6	2.0	–	mA
I_{21}	maximum output sink current	DC and AC	1.0	–	–	mA
	maximum output source current		2.0	–	–	mA
B	–1 dB video bandwidth	B/G, L standard; $C_{21} < 50$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
	–3 dB video bandwidth		7	8	–	MHz
α_H	suppression of video signal harmonics	note 9a; $C_{21} < 50$ pF; $R_L > 1$ kΩ; AC load	35	40	–	dB
RR	ripple rejection at pin 21	see Fig.12; video signal: grey level;				
		B/G	32	35	–	dB
		L	26	30	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 10 and 22)						
R_{22}	input resistance	note 2	2.6	3.3	4.0	kΩ
C_{22}	input capacitance		1.4	2	3.0	pF
V_{22}	DC voltage at input		1.5	1.8	2.1	V
G_v	voltage gain	note 10; B/G and L	6.5	7	7.5	dB
V_{o10}	upper video clipping		3.9	4.0	–	V
	lower video clipping		–	1.0	1.1	V
R_{10}	output resistance	note 2	–	–	10	Ω
$I_{int\ 10}$	internal bias current for emitter-follower	DC	2.0	2.5	–	mA
I_{10}	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.4	–	–	mA
B	–1 dB video bandwidth	B/G, L; $C_{10} < 20$ pF; $R_L > 1$ kΩ; AC load	8.4	11	–	MHz
	–3 dB video bandwidth		11	14	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to CVBS output (pin 10; 330 Ω between pins 21 and 22, sound carrier off)						
$V_{o\,CVBS}$	CVBS output signal on pin 10 (peak-to-peak value)	note 10	1.7	2.0	2.3	V
	CVBS output level	sync level (B/G)	–	1.35	–	V
		sync level (L)	–	1.35	–	V
		peak level (MAC)	–	1.35	–	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt in B/G standard	note 11; gain variation	–	–	1	%
	black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; note 11; gain variation	–	–	1.9	%
ΔG	differential gain	CCIR line 330	–	2	5	%
$\Delta\varphi$	differential phase		–	1	2	deg
B	–1 dB video bandwidth	B/G, L; $C_{10} < 20$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
	–3 dB video bandwidth		7	8	–	MHz
B_{MAC}	–1 dB video bandwidth	MAC; $C_{10} < 20$ pF; $R_L > 1$ kΩ; AC load	8.4	11	–	MHz
	–3 dB video bandwidth		11	14	–	MHz
S/N (W)	signal-to-noise ratio; weighted	see Fig.6 and note 12	56	60	–	dB
S/N	signal-to-noise ratio; unweighted		49	53	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.7 and note 13; f = 1.1 MHz	58	64	–	dB
	intermodulation at 'yellow'		60	66	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	see Fig.7 and note 13; f = 3.3 MHz	58	64	–	dB
	intermodulation at 'yellow'		59	65	–	dB
α_c	residual vision carrier (RMS value)	B/G and L standard; fundamental wave and harmonics	–	2	10	mV
		MAC standard; fundamental wave and harmonics	–	20	50	mV
α_H	suppression of video signal harmonics	note 9a	35	40	–	dB
	spurious elements	note 9b	40	–	–	dB
RR	ripple rejection at pin 10	see Fig.12; video signal: grey level; B/G	25	28	–	dB
VIF-AGC detector (pin 28)						
I_{28}	charging current	B/G, L and MAC; note 11	0.8	1	1.2	mA
	additional charging current	L in event of missing VITS pulses and no white video content	2.0	2.5	3.0	μA
	discharging current	B/G	16	20	24	μA
		normal mode L and MAC	240	300	360	nA
		fast mode L and MAC	32	40	48	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{resp}	AGC response to an increasing VIF step	B/G, L and MAC; note 14	–	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step	B/G	–	2.2	3.5	ms/dB
		fast mode L and MAC	–	1.1	1.8	ms/dB
		normal mode L and MAC; note 14	–	150	240	ms/dB
ΔIF	VIF amplitude step for activating fast AGC mode	L and MAC	–2	–6	–12	dB
V_3	threshold voltage level	see Fig.9				
	for additional charging current	L	–	1.95	–	V
	for fast mode L	L	–	1.65	–	V
	for fast mode MAC	MAC	–	1.9	–	V
Tuner AGC (pin 19)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1/2, 4/5; R_{TOP} = 22 kΩ, I_{19} = 0.4 mA	–	2	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1/2, 4/5; R_{TOP} = 0 Ω, I_{19} = 0.4 mA	50	100	–	mV
V_{19}	permissible output voltage	note 2; from external source	–	–	13.2	V
	saturation voltage	I_{19} = 1.7 mA	–	–	0.2	V
ΔV_{19}	variation of take over point by temperature	I_{19} = 0.4 mA	–	0.03	0.07	dB/K
I_{19}	sink current	see Fig.4				
		no tuner gain reduction; V_{19} = 12 V	–	–	2.5	µA
		V_{19} = 13.2 V	–	–	5	µA
		maximum tuner gain reduction	1.7	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 23; see Fig.8 and note 15)						
S	control steepness $\Delta I_{23} / \Delta f$	note 16; B/G and L	–0.5	–0.72	–1.0	µA/kHz
Δf_{IF}	frequency variation by temperature	note 5; I_{AFC} = 0	–	–	±20	ppm/K
V_{23}	output voltage upper limit	see Fig.8	$V_P - 0.6$	$V_P - 0.3$	–	V
	output voltage lower limit		–	0.3	0.6	V
I_{23}	output current source		160	200	240	µA
	output current sink		160	200	240	µA
$\Delta I_{23residual}$	residual video modulation current (peak-to-peak value)	B/G and L	–	20	30	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound IF amplifier (pins 31 and 32)						
$V_{i\,SIF}$	input sensitivity (RMS value)	FM-mode; –3 dB at intercarrier output pin 20	–	30	70	μV
		AM-mode; –3 dB at AF output pin 12	–	70	100	μV
	maximum input signal (RMS value)	FM-mode; +1 dB at intercarrier output pin 20	30	70	–	mV
		AM-mode; +1 dB at AF output pin 12	100	140	–	mV
G_{SIF}	SIF gain control range	see Fig.5, FM	60	67	–	dB
		see Fig.5, AM	60	67	–	dB
R_i	input resistance (differential)	note 2	1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{31/32}$	DC voltage		–	3.4	–	V
$\alpha_{SIF/VIF}$	crosstalk attenuation between SIF and VIF input	pins 1/2, 4/5 - 31/32; note 3	50	–	–	dB
SIF AGC detector (pin 8)						
I_8	charging current	FM mode	8	12	16	μA
		AM mode	0.8	1.2	1.6	μA
	discharging current	FM mode	8	12	16	μA
		normal mode AM	1	1.4	1.8	μA
		fast mode AM	60	85	110	μA
Single reference QSS intercarrier mixer (pin 20)		B/G				
V_o	IF intercarrier level (RMS value)	SC_1; sound carrier 2 off	75	100	125	mV
B	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
α_H	residual sound carrier (RMS value)	fundamental wave	–	2	–	mV
		harmonics	–	0.75	–	mV
R_{20}	output resistance	note 2	–	–	25	Ω
V_{20}	DC voltage		–	2.0	–	V
I_{int20}	internal bias current for emitter-follower	DC	1.5	1.9	–	mA
I_{20}	maximum output sink current	DC and AC	1.1	1.5	–	mA
	maximum output source current		3.0	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM input switch and limiter amplifier 1 (pins 17 and 18; note 17)						
$V_{i\,FM}$	input signal for lock-in		–	–	100	μV
	input signal (RMS value)	(S+N)/N = 40 dB	–	300	400	μV
	allowed input signal (RMS value)		200	–	–	mV
$R_{17,18}$	input resistance	note 2; activated input	480	600	720	Ω
		note 2; not activated input	–	–	100	Ω
$V_{17,18}$	DC voltage	activated input	–	2.8	–	V
		not activated input pin 17	–	1.8	–	V
		not activated input pin 18	–	–	0.1	V
α_i	crosstalk attenuation	activated to not activated input; not activated input terminated with an impedance of 600 Ω (AC-coupled)	44	50	–	dB
Limiter amplifier 2 (pin 16; note 17)						
$V_{i\,FM}$	input signal for lock-in		–	–	100	μV
	input signal (RMS value)	(S+N)/N = 40 dB; PLL1 has to be in locked mode; auto mute off	–	300	400	μV
	allowed input signal (RMS value)		200	–	–	mV
	input signal for no auto mute; PLL enabled (RMS value)		0.7	1	1.5	mV
ΔV_{16}	hysteresis of level detector for auto mute		–3	–6	–8	dB
R_{16}	input resistance	note 2	480	600	720	Ω
V_{16}	DC voltage		–	2.0	–	V
FM-PLL demodulators						
$f_{i\,FM}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
	holding range of PLL	upper limit	9.0	–	–	MHz
		lower limit	–	–	3.5	MHz
t_{acqu}	acquisition time		–	–	4	μs
FM operation (standard B/G) (pins 12 and 13; note 17a)						
$V_{o\,AF12,13}$	AF output signal (RMS value)	27 kHz (= 54% FM deviation); see Fig.3 and note 18				
		$R_{x,y}$ = 470 Ω	200	250	300	mV
		$R_{x,y}$ = 0 Ω	400	500	600	mV
	clipping level	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 18	–	–	±53	kHz
ΔV_o	temperature drift of AF output signal		–	3	7	10^{-3}dB/K
ΔV_o	difference between both AF output signals		–	–	±1.0	dB
$V_{14,15}$	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 19	1.2	–	3.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{12,13}$	output resistance	note 2	–	–	100	Ω
$V_{12,13}$	DC voltage	tracked with supply voltage	–	$V_P/2$	–	V
$I_{12,13}$	maximum sink and source current	DC and AC	–	–	1.1	mA
B	–3 dB audio frequency bandwidth		100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%
S/N(W)	signal-to-noise ratio; weighted	FM-PLL only; with 50 µs de-emphasis; 27 kHz (= 54% FM deviation); CCIR468-4	55	60	–	dB
V_{sc}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
α_{AM}	AM suppression	with 50 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (= 54% FM deviation)	46	50	–	dB
$\alpha_{12/13}$	crosstalk attenuation between AF outputs	f = 50 Hz to 12.5 kHz; $R_L \geq 10$ kΩ; $C_L = 1$ nF	66	70	–	dB
$\alpha_{12,13}$	mute attenuation of AF1 and AF2 signal	pin 12 and 13; standard B/G and L	70	80	–	dB
$\Delta V_{12,13}$	DC jump of AF output terminals for switching AF output to mute state and vice versa	both FM PLLs have to be in locked mode; note 20	–	±50	±150	mV
RR	ripple rejection at pins 12 and 13	see Fig.12; $R_x = R_y = 0$ Ω	26	30	–	dB
Single reference QSS AF performance for FM operation (standard B/G) notes 21 and 22 picture to sound carrier ratio: PC/SC_1 = 13 dB; PC/SC_2 = 20 dB; (transmitter) sound attenuation of VIF SAW filter: minimum 33 dB						
measurement condition: PC/SC_1 ratio at pins 1 and 2; note 23			40	–	–	dB
S/N(W)	signal-to-noise ratio; weighted	27 kHz (= 54% FM deviation) CCIR 468-4				
	black picture	SC_1 / SC_2	53/48	58/55	–	dB
	white picture	SC_1 / SC_2	52/47	55/53	–	dB
	6 kHz sine wave (black to white modulation)	SC_1 / SC_2	44/42	48/46	–	dB
	250 kHz square wave (black to white modulation)	SC_1 / SC_2; note 24	48/40	53/45	–	dB
	sound carrier subharmonics	SC_1 / SC_2: 2.75 MHz ± 3 kHz	45/44	51/50	–	dB
		SC_1 / SC_2: 2.87 MHz ± 3 kHz	46/45	52/51	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM operation (standard L) pin 12; note 25						
$V_{o\,AF}$	AF output signal (RMS value)	m = 54%	400	500	600	mV
THD	total harmonic distortion	m = 54%; see Fig.11	–	0.5	1.0	%
B	–3 dB AF bandwidth		100	125	–	kHz
S/N(W)	signal-to-noise ratio; weighted	CCIR 468-4; see Fig.10	47	53	–	dB
V_{12}	DC potential	tracked with supply voltage	–	$V_P/2$	–	V
RR	ripple rejection at pin 12	see Fig.12	22	25	–	dB
Standard switch (pin 9)						
V_9	DC potential for preferred settings; for other settings see Table 2					
V_{IH}	input voltage for negative standard	note 26; B/G, MAC	2.8	–	V_P	V
V_{IT}	input voltage for negative standard	negative AGC OFF	1.3	–	2.3	V
V_{IL}	input voltage for positive standard	L	0	–	0.8	V
I_{IL}	LOW level input current	V_9 = 0 V	200	250	300	µA
VIF input switch (pin 30)						
V_{30}	DC potential for preferred settings; for other settings see Table 2					
V_{IH}	input voltage for VIF input A	note 26; B/G, L	2.8	–	V_P	V
V_{IT}	input voltage for VIF input B	MAC	1.3	–	2.3	V
V_{IL}	input voltage for VIF input B	B/G, L	0	–	0.8	V
I_{IL}	LOW level input current	V_{30} = 0 V	180	230	280	µA
FM input and L accent switch (pin 11)						
V_{11}	DC potential for FM input selection					
	input pin 17 activated	note 26	2.8	–	V_P	V
	input pin 18 activated	see Fig.3; 22 kΩ potentiometer only for L accent alignment required	0	–	2.0	V
	DC potential for standard L VCO frequency switching					
	for L standard	note 26	2.8	–	V_P	V
	for L accent standard and alignment		0	–	2.0	V
I_{IL}	LOW level input current	V_{11} = 0 V	160	200	240	µA

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as an application information for designing the television receiver.
3. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 38.9 MHz.
4. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with sync level within gain control range). Resonance circuit of VCO: $Q_0 > 50$; C_{ext} = 6.8 pF; $C_{int} \approx 10$ pF (loop voltage approximately 2.7 V).
5. Temperature coefficient of external LC-circuit is equal to zero.
6. $V_{i\,IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
7. $V_{i\,IF}$ signal for nominal video signal.

8. Offset current measured between pin 7 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at VIF input (pins 1, 2, 4 and 5) and VIF amplifier gain at minimum ($V_{28} = V_P$). Due to sample and hold mode of the FPLL in L standard, the leakage current of the loop filter capacitor (C = 220 nF) should not exceed 500 nA.
9. Measurements taken with SAW filter G3962 (sound carrier suppression: 40 dB); loop bandwidth BL = 60 kHz; a. modulation VSB, $f_{video} > 0.5$ MHz; b. f_{video} = 10 kHz to 10 MHz. Sound carrier on. SIF SAW filter G3950.
10. The 7 dB buffer gain accounts for 1 dB loss (not valid for MAC) in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 21 to pin 22).
11. The leakage current of the AGC capacitor should not exceed 1 µA at B/G standard respectively 10 nA current at L standard. Larger currents will increase the tilt.
12. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 10). B = 5 MHz weighted in accordance with CCIR 567.
13. The intermodulation figures are defined: $\alpha_{1.1}$ = 20 log (V_0 at 4.4 MHz / V_0 at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal $\alpha_{3.3}$ = 20 log (V_0 at 4.4 MHz / V_0 at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
14. Response speed valid for a VIF input level range of 200 µV up to 70 mV.
15. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.8. The AFC-steepness can be changed by the resistors at pin 23.
16. Depending on the ratio $\Delta C / C_0$ of the LC resonant circuit of VCO (Q > 50; see note 4; $C_0 = C_{int} + C_{ext}$).
17. Input level for second IF from an external generator with 50 Ω source impedance, AC coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pin 8 and pin 28 has to be connected to positive supply voltage. S/N and THD measurements are taken at 50 µs de-emphasis. The not tested FM-PLL has to be locked to an unmodulated carrier.
    a. second IF input level 10 mV RMS.
18. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV RMS ($R_x = R_y = 0$ Ω; see Fig.3). By using $R_x = R_y$ = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS) and adapted to the stereo decoder family TDA9840. For handling an FM deviation of more than 53 kHz the AF output signals have to be reduced by using R_x and R_y in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended ($R_x = R_y$ = 470 Ω).
19. The leakage current of the decoupling capacitor (2.2 µF) should not exceed 1 µA.
20. In the event of activated auto mute state the second FM-PLL oscillator is switched off, if the input signal at pin 16 is missing or too weak (see Fig.3). In the event of switching the second FM-PLL oscillator on by the auto mute stage an increased DC jump is the consequence. Note, that noise at pin 16 disables the mute state (at low SIF input signal), but this will not lead to false identification of the used stereo decoder family TDA9840.
21. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    - Incidental phase modulation for black-to-white jump less than 0.5 degree.
    - QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sinewave black-to-white video modulation.
22. Measurements are taken with SAW filter G3962 (Siemens) for vision IF (supressed sound carrier) and G9350 (Siemens) for sound IF (supressed picture carrier). Input level $V_{i\,SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
23. The PC/SC_1 ratio is calculated as the addition of TV transmitter PC/SC_1 ratio and SAW filter PC/SC_1 ratio. This PC/SC_1 ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC_1 ratio will change these values.
24. The used loop filter is related to Fig.3 but with an additional capacitor of 6.8 nF in parallel. Without this capacitor the S/N value will decrease by typically 5 dB.
25. Measurements are taken with SAW filter K9350 (Siemens) for sound IF (supressed picture carrier).
26. The input voltage has to be V > 2.8 V, or open-circuit.

Table 1 Input frequencies and carrier ratios.

		B/G STANDARD	L STANDARD	L ACCENT STANDARD	UNIT
picture carrier	f_{pc}	38.9	38.9	33.9	MHz
sound carrier	f_{sc1}	33.4	32.4	40.4	MHz
	f_{sc2}	33.158	–	–	MHz
picture to sound carrier ratio	SC_1	13	10	10	dB
	SC_2	20	–	–	dB

Table 2 Switch logic.

INPUT SWITCH (pin 30)	STANDARD SWITCH (pin 9)	SELECTED VIF INPUT	SELECTED STANDARD	VIDEO POLARITY	FM-PLL		AF-AMPLIFIER	
					1	2	1	2
2.8 V to V_P	2.8 V to V_P	A	B/G	negative	on	on	FM	FM
	1.3 V to 2.3 V		B/G, with external VIF AGC	negative	on	on	FM	FM
	0 to 0.8 V		L	positive	off	off	AM	mute
1.3 V to 2.3 V	2.8 V to V_P	B	MAC (note 1)	negative	off	off	mute	mute
	1.3 V to 2.3 V		MAC (note 1), with external VIF AGC	negative	off	off	mute	mute
	0 to 0.8 V		L (note 1)	positive	off	off	AM	mute
0 to 0.8 V	2.8 V to V_P	B	B/G	negative	on	on	FM	FM
	1.3 V to 2.3 V		B/G, with external VIF AGC	negative	on	on	FM	FM
	0 to 0.8 V		L	positive	off	off	AM	mute

Note to Table 2

1. Without external sound trap (video signal internally switched to video buffer).

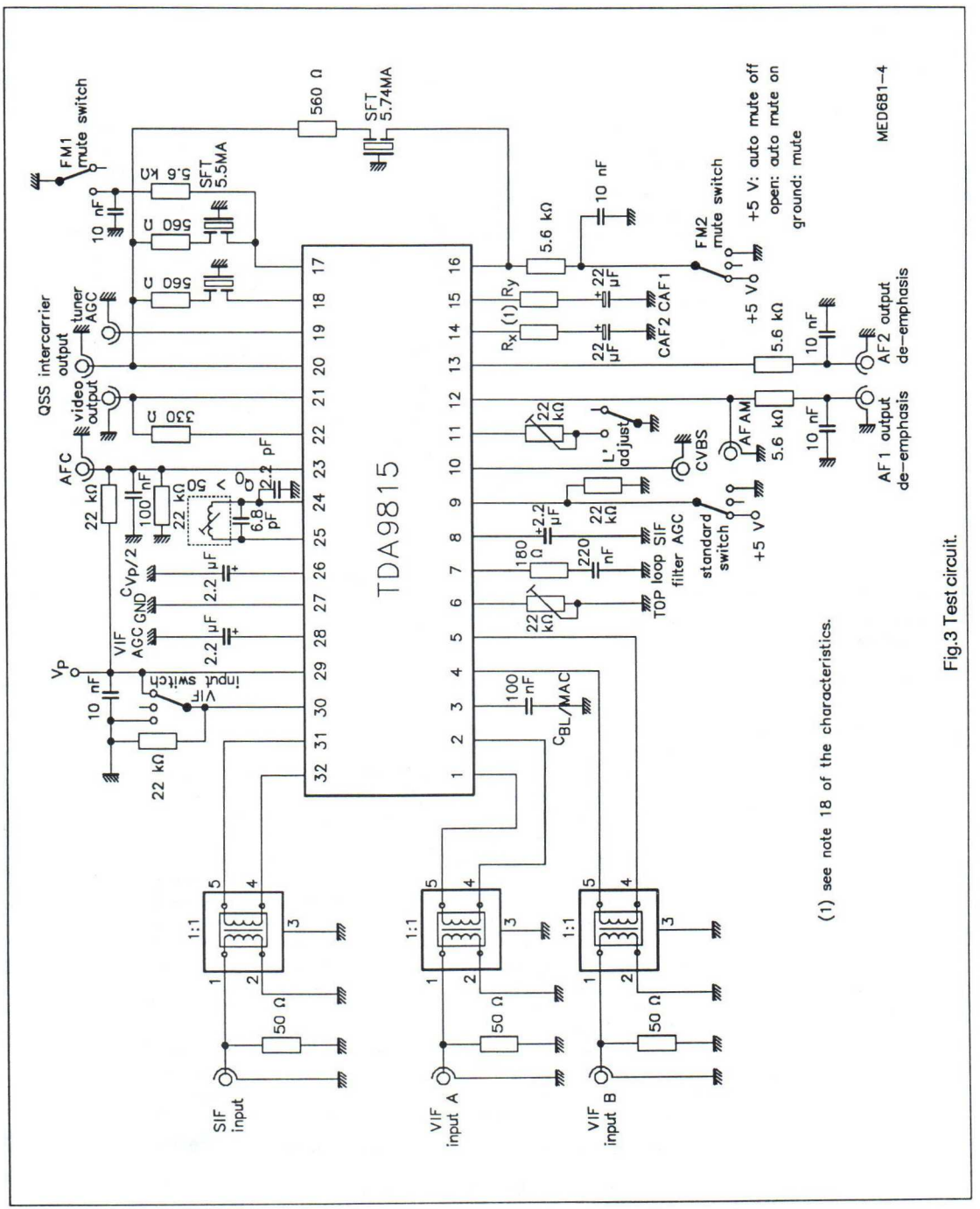


Fig.3 Test circuit.

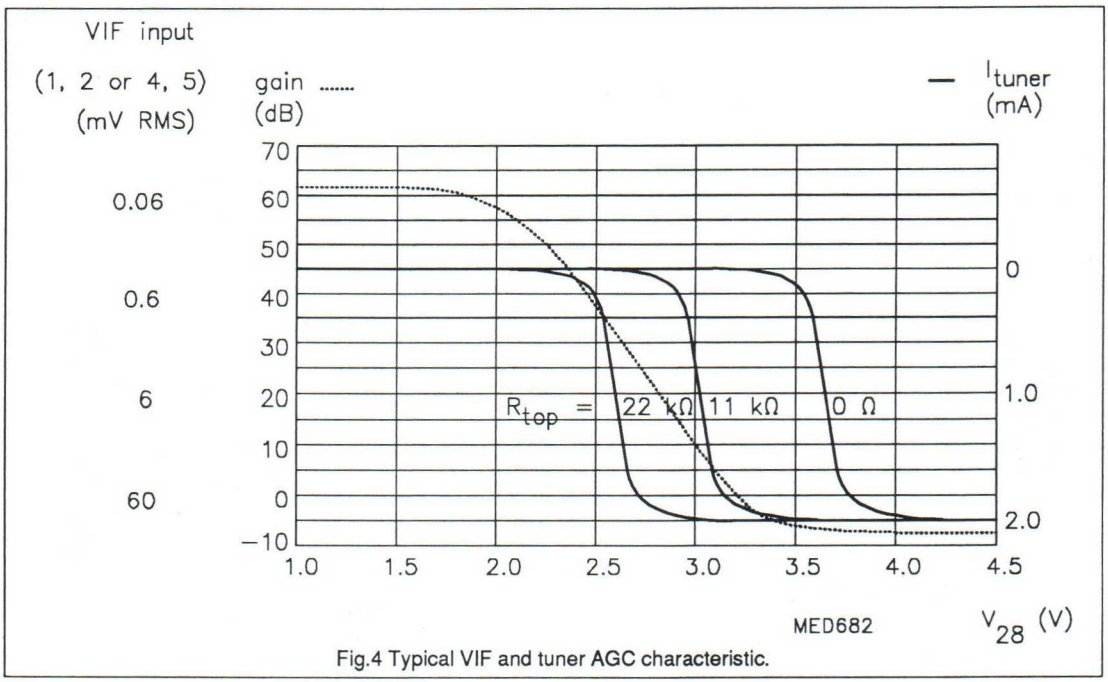


Fig.4 Typical VIF and tuner AGC characteristic.

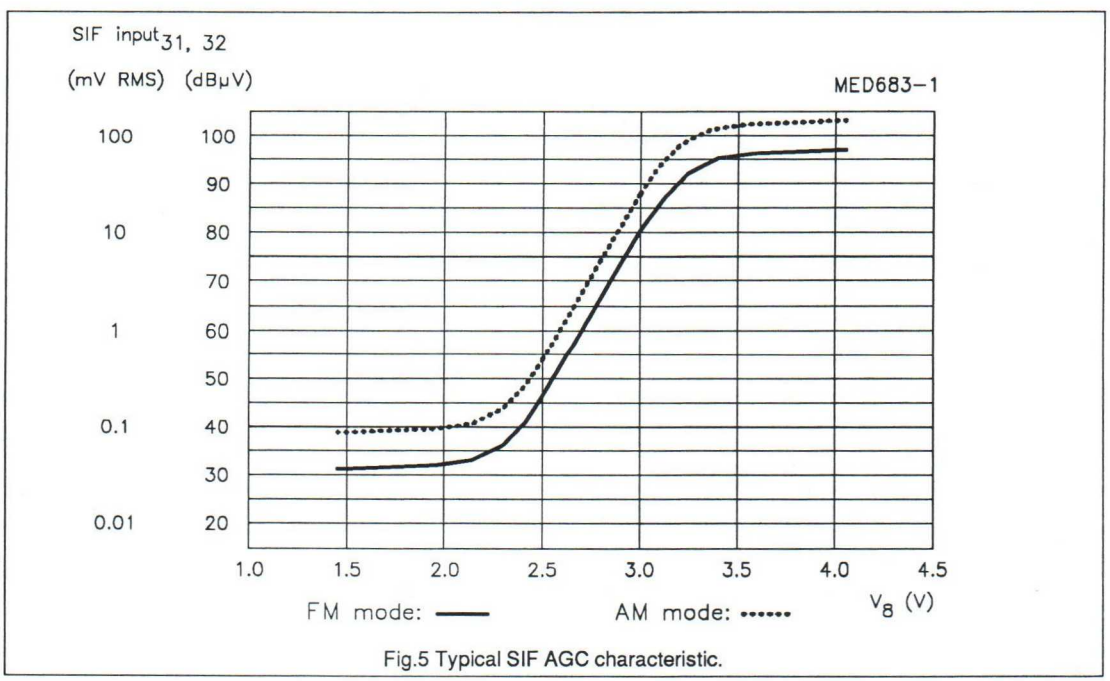


Fig.5 Typical SIF AGC characteristic.

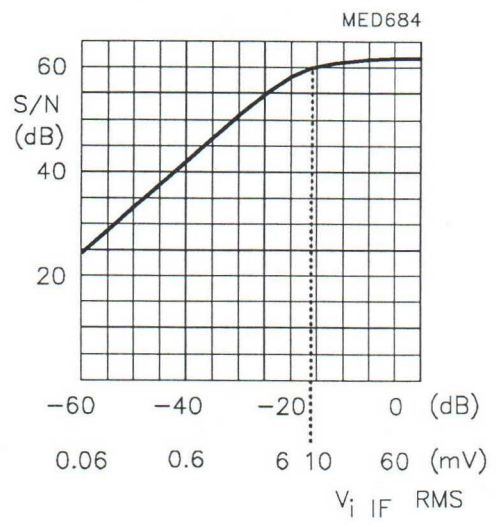
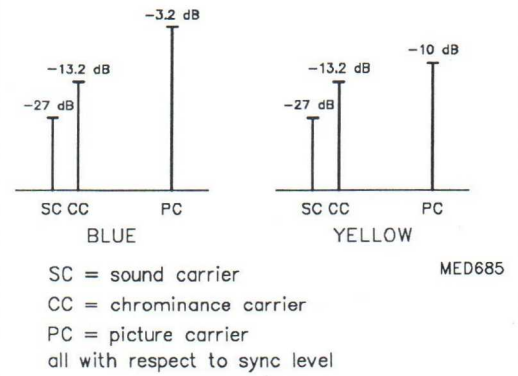


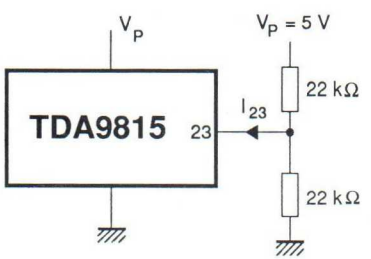
Fig.6 Typical S/N as a function of IF input voltage.



SC = sound carrier
CC = chrominance carrier
PC = picture carrier
all with respect to sync level

The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SWIF G1956).

Fig.7 Input signal conditions.



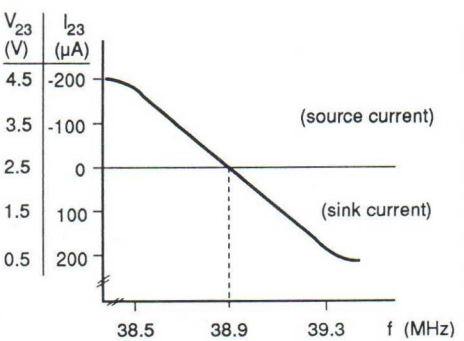


Fig.8 Measurement conditions and typical AFC characteristic.

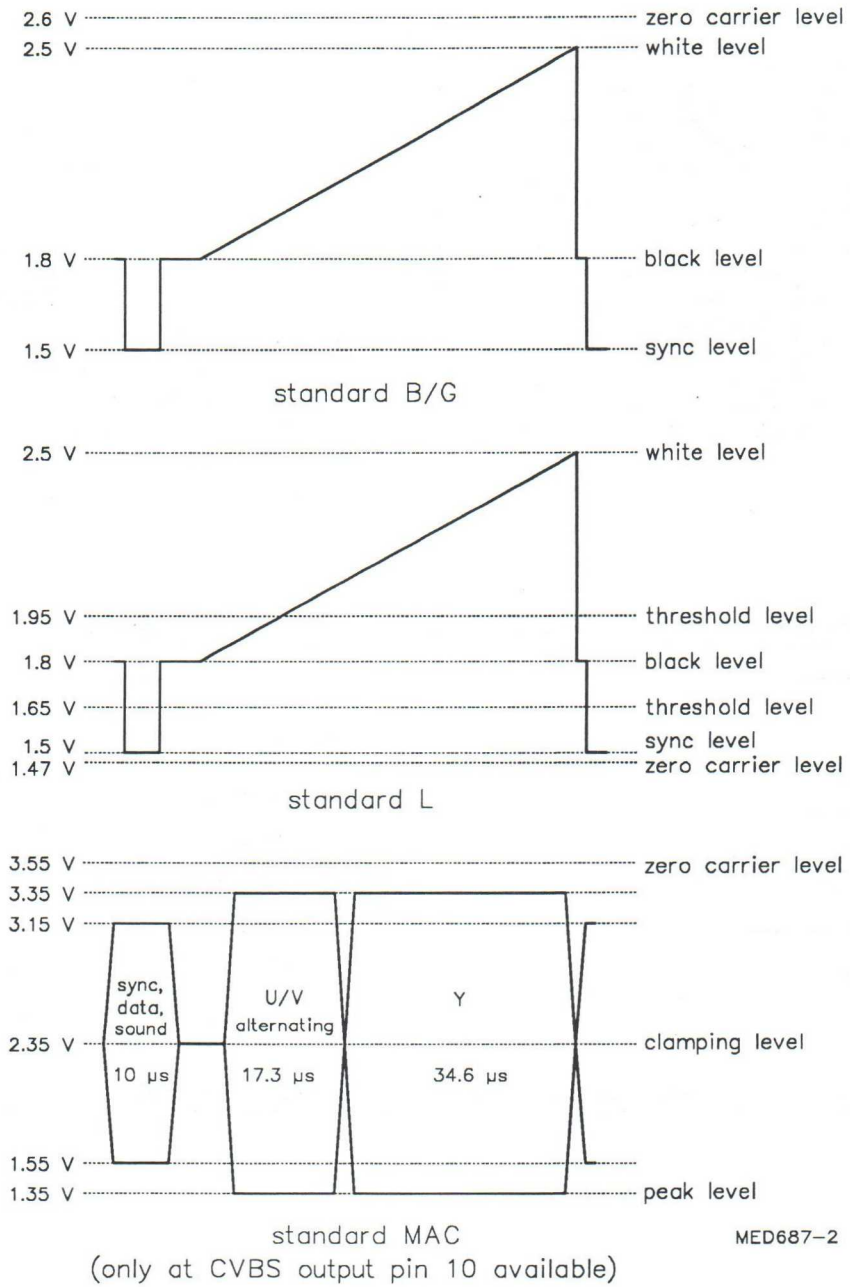


Fig.9 Typical video signal levels on output pin 21 (sound carrier off).

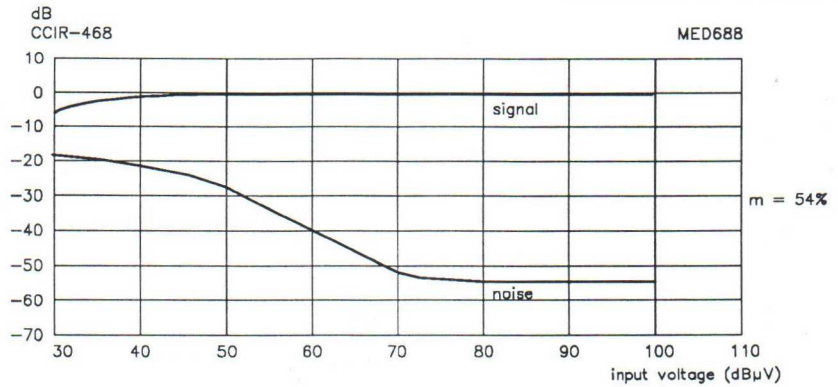


Fig.10 Typical audio S/N as a function of input signal at AM standard.

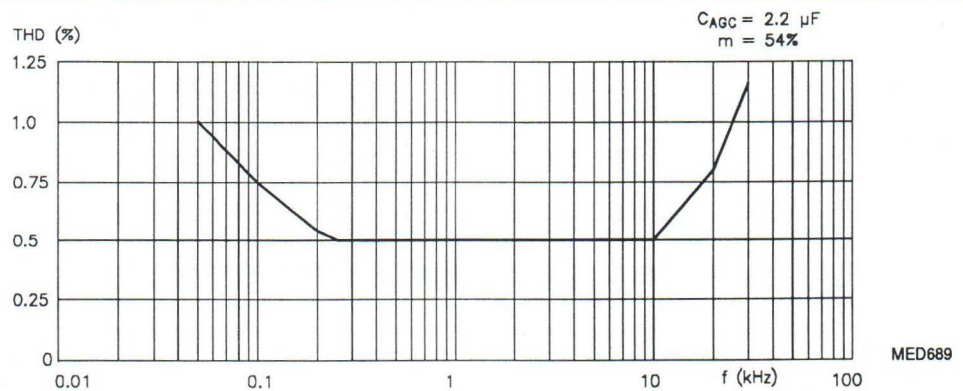


Fig.11 Typical THD as a function of audio frequency at AM standard.

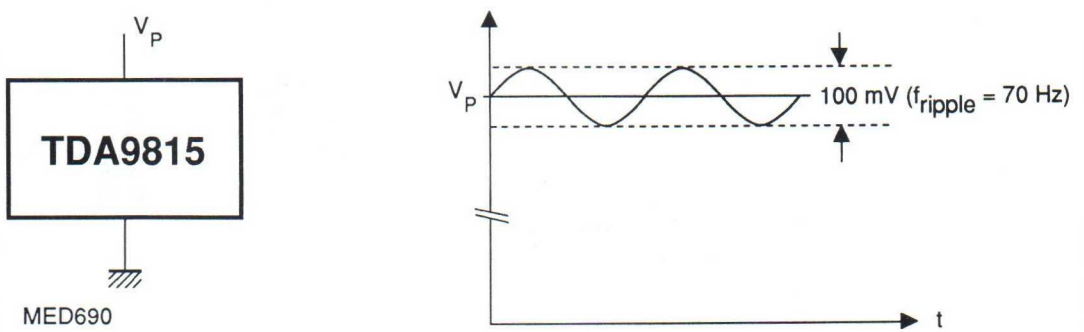
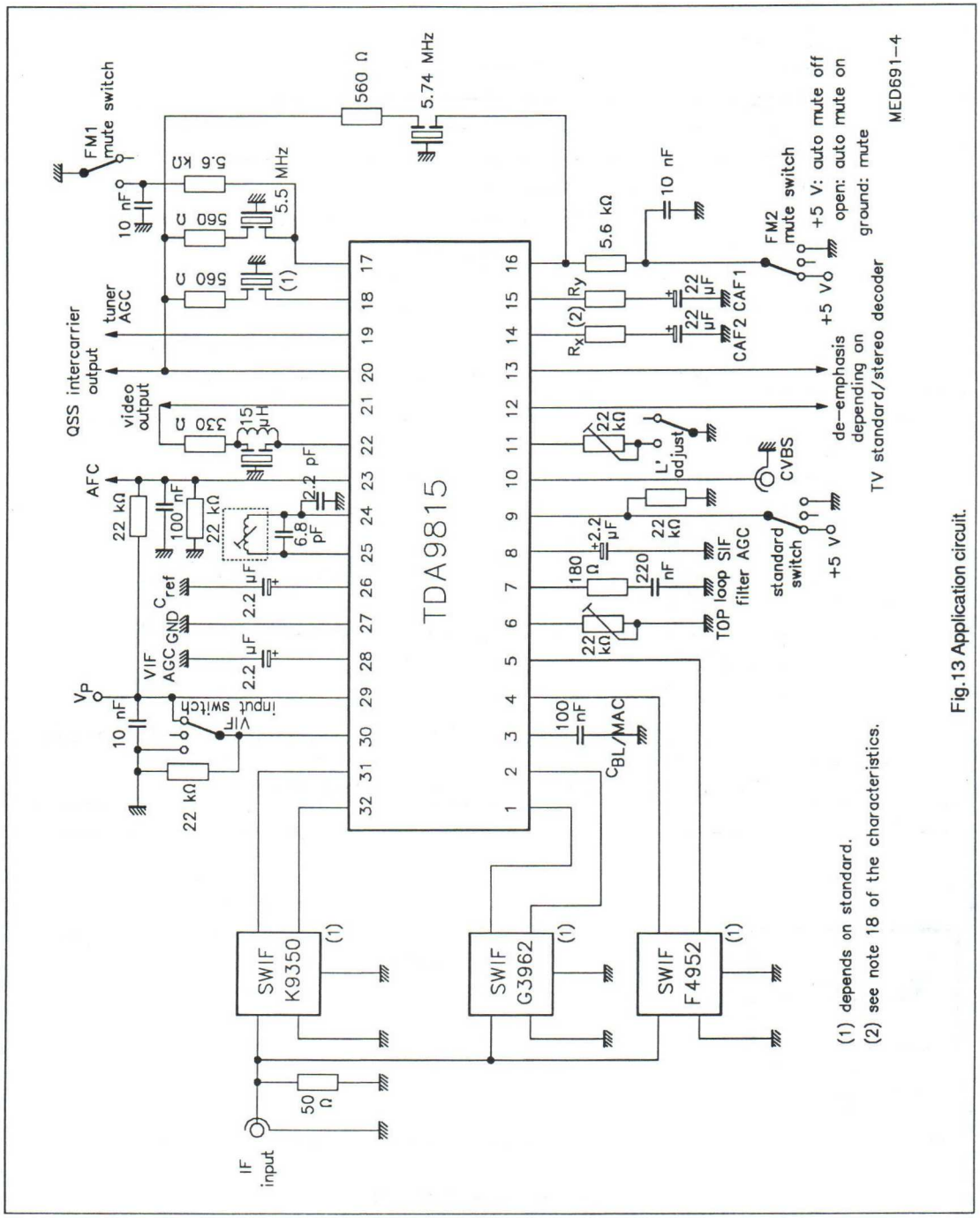


Fig.12 Ripple rejection condition.



(1) depends on standard.
(2) see note 18 of the characteristics.

Fig.13 Application circuit.

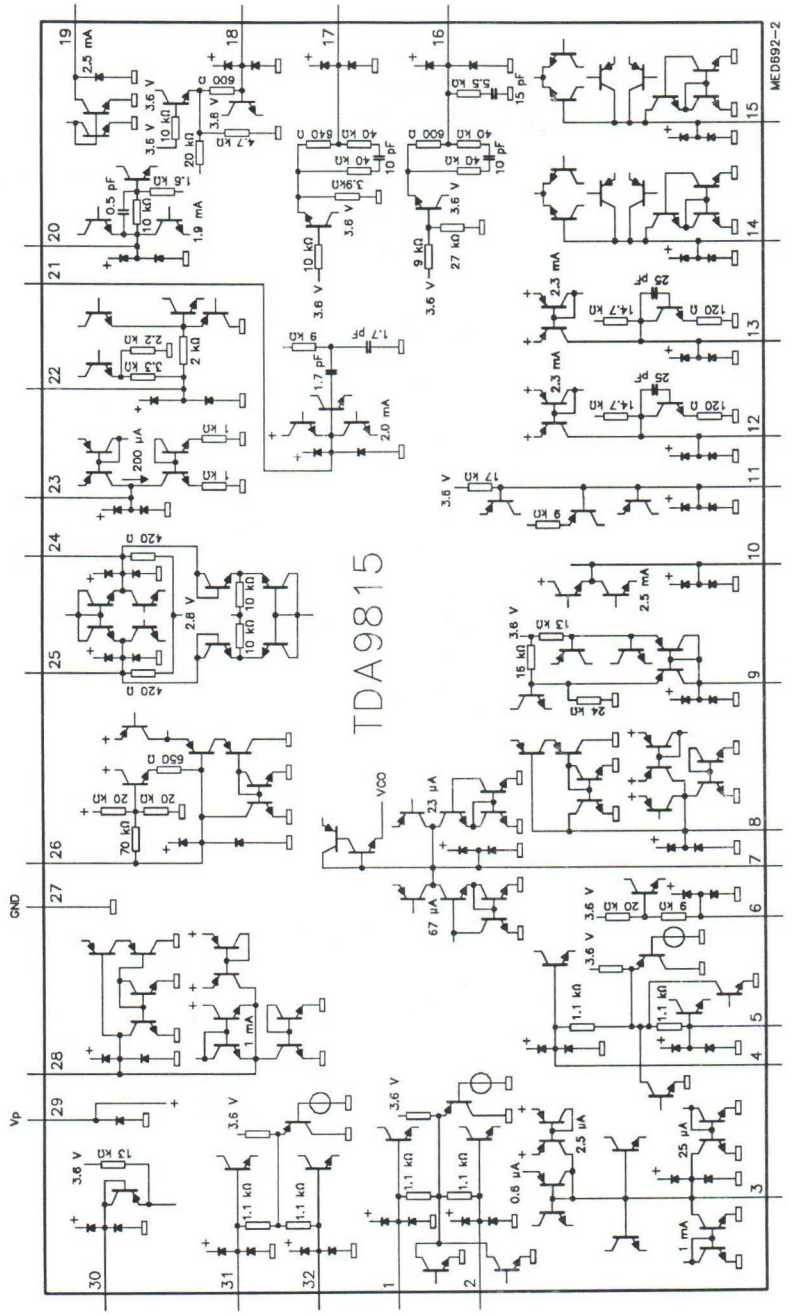


Fig.14 Internal circuits.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 91

TDA9820

Multistandard / dual channel TV FM intercarrier sound demodulator

FEATURES

- Multistandard application for sound standards M, B/G, I, D/K
- Two alignment-free PLL FM demodulators
- Four-input source selector for one of the two FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9820 is a monolithic, integrated, multistandard TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9820	16	DIL	plastic	SOT38
TDA9820T	16	DIL	plastic	SO16

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

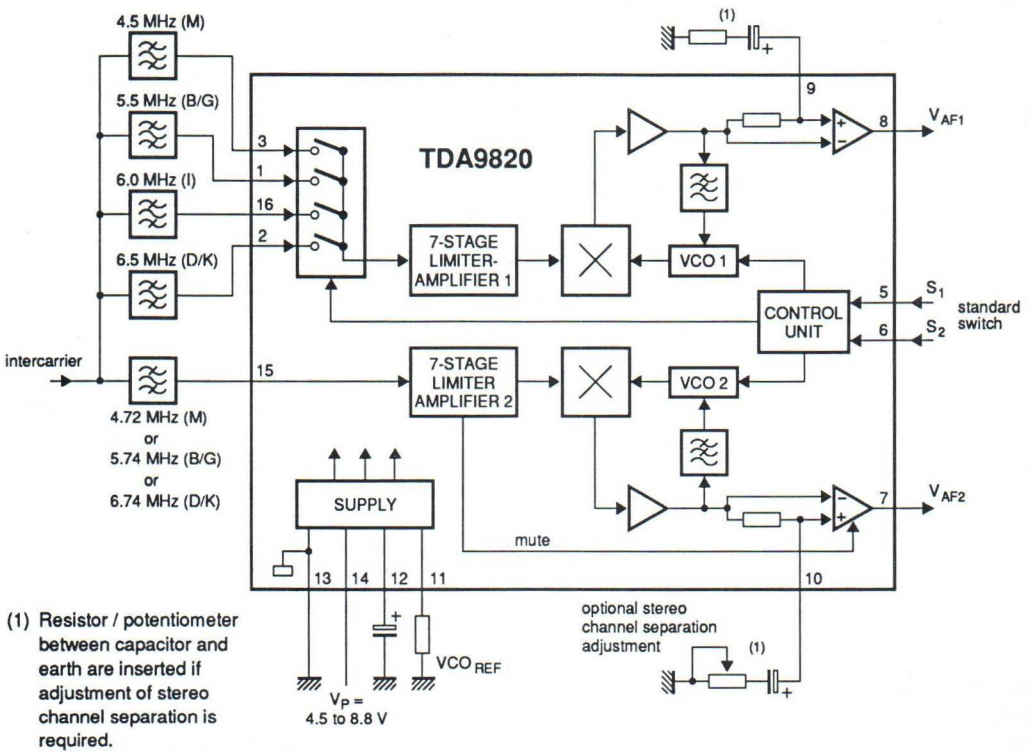


Fig.1 Block diagram.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
$IN_{1(D/K)}$	2	first intercarrier input at 6.5 MHz
$IN_{1(M)}$	3	first intercarrier input at 4.5 MHz
n.c.	4	not connected
S_1	5	standard switch bit 1
S_2	6	standard switch bit 2
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
IN_2	15	second intercarrier input
$IN_{1(I)}$	16	first intercarrier input at 6.0 MHz

PIN CONFIGURATION

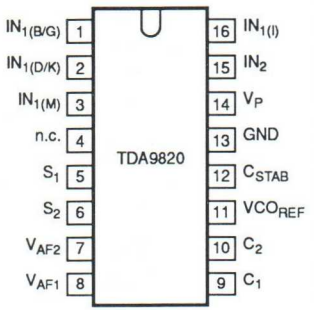


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

Source selector

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.

One of the four filtered sound carriers from pins 1, 2, 3 or 16 is fed to limiter-amplifier 1 via the appropriate electronic switch in the source selector. The electronic switch of the sound carrier is selected by the control unit (see Logic Table).

The second sound carrier of the intercarrier signal is directly fed from pin 15 to limiter-amplifier 2.

FM demodulators

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensures that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. High amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as followes:

a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9

b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

Control unit

The control unit selects the required sound standard according to the voltages on pin 5 and pin 6. The control unit performs the following:

(a) selects the free-running frequencies of VCO1 and VCO2

(b) switches the source selector (the four possible combinations are shown in Table 1).

Table 1 Logic Table

STANDARD	S1 (pin 5)	S2 (pin 6)	FREQUENCY VCO1	FREQUENCY VCO2	SOURCE SELECTOR CONNECTION
B/G	1	1	5.5 MHz	5.74 MHz	pin 1
M	1	0	4.5 MHz	4.72 MHz	pin 3
I	0	1	6.0 MHz	OFF	pin 16
D/K	0	0	6.5 MHz	6.74 MHz	pin 2

Note to Table 1

In columns S1 and S2:
0 = LOW
1 = HIGH.

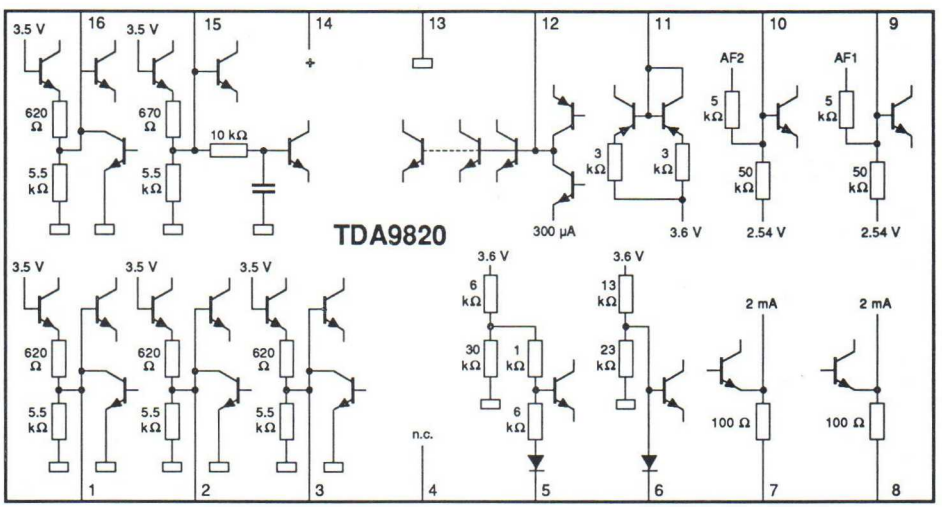


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	–0.5	9.0	V
V_i	input signal (pins 1, 2, 3, 15 and 16)	–0.5	5.0	V
V_{adj}	adjustment voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1,2,3,16/15(rms)}$ = 10 mV; T_{amb} = 25 °C; measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Source selector and limiter-amplifier 1 (pins 1, 2, 3 and 16)						
V_I	DC input voltage	input activated	–	2.55	–	V
		input not activated	–	–	0.1	V
R_I	input resistance	input activated	480	600	720	Ω
		input not activated	–	–	100	Ω
$V_{i(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB	–	100	250	μV
	allowed input signal (RMS value)		200	–	–	mV
α_i	crosstalk attenuation	not activated input to activated input	–	50	–	dB
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	μV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
R_{15}	input resistance		480	600	720	Ω
δ	hysteresis of level detector		–	12	–	dB
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – – –	4.5 5.5 6.0 6.5	– – – –	MHz MHz MHz MHz
f_{VCO2}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – –	4.72 5.74 6.74	– – –	MHz MHz MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	resistance at pin 11	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output amplifiers AF1 (pin 8) and AF2 (pin 7)						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
$\Delta V_o/\Delta V_o$	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 µs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment (pin 9 and pin 10)	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
THD	distortion (pin 8 and pin7)	with 50 µs de-emphasis	–	0.1	0.3	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 µs de-emphasis; m = 0.3; Δfi = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 µs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
Control unit (see Table 1)						
$V_{5,6}$	voltage for 'low'		0	–	0.8	V
$I_{5,6}$	input current	$0 < V_{5,6} < 0.8$	–	–180	–250	µA
$R_{5,6}$	allowed resistance to ground	$0 < V_{5,6} < 0.8$ ('low')	–	–	3.0	kΩ
V_5	voltage for HIGH (note 2)		2.2	–	V_P	V
V_6	voltage for HIGH (note 2)		1.8	–	V_P	V
$I_{5,6}$	input current	$V_{5,6} = V_P$	–	–	10	µA

Notes to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.
2. An open pin (n.c.) is interpreted as HIGH.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

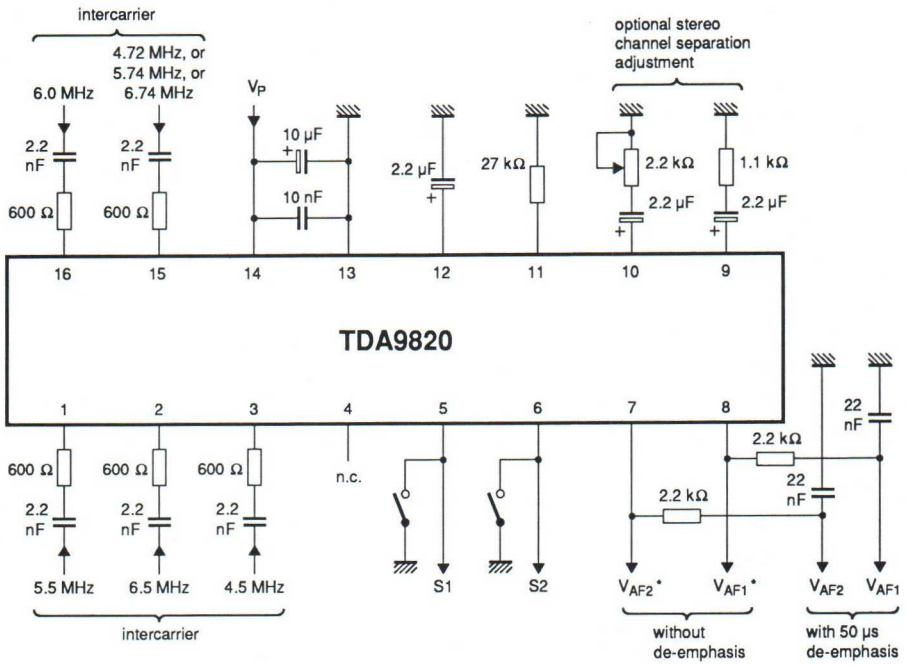


Fig.4 Test circuit.

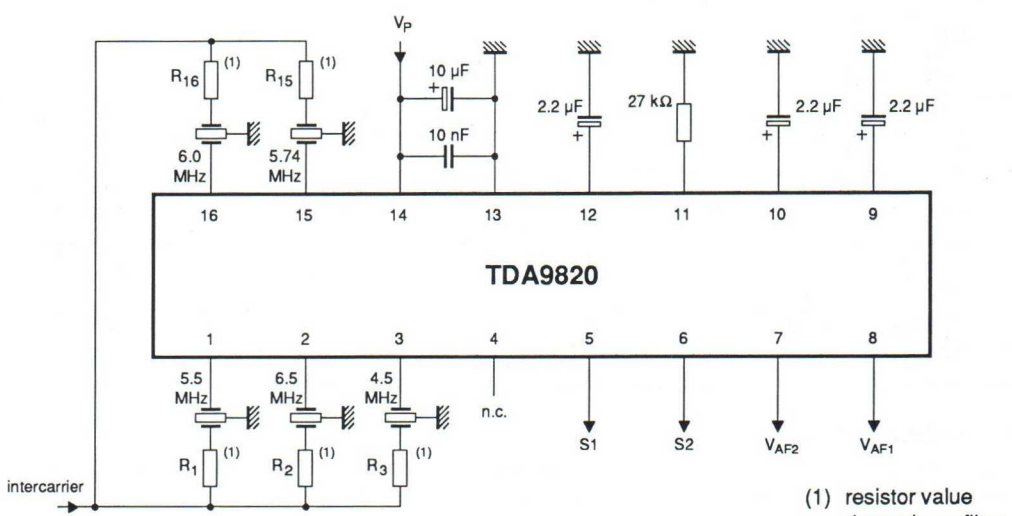


Fig.5 Application circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA9821

Dual channel TV FM intercarrier sound demodulator

FEATURES

- Two alignment-free PLL FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9821 is a monolithic, integrated, TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9821	16	DIL	plastic	SOT38

Dual channel TV FM intercarrier sound demodulator

TDA9821

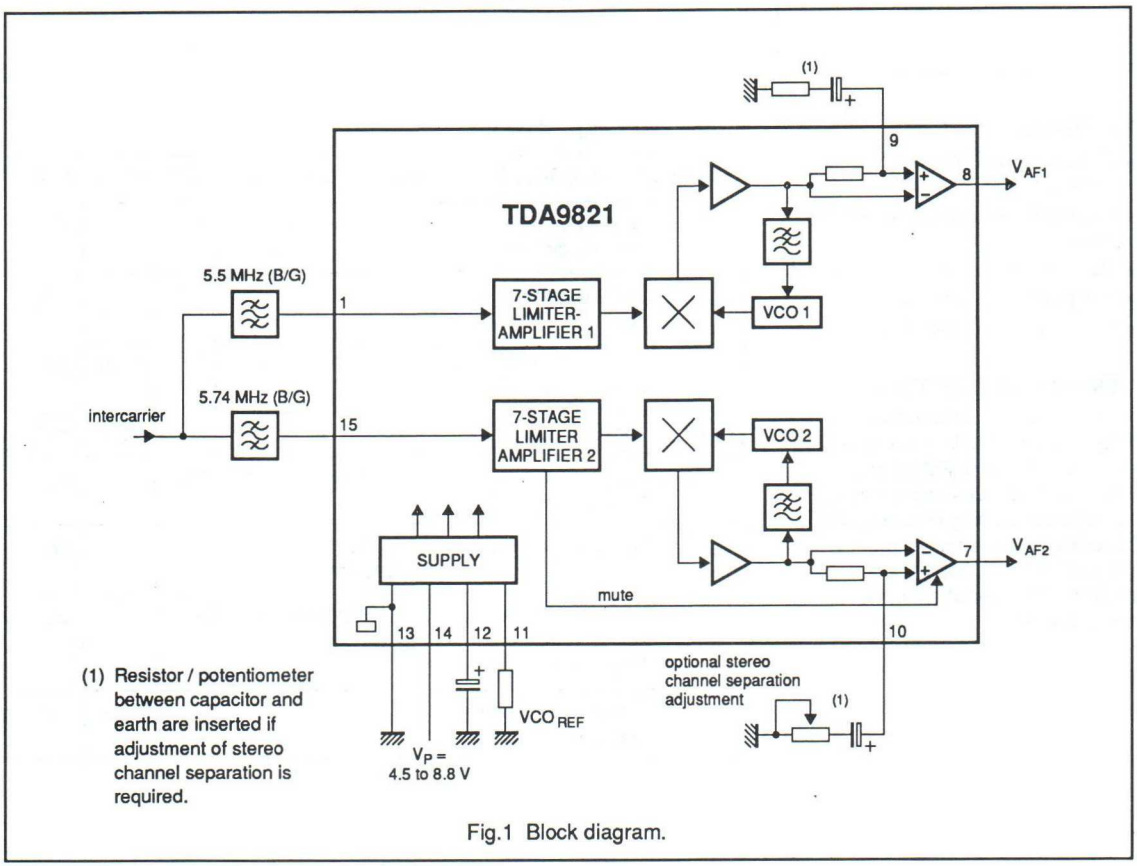


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

FM demodulators

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensure that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. The high amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as follows:

a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9

b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Normally stereo channel separation is adjusted in the stereo decoder for the B/G standard.

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

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PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
n.c.	2	not connected
n.c.	3	
n.c.	4	
n.c.	5	
n.c.	6	
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
$IN_{2(B/G)}$	15	second intercarrier input
n.c.	16	not connected

PIN CONFIGURATION

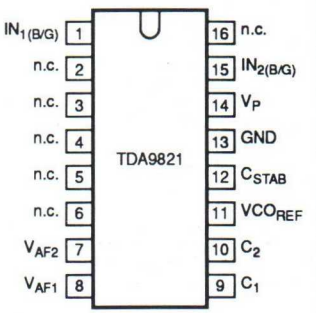


Fig.2 Pin configuration.

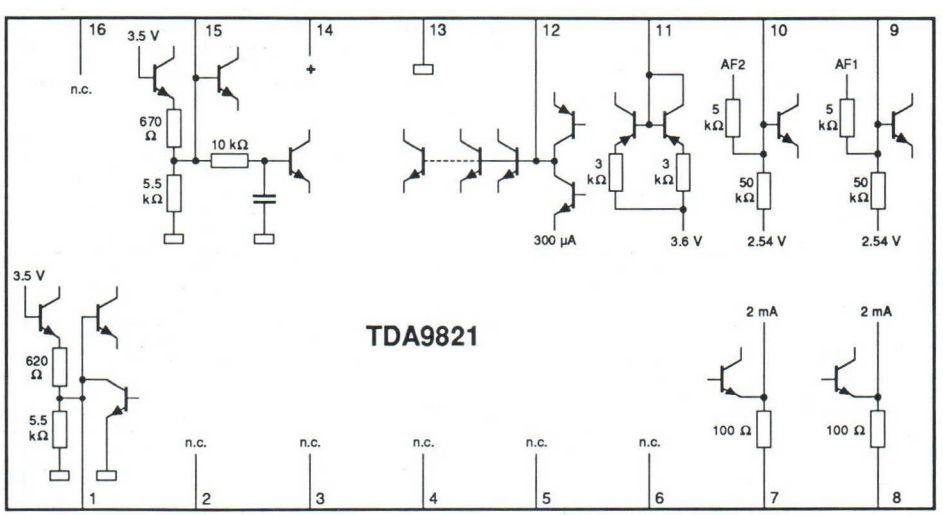


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	–0.5	9.0	V
V_i	input signal (pin 1 and pin 15)	–0.5	5.0	V
V_{adj}	adjusting voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1/15(rms)}$ = 10 mV; T_{amb} = 25 °C;measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Limiter-amplifier 1						
V_1	DC input voltage		–	2.55	–	V
R_1	input resistance		480	600	720	Ω
$V_{1(rms)}$	input signal(RMS value)	(S+N)/N = 40 dB	–	100	250	µV
	allowed input signal (RMS value)		200	–	–	mV
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	µV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
ΔV_{15}	mute hysteresis		–	12	–	dB
R_{15}	input resistance		480	600	720	Ω
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequency	R_{11} = 27 kΩ	–	5.5	–	MHz
f_{VCO2}	free-running frequency	R_{11} = 27 kΩ	–	5.74	–	MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulators VCO1 and VCO2 (continued)						
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	R_{11} = 27 kΩ	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz
Output amplifiers AF1 (pin 8) and AF2 (pin 7) and overall performance						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 μs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment at pin 9	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
	at pin 10		–	1.1	2.2	kΩ
THD	total harmonic distortion at pin 8	with 50 μs de-emphasis	–	0.1	0.3	%
	at pin 7		–	0.25	0.5	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 μs de-emphasis; m = 0.3; Δf_i = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 μs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB

Note to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.

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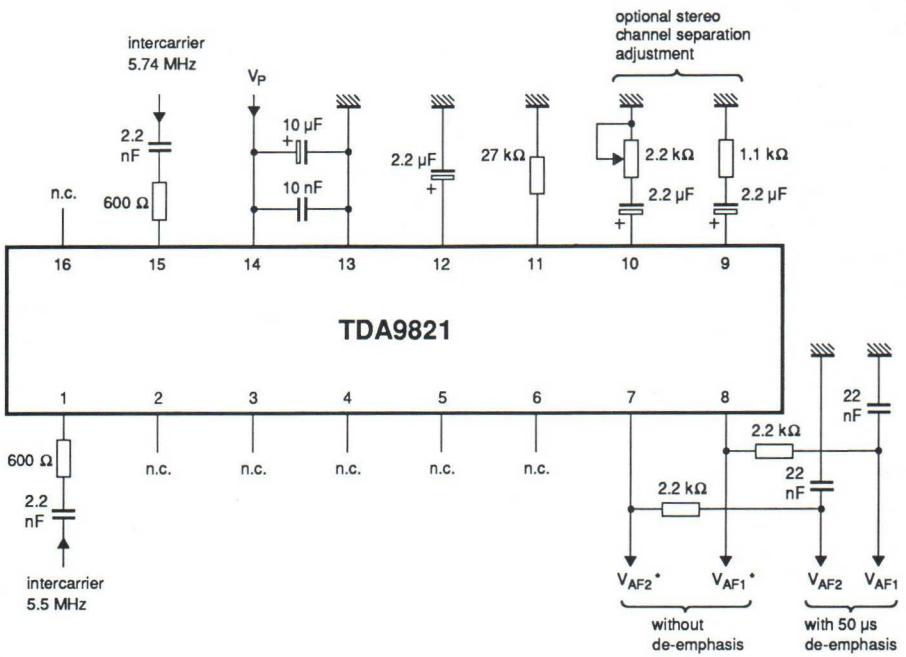


Fig.4 Test circuit.

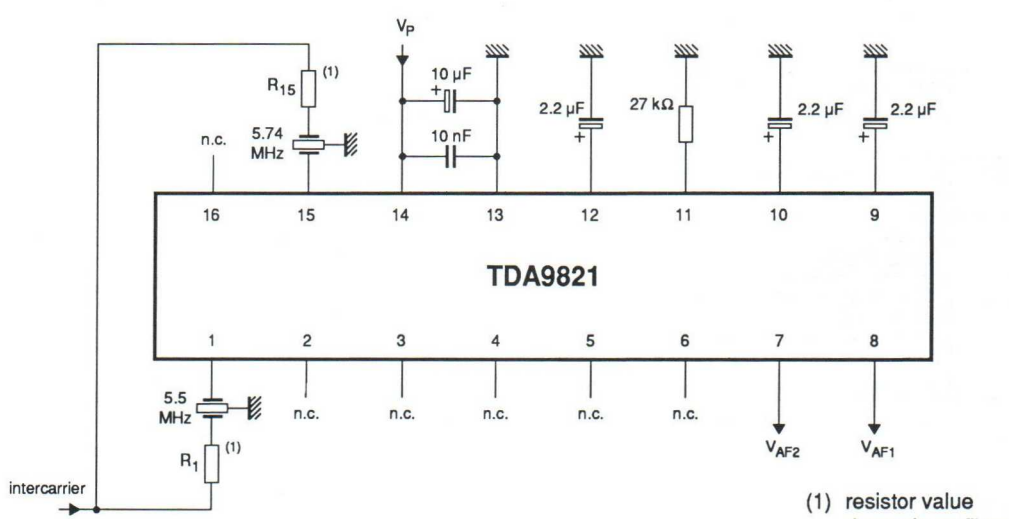


Fig.5 Application circuit.

TV sound AM-demodulator and audio source switch TDA9830

FEATURES

- Adjustment free wideband synchronous AM demodulator
- Audio source-mute switch (low noise)
- Audio level according EN50049
- 5 to 8 V power supply or 12 V alternative
- Low power consumption.

GENERAL DESCRIPTION

The TDA9830, a monolithic integrated circuit, is designed for AM-sound demodulation used in L- and L'-standard. The IC provides an audio source selector and also mute switch.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{14}	positive supply voltage	4.5	5.0	8.8	V
V_{11}	supply voltage (alternative)	10.8	12.0	13.2	V
$I_{14,11}$	supply current	24	30	36	mA
V_{i-16}	IF sensitivity (RMS value) (for –3 dB AF-signal)	–	60	100	μV
G_v	gain control	60	66	–	dB
V_6	AF output signal (m = 54%) (RMS value)	400	500	600	mV
V_6	S/N ratio acc. CCIR468-3 (IF-signal 10 mV_{RMS})	47	53	–	dB
$V_{7,9}$	AF input signal (for THD < 1.5%) (RMS value)	–	–	1.2	V
V_8	crosstalk and mute attenuation	80	90	–	dB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9830	16	DIL	plastic	SOT38GG
TDA9830T	16	SO	plastic	SOT109

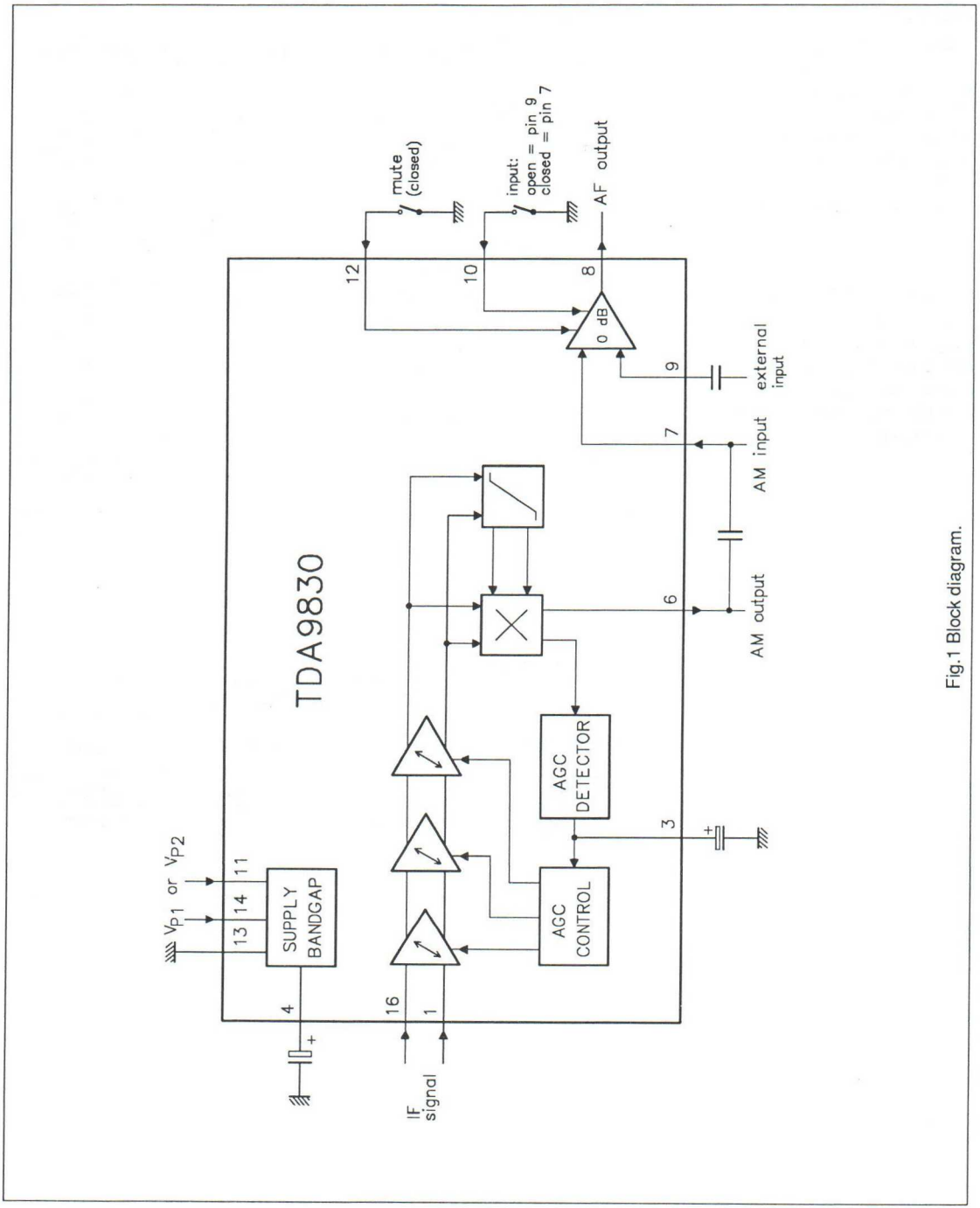


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IFIN	1	sound IF differential input signal
n.c.	2	not connected
C_{AGC}	3	AGC capacitor
C_{REF}	4	REF voltage filtering capacitor
n.c.	5	not connected
AMOUT	6	AM demodulator output
AMIN	7	input signal (from AM) to audio switch
AFOUT	8	output signal from audio switch
EXTIN	9	input signal (from external) to audio switch
SWITCH	10	switch input select control
V_{p2}	11	supply voltage +12 V (alternative)
MUTE	12	mute control
GND	13	ground (0 V)
V_{p1}	14	supply voltage +5 to +8 V
n.c.	15	not connected
IFIN	16	sound IF differential input signal

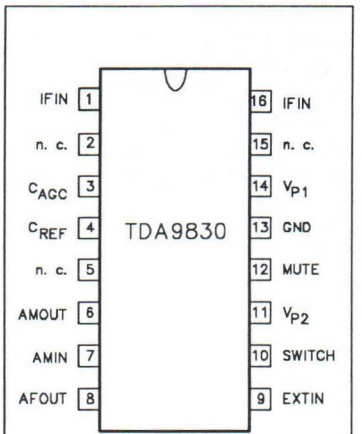


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Sound IF input

The sound IF amplifier consists of three AC-coupled differential amplifier stages each with approximately 20 dB gain. At the output of each stage is a multiplier for gain controlling (→ current distribution gain control). The overall control range is approximately –6 to +60 dB and the frequency response (–3 dB) of the IF amplifier is approximately 6 to 70 MHz. The steepness of gain control is approximately 10 mV/dB.

IF AGC

The automatic gain control voltage to maintain the AM demodulator output signal at a constant level is generated by a mean level detector. This AGC-detector charges and discharges the capacitor at pin 3 controlled by the output signal of the AM-demodulator compared to an internal reference voltage. The maximum charge/discharge current is approximately 5 μA. This value in combination with the value of the AGC capacitor and the AGC steepness determines the lower cut-off audio frequency and the THD-figure at low modulation frequency of the whole AM-demodulator. Therefore a large time constant has to be choosen which leads to slow AGC reaction at IF level change. To speed up the AGC in case of IF signal jump from low to high level, there is an additional comparator built in, which can provide additional discharge current from the AGC capacitor up to 5 mA in a case of overloading the AM demodulator by the internal IF signal.

AM-demodulator

The IF amplifier output signal is fed to a limiting amplifier (two stages) and to a multiplier circuit. However the limiter output signal (which is not any more AM modulated) is also fed to the multiplier, which provides AM demodulation (in phase demodulation). After lowpass filtering ($f_g \approx 400$ kHz) for carrier rejection and buffering, the demodulator output signal is present at pin 6. The AM demodulator operates over a wide frequency range, so that in combination with the frequency response of the IF amplifier applications in a frequency range from approximately 6 MHz up to 70 MHz are possible.

Audio switch

This circuit is an operational amplifier with three input stages and internal feedback network determining gain (0 dB) and frequency response ($f_g \approx 700$ kHz). Two of the input stages are connected to pin 7 and pin 9, the third input stage to an internal reference voltage. Controlled by the switching pins 10 and 12, one of the three input stages can be activated and a choice made between two different AF signals or mute state. The selected signal is present at pin 8. The decoupling capacitors at the input pins are needed, because the internally generated bias voltage for the input stages must not be influenced by the application in order to avoid DC-plop in case of switching.

The AM demodulator output is designed to provide almost the same DC voltage as the input bias voltage of the audio switch. But there may be spread between both voltages. Therefore it is possible to connect pin 6 directly to pin 7 (without a decoupling capacitor), but in this event the DC-plop for switching can increase up to 100 mV.

Reference circuit

This circuit is a band gap stabilizer in combination with a voltage regulation amplifier, which provides an internal reference voltage of about 3.6 V nearly independent from supply voltage and temperature. This reference voltage is filtered by the capacitor at pin 4 in order to reduce noise. It is used as a reference to generate all important voltages and currents of the circuit.

For application in 12 V power supply concepts, there is an internal voltage divider in combination with a Darlington transistor in order to reduce the supply voltage for all IC function blocks to approximately 6 V. This is necessary because of use of modern high frequency IC technology, where most of the used integrated components are only allowed to operate at maximum 9 V supply voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{14-13}	supply voltage V_{P1}	−0.5	+8.9	V
V_{11-13}	supply voltage V_{P2}	−0.5	+13.3	V
$V_{10,12-13}$	switching voltage	−0.5	V_P + 0.5	V
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	storage temperature	−25	+150	°C

Note to the limiting values

1. To avoid an inadmissible increase of ambient temperature, it is not allowed to short-circuit pin 11 for more than 10 seconds to ground.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT38	74 K/W
	SOT109	100 K/W

CHARACTERISTICS

V_{P1} = 5.0 V at pin 14; T_{amb} = +25 °C; sound carrier f_{SC} = 32.4 MHz modulated with f = 1 kHz and modulation depth m = 54%. IF input signal (sound carrier): V_{1-16} = 10 mV_{RMS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-13}	positive supply voltage V_{P1}	note 1	4.5	5.0	8.8	V
V_{11-13}	positive supply voltage V_{P2}	note 1	10.8	12.0	13.2	V
I_{11}/I_{14}	current consumption		24	30	36	mA
IF amplifier and gain control						
R_{1-16}	input resistance		1.75	2.2	2.65	kΩ
C_{1-16}	input capacitance		1.0	1.5	2.2	pF
V_{1-16}	minimum IF input signal (RMS value)	note 2	–	60	100	μV
V_{1-16}	maximum IF input signal (RMS value)	note 3	70	120	–	mV
G_v	gain control		60	66	–	dB
I_3	maximum AGC charging/discharging current		3.5	5	7	μA
I_3	fast AGC discharging current		–	–	5	mA
$V_3 - V_{13}$	gain control voltage ($G_{min} - G_{max}$)		1.5	–	2.8	V
B	–3 dB IF bandwidth	upper cut-off frequency	50	70	–	MHz
		lower cut-off frequency	–	6	10	MHz
$V_{1/16-13}$	DC potential		–	1.7	–	V
AM-Demodulator						
V_{6-13}	AF output signal (RMS value)		400	500	600	mV
B	–3 dB AF bandwidth	upper cut-off frequency	100	–	–	kHz
		lower cut-off frequency; note 7	–	–	20	Hz
V_{6-13}	THD		–	0.8	2	%
V_{6-13}	S/N (weighted acc. CCIR 468-3)		47	53	–	dB
V_{6-13}	DC potential		2.00	2.15	2.30	V
R_6	output resistance (emitter follower with 0.5 mA bias current)		–	300	–	Ω
I_{6abs}	allowable AC output current		–	–	0.3	mA
I_6	allowable DC output current		–	–	–0.5	mA
Audio-switch						
$V_{7,9-13}$	AF-input-signal for THD < 1.5% (RMS value)		–	–	1.2	V
V_{8-13}	S/N ratio of audio switch (in accordance with CCIR 468-3)	reference signal at pin 7/9 is 0.5 V_{RMS}	70	80	–	dB
B	–3 dB AF bandwidth	upper limit	100	–	–	kHz
V_{8-13}	THD at 1 V_{RMS} input signal at pin 7 or 9		–	0.1	1.0	%
V_{8-13}	crosstalk and mute attenuation	20 Hz to 20 kHz	80	90	–	dB
$V_{7,8,9-13}$	DC-potential		2.00	2.15	2.30	V
$R_{7,9-13}$	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{7,9-8}$	gain of audio switch		–0.5	0	+0.5	dB
V_{10-13}	audio switching voltage to activate pin 7		0	–	0.8	V
V_{10-13}	audio switching voltage to activate pin 9	note 4	1.5	–	V_P	V
V_{12-13}	input voltage for MUTE-ON		0	–	0.8	V
	input voltage for MUTE-OFF	note 4	1.5	–	V_P	V
$I_{10,12}$	output current of switching-pins at $V_{10,12-13} = 0$ V		–110	–145	–185	μA
V_{8-13}	DC-plop at AF output pin with switching from internal to external audio signal or to mute-state or vice-versa	note 5	–	5	10	mV
R_8	output resistance		70	100	150	Ω
Ripple rejection note 6						
RR	AF signal output: $\alpha_{RR} = V_{ripple}$ on V_P / V_{ripple} on V_{out}		26	30	–	dB
	AF signal output with AF signal from external source		40	44	–	dB

Notes to the characteristics

1. In the power supply voltage range V_{P1} = 5.0 V up to 8.0 V the performance will not change essentially. With power supply from V_{P2} = 12.0 V the performance will be comparable with the performance at V_{P1} = 5.0 V up to 8.0 V.
   The unused power supply pin must be not connected.
2. Start of gain control (low IF input signal) at –3 dB AF signal reduction at pin 6.
3. End of gain control (high IF input signal) at +1 dB AF signal expansion at pin 6.
4. This state is also valid for pin left open-circuit.
5. If a DC-plop of about maximum 100 mV is acceptable when switching from internal to external audio-signal or from internal to mute state or vice-versa, the capacitor between pin 6 and 7 can be omitted and pin 6 can be connected to pin 7.
6. Measured with V_{ripple} = 200 $mV_{(p-p)}$ at 70 Hz superimposed on supply voltage V_P.
7. Dependent on value of AGC capacitor.

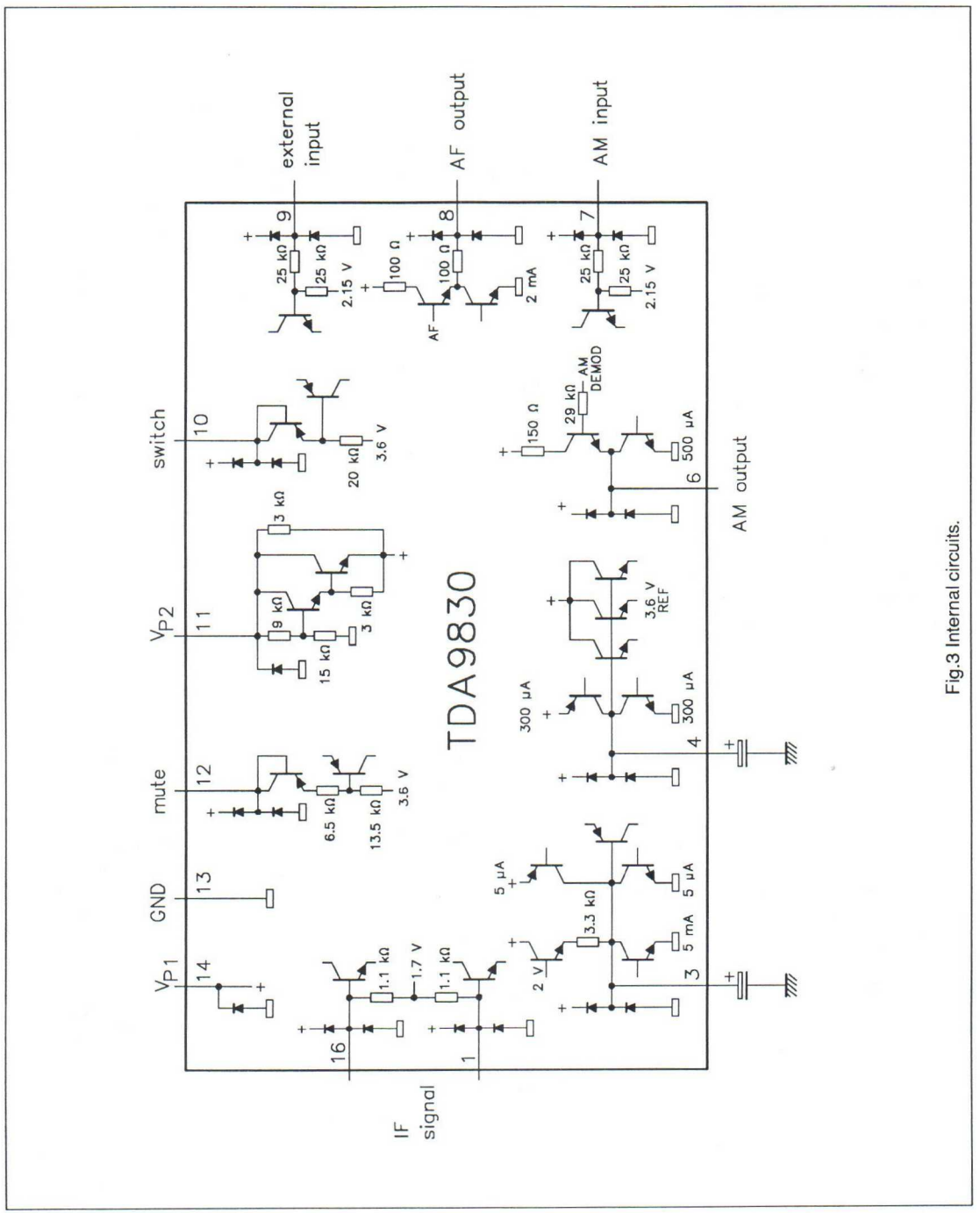


Fig.3 Internal circuits.

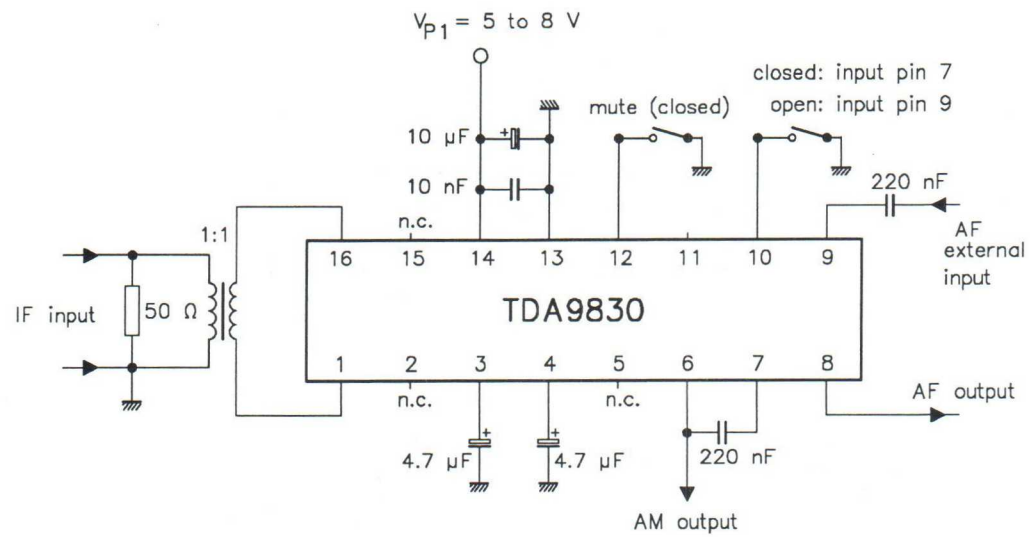


Fig.4 Test circuit 5 to 8 V supply.

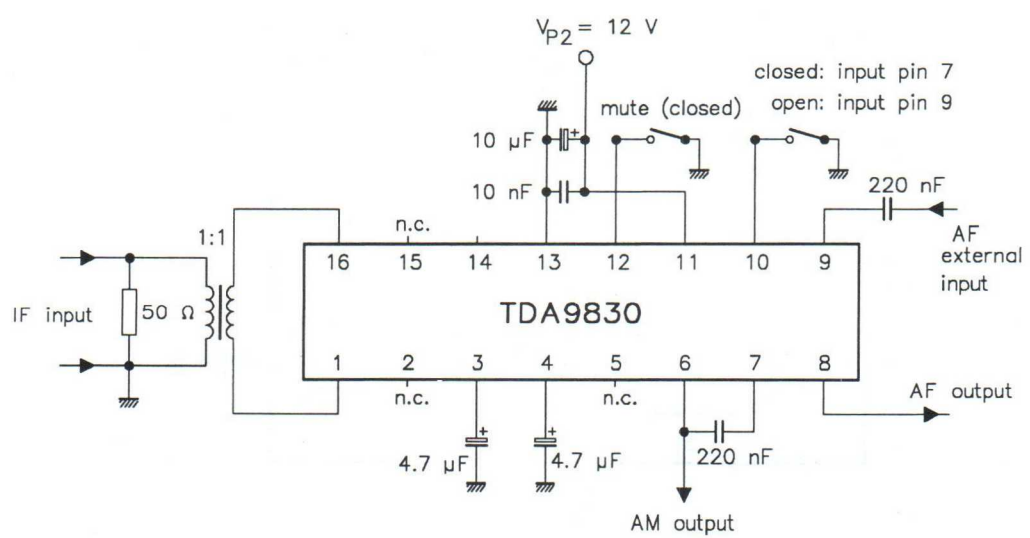


Fig.5 Test circuit 12 V supply.

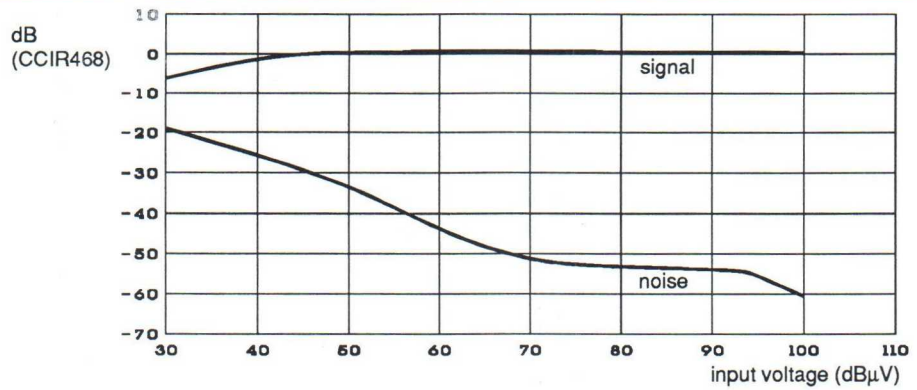


Fig.6 S/N figure as a function of the IF input signal.

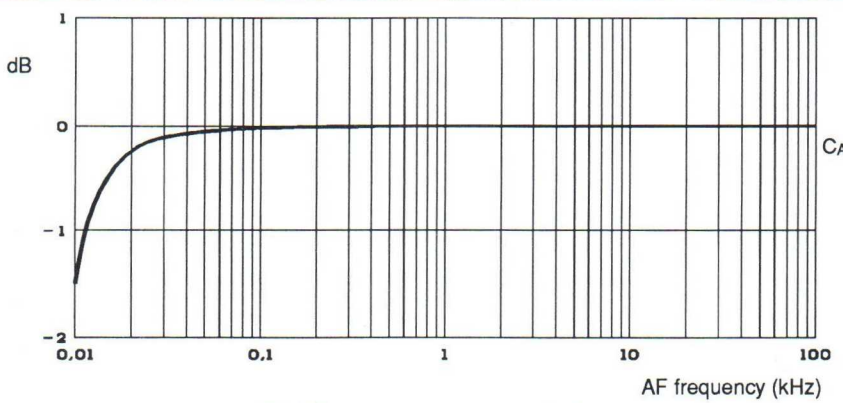


Fig.7 Frequency response at pin 6.

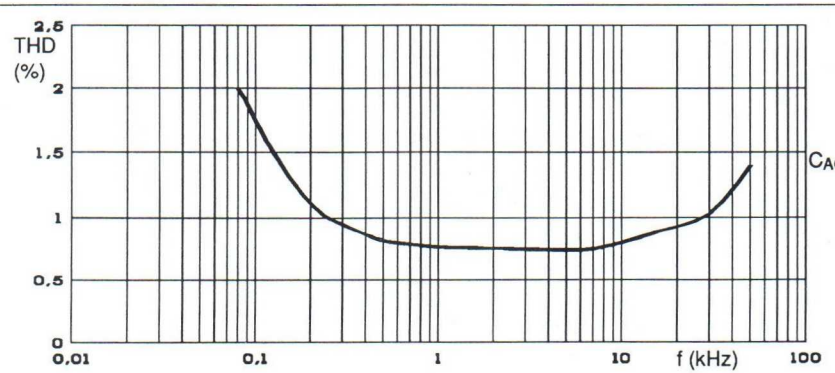


Fig.8 THD at pin 6.

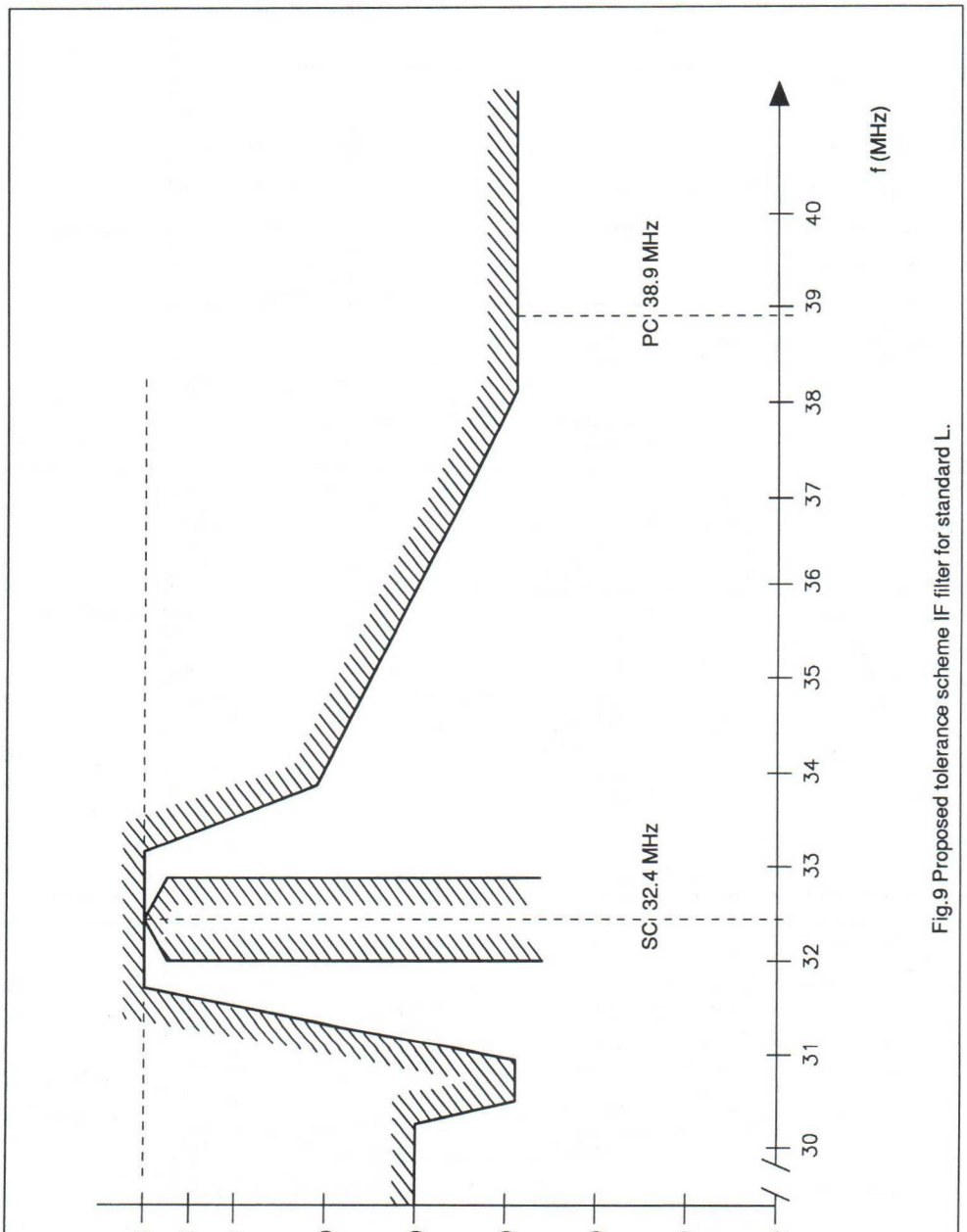


Fig.9 Proposed tolerance scheme IF filter for standard L.

With an IF filter according to this proposal, the video buzz suppression on the audio output is better than 50 dB (in accordance with CCIR468-3, m = 54%) for the worst case video modulation with 6 kHz sinewave black-to-white.

TV and VTR stereo/dual sound processor with digital identification and I²C-bus

TDA9840

FEATURES

- Supply voltage 5 to 8 V
- De-emphasis
- Source selector
- Level and stereo matrix adjustment possible via the I²C-bus
- I²C-bus transceiver
- AF inputs for NICAM or AM sound (standard L)
- AF outputs for Main and SCART
- AF input and output signals selectable via the I²C-bus
- Information for identified transmission mode is readable via I²C-bus
- Software is compatible with the TDA8415/16/17
- Quartz oscillator and clock generator
- Three digital PLL, alignment-free
- Two digital integrators, alignment-free
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection of all pins.

GENERAL DESCRIPTION

The TDA9840 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.3 s; identification concerning the main functions).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9840	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA9840T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)		15.5	16.5	20.5	mA
$V_{i(rms)}$	nominal input signal voltage (V_{i1}, V_{i2}, V_{i3}) (RMS value)	54% modulation	–	250	–	mV
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3% 54% modulation	–	500	–	mV
$V_{o(rms)}$	clipping level of the output signal voltages (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
ΔG_v	stereo control range for V_{i1} (0.1 dB steps)		+2.4	+2.5	+2.6	dB
			–2.3	–2.4	–2.5	dB
	level control range for V_{i2} (0.5 dB steps)		+2.4	+2.5	+2.6	dB
			–1.9	–2.0	–2.1	dB
$V_{i\,pil}$	input voltage sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"*	66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature range		0	–	+70	°C
f_{ident}	identification window width	normal mode				
		STEREO	2.0	–	2.0	Hz
		DUAL	2.3	–	2.3	Hz
		fast mode				
		STEREO	3.8	–	3.8	Hz
		DUAL	5.8	–	5.8	Hz
$t_{ident\ ON}$	total identification time ON	normal mode				
		STEREO	0.35	–	2.3	s
		DUAL	0.35	–	2.0	s
		fast mode				
		STEREO	0.175	–	1.1	s
		DUAL	0.175	–	1.0	s
$V_{i\,tuner}$	identification voltage sensitivity		–	28	–	dBμV
Δf_{pil}	pull-in frequency range of pilot PLL	f_ω = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz

BLOCK DIAGRAMS

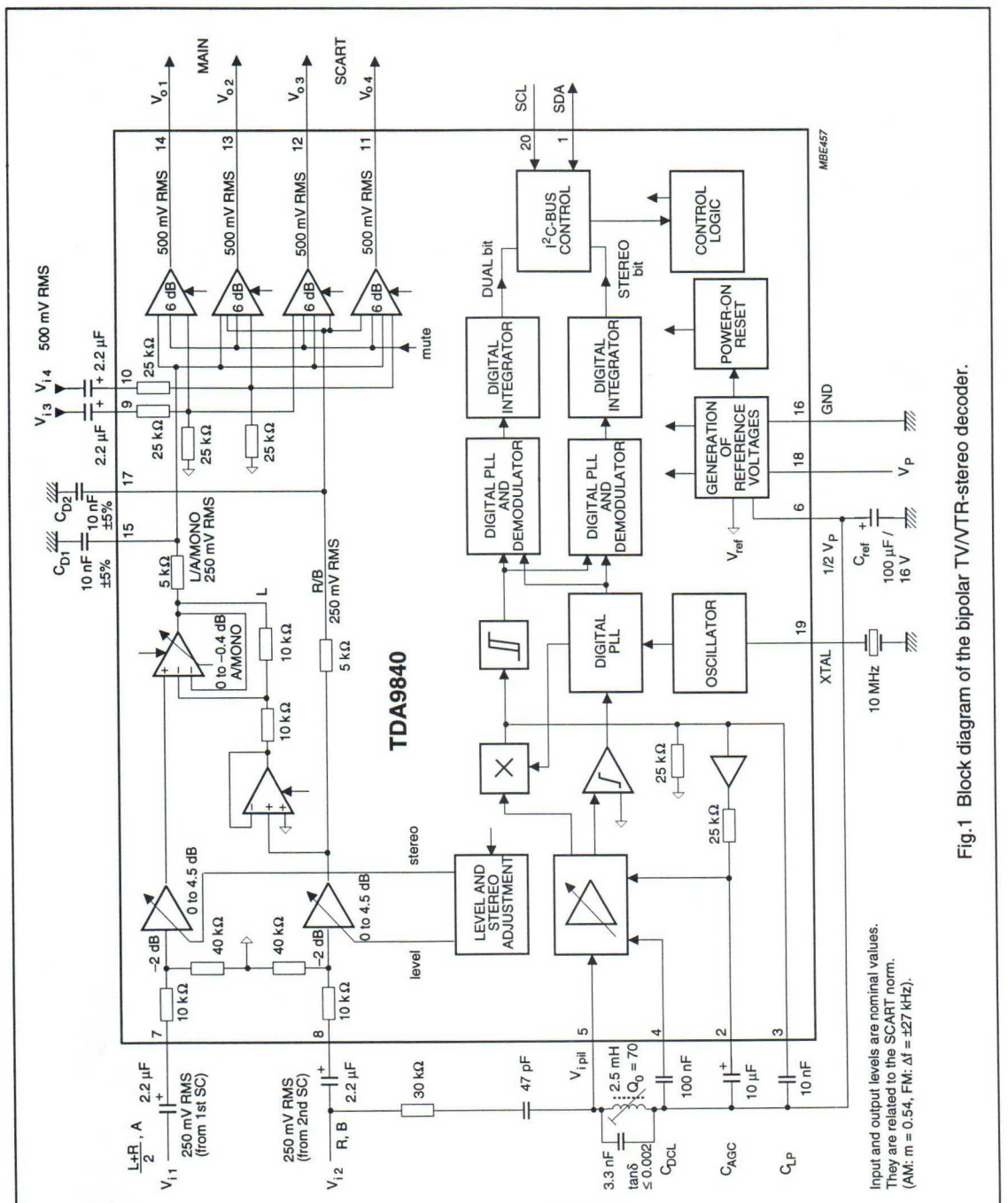


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

Input and output levels are nominal values. They are related to the SCART norm. (AM: m = 0.54, FM: Δf = ±27 kHz).

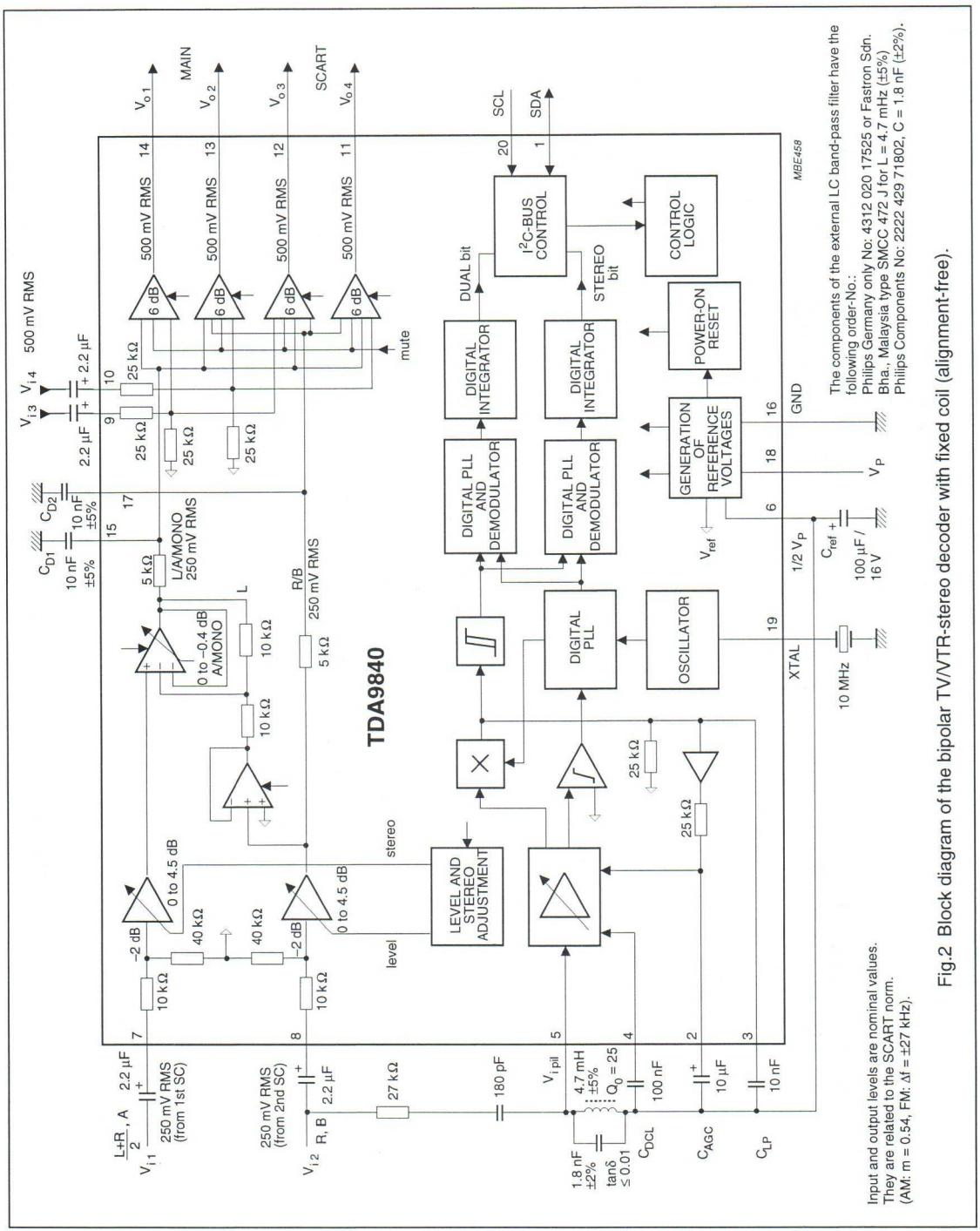


Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
C_{AGC}	2	AGC capacitor of pilot frequency amplifier
C_{LP}	3	identification low-pass capacitor
C_{DCL}	4	DC loop capacitor
$V_{i\,pil}$	5	pilot frequency input voltage
C_{ref}	6	capacitor of reference voltage ($\frac{1}{2}V_P$)
$V_{i\,1}$	7	AF input signal $V_{i\,1}$ (from 1st sound carrier)
$V_{i\,2}$	8	AF input signal $V_{i\,2}$ (from 2nd sound carrier)
$V_{i\,3}$	9	AF input signal $V_{i\,3}$ (NICAM or AM sound (standard L))
$V_{i\,4}$	10	AF input signal $V_{i\,4}$ (NICAM)
$V_{o\,4}$	11	AF output signal $V_{o\,4}$ (SCART)
$V_{o\,3}$	12	AF output signal $V_{o\,3}$ (SCART)
$V_{o\,2}$	13	AF output signal $V_{o\,2}$ (main)
$V_{o\,1}$	14	AF output signal $V_{o\,1}$ (main)
C_{D1}	15	50 µs de-emphasis capacitor of AF Channel 1
GND	16	ground (0 V)
C_{D2}	17	50 µs de-emphasis capacitor of AF Channel 2
V_P	18	supply voltage (+5 to +8 V)
XTAL	19	10 MHz crystal input
SCL	20	I²C-bus clock input

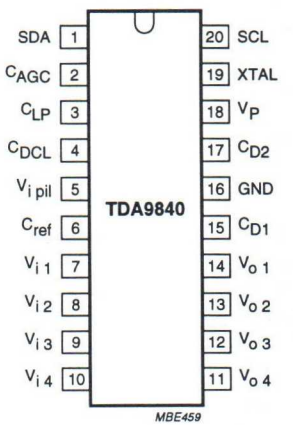


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9840 (see Fig.1) receives the signals from the FM-demodulators in a TV two sound-carrier system. The circuit is realized by the H00485 bipolar process.

The IC is intended for use in economic TV and VTR receivers. Therefore optimum relationship between integration of functions and use of external components has been striven for. Additionally a new type of identification circuit has been developed.

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers.The circuit incorporates level- and stereo-adjustment to correct the spreading in the FM detector output levels. Dematrixing uses the technique of two amplifiers processing the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs ('forced mono').

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.

A source selector, controlled via the I²C-bus, allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz / AM: m = 0.54) of 250 mV RMS ($V_{i\,1}$, $V_{i\,2}$), respectively 500 mV RMS ($V_{i\,3}$,$V_{i\,4}$). A nominal gain of 6 dB for $V_{i\,1}$ and $V_{i\,2}$ signals and 0 dB for $V_{i\,3}$ and $V_{i\,4}$ signals is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD ≤1.5%) is 1.6 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs $V_{o\,1}$, $V_{o\,2}$,$V_{o\,3}$ and $V_{o\,4}$. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC high-pass filter and single tuned LC band-pass filter to the input of a gain controlled amplifier. The external LC band-pass filter in combination with the external RC high-pass filter should have a loaded Q-factor of about 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of about 12 is proposed. This may cause a loss in sensitivity of about 2 to 3 dB. A digital PLL circuit generates a reference carrier, which is synchronized with the pilot carrier.

This reference carrier and the gain controlled pilot signal are fed to the AM-synchronous demodulator. The demodulator detects the identification signal, which is fed through a low-pass filter with external capacitor C_{LP} (pin 3) to a Schmitt-trigger for pulse shaping and suppression of low level spurious signal components. This is a measure against mis-identification.

The identification signal is amplified and fed through an AGC low-pass filter with external capacitor C_{AGC} (pin 2) to obtain the AGC voltage for controlling the gain of the pilot signal amplifier.

The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be read out via the I²C-bus.

A 10 MHz quartz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_p-variations from the transmitter can be tracked in case of missing synchronisation with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (approximately ±1 Hz) to reduce mis-identification.

Figure 2 shows an example of the alignment-free f_p band-pass filter. To achieve the required Q_L of approximately 12, the Q_0 at f_p of the coil was chosen to be approximately 25 (effective Q_0 including PCB influence). Using coils with other Q_0, the RC-network (R_{FP}, C_{FP}) has to be adapted accordingly. It is assumed that the loss factor tanδ of the resonance capacitor is ≤0.01 at f_p.

Copper areas under the coil might influence the loaded Q and have to be taken into account. Care has also to be taken in environments with strong magnetic fields when using coils without magnetic shielding.

I²C-bus transceiver

The complete IC is controlled by a microcomputer via the I²C-bus. The built-in I²C-bus transceiver transmits the identification result to the I²C-bus and receives the control data for the source selector and level control. The I²C-bus protocol is given in Tables 2 to 12 respectively.

The data transmission between the microcontroller and the other I²C-bus controlled ICs is not disturbed, when the supply voltage of the TDA9840 is not connected or when powering up or down. Finally, a Schmitt-trigger is built-in the SDA/SCL interface to suppress spikes from the I²C-bus.

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $\frac{1}{2}V_P$. For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{ref} = 100 µF/16 V in conjunction with the high ohmic input of the $\frac{1}{2}V_P$ pin (pin 6). Additional DC-load on this pin is prohibited.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, the 117/274 Hz integrator and the registers will be reset. Both AF channels (Main and SCART) are muted.

Fast mode / test mode

The TDA9840 has a fast mode (test mode) to reduce the integration time of the 117/274 Hz integrator from approximately 1 to 0.5 s.

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal pin loading diagram is given in Fig.7.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)		−0.3	10	V
V_i	voltage at pins 1 and 20		−0.3	5.5	V
V_i	voltage at pins 2 to 15, 17 and 19		−0.3	V_P	V
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{esd}	electrostatic handling for all pins	note 1	−	±300	V

Note

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP20	73	K/W
	SO20	90	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; nominal input signal $V_{i\,1,2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz); nominal input signal $V_{i\,3,4}$ = 0.5 V RMS value (AM: m = 0.54); nominal output signal $V_{o\,1,2,3,4}$ = 0.5 V RMS value; f_{AF} = 1 kHz; $V_{i\,pil}$ = 16 mV RMS value; f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with *"CCIR468-3"*, working oscillator frequency f_ω = 10.008 MHz; currents into the IC positive; measured in test circuit according to Fig.5, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)		15.5	16.5	20.5	mA
P_{tot}	total power dissipation		69.75	82.5	180.4	mW
$V_{n(DC)}$	DC voltage (pins 7 to 15 and 17)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$V_{ref(DC)}$	DC reference voltage (pin 6)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$I_{L(DC)}$	DC leakage current (pin 6)		–	–	±1	µA
AF Inputs; $V_{i\,1}$ and $V_{i\,2}$ (pins 7 and 8)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.25	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%; note 1				
		V_P = 5 V	0.625	0.715	–	V
		V_P = 8 V	1.050	1.200	–	V
		THD ≤ 1.5%; note 2				
		V_P = 5 V	0.780	0.900	–	V
		V_P = 8 V	1.300	1.500	–	V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 3	5	6	7	dB
ΔG_v (V_{o1})	stereo control range	only at pin 7	+2.4	+2.5	+2.6	dB
			–2.3	–2.4	–2.5	dB
	nominal step	maximum 49 steps	–	0.1	–	dB
ΔG_v (V_{o2})	level control range	only at pin 8	+2.4	+2.5	+2.6	dB
			–1.9	–2.0	–2.1	dB
	nominal step	maximum 9 steps	–	0.5	–	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 15 and 17)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF input pin (pins 9 and 10)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.5	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.25	1.40	–	V
		V_P = 8 V	2.10	2.35		V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 3	–1	0	1	dB
R_i	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF outputs (pins 11 to 14)						
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3%; 54% modulation	–	0.5	–	V
$V_{o(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		150	250	350	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	–	kΩ
B	frequency response (bandwidth)	f_i = 40 to 20000 Hz; note 4	−0.5	–	+0.5	dB
$B_{-3\ dB}$	frequency response	−3 dB; note 4	300	350	400	kHz
THD	total harmonic distortion	note 3	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"* (quasi-peak)	66	75	–	dB
α_{cr}	crosstalk attenuation for	notes 3 and 5				
	DUAL	$\lvert Z_s \rvert \leq 1$ kΩ	70	75	–	dB
	STEREO	$\lvert Z_s \rvert \leq 1$ kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_s \rvert \leq 1$ kΩ; note 3	76	80	–	dB
ΔV_{DC}	change of DC level output voltage between any two modes of operation	after switching	–	–	±10	mV
PSRR	power supply ripple rejection	f_r = 70 Hz; see Fig.6	50	65	–	dB
$I_{O(DC)}$	DC output current		–	–	±20	μA
α_{I2C}	noise from I²C-bus	note 6	–	90	80	dB
10 MHz crystal oscillator (pin 19)						
f_r	series resonant frequency of crystal (fundamental mode)	C_L = 20 pF	9.995	10.008	10.021	MHz
f_ω	working oscillator frequency (running in parallel resonance mode)	over operating temperature range including ageing and influence of drive circuit	9.988	10.008	10.028	MHz
R_r	equivalent crystal series resistance	even at extremely low drive level (<1 pW) over operating temperature range with C_0 = 6 pF	–	60	200	Ω
R_n	crystal series resistance of unwanted mode		2 × R_r	–	–	Ω
C_0	crystal parallel capacitance	with $R_r \leq 100$ Ω	–	6	10	pF
C_1	crystal motional capacitance		–	25	50	fF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{XTAL}	level of drive in operation		–	–	5	µW
$V_{OSC(p-p)}$	oscillator operating voltage (peak-to-peak value)		500	550	600	mV
Pilot processing						
$V_{i\ pil(rms)}$	pilot input voltage level at pin 5 (RMS value)	unmodulated	5	–	100	mV
$R_{i\ pil}$	pilot input resistance		500	1000	–	kΩ
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in frequency range (referred to f_{pil} = 54.6875 kHz)	f_ω = 9.988 MHz				
		lower side	–405	–	–405	Hz
		upper side	192	–	192	Hz
		f_ω = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz
		f_ω = 10.028 MHz				
		lower side	–188	–	–188	Hz
		upper side	411	–	411	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response	–3 dB	450	600	750	Hz
R_3	low-pass output resistance		18.75	25	31.25	kΩ
$V_{4(rms)}$	identification threshold voltage (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	high sensitivity	40	–	50	
	loaded quality factor of resonance circuit with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
$t_{acqui\ AGC}$	AGC acquisition time	$V_{i\ pil(rms)}$ switched from 0 to 100 mV RMS value	–	–	0.1	s
Identification (internal functions)						
$V_{i\ tuner}$	identification voltage sensitivity (pin 5)	note 7	–	28	–	dBµV
C/N	pilot carrier-to-noise ratio for start of identification	note 8	–	33	–	dB/Hz
H	hysteresis	note 7	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{det}	pull-in frequency range of identification PLL (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode lower side				
		STEREO	−0.38	–	−0.38	Hz
		DUAL	−0.69	–	−0.69	Hz
		normal mode upper side				
		STEREO	0.69	–	0.69	Hz
		DUAL	0.69	–	0.69	Hz
		fast mode lower side				
		STEREO	−0.89	–	−0.89	Hz
		DUAL	−2.05	–	−2.05	Hz
		fast mode upper side				
		STEREO	1.15	–	1.15	Hz
		DUAL	2.05	–	2.05	Hz
t_{det}	pull-in time of identification PLL (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode				
		STEREO	0	–	1.35	s
		DUAL	0	–	0.72	s
		fast mode				
		STEREO	0	–	0.57	s
		DUAL	0	–	0.25	s
f_{ident}	identification window frequency width (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode; note 9				
		STEREO	2.0	–	2.0	Hz
		DUAL	2.3	–	2.3	Hz
		fast mode; note 9				
		STEREO	3.8	–	3.8	Hz
		DUAL	5.8	–	5.8	Hz
t_{integr}	integrator time constant	normal mode	0.94	–	0.94	s
		fast mode	0.47	–	0.47	s
$t_{ident(on)}$	total identification time on	normal mode; note 10				
		STEREO	0.35	–	2.3	s
		DUAL	0.35	–	2.0	s
		fast mode; note 10				
		STEREO	0.175	–	1.1	s
		DUAL	0.175	–	1.0	s
$t_{ident(off)}$	total identification time off	normal mode; note 11				
		STEREO	0.6	–	1.6	s
		DUAL	0.6	–	1.6	s
		fast mode; note 11				
		STEREO	0.3	–	0.8	s
		DUAL	0.3	–	0.8	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus transceiver (pins 1 and 20)						
f_{CI}	clock frequency		0	–	100	kHz
I²C-bus: SCL (pin 20)						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
t_{low}	timing LOW period		4.7	–	–	µs
t_{high}	timing HIGH period		4.0	–	–	µs
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
I_{IL}	LOW level input current		–	–	−10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I²C-bus: SDA (pin 1)						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
t_{su}	data set-up time		0.25	–	–	µs
I_{IL}	LOW level input current		–	–	−10	µA
I_{OL}	LOW level output current		−3	–	–	mA
I_{IH}	HIGH level input current		–	–	10	µA

Notes

1. Input control amplifiers with $\Delta G_v = 0$ dB.
2. Input control amplifiers with $\Delta G_v = -2$ dB.
3. $V_o = 0.5$ V RMS value; f = 1 kHz; input control amplifiers with $\Delta G_v = 0$ dB.
4. Without de-emphasis capacitors with respect to nominal gain.
5. In dual mode: A (B)-signal into B (A) channel.
   In stereo mode: R-signal into left channel; L-signal = 0.
6. Test procedure tbf (same as TDA9855).
7. Tuner input signal, measured with PCALH reference front end (½EMF, 75 Ω, 2T/20T/white bar, 100% video) and $PC/SC_1 = 13$ dB; $PC/SC_2 = 20$ dB. The pilot band-pass has to be aligned.
8. Bandwidth of the pilot BP-filter $B_{-3\ dB} = 1.2$ kHz. $V_{i\,2}$ input driven with identification-modulated pilot carrier and white noise.
9. Identification window is defined as total pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
10. The maximum total system identification time ON is equal to $t_{ident(on)}$ plus $t_{acqui\ AGC}$ plus $t_{I^2C\ read\text{-}out}$.
11. The maximum total system identification time OFF is equal to $t_{ident(off)}$ plus $t_{I^2C\ read\text{-}out}$.

I²C-BUS PROTOCOL FOR THE TV AND VTR STEREO/DUAL SOUND PROCESSOR TDA9840

The TDA9840 has an I²C-bus interface with five registers: status, test, switch, level and stereo adjustment register controlled by a microcontroller via I²C-bus. The status register can be read and the other registers are write registers. The status byte represents the transmitter status detected by the identification circuit and the power-on reset status. The switch register controls the source selectors of the AF signal part, and the level and stereo adjustment register set the input level and stereo adjustment stage. Additionally, a test register is built-in to reduce the detection time of the identification circuit (test mode, fast mode respectively).

I²C-bus transceiver and data-handling (bus specification)

The TDA9840 is controlled by a microcomputer via the bidirectional 2-line I²C-bus. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

When the bus is free, both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change, when the clock signal on the SCL line is LOW. The set-up and hold times are specified in the Chapter "Characteristics"

A HIGH-to-LOW transition of the SDA line, while SCL is HIGH, is defined as the start condition. A LOW-to-HIGH transition of the SDA line, while SCL is HIGH, is defined as the stop condition. The bus transceiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Data format transmitter mode

For the data transmission no subaddress is to be transmitted, because there is only one read register implemented. So the total number of bytes reduces from three to two. The second byte represents the status of the IC.

Status register (see Table 4)

The bit D7 (PONRES) represents the status of the IC and indicates whether the power-on reset was activated by switching-on the supply voltage or a supply voltage breakdown.

If so, the I²C-bus transceiver, the digital PLLs and integrators are initialized and the PONRES bit is set to HIGH. After a successful reading of the status register, the bit D7 will be reset to LOW.

The bits D5 and D6 represent the transmitter status detected by the identification circuit (stereo, dual or mono transmission). The other bits are set to 0 (default).

Data format for the receiver

Table 1 Registers for receiver mode (see Table 6)

REGISTER	VALUE
Switch register	$(00)_{HEX}$
Port register	$(01)_{HEX}$ (without function)
Level adjustment register	$(02)_{HEX}$
Stereo adjustment register	$(03)_{HEX}$
Test register	$(04)_{HEX}$

The port register is without function, because this IC has no control ports as TDA8415/6/7. A data byte for the subaddress $(01)_{HEX}$ will not be stored in any register. An acknowledge will be sent to the microcontroller.

The first byte of the data transmission is the slave address and the second byte is the subaddress indicating the data register in which the data shall be stored. Starting from subaddress $(00)_{HEX}$ the n-th data byte will automatically be stored under subaddress n – 1.

All 8 bits of the subaddress are decoded by the device. The subaddresses from $(04)_{HEX}$ to $(FF)_{HEX}$ are forbidden for the user. If the I²C-bus transceiver receives subaddresses from $(05)_{HEX}$ to $(FF)_{HEX}$, no acknowledge will be sent back to the microcontroller.

Switch register

The source selector is controlled by the switch register. Table 7 shows the modes of operation. Note, that in the event of the external operation mode, no further selection is possible.

Level adjustment register

The information about the level adjustment of the AF channel $V_{i\,2}$ (pin 8) is stored in the level adjustment register (see Table 10). There are 10 steps (positions) of the AF level adjustment stage. The level range is from 2.5 dB up to −2.0 dB in 0.5 dB steps.

After a power-on reset, the data byte of the level adjustment register will be set to $(00)_{HEX}$: 0 dB gain at the AF input $V_{i\,2}$.

Stereo adjustment register

The information about the stereo adjustment of the AF channel $V_{i\,1}$ (pin 7) is stored in the stereo adjustment register (see Table 11). There are 50 steps (positions) of the AF stereo adjustment stage. The stereo range is from 2.5 dB up to −2.4 dB in 0.1 dB steps.

After a power-on reset, the data byte of the stereo adjustment register will be set to $(00)_{HEX}$: 0 dB gain at the AF input $V_{i\,1}$.

Test register (also used for fast mode)

Table 12 shows the meaning of the test register. The integration time of the integrator is approximately 1 s (normal mode, default). If the data byte of this register is set to HIGH, the integration time is reduced from approximately 1 to approximately 0.5 s (fast mode, test mode). The pull-in ranges of the identification PLLs are changed to:

Stereo: −0.89/+1.15 Hz

Dual: ±2.05 Hz.

If the integration time of the integrator is switched from one mode to the other (i.e. from fast mode/test mode to normal mode), the status register bits D5 and D6 might set to zero internally (MONO). Therefore, the previous status register information has to be stored by the microcontroller until the transmitter status is detected again by the identification circuit (now in the new mode) the first time.

The data byte of the test register can be reset in two different ways to $(00)_{HEX}$: integration time approximately 1 s, normal mode:

- after a power-on reset, for instance by switching the power supply V_p off and on again
- data transmission via I²C-bus for the test register (see Table 12).

Level and stereo adjustment

For the level and stereo adjustment of both AF channels $V_{i\,1}$ and $V_{i\,2}$, the following procedure will be recommended.

Level adjustment of the AF channel $V_{i\,2}$

- Feeds AF signal at the input $V_{i\,2}$
- Sets the data byte of the switch register (dual mode) to $(1A)_{HEX}$
- Measures the signal at the outputs $V_{o\,2}$ or $V_{o\,4}$
- Adjusts the output level with the level adjustment register.

Stereo adjustment of the AF channel $V_{i\,1}$

- Feeds AF stereo signals at the inputs $V_{i\,1}$ ((L+R)/2) and $V_{i\,2}$ (R)
- Sets the data byte of the switch register (stereo mode) to $(2A)_{HEX}$
- Measures the crosstalk attenuation between $V_{o\,1}$ and $V_{o\,2}$ or $V_{o\,3}$ and $V_{o\,4}$
- Adjusts the crosstalk attenuation with the stereo adjustment register.

During the stereo adjustment the data byte of the level adjustment register does not change.

After the level and stereo adjustment, the bytes of the level and stereo adjustment register must be stored by the microcontroller in a memory. (To avoid mis-adjustment it would be wise to compare the stored bytes with the proper adjustment bytes). If the PONRES bit of the status register will be set to HIGH (see status register) the data bytes for these both registers must be sent out of the memory to the TDA9840 via I²C-bus. Also the data byte of the switch register (see Table 7) must be changed, because the AF outputs are muted.

I²C-BUS FORMAT

X is the read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter). If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Table 2 I²C-bus; SLAVE ADDRESS/SUBADDRESS/DATA format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

Table 3 Explanation of Table 2

BIT	FUNCTION
S	start condition
SLAVE ADDRESS	1000 010X
A	acknowledge, generated by the slave
SUBADDRESS	dual sound A/B
DATA	data byte, see Table 6
P	stop condition

Table 4 I²C-bus; SLAVE ADDRESS/DATA to read the status byte (X = 1 in the address byte)

FUNCTION	SLAVE ADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	1000 0101	PONRES	ST	DS	0	0	0	0	0

Table 5 Explanation of Table 4

BIT	FUNCTION
PONRES = 0	after a successful reading of the status register
PONRES = 1	after power-on reset or after supply breakdown
ST = 0; DS = 0	MONO sound identified
ST = 0; DS = 1	DUAL sound identified
ST = 1; DS = 0	STEREO sound identified
ST = 1; DS = 1	incorrect identification

Table 6 I²C-bus; SUBADDRESS/DATA for writing (X = 0 in the address byte)

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Switching	0000 0000	0	SW6	SW5	SW4	SW3	SW2	SW1	SW0
Without function (note 1)	0000 0001	0	0	0	0	0	0	0	0
Level adjustment	0000 0010	0	0	0	0	LV3	LV2	LV1	LV0
Stereo adjustment	0000 0011	0	0	ST5	ST4	ST3	ST2	ST1	ST0

Note

1. This byte is acknowledged by the TDA9840.

Function of the bits:

- SW6 to SW0 input and output AF selection; see Table 7
- LV3 to LV0 level adjustment; see Table 9
- ST5 to ST0 stereo adjustment; see Table 11.

Table 7 Data byte to select AF inputs and AF outputs [subaddress $(00)_{HEX}$]

TRANSMISSION MODE		INPUT SIGNAL				OUTPUT SIGNAL				DATA								
		ST/DS/M		EXT		MAIN		SCART										
		V_{i1} PIN 7	V_{i2} PIN 8	V_{i3} PIN 9	V_{i4} PIN 10	V_{o1} PIN 14	V_{o2} PIN 13	V_{o3} PIN 12	V_{o4} PIN 11	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	00
MONO	M	M	–	–	–	M	M	M	M	0	0	0	1	0	0	0	0	10
STEREO	ST	S	R	–	–	S	S	S	S	0	0	0	1	0	0	0	0	10
		S	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	2A
DUAL	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	12
		A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	1A
		A	B	–	–	A	B	B	A	0	0	0	1	0	1	1	0	16
		A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	1E
External	–	–	–	C	D	C	D	C	D	0	1	1	1	1	0	1	0	7A

Table 8 Explanation of Table 7

SIGNAL	DESCRIPTION
R	right
L	left
S	$\frac{(L+R)}{2}$
A and B	dual sound A/B

SIGNAL	DESCRIPTION
C	NICAM or AM sound (standard L)
D	NICAM
M	mono sound
DS	dual sound
ST	stereo sound

Table 9 AF switch configuration

INPUT		OUTPUT	
TRANSMITTER STATUS	**SIGNAL**	**MAIN**	**SCART**
MONO	M	M	M
		M	M
STEREO	L	L or M	L or M
	R	R or M	R or M
DUAL	A	A	A or B
	B	B	A or B
External	C	C	C
	D	D	D

Table 10 Data byte to select level adjustment [subaddress $(02)_{HEX}$]

ΔG_V (dB)	DATA								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
+2.5	0	0	0	0	1	1	0	1	0D
+2.0	0	0	0	0	1	1	0	0	0C
+1.5	0	0	0	0	1	0	1	1	0B
+1.0	0	0	0	0	1	0	1	0	0A
+0.5	0	0	0	0	1	0	0	1	09
0	0	0	0	0	0	0	0	0	00
−0.5	0	0	0	0	0	0	0	1	01
−1.0	0	0	0	0	0	0	1	0	02
−1.5	0	0	0	0	0	0	1	1	03
−2.0	0	0	0	0	0	1	0	0	04

Table 11 Data byte to select stereo adjustment (subaddress $(03)_{HEX}$)

ΔG_V (dB)	DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
+2.5	0	0	1	1	1	0	0	1	39
+2.4	0	0	1	1	1	0	0	0	38
+2.3	0	0	1	1	0	1	1	1	37
+2.2	0	0	1	1	0	1	1	0	36
+2.1	0	0	1	1	0	1	0	1	35
+2.0	0	0	1	1	0	1	0	0	34
+1.9	0	0	1	1	0	0	1	1	33
+1.8	0	0	1	1	0	0	1	0	32
+1.7	0	0	1	1	0	0	0	1	31
+1.6	0	0	1	1	0	0	0	0	30
+1.5	0	0	1	0	1	1	1	1	2F
+1.4	0	0	1	0	1	1	1	0	2E
+1.3	0	0	1	0	1	1	0	1	2D
+1.2	0	0	1	0	1	1	0	0	2C
+1.1	0	0	1	0	1	0	1	1	2B
+1.0	0	0	1	0	1	0	1	0	2A
+0.9	0	0	1	0	1	0	0	1	29
+0.8	0	0	1	0	1	0	0	0	28
+0.7	0	0	1	0	0	1	1	1	27
+0.6	0	0	1	0	0	1	1	0	26
+0.5	0	0	1	0	0	1	0	1	25
+0.4	0	0	1	0	0	1	0	0	24
+0.3	0	0	1	0	0	0	1	1	23
+0.2	0	0	1	0	0	0	1	0	22
+0.1	0	0	1	0	0	0	0	1	21

ΔG_V (dB)	DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	0	0	00
−0.1	0	0	0	0	0	0	0	1	01
−0.2	0	0	0	0	0	0	1	0	02
−0.3	0	0	0	0	0	0	1	1	03
−0.4	0	0	0	0	0	1	0	0	04
−0.5	0	0	0	0	0	1	0	1	05
−0.6	0	0	0	0	0	1	1	0	06
−0.7	0	0	0	0	0	1	1	1	07
−0.8	0	0	0	0	1	0	0	0	08
−0.9	0	0	0	0	1	0	0	1	09
−1.0	0	0	0	0	1	0	1	0	0A
−1.1	0	0	0	0	1	0	1	1	0B
−1.2	0	0	0	0	1	1	0	0	0C
−1.3	0	0	0	0	1	1	0	1	0D
−1.4	0	0	0	0	1	1	1	0	0E
−1.5	0	0	0	0	1	1	1	1	0F
−1.6	0	0	0	1	0	0	0	0	10
−1.7	0	0	0	1	0	0	0	1	11
−1.8	0	0	0	1	0	0	1	0	12
−1.9	0	0	0	1	0	0	1	1	13
−2.0	0	0	0	1	0	1	0	0	14
−2.1	0	0	0	1	0	1	0	1	15
−2.2	0	0	0	1	0	1	1	0	16
−2.3	0	0	0	1	0	1	1	1	17
−2.4	0	0	0	1	1	0	0	0	18

Table 12 Data byte to select integration time [subaddress $(04)_{HEX}$]

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Test byte	0000 0100	X	X	X	X	X	X	INTFU	INT1SN

Function of the bits:

- INTFU = 0 integrator function disabled
- INTFU = 1 integrator function enabled
- INT1SN = 0 integration time approximately 1 s (default)
- INT1SN = 1integration time approximately 0.5 s.

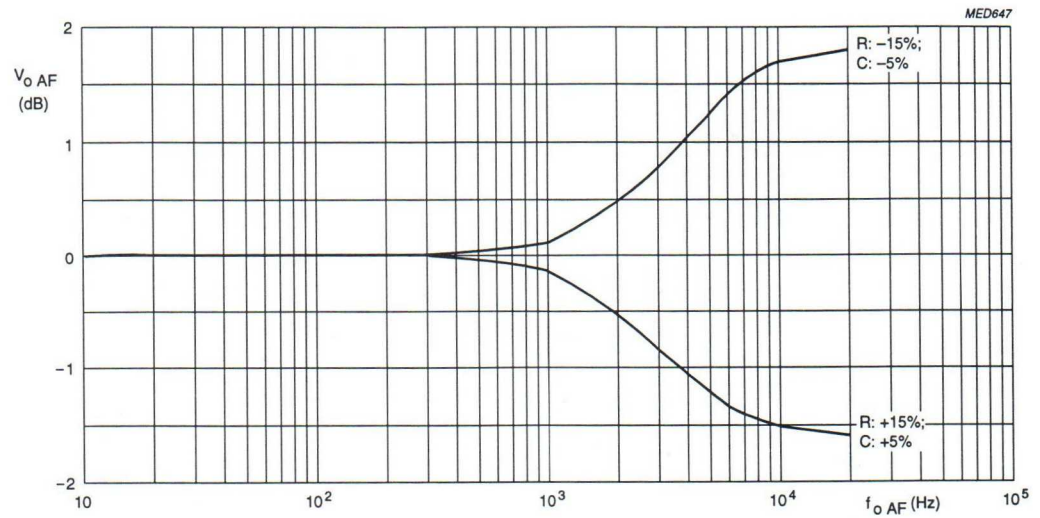


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%), $R_{internal}$ = 5 kΩ (±15%).

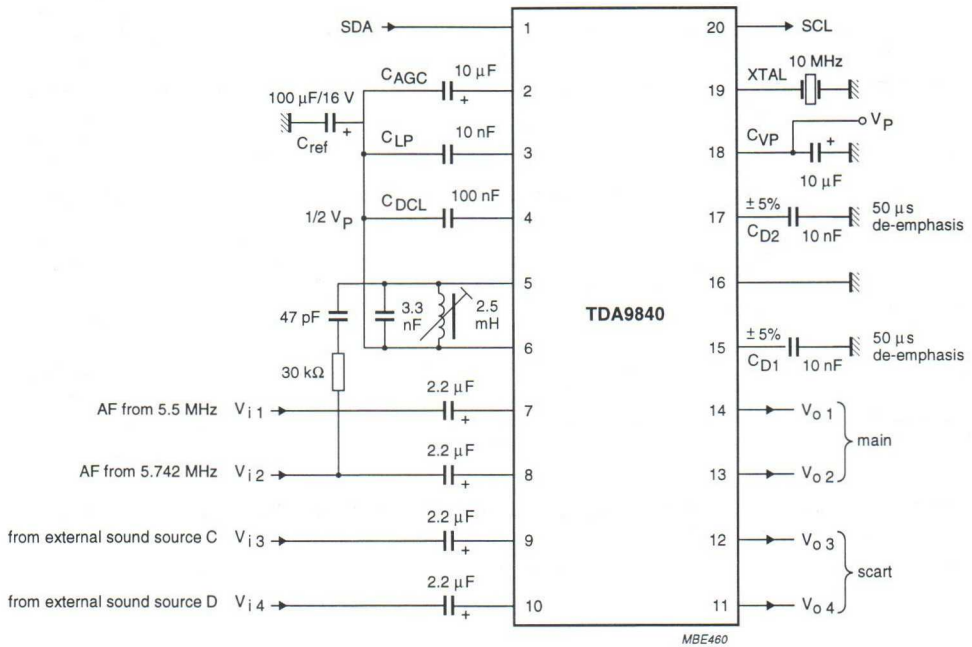


Fig.5 Test circuit of the stereo decoder TDA9840.

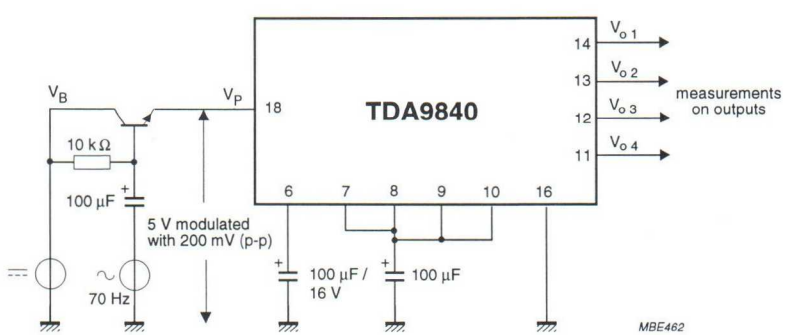


Fig.6 Test circuit for measurement of ripple rejection.

INTERNAL CIRCUITRY

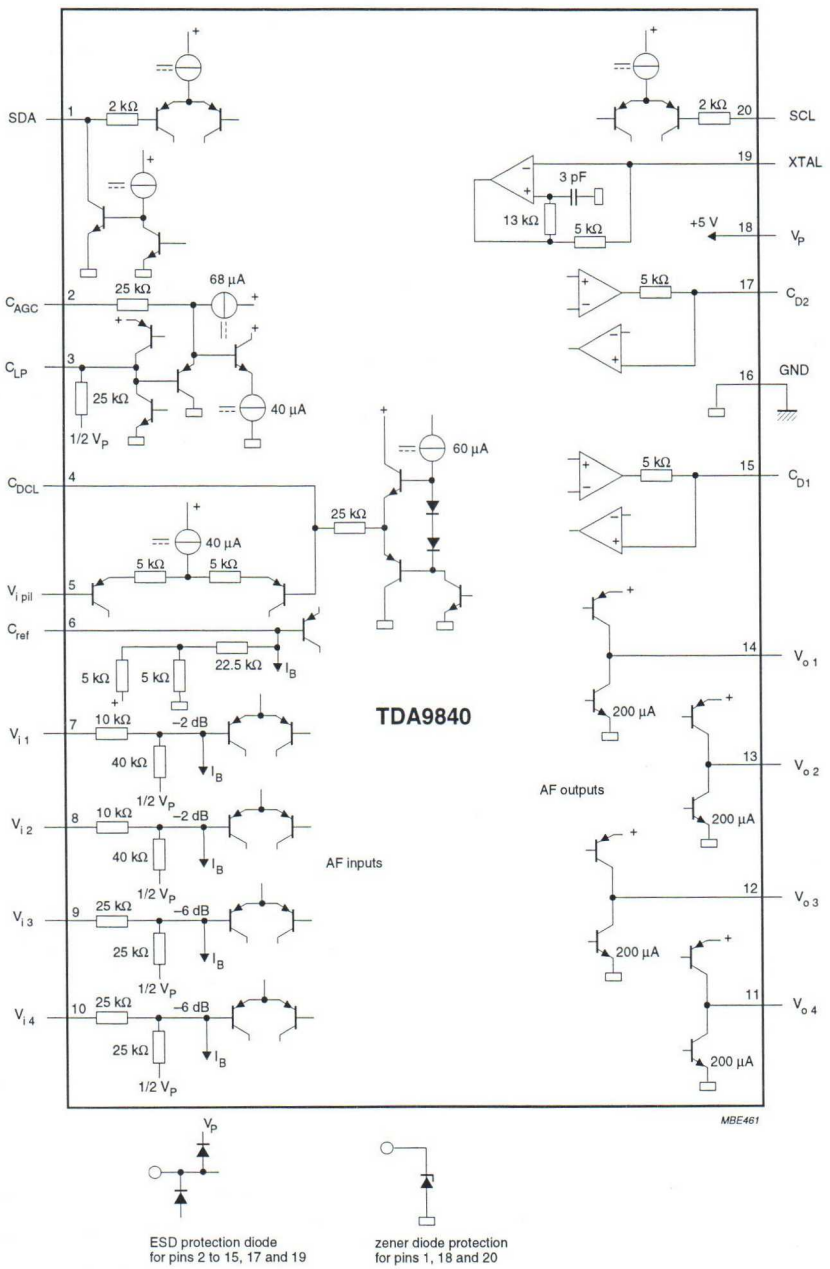


Fig.7 Internal circuits.

TV and VTR stereo/dual sound processor with digital identification

TDA9845

FEATURES

- Supply voltage 5 to 8 V
- Source selector
- Stereo matrix
- AF input for mono source
- AF outputs for Main
- LED operation mode indication (stereo and dual)
- High identification reliability.

GENERAL DESCRIPTION

The TDA9845 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.1 s; identification concerning the main functions).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)	without LED current	12	13	16.5	mA
$V_{i(rms)}$	nominal input signal voltage ($V_{i\,1}$, $V_{i\,2}$, $V_{i\,3}$) (RMS value)	54% modulation				
		B/G	–	250	–	mV
		L (only for $V_{i\,1}$)	–	500	–	mV
$V_{o(rms)}$	nominal output signal voltage (RMS value)	54% modulation	–	500	–	mV
$V_{o(rms)}$	clipping level of the output signal voltages (RMS value)	THD ≤1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
I_{LON}	input current	LED ON	–	–	12	mA
$V_{i\,pil}$	input voltage sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"*	66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature range		0	–	+70	°C
f_{ident}	identification window width	STEREO	2.2	–	2.2	Hz
		DUAL	2.3	–	2.3	Hz
$t_{ident\ ON}$	total identification time ON		0.35	–	2.1	s
$V_{i\,tuner}$	identification voltage sensitivity		–	28	–	dBμV
Δf_{pil}	pull-in frequency range of pilot PLL	f_ω = 10.008 MHz				
		lower side	–296	–	–296	Hz
		upper side	302	–	302	Hz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9845	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA9845T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAMS

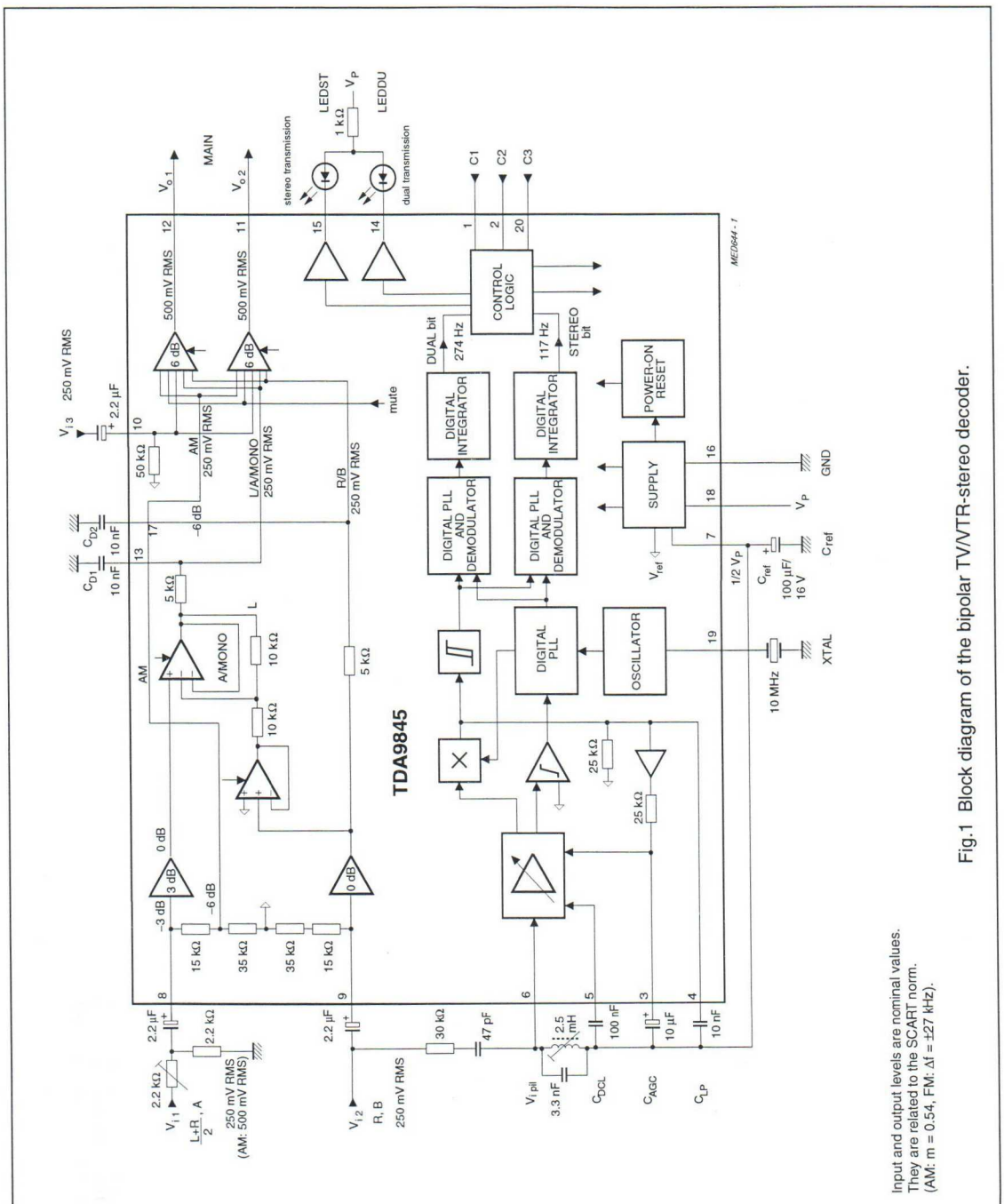
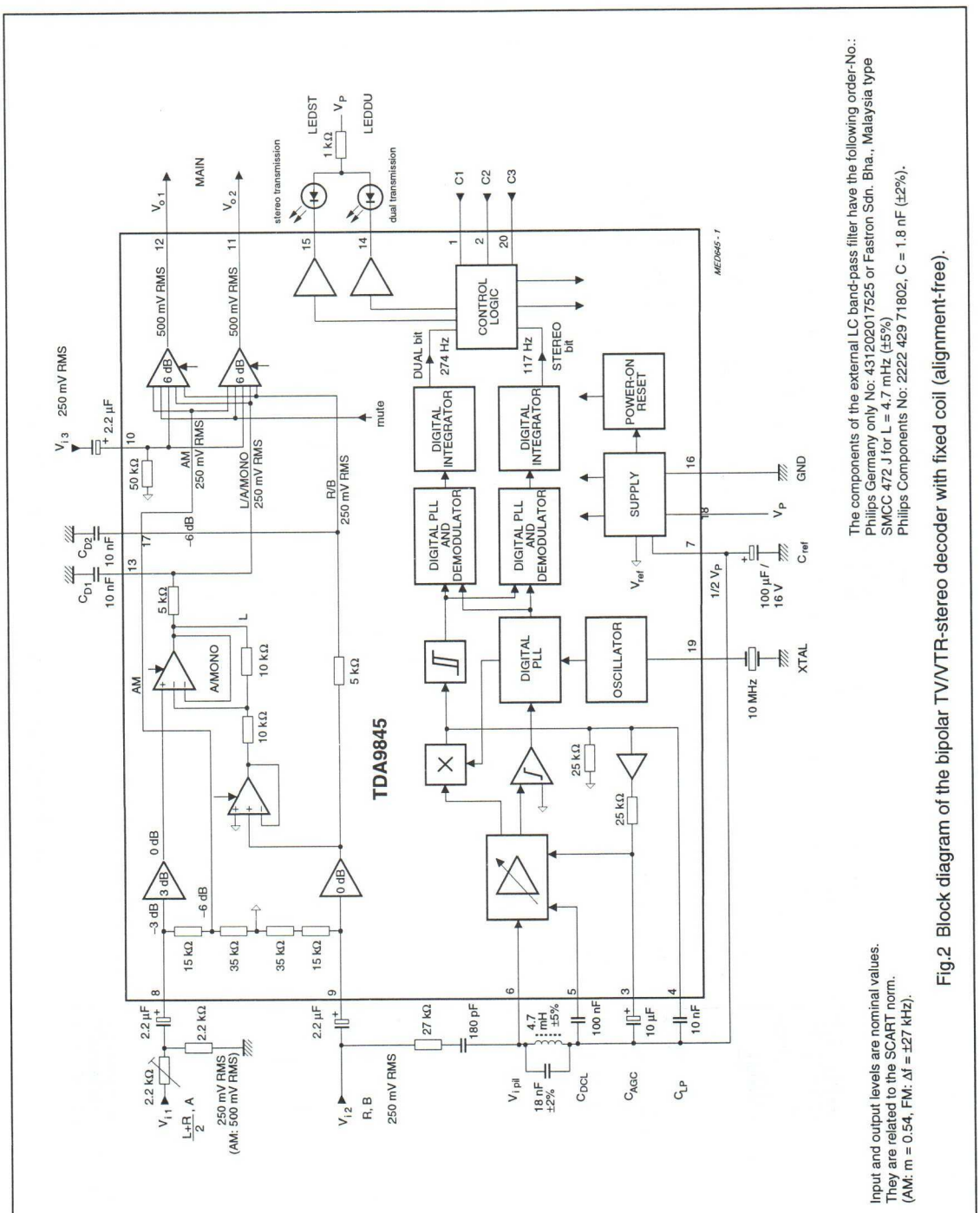


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

Input and output levels are nominal values.
They are related to the SCART norm.
(AM: m = 0.54, FM: Δf = ±27 kHz).



Input and output levels are nominal values.
They are related to the SCART norm.
(AM: m = 0.54, FM: Δf = ±27 kHz).

The components of the external LC band-pass filter have the following order-No.:
Philips Germany only No: 4312020175 25 or Fastron Sdn. Bha., Malaysia type
SMCC 472 J for L = 4.7 mHz (±5%)
Philips Components No: 2222 429 71802, C = 1.8 nF (±2%).

Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

PINNING

SYMBOL	PIN	DESCRIPTION
C1	1	control input Port C1
C2	2	control input Port C2
C_{AGC}	3	AGC capacitor of pilot frequency amplifier
C_{LP}	4	identification low-pass capacitor
C_{DCL}	5	DC loop capacitor
$V_{i\,pil}$	6	pilot frequency input voltage
C_{ref}	7	capacitor of reference voltage ($\frac{1}{2}V_P$)
$V_{i\,1}$	8	AF input signal voltage 1 (from sound carrier 1 or AM sound (standard L)
$V_{i\,2}$	9	AF input signal voltage 2 (from sound carrier 2)
$V_{i\,3}$	10	AF input signal voltage 3 (Mono sound)
$V_{o\,2}$	11	AF output signal voltage 2 (Main)
$V_{o\,1}$	12	AF output signal voltage 1 (Main)
C_{D1}	13	50 µs de-emphasis capacitor of AF Channel 1
LEDDU	14	LED (dual)
LEDST	15	LED (stereo)
GND	16	ground (0 V)
C_{D2}	17	50 µs de-emphasis capacitor of AF Channel 2
V_P	18	supply voltage (+5 to +8 V)
XTAL	19	10 MHz crystal input
C3	20	control input Port C3

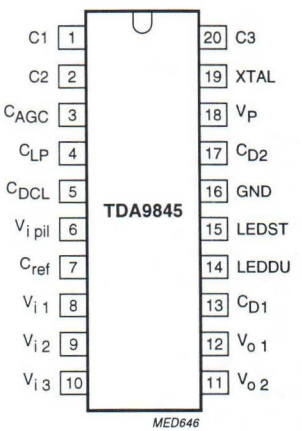


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers. Dematrixing uses the technique of two amplifiers processing the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs ('forced mono').

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.

A source selector, controlled via the control input ports allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz) of 250 mV RMS ($V_{i\,1}$, $V_{i\,2}$) and for a nominal input signal (AM: m = 0.54) of 500 mV RMS ($V_{i\,1}$), respectively 250 mV RMS ($V_{i\,3}$). A nominal gain of 6 dB for $V_{i\,1}$ and $V_{i\,2}$ signals (0 dB for $V_{i\,1}$ signal (AM sound)) and 6 dB for $V_{i\,3}$ signal is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD ≤1.5%) is 1.60 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs $V_{o\,1}$, $V_{o\,2}$. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC high-pass filter and single tuned LC band-pass filter to the input of a gain controlled amplifier. The external LC band-pass filter in combination with the external RC high-pass filter should have a loaded Q-factor of approximately 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of approximately 12 is proposed. This may cause a loss in sensitivity of approximately 2 to 3 dB. A digital PLL circuit generates a reference carrier, which is synchronized with the pilot carrier. This reference carrier and the gain controlled pilot signal are fed to the AM-synchronous demodulator. The demodulator detects the identification signal, which is fed through a low-pass filter with external capacitor C_{LP} (pin 4) to a Schmitt-trigger for pulse shaping and suppression of low level spurious signal components. This is a measure against mis-identification.

The identification signal is amplified and fed through an AGC low-pass filter with external capacitor C_{AGC} (pin 3) to obtain the AGC voltage for controlling the gain of the pilot signal amplifier.

The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be indicated via LEDs.

A 10 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_p-variations from the transmitter can be tracked in the event of missing synchronization with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (±1 Hz) to reduce mis-identification.

Figure 2 shows an example of the alignment-free f_p band-pass filter. To achieve the required Q_L of around 12, the Q_0 at f_p of the coil was chosen to be around 25 (effective Q_0 including PCB influence). Using coils with other Q_0, the RC-network (R_{FP}, C_{FP}) has to be adapted accordingly. It is assumed that the loss factor tanδ of the resonance capacitor is ≤0.01 at f_p.

Copper areas under the coil might influence the loaded Q and have to be taken into account. Care has also to be taken in environments with strong magnetic fields when using coils without magnetic shielding.

Control input ports

The complete IC is controlled by the three control input ports C1, C2 and C3 (TTL-level). With these ports the user can select between different AF sources according to the transmitter status (see Table 1). Finally Schmitt-triggers are added in the input port interfaces to suppress spikes from the control lines C1, C2 and C3.

After a power-on reset, the logic is reset (mute mode for the AF channel). After some time (≤1 ms), when the power-on reset is automatically deactivated, the switch position of the Main channel is changed according to the control input port levels C1, C2 and C3.

For standard L, the AM sound is fed via the AF input ($V_{i\,1}$) to the two AF outputs ($V_{o\,1}$,$V_{o\,2}$). This can also be achieved by feeding at AF input $V_{i\,3}$.

The logic level combination 111 of the control input ports (C3, C2 and C1) is **not allowed** (see Table 1).

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $\frac{1}{2}V_P$. For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{ref} = 100 µF/16 V in conjunction with the high ohmic input of the $\frac{1}{2}V_P$ pin (pin 7). No additional DC load on this pin is allowed.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, the 117/274 Hz integrator and the logic will be reset. The AF channel (Main) is muted (≤1 ms).

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal pin loading diagram is given in Fig.7.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)		−0.3	10	V
V_i	voltage at pins 1, 2 and 20		−0.3	9.0	V
V_i	voltage at pins 3 to 13, 17 and 19		−0.3	V_P	V
V_i	voltage at pins 14 and 15		−0.3	10	V
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{esd}	electrostatic handling for all pins	note 1	−500	+500	V

Note

1. Charge device model class A: discharging a 200 pF capacitor through a Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP20	73	K/W
	SO20	90	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; nominal input signal $V_{i\,1,\,2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz); nominal input signal $V_{i\,1}$ = 0.5 V RMS value (AM: m = 0.54); nominal input signal $V_{i\,3}$ = 0.25 V RMS value (AM: m = 0.54); nominal output signal $V_{o\,1,\,2}$ = 0.5 V RMS value; f_{AF} = 1 kHz; $V_{i\,pil}$ = 16 mV RMS value; f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with *"CCIR468-3"*, working oscillator frequency f_ω = 10008 MHz; currents into the IC positive; measured in test circuit Fig.5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)	without LED current	12	13	16.5	mA
P_{tot}	total power dissipation		54	65	145.2	mW
$V_{n(DC)}$	DC voltage (pins 8 to 13 and 17)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$V_{ref(DC)}$	DC reference voltage (pin 7)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$I_{L(DC)}$	DC leakage current (pin 7)		–	–	±1	µA
AF Inputs; $V_{i\,1}$ and $V_{i\,2}$ (pins 8 and 9)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation				
		B/G	–	0.25	–	V
		L (only $V_{i\,1}$)	–	0.5	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤1.5%				
		V_P = 5 V; B/G	0.625	0.715	–	V
		V_P = 8 V; B/G	1.050	1.200	–	V
		V_P = 5 V; L (only $V_{i\,1}$)	1.200	1.600	–	V
		V_P = 8 V; L (only $V_{i\,1}$)	2.100	2.356	–	V
G_v	AF signal voltage gain	G = V_o/V_i; note 1				
		B/G	5	6	7	dB
		L (only $V_{i\,1}$)	−1	0	+1	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 13 and 17)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF input pin (pin 10)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.25	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤1.5%				
		V_P = 5 V	0.625	0.715	–	V
		V_P = 8 V	1.050	1.200		V
G_v	AF signal voltage gain	G = V_o/V_i; note 1	5	6	7	dB
R_i	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF outputs (pins 11 and 12)						
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤0.3%; 54% modulation	–	0.5	–	V
$V_{o(rms)}$	clipping voltage level (RMS value)	THD ≤1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		150	250	350	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	–	kΩ
B	frequency response (bandwidth)	f_i = 40 to 20000 Hz; note 2	–0.5	–	+0.5	dB
$B_{-3\ dB}$	frequency response	–3 dB; note 2	300	350	400	kHz
THD	total harmonic distortion	note 1	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"* (quasi-peak)	66	75	–	dB
α_{cr}	crosstalk attenuation for	notes 1 and 3				
	DUAL	$\lvert Z_s \rvert \leq 1$ kΩ	70	75	–	dB
	STEREO	$\lvert Z_s \rvert \leq 1$ kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_s \rvert \leq 1$ kΩ; note 1	76	80	–	dB
ΔV_{DC}	change of DC level output voltage between any two modes of operation	after switching	–	–	±10	mV
PSRR	power supply ripple rejection	f_r = 70 Hz; see Fig.6	50	65	–	dB
$I_{O(DC)}$	DC output current		–	–	±20	μA
10 MHz crystal oscillator (pin 19)						
f_r	series resonant frequency of crystal (fundamental mode)	C_L = 20 pF	9.995	10.008	10.021	MHz
f_ω	working oscillator frequency (running in parallel resonance mode)	over operating temperature range including ageing and influence of drive circuit	9.988	10.008	10.028	MHz
R_r	equivalent crystal series resistance	even at extremely low drive level (<1 pW) over operating temperature range with C_0 = 6 pF	–	60	200	Ω
R_n	crystal series resistance of unwanted mode		$2 \times R_r$	–	–	Ω
C_0	crystal parallel capacitance	with $R_r \leq 100$ Ω	–	6	10	pF
C_1	crystal motional capacitance		–	25	50	fF
P_{XTAL}	level of drive in operation		–	–	5	μW
$V_{OSC(p-p)}$	oscillator operating voltage (peak-to-peak value)		500	550	600	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pilot processing						
$V_{i\ pil(rms)}$	pilot input voltage level at pin 6 (RMS value)	unmodulated	5	–	100	mV
$R_{i\ pil}$	pilot input resistance		500	1000	–	kΩ
$C_{i\ pil}$	pilot input capacitance		–	–	3	pF
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in frequency range (referenced to f_{pil} = 54.6875 kHz)	f_{ω} = 9.988 MHz				
		lower side	−405	–	−405	Hz
		upper side	192	–	192	Hz
		f_{ω} = 10.008 MHz				
		lower side	−296	–	−296	Hz
		upper side	302	–	302	Hz
		f_{ω} = 10.028 MHz				
		lower side	−188	–	−188	Hz
		upper side	411	–	411	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response	−3 dB	450	600	750	Hz
R_4	low-pass output resistance		18.75	25	31.25	kΩ
$V_{4(rms)}$	identification threshold voltage (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	HIGH sensitivity; see Fig.1	40	–	50	
	loaded quality factor of resonance circuit with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
$t_{acqui\ AGC}$	AGC acquisition time	$V_{i\ pil(rms)}$ switched from 0 to 100 mV RMS value	–	–	0.1	s
Identification (internal functions)						
$V_{i\ tuner}$	identification voltage sensitivity	note 4	–	28	–	dBμV
C/N	pilot carrier-to-noise ratio for start of identification	note 5	–	33	–	dB/Hz
H	hysteresis	note 4	–	–	2	dB
f_{det}	pull-in frequency range of identification PLL (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	lower side				
		STEREO	−0.63	–	−0.63	Hz
		DUAL	−0.69	–	−0.69	Hz
		upper side				
		STEREO	0.63	–	0.63	Hz
		DUAL	0.69	–	0.69	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{det}	pull-in time of identification PLL (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	STEREO	0	–	0.8	s
		DUAL	0	–	0.8	s
f_{ident}	identification window frequency width (referenced to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	STEREO; note 6	2.2	–	2.2	Hz
		DUAL; note 6	2.3	–	2.3	Hz
t_{integr}	integrator time constant		0.94	–	0.94	s
$t_{ident(on)}$	total identification time on	STEREO; note 7	0.35	–	2.0	s
		DUAL; note 7	0.35	–	2.0	s
$t_{ident(off)}$	total identification time off	STEREO; note 8	0.60	–	1.5	s
		DUAL; note 8	0.60	–	1.5	s
LED (pins 14 and 15)						
$V_{L(off)}$	output voltage	LED off	–	–	8.8	V
$V_{L(on)}$	output voltage	LED on	–	–	0.7	V
$I_{L(off)}$	input current	LED off	–	–	1	µA
$I_{L(on)}$	input current	LED on	–	–	12	mA
Control input ports C1, C2 and C3 (pins 1, 2 and 20)						
V_{CL}	LOW level input voltage		0	–	0.8	V
V_{CH}	HIGH level input voltage		2.4	–	8.8	V
I_{CL}	LOW level input current		–	–	–1	µA
I_{CH}	HIGH level input current		–	–	1	µA

Notes

1. V_o = 0.5 V RMS value; f = 1 kHz.
2. Without de-emphasis capacitors with respect to nominal gain.
3. In dual mode: A (B)-signal into B (A) channel.
   In stereo mode: R-signal into left channel; L-signal = 0.
4. Tuner input signal, measured with PCALH reference front end (½EMF, 75 Ω, 2T/20T/white bar, 100% video) and PC/SC_1 = 13 dB; PC/SC_2 = 20 dB. The pilot band-pass has to be aligned.
5. Bandwidth of the pilot BP-filter $B_{-3\ dB}$ = 1.2 kHz. $V_{i\,2}$ input driven with identification-modulated pilot carrier and white noise.
6. Identification window is defined as twice the pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
7. The maximum total system identification time ON is equal to $t_{ident(on)}$ plus $t_{acqui\ AGC}$.
8. The maximum total system identification time OFF is equal to $t_{ident(off)}$.

Table 1 Control input port matrix to select AF inputs and AF outputs

INPUT/OUTPUT	MODE	INPUT SIGNAL			OUTPUT SIGNAL		CONTROL INPUT			LED	
		ST/DS/M		EXT	MAIN		PORT(1)				
		V_{i1} PIN 8	V_{i2} PIN 9	V_{i3} PIN 10	V_{o1} PIN 12	V_{o2} PIN 11	C3 PIN 20	C2 PIN 2	C1 PIN 1	DUAL PIN 14	STEREO PIN 15
Mute; note 2	–	–	–	–	no signal		0	0	0	OFF	OFF
Sound mute	–	–	–	–	no signal		1	0	0	note 3	note 3
Mono	M	M	–	–	M	M	0	0	1	OFF	OFF
		M	–	–	M	M	0	1	0	OFF	OFF
		AM	–	–	AM	AM	0	1	1	OFF	OFF
Stereo	ST	S	R	–	L	R	0	0	1	OFF	ON
		S	R	–	S	S	0	1	0	OFF	ON
		S	R	–	S	S	0	1	1	OFF	ON
Dual	DS	A	B	–	A	B	0	0	1	ON	OFF
		A	B	–	A	A	0	1	0	ON	OFF
		A	B	–	B	B	0	1	1	ON	OFF
External; note 4	–	–	–	C	C	C	1	0	1	note 3	note 3
		–	–	C	C	C	1	1	0	OFF	OFF

Notes

1. The combination 111 is **not allowed**.
2. In mute mode the content of the 117 Hz/274 Hz integrator will be reset. The LEDs are switched OFF.
3. The LED show the identification status.
4. In external mode, in the combination 110 only the LEDs are switched OFF.

Table 2 Explanation of Table 1

SIGNAL	DESCRIPTION
R	right
L	left
S	$\frac{(L+R)}{2}$
A and B	dual sound A/B
C	external sound source
AM	AM sound (standard L)
M	mono sound
DS	dual sound
ST	stereo sound

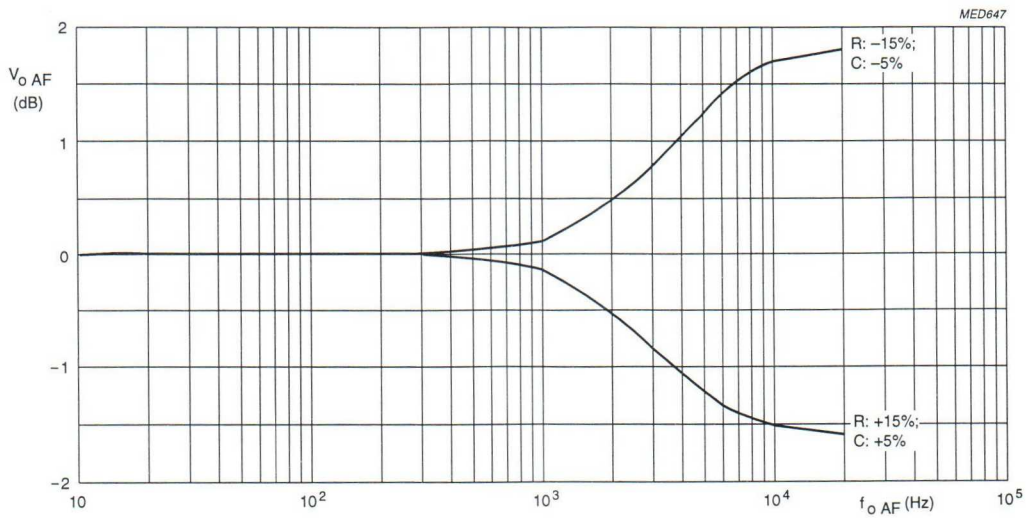


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%), $R_{internal}$ = 5 kΩ (±15%).

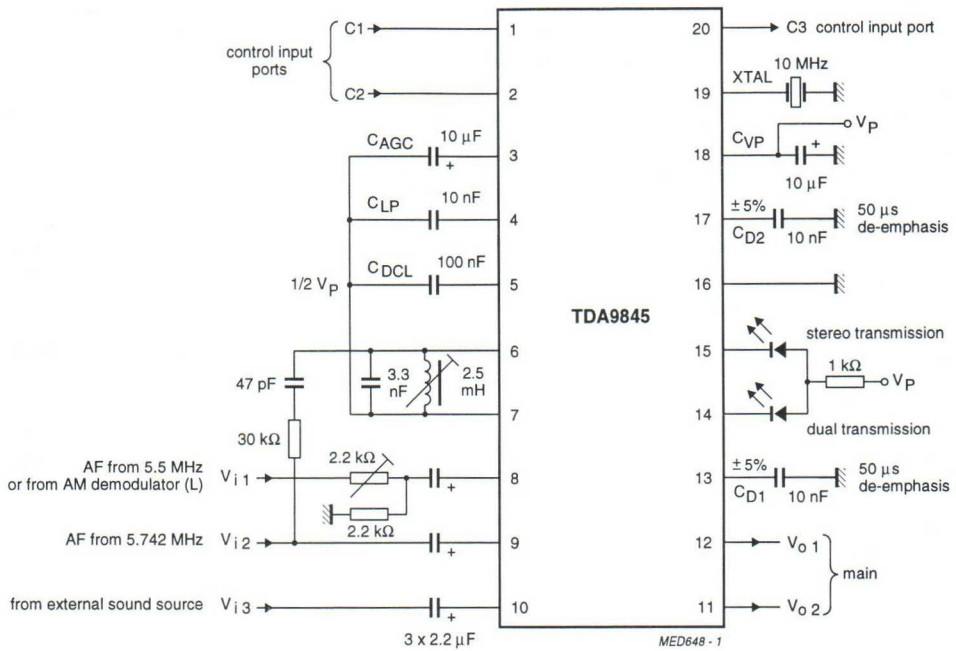


Fig.5 Test circuit of the stereo decoder TDA9845.

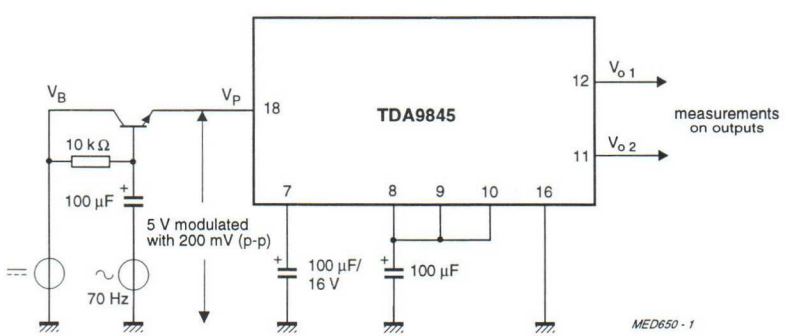


Fig.6 Test circuit for measurement of ripple rejection.

INTERNAL CIRCUITRY

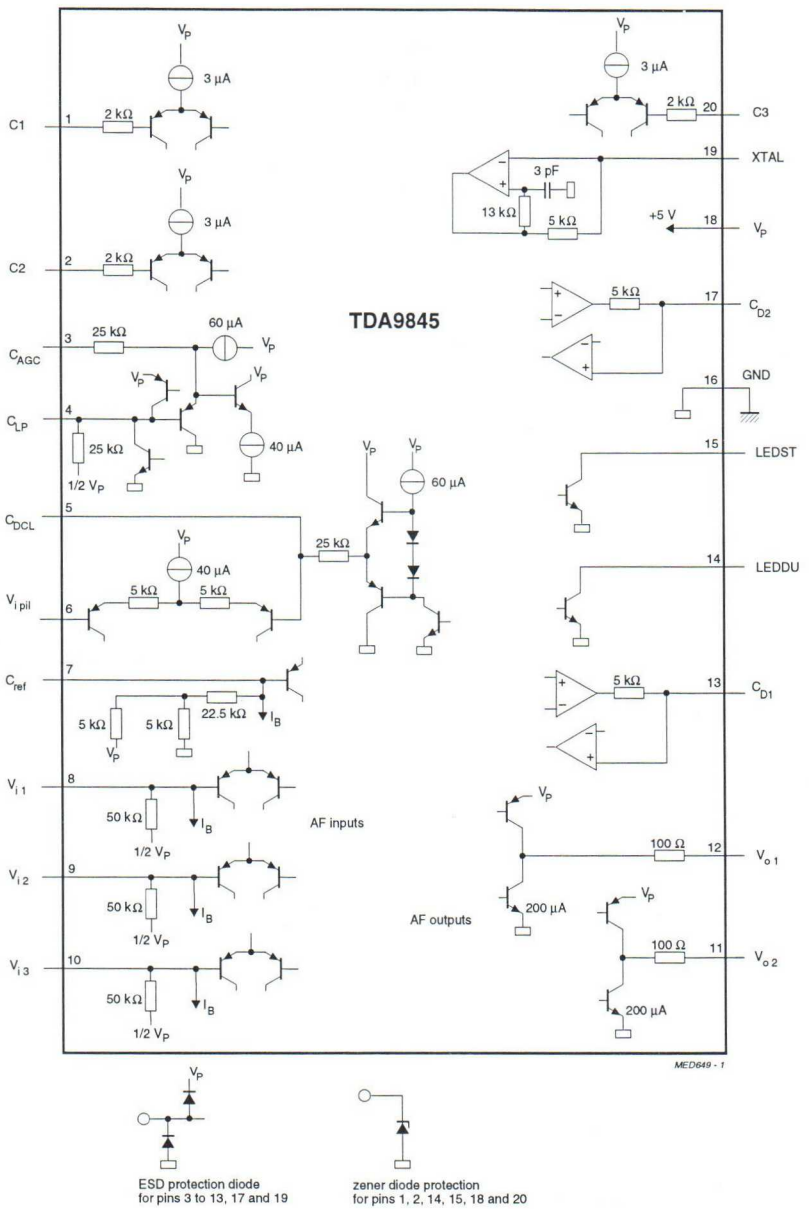


Fig.7 Internal circuitry.

TV and VTR stereo/dual sound processor with digital identification

TDA9847

FEATURES

- Supply voltage 5 to 8 V
- Source selector
- Stereo matrix
- AF inputs for external stereo AF signals (SCART or NICAM)
- AF outputs for Main and SCART
- Two LED output stages (for status display)
- High identification reliability.

GENERAL DESCRIPTION

The TDA9847 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.1 s; identification concerning the main functions).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 22)		4.5	5	8.8	V
I_P	supply current (pin 22)	without LED current	14	15	20	mA
V_i	nominal input signal (RMS value)	54% modulation;				
		B/G	–	250	–	mV
		L	–	500	–	mV
V_o	nominal output signal (RMS value)	54% modulation	–	500	–	mV
V_o	clipping level of the output signals (RMS value)	THD ≤ 1.5%; B/G or L				
		V_P = 5 V	1.4	1.60	–	V
		V_P = 8 V	2.4	2.65	–	V
I_{LED}	input current	LED ON	–	–	12	mA
$V_{i\ pil}$	input sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio		66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature		0	–	+70	°C
f_{ident}	identification window width		–	–	2.2	Hz
t_{ident}	total identification time ON		0.35	–	2.1	s
$V_{i\ tuner}$	identification sensitivity (pin 5)		–	28	–	dBμV
Δf_{pil}	pull-in range of pilot PLL	f_0 = 10.008 MHz	–300	–	+300	Hz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9847	24	DIL24SHR	plastic	SOT234AH
TDA9847T	24	SO24L	plastic	SOT137AH

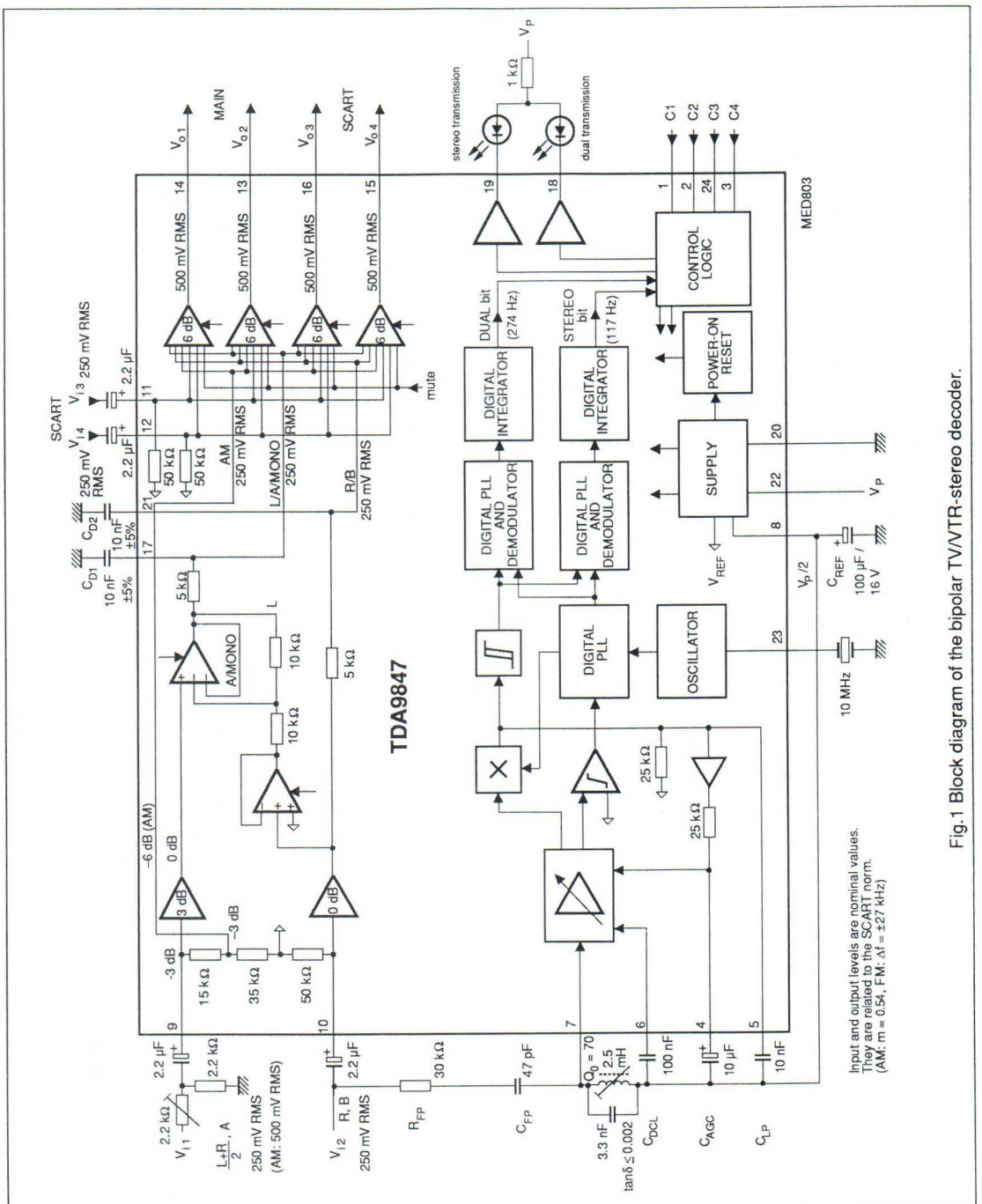


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

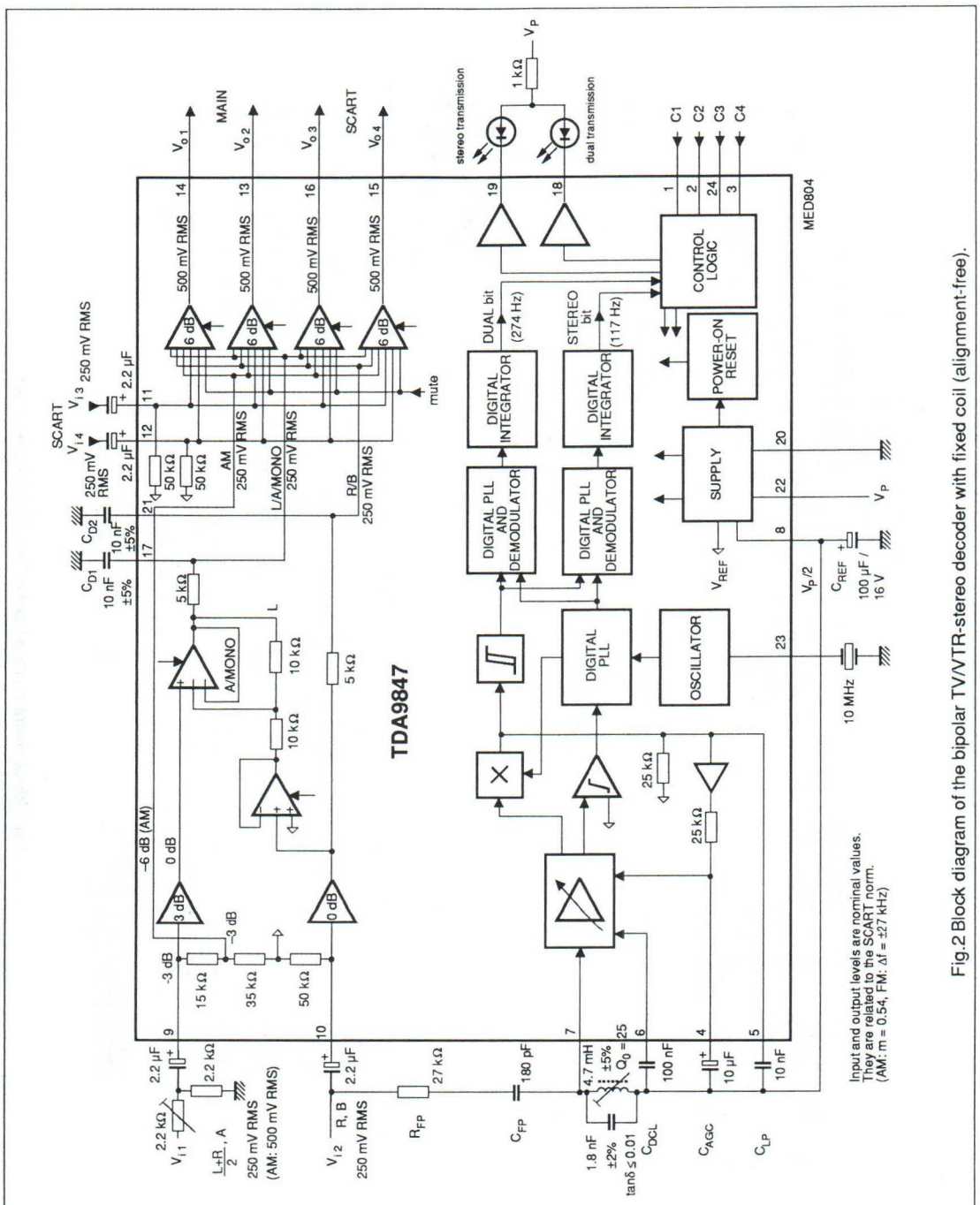


Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

PINNING

SYMBOL	PIN	DESCRIPTION
C1	1	control input Port C1
C2	2	control input Port C2
C4	3	control input Port C4
C_{AGC}	4	AGC capacitor of pilot frequency amplifier
C_{LP}	5	identification low-pass capacitor
C_{DCL}	6	DC loop capacitor
$V_{i\,pil}$	7	pilot frequency input
C_{REF}	8	$V_P/2$ capacitor
$V_{i\,1}$	9	AF input signal 1 (from first sound carrier or AM sound (standard L))
$V_{i\,2}$	10	AF input signal 2 (from second sound carrier)
$V_{i\,3}$	11	AF input signal 3 (SCART)
$V_{i\,4}$	12	AF input signal 4 (SCART)
$V_{o\,2}$	13	AF output signal 2 (Main)
$V_{o\,1}$	14	AF output signal 1 (Main)
$V_{o\,4}$	15	AF output signal 4 (SCART)
$V_{o\,3}$	16	AF output signal 3 (SCART)
C_{D1}	17	50 µs de-emphasis capacitor of AF Channel 1
LEDDU	18	LED (dual)
LEDST	19	LED (stereo)
GND	20	ground (0 V)
C_{D2}	21	50 µs de-emphasis capacitor of AF Channel 2
V_P	22	supply voltage (+5 to +8 V)
XTAL	23	10 MHz crystal
C3	24	control input Port C3

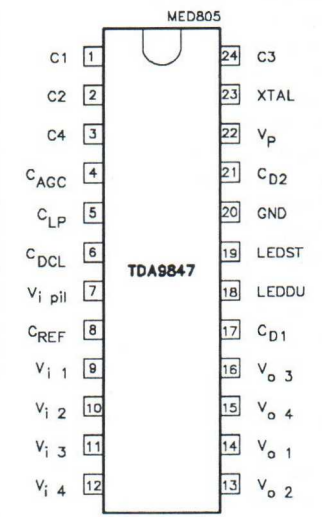


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9847 (block diagram, Fig.1) receives the signals from the FM-demodulators in a TV two sound carrier system.
The IC is intended for use in economic TV and VTR receivers. Therefore optimum relation between integration of functions and use of external components has been strived for. Additionally a new type of identification circuit has been developed.

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers. Dematrixing uses the technique of two amplifiers to switch and sum the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs ('forced mono').
De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.
A source selector, controlled via the control input ports, allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz) of 250 mV RMS (V_{i1}, V_{i2}) and for a nominal input signal (AM: m = 0.54) of 500 mV RMS (V_{i1}), respectively 250 mV RMS (V_{i3}, V_{i4}). A nominal gain of 6 dB for V_{i1} and V_{i2} signals (0 dB for V_{i1} signal (AM sound)) and 6 dB for V_{i3} and V_{i4} signals is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD ≤ 1.5%) is 1.60 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs V_{o1}, V_{o2}, V_{o3} and V_{o4}. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC-high-pass and single tuned LC-band-pass to the input of a gain controlled amplifier. The external LC-band-pass in combination with the external RC-high-pass should have a loaded Q-factor of approximately 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of approximately 12 is proposed. This may cause a loss in sensitivity of approximately 2 to 3 dB. A digital PLL circuit generates the synchronized pilot carrier. This carrier is used for the synchronous AM-demodulation to obtain the identification signal which is low-pass filtered. The identification signal output is also fed back via a low-pass (internal R, external C) to the control input of the AGC-amplifier.
A Schmitt-trigger circuit is performing pulse shaping of the identification signal, when the signal level is higher than the Schmitt-trigger threshold. For smaller signal levels there is no AC output signal. This is a measure against mis-identification caused by spurious signal components.
The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be indicated via LEDs. A 10 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_P-variations from the transmitter can be tracked in the event of missing synchronization with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (±1 Hz) to reduce mis-identification.
Fig.2 shows an example of the alignment-free f_P band-pass. To achieve the required Q_L of around 12 the Q_o at f_P of the coil was chosen to be around 25 (effective Q_o including PCB influence). Using coils with other Q_o the RC-network (R_{FP}, C_{FP}) has to be adapted accordingly. It is assumed that the loss factor $\tan\delta$ of the resonance capacitor is ≤ 0.01 at f_P.

Control input ports

The complete IC is controlled by the four control input ports C1, C2, C3 and C4. Which AF output channel pair can be selected is determined by the control input port C4 (LOW: Main; HIGH: SCART; 3-STATE: preset position (see General information)). With the other control input ports C1, C2 and C3 the user can select between different AF sources in accordance with the transmitter status (see Tables 1 and 2). Finally, Schmitt-triggers are added in the input port interfaces to suppress spikes on the control lines C1, C2, C3 and C4.
After a power-on reset both registers are reset (mute mode for both AF channel pairs). After some time (≤ 1 ms), when the power-on reset is automatically deactivated, the switch positions of the Main channel (C4 = LOW) are changed in accordance with the other control input port levels. If C4 is HIGH after a power-on reset, the switch positions of the SCART channel cannot change. The reason is, that the Main register is reset (mute mode; see Table 1). Thus, at first the Main register byte has to be changed out of the mute function, e. g. sound mute.

After that, when C4 is HIGH (see Table 2), the switch positions of the SCART channel are changed in accordance with the other control line levels.
When the supply voltage of the TDA9847 is not connected (stand-by function), the control lines remain undisturbed.
The logic level combination 1000 of the control input ports (C4, C3, C2 and C1) is forbidden for the user (see Table 2).

Operating mode selection

Tables 1 and 2 show the different operating modes of this stereo decoder.

Mute mode

This IC has two different mute modes: mute and sound mute.
In the mute mode, when all control input lines are set to LOW, all AF channels are muted ('fast mute'). Finally, the integrators are reset provided the user does not leave this mode (identification is disabled). When the user changes this mode, the identification circuit starts with the detection.
In the sound mute mode each AF channel can be separately muted (0100 = Main and 1100 = SCART). The identification circuit is activated and the LEDs are ON or OFF in accordance with the detection status of this circuit.

Mono mode

For the transmitter status mono the user must set the TDA9847 in the mono mode with X001 or X010 (see Tables 1 and 2). The level combination X011 is reserved for the AM sound (standard L), because in this mode the de-emphasis is deactivated and the gain of the AF signal from input to output is reduced from 6 dB to 0 dB. At the AF outputs the signal has the same level for standards with FM or AM modulated sound assuming the same modulation degree.

Stereo mode

In this mode the choice between stereo and mono ('forced mono') signals is common for both AF channel pairs. The mode for Main and SCART is achieved by control of the Main channel (see Tables 1 and 2).

Dual mode

In this mode there is no restriction to select AF inputs and outputs independently in both channels.

External mode

External sound sources, e. g. from SCART input, are fed to both AF channel pair outputs. When the user chooses the external mode of the Main channel (see Table 1), the identification circuit is still running, but the LEDs are switched OFF.

Programming of the Main and SCART register

General information

The switch positions of both AF channels are directly controlled by the data byte of the Main and SCART register. These registers are programmable by a microcontroller. In the 3-STATE mode the logic content of the C1, C2 and C3 control lines remains stored in the registers for Main and SCART, so the switch positions in the source selector do not change. The logic content of these control lines can be changed without changing the switch positions of the source selector (preset position) to prepare the new operating mode selection for the Main or SCART channel. The execution of this new mode is achieved by leaving the preset position (3-STATE): When the C4 level goes LOW, the logic content of the control lines C1, C2 and C3 are valid for the Main channel (see Table 1) and in the event of HIGH the C1, C2 and C3 are valid for the SCART channel (see Table 2).
The identification bits and the control line levels influence the operating mode selection for the AF switches in the source selector and dematrix, e. g. both AF channels are programmed in the mono mode (X001, see Tables 1 and 2). The LEDs are switched OFF. When the identification circuit detects the stereo identification frequency (f_S = 117 Hz) the dematrix is immediately switched in the stereo mode without changing the control line levels. The stereo signals are routed to all AF outputs. In the event of dual frequency detection (f_D = 274 Hz) both dual sounds are fed to the AF output pairs.

Microcontroller with 3-STATE output ports

Fig.8 shows an example of an application circuit for TDA9847 (V_P = 4.5 V to 8.8 V) in conjunction with a microcontroller, which has a LOW/HIGH ohmic/HIGH output port to control the Main and SCART channel (C4 control line). For the C1, C2 and C3 line the microcontroller requires only LOW/HIGH output ports. Two resistors R_{C4A} and R_{C4B} are necessary for the C4 line to generate the 3-STATE voltage. The values and tolerances of these components are given in this figure. When the microcontroller has only open drain ports available for the C1, C2 and C3 control line, external pull-up resistors must be connected to these control lines.
Fig.9 shows an example of a timing diagram to program the Main and SCART register of the TDA9847 with a microcontroller via the control lines C1, C2, C3 and C4. Both registers are programmed with the

same control line levels: C1 = LOW, C2 = HIGH and C3 = LOW.
The dual identification frequency is detected and the dual LED is switched ON. The A-signal (dual mode) is fed to all AF outputs (see Tables 1 and 2). This is shown in the beginning of this timing diagram.
The second period of time shows the programming of the external mode (C3 goes to HIGH: CC-signal) for the Main channel. The switch positions are immediately changed to the external AF source, because the C4 level is LOW. The dual LED is switched OFF by the logic (see External mode).
The next periods of time show the way to change the switch positions for the SCART channel to route B-signals to the AF outputs (dual mode: BB). At first the control output port of the microcontroller for the C4 line goes into the HIGH ohmic state. The changing of the C1, C2 or C3 level has no influence on the register data. In the timing diagram the C1 level changes from LOW-to-HIGH and the C3 level goes from HIGH-to-LOW. In the next steps the C4 line goes from 3-STATE-to-HIGH, and the level of the other control lines are valid for the SCART channel, and the B-signals are fed (dual mode: BB) to the AF outputs of the Main channel.
After some time in this example the C1 and C2 levels change from HIGH-to-LOW and the C3 level goes from LOW-to-HIGH (sound mute). The SCART channel is immediately muted, because the level of the C4 line is HIGH.
The last period of time shows the programming of the dual mode (AA) for the Main channel. At first the control output port of the microcontroller for the C4 line goes into the HIGH ohmic state. The changing of the C1, C2 or C3 level has no influence on the register data. The switch positions of the SCART channel stay in the sound mute.
In the 3-STATE mode the C2 level changes from LOW-to-HIGH, and the C3 level goes from HIGH-to-LOW. When the C4 level is LOW, the level of the other control lines are valid for the Main channel. The A-signal (dual mode) is fed to the Main outputs.
The operation mode mute (see Table 1) can be achieved from any position of the C4 control line without going via 3-STATE.
Fig.10 shows the hold and set-up time of the C1, C2 and C3 control line in the 3-STATE mode, which are specified in the CHARACTERISTICS.

Microcontroller with LOW/HIGH output ports

Fig.11 shows an example of an application circuit for TDA9847 (V_P = 4.5 V to 8.8 V) in conjunction with a microcontroller, which has open drain output ports to control the Main and SCART channel. Four resistors and two output ports of the microcontroller are necessary to generate the 3-STATE voltage. The other control lines have a pull-up resistor (10 kΩ) in the event of open drain output stages. These resistors are not necessary for LOW/HIGH output ports of the microcontroller having internal pull-up or push-pull stages. The values and tolerances of these components are given in this figure. Table 3 shows the conversion logic truth table.
The programming of the different operation mode selections are explained in the previous chapter.

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $V_P/2$. For a fast setting to $V_P/2$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{REF} = 100 µF/16 V in conjunction with the high ohmic input of the $V_P/2$ pin (pin 8). No additional load for this pin is allowed.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117 Hz / 274 Hz DPLL, the 117 Hz / 274 Hz integrator and the logic will be reset. Both AF channels (Main and SCART) are muted (≤ 1 ms).

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal circuit diagram including ESD components (only details behind the pins) is shown in Fig.6.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 22)	−0.3	+10	V
V_i	input voltage at pins 1 to 3 and 24	−0.3	+9.0	V
V_i	input voltage at pins 4 to 17, 21 and 23	−0.3	V_P	V
V_i	input voltage at pins 18 and 19	−0.3	+10	V
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	−	±500	V

Note to the Limiting Values

1. Charge device model class A: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT234AH	70 K/W
	SOT137AH	90 K/W

CHARACTERISTICS

V_P = 5 V, T_{amb} = +25 °C, nominal input signal $V_{i\,1,2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz), nominal input signal $V_{i\,1}$ = 0.5 V RMS value (AM: m = 0.54), nominal input signal $V_{i\,3,4}$ = 0.25 V RMS value, nominal output signal $V_{o\,1,2,3,4}$ = 0.5 V RMS value, f_{AF} = 1 kHz, $V_{i\,pil}$ = 16 mV RMS value, f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with CCIR468-3, f_{OSC} = 10 MHz; currents into the IC positive; measured in test circuit Fig.5, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 22)		4.5	5	8.8	V
I_P	supply current (pin 22)	without LED current	14	15	20	mA
P_{tot}	total power dissipation		63	75	176	mW
V_n	DC voltage (pins 9 to 17 and 21)		$V_P/2 - 0.1$	$V_P/2$	$V_P/2 + 0.1$	V
V_{REF}	DC reference voltage (pin 8)		$V_P/2 - 0.1$	$V_P/2$	$V_P/2 + 0.1$	V
I_{leak}	DC leakage current (pin 8)		–	–	±1	µA
AF inputs ($V_{i\,1}$ (pin 9) and $V_{i\,2}$ (pin 10))						
V_i	nominal input signal (RMS value)	54% modulation				
		B/G	–	0.25	–	V
		L (only $V_{i\,1}$)	–	0.50	–	V
V_i	clipping level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V; B/G	0.625	0.70	–	V
		V_P = 8 V; B/G	1.050	1.15	–	V
		V_P = 5 V; L (only $V_{i\,1}$)	1.200	1.40	–	V
		V_P = 8 V; L (only $V_{i\,1}$)	2.100	2.35	–	V
G_v	AF signal gain	$G = V_o/V_i$; note 1				
		B/G	5	6	7	dB
		L (only $V_{i\,1}$)	−1	0	+1	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 17 and 21)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF inputs (SCART) (pins 11 and 12)						
V_i	nominal input signal (RMS value)	54% modulation	–	0.25	–	V
V_i	clipping level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	0.625	0.70	–	V
		V_P = 8 V	1.050	1.15	–	V
G_v	AF signal gain	$G = V_o/V_i$; note 1	5	6	7	dB
R_i	input resistance		40	50	60	kΩ
AF outputs (pins 13 to 16)						
V_o	nominal output signal (RMS value)	THD ≤ 0.3%; 54% modulation	–	0.5	–	V
V_o	clipping level (RMS value)	THD ≤ 1.5%; B/G or L				
		V_P = 5 V	1.4	1.60	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		250	350	450	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	frequency response (bandwidth)	f = 40 to 20000 Hz; note 2	–0.5	–	+0.5	dB
$B_{-3\,dB}$	frequency response at –3 dB	note 2	300	350	400	kHz
THD	total harmonic distortion	note 1	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	CCIR468-3 (quasi-peak)	66	75	–	dB
α_{cr}	crosstalk attenuation for	notes 1 and 3				
	dual	$\lvert Z_s \rvert \leq 1$ kΩ	70	75	–	dB
	stereo	$\lvert Z_s \rvert \leq 1$ kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_s \rvert \leq 1$ kΩ; note 1	76	80	–	dB
ΔV_{DC}	change of output DC level between any two modes of operation	after switching	–	–	±10	mV
RR	ripple rejection	f_r = 70 Hz; see Fig.7	50	65	–	dB
$I_{o\,DC}$	DC output current		–	–	±20	µA
10 MHz crystal oscillator (pin 23)						
f_o	series resonance frequency of crystal	$C_L = \infty$	9.995	10.008	10.021	MHz
$\Delta f/f_{o\,typ}$	spread of oscillator frequency		–2000	–	+2000	10^{-6}
R_s	crystal series resistance		–	60	–	Ω
$V_{i\,XTAL}$	input signal (peak-to-peak value)		500	550	600	mV
Pilot processing						
$V_{i\,pil}$	pilot input sensitivity on pin 7 (RMS value)	unmodulated	5	–	100	mV
$R_{i\,pil}$	pilot input resistance		500	1000	–	kΩ
$C_{i\,pil}$	pilot input capacitance		–	–	3	pF
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in range	f_o = 10.008 MHz; note 6	±300	–	±300	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response at –3 dB		450	600	750	Hz
R_5	low-pass output resistance		18.75	25	31.25	kΩ
V_5	identification threshold (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	high sensitivity	40	–	50	
	with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
Identification (internal functions)						
$V_{i\,tuner}$	identification sensitivity	note 4	–	28	–	dBµV
C/N	pilot carrier-to-noise ratio for start of identification	note 5	–	33	–	dB/Hz
H	hysteresis	note 4	–	–	2	dB
f_{det}	pull-in range of identification PLL	note 6	±0.69	–	±0.69	Hz
t_{det}	pull-in time of identification PLL		0	–	0.8	s
f_{ident}	identification window width	note 7	–	–	2.2	Hz
t_{integr}	integrator time constant		–	–	0.94	s
$t_{ident\,on}$	total identification time ON		0.35	–	2.1	s
$t_{ident\,off}$	total identification time OFF		0.60	–	1.5	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LED (pins 18 and 19)						
V_{LOFF}	output voltage	LED OFF	–	–	8.8	V
V_{LON}	output voltage	LED ON	–	–	0.7	V
I_{LOFF}	input current	LED OFF	–	–	1	μA
I_{LON}	input current	LED ON	–	–	12	mA
Control input ports C_1, C_2 and C_3 (pins 1, 2 and 24)						
V_{CL}	LOW level input voltage		0	–	0.8	V
V_{CH}	HIGH level input voltage		2.0	5.0	8.8	V
I_{CL}	LOW level input current		–	–	−1	μA
I_{CH}	HIGH level input current		–	–	1	μA
Control input port C_4 (pin 3)						
V_{CL}	LOW level input voltage		0	–	0.8	V
V_{CT}	3-STATE level input voltage		1.5	1.8	2.1	V
V_{CH}	HIGH level input voltage		2.8	5.0	8.8	V
I_{CL}	LOW level input current		–	–	−1	μA
I_{CT}	3-STATE level input current		–	–	−1	μA
I_{CH}	HIGH level input current		–	–	1	μA
t_{HD-H}	HIGH level hold time	see Fig.10	5	–	–	μs
t_{HD-L}	LOW level hold time	see Fig.10	5	–	–	μs
t_{SU-DH}	HIGH level set-up time	see Fig.10	0.25	–	–	μs
t_{SU-DL}	LOW level set-up time	see Fig.10	0.25	–	–	μs

Notes to the characteristics

1. V_o = 0.5 V RMS value, f = 1 kHz.
2. Without de-emphasis capacitors with respect to nominal gain.
3. In dual mode: A (B)-signal into B (A) channel.
   In stereo mode: R-signal into left channel; L-signal = 0.
4. Tuner input signal, measured with PCALH reference front end (EMF/2, 75 Ω, 2T/20T/white bar, 100% video) and PC/SC_1 = 13 dB, PC/SC_2 = 20 dB. The pilot band-pass has to be aligned.
5. Bandwidth of the pilot BP-filter $B_{-3\ dB}$ = 1.2 kHz. $V_{i\,2}$ input driven with identification-modulated pilot carrier and white noise.
6. The pull-in range is symmetrical to rated frequency.
7. Identification window is defined as twice the pull-in range of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).

Table 1 Control input port matrix to select AF inputs and AF outputs (Main channel).

INPUT / OUTPUT	MODE	INPUT SIGNAL				OUTPUT SIGNAL				CONTROL INPUT PORT				LED	
		ST/DS/M		SCART		MAIN		SCART							
		V_{i1}	V_{i2}	V_{i3}	V_{i4}	V_{o1}	V_{o2}	V_{o3}	V_{o4}	C4	C3	C2	C1	DUAL	STEREO
PIN		9	10	11	12	14	13	16	15	3	24	2	1	18	19
Mute	–	–	–	–	–	no signal				0	0	0	0	off	off
Sound mute	–	–	–	–	–	no signal		*	*	0	1	0	0	on/off	on/off
Mono	M	M	–	–	–	M	M	*	*	0	0	0	1	off	off
		M	–	–	–	M	M	*	*	0	0	1	0	off	off
		AM	–	–	–	AM	AM	*	*	0	0	1	1	off	off
Stereo	ST	S	R	–	–	L	R	*	*	0	0	0	1	off	on
		S	R	–	–	S	S	*	*	0	0	1	0	off	on
		S	R	–	–	S	S	*	*	0	0	1	1	off	on
Dual sound	DS	A	B	–	–	A	B	*	*	0	0	0	1	on	off
		A	B	–	–	A	A	*	*	0	0	1	0	on	off
		A	B	–	–	B	B	*	*	0	0	1	1	on	off
External	–	–	–	C	D	C	D	*	*	0	1	0	1	off	off
		–	–	C	D	C	C	*	*	0	1	1	0	off	off
		–	–	C	D	D	D	*	*	0	1	1	1	off	off

Where:

* = content see Table 2

Mute mode: The content of the 117 Hz/274 Hz integrator will be reset. The LEDs are switched off.

Table 2 Control input port matrix to select AF inputs and AF outputs (SCART channel).

INPUT / OUTPUT PIN	MODE	INPUT SIGNAL ST/DS/M V_{i1} 9	V_{i2} 10	SCART V_{i3} 11	V_{i4} 12	OUTPUT SIGNAL MAIN V_{o1} 14	V_{o2} 13	SCART V_{o3} 16	V_{o4} 15	CONTROL INPUT PORT C4 3	C3 24	C2 2	C1 1
Sound mute	–	–	–	–	–	*	*	no signal		1	1	0	0
Mono	M	M	–	–	–	*	*	M	M	1	0	0	1
		M	–	–	–	*	*	M	M	1	0	1	0
		AM	–	–	–	*	*	AM	AM	1	0	1	1
Stereo	ST	S	R	–	–	*	*	L	R	depends on setting of Main			
		S	R	–	–	*	*	S	S				
		S	R	–	–	*	*	S	S				
Dual sound	DS	A	B	–	–	*	*	A	B	1	0	0	1
		A	B	–	–	*	*	A	A	1	0	1	0
		A	B	–	–	*	*	B	B	1	0	1	1
External	–	–	–	C	D	*	*	C	D	1	1	0	1
		–	–	C	D	*	*	C	C	1	1	1	0
		–	–	C	D	*	*	D	D	1	1	1	1

Where:

* = content see Table 1
R = right
L = left
S = (L + R)/2
A and B = dual sound A/B
C and D = external sound source (SCART)
AM = AM sound (standard L)
M = mono
DS = dual sound
ST = stereo

The combination 1000 of the control input ports is not allowed for the user.

Table 3 Conversion logic truth table for the C4 control line (see Fig.11).

MICROPROCESSOR OUTPUT CONTROL PORTS		TDA9847	
C41	C42	C4	C4-level
0	0	1	≥ 3.2 V
1	0	3-STATE	1.8 V ± 0.25 V
1	1	0	≤ 0.45 V
0	1	not allowed	undefined

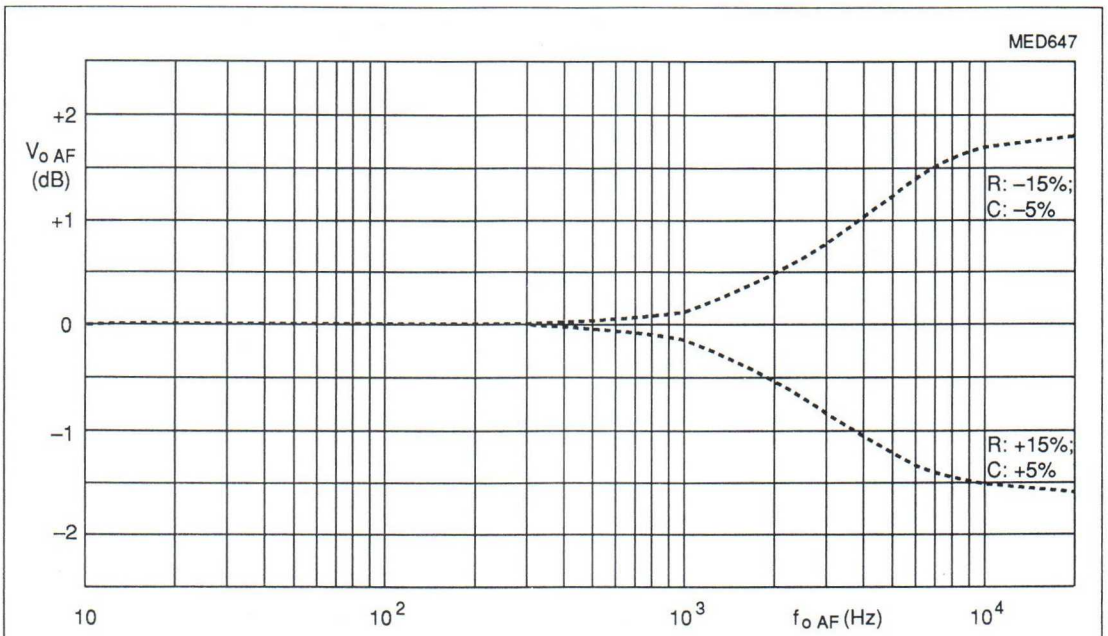


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%), $R_{internal}$ = 5 kΩ (±15%).

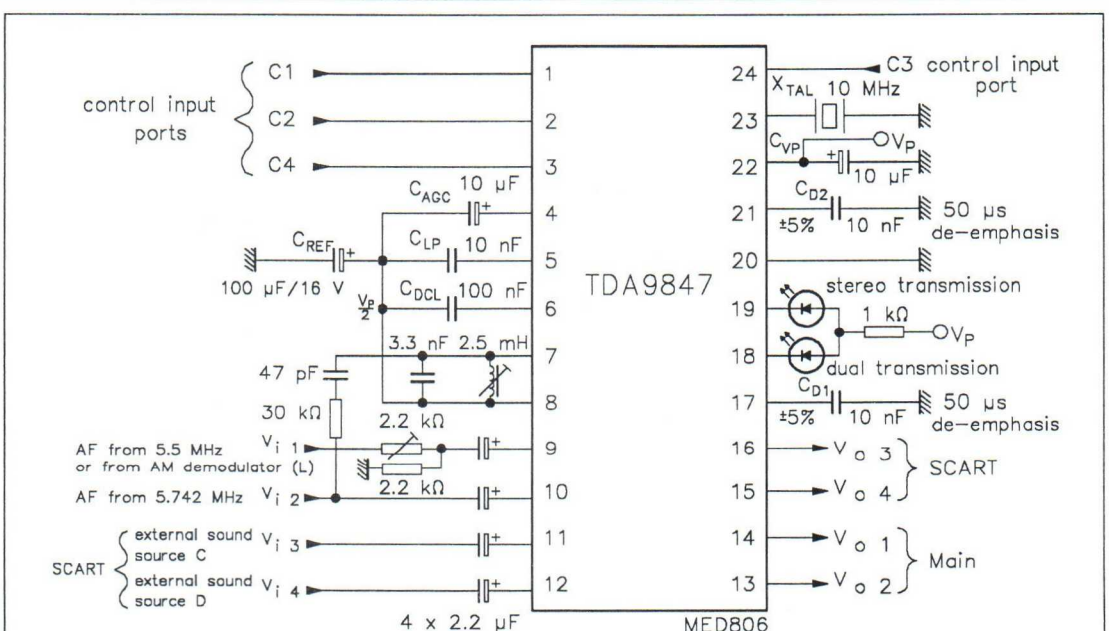


Fig.5 Test circuit of the stereo decoder TDA9847.

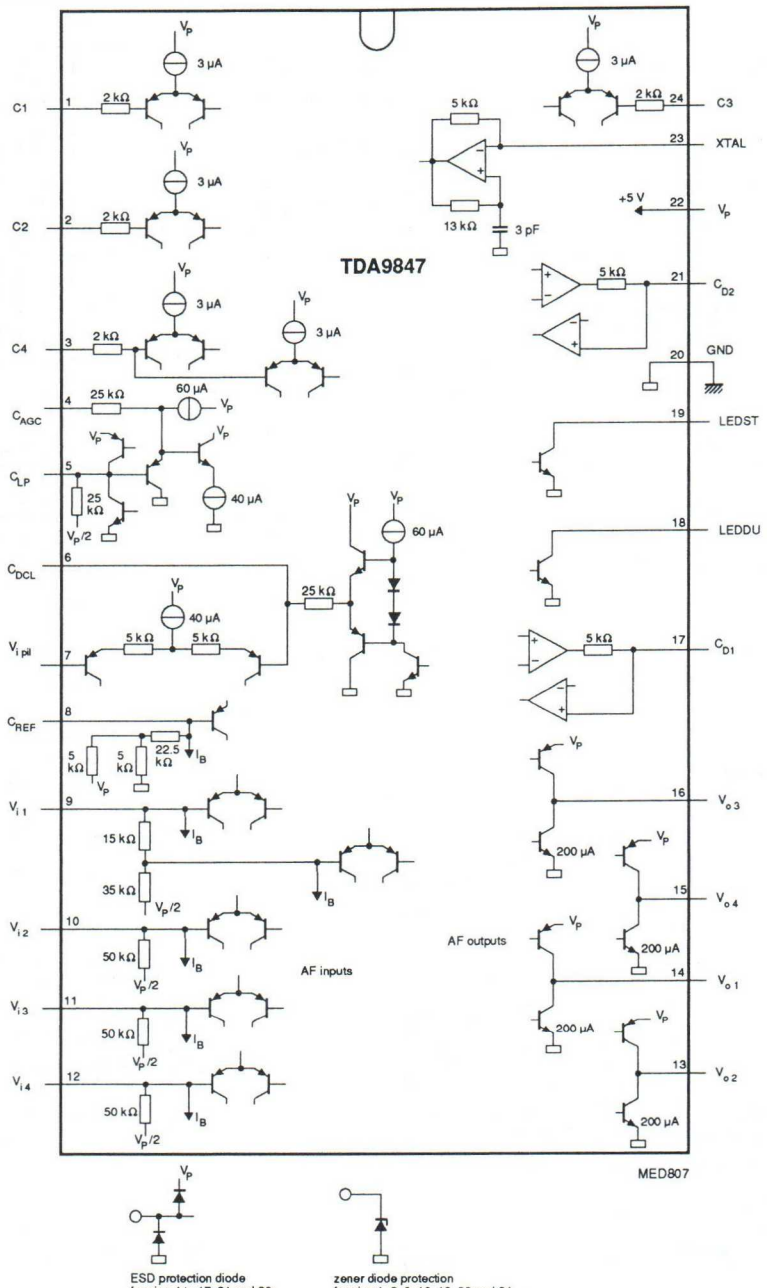


Fig.6 Internal circuits.

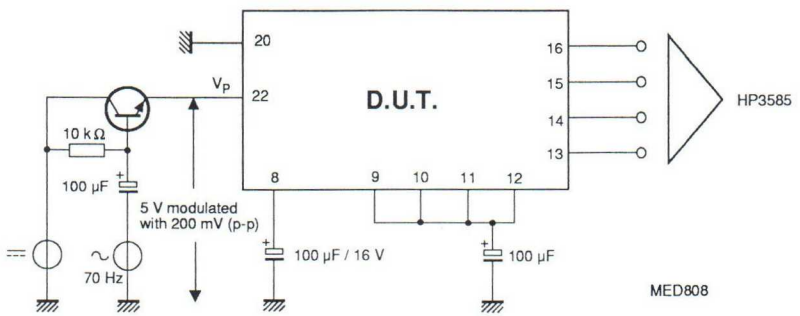


Fig.7 Test circuit for measurement of ripple rejection.

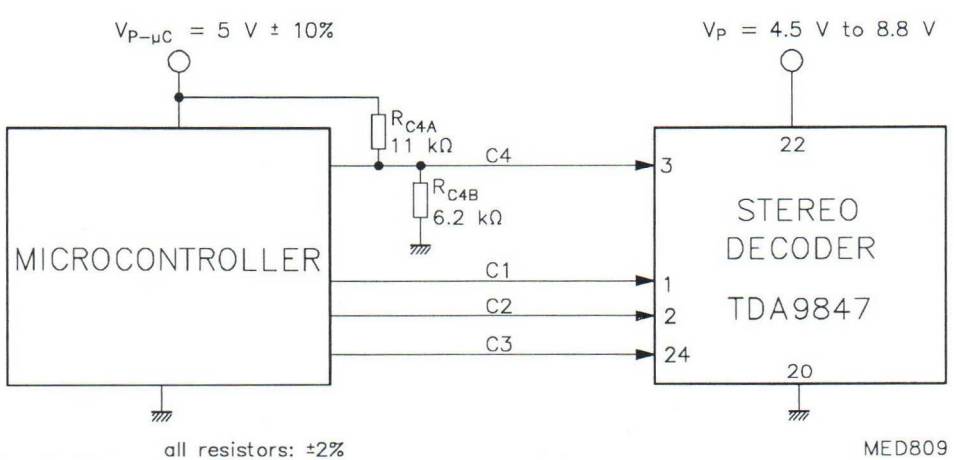


Fig.8 Application circuit for the stereo decoder TDA9847 in conjunction with a microcontroller (LOW/HIGH output ports with internal pull-ups or push-pull stages (C1, C2 and C3) and LOW/HIGH ohmic/HIGH output port (C4)).

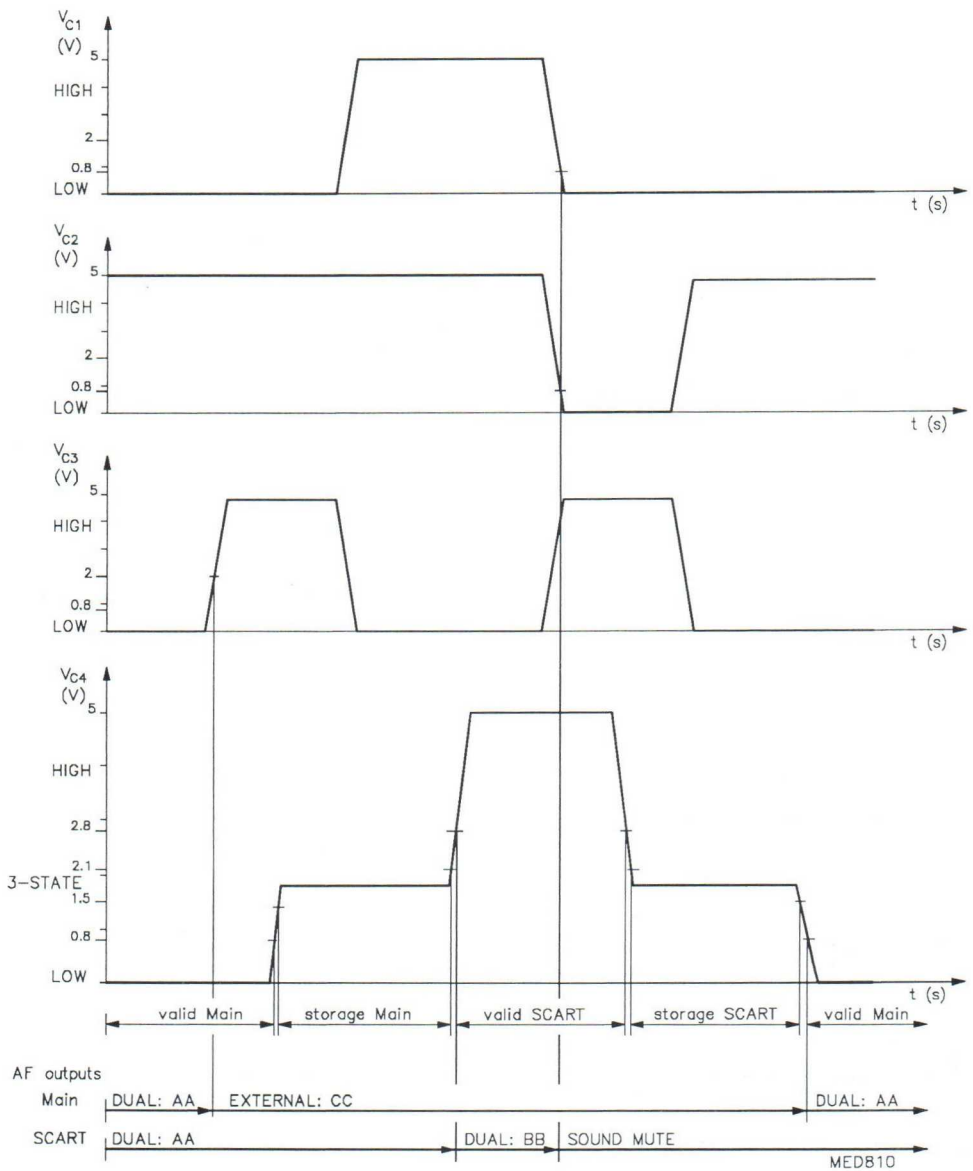


Fig.9 Programming the Main and SCART register of the TDA9847 with a microcontroller via the control lines C1, C2, C3 and C4. The dual identification frequency is detected.

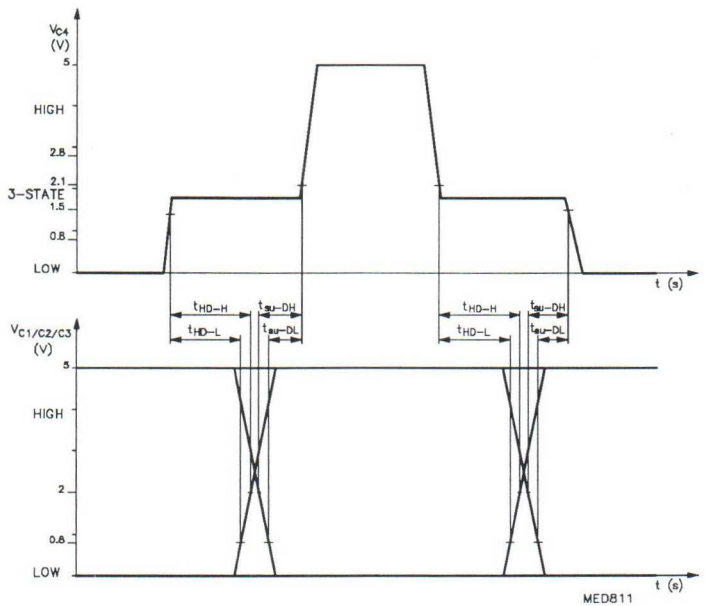


Fig.10 Waveforms showing the hold and set-up times of the C1, C2 and C3 control line in the 3-STATE mode.

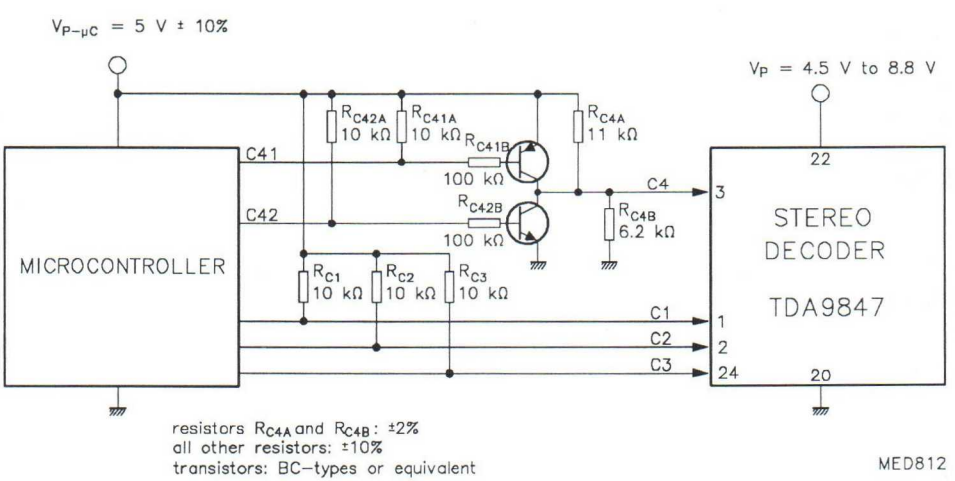


Fig.11 Application circuit for the stereo decoder TDA9847 in conjunction with a microcontroller (LOW/HIGH with open drain output ports).

I²C-bus controlled BTSC stereo / SAP decoder and audio processor

TDA9854

FEATURES

- Quasi alignment-free BTSC stereo decoder due to auto adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Audio processor
  - Selector for internal and external signals (line in)
  - Subwoofer or surround output with separate volume control
  - Volume control
  - Special loudness characteristic automatically controlled in combination with volume setting
  - Bass and treble control
  - Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9854 is a bipolar-integrated BTSC stereo / SAP decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9854	52	SHDIL	plastic	SOT247AH

A license is required for the use of this product. For further information, please contact

THAT Corporation
Licensing Operations
734 Forest St.
Marlborough, MA 01752
USA

Tel: (508) 229-2500
Fax: (508) 229-2590

THAT Corporation
Tokyo Office
405 Palm House, 1-20-2 Honmachi
Shibuya-ku, Tokyo 151
Japan

Tel: (03) 3378-0915
Fax: (03) 3374-5191

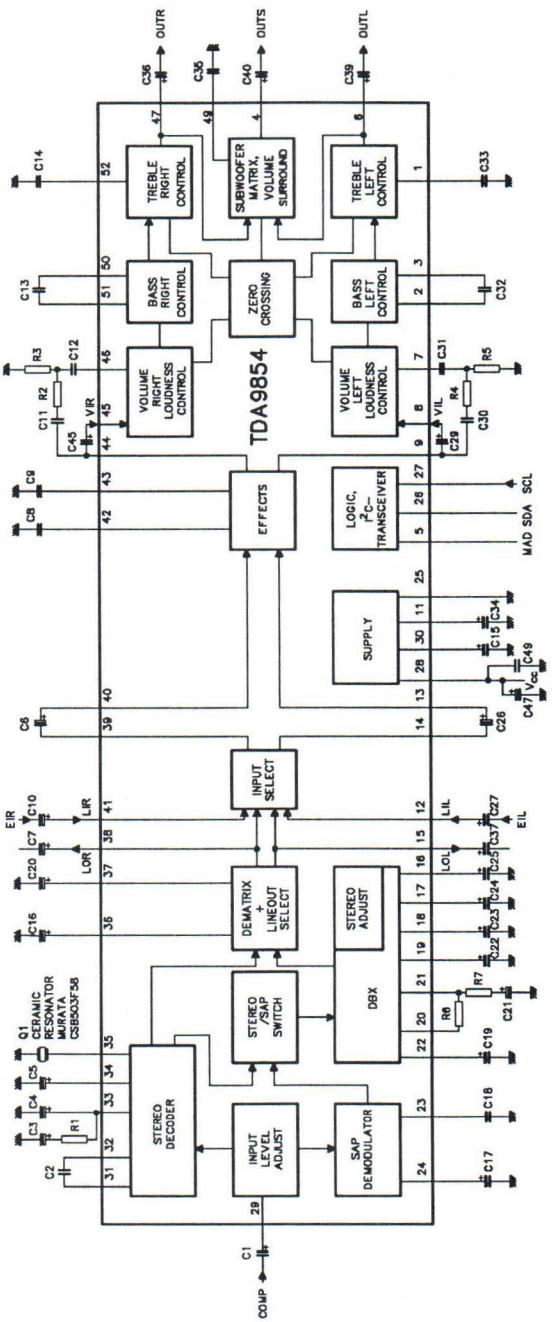


Fig.1 Block, application and test diagram.

COMPONENT LIST

elco ±20%; foil or ceramic ±10%; resistors ±5% unless otherwise specified.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	elco	63 V
C2	470 nF	foil	
C3	4.7 µF	elco	63 V
C4	220 nF	foil	
C5	10 µF	elco	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	elco	16 V
C7	4.7 µF	elco	16 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	elco	63 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C13	33 nF	foil	±5%
C14	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C15	100 µF	elco	16 V
C16	4.7 µF	elco	63 V
C17	4.7 µF	elco	63 V
C18	100 nF	foil	
C19	10 µF	elco	63 V
C20	4.7 µF	elco	63 V
C21	47 nF	foil	±5%
C22	1 µF	elco	63 V
C23	1 µF	elco	63 V
C24	10 µF	elco	63 V ±10%
C25	10 µF	elco	63 V ±10%
C26	2.2 µF	elco	16 V
C27	2.2 µF	elco	63 V
C29	2.2 µF	elco	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C31	150 nF	foil	±5%
C32	33 nF	foil	±5%
C33	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	elco	16 V
C35	150 nF	foil	±5%
C36	4.7 µF	elco	16 V
C37	4.7 µF	elco	16 V
C39	4.7 µF	elco	16 V
C40	4.7 µF	elco	16 V
C45	2.2 µF	elco	16 V
C47	220 µF	elco	25 V
C49	100 nF	foil or ceramic	SMD 1206

COMPONENT	VALUE	REMARK
R1	2.2 kΩ	
R2	20 kΩ	
R3	2.2 kΩ	
R4	20 kΩ	
R5	2.2 kΩ	
R6	8.2 kΩ	±2%
R7	160 Ω	±2%
Q1	503.5 kHz	MURATA CSB503F58

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{comp}	input signal (RMS value)	100% modulation L + R; f = 300 Hz	–	250	–	mV
V_{LOR}, V_{LOL}	output signal (RMS value)		–	500	–	mV
G_{LA}	input level adjustment control range		–3.5	–	+4.0	dB
α_{st}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion	f = 1 kHz	–	0.2	–	%
$V_{I,O}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
G_c	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f = 40 Hz	–	17	–	dB
G_b	bass control range	f = 40 Hz	–12	–	+16.5	dB
G_t	treble control range	f = 15 kHz	–12	–	+12	dB
G_v	subwoofer control range	f = 40 Hz	–14	–	+14	dB
S/N	signal-to-noise ratio	line out (mono); V_O = 0.5 V (RMS)				
	CCIR noise weighting filter (peak value)		–	60	–	dB
	DIN noise weighting filter (RMS value)		–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_O = 2 V (RMS); gain = 0 dB				
	CCIR noise weighting filter (peak value)		–	94	–	dB
	DIN noise weighting filter (RMS value)		–	107	–	dBA

PINNING

SYMBOL	PIN	DESCRIPTION
TL	1	treble control capacitor, left channel
B1L	2	bass control capacitor, left channel
B2L	3	bass control capacitor, left channel
OUTS	4	output subwoofer or output surround sound
MAD	5	programmable address bit (module address)
OUTL	6	output, left channel
LDL	7	input loudness, left channel
VIL	8	input volume control, left channel
EOL	9	output effects, left channel
i.c.	10	internal connected
V_{REF}	11	reference voltage $0.5V_{CC}$
LIL	12	line input, left channel
FIL	13	input effects, left channel
SOL	14	output selector, left channel
LOL	15	line output, left channel
TW	16	capacitor timing wideband for dbx
TS	17	capacitor timing spectral for dbx
CW	18	capacitor wideband for dbx
CS	19	capacitor spectral for dbx
VEO	20	variable emphasis out for dbx
VEI	21	variable emphasis in for dbx
CNR	22	capacitor noise reduction for dbx
CM	23	capacitor mute for SAP
CD	24	capacitor DC decoupling for SAP
GND	25	ground
SDA	26	serial data input/output
SCL	27	serial clock input
V_{CC}	28	supply voltage
COMP	29	input composite signal
VCAP	30	capacitor for electronic filtering of supply
CP1	31	capacitor for pilot detector
CP2	32	capacitor for pilot detector
CPH	33	capacitor for phase detector
CA	34	capacitor for filter adjust
CER	35	ceramic resonator
CMO	36	capacitor DC decoupling mono
CSS	37	capacitor DC decoupling stereo/SAP
LOR	38	line output, right channel
SOR	39	output selector, right channel
FIR	40	input effects, right channel
LIR	41	line input, right channel
PS2	42	capacitor 2 pseudo function
PS1	43	capacitor 1 pseudo function

SYMBOL	PIN	DESCRIPTION
EOR	44	output effects, right channel
VIR	45	input volume control, right channel
LDR	46	input loudness, right channel
OUTR	47	output, right channel
n.c.	48	not connected
SW	49	filter capacitor for subwoofer
B2R	50	bass control capacitor, right channel
B1R	51	bass control capacitor, right channel
TR	52	treble control capacitor

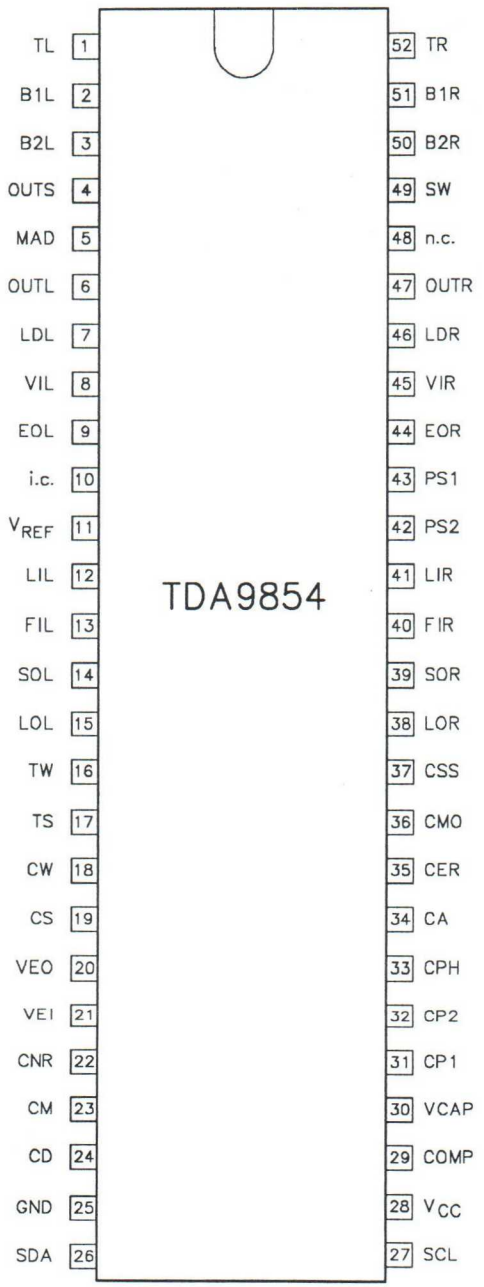


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Decoder

Input level adjustment

The composite input signal is fed to the input level adjustment stage. In order to compensate tolerances of the FM demodulator which supplied the composite input signal, the TDA9854 provides an input level adjustment stage. The control range is between –3.5 dB and +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 2 and 3 and the level adjust setting of Table 15 allows an optimal signal adjustment during the set alignment in the production line. This value has to be stored in a none volatile memory. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 µs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded subsignal L – R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation can be adjusted by an automatic procedure or manually. A detailed description of this alignment is provided in the ADJUSTMENT PROCEDURE. The stereo identification can be read by the I²C-bus (see Table 1). Two different pilot thresholds can be selected via I²C-bus (see Table 17).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in case of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 1).

Switch

The stereo/SAP switch feeds either the L – R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/line out select circuit. Table 14 shows the different switch modes provided at the output pins LOR and LOL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system according to the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

Selector

The selector allows selecting either the internal line out signals LOR or LOL (dematrix out) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Table 8). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS).The output of the selector is AC coupled to the effects circuit via pins SOR/SOL and FIR/FIL to avoid offset voltages.

Effects

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 12).

Volume/loudness

The volume control range is between +16 dB and –71 dB in steps of 1 dB and ends with a mute step (see Table 4). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of –12 dB. At –12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via the I²C-bus control (see Table 10). The left and right volume control stages include two independent zero crossing detectors. In the zero cross mode a change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting. The zero crossing mode is realized between adjoining steps and

between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case of need to mute only one channel, two steps are necessary. The first step is a transmission from any steps to –71 dB and the second is –71 dB step to mute. The step of –71 dB to mute has no zero crossing but it is not relevant. This procedure has to be provided by software.

Bass control

A single external 33 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass control range of +16.5 dB to –12 dB in steps of 1.5 dB at low frequencies (40 Hz). Internally the basic step width is 3 dB, with intermediate steps are obtained by a toggle function that provides additional an 1.5 dB boost or attenuation (see Table 5). Please note that both loudness and bass control together result in a maximum bass boost of 34.5 dB for low volume steps.

Treble control

The adjustable range of the treble control stage is between –12 dB and +12 dB in steps of 3 dB. The filter characteristic is determined by an external 5.6 nF capacitor for each channel. The logic circuitry is arranged in a way that the same data words (HEX 06 to 16) can be used for both tone controls if a bass control range from –12 dB to +12 dB and a treble control range from –12 dB to +12 dB with 3 dB steps are used (see Tables 5 and 6).

Subwoofer; surround sound control

The subwoofer or the surround mode can be activated with the control bit SUR (see Table 3). A low bit provides an output signal (L + R)/2 in subwoofer mode, a high bit selects surround mode and provides an output signal (L – R)/2. The signal is fed through a volume control stage with a range between +14 dB and –14 dB in 2 dB steps on top of the main channel control to the output pin OUTS. The last setting is the mute position (see Table 7). The capacitor C35 at pin SW provides a 230 Hz low-pass filter in subwoofer mode. In surround mode this capacitor should be disconnected. If balance is not in mid position the selected left and right output levels will be combined.

Mute

The mute function can be activated independently with the last step of volume or subwoofer/surround control at the left, right or center output. By setting the general mute bit GMU via the I²C-bus all audio part outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:
TZCM = 0:
forced mute with direct execution,
TZCM = 1:
execution in time with signal zero crossing.
In the zero cross mode a change of the GMU bit is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:
- a first transmission for mute execution
- a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)
- a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	9.5	V
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1			
V_n	voltage at all other pins to pin GND		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	43 K/W

Requirements for the composite input signal to ensure proper system performance.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R}$	composite input level for 100% modulation L + R (25 kHz deviation), RMS, f = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_O	output impedance	note 1	–	low-ohmic	5	kΩ
$f_{-2\ dB}$	roll-off frequencies (25 kHz deviation L + R)	low frequency (–2 dB)	–	–	5	Hz
		high frequency (–2 dB)	100	–	–	kHz
THD	total harmonic distortion L + R; f = 1 kHz	25 kHz deviation	–	–	0.5	%
		125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f = 1 kHz; 75 μs de-emphasis				
		critical picture modulation	44	–	–	dB
		with sync only	54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n x f_H; no de-emphasis; L + R: 25 kHz deviation, f = 1 kHz	40	–	–	dB

Notes to the requirements

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see input level adjustment control) must be taken into account.
2. In order to prevent clipping at overmodulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V, source resistance ≤ 600 Ω, output load R_L ≥ 10 kΩ, C_L ≤ 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; volume gain control G_c = 0 dB; bass linear; treble linear; loudness off; effects linear; composite input signal according to BTSC standard; see block diagram unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{DC}	DC voltage at signal handling pins		–	$V_{CC}/2$	–	V
DECODER SECTION						
Input level adjustment control						
G_{LA}	input level adjustment control	maximum gain	–	4.0	–	dB
		maximum attenuation	–	–3.5	–	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(RMS)}$	maximum input level		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input level for 100% modulation L + R (25 kHz deviation) (RMS value)	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input level for 100% modulation L – R (50 kHz deviation) (peak value)		–	707	–	mV
MPX_{max}	headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15% for 75 µs equivalent input modulation	9	–	–	dB
MPX_{pilot}	nominal stereo pilot level (RMS value)		–	50	–	mV
ST_{ON}	pilot threshold STEREO ON (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
ST_{OFF}	pilot threshold STEREO OFF (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hyst	hysteresis		–	2.5	–	dB
Out_{L+R}	output level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{ST}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation; alignment at f_L = 300 Hz; f_R = 3.1 kHz				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB
$L,R_{(f)}$	L, R frequency response	14% modulation; $f_{reference}$ = 300 Hz L or R				
		50 Hz to 11 kHz	–3	–	–	dB
		12 kHz	–	–3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f = 1 kHz	–	0.2	1.0	%
S/N	S/N CCIR 468-2 weighted; quasi peak; V_O = 500 mV (RMS)	LINE OUT in position MONO	50	60	–	dB
Stereo decoder, oscillator (VCXO)						
f_o	nominal VCXO frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free running frequency		500.0	–	507.0	kHz
Remark: The oscillator is designed to work together with MURATA resonator CSB503F58 for TDA9854. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58 for TDA9854.						
Δf_H	capture range (nominal pilot)		±190	±265	–	Hz
SAP demodulator						
Remark: The internal SAP carrier level is determined by the composite input level and the level adjust gain.						
SAP_{IN}	nominal SAP carrier input level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
SAP_{ON}	pilot threshold SAP ON (RMS value)		–	–	85	mV
SAP_{OFF}	pilot threshold SAP OFF (RMS value)		35	–	–	mV
SAP_{HYS}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output level at LINE OUT (RMS value)	LINE OUT (LOL, LOR) in position SAP / SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
F_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; $f_{reference}$ = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	1 kHz	–	0.5	2.0	%
LINE OUT (at pins LOL, LOR)						
V_o	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
Headr	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
Out_{DC}	DC output voltage		0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ST-SAP}	idle crosstalk L, R into SAP	100% modulation; f = 1 kHz; L or R; LINE OUT switched to SAP / SAP	50	–	–	dB
α_{SAP-ST}	idle crosstalk SAP into L, R	100% modulation; f = 1 kHz; SAP; LINE OUT switched to stereo	50	–	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dbx noise reduction circuit						
t_{adj}	stereo adjust time	see adjustment procedure	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin 17 via current meter connected to $V_{CC}/2 + 1$ V	–	24	–	µA
ΔI_s	spread of timing current		–	–	15	%
$I_{s\ range}$	timing current adjustment range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$I_s/3$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s
AUDIO PART Circuit section from pins LIL, LIR to pins OUTL, OUTR, OUTS Select in to input line control						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27}, C_{29} = 2.2 µF; $Z_i = Z_{i\ min}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1 V (RMS); G_c = 0 dB	–	0.02	0.5	%
		V_i = 2 V (RMS); G_c = 0 dB	–	0.02	0.5	%
RR	power supply ripple rejection	$V_{r(RMS)} < 200$ mV; f = 100 Hz	47	50	–	dB
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 1	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak	–	40	80	µV
		measured in dBA	–	8	–	µV
α_{cs}	channel separation	V_i = 1 V; f = 1 kHz	75	–	–	dB
		V_i = 1 V; f = 12.5 kHz	75	–	–	dB
Selector (from pins LOL, LOR, LIL, LIR to pins SOL, SOR)						
Z_i	input impedance		16	20	24	kΩ
α_s	input isolation of one selected source to the other input	f = 1 kHz; V_i = 1 V	86	96	–	dB
		f = 12.5 kHz; V_i = 1 V	80	96	–	dB
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector out by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
G_c	voltage gain, selector		–	0	–	dB
Effect controls						
Z_i	input impedance		8.8	11.0	13.2	kΩ
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.3	–	–	–	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume tone control part (input pins VIL, VIR to pins OUTX, to pin OUTS)						
Z_i	input impedance volume input		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_c = 16 dB	–	110	220	µV
		G_c = 0 dB	–	33	50	µV
		mute position	–	10	–	µV
G_c	total continuous control range					
	maximum boost		–	16	–	dB
	maximum attenuation		–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_c = +16 to –50 dB	–	–	2	dB
		G_c = –51 to –71 dB	–	–	3	dB
ΔG_t	gain tracking error	G_c = +16 to –50 dB	–	–	2	dB
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_c = +16 to 0 dB	–	0.2	10.0	mV
		G_c = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_c = +16 to +1 dB	–	2	15	mV
		G_c = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components; see Fig.4;				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control (see Fig.5)						
G_b	bass control maximum boost	f = 40 Hz	15.5	16.5	17.5	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
G_{step}	step resolution	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	15	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble control (see Fig.6)						
G_t	treble control maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution	f = 15 kHz	–	3	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	10	mV
Subwoofer or surround control						
G_s	subwoofer control	f = 40 Hz				
	maximum boost		12	14	16	dB
	maximum attenuation		12	14	16	dB
G_{step}	step resolution		–	2	–	dB
α_m	mute attenuation		60	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_s = 0 to +14 dB	–	–	10	mV
		G_s = 0 to –14 dB	–	–	5	mV
	DC step offset between any step to mute	G_s = +2 to +14 dB without input offset (pin SW connected to V_{REF})	–	–	15	mV
		G_s = +2 to +14 dB inclusive offset from OUTR, OUTL	–	–	50	mV
		G_s = 0 to –14 dB	–	–	10	mV
R_F	internal resistor for low-pass filter with external capacitor at pin SW		4	5	6	kΩ
L + R_{REJ}	common mode rejection in surround sound at pin OUTS	mono signal at VIL/VIR; f = 1 kHz; V_i = 1 V; balance = 0 dB	26	36	–	dB
Muting at power supply drop for OUTL, OUTR, OUTS						
$V_{CC-DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power on reset						
When reset is active the GMU-bit (general mute) and the LMU-bit (LINEOUT-mute) is set and the I²C-bus receiver is in reset position						
V_{CC}	start of reset	increasing supply voltage	–	–	2.5	V
	end of reset		5.2	6	6.8	V
	start of reset	decreasing supply voltage	4.2	5	5.8	V
Digital part (I²C-bus pins; note 2)						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The transmission contains:
   - total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   - clock frequency = 50 kHz
   - repetition burst rate = 400 Hz
   - maximum bus signal amplitude = 5 V_{p-p}.
2. The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request. The maximum clock frequency is 100 kHz.

ADJUSTMENT PROCEDURE

Composite input level adjustment. Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R, f = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ± 20 mV). Store the setting in a none volatile memory. Adjustment of spectral and wideband expander via stereo channel separation adjust.

Automatic adjustment procedure

- Capacitors of external inputs EIL, EIR must be grounded
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus. To avoid anoing sound level set GMU bit to '1' during adjustment procedure
- Effects, loudness off
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 8)
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 14)
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself
- After 1 s, stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see I²C-bus protocol) and store it in a none volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

Manual adjust

Manual adjust is necessary when no dual tone generator is available (e.g. for service).

- After POWER ON, spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz, 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz, 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimal adjust
- Store data in none volatile memory.

After every POWER ON, the alignment data and the input level adjustment data must be loaded from the none volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 18, as recommended by dbx.

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/W	A	DATA	MA	DATA	P

Where:

S	=	start condition, generated by the master
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	1 (read), generated by the master
A	=	acknowledge, generated by the slave
DATA	=	slave transmits an 8-bit data word
MA	=	acknowledge, generated by the master
P	=	stop condition, generated by the master

Table 1 Definition of the transmitted bytes after read condition.

FUNCTION	BYTE	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Function of the bits:

STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1x to A2x	stereo alignment read data
A1x	for wideband expander
A2x	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then the slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmitts condition P.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/W	A	SUBADDRESS	A	DATA	A	P

Where:

S	=	start condition
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	0 (write)
A	=	acknowledge, generated by the slave
SUBADDRESS (SAD)	=	see Table 2
DATA	=	see Table 3
P	=	stop condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress according to the order of Table 2 is performed.

Subaddress

Table 2 Second byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	HEX
volume right	VR	0	0	0	0	0	0	0	0	00
volume left	VL	0	0	0	0	0	0	0	1	01
bass	BA	0	0	0	0	0	0	1	0	02
treble	TR	0	0	0	0	0	0	1	1	03
subwoofer	SW	0	0	0	0	0	1	0	0	04
control 1	CON1	0	0	0	0	0	1	0	1	05
control 2	CON2	0	0	0	0	0	1	1	0	06
control 3	CON3	0	0	0	0	0	1	1	1	07
alignment 1	ALI1	0	0	0	0	1	0	0	0	08
alignment 2	ALI2	0	0	0	0	1	0	0	1	09
alignment 3	ALI3	0	0	0	0	1	0	1	0	0A

Definition of third byte

Table 3 Third byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
bass	BA	0	0	0	BA4	BA3	BA2	BA1	BA0
treble	TR	0	0	0	TR4	TR3	TR2	TR1	0
subwoofer	SW	0	0	SW5	SW4	SW3	SW2	0	0
control 1	CON1	GMU	0	LOFF	0	SUR	SC2	SC1	SC0
control 2	CON2	SAP	STEREO	TZCM	VZCM	LMU	EF2	EF1	EF0
control 3	CON3	0	0	0	0	L3	L2	L1	L0
alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
alignment 3	ALI3	ADJ	1	1	0	1	TC2	TC1	TC0

Function of the bits:

VR0 to VR6	volume control right
VL0 to VL6	volume control left
BA0 to BA4	bass control
TR1 to TR3	treble control
SW2 to SW5	subwoofer, surround control
GMU	mute control for all outputs (general mute)
LOFF	switch loudness on/off
SUR	surround/subwoofer SUR = 1 → (L – R)/2; SUR = 0 → (L + R)/2
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (treble and subwoofer/surround output stage)
VZCM	zero cross mode in volume operation
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjust
ADJ	stereo adjust on/off
A1X	stereo alignment data for wideband expander
A2X	stereo alignment data for spectral expander
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 4 Volume setting in register VR and VL.

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
16	1	1	1	1	1	1	1	7F
15	1	1	1	1	1	1	0	7E
14	1	1	1	1	1	0	1	7D
13	1	1	1	1	1	0	0	7C
12	1	1	1	1	0	1	1	7B
11	1	1	1	1	0	1	0	7A
10	1	1	1	1	0	0	1	79
9	1	1	1	1	0	0	0	78
8	1	1	1	0	1	1	1	77
7	1	1	1	0	1	1	0	76
6	1	1	1	0	1	0	1	75
5	1	1	1	0	1	0	0	74
4	1	1	1	0	0	1	1	73
3	1	1	1	0	0	1	0	72
2	1	1	1	0	0	0	1	71
1	1	1	1	0	0	0	0	70
0	1	1	0	1	1	1	1	6F
−1	1	1	0	1	1	1	0	6E
−2	1	1	0	1	1	0	1	6D
−3	1	1	0	1	1	0	0	6C
−4	1	1	0	1	0	1	1	6B
−5	1	1	0	1	0	1	0	6A
−6	1	1	0	1	0	0	1	69
−7	1	1	0	1	0	0	0	68
−8	1	1	0	0	1	1	1	67
−9	1	1	0	0	1	1	0	66
−10	1	1	0	0	1	0	1	65
−11	1	1	0	0	1	0	0	64
−12	1	1	0	0	0	1	1	63
−13	1	1	0	0	0	1	0	62
−14	1	1	0	0	0	0	1	61
−15	1	1	0	0	0	0	0	60
−16	1	0	1	1	1	1	1	5F
−17	1	0	1	1	1	1	0	5E
−18	1	0	1	1	1	0	1	5D
−19	1	0	1	1	1	0	0	5C
−20	1	0	1	1	0	1	1	5B
−21	1	0	1	1	0	1	0	5A
−22	1	0	1	1	0	0	1	59
−23	1	0	1	1	0	0	0	58
−24	1	0	1	0	1	1	1	57
−25	1	0	1	0	1	1	0	56
−26	1	0	1	0	1	0	1	55
−27	1	0	1	0	1	0	0	54
−28	1	0	1	0	0	1	1	53
−29	1	0	1	0	0	1	0	52
−30	1	0	1	0	0	0	1	51
−31	1	0	1	0	0	0	0	50
−32	1	0	0	1	1	1	1	4F
−33	1	0	0	1	1	1	0	4E

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
–34	1	0	0	1	1	0	1	4D
–35	1	0	0	1	1	0	0	4C
–36	1	0	0	1	0	1	1	4B
–37	1	0	0	1	0	1	0	4A
–38	1	0	0	1	0	0	1	49
–39	1	0	0	1	0	0	0	48
–40	1	0	0	0	1	1	1	47
–41	1	0	0	0	1	1	0	46
–42	1	0	0	0	1	0	1	45
–43	1	0	0	0	1	0	0	44
–44	1	0	0	0	0	1	1	43
–45	1	0	0	0	0	1	0	42
–46	1	0	0	0	0	0	1	41
–47	1	0	0	0	0	0	0	40
–48	0	1	1	1	1	1	1	3F
–49	0	1	1	1	1	1	0	3E
–50	0	1	1	1	1	0	1	3D
–51	0	1	1	1	1	0	0	3C
–52	0	1	1	1	0	1	1	3B
–53	0	1	1	1	0	1	0	3A
–54	0	1	1	1	0	0	1	39
–55	0	1	1	1	0	0	0	38
–56	0	1	1	0	1	1	1	37
–57	0	1	1	0	1	1	0	36
–58	0	1	1	0	1	0	1	35
–59	0	1	1	0	1	0	0	34
–60	0	1	1	0	0	1	1	33
–61	0	1	1	0	0	1	0	32
–62	0	1	1	0	0	0	1	31
–63	0	1	1	0	0	0	0	30
–64	0	1	0	1	1	1	1	2F
–65	0	1	0	1	1	1	0	2E
–66	0	1	0	1	1	0	1	2D
–67	0	1	0	1	1	0	0	2C
–68	0	1	0	1	0	1	1	2B
–69	0	1	0	1	0	1	0	2A
–70	0	1	0	1	0	0	1	29
–71	0	1	0	1	0	0	0	28
mute	0	1	0	0	1	1	1	27

Table 5 Bass setting in register BA.

G_b (dB)	DATA					HEX
	D4 BA4	D3 BA3	D2 BA2	D1 BA1	D0 BA0	
16.5	1	1	0	0	1	19
15	1	1	0	0	0	18
13.5	1	0	1	1	1	17
12	1	0	1	1	0	16
10.5	1	0	1	0	1	15
9	1	0	1	0	0	14
7.5	1	0	0	1	1	13
6	1	0	0	1	0	12
4.5	1	0	0	0	1	11
3	1	0	0	0	0	10
1.5	0	1	1	1	1	0F
0	0	1	1	1	0	0E
–1.5	0	1	1	0	1	0D
–3	0	1	1	0	0	0C
–4.5	0	1	0	1	1	0B
–6	0	1	0	1	0	0A
–7.5	0	1	0	0	1	09
–9	0	1	0	0	0	08
–10.5	0	0	1	1	1	07
–12	0	0	1	1	0	06

Table 6 Treble setting in register TR.

G_t (dB)	DATA				HEX
	D4 TR4	D3 TR3	D2 TR2	D1 TR1	
12	1	0	1	1	16
9	1	0	1	0	14
6	1	0	0	1	12
3	1	0	0	0	10
0	0	1	1	1	0E
–3	0	1	1	0	0C
–6	0	1	0	1	0A
–9	0	1	0	0	08
–12	0	0	1	1	06

Table 7 Subwoofer/surround setting in register SW.

G_s (dB)	DATA D5 SW5	D4 SW4	D3 SW3	D2 SW2	HEX
14	1	1	1	1	3C
12	1	1	1	0	38
10	1	1	0	1	34
8	1	1	0	0	30
6	1	0	1	1	2C
4	1	0	1	0	28
2	1	0	0	1	24
0	1	0	0	0	20
–2	0	1	1	1	1C
–4	0	1	1	0	18
–6	0	1	0	1	14
–8	0	1	0	0	10
–10	0	0	1	1	0C
–12	0	0	1	0	08
–14	0	0	0	1	04
mute	0	0	0	0	00

Table 8 Selector setting in register CON1.

FUNCTION: input connected to output	SOR, SOL	DATA D2 SC2	D1 SC1	D0 SC0
input	LOR, LOL	0	0	0
input	LOR, LOR	0	0	1
input	LOL, LOL	0	1	0
input	LOL, LOR	0	1	1
input	LIR, LIL	1	0	0
input	LIR, LIR	1	0	1
input	LIL, LIL	1	1	0
input	LIL, LIR	1	1	1

Table 9 SUR bit setting in register CON1.

FUNCTION	DATA D3
surround sound	1
subwoofer	0

Table 10 LOFF bit setting in register CON1.

CHARACTERISTIC	DATA D5
with loudness	0
linear	1

Table 11 Mute setting.

REGISTER CON1		REGISTER CON2	
FUNCTION	**DATA D7 GMU**	**FUNCTION**	**DATA D3 LMU**
forced mute at OUTR, OUTL, OUTS	1	forced mute at LOR, LOL	1
audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 12 Effects setting in register CON2.

FUNCTION	DATA D2 EF2	D1 EF1	D0 EF0
stereo linear on	0	0	0
pseudo on	0	0	1
spatial stereo, 30% anti-phase crosstalk	0	1	0
spatial stereo, 50% anti-phase crosstalk	0	1	1
forced mono	1	1	1

Table 13 Zero cross detection setting in register CON2.

FUNCTION	DATA D5 TZCM	FUNCTION	DATA D4 VZCM
direct mute control	0	direct volume control	0
mute control delayed until the next zero crossing	1	volume control delayed until the next zero crossing	1

Table 14 Switch setting at line out.

FUNCTION		DATA	DATA	
line out signals at		**transmission status**	**setting bits in register CON2**	
LOL	**LOR**	**internal switch readable bits in register ALR1, ALR2: D6 SAPP D5 STP**	**D7 SAP**	**D6 STEREO**
SAP	SAP	SAP received	1	1
mute	mute	no SAP received	1	1
left	right	stereo received	0	1
mono	mono	no stereo received	0	1
mono	SAP	SAP received	1	0
mono	mute	no SAP received	1	0
mono	mono		0	0

Table 15 Level adjust setting in register CON3.

G_I (dB)	DATA				HEX
	D3 L3	D2 L2	D1 L1	D0 L0	
+4	1	1	1	1	0F
+3.5	1	1	1	0	0E
+3	1	1	0	1	0D
+2.5	1	1	0	0	0C
+2	1	0	1	1	0B
+1.5	1	0	1	0	0A
+1	1	0	0	1	09
+0.5	1	0	0	0	08
0	0	1	1	1	07
–0.5	0	1	1	0	06
–1	0	1	0	1	05
–1.5	0	1	0	0	04
–2	0	0	1	1	03
–2.5	0	0	1	0	02
–3	0	0	0	1	01
–3.5	0	0	0	0	00

Table 16 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2.

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
nominal gain	1	0	0	0	0
	0	1	1	1	1
gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

Table 17 STS bit setting in register ALI2 (pilot threshold stereo on).

FUNCTION	DATA D7
STON ≤ 35 mV	1
STON ≤ 30 mV	0

Table 18 Timing current setting in register ALI3.

$I_{s\ range}$	DATA D2 TC2	DATA D1 TC1	DATA D0 TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
nominal	0	1	1
–10%	0	1	0
–20%	0	0	1
–30%	0	0	0

Table 19 ADJ bit setting in register ALI3.

FUNCTION	DATA D7
stereo decoder operation mode	0
auto adjustment of channel separation	1

CURVE	CAPACITANCE AT PIN 43 (nF)	CAPACITANCE AT PIN 42 (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

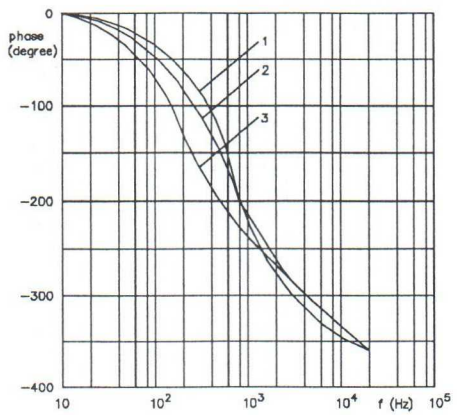


Fig.3 Pseudo (phase in degrees) as a function of frequency (left output).

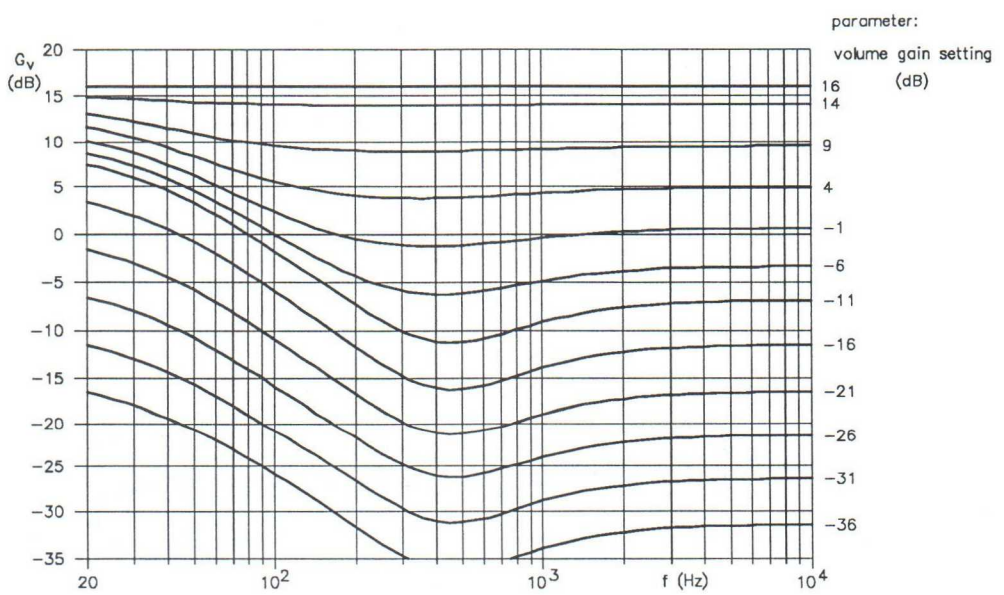


Fig.4 Volume control with loudness.

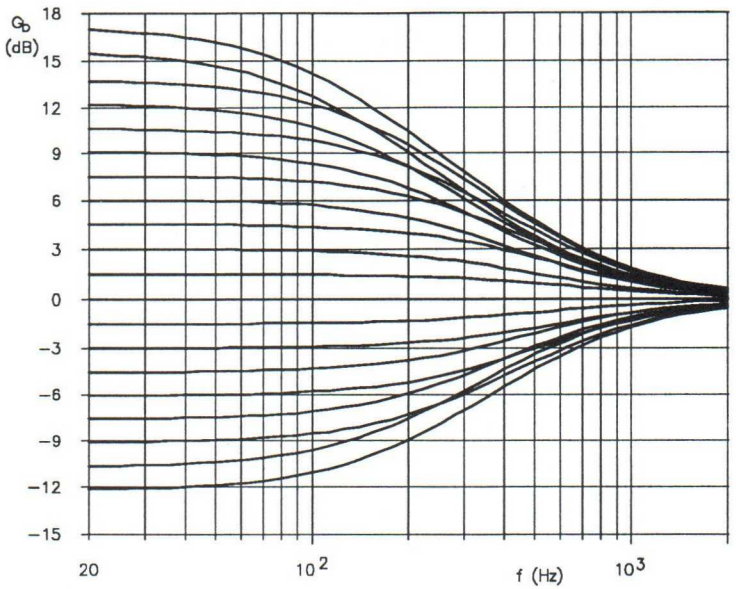


Fig.5 Bass control.

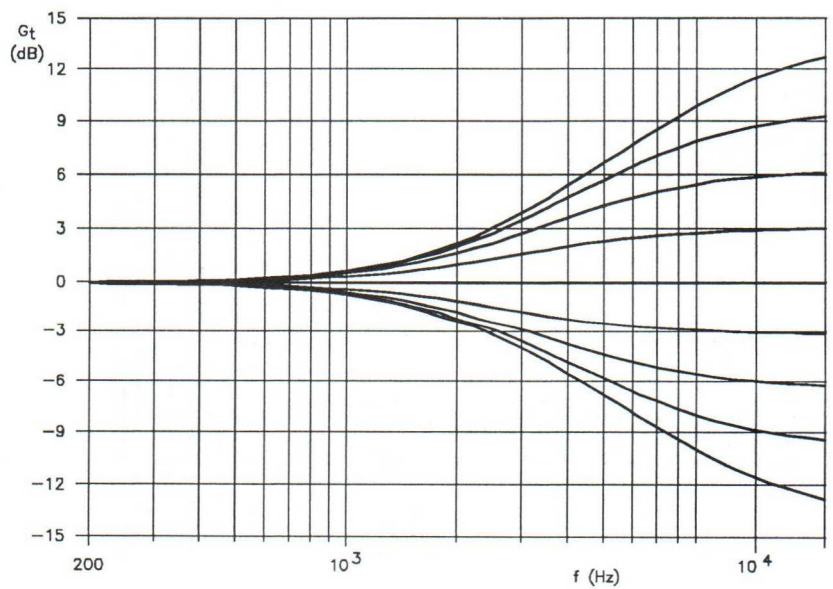


Fig.6 Treble control.

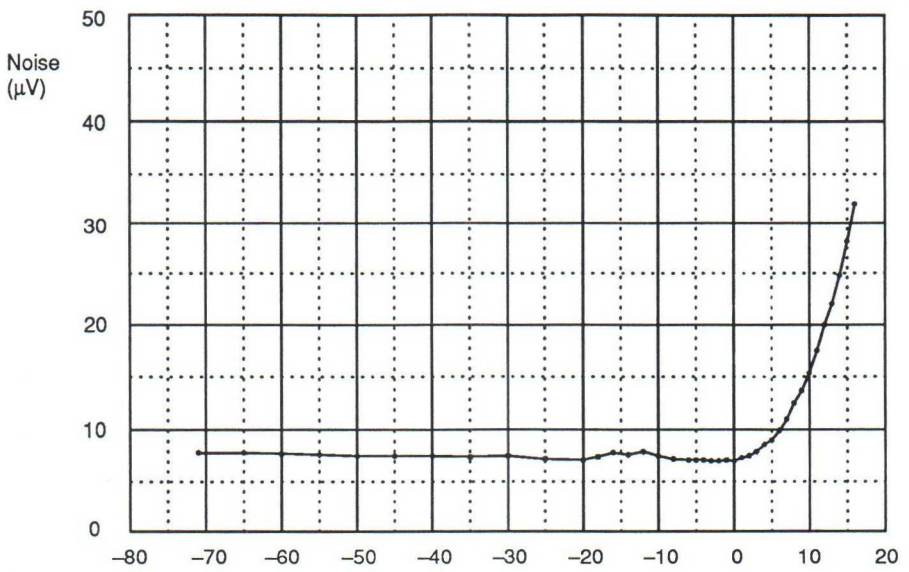


Fig.7 Noise as function of gain in dBA (RMS value).

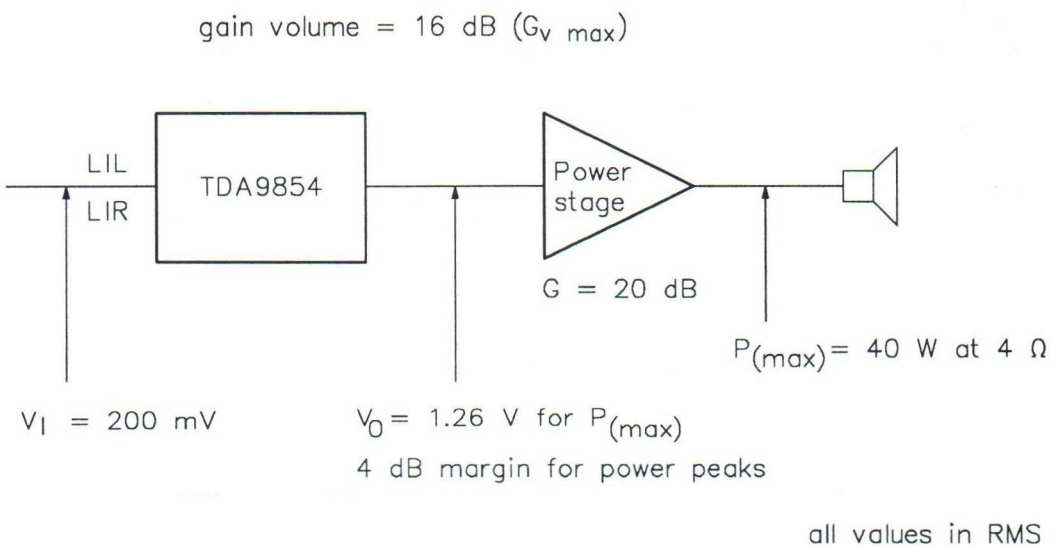


Fig.8 Level diagram.

APPLICATION HINTS

Selection of input signals by using the zero crossing mute mode

A selection between the internal signal path and the external input LIL/LIR produces a modulation click depending on the difference of the signal values at the time of switching. At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (TZCM = 1) and then the mute bit (GMU = 1) via the I²C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time before t_2, the microcontroller has to send the forced mute mode (TZCM = 0) and the return to the zero crossing mode (TZCM = 1) to be sure that mute is enabled.

The output signal remains muted until the next signal zero crossing of input B occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. The zero cross function is working at the lowest frequency of 40 Hz.

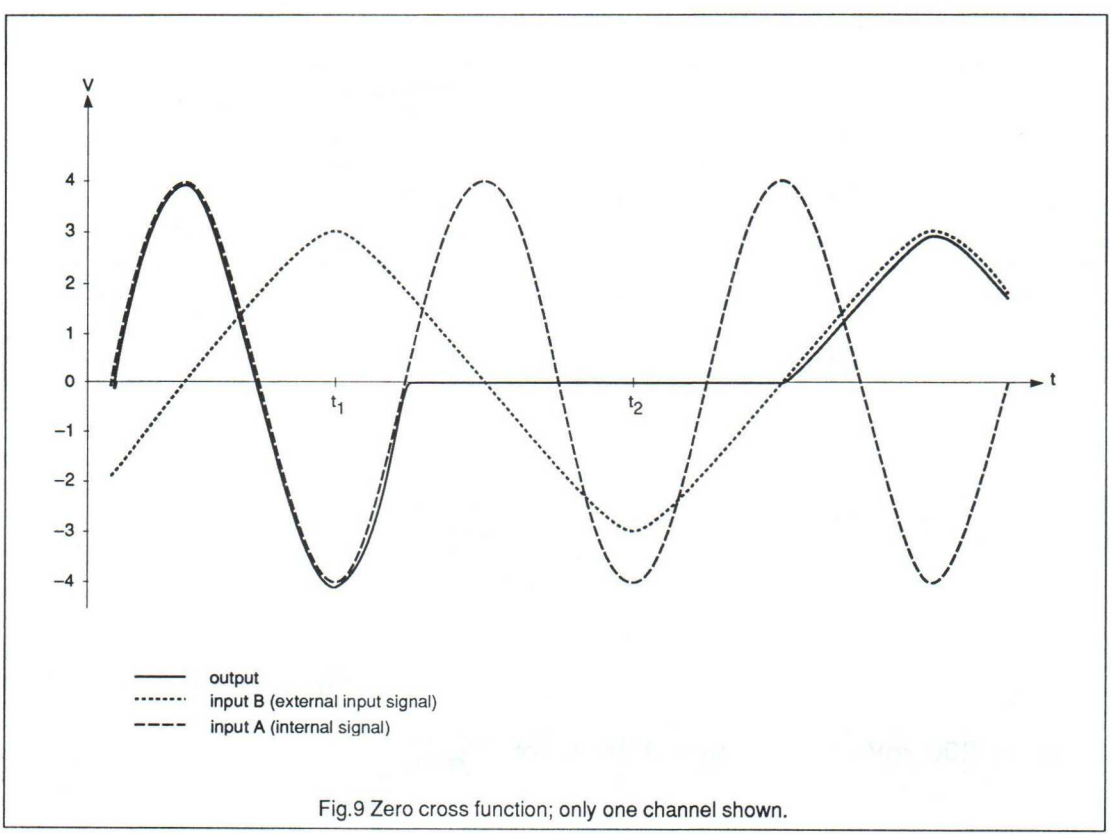


Fig.9 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.10 shows the basic loudness circuit with an external low-pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_1. Both result in a loudness control range of +16 dB to −12 dB. Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with G_v = −21 dB and R_1 = 33 kΩ results in R_3 = 3.2 kΩ.

For the low-pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz $G_v = G_{v\,reference}$ + 3 dB = −18 dB; f = 1 kHz and C_1 = 100 nF

If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

Fig.11 shows an example of the loudness circuit with bass and treble boost.

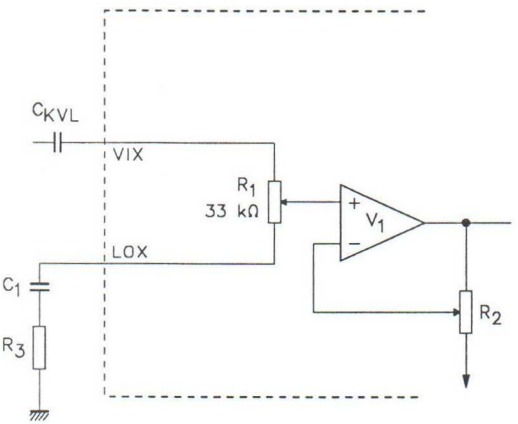


Fig.10 Basic loudness circuit.

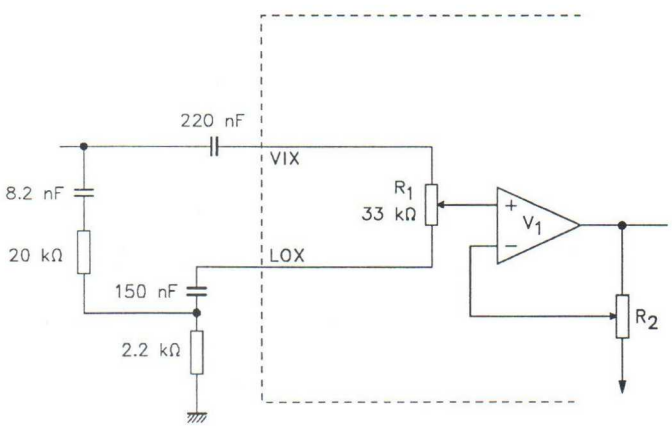


Fig.11 Loudness circuit with bass and treble boost.

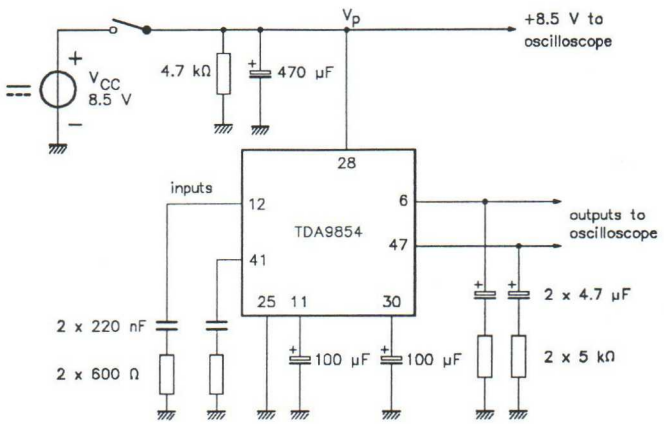


Fig.12 Turn-on/off power supply circuit diagram.

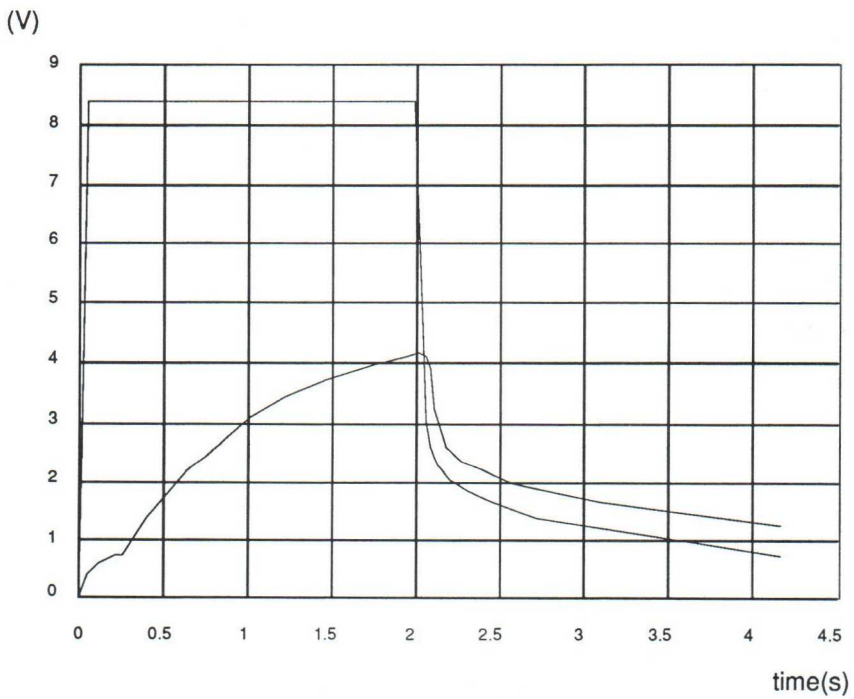
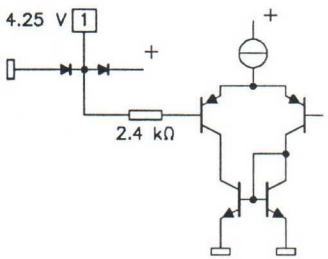
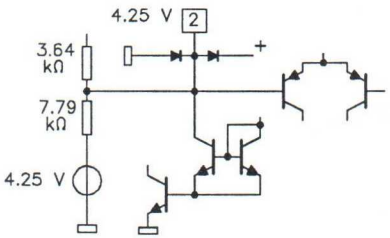


Fig.13 Turn-on/off behaviour.

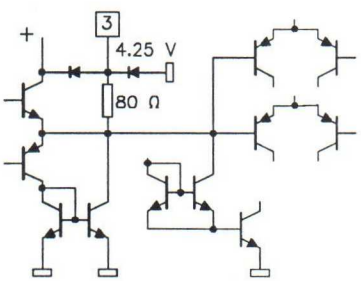
INTERNAL PIN CONFIGURATIONS



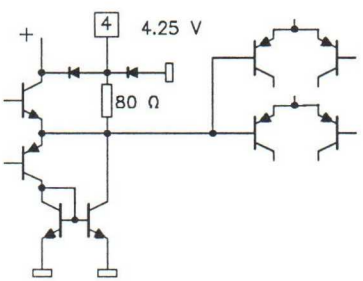
Pin 1: Treble control capacitor, left
Pin 52: Treble control capacitor, right



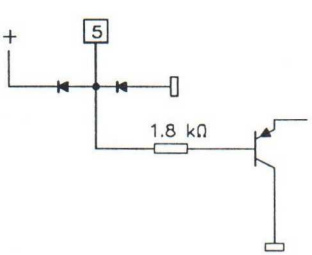
Pin 2: Bass control capacitor input, left
Pin 51: Bass control capacitor input, right



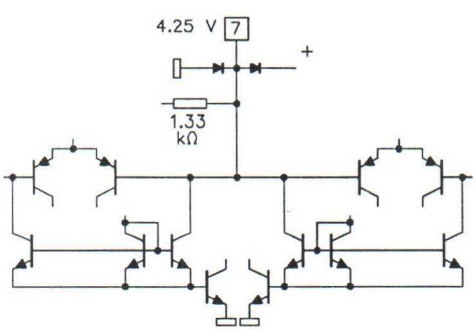
Pin 3: Bass control capacitor output, left
Pin 50: Bass control capacitor output, right



Pin 4: Output subwoofer
Pin 6: Output, left channel
Pin 14: Output selector, left channel
Pin 39: Output selector, right channel
Pin 47: Output, right channel

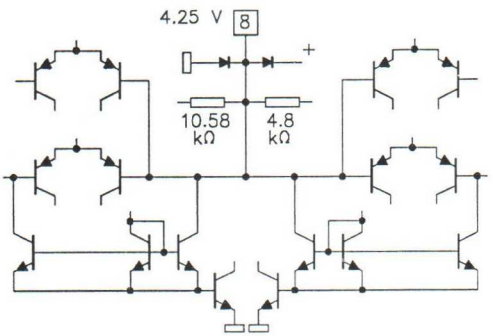


Pin 5: MAD (I²C–bus address switch)

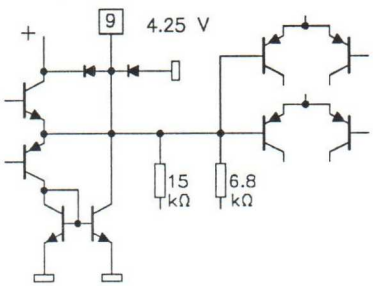


Pin 7: Input loudnes, left
Pin 46: Input loudness, right

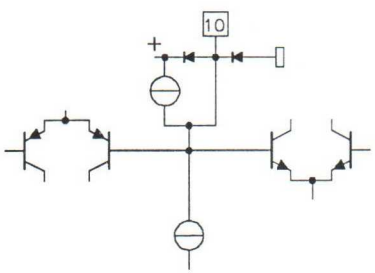
Fig.14 Internal circuits (continued in Fig.15).



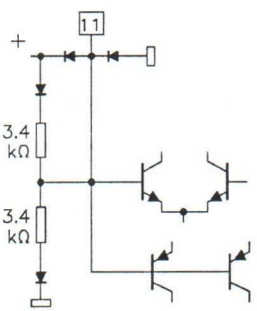
Pin 8: Input volume, left
Pin 45: Input volume, right



Pin 9: Output effects, left
Pin 44: Output effects, right

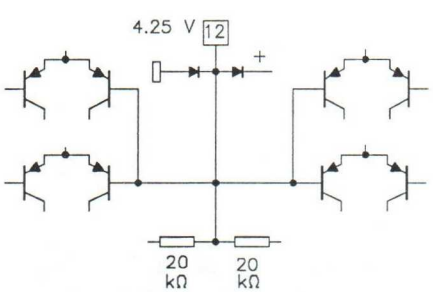


Pin 10: Internal connected

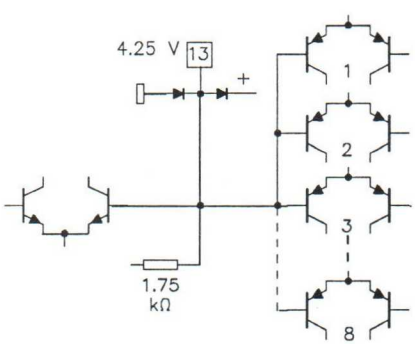


Pin 11: Reference voltage

$0.5 \times V_{CC}$

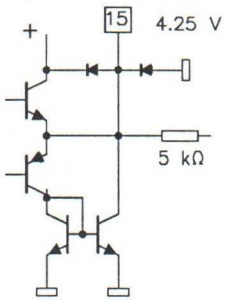


Pin 12: Line input, left
Pin 41: Line input, right

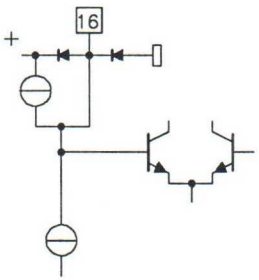


Pin 13: Input effects, left
Pin 40: Input effects, right

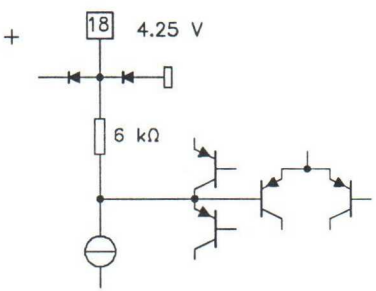
Fig.15 Internal circuits (continued from Fig.14).



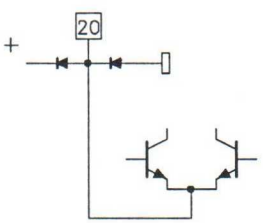
Pin 15: Line output, left
Pin 38: Line output, right



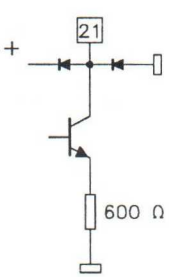
Pin 16: Timing capacitor wideband for DBX
Pin 17: Timing capacitor spectral for DBX



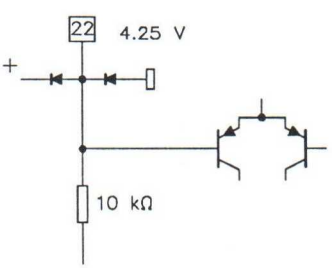
Pin 18: Capacitor wideband for DBX
Pin 19: Capacitor spectral for DBX



Pin 20: Variable emphasis out for DBX

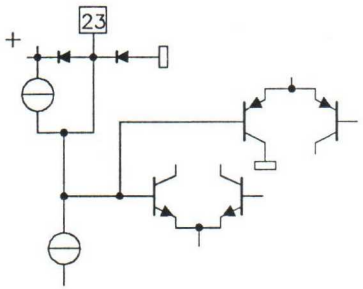


Pin 21: Variable emphasis in for DBX

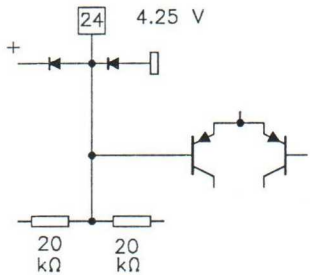


Pin 22: Capacitor noise reduction for DBX

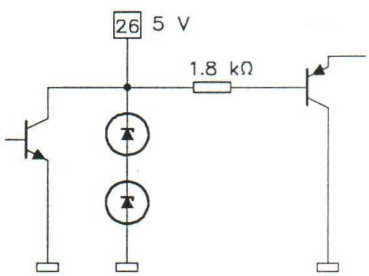
Fig.16 Internal circuits (continued from Fig.15).



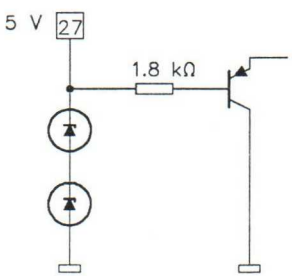
Pin 23: Capacitor mute for SAP



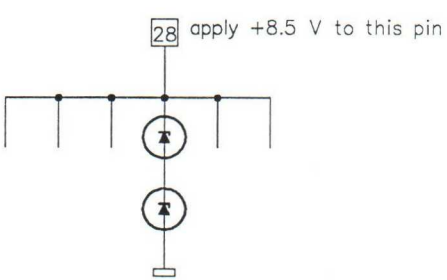
Pin 24: Capacitor DC decoupling for SAP



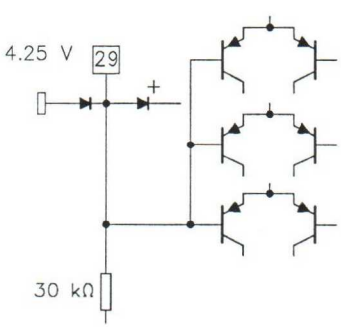
Pin 26: SDA (I²C–bus DATA input/output)



Pin 27: SCL (I²C–bus CLOCK)

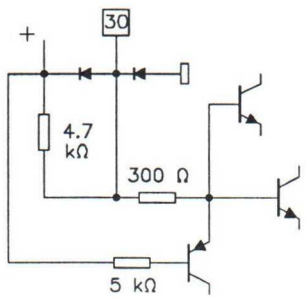


Pin 28: Supply voltage

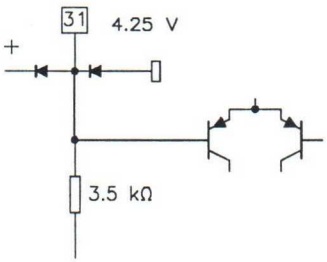


Pin 29: Input composite signal

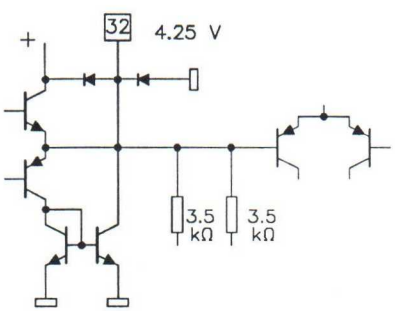
Fig.17 Internal circuits (continued from Fig.16).



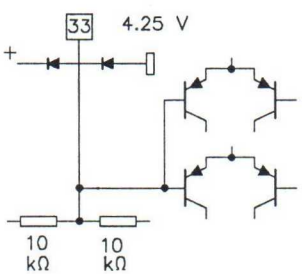
Pin 30: Smoothing capacitor for supply



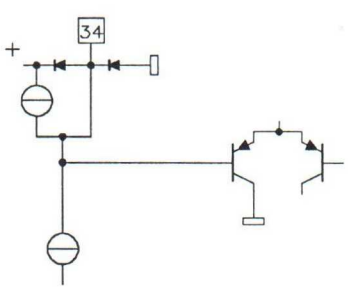
Pin 31: Capacitor for pilot detector



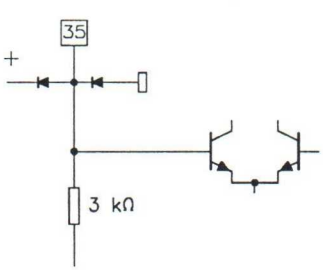
Pin 32: Capacitor for pilot detector



Pin 33: Capacitor for phase detector

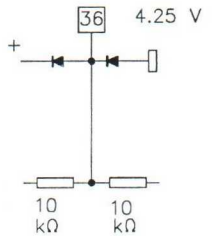


Pin 34: Capacitor for filter adjust

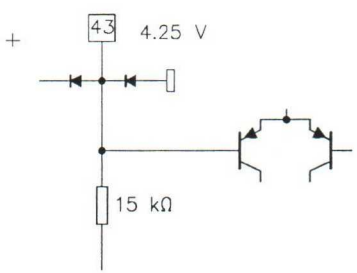


Pin 35: Ceramic resonator

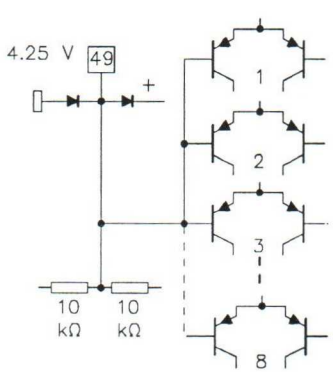
Fig.18 Internal circuits (continued from Fig.17).



Pin 36: Capacitor DC decoupling mono
Pin 37: Capacitor DC decoupling stereo/SAP



Pin 43: Capacitor 1 pseudo function
Pin 42: Capacitor 2 pseudo function



Pin 49: Capacitor subwoofer

Fig.19 Internal circuits (continued from Fig.18).

I²C-bus controlled BTSC stereo / SAP decoder and audio processor

TDA9855

FEATURES

- Quasi alignment-free BTSC stereo decoder due to auto adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Audio processor
  - Selector for internal and external signals (line in)
  - Automatic volume level control
  - Subwoofer or surround output with separate volume control
  - Volume control
  - Special loudness characteristic automatically controlled in combination with volume setting
  - Bass and treble control
  - Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9855 is a bipolar-integrated BTSC stereo / SAP decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9855	52	SHDIL	plastic	SOT247AH
TDA9855WP	68	PLCC	plastic	SOT188CG

A license is required for the use of this product. For further information, please contact

THAT Corporation
Licensing Operations
734 Forest St.
Marlborough, MA 01752
USA

Tel: (508) 229-2500
Fax: (508) 229-2590

THAT Corporation
Tokyo Office
405 Palm House, 1-20-2 Honmachi
Shibuya-ku, Tokyo 151
Japan

Tel: (03) 3378-0915
Fax: (03) 3374-5191

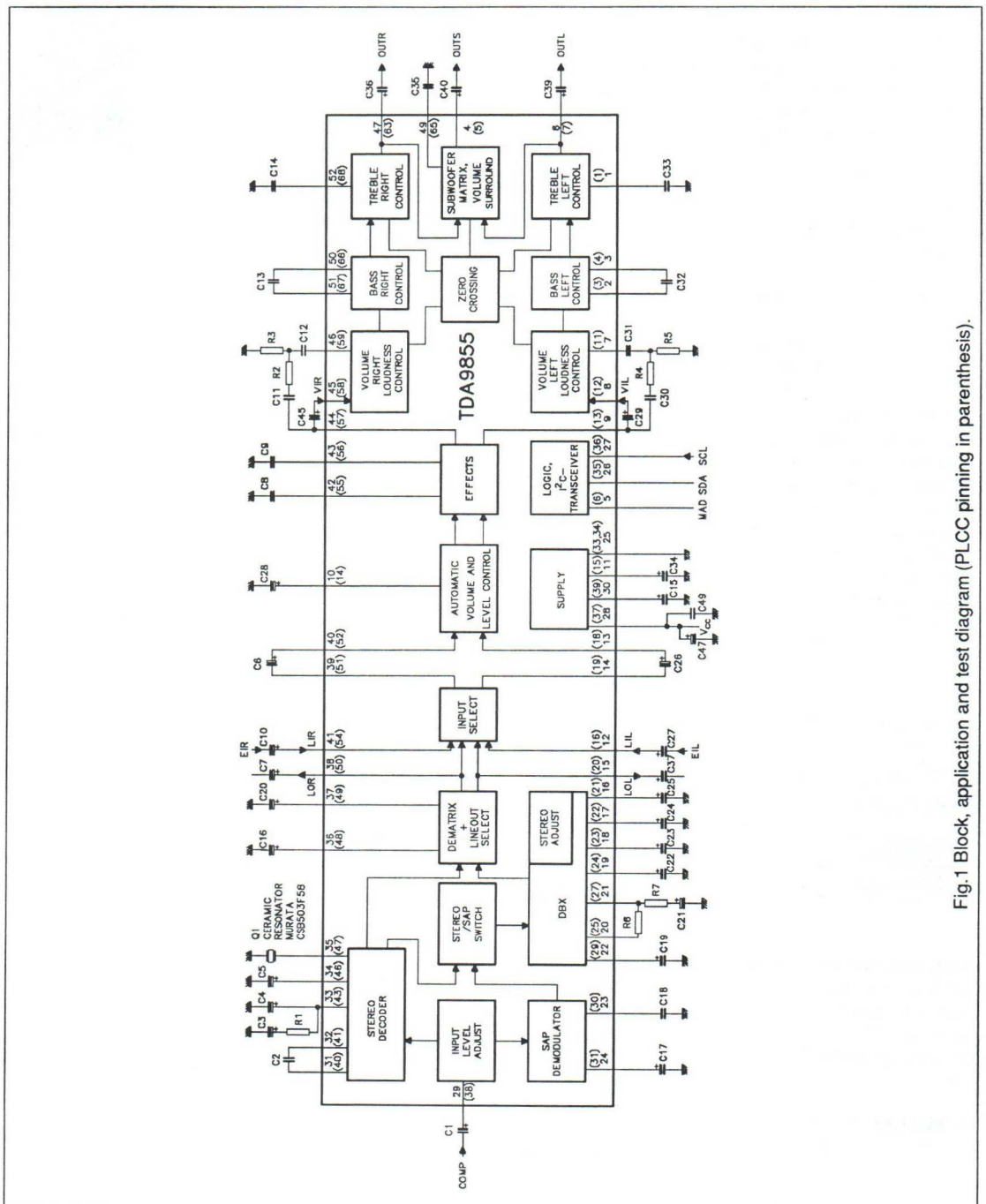


Fig.1 Block, application and test diagram (PLCC pinning in parenthesis).

COMPONENT LIST

elco ±20%; foil or ceramic ±10%; resistors ±5% unless otherwise specified.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	elco	63 V
C2	470 nF	foil	
C3	4.7 µF	elco	63 V
C4	220 nF	foil	
C5	10 µF	elco	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	elco	16 V
C7	4.7 µF	elco	16 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	elco	63 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C13	33 nF	foil	±5%
C14	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C15	100 µF	elco	16 V
C16	4.7 µF	elco	63 V
C17	4.7 µF	elco	63 V
C18	100 nF	foil	
C19	10 µF	elco	63 V
C20	4.7 µF	elco	63 V
C21	47 nF	foil	±5%
C22	1 µF	elco	63 V
C23	1 µF	elco	63 V
C24	10 µF	elco	63 V ±10%
C25	10 µF	elco	63 V ±10%
C26	2.2 µF	elco	16 V
C27	2.2 µF	elco	63 V
C28	4.7 µF	elco	63 V ±10%
C29	2.2 µF	elco	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C31	150 nF	foil	±5%
C32	33 nF	foil	±5%
C33	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	elco	16 V
C35	150 nF	foil	±5%
C36	4.7 µF	elco	16 V
C37	4.7 µF	elco	16 V
C39	4.7 µF	elco	16 V
C40	4.7 µF	elco	16 V
C45	2.2 µF	elco	16 V
C47	220 µF	elco	25 V
C49	100 nF	foil or ceramic	SMD 1206

COMPONENT	VALUE	REMARK
R1	2.2 kΩ	
R2	20 kΩ	
R3	2.2 kΩ	
R4	20 kΩ	
R5	2.2 kΩ	
R6	8.2 kΩ	±2%
R7	160 Ω	±2%
Q1	503.5 kHz	MURATA CSB503F58

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{comp}	input signal (RMS value)	100% modulation L + R; f = 300 Hz	–	250	–	mV
V_{LOR}, V_{LOL}	output signal (RMS value)		–	500	–	mV
G_{LA}	input level adjustment control range		–3.5	–	+4.0	dB
α_{st}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion	f = 1 kHz	–	0.2	–	%
$V_{I,O}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_c	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f = 40 Hz	–	17	–	dB
G_b	bass control range	f = 40 Hz	–12	–	+16.5	dB
G_t	treble control range	f = 15 kHz	–12	–	+12	dB
G_v	subwoofer control range	f = 40 Hz	–14	–	+14	dB
S/N	signal-to-noise ratio	line out (mono); V_O = 0.5 V (RMS)				
	CCIR noise weighting filter (peak value)		–	60	–	dB
	DIN noise weighting filter (RMS value)		–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_O = 2 V (RMS); gain = 0 dB				
	CCIR noise weighting filter (peak value)		–	94	–	dB
	DIN noise weighting filter (RMS value)		–	107	–	dBA

PINNING

SYMBOL	SOT188	SOT247	DESCRIPTION
TL	1	1	treble control capacitor, left channel
n.c.	2	–	not connected
B1L	3	2	bass control capacitor, left channel
B2L	4	3	bass control capacitor, left channel
OUTS	5	4	output subwoofer or output surround sound
MAD	6	5	programmable address bit (module address)
OUTL	7	6	output, left channel
n.c.	8 to 10	–	not connected
LDL	11	7	input loudness, left channel
VIL	12	8	input volume control, left channel
EOL	13	9	output effects, left channel
CAV	14	10	automatic volume control capacitor
V_{REF}	15	11	reference voltage $0.5V_{CC}$
LIL	16	12	line input, left channel
n.c.	17	–	not connected
AVL	18	13	input automatic volume control, left channel
SOL	19	14	output selector, left channel
LOL	20	15	line output, left channel
TW	21	16	capacitor timing wideband for dbx
TS	22	17	capacitor timing spectral for dbx
CW	23	18	capacitor wideband for dbx
CS	24	19	capacitor spectral for dbx
VEO	25	20	variable emphasis out for dbx
n.c.	26	–	not connected
VEI	27	21	variable emphasis in for dbx
n.c.	28	–	not connected
CNR	29	22	capacitor noise reduction for dbx
CM	30	23	capacitor mute for SAP
CD	31	24	capacitor DC decoupling for SAP
n.c.	32	–	not connected
GND	33	–	analog ground
GND	34	–	digital ground
GND	–	25	common ground
SDA	35	26	serial data input/output
SCL	36	27	serial clock input
V_{CC}	37	28	supply voltage
COMP	38	29	input composite signal
VCAP	39	30	capacitor for electronic filtering of supply
CP1	40	31	capacitor for pilot detector
CP2	41	32	capacitor for pilot detector
n.c.	42	–	not connected
CPH	43	33	capacitor for phase detector
n.c.	44, 45	–	not connected

SYMBOL	SOT188	SOT247	DESCRIPTION
CA	46	34	capacitor for filter adjust
CER	47	35	ceramic resonator
CMO	48	36	capacitor DC decoupling mono
CSS	49	37	capacitor DC decoupling stereo/SAP
LOR	50	38	line output, right channel
SOR	51	39	output selector, right channel
AVR	52	40	input automatic volume control, right channel
n.c.	53	–	not connected
LIR	54	41	line input, right channel
PS2	55	42	capacitor 2 pseudo function
PS1	56	43	capacitor 1 pseudo function
EOR	57	44	output effects, right channel
VIR	58	45	input volume control, right channel
LDR	59	46	input loudness, right channel
n.c.	60 to 62	–	not connected
OUTR	63	47	output, right channel
n.c.	64	48	not connected
SW	65	49	filter capacitor for subwoofer
B2R	66	50	bass control capacitor, right channel
B1R	67	51	bass control capacitor, right channel
TR	68	52	treble control capacitor

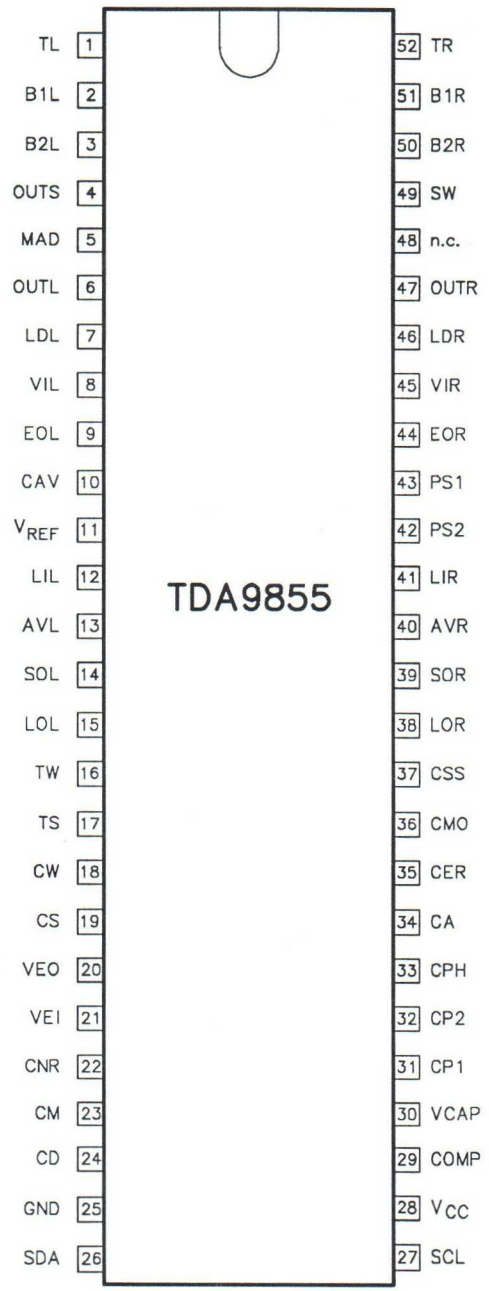


Fig.2 Pin configuration for SHRDIL-version.

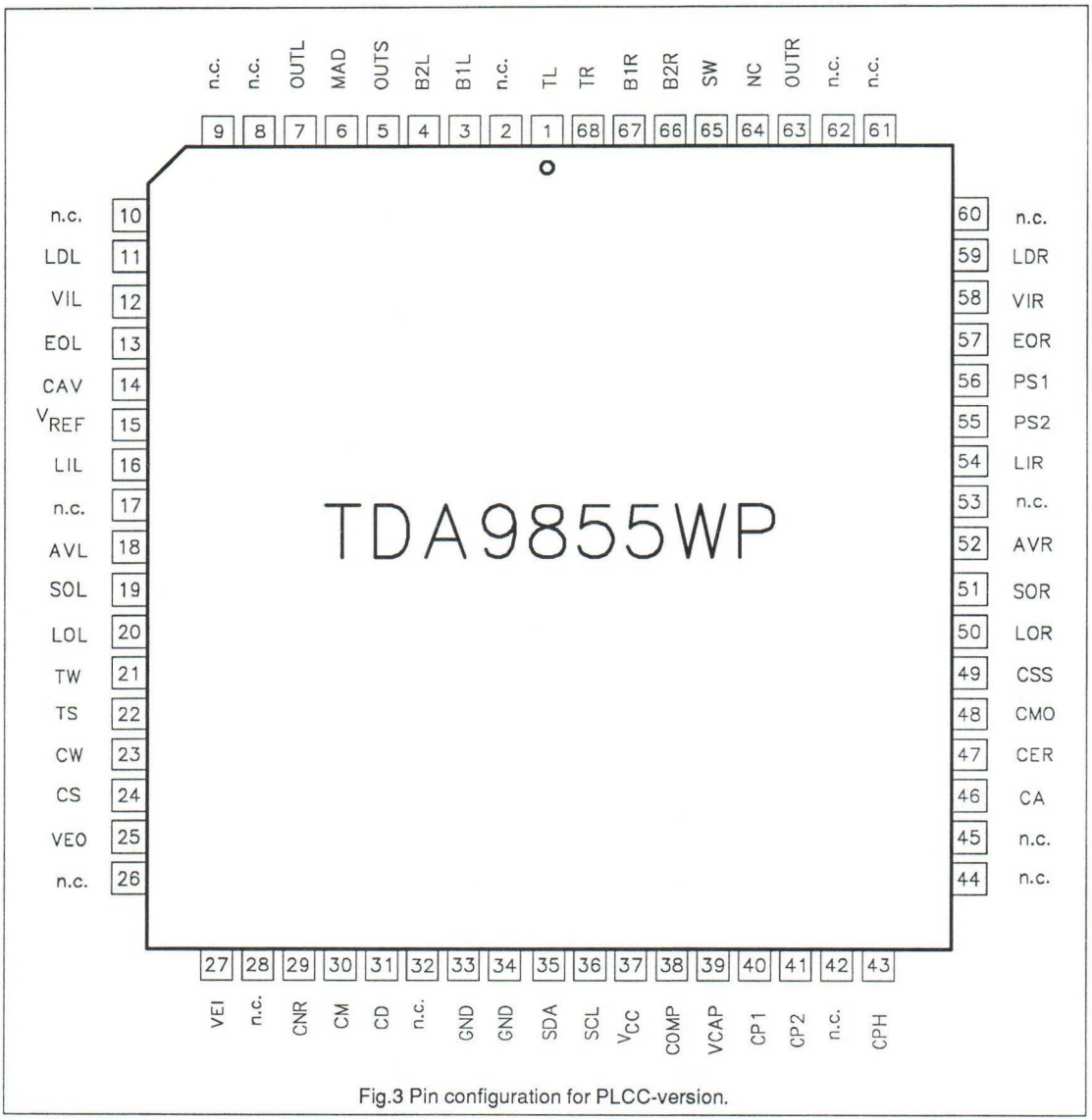


Fig.3 Pin configuration for PLCC-version.

FUNCTIONAL DESCRIPTION

Decoder

Input level adjustment

The composite input signal is fed to the input level adjustment stage. In order to compensate tolerances of the FM demodulator which supplied the composite input signal, the TDA9855 provides an input level adjustment stage. The control range is between –3.5 dB and +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 2 and 3 and the level adjust setting of Table 16 allows an optimal signal adjustment during the set alignment in the production line. This value has to be stored in a none volatile memory. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 µs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded subsignal L – R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation can be adjusted by an automatic procedure or manually. A detailed description of this alignment is provided in the ADJUSTMENT PROCEDURE. The stereo identification can be read by the I²C-bus (see Table 1). Two different pilot thresholds can be selected via I²C-bus (see Table 18).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in case of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 1).

Switch

The stereo/SAP switch feeds either the L – R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/line out select circuit. Table 15 shows the different switch modes provided at the output pins LOR and LOL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system according to the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

Selector

The selector allows selecting either the internal line out signals LOR or LOL (dematrix out) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Table 8). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

Automatic volume level control

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range between 0.1 and 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched off. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor at pin CAV determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I²C-bus (see notes 3 and 4 of the CHARACTERISTICS).

Effects

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 13).

Volume/loudness

The volume control range is between +16 dB and –71 dB in steps of 1 dB and ends with a mute step (see Table 4). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of –12 dB. At –12 dB volume control the maximum loudness boost is obtained. The filter characteristic is

determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via the I²C-bus control (see Table 10). The left and right volume control stages include two independent zero crossing detectors. In the zero cross mode a change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting. The zero crossing mode is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case of need to mute only one channel, two steps are necessary. The first step is a transmission from any steps to –71 dB and the second is –71 dB step to mute. The step of –71 dB to mute has no zero crossing but it is not relevant. This procedure has to be provided by software.

Bass control

A single external 33 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass control range of +16.5 dB to –12 dB in steps of 1.5 dB at low frequencies (40 Hz). Internally the basic step width is 3 dB, with intermediate steps are obtained by a toggle function that provides additional an 1.5 dB boost or attenuation (see Table 5). Please note that both loudness and bass control together result in a maximum bass boost of 34.5 dB for low volume steps.

Treble control

The adjustable range of the treble control stage is between –12 dB and +12 dB in steps of 3 dB. The filter characteristic is determined by an external 5.6 nF capacitor for each channel. The logic circuitry is arranged in a way that the same data words (HEX 06 to 16) can be used for both tone controls if a bass control range from –12 dB to +12 dB and a treble control range from –12 dB to +12 dB with 3 dB steps are used (see Tables 5 and 6).

Subwoofer; surround sound control

The subwoofer or the surround mode can be activated with the control bit SUR (see Table 3). A low bit provides an output signal (L + R)/2 in subwoofer mode, a high bit selects surround mode and provides an output signal (L – R)/2. The signal is fed through a volume control stage with a range between +14 dB and –14 dB in 2 dB steps on top of the main channel control to the output pin OUTS. The last setting is the mute position (see Table 7). The capacitor C35 at pin SW provides a 230 Hz low-pass filter in subwoofer mode. In surround mode this capacitor should be disconnected. If balance is not in mid position the selected left and right output levels will be combined.

Mute

The mute function can be activated independently with the last step of volume or subwoofer/surround control at the left, right or center output. By setting the general mute bit GMU via the I²C-bus all audio part outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:

TZCM = 0:
forced mute with direct execution,

TZCM = 1:
execution in time with signal zero crossing.

In the zero cross mode a change of the GMU bit is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:

- a first transmission for mute execution
- a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)
- a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	9.5	V
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1			
V_n	voltage at all other pins to pin GND		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT247AH	43 K/W
	SOT188CG	38 K/W

Requirements for the composite input signal to ensure proper system performance.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R}$	composite input level for 100% modulation L + R (25 kHz deviation), RMS, f = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_O	output impedance	note 1	–	low-ohmic	5	kΩ
$f_{-2\ dB}$	roll-off frequencies (25 kHz deviation L + R)	low frequency (–2 dB)	–	–	5	Hz
		high frequency (–2 dB)	100	–	–	kHz
THD	total harmonic distortion L + R; f = 1 kHz	25 kHz deviation	–	–	0.5	%
		125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f = 1 kHz; 75 μs de-emphasis				
		critical picture modulation	44	–	–	dB
		with sync only	54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n x f_H; no de-emphasis; L + R: 25 kHz deviation, f = 1 kHz	40	–	–	dB

Notes to the requirements

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see input level adjustment control) must be taken into account.
2. In order to prevent clipping at overmodulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V, source resistance ≤ 600 Ω, output load R_L ≥ 10 kΩ, C_L ≤ 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; volume gain control G_c = 0 dB; bass linear; treble linear; loudness off; AVL off; effects linear; composite input signal according to BTSC standard; see block diagram unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{DC}	DC voltage at signal handling pins		–	$V_{CC}/2$	–	V
DECODER SECTION						
Input level adjustment control						
G_{LA}	input level adjustment control	maximum gain	–	4.0	–	dB
		maximum attenuation	–	–3.5	–	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(RMS)}$	maximum input level		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input level for 100% modulation L + R (25 kHz deviation) (RMS value)	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input level for 100% modulation L – R (50 kHz deviation) (peak value)		–	707	–	mV
MPX_{max}	headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15% for 75 µs equivalent input modulation	9	–	–	dB
MPX_{pilot}	nominal stereo pilot level (RMS value)		–	50	–	mV
ST_{ON}	pilot threshold STEREO ON (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
ST_{OFF}	pilot threshold STEREO OFF (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hyst	hysteresis		–	2.5	–	dB
Out_{L+R}	output level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{ST}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation; alignment at f_L = 300 Hz; f_R = 3.1 kHz				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB
$L,R_{(f)}$	L, R frequency response	14% modulation; $f_{reference}$ = 300 Hz L or R				
		50 Hz to 11 kHz	–3	–	–	dB
		12 kHz	–	–3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f = 1 kHz	–	0.2	1.0	%
S/N	S/N CCIR 468-2 weighted; quasi peak; V_O = 500 mV (RMS)	LINE OUT in position MONO	50	60	–	dB
Stereo decoder, oscillator (VCXO)						
f_o	nominal VCXO frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free running frequency		500.0	–	507.0	kHz
Remark: The oscillator is designed to work together with MURATA resonator CSB503F58 for TDA9855. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58 for TDA9855.						
Δf_H	capture range (nominal pilot)		±190	±265	–	Hz
SAP demodulator						
Remark: The internal SAP carrier level is determined by the composite input level and the level adjust gain.						
SAP_{IN}	nominal SAP carrier input level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
SAP_{ON}	pilot threshold SAP ON (RMS value)		–	–	85	mV
SAP_{OFF}	pilot threshold SAP OFF (RMS value)		35	–	–	mV
SAP_{HYS}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output level at LINE OUT (RMS value)	LINE OUT (LOL, LOR) in position SAP / SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
F_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; $f_{reference}$ = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	1 kHz	–	0.5	2.0	%
LINE OUT (at pins LOL, LOR)						
V_o	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
Headr	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
Out_{DC}	DC output voltage		0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$\alpha_{ST\text{-}SAP}$	idle crosstalk L, R into SAP	100% modulation; f = 1 kHz; L or R; LINE OUT switched to SAP / SAP	50	–	–	dB
$\alpha_{SAP\text{-}ST}$	idle crosstalk SAP into L, R	100% modulation; f = 1 kHz; SAP; LINE OUT switched to stereo	50	–	–	dB
$\Delta V_{ST\text{-}SAP}$	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dbx noise reduction circuit						
t_{adj}	stereo adjust time	see adjustment procedure	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin 17 (pin 22) via current meter connected to $V_{CC}/2 + 1$ V	–	24	–	µA
ΔI_s	spread of timing current		–	–	15	%
$I_{s\ range}$	timing current adjustment range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$I_s/3$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s
AUDIO PART Circuit section from pins LIL, LIR to pins OUTL, OUTR, OUTS Select in to input line control						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27}, C_{29} = 2.2 µF; $Z_i = Z_{i\ min}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 1 V (RMS); G_c = 0 dB; AVL off	–	0.05	–	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL off	–	0.02	–	%
RR	power supply ripple rejection	$V_{r(RMS)}$ < 200 mV; f = 100 Hz	47	50	–	dB
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 1	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak	–	40	80	µV
		measured in dBA	–	8	–	µV
α_{cs}	channel separation	V_i = 1 V; f = 1 kHz	75	–	–	dB
		V_i = 1 V; f = 12.5 kHz	75	–	–	dB
Selector (from pins LOL, LOR, LIL, LIR to pins SOL, SOR)						
Z_i	input impedance		16	20	24	kΩ
α_s	input isolation of one selected source to the other input	f = 1 kHz; V_i = 1 V	86	96	–	dB
		f = 12.5 kHz; V_i = 1 V	80	96	–	dB
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector out by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
G_c	voltage gain, selector		–	0	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic volume level control (AVL)						
Z_i	input impedance		8.8	11.0	13.2	kΩ
$V_{i(RMS)}$	maximum input voltage	THD < 0.2%	2	–	–	V
G_v	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{i(RMS)}$	input level at maximum boost	see Fig.4	–	0.1	–	V
	input level at maximum attenuation		–	1.125	–	V
$V_{o(RMS)}$	output level in AVL operation range		160	200	250	mV
$V_{DC\ OFF}$	DC offset between different gain steps	note 2; voltage at pin CAV				
		6.50 V to 6.33 V	–	–	6	mV
		6.33 V to 6.11 V	–	–	6	mV
		6.11 V to 5.33 V	–	–	6	mV
		5.33 V to 2.60 V	–	–	6	mV
R_{att}	discharge resistors for attack time constant	note 3;				
		AT1 = 0; AT2 = 0	340	420	520	Ω
		AT1 = 1; AT2 = 0	590	730	910	Ω
		AT1 = 0; AT2 = 1	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	note 4	1.6	2.0	2.4	μA
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.5	–	–	–	–
Volume tone control part (input pins VIL, VIR to pins OUTX, to pin OUTS)						
Z_i	input impedance volume input		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_c = 16 dB	–	110	220	μV
		G_c = 0 dB	–	33	50	μV
		mute position	–	10	–	μV
G_c	total continuous control range					
	maximum boost		–	16	–	dB
	maximum attenuation		–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_c = +16 to –50 dB	–	–	2	dB
		G_c = –51 to –71 dB	–	–	3	dB
ΔG_t	gain tracking error	G_c = +16 to –50 dB	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_c = +16 to 0 dB	–	0.2	10.0	mV
		G_c = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_c = +16 to +1 dB	–	2	15	mV
		G_c = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components; see Fig.6;				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control (see Fig.7)						
G_b	bass control maximum boost	f = 40 Hz	15.5	16.5	17.5	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
G_{step}	step resolution	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	15	mV
Treble control (see Fig.8)						
G_t	treble control maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution	f = 15 kHz	–	3	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	10	mV
Subwoofer or surround control						
G_s	subwoofer control	f = 40 Hz				
	maximum boost		12	14	16	dB
	maximum attenuation		12	14	16	dB
G_{step}	step resolution		–	2	–	dB
α_m	mute attenuation		60	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_s = 0 to +14 dB	–	–	10	mV
		G_s = 0 to –14 dB	–	–	5	mV
	DC step offset between any step to mute	G_s = +2 to +14 dB without input offset (pin SW connected to V_{REF})	–	–	15	mV
		G_s = +2 to +14 dB inclusive offset from OUTR, OUTL	–	–	50	mV
		G_s = 0 to –14 dB	–	–	10	mV
R_F	internal resistor for low-pass filter with external capacitor at pin SW		4	5	6	kΩ
L + R_{REJ}	common mode rejection in surround sound at pin OUTS	mono signal at VIL/VIR; f = 1 kHz; V_i = 1 V; balance = 0 dB	26	36	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop for OUTL, OUTR, OUTS						
$V_{CC-DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power on reset						
When reset is active the GMU-bit (general mute) and the LMU-bit (LINEOUT - mute) is set and the I²C-bus receiver is in reset position						
V_{CC}	start of reset	increasing supply voltage	–	–	2.5	V
	end of reset		5.2	6	6.8	V
	start of reset	decreasing supply voltage	4.2	5	5.8	V
Digital part (I²C-bus pins; note 5)						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The transmission contains:
   - total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   - clock frequency = 50 kHz
   - repetition burst rate = 400 Hz
   - maximum bus signal amplitude = 5 V_{p-p}.
2. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB, –15 dB.
3. Attack time constant = C_{AV} x R_{att}.
4. $$\text{Decay time} = \frac{C_{AV} \times 0.76\ V \left(10^{-\frac{G_{v1}}{20}} - 10^{-\frac{G_{v2}}{20}}\right)}{I_{dec}}$$
   Example: C_{AV} = 4.7 μF; I_{dec} = 2 μA; G_{v1} = –9 dB; G_{v2} = +6 dB → decay time result: 4.14 s.
5. The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request. The maximum clock frequency is 100 kHz.

ADJUSTMENT PROCEDURE

Composite input level adjustment. Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R, f = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ± 20 mV). Store the setting in a none volatile memory. Adjustment of spectral and wideband expander via stereo channel separation adjust.

Automatic adjustment procedure

- Capacitors of external inputs EIL, EIR must be grounded
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus. To avoid anoing sound level set GMU bit to '1' during adjustment procedure
- Effects, AVL, loudness off
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 8)
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 15)
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself
- After 1 s, stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see I²C-bus protocol) and store it in a none volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

Manual adjust

Manual adjust is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz, 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz, 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimal adjust
- Store data in none volatile memory.

After every POWER ON, the alignment data and the input level adjustment data must be loaded from the none volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 19, as recommended by dbx.

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/W	A	DATA	MA	DATA	P

Where:

S	=	start condition, generated by the master
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	1 (read), generated by the master
A	=	acknowledge, generated by the slave
DATA	=	slave transmits an 8-bit data word
MA	=	acknowledge, generated by the master
P	=	stop condition, generated by the master

Table 1 Definition of the transmitted bytes after read condition.

FUNCTION	BYTE	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Function of the bits:

STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1x to A2x	stereo alignment read data
A1x	for wideband expander
A2x	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then the slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmitts condition P.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/W	A	SUBADDRESS	A	DATA	A	P

Where:

S	=	start condition
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	0 (write)
A	=	acknowledge, generated by the slave
SUBADDRESS (SAD)	=	see Table 2
DATA	=	see Table 3
P	=	stop condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress according to the order of Table 2 is performed.

Subaddress

Table 2 Second byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	HEX
volume right	VR	0	0	0	0	0	0	0	0	00
volume left	VL	0	0	0	0	0	0	0	1	01
bass	BA	0	0	0	0	0	0	1	0	02
treble	TR	0	0	0	0	0	0	1	1	03
subwoofer	SW	0	0	0	0	0	1	0	0	04
control 1	CON1	0	0	0	0	0	1	0	1	05
control 2	CON2	0	0	0	0	0	1	1	0	06
control 3	CON3	0	0	0	0	0	1	1	1	07
alignment 1	ALI1	0	0	0	0	1	0	0	0	08
alignment 2	ALI2	0	0	0	0	1	0	0	1	09
alignment 3	ALI3	0	0	0	0	1	0	1	0	0A

Definition of third byte

Table 3 Third byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
bass	BA	0	0	0	BA4	BA3	BA2	BA1	BA0
treble	TR	0	0	0	TR4	TR3	TR2	TR1	0
subwoofer	SW	0	0	SW5	SW4	SW3	SW2	0	0
control 1	CON1	GMU	AVLON	LOFF	0	SUR	SC2	SC1	SC0
control 2	CON2	SAP	STEREO	TZCM	VZCM	LMU	EF2	EF1	EF0
control 3	CON3	0	0	0	0	L3	L2	L1	L0
alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0

Function of the bits:

VR0 to VR6	volume control right
VL0 to VL6	volume control left
BA0 to BA4	bass control
TR1 to TR3	treble control
SW2 to SW5	subwoofer, surround control
GMU	mute control for all outputs (general mute)
AVLON	AVL on/off
LOFF	switch loudness on/off
SUR	surround/subwoofer SUR = 1 → (L – R)/2; SUR = 0 → (L + R)/2
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (treble and subwoofer/surround output stage)
VZCM	zero cross mode in volume operation
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjust
ADJ	stereo adjust on/off
A1X	stereo alignment data for wideband expander
A2X	stereo alignment data for spectral expander
AT1, AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 4 Volume setting in register VR and VL.

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
16	1	1	1	1	1	1	1	7F
15	1	1	1	1	1	1	0	7E
14	1	1	1	1	1	0	1	7D
13	1	1	1	1	1	0	0	7C
12	1	1	1	1	0	1	1	7B
11	1	1	1	1	0	1	0	7A
10	1	1	1	1	0	0	1	79
9	1	1	1	1	0	0	0	78
8	1	1	1	0	1	1	1	77
7	1	1	1	0	1	1	0	76
6	1	1	1	0	1	0	1	75
5	1	1	1	0	1	0	0	74
4	1	1	1	0	0	1	1	73
3	1	1	1	0	0	1	0	72
2	1	1	1	0	0	0	1	71
1	1	1	1	0	0	0	0	70
0	1	1	0	1	1	1	1	6F
–1	1	1	0	1	1	1	0	6E
–2	1	1	0	1	1	0	1	6D
–3	1	1	0	1	1	0	0	6C
–4	1	1	0	1	0	1	1	6B
–5	1	1	0	1	0	1	0	6A
–6	1	1	0	1	0	0	1	69
–7	1	1	0	1	0	0	0	68
–8	1	1	0	0	1	1	1	67
–9	1	1	0	0	1	1	0	66
–10	1	1	0	0	1	0	1	65
–11	1	1	0	0	1	0	0	64
–12	1	1	0	0	0	1	1	63
–13	1	1	0	0	0	1	0	62
–14	1	1	0	0	0	0	1	61
–15	1	1	0	0	0	0	0	60
–16	1	0	1	1	1	1	1	5F
–17	1	0	1	1	1	1	0	5E
–18	1	0	1	1	1	0	1	5D
–19	1	0	1	1	1	0	0	5C
–20	1	0	1	1	0	1	1	5B
–21	1	0	1	1	0	1	0	5A
–22	1	0	1	1	0	0	1	59
–23	1	0	1	1	0	0	0	58
–24	1	0	1	0	1	1	1	57
–25	1	0	1	0	1	1	0	56
–26	1	0	1	0	1	0	1	55
–27	1	0	1	0	1	0	0	54
–28	1	0	1	0	0	1	1	53
–29	1	0	1	0	0	1	0	52
–30	1	0	1	0	0	0	1	51
–31	1	0	1	0	0	0	0	50
–32	1	0	0	1	1	1	1	4F
–33	1	0	0	1	1	1	0	4E

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
–34	1	0	0	1	1	0	1	4D
–35	1	0	0	1	1	0	0	4C
–36	1	0	0	1	0	1	1	4B
–37	1	0	0	1	0	1	0	4A
–38	1	0	0	1	0	0	1	49
–39	1	0	0	1	0	0	0	48
–40	1	0	0	0	1	1	1	47
–41	1	0	0	0	1	1	0	46
–42	1	0	0	0	1	0	1	45
–43	1	0	0	0	1	0	0	44
–44	1	0	0	0	0	1	1	43
–45	1	0	0	0	0	1	0	42
–46	1	0	0	0	0	0	1	41
–47	1	0	0	0	0	0	0	40
–48	0	1	1	1	1	1	1	3F
–49	0	1	1	1	1	1	0	3E
–50	0	1	1	1	1	0	1	3D
–51	0	1	1	1	1	0	0	3C
–52	0	1	1	1	0	1	1	3B
–53	0	1	1	1	0	1	0	3A
–54	0	1	1	1	0	0	1	39
–55	0	1	1	1	0	0	0	38
–56	0	1	1	0	1	1	1	37
–57	0	1	1	0	1	1	0	36
–58	0	1	1	0	1	0	1	35
–59	0	1	1	0	1	0	0	34
–60	0	1	1	0	0	1	1	33
–61	0	1	1	0	0	1	0	32
–62	0	1	1	0	0	0	1	31
–63	0	1	1	0	0	0	0	30
–64	0	1	0	1	1	1	1	2F
–65	0	1	0	1	1	1	0	2E
–66	0	1	0	1	1	0	1	2D
–67	0	1	0	1	1	0	0	2C
–68	0	1	0	1	0	1	1	2B
–69	0	1	0	1	0	1	0	2A
–70	0	1	0	1	0	0	1	29
–71	0	1	0	1	0	0	0	28
mute	0	1	0	0	1	1	1	27

Table 5 Bass setting in register BA.

G_b (dB)	DATA D4 BA4	D3 BA3	D2 BA2	D1 BA1	D0 BA0	HEX
16.5	1	1	0	0	1	19
15	1	1	0	0	0	18
13.5	1	0	1	1	1	17
12	1	0	1	1	0	16
10.5	1	0	1	0	1	15
9	1	0	1	0	0	14
7.5	1	0	0	1	1	13
6	1	0	0	1	0	12
4.5	1	0	0	0	1	11
3	1	0	0	0	0	10
1.5	0	1	1	1	1	0F
0	0	1	1	1	0	0E
–1.5	0	1	1	0	1	0D
–3	0	1	1	0	0	0C
–4.5	0	1	0	1	1	0B
–6	0	1	0	1	0	0A
–7.5	0	1	0	0	1	09
–9	0	1	0	0	0	08
–10.5	0	0	1	1	1	07
–12	0	0	1	1	0	06

Table 6 Treble setting in register TR.

G_t (dB)	DATA D4 TR4	D3 TR3	D2 TR2	D1 TR1	HEX
12	1	0	1	1	16
9	1	0	1	0	14
6	1	0	0	1	12
3	1	0	0	0	10
0	0	1	1	1	0E
–3	0	1	1	0	0C
–6	0	1	0	1	0A
–9	0	1	0	0	08
–12	0	0	1	1	06

Table 7 Subwoofer/surround setting in register SW.

G_S (dB)	DATA D5 SW5	D4 SW4	D3 SW3	D2 SW2	HEX
14	1	1	1	1	3C
12	1	1	1	0	38
10	1	1	0	1	34
8	1	1	0	0	30
6	1	0	1	1	2C
4	1	0	1	0	28
2	1	0	0	1	24
0	1	0	0	0	20
–2	0	1	1	1	1C
–4	0	1	1	0	18
–6	0	1	0	1	14
–8	0	1	0	0	10
–10	0	0	1	1	0C
–12	0	0	1	0	08
–14	0	0	0	1	04
mute	0	0	0	0	00

Table 8 Selector setting in register CON1.

FUNCTION: input connected to output	SOR, SOL	DATA D2 SC2	D1 SC1	D0 SC0
input	LOR, LOL	0	0	0
input	LOR, LOR	0	0	1
input	LOL, LOL	0	1	0
input	LOL, LOR	0	1	1
input	LIR, LIL	1	0	0
input	LIR, LIR	1	0	1
input	LIL, LIL	1	1	0
input	LIL, LIR	1	1	1

Table 9 SUR bit setting in register CON1.

FUNCTION	DATA D3
surround sound	1
subwoofer	0

Table 10 LOFF bit setting in register CON1.

CHARACTERISTIC	DATA D5
with loudness	0
linear	1

Table 11 AVLON bit setting in register CON1.

FUNCTION	DATA D6
automatic volume control off	0
automatic volume control on	1

Table 12 Mute setting.

REGISTER CON1		REGISTER CON2	
FUNCTION	DATA D7 GMU	FUNCTION	DATA D3 LMU
forced mute at OUTR, OUTL, OUTS	1	forced mute at LOR, LOL	1
audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 13 Effects setting in register CON2.

FUNCTION	DATA D2 EF2	D1 EF1	D0 EF0
stereo linear on	0	0	0
pseudo on	0	0	1
spatial stereo, 30% anti-phase crosstalk	0	1	0
spatial stereo, 50% anti-phase crosstalk	0	1	1
forced mono	1	1	1

Table 14 Zero cross detection setting in register CON2.

FUNCTION	DATA D5 TZCM	FUNCTION	DATA D4 VZCM
direct mute control	0	direct volume control	0
mute control delayed until the next zero crossing	1	volume control delayed until the next zero crossing	1

Table 15 Switch setting at line out.

FUNCTION		DATA	DATA	
line out signals at		transmission status	setting bits in register CON2	
LOL	LOR	internal switch readable bits in register ALR1, ALR2: D6 SAPP D5 STP	D7 SAP	D6 STEREO
SAP	SAP	SAP received	1	1
mute	mute	no SAP received	1	1
left	right	stereo received	0	1
mono	mono	no stereo received	0	1
mono	SAP	SAP received	1	0
mono	mute	no SAP received	1	0
mono	mono		0	0

Table 16 Level adjust setting in register CON3.

G_I (dB)	DATA D3 L3	D2 L2	D1 L1	D0 L0	HEX
+4	1	1	1	1	0F
+3.5	1	1	1	0	0E
+3	1	1	0	1	0D
+2.5	1	1	0	0	0C
+2	1	0	1	1	0B
+1.5	1	0	1	0	0A
+1	1	0	0	1	09
+0.5	1	0	0	0	08
0	0	1	1	1	07
−0.5	0	1	1	0	06
−1	0	1	0	1	05
−1.5	0	1	0	0	04
−2	0	0	1	1	03
−2.5	0	0	1	0	02
−3	0	0	0	1	01
−3.5	0	0	0	0	00

Table 17 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2.

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
nominal gain	1	0	0	0	0
	0	1	1	1	1
gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

Table 18 STS bit setting in register ALI2 (pilot threshold stereo on).

FUNCTION	DATA D7
STON ≤ 35 mV	1
STON ≤ 30 mV	0

Table 19 Timing current setting in register ALI3.

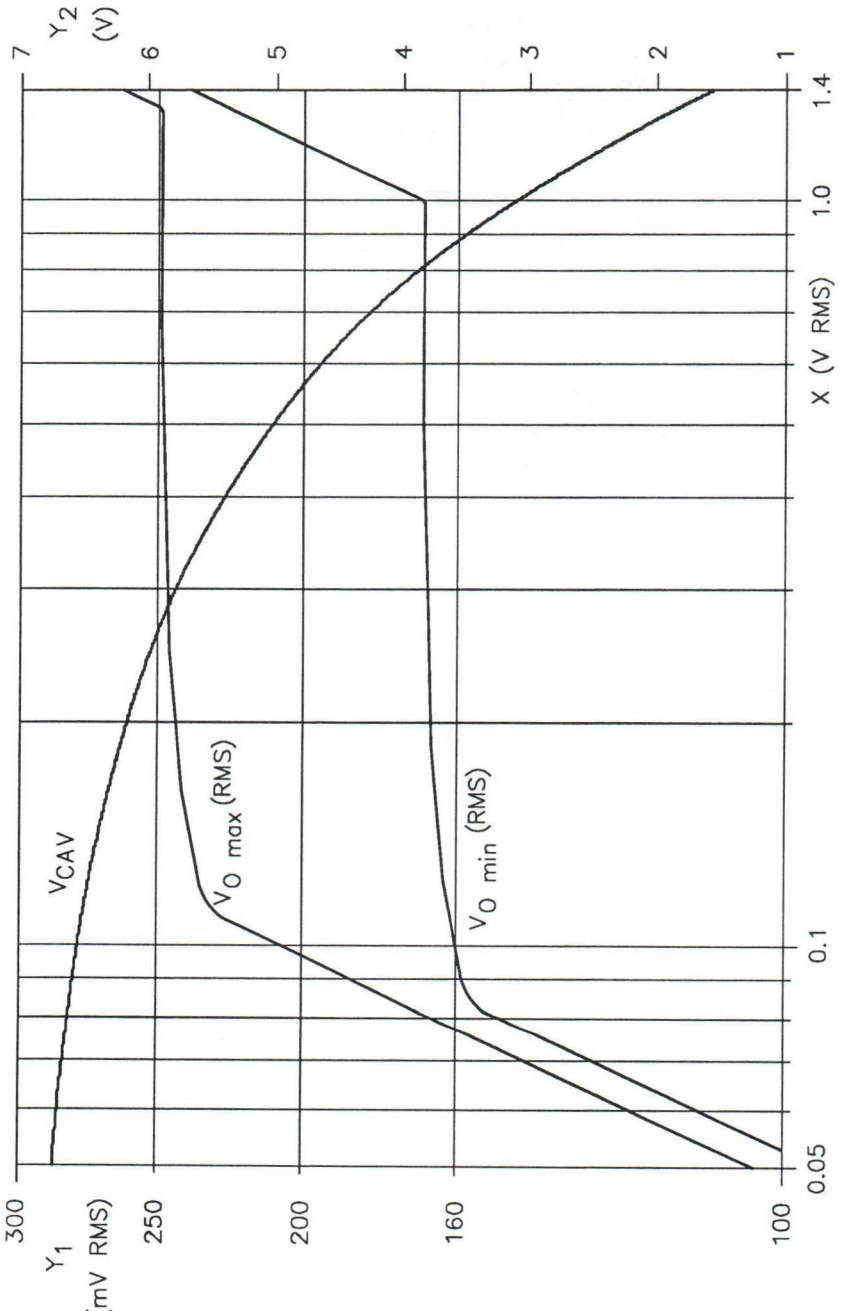
$I_{s\ range}$	DATA D2 TC2	D1 TC1	D0 TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
nominal	0	1	1
−10%	0	1	0
−20%	0	0	1
−30%	0	0	0

Table 20 AVL attack time setting in register ALI3.

R_{att} (Ω)	DATA D6 AT1	D5 AT2
420	0	0
730	1	0
1200	0	1
2100	1	1

Table 21 ADJ bit setting in register ALI3.

FUNCTION	DATA D7
stereo decoder operation mode	0
auto adjustment of channel separation	1



AVL measured at pin EOL/EOR
Y_1 axis: output level in AVL operation with typically 200 mV
Y_2 axis: V_{CAV} DC voltage at pin CAV corresponds with typical gain steps in a range of +6 to −15 dB
X axis: input level V_i

Fig.4 Automatic volume level control diagram.

CURVE	CAPACITANCE AT PIN 43 (56) (nF)	CAPACITANCE AT PIN 42 (55) (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

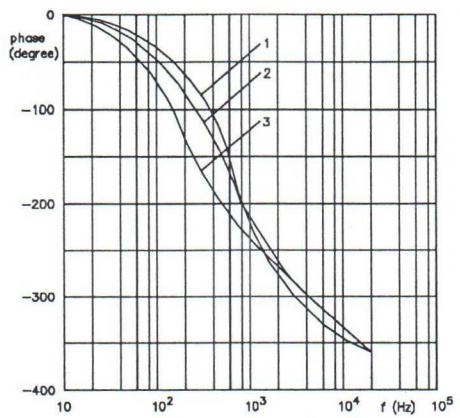


Fig.5 Pseudo (phase in degrees) as a function of frequency (left output).

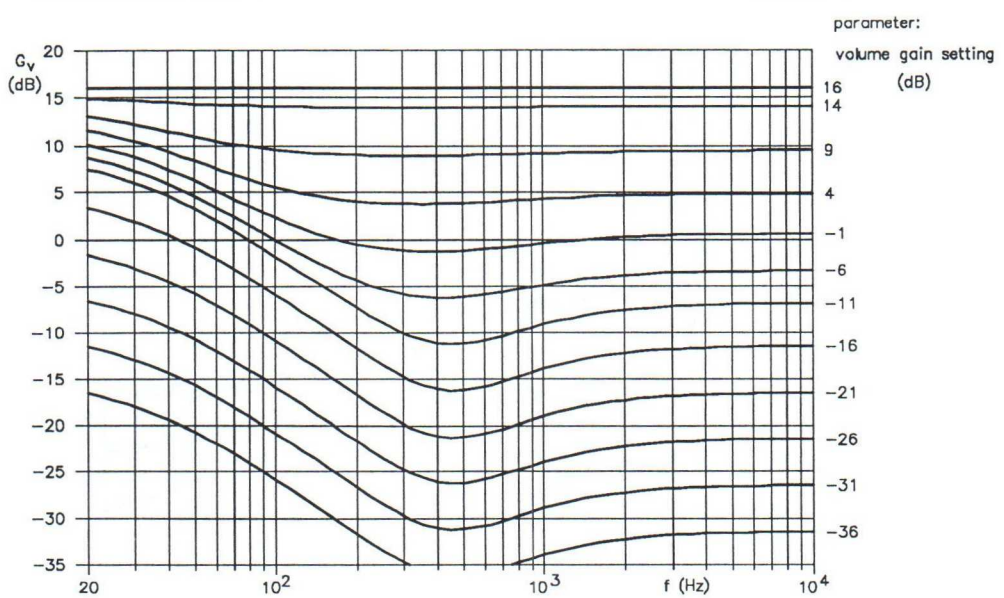


Fig.6 Volume control with loudness.

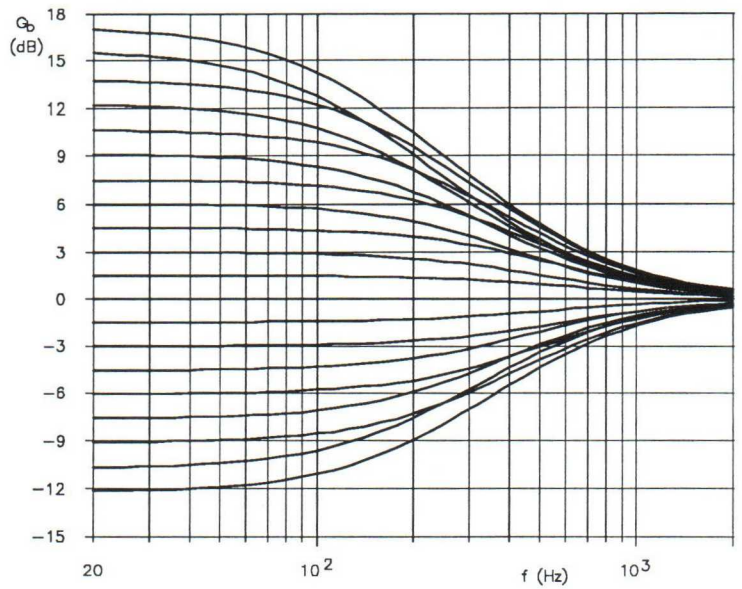


Fig.7 Bass control.

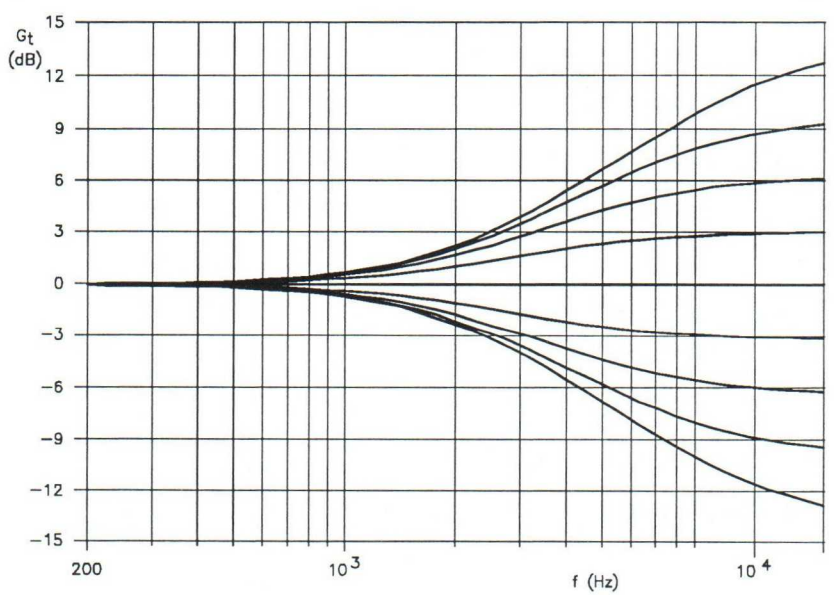


Fig.8 Treble control.

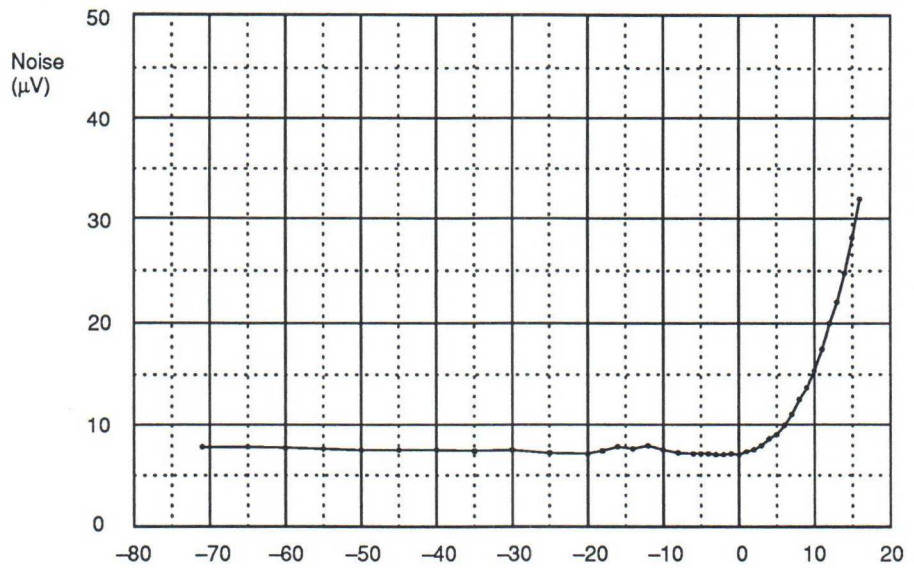


Fig.9 Noise as function of gain in dBA (RMS value).

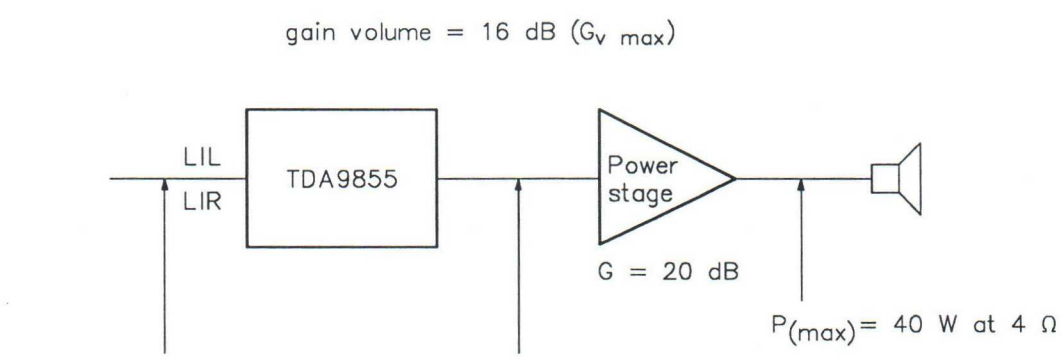


Fig.10 Level diagram.

APPLICATION HINTS

Selection of input signals by using the zero crossing mute mode

A selection between the internal signal path and the external input LIL/LIR produces a modulation click depending on the difference of the signal values at the time of switching. At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (TZCM = 1) and then the mute bit (GMU = 1) via the I²C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time before t_2, the microcontroller has to send the forced mute mode (TZCM = 0) and the return to the zero crossing mode (TZCM = 1) to be sure that mute is enabled.

The output signal remains muted until the next signal zero crossing of input B occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. The zero cross function is working at the lowest frequency of 40 Hz.

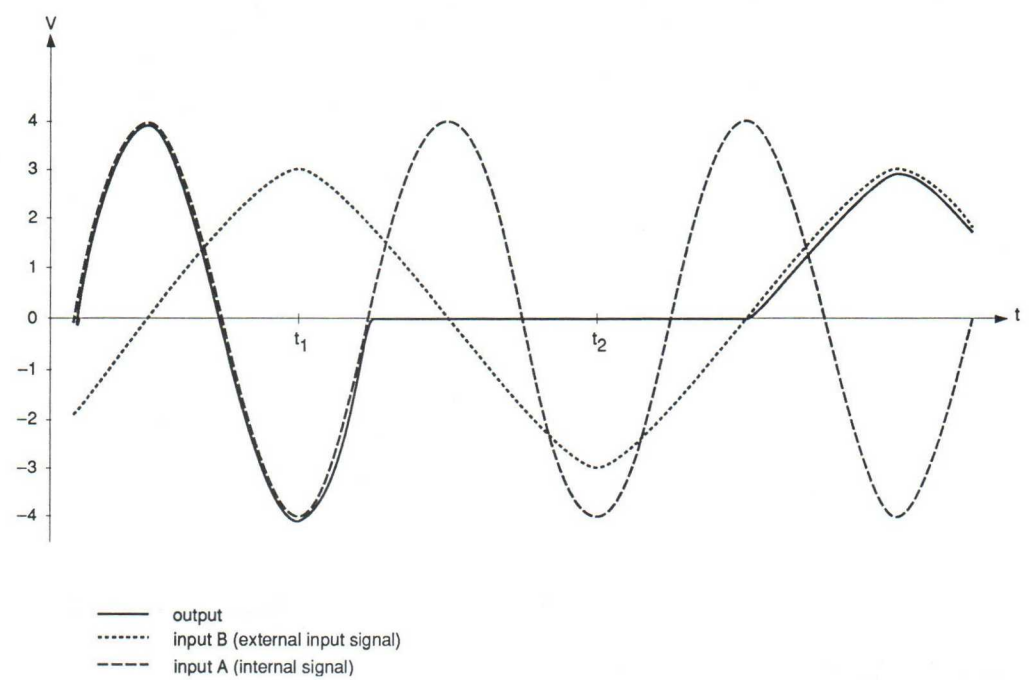


Fig.11 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.12 shows the basic loudness circuit with an external low-pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_1. Both result in a loudness control range of +16 dB to −12 dB.
Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with G_v = −21 dB and R_1 = 33 kΩ results in R_3 = 3.2 kΩ.
For the low-pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v\,reference}$ + 3 dB = −18 dB;
f = 1 kHz and C_1 = 100 nF
If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.
Fig.13 shows an example of the loudness circuit with bass and treble boost.

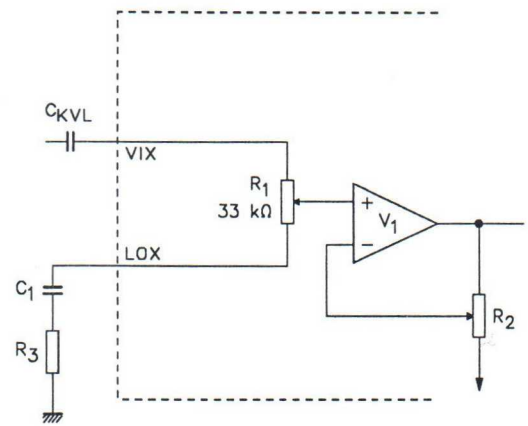


Fig.12 Basic loudness circuit.

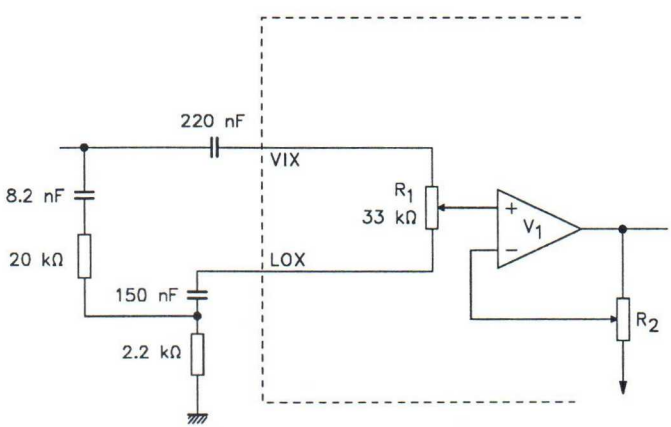


Fig.13 Loudness circuit with bass and treble boost.

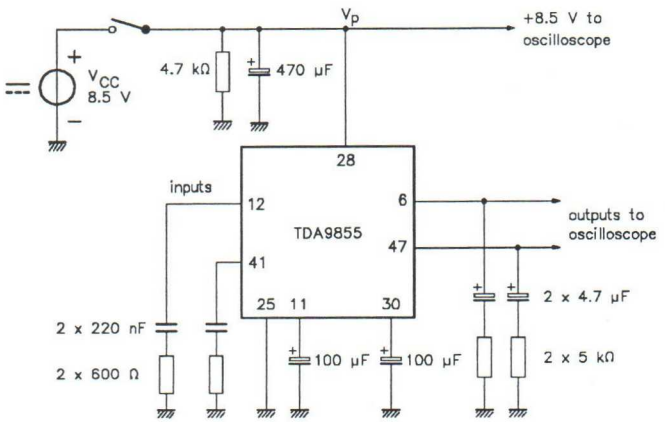


Fig.14 Turn-on/off power supply circuit diagram.

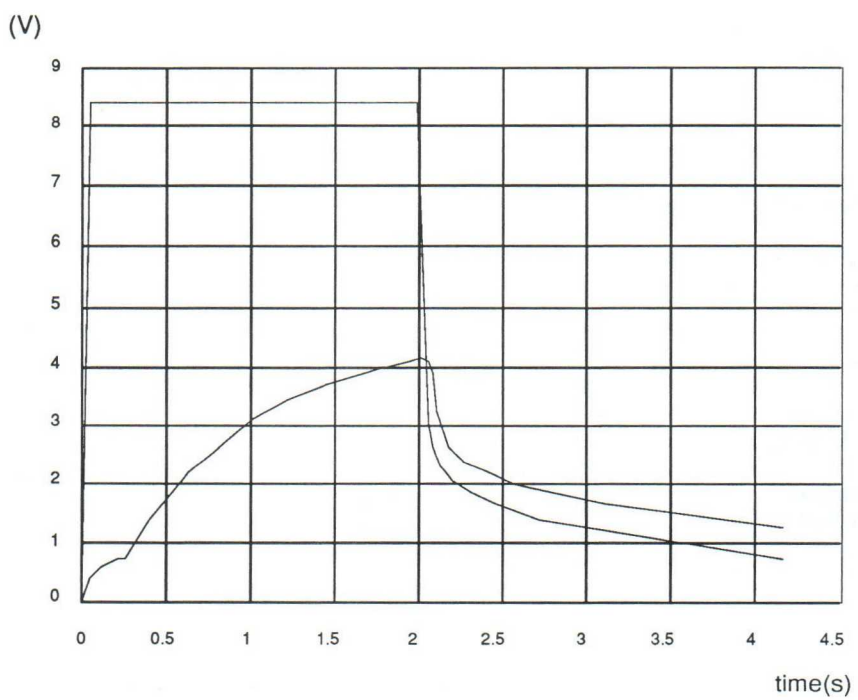
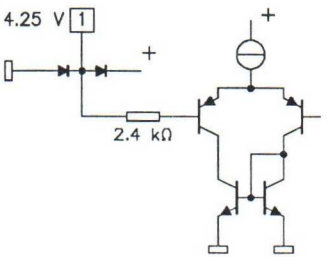
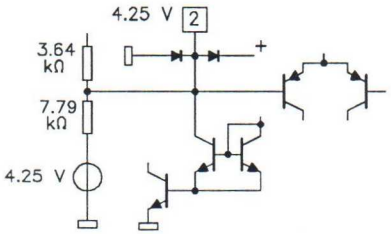


Fig.15 Turn-on/off behaviour.

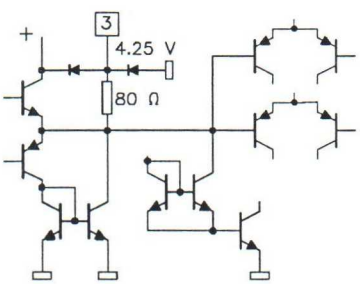
INTERNAL PIN CONFIGURATIONS (pin numbers for SHRDIL-version)



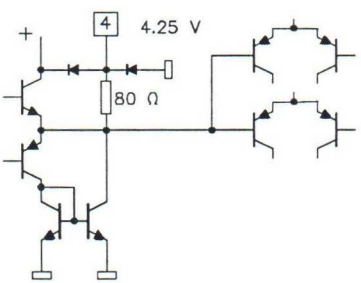
Pin 1: Treble control capacitor, left
Pin 52: Treble control capacitor, right



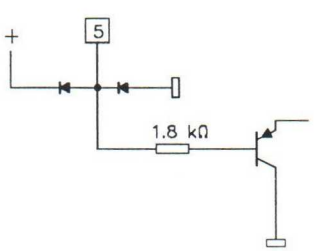
Pin 2: Bass control capacitor input, left
Pin 51: Bass control capacitor input, right



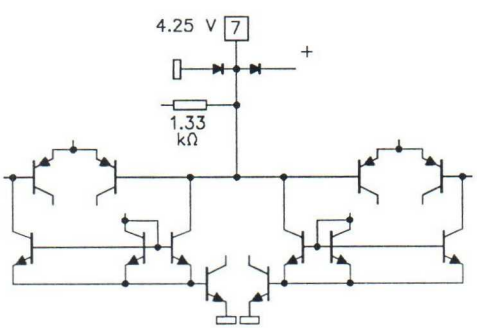
Pin 3: Bass control capacitor output, left
Pin 50: Bass control capacitor output, right



Pin 4: Output subwoofer
Pin 6: Output, left channel
Pin 14: Output selector, left channel
Pin 39: Output selector, right channel
Pin 47: Output, right channel

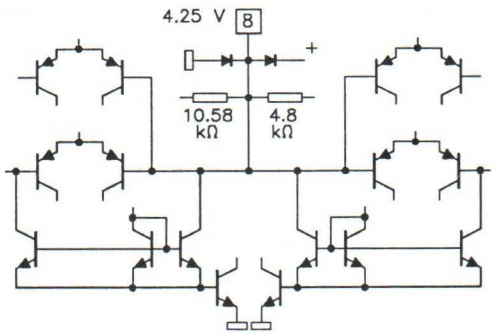


Pin 5: MAD (I²C–bus address switch)

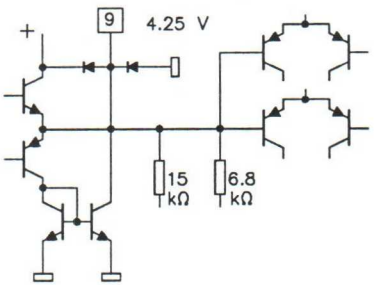


Pin 7: Input loudnes, left
Pin 46: Input loudness, right

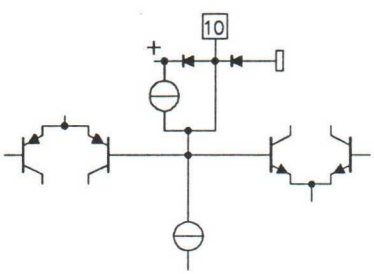
Fig.16 Internal circuits (continued in Fig.17).



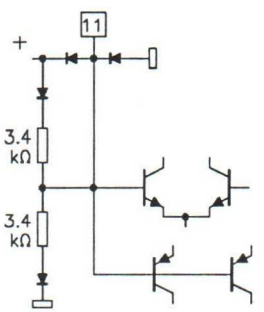
Pin 8: Input volume, left
Pin 45: Input volume, right



Pin 9: Output effects, left
Pin 44: Output effects, right

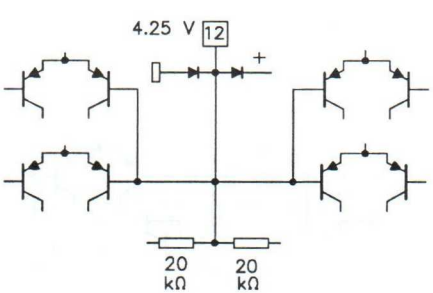


Pin 10: Automatic volume control capacitor

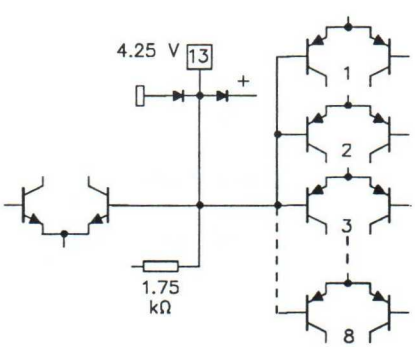


Pin 11: Reference voltage

$0.5 \times V_{CC}$

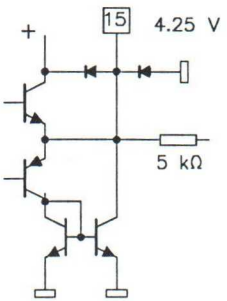


Pin 12: Line input, left
Pin 41: Line input, right

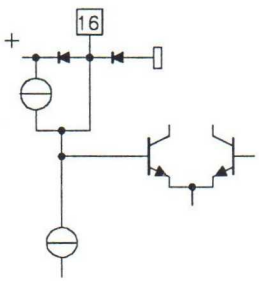


Pin 13: Input automatic volume control, left
Pin 40: Input automatic volume control, right

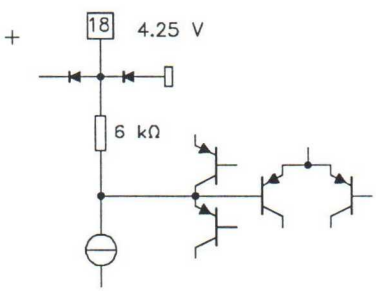
Fig.17 Internal circuits (continued from Fig.16).



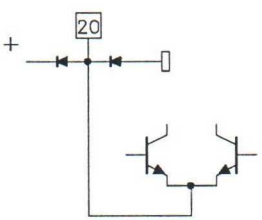
Pin 15: Line output, left
Pin 38: Line output, right



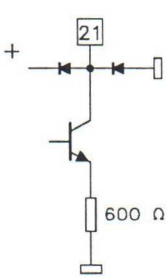
Pin 16: Timing capacitor wideband for DBX
Pin 17: Timing capacitor spectral for DBX



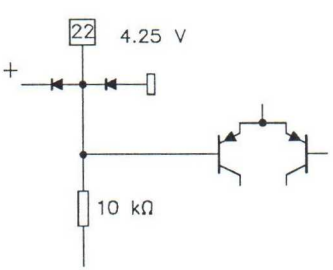
Pin 18: Capacitor wideband for DBX
Pin 19: Capacitor spectral for DBX



Pin 20: Variable emphasis out for DBX

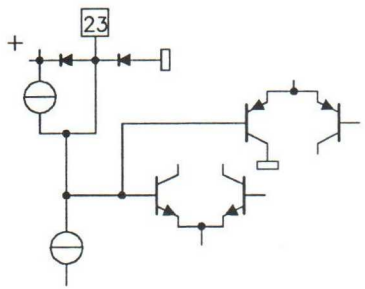


Pin 21: Variable emphasis in for DBX

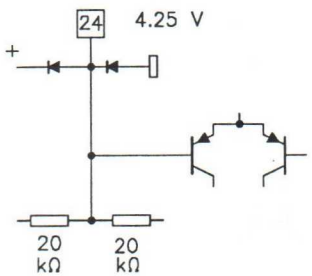


Pin 22: Capacitor noise reduction for DBX

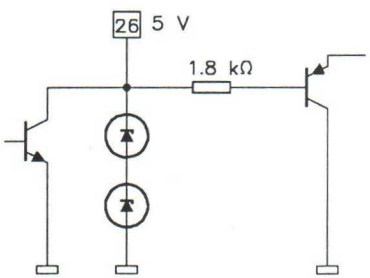
Fig.18 Internal circuits (continued from Fig.17).



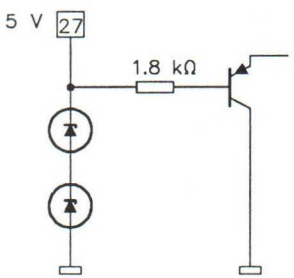
Pin 23: Capacitor mute for SAP



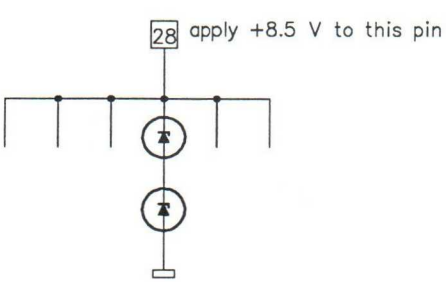
Pin 24: Capacitor DC decoupling for SAP



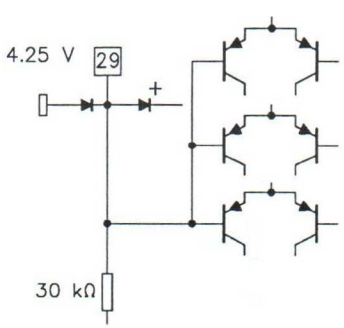
Pin 26: SDA (I²C–bus DATA input/output)



Pin 27: SCL (I²C–bus CLOCK)

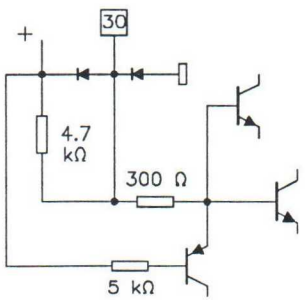


Pin 28: Supply voltage

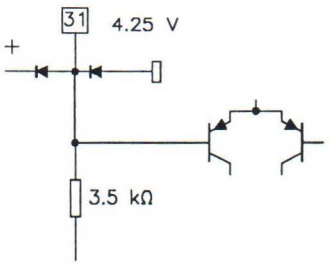


Pin 29: Input composite signal

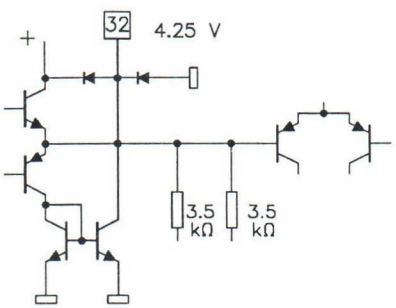
Fig.19 Internal circuits (continued from Fig.18).



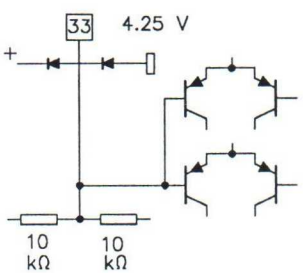
Pin 30: Smoothing capacitor for supply



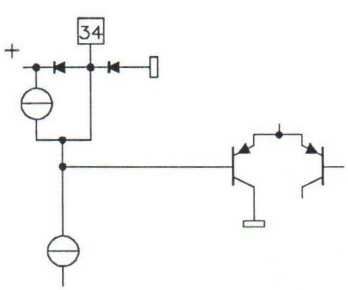
Pin 31: Capacitor for pilot detector



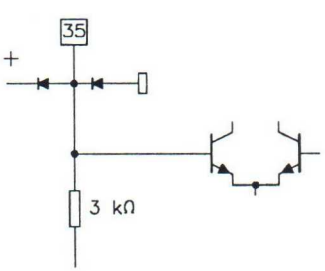
Pin 32: Capacitor for pilot detector



Pin 33: Capacitor for phase detector

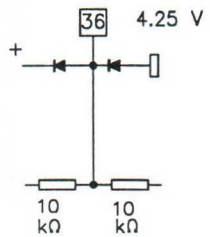


Pin 34: Capacitor for filter adjust

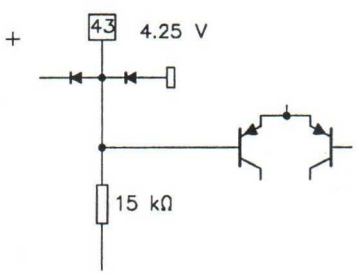


Pin 35: Ceramic resonator

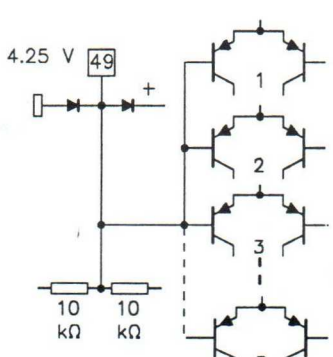
Fig.20 Internal circuits (continued from Fig.19).



Pin 36: Capacitor DC decoupling mono
Pin 37: Capacitor DC decoupling stereo/SAP



Pin 43: Capacitor 1 pseudo function
Pin 42: Capacitor 2 pseudo function



Pin 49: Capacitor subwoofer

Fig.21 Internal circuits (continued from Fig.20).

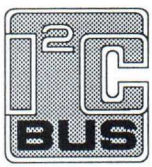
Universal HiFi audio processor for TV TDA9860

FEATURES

- Multi-source selector switches six AF inputs (three stereo sources or six mono sources)
- Each of the input signals can be switched to each of the outputs (crossbar switch)
- Outputs for loudspeaker channel, headphone channel and peri-TV connector (SCART)
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added externally
- Two general purpose logic output ports
- I^2C-bus control of all functions.

GENERAL DESCRIPTION

The TDA9860 provides control facilities for the main, the headphone and the SCART channel of a TV set. Due to extended switching possibilities, signals from 3 stereo sources can be handled.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 6)	7.2	8.0	8.8	V
I_P	supply current	–	25	–	mA
V_i	input signal levels for 0 dB gain (RMS value)	2	–	–	V
V_o	output signal levels for 0 dB gain (RMS value)	2	–	–	V
G_v	gain in main channel				
	volume control (1 dB steps, balance included)	–63	–	+15	dB
	bass control (1.5 dB steps)	–12	–	+15	dB
	treble control (3 dB steps)	–12	–	+12	dB
	gain in headphone channel				
	volume control (2 dB steps)	–70	–	0	dB
	gain for muting in all channels	–80	–	–	dB
THD	total harmonic distortion	–	0.1	–	%
S/N	signal-to-noise ratio	–	85	–	dB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9860	32	SDIL	plastic	SOT232

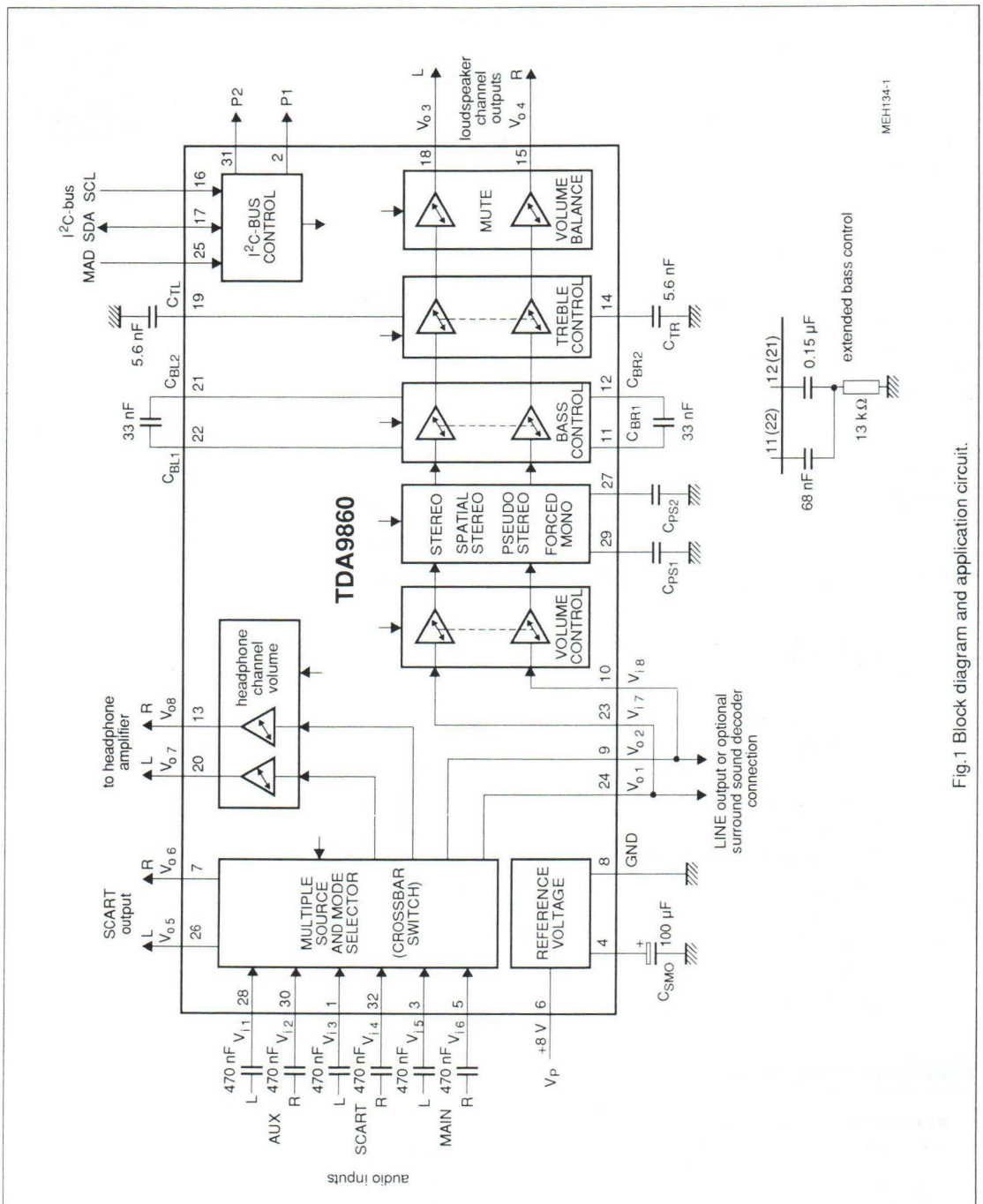


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,3}$	1	SCART input signal LEFT
P1	2	port 1 output
$V_{i\,5}$	3	MAIN input signal LEFT
C_{SMO}	4	smoothing capacitor of reference voltage
$V_{i\,6}$	5	MAIN input signal RIGHT
V_P	6	positive supply voltage
$V_{o\,6}$	7	SCART output signal RIGHT
GND	8	ground
$V_{o\,2}$	9	MAIN output signal RIGHT
$V_{i\,8}$	10	input signal RIGHT to loudspeaker channel
C_{BR1}	11	bass capacitor RIGHT 1
C_{BR2}	12	bass capacitor RIGHT 2
$V_{o\,8}$	13	headphone output signal RIGHT
C_{TR}	14	treble capacitor RIGHT
$V_{o\,4}$	15	loudspeaker channel output signal RIGHT
SCL	16	I^2C-bus clock line
SDA	17	I^2C-bus data line
$V_{o\,3}$	18	loudspeaker channel output signal LEFT
C_{TL}	19	treble capacitor LEFT
$V_{o\,7}$	20	headphone output signal LEFT
C_{BL2}	21	bass capacitor LEFT 2
C_{BL1}	22	bass capacitor LEFT 1
$V_{i\,7}$	23	input signal LEFT to loudspeaker channel
$V_{o\,1}$	24	MAIN output signal LEFT
MAD	25	module address select input
$V_{o\,5}$	26	SCART output signal LEFT
C_{PS2}	27	pseudo stereo capacitor 2
$V_{i\,1}$	28	AUX input signal LEFT
C_{PS1}	29	pseudo stereo capacitor 1
$V_{i\,2}$	30	AUX input signal RIGHT
P2	31	port 2 output
$V_{i\,4}$	32	SCART input signal RIGHT

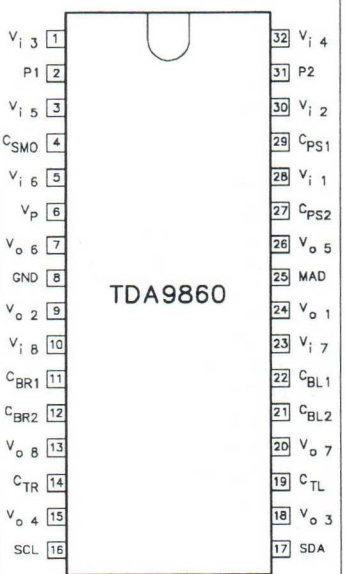


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9860 consists of the following functions:

- source select switching block
- loudspeaker channel with effect controls
- headphone channel
- two port outputs for general purpose
- I^2C-bus control

Source select switching block

The TDA9860 selects and switches the input signals from three stereo or six mono sources as there are MAIN, AUX and SCART (Fig.1) to one of the outputs SCART, loudspeaker and headphone (crossbar-switching Table 3). Due to the fact, that the main channel (LINE outputs) is looped outside the circuit (from pins 9 and 24 to pins 10 and 23), signals can be used as LINE output or to insert a 'surround sound decoder'.

Loudspeaker channel

Volume control is divided into the parts volume 1 and volume 2 / balance. The first part (55 dB) controls left and right channels simultaneously; the second part (23 dB) controls volume and balance of left and right channels independently. Treble control provides a control range from −12 to +12 dB and bass control from −12 to +15 dB. Extended bass control can be provided by an external T-network (Fig.1) from −15 to +19 dB (2 dB steps).

Effect controls

'Linear stereo', 'stereo with spatial effect (30% or 52% anti-phase crosstalk)' and 'forced mono with or without pseudo-stereo effect' are controlled by three bits. A muting of 85 dB is provided.

Headphone channel

The headphone channel is only equipped with volume / balance control. A muting of 85 dB is provided.

I^2C-bus control

All settings of control are stored in subaddress registers. Data transmission is simplified by auto-incrementing the subaddresses. The on-chip power on reset sets the mute bit to active, so all 3 stereo outputs are muted.
The muting can be switched off by writing a '0' (non-muted) into the mute control bits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 6)	0	10	V
V_n	voltage on all pins, ground excluded	0	V_P	V
I_O	output current			
	at pins 15, 18, 13, 20, 7 and 26	–	2.5	mA
	at pins 2 and 31	–	1.5	mA
P_{tot}	total power dissipation	–	850	mW
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±300	V
	electrostatic handling for all pins (note 2)	–	±2000	V

Notes to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	60 K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = +25 °C; treble and bass in linear positions; balance in mid position; spatial function, pseudo-stereo function and forced-mono function in off position and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 6)		7.2	8.0	8.8	V
I_P	supply current (pin 6)		–	25	–	mA
V_{ref}	internal reference voltage		–	$V_P/2$	–	V
V_4	voltage (pin 4)		–	$V_P - 0.1$	–	V
DC voltage on pins						
V_I	DC input voltage (pins 1, 3, 5, 10, 23, 28, 30 and 32)		–	$V_P/2$	–	V
V_O	DC output voltage (pins 7, 9, 13, 15, 18, 20, 24 and 26)		–	$V_P/2$	–	V
V_C	DC voltage on capacitors (pins 11, 12, 14, 19, 21, 22, 27 and 29)		–	$V_P/2$	–	V
Audio select switch. Line, SCART and headphone outputs (controlled via I^2C-bus, Table 3)						
V_i	maximum AF input signal on pins 1, 3, 5, 28, 30, 32 (RMS value)	THD ≤ 0.5% on output pins	2	–	–	V
R_i	input resistance (pins 1, 3, 5, 28, 30, 32)		20	30	40	kΩ
f	frequency response for all AF outputs	–0.5 dB	20	–	20000	Hz
V_o	maximum AF output signal on pins 7, 9, 24, 26 (RMS value)	THD ≤ 0.5%	2	–	–	V
R_L	allowed external load resistance					
	on output (pins 9 and 24)		10	–	–	kΩ
	on output (pins 7 and 26)		5	–	–	kΩ
G_v	gain for all signal arms		–	0	–	dB
α_{cr}	switch crosstalk on outputs between AF inputs at f = 10 kHz	unused inputs connected to ground	–	90	–	dB
LOUDSPEAKER CHANNEL (controlled via I^2C-bus, Table 3)						
Volume control 1 (LEFT and RIGHT simultaneously)		f = 1 kHz, 55 steps				
V_i	maximum input signal (RMS value; pins 10 and 23)	G_v = 0; THD ≤ 0.5% on output pins 15 and 18	2	–	–	V
R_i	input resistance (pins 10 and 23)		7.5	10	–	kΩ
G_v	nominal volume control		–40	–	+15	dB
	minimum volume control		–38	–	+14	dB
ΔG_v	step width	G_v = –32 to +15 dB	0.5	1.0	1.5	dB
		G_v = –40 to –33 dB	0.25	1.0	1.75	dB
	gain set error	G_v = –32 to +15 dB	–	–	1	dB
		G_v = –40 to –33 dB	–	–	2	dB
Volume 2 / balance control		f = 1 kHz, 24 steps				
G_v	nominal volume control		–24	–	0	dB
	minimum volume control		–23	–	–1	dB
	gain in mute position		–80	–85	–	dB
ΔG_v	step width		0.5	1.0	1.5	dB
	gain tracking error		–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bass control						
G_v	controllable bass	C_B = 33 nF				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
ΔG_v	step width		1	1.5	2	dB
G_v	controllable enhanced bass	Fig.1				
	maximum boost	f = 60 Hz	18	19	20	dB
	maximum attenuation	f = 60 Hz	14	15	16	dB
ΔG_v	step width		1	2	3	dB
Treble control						
G_v	controllable treble					
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_v	step width (resolution)		2.5	3	3.5	dB
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo		–	Fig.3	–	
Loudspeaker channel outputs (pins 15 and 18)						
V_o	maximum output signal (RMS value; pins 15 and 18)	THD ≤ 0.5%; R_L > 10 kΩ; C_L < 1.5 nF	2	–	–	V
$\Delta V_{15, 18}$	maximum DC offset voltage	between adjoining step and any step to mute				
	for volume control	G_v = 0 to +15 dB/mute	–	2	15	mV
		G_v = –64 to 0 dB/mute	–	0.5	10	mV
	for bass control	G_v = 0 to +15 dB/mute	–	2	15	mV
		G_v = –12 to 0 dB/mute	–	0.5	10	mV
	for treble control	G_v = –12 to +12 dB/mute	–	0.5	10	mV
R_o	output resistance (pins 15 and 18)		–	–	100	Ω
R_L	allowed output load resistor		10	–	–	kΩ
C_L	allowed output load capacitor		–	–	1.5	nF
$V_{N(W)}$	weighted noise voltage at output (quasi-peak level)	CCIR468-3				
	for +15 dB gain		–	102	–	μV
	for 0 dB gain		–	32	–	μV
	for –40 dB gain		–	27	–	μV
	for mute position	G_v = –80 dB	–	20	–	μV
B	AF bandwidth	–1 dB	–	20 to 20000	–	Hz
THD	total harmonic distortion	f = 20 to 12500 Hz				
	for V_i = 0.2 V (RMS value)	G_v = –30 to +15 dB	–	0.1	0.3	%
	for V_i = 1 V (RMS value)	G_v = –30 to 0 dB	–	0.1	0.3	%
	for V_i = 2 V (RMS value)	G_v = –30 to –6 dB	–	0.1	0.3	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{sp}	stereo channel separation	f = 10 kHz; G_v = 0 dB; opposite input grounded by 1 kΩ resistor	–	75	–	dB
α_{bus}	crosstalk of I^2C-bus	G_v = 0 dB; note 1	–	100	–	dB
RR_{100}	ripple rejection with 100 Hz ripple on V_P	G_v = 0 dB; V_R < 200 mV RMS	–	55	–	dB
HEADPHONE CHANNEL (controlled via I^2C-bus, Table 3)						
Volume control headphone channel		f = 1 kHz, 36 steps				
G_v	nominal volume control		–70	–	0	dB
	minimum volume control		–67	–	–1	dB
	gain in mute position		–80	–85	–	dB
ΔG_v	step width (resolution)	G_v = –36 to 0 dB	1.5	2	2.5	dB
		G_v = –70 to –36 dB	1	2	3	dB
	gain set error	G_v = –36 to 0 dB	–	–	1	dB
		G_v = –70 to –36 dB	–	–	3	dB
$\Delta V_{13, 20}$	DC offset voltage	for adjoining step and step to mute G_v = –70 to 0 dB	–	0.5	10	mV
Headphone channel output (pins 13 and 20)						
V_o	maximum output signal (RMS value)	THD ≤ 0.5%; R_L > 10 kΩ; C_L < 1.5 nF	2	–	–	V
R_o	output resistance		–	–	100	Ω
R_L	allowed output load resistor		10	–	–	kΩ
C_L	allowed output load capacitor		–	–	1.5	nF
$V_{N(W)}$	weighted noise voltage at output (quasi-peak level) CCIR468-3					
	for 0 dB gain		–	20	–	μV
	for –16 dB gain		–	15	–	μV
	for mute position	G_v = –80 dB	–	12	–	μV
B	AF bandwidth	–1 dB	–	20 to 20000	–	Hz
THD	total harmonic distortion	f = 20 to 12500 Hz				
	for V_i = 1 V (RMS value)	G_v = –40 to 0 dB	–	0.08	0.25	%
α_{sp}	stereo channel separation	f = 10 kHz; G_v = 0 dB; opposite input grounded by 1 kΩ resistor	–	75	–	dB
α_{bus}	crosstalk of I^2C-bus	G_v = 0 dB; note 1	–	100	–	dB
RR_{100}	ripple rejection with 100 Hz ripple on V_P	G_v = 0 dB; V_R < 200 mV RMS	–	55	–	dB
SCART output (pins 7 and 26)						
V_o	maximum output signal (RMS value)	THD ≤ 0.5%; R_L > 5 kΩ	2	–	–	V
R_L	admissible output load resistor		5	–	–	kΩ
Power on reset						
V_{PONR}	increasing supply voltage					
	start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{PONR}	decreasing supply voltage start of reset		4.4	5.2	6.0	V
I²C-bus, SCL and SDA (pins 16 and 17, observe I²C-bus specification)						
$V_{16,17}$	input voltage HIGH-level		3	–	V_P	V
	input voltage LOW-level		0	–	1.5	V
$I_{16,17}$	input current		–	–	±10	μA
V_{ACK}	output voltage at acknowledge (pin 17)	I_{17} = –3 mA	–	–	0.4	V
Module address (pin 25)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	V_P	V
Port outputs P1 and P2 (open-collector outputs pins 2 and 31)						
V_{OL}	LOW level output voltage	$I_{2,31}$ = 1 mA (sink)	–	–	0.3	V
$I_{2,31}$	port output current	sink current	–	–	1	mA

Note to the characteristics

1. α_{bus} = 20 log V_{bus} / V_o (V_{bus} = spurious bus signal voltage on AF output pin).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = 1000 0000 (V_{25} = LOW) or 1000 0010 (V_{25} = HIGH)
A = acknowledge, generated by the slave or by the master
SUBADDRESS = subaddress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

This circuit only operates as a slave transmitter.
If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission.

FUNCTION	SUBADDRESS	HEX	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
loudspeaker channel										
volume control both	0000 0000	00	0	0	V05	V04	V03	V02	V01	V00
volume/balance left	0000 0001	01	0	0	0	VL4	VL3	VL2	VL1	VL0
volume/balance right	0000 0010	02	0	0	0	VR4	VR3	VR2	VR1	VR0
bass control byte	0000 0011	03	0	0	0	BA4	BA3	BA2	BA1	BA0
treble control byte	0000 0100	04	0	0	0	0	TR3	TR2	TR1	TR0
headphone channel										
volume control left	0000 0101	05	0	0	VHL5	VHL4	VHL3	VHL2	VHL1	VHL0
volume control right	0000 0110	06	0	0	VHR5	VHR4	VHR3	VHR2	VHR1	VHR0
switching control byte										
headphone output	0000 0111	07	0	MU0	0	0	I03	I02	I01	I00
SCART output	0000 1000	08	0	MU1	P1	P2	I13	I12	I11	I10
loudspeaker output	0000 1001	09	EF2	MU2	EF1	ST	I23	I22	I21	I20

Table 2 Bits of data bytes.

FUNCTION OF THE BITS IN TABLE 1	DESCRIPTION
V00 to V05	volume control common for loudspeaker channel
VL0 to VL4	volume control LEFT for loudspeaker channel
VR0 to VR4	volume control RIGHT for loudspeaker channel
BA0 to BA4	bass control for LEFT and RIGHT loudspeaker channel
TR0 to TR3	treble control for LEFT and RIGHT loudspeaker channel
VHL0 to VHL5	volume control LEFT for headphone channel
VHR0 to VHR5	volume control RIGHT for headphone channel
I00 to I03	input selection for headphone channel
I10 to I13	input selection for SCART channel
I20 to I23	input selection for loudspeaker channel
MU0, MU1 and MU2	mute control bits: 0 = non-muted; 1 = muted
EF1, EF2 and ST	special mode control bits
P1 and P2	control bits for ports P1 (pin 2) and P2 (pin 31); output levels: 0 = LOW; 1 = HIGH

Table 3 Output and input selection by subaddress bytes 07, 08 and 09.

OUTPUT AND INPUT CONTROL BYTES, MUTE INCLUDED (EFFECTS TABLE 4)												
SELECT OUTPUT PINS		**INPUT GROUP**	**INPUT SIGNAL**	**ADDR**	**DATA BYTE TO SUBADDRESS**							
Loudspeaker channels												
output pin 18	output pin 15			09	EF2	MU2	EF1	ST	I23	I22	I21	I20
SCART channels												
output pin 26	output pin 7			08	0	MU1	P1	P2	I13	I12	I11	I10
headphone channels												
output pin 20	output pin 13			07	0	MU0	0	0	I03	I02	I01	I00
SELECT INPUT SIGNAL PINS				**HEX**	**BITS OF DATA BYTE**							
28	28	AUX LEFT	V_{i1}	XB	X	0	X	X	1	0	1	1
30	30	AUX RIGHT	V_{i2}	X9	X	0	X	X	1	0	0	1
28	30	AUX STEREO	V_{i1} and V_{i2}	X7	X	0	X	X	0	1	1	1
1	1	SCART LEFT	V_{i3}	XA	X	0	X	X	1	0	1	0
32	32	SCART RIGHT	V_{i4}	X5	X	0	X	X	0	1	0	1
1	32	SCART STEREO	V_{i3} and V_{i4}	X6	X	0	X	X	0	1	1	0
3	3	MAIN LEFT	V_{i5}	XC	X	0	X	X	1	1	0	0
5	5	MAIN RIGHT	V_{i6}	XD	X	0	X	X	1	1	0	1
3	5	MAIN STEREO	V_{i5} and V_{i6}	X8	X	0	X	X	1	0	0	0

X = don't care

Table 4 Effect controls.

SETTING SPECIAL MODES	HEX	DATA BYTE TO SUBADDRESS 09							
		EF2	MU2	EF1	ST	I23	I22	I21	I20
stereo with spatial (52%)	BX	1	0	1	1	X	X	X	X
stereo with spatial (30%)	3X	0	0	1	1	X	X	X	X
stereo without spatial	1X	0	0	0	1	X	X	X	X
forced mono with pseudo stereo	2X	0	0	1	0	X	X	X	X
forced mono without pseudo stereo	0X	0	0	0	0	X	X	X	X

Table 5 Volume 2 / balance control LEFT.

G_v	DATA					
(dB)	HEX	VL4	VL3	VL2	VL1	VL0
0	1F	1	1	1	1	1
–1	1E	1	1	1	1	0
–2	1D	1	1	1	0	1
–3	1C	1	1	1	0	0
–4	1B	1	1	0	1	1
–5	1A	1	1	0	1	0
–6	19	1	1	0	0	1
–7	18	1	1	0	0	0
–8	17	1	0	1	1	1
–9	16	1	0	1	1	0
–10	15	1	0	1	0	1
–11	14	1	0	1	0	0
–12	13	1	0	0	1	1
–13	12	1	0	0	1	0
–14	11	1	0	0	0	1
–15	10	1	0	0	0	0
–16	0F	0	1	1	1	1
–17	0E	0	1	1	1	0
–18	0D	0	1	1	0	1
–19	0C	0	1	1	0	0
–20	0B	0	1	0	1	1
–21	0A	0	1	0	1	0
–22	09	0	1	0	0	1
–23	08	0	1	0	0	0
mute left	07	0	0	1	1	1

Table 6 Volume 2 / balance control RIGHT.

G_v	DATA					
(dB)	HEX	VR4	VR3	VR2	VR1	VR0
0	1F	1	1	1	1	1
–1	1E	1	1	1	1	0
–2	1D	1	1	1	0	1
–3	1C	1	1	1	0	0
–4	1B	1	1	0	1	1
–5	1A	1	1	0	1	0
–6	19	1	1	0	0	1
–7	18	1	1	0	0	0
–8	17	1	0	1	1	1
–9	16	1	0	1	1	0
–10	15	1	0	1	0	1
–11	14	1	0	1	0	0
–12	13	1	0	0	1	1
–13	12	1	0	0	1	0
–14	11	1	0	0	0	1
–15	10	1	0	0	0	0
–16	0F	0	1	1	1	1
–17	0E	0	1	1	1	0
–18	0D	0	1	1	0	1
–19	0C	0	1	1	0	0
–20	0B	0	1	0	1	1
–21	0A	0	1	0	1	0
–22	09	0	1	0	0	1
–23	08	0	1	0	0	0
mute right	07	0	0	1	1	1

Table 7 Volume 1 to control both channels.

G_v	DATA						
(dB)	HEX	V05	V04	V03	V02	V01	V00
+15	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+13	3D	1	1	1	1	0	1
+12	3C	1	1	1	1	0	0
+11	3B	1	1	1	0	1	1
+10	3A	1	1	1	0	1	0
+9	39	1	1	1	0	0	1
+8	38	1	1	1	0	0	0
+7	37	1	1	0	1	1	1
+6	36	1	1	0	1	1	0
+5	35	1	1	0	1	0	1
+4	34	1	1	0	1	0	0
+3	33	1	1	0	0	1	1
+2	32	1	1	0	0	1	0
+1	31	1	1	0	0	0	1
0	30	1	1	0	0	0	0
−1	2F	1	0	1	1	1	1
−2	2E	1	0	1	1	1	0
−3	2D	1	0	1	1	0	1
−4	2C	1	0	1	1	0	0
−5	2B	1	0	1	0	1	1
−6	2A	1	0	1	0	1	0
−7	29	1	0	1	0	0	1
−8	28	1	0	1	0	0	0
−9	27	1	0	0	1	1	1
−10	26	1	0	0	1	1	0
−11	25	1	0	0	1	0	1
−12	24	1	0	0	1	0	0
−13	23	1	0	0	0	1	1
−14	22	1	0	0	0	1	0
−15	21	1	0	0	0	0	1
−16	20	1	0	0	0	0	0
−17	1F	0	1	1	1	1	1
−18	1E	0	1	1	1	1	0
−19	1D	0	1	1	1	0	1
−20	1C	0	1	1	1	0	0
−21	1B	0	1	1	0	1	1
−22	1A	0	1	1	0	1	0
−23	19	0	1	1	0	0	1
−24	18	0	1	1	0	0	0
−25	17	0	1	0	1	1	1
−26	16	0	1	0	1	1	0
−27	15	0	1	0	1	0	1
−28	14	0	1	0	1	0	0
−29	13	0	1	0	0	1	1
−30	12	0	1	0	0	1	0
−31	11	0	1	0	0	0	1
−32	10	0	1	0	0	0	0
−33	0F	0	0	1	1	1	1
−34	0E	0	0	1	1	1	0
−35	0D	0	0	1	1	0	1
−36	0C	0	0	1	1	0	0
−37	0B	0	0	1	0	1	1
−38	0A	0	0	1	0	1	0
−39	09	0	0	1	0	0	1
−40	08	0	0	1	0	0	0

Table 8 Bass control LEFT and RIGHT.

G_v	DATA					
(dB)	HEX	BA4	BA3	BA2	BA1	BA0
+15	19	1	1	0	0	1
+13.5	18	1	1	0	0	0
+12	17	1	0	1	1	1
+10.5	16	1	0	1	1	0
+9	15	1	0	1	0	1
+7.5	14	1	0	1	0	0
+6	13	1	0	0	1	1
+4.5	12	1	0	0	1	0
+3	11	1	0	0	0	1
+1.5	10	1	0	0	0	0
0	0F	0	1	1	1	1
0	0E	0	1	1	1	0
−1.5	0D	0	1	1	0	1
−3	0C	0	1	1	0	0
−4.5	0B	0	1	0	1	1
−6	0A	0	1	0	1	0
−7.5	09	0	1	0	0	1
−9	08	0	1	0	0	0
−10.5	07	0	0	1	1	1
−12	06	0	0	1	1	0

Table 9 Treble control LEFT and RIGHT.

G_v	DATA					
(dB)	HEX	0	TR3	TR2	TR1	TR0
+12	0A	0	1	0	1	0
+9	09	0	1	0	0	1
+6	08	0	1	0	0	0
+3	07	0	0	1	1	1
0	06	0	0	1	1	0
−3	05	0	0	1	0	1
−6	04	0	0	1	0	0
−9	03	0	0	0	1	1
−12	02	0	0	0	1	0

Table 10 Volume control of headphone LEFT.

G_v	DATA						
(dB)	HEX	VHL5	VHL4	VHL3	VHL2	VHL1	VHL0
0	3F	1	1	1	1	1	1
−2	3E	1	1	1	1	1	0
−4	3D	1	1	1	1	0	1
−6	3C	1	1	1	1	0	0
−8	3B	1	1	1	0	1	1
−10	3A	1	1	1	0	1	0
−12	39	1	1	1	0	0	1
−14	38	1	1	1	0	0	0
−16	37	1	1	0	1	1	1
−18	36	1	1	0	1	1	0
−20	35	1	1	0	1	0	1
−22	34	1	1	0	1	0	0
−24	33	1	1	0	0	1	1
−26	32	1	1	0	0	1	0
−28	31	1	1	0	0	0	1
−30	30	1	1	0	0	0	0
−32	2F	1	0	1	1	1	1
−34	2E	1	0	1	1	1	0
−36	2D	1	0	1	1	0	1
−38	2C	1	0	1	1	0	0
−40	2B	1	0	1	0	1	1
−42	2A	1	0	1	0	1	0
−44	29	1	0	1	0	0	1
−46	28	1	0	1	0	0	0
−48	27	1	0	0	1	1	1
−50	26	1	0	0	1	1	0
−52	25	1	0	0	1	0	1
−54	24	1	0	0	1	0	0
−56	23	1	0	0	0	1	1
−58	22	1	0	0	0	1	0
−60	21	1	0	0	0	0	1
−62	20	1	0	0	0	0	0
−64	1F	0	1	1	1	1	1
−66	1E	0	1	1	1	1	0
−68	1D	0	1	1	1	0	1
−70	1C	0	1	1	1	0	0
mute left	1B	0	1	1	0	1	1

Table 11 Volume control of headphone RIGHT.

G_v	DATA						
(dB)	HEX	VHR5	VHR4	VHR3	VHR2	VHR1	VHR0
0	3F	1	1	1	1	1	1
−2	3E	1	1	1	1	1	0
−4	3D	1	1	1	1	0	1
−6	3C	1	1	1	1	0	0
−8	3B	1	1	1	0	1	1
−10	3A	1	1	1	0	1	0
−12	39	1	1	1	0	0	1
−14	38	1	1	1	0	0	0
−16	37	1	1	0	1	1	1
−18	36	1	1	0	1	1	0
−20	35	1	1	0	1	0	1
−22	34	1	1	0	1	0	0
−24	33	1	1	0	0	1	1
−26	32	1	1	0	0	1	0
−28	31	1	1	0	0	0	1
−30	30	1	1	0	0	0	0
−32	2F	1	0	1	1	1	1
−34	2E	1	0	1	1	1	0
−36	2D	1	0	1	1	0	1
−38	2C	1	0	1	1	0	0
−40	2B	1	0	1	0	1	1
−42	2A	1	0	1	0	1	0
−44	29	1	0	1	0	0	1
−46	28	1	0	1	0	0	0
−48	27	1	0	0	1	1	1
−50	26	1	0	0	1	1	0
−52	25	1	0	0	1	0	1
−54	24	1	0	0	1	0	0
−56	23	1	0	0	0	1	1
−58	22	1	0	0	0	1	0
−60	21	1	0	0	0	0	1
−62	20	1	0	0	0	0	0
−64	1F	0	1	1	1	1	1
−66	1E	0	1	1	1	1	0
−68	1D	0	1	1	1	0	1
−70	1C	0	1	1	1	0	0
mute right	1B	0	1	1	0	1	1

CURVE	CAPACITANCE AT PIN 29 (nF)	CAPACITANCE AT PIN 27 (nF)	EFFECT
1	15	15	normal
2	47	5.6	intensified
3	68	5.6	more intensified

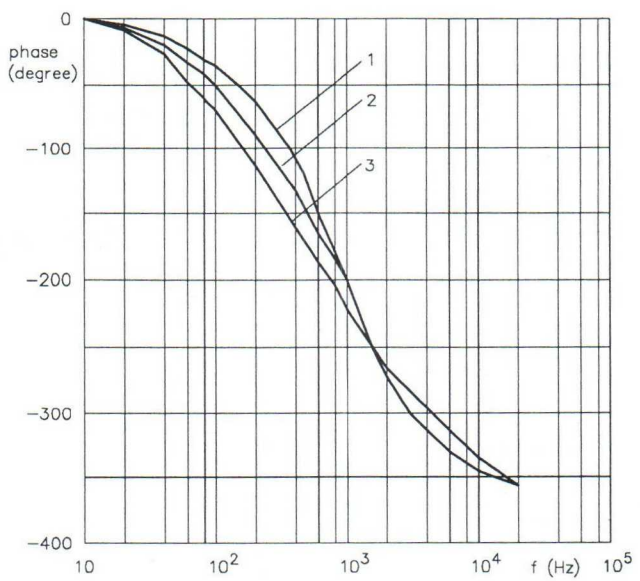


Fig.3 Pseudo (phase) as a function of frequency.

8-bit high-speed analog-to-digital converter TDF8704

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- Extended temperature range (–40 to +85 °C)
- High signal-to-noise ratio over a large analog input frequency range (7.4 effective bits at 4.43 MHz full-scale input and at f_{clk} = 50 MHz)
- Binary 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Stable internal reference voltage regulator included
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion for extended temperature applications
- Automotive
- RF, satellite and GPS (Global Positioning System)
- Medical
- General industrial
- Digital video (VCR, TV and satellite).

GENERAL DESCRIPTION

The TDF8704T is an 8-bit high-speed analog-to-digital converter (ADC) for general industrial applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	46	mA
I_{CCD}	digital supply current		–	23	35	mA
I_{CCO}	output stages supply current		–	16	21	mA
ILE	DC integral linear error		–	±0.4	±1	LSB
DLE	DC differential linearity error		–	±0.2	±0.5	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
$f_{clk(max)}$	maximum clock frequency		50	–	–	MHz
P_{tot}	total power dissipation		–	380	535	mW

Note

1. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 50 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDF8704T/2	24	SO24L	plastic	SOT137-1	20 MHz
TDF8704T/4	24	SO24L	plastic	SOT137-1	40 MHz
TDF8704T/5	24	SO24L	plastic	SOT137-1	50 MHz

BLOCK DIAGRAM

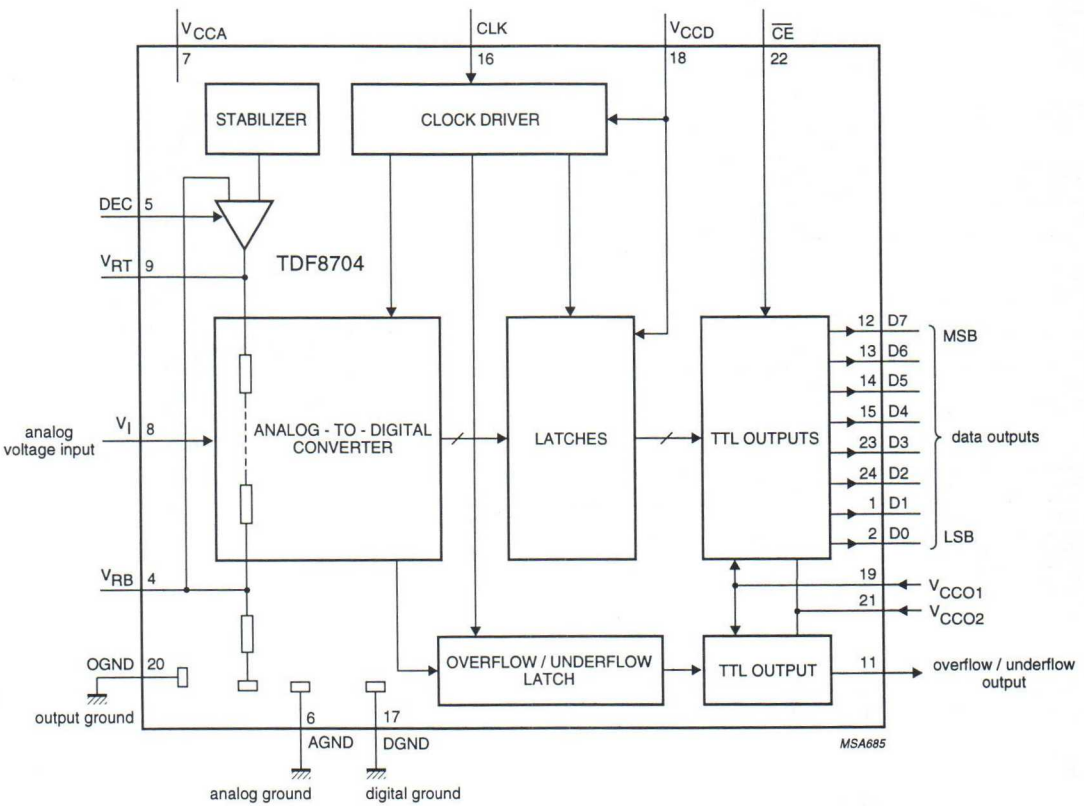


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage BOTTOM (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
AGND	6	analog ground
V_{CCA}	7	analog supply voltage (+5 V)
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	digital supply voltage (+5 V)
V_{CCO1}	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

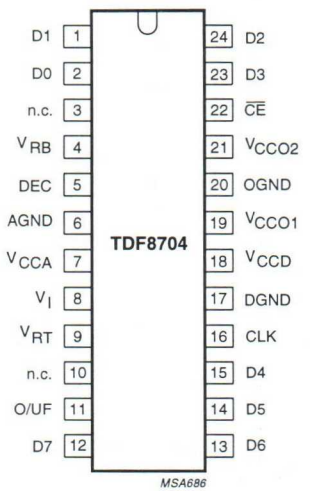


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{CCO}	output stages supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
T_j	junction temperature		–	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7$ to $V_6 = 4.75$ to 5.25 V; $V_{CCD} = V_{18}$ to $V_{17} = 4.75$ to 5.25 V; $V_{CCO} = V_{19}$ and V_{21} to $V_{20} = 4.75$ to 5.25 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCO} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCA} to $V_{CCD} = -0.25$ to +0.25 V; $T_{amb} = -40$ to +85 °C; typical readings taken at $V_{CCA} = V_{CCD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	46	mA
I_{CCD}	digital supply current		–	23	35	mA
I_{CCO}	output stages supply current	all outputs LOW	–	16	21	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{clk} = 2.7$ V	–	–	100	µA
		$V_{clk} = V_{CCD}$	–	–	300	µA
Z_I	input impedance	$f_{clk} = 50$ MHz	–	2	–	kΩ
C_I	input capacitance	$f_{clk} = 50$ MHz	–	4.5	–	pF
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGDN; SEE FIGS 3 AND 4 AND TABLE 1)						
$V_{I(B)}$	input voltage (BOTTOM)		1.21	1.25	1.29	V
$V_{I(0)}$	input voltage	output code = 0	1.42	1.48	1.51	V
$V_{os(B)}$	offset voltage (BOTTOM)	$V_{I(0)}$ to $V_{I(B)}$	210	225	240	V
$V_{I(T)}$	input voltage (TOP)		3.37	3.46	3.58	V
$V_{I(255)}$	input voltage	output code = 255	3.14	3.22	3.30	V
$V_{os(T)}$	offset voltage (TOP)	$V_{I(T)}$ to $V_{I(255)}$	225	240	255	V
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		1.69	1.74	1.79	V
I_L	load current on V_{RT} and V_{RB}		–300	–	+300	µA
I_{IL}	LOW level input current	$V_I = 1.25$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_I = 3.46$ V	40	150	400	µA
Z_I	input impedance	$f_i = 4.43$ MHz	–	10	–	kΩ
C_I	input capacitance	$f_i = 4.43$ MHz	–	14	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT $\overline{CE}$ (REFERENCED TO DGND) SEE TABLE 2						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	μA
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	200	–	Ω
Outputs						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA; T_{amb} = 0 to +85 °C	0	–	0.4	V
		I_O = 1 mA; T_{amb} = 0 to −40 °C	–	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics						
CLOCK INPUT CLK (NOTE 1; SEE FIG.15)						
$f_{clk(max)}$	maximum clock frequency					
	TDF8704T/2		20	–	–	MHz
	TDF8704T/4		40	–	–	MHz
	TDF8704T/5		50	–	–	MHz
t_{CPH}	clock pulse width HIGH		7	–	–	ns
t_{CPL}	clock pulse width LOW		7	–	–	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		–	±0.4	±1.0	LSB
DLE	DC differential linearity error		–	±0.2	±0.5	LSB
AILE	AC integral linearity error	note 2	–	–	±2.0	LSB
BANDWIDTH (f_{clk} = 40 MHz)						
B	−0.5 dB analog bandwidth (note 3)	full-scale sine wave	–	12	–	MHz
		75% full-scale sine wave	–	16	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.8; note 4	–	2.5	3.5	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.8; note 4	–	3.0	4.0	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HARMONICS (f_{clk} = 40 MHz)						
h_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	–64	–60	dB
	third harmonics		–	–58	–55	dB
THD	total harmonic distortion	f_i = 4.43 MHz	–	–56	–	dB
SIGNAL-TO-NOISE RATIO						
S/N	signal-to-noise ratio	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	46	48	–	dB
EFFECTIVE BITS; NOTE 5; SEE FIGS 9, 10 AND 11						
EB	effective bits TDF8704T/2	f_{clk} = 20 MHz				
		f_i = 1.25 MHz	–	7.8	–	bits
		f_i = 4.43 MHz	–	7.6	–	bits
	effective bits TDF8704T/4	f_{clk} = 40 MHz				
		f_i = 4.43 MHz	–	7.5	–	bits
		f_i = 7.5 MHz	–	7.3	–	bits
		f_i = 10 MHz	–	7.0	–	bits
	effective bits TDF8704T/5	f_{clk} = 50 MHz				
		f_i = 4.43 MHz	–	7.4	–	bits
		f_i = 7.5 MHz	–	7.2	–	bits
		f_i = 10 MHz	–	6.9	–	bits
TWO-TONE (NOTE 6)						
TTIR	two-tone intermodulation rejection	f_{clk} = 40 MHz	–	–56	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 128	–	10^{-11}	–	times/ samples
DIFFERENTIAL GAIN (NOTE 7)						
G_{diff}	differential gain	f_{clk} = 20 MHz; f_i = 4.43 MHz	–	0.6	–	%
DIFFERENTIAL PHASE (NOTE 7)						
φ_{diff}	differential phase	f_{clk} = 40 MHz; f_i = 4.43 MHz	–	0.8	–	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (note 8; see Figs 5 and 7; f_{clk} = 50 MHz)						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	12	15	ns
3-state output delay times (see Figs 6 and 7)						
t_{dZH}	enable HIGH		–	6	10	ns
t_{dZL}	enable LOW		–	12	16	ns
t_{dHZ}	disable HIGH		–	50	54	ns
t_{dLZ}	disable LOW		–	10	14	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must be less than 1 ns.
2. Full-scale sine wave (f_i = 4.43 MHz; f_{clk} = 50 MHz).
3. Determined by beat frequency method on a reconstructed sine wave signal for no missing codes and no glitches.
4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
5. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
6. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
7. Measurement taken using video analyser VM700A.
8. Output data acquisition: the output data is available after the maximum delay time of t_d.

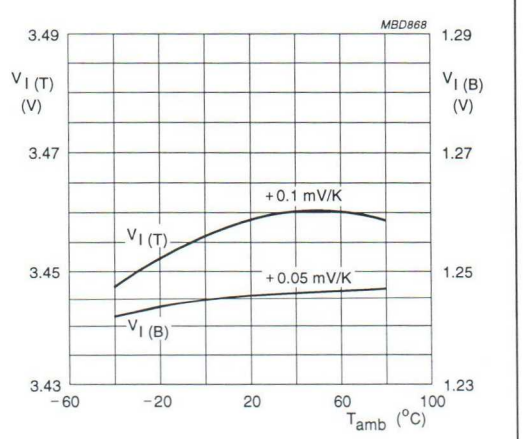


Fig.3 Influence of T_{amb} on $V_{I(T)}$ and $V_{I(B)}$ under 5 V supply.

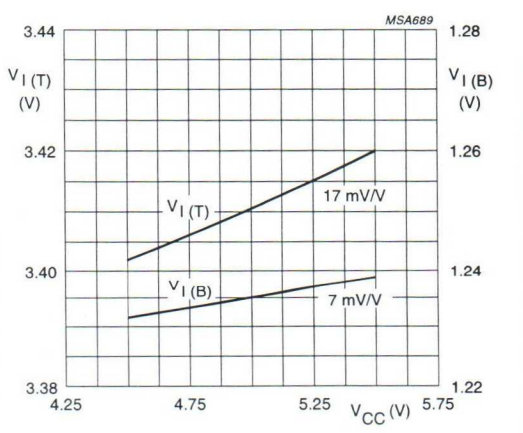


Fig.4 Influence of supply voltage on $V_{I(T)}$ and $V_{I(B)}$ under T_{amb} = 25 °C.

Table 1 Output coding and input voltage (typical values; referenced to AGND).

STEP	$V_{I(p-p)}$	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.48	1	1	0	0	0	0	0	0	0
0	1.48	0	0	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1
.	.	.	.		.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	3.46	0	1	1	1	1	1	1	1	1
Overflow	>3.46	1	1	1	1	1	1	1	1	1

Table 2 Mode selection.

$\overline{CE}$	D7 TO D0	O/UF
1	high impedance	high impedance
0	active; binary	active

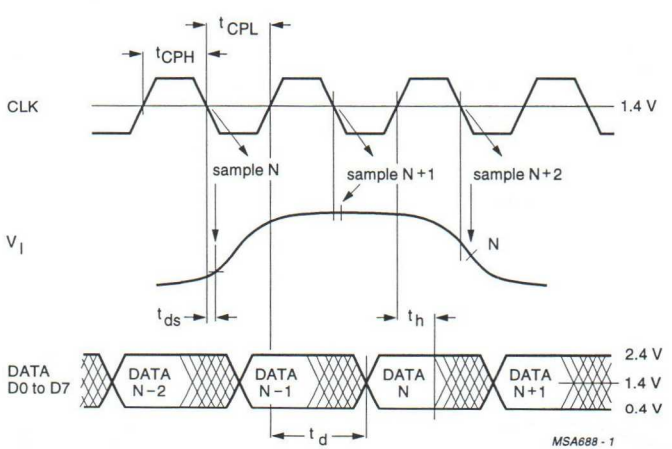
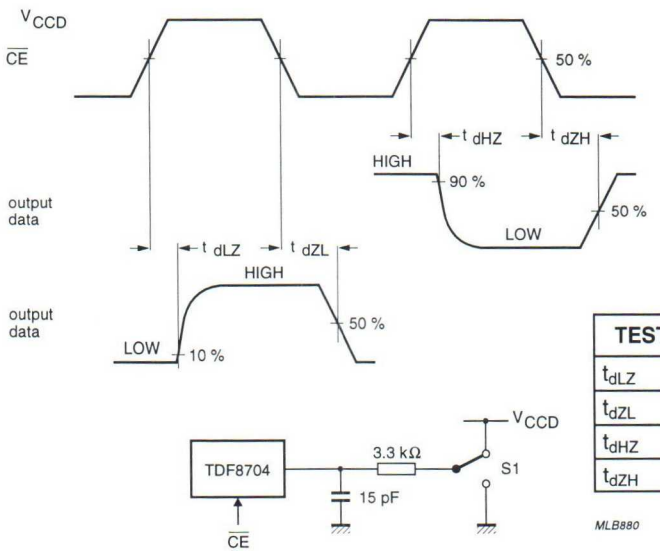


Fig.5 Timing diagram for data output.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.6 Timing diagram and test conditions of 3-state output delay time.

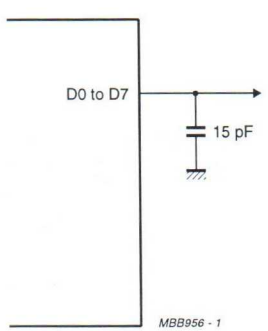


Fig.7 Load circuit for timing measurement.

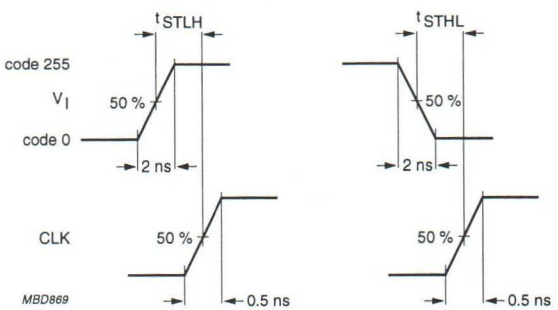
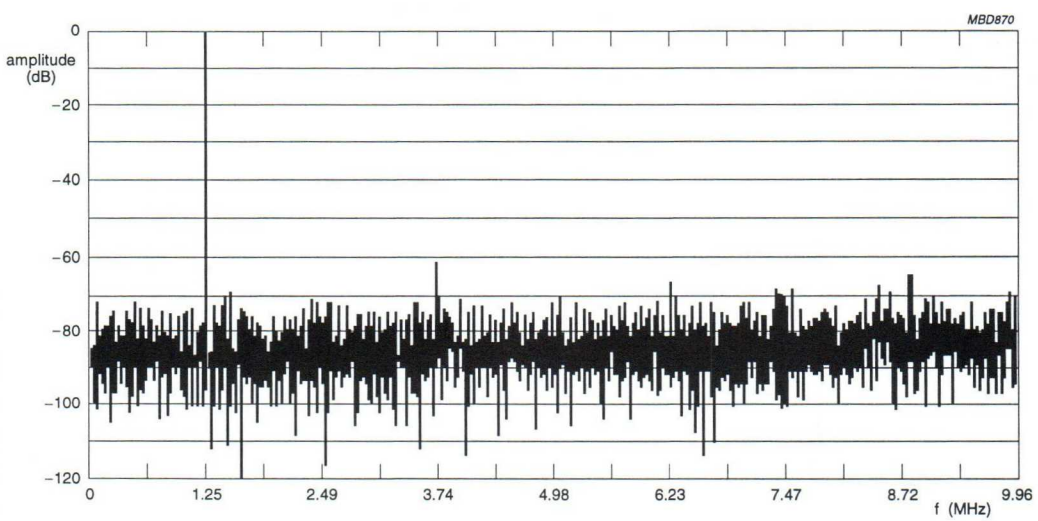
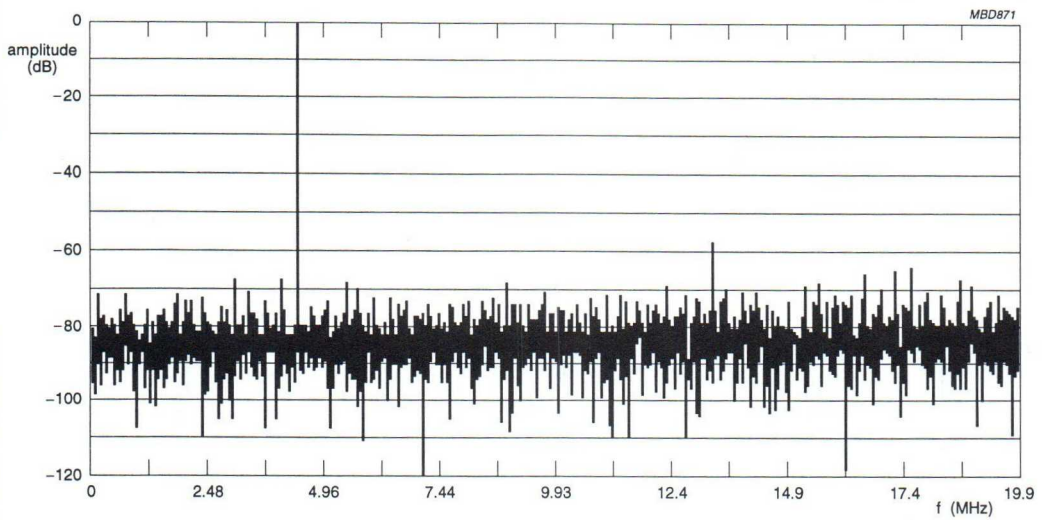


Fig.8 Analog input settling-time diagram.



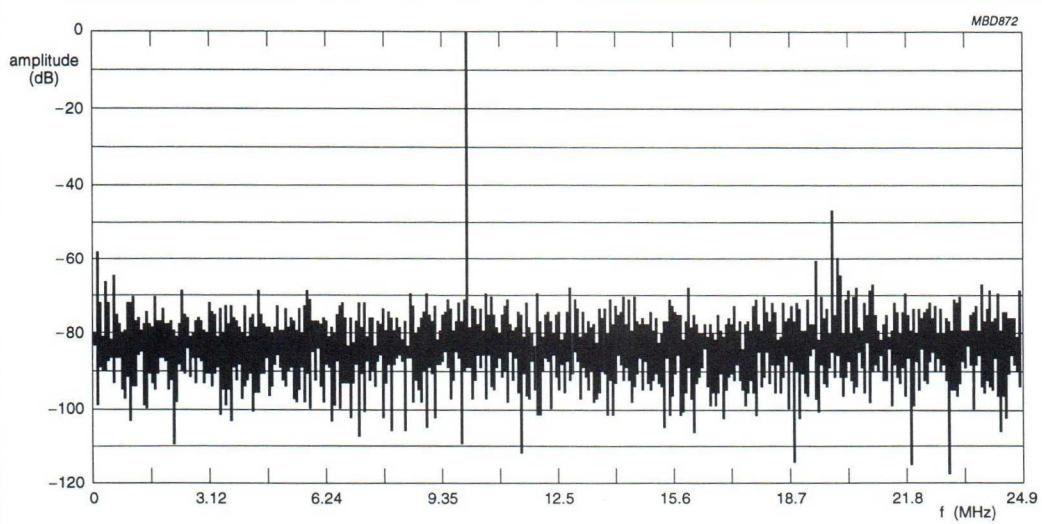
Effective bits: 7.89; THD = −61.05 dB.
Harmonic levels (dB): 2nd = −84.07; 3rd = −62.50; 4th = −92.01; 5th = −66.56; 6th = −101.15.

Fig.9 Fast Fourier Transform (f_{clk} = 20 MHz; f_i = 1.25 MHz).



Effective bits: 7.61; THD = −57.11 dB.
Harmonic levels (dB): 2nd = −68.53; 3rd = −58.36; 4th = −74.89; 5th = −65.37; 6th = −76.08.

Fig.10 Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 4.43 MHz).



Effective bits: 6.91; THD = −46.13 dB.
Harmonic levels (dB): 2nd = −59.66; 3rd = −46.67; 4th = −70.80; 5th = −57.96; 6th = −72.16.

Fig.11 Fast Fourier Transform (f_{clk} = 50 MHz; f_i = 10 MHz).

INTERNAL PIN CONFIGURATIONS

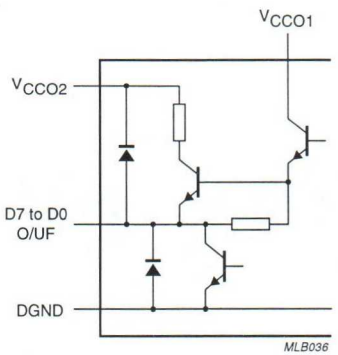


Fig.12 TTL data and overflow/underflow outputs.

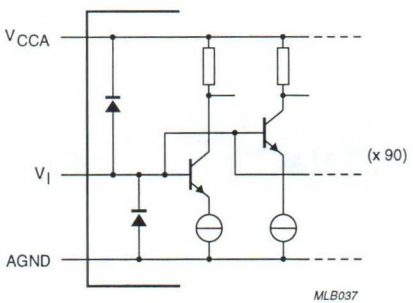


Fig.13 Analog inputs.

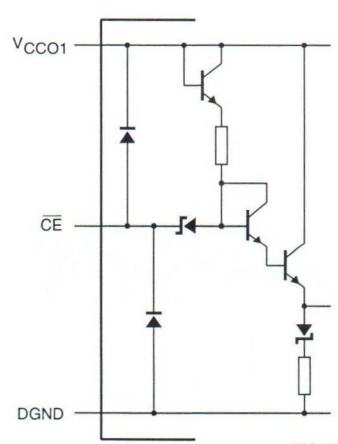


Fig.14 CE (3-state) input.

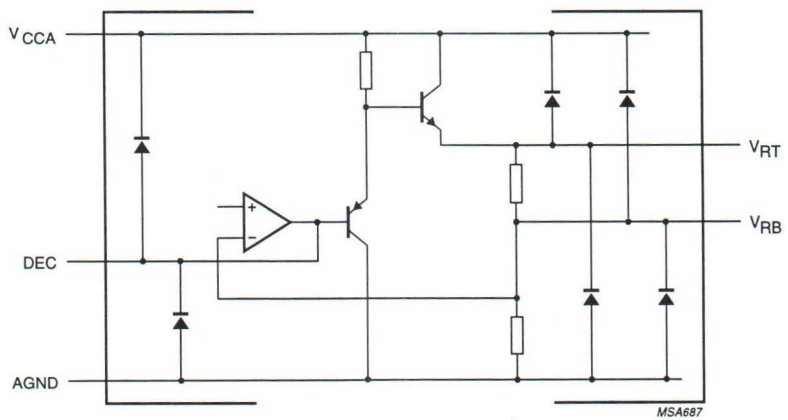


Fig.15 V_{RB}, V_{RT} and DEC.

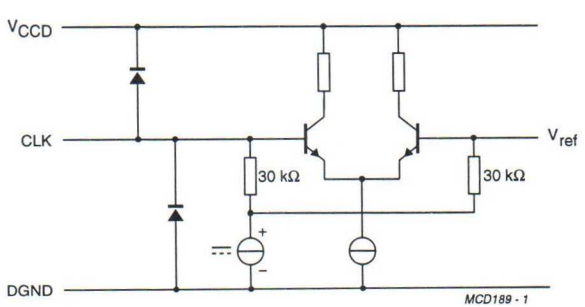
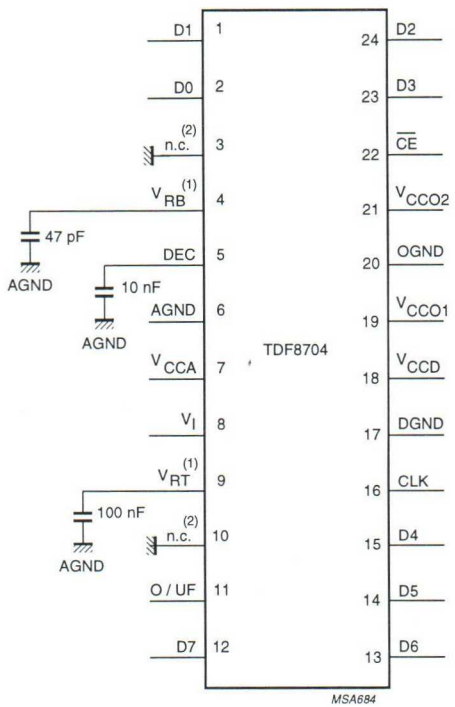


Fig.16 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

(1) V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.

(2) Pins 3 and 10 should be connected to DGND in order to prevent noise influence.

Fig.17 Application diagram.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to	100 kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +	125 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

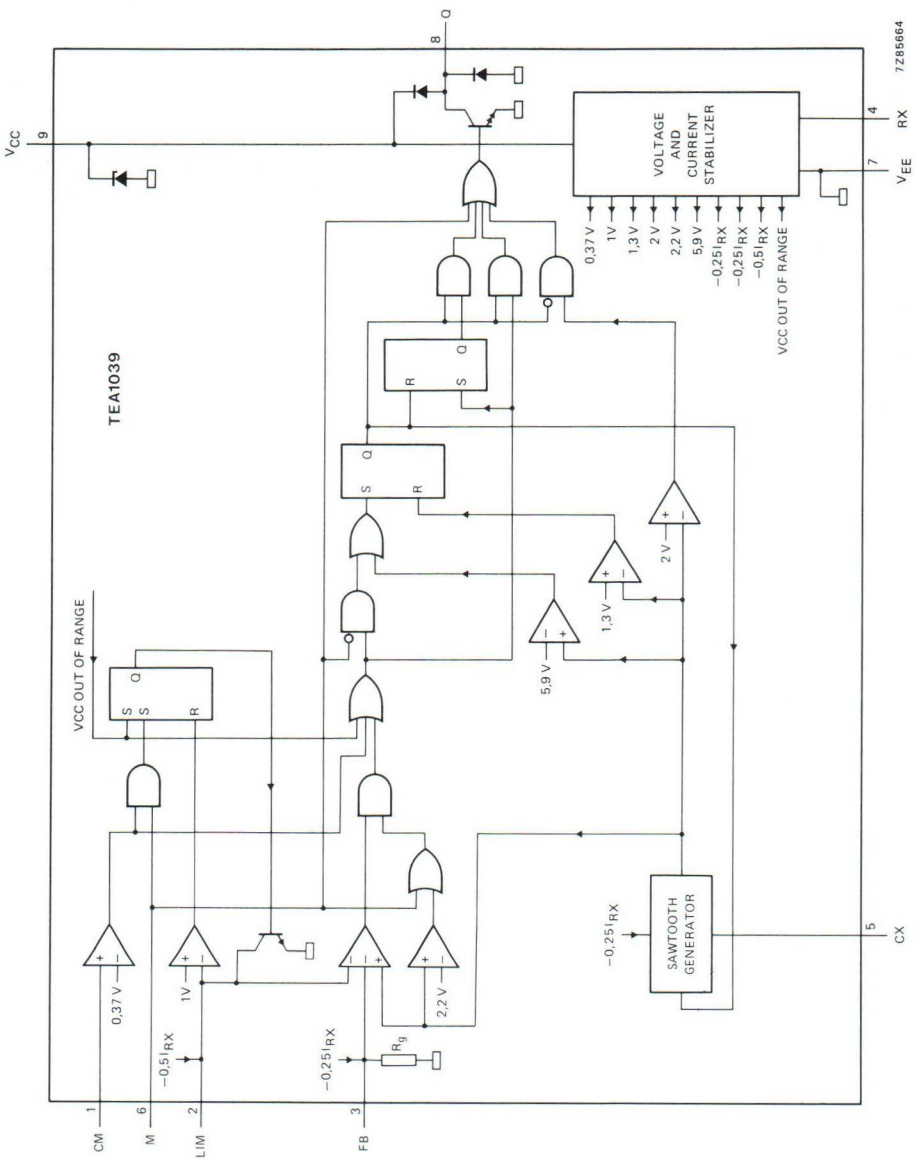


Fig. 1 Block diagram.

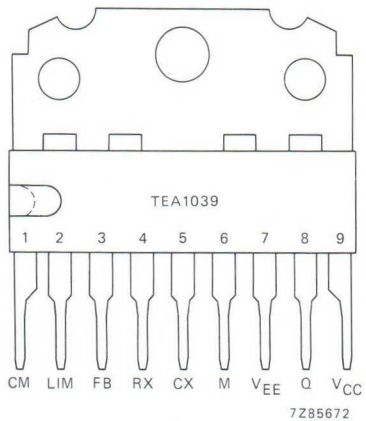


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20 V
Supply current range, current source	I_{CC}	−30 to +30 mA
Input voltage range, all inputs	V_I	−0,3 to +6 V
Input current range, all inputs	I_I	−5 to +5 mA
Output voltage range	V_{8-7}	−0,3 to +20 V
Output current range		
output transistor ON	I_8	0 to 1 A
output transistor OFF	I_8	−100 to + 50 mA
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125 °C
Power dissipation (see Fig. 3)	P_{tot}	max. 2 W

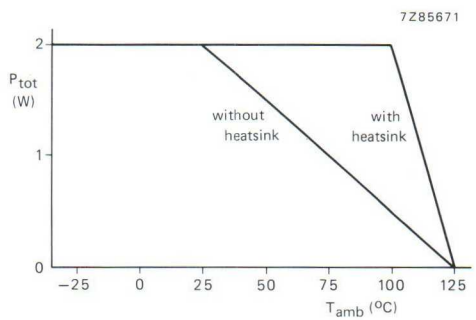


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

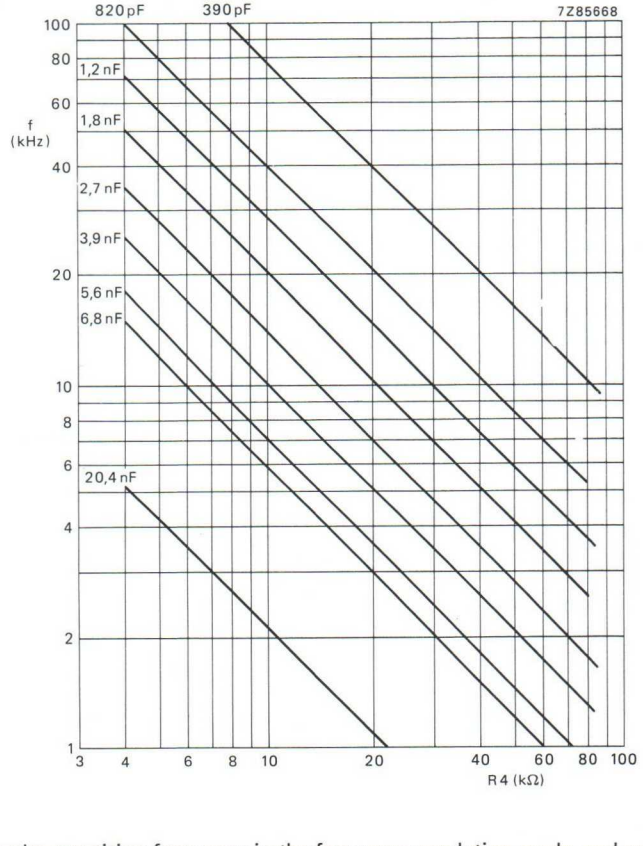


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

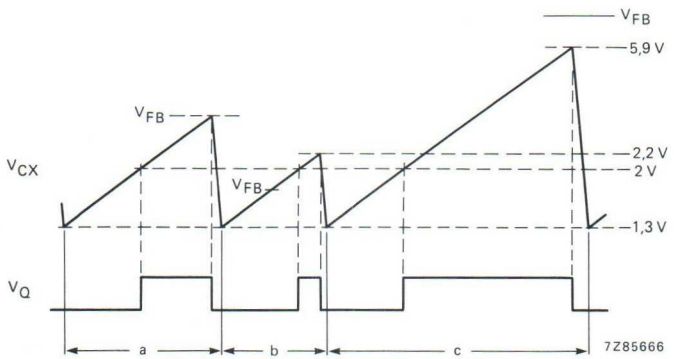


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

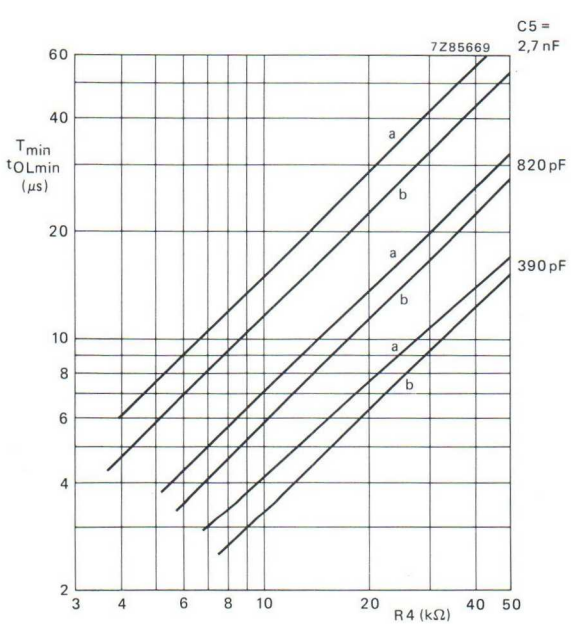


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

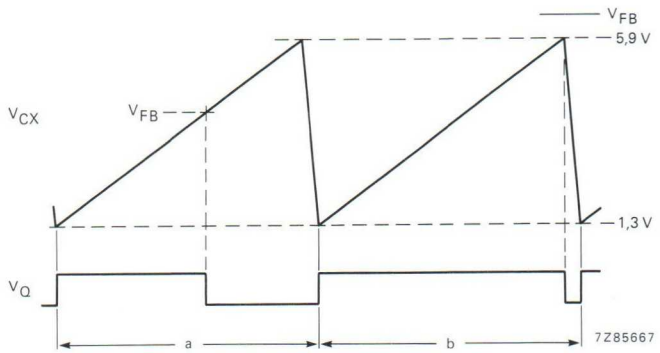


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

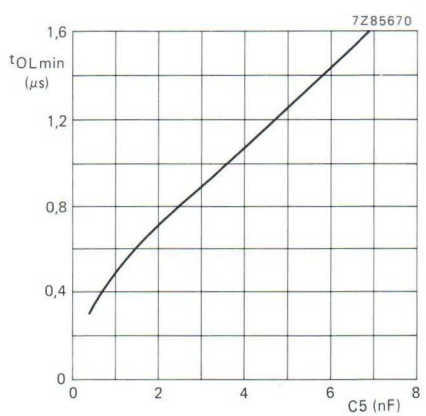


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

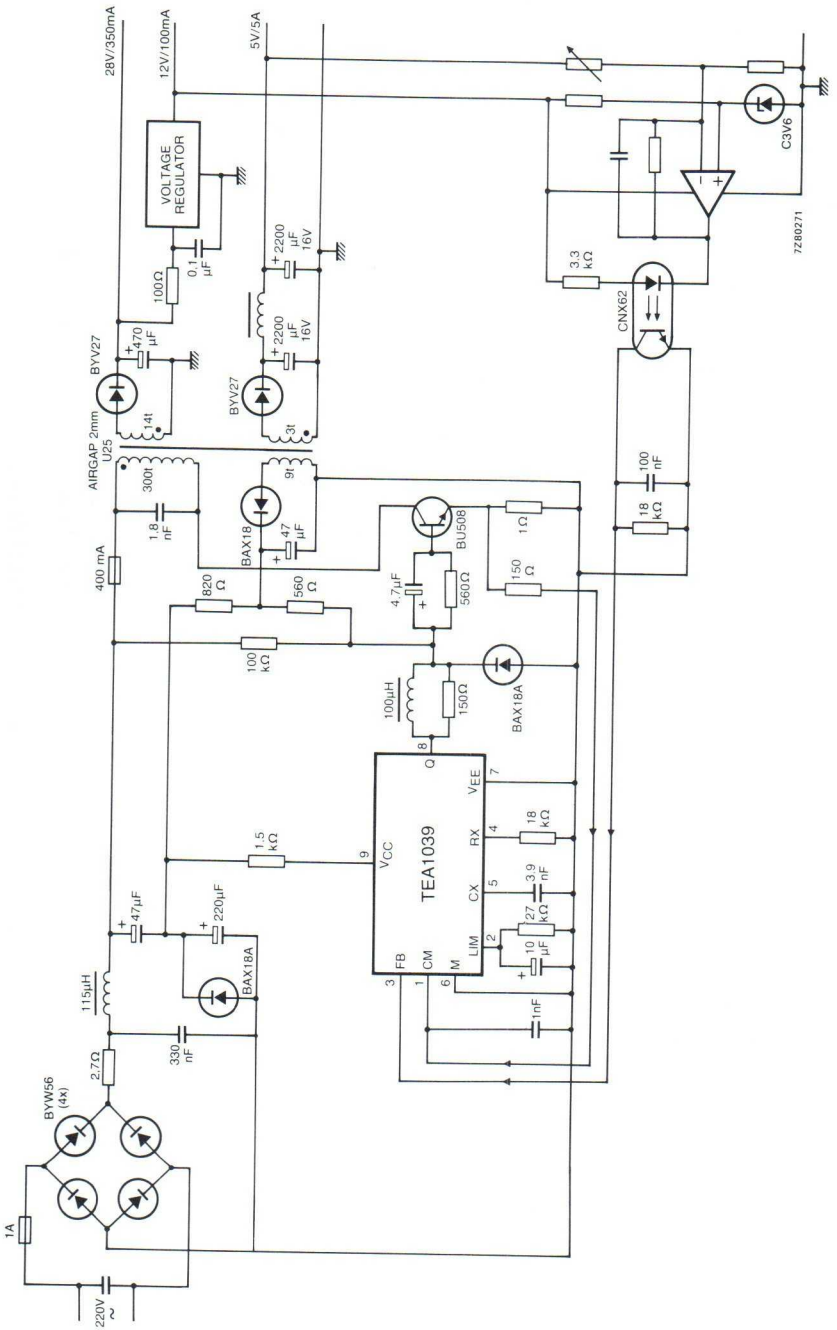


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

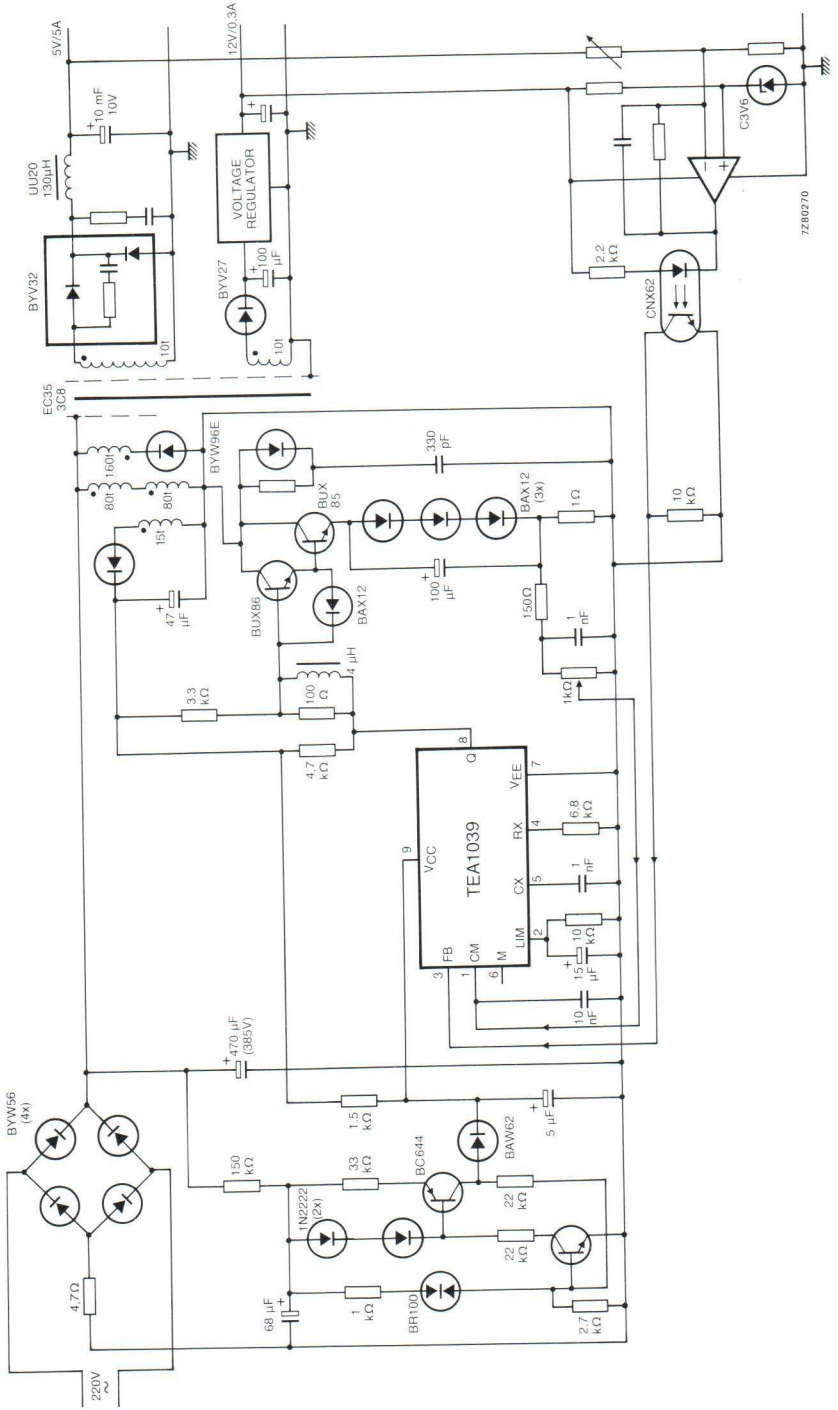


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

PLL STEREO DECODER (BTSC SYSTEM)

GENERAL DESCRIPTION

The TEA5582, a 20-pin integrated phase-locked loop (PLL) stereo decoder, is designed primarily for low cost stereo decoding in a low- to medium-line TV. The MUX input (pin 1) is a low impedance current input, the gain of the input amplifier is therefore determined by the external resistor R1 (see Fig.5). All characteristics are measured with R1 = 47 kΩ. The de-emphasis of (L, R) and (L−R) can be chosen by means of external capacitors and resistors. The supply voltage range of the device is from 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- LED driver for stereo indicator
- Smooth mono/stereo control
- Matrix and two amplifiers for left and right output signals
- A source selector to switch between the MUX signal and an external signal
- Mute circuit for 60 dB muting of the output level
- External de-emphasis control of (L, R) and (L−R)
- 6 dB fixed attenuation of (L−R) with respect to (L + R) prior to matrix
- All pins are protected against Electrostatic Discharge (ESD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Decoder						
Overall gain	mono; R1 = 47 kΩ	$G_o(V_o/V_i)$	4	5.8	7	dB
AF output voltage (RMS value)		$V_{14} = V_{15}$	–	245	–	mV
Total harmonic distortion	V_o = 600 mV	THD	–	0.3	–	%
Output channel unbalance		$\lvert V_{14}/V_{15}\rvert$	–	0.1	–	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Source selector						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Output amplifiers						
Gain output amplifier						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	−0.5	0	+0.5	dB
AF output voltage (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

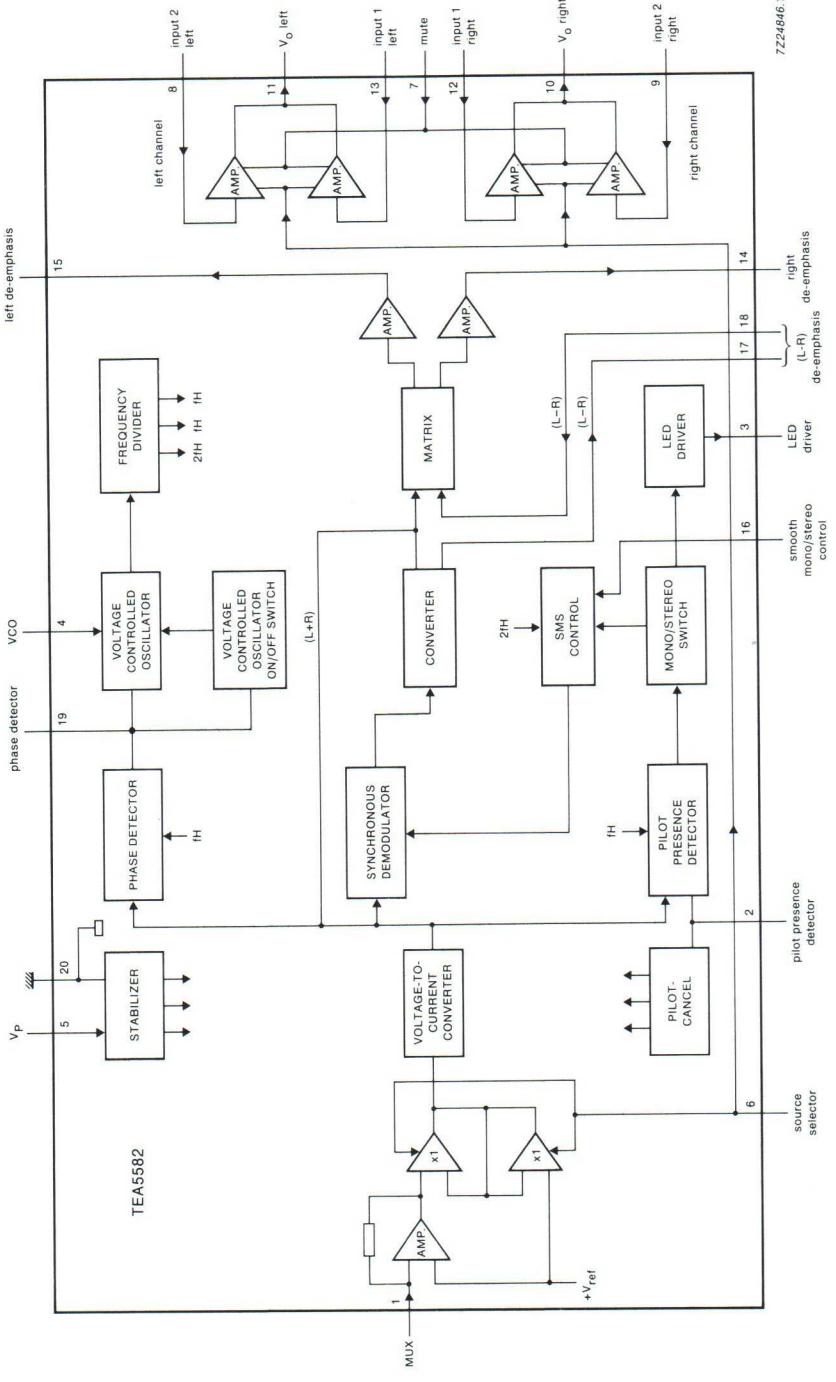


Fig.1 Block diagram.

PINNING

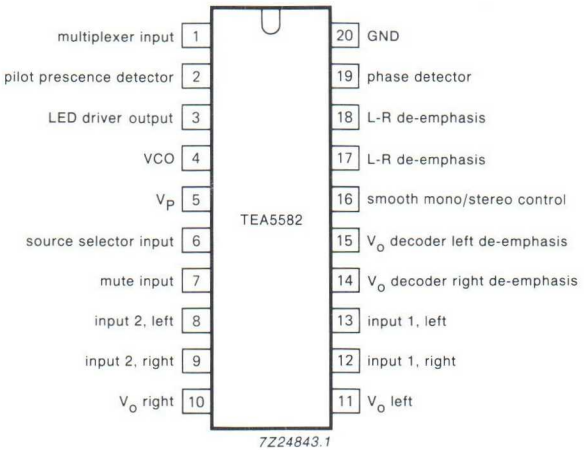


Fig.2 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 5)	V_P	–	18	V
LED-driver current (peak value)	I_3	–	75	mA
Total power dissipation	P_{tot}	see Fig.3		
Storage temperature range	T_{stg}	−65	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C
Electrostatic handling *	V_{es}	−2	+2	kV

* ESD withstand voltage is defined by MIL STD 883C (C = 100 pF; R = 1.5 kΩ).

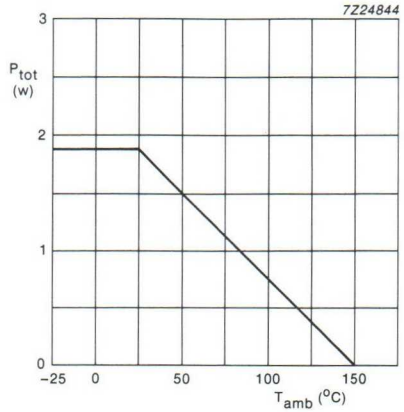


Fig.3 Power derating curve.

DC CHARACTERISTICS

All voltages are with respect to ground (pin 20); all currents are positive into the device; all parameters are measured in the test set-up (see Fig.5) at a nominal supply voltage of V_S = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Power dissipation		P_{tot}	–	160	–	mW
Voltage						
pin 1		V_1	–	2.1	–	V
pins 8, 9, 10, 11, 12 and 13		V_8-V_{13}	–	4.2	–	V
DC output current						
pins 14 and 15		$-I_{14}$, I_{15}	1.1	1.4	1.8	mA
LED-driver current						
pin 3		I_3	–	–	20	mA
Switch "VCO-OFF"						
voltage	I_{19} = 50 μA	V_{19}	–	2	–	V
Switch "VCO-OFF"						
current		I_{19}	50	–	–	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

Measured in the test circuit of Fig.5; V_S = 8.5 V; T_{amb} = 25 °C.
AC conditions: (1) input signal (V_i) of 815 mV p-p for L = 1, R = 1 (mono) f_m = 1 kHz (= 80% modulation). (2) MUX input signal (V_i) of 1.2 V p-p for L = 1, R = 0 and no DBX; f_m = 1 kHz (stereo) and V_{pilot} = 200 mV p-p. (3) S1 open, unless specified (without L–R filter); voltage controlled oscillator (VCO) adjusted to 188.8 kHz at V_i = 0 V; values are measured with an external IF roll-off network (–2 dB at 31.5 kHz = $2f_H$) at the input (dashed components RS and CS in Fig.5).
All the above conditions apply unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Overall performance (V_i to V_o)						
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R1 = 47 kΩ	G_o (V_o/V_i)	4	5.8	7	dB
AF output voltage (mono) (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
AF output voltage (mono) (RMS value)		$V_{15} = V_{14}$	–	245	–	mV
Total harmonic distortion	note 1	THD	–	0.3	0.5	%
Output voltage	THD = 1%	$V_{11} = V_{10}$	–	800	–	mV
Output channel unbalance		$\lvert V_{11}/V_{10} \rvert$	–	0.1	1	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Signal-to-noise ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
Pilot presence detector	note 2					
Switching to:						
stereo		V_{pilot}	–	40	60	mV
mono		V_{pilot}	15	30	–	mV
hysteresis		ΔV_{pilot}	–	2.5	–	dB
Smooth mono/stereo control (pin 16)	see Fig.4					
Channel separation (α)						
Full stereo	$V_{16} \geqslant 1.25$ V	α	24	28	–	dB
Smooth operation	V_{16} = typ. 1 V	α	–	10	–	dB
Full mono	$V_{16} \leqslant 0.75$ V	α	–	–	1	dB
Attenuation (L–R)			–	6	–	dB

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f_{pilot} = 15.734 kHz (1 fH)	αfH	32	36	–	dB
Subcarrier suppression f = 2 fH		α2fH	–	60	–	dB
VCO suppression f = 12fH		α12fH	–	75	–	dB
SAP signal suppression (Second Audio Programme) f = 5fH		α5fH	–	60	–	dB
Intermodulation suppression	note 4					
f_m = 8.367 kHz	spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 10.823 kHz	spurious signal f_s = 1 kHz	α_3	–	70	–	dB
Ripple rejection	f = 120 Hz; V_{ripple} = 100 mV; mono	RR_{120}	–	50	–	dB
VCO						
R adjust (R5)	f_{osc} = 188.808 kHz R7 = 10 kΩ 5% C6 = 820 pF 1%	R_{adj}	0	–	8	kΩ
Capture range	deviation from f_{osc} centre frequency; V_{pilot}=200 mV p-p	$\Delta f/f$	–	4.5	–	%
Temperature coefficient	uncompensated	TC	–	250 x 10^{-6}	–	K^{-1}
Output amplifiers						
Gain						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	–0.5	0	+0.5	dB
Input impedance		Z_i	–	50	–	kΩ
Output impedance		Z_o	–	10	–	Ω
External load impedance		Z_1	10	–	–	kΩ
External load capacitance		Z_1	–	–	1.5	nF
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
DC offset voltage at outputs	mute OFF-to-ON	ΔV	–	10	50	mV
	mute ON-to-OFF	ΔV	–	10	50	mV
Source selector (pin 6)						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Switching level	MUX selected					
voltage		V_{IL}	–	–	0.8	V
current	$V_I = 0.8$ V	I_{IL}	–	10	25	μA
Switching level	external selected					
voltage		V_{IH}	2	–	V_P	V
current	$V_I = V_P$	I_{IH}	–	0.1	1	μA
Muting circuit (pin 7)						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2	–	V_P	V
Input current	mute ON; $V_{IL} = 0.8$ V	$-I_{IL}$	–	10	25	μA
	mute OFF; $V_{IH} = V_P$	I_{IL}	–	0.1	1	μA

DEVELOPMENT DATA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Adjustable.
3. S1 closed; reference: AF output voltage f = 1 kHz (mono).
4. Intermodulation suppression (Beat-Frequency Components (BFC)):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 8.367\text{ kHz}) - fH$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 10.823\text{ kHz}) - 2fH$$

measured with 100% modulated input signal: L = R; pilot signal = 200 mV p-p; f_m = 8.367 or 10.823 kHz.

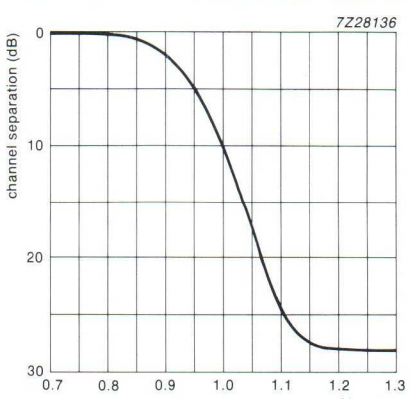


Fig.4 Smooth mono/stereo control.

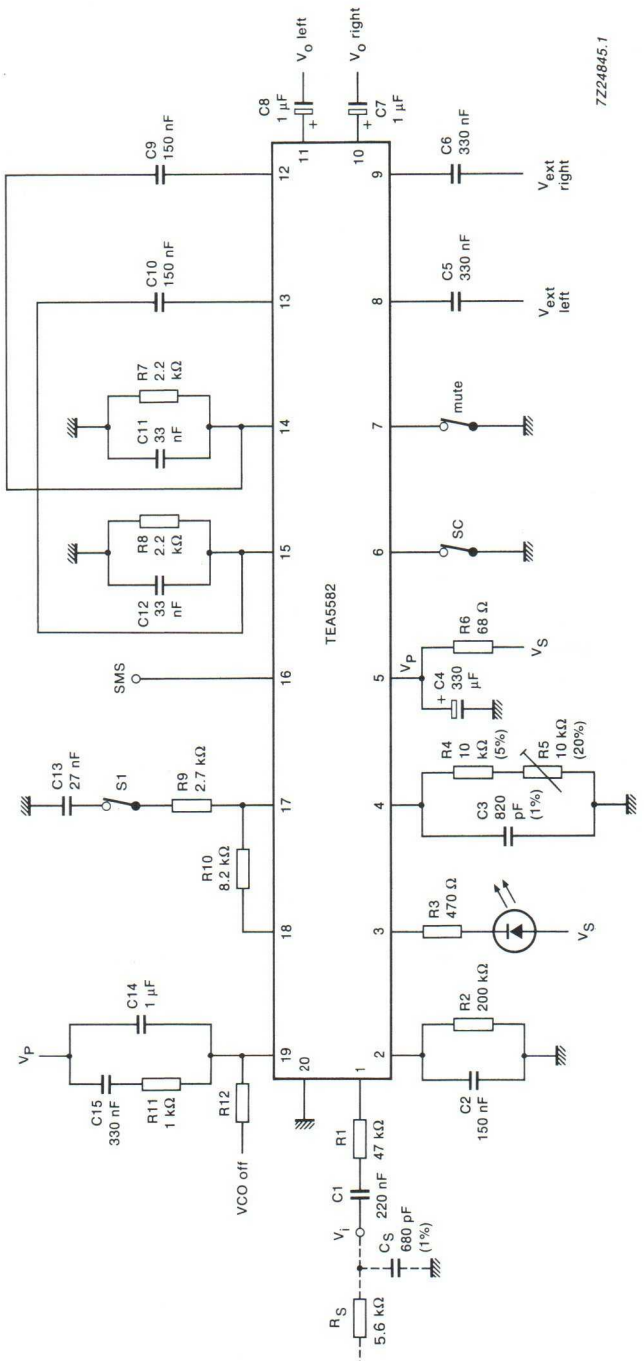


Fig.5 Test and application circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	September 1990

TEA7650H

Video signal processor for CD-video/laser vision

FEATURES

- Modulation Transfer Function correction (MTF) at signal input for both standards
- HF drop out detector
- Data slicer, data output for program information (IEC standards)
- Separation of signals for Electronic Time Base Correction (ETBC)
- Noise reduction with chrominance trap, noise level adjust point
- Dynamic picture insertion and 6 dB video attenuation of main picture
- Bandgap reference voltage output, suitable for CCD delay line

GENERAL DESCRIPTION

Bipolar IC for video signal processing used in CD-Video/LaserVision players.

Standard PAL respectively NTSC output signal (CVBS).

MTF amplifier.

FM-demodulator followed by de-emphasis stage.

PAL/NTSC switch for switching the MTF and de-emphasis.

Drop out detector with drop out switch, also externally switchable.

+5 volt supply, only 325 mW total power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 12, 30, 47)	-	5	-	V
I_P	total supply current	-	-	65	mA
$V_{i\ (p-p)}$	FM input signal at pin 7 (peak-to-peak value)	50	-	300	mV
$V_{o\ (p-p)}$	CVBS output signal for CCDs (peak sync – peak white, pin 29)	-	850	-	mV
V_{29}	black level voltage (pin 29)	-	1.85	-	V
$V_{i\ (p-p)}$	delayed CVBS input signal for drop out path at pin 27 (peak-to-peak value)	-	700	-	mV
$V_{i\ (p-p)}$	delayed CVBS input signal at pin 31 from ETBC path (peak-to-peak value)	-	600	-	mV
$V_{o\ (p-p)}$	main CVBS output signal at pin 42 (peak-to-peak value)	-	1	-	V
V_{42}	black level voltage (pin 42)	-	2.2	-	V
$V_{o\ (p-p)}$	chrominance output signals at pins 44, 48 (peak-to-peak value) PAL (burst) NTSC (burst)	 - -	 760 725	 - -	 mV mV
V_{ref}	reference output voltage (pin 41)	-	1.6	-	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA7650H	48	QFP48	plastic	SOT196A

Video signal processor for CD-video/laser vision

TEA7650H

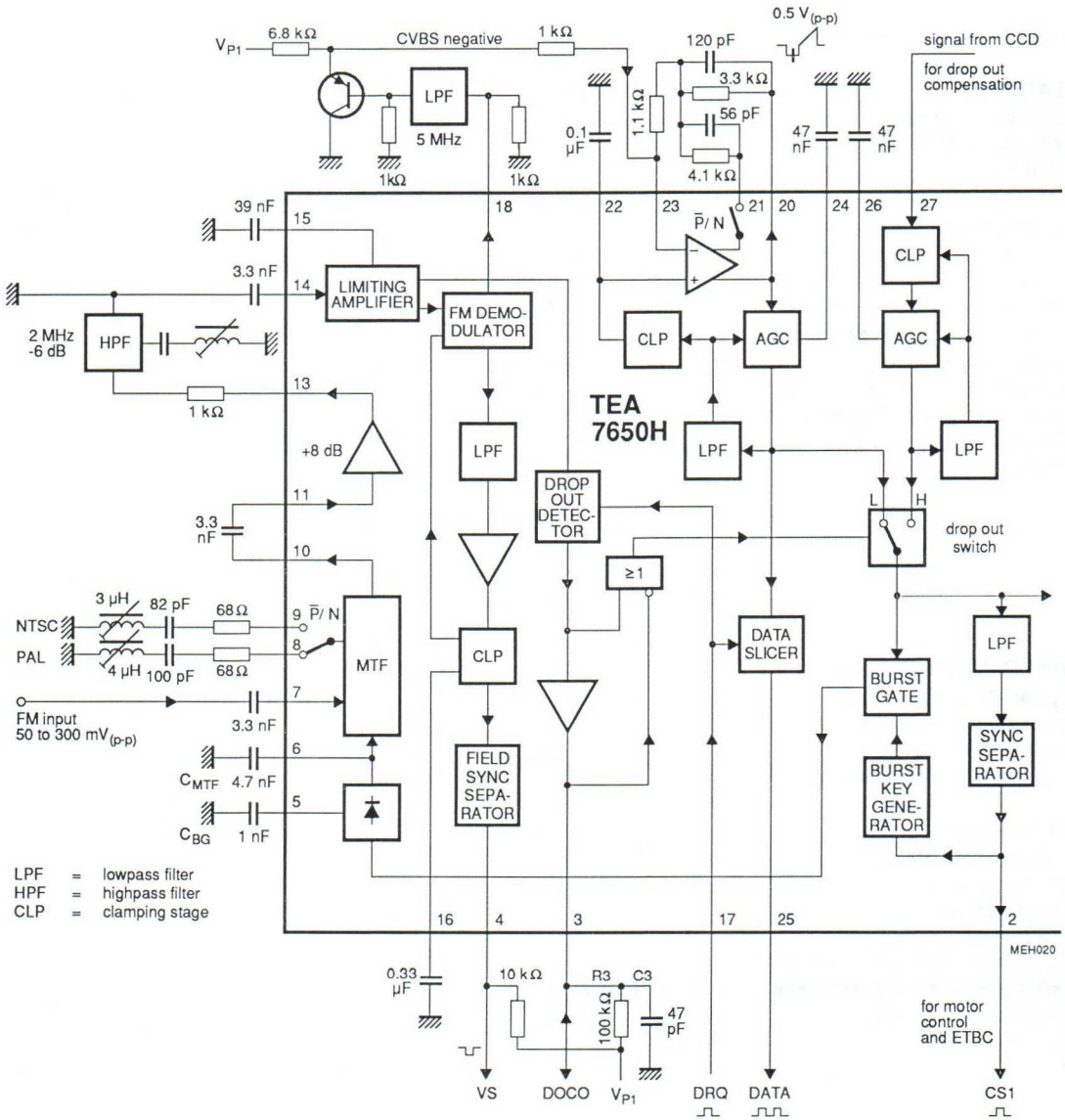


Fig.1(a) Block and test circuit; (continued in Fig.1(b)).

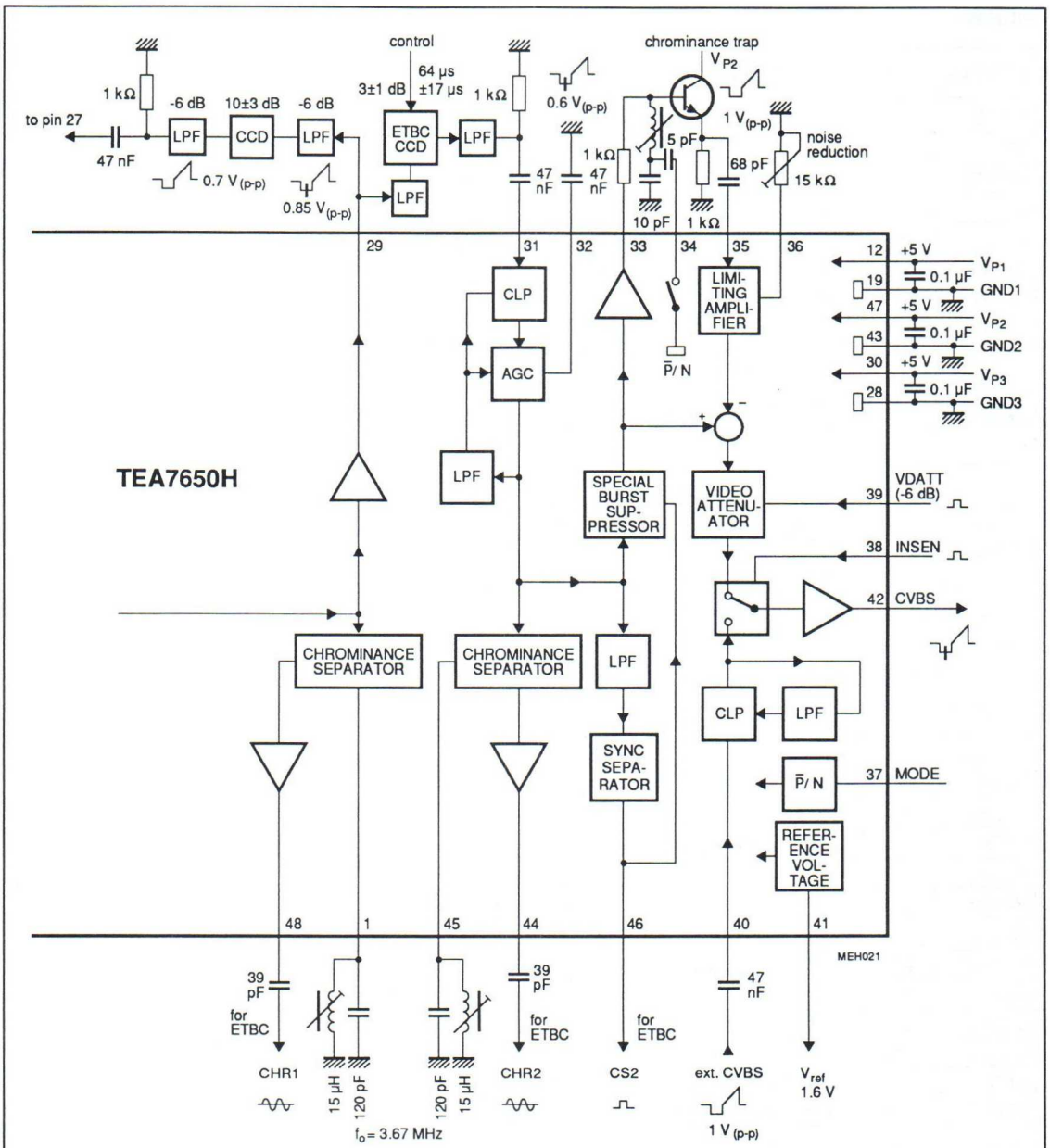


Fig.1(b) Block and test circuit; (continued from Fig.1(a)).

PINNING

SYMBOL	PIN	DESCRIPTION
CRSC1	1	3.67 MHz resonant circuit 1
CS1	2	line synchronization output pulse 1 (composite sync)
DOCO	3	drop out control, input/output for external control
VS	4	field sync output
C_{BG}	5	charging capacitor for burst rectifier
C_{MTF}	6	charging capacitor for MTF control voltage
FM-IN	7	FM input signal from preamplifier
FREF1	8	PAL resonant circuit for the MTF
FREF2	9	NTSC resonant circuit for the MTF
MTFO	10	MTF output signal (corrected FM signal)
AMPIN	11	input for 8 dB amplifier (FM signal)
V_{P1}	12	+5 V supply (referred to pins 6 to 15 and 18)
AMPO	13	output of 8 dB amplifier (FM signal)
LIMIN1	14	limiter amplifier input (FM signal to demodulator)
C_{LIM}	15	capacitor for slicing level control of limiter
C_{DEM}	16	capacitor for clamping level of FM demodulator
DRQ	17	data request input for data at pin 25
DEMO	18	FM demodulator output (CVBS negative)
GND1	19	ground (0 V) for V_{P1}
FBO1	20	feedback output at PAL and NTSC (de-emphasis)
FBO2	21	feedback output, additional at NTSC (de-emphasis)
C_{CVBS}	22	capacitor for clamping of CVBS amplifier
DEEMI	23	de-emphasis input for CVBS from demodulator
C_{AGC1}	24	capacitor for AGC of CVBS amplifier
DATA	25	data output of information code
C_{AGC2}	26	capacitor for AGC of drop out amplifier
PRLIN	27	input signal of preceding line from CCD delay
GND3	28	ground (0 V) for V_{P3}
DOSW	29	drop out switch buffer output (to CCD delay and ETBC)
V_{P3}	30	+5 V supply (referred to pins 5, 17, 20 to 36, 38 to 42)
VIDIN	31	CVBS input signal from ETBC
C_{AGC3}	32	capacitor for AGC of CVBS follower amplifier
VIBUF	33	video signal buffer output to chroma trap circuitry
FTRAP	34	switching output for chroma trap at NTSC
LIMI2	35	limiter amplifier input for noise reduction
NRADJ	36	noise level adjust point (resistor to ground)
MODE	37	standard select input PAL/NTSC (PAL = LOW)
INSEN	38	insertion enable input
VDATT	39	6 dB CVBS attenuation (active HIGH)

SYMBOL	PIN	DESCRIPTION
EXVID	40	external CVBS input for insertion
V_{ref}	41	reference voltage output (1.6 V)
CVBS	42	main CVBS output signal
GND2	43	ground (0 V) for V_{P2}
CHR2	44	chrominance output signal 2
CRSC2	45	3.67 MHz resonant circuit 2
CS2	46	line synchronization pulse 2 (composite sync)
V_{P2}	47	+5 V supply (referred to pins 1 to 4, 16, 37, 43 to 48)
CHR1	48	chrominance output signal 1

PIN CONFIGURATION

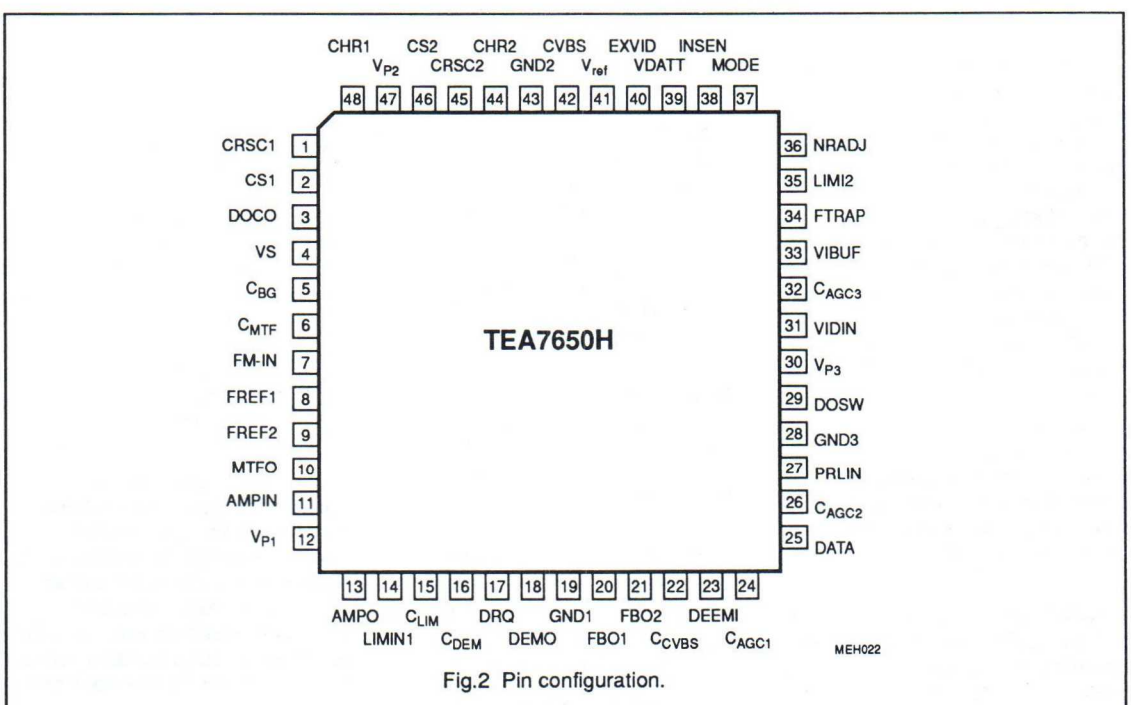


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 is the block diagram of the Video Signal Processor (VSP) including the peripherial circuitry for the video signal processing.The pulse-width modulated FM signal from the preamplifier is fed, via a DC blocking capacitor, into the IC (pin 7) at the input to the Modulation Transfer Function (MTF) circuit which corrects for the characteristic of the optical reading system.

MTF correction

Due to the finite diameter of the laser beam spot and the tangential velocity of the track of pits on the disk, the MTF of the optical system acts like a radius-dependent low-pass filter for the FM input signal. Although the video signal can be recovered without correction, the ratio of the amplitudes of the chrominance and luminance signals would not then be the same at the most inner and the most outer part of the disk. This influence of the disk radius is automatically corrected by the Video Signal Processor. The principle of correction is to use the deviation of the demodulated burst signal to generate an error voltage in order to control the frequency selective MTF circuit. The burst measurement operates as follows: A burst-key generator is triggered by the line synchronization pulse (CS1) to generate a burst-key pulse which activates the burst gate and rectifier stage. The signal at the rectifier output (pin 6) is used to control the amplification of the MTF circuit.

The carrier frequency in the PAL standard is different to that in the NTSC standard, therefore two separate resonant circuits are required on pins 8 and 9. They are selected by the PAL/NTSC system selector (pin 37).

The MTF-corrected FM signal at pin 10 is amplified (+8 dB) and fed, via the external filter which removes the audio frequency components from the signal, into the demodulator at pin 14.

Demodulation

The FM signal is first fed into a limiter circuit (pin 14) with automatic slicing level control to suppress the main carier in the demodulated signal. The demodulator has two outputs. The first (internal) clamps the demodulated video signal on peak-sync by controlling the transconductance of the demodulator. The FM signal can now be demodulated during disk start-up, thereby facilitating fast run-in. The second output signal from the demodulator (pin 18) is passed through an external 5 MHz low-pass filter to extract the CVBS signal. The CVBS signal is then fed into the de-emphasis network to compensate for the pre-emphasis of the video signal recorded on the disk.

De-emphasis

The de-emphasis circuit consists of an internal inverting amplifier and an external RC feedback network. Since the pre-emphasis on the disk in the PAL standard is different from that in the NTSC standard, the time constants are switchable. When PAL is selected, the first arm of the feedback network is active, otherwise both operate in parallel.The de-emphasized video signal is fed into an AGC stage (pin 20) where it is clamped on its black level and amplitude-controlled to a constant level. The signal is then fed into the data slicer and the drop out switch.

Data slicer

Coded signals on the video disk are extracted by the data slicer (output pin 25) when the Data Request input is activated (pin 17).

Drop out compensation

The drop out detector (DOD) in the IC is triggered by every positive or negative transition of the FM signal. A drop out is detected when the half-cycle period is outside the limits. Protection against a drop out is achieved by use of a video signal delayed by one line. The signal at the output of the drop out switch is fed out of the IC via a buffer (pin 29) and then through a delaying device (CCD) before being fed back into the IC (pin 27). The delayed video signal appears at the input of an AGC circuit to compensate for gain tolerances of the delay line and avoids the need for an external adjustment. When a drop out is detected, the drop out detector activates the video switch so that the lost information of the line is substituted by the information of the preceding line.

The drop out pulse is also present at pin 3 and can be used for different purposes. This pin can also act as an input to control the drop out switch by an external signal for test purposes.

Time error compensation

In a videodisk player timing errors are caused by deviations of the rotational speed of the motor, imperfections in the disk and unavoidable tolerances in the centering of the disk on the turntable. Track excentricity is the main cause of timing errors.

To minimize timing errors, it is necessary in the first place to keep the rotational speed of the disk as constant as possible. Referring back to the output of the switch in Fig.1, the video signal is also fed into a sync seperator and a chrominance separator with its external resonant circuits tuned to the chrominance subcarrier frequency. The phase of the line synchronization pulses (CS1, pin 2) can be used to control the speed of the turntable motor.

However, with this method it is not possible to obtain an acceptable reduction of timing errors for frequencies of 25 Hz and above. To reduce errors, use is made of an external Electronic Time Base Corrector (ETBC) between pins 27 and 31 which functions as a variable delay line driven by an error signal.

This error signal can be extracted from the output signal CS1 (pin 2), CHR1 (pin 48), CS2 (pin 46) and CHR2 (pin 44).

Since the line sync pulses (CS1) are not suitable to achieve an accurate enough measurement of time difference, use is made of the 3.58 MHz burst signal derived from the chrominance signal CHR1. If the same zero crossing of the burst signal is used in every line, the actual time can be measured with sufficient accuracy.

The CVBS signal leaving the ETBC might still have small timing errors due to residual control error. A second (feedback) loop is therefore required. The CVBS signal is fed into an AGC circuit (pin 31) that compensates for gain tolerances in the ETBC. As in the first loop, the line synchronization pulses (CS2) and the chrominance signal (CHR2) are derived from the CVBS signal by using second sync and chrominance separators. The error signal obtained by comparison in this feedback loop is added to the error signal obtained in the first loop.

Using the burst signal for accurate measurements is a problem in the PAL format due to its alternating phase. A special 3.75 MHz (240 fh) burst has therefore been added to the video signal recorded on the PAL disk. This burst is inserted on the top level of the line sync pulses.

In dual standard applications, the resonant circuits of the chrominance separators (pins 1 and 45) should be tuned to 3.67 MHz to ensure good separation of the special burst or the chrominance subcarrier.

When the timebase-corrected CVBS signal has by-passed the second sync and chrominance separators, it reaches the special burst suppressor which removes the special burst. The signal is then fed into the noise reduction circuit.

Noise reduction

A noise reduction circuit can be used to improve the apparent picture quality of a noisy signal. It operates as follows: First the timebase corrected CVBS signal is buffered (pin 33) and then fed into an external network which removes the chrominance subcarrier and all low-frequency components. It is then fed into a limiter (pin 35) which ensures that only small amplitudes (mainly noise) are removed from the main signal.

The chrominance subcarrier trap is switched to either the PAL subcarrier frequency (4.43 MHz) or the NTSC subcarrier (3.58 MHz) by the PAL/NTSC system selector (pin 37) using the additional small capacitor at pin 34. An external resistor at pin 36 is included so that manufacturers can select their preferred level of noise reduction, or none at all, by grounding the pin.

Picture insertion

The CVBS signal containing the information to be displayed is applied to pin 40. A clamp circuit ensures that the black level of this signal is the same as that of the main signal. Both signals are applied to the insertion switch.

When, for example, a character is to be displayed the 6 dB attenuation (pin 39) is first activated to generate a reduced contrast background area around the character (with respect to the black level so that the original picture is still visible). Next, the insertion switch (pin 38) is activated and the character appears at the output. By switching back to the original picture, the procedure operates in the reverse sequence.

Other examples of the picture insertion facility are displaying a background picture during start-up of the video disk player or the use of picture-in-picture.

A buffer is provided at the CVBS output (pin 42) which delivers a CVBS signal clamped to black level and controlled to a peak-to-peak amplitude of 1 V.

Reference voltage

A reference voltage of 1.6 V is provided by a bandgap circuit. Internally, all control circuits are supplied with this reference voltage. Externally, it can be used for various purposes.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage 1 (pin 12)	0	6	V
V_{P2}	supply voltage 2 (pin 47)	0	6	V
V_{P3}	supply voltage 3 (pin 30)	0	6	V
V_n	voltage on all pins except ground pins	0	V_P	V
P_{tot}	total power dissipation	0	360	mW
T_{stg}	storage temperatur range	–25	+150	°C
T_{amb}	operating ambient temperatur range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins	±400	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	92	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = V_{P3} = 5$ V, $T_{amb} = 25$ °C, measurements taken in Fig.1 ; unless otherwise specified.

Voltages referred to GND1 (pin 19): V_{P1} and voltage at pins 6 to 15, 18
GND2 (pin 43): V_{P2} and voltage at pins 1 to 4, 16, 37, 44 to 48
GND3 (pin 28): V_{P3} and voltage at pins 5, 17, 20 to 36, 38 to 42

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage 1 (pin 12)		4.5	5	5.5	V
V_{P2}	supply voltage 2 (pin 47)		4.5	5	5.5	V
V_{P3}	supply voltage 3 (pin 30)		4.5	5	5.5	V
$I_{12+30+47}$	total supply current		-	-	65	mA
Standard select input (pin 37)						
V_{IL}	input voltage for standard PAL (LOW)		0	-	1	V
V_{IH}	input voltage for standard NTSC (HIGH), alternative measure for standard NTSC	pin connected pin open-circuit	3 -	- -	V_{P2} -	V
I_{IL}	input current (LOW)	$V_{37} = 1$ V	-	-	–100	µA
I_{IH}	input current (HIGH)	$V_{37} = 4$ V	-	-	20	µA

Video signal processor for CD-video/laser vision

TEA7650H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Modulation transfer function MTF (referred to GND1, pin 19)						
$V_{i\,(p\text{-}p)}$	FM input signal at pin 7 (peak-to-peak value)		50	-	300	mV
	for proper MTF correction		50	-	200	mV
Z_7	input impedance		-	5	-	kΩ
	MTF control signal					
$I_{(p\text{-}p)}$	output current for storage of the burst amplitude at pin 5 (peak-to-peak value)		-	200	-	μA
I_6	burst amplitude integrator, charging current (pin 6)		-	±50	-	μA
g	conductance $g = dI_6 / dV_5$		-	–1	-	mS
	MTF frequency selection (pins 8 and 9)	pin 8 aktive for PAL; pin 9 active for NTSC				
$V_{o\,(p\text{-}p)}$	output signal		-	$V_{7\,(p\text{-}p)}$	-	mV
Z	output impedance		-	-	10	Ω
$I_{o\,(p\text{-}p)}$	output current		-	-	4.5	mA
$V_{o\,(p\text{-}p)}$	MTF output signal (pin 10)		-	-	300	mV
Z_{10}	MTF output impedance		-	-	100	Ω
G_v	signal gain	$G_v = V_{10} / V_7$				
G_o	$G_v = G_o + 20 \log\ G_r\,(V_6)$		-	0	-	dB
G_r	minimum gain	$V_6 = 0$	-	0	-	dB
	maximum gain	$V_6 = 2.6$ V	-	300Ω/R8	-	
	maximum gain	$V_6 = 2.6$ V	-	300Ω/R9	-	
B	bandwith	–3 dB; $G_r = 0$	15	-	-	MHz
α_{2H}	second harmonic suppression	f = 8 MHz	40	-	-	dB
MTF following amplifier (pins 11 and 13)						
$V_{i\,(p\text{-}p)}$	FM input signal at pin 11 (peak-to-peak value)		-	-	300	mV
Z_{11}	intput impedance		10	-	-	kΩ
R_E	internal emitter resistor to ground		-	1.8	-	kΩ
Z_{13}	output impedance (pin 13)		-	-	50	Ω
$I_{o\,(p\text{-}p)}$	output current at pin 13 (peak-to-peak value)		-	-	1	mA
G_v	voltage gain (pins 13-11)		-	8	-	dB
B	bandwith (pin 13)	–3 dB	15	-	-	MHz
α_{2H}	second harmonic suppression		40	-	-	dB

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifier for demodulator						
$V_{i\,(p\text{-}p)}$	input signal for proper demodulation at pin 14 (peak-to-peak value)		0.1	-	1	V
Z_{14}	input impedance		10	-	-	kΩ
$I_{(p\text{-}p)}$	charging current of 2nd harmonic control at pin 15 (peak-to-peak value)		-	200	-	μA
FM demodulator with pulswidth-modulated current output ($f = 2\,f_{in}$). Referred to GND1, pin 19						
$I_{(p\text{-}p)}$	output current pulse at pin 18 (peak-to-peak value)		-	–3.2	-	mA
I_{18}	mean (average) DC current	for top sync	-	–1.75	-	mA
Z_{18}	output impedance		30	-	-	kΩ
V_{18}	DC output voltage range		0	-	2	V
S	transconductance	at PAL	-	–210	-	μA/MHz
		at NTSC	-	–185	-	μA/MHz
N	static non-linearity		-	-	10	%
B	bandwidth	±1 dB	5	-	-	MHz
α	main carrier suppression	$V_{14\,(p\text{-}p)} = 100$ mV	35	-	-	dB
$I_{(p\text{-}p)}$	charging current at pin 16 (amplitude storage for top sync, peak-to-peak value)		-	26	-	μA
De-emphasis amplifier (output pin 21 only for NTSC active). Referred to GND3, pin 28						
Z_{23}	input impedance (pin 23)		10	-	-	kΩ
I_{23}	DC input current		-	-	2	μA
$I_{(p\text{-}p)}$	charging current for black clamping capacitor at pin 22 (peak-to-peak value)		-	3	-	μA
$R_{20,\,21}$	output impedance (pins 20 and 21)		-	-	100	Ω
$V_{20,\,21}$	DC output voltage (black level)		-	2.2	-	V
BW_g	gain bandwidth product		40	-	-	MHz
$I_{24\,(p\text{-}p)}$	charging current for AGC capacitor at pin 24 (peak-to-peak value)		-	11	-	μA
Composite sync output CS1 (pin 2; referred to GND2, pin 43)						
V_{oH}	sync output voltage (active HIGH)	$I_2 = -0.5$ mA	4	-	-	V
V_{oL}	sync output voltage (LOW)	$I_2 = 0.5$ mA	-	-	0.4	V
t_d	delay of positive going sync edge		-	-	300	ns
Δt_d	jitter of positive going sync edge		-	-	40	ns
t_r, t_f	rise and fall time	$C_L = 22$ pF	-	-	200	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sync output (VS), open collector output with 500 Ω internal series resistor, referred to GND2, pin 43						
V_4	sync output voltage active LOW (pin 4)	$I_4 = -0.5$ mA	-	-	0,7	V
t_d	delay time		-	18	-	µs
t_e	elongation time		-	70	-	µs
Drop out processing. (referred to GND3, pin 28)						
f_i	frequency range for no drop out recognition					
f_1	minimum value at PAL		-	5.6	-	MHz
f_2	maximum value at PAL		-	9.7	-	MHz
f_1	minimum value at NTSC		-	6.97	-	MHz
f_2	maximum value at NTSC		-	11.1	-	MHz
t_d	delay time on negative going edge for an abrupt drop out with $f < 0.5\ f_1$ or $f > 1.5\ f_2$		-	-	250	ns
t_e	drop out elongation time	C3 = 47 pF; R3 =100 kΩ	-	3.5	-	µs
V_3	output voltage during drop out	internal R_S = 500 Ω $I_3 = -0.5$ mA	-	-	0.7	V
$V_{3\ thr}$	threshold voltage of drop out switch		-	2	-	V
$V_{3\ DO}$	input voltage for forced drop out switching		0		0.7	V
$V_{i\ (p-p)}$	delayed video input signal at pin 27 (peak-to-peak value)	$R_G \leq 1$ kΩ	-	700	-	mV
V_{27}	DC input voltage (black level)		-	2.2	-	V
Z_{27}	input impedance		10	-	-	kΩ
$I_{(p-p)}$	charging current for coupling capacitor at pin 27 (peak-to-peak value)		-	3	-	µA
$I_{(p-p)}$	charging current for AGC of the delayed signal at pin 26 (peak-to-peak value)		-	11	-	µA
Chrominance output for purpose of ETBC, with R_L = 5 kΩ (pin 48) and nominal input signal. Resonant circuit at pin 1 tuned to 4.43 MHz for PAL (3.58 MHz for NTSC). Referred to GND2, pin 43. See previous comment to characteristics.						
$V_{o\ (p-p)}$	burst amplitude (peak-to-peak value) at pin 48	PAL; f = 4.43 MHz	-	760	-	mV
		NTSC; f = 3.58 MHz	-	725	-	mV
Z_{48}	output impedance		-	-	250	Ω
$I_{o\ (p-p)}$	output current (peak-to-peak value)		-	-	700	µA
α_{CR}	crosstalk attenuation from pin 44		32	-	-	dB
R_1	output impedance for resonant circuit		-	1.4	-	kΩ

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Electronic time base control ETBC and CCD delay (external). Referred to GND3, pin 28.						
$V_{o\ (p-p)}$	CVBS output signal of emitter output at pin 29 (peak-to-peak value)	$V_{20\ (p-p)}$= 0.5 V ±3 dB (peak-to-peak value)	-	850	-	mV
	burst amplitude in signal	for PAL	-	230	-	mV
		for NTSC	-	219	-	mV
V_{29}	DC output voltage (black level)		-	1.85	-	V
Z_{29}	output impedance		-	$-V_t / I_{29}$	-	Ω
I_{29}	output current (source)		-	-	–3	mA
S/N	signal-to-noise ratio from pin 7 to pin 29	5 MHz unweighted	50	-	-	dB
$\Delta V_{o\ (p-p)}$	difference of CVBS amplitude (peak-to-peak value)	switching from main to delayed signal; $V_{27\ (p-p)}$ = 0.7 V				
	at pin 29 referred to 0 dB level	0 dB	-		±2	%
	at pin 29 referred to ±4 dB level	±4 dB	-	-	±6	%
α_{CR}	crosstalk attenuation	f = 2 MHz	35	-	-	dB
ΔV_{29}	offset voltage after switching		-	-	10	mV
ΔV_S	spike amplitude at switching (pin 29)	t_S > 50 ns	-	-	15	mV
Chrominance and luminance amplifier (referred to GND3, pin 28).						
$V_{i\ (p-p)}$	delayed CVBS input signal (pin 31)	$R_G \leq 1$ kΩ	-	600	-	mV
V_{31}	DC input voltage (black level)		-	2.2	-	V
Z_{31}	input impedance		10	-	-	kΩ
$I_{(p-p)}$	charging current for coupling capacitor at pin 31 (peak-to-peak value)		-	3	-	µA
$I_{(p-p)}$	charging current for AGC at pin 32 (peak-to-peak value)		-	11	-	µA
Chrominance output for purpose of ETBC, with R_L = 5 kΩ (pin 44) and nominal input signal. Resonant circuit at pin 45 tuned to 4.43 MHz for PAL (3.58 MHz for NTSC). Referred to GND2, pin 43. See previous comment to characteristics.						
$V_{o\ (p-p)}$	burst amplitude (peak-to-peak value) at pins 44					
	for PAL	f = 4.43 MHz	-	760	-	mV
	for NTSC	f = 3.58 MHz	-	725	-	mV
Z_{44}	output impedance		-	-	250	Ω
$I_{o\ (p-p)}$	output current (peak-to-peak value)		-	-	700	µA
α_{CR}	crosstalk attenuation from pin 48		32	-	-	dB
R_{45}	output impedance for resonant circuit		-	1.4	-	kΩ

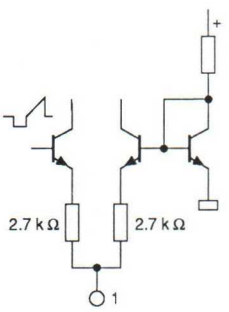
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance noise reduction (referred to GND3, pin 28)						
$V_{(p-p)}$	output signal at pin 33 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±3 dB at pin 31	-	1	-	V
V_{33}	DC output voltage (black level)		-	2.2	-	V
I_E	internal emitter current to ground of emitter follower		-	1	-	mA
Z_{33}	output impedance		-	-	100	Ω
$I_{o(p-p)}$	AC output current at pin 33 (peak-to-peak value)		-	-	1.5	mA
$I_{(p-p)}$	chroma trap switch, active for NTSC input current (peak-to-peak value)		-	-	350	µA
Z_{34}	input impedance (pin 34)		-	-	50	Ω
$V_{i(p-p)}$	limiter amplifier input signal at pin 35 (peak-to-peak value)		-	1	-	V
	input signal for start of limiting		0	-	100	mV
Z_{35}	intput impedance		-	2	-	kΩ
V_{36}	voltage range for limiter control (pin 36)		0.1	-	1.5	V
	voltage for control-off		-	0	-	V
I_{36}	DC output current		-	–100	-	µA
Main CVBS output (referred to GND3, pin 28).						
$V_{o(p-p)}$	CVBS output signal of emitter output at pin 42 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±0 dB at pin 31	-	1	-	V
$\Delta V_{o(p-p)}$	residual variation of output voltage at pin 42 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±3 dB at pin 31	-	-	±3	%
V_{42}	DC output voltage (black level)		-	2.2	-	V
I_E	internal emitter current to ground of emitter follower		-	300	-	µA
Z_{42}	output impedance		-	-	100	Ω
I_o	output source current		-	-	–5	mA
B	video bandwidth	–3 dB	5			MHz
S/N	signal-to-noise ratio from pin 31 to pin 42	5 MHz unweighted	60	-	-	dB
α_{CR}	crosstalk attenuation between main and inserted signal	f = 5 MHz	45	-	-	dB
	differences at output due to switching from main to inserted signal (pin 42)					
α_{burst}	suppression of special burst		35	-	-	dB
ΔV_{42}	offset voltage after switching		-	-	50	mV
ΔV_S	spike amplitude at switching	t_S > 50 ns	-	-	20	mV
ΔV_{VID}	video attenuation for internal signal	V_{39} = HIGH	-	6	-	dB

CHARACTERISTICS (continued)

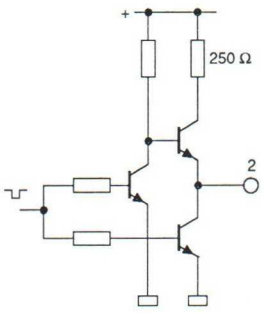
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External video insertion input and switching control						
$V_{i\,(p\text{-}p)}$	input signal at pin 40 (peak-to-peak value)	$R_G \leq 1\ k\Omega$	-	1	-	V
V_{40}	DC voltage (black level)		-	2.9	-	V
G_v	voltage gain (pins 42-40)		-	0	-	dB
Z_{40}	intput impedance		10	-	-	kΩ
$I_{(p\text{-}p)}$	charging current at pin 40 (peak-to-peak value)		-	3	-	µA
B	video bandwith	–3 dB	8	-	-	MHz
V_{38}	voltage for insertion-on (HIGH)		3	-	V_P	V
	voltage for insertion-off (LOW)		0	-	1	V
I_{38}	input current (HIGH)	$V_{38} = 4$ V	-	-	2	µA
	input current (LOW)	$V_{38} = 1$ V	-	-	–10	µA
t_d	switchover delay time		-	-	50	ns
V_{39}	voltage for video attenuation-on (HIGH)	–6 dB video	3	-	V_P	V
	voltage for video attenuation-off (LOW)	0 dB video	0	-	1	V
I_{39}	input current (HIGH)	$V_{39} = 4$ V	-	-	2	µA
I_{39}	input current (LOW)	$V_{39} = 1$ V	-	-	–10	µA
t_d	switchover delay time		-	-	100	ns
Data output and data request input (pins 25 and 17)						
V_{25}	output voltage HIGH-level (pin 25)	$I_{25} = -0.5$ mA	3.5	-	-	V
	output voltage LOW-level	$I_{25} = 0.5$ mA	-	-	0.8	V
t_p	duty factor (t_p / T)		-	50	-	%
t_r and t_f	rise and fall time	$C_L = 22$ pF	-	-	150	ns
t_d	delay time		-	-	200	ns
V_{17}	voltage for data request-on (HIGH) at pin 17		3	-	V_P	V
	voltage for data request-off (LOW)		0	-	1	V
I_{17}	input current (HIGH)	$V_{17} = 4$ V	-	-	20	µA
	input current (LOW)	$V_{17} = 1$ V	-	-	–100	µA
t_d	data delay time		-	-	200	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite sync output CS2 (referred to GND2, pin 43)						
V_{46}	sync output voltage (active HIGH)	I_{46} = –0.5 mA	4	-	-	V
	sync output voltage at pin 46 (LOW)	I_{46} = 0.5 mA	-	-	0.4	V
t_d	delay of positive going sync edge		-	-	300	ns
Δt_d	jitter of positive going sync edge		-	-	40	ns
t_r	rise time	$C_{L\ 46}$ = 22 pF	-	-	150	ns
t_f	fall time	$C_{L\ 46}$ = 22 pF	--	-	200	ns
Reference output voltage (refered to GND3, pin 28)						
V_{ref}	reference output voltage (pin 41)		-	1.6	-	V
R_{41}	output resistance		-	-	5	kΩ
I_{ref}	output current (used for CCD reference)		-	-	±10	μA
dV_{41}/dV_P	supply voltage dependence		-	-	–20	dB
dV_{41}	dependence of junction temperature	T_j = 20 to 120 °C	-	-	±30	mV

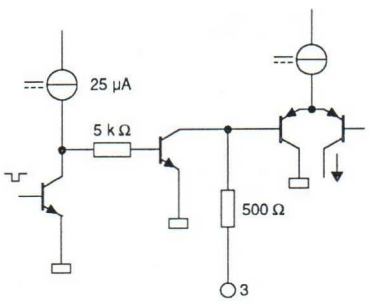
APPLICATION INFORMATION



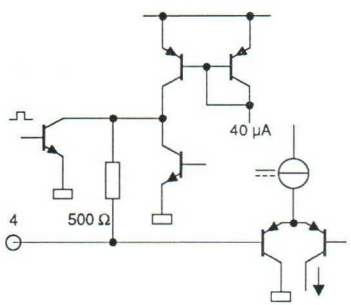
Pins 1 or 45: Frequency selection



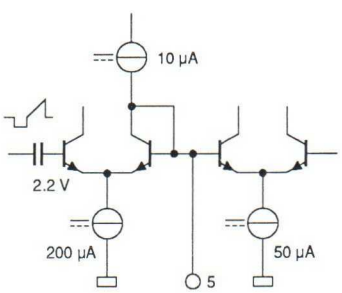
Pin 2: Output of first sync separator



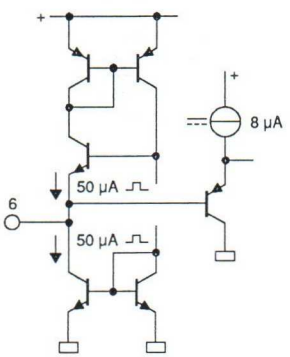
Pin 3: Output of dropout detector



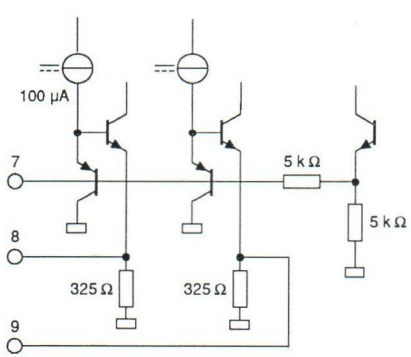
Pin 4: Output of vertical sync separator



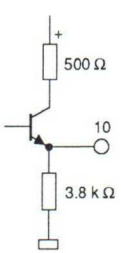
Pin 5: Output of burst rectifier



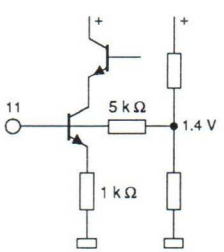
Pin 6: Burst amplitude integrator



Pins 7, 8 or 9: MTF corrector



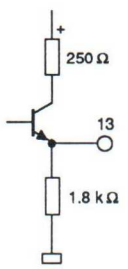
Pin 10: Output of MTF corrector



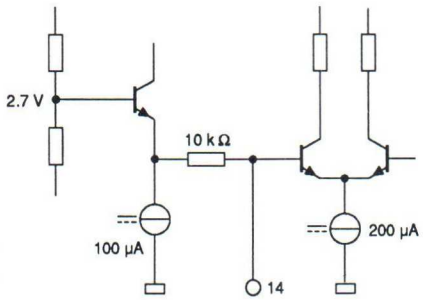
Pin 11: Input of 8 dB amplifier

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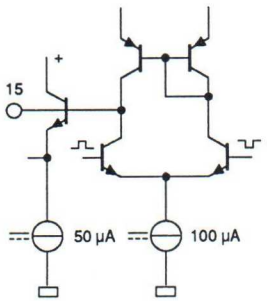
Fig.3(a) Internal circuits; (continued in Fig.4(b)).



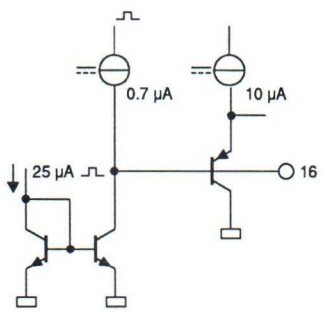
Pin 13: 8 dB amplifier output



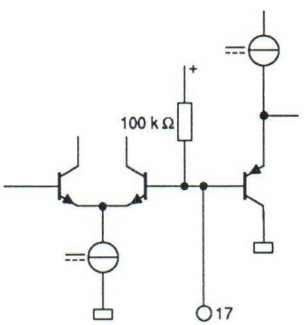
Pin 14: Input of limiter amplifier



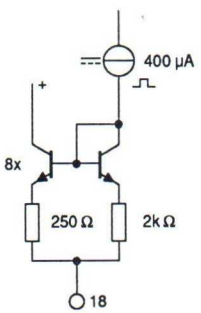
Pin 15: Control input of limiter amplifier



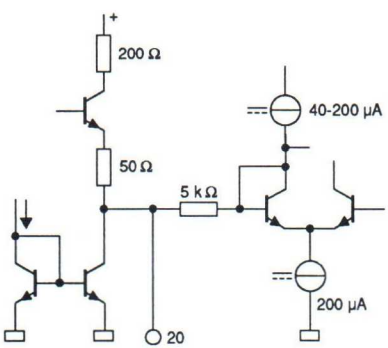
Pin 16: Demodulator control



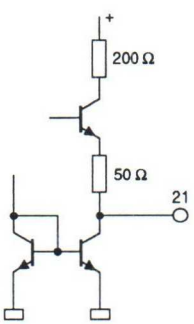
Pin 17: Input data request



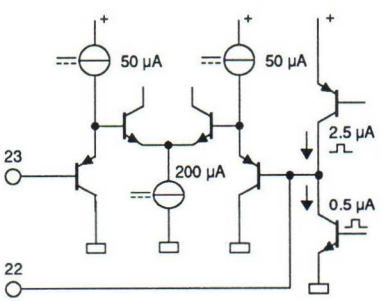
Pin 18: Output of FM-demodulator



Pin 20: De-emphasis amplifier output



Pin 21: De-emphasis amplifier output

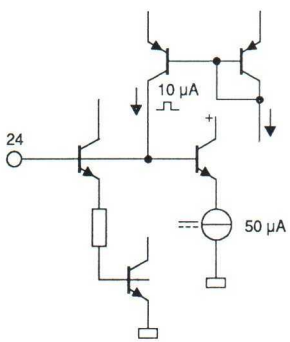


Pins 22 and 23: De-emphasis amplifier inputs

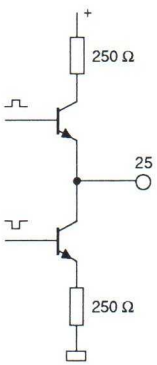
MEH024

Fig.3(b) Internal circuits; (continued from Fig.3(a)).

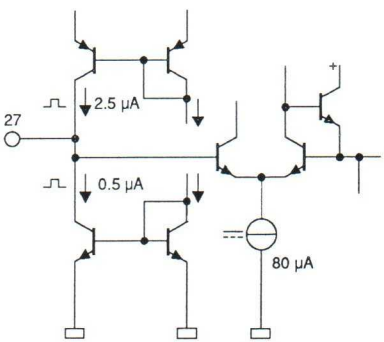
APPLICATION INFORMATION (continued)



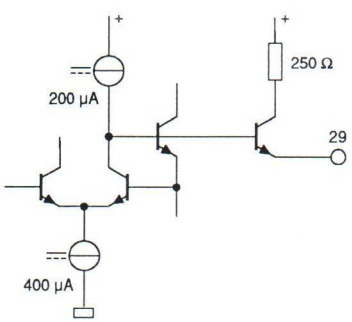
Pins 24, 26 or 32: AGC control input



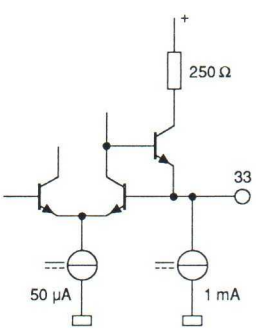
Pin 25: Data slicer output



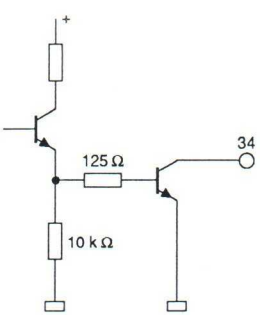
Pins 27 or 31: Video input



Pin 29: Video output



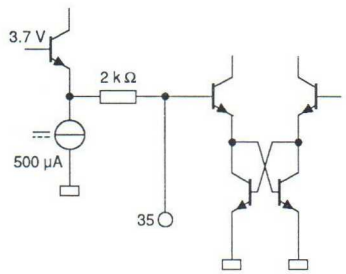
Pin 33: Video output



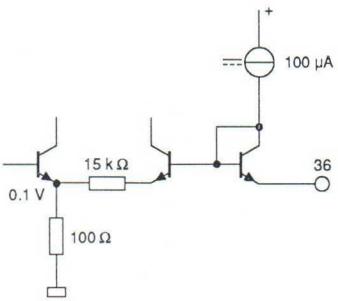
Pin 34: PAL/NTSC switch

MEH025

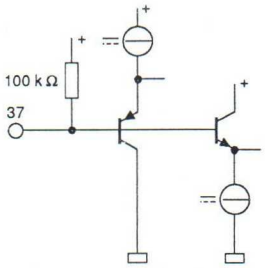
Fig.3(c) Internal circuits; (continued from Fig.3(b)).



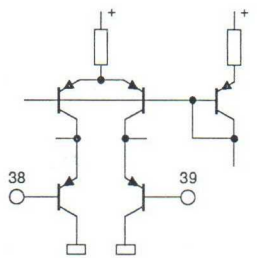
Pin 35: Input of noise reduction circuit



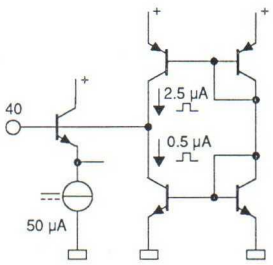
Pin 36: Noise reduction adjust



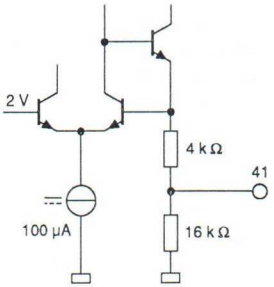
Pin 37: PAL/NTSC select



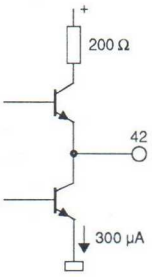
Pins 38 and 39: Insertion and video attenuation inputs



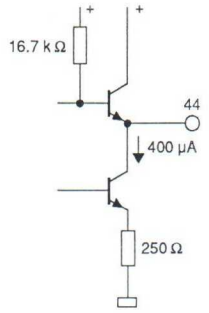
Pin 40: Video input



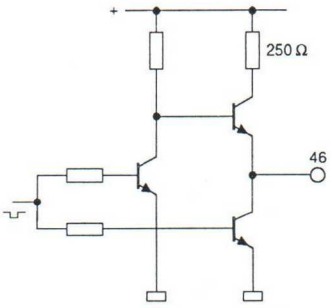
Pin 41: Reference voltage output



Pin 42: Video output



Pins 44 or 48: Chroma output
(Pin 45: Go to pin 1)



Pin 46: Output of second sync separator

MEH026

Fig.3(d) Internal circuits; (continued from Fig.3(c)).

2.5 GHz bi-directional I²C-bus controlled synthesizer

TSA5055T

GENERAL DESCRIPTION

The TSA5055T is a single chip PLL frequency synthesizer designed for satellite TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the six output ports and set the charge-pump current. Four of these ports can also be used as input ports (3 general purpose I/O ports, one A/D converter). Digital information concerning these ports can be read out of the TSA5055T on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage to port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 2.5 GHz single-chip system
- Low power 5 V, 60 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- 5-level A/D converter
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 6 controllable outputs, 4 bi-directional
- Power-down flag
- Available in SOT109A package

APPLICATIONS

- Satellite TV
- High IF cable tuning systems



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5	5.5	V
I_{CC}	supply current	–	60	80	mA
Δf	frequency range	1	–	2.5	GHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	1 GHz to 1.8 GHz	50	–	300	mV
	1.8 GHz to 2.6 GHz	70	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current				
	P7, P6, P5, P4	–	–	10	mA
	output current				
	P3, P0	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	70	°C
T_{stg}	storage temperature range	–40	–	125	°C
$R_{th\ j\text{-}a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5055T	16	SO	plastic	SOT109A

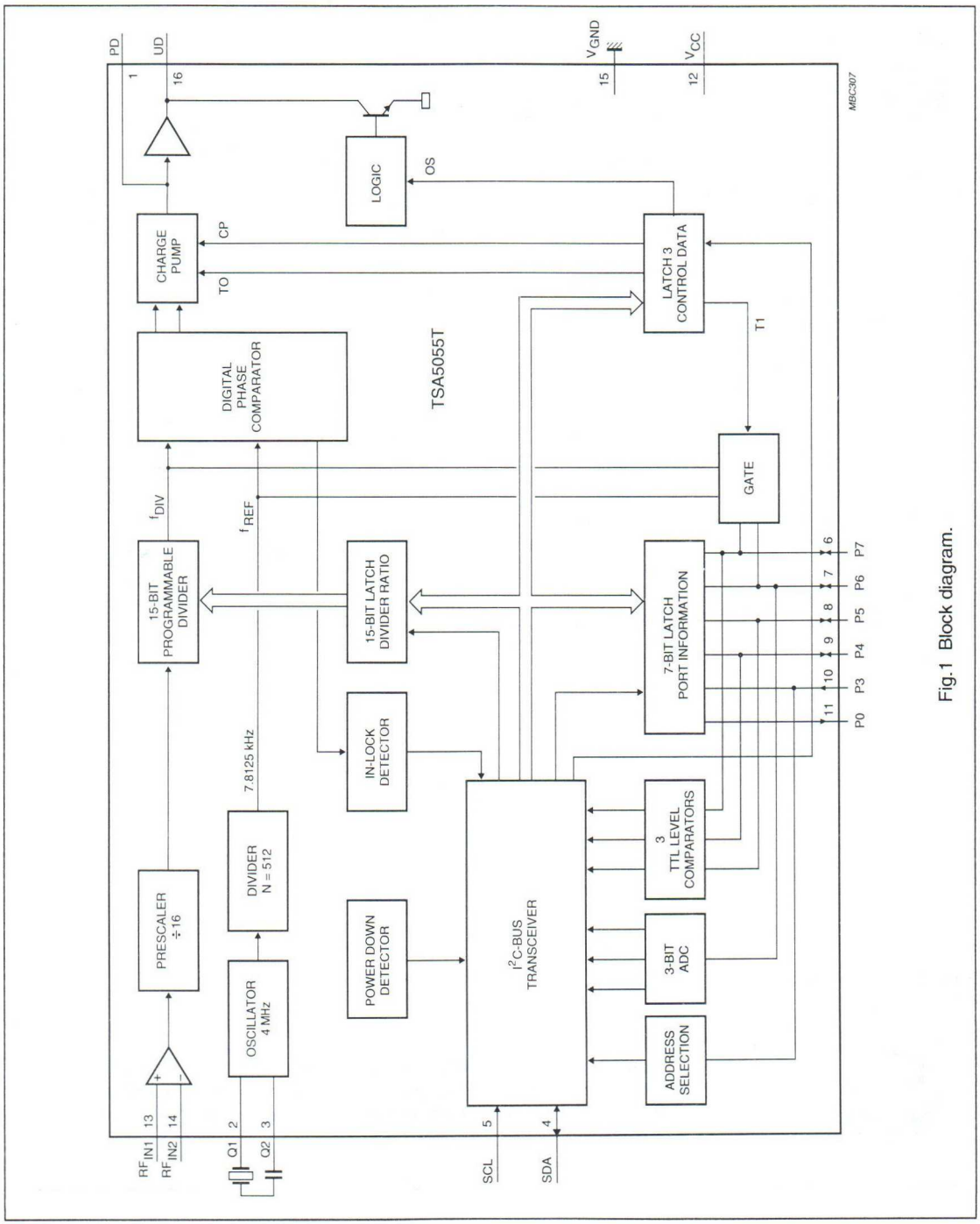


Fig.1 Block diagram.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P6}	input/output ports P7 - P0	−3	16	V
V_{P13}	prescaler inputs	−0.3	2.5	V
V_{P16}	drive output	−0.3	V_{CC}	V
I_{6L}	output ports P7 - P4 (open collector)	−1	15	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (1000 V).

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output/input (general purpose)
P6	7	port output/input (A/D converter)
P5	8	port output/input (general purpose)
P4	9	port output/input (general purpose)
P3	10	port output/input (address selection)
P0	11	port output
V_{CC}	12	voltage supply
RF_{IN1}	13	UHF/VHF signal input 1
RF_{IN2}	14	UHF/VHF signal input 2 (decoupled)
GND	15	ground
UD	16	drive output

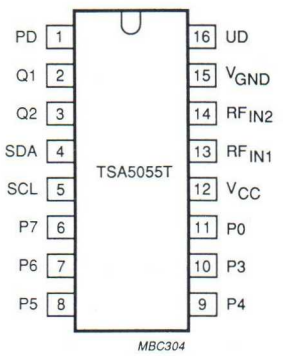


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TSA5055T is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode :
R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5055T. The bus transceiver has an auto-increment facility that permits the programming of the TSA5055T within one single transmission (address + 4 data bytes).

The TSA5055T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 16, the step size is 125 kHz. A 3.2 MHz crystal can offer a step size of 100 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	X	X	P0	A	byte 5

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7 - P4 = 1 open-collector outputs are active

P7 - P0 = 0 outputs are in high impedance state

P3 - P0 = 1 current-limited outputs are active

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

X don't care.

READ mode :

R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5055T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5055T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5055T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.The TSA5055T will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5055T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

The I2, I1 and I0 bits represent the status of the I/O ports P7, P5 and P4 respectively. A logic '0' indicates a low level and a logic '1' a high level (TTL levels). A built-in 5-level A/D converter is available at I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television, as shown in Fig. 3. The relationship between bits A2, A1, A0 and the input voltage at port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I1	I1	I0	A2	A1	A0	–	byte 2

POR power-on-reset flag. (POR = 1 on power-on)

FL in-lock flag (FL = 1 when the loop is phase-locked).

I2, I1, I0 digital information for I/O ports P7, P5 and P4 respectively

A2, A1, A0 digital outputs of the 5-level A/D converter. Accuracy is ½ LSB (see Table 3).

MSB is transmitted first.

Address selection (see Table 4)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 3) in one system. The relationship between MA1 and MA0 and the input voltage at port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on port P6	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 $_{CC}$	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

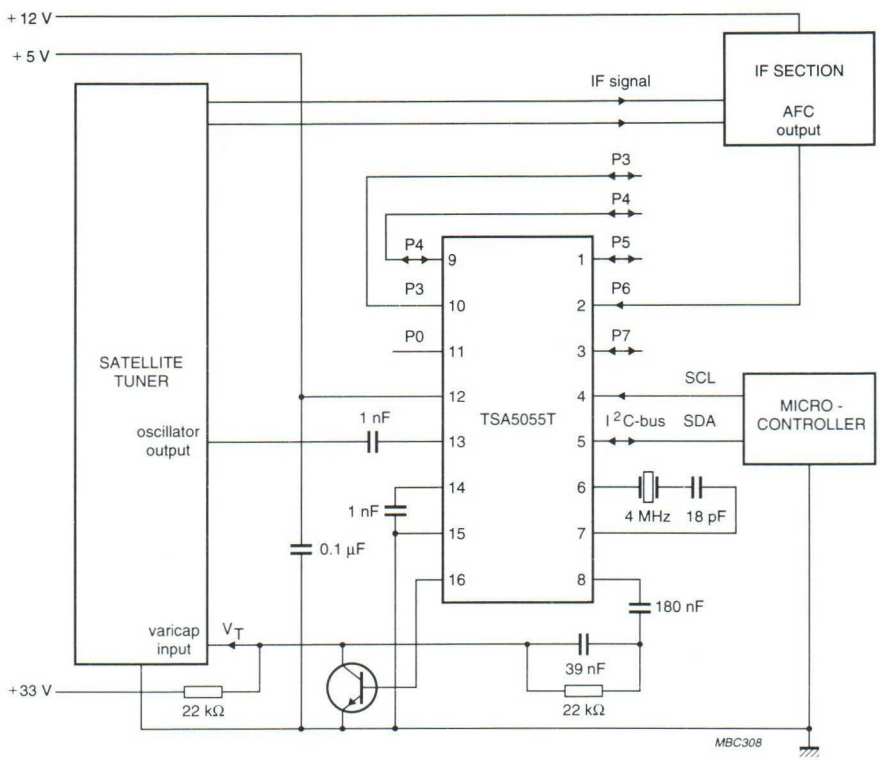


Fig.3 Typical application diagram.

CHARACTERISTICS

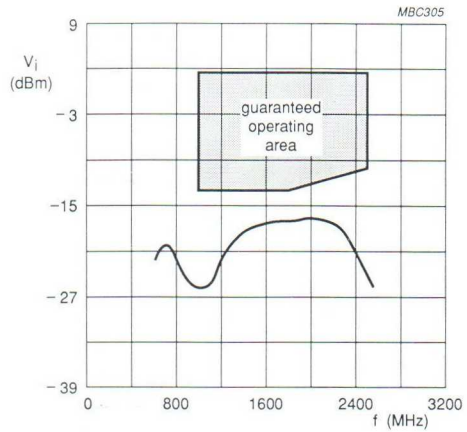
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.75	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	70	°C
f_{RF}	RF input frequency range		1	–	2.5	GHz
N	divider		256	–	32767	
I_{CC}	supply current		–	60	80	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
$V_{I\ (RMS)}$	input voltage level (RMS value) f = 1 to 1.8 GHz f = 1.8 to 2.5 GHz	V_{CC} = 4.75 to 5.5 V; T_{amb} = –10 to 70 °C see typical sensitivity curve in Fig. 4	 50/–13 70/–10	 – –	 300/2.6 300/2.6	 mV mV
R_I	prescaler input impedance	see Smith chart in Fig. 5	–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports P3, P0 (current limited)						
I_{LO}	leakage current	V_{10H} = 13.5 V	–	–	10	µA
I_{OS}	output sink current	V_{10} = 13.5 V	0.7	1	1.5	mA
Output ports P7 to P4 (open collector) (see note 1)						
I_{LO}	leakage current	V_{6H} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_{6L} = 10 mA note 2	–	–	0.7	V
Input ports P6, P3						
I_{IH}	input current HIGH	V_{7H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{7L} = 0	–10	–	–	µA
Input ports P7, P5, P4						
V_{IH}	input voltage HIGH		2.7	–	–	V
V_{IL}	input voltage LOW		–	–	0.8	V
I_{IH}	input current HIGH	V_{6H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{6L} = 0	–10	–	–	µA
Bus inputs SCL, SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{5H} = 5 V; V_{CC} = 0	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bus inputs SCL, SDA						
I_{IL}	input current LOW	V_{5H} = 5 V; V_{CC} = 5 V	–	–	10	µA
		V_{5L} = 0; V_{CC} = 0	–10	–	–	µA
		V_{5L} = 0; V_{CC} = 5 V	–10	–	–	µA
Output SDA (open collector)						
I_{4H}	leakage current	V_{4H} = 5.5 V	–	–	10	µA
V_{4L}	output voltage	I_{4L} = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{OH}	output current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{OL}	output current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{16}	output voltage	V_{IL} = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V_{IL} = 2 V	–	–	250	mV
h_{FE}	operational amplifier current gain $I_{16}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V_{IL} = 2 V; I_{16} = 10 µA	2000	–	–	

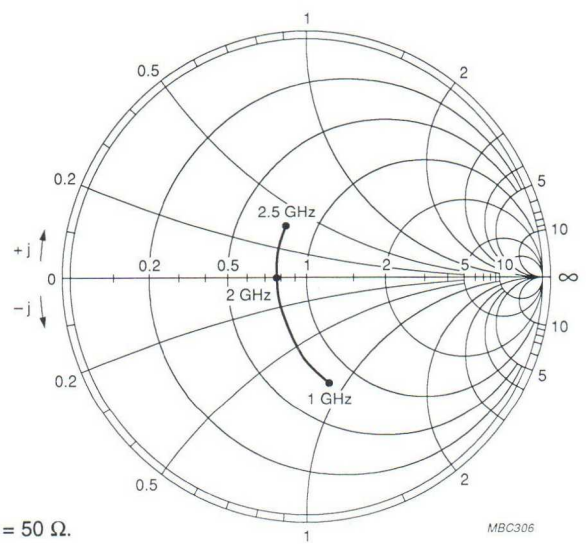
Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open collector active.



V_{CC} = 5 V; T_{amb} = 25 °C.

Fig.4 Prescaler typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.5 Prescaler Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

K_O = 4×10^6

C1 and C2 = loop filter capacitors.

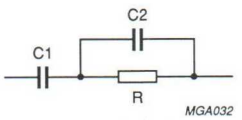


Fig.6 Loop filter.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	µs
Time span between the loop losing lock and FL-flag resetting	0	128	µs

FLOCK FLAG APPLICATION

- K_{VCO} = 50 MHz/V (UHF band)
- I_{CP} = 220 µA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ±85.8 kHz.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (3 addresses)
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 current limited outputs (1 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

GENERAL DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102
TSA5511T	16	SO	plastic	SOT109A
TSA5511AT	20	SO	plastic	SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open–collector output current	10	–	–	mA
I_O	current–limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

Fig.1 Block diagram.

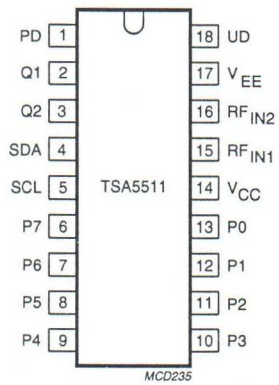


Fig.2 Pin configuration for SOT102.

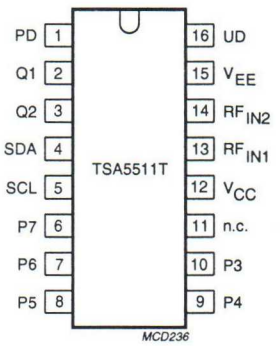


Fig.3 Pin configuration for SOT109.

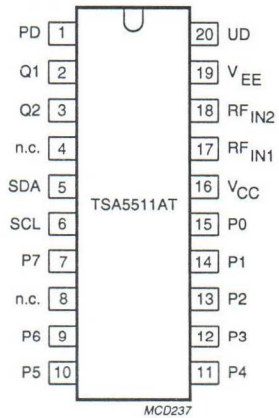


Fig.4 Pin configuration for SOT163.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	–	13	port output
n.c.	–	11	–	not connected
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5511 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5511. The bus transceiver has an auto-increment facility which permits the programming of the TSA5511 within one single transmission (address + 4 data bytes).

The TSA5511 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	byte 5

Note to Table 1

*	not valid for TSA5511T.
MA1, MA0	programmable address bits (see Table 4)
A	acknowledge bit
N14 to N0	programmable divider bits

$$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2^{1} + N0$$

CP	charge-pump current
CP = 0	50 μA
CP = 1	220 μA
P3 to P0 = 1	limited-current output is active
P7 to P4 = 1	open-collector output is active
P7 to P0 = 0	outputs are in high impedance state
T1, T0, OS = 0 0 0	normal operation
T1 = 1	P6 = f_{ref}, P7 = f_{DIV}
T0 = 1	3-state charge-pump
OS = 1	operational amplifier output is switched off (varicap drive disable)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5511 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5511 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5511 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5511 will then release the data line to allow the processor to generate a STOP condition.
When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.
The POR flag (power-on reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5511 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit (Fig.5). The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

Note to Table 2

POR	power-on reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 ADC levels

VOLTAGE APPLIED ON THE PORT P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	VOLTAGE APPLIED ON PORT P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); all pin numbers refer to DIL18 version

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output voltage	−0.3	6	V
V_5	serial clock input voltage	−0.3	6	V
$V_{6\text{-}13}$	P7 to P0 input/output voltage	−0.3	+16	V
V_{15}	prescaler input voltage	−0.3	V_{CC}	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
$I_{6\text{-}9}$	P7 to P4 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	IC storage temperature range	−40	+150	°C
T_j	maximum junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL18	80 K/W
	SO16	110 K/W
	SO20	80 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C, unless otherwise specified
All pin numbers refer to DIL18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	+80	°C
f	input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency range	crystal series resonance resistance ≤ 150 Ω	3.2	4.0	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to +80 °C; see typical sensitivity curve Fig.6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance (see Fig.7)		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (current-limited) P0 to P3						
I_{LO}	output leakage current	V_O = 13.5 V	–	–	10	µA
I_{sink}	output sink current	V_O = 12 V	0.7	1.0	1.5	mA
Output ports (open collector) P4 to P7 (see note 1)						
I_{LO}	output leakage current	V_O = 13.5 V	–	–	10	µA
V_{OL}	LOW level output voltage	I_{OL} = 10 mA; note 2	–	–	0.7	V
Input port P3						
I_{OH}	HIGH level input current	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	LOW level input current	V_{OL} = 0 V	–10	–	–	µA
Input ports P4, P5 and P7						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.7	–	–	V
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{CC} = 0 V	–	–	10	µA
		V_{IH} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC} = 0 V	–10	–	–	µA
		V_{IL} = 0 V; V_{CC} = 5 V	–10	–	–	µA
Output SDA (pin 4; open collector)						
I_{LO}	output leakage current	V_O = 5.5 V	–	–	10	µA
V_O	output voltage	I_O = 3 mA	–	–	0.4	V
Charge-pump output PD (pin 1)						
I_{OH}	HIGH level output current (absolute value)	CP = 1	90	220	300	µA
I_{OL}	LOW level output current (absolute value)	CP = 0	22	50	75	µA
V_1	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{IL} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

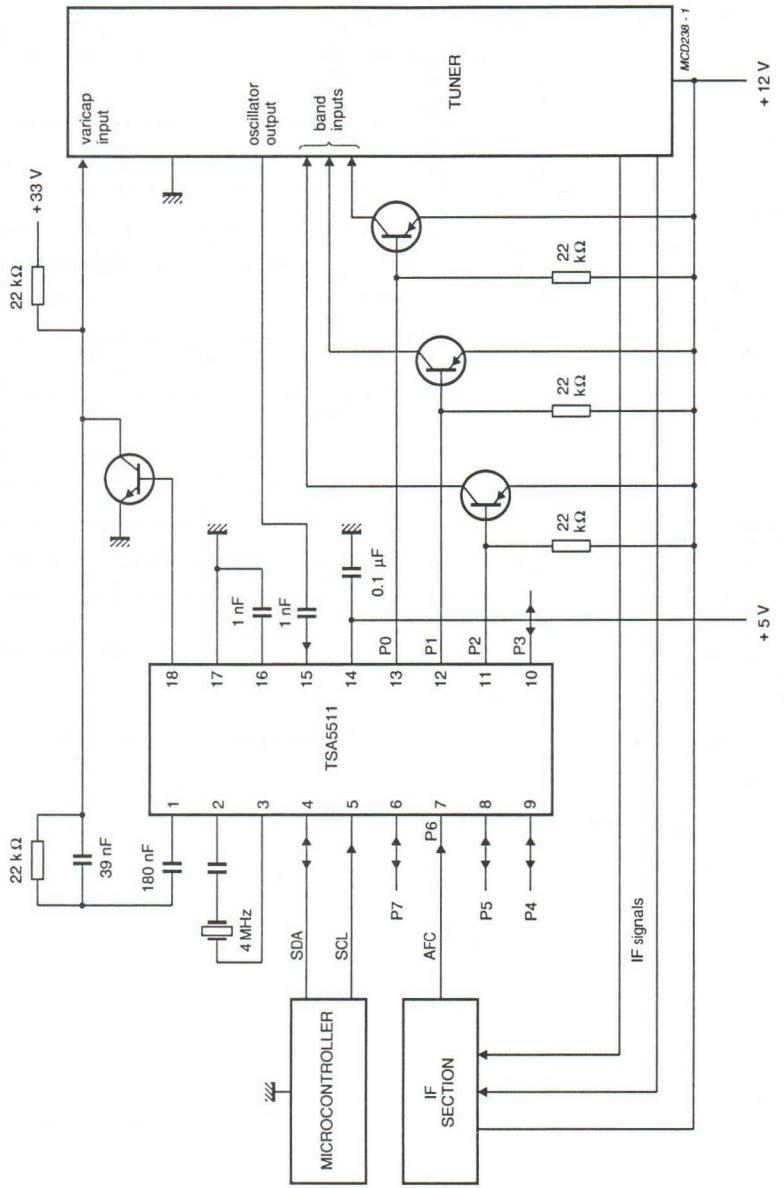


Fig.5 Typical application (DIL18).

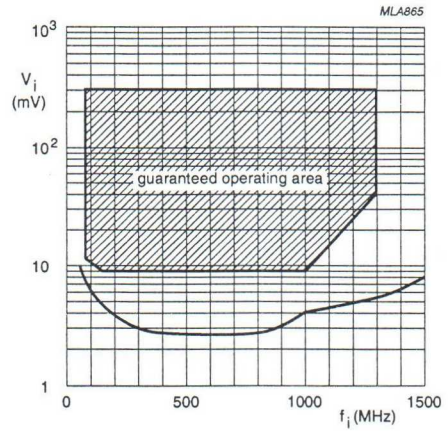


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

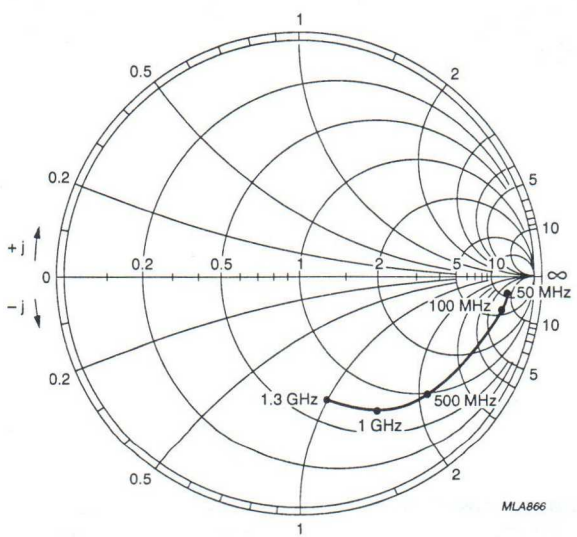


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

Where:

K_{VCO} = oscillator slope (Hz/V)
I_{CP} = charge-pump current (A)
K_O = 4 x 10E6
C1 and C2 = loop filter capacitors (see Fig.8)

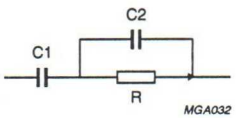


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5512

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (3 addresses)
- Analog-to-digital converter
- 8 bus controlled ports (6 for TSA5512T), 8 open collector outputs (4 bidirectional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5512 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5512 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δfr	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open–collector output current	5	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5512	18	DIL	plastic	SOT102
TSA5512T	16	SO	plastic	SOT109A
TSA5512AT	20	SO	plastic	SOT163A
TSA5512M	20	SSOP	plastic	SOT266

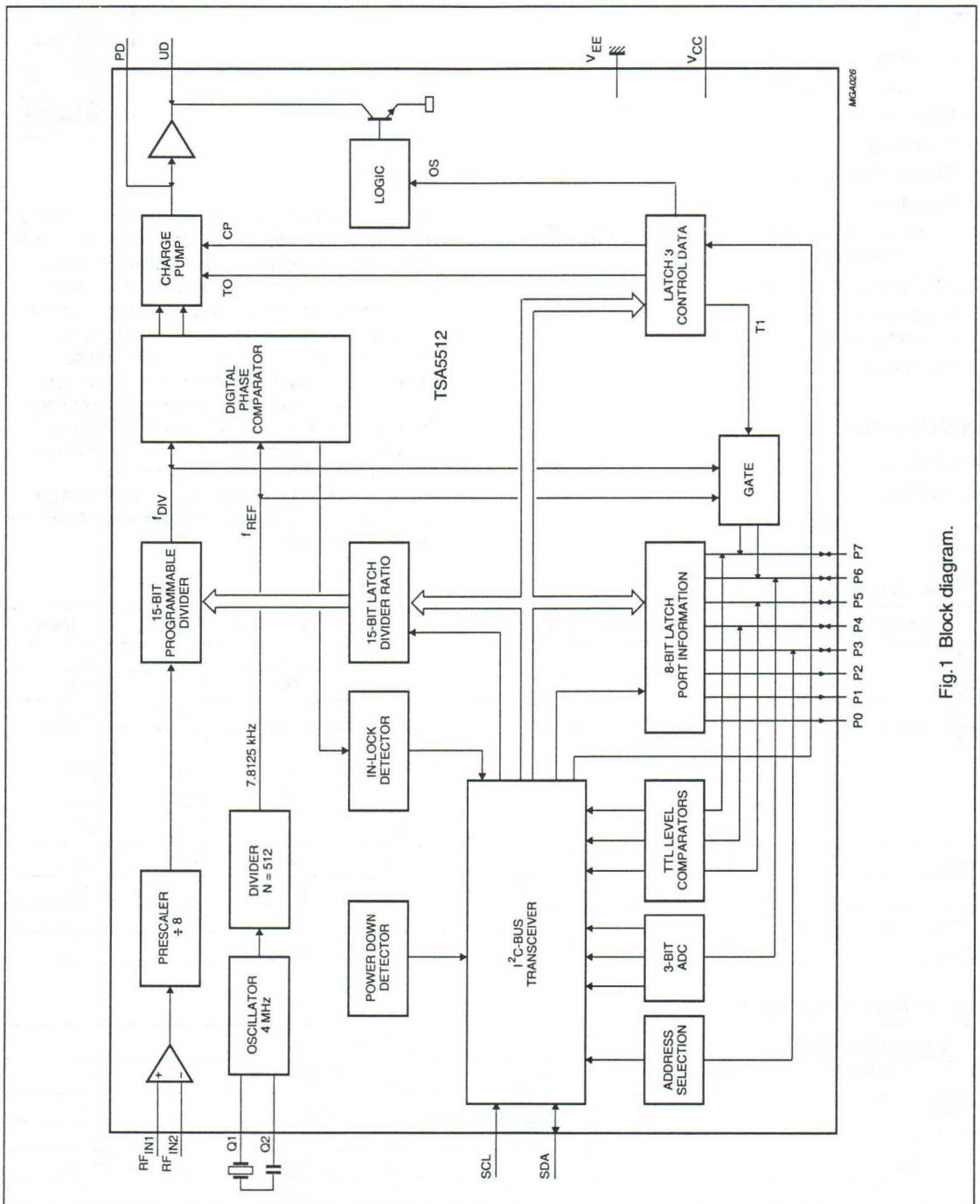


Fig.1 Block diagram.

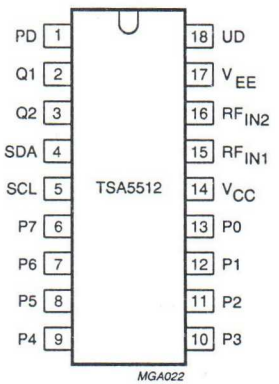


Fig.2 Pin configuration for SOT102.

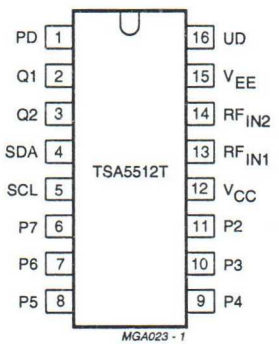


Fig.3 Pin configuration for SOT109.

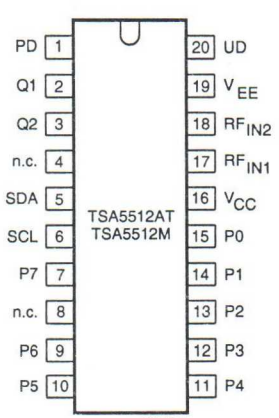


Fig.4 Pin configuration for SOT163/SOT266.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163 SOT266	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	11	13	port output
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5512 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5512. The bus transceiver has an auto-increment facility which permits the programming of the TSA5512 within one single transmission (address + 4 data bytes).

The TSA5512 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2	P1*	P0*	A	byte 5

Note to Table 1

*	not valid for TSA5512T.
MA1, MA0	programmable address bits (see Table 4)
A	acknowledge bit
N14 to N0	programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP	charge-pump current
CP = 0	50 µA
CP = 1	220 µA
P7 to P0 = 1	open-collector output is active
P7 to P0 = 0	outputs are in high impedance state
T1, T0, OS = 0 0 0	normal operation
T1 = 1	P6 = f_{ref}, P7 = f_{DIV}
T0 = 1	3-state charge-pump
OS = 1	operational amplifier output is switched off (varicap drive disable)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5512 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5512 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5512 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5512 will then release the data line to allow the processor to generate a STOP condition.
When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.
The POR flag (power-on reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5512 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit (Fig.8). The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

Note to Table 2

POR	power-on reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 ADC levels

VOLTAGE APPLIED ON THE PORT P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	VOLTAGE APPLIED ON PORT P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); all pin numbers refer to DIL18 version

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output voltage	−0.3	6	V
V_5	serial clock input voltage	−0.3	6	V
$V_{6\text{-}13}$	P7 to P0 input/output voltage	−0.3	+16	V
V_{15}	prescaler input voltage	−0.3	V_{CC}	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
$I_{6\text{-}13}$	P7 to P0 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	IC storage temperature range	−40	+150	°C
T_j	maximum junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL18	80 K/W
	SO16	110 K/W
	SO20	80 K/W
	SSOP20	120 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C, unless otherwise specified
All pin numbers refer to DIL18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	+80	°C
f	input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency range	crystal series resonance resistance ≤ 150 Ω	3.2	4.0	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to +80 °C; see typical sensitivity curve Fig.6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance (see Fig.7)		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (open collector) P0 to P7 (see note 1)						
I_{LO}	output leakage current	V_O = 13.5 V	–	–	10	µA
V_{OL}	LOW level output voltage	I_{OL} = 5 mA; note 2	–	–	0.7	V
Input port P3						
I_{OH}	HIGH level input current	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	LOW level input current	V_{OL} = 0 V	–10	–	–	µA
Input ports P4, P5 and P7						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.7	–	–	V
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
SCL and SDA inputs						
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
V_{IL}	LOW level input voltage		–	–	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{CC} = 0 V	–	–	10	µA
		V_{IH} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC} = 0 V	−10	–	–	µA
		V_{IL} = 0 V; V_{CC} = 5 V	−10	–	–	µA
Output SDA (pin 4; open collector)						
I_{LO}	output leakage current	V_O = 5.5 V	–	–	10	µA
V_O	output voltage	I_O = 3 mA	–	–	0.4	V
Charge-pump output PD (pin 1)						
I_{OH}	HIGH level output current (absolute value)	CP = 1	90	220	300	µA
I_{OL}	LOW level output current (absolute value)	CP = 0	22	50	75	µA
V_1	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{IL} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with all open-collector ports active.

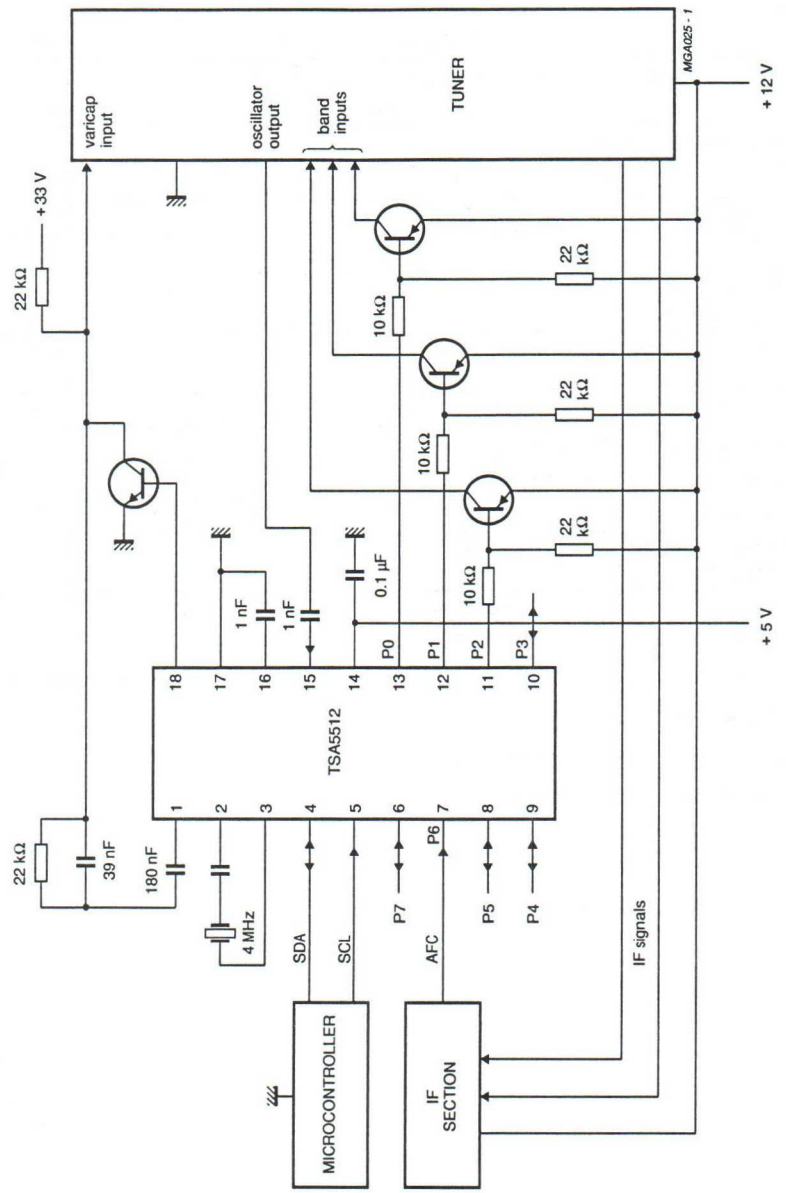


Fig.5 Typical application (DIL18).

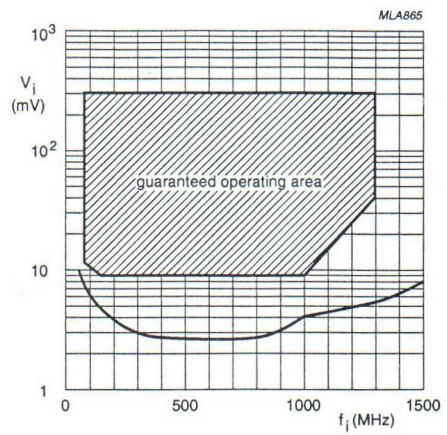


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

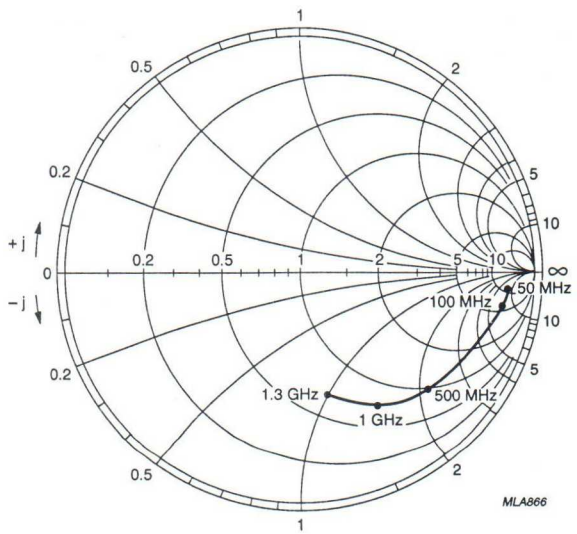


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

Where:

K_{VCO} = oscillator slope (Hz/V)
I_{CP} = charge-pump current (A)
K_O = 4 x 10E6
C1 and C2 = loop filter capacitors (see Fig.8)

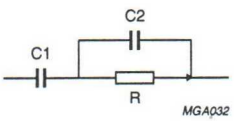


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5514

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (4 addresses)
- 5-level analog-to-digital converter
- 7 bus controlled ports; 3 output, 4 open collector input/output
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5514 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the seven output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5514 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage to AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δfr	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open–collector output current	10	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5514	18	DIL	plastic	SOT102
TSA5514T	16	SO	plastic	SOT109A
TSA5514AT	20	SO	plastic	SOT163A

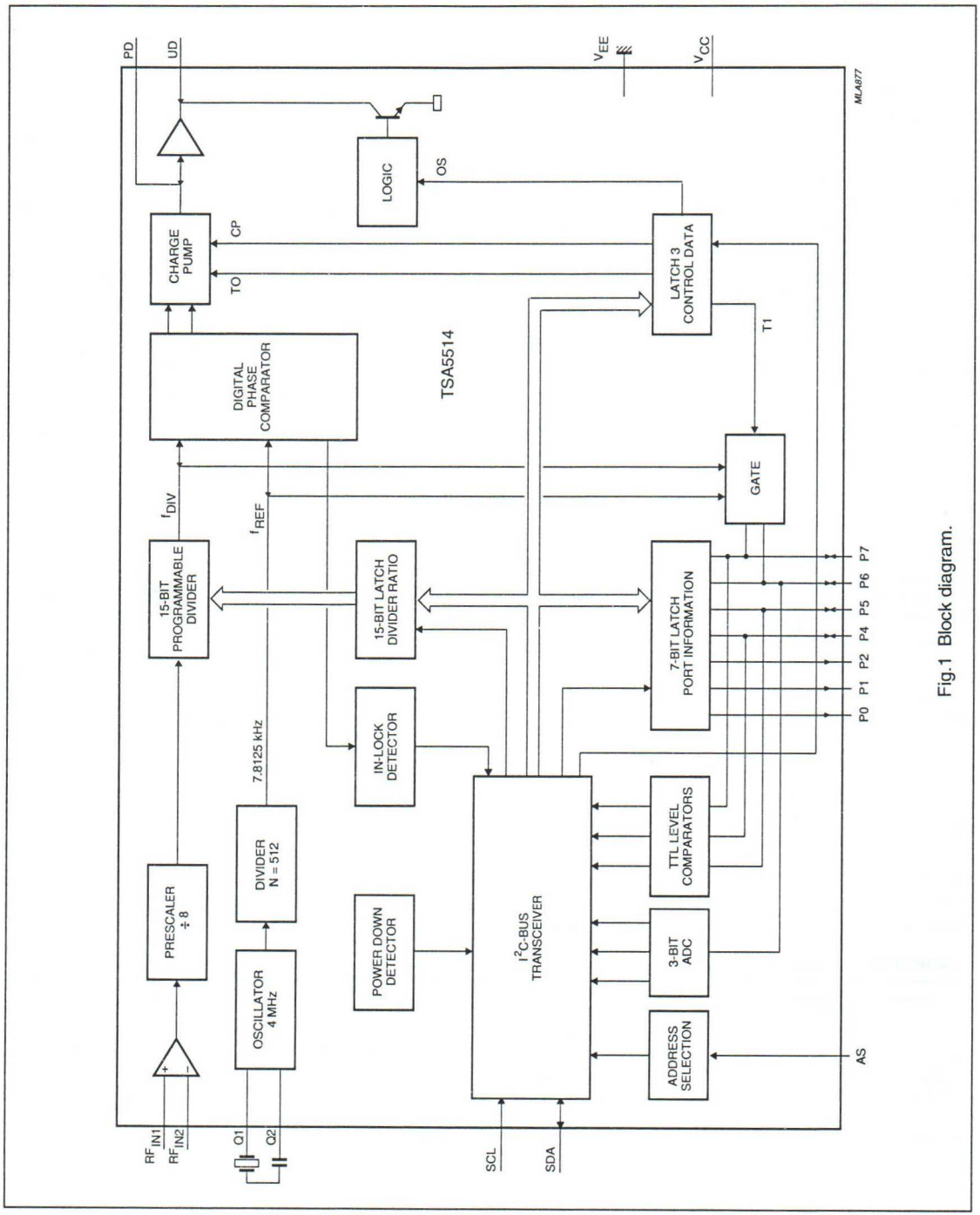


Fig.1 Block diagram.

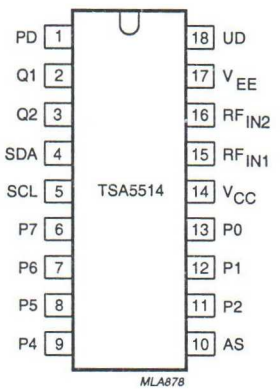


Fig.2 Pin configuration for SOT102.

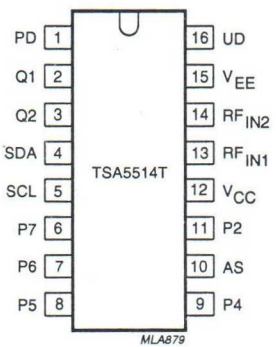


Fig.3 Pin configuration for SOT109.

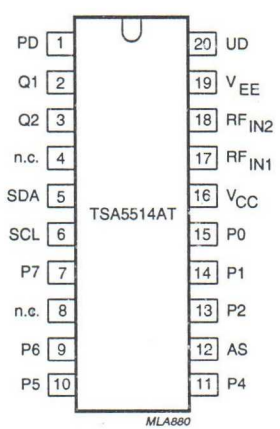


Fig.4 Pin configuration for SOT163.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
AS	10	10	12	address selection input
P2	11	11	13	port output
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5514 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5514. The bus transceiver has an auto-increment facility which permits the programming of the TSA5514 within one single transmission (address + 4 data bytes).

The TSA5514 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	x	x	x	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	x	P2	P1*	P0*	A	byte 5

Note to Table 1

*	Not valid for TSA5514T
MA1, MA0	programmable address bits (see Table 4)
A	acknowledge bit
N14 to N0	programmable divider bits

$$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2^{1} + N0$$

CP	charge-pump current
CP = 0	50 µA
CP = 1	220 µA
P7 to P0 = 1	open-collector output is active
P7 to P0 = 0	outputs are in high impedance state
T1, T0, OS = 0 0 0	normal operation
T1 = 1	P6 = f_{ref}, P7 = f_{DIV}
T0 = 1	3-state charge-pump
OS = 1	operational amplifier output is switched off (varicap drive disable)

x = don't care

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5514 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5514 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5514 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5514 will then release the data line to allow the processor to generate a STOP condition.
When ports P4 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5514 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit (Fig.8). The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR	power-on reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system.
The relationship between MA1 and MA0 and the input voltage on AS pin is given in Table 4.

Table 3 ADC levels

VOLTAGE APPLIED ON THE PORT P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	VOLTAGE APPLIED ON PIN AS
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to V_{CC}

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); all pin numbers refer to DIL18 version

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output voltage	−0.3	6	V
V_5	serial clock input voltage	−0.3	6	V
V_{10}	address selection input voltage	−0.3	6	V
$V_{6\text{-}13}$	P7 to P0 input/output voltage	−0.3	+16	V
V_{15}	prescaler input voltage	−0.3	+2.5	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
$I_{6\text{-}13}$	P7 to P0 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	IC storage temperature range	−40	+150	°C
T_j	maximum junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL18	80 K/W
	SO16	110 K/W
	SO20	80 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C, unless otherwise specified
All pin numbers refer to DIL18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	+80	°C
f	input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency range	crystal series resonance resistance ≤ 150 Ω	3.2	4.0	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to +80 °C; see typical sensitivity curve Fig.6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance (see Fig.7)		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (open collector) P0 to P2; P4 to P7 (see note 1)						
I_{LO}	output leakage current	V_O = 13.5 V	–	–	10	µA
V_{OL}	LOW level output voltage	I_{OL} = 10 mA; note 2	–	–	0.7	V
Address selection input						
I_{OH}	HIGH level input current	V_{OH} = 5 V	–	–	20	µA
I_{OL}	LOW level input current	V_{OL} = 0 V	–20	–	–	µA
Input ports P4, P5 and P7						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.7	–	–	V
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
SCL and SDA inputs						
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
V_{IL}	LOW level input voltage		–	–	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{CC} = 0 V V_{IH} = 5 V; V_{CC} = 5 V	– –	– –	10 10	µA µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC} = 0 V V_{IL} = 0 V; V_{CC} = 5 V	–10 –10	– –	– –	µA µA
Output SDA (pin 4; open collector)						
I_{LO}	output leakage current	V_O = 5.5 V	–	–	10	µA
V_O	output voltage	I_O = 3 mA	–	–	0.4	V
Charge-pump output PD (pin 1)						
I_{OH}	HIGH level output current (absolute value)	CP = 1	90	220	300	µA
I_{OL}	LOW level output current (absolute value)	CP = 0	22	50	75	µA
V_1	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{IL} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

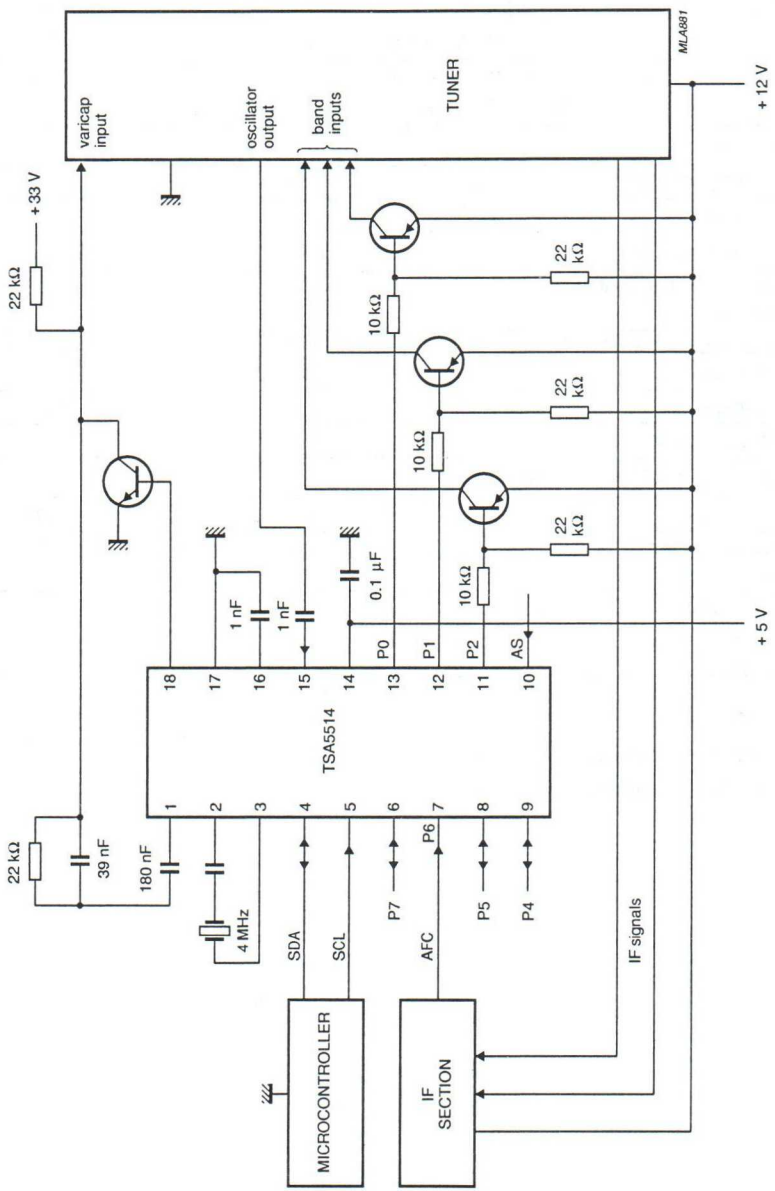


Fig.5 Typical application (DIL18).

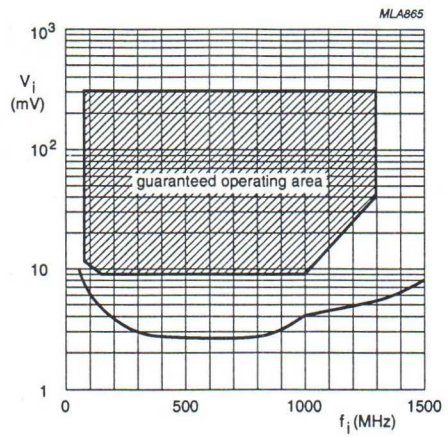


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

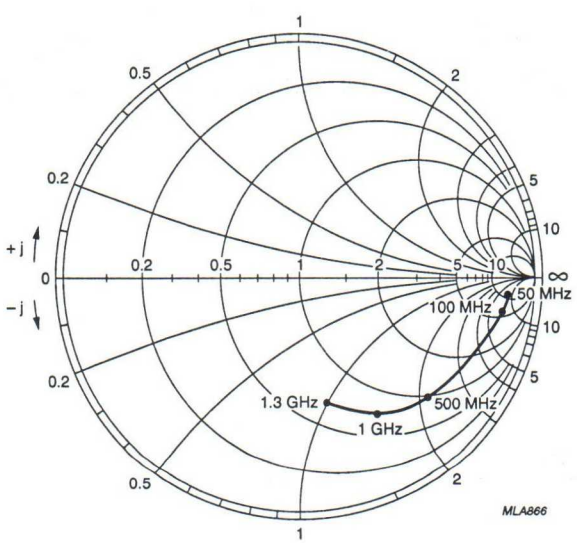


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

Where:

K_{VCO} = oscillator slope (Hz/V)
I_{CP} = charge-pump current (A)
K_O = 4 x 10E6
C1 and C2 = loop filter capacitors (see Fig.8)

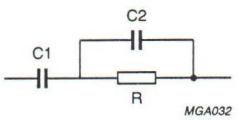


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

GENERAL DESCRIPTION

The TSA5515T is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the three output ports and set the charge-pump current. A flag is set when the loop is "in-lock". Another flag is set when a power dip occurs on the supply line. These flags are read out of the TSA5515T on SDA line (one status byte) during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage on the AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 1.3 GHz single-chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 3 bus-controlled output ports
- Power-down flag
- Available in SOT108A package

APPLICATIONS

- TV tuners
- VCR tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current				
	P7	–	–	5	mA
	P1, P2	–	–	20	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range	–40	–	125	°C
$R_{th\ j\text{-}a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5515T	14	SO	plastic	SOT108A

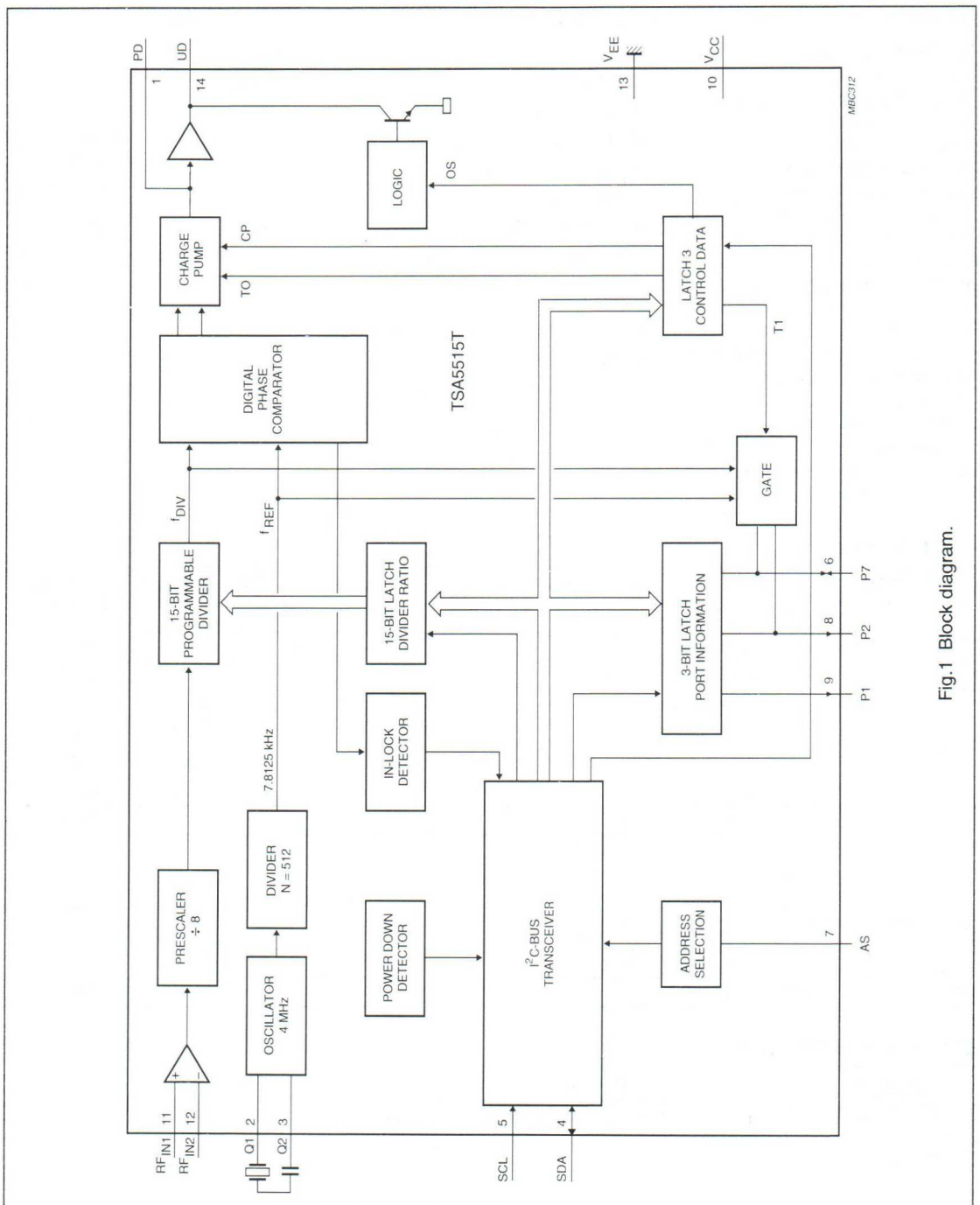


Fig.1 Block diagram.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P7}	address selection	−0.3	6	V
V_{P6}	output ports P7, P2, P1	−0.3	16	V
V_{P11}	prescaler inputs	−0.3	2.5	V
V_{P14}	drive output	−0.3	V_{CC}	V
I_{6L}	output port P7 (open collector)	−1	10	mA
I_{8L}	output port P2, P1 (open collector)	−1	25	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (> 1500 V).

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output
AS	7	input for address selection
P2	8	port output
P1	9	port output
V_{CC}	10	voltage supply
RF_{IN1}	11	UHF/VHF signal input 1
RF_{IN2}	12	UHF/VHF signal input 2 (decoupled)
GND	13	ground
UD	14	drive output

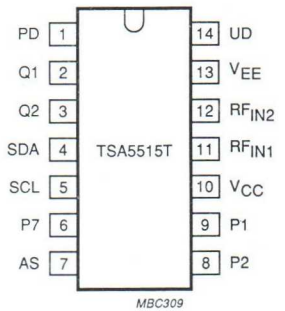


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TSA5515T is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode :
R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5515T. The bus transceiver has an auto-increment facility, which permits the programming of the TSA5515T within one single transmission (address + 4 data bytes).

The TSA5515T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 8, the step size is 62.5 kHz. A 3.2 MHz crystal can offer a step size of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	X	X	X	OS	A	byte 4
Output ports control bits	P7	X	X	X	X	P2	P1	X	A	byte 5

MA1, MA0 programmable address bits (see Table 3)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7, P2, P1 = 1 open-collector outputs are active

P7, P2, P1 = 0 outputs are in high impedance state

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P2 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

X don't care.

READ mode :
R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5515T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5515T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5515T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.The TSA5515T will then release the data line to allow the processor to generate a STOP condition.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5515T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	1	1	1	1	1	1	–	byte 2

POR power-on-reset flag. (POR = 1 on power-on)

FL in-lock flag (FL = 1 when the loop is phase-locked).

MSB is transmitted first.

Address selection (see Table 3)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 4) in one system. The relationship between MA1 and MA0 and the input voltage on AS input is given in Table 3.

Table 3 Address selection

MA1	MA0	Voltage applied on AS pin
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to V_{CC}

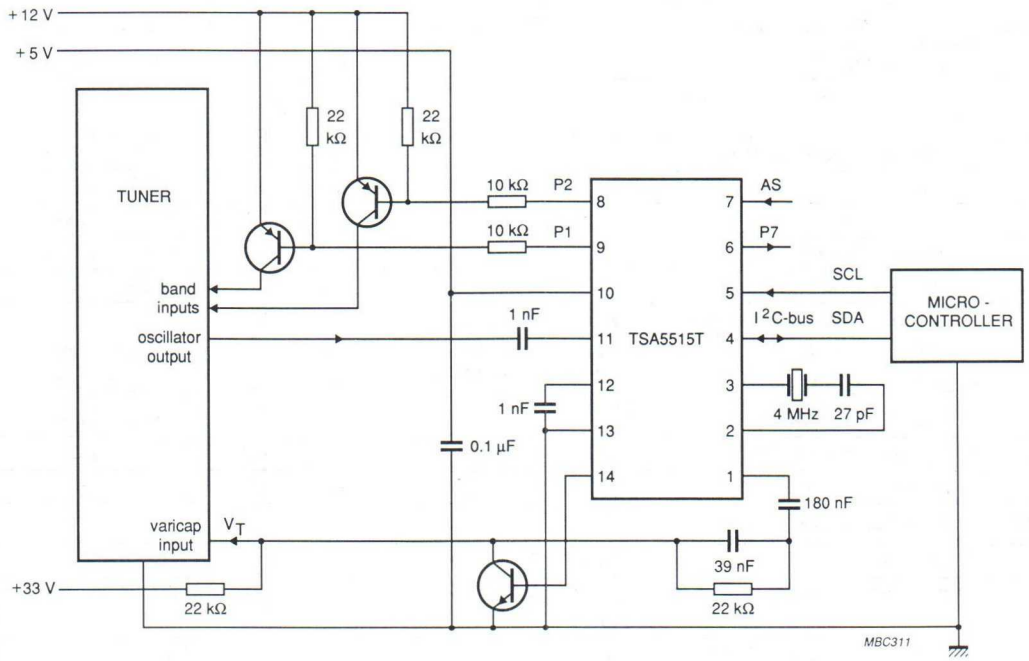


Fig.3 Typical application diagram.

CHARACTERISTICS

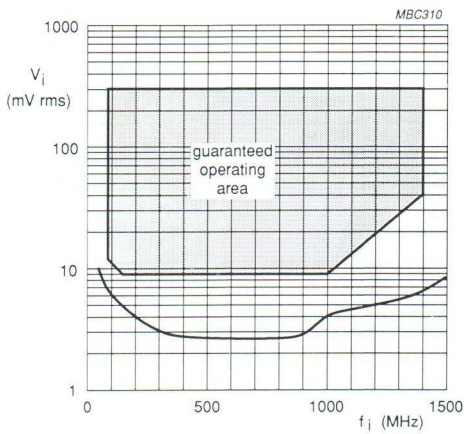
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		−10	–	80	°C
f_{CLK}	clock input frequency range		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		−480	−400	−320	Ω
$V_{I\ (RMS)}$	input voltage level (RMS value)	V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to 80 °C see typical sensitivity curve in Fig. 4				
	f = 80 to 150 MHz		12	–	300/2.6	mV
	f = 150 to 1000 MHz		9	–	300/2.6	mV
	f = 1000 to 1300 MHz		40	–	300/2.6	mV
R_I	prescaler input impedance	see Smith chart in Fig. 5	–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (open collector) (see note 1)						
I_{LO}	leakage current	V_{6H} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW (P7)	I_{6L} = 5 mA note 2	–	–	0.5	V
	output voltage LOW (P2, P1)	I_{8L} = 20 mA note 2	–	–	0.5	V
Address selection input (AS)						
I_{IH}	input current HIGH	V_{7H} = 5 V	–	–	20	µA
I_{IL}	input current LOW	V_{7L} = 0	−20	–	–	µA
Bus inputs SCL, SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{5H} = 5 V; V_{CC} = 0	–	–	10	µA
		V_{5H} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	input current LOW	V_{5L} = 0; V_{CC} = 0	−10	–	–	µA
		V_{5L} = 0; V_{CC} = 5 V	−10	–	–	µA
Output SDA (open collector)						
I_{LO}	leakage current	V_{4H} = 5.5 V	–	–	10	µA
V_{4L}	output voltage	I_{4L} = 3 mA	–	–	0.4	V
V_{14}	output voltage	V_{1L} = 0	–	–	100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{14}	output voltage	V_{1L} = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V_{1L} = 2 V	–	–	200	mV
h_{FE}	operational amplifier current gain $I_{14}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V_{1L} = 2 V; I_{14} = 10 µA	2000	–	–	

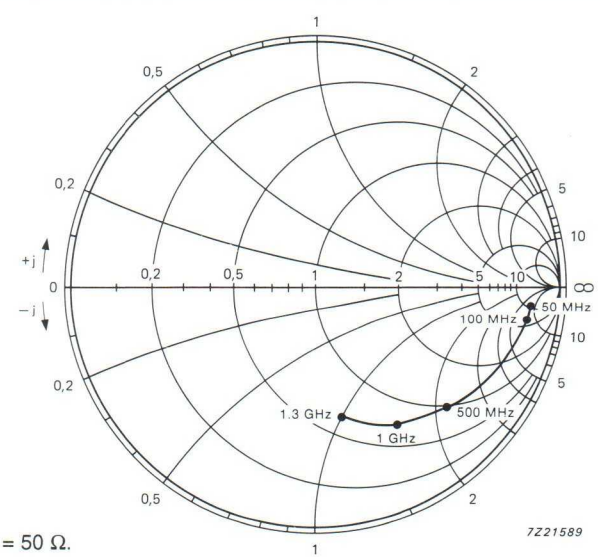
Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. A maximum of 1 port at the same time may sink 5 or 20 mA, to guarantee V_O = 0.5 V.



V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to 80 °C.

Fig.4 Prescaler typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.5 Prescaler Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)
I_{CP} = charge-pump current (A)
K_O = 4×10^6
C1 and C2 = loop filter capacitors.

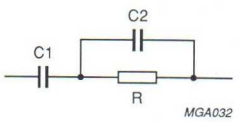


Fig.6 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ±27.5 kHz.

Table 4 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

1.3 GHz universal bus-controlled TV synthesizer

TSA5520; TSA5521

FEATURES

- Complete 1.3 GHz single chip system
- Four pnp band switch buffers (40 mA)
- 33 V output tuning voltage
- In-lock detector
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (60 or 280 μA)
- Varicap drive disable
- Universal bus protocol I^2C-bus or 3-wire bus (the TSA5520/5521 I^2C-bus mode only includes the write mode; if both read and write modes are required the TSA5526/5527 devices should be selected):
  - bus protocol for 18 or 19 bits transmission (3-wire bus)
  - extra protocol for 27 bits for test and features (3-wire bus)
  - address plus 4 data bytes transmission (I^2C-bus)
  - three independent I^2C-bus addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5520M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5520T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5521M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5521T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	20	25	mA
I_{CC2}	band switch supply current	note 1	–	50	55	mA
f_{RF}	RF input frequency		64	–	1300	MHz
$V_{i(RF)}$	RF input voltage	80 to 150 MHz	–25	–	3	dBm
		150 MHz to 1 GHz	–28	–	3	dBm
		1 to 1.3 GHz	–15	–	3	dBm
f_{xtal}	crystal oscillator input frequency		3.2	4.0	4.48	MHz
$I_{o(pnp)}$	pnp band switch buffers output current	note 2	4	–	50	mA
P_{tot}	total power dissipation	note 3	–	250	400	mW
T_{stg}	storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C

Notes

1. One band switch buffer ON with 40 mA.
2. One buffer ON, I_o = 40 mA; two buffers ON, maximum sum of I_o = 50 mA.
3. The power dissipation is calculated as follows:

$$P_D = V_{CC1} \times I_{CC1} + V_{CC2} \times (I_{CC2} - I_o) + I_o \times V_{CE(satpnp)} + (V33/2)^2/27\ k\Omega$$

GENERAL DESCRIPTION

The device is a single-chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier and the 33 V output. Four high-current pnp band switch buffers are provided for band switching. Two pnp buffers can be switched on simultaneously. The sum of the collector currents is limited to 50 mA.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz using a 4 MHz crystal.

The lock detector output is LOW when the PLL loop is locked. In the test mode, this output is used as a TEST output for f_{ref} and $1/2f_{div}$ (see Table 6). The device can be controlled in accordance with the I²C-bus format or the 3-wire bus format depending on the voltage applied to the SW input (see Table 2).

I²C-bus format (SW = GND)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four pnp band switch buffers, set the charge-pump current and the reference divider ratio.

The device has three independent I²C-bus addresses which can be selected by applying a specific voltage on the CE input (see Table 4). The general address C2 is always valid. When the I²C-bus format is fully used, TSA5520 and TSA5521 are equal.

3-wire bus format (SW = V_{CC1} or open-circuit)

Data is transmitted to the device during a HIGH level on the CE input (enable line pin 15). The device is compatible with 18-bit and 19-bit data formats. The first four bits are used to program the pnp band switch buffers and the remaining bits are used to control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes. The difference between TSA5520 and TSA5521 are given in Table 1.

When the 27-bit format is used, the TSA5520/TSA5521 are equal and the reference divider is controlled by the RSA and RSB bits (see Table 7). More details are given in the functional description (3-wire bus mode).

Table 1 Differences between TSA5520 and TSA5521

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER	FREQUENCY STEP (kHz)
TSA5520	18-bit	512(1)	62.5
TSA5520	19-bit	1024(1)	31.25
TSA5521	19-bit	640(2)	50

Notes

1. The selection of the reference divider is given by an automatic identification of the data word length.
2. The reference divider is set to 640 at power-on reset.

BLOCK DIAGRAM

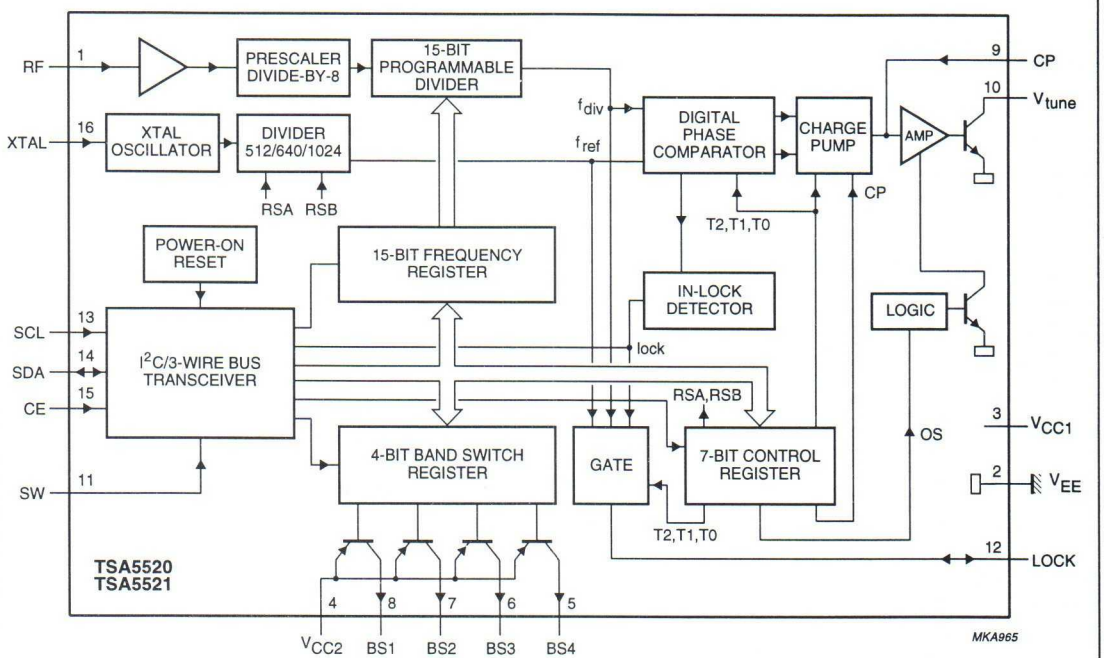


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RF	1	RF signal input
GND	2	ground
V_{CC1}	3	supply voltage (+5 V)
V_{CC2}	4	band switch supply voltage (+12 V)
BS4	5	pnp band switch buffer output 4
BS3	6	pnp band switch buffer output 3
BS2	7	pnp band switch buffer output 2
BS1	8	pnp band switch buffer output 1
CP	9	charge-pump output
V_{tune}	10	tuning voltage output
SW	11	bus format selection input, I²C-bus or 3-wire
LOCK	12	lock detector output
SCL	13	serial clock input
SDA	14	serial data input/output
CE	15	chip enable/address selection input
XTAL	16	crystal oscillator input

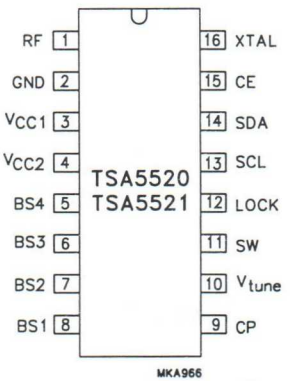


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The device is controlled via the I²C-bus or the 3-wire bus depending on the voltage applied to the SW input (pin 11). A HIGH level on the SW input enables the 3-wire bus inputs which are CE (Chip Enable), SDA (serial data input) and SCL (serial clock input). A LOW level on the SW input enables the I²C-bus inputs which are AS (address selection input), SDA (serial data input/output) and SCL (serial clock input). The bus format selection is given in Table 2.

I²C-bus mode (SW = GND); see Table 3

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are required to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is divider byte 1 (DB1) or the control byte (CB). The bits in the data bytes are defined in Table 3.

The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and band switch data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2), the control register is loaded after the 8th clock pulse of the control byte (CB) and the band switch register is loaded after the 8th clock pulse of the band switch byte (BB).

I²C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 3) in one system by applying a specific voltage to the CE input.

The relationship between MA1 and MA0 and the input voltage applied to the CE input is given in Table 5.

Table 2 Bus format selection

PIN	NAME	3-WIRE BUS MODE	I²C BUS MODE
11	SW	OPEN or HIGH	LOW
13	SCL	clock input	SCL input
14	SDA	data input	SDA input/output
15	CE	chip enable input	address selection input

Table 3 I²C-bus data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band switch byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

Table 4 Description of Table 3

SYMBOL	DESCRIPTION
A	acknowledge
MA1 and MA0	programmable address bits (see Table 5)
N14 to N0	programmable divider bits; $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$
CP	charge-pump current; CP = 0 = 60 μA; CP = 1 = 280 μA
T2 to T0	test bits (see Table 6); for normal operation T2 = 0, T1 = 0 and T0 = 1
RSA and RSB	reference divider ratio select bits (see Table 7)
OS	tuning amplifier control bit; for normal operation OS = 0 and tuning voltage is ON; when OS = 1 tuning voltage is OFF (high impedance)
BS4 to BS1	pnp band switch buffers control bits; when BS_n = 0 buffer n is OFF; when BS_n = 1 buffer n is ON
X	don't care

Table 5 I²C-bus address selection

VOLTAGE APPLIED TO THE CE INPUT (SW = GND)	MA1	MA0
0 to $0.1V_{CC1}$	0	0
Always valid	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

3-wire bus mode (SW = open-circuit or V_{CC1}); see Figs 3, 4 and 5

During a HIGH level on the CE input, the data is clocked into the data register at the HIGH-to-LOW transition of the clock pulse. The first four bits control the band switch buffers and are loaded into the internal band switch register on the 5th rising edge of the clock pulse. The frequency bits are loaded into the frequency register at the HIGH-to-LOW transition of the chip enable line when an 18-bit or 19-bit data word is transmitted.

At power-on the charge-pump current is set to 280 μA, the tuning voltage output is disabled (V_{tune} = 33 V in application; see Fig.12), the test bits T2, T1 and T0 are set to the normal mode and RSB is set to 1 (TSA5520) or 0 (TSA5521). When an 18-bit data word is transmitted, the most significant bit of the divider N14 is internally set to 0 and bit RSA is set to 1. When a 19-bit data word is transmitted, bit RSA is set to 0.

When a 27-bit word is transmitted, the frequency bits are loaded into the frequency register on the 20th rising edge of the clock pulse and the control bits at the HIGH-to-LOW transition of the chip enable line. In this mode, the reference divider is given by the RSA and RSB bits (see Table 7). The test bits T2, T1 and T0, the charge-pump bit CP, the ratio select bit RSB and the OS bit can only be selected or changed with a 27-bit transmission. They remain programmed if an 18-bit or a 19-bit transmission occurs. Only RSA is controlled by the transmission length when the 18-bit or 19-bit format is used.

A data word of less than 18 bits will not affect the frequency register of the device. The definition of the bits is unchanged compared to the I^2C bus mode.

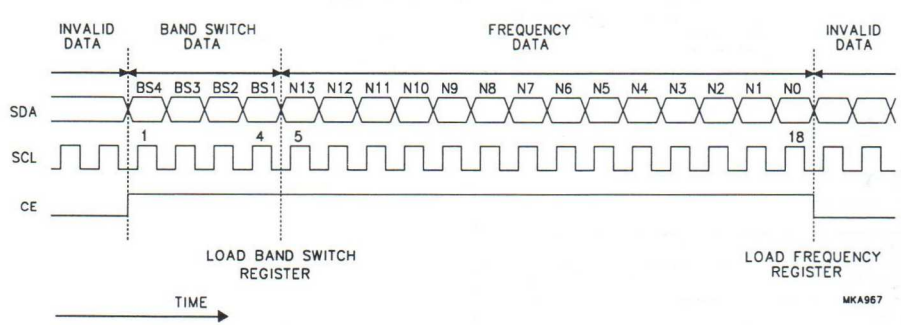
The power-on detection threshold voltage V_{POR} is fixed to V_{CC1} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state described above.

Table 6 Test bits

T2	T1	T0	DEVICE OPERATION
0	0	1	normal mode
0	1	X	charge-pump is OFF
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f_{ref} is available at LOCK output
1	0	1	$\frac{1}{2}f_{div}$ is available at LOCK output

Table 7 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

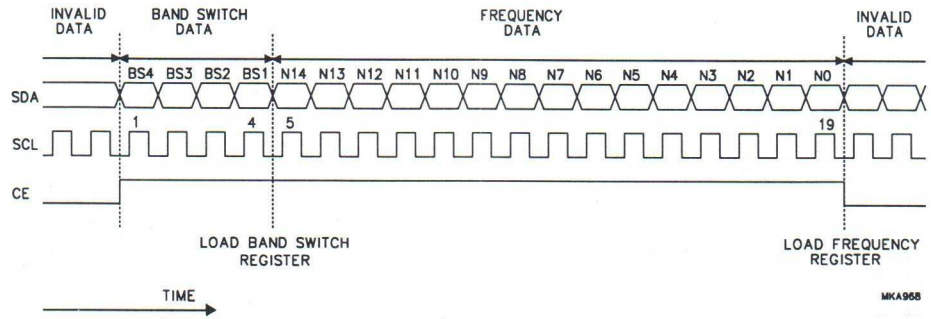


For TSA5520 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5521 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5520/TSA5521 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.3 Normal mode; 18-bit data format (RSA = 1).

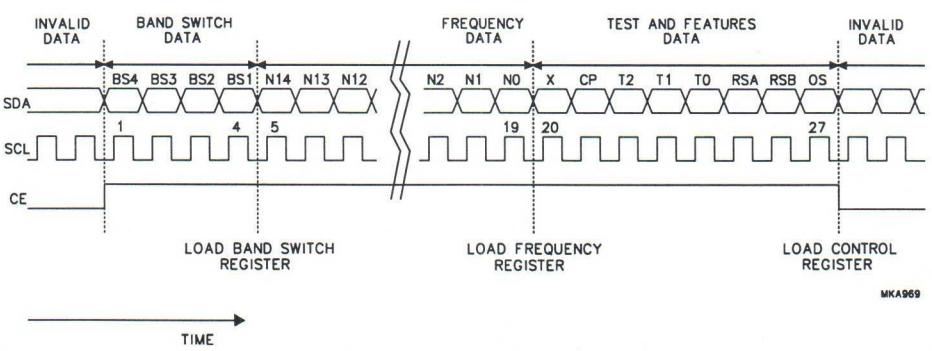


For TSA5520 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5521 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5520/TSA5521 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.4 Normal mode; 19-bit data format (RSA = 0).



For TSA5520 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5521 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5520/TSA5521 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.5 Test and features mode; 27-bit data format.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC1}	supply voltage; +5 V (pin 3)		−0.3	6.0	V
V_{CC2}	band switch supply voltage; +12 V (pin 4)		−0.3	16	V
$V_{i(RF)}$	prescaler input voltage		−0.3	V_{CC1}	V
$V_{o(BSn)}$	band switch buffers output voltage (pins 5 to 8)		−0.3	V_{CC2}	V
$I_{o(BSn)}$	band switch buffers output current		−1	50	mA
$V_{o(CP)}$	charge-pump output voltage (pin 9)		−0.3	V_{CC1}	V
$V_{o(tune)}$	output tuning voltage (pin 10)		−0.3	35	V
$V_{i(SW)}$	input switching voltage (pin 11)		−0.3	V_{CC1}	V
$V_{o(LOCK)}$	lock output voltage (pin 12)		−0.3	V_{CC1}	V
$V_{i(SCL)}$	serial clock input voltage (pin 13)		−0.3	6.0	V
$V_{i/o(SDA)}$	serial data input/output voltage (pin 14)		−0.3	6.0	V
$I_{o(SDA)}$	serial data output current		−1	10	mA
$V_{i(CE)}$	chip enable input voltage (pin 15)		−0.3	6.0	V
$V_{i(xtal)}$	crystal oscillator input voltage (pin 16)		−0.3	V_{CC1}	V
T_{stg}	storage temperature		−40	+150	°C
T_j	maximum junction temperature		−	+150	°C
t_{sc}	short-circuit time; every pin except pin 4 to pin 3 and every pin to pin 2	note 1	−	10	s

Note

1. Short-circuit between V_{CC1} and V_{CC2} is allowed provided the voltage applied to V_{CC2} is less than the 6 V maximum rating at V_{CC1}.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO16	110	K/W
	SSOP16	142	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices. Every pin withstands the ESD test in accordance with MIL-STD-883C category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; V_{CC2} = V_{CC1} to 13.2 V; T_{amb} = –20 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC1}	supply voltage		4.5	–	5.5	V
V_{CC2}	band switch buffers supply voltage		V_{CC1}	12	13.5	V
I_{CC1}	supply current	at power-on	–	20	25	mA
I_{CC2}	band switch buffers supply current	at power-on	–	0.5	1	mA
		one band switch buffer is ON; I_{source} = 40 mA	–	50	55	mA
		two band switch buffers are ON; I_{source} = 40 mA + 5 mA (any combination)	–	56	62	mA
V_{POR}	supply voltage below which POR is active		1.5	2.0	–	V
f_{RF}	RF input frequency		64	–	1300	MHz
DR	divider ratio	15-bit frequency word	256	–	32767	
		14-bit frequency word	256	–	16383	
f_{xtal}	crystal oscillator input frequency	R_{xtal} = 25 to 200 Ω	3.2	4.0	4.48	MHz
Z_{xtal}	crystal oscillator input impedance (absolute value)	f_i = 4 MHz	600	1200	–	Ω
Prescaler (see Figs 6 and 7)						
$V_{i(RF)}$	RF input level	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
$Z_{i(RF)}$	input impedance	see Fig.7				
pnp band switch buffers outputs (pins 5 to 8)						
I_{LO}	output leakage current	V_{CC2} = 13.5 V; V_o = 0 V	–10	–	–	µA
$V_{o(sat)}$	output saturation voltage	I_{source} = 40 mA; $V_{o(sat)} = V_{CC2} - V_o$	–	0.2	0.4	V
LOCK output (pnp collector output)						
$I_{o(ool)}$	output current when out-of-lock	V_{CC1} = 5.5 V; V_o = 5.5 V	–	–	100	µA
$V_{osat(ool)}$	output saturation voltage when out-of-lock	I_{source} = 200 µA; $V_{o(sat)} = V_{CC1} - V_o$	–	0.4	0.8	V
$V_{o(LOCK)}$	LOCK output voltage		–	0.01	0.4	V
SW input (bus format input)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	V_{CC1}	V
I_{IH}	HIGH level input current	V_{SW} = V_{CC1}	–	–	10	µA
I_{IL}	LOW level input current	V_{SW} = 0 V	–100	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CE input (chip enable/address selection)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	5.5	V
I_{IH}	HIGH level input current	V_{CE} = 5.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{CE} = 0 V	–10	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	V_{BUS} = 5.5 V; V_{CC1} = 0 V	–	–	10	µA
		V_{BUS} = 5.5 V; V_{CC1} = 5.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{BUS} = 1.5 V; V_{CC1} = 0 V	–	–	10	µA
		V_{BUS} = 0 V; V_{CC1} = 5.5 V	–10	–	–	µA
f_{clk}	clock frequency		–	100	400	kHz
SDA outputs (I^2C-bus mode)						
I_{LO}	output leakage current	V_{SDA} = 5.5 V	–	–	10	µA
V_o	output voltage	I_{sink} = 3 mA	–	–	0.4	V
Charge-pump output CP						
$\|I_{ICPH}\|$	HIGH charge-pump current	CP = 1	–	280	–	µA
$\|I_{ICPL}\|$	LOW charge-pump current	CP = 0	–	60	–	µA
V_{CP}	output voltage	in-lock; T_{amb} = 25 °C	–	1.95	–	V
$I_{LI(off)}$	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
Tuning voltage output V_{tune}						
$I_{LO(off)}$	leakage current when switched-off	OS = 1; V_{tune} = 33 V	–	–	10	µA
V_o	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_L = 27 kΩ; V_{tune} = 33 V	0.2	–	32.7	V
3-wire bus timing (see Figs 6 and 7)						
t_{HIGH}	clock high time		2	–	–	µs
$t_{SU;DAT}$	data set-up time		2	–	–	µs
$t_{HD;DAT}$	data hold time		2	–	–	µs
$t_{SU;ENSCL}$	enable to clock set-up time		10	–	–	µs
$t_{HD;ENDAT}$	enable to data hold time		2	–	–	µs
t_{EN}	enable between two transmissions		10	–	–	µs
$t_{HD;ENSCL}$	enable to clock active edge hold time		6	–	–	µs

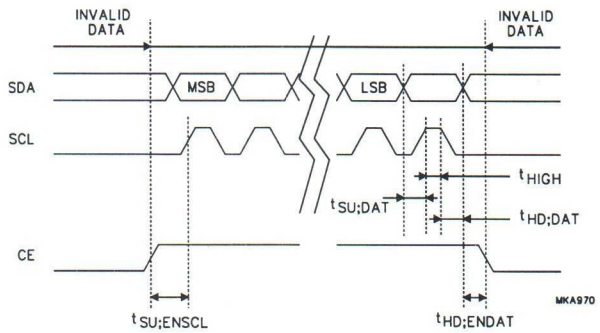


Fig.6 Timing diagram for 3-wire bus; SDA, SCL and CE.

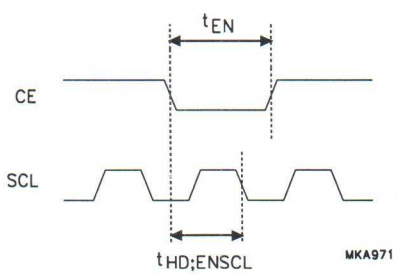


Fig.7 Timing diagram for 3-wire bus; CE and SCL.

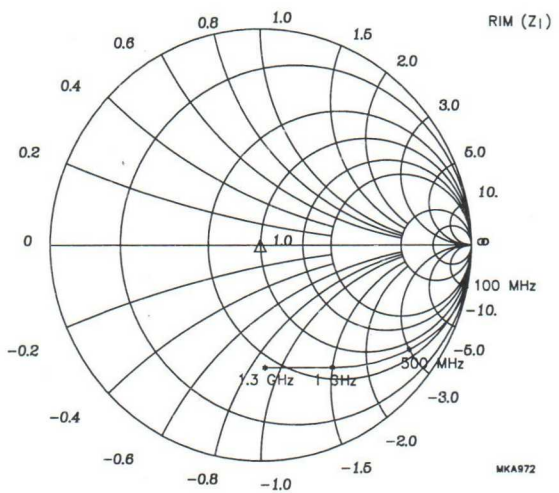


Fig.8 Prescaler Smith chart of typical input impedance at pin 1.

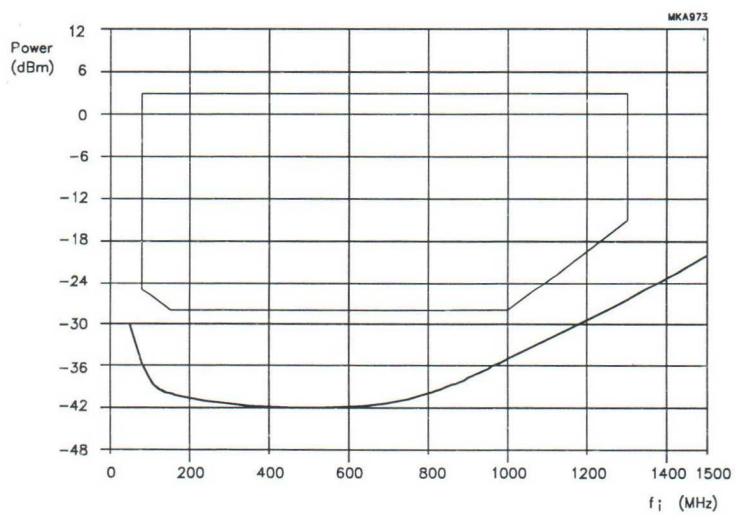


Fig.9 Prescaler typical input sensitivity curve.

INTERNAL PIN CONFIGURATION

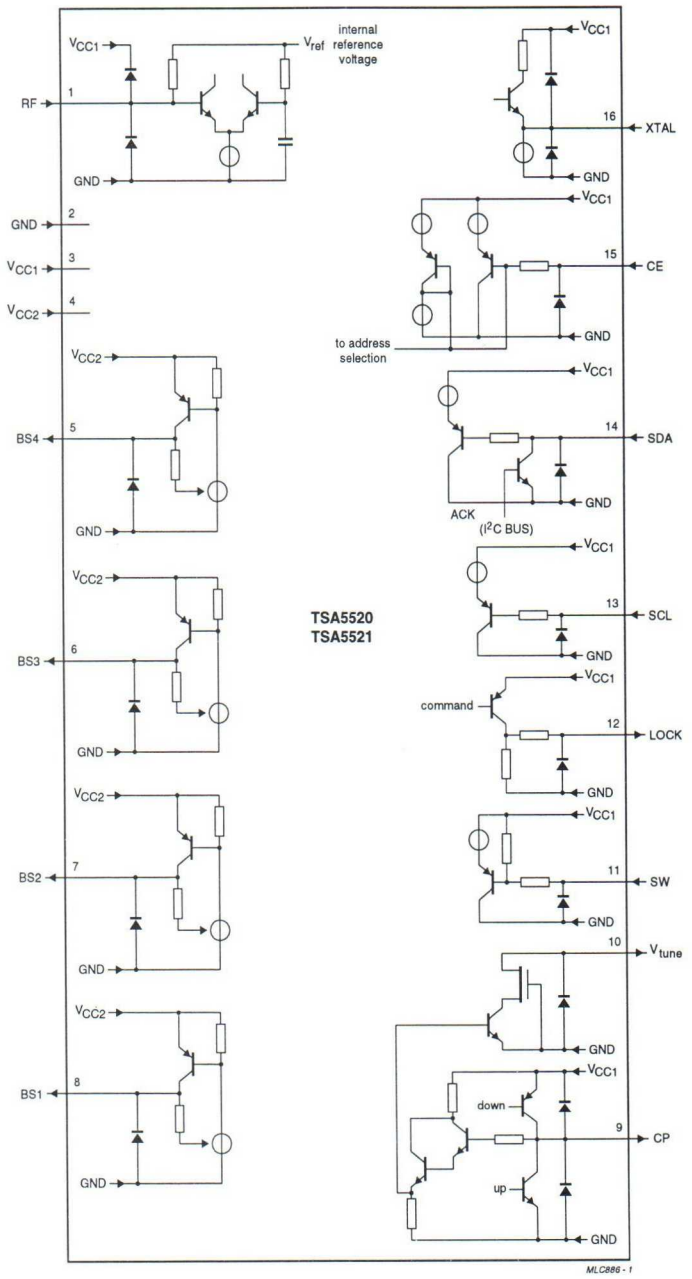


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. Figs 11 and 12 show a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred but it can, however, also be connected to ground.

Examples of I²C-bus sequences (SW = GND)

Tables 8 to 12 show the various sequences where f_{osc} = 100 MHz, BS4 = ON, I_{CP} = 280 µA, N = 512, f_{xtal} = 4 MHz, S = stop, A = acknowledge and P = stop. The sequence is as follows:
start + address byte + divider byte 1 + divider byte 2 + control byte + band switch byte + stop.

For the complete sequence see Table 8 (sequence 1) or Table 9 (sequence 2).

Table 8 Complete sequence 1

S	C2	A	06	A	40	A	CE	A	08	A	P

Table 9 Complete sequence 2

S	C2	A	CE	A	08	A	06	A	40	A	P

Table 10 Divider bytes only sequence

S	C2	A	06	A	40	A	P

Table 11 Control and band switch bytes only sequence

S	C2	A	CE	A	08	A	P

Table 12 Control byte only sequence

S	C2	A	CE	A	P

Other I²C-bus sequences are not allowed. Other I²C-bus addresses may be selected by applying an appropriate voltage to the CE input.

Examples of 3-wire bus sequences (TSA5520; SW = OPEN)

Table 13 18-bit sequence (f_{osc} = 800 MHz, BS4 = ON)

1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

Table 14 19-bit sequence (f_{osc} = 650 MHz, BS3 = ON)

0	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0

The reference divider is automatically set to 512 unless RSB has been programmed to 0 during a 27-bit sequence.

Table 15 27-bit sequence (f_{osc} = 750 MHz, BS1 = ON, N = 640, I_{cp} = 60 µA, no test function)

0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0

The reference divider is automatically set to 1024 unless RSB has been programmed to 0 during a 27-bit sequence. This sequence sets RSA = RSB = 0; CP = 0.

Table 16 19-bit sequence

0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 µA.

Table 17 18-bit sequence

0	0	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 µA.

Table 18 27-bit sequence (f_{osc} = 650 MHz, BS1 = ON)

0	0	0	1	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0

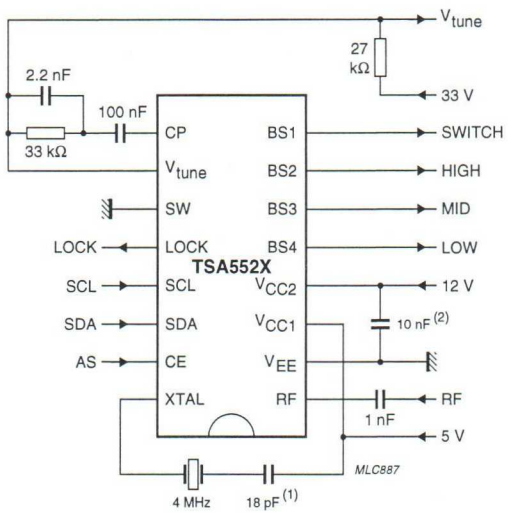
This sequence sets RSA to 0, RSB to 1 and CP to 1. After this sequence I_{CP} = 280 µA, N = 1024 (19-bit transmission) and N = 512 (18-bit transmission), RSB = 1.

Example of 3-wire bus sequence (TSA5521; SW = OPEN)

Table 19 19-bit sequence (f_{osc} = 700 MHz, BS3 = ON)

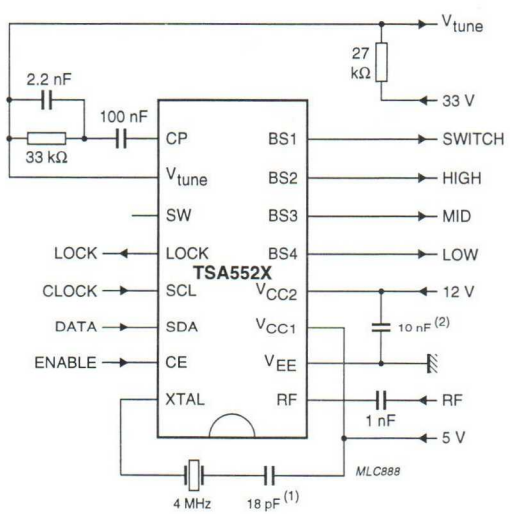
0	1	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

N = 640 unless RSB has been programmed to 0 during a 27-bit sequence.



(1) Connection to ground is also allowed.
(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.11 Typical I²C-bus application.



(1) Connection to ground is also allowed.
(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.12 Typical 3-wire bus application.

1.4 GHz I²C-bus controlled synthesizer TSA5522

FEATURES

- Complete 1.4 GHz single chip system
- Three pnp band switch buffers (20 mA)
- Four bus-controlled bidirectional ports (npn open-collector outputs); only one port in 16-pin version
- 33 V tuning voltage output
- In-lock detector
- 5-step ADC
- Mixer-Oscillator (M/O) band switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250 μA)
- Varicap drive disable
- I²C-bus format
  - address plus 4 data bytes transmission (write mode)
  - address plus 1 status byte transmission (read mode)
  - three independent addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front-ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5522M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TSA5522T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (+12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	22	30	mA
I_{CC2}	band switch supply current	note 1	–	27	32	mA
f_{RF}	RF input frequency		64	–	1400	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	– 25	–	3	dBm
		f_i = 150 to 1000 MHz	– 28	–	3	dBm
		f_i = 1000 to 1400 MHz	– 26	–	3	dBm
f_{xtal}	crystal oscillator input frequency		–	4	–	MHz
$I_{o(pnp)}$	pnp band switch buffers output current		–	20	25	mA
$I_{o(npn)}$	npn open-collector output current		–	20	25	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
T_{stg}	storage temperature (IC)		–40	–	+150	°C

Note

1. One band switch buffer ON; I_o = 20 mA.

GENERAL DESCRIPTION (see Fig.1)

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three high-current pnp band switch buffers are provided for band switching together with four open-collector npn outputs (only one open-collector output on 16-pin devices). These ports can also be used as input ports [one Analog-to Digital Converter (ADC) and three general purpose I/O ports (not available on 16-pin devices)]. An output is provided to control a Philips mixer/oscillator IC in combination with the pnp buffers state.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz with a 4 MHz crystal. The LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation.

The ADC is available for digital AFC control. The ADC code is read during a read operation on the I²C-bus. The ADC input is combined with the port P6. In the TEST mode, this port is also used as a TEST output for f_{ref} and $\frac{1}{2}f_{div}$ (see Table 4).

I²C-bus format

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and the reference divider ratio. The device has three independent I²C-bus addresses selected by applying a specific voltage on AS input (see Table 3). The general address C2 is always valid.

BLOCK DIAGRAM

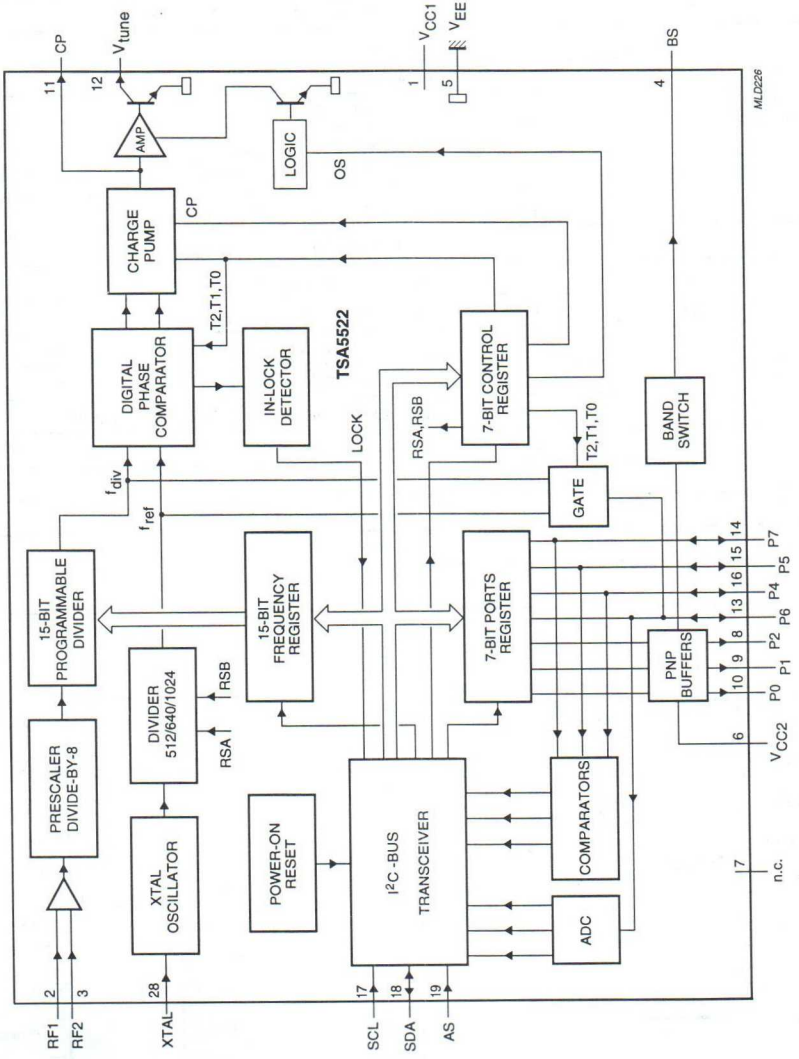


Fig.1 Block diagram (SSOP20).

PINNING

SYMBOL	SO16	SSOP20	DESCRIPTION
V_{CC1}	1	1	voltage supply (+5 V)
RF1	2	2	RF signal input 1
RF2	3	3	RF signal input 2
BS	4	4	band switch output to mixer/oscillator drive
V_{EE}	5	5	ground
V_{CC2}	6	6	voltage supply (+12 V)
n.c.	–	7	not connected
P2	7	8	pnp band switch buffer output 2
P1	8	9	pnp band switch buffer output 1
P0	9	10	pnp band switch buffer output 0
CP	10	11	charge-pump output
V_{tune}	11	12	tuning voltage output
P6	12	13	npn open-collector output/ADC input
P7	–	14	npn open-collector output/comparator input
P5	–	15	npn open-collector output/comparator input
P4	–	16	npn open-collector output/comparator input
SCL	13	17	serial clock input
SDA	14	18	serial data input/output
AS	15	19	address selection input
XTAL	16	20	crystal oscillator input

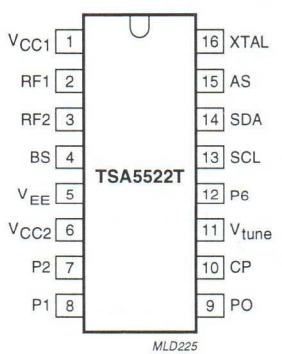


Fig.2 Pin configuration (SO16).

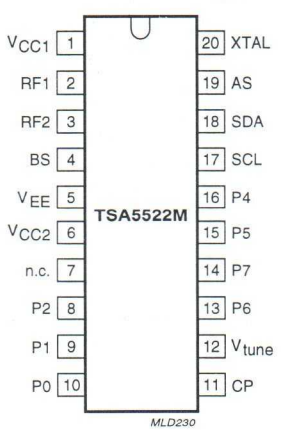


Fig.3 Pin configuration (SSOP20).

FUNCTIONAL DESCRIPTION

The device is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/W bit for selecting the READ or the WRITE mode.

I²C-bus mode

WRITE MODE (R/W = 0); see Table 1

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are required to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is divider byte 1 (DB1) or control byte (CB). The bits in the data bytes are defined in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and ports data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2), the control register is loaded after the 8th clock pulse of the control byte (CB) and the ports register is loaded after the 8th clock pulse of the ports byte (PB).

I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 3) in one system by applying a specific voltage on the AS input.

The relationship between MA1 and MA0 and the input voltage on the AS input is given in Table 3.

Table 1 I²C-bus data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Ports byte (PB)	P7[1]	P6	P5[1]	P4[1]	X	P2	P1	P0	A

Note

1. Not available on 16-pin devices.

Table 2 Description of Table 1

SYMBOL	DESCRIPTION
MA1, MA0	programmable address bits (see Table 3)
N14 to N0	programmable divider bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$
CP	charge-pump current; CP = 0 = 50 μA; CP = 1 = 250 μA
T2 to T0	test bits (see Table 4). For normal operation T2 = 0; T1 = 0; T0 = 1
RSA, RSB	reference divider ratio select bits (see Table 5)
OS	tuning amplifier control bit; for normal operation OS = 0 and tuning voltage is ON; when OS = 1 tuning voltage is OFF (high impedance)
P2 to P0	pnp band switch buffers control bits
P7 to P4	npn open collector control bits when P_n = 0 output n is OFF; when P_n = 1 output n is ON
X	don't care

Table 3 Address selection

VOLTAGE APPLIED ON AS INPUT	MA1	MA2
0 to $0.1V_{CC1}$	0	0
Always valid	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

Table 4 Test bits

T2	T1	T0	DEVICE OPERATION
0	0	1	normal mode
0	1	X	charge-pump is OFF
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f_{ref} is available at LOCK output
1	0	1	$\frac{1}{2}f_{div}$ is available at LOCK output

Table 5 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

Table 6 Band switch output levels

P2	P1	P0	VOLTAGE ON BS OUTPUT	PHILIPS M/O BAND
0	1	0	0.25 V	band A
1	0	0	$0.4V_{CC1}$	band B
0	0	1	$0.8V_{CC1}$	band C

READ MODE; R/W = 1 (see Table 7)

Data can be read from the device by setting the R/W bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition. When ports P4 to P7 are used as inputs, the corresponding bits **must** be logic 0 (high impedance state). The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag (FL) which indicates when the loop is locked (FL = 1).

The bits I2, to I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 indicates a HIGH level (see "Characteristics").

A built-in ADC is available at pin P6. This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2 to A0 is given in Table 8.

Table 7 READ data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	1	A[1]
Status byte (SB)	POR[2]	FL[3]	I2[4]	I1[4]	I0[4]	A2[5]	A1[5]	A0[5]	–

Notes

1. A = acknowledge.
2. POR = power-on-reset (POR = 1 at power-on).
3. FL = in-lock flag (FL = 1 when loop is locked).
4. I2 to I0 = digital levels for I/O ports P7, P5 and P4 respectively.
5. A2 to A0 = digital outputs of the 5-level ADC.

Table 8 ADC levels

VOLTAGE APPLIED ON PORT P6[1]	A2	A1	A0
$0.6V_{CC1}$ to 13.5V	1	0	0
$0.45V_{CC1}$ to $0.6V_{CC1}$	0	1	1
$0.3V_{CC1}$ to $0.45V_{CC1}$	0	1	0
$0.15V_{CC1}$ to $0.3V_{CC1}$	0	0	1
0 to $0.15V_{CC1}$	0	0	0

Note

1. Accuracy is $0.02V_{CC1}$.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX	UNIT
V_{CC1}	supply voltage +5 V	−0.3	6.0	V
V_{CC2}	supply voltage + 12 V	−0.3	16	V
$V_{i(RF)}$	prescaler input voltage	−0.3	V_{CC1}	V
$V_{o(BS)}$	band switch output voltage	−0.3	V_{CC1}	V
$V_{o(pnp)}$	pnp band switch buffer output voltage	− 0.3	V_{CC2}	V
$I_{o(pnp)}$	pnp band switch buffers output current	−1	25	mA
V_{npn}	npn open-collector output voltage	−0.3	16	V
I_{npn}	npn open-collector output current	−1	25	mA
$V_{o(CP)}$	charge-pump output voltage	−0.3	V_{CC1}	V
$V_{o(tune)}$	output tuning voltage	−0.3	35	V
$V_{i(SCL)}$	serial clock input voltage	−0.3	6.0	V
$V_{i/o(SDA)}$	serial data input/output voltage	−0.3	6.0	V
$I_{o(SDA)}$	serial data output current	−1	5	mA
$V_{i(AS)}$	address selection input voltage	−0.3	V_{CC1}	V
$V_{i(xtal)}$	crystal oscillator input voltage	−0.3	V_{CC1}	V
T_{stg}	storage temperature range (IC)	−40	+150	°C
T_j	maximum junction temperature	−	+150	°C
t_{sc}	short circuit time; every pin to V_{CC1} or GND	−	10	s

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices. Every pin withstands the ESD test in accordance with *MIL-STD-883C* category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO16	110	K/W
	SSOP20	120	K/W

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; V_{CC2} = V_{CC1} to 13.2 V; T_{amb} = –20 to 85 °C; unless otherwise specified; see note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	supply voltage (+12 V)		V_{CC1}	–	13.5	V
I_{CC1}	supply current		–	22	30	mA
I_{CC2}	supply current	One band switch buffer is ON; I_{source} = 20 mA	–	27	32	mA
f_{RF}	RF input frequency		64	–	1400	MHz
DR	divider ratio	15-bit frequency word	256	–	32767	MHz
Crystal oscillator						
f_{xtal}	crystal oscillator input frequency	R_{xtal} = 25 to 300 Ω	3.2	4	4.48	MHz
Z_{xtal}	crystal oscillator input impedance (absolute value)	f_i = 4 MHz	600	1200	–	Ω
Prescaler						
$V_{i(RF)}$	RF input level	V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 80 to 150 MHz	–25	–	3	dB
		V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 150 to 1000 MHz	–28	–	3	dB
		V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 1000 to 1400 MHz	–26	–	3	dB
pnp band switch buffers outputs						
$\|I_{LO}\|$	output leakage current	V_{CC2} = 13.5 V; V_o = 0 V	–10	–	–	µA
$V_{o(sat)}$	output saturation voltage	I_{source} = 20 mA; note 1	-	0.2	0.5	V
npn open-collector outputs P4, P5, P6 and P7; see note 2						
$\|I_{LO}\|$	output leakage current	V_{CC1} = 5.5 V; V_o = 13.5 V	–	–	10	µA
$V_{o(sat)}$	output saturation voltage	I_{sink} = 20 mA; note 3	–	0.2	0.5	V
C_{OL}	allowed capacitive loading on output pins	V_{OL} = 13.5 V			10	nF
Input ports P7, P5 and P4; see note 2						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
AS input (Address Selection)						
$I_{IH(AS)}$	HIGH level input current	$V_{AS} = V_{CC1}$	–	–	50	µA
$I_{IL(AS)}$	LOW level input current	$V_{AS} = 0$ V	–50	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	$V_{IH} = 5.5$ V; $V_{CC1} = 0$ V	–	–	10	µA
		$V_{IH} = 5.5$ V; $V_{CC1} = 5.5$ V	–	–	10	µA
I_{IL}	LOW level input current	$V_{IL} = 0$ V; $V_{CC1} = 5.5$ V	–10	–	–	µA
f_{clk}	input clock frequency		–	100	400	kHz
SDA output (I²C bus mode)						
I_{ILO}	output leakage current	$V_O = 5.5$ V	–	–	10	µA
V_o	output voltage	$I_{sink} = 3$ mA	–	–	0.4	µA
BS output (M/O band selection)						
$V_{o(BS)}$	output voltage	band A; $I_{source} = 20$ µA	–	0.25	0.5	V
		band B; $I_{source} = 20$ µA	$0.36V_{CC1}$	$0.4V_{CC1}$	$0.43V_{CC1}$	V
		band C; $I_{source} = 20$ µA	$0.7V_{CC1}$	$0.8V_{CC1}$	$0.9V_{CC1}$	V
		band C; $I_{source} = 50$ µA	3.1	–	–	V
Charge-pump output CP						
$\lvert I_{ICPH} \rvert$	HIGH charge pump current (absolute value)	CP = 1	–	250	–	mA
$\lvert I_{ICPL} \rvert$	LOW charge pump current (absolute value)	CP = 0	–	50	–	mA
$V_{o(CP)}$	output voltage	in-lock; $T_{amb} = +25$ °C	–	1.95	–	V
$I_{LI(off)}$	off-state leakage current	T2 = 0; T1 = 1	–5	1	15	nA
Tuning voltage output V_{tune}						
$I_{LO(off)}$	leakage current when switched-off	OS = 1; $V_{tune} = 33$ V	–	–	10	µA
V_o	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; $R_L = 27$ kΩ; $V_{tune} = 33$ V	0.4	–	32.6	V
$V_{ripple(p-p)}$	acceptable ripple voltage on V_{CC1} (peak-to-peak value)	$f_{ripple} = 300$ Hz to 300 kHz	–	–	30	mV

Notes to the characteristics

1. A single pnp band switch buffer is ON.
2. P4, P5 and P7 I/O ports are not available in 16-pin package. In 20-pin package, when a port is active, the collector voltage must not exceed 6 V.
3. A single npn open-collector output is ON.

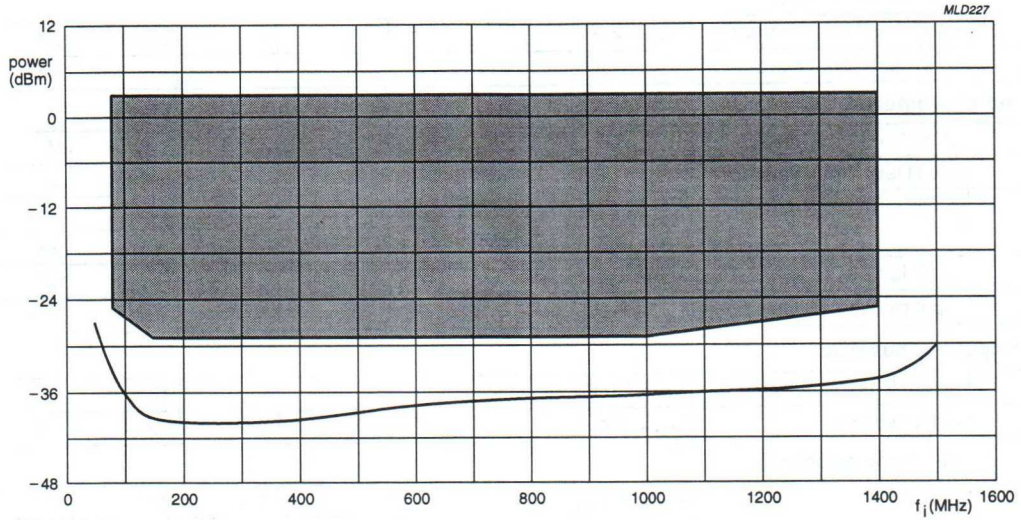


Fig.4 Prescaler typical input sensitivity curve.

INTERNAL PIN CONFIGURATION

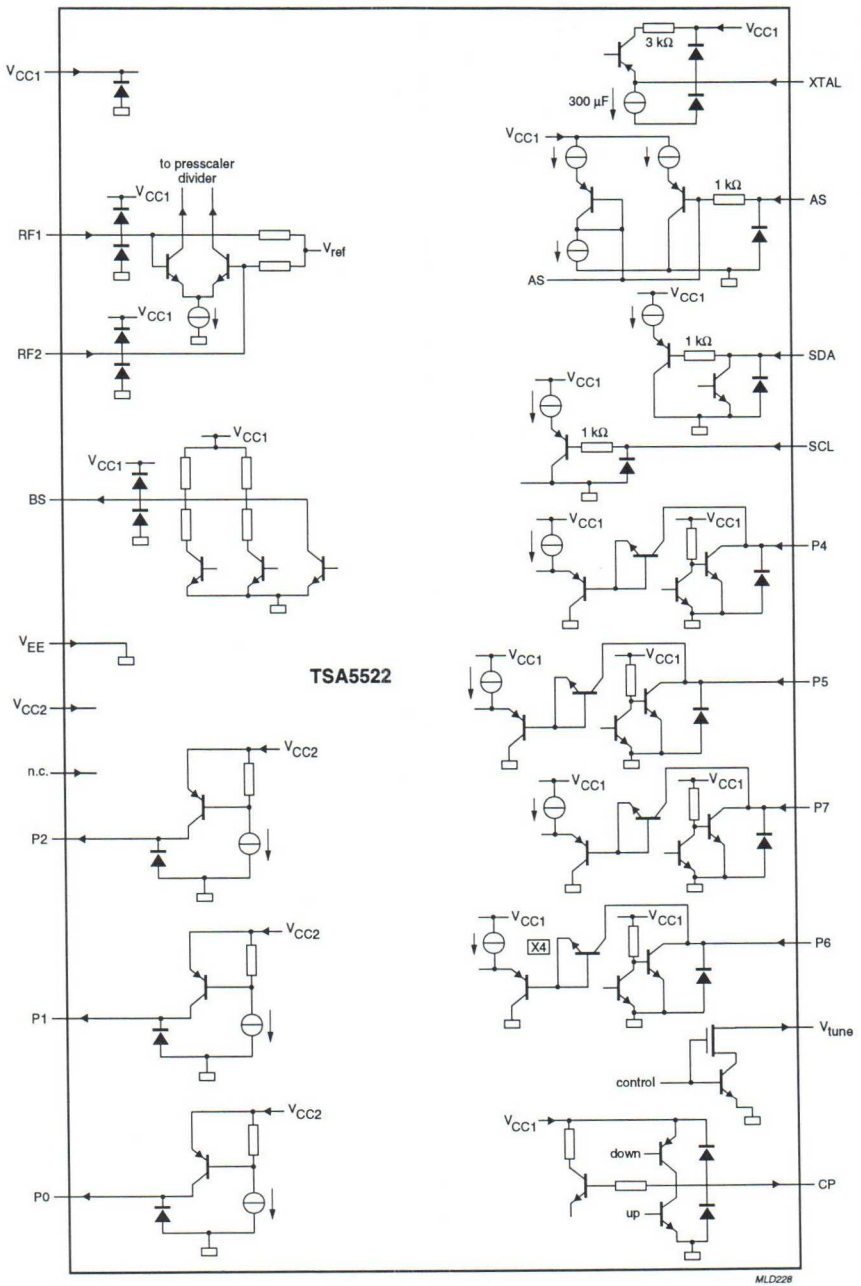


Fig.5 Internal pin configuration.

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. Figure 6 shows a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred, but it can, however, also be connected to ground.

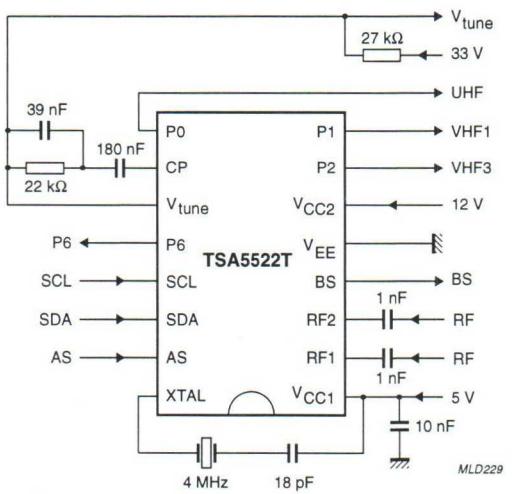


Fig.6 Typical application (SO16).

Flock flag (FL) definition

When the LOCK output is LOW the maximum frequency deviation (Δf) from stable frequency can be expressed as follows: $\Delta f = \pm\frac{K_{VCO}}{K_O} \times I_{CP} \times \frac{(C1 + C2)}{(C1 \times C2)}$

where:

K_{VCO} = oscillator slope Hz/V

I_{CP} = charge-pump current (A)

$K_O = 4 \times 10E6$

C1, C2 = loop filter capacitors.

In the application:

K_{VCO} = 16 MHz/V (UHF band)

I_{CP} = 250 μA

C1 = 180 nF, C2 = 39 nF

Δf = ±31.2 kHz.

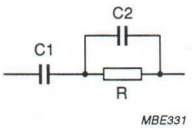


Fig.7 Loop filter.

Table 9 LOCK output / FL flag setting

DESCRIPTION	CONDITION	MIN.	MAX.	UNIT
Time span between actual phase lock and LOCK bit is LOW (or FL flag = 1)	RSA = 1; RSB = 1	1024	1152	μs
	RSA = 1; RSB = 1	2048	2304	μs
	RSB = 0	1280	1440	μs
Time span between the loop losing lock and LOCK bit is HIGH or (FL flag = 0)		0	300	μs

1.3 GHz universal bus-controlled TV synthesizer

TSA5526; TSA5526A TSA5527; TSA5527A

FEATURES

- Complete 1.3 GHz single chip system
- Four pnp band switch buffers (40 mA)
- 33 V output tuning voltage
- In-lock detector
- 5-step ADC
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (60 or 280 μA)
- Programmable automatic charge-pump current switch
- Varicap drive disable
- Universal bus protocol I²C-bus or 3-wire bus:
  - bus protocol for 18 or 19 bits transmission (3-wire bus)
  - extra protocol for 27 bits for test and features (3-wire bus)
  - address plus 4 data bytes transmission (I²C-bus write mode)
  - address plus 1 status byte transmission (I²C-bus read mode)
  - three independent I²C-bus addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5526M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5526AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5526AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TSA5527AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TSA5527AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	20	25	mA
I_{CC2}	band switch supply current	note 1	–	50	55	mA
f_{RF}	RF input frequency		64	–	1300	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
f_{xtal}	crystal oscillator input frequency		3.2	4.0	4.48	MHz
$I_{o(pnp)}$	pnp band switch buffers output current	note 2	4	–	50	mA
P_{tot}	total power dissipation	note 3	–	250	400	mW
T_{stg}	storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C

Notes

1. One band switch buffer ON, I_o = 40 mA.
2. One band switch buffer ON, I_o = 40 mA; two buffers ON, maximum sum of I_o = 50 mA.
3. The power dissipation is calculated as follows:

$$P_D = V_{CC1} \times I_{CC1} + V_{CC2} \times (I_{CC2} - I_o) + I_o \times V_{CE(satpnp)} + (V33/2)^2/27\,k\Omega$$

GENERAL DESCRIPTION

The device is a single-chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier and the 33 V output. Four high-current pnp band switch buffers are provided for band switching. Two pnp buffers can be switched on simultaneously. The sum of the collector currents is limited to 50 mA.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz using a 4 MHz crystal.

The device can be controlled in accordance with the I²C-bus format or the 3-wire bus format depending on the voltage applied to the SW input (see Table 2).In the 3-wire bus mode (SW = HIGH) pin 12 is the LOCK output. The lock output is LOW when the PLL loop is locked. In the I²C-bus mode (SW = LOW) the LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC input is available on pin 12 for AFC control in the I²C-bus mode only. The ADC code is read during a read operation on the I²C-bus. In the TEST mode pin 12 is used as a TEST output for f_{ref} and $\frac{1}{2}f_{div}$ in the I²C-bus mode and the 3-wire bus mode (see Table 6).

When the automatic charge-pump current switch mode is activated, depending on the device given in Table 6, and when the loop is phase-locked, the charge-pump current value is automatically switched to LOW. This action is taken to improve the carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a read operation on the I²C-bus (see Table 8).

I²C-bus format (SW = GND)

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the four pnp band switch buffers, set the charge-pump current and the reference divider ratio.

The device has three independent I²C-bus addresses which can be selected by applying a specific voltage on the CE input (see Table 5). The general address C2 is always valid. When the I²C-bus format is fully used, TSA5526 and TSA5527 are equal.

3-wire bus format (SW = V_{CC1} or open-circuit)

Data is transmitted to the device during a HIGH level on the CE input (enable line pin 15). The device is compatible with 18-bit and 19-bit data formats. The first four bits are used to program the pnp band switch buffers and the remaining bits are used to control the programmable divider. A 27-bit data format may also be used to set the charge-pump current, the reference divider ratio and for test purposes. The differences between TSA5526 and TSA5527 are given in Table 1.

When the 27-bit format is used, the TSA5526/TSA5527 are equal and the reference divider is controlled by the RSA and RSB bits (see Table 7). More details are given in the functional description (3-wire bus mode).

Table 1 Differences between TSA5526 and TSA5527

TYPE NUMBER	DATA WORD	REFERENCE DIVIDER	FREQUENCY STEP (kHz)
TSA5526	18-bit	512(1)	62.5
TSA5526	19-bit	1024(1)	31.25
TSA5527	19-bit	640(2)	50

Notes

1. The selection of the reference divider is given by an automatic identification of the data word length.
2. The reference divider is set to 640 at power-on reset.

BLOCK DIAGRAM

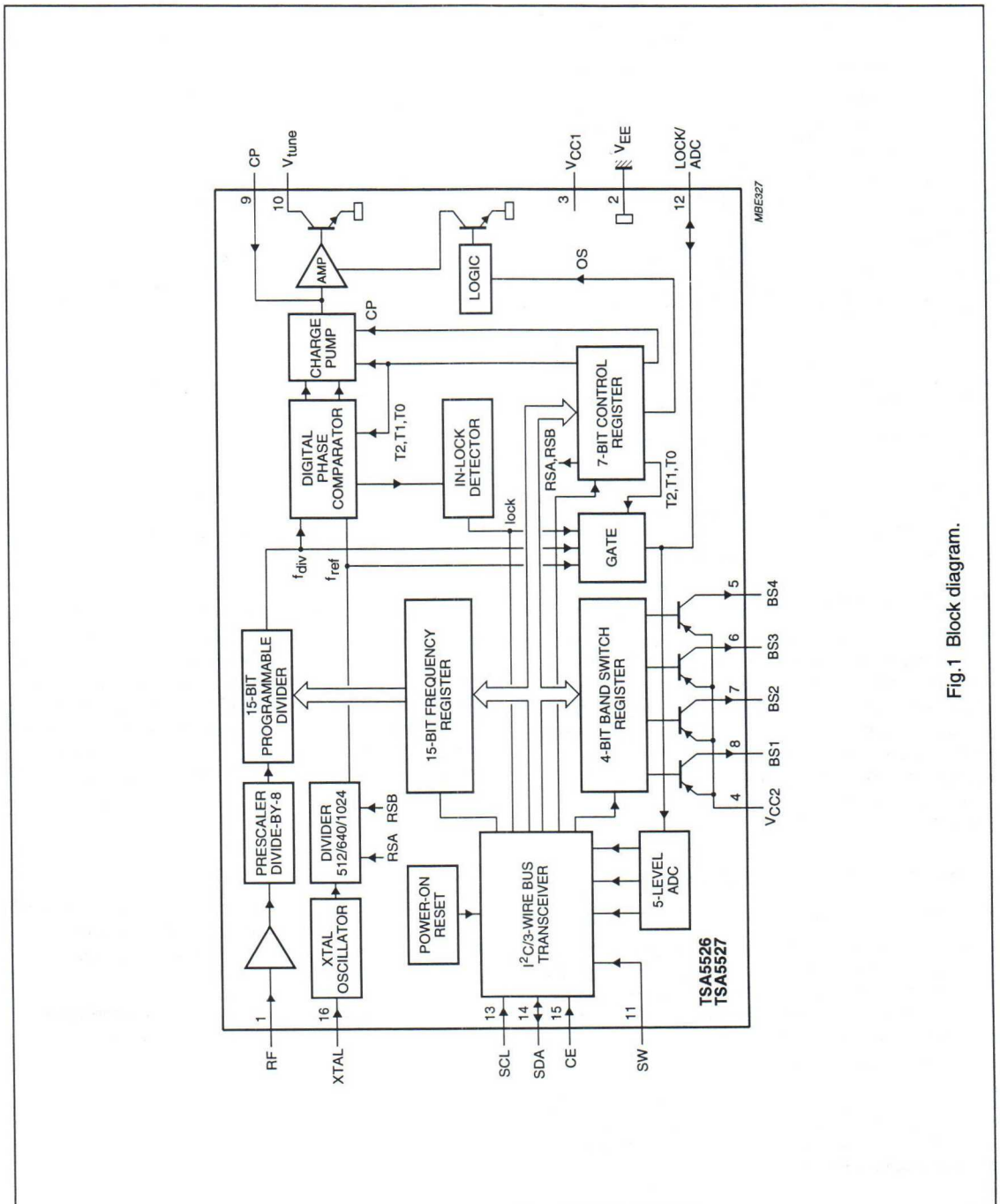


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RF	1	RF signal input
V_{EE}	2	ground
V_{CC1}	3	supply voltage (+5 V)
V_{CC2}	4	band switch supply voltage (+12 V)
BS4	5	pnp band switch buffer output 4
BS3	6	pnp band switch buffer output 3
BS2	7	pnp band switch buffer output 2
BS1	8	pnp band switch buffer output 1
CP	9	charge-pump output
V_{tune}	10	tuning voltage output
SW	11	bus format selection input, I²C-bus or 3-wire
LOCK/ADC	12	lock detector output (3-wire bus/ ADC input (I²C-bus)
SCL	13	serial clock input
SDA	14	serial data input/output
CE	15	chip enable/address selection input
XTAL	16	crystal oscillator input

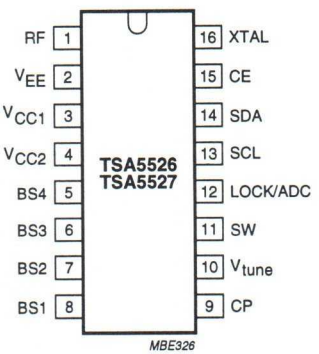


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The device is controlled via the I²C-bus or the 3-wire bus depending on the voltage applied to the SW input (pin 11). A HIGH level on the SW input enables the 3-wire bus inputs which are CE (chip enable), SDA (serial data input) and SCL (serial clock input). A LOW level on the SW input enables the I²C-bus inputs which are AS (address selection input), SDA (serial data input/output) and SCL (serial clock input). The bus format selection is given in Table 2.

I²C-bus mode (SW = GND); see Table 3

WRITE MODE (R/W = 0)

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are required to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is divider byte 1 (DB1) or the control byte (CB). The bits in the data bytes are defined in Table 3.

The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and band switch data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to readdress the device. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2), the control register is loaded after the 8th clock pulse of the control byte (CB) and the band switch register is loaded after the 8th clock pulse of the band switch byte (BB).

I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 3) in one system by applying a specific voltage to the CE input.

The relationship between MA1 and MA0 and the input voltage applied to the CE input is given in Table 5.

Table 2 Bus format selection

PIN	NAME	3-WIRE BUS MODE	I²C BUS MODE
11	SW	OPEN or HIGH	LOW
12	LOCK/ADC	LOCK/TEST output	ADC input/TEST output
13	SCL	clock input	SCL input
14	SDA	data input	SDA input/output
15	CE	chip enable input	address selection input

Table 3 I²C-bus data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band switch byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

Table 4 Description of Table 3

SYMBOL	DESCRIPTION
A	acknowledge
MA1 and MA0	programmable address bits (see Table 5)
N14 to N0	programmable divider bits; $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$
CP	charge-pump current; CP = 0 = 60 μA; CP = 1 = 280 μA (default)
T2 to T0	test bits (see Table 6); for normal operation T2 = 0, T1 = 0 and T0 = 1
RSA and RSB	reference divider ratio select bits (see Table 7)
OS	tuning amplifier control bit; for normal operation OS = 0 and tuning voltage is ON; when OS = 1 tuning voltage is OFF (high impedance)
BS4 to BS1	pnp band switch buffers control bits; when $BS_n = 0$ buffer n is OFF; when $BS_n = 1$ buffer n is ON
X	don't care

Table 5 I²C-bus address selection

VOLTAGE APPLIED TO THE CE INPUT (SW = GND)	MA1	MA0
0 V to $0.1V_{CC1}$	0	0
Always valid	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

Table 6 Test bits

T2	T1	T0	TSA5526; TSA5527	TSA5526A; TSA5527A	REMARKS
0	0	0	normal operation with automatic charge-pump switch ON	automatic charge-pump switch OFF	
0	0	1	normal operation with automatic charge-pump switch OFF	automatic charge-pump switch ON	status at POR
0	1	X	charge-pump is OFF	charge-pump is OFF	
1	1	0	charge-pump is sinking current	charge-pump is sinking current	
1	1	1	charge-pump is sourcing current	charge-pump is sourcing current	
1	0	0		f_{ref} is available at LOCK output	the ADC cannot be used when test mode is active
1	0	1		$\frac{1}{2}f_{div}$ is available at LOCK output	the ADC cannot be used when test mode is active

Table 7 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

READ MODE (R/W = 1); see Table 8

Data can be read from the device by setting the R/W bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs.

The device will then release the data line to allow the microcontroller to generate a stop condition. The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag (FL) which indicates when the loop is locked (FL = 1).

The Automatic Charge-Pump Switch flag (ACPS) is LOW when the automatic charge-pump switch mode is ON and the loop is locked. In other conditions ACPS = 1. When ACPS = 0, the charge-pump current is forced to the LOW value.

A built-in ADC is available at pin 12 (I^2C-bus only). This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2 to A0 is given in Table 9.

Table 8 Read data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 1	A[1]
Status byte (SB)	POR[2]	FL[3]	ACPS[4]	1	1	A2[5]	A1[5]	A0[5]	–

Notes

1. A = acknowledge.
2. POR = power-on-reset flag (POR = 1 at power-on).
3. FL = in-lock flag (FL = 1 when the loop is locked).
4. ACPS = automatic charge-pump switch flag (active ACPS = 0; non-active ACPS = 1).
5. A2 to A0 = digital outputs of the 5-level ADC.

Table 9 ADC levels

VOLTAGE APPLIED AT ADC INPUT	A2	A1	A0
$0.6V_{CC1}$ to V_{CC1}	1	0	0
$0.45V_{CC1}$ to $0.6V_{CC1}$	0	1	1
$0.3V_{CC1}$ to $0.45V_{CC1}$	0	1	0
$0.15V_{CC1}$ to $0.3V_{CC1}$	0	0	1
0 to $0.15V_{CC1}$	0	0	0

3-wire bus mode (SW = open-circuit or V_{CC1}); see Figs 3, 4 and 5

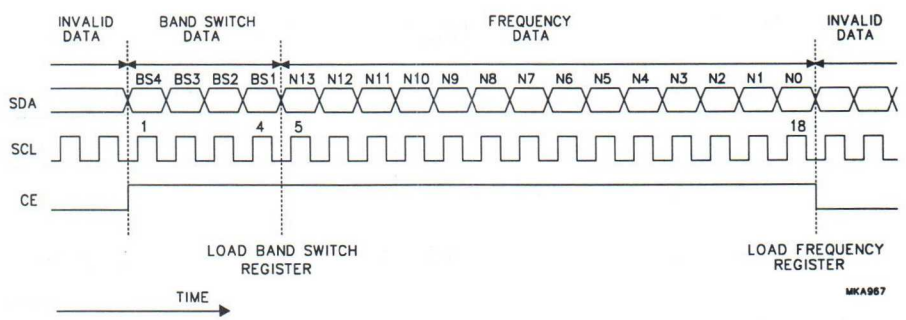
During a HIGH level on the CE input, the data is clocked into the data register at the HIGH-to-LOW transition of the clock pulse. The first four bits control the band switch buffers and are loaded into the internal band switch register on the 5th rising edge of the clock pulse. The frequency bits are loaded into the frequency register at the HIGH-to-LOW transition of the chip enable line when an 18-bit or 19-bit data word is transmitted.

At power-on the charge-pump current is set to 280 μA, the tuning voltage output is disabled (V_{tune} = 33 V in application; see Fig.12), the test bits T2, T1 and T0 are set to the 0 0 1 state in the normal mode with ACPS OFF for TSA55226/27 and ACPS ON for TSA5526A/5527A. RSB is set to 1 (TSA5526) or 0 (TSA5527). When an 18-bit data word is transmitted, the most significant bit of the divider N14 is internally set to 0 and bit RSA is set to 1. When a 19-bit data word is transmitted, bit RSA is set to 0.

When a 27-bit word is transmitted, the frequency bits are loaded into the frequency register on the 20th rising edge of the clock pulse and the control bits at the HIGH-to-LOW transition of the chip enable line. In this mode, the reference divider is given by the RSA and RSB bits (see Table 7). The test bits T2, T1 and T0, the charge-pump bit CP, the ratio select bit RSB and the OS bit can only be selected or changed with a 27-bit transmission. They remain programmed if an 18-bit or a 19-bit transmission occurs. Only RSA is controlled by the transmission length when the 18-bit or 19-bit format is used.

A data word of less than 18 bits will not affect the frequency register of the device. The definition of the bits is unchanged compared to the I^2C bus mode.

The power-on detection threshold voltage V_{POR} is fixed to V_{CC1} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state previously described.

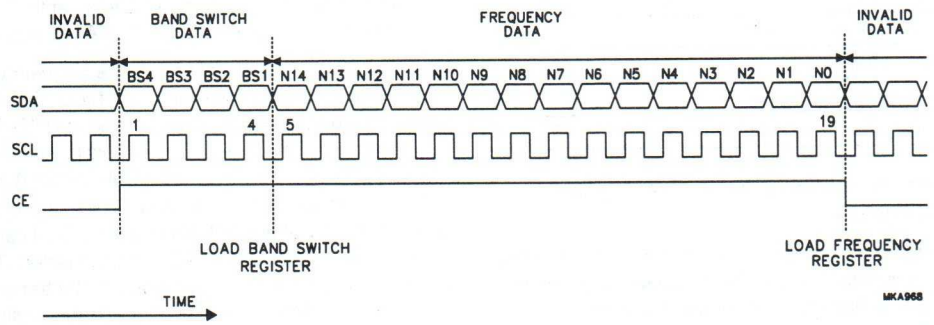


For TSA5526 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5526/TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.3 Normal mode; 18-bit data format (RSA = 1).

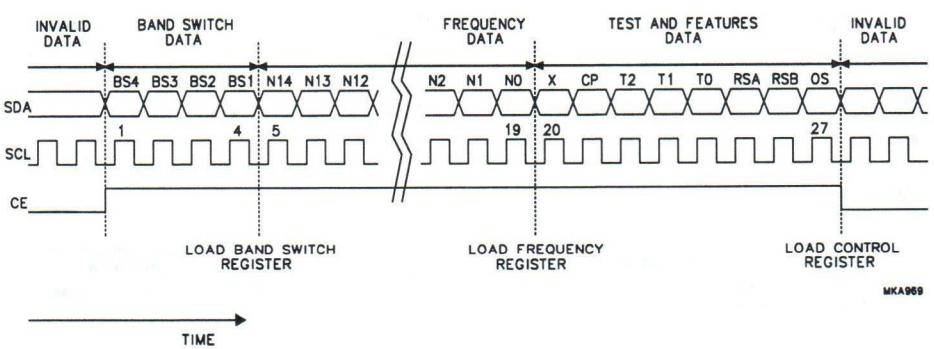


For TSA5526 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5526/TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.4 Normal mode; 19-bit data format (RSA = 0).



For TSA5526 bit RSB = 1 at power-on; the reference divider is 512 or 1024.

For TSA5527 bit RSB = 0 at power-on; the reference divider is 640.

For TSA5526/TSA5527 the value of RSB can also be programmed by using the 27-bit data format. When returning to the normal mode, bit RSB remains as programmed with the 27-bit data word.

Fig.5 Test and features mode; 27-bit data format.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC1}	supply voltage; +5 V (pin 3)		−0.3	6.0	V
V_{CC2}	band switch supply voltage; +12 V (pin 4)		−0.3	16	V
$V_{i(RF)}$	prescaler input voltage		−0.3	V_{CC1}	V
$V_{o(BSn)}$	band switch buffers output voltage (pins 5 to 8)		−0.3	V_{CC2}	V
$I_{o(BSn)}$	band switch buffers output current		−1	50	mA
$V_{o(CP)}$	charge-pump output voltage (pin 9)		−0.3	V_{CC1}	V
$V_{o(tune)}$	output tuning voltage (pin 10)		−0.3	35	V
$V_{i(SW)}$	input switching voltage (pin 11)		−0.3	V_{CC1}	V
$V_{o(LOCK)}$	lock output voltage (pin 12)		−0.3	V_{CC1}	V
$V_{i(SCL)}$	serial clock input voltage (pin 13)		−0.3	6.0	V
$V_{i/o(SDA)}$	serial data input/output voltage (pin 14)		−0.3	6.0	V
$I_{o(SDA)}$	serial data output current		−1	10	mA
$V_{i(CE)}$	chip enable input voltage (pin 15)		−0.3	6.0	V
$V_{i(xtal)}$	crystal oscillator input voltage (pin 16)		−0.3	V_{CC1}	V
T_{stg}	storage temperature		−40	+150	°C
T_j	maximum junction temperature		−	+150	°C
t_{sc}	short-circuit time; every pin except pin 4 to pin 3 and every pin to pin 2	note 1	−	10	s

Note

1. Short-circuit between V_{CC1} and V_{CC2} is allowed provided the voltage applied to V_{CC2} is less than the 6 V maximum rating at V_{CC1}.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO16	110	K/W
	SSOP16	142	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices. Every pin withstands the ESD test in accordance with *MIL-STD-883C* category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; V_{CC2} = V_{CC1} to 13.2 V; T_{amb} = –20 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC1}	supply voltage		4.5	–	5.5	V
V_{CC2}	band switch buffers supply voltage		V_{CC1}	–	13.5	V
I_{CC1}	supply current	at power-on	–	20	25	mA
I_{CC2}	band switch buffers supply current	at power-on	–	0.5	1	mA
		one band switch buffer is ON; I_{source} = 40 mA	–	50	55	mA
		two band switch buffers are ON; I_{source} = 40 mA + 5 mA (any combination)	–	56	62	mA
V_{POR}	supply voltage below which POR is active		1.5	2.0	–	V
f_{RF}	RF input frequency		64	–	1300	MHz
DR	divider ratio	15-bit frequency word	256	–	32767	
		14-bit frequency word	256	–	16383	
f_{xtal}	crystal oscillator input frequency	R_{xtal} = 25 to 300 Ω	3.2	4	4.48	MHz
Z_{xtal}	crystal oscillator input impedance (absolute value)	f_i = 4 MHz	600	1200	–	Ω
Prescaler (see Figs 6 and 7)						
$V_{i(RF)}$	RF input level	f_i = 80 to 150 MHz	–25	–	3	dBm
		f_i = 150 to 1000 MHz	–28	–	3	dBm
		f_i = 1000 to 1300 MHz	–15	–	3	dBm
$Z_{i(RF)}$	input impedance	see Fig.8				
pnp band switch buffers outputs (pins 5 to 8)						
I_{LO}	output leakage current	V_{CC2} = 13.5 V; V_o = 0 V	–10	–	–	µA
$V_{o(sat)}$	output saturation voltage	I_{source} = 40 mA; $V_{o(sat)} = V_{CC2} - V_o$	–	0.2	0.4	V
LOCK output (pnp collector output)						
$I_{o(ool)}$	output current when out-of-lock	V_{CC1} = 5.5 V; V_o = 5.5 V	–	–	100	µA
$V_{osat(ool)}$	output saturation voltage when out-of-lock	I_{source} = 200 µA; $V_{o(sat)} = V_{CC1} - V_o$	–	0.4	0.8	V
$V_{o(LOCK)}$	lock output voltage		–	0.01	0.4	V
ADC input (I^2C-bus mode) pin 12						
$V_{i(ADC)}$	ADC input voltage	see Table 9	0	–	V_{CC1}	V
$I_{IH(ADC)}$	HIGH level input current	$V_{ADC} = V_{CC1}$	–	–	10	µA
$I_{IL(ADC)}$	LOW level input current	V_{ADC} = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SW input (bus format switch)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	V_{CC1}	V
I_{IH}	HIGH level input current	$V_{SW} = V_{CC1}$	–	–	10	µA
I_{IL}	LOW level input current	$V_{SW} = 0$ V	–100	–	–	µA
CE input (chip enable/address selection)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	5.5	V
I_{IH}	HIGH level input current	$V_{CE} = 5.5$ V	–	–	10	µA
I_{IL}	LOW level input current	$V_{CE} = 0$ V	–10	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	$V_{BUS} = 5.5$ V; $V_{CC1} = 0$ V	–	–	10	µA
		$V_{BUS} = 5.5$ V; $V_{CC1} = 5.5$ V	–	–	10	µA
I_{IL}	LOW level input current	$V_{BUS} = 1.5$ V; $V_{CC1} = 0$ V	–	–	10	µA
		$V_{BUS} = 0$ V; $V_{CC1} = 5.5$ V	–10	–	–	µA
f_{clk}	clock frequency		–	100	400	kHz
SDA outputs (I^2C-bus mode)						
I_{LO}	output leakage current	$V_{SDA} = 5.5$ V	–	–	10	µA
V_o	output voltage	$I_{sink} = 3$ mA	–	–	0.4	V
Charge-pump output CP						
$\|I_{ICPH}\|$	HIGH charge-pump current	CP = 1	–	280	–	µA
$\|I_{ICPL}\|$	LOW charge-pump current	CP = 0	–	60	–	µA
V_{CP}	output voltage	in-lock; $T_{amb} = 25$ °C	–	1.95	–	V
$I_{LI(off)}$	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
Tuning voltage output V_{tune}						
$I_{LO(off)}$	leakage current when switched-off	OS = 1; $V_{tune} = 33$ V	–	–	10	µA
V_o	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; $R_L = 27$ kΩ; $V_{tune} = 33$ V	0.2	–	32.7	V
3-wire bus timing (see Figs 6 and 7)						
t_{HIGH}	clock high time		2	–	–	µs
$t_{SU;DAT}$	data set-up time		2	–	–	µs
$t_{HD;DAT}$	data hold time		2	–	–	µs
$t_{SU;ENSCL}$	enable to clock set-up time		10	–	–	µs
$t_{HD;ENDAT}$	enable to data hold time		2	–	–	µs
t_{EN}	enable between two transmissions		10	–	–	µs
$t_{HD;ENSCL}$	enable to clock active edge hold time		6	–	–	µs

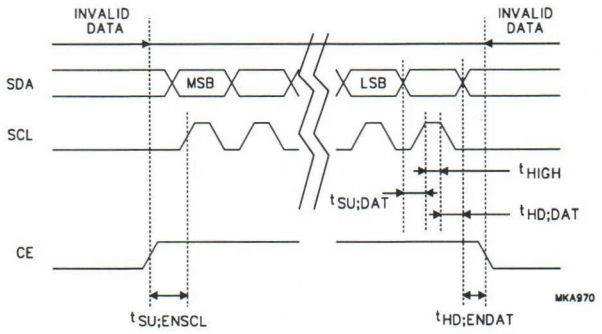


Fig.6 Timing diagram for 3-wire bus; SDA, SCL and CE.

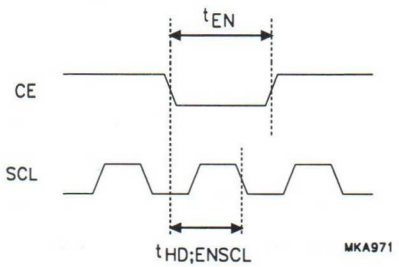


Fig.7 Timing diagram for 3-wire bus; CE and SCL.

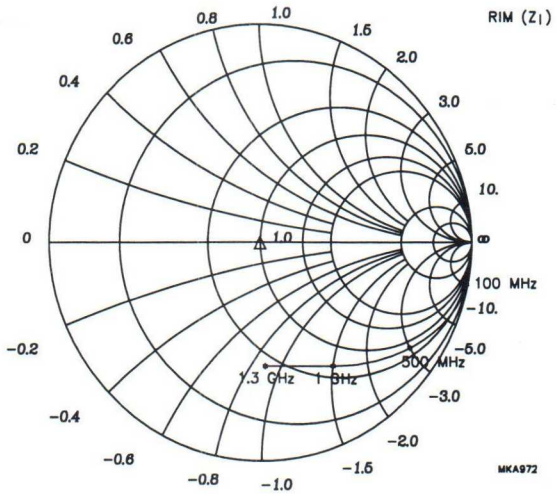


Fig.8 Prescaler Smith chart of typical input impedance at pin 1.

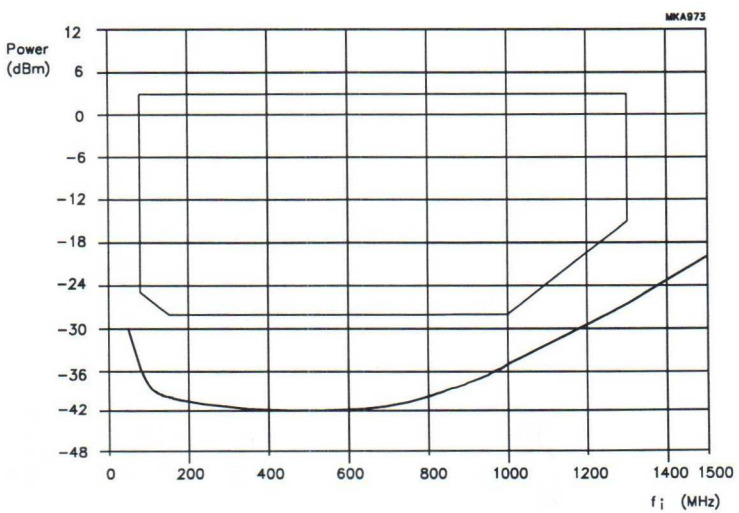


Fig.9 Prescaler typical input sensitivity curve.

INTERNAL PIN CONFIGURATION

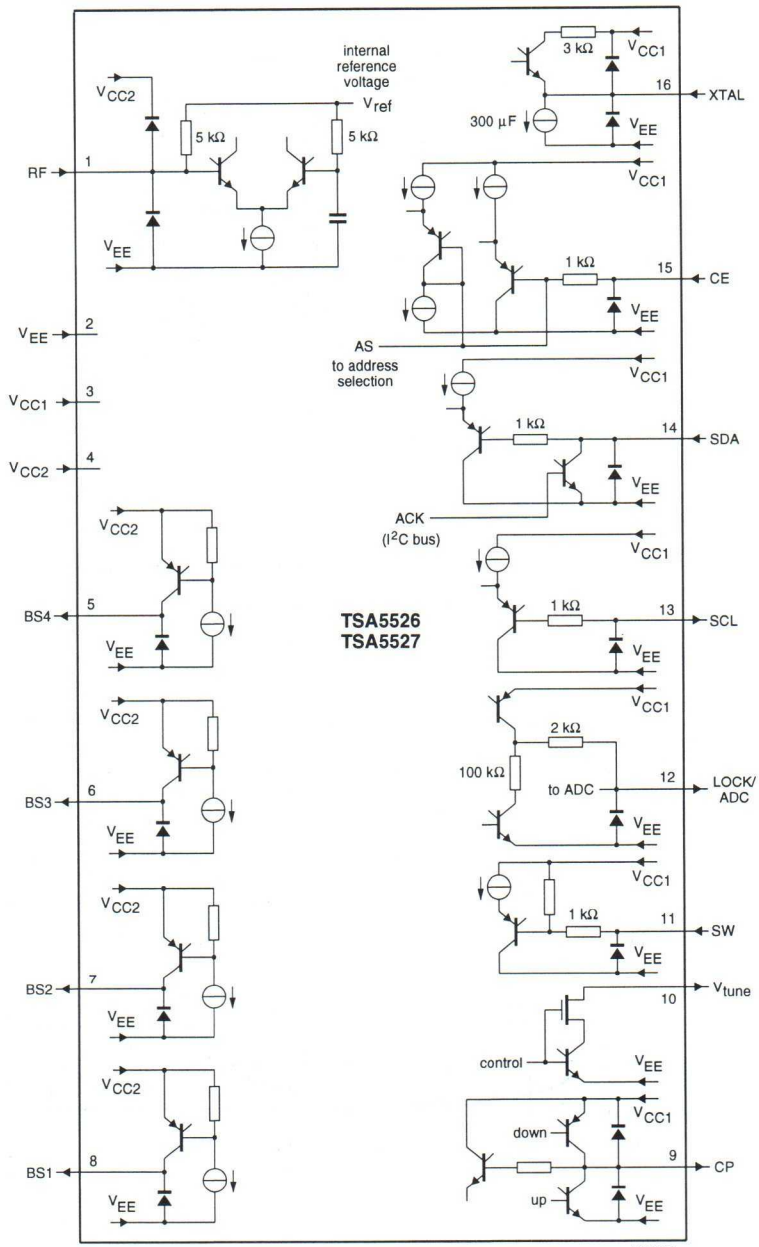


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. Figs 11 and 12 show a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred but it can, however, also be connected to ground.

Examples of I²C-bus sequences (SW = V_{EE})

Tables 10 to 14 show the various sequences where f_{osc} = 100 MHz, BS4 = ON, I_{CP} = 280 μA, N = 512, f_{xtal} = 4 MHz, S = stop, A = acknowledge and P = stop. The sequence is as follows:
start + address byte + divider byte 1 + divider byte 2 + control byte + band switch byte + stop.

For the complete sequence see Table 10 (sequence 1) or Table 11 (sequence 2).

Table 10 Complete sequence 1

S	C2	A	06	A	40	A	CE	A	08	A	P

Table 11 Complete sequence 2

S	C2	A	CE	A	08	A	06	A	40	A	P

Table 12 Divider bytes only sequence

S	C2	A	06	A	40	A	P

Table 13 Control and band switch bytes only sequence

S	C2	A	CE	A	08	A	P

Table 14 Control byte only sequence

S	C2	A	CE	A	P

Other sequences are not allowed in the write mode.

Table 15 One status byte acquisition

S	C3	A	XX(1)	X(2)	P

Notes

1. XX = the read status byte.
2. X = no acknowledge from the master means end of sequence.

Table 16 Two status byte acquisition

S	C3	A	XX[1]	A	XX[1]	X[2]	P

Notes

1. XX = the read status byte.
2. X = no acknowledge from the master means end of sequence.

Other I²C-bus addresses may be selected by applying an appropriate voltage to the CE input.

Examples of 3-wire bus sequences (TSA5526; SW = OPEN)

Table 17 18-bit sequence (f_{osc} = 800 MHz, BS4 = ON)

1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

The reference divider is automatically set to 512 unless RSB has been programmed to 0 during a 27-bit sequence (see Table 19).

Table 18 19-bit sequence (f_{osc} = 650 MHz, BS3 = ON)

0	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0

The reference divider is automatically set to 512 unless RSB has been programmed to 0 during a 27-bit sequence (see Table 19).

Table 19 27-bit sequence (f_{osc} = 750 MHz, BS1 = ON, N = 640, I_{cp} = 60 µA, no test function)

0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0

The reference divider is automatically set to 1024 unless RSB has been programmed to 0 during a 27-bit sequence. This sequence sets RSA = RSB = 0; CP = 0.

Table 20 19-bit sequence

0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 µA.

Table 21 18-bit sequence

0	0	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0

This sequence will program f_{osc} to 600 MHz in 50 kHz steps. I_{CP} remains at 60 µA.

Table 22 27-bit sequence (f_{osc} = 650 MHz, BS1 = ON)

0	0	0	1	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0

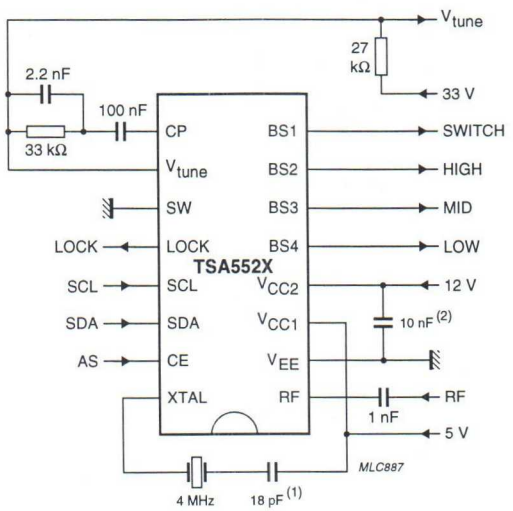
This sequence sets RSA to 0, RSB to 1 and CP to 1. After this sequence I_{CP} = 280 µA, N = 1024 (19-bit transmission) and N = 512 (18-bit transmission), RSB = 1.

Example of 3-wire bus sequence (TSA5527; SW = OPEN)

Table 23 19-bit sequence (f_{osc} = 700 MHz, BS3 = ON)

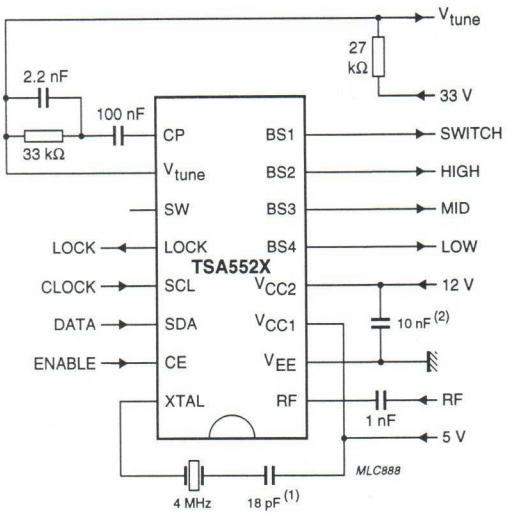
0	1	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0

N = 640 unless RSB has been programmed to 0 during a 27-bit sequence.



(1) Connection to ground is also allowed.
(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.11 Typical I²C-bus application.



(1) Connection to ground is also allowed.

(2) Capacitor prevents parasitic oscillation on the V_{CC2} line.

Fig.12 Typical 3-wire bus application.

Flock flag (FL) definition

When the LOCK output is LOW the maximum frequency deviation (Δf) from the stable frequency can be expressed as follows: $\Delta f = \pm \frac{K_{VCO}}{K_O} \times I_{CP} \times \frac{(C1 + C2)}{(C1 \times C2)}$

where;

K_{vco} = oscillator slope Hz/V

I_{CP} = charge-pump current (A)

$K_O = 4 \times 10E6$

C1, C2 = loop filter capacitors.

In the application:

K_{VCO} = 16 MHz/V (UHF band).

I_{CP} = 60 µA.

C1 = 100 nF, C2 = 2.2 nF.

$\Delta f = \pm 111$ kHz.

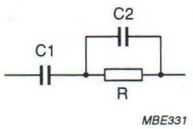


Fig.13 Loop filter.

Table 24 LOCK output/FL flag setting

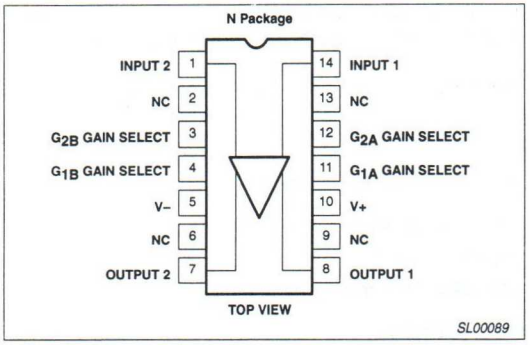
DESCRIPTION	CONDITION	MIN.	MAX.	UNIT
The time span between actual phase-lock and LOCK output is LOW (or FL flag = 1)	RSA = 1; RSB = 1	1024	1152	µs
	RSA = 0; RSB = 1	2048	2304	µs
	RSB = 0	1280	1440	µs
The time span between the loop losing lock and LOCK output is HIGH (or FL flag = 0)		0	300	µs

Differential video amplifier — μA733/733C

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

PIN CONFIGURATION



FEATURES

- 120MHz bandwidth
- 250kΩ input resistance
- Selectable gains of 10, 100, and 400
- No frequency compensation required
- MIL-STD-883A, B, C available

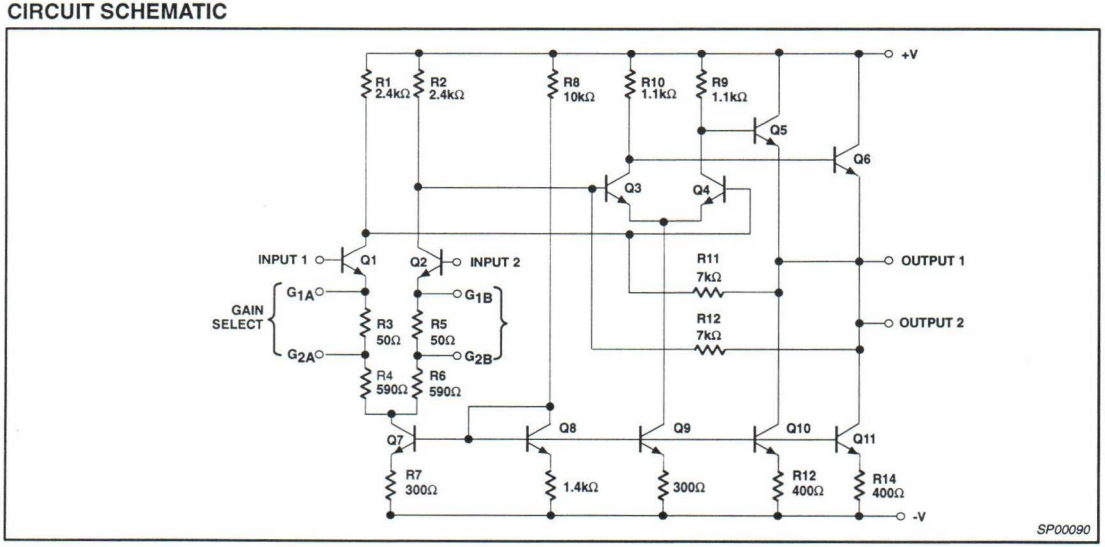
APPLICATIONS

- Video amplifier
- Pulse amplifier in communications
- Magnetic memories
- Video recorder systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE	DWG #
14-Pin Plastic Dual In–Line Package (DIP)	-55°C to +125°C	μA733N	0405B
14-Pin Plastic Dual In–Line Package (DIP)	0 to +70°C	μA733CN	0405B

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	μA733C	0 to +70	°C
	μA733	-55 to +125	°C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1]	1420	mW

NOTE:
1. The following derating factors should be applied above 25°C:
   N package at 11.4mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_S=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$							
	Gain 1[2]		250	400	600	300	400	500	V/V
	Gain 2[2]		80	100	120	90	100	110	V/V
	Gain 3[3]		8	10	12	9	10	11	V/V
	Gain 1[1]			40			40		
BW	Gain 2[2]			90			90		MHz
	Gain 3[3]			120			120		
t_R		V_{OUT} = $1V_{P-P}$							
	Gain 1[1]			10.5			10.5		ns
	Gain 2[2]			4.5	12		4.5	10	ns
	Gain 3[3]			2.5			2.5		ns
t_{PD}		V_{OUT} = $1V_{P-P}$							
	Gain 1[1]			7.5			7.5		ns
	Gain 2[2]			6.0	10		6.0	10	ns
	Gain 3[3]			3.6			3.6		ns
R_{IN}									
	Gain 1[2]			4.0			4.0		kΩ
	Gain 2[2]		10	30		20	30		kΩ
	Gain 3[3]			250			250		kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW=1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR									
	Gain 2	V_{CM}=±1V, f≤100kHz	60	86		60	86		dB
	Gain 2	V_{CM}=±1V, f=5MHz		60			60		dB

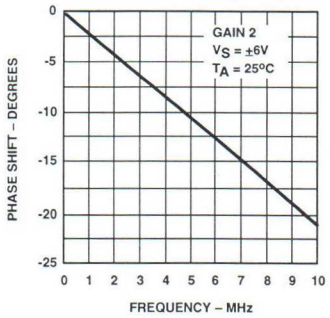
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
	Output offset voltage	$R_L = \infty$							
	Gain 1[1]			0.6	1.5		0.6	1.5	V
	Gain 2 and 3[2, 3]			0.35	1.5		0.35	1.0	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	R_L=2kΩ	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**-55°C ≤ T_A ≤ 125°C**			
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**UNIT**
	Differential voltage gain	R_l = 2kΩ, $V_{OUT} = 3V_{P-P}$							
	Gain 1[1]		250		600	200		600	V/V
	Gain 2[2]		80		120	80		120	V/V
	Gain[3]		8		12	8		12	V/V
R_{IN}	Input resistance								
	Gain 2[2]		8			8			kΩ
I_{OS}	Input offset current				6			5	µA
I_{BIAS}	Input bias current				40			40	µA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2	V_{CM}=±V, F≤100kHz	50			50			dB
SVRR	Supply voltage rejection ratio								
	Gain 2	ΔV_S=±0.5V	50			50			dB
V_{OS}	Output offset voltage	$R_L = \infty$							
	Gain 1[1]				1.5			1.5	V
	Gain 2 and 3[2, 3]				1.5			1.2	V
V_{DIFF}	Output voltage swing, differential	R_L = 2kΩ	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

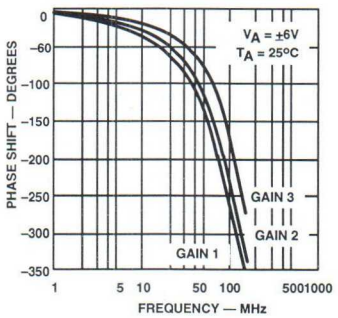
NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

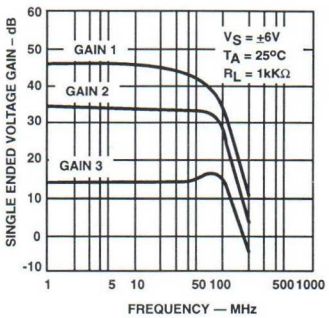
Phase Shift as a Function of Frequency



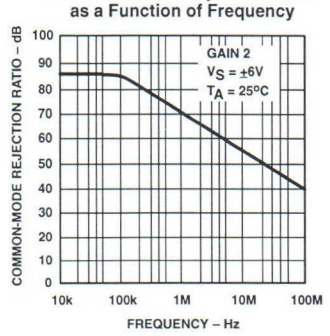
Phase Shift as a Function of Frequency



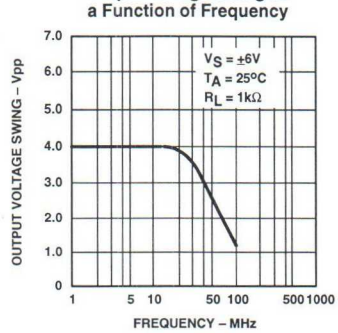
Voltage Gain as a Function of Temperature



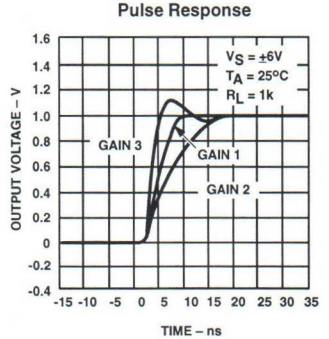
Common-Mode Rejection Ratio as a Function of Frequency



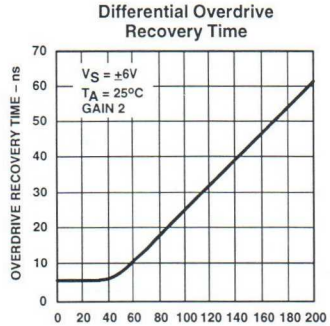
Output Voltage Swing as a Function of Frequency



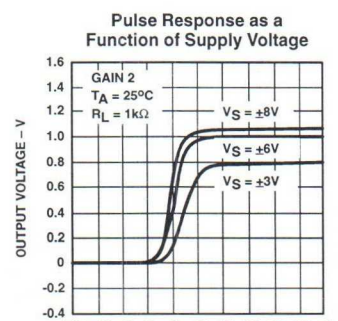
Pulse Response



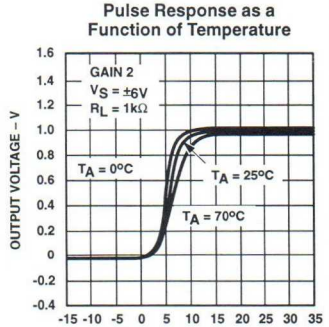
Differential Overdrive Recovery Time



Pulse Response as a Function of Supply Voltage



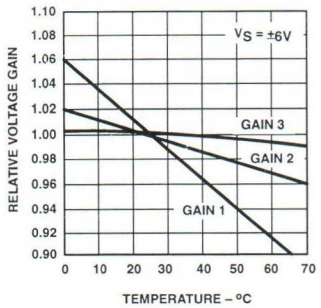
Pulse Response as a Function of Temperature



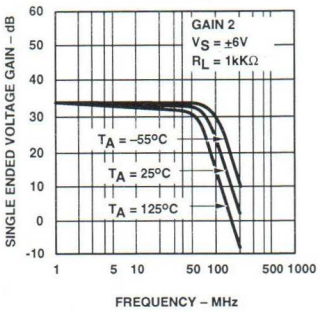
SL00091

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

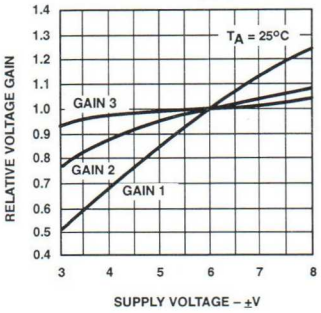
Voltage Gain as a Function of Temperature



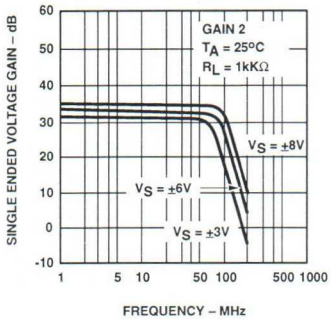
Gain vs. Frequency as a Function of Temperature



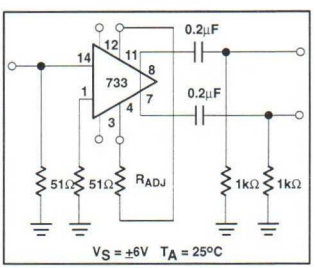
Voltage Gain as a Function of Supply Voltage



Gain vs. Frequency as a Function of Supply Voltage

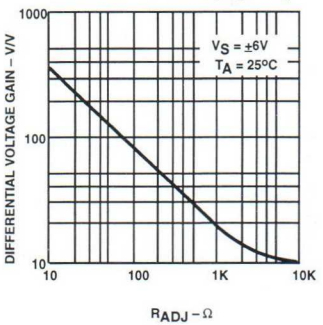


Voltage Gain Adjust Circuit

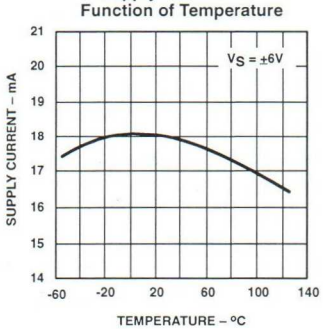


(Pin numbers apply to K Package)

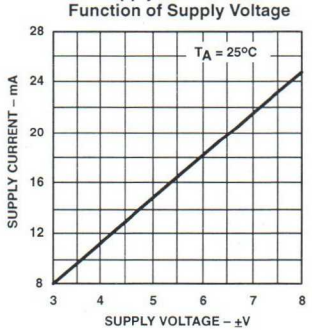
Voltage Gain as a Function of RADJ (Figure 3)



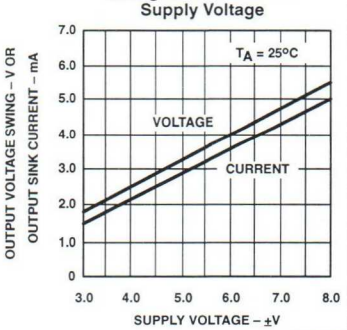
Supply Current as a Function of Temperature



Supply Current as a Function of Supply Voltage

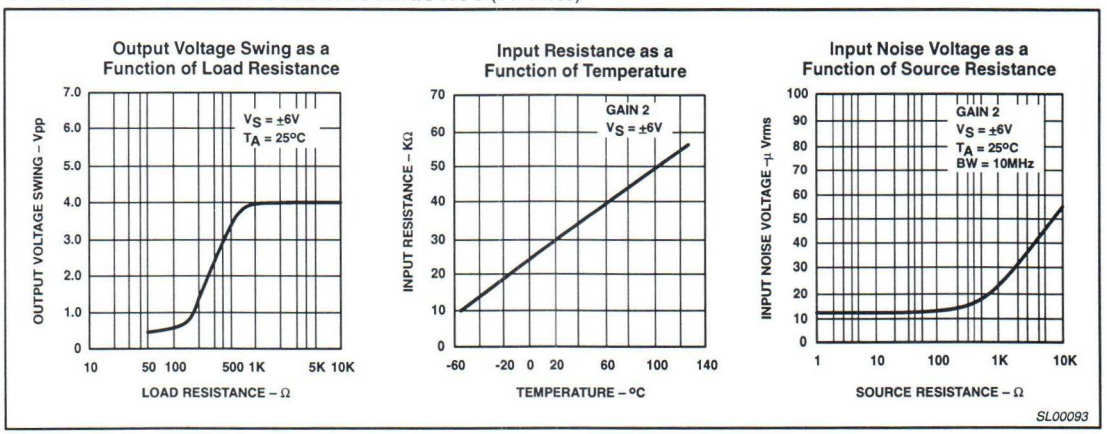


Output Voltage and Current Swing as a Function of Supply Voltage

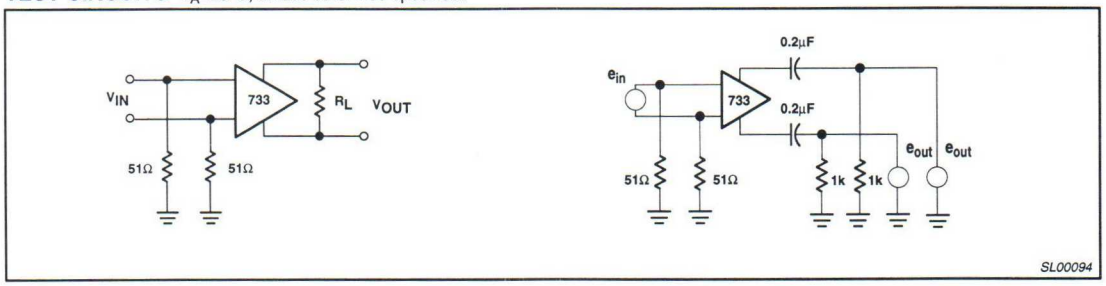


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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST CIRCUITS T_A=25°C, unless otherwise specified.



PACKAGE INFORMATION

	Page
PACKAGE OUTLINES	
Index	4790
CDIP	4793
DBS	4794
DIP	4797
LQFP	4809
PLCC	4811
QFP	4815
SDIP	4824
SIL	4828
SO	4831
SSOP	4840
VSO	4844
SOLDERING	4845

INDEX

NAME	DESCRIPTION	VERSION	PAGE
CDIP			
CDIP14	ceramic dual in-line package; 14 leads (300 mil)	0581B	4793
DBS (DIL-bent-SIL)			
DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1; SOT111; SOT111BE	4794
DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm)	SOT157-2; SOT157	4795
DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6; SOT141; SOT141B; SOT141RGA	4796
DIP (dual in-line package)			
DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1; SOT97; SOT97A; 0404B	4797
DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1; SOT27; 0405B	4798
DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1; SOT38; SOT38GE; SOT38GE1; SOT38GG; SOT38GG2; SOT38WE-2	4799
DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4; SOT38; 0406C	4800
DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1; SOT102(1); SOT102HE; SOT102RG; SOT102RG4	4801
DIP18	plastic dual in-line package; 18 leads (300 mil); slim corner leads	SOT102-2; SOT102(1)	4802
DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1; SOT146; SOT146EF4	4803
DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1; SOT101; SOT101A; SOT101B	4804
DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1; SOT117; SOT117AG	4805
DIP32	plastic dual in-line package; 32 leads (600 mil)	SOT201-1; SOT201	4806
DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1; SOT129	4807
DIP48	plastic dual in-line package; 48 leads (600 mil)	SOT240-1; SOT240; SOT240A	4808
LQFP (low profile quad flat package)			
LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1	4809
LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2	4810

NAME	DESCRIPTION	VERSION	PAGE
PLCC (plastic leaded chip carrier)			
PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2; SOT261; SOT261CG	4811
PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2; SOT187	4812
PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2; SOT188; SOT188A; SOT188AA; SOT188CG	4813
PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2; SOT189CG	4814
QFP (quad flat package)			
QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1; SOT205A; SOT205AG	4815
QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2; SOT307B	4816
QFP48	plastic quad flat package; 48 leads (lead length 2.5 mm); body 10 × 10 × 1.75 mm	SOT196-1; SOT196A	4817
QFP64	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1; SOT208; SOT208A	4818
QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2; SOT319	4819
QFP80	plastic quad flat package; 80 leads (lead length 1.6 mm); body 14 × 20 × 3.0 mm	SOT310-1	4820
QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	4821
QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT317-1; SOT317 SOT317B4	4822
QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2	4823
SDIP (shrink dual in-line package)			
SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1; SOT234; SOT234AH; SOT234AH2	4824
SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1; SOT232; SOT232A; SOT232AG; SOT232AH	4825
SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1; SOT270	4826
SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1; SOT247; SOT247AG; SOT247AH	4827

NAME	DESCRIPTION	VERSION	PAGE
SIL (single in-line)			
SIL9MP	plastic single in-line medium power package; 9 leads	SOT142-1; SOT142	4828
SIL9P	plastic single in-line power package; 9 leads	SOT131-2; SOT131	4829
SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1; SOT110; SOT110B	4830
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1; SOT96A; 0174C	4831
SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1; SOT108A; 0175D	4832
SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1; SOT109; SOT109A; 0005D	4833
SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1; SOT162A	4834
SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1; SOT163; SOT163A; SOT163AG7	4835
SO20	plastic small outline package; 20 leads; body width 5.3 mm	SOT336-1	4836
SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1; SOT137; SOT137A; SOT137AH; SOT137AH1	4837
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1; SOT136; SOT136A	4838
SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1; SOT287; SOT287AH	4839
SSOP (shrink small outline package)			
SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1	4840
SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1; SOT266	4841
SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	4842
SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	4843
VSO (very small outline)			
VSO40	plastic very small outline package; 40 leads	SOT158-1; SOT158	4844

Note

1. In general SOT102 refers to SOT102-1 except for TDA3827 and TDA4670 where SOT102 refers to SOT102-2.

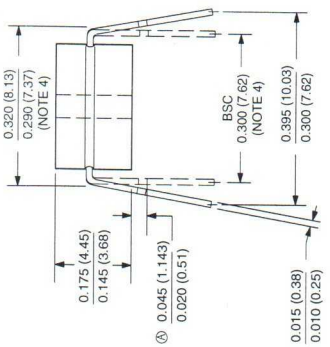
CDIP

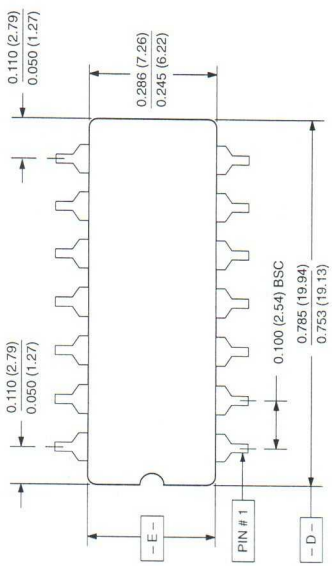
CDIP14: ceramic dual in-line package; 14 leads (300 mil)

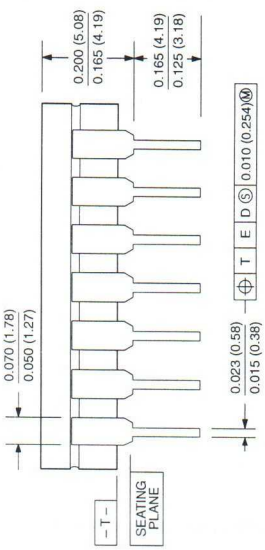
0581B

NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.



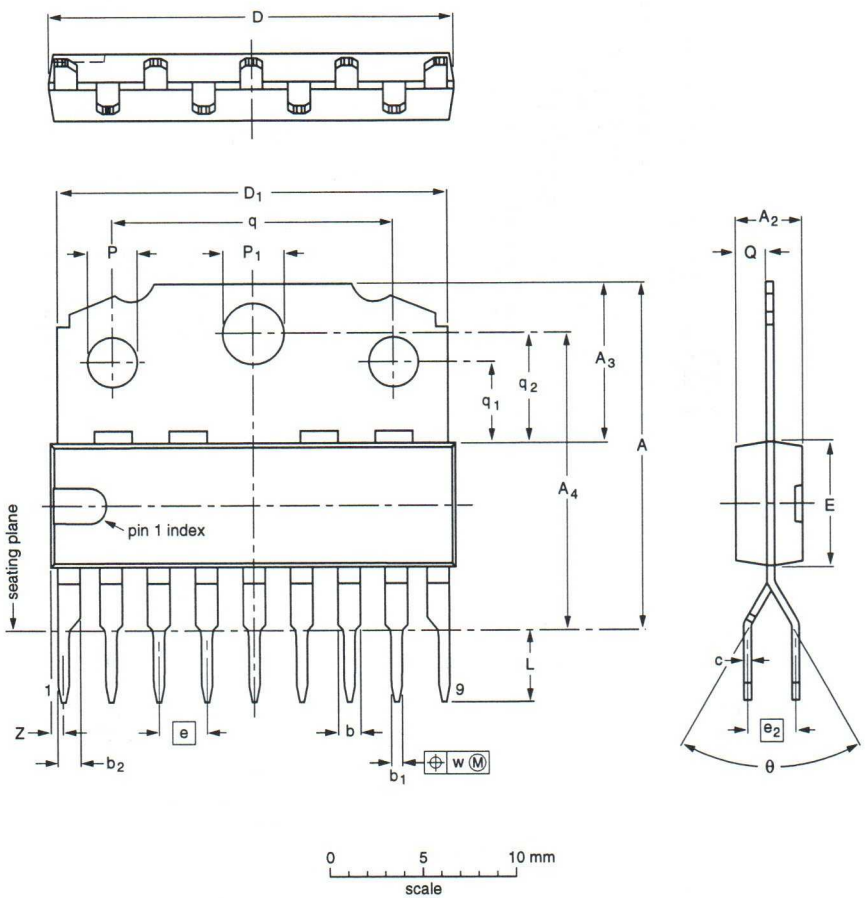




853-0581B 06688

DBS

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads SOT111-1



DIMENSIONS (mm are the original dimensions)

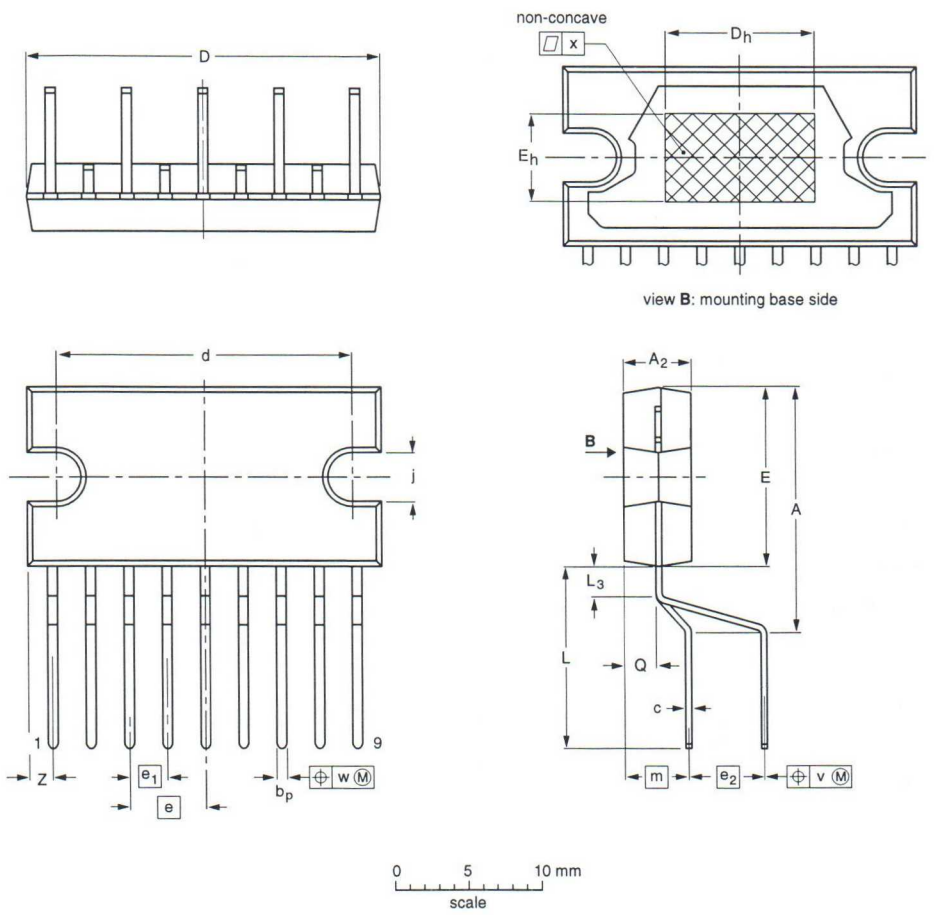
UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	e_2	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.	θ
mm	18.5 17.8	3.7	8.7 8.0	15.5 15.1	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0	65° 55°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT111-1						~~92-11-17~~ 95-03-11

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm) **SOT157-2**



DIMENSIONS (mm are the original dimensions)

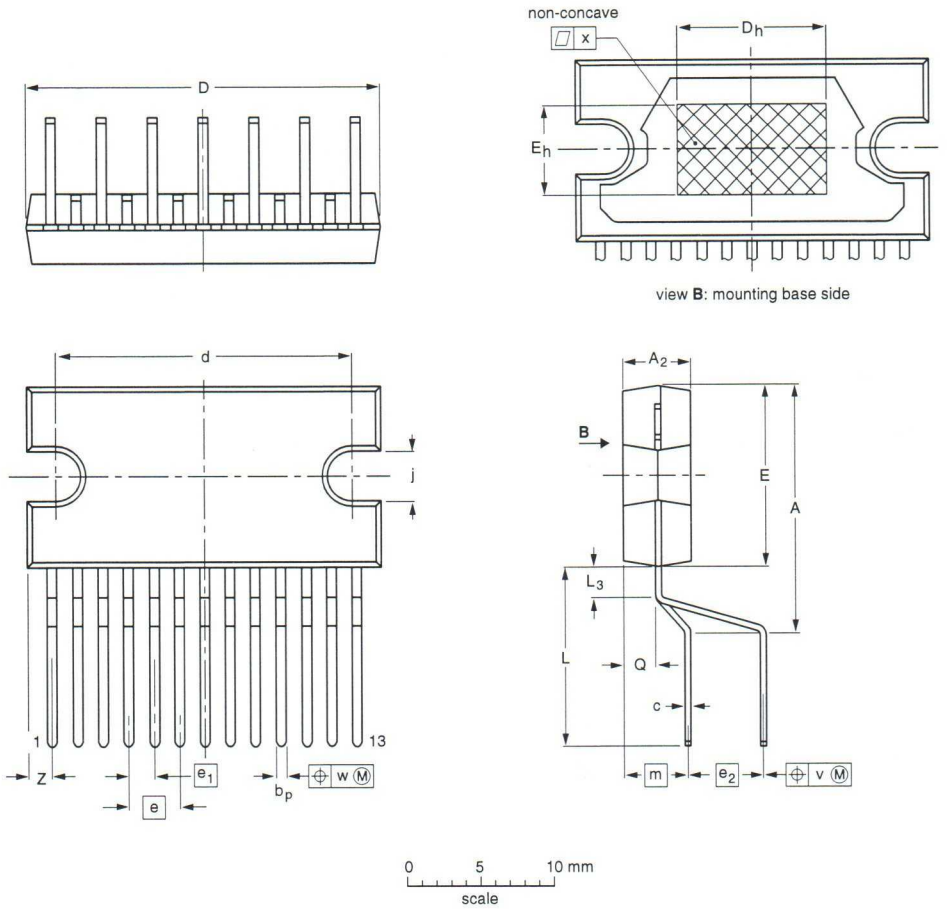
UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	5.08	2.54	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT157-2						~~92-10-12~~ 95-03-11

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

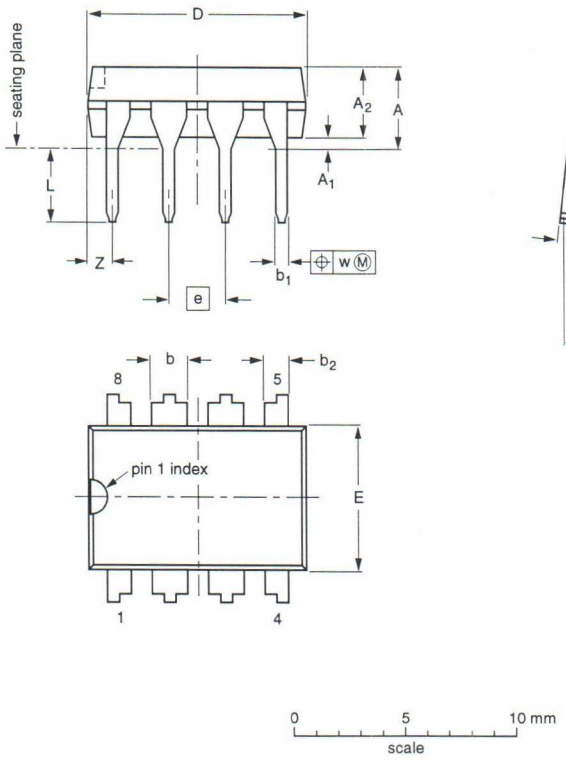
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~92-11-17~~ 95-03-11

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

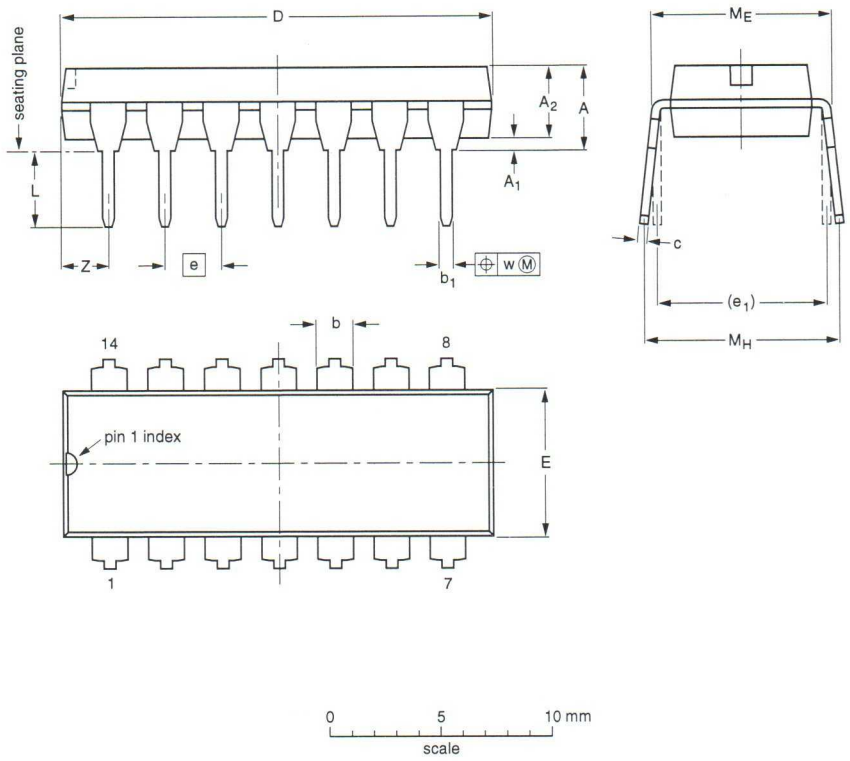
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

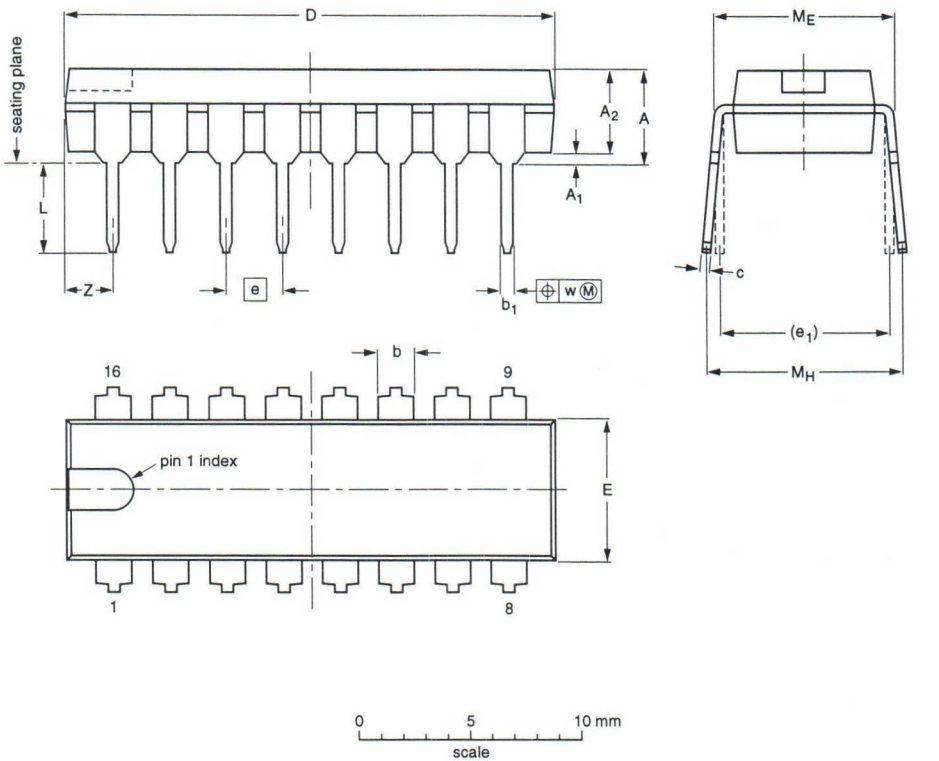
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

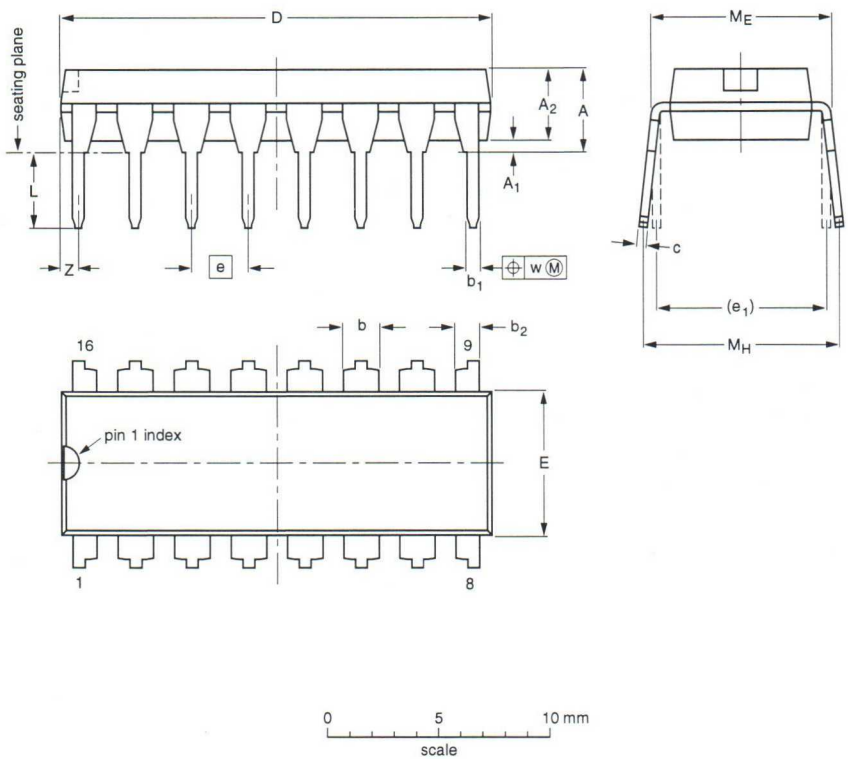
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

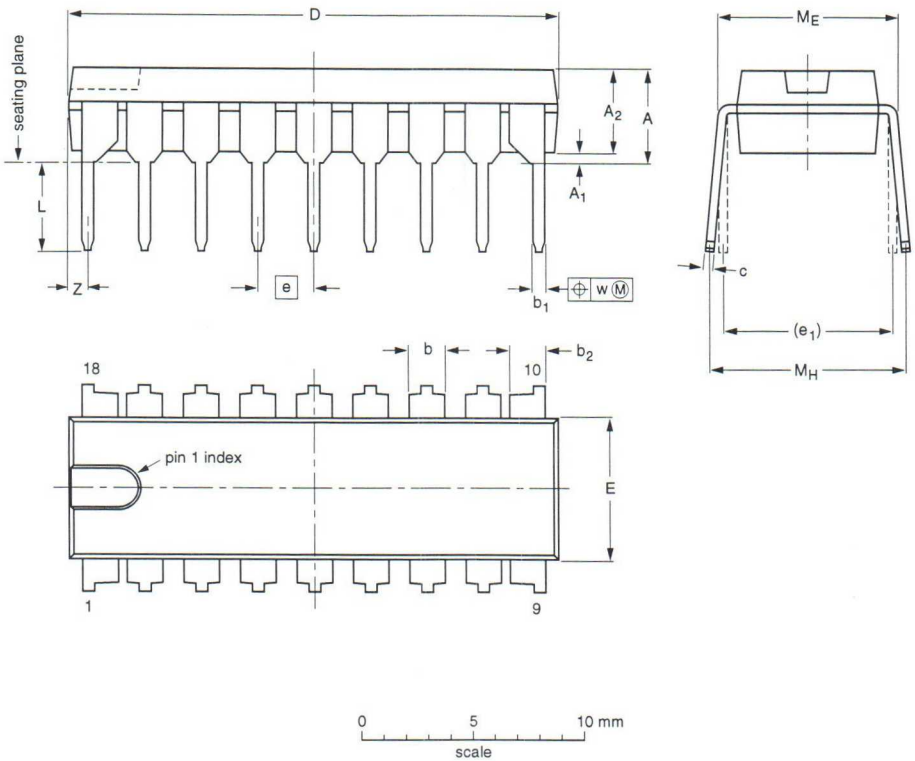
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

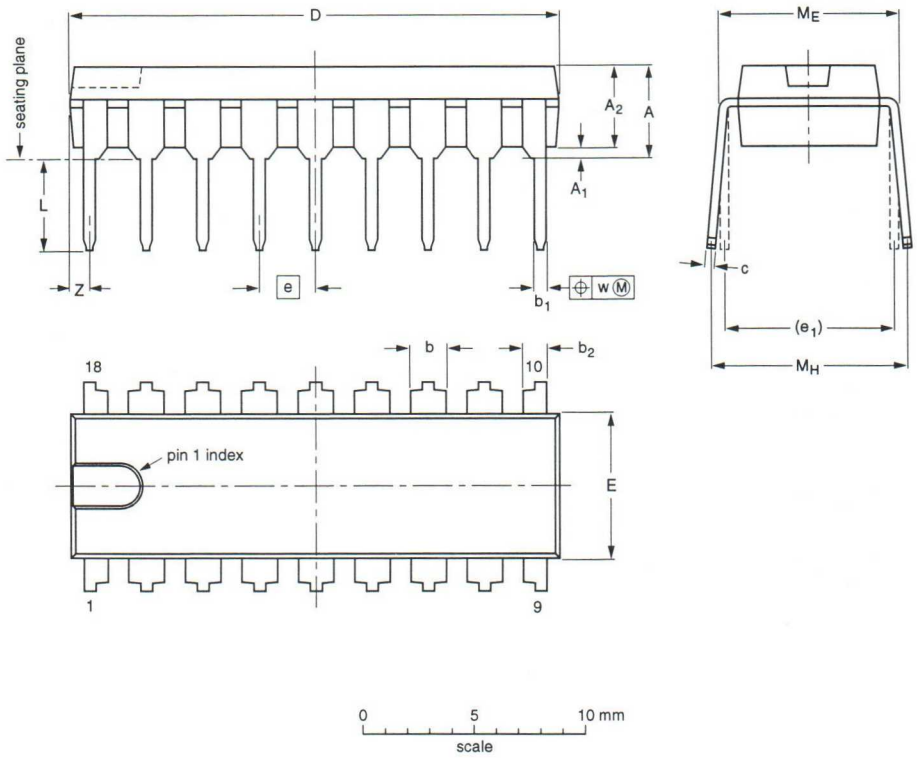
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

DIP18: plastic dual in-line package; 18 leads (300 mil); slim corner leads **SOT102-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.05 0.75	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.041 0.030	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

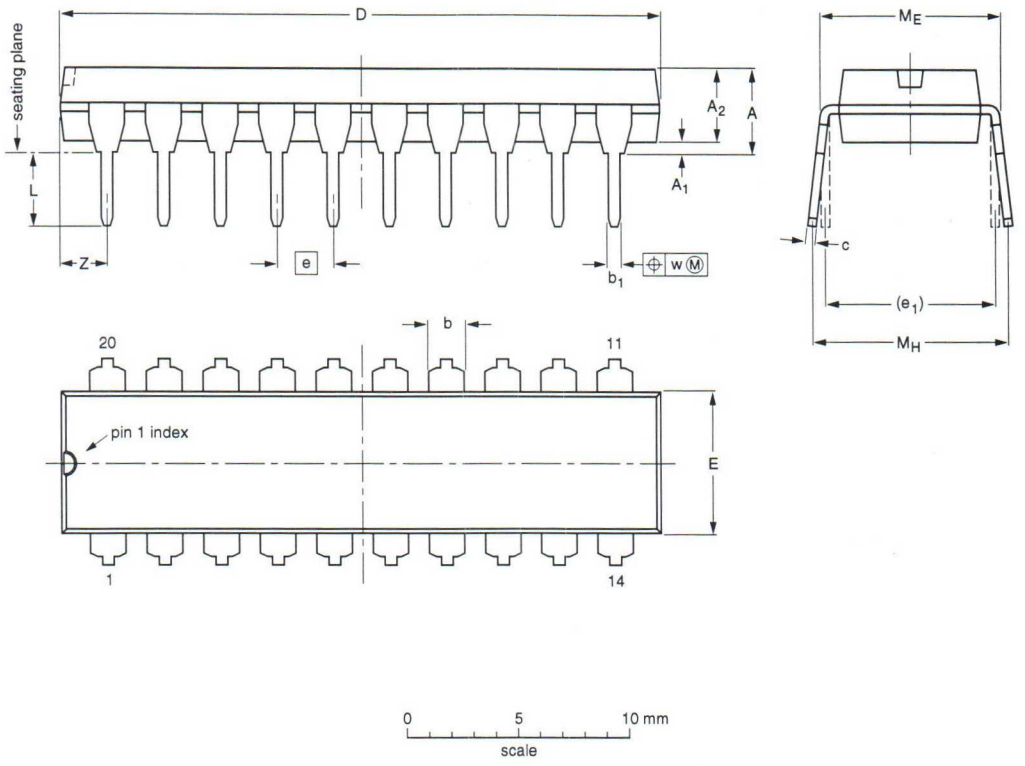
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-2						~~93-10-14~~ 95-01-23

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

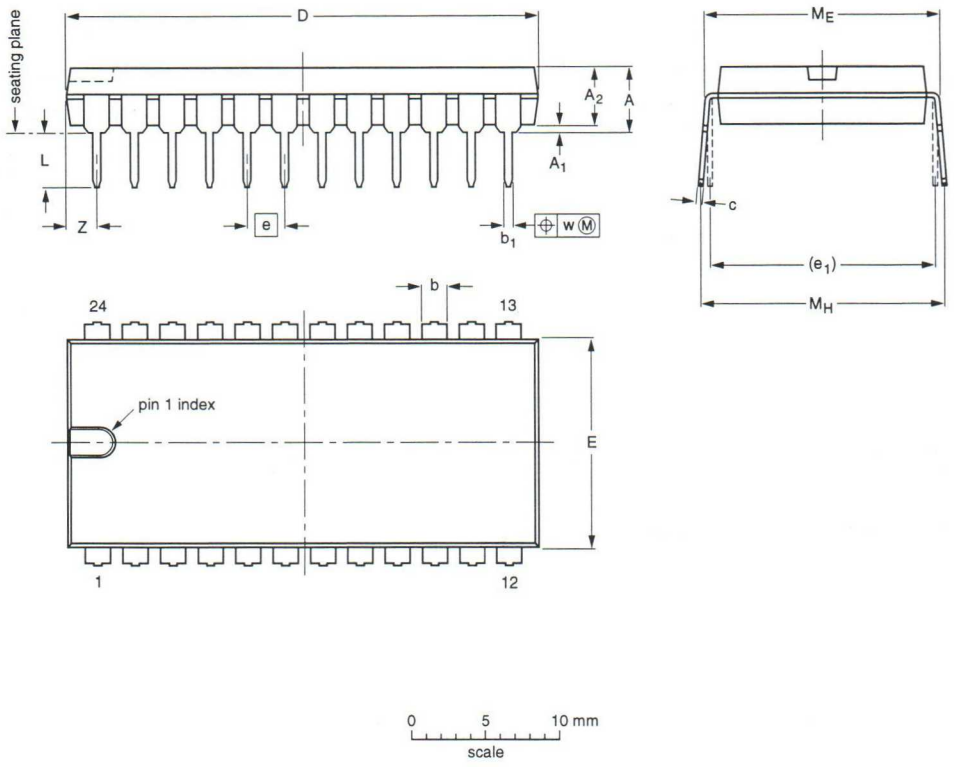
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-03-11

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

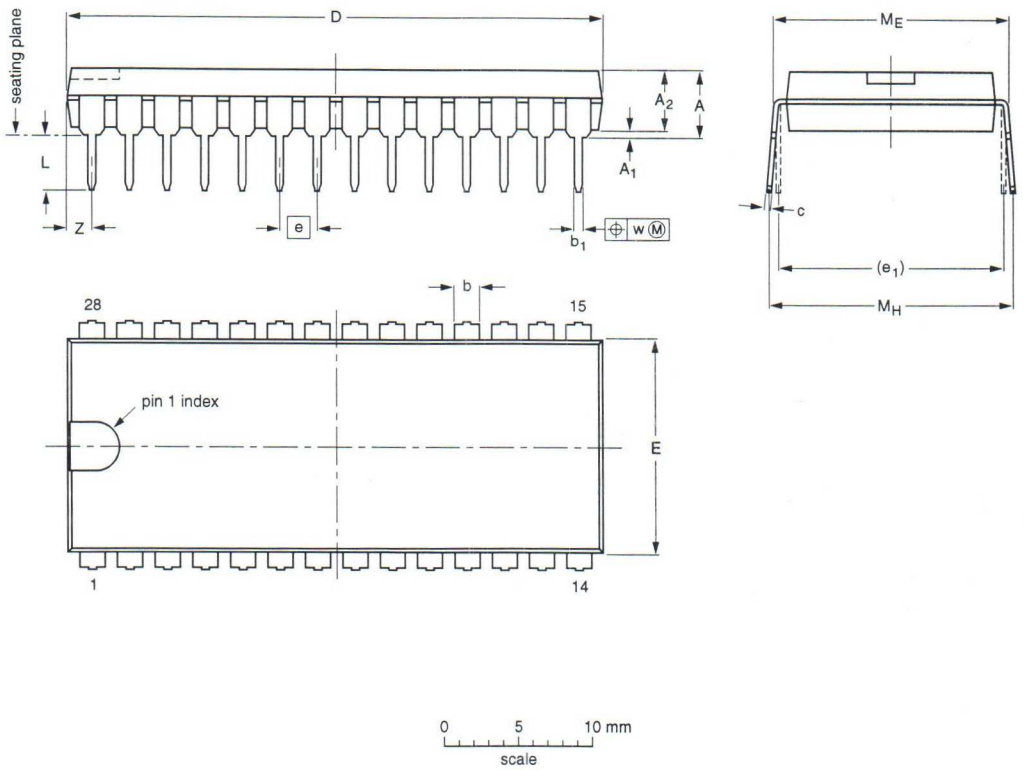
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

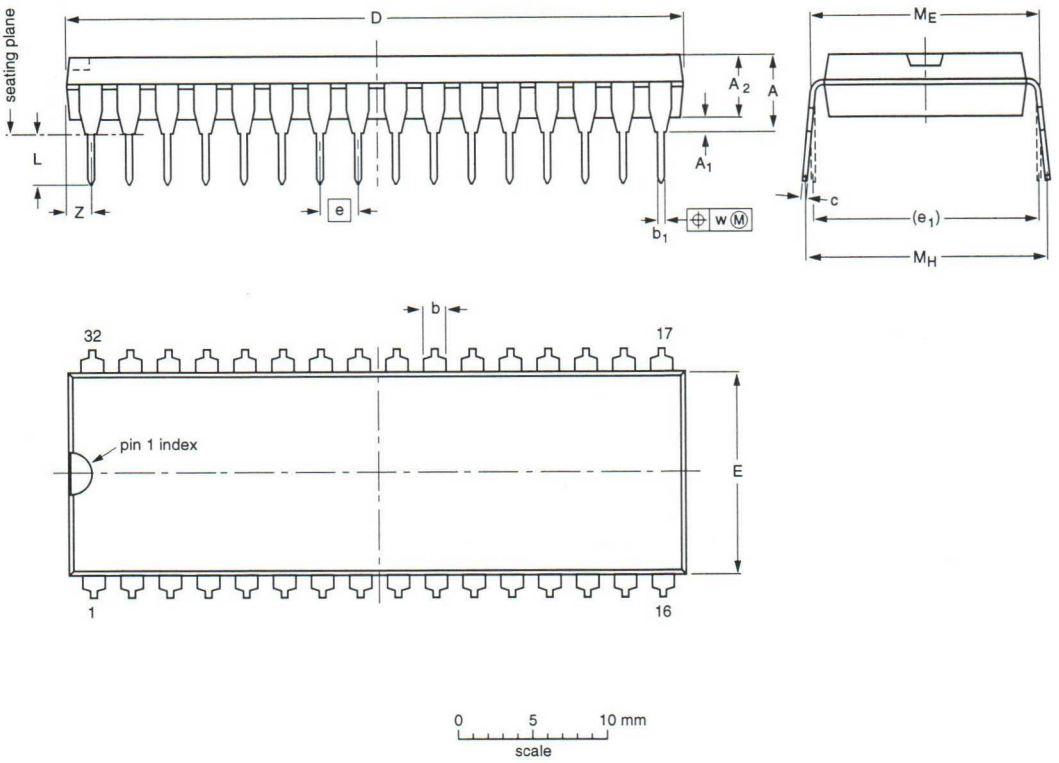
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP32: plastic dual in-line package; 32 leads (600 mil) **SOT201-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

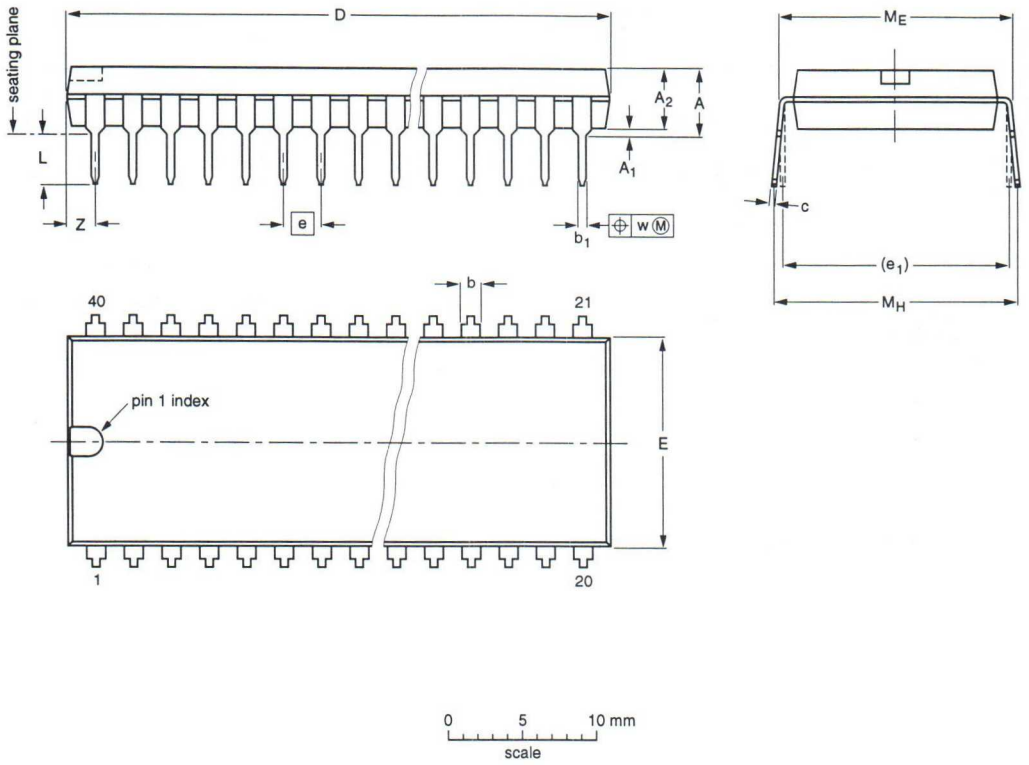
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.0	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	41.6 40.6	14.2 13.8	2.54	15.24	3.6 3.2	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.64 1.60	0.56 0.54	0.10	0.60	0.14 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT201-1						~~90-01-22~~ 95-01-25

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

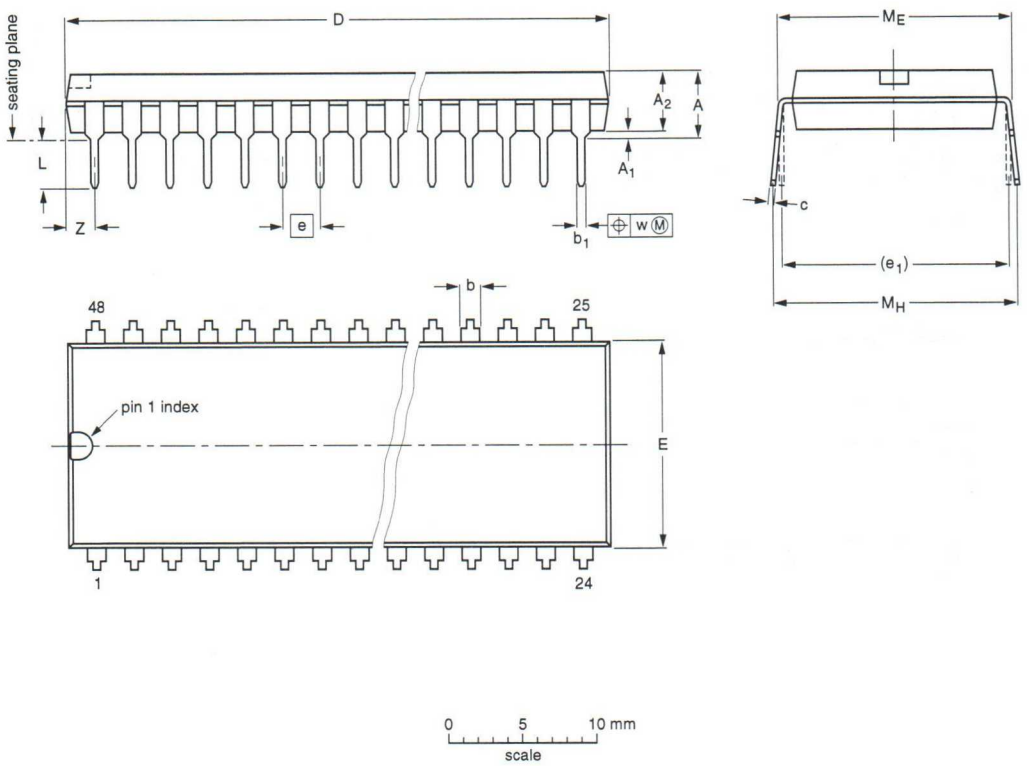
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

DIP48: plastic dual in-line package; 48 leads (600 mil)

SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

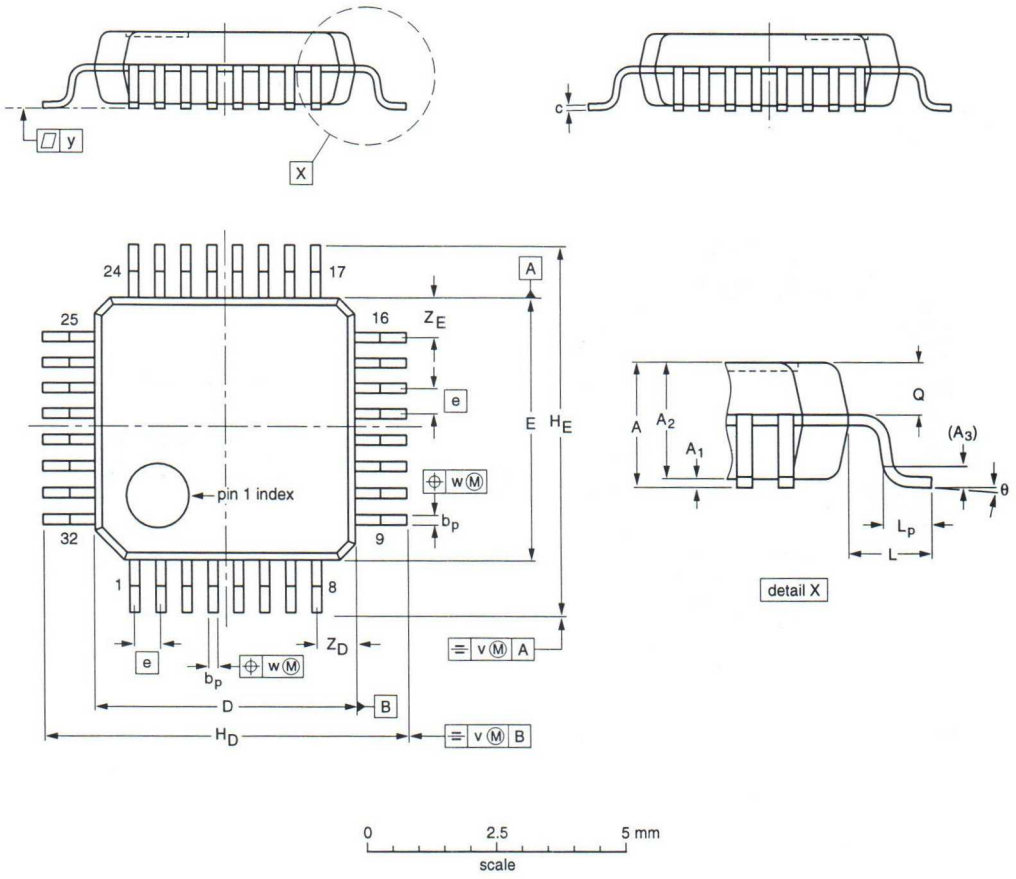
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

LQFP

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm

SOT401-1



DIMENSIONS (mm are the original dimensions)

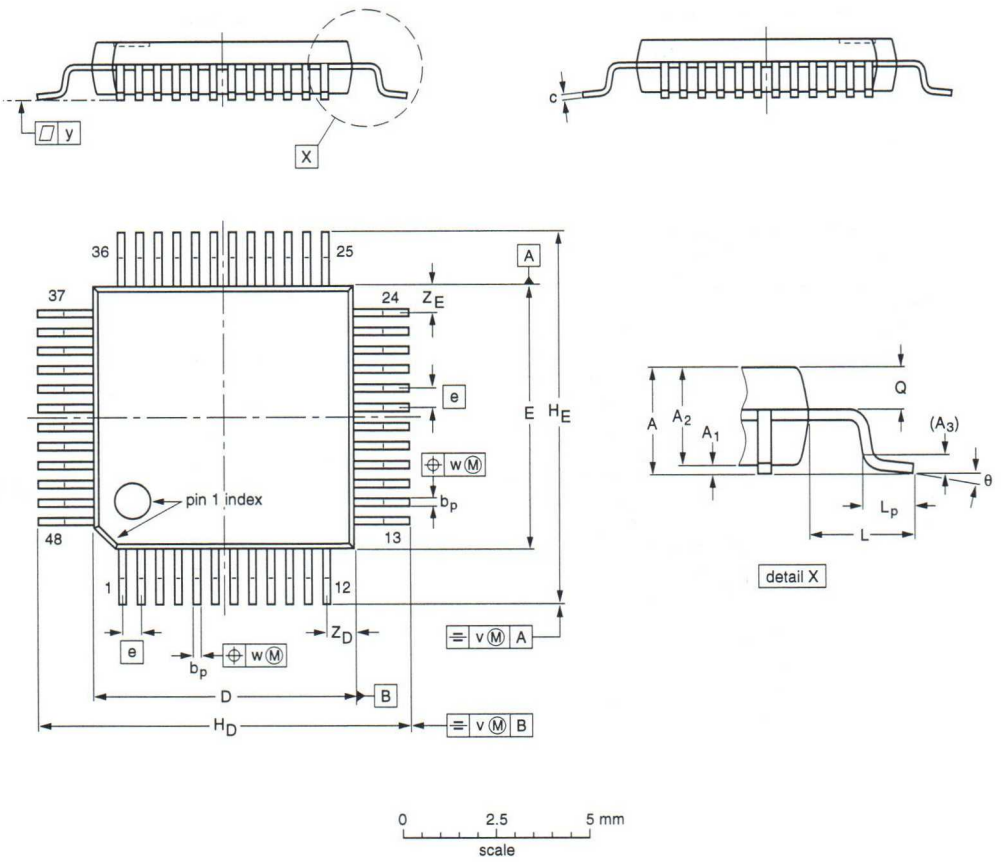
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~94-04-25~~ 95-02-28

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

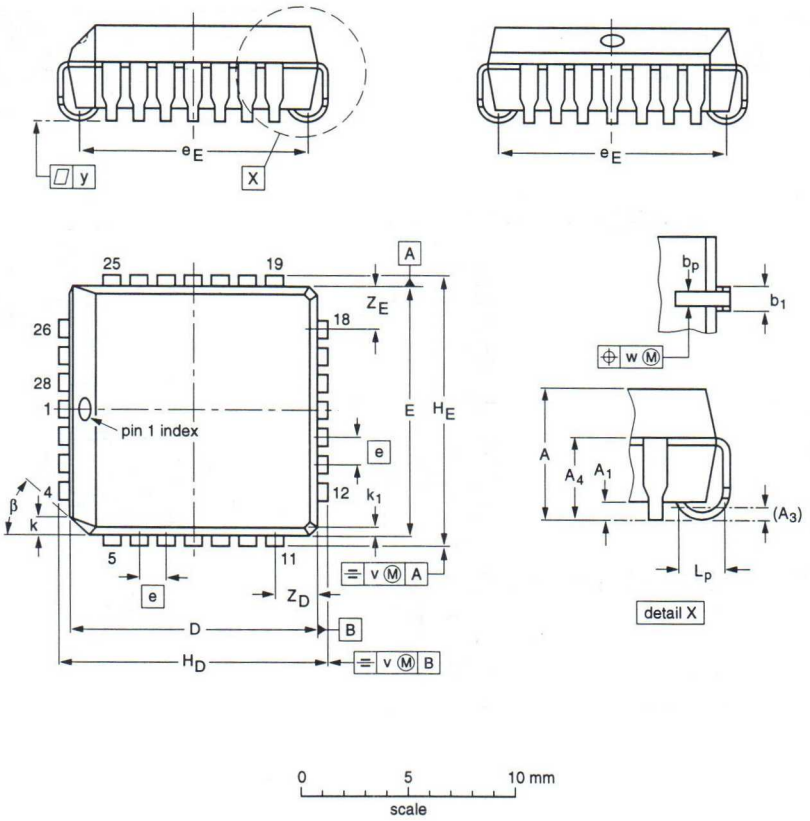
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-02-25

PLCC

PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

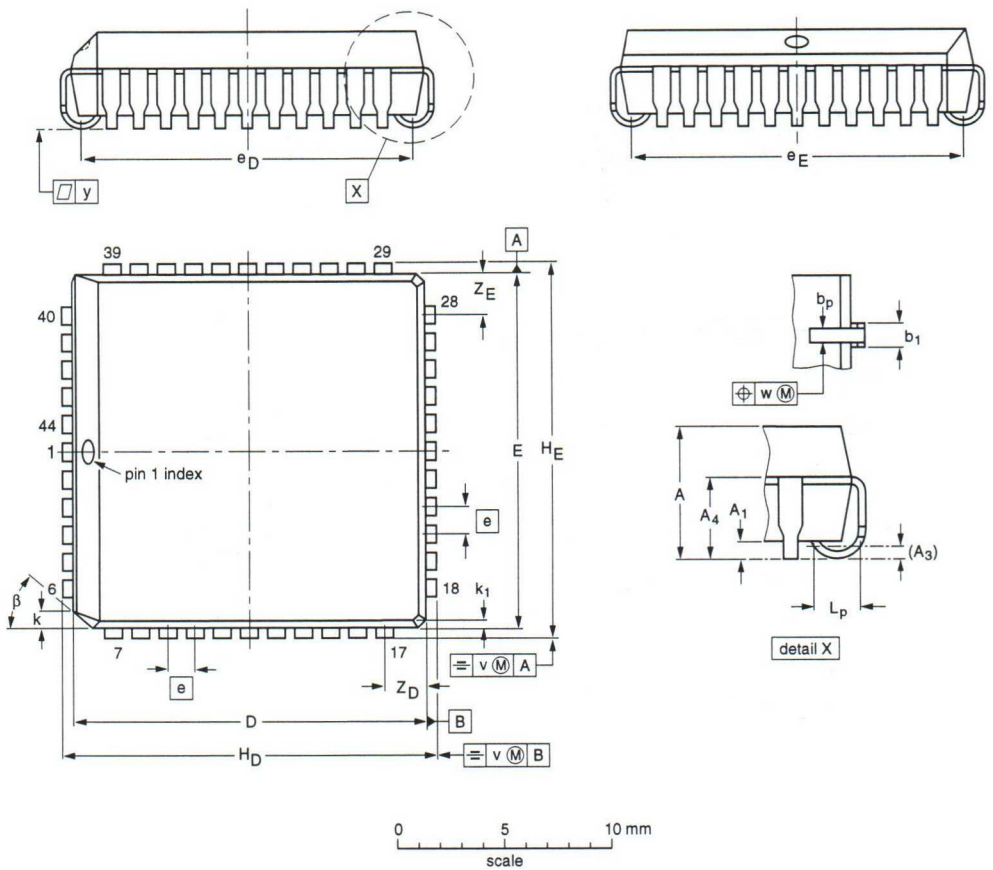
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

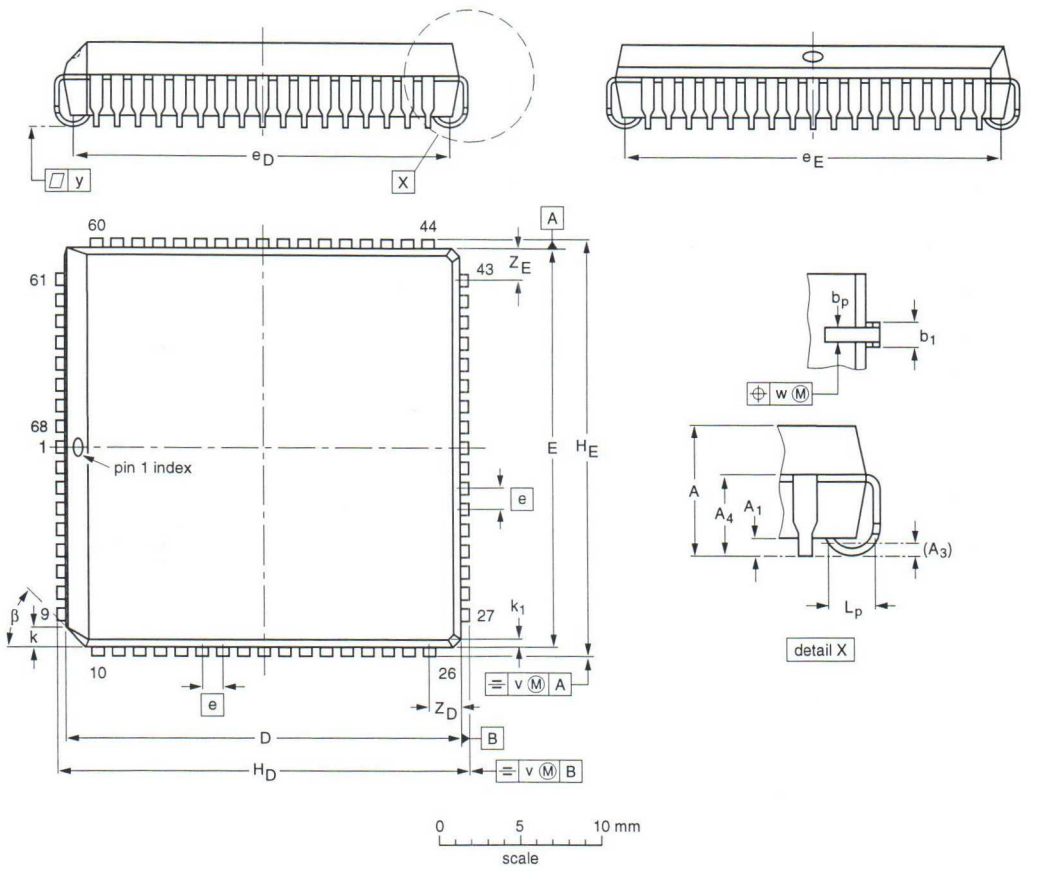
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

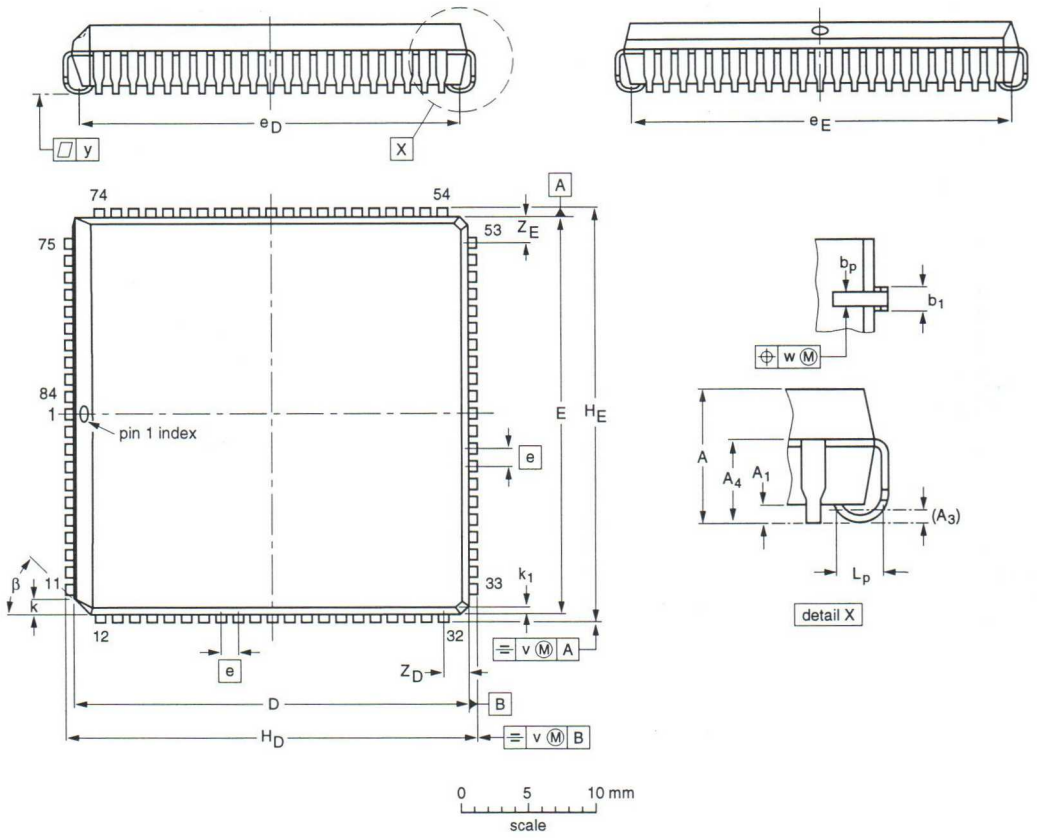
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

PLCC84: plastic leaded chip carrier; 84 leads

SOT189-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

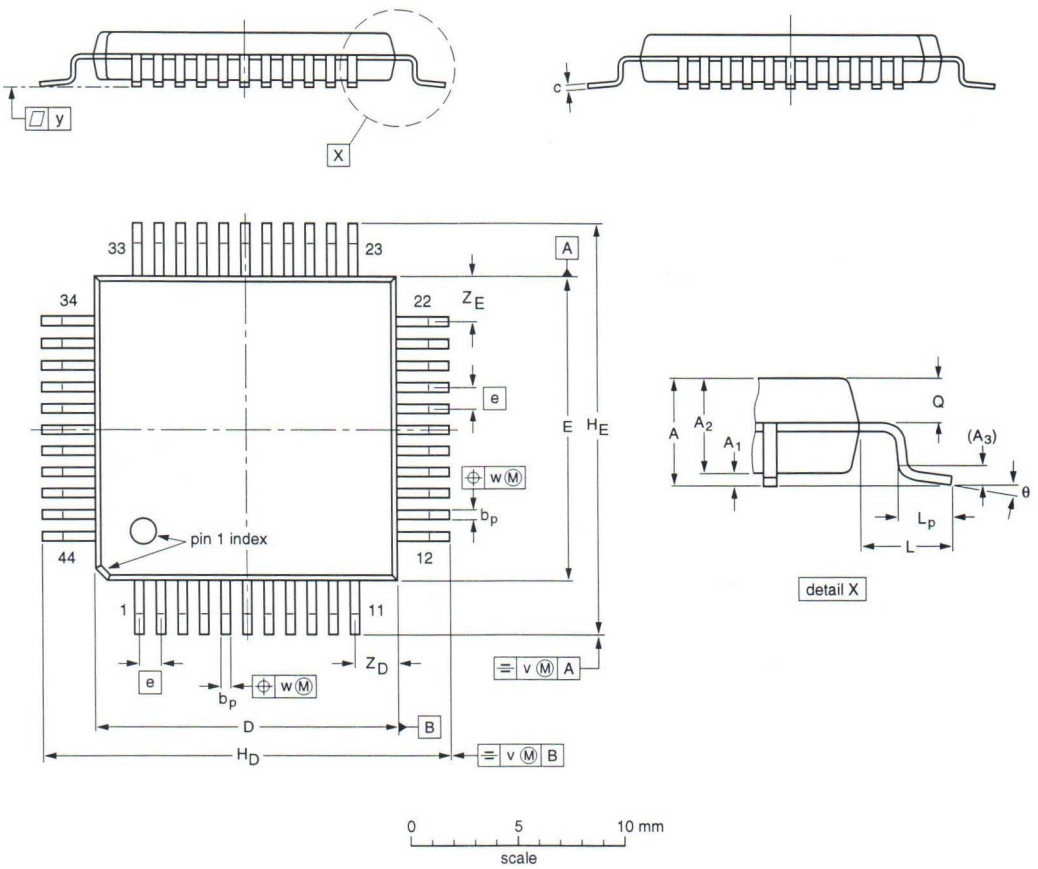
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-2						~~92-11-17~~ 95-03-11

QFP

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm SOT205-1



DIMENSIONS (mm are the original dimensions)

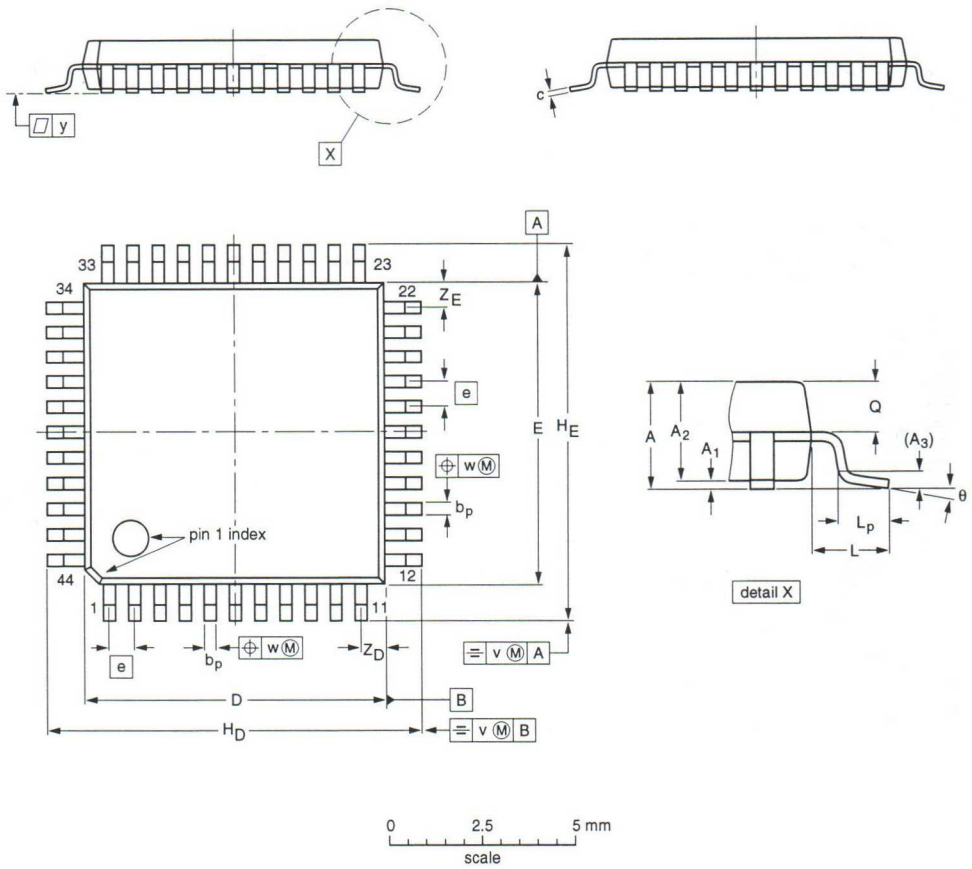
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

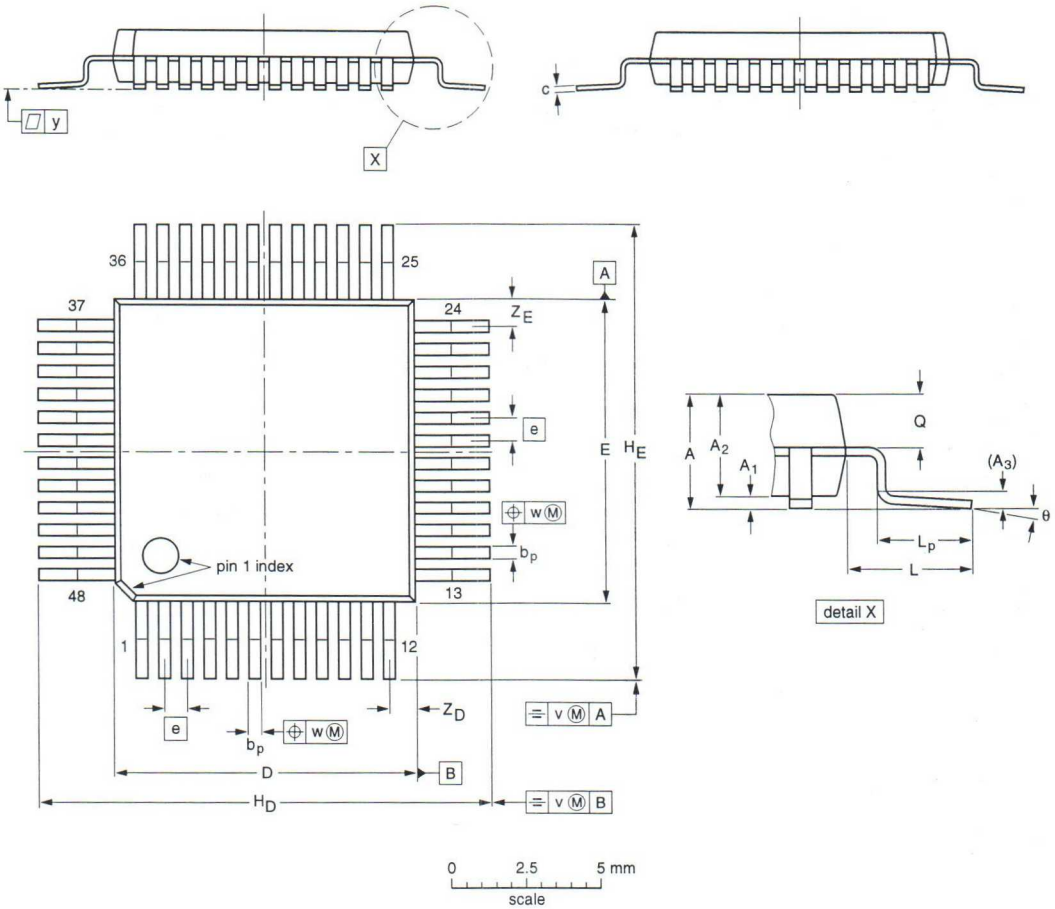
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

QFP48: plastic quad flat package; 48 leads (lead length 2.5 mm); body 10 x 10 x 1.75 mm **SOT196-1**



DIMENSIONS (mm are the original dimensions)

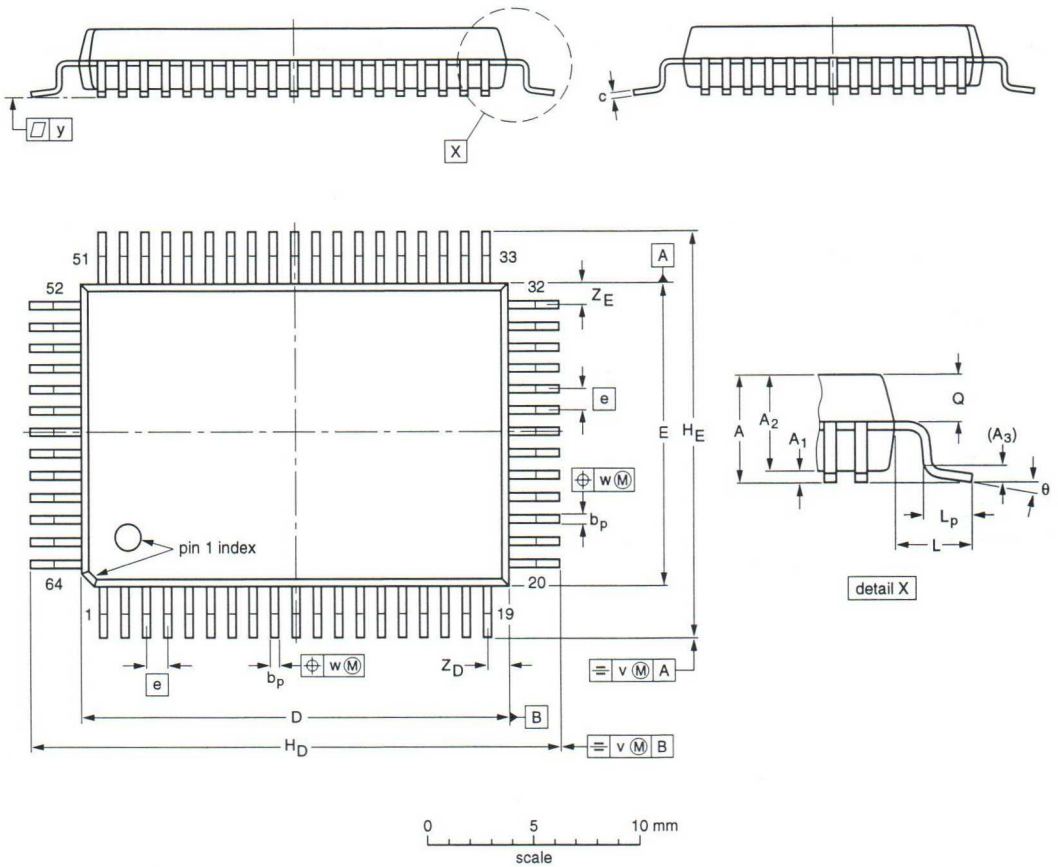
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.20	0.3 0.1	1.85 1.65	0.25	0.42 0.28	0.25 0.14	10.1 9.9	10.1 9.9	0.75	15.5 14.5	15.5 14.5	2.5	2.4 1.6	1.05 0.75	0.3	0.15	0.1	1.05 0.70	1.05 0.70	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT196-1						~~92-11-17~~ 95-02-04

QFP64: plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 x 20 x 2.75 mm **SOT208-1**



DIMENSIONS (mm are the original dimensions)

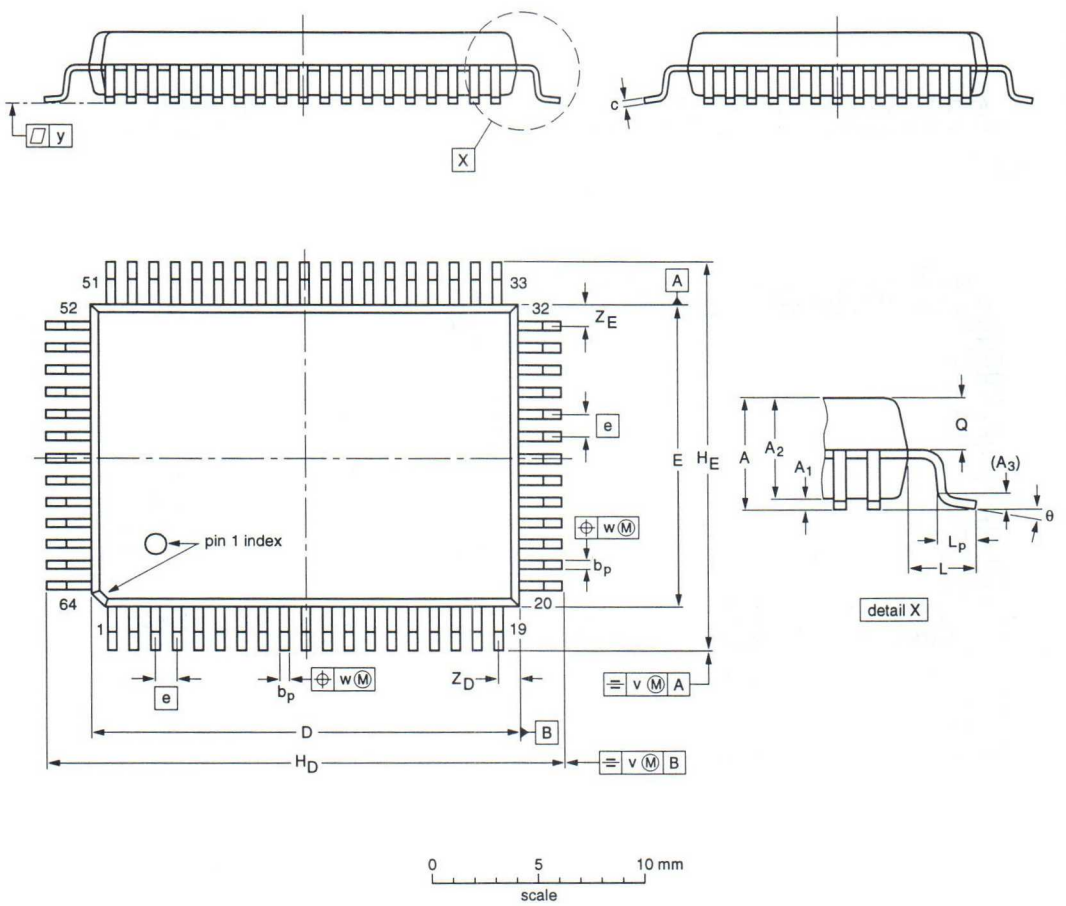
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.30 0.05	2.85 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	25.2 24.2	19.2 18.2	2.35	1.55 0.85	1.45 1.15	0.3	0.15	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT208-1	133E02C					~~92-11-17~~ 95-02-04

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

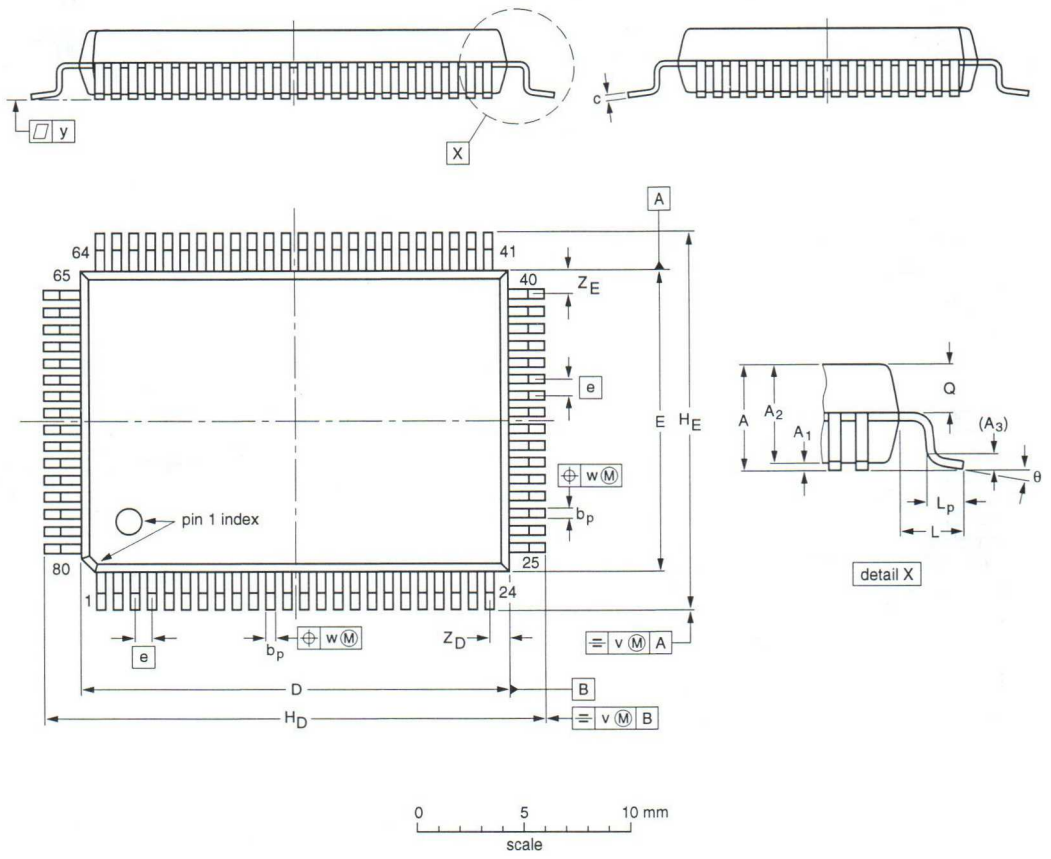
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

QFP80: plastic quad flat package; 80 leads (lead length 1.6 mm); body 14 x 20 x 3.0 mm **SOT310-1**



DIMENSIONS (mm are the original dimensions)

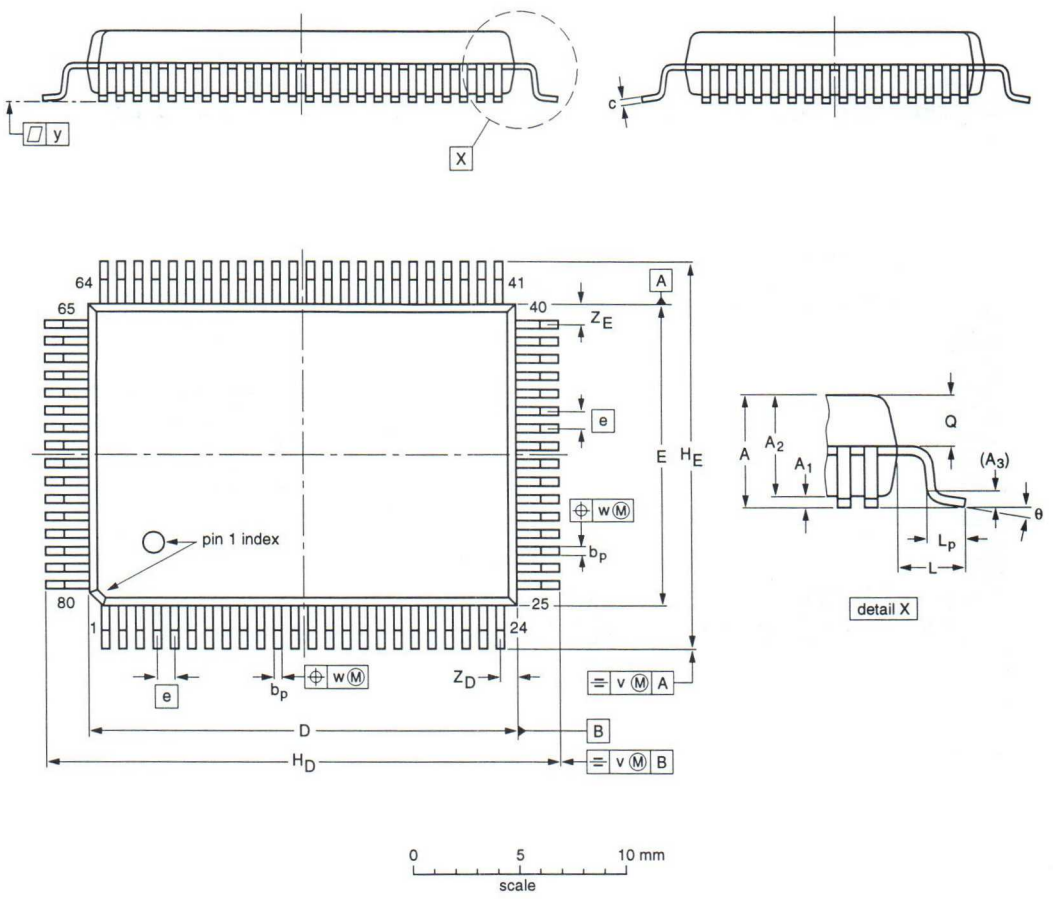
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.4	0.2 0	3.2 2.8	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	23.6 22.8	17.6 16.8	1.6	1.1 0.5	1.55 1.25	0.3	0.15	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT310-1						~~92-06-30~~ 95-02-04

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

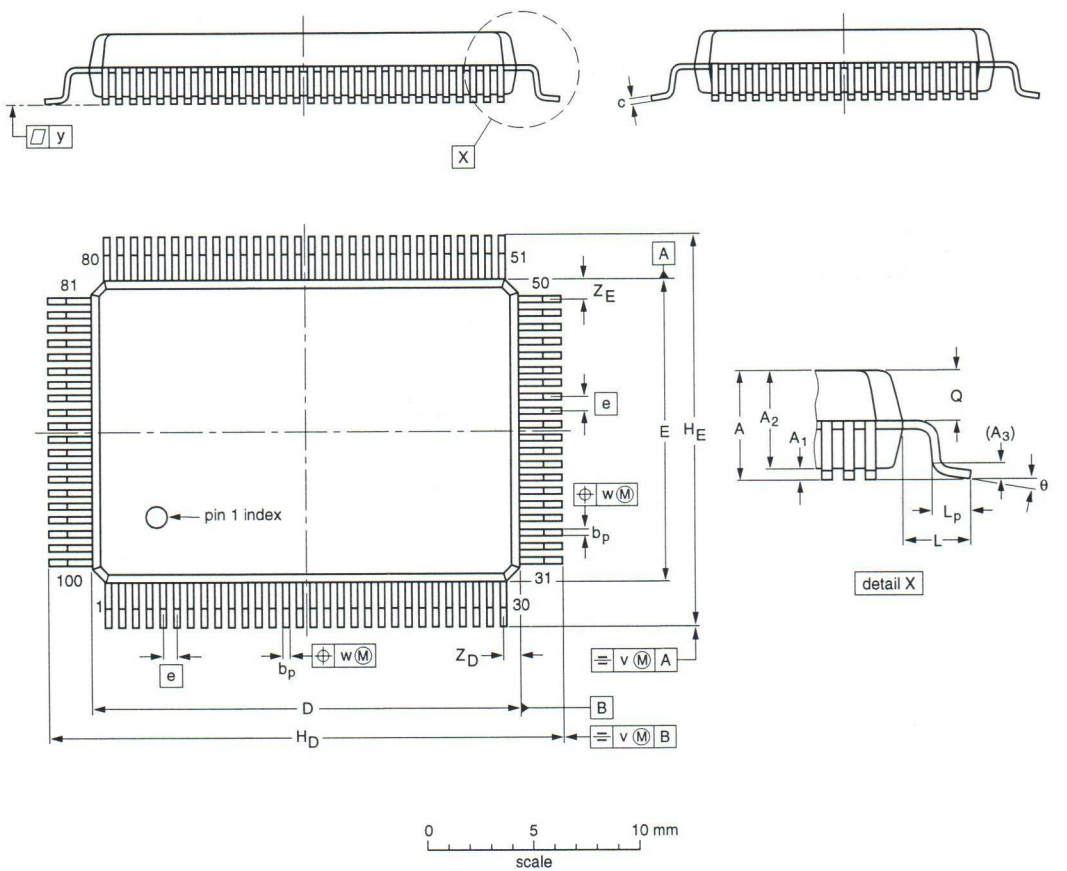
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~92-12-15~~ 95-02-04

QFP100: plastic quad flat package;
100 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT317-1**



DIMENSIONS (mm are the original dimensions)

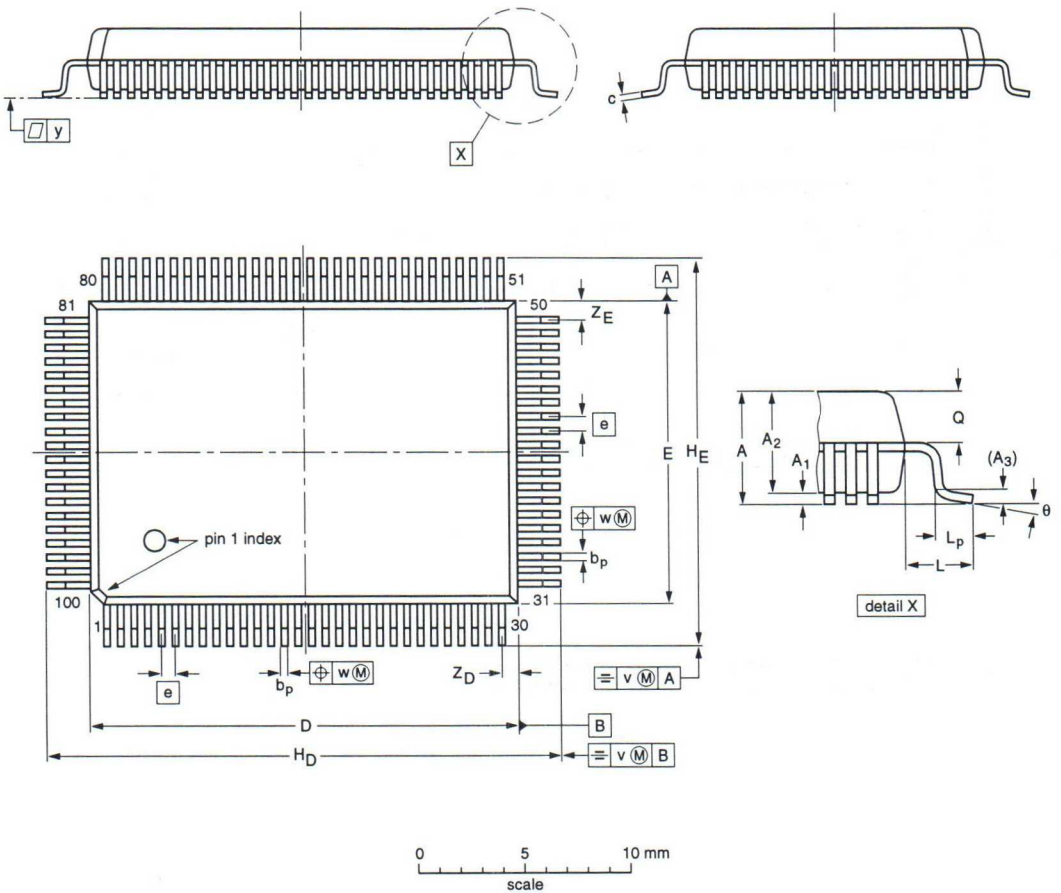
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.40 0.25	0.25 0.13	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.43 1.23	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-1						~~92-11-17~~ 95-02-04

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

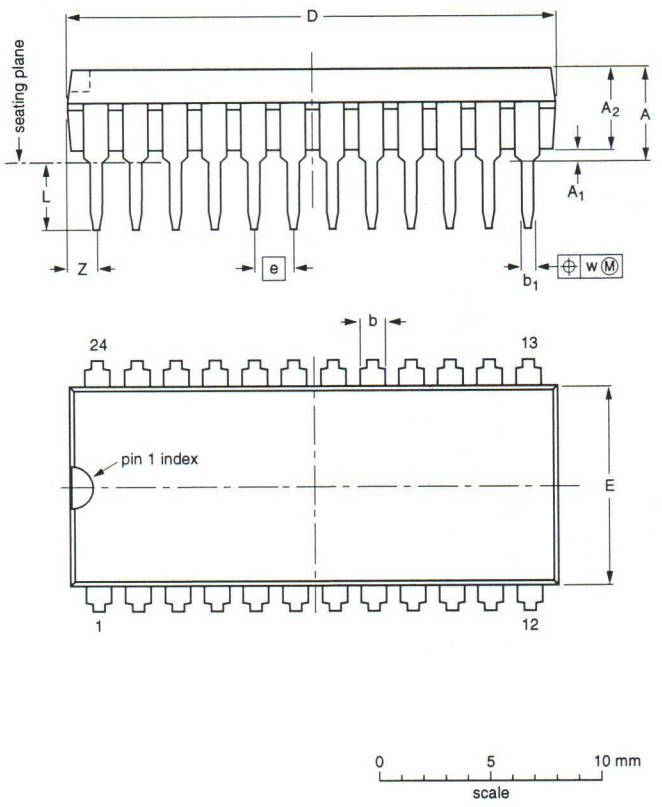
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~92-11-17~~ 95-02-04

SDIP

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil)

SOT234-1



DIMENSIONS (mm are the original dimensions)

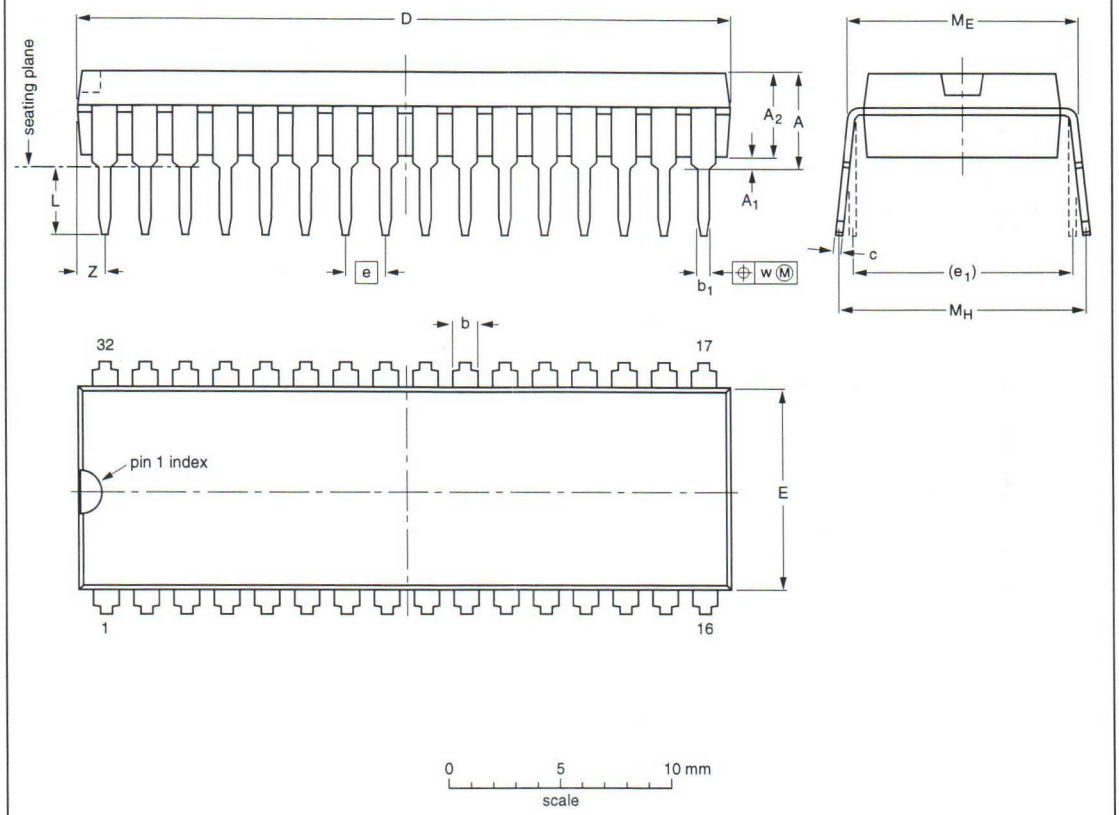
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

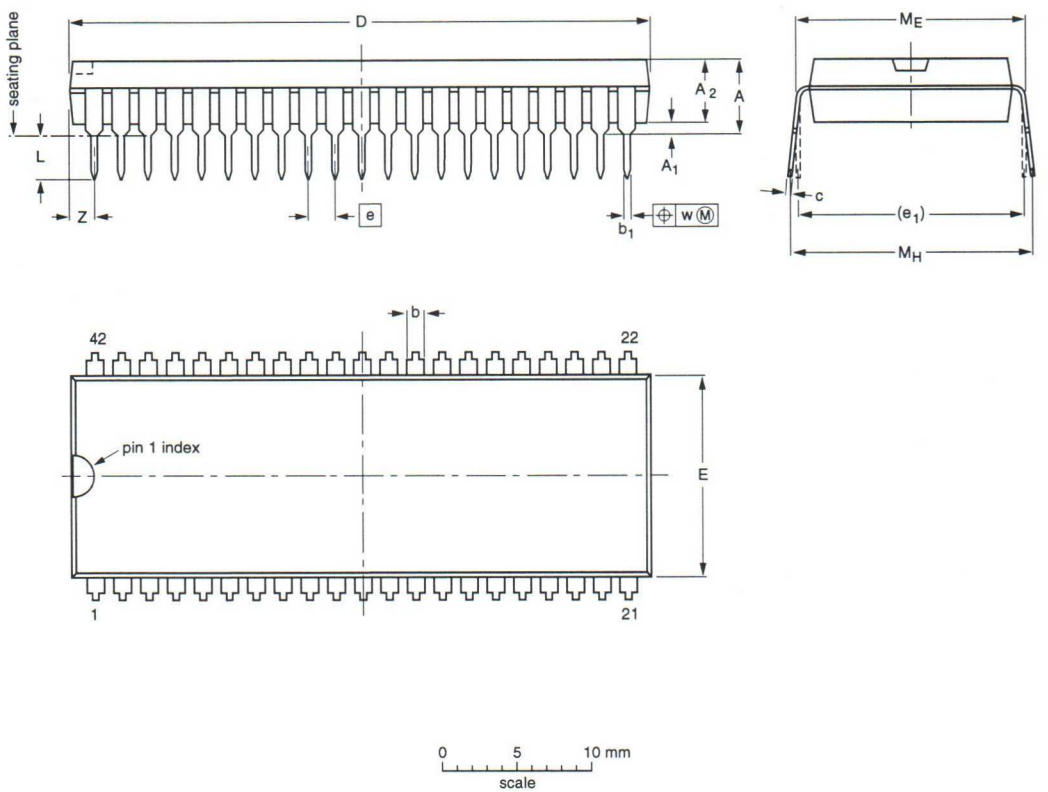
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

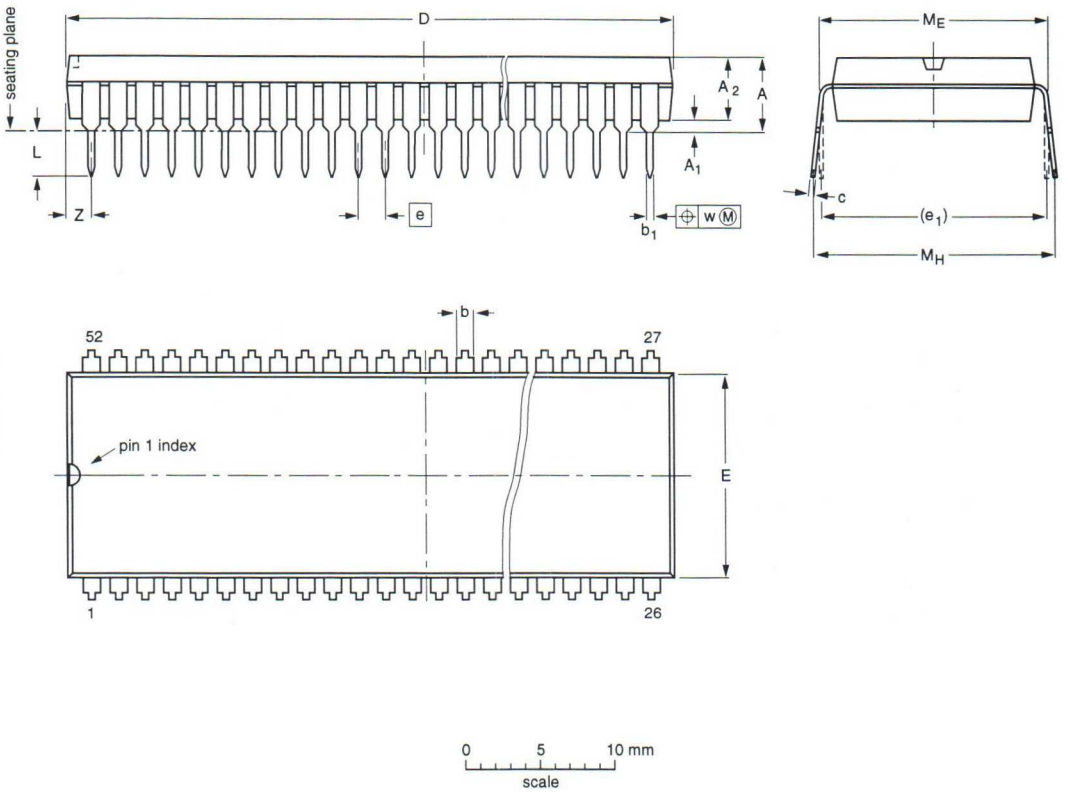
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

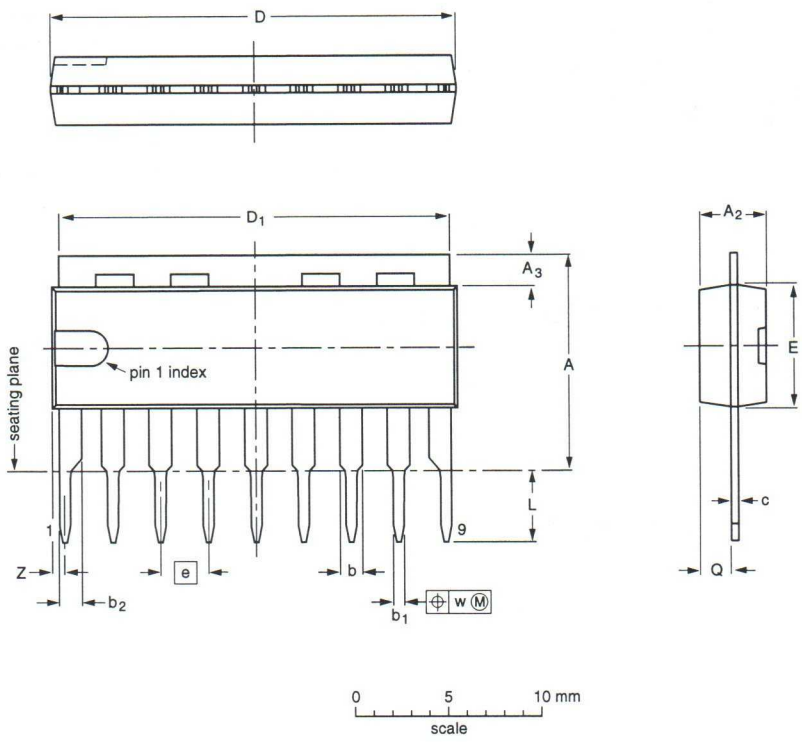
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

SIL

SIL9MP: plastic single in-line medium power package; 9 leads SOT142-1



DIMENSIONS (mm are the original dimensions)

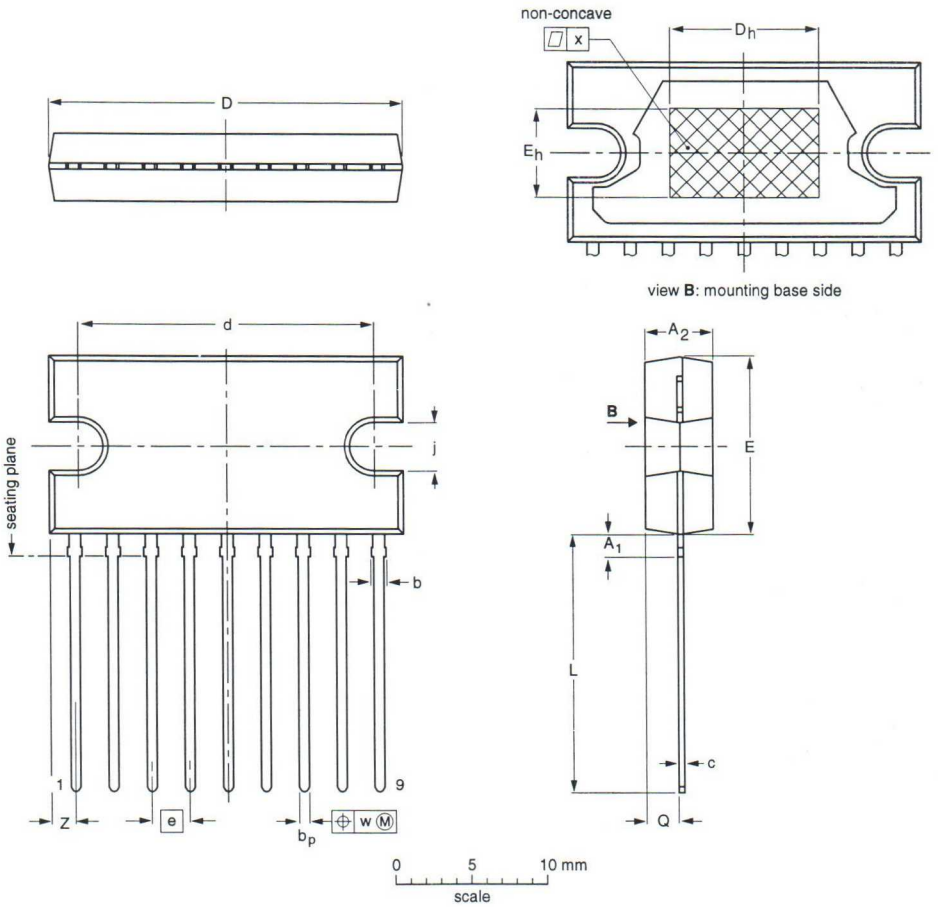
UNIT	A	A_2 max.	A_3	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	Q	w	$Z^{(1)}$ max.
mm	12 11	3.7	1.8 1.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	1.75 1.55	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT142-1						~~92-11-17~~ 95-02-09

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

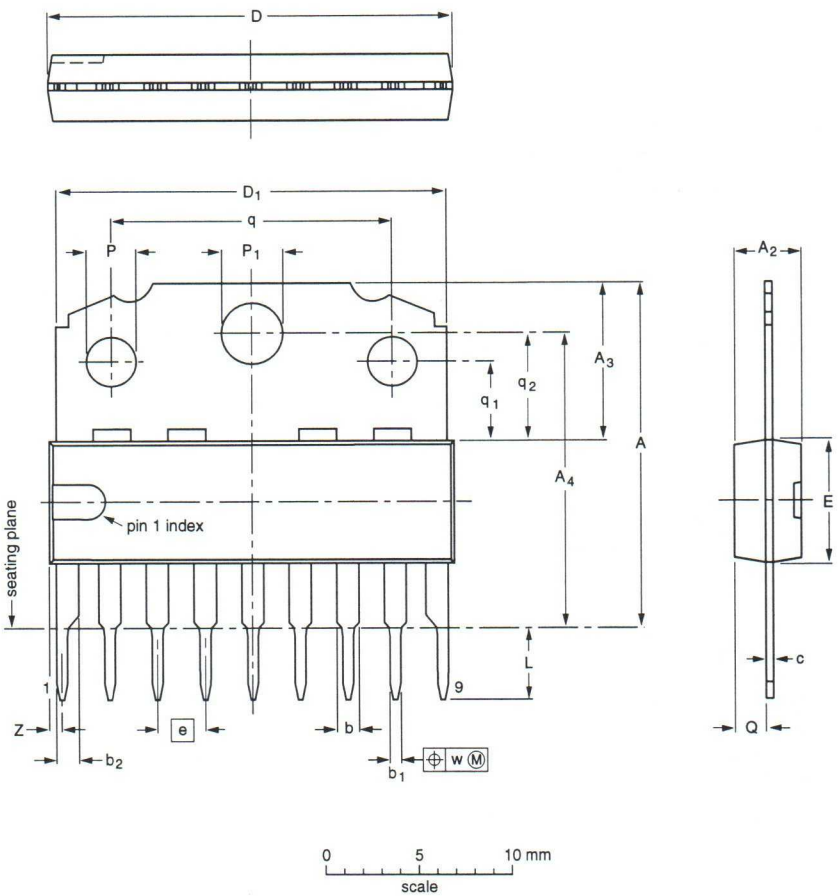
UNIT	A_1 max.	A_2	b max.	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	Q	w	x	$Z^{(1)}$
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

SIL9MPF: plastic single in-line medium power package with fin; 9 leads **SOT110-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

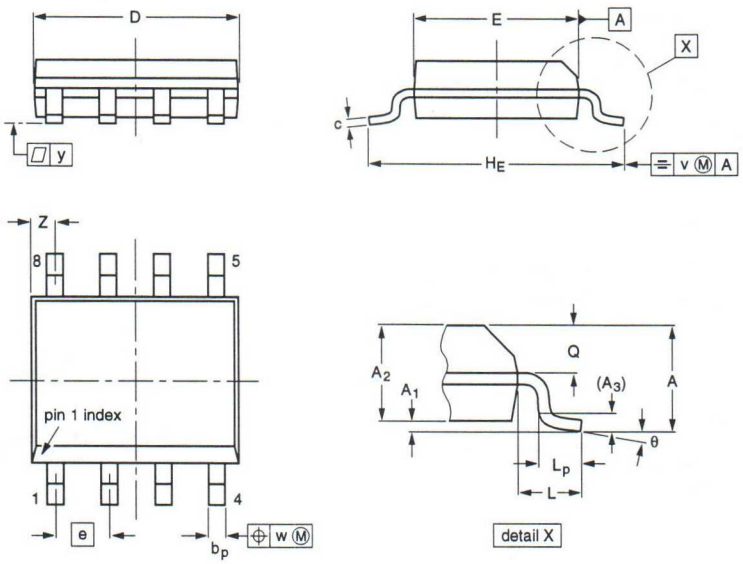
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						~~92-11-17~~ 95-02-25

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

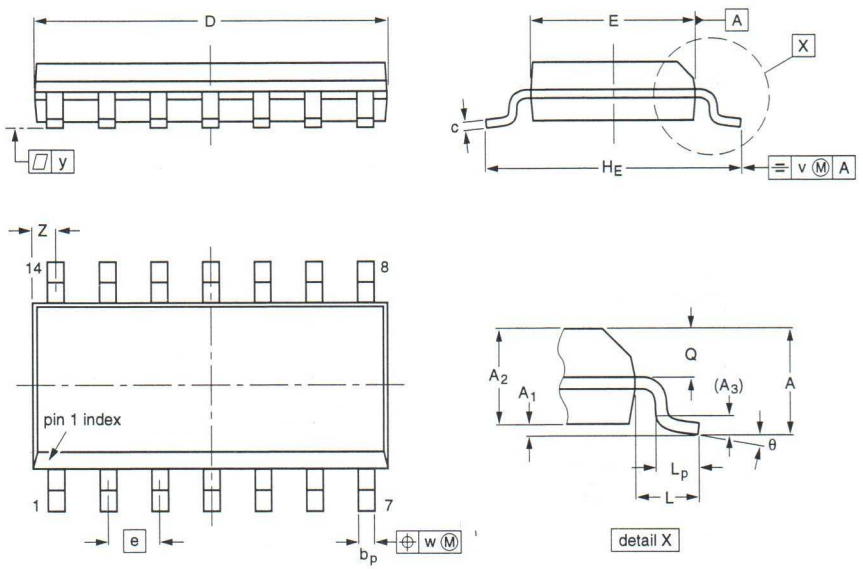
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

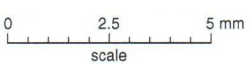
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

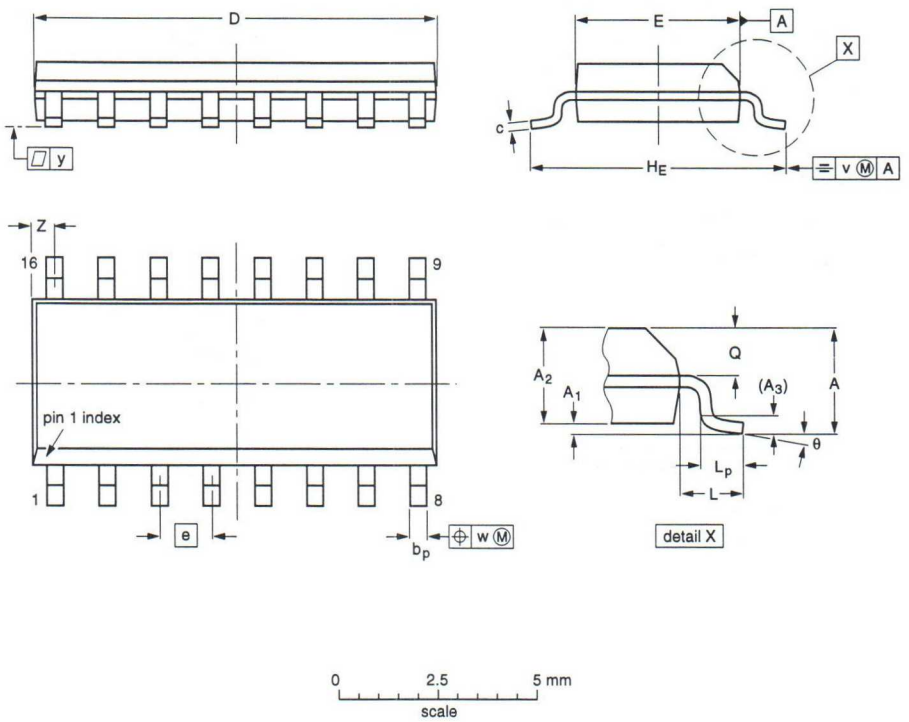
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

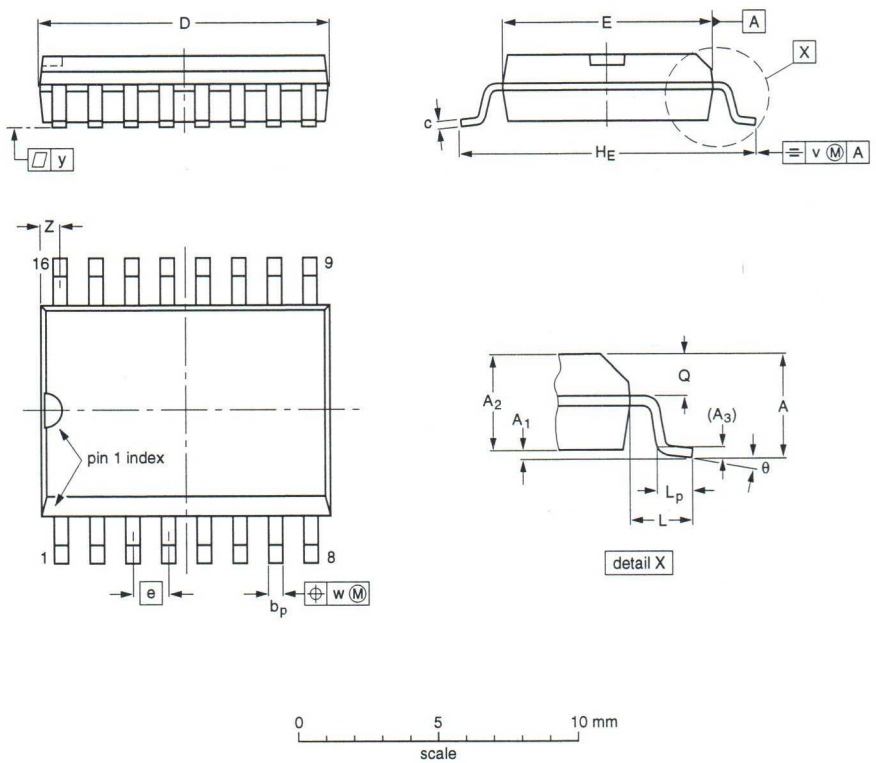
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

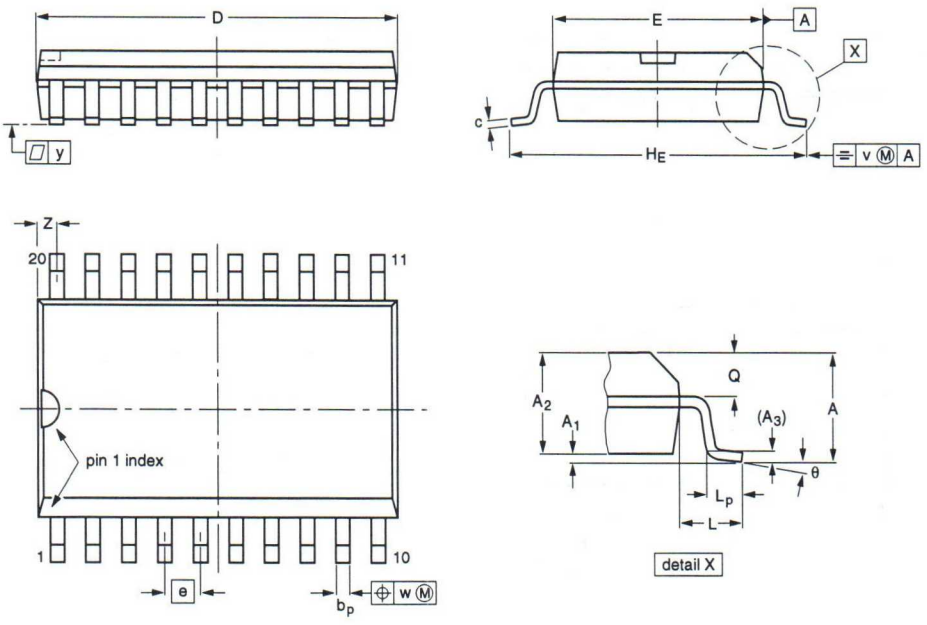
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

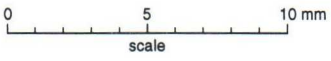
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

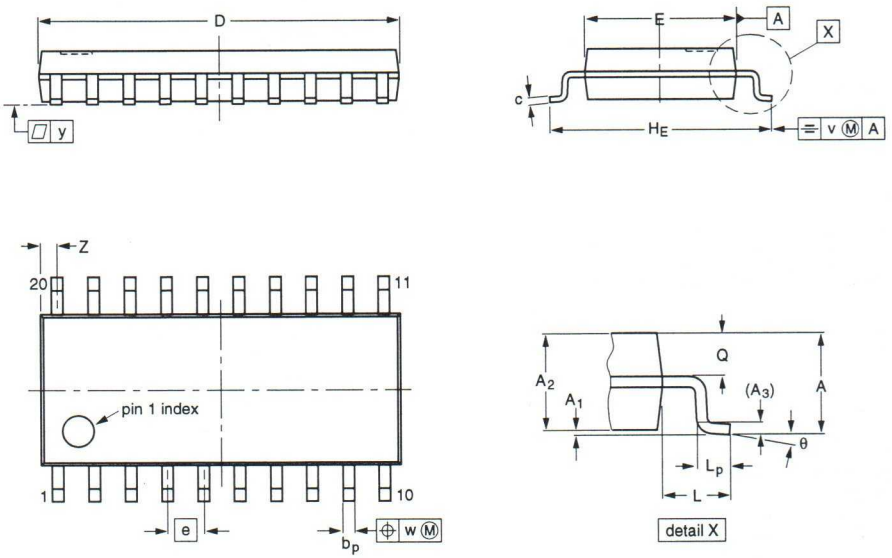
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

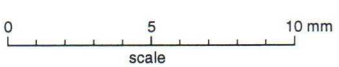
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SO20: plastic small outline package; 20 leads; body width 5.3 mm **SOT336-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

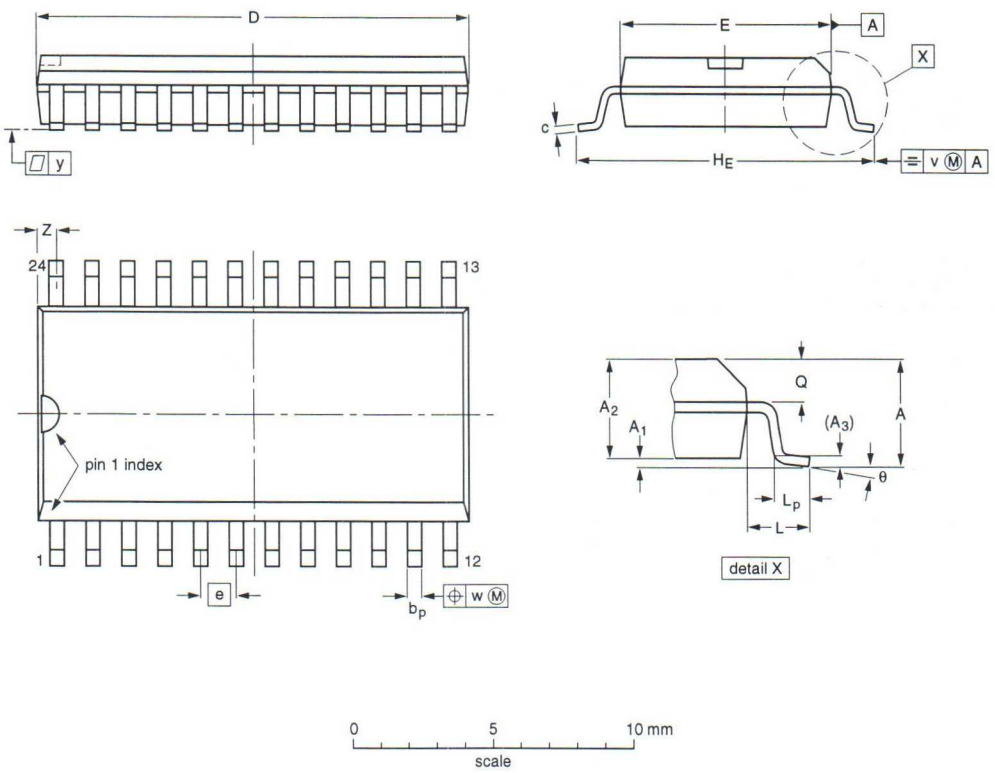
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.10	0.20 0.05	1.9 1.7	0.25	0.50 0.35	0.25 0.15	12.9 12.5	5.4 5.2	1.27	8.1 7.5	1.25	0.9 0.4	0.9 0.7	0.25	0.25	0.1	0.85 0.40	8° 0°
inches	0.083	0.079 0.002	0.075 0.067	0.01	0.020 0.014	0.0098 0.0059	0.51 0.49	0.21 0.20	0.050	0.319 0.295	0.049	0.035 0.016	0.035 0.028	0.01	0.01	0.004	0.033 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT336-1						~~92-10-05~~ 95-03-28

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

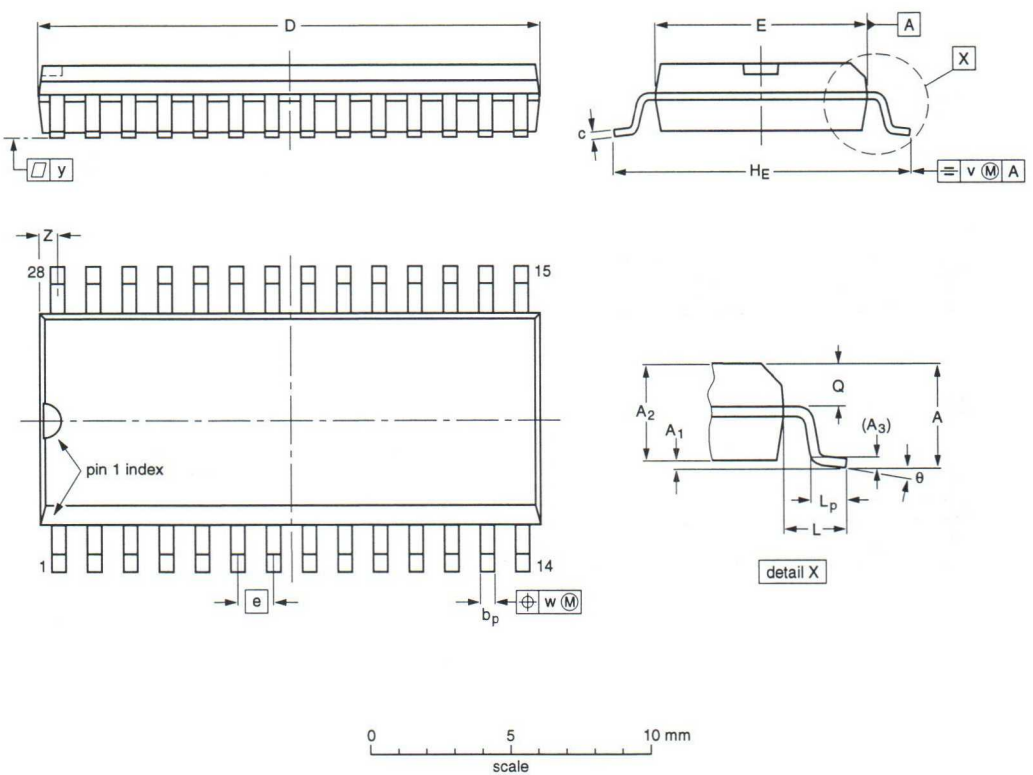
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

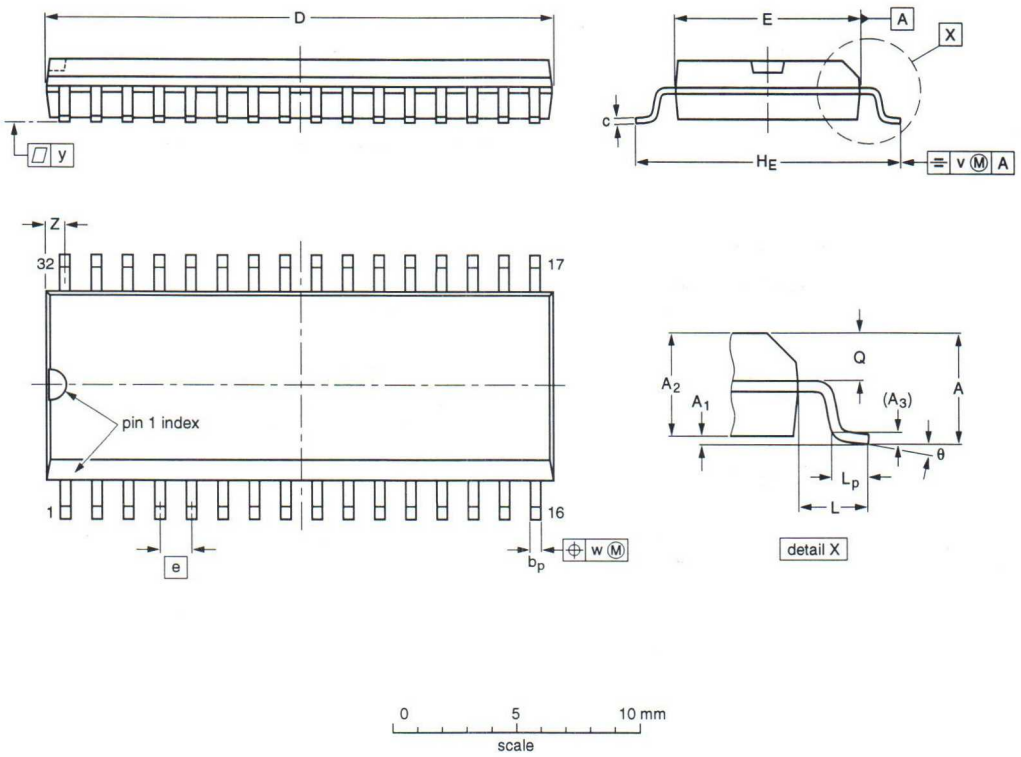
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8° 0°
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

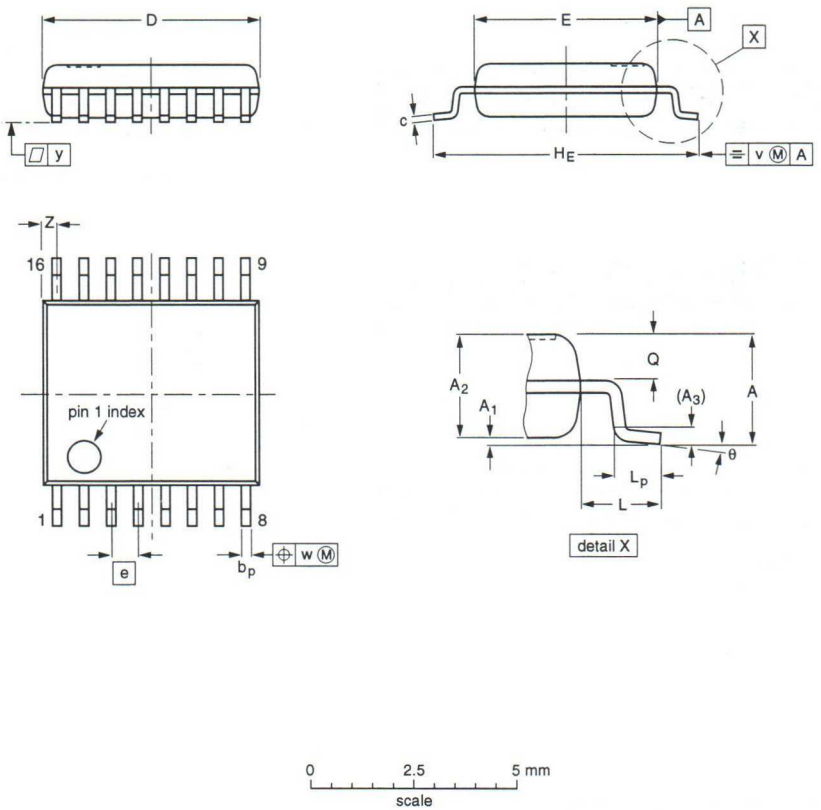
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~92-11-17~~ 95-01-25

SSOP

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1



DIMENSIONS (mm are the original dimensions)

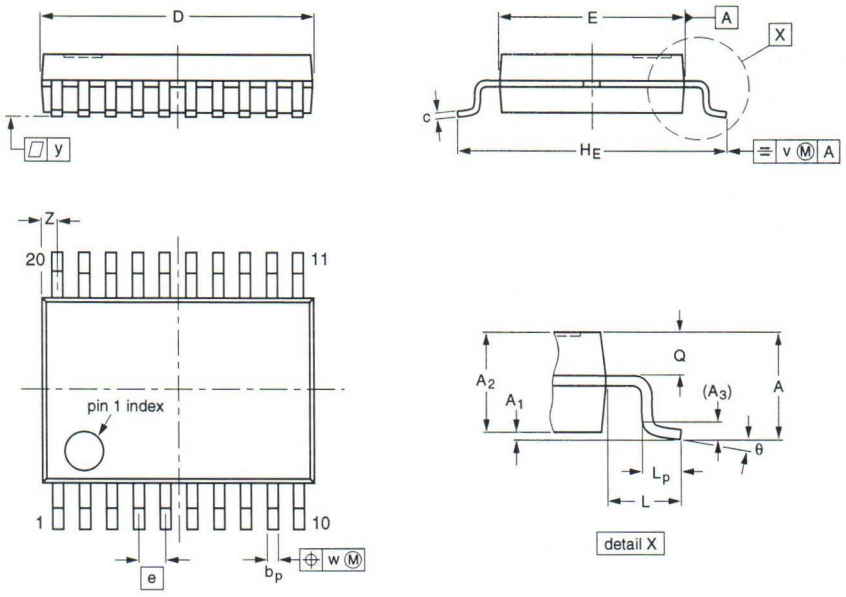
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

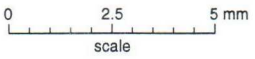
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

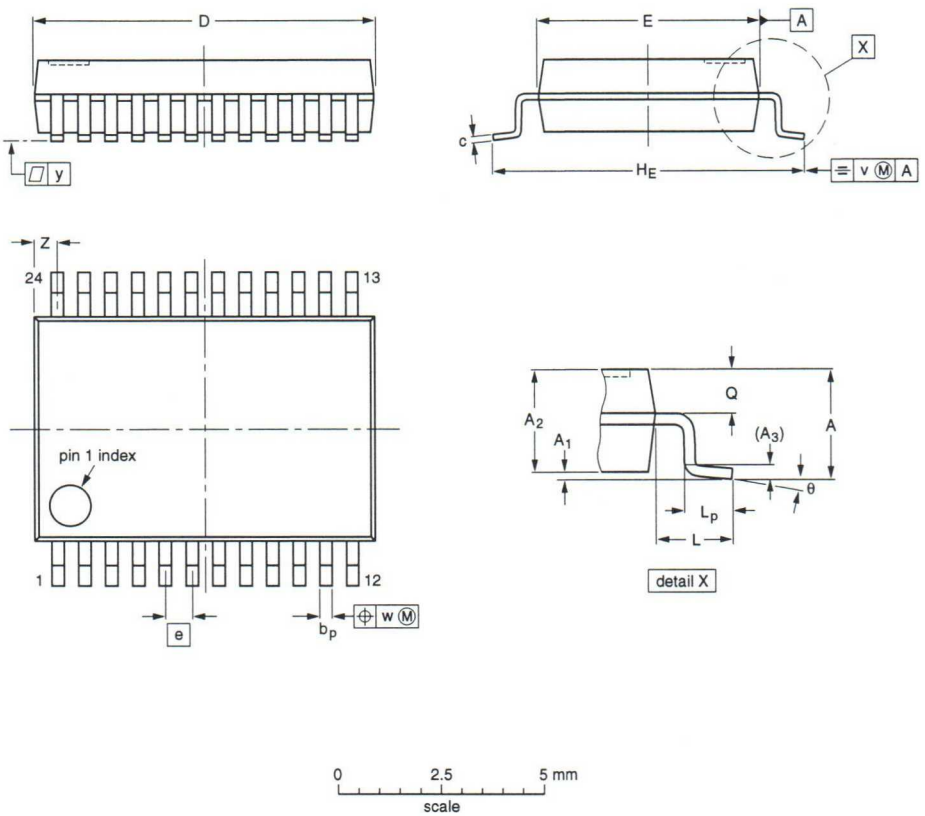
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

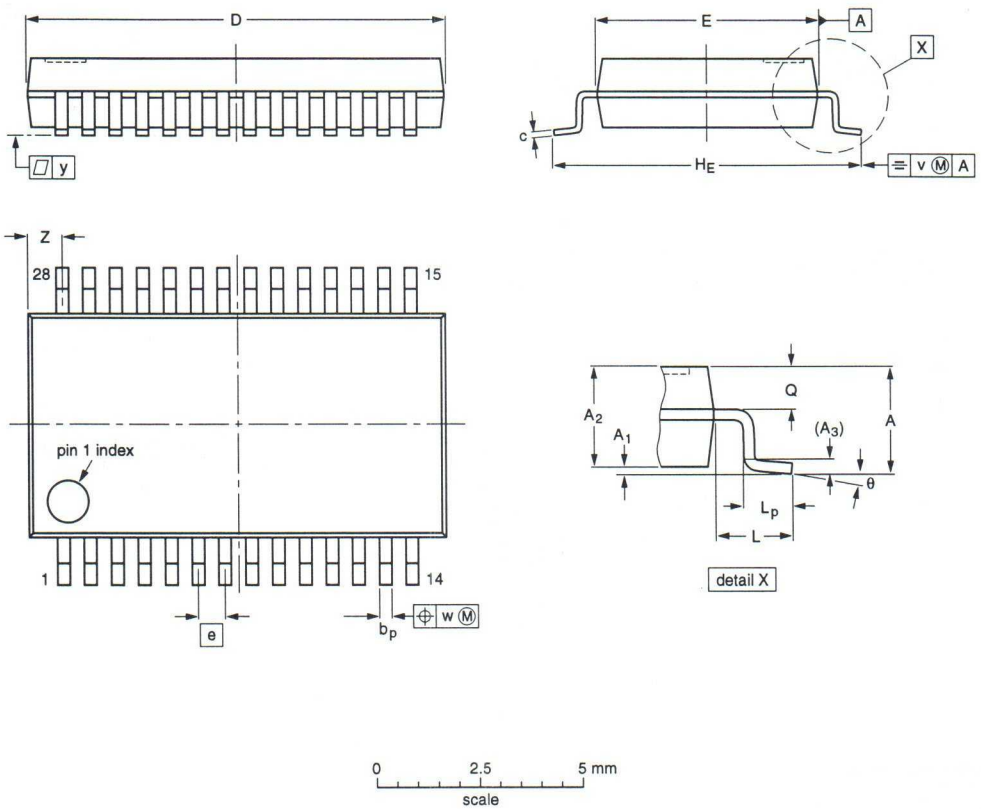
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

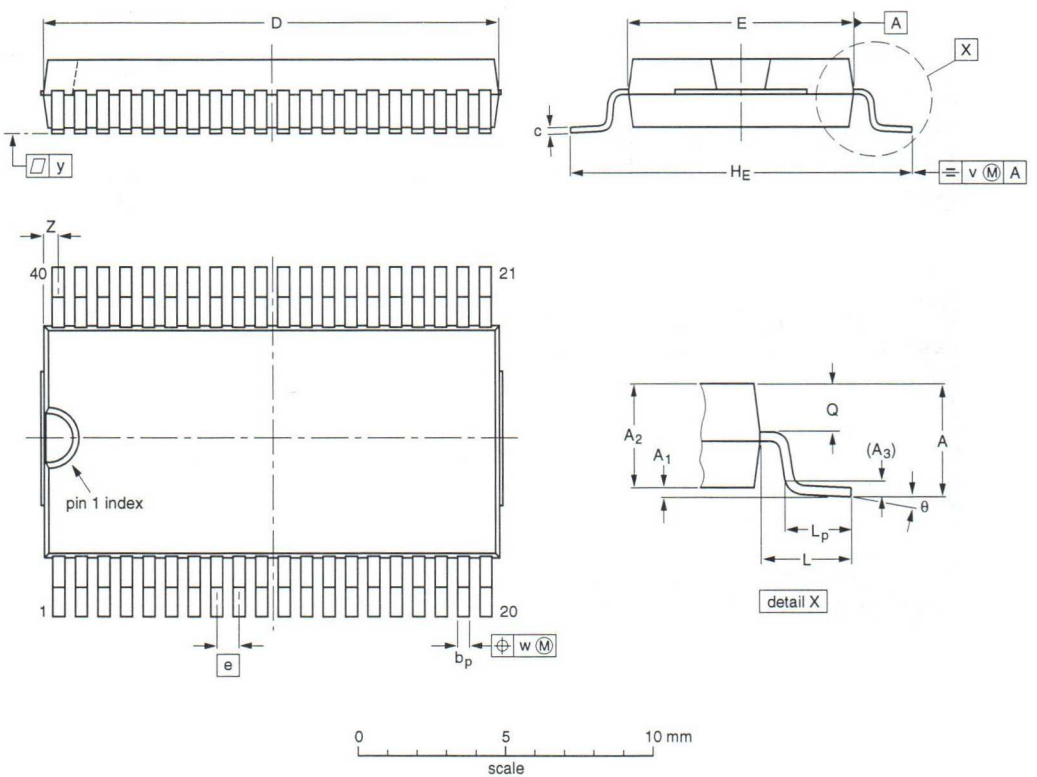
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

VSO

VSO40: plastic very small outline package; 40 leads SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package (DIL-bent-SIL)
SIL	plastic single in-line package

Soldering by dip or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

Table 3 Suitability of surface mounted ICs for various soldering methods
Rating from 1 to 4: **'1' indicates least suitable** (soldering is achievable with difficulty); **'4' indicates most suitable** (soldering is not difficult).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	4	4	4	4	1	4
SSOP	4	4	4	2	1	2
TSSOP	3	3	3	2	1	1
VSO	3	3	4	3	4	3
QFP	3	3	4	2	4	2
LQFP	3	3	4	2	1	1
SQFP	3	3	4	2	1	1
TQFP	3	3	4	2	1	1
PLCC	2	3	3	1	1	3

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering the following types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1) as these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1) as these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1) as these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C.

Data handbook system

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Printed in the USA

5170G/533051/21M/02/pp1616 (out of 4840) Date of release: 04-95

Document order number: 9397-750-00074

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