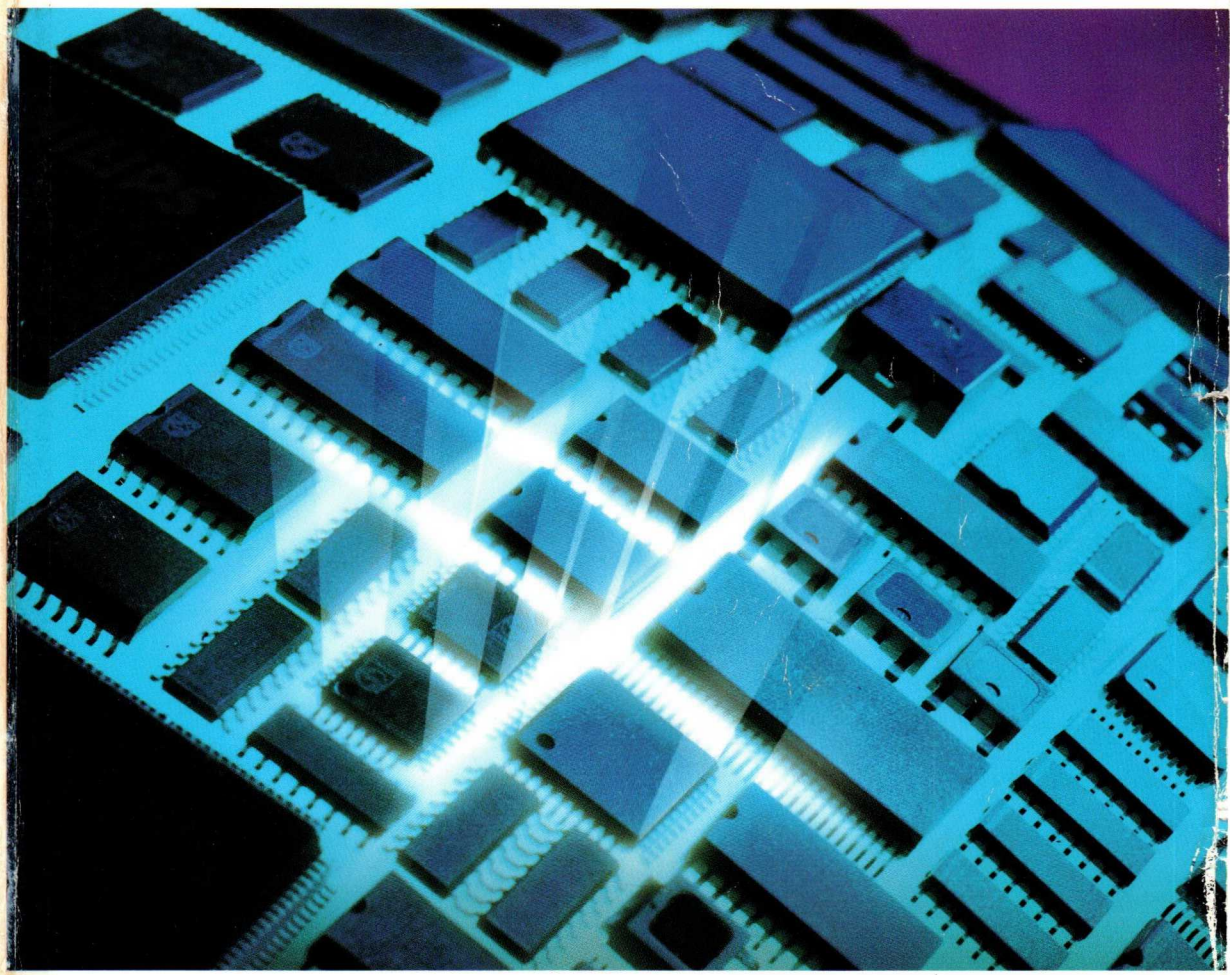
INTEGRATED CIRCUITS

High-Speed CMOS Logic Family



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DATA HANDBOOK IC06

Philips Semiconductors

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PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

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High Speed CMOS Logic Family

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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INTRODUCTION

HIGH-SPEED CMOS (HCMOS) LOGIC IC FAMILY

The HCMOS family of logic ICs is manufactured using a self-aligning 3 μm polycrystalline silicon-gate CMOS process combined with local oxidation of silicon (LOCOS). HCMOS ICs have the low power consumption, high immunity to input noise and wide operating temperature range of earlier silicon-gate CMOS circuits together with the high-speed and drive capability of bipolar, low-power Schottky TTL (LSTTL). They are also immune to latch-up and all types are available in DIL packages and in space-saving SO packages.

Many HCMOS circuits are pin-compatible with existing 54/74 LSTTL and HE4000B CMOS logic ICs. HCT types are ideal replacements for LSTTL. HCT types can also interface between TTL and CMOS ICs.

Three types of HCMOS ICs are available:

- 74HC: CMOS input switching levels 30%V_{CC} and 70%V_{CC} (typical switching threshold 50%V_{CC}), supply voltage 2 V to 6 V
- 74HCT: TTL input switching levels 0.8 V and 2 V (typical switching threshold 28%V_{CC}), supply voltage 4.5 V to 5.5 V
- 74HCU: CMOS input switching levels 20%V_{CC} and 80%V_{CC} (typical switching threshold 50%V_{CC}), supply voltage 2 V to 6 V; unbuffered to allow operation in the linear mode

The HCMOS family also includes several complex circuits for switching or multiplexing analog signals. These circuits have low crosstalk and feedthrough, and a very large frequency bandwidth.
There are also two FIFOs and three PLLs in the HCMOS range, of which one (HC/HCT297) is a fully digital type.

HCMOS FEATURES

- Very low power dissipation
- The switching levels of 74HC types are 30% and 70% of V_{CC}
- DC noise margin of 74HC types three times that of TTL ICs
- Logic output levels 0.1 V and V_{CC} – 0.1 V
- All types, except 74HCU are fully buffered
- Typical gate propagation delay of 8 ns
- Can operate up to 60 MHz (typical)
- Fanout capability of 10 LSTTL loads (4 mA); this is increased to 15 LSTTL loads (6 mA) for types with bus-driver outputs
- Wide supply voltage range
- Latch-up free
- Inputs protected against electrostatic discharge
- Functions and pinning identical to most popular LSTTL and CMOS HE4000B families
- Analog switching types operating up to 10 V
- Symmetrical output sourcing and sinking currents and equal output rise and fall times
- All types available in plastic SO packages for surface mounting and plastic DIL packages
- Choice of operating temperature range:
  –40 to + 85 °C or –40 to + 125 °C
- Approved to JEDEC standard No. 7A

SELECTION GUIDE

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FUNCTIONAL INDEX

type no.	description	pins	classification	page
NAND/NOR gates/EXCLUSIVE-NOR gates				
HC/HCT00	quad 2-input NAND gate	14	SSI	107
HC/HCT02	quad 2-input NOR gate	14	SSI	111
HC/HCT03	quad 2-input NAND gate (with open collector outputs)	14	SSI	115
HC/HCT10	triple 3-input NAND gate	14	SSI	137
HC/HCT20	dual 4-input NAND gate	14	SSI	153
HC/HCT27	triple 3-input NOR gate	14	SSI	161
HC/HCT30	8-input NAND gate	14	SSI	165
HC/HCT133	13-input NAND gate	14	SSI	263
HC/HCT4002	dual 4-input NOR gate	14	SSI	789
HC7266	quad 2-input EXCLUSIVE-NOR gate	14	SSI	1209
AND/OR/EXCLUSIVE-OR gates				
HC/HCT08	quad 2-input AND gate	14	SSI	133
HC/HCT11	triple 3-input AND gate	14	SSI	141
HC/HCT21	dual 4-input AND gate	14	SSI	157
HC/HCT32	quad 2-input OR gate	14	SSI	169
HC58	dual AND/OR gate	14	SSI	177
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	14	SSI	207
HC/HCT4075	triple 3-input OR gate	14	SSI	961
Invertors/buffers/line drivers/level shifters				
HC/HCT04	hex invertor	14	SSI	121
HCU04	hex invertor (unbuffered)	14	SSI	125
HC/HCT125*	quad driver/line driver; 3-state; output enable active LOW	14	MSI	243
HC/HCT126*	quad driver/line driver; 3-state; output enable active HIGH	14	MSI	249
HC/HCT240*	octal buffer/line driver; 3-state; inverting	20	MSI	485
HC/HCT241*	octal line driver; 3-state; output enable active LOW or HIGH	20	MSI	491
HC/HCT244*	octal line driver; 3-state; output enable active LOW	20	MSI	509
HC/HCT365*	hex buffer/line driver; 3-state	16	MSI	603
HC/HCT366*	hex buffer/line driver; 3-state; inverting	16	MSI	607
HC/HCT367*	hex buffer/line driver; 3-state	16	MSI	611
HC/HCT368*	hex buffer/line driver; 3-state; inverting	16	MSI	615

FUNCTIONAL INDEX

type no.	description	pins	classification	page
HC/HCT540*	octal buffer/line driver; 3-state; inverting	20	MSI	669
HC/HCT541*	octal buffer/line driver; 3-state	20	MSI	675
HC4049	hex inverting HIGH-to-LOW level shifter	16	SSI	865
HC4050	hex HIGH-to-LOW level shifter	16	SSI	871
HC/HCT7540*	octal Schmitt trigger buffer/line driver; 3-state; inverting	20	MSI	1269
HC/HCT7541*	octal Schmitt trigger buffer/line driver; 3-state	20	MSI	1275
Flip-flops/latches/registers				
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	14	FF	181
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	14	FF	187
HC/HCT75	quad bistable transparent latch	16	SSI	193
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	14	FF	217
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	16	FF	223
HC/HCT112	dual JK flip-flop with reset; negative-edge trigger	16	FF	229
HC/HCT173*	dual D-type flip-flop; positive-edge trigger; 3-state	16	MSI	369
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	16	MSI	375
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	16	MSI	381
HC/HCT259	8-bit addressable latch	16	MSI	545
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	20	MSI	551
HC/HCT373*	octal D-type transparent latch; 3-state	20	MSI	619
HC/HCT374*	octal D-type flip-flop; positive edge trigger; 3-state	20	MSI	625
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	20	MSI	631
HC/HCT533*	octal D-type transparent latch; 3-state inverting	20	MSI	657
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI	663
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out	20	MSI	681

FUNCTIONAL INDEX

type no.	description	pins	classification	page
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out	20	MSI	687
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out	20	MSI	693
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out	20	MSI	699
HC/HCT670*	4 × 4 register file; 3-state	16	MSI	777
HC/HCT7030	9-bit × 64-word FIFO register; 3-state	28	LSI	1141
HC/HCT40105	4-bit × 16-word FIFO register; 3-state	16	MSI	1383
HC/HCT7403	4-bit × 64-word FIFO register; 3-state	16	LSI	1213
HC/HCT7404	5-bit × 64-word FIFO register; 3-state	18/20	LSI	1241
Shift registers				
HC/HCT164	8-bit serial in/parallel-out shift register	14	MSI	351
HC/HCT165	8-bit serial in/parallel-out shift register	16	MSI	357
HC/HCT166	8-bit serial in/parallel-out shift register	16	MSI	363
HC/HCT194	4-bit bi-directional universal shift register	16	MSI	445
HC/HCT195	4-bit parallel access shift register	16	MSI	453
HC/HCT299*	8-bit universal shift register; 3-state	20	MSI	577
HC/HCT594	8-bit shift register with output register	16	MSI	711
HC/HCT595	8-bit serial-in/serial-or parallel-out shift register with output latches; 3-state	16	MSI	721
HC/HCT597	8-bit shift register with input flip-flops	16	MSI	733
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	16	MSI	793
HC/HCT4094	8-stage shift-and-store bus register	16	MSI	965
HC/HCT7597	8-bit shift register with input latches	16	MSI	1281
HC/HCT7731	quad 64-bit static shift register	16	LSI	1291
HC/HCT40104*	4-bit bi-directional universal shift register; 3-state	16	MSI	1377
Arithmetic circuits				
HC/HCT85	4-bit magnitude comparator	16	MSI	199
HC/HCT181	4-bit arithmetic unit	24	MSI	387
HC/HCT182	look-ahead carry generator	16	MSI	401
HC/HCT280	9-bit odd/even parity generator/checker	14	MSI	557
HC/HCT283	4-bit binary full adder with fast carry	16	MSI	563
HC/HCT583	4-bit BCD full adder with fast carry	16	MSI	705

type no.	description	pins	classification	page
HC/HCT688	8-bit magnitude comparator	20	MSI	783
HC/HCT7080	16-bit odd/even parity generator/checker	20	MSI	1189
Counters				
HC/HCT93	4-bit binary ripple counter	14	MSI	211
HC/HCT160	presettable synchronous BCD decade counter; assynchronous reset	16	MSI	321
HC/HCT161	presettable synchronous 4-bit binary counter; assynchronous reset	16	MSI	329
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	16	MSI	335
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	16	MSI	343
HC/HCT190	presettable synchronous BCD decade up/down counter	16	MSI	409
HC/HCT191	presettable synchronous 4-bit binary up/down counter	16	MSI	419
HC/HCT192	presettable synchronous BCD decade up/down counter	16	MSI	429
HC/HCT193	presettable synchronous 4-bit binary up/down counter	16	MSI	437
HC/HCT390	dual decade ripple counter	16	MSI	637
HC/HCT393	dual 4-bit binary ripple counter	14	MSI	643
HC/HCT4017	Johnson decade counter with 10 decoded outputs	16	MSI	811
HC/HCT4020	14-stage binary ripple counter	16	MSI	819
HC/HCT4024	7-stage binary ripple counter	14	MSI	825
HC/HCT4040	12-stage binary ripple counter	16	MSI	831
HC/HCT4059	programmable divide-by-n counter	24	MSI	915
HC/HCT4060	14-stage binary ripple counter with oscillator	16	MSI	925
HC/HCT4510	BCD up-down counter	16	MSI	1027
HC/HCT4516	binary up/down counter	16	MSI	1059
HC/HCT4518	dual synchronous BCD counter	16	MSI	1069
HC/HCT4520	dual synchronous 4-bit binary counter	16	MSI	1075
HC/HCT6323A	programmable ripple counter with oscillator; 3-state	8	MSI	1123
HC/HCT40102	8-stage synchronous BCD down counter	16	MSI	1359
HC/HCT40103	8-bit synchronous down counter	16	MSI	1367

type no.	description	pins	classification	page
Multiplexers				
HC/HCT151	8-input multiplexer	16	MSI	291
HC/HCT153	dual 4-input multiplexer	16	MSI	297
HC/HCT157	quad 2-input multiplexer	16	MSI	309
HC/HCT158	quad 2-input multiplexer; inverting	16	MSI	315
HC/HCT251	8-input multiplexers; 3-state	16	MSI	521
HC/HCT253*	dual 4-input multiplexer; 3-state	16	MSI	527
HC/HCT257*	quad 2-input multiplexer; 3-state	16	MSI	533
HC/HCT258	quad 2-input multiplexer; 3-state; inverting	16	MSI	539
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	20	MSI	585
HC/HCT356*	8-input multiplexer/register; 3-state	20	MSI	595
Decoders/demultiplexers				
HC/HCT42	BCD to decimal decoder (1-of-10)	16	MSI	173
HC/HCT137	3-to-8 line decoder/demultiplexer with address latches	16	MSI	267
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	16	MSI	275
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	16	MSI	281
HC/HCT147	10-to-4 line priority encoder	16	MSI	287
HC/HCT154	4-to-16 line decoder/demultiplexer	24	MSI	303
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches	16	MSI	471
HC/HCT238	3-to-8 line decoder/demultiplexer	16	MSI	479
HC/HCT4511	BCD to 7-segment latch/decoder/driver	16	MSI	1037
HC/HCT4514	4-to-16 line decoder/multiplexer with input latches	24	MSI	1045
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	24	MSI	1053
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	16	MSI	1091
Switches/multiplexers/demultiplexers				
HC/HCT4016	quad bilateral switches (uncompensated switches)	14	SSI	799
HC/HCT4051	8-channel analog multiplexer/demultiplexer	16	MSI	877
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	16	MSI	889
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	16	MSI	901

type no.	description	pins	classification	page
HC/HCT4066	quad bilateral switches	14	SSI	935
HC/HCT4067	16-channel analog multiplexer/demultiplexer	24	MSI	947
HC/HCT4316	quad bilateral switches with separate analog ground	16	MSI	971
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	20	MSI	985
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	20	MSI	999
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	20	MSI	1013
Bus transceivers				
HC/HCT242*	quad bus transceiver; 3-state; inverting	14	MSI	497
HC/HCT243*	quad bus transceiver; 3-state	14	MSI	503
HC/HCT245*	octal bus transceiver; 3-state	20	MSI	515
HC/HCT640*	octal bus transceiver; 3-state; inverting	20	MSI	741
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	20	MSI	747
HC/HCT646*	octal bus transceiver/register; 3-state	24	MSI	753
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	24	MSI	761
HC/HCT652	octal bus transceiver/register; 3-state	24	MSI	769
HC/HCT7245*	octal Schmitt-trigger transceiver; 3-state	20	MSI	1205
Schmitt triggers				
HC/HCT14	hex inverting Schmitt trigger	14	SSI	145
HC/HCT132	quad 2-input NAND Schmitt trigger	14	SSI	255
HC7014	hex non-inverting precision Schmitt-trigger	14	SSI	1137
HC/HCT7132	quad preciscion adjustable Schmitt-trigger/comparator with output latches; 3-state	14	MSI	1195
HC/HCT9014	nine wide Schmitt trigger buffer/line driver; inverting	20	MSI	1299
HC/HCT9015	nine wide Schmitt trigger buffer/line driver	20	MSI	1305
HC/HCT9114	nine wide Schmitt trigger buffer; open drain output; inverting	20	MSI	1347
HC/HCT9115	nine wide Schmitt trigger buffer; open drain output	20	MSI	1353

type no.	description	pins	classification	page
One-shot multivibrators				
HC/HCT123	dual retriggerable monostable multivibrator with reset	16	MSI	235
HC/HCT221	dual non-retriggerable monostable multivibrator with reset	16	MSI	459
HC/HCT423	dual retriggerable monostable multivibrator with reset	16	MSI	649
HC/HCT4538	dual retriggerable precision monostable multivibrator	16	MSI	1081
HC/HCT5555	programmable delay timer with oscillator	16	MSI	1101
Miscellaneous				
HC/HCT297	digital phase-locked-loop filter	16	MSI	569
HC/HCT4046A	phase-locked-loop with VCO	16	MSI	837
HC/HCT7046A	phase-locked-loop with lock detector	16	MSI	1159
HC/HCT9046A	PLL with bandgap controlled VCO	16	MSI	1311
New releases				
HC/HCT9323A	programmable ripple counter with oscillator	8	MSI	80
HCT1284	parallel printer interface transceiver/ buffer	20	MSI	83

NOTE:
⋆ Types with a bus-driver output stage.

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type no.	description	page
HC/HCT00	quad 2-input NAND gate	107
HC/HCT02	quad 2-input NOR gate	111
HC/HCT03	quad 2-input NAND gate (with open collector outputs)	115
HC/HCT04	hex invertor	121
HCU04	hex invertor (unbuffered)	125
HC/HCT08	quad 2-input AND gate	133
HC/HCT10	triple 3-input NAND gate	137
HC/HCT11	triple 3-input AND gate	141
HC/HCT14	hex inverting Schmitt trigger	145
HC/HCT20	dual 4-input NAND gate	153
HC/HCT21	dual 4-input AND gate	157
HC/HCT27	triple 3-input NOR gate	161
HC/HCT30	8-input NAND gate	165
HC/HCT32	quad 2-input OR gate	169
HC/HCT42	BCD to decimal decoder (1-of-10)	173
HC58	dual AND/OR gate	177
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	181
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	187
HC/HCT75	quad bistable transparent latch	193
HC/HCT85	4-bit magnitude comparator	199
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	207
HC/HCT93	4-bit binary ripple counter	211
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	217
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	223
HC/HCT112	dual JK flip-flop with reset; negative-edge trigger	229
HC/HCT123	dual retriggerable monostable multivibrator with reset	235
HC/HCT125*	quad driver/line driver; 3-state; output enable active LOW	243
HC/HCT126*	quad driver/line driver; 3-state; output enable active HIGH	249
HC/HCT132	quad 2-input NAND Schmitt trigger	255
HC/HCT133	13-input NAND gate	263
HC/HCT137	3-to-8 line decoder/demultiplexer with address latches	267
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	275
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	281
HC/HCT147	10-to-4 line priority encoder	287
HC/HCT151	8-input multiplexer	291
HC/HCT153	dual 4-input multiplexer	297

type no.	description	page
HC/HCT154	4-to-16 line decoder/demultiplexer	303
HC/HCT157	quad 2-input multiplexer	309
HC/HCT158	quad 2-input multiplexer; inverting	315
HC/HCT160	presettable synchronous BCD decade counter; assynchronous reset	321
HC/HCT161	presettable synchronous 4-bit binary counter; assynchronous reset	329
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	335
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	343
HC/HCT164	8-bit serial in/parallel-out shift register	351
HC/HCT165	8-bit serial in/parallel-out shift register	357
HC/HCT166	8-bit serial in/parallel-out shift register	363
HC/HCT173*	dual D-type flip-flop; positive-edge trigger; 3-state	369
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	375
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	381
HC/HCT181	4-bit arithmetic unit	387
HC/HCT182	look-ahead carry generator	401
HC/HCT190	presettable synchronous BCD decade up/down counter	409
HC/HCT191	presettable synchronous 4-bit binary up/down counter	419
HC/HCT192	presettable synchronous BCD decade up/down counter	429
HC/HCT193	presettable synchronous 4-bit binary up/down counter	437
HC/HCT194	4-bit bi-directional universal shift register	445
HC/HCT195	4-bit parallel access shift register	453
HC/HCT221	dual non-retriggerable monostable multivibrator with reset	459
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches	471
HC/HCT238	3-to-8 line decoder/demultiplexer	479
HC/HCT240*	octal buffer/line driver; 3-state; inverting	485
HC/HCT241*	octal line driver; 3-state; output enable active LOW or HIGH	491
HC/HCT242*	quad bus transceiver; 3-state; inverting	497
HC/HCT243*	quad bus transceiver; 3-state	503
HC/HCT244*	octal line driver; 3-state; output enable active LOW	509
HC/HCT245*	octal bus transceiver; 3-state	515
HC/HCT251	8-input multiplexers; 3-state	521
HC/HCT253*	dual 4-input multiplexer; 3-state	527
HC/HCT257*	quad 2-input multiplexer; 3-state	533
HC/HCT258	quad 2-input multiplexer; 3-state; inverting	539
HC/HCT259	8-bit addressable latch	545

type no.	description	page
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	551
HC/HCT280	9-bit odd/even parity generator/checker	557
HC/HCT283	4-bit binary full adder with fast carry	563
HC/HCT297	digital phase-locked-loop filter	569
HC/HCT299*	8-bit universal shift register; 3-state	577
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	585
HC/HCT356*	8-input multiplexer/register; 3-state	595
HC/HCT365*	hex buffer/line driver; 3-state	603
HC/HCT366*	hex buffer/line driver; 3-state; inverting	607
HC/HCT367*	hex buffer/line driver; 3-state	611
HC/HCT368*	hex buffer/line driver; 3-state; inverting	615
HC/HCT373*	octal D-type transparent latch; 3-state	619
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state	625
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	631
HC/HCT390	dual decade ripple counter	637
HC/HCT393	dual 4-bit binary ripple counter	643
HC/HCT423	dual retriggerable monostable multivibrator with reset	649
HC/HCT533*	octal D-type transparent latch; 3-state inverting	657
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	663
HC/HCT540*	octal buffer/line driver; 3-state; inverting	669
HC/HCT541*	octal buffer/line driver; 3-state	675
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out	681
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out	687
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out	693
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out	699
HC/HCT583	4-bit BCD full adder with fast carry	705
HC/HCT594	8-bit shift register with output register	711
HC/HCT595	8-bit serial-in/serial or parallel-out shift register with output latches; 3-state	721
HC/HCT597	8-bit shift register with input flip-flops	733
HC/HCT640*	octal bus transceiver; 3-state; inverting	741
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	747
HC/HCT646*	octal bus transceiver/register; 3-state	753
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	761
HC/HCT652	octal bus transceiver/register; 3-state	769

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HC/HCT670*	4 × 4 register file; 3-state	777
HC/HCT688	8-bit magnitude comparator	783
HC/HCT4002	dual 4-input NOR gate	789
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	793
HC/HCT4016	quad bilateral switches (uncompensated switches)	799
HC/HCT4017	Johnson decade counter with 10 decoded outputs	811
HC/HCT4020	14-stage binary ripple counter	819
HC/HCT4024	7-stage binary ripple counter	825
HC/HCT4040	12-stage binary ripple counter	831
HC/HCT4046A	phase-locked-loop with VCO	837
HC4049	hex inverting HIGH-to-LOW level shifter	865
HC4050	hex HIGH-to-LOW level shifter	871
HC/HCT4051	8-channel analog multiplexer/demultiplexer	877
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	889
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	901
HC/HCT4059	programmable divide-by-n counter	915
HC/HCT4060	14-stage binary ripple counter with oscillator	925
HC/HCT4066	quad bilateral switches	935
HC/HCT4067	16-channel analog multiplexer/demultiplexer	947
HC/HCT4075	triple 3-input OR gate	961
HC/HCT4094	8-stage shift-and-store bus register	965
HC/HCT4316	quad bilateral switches with separate analog ground	971
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	985
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	999
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	1013
HC/HCT4510	BCD up-down counter	1027
HC/HCT4511	BCD to 7-segment latch/decoder/driver	1037
HC/HCT4514	4-to-16 line decoder/multiplexer with input latches	1045
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	1053
HC/HCT4516	binary up/down counter	1059
HC/HCT4518	dual synchronous BCD counter	1069
HC/HCT4520	dual synchronous 4-bit binary counter	1075
HC/HCT4538	dual retriggerable precision monostable multivibrator	1081
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	1091
HC/HCT5555	programmable delay timer with oscillator	1101
HC/HCT6323A	programmable ripple counter with oscillator; 3-state	1123
HC/HCT7014	hex non-inverting precision Schmitt-trigger	1137

type no.	description	page
HC/HCT7030	9-bit x 64-word FIFO register; 3-state	1141
HC/HCT7046A	phase-locked-loop with lock detector	1159
HC/HCT7080	16-bit odd/even parity generator/checker	1189
HC/HCT7132	quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state	1195
HC/HCT7245*	octal Schmitt-trigger transceiver; 3-state	1205
HC7266	quad 2-input EXCLUSIVE-NOR gate	1209
HC/HCT7403	4-bit x 64-word FIFO register; 3-state	1213
HC/HCT7404	5-bit x 64-word FIFO register; 3-state	1241
HC/HCT7540*	octal Schmitt trigger buffer/line driver; 3-state; inverting	1269
HC/HCT7541*	octal Schmitt trigger buffer/line driver; 3-state	1275
HC/HCT7597	8-bit shift register with input latches	1281
HC/HCT7731	quad 64-bit static shift register	1291
HC/HCT9014	nine wide Schmitt trigger buffer/line driver; inverting	1299
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HC/HCT9114	nine wide Schmitt trigger buffer;open drain output; inverting	1347
HC/HCT9115	nine wide Schmitt trigger buffer;open drain output	1353
HC/HCT40102	8-stage synchronous BCD down counter	1359
HC/HCT40103	8-bit synchronous down counter	1367
HC/HCT40104*	4-bit bi-directional universal shift register; 3-state	1377
HC/HCT40105	4-bit x 16-word FIFO register; 3-state	1383
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HC/HCT9323A	programmable ripple counter with oscillator	80
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NOTE:

* Types with a bus-driver output stage.

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HIGH-SPEED CMOS PRODUCTS PART NUMBERING SYSTEM

Example: 74 XXX XXXXX XX

Complete type number which can be split as follows:

Package Code:
- N = Plastic Dual In-Line
- D = Plastic SO
- NB = Plastic DIL; burn-in
- DB = Plastic SSOP type II
- PW = Plastic TSSOP type I

= Device number (up to 5 digits)

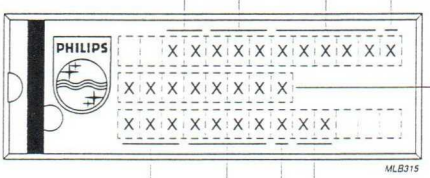
HC = CMOS input switching levels, supply voltage range 2V to 6V, fully buffered.

HCT = TTL input switching levels, supply voltage range 5V ±10%; fully buffered.

HCU = CMOS input switching levels; supply voltage range 2 to 6V; unbuffered (single-stage devices)

74 = commercial (–40°C to 85°C) and extended (–40°C to +125°C) operating temperature range

MARKING



TYPE NUMBER DESIGNATIONS

74 = standard temperature range: −40 to +85 °C and −40 to +125 °C

HCU = CMOS input switching levels; supply voltage range 2 to 6 V; unbuffered (single-stage devices)

HCT = TTL input switching levels; supply voltage range 4.5 V to 5.5 V; fully buffered

HC = CMOS input switching levels; supply voltage range 2 to 6 V; fully buffered

device number (up to 5 digits; may include a suffix letter*)

package code: N = plastic DIL, D = plastic mini-pack (SO), DB = SSOP type 11, NB = plastic DIL with burn-in.

TRACEABILITY

PRODUCTION INFORMATION

layout number and product status

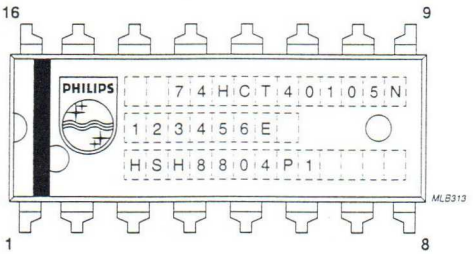
CECC quality assessment level

date code

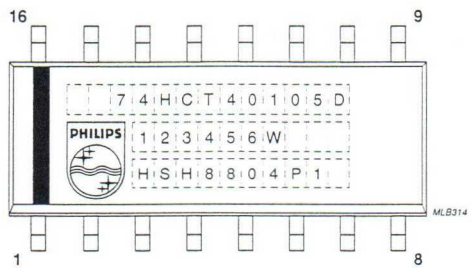
factory identification

* Example suffix "B": this type has bus driver output capability in contrast with the plain version.

MARKING EXAMPLES



Example of 16-lead dual in-line plastic package.



Example of 16-lead small-outline plastic SO mini-pack package.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

RATING SYSTEMS

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design to that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

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Note: The information in this user guide is intended as a design-aid and does not constitute a guarantee.

INTRODUCTION

The 74HC/HCT/HCU family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - these circuits have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). An extensive product range (most TTL functions and some devices from the successful HE4000B series: analog multiplexers, long time-constant multivibrators, phase-locked loops) and the aforementioned performance open new avenues in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1. The propagation delay of metal-gate CMOS ruled out CMOS for many applications until the arrival of our HE4000B series. Now, our 3 μm gate HCMOS technology has a speed comparable to LSTTL while retaining the important CMOS qualities, see Fig.1.

Table 2 compares the operating characteristics of the 74HC and 74HCT IC types with those of LSTTL in more detail. 74HC and 74HCT devices are ideal for use in new equipment designs and, as alternatives to TTL devices, in existing designs. The 74HCT circuits which are direct replacements for LSTTL circuits also enhance performance in many respects.

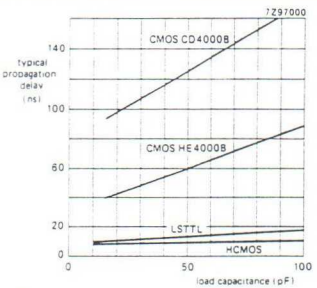


Fig. 1 Propagation delay as a function of load capatance; V_{CC} = 5 V, T_{amb} = 25 °C.

Table 1 Comparison of CMOS and TTL technologies; supply voltage V_{CC} = 5 V; ambient temperature T_{amb} = 25 °C; load capacitance C_L = 15 pF

parameters	technology	HCMOS	metal gate CMOS	standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
	family	74HC	4000 CD HE	74	74LS	74S	74ALS	74AS	74F
Power dissipation, typ. (mW)									
Gate	static	0.0000025	0.001	10	2	19	1.2	8.5	5.5
	dynamic @ 100 kHz	0.075	0.1	10	2	19	1.2	8.5	5.5
Counter	static	0.000005	0.001	300	100	500	60	–	190
	dynamic @ 100 kHz	0.125	0.120	300	100	500	60	–	190
Propagation delay (ns)									
Gate	typical	8	94 40	10	9.5	3	4	1.5	3
	maximum	14	190 80	20	15	5	7	2.5	4
Delay/power product (pJ)									
Gate	at 100 kHz	0.52	9 4	100	19	57	4.8	13	16.5
Maximum clock frequency (MHz)									
D-type flip-flop	typical	55	4 12	25	33	100	60	160	125
	minimum	30	2 6	15	25	75	40	–	100
Counter	typical	45	2 6	32	32	70	45	–	125
	minimum	25	1 3	25	25	40	–	–	100
Output drive (mA)									
	standard outputs	4	0.51 0.8	16	8	20	8	20	20
	bus outputs	6	1.6	48	24	64	24	48	64
Fan-out (LS-loads)									
	standard outputs	10	1 2	40	20	50	20	50	50
	bus outputs	15	4	120	60	160	60	120	160

Table 2: Comparison of HCMOS and LSTTL circuits (V_{CC} = 5 V unless stated otherwise; C_L = 50 pF)

characteristic	74HCXXX (note 1) 74HCTXXX	74LSXXX
Max. quiescent power dissipation over temp. range at V_{CCmax}		
per gate (mW)	0.027	6
per flip-flop (mW)	0.11	22
per 4-stage counter (mW)	0.44	175
per transceiver/buffer (mW)	0.055	60
Max. dynamic power dissipation (C_L = 50 pF)		
at f_i (MHz)	0.1 1 10	0.1 to 1 10
per gate (mW)	0.25 2.25 22	6 22
per flip-flop (mW)	0.35 2.5 24	22 27
per 4-stage counter (mW)	0.70 3 27	175 200
per buffer/transceiver (mW)	0.30 2.5 24	60 90
Operating supply voltage (V)	2 to 6 (HC) 4.5 to 5.5 (HCT)	4.75 to 5.25
Operating temperature range (°C)	−40 to +85 −40 to +125	0 to +70
Max. noise margin (V_{NMH}/V_{NML} V; I_{OHCMOS} = 20 μA; I_{OLSTTL} = 4 mA)	1.4/1.4 (HC) 2.9/0.7 (HCT)	0.7/0.4
Input switching voltage stability over temp. range	±60 mV	±200 mV
Min. output drive current at $T_{amb\ max}$ and V_{CCmin} (mA)		
source current (V_{OH} = 2.7 V; note 2)		
standard logic	−8	−0.4
bus logic	−12	−2.6
sink current		
standard logic (V_{OL} = 0.4 V)	4	4
standard logic (V_{OL} = 0.5 V)	6	8
bus logic (V_{OL} = 0.4 V)	8	12
bus logic (V_{OL} = 0.5 V)	9	24
Typ. output transition time (ns) (C_L = 15 pF)		
standard logic		
t_{TLH}	6	15
t_{THL}	6	6
bus logic		
t_{TLH}	4	15
t_{THL}	4	6
Typ. propagation delay (ns) (C_L = 15 pF; note 3)		
gate t_{PHL}/t_{PLH}	8/8	8/11
flip-flop t_{PLH}	14	15
t_{PHL}	14	22
Typ. clock rate of a flip-flop; note 5 (MHz)	50	33
Max. input current (μA)		
I_{IL}	−1	−400 to −800
I_{IH}	1	40
3-state output leakage current (± μA)	5	20
Reliability (%/1000 h at 60% confidence level)	0.0005	0.008 (note 4)

Notes

1. Data valid for HCMOS between −40 °C and +85 °C.
2. V_{OH} for a few LSTTL bus outputs is specified as 2.4 V.
3. Refer to data sheets for the effect of capacitive loading.
4. RADC report.
5. Measured with a 50% duty factor for HCMOS. For LSTTL, per industry convention, the maximum clock frequency is specified with no constraints on rise and fall times, pulse width or duty factor.

CONSTRUCTION

Our HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate CMOS process. Figure 2 shows the construction of a basic inverter from the HE4000B series and its HCMOS successor.

The polysilicon gate of a HCMOS transistor is deposited over a thin gate oxide before the source and drain diffusions are defined. Source and drain regions are formed using ion implantation, with the polysilicon gates acting as masks for the implantation. The source and drain are automatically aligned to the gate, minimizing gate-to-source and gate-to-drain capacitances. In addition, the junction capacitances, which are proportional to the junction area, are reduced because of the shallower diffusions. Figure 3(c) shows the parasitic capacitances in a CMOS inverter.

In a metal-gate CMOS transistor, the source and drain are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. This is why a metal-gate CMOS transistor has a higher overlap capacitance than an HCMOS transistor. Furthermore, the deeper diffusions of metal-gate CMOS make the junction capacitance larger.

In a silicon-gate MOS transistor, there are three interconnect layers (diffusion, polysilicon and metal) instead of the two layers (diffusion and metal) in a metal-gate MOS transistor. This makes a silicon-gate MOS transistor more compact. The shorter gate length means higher drive capability, which in turn increases the speed at which a silicon-gate MOS transistor can charge or discharge junction capacitance. The drain current of a saturated MOS transistor which determines the speed of the transistor is:

$$I_{DS} = \frac{-\beta}{2} \times \frac{\text{gate width}}{\text{gate length}} \times (\text{gate voltage - threshold voltage})^2$$

where β is the current gain factor which is proportional to the thickness of the oxide layer.

The threshold voltage is typically 0.7 V for HCMOS.

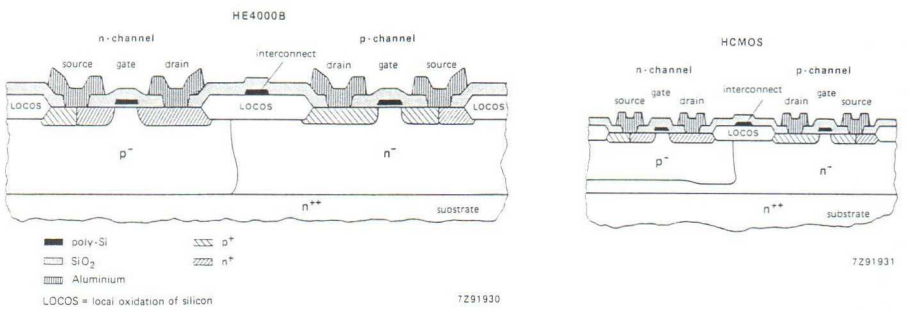


Fig. 2 Basic inverter (left) in HE4000B CMOS, 6 μm gate, and (right) in HCMOS, 3 μm gate.

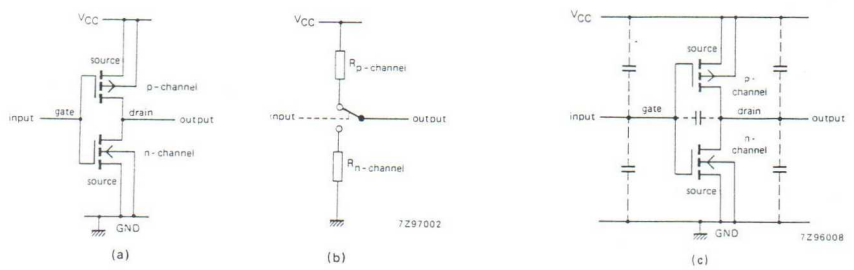


Fig. 3 (a) Basic CMOS inverter; (b) electrical equivalent; (c) parasitic capacitances in a CMOS inverter.

AC CHARACTERISTICS

Test conditions

The propagation delays and transition times specified in the HCMOS data sheets are guaranteed when the circuits are tested according to the conditions stated in the chapter 'Family Characteristics', section 'Family Specifications'. For some circuits such as counters and flip-flops, the test conditions are defined further by the a.c. set-up requirements specified in the data sheet.

Values given in the data sheets are for the whole operating temperature range (−40 to +125 °C) and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for 74HC devices, and 4.5 V for 74HCT devices. This is a much tougher specification than that commonly used for LSTTL, where the characteristics are usually only specified at 25 °C and for a 5 V supply. Furthermore, the published a.c. characteristics of HCMOS are guaranteed for a capacitive test load of 50 pF, a more realistic load than the 15 pF specified for LSTTL and one that loads the device as the output switches. The published values for HCMOS are therefore representative of those measured in actual systems.

Comparing the speed of HCMOS and LSTTL

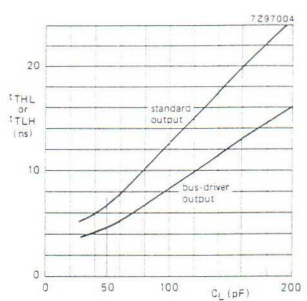
A feature of a HCMOS circuit is its speed - in general, comparable to that of its LSTTL equivalent. Owing to the different (more informative) way of specifying data for HCMOS devices, it will be useful to indicate how to compare the published data for HCMOS and LSTTL.

For example, in an LSTTL specification, the use of a 15 pF load instead of a 50 pF one means the maximum propagation delays and enable times published for the LSTTL device will be up to 2.5 ns (typ. 1.3 ns) shorter than those for the HCMOS equivalent. In addition, measuring at the nominal LSTTL supply voltage of 5 V instead of 4.5 V (HCMOS) reduces propagation delays and enable times by a further 10%. So, a 30 ns propagation delay for a HCMOS device is equivalent to a (30 - 2.5)0.9 = 25 ns delay for an LSTTL device measured at 4.5 V and with a 15 pF load.

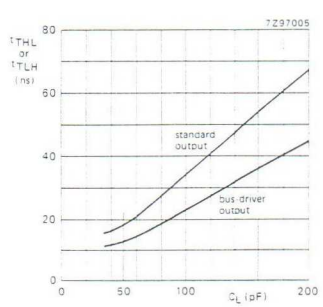
Disable times are measured under different test conditions too - for HCMOS with a 50 pF, 1 kΩ load, for LSTTL with a 5 pF, 2 kΩ load or for a 45 pF, 667 Ω load. To compare a HCMOS disable time with that for a LSTTL device with a 5 pF load, subtract 4 ns from the published HCMOS disable time and multiply by 0.9. To compare a value for a 45 pF load, subtract 2 ns and multiply by 0.9. For example, a 30 ns HCMOS disable time is equivalent to (30 - 4)0.9 = 23 ns for a 5 pF load and (30 - 2)0.9 = 25 ns for a 45 pF load.

Set-up hold and removal times are not affected by output load, only by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the HCMOS value by 0.9.

(a) V_{CC} = 6 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 2 V

Fig. 4 Typical output transition times as a function of load capacitance; T_{amb} = 25 °C; for 74HCT circuits the data at V_{CC} = 4.5 V only is valid.

Operating frequency is also unaffected by output load, but is affected by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the value for HCMOS at 4.5 V by 1.1.

In general, these guidelines apply both to 74HC and to 74HCT devices. For 74HCT devices however, the propagation delay is the time for the output to reach 1.4 V (compared with 50%V_{CC} for 74HC devices), so HIGH-to-LOW output transition times are slightly more dependent on load and the LOW-to-HIGH transition times are slightly less dependent on load than the 74HC versions.

Propagation delays and transition times

The symmetrical push-pull output structure of both 74HC and 74HCT devices gives symmetrical rise/fall times and provides for a well-balanced system design. Table 3 shows the maximum output transition times for all standard and bus-driver HCMOS outputs.

The influence of capacitive loading on output transitions is shown in Fig.4; A good approximation of the output transition times can be calculated using the data of Table 4.

Table 3: Maximum output transition times (C_L = 50 pF)

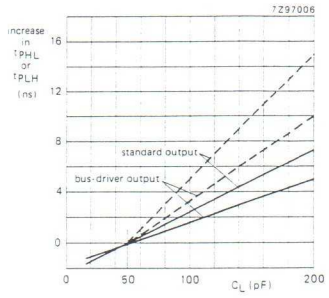
	V_{CC} (V)	maximum output transition time (ns) T_{amb} = 25 °C	T_{amb} = 85 °C	T_{amb} = 125 °C
standard	2	75	95	110
output	4.5*	15	19	22
	6	13	16	19
bus-driver	2	60	75	90
output	4.5*	12	15	18
	6	10	13	15

* 74HC and 74HCT devices; all other data for 74HC devices only.

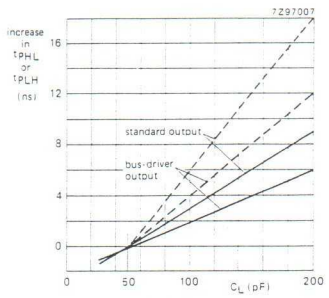
Table 4: Typical output transition times for load capacitances greater than the standard 50 pF load, see Fig.4

V_{CC}	t_{THL} or t_{TLH} standard output	bus-driver output
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

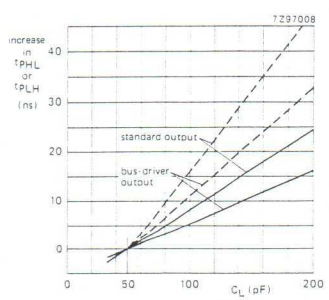
Note: values in pF are the load capacitance minus 50 pF.



(a) V_{CC} = 6 V



(b) V_{CC} = 4.5 V



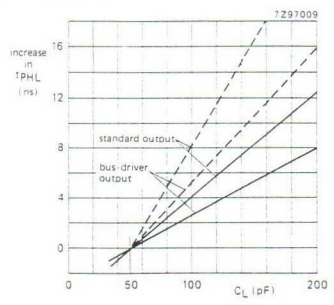
(c) V_{CC} = 2 V

– – – expected maximum

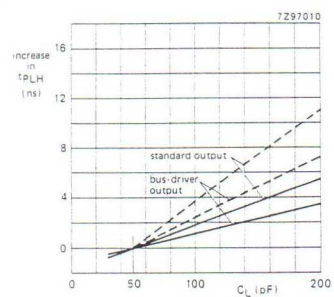
——— typical value

Fig. 5 Increase in propagation delay for 74HC devices as a function of load capacitance; T_{amb} = 25 °C.

A parameter specified for TTL devices is the output short-circuit current HIGH (I_{OS}). Originally intended to reassure the TTL user that the device would withstand accidental grounding, this parameter has become a measure of the ability of the circuit to charge the line capacitance and is used to calculate propagation delays. In CMOS devices however, there is no need to specify I_{OS} because the purely capacitive loads allow extrapolation of the a.c. parameters over the whole loading range. Figure 5 (for 74HC devices) and Fig.6 (for 74HCT devices) show the increase in propagation delay for loads greater than 50 pF. The additional delay can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs 33 to 36), the propagation delay is the time taken for the output voltage to reach 50% of V_{CC} for 74HC devices, or 1.4 V for 74HCT devices. Since a saturated output transistor acts as a current source, the additional delay is $\Delta CV/I$, where ΔC is the load capacitance minus 50 pF, V is the voltage swing at the output to the switching level of the next circuit, and I is the average source current of the saturated output.



(a) HIGH-to-LOW transition



(b) LOW-to-HIGH transition

– – – expected maximum
——— typical value

Fig. 6 Increase in propagation delay for 74HCT devices as a function of load capacitance; the different values for t_{PHL} and t_{PLH} are due to the asymmetrical reference level of 1.3 V at the outputs; T_{amb} = 25 °C; V_{CC} = 4.5 V.

Supply voltage dependence of propagation delay

The dynamic performance of a CMOS device depends on its drain characteristics. These are related to the switching thresholds and the gate-to-source voltage V_{GS} which is equal to the supply voltage V_{CC}. A reduction in V_{CC} adversely affects the drain characteristics, increasing the propagation delays.

Over the supply voltage range of 74HCT devices, 4.5 V to 5.5 V, the effects of different propagation delays on performance are minimal. Over the supply voltage range of 74HC circuits, 2 to 6 V, the effects on performance are significant, see Figs 7 and 8.

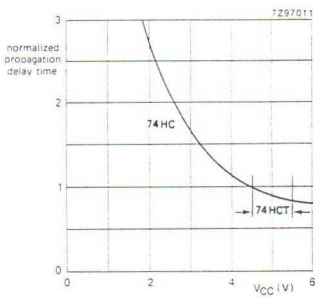


Fig. 7 Propagation delay as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

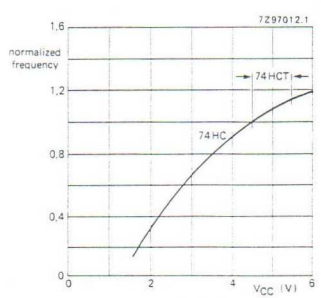


Fig. 8 Operating frequency as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

Temperature dependence of propagation delay

In TTL circuits, β (current gain), internal resistances and forward-voltage drops are all temperature-dependent. In HCMOS circuits, essentially only the carrier mobility, which affects the propagation delay, is temperature dependent. In general, propagation delay increases by about 0.3% per °C above 25 °C.

Between 25 °C and 125 °C,

$$t_p = t_p'(1.003)^{T_{amb}-25}$$

where:
t_p' is the propagation delay at 25 °C,
T_{amb} is the ambient temperature in °C.

Between −40 °C and +25 °C,

$$t_p = t_p'(0{,}997)^{25-T_{amb}}$$

Figure 9 shows the temperature dependence of a characteristic such as propagation delay.

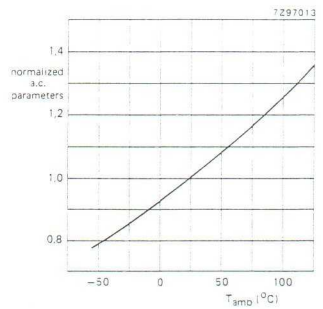


Fig. 9 Typical influence of temperature on AC parameters; V_{CC} = 5 V.

Derating system for AC characteristics

Because HCMOS devices are a coherent family, manufactured under strictly-controlled conditions, it is possible to have a common set of derating coefficients for temperature and supply voltage that is valid for all AC characteristics of all devices. Table 5 shows the derating coefficients which are derived from the published values of the AC characteristics at 25 °C for V_{CC} = 4.5 V, denoted by x in the Table. The coefficients have been established after extensive high-temperature testing at many supply voltages. A temperature coefficient of −0.4%/°C was established after comparing the test results with worst-case calculations. The voltage derating given in Table 5 is conservative compared with that shown in Fig.7 for propagation delay. For operating frequencies (Fig.8), the reciprocal of the derating coefficients shown should be used.

Table 5: Derating coefficients for the AC characteristics of HCMOS devices

supply voltage	ambient temperature 25 °C	85 °C	125 °C
2 V	5 (5x)	6.25 (5y)	7.5 (5z)
4.5 V*	1 (x)	1.25 (y = 1.25x)	1.5 (z = 1.5x)
6 V	0.85 (0.85x)	1.0625 (0.85y)	1.275 (0.85z)

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

* 74HC and 74HCT devices; all other data for 74HC devices only.

Clock pulse requirements

All HCMOS flip-flops and counters contain master-slaves with level-sensitive clock inputs. When the voltage at the clock input reaches the voltage threshold of the device, data in the master (input) section is transferred to the slave (output) section. The threshold for 74HC devices is typically 50% of V_{CC} and that for 74HCT devices is 28% of V_{CC} (1.4 V at V_{CC} = 5 V). The thresholds are virtually independent of temperature.

The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at V_{CC} = 4.5 V).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at the clock input, which eliminates the need to specify a maximum rise/fall time. The flip-flops 74HC/HCT73, 74, 107, 109 and 112 have special Schmitt-trigger circuits for increased tolerance to slow rise/fall times and ground noise.

The published maximum input clock frequency ratings for clocked devices are for a 50% duty factor input clock. At these rated frequencies, the outputs will swing between V_{CC} and GND, assuming no DC load on the outputs. This is a very conservative and reliable method of rating the

clock-input-frequency limits for HCMOS devices which are always at least as good as those for LSTLL even though they may appear to be inferior. This is because the maximum operating frequency of a TTL device is published, not for a 50% duty factor clock, but for a minimum clock pulse width.

System (parallel) clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig.10.

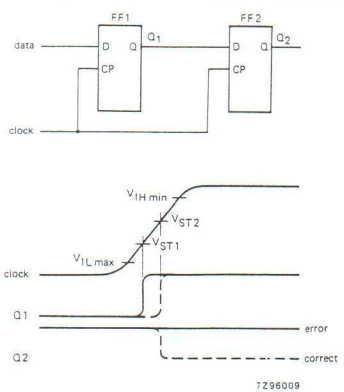


Fig. 10 In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors. V_{ST1} is the clock threshold of device 1; V_{ST2} is the clock threshold of device 2.

To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

For a HCMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for V_{CC} = 2 V, 4.5 V and 6 V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

Clock pulse considerations as functions of maximum frequency

The minimum input frequency is measured with a clock that has a 50% duty factor. For a stand-alone flip-flop, the following direct relationship exists between the minimum required width of the clock pulse t_W LOW or t_W HIGH (whichever is the longest) and the measured maximum frequency:

$$f_{max} = 1/2t_W$$

If two or more flip-flops are synchronously clocked in parallel, other timing conditions may cause a lower maximum frequency than that which can be calculated from the pulse width measurements. An example is shown in Fig.11.

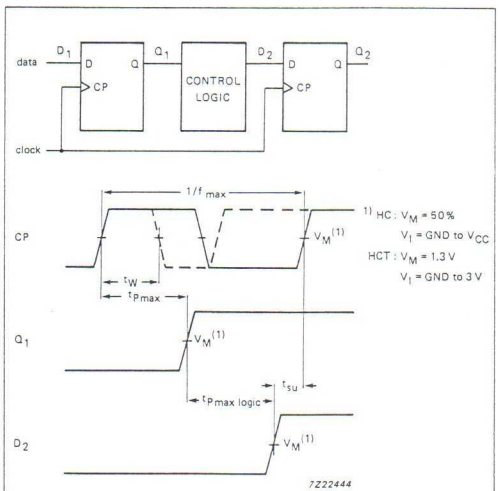


Fig. 11 Timing conditions for parallel clocking.

The maximum frequency is now determined by:

$$f_{max} = \frac{1}{t_{P\ max}(CP \text{ to } Q_1) + t_{P\ max}(\text{control logic}) + t_{su}(D_2 \text{ to } CP)}$$

The measured minimum width (t_W) of the clock pulse as shown in Fig.11 would suggest a higher obtainable frequency in this example. This parallel clocking scheme is often encountered in counter circuits (e.g. '160' or '190' series).

If the internal delays and set-up times exceed the minimum required duration for the clock pulse, the maximum frequency will be entirely determined by these internal delays and set-up times.

Cascading HCMOS counters in a parallel clocking scheme may also result in lower maximum frequencies than those given for stand-alone ICs. This is because the frequency will then be determined by the propagation delay of a count output, for example the delay of the intermediate logic and the set-up time between the clock enable and the count input of the succeeding counter IC.

Minimum AC characteristics

Minimum propagation delays are not specified in the data sheets. However, an increasing number of HCMOS users are asking for minimum propagation delay values so that they can make conclusive data handling calculations. Since our test programs don't include lower limits for propagation delays, it's impossible for us to guarantee these values for the entire HCMOS family. However, propagation delays for the whole HCMOS family have been constantly monitored by our Quality Department over the past three years. The very small deviations from the typical values that were observed between May 1985 and February 1988 are shown, together with their three sigma values, in Fig.12. The indicated mean value $\bar{x}$ is within a few percent of the published typical values. Users can derive their own minimum expected values from this figure and the typical propagation delays published in the data sheets.

A conservative estimate of minimum propagation delay is one third of the typical value. For set-up and hold times, the guard-band which should be applied to obtain max./min. limits is 5 ns for typical values between the limits of −5 ns and +5 ns. For typical values beyond −5 ns and +5 ns, the distribution shown in Fig.12 applies.

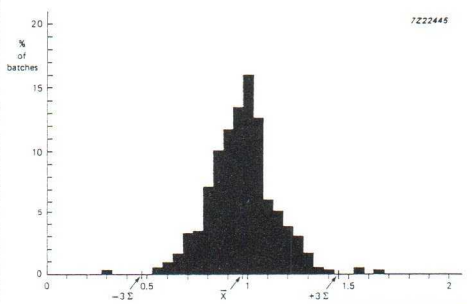


Fig. 12 Batch-to-batch variation of propagation delay (t_{PLH}/t_{PHL}).

Table 6 gives the derating coefficients for calculating the minimum propagation delays of HCMOS devices at various supply voltages and temperatures.

Table 6: Derating coefficient for the expected minimum propagation delay of HCMOS devices

supply voltage	ambient temperature 25 °C	−40 °C
2 V	2 (2x)	1.67 (2y)
4.5 V*	1 (x)	0.83 (y = 0.83 x)
6 V	0.8 (0.8x)	0.66 (0.8y)

Note: The minimum value is reached at the lowest possible temperature.

All coefficients are derived from the value of the AC characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

* 74HC and 74HCT devices; all other data for 74HC devices only.

POWER DISSIPATION

Static

When a HCMOS device is not switching, the p-channel and n-channel transistors don't conduct at the same time, so leakage current flows between V_{CC} and GND. Because this leakage current is typically a few nA, HCMOS power dissipation is extremely low.

Static power dissipation can be calculated for both 74HC and 74HCT devices from the maximum quiescent current specified in the data sheets, see Table 7.

Table 7: Maximum quiescent current of HCMOS devices at V_{CCmax}* (V_I = V_{CC} or GND; I_O = 0)

device complexity	quiescent current typical at 25 °C	maximum 25 °C	maximum 85 °C	maximum 125 °C
SSI	2 nA	2 μA	20 μA	40 μA
FF	4 nA	4 μA	40 μA	80 μA
MSI	8 nA	8 μA	80 μA	160 μA
LSI	50 nA	50 μA	500 μA	1000 μA

* 6 V for 74 HC; 5.5 V for 74 HCT.

Dynamic

When a device is clocked, power is dissipated charging and discharging on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. However, this transient energy loss is typically only 10% of that due to parasitic capacitance.

The total dynamic power dissipation per device (P_D) is:

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \quad (1)$$

where:

C_{PD} is the power dissipation capacitance per package
f_i is the input frequency
f_o is the output frequency
C_L is the total external load capacitance per output.

The second term of equation (1) implies summing the product of the effective output load capacitance and frequency for each output. However, a good approximation of the total dynamic power dissipation of an HCMOS system can be obtained by summing the published C_{PD} values and load capacitance for the HCMOS devices used and, assuming an average frequency, using equation (1).

For one-shot circuits, gates configured as oscillators, phase-locked loops and devices used in a linear mode, additional dissipation is caused by static supply currents (I_{CC}) whose values are given in the device data sheets.

Power dissipation capacitance

C_{PD} is specified in the device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Fig.13. The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Table 8 gives the pin status for HCMOS devices during a C_{PD} test. Devices which can be separated into independent sections are measured per section, the others are measured per device.

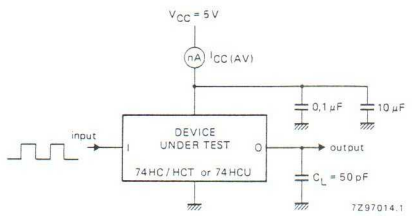


Fig. 13 Test set-up for determining C_{PD}. The input pulse is a square wave between V_{CC} and GND; $t_r = t_f \leqslant 6$ ns; $T_{amb} = 25\,^{\circ}C$. All switching outputs are loaded with 50 pF (including test jig capacitance). Unused inputs are connected to V_{CC} or GND.

The recommended test frequency for determining C_{PD} is 1 MHz, but this is best increased to 10 MHz when I_{CC} is low and the device quiescent current influences $I_{CC(AV)}$. Loading the switched outputs gives a more realistic value of C_{PD}, because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

The values of C_{PD} in the data sheet have been calculated using:

$$C_{PD} = \frac{I_{dyn(device)}}{V_{CC} f_i}$$

where:

$I_{dyn(device)} = I_{CC(AV)} - I_{dyn(load)}$
and
$I_{dyn(load)} = \Sigma(C_L V_{CC} f_o)$

USER GUIDE

Table 8: Pin conditions for C_{PD} tests.

74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
02	50	C	P	L	O	D	D	G	D	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
03	0	P	H	B	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
U04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
08	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
11	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
20	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
21	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
27	50	P	L	D	D	D	O	G	O	D	D	D	C	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
30	50	P	H	H	H	H	H	G	C	O	O	H	H	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
42	100	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	–	–	–	–	–	–	–	–	–	–	–	–
58	50	P	D	D	D	D	O	G	O	L	L	L	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
73	50	P	H	H	V	D	D	D	O	O	D	G	C	C	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
74	50	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
75	50	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	–	–	–	–	–	–	–	–	–	–	–	–
85	50	L	H	P	H	O	C	O	G	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
86	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
107	50	H	C	C	H	O	O	G	D	D	D	D	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
109	50	H	H	L	P	H	C	C	G	O	O	D	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
112	50	P	H	H	H	C	C	O	G	O	D	D	D	D	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
123	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
125	50	L	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
126	50	H	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
132	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
133	50	P	H	H	H	H	H	H	G	C	H	H	H	H	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–

Table 8: Pin conditions for C_{PD} tests.

74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
137	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
138	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
139	100	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
147	50	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
151	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
153	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
154	100	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V	–	–	–	–
157	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
158	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
160	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
161	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
162	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
163	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
164	200	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
165	50	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
166	25	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
173	25	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	–	–	–	–	–	–	–	–	–	–	–	–
174	25	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–
175	50	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
181	300	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	C	L	H	L	H	L	H	V	–	–	–	–
182	150	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	–	–	–	–	–	–	–	–	–	–	–	–
190	55	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
191	53	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
192	55	D	C	C	H	P	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
193	50	D	C	C	H	P	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
194	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
195	125	H	H	L	D	D	D	D	G	H	P	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
221	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
237	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
238	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
240	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–	–	–
241	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–	–	–
242	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
243	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
244	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–	–	–
245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–
251	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
253B	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
257	50	P	L	H	C	D	D	O	G	O	D	D	O	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
258	50	P	L	H	C	D	D	O	G	O	D	D	O	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
259	25	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–
273	25	H	C	Q	D	O	O	D	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–
280	100	L	L	O	L	C	C	G	P	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
283	250	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	–	–	–	–	–	–	–	–	–	–	–	–
297	12	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
299	250	H	L	L	C	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	–	–	–	–	–	–	–	–
354	100	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	–	–	–	–	–	–	–	–
356	50	D	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	L	H	C	C	V	–	–	–	–	–	–	–	–
365	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
366	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
367	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
368	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
373	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
374	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
377	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
390	50	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
393	47	P	L	C	C	C	C	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–

74HC/ HCT	equiv. load (pF)	pin numbers 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
423	100	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
533	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
534	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
563	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
564	25	L	Q	D	D	D	D	D	D	D	G	P	O	D	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
573	25	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
574	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
583	200	H	H	H	L	H	C	C	G	C	C	C	L	P	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
594	225	C	C	C	C	C	C	C	G	C	H	P	P	H	Q	C	V	–	–	–	–	–	–	–	–	–	–	–	–
595	225	C	C	C	C	C	C	C	G	C	H	P	P	P	Q	C	V	–	–	–	–	–	–	–	–	–	–	–	–
597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
640	25	H	P	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
643	50	H	P	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
646	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
648	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
652	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
670	200	L	L	L	L	P	C	C	G	C	C	L	H	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–
4002	50	C	P	L	L	L	O	G	O	D	D	D	D	O	V	–	–	–	–	–	–	–							
4015	100	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	–	–	–	–	–	–						
4016	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–							
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	–	–	–	–	–	–						
4020	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–						
4024	48	P	L	C	C	C	C	G	O	C	O	C	C	O	V	–	–	–	–	–	–	–							
4040	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–						
4046A	50	O	C	L	O	H	O	O	G	L	O	O	O	O	P	O	V	–	–	–	–	–	–						
4049	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–						
4050	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–						

74HC/ HCT	equiv. load (pF)	pin numbers
4051	0	O O O O O L G G L L P O O O O V – – – – – –
4052	0	O O O O O L G G L L P O O O O V – – – – – –
4053	0	O O O O O L G G L L P O O O O V – – – – – –
4059	17	P D H L L L L L L L H G H H L L L L L L L L C V – –
4060*	106	C C C C C C C G C C P L C C C V – – – – – –
4066	0	O O O O D D G O O O O D P V – – – – – – – –
4067	0	O O O O O O O O O P L G L L L O O O O O O O O V – –
4075	75	P L D D D O G L C O D D D V – – – – – – –
4094	250	H Q P C C C C G C C C C C C H V – – – – – –
4316	0	O O O O P D L G G O O O O D D V – – – – – –
4351	0	O O O O O O L H G G H P L O L O O O O V – – – –
4352	0	O O O O O O L H G G H P L O L O O O O V – – – –
4353	0	O O O O O O L H G G H P L O L O O O O V – – – –
4510	55	L C D D L C C G L H C D D C P V – – – – – –
4511	200	L L H H L L P G C C O O C O C V – – – – – –
4514	100	H P L O O O O O C O C G O O O O O O O O L L L V – –
4515	100	H P L O O O O O C O C G O O O O O O O O L L L V – –
4516	50	L C D D L C C G L H C D D C P V – – – – – –
4518	45	P H C C C C L G D D O O O O D V – – – – – –
4520	47	P H C C C C L G D D O O O O D V – – – – – –
4538	100	G R H P H C C G O O D D L O G V – – – – – –
4543	50	H L L H L P L G C C C C O O O V – – – – – –
5555	–	not applicable
6323A	7	C O O G O O P V – – – – – – – – – –
7014	50	P C D O D O G O D O D O D V – – – – – – – – – – – – – –
7030	7	G G C P Q Q Q Q Q Q Q Q Q G L C C C C C C C C C C P H V
7046A	50	O C L O H O O G L O O O O P O V – – – – – –
7080	50	L P L L L L L L L G L L L L L L L C V – – – – – –
7132	–	not applicable
7245	50	H P D D D D D D D G O O O O O O C L V – – – – – –
7266	50	P L C O D D G D D O O D D V – – – – – – –
7403	200	L C P Q Q Q Q G H C C C C C P V – – – – – –

74HC/ HCT	equiv. load (pF)	pin numbers																						
7404	225	L	C	P	Q	Q	Q	Q	G	H	C	C	C	C	C	P	V	–	–	–	–	–	–	
7540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–
7541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–
7597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	
7731	25	C	P	Q	L	D	D	O	G	O	D	D	D	D	D	O	V	–	–	–	–	–	–		
9014	50	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–
9015	50	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–
9046	–	not applicable																							
9114	0	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	B	V	–	–	–	–
9115	0	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	V	–	–	–	–
40102	5	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–		
40103	3	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–		
40104	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–		
40105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	C	P	V	–	–	–	–	–	–		

* load word;

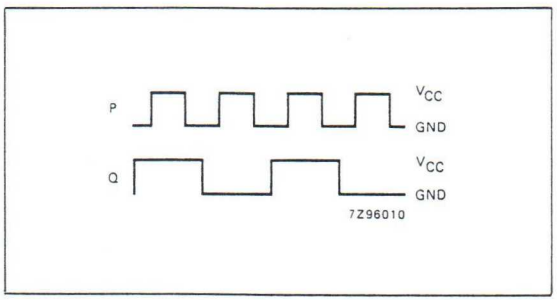
0:	0	0	0	0
1:	1	1	1	1
2:	X	X	X	X
3:	X	X	X	X

USER GUIDE

Key

V	=	V_{CC} (+5V)
G	=	ground
H	=	logic 1 (V_{CC}) - inputs at V_{CC} for HC types; 3.5 V for HCT types
L	=	logic 0 (ground)
D	=	don't care - either H or L but not switching
C	=	a 50 pF load to ground is allowed
O	=	an open pin; 50 pF to ground is allowed
P	=	input pulse (see ilustration)
Q	=	half frequency pulse (see illustration)
R	=	1 kΩ pull-up resistor to an additional 5 V supply other than the V_{CC} supply
B	=	both R and C.

Input pulses



Conditions for C_{PD} tests

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. C_{PD} is specified per-independent-decoder.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With three-state multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches. The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

Three-state buffers and transceivers. C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. Three-state latches are measured with their outputs enabled. C_{PD} is specified per-latch.

Flip-flops. Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a squarewave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

Additional power dissipation in 74HCT devices

When the inputs of a 74HCT device are driven by a TTL device at the specified minimum HIGH output level of V_{OH} = 2.4 V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current (ΔI_{CC}). This current has been considerably reduced by proprietary development of 74HCT input stages, see '74HCT inputs'.

The value of ΔI_{CC} specified in the data sheets is per input and at the worst-case input voltage of V_{CC}-2.1 V for V_{CC} between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum V_{CC} and minimum V_{OH}), see Table 9.

The additional power dissipation P is:

$P = V_{CC} \times \Delta I_{CC} \times$ duty factor HIGH $\times$ unit load coefficient

The unit load coefficient for an input is a factor by which the value of ΔI_{CC} given in the data sheet has to be multiplied. A unit load coefficient is published for each 74HCT device. It is a function of the size of the input p-channel transistor.

Table 9: Worst-case additional quiescent supply current (ΔI_{CC}) for 74HCT devices

	T_{amb} (°C)				UNIT	TEST CONDITIONS		
	74HCT					V_{CC} V	V_I	OTHER
	+25		−40 to +85	−40 to +125				
	typ.	max.	max.	max.				
ΔI_{CC} per input pin for a unit load coefficient of 1*	100	360	450	490	μA	4.5 to 5.5	V_{CC}−2.1 V	other inputs at V_{CC} or GND I_O = 0

* The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

Power dissipation due to slow input rise/fall times

When an output stage switches, there is a brief period when both output transistors conduct. The resulting 'through-current' is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time.

As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at $V_I = 0.5\,V_{CC}$ for 74HC devices, and $V_I = 28\%V_{CC}$ for 74HCT devices, the maximum current being determined by the geometry of the input transistors. The through-current is proportional to $V_{CC}{}^n$ where n is about 2.2. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig.14.

When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation, see Schmitt-trigger data sheets. In the case of RC oscillators, or oscillators constructed with Schmitt triggers this contribution to the power dissipation is frequency-dependent.

Comparison with LSTTL power dissipation

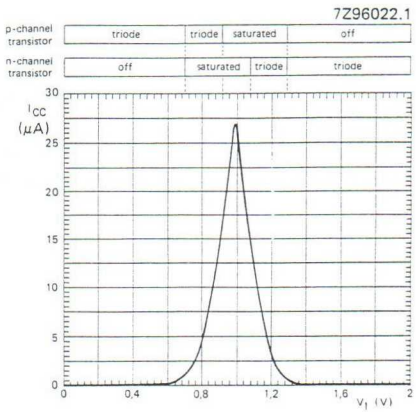
The dynamic power dissipation of a HCMOS device is frequency-dependent; above 1 MHz, that of an LSTTL device is too. Below 1 MHz, the dynamic component of power dissipation of an LSTTL device is negligible compared to the static component. Figure 15 shows the average power dissipation of four HCMOS devices and their LSTTL equivalents. Because all functions in a multi-functional LSTTL device are biased when power is applied, for comparison, the dissipation of whole HCMOS devices besides individual functions are given.

In Fig.15 it can be seen that:

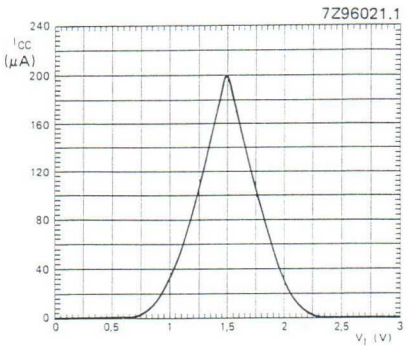
- for SSI gate types, the HCMOS power dissipation is less than LSTTL power dissipation below about 1 MHz
- for more complex types such as a 74HC/HCT138 3-to-8 line decoder HCMOS power dissipation is less than LSTTL power dissipation up to 10 MHz.

In typical microcomputer systems, the operating frequency or the data/address signal rates will usually vary, whereas Fig.15 is for continuous operation at a constant frequency. Average operating frequencies are usually far below the peak frequencies, particularly in the 100 kHz region where the power dissipation of HCMOS is several orders of magnitude less than that of LSTTL.

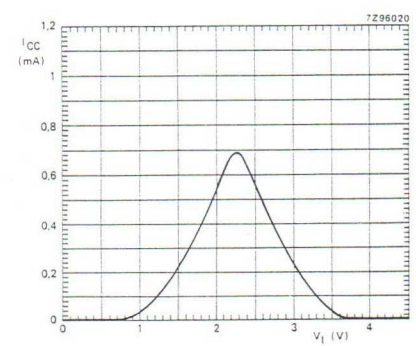
For further information, see chapter 'Power dissipation'.



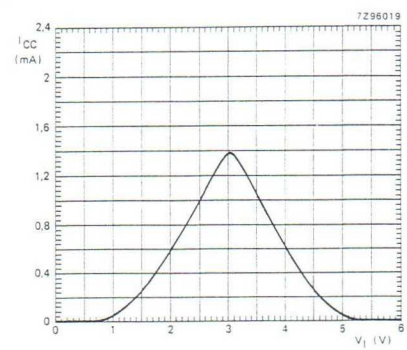
(a) V_{CC} = 2 V



(b) V_{CC} = 3 V



(c) V_{CC} = 4.5 V



(d) V_{CC} = 6 V

Fig. 14 Typical DC supply current as a function of input voltage for 74HC circuits; normalized curves for a unit load coefficient of 1. The I_{CC} for a specific 74HC circuit can be calculated by multiplying the values of I_{CC} shown by the unit load coefficient for the 74HCT type given in the data sheet.

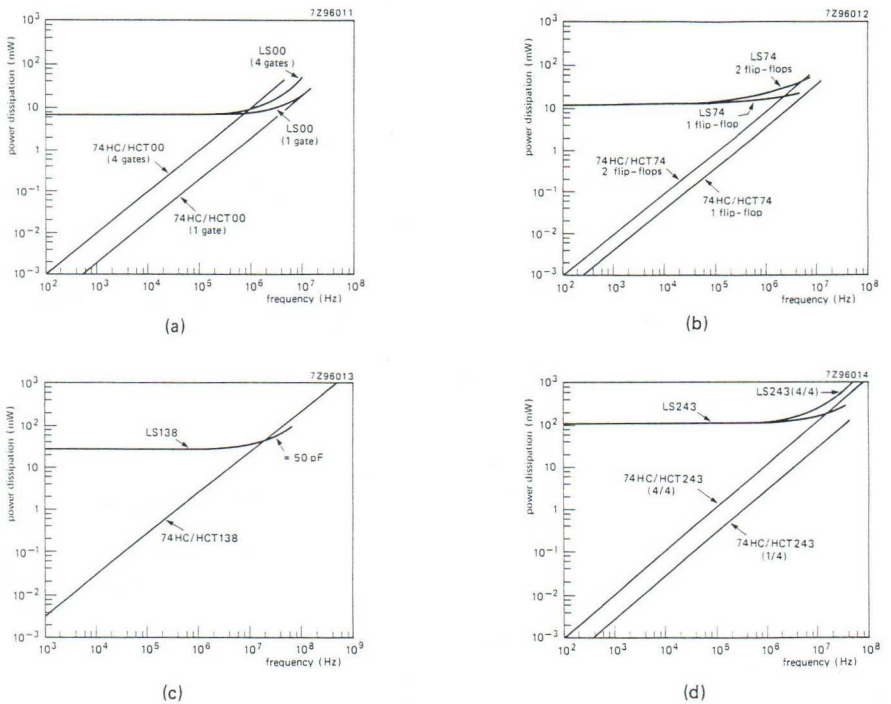


Fig. 15 Typical power dissipation as a function of operating frequency for a variety of LSTTL and HCMOS circuits; (a) quad 2-input NAND gate, (b) dual D-type flip-flop, (c) 3-to-8 line decoder/demultiplexer; inverting, (d) quad 3-state bus transceiver.

SUPPLY VOLTAGE

Range

The supply voltage range of 74HC devices is 2 V to 6 V (Fig.16). This ensures continued use of HCMOS with future generations of memory and microcomputer requiring supply voltages of less than 5 V, simplifies the regulation requirements of power supplies, facilitates battery operation and allows lithium battery back-up. When 74HC devices are used in linear applications, for example when they are used as RC oscillators, a supply of at least 3 V is recommended to ensure sufficient margin for operation in the linear region.

74HCT devices are pin-compatible with LSTTL circuits and are intended as power-saving replacements for them. The 74HCT devices will operate from the traditional 5 V LSTTL supply, but the voltage range is extended to ±10% for both LSTTL temperature ranges (−40 to +85 °C and −40 to +125 °C). This allows extended temperature range LSTTL devices to be replaced by 74HCT devices.

The absolute maximum supply or ground current per pin is ±50 mA for devices with standard output drive, and ±70 mA for devices with bus driver outputs. These currents are only drawn when the outputs of a device are heavily loaded. The average dynamic current at very high frequencies can be calculated using C_{PD}.

The maximum rated supply voltage of HCMOS devices is 7 V and any voltage above this may destroy the device, even though the on-chip parasitic diode break-down voltage is at least 20 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The V_{CC} and GND potentials must never be reversed as this can cause excessive currents to flow through the input protection diodes.

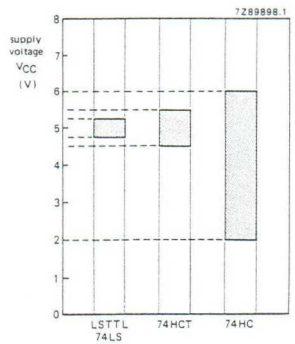


Fig. 16 Supply voltage ranges for LSTTL and HCMOS circuits. The supply voltage range for 74HCT circuits retain the LSTTL nominal supply of 5 V, but the range has been extended from ±5% to ±10% for both the standard and the extended temperature range. 74HC circuits operate with a supply voltage as low as 2 V.

Battery back-up

A battery back-up for a 74HC system is extremely simple. Figure 17 shows an example. The minimum battery voltage required is only 2 V plus one diode drop.

In the example, HIGH-to-LOW level shifters (74HC4049 or 74HC4050) prevent positive input currents into the system due to input signals greater than one diode drop above V_{CC}. If the circuit is such that input voltages can exceed V_{CC}, external resistors should be included to limit the input current to 15 mA for one input (7.5 mA per input for two inputs, 5 mA per input for three inputs, etc.).

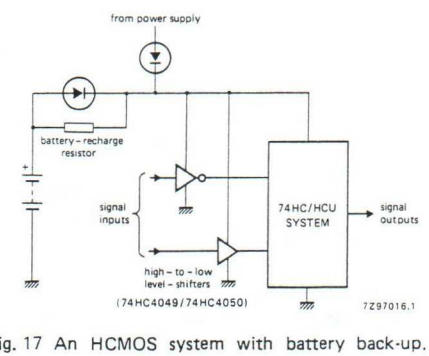


Fig. 17 An HCMOS system with battery back-up.

External resistors may also be necessary in the output circuits to limit the current to 20 mA if the output can be pulled above V_{CC} or below GND. These current limits are set by the parasitic V_{CC}/GND diodes present in all outputs, including three-state outputs.

For further information, see chapter 'Battery back-up'.

Power supply regulation and decoupling

The wide power supply range of 2 V to 6 V may suggest that voltage regulation is unnecessary. However, a changing supply voltage will affect system speed, noise immunity and power consumption. Noise immunity, and even the operation of the circuit, can be affected by spikes on the supply lines, so matched decoupling is always necessary in dynamic systems.

Both 74HC and 74HCT devices have the same power supply regulation and decoupling requirements. The best method of minimizing spikes on the supply lines is simple enough – use a good power supply, provide good ground bussing and low AC impedances from the V_{CC} and GND pins of each device. The minimum decoupling capacitance depends on the voltage spikes that can be tolerated, which in general should be limited to 400 mV. A local voltage regulator on a printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50 μF. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1 μF tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level-sensitive devices can be decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

For further information, see chapter 'Power supply decoupling'.

INPUT/OUTPUT PROTECTION

The gate input of a MOS transistor acts as a capacitor (<1 pF) with very low leakage current (<1 pA). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device.

The integration process of the HCMOS family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance of an HCMOS device is typically 100 Ω under all biasing conditions, even when V_{CC} is short-circuited to GND – an improvement over direct input diode clamps during power-up.

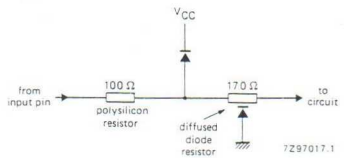


Fig. 18 Standard input protection of 74HC/HCT/HCU inputs against electrostatic discharge.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig.18). The typical forward voltage of the diodes is 0.9 V at 2 mA and the reverse breakdown voltage is 20 V. In some applications such as oscillators, the diodes conduct during normal operation, in which case the input current should be limited. The maximum positive input current $+I_{IK}$ per input is 20 mA. For devices with a standard output, the total positive input current is 50 mA; for devices with a bus-driver output, the total input current is 70 mA. The maximum negative input current $-I_{IK}$ per pin is:

14 mA for one input
9 mA for two inputs
6 mA for three inputs
5 mA for four inputs
4 mA for five inputs
3 mA for six to eight inputs.

High-to-low level shifters 74HC4049 and 74HC4050 have a single-sided input protection network (Fig.19) which protects against electrostatic input voltages. The diode D1 is the parasitic drain-to-GND diode of the thick field oxide protection device.

All input pins can withstand discharge voltages up to 2.5 kV (typ.) when tested according to MIL-STD-883B, method 3015, see Fig.20. The output configurations of standard, bus driver, three-state, open drain and I/O ports can withstand >3.5 kV (typ.) because of the large diodes formed by the drain surfaces of the output transistors.

Figure 21 shows the voltage pulse for the discharge test. The rise time t_r prescribed by MIL-STD-883B is ≤15 ns, but in practice it is helpful to adjust the test set-up to give a rise time of 13 ± 2 ns to avoid correlation problems.

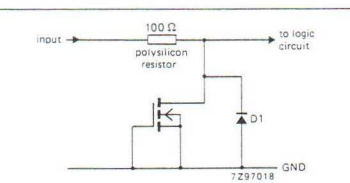
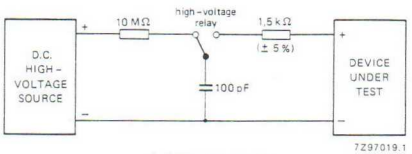


Fig. 19 Input protection of 74HC4049 and 74HC4050.

Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see chapter 'Handling precautions').



(a) Test circuit

mode	device under test	
	+	−
1	input	GND
2	GND	input
3	input	V_{CC}
4	V_{CC}	input
5	output	GND
6	GND	output
7	output	V_{CC}
8	V_{CC}	output
9	input	output
10	output	input
11	V_{CC}	GND
12	GND	V_{CC}

all other pins should be left open circuit

(b) Test modes

Fig. 20 Electrostatic discharge test.

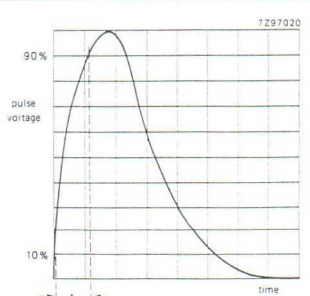


Fig. 21 Test voltage for electrostatic discharge test.

INPUT CIRCUITS

74HC inputs

The 74HC input circuit (Fig.22) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages greater than V_{CC} or less than GND. The circuit is intended for AC working and cannot handle heavy DC currents for long periods; the maximum input diode current is 20 mA.

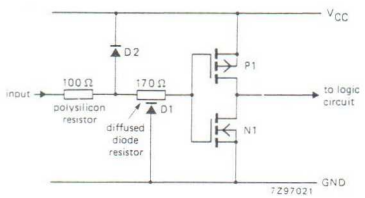


Fig. 22 74HC input circuit.

The 74HC input circuit has no active input current; the only current flowing is through the reversed-biased diodes D1 and D2, typically a few nA reaching a maximum when $V_I = V_{CC}$ or GND.

The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving a typical switching threshold of 50% V_{CC}, see Fig.23. This threshold is almost independent of temperature, a ±60 mV variation of the switching point from −40 to +125 °C being typical. The temperature dependence of V_{IL} is −0.6 mV/°C, that of V_{IH} is +0.6 mV/°C. The only other factors that affect the switching threshold are the spreads of β and V_T of P1 and N1 between devices.

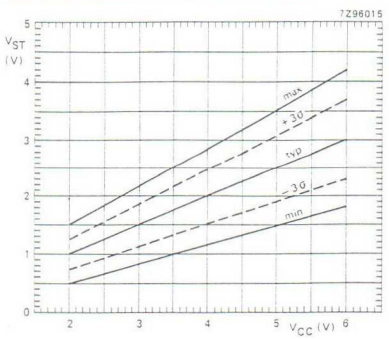


Fig. 23 74HC input switching level as a function of supply voltage.

There is no current path from V_{CC} to GND when the input is lower than V_{TN}, or higher than $V_{CC}-V_{TP}$. However, when the input voltage is in the linear region, a static current path from V_{CC} or GND flows in the input stage (Fig.14). This current is negligible under normal operating conditions when the input rise time $t_r \leqslant 15$ ns, but the power dissipation should be taken into account for devices operating in the linear region. Owing to the voltage gain of the input stage, there is no static flow-through current in the second and subsequent stages. Small currents do flow in these stages during operation when both n-channel and p-channel transistors conduct for brief periods and their effect is included in the C_{PD} value in the data sheets.

74HCT inputs

The 74HCT input stage is similar to that of a 74HC device. It has the same characteristics for LSTTL levels as a 74HC input has for CMOS levels, so there is no trade-off in speed or power dissipation. The switching threshold is lower, 1.4 V at V_{CC} = 5 V. In addition, the 74HCT input circuit, shown in Fig.24, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural drain voltage of the p-channel transistor (P1) is approximately $V_{CC}-0.6$ V, but when the input voltage is LOW, an auxiliary pull-up transistor (P2) raises this to V_{CC}, cutting off p-channel transistor P3 completely. The input stage is well matched to the load presented by the second stage so that symmetrical propagation delays are obtained.

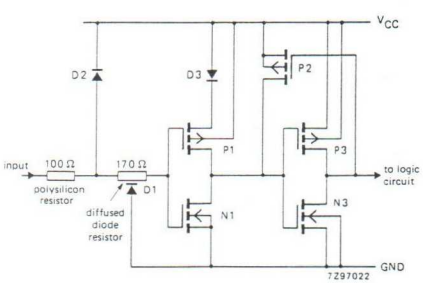


Fig. 24 74HCT input circuit.

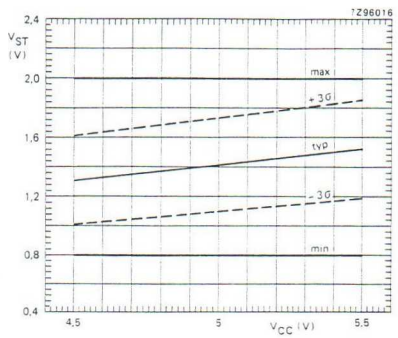


Fig. 25 74HCT input switching level as a function of supply voltage.

Figure 25 shows the switching level as a function of supply voltage.

A TTL HIGH level can be as low as 2.4 V. An input of this order to a HCMOS device would not cut off P1 completely, and additional supply current would flow through the input stage. A level-shift diode D3 and the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and gives an input switching level compatible with LSTTL. Figure 26 shows the input stage through-current with and without the diode circuit. The peak in the curve occurs at the input switching threshold.

The input stage through-current is virtually zero for a typical TTL HIGH level input of 3.5 V. Thus, this unique 74HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and maximum through-currents ΔI_{CC} per input are given in the data sheets.

In a system where 74HCT devices are only driven by LSTTL devices, $V_{OH\ min}$ can be 2.7 V except for some bus drivers. With V_{OH} = 2.7 V, ΔI_{CC} is half the published value.

Maximum input rise/fall times

All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 500 ns at V_{CC} = 4.5 V.

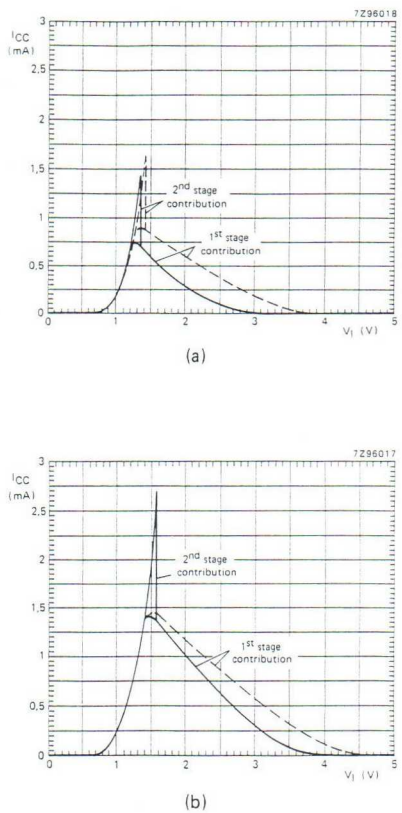


Fig. 26 Additional quiescent supply current ΔI_{CC} (typ.) per input pin of a 74HCT device as a function of supply voltage (unit load coefficient is 1); (a) V_{CC} = 4.5 V, (b) V_{CC} = 5.5 V.

The flip-flops 74HC/HCT73, 74, 107, 109 and 112 incorporate Schmitt-trigger input circuits and the 74HC/HCT14 and 132 are dedicated Schmitt triggers with specified input levels.

For further information, see chapter 'Schmitt trigger applications'.

Termination of unused inputs

To prevent any possibility of linear operation of the input circuitry of an LSTTL device, it is good practice to terminate all unused LSTTL inputs to V_{CC} via a 1.2 kΩ resistor. Inputs should not be connected directly to GND or V_{CC}, and they should not be left floating.

Unlike LSTTL inputs, the impedance of 74HC and 74HCT inputs is very high and unused inputs must be terminated to prevent the input circuitry floating into the linear mode of operation which would increase the power dissipation and could cause oscillation. Unused 74HC and 74HCT inputs should be connected to V_{CC} or GND, either directly (a distinct advantage over LSTTL), or via resistors of between 1 kΩ and 1 MΩ. Since the resistors used to terminate the inputs of LSTTL devices are usually between 220 Ω and 1.2 kΩ, it is often possible to directly replace LSTTL circuits with their 74HCT counterparts.

Some of the bidirectional (transceiver) logic devices in the HCMOS family have common I/O pins. These pins cannot be connected directly to V_{CC} or GND. Instead, when defined as inputs, they should be connected via a 10 kΩ resistor to V_{CC} or GND.

Input current

Figure 27 shows the typical input leakage current of a HCMOS device as a function of ambient temperature for a V_{CC} of 6 V. Over the total operating temperature range, the input leakage current is well below the rating specified in the JEDEC standard (100 nA between −55 °C and +25 °C and 1 μA at +85 °C and +125 °C. The reason for this difference between the measured performance and the rating is the high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the rating is end-of-line, allowing some leakage current shift due to the ingress of moisture or foreign material.

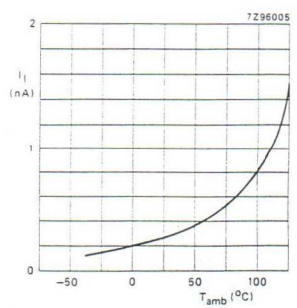


Fig. 27 Typical HCMOS input leakage current I_I as a function of ambient temperature T_{amb}.

Input capacitance

Since CMOS inputs present essentially no load, fan-out is limited only by the input capacitance. This is specified as 3.5 pF (typ.) and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Figs 28 and 29 show the typical input capacitances for powered 74HC and 74HCT devices. The initial decrease in capacitance as V_I rises from zero or falls from 5 V is due to increased reverse bias on the protection diodes. The peak is caused by internal Miller feedback capacitance when the inverter is in its linear mode. A conservative value for the maximum input capacitance is 10 pF (20 pF for I/O pins owing to the output drain capacitance). Input capacitance is measured with all other inputs tied to ground.

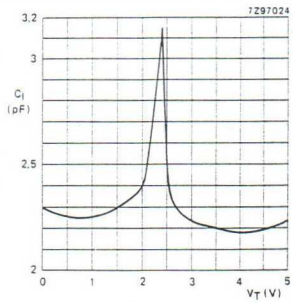


Fig. 28 Typical input capacitance C_I of a 74HC device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

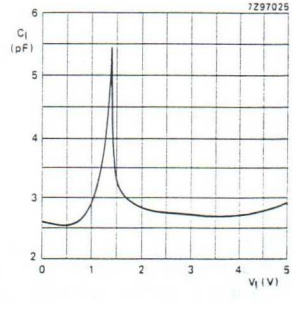


Fig. 29 Typical input capacitance C_I of a 74HCT device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

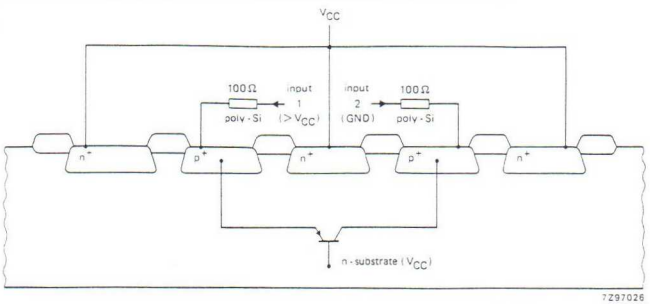


Fig. 30 Cross-section of the input protection of an HCMOS device showing the parasitic pnp transistor between adjacent inputs.

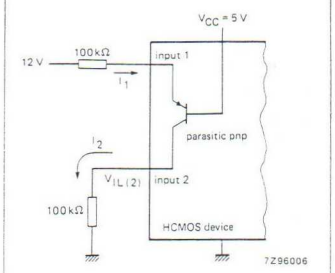


Fig. 31 12 V-to-5 V logic-level conversion at HCMOS inputs using 100 kΩ series resistors.

Coupling of adjacent inputs

Parasitic bipolar pnp transistors can be present between adjacent inputs, e.g. between an input protection diode to V_{CC} and the same diode at the adjacent input, as shown in Fig.30. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current into the terminal (I_1) can cause a current I_2 in the parasitic transistor and in the adjacent input (Fig.31). Because I_2 in the adjacent input has to be drained by the source driving that input, the source resistance (R) must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

The ratio of the parasitic adjacent input current (I_2) to the forced input current (I_1) denoted α:

$$\alpha = \frac{I_2}{I_1}.$$

α has been reduced to less than 0.05 (typically 0.001) in the HCMOS family by the use of deep guard rings and optimum bonding pad spacing.

A low α permits proper logic operation in the presence of transients and also allows HIGH-to-LOW voltage translation simply by adding series input resistors. For example, in Fig.31, 12 V system logic is converted to 5 V system logic by adding a 100 kΩ resistor in each input. Since the logic signals are delayed by 1-2 μs, this arrangement is suitable for rather slow 12 V control logic such as that in automotive applications. When the input diodes are used as clamps for logic level translation, the total input current should be limited to 20 mA.

Input voltage and forward diode input current

As a general rule, CMOS logic devices with input clamp diodes (Fig.18) should be operated between the power supply rails. Neglecting the input series polysilicon resistor shown in Fig.18, this means: $-0.5\ V \leqslant V_I \leqslant V_{CC} + 0.5\ V$.

This rule is JEDEC Std. No. 7A and is intended to prevent users damaging devices similar to HCMOS that do not have the polysilicon resistor. HCMOS devices however meet the tougher rating: $-1.5\ V \leqslant V_I \leqslant V_{CC} + 1.5\ V$. Furthermore, virtually all HCMOS devices can operate reliably up to the rating without logic errors.

The maximum permissible continuous current forced into an input or output of a HCMOS device is ±20 mA (JEDEC rating).

OUTPUT CIRCUITS

Output drive

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All 74HC and 74HCT outputs are buffered for consistent current drives and AC characteristics throughout the HCMOS family. Well-matched output n-channel and p-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of HCMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that a system will operate correctly with worst-case LOW and HIGH input signals and that noise immunity margins will be preserved. HCMOS capability is expressed as the source or sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept is not applicable.

With a specified output drive of 4 mA (at V_{OLmax} = 0.4 V), the HCMOS capability exceeds 4000 ULs, and with a 20 μA (at V_{OL} = 0.1 V) specification the HCMOS capability is 20 ULs. A standard HCMOS output can drive ten LSTTL loads and maintain $V_{OL} \leqslant 0.4$ V over the full temperature range. A bus driver output can drive 15 LSTTL loads under the same conditions. Table 10 shows the output drive capabilities of some HCMOS devices expressed in LSTTL unit loads. The output current may be increased for higher output voltages. For example, extrapolating the 6 mA bus driver capability at V_{OL} = 0.33 V and T_{amb} = 85 °C to a V_{OL} of 0.5 V gives an output drive capability of 9 mA.

Output current derating as a function of temperature is shown in Fig.32 and is valid for all types of output. Output source and sink drives at V_{CC} = 2 V, 4.5 V and 6 V are given in Figs 33 to 36 which show the output current as a function of output voltage; these graphs indicate the typical output currents and the expected minimum output currents. They can serve as a design aid when calculating transmission line effects or when charging highly capacitive loads.

The expected minimum curves are not guaranteed; they are tested only at the values given in the data sheets.

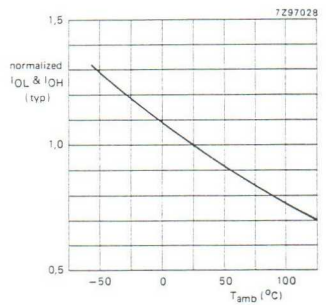
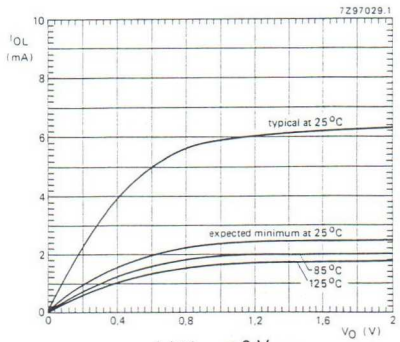


Fig. 32 Derating curve for output drive currents I_{OL} and I_{OH}.

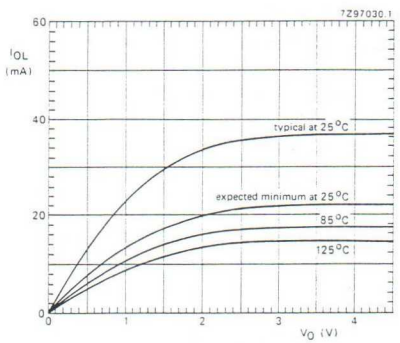
Table 10: Comparison of the output drive capabilities of LSTTL and HCMOS ($V_{OL} \leqslant 0.4$ V)

LS device	output	drive capacity	HCMOS equiv.	type	output	drive capacity
74LS00	4 mA	10 UL	74HC00	standard	4 mA	10 UL
74LS138	4 mA	10 UL	75HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

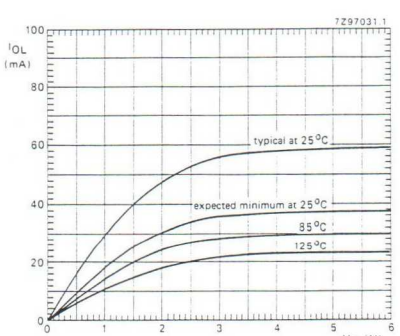
UL = unit load.



(a) V_{CC} = 2 V

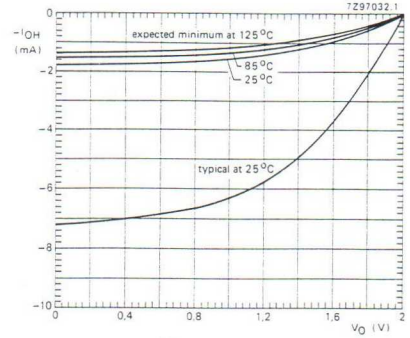


(b) V_{CC} = 4.5 V

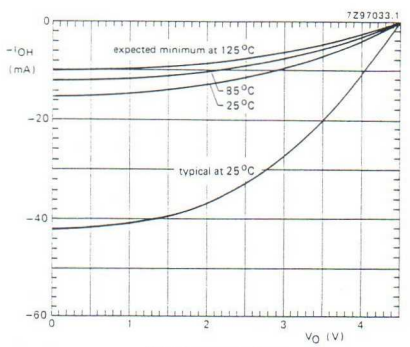


(c) V_{CC} = 6 V

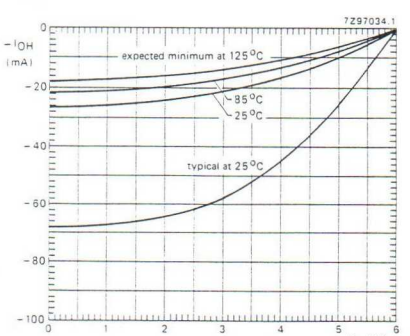
Fig. 33 Standard output n-channel sink current.



(a) V_{CC} = 2 V

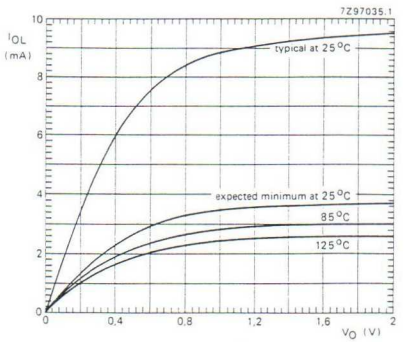


(b) V_{CC} = 4.5 V

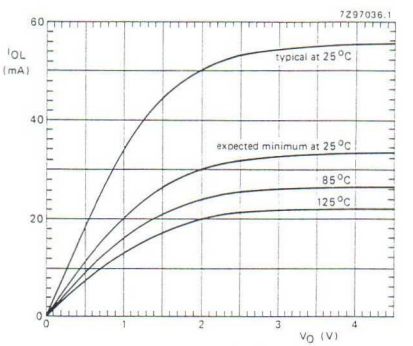


(c) V_{CC} = 6 V

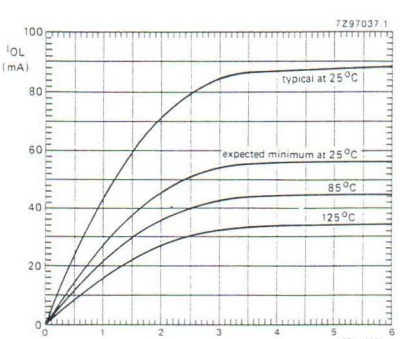
Fig. 34 Standard output p-channel source current.



(a) V_{CC} = 2 V

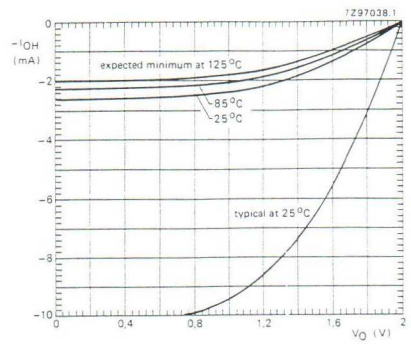


(b) V_{CC} = 4.5 V

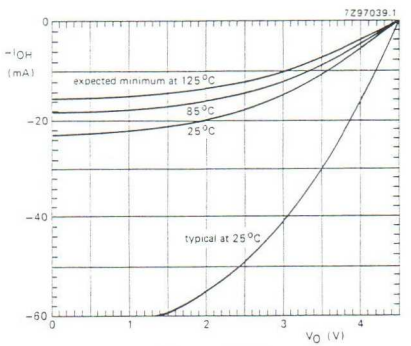


(c) V_{CC} = 6 V

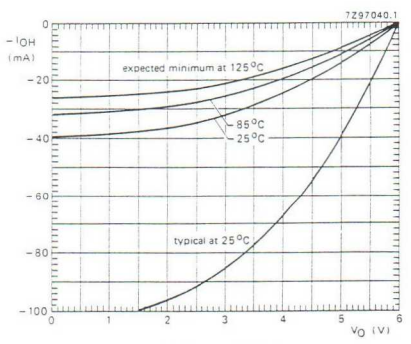
Fig. 35 Bus-driver output n-channel sink current.



(a) V_{CC} = 2 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 6 V

Fig. 36 Bus-driver output p-channel source current.

Push-pull outputs

A typical push-pull output stage is shown in Fig.37. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage V_O of all HCMOS devices in the case of externally-forced voltages such that $-0.5\ V \leqslant V_O \leqslant V_{CC} + 0.5\ V$. For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA DC, line ringing and power supply spikes in normal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminium traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry.

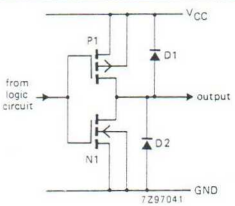


Fig. 37 Basic CMOS output stage.

The maximum rated DC current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminium migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum DC current rating to be exceeded. However, one output may be shorted for up to 5 s without causing any direct damage to the IC.

The life of the IC will not be shortened if not more than **one** input or output at a time is forced to GND or V_{CC} during in-circuit logic testing ('back drive') as long as the following rules are obeyed:

- maximum duration : 1 ms
- maximum duty factor : 10 %
- maximum V_{CC} : 6 V

Non-standard inputs or outputs may not be in-circuit tested. Examples of non-standard inputs/outputs are:

- timing pins (R_X, C_X) of monostables '123', '221', '423' and '4538'
- the Y and Z pins of all compensated analog switches ('4051' series, '4351' series, '4066' and '4077')
- pins for external timing components of PLLs '4046A' and '7046A'
- the R_{TC} and C_{TC} pins of the '4060'.

The only exception to this rule is the non-standard output of the '4511'.

Three-state outputs

In the typical three-state output circuit shown in Fig.38, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors. A LOW at EO puts the output in the high-impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output and its function table is shown in Fig.39.

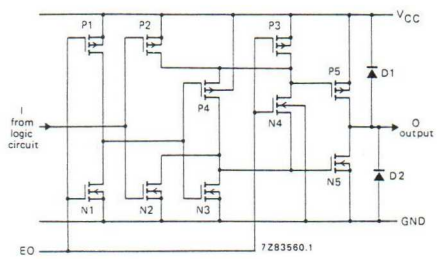
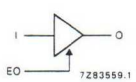


Fig. 38 Typical three-state output circuit.



(a) logic symbol

inputs		outputs
I	EO	O
X	L	Z
L	H	L
H	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

(b) function table

Fig. 39 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. To minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. In general, this requires that the output enable signals should not overlap. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This avoids overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

When designing with three-state outputs, note that disable propagation delays are measured for an RC load when the output voltage has changed by 10% of the voltage swing. This 10% level is adequate to ensure that a device output has turned off. Although this method provides a standard reference for measuring disable times, it implies that the output is already off for 10% of the RC time. Because all disable times are measured with a load of 1 kΩ and 50 pF, subtract the 10% RC time (5 ns) from the values published in the data sheets to obtain the real internal disable propagation delay.

Diodes D1 and D2 are parasitic diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one V_{BE} above V_{CC}, of importance in large systems where sections of the system may be powered-down (V_{CC} = 0 V), in which case the output diode current has to be limited to 20 mA.

All I/O ports and transceivers have a three-state output as shown in Fig.38. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause V_{CC} current. If necessary, terminate the input with a 10 kΩ resistor, see 'Termination of unused inputs'.

Open-drain outputs

In TTL families, several functions are offered with open-collector outputs to enhance logic functions by using OR-tied logic. The advantage of OR-tied logic is the logic elements saved and hence the lower power dissipation. However, this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not encountered in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, the 74HC/HCT03 (quad 2-input NAND gate) has an open-drain n-channel output, see Fig.40. The parasitic diode D1 is not present (there being no p-channel transistor); this allows the output voltage to be pulled above V_{CC} to V_{Omax} making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open-drain output is protected against electrostatic discharge.

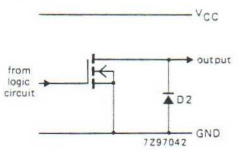


Fig. 40 Open-drain output circuit.

Increased drive capability of gates

To increase output drive, the inputs and outputs of gates in the same package may be connected in parallel. It is advisable to restrict parallel connection to gates within one package to avoid large transient supply currents due to different gate-switching times.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Output capacitance

For push-pull outputs, no output capacitance is specified because either the n-channel transistor or the p-channel transistor creates a low-impedance path to the supply rails.

Three-state outputs can be switched to the high impedance OFF-state, and because many of them can be connected to a bus line, the output capacitance is needed to calculate the total capacitive load. For bus-driven 3-state outputs in a DIL package, the output capacitance is 6 pF (typ.) and 20 pF (max.).

STATIC NOISE IMMUNITY

The static noise immunity can be divided into:

- the static noise margin LOW. This is the voltage difference between V_{ILmax} of the driven device and V_{OLmax} of the driver.
- the static noise margin HIGH. This is the difference between V_{OHmin} of the driver and V_{IHmin} of the driven device.

For 74HC devices, both the LOW level noise margin and the HIGH-level noise margin is 28% of V_{CC}. This is a considerable improvement over LSTTL where the LOW-level noise margin is only 8% of V_{CC} and the HIGH level noise margin is just 14% of V_{CC}. The margins are even greater for HCMOS at higher supply voltages as shown in Fig.41. As 74HCT devices have the same switching levels as LSTTL, their noise margins are also the same.

The superior noise immunity of the 74HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs 42 and 43.

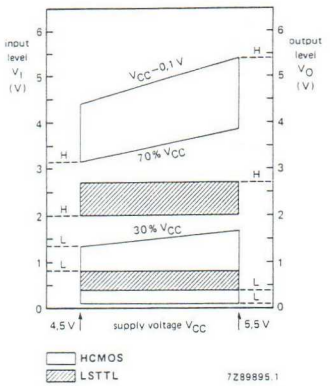


Fig. 41 Worst-case input and output voltages over an operating supply range of 4.5 V to 5.5 V.

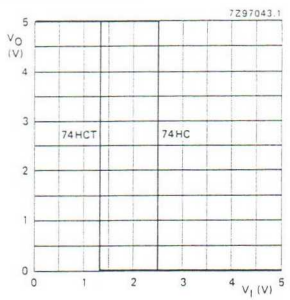


Fig. 42 Typical input-to-output transfer characteristic for 74HC and 74HCT devices.

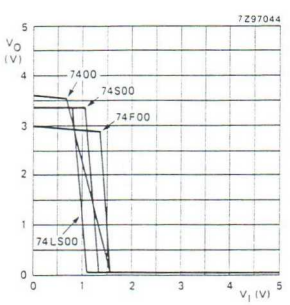


Fig. 43 Input-to-output transfer characteristics for TTL devices.

Table 11 shows the input noise margin of HCMOS devices where like devices are interfaced. Output voltages are also given.

Table 11: Noise immunity and noise margin for HCMOS devices (V_{CC} = 4.5 V)

		74HC	74HCT	74HCU
V_{ILmax}	(V)	1.35	0.8	0.9
V_{IHmin}	(V)	3.15	2	3.6
V_{OLmax}	(V)	0.1	0.1	0.5
V_{OHmin}	(V)	4.4	4.4	4
Noise margin low				
V_{NML}	(V)	1.25	0.7	0.4
Noise margin high				
V_{NMH}	(V)	1.25	2.4	0.4

Table 12 shows the input noise margin of 74HCT devices interfacing with LSTTL devices; the 74HCT or LSTTL output is fully-loaded, V_{CC} = 4.5 V and T_{amb} is 0 °C to +70 °C (the only convenient temperature range when using LSTTL characteristics).

Table 12: Noise immunity and noise margin for 74HCT and LSTTL device interfacing

		74HCT	LSTTL
V_{ILmax}	(V)	0.8	0.8
V_{IHmin}	(V)	2	2
V_{OLmax}	(V)	0.33 (note 1) 0.1 (note 2)	0.4
V_{OHmin}	(V)	3.84 (note 1) 4.4 (note 2)	2.7
Noise margins (V):			
from 74HCT to LS		V_{NML}	0.47
		V_{NMH}	1.84
from LS to 74HCT		V_{NML}	0.4
		V_{NMH}	0.7
from LS to LS		V_{NML}	0.4
		V_{NMH}	0.7
from 74HCT to 74HCT		V_{NML}	0.7
		V_{NMH}	2.4

Notes

1. 4 mA load (i.e. 10 LSTTL inputs).
2. 20 μA load (i.e. 20 74HCT inputs).

Whenever a 74HCT output drives either an LSTTL or a 74HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or 74HCT input. This improvement is larger for V_{NMH} owing to the superior output sourcing current of the rail-to-rail HCMOS output swing compared with the limited totem-pole pull-up output voltage of LSTTL.

DYNAMIC NOISE IMMUNITY

As for static noise immunity, dynamic noise immunity can be divided into two parts:

- a dynamic noise margin LOW
- a dynamic noise margin HIGH.

For 74HC devices, both margins are similar; for 74HCT devices, the dynamic noise margin LOW is the smaller of the two. To plot it, a pulse of known magnitude, V_p, is applied to the input of a device and its width, t_W, is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. The pulse width is measured at half pulse height, $V_p/2$. The rise and fall times, t_r and t_f are 0.6 ns.

V_p is then reduced in increments and t_W for each new value is ascertained.

The test is repeated for different supply voltages — for 74HC devices between 2 V and 6 V, and at 5 V for 74HCT devices. A range of output currents, I_O, are also used. Increasing the DC load reduces the dynamic noise immunity.

Figure 44 shows the amplitude of positive-going pulses that can be withstood in the LOW state for 74HC and 74HCT devices. The curves are worst-case ones with fully-loaded drivers, so a system using only 74HC or 74HCT devices will have 0.23 V more noise margin for all t_W.

For typical input switching thresholds of 1.4 V and 2.25 V for 74HCT (V_{CC} = 5 V) and 74HC (V_{CC} = 4.5 V) respectively, the noise margins will be 0.83 V [(1.4 − 0.8) + 0.23 V] larger for 74HCT and 1.13 V [(2.25 − 1.35) + 0.23 V] larger for 74HC devices.

The main causes of unwanted input pulses are spikes due to outputs switching, which dumps large currents on the GND lines, or reflections when long lines (longer than about 32 cm) are driven. For more information on the latter, see chapter 'Replacing LSTTL and driving transmission lines'.

The best example of an unwanted pulse generator is an octal device with bus outputs of which seven are switching simultaneously and the eighth, most remote, output is LOW. Figure 45(a) shows the maximum pulse voltage measured on the unswitched output of a 74HC/HCT374 as a function of V_{CC}. Figures 45(b) and 45(c) show this maximum volt-

age and the pulse width as functions of the number of outputs that are switching. It should be emphasised that any pulses produced by switching outputs won't cause other devices to respond even in worst-case conditions. This is because Fig.44 is based on a worst-case V_{OL} and the maximum expected pulse height of Fig.45 occurs for a best-case V_{OL}. So, even when a pulse of the maximum expected height shown in Fig.45 occurs, there is still a noise margin. This can be verified by plotting the pulse heights of Fig.45 on the curves of Figs 44(a) and 44(b).

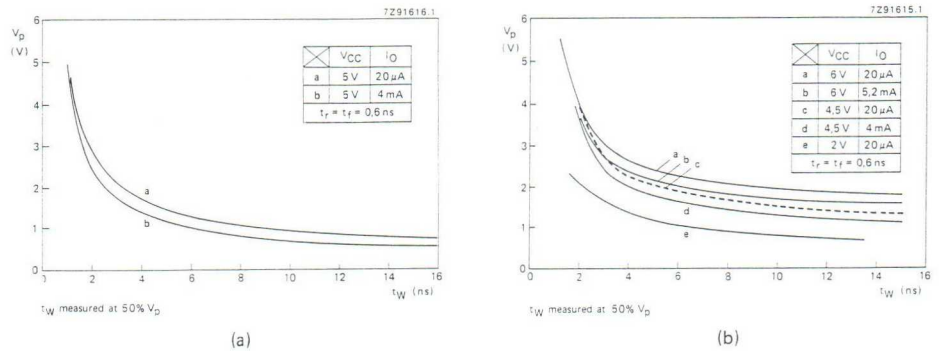


Fig. 44 Amplitude of the positive-going pulses that can be withstood in the LOW state (worst-case, fully-loaded driver) for (a) 74HCT devices and (b) 74HC devices.

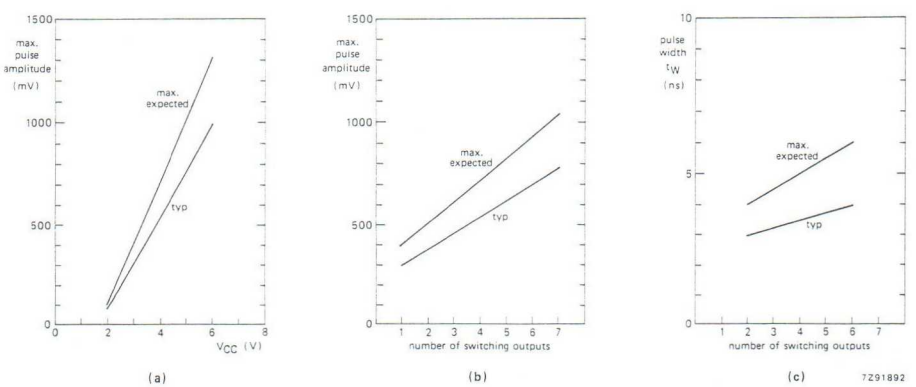


Fig. 45 (a) Amplitude of the voltage pulse (on pin 2, the most remote) due to switching seven of the bus-driver outputs of a 74HC/HCT374 octal flip-flop; C_L = 150 pF, T_{amb} = 25 °C. (b) Amplitude of the voltage pulse (on pin 2) as a function of the number of outputs switched; V_{CC} = 5 V, C_L = 150 pF. (c) Pulse width as a function of the number of outputs switched; V_{CC} = 4.5 to 6 V, C_L = 150 pF. For V_{CC} = 2 V, the maximum expected pulse width is about 10 ns.

BUFFERED DEVICES

Definition

Often the terms 'buffer devices', 'buffered inputs' or 'buffered outputs' are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switching levels and output impedances were not constant, so neither were output rise/fall times or propagation delay times. The Jedec JC40.2 committee define a buffered device to be at least two active stages with the output independent of the input logic voltage level and independent of the number of inputs that are HIGH or LOW.

A buffer meeting this definition is the AND-function circuit of Fig.46. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

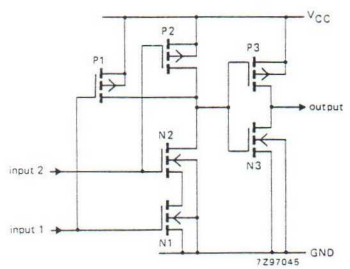


Fig. 46 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

All 74HC and 74HCT devices comprise at least two stages to minimize any pattern sensitivity of propagation delay time. Buffering also improves static noise immunity due to increased voltage gain, giving almost ideal transfer characteristics.

The designation 74HCU is used to denote single-stage devices. These have the same specification as 74HC devices but their input and output voltage parameters are relaxed. 74HCU devices don't have the high gain of 74HC/HCT versions, which makes them more suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

Output buffering

All 74HC and 74HCT devices have buffered outputs for optimum performance. To demonstrate the benefits of output buffering, consider what would happen without it. In the single-stage device shown in Fig.47, the output impedance depends on the DC input voltage. Consequently, the noise margins at the output become a function of the input voltage, even when V_I is a legal HIGH or LOW level.

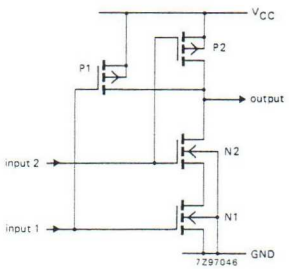


Fig. 47 Unbuffered NAND gate.

The steady-state impedance of the circuit of Fig.47 is also affected by the state of the inputs. Given that P1 and P2 have identical performances (same size), there are two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. Therefore, without output buffering, the state of output conduction depends on the number of inputs that are HIGH or LOW.

Input buffering

An input is considered to be buffered when its switching threshold is unaffected by the logic states of other inputs. In the example of Fig.47 that has unbuffered inputs, the switching threshold of input 1 varies with a HIGH level at input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching threshold of the device. The result can be seen in Fig.48 where curve 1+2 occurs when the two inputs are tied together, and curve 1 or 2 is the switching threshold when the accompanying input is at V_{CC}.

For true input buffering, an input must have an inverter stage with sufficient gain to ensure that logic levels give independent on-chip levels. Some gates in the 74HC series (usually AND or OR gates) have unbuffered inputs, however all devices meet the family logic level requirements. All 74HCT devices have buffered inputs.

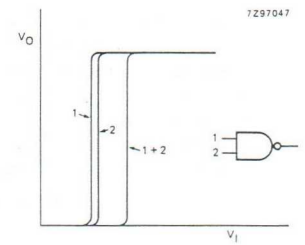


Fig. 48 Example of different switching levels in unbuffered inputs.

PERFORMANCE OF OSCILLATORS

When HCMOS devices are used in RC, crystal or Schmitt trigger oscillators or in analog amplifiers:

- a supply voltage of at least 3 V is required. Below this value, the transconductance of crystal oscillators is too low to start oscillations. In analog circuits, insufficient output current is available to drive external components;
- slow input rise and fall times cause the input stage of a HCMOS device to draw current. This additional quiescent supply current ΔI_{CC} is given in the data sheets for 74HCT devices since these can be used as LSTTL replacements and may be driving a significant load. The total I_{CC} for 74HC devices can be calculated by multiplying the value of I_{CC} read from Fig.14 by the unit load coefficient given in the data sheet for the 74HCT device;
- in general, frequency stability won't be affected by supply voltage, so long as the permissible output currents of the devices are not exceeded.

For further information, see chapters 'Crystal oscillators' and 'Astable multivibrators'.

LATCH-UP FREE

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply overvoltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating (±20 mA), and that V_{CC} should also be not more than twice V_{CCmax} (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC. In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1 μs pulses of 300 mA with a duty factor of 0.001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1 μs pulses of 400 mA with a duty factor of 0.001. However, because there is an internal polysilicon 100 Ω resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ($V_I = V_{CC} + 0.7\ V + 100 I_I$) that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires breakdown. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

For further information, see chapter 'Standardizing latch-up immunity tests' in the Designers Guide, High-speed CMOS.

DROP-IN REPLACEMENTS FOR LSTTL

74HCT devices are power-saving, drop-in replacements for LSTTL devices. Because most systems are operated at frequencies far below the maximum possible, 74HCT devices can also be used to good effect in systems using ALS, AS, S, and FAST devices.

Fan-out should be considered when replacing a TTL device by a 74HCT device. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). Table 13 shows the fan-out of 74HCT to the different TTL families.

The fan-outs given in Table 13 are derived at a voltage drop of max. 0.4 V (V_{OL}). In the "74" TTL series, an extended V_{OL} figure is often seen, e.g. 8 mA at 0.5 V voltage drop for LSTTL. If this figure is used to determine the fan-out of the TTL device it can result in a higher fan-out than is possible with 74HCT. This can be resolved by replacing as many of the driven TTL parts as possible by 74HCT devices to reduce the sink current requirement (the 74HCT input current is negligible). In addition, power dissipation is reduced significantly by using 74HCT.

Table 13: Fan-out of 74HCT to TTL circuits

74HCT	TTL	LS	ALS	FAST	S & AS
standard output	2	10	20	6	2
bus-driver output	3	15	30	10	3

BUS SYSTEMS

CMOS is being used to an increasing extent in microprocessor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

For optimum results, use only 74HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig.49(b)) which, unlike the conventional TTL bus termination, draws no heavy DC current and is more suited to HCMOS outputs.

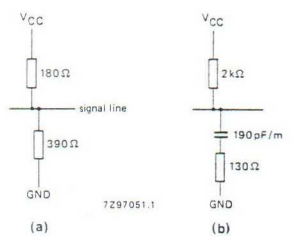


Fig. 49 Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a 10 kΩ series resistor in the HCMOS logic line. This will limit current to ±20 mA for external voltages of up to ±200 V, however, for correct functioning, the DC input current should be kept below those values stated in 'Input/output protection'. The recommended board edge input protection is shown in Fig.50.

In the circuit of Fig.50, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. 74HC4049 or 74HC4050).

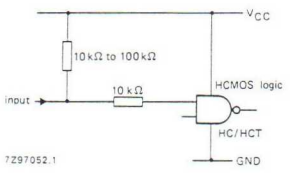


Fig. 50 Example of the board edge input protection circuit.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Since HCMOS bus-drivers do not have built-in hysteresis, slowly-rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series 74HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers 74HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section 'Propagation delays and transition times' of this User Guide.

PACKAGE PIN CAPACITANCE

In purely digital circuits, the input capacitance or three-state output capacitance is sufficient to determine the dynamic characteristics. However, when a HCMOS device is used in the linear region, it is necessary to take pin capacitance into account, e.g. to prevent crosstalk in analog switches or peaks in the frequency response of PLLs.

The use of SO packages with their low pin capacitances is recommended for HCMOS analog designs. Table 14 gives the pin-to-pin capacitances for the plastic DIL and SO packages used for HCMOS. Measurements were made using a dummy package with all unused pins connected to ground.

Table 14: Typical pin capacitances (pF) of SO and DIL packages

	SO-14 & SO-16	DIL-16	SO-20	DIL-20	SO-24	DIL-24
capacitance to ground of:						
corner pins	0.41	0.97				
all other pins	0.21	0.37				
any end two pins			0.65	1.12		
all other pins			0.25	0.40		
any end three pins					0.65	1.64
all other pins					0.33	0.65
capacitance between adjacent pins:						
including a corner pin	0.15	0.40				
all other pins	0.04	0.13				
any end three pins			0.28	0.49		
all other pins			0.14	0.22		
any end three pins					0.30	0.70
all other pins					0.12	0.28

POWER-ON RESET

The power-on reset (POR) circuit used to automatically set HCMOS ICs in a defined reset state after power-up is shown in Fig.51.

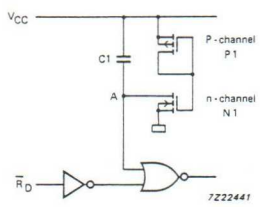


Fig. 51 Power-on reset circuit.

When the IC is powered-up, node A follows the rise of V_{CC} through C1 and the circuit is reset. When the gate voltage of transistor N1 exceeds its threshold level (typically 0.7 V) because it is biased with V_{CC} via transistor P1, capacitor C1 discharges and pulls node A below the switching level of the NOR gate. The IC cannot be used during the POR release time which is the discharge time of C1 (typically 3 μs at V_{CC} = 4.5 V and 35 μs at V_{CC} = 2 V). The sensitivity of the POR circuit to supply voltage reduction is indicated in Table 15. The typical values of parameters t_W and V_L used in Table 15 are illustrated in Fig.52.

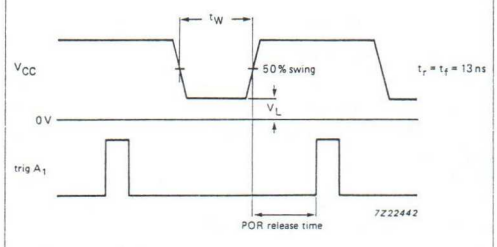


Fig. 52 V_L as a function of the duration of a LOW pulse on the supply voltage.

Table 15: Sensitivity of HCMOS POR circuitry to V_{CC} reduction

	V_{CC} (V)		
t_W (μs)	2	4.5	6
	V_{Lmax} (V)	V_{Lmax} (V)	V_{Lmax} (V)
8	0.8	2.2	2.8
6	0.75	2.2	2.8
4	0.7	2.2	2.8
2	0.6	2.1	2.8
1	0.5	2.0	2.8
0.5	0.4	1.9	2.8
0.1	0.4	1.9	2.8
0.05	0.4	–	–
0.02	0.3	–	–
0.015	0.15	1.7	2.5

The time taken for a transition to propagate from $\overline{R}$ to Q is about the time taken for the reset action to take effect. Also of course, node A in Fig.51 must rise to a level above the switching level of the NOR gate. Because of this, the Q output of the IC may initially follow the V_{CC} ramp as indicated in Fig.53. If the V_{CC} ramp is fast (typically less than 100 ns), the amplitude of the Q output pulse can exceed $V_{CC}/2$ and have a duration of about 10 ns.

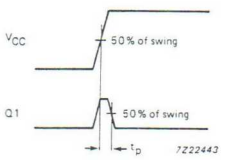


Fig. 53 Initial output pulse during power-up.

Normally, the Q output pulse is negligible because the V_{CC} ramp is slow (typically more than 0.5 μs) due to the charging time of large-value smoothing and decoupling capacitors. With a slow V_{CC} ramp, the amplitude of the Q output pulse remains well below the switching level of the succeeding stage. In any event, it is most unlikely that a system will be triggered by the Q output pulse because it only occurs during power-up.

QUALITY INFORMATION

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

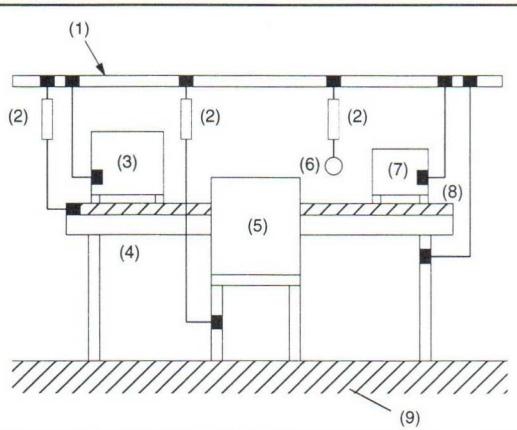
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time.
Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, endure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way a unmounted MOS devices. they should also carry waning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair
(6) Wrist strap.
(7) Electrical equipment.
(8), (9) Conductive surface/antistatic sheet.

Figure 1. Protected work station

NEW RELEASES

Programmable ripple counter with oscillator; (3-State)

74HC/HCT9323A

FEATURES

- 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 85MHz (V_{CC} = 5V ± 10%)
- 3-State output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3V to 6V
- Oscillator stop function ($\overline{MR}$)
- Output capability: bus driver → (15 LSTTL)
- I_{CC} category: MSI

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation

DESCRIPTION

The 74HC/HCT9323A are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT 9323A are oscillators designed for quartz crystal combined with a programmable 3-State counter, a 3-State output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator and sets the output buffer in the 3-State condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive. In the HCT version, the $\overline{MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C, $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			HC	HCT	
t_{PLH} t_{PHL}	Propagation delay X1 to OUT (S1 = S2 = LOW)	C_L = 50pF; V_{CC} = 5V	8	8	ns
f_{max}	Maximum clock frequency		150	150	MHz
C_I	Input capacitance except X1 and X2		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package				pF

NOTES:

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + (C_L + V_{CC}^2 \times f_O) + (I_{pull\text{-}up} \times V_{CC})$

where:

f_I = inputfrequency in MHz..
f_O = output frequency in MHz.
V_{CC} = Supply voltage in V.
C_L = Output load capacitance in pF.
$I_{pull\text{-}up}$ = Pull-up currents in µA.

For HC and HCT an external clock is applied to X1 with:

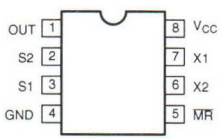
$t_r = t_f \leq$ 6ns, V_I is GND to V_{CC}, $\overline{MR}$ = HIGH.

$I_{pull\text{-}up}$ is the summation of $-I_I$ (µA) of S1 and S2 inputs at the LOW state.

ORDERING INFORMATION

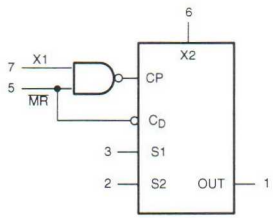
PACKAGES	TEMPERATURE RANGE	ORDER NUMBER	DWG NUMBER
8-Pin Plastic SO	0°C to +70°C	74HC/HCT9323A D	SOT96-1

PIN CONFIGURATION



SK00013

IEC LOGIC SYMBOL



SK00014

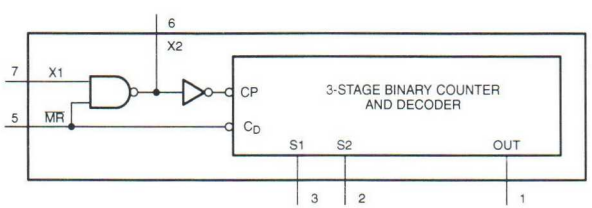
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OUT	Counter output
3, 2	S1-S2	Mode select inputs for divide by 1, 2, 4 or 8
4	GND	Ground (0V)
5	$\overline{MR}$	Master reset (active LOW)
6	X2	Oscillator pin
7	X1	Clock input/oscillator pin
8	V_{CC}	Positive supply voltage

FUNCTION TABLE

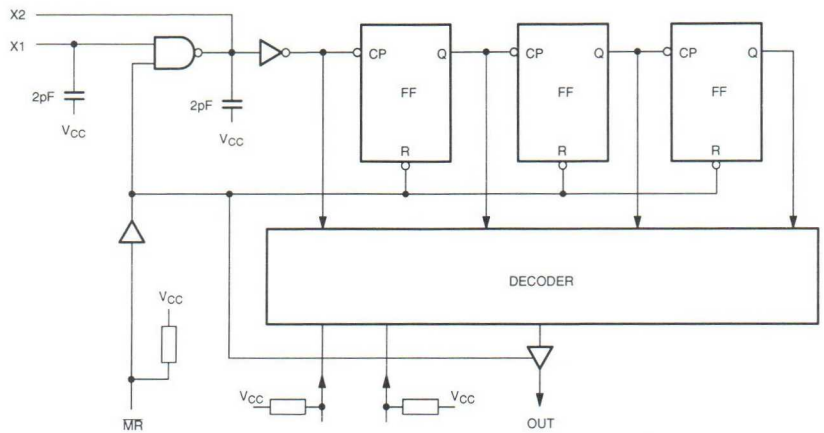
INPUTS		OUTPUTS
S1	S2	OUT
0	0	f_I
0	1	$f_I/2$
1	0	$f_I/4$
1	1	$f_I/8$

FUNCTIONAL DIAGRAM



SK00015

LOGIC DIAGRAM



Internal capacitors typical 2pF each, including stray capacitors on pins X1 and X2, total capacitance will be typical 7pF per pin

SK00016

Parallel printer interface transceiver/buffer — 74HCT1284

FEATURES

- Asynchronous operation
- 4-Bit transceivers
- 3 additional buffer/driver lines
- TTL compatible inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Input Hysteresis
- Low Noise Operation
- Center Pin V_{CC} & GND
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B side

DESCRIPTION

The 74HCT1284 parallel interface chip is designed to provide an asynchronous, 4-bit, bi-directional, parallel printer interface for personal computers. Three additional lines are included to provide handshaking signals between the host and the peripheral. The part is designed to match IEEE 1284 standard.

The 4 transceiver pins (A/B 1-4) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y5-Y7 lines have totem pole or open drain style outputs depending on the state of the high drive enable pin HD. The A bus only has totem pole style outputs. All inputs are TTL compatible with at least 400mV of input hysteresis at V_{CC} = 5.0V.

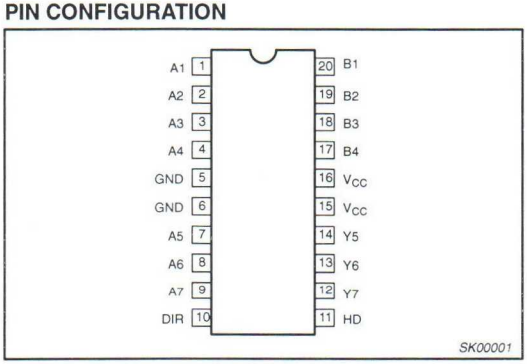
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Bn to An	C_L = 50pF; V_{CC} = 5V	5.3 5.6	ns ns
C_{IN}	Input capacitance A_n, DIR, HD	V_I = 0V or V_{CC}	5	pF
C_{OUT}	Output capacitance B_n, Y_n	V_O = 0V or V_{CC}; 3-State	14	pF
I_{CC}	Total supply current	V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	0°C to +70°C	74HCT1284N	SOT146-1
20-pin plastic SOL	0°C to +70°C	7HCT1284D	SOT163-1
20-pin plastic SSOP Type II	0°C to +70°C	74HCT1284DB	SOT339-1
20-pin plastic TSSOP Type I	0°C to +70°C	74HCT1284PW	SOT360-1

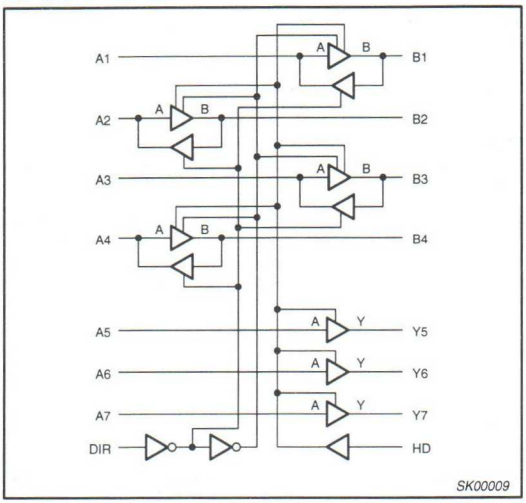
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2,3,4 20,19,18,17	A1 - A4 B1 - B4	Data inputs/outputs
7,8,9 14,13,12	A5 - A7 Y5 - Y7	Buffer/Driver lines
10,11	DIR,HIGH DRIVE	Direction, Drive
5,6	GND	Ground (0V)
15,16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	INPUTS/OUTPUTS	
DIR	HD	A5-7	Y5-7	A1-4	B1-4
L	L	L	L	A = B	Inputs
L	L	H	Z	A = B	Inputs
L	H	L	L	A = B	Inputs
L	H	H	H	A = B	Inputs
H	L	L	L	Inputs Low	Outputs Low
H	L	H	Z	Inputs High	Outputs Z
H	H	L	L	Inputs	B = A
H	H	H	H	Inputs	B = A

H = High Voltage
L = Low Voltage
Z = High Impedance, Off-State

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	±20	mA
V_I	DC input voltage[3]		–2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	±50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	±50	mA
T_{stg}	Storage temperature range		–65 to 150	°C
I_{CC}/I_{GND}	Continuous current through V_{CC} or GND		±200	mA

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.7	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–14	mA
I_{OL}	Low-level output current		14	mA
T_{amb}	Operating free-air temperature range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = 25°C			T_{amb} = 0°C to +70°C		
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	High-level output voltage	A_n	V_{CC} = Min to Max; I_{OH} = –50μA	V_{CC}–0.2	V_{CC}		V_{CC}–0.2		V
			V_{CC} = 4.7V; I_{OH} = –4mA	4.3	4.6		3.7		V
		B_n or Y_n	V_{CC} = 4.7V; I_{OH} = –14mA	2.6	2.9		2.4		V
V_{OL}	Low-level output voltage	A_n	V_{CC} = Min to Max; I_{OL} = 50μA; V_I = V_{IL} or V_{IH}		0	0.2		0.2	V
			V_{CC} = 4.7V; I_{OL} = 4mA; V_I = V_{IL} or V_{IH}		0.1	0.25		0.4	V
		B_n or Y_n	V_{CC} = 4.7V; I_{OL} = 14mA; V_I = V_{IL} or V_{IH}		0.15	0.3		0.4	V
V_{HYS}	Input Hysteresis		V_{CC} = 5.0V	0.4	0.50		0.4		V
R_D	B/Y side Output Impedance		See Figure 1	8	15	22	8	22	Ω
I_I	Input leakage current (A5–A7)		V_{CC} = 5.5V; V_O = V_{CC} or GND		±0.5	±1.0		±5.0	μA
I_{OFF}	B/Y Side Power-off leakage current		V_{CC} = 0.0V; V_O = 0 to 7V		±1	±10		±100	μA
I_{OZH}	3-State output High current Y_n		V_{CC} = 5.5V; V_O = V_{CC}; V_I = V_{IL} or V_{IH}		1	5		20	μA
I_{OZL}	3-State output Low current Y_n		V_{CC} = 5.5V; V_O = GND; V_I = V_{IL} or V_{IH}		–1	–5		–20	μA
$I_{IH}+I_{OZH}$	current (A_1 – A_4, B_n)		V_{CC} = 5.5V; $V_{I/O}$ = V_{CC}		1	5		25	μA
$I_{IL}+I_{OZL}$	current (A_1 – A_4, B_n)		V_{CC} = 5.5V; $V_{I/O}$ = GND		–1	–5		–25	μA
I_{CC}	Quiescent Supply Current		V_{CC} = 5.5V; I_O = 0; V_I = GND or V_{CC}		0.5	250		400	μA

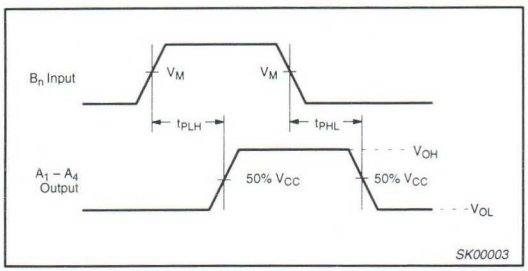
AC CHARACTERISTICS

GND = 0V, t_R = t_F = 3.0ns, C_L = 50pF, R_L = 500Ω

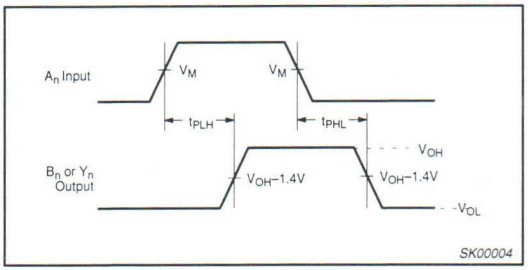
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = 25°C V_{CC} = 5.0V			T_{amb} = 0 to + 70°C V_{CC} = Min to Max		
			MIN	TYP	MAX	MIN	MAX	
SR	B-Side Slew Rate		0.05	0.11	0.4	0.05	0.4	V/ns
t_{PLH} t_{PHL}	Propagation delay A toY or A to B	2	5.0 5.0	13.9 21.0	17.1 25.7	5.0 5.0	22 31	ns
t_{PLH} t_{PHL}	Propagation delay B to A	1	1.5 1.5	5.3 5.6	7.5 7.9	1.5 1.5	9.0 10.0	ns
t_{PZH} t_{PHZ}	Output enable/disable time to/from High level HD to Y or HD to B	3	4.0 2.0	12.0 6.5	16.0 9.1	4.0 2.0	20.0 11.0	ns
t_{PZL} t_{PLZ}	Output enable/disable time to/from Low level A to Y or A to B	4	5.0 1.5	12.7 5.0	16.3 7.1	5.0 1.5	20.0 9.0	ns

AC WAVEFORMS

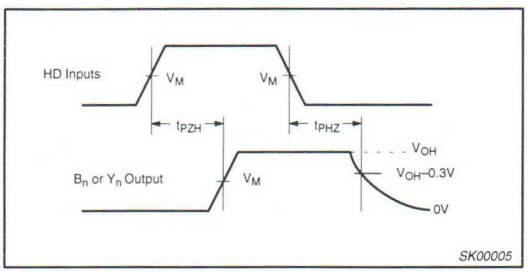
For all waveforms, $V_M = 1.5V$.



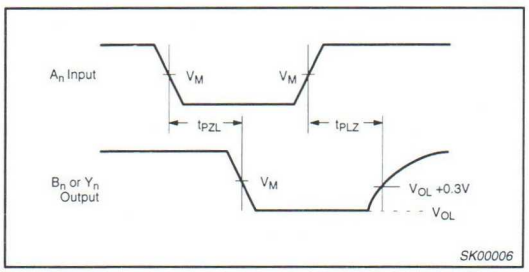
Waveform 1. Propagation Delay for Bn to A1–A4



Waveform 2. Propagation Delay for An to Bn or Yn Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output enable Time to Low Level and Output disable Time from Low Level

TEST CIRCUITS AND WAVEFORM

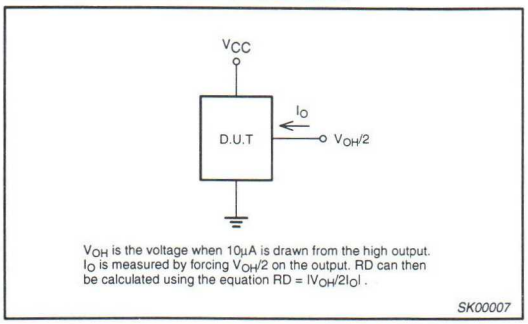
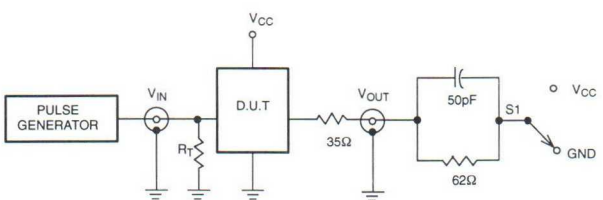


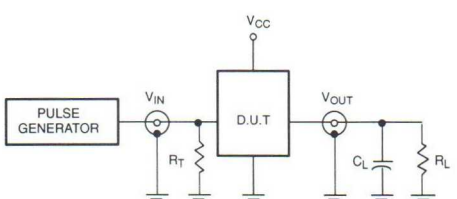
Figure 1. Output Impedance RD



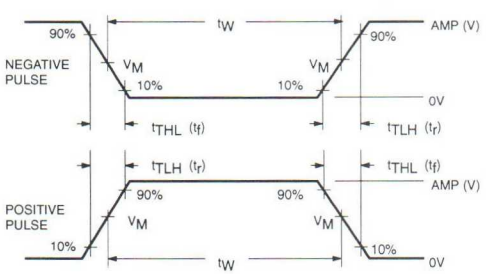
Test Circuit for B_n or Y_n Outputs

SWITCH POSITION
B_n or Y_n Outputs

TEST	SWITCH
t_{PLH}	GND
t_{PHL}	V_{CC}
t_{PZH}	GND
t_{PHZ}	GND
t_{PZL}	V_{CC}
t_{PLZ}	V_{CC}



Test Circuit for A_n Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_r	t_f
74HCT	3.0V	1MHz	500ns	3ns	3ns

SK00008

HCMOS FAMILY CHARACTERISTICS

	page
Family specifications	91
Data sheet specification guide	101
Definitions of symbols	103

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", the specified maximum operating supply voltage is 10 V.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	°C	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: – standard outputs – bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT/HCU
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", the specified maximum operating supply voltage is 11 V.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current SSI flip-flops MSI LSI			 2.0 4.0 8.0 50.0		 20.0 40.0 80.0 500		 40.0 80.0 160.0 1000	 μA μA μA μA	 6.0 6.0 6.0 6.0	V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$ $I_O = 0$

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current SSI flip-flops MSI LSI			 2.0 4.0 8.0 50.0		 20.0 40.0 80.0 500		 40.0 80.0 160.0 1000	 μA μA μA μA	 5.5 5.5 5.5 5.5	V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$ $I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case ($V_I = 2.4$ V; $V_{CC} = 5.5$ V) specification is: $\Delta I_{CC} = 0.65$ mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 3 and 4
t_{THL}/ t_{TLH}	output transition time bus driver outputs		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 3 and 4

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4.5	Figs 8 and 9
t_{THL}/ t_{TLH}	output transition time bus driver outputs		5	12		15		18	ns	4.5	Figs 8 and 9

HCU TYPES

AC WAVEFORMS 74HCU

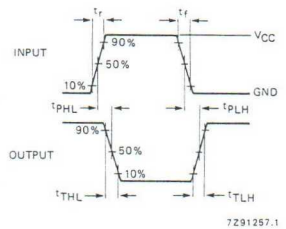


Fig. 1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

TEST CIRCUIT FOR 74HCU

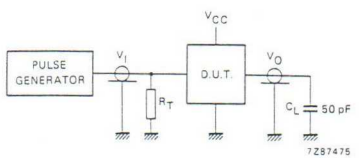


Fig. 2 Test circuit.

Definitions for Fig. 2:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HC TYPES

AC WAVEFORMS 74HC

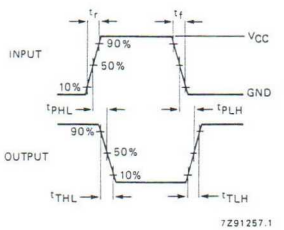


Fig. 3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HC

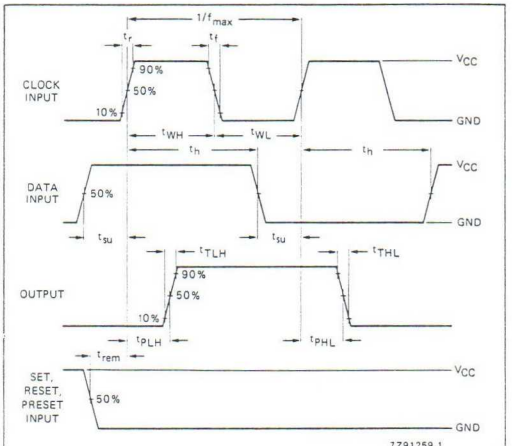


Fig. 4 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 4

1. In Fig. 4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

HC TYPES (continued)

TEST CIRCUIT FOR 74HC

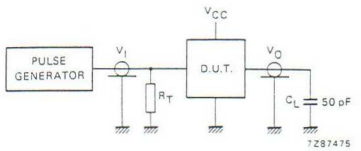


Fig. 5 Test circuit.

Definitions for Fig. 5:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

AC WAVEFORMS 74HC (continued)

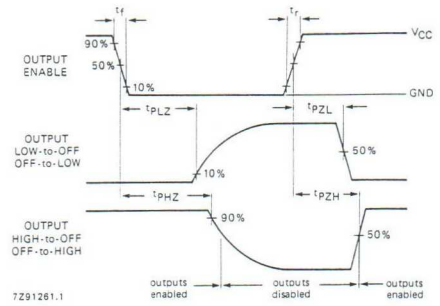
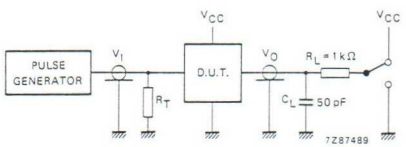


Fig. 6 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HC



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 7 Test circuit for 3-state outputs.

Definitions for Fig. 7:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES

AC WAVEFORMS 74HCT

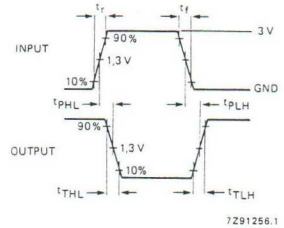


Fig. 8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HCT

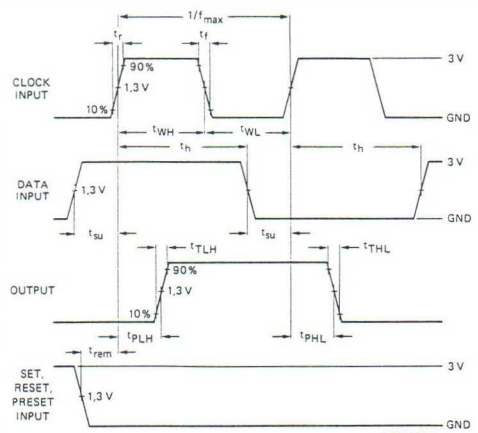


Fig. 9 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 9

1. In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

TEST CIRCUIT FOR 74HCT

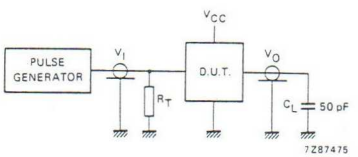


Fig. 10 Test circuit.

Definitions for Fig. 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES (continued)

AC WAVEFORMS 74HCT (continued)

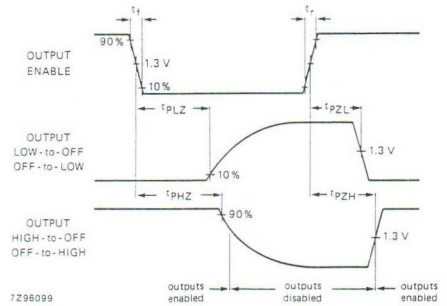
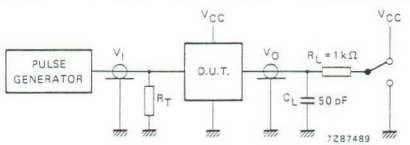


Fig. 11 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HCT



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

INTRODUCTION

The 74HCMOS data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for the longest data path through the device with a 15 pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_r and t_f.

LOGIC SYMBOLS

Two logic symbols are given for each device – the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEC Logic Symbol as developed by the IEC (International Electrotechnical Commission).

The IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) which supersedes Publication 117-15, published in 1972.

RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System – IEC134) lists the maximum limits to which the device can be subjected without damage. This doesn't imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won't have been shortened.

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table lists the operating ambient temperature and the conditions under which the limits in the "DC CHARACTERISTICS" and "AC CHARACTERISTICS" tables will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

The "DC CHARACTERISTICS" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} can be tested by the user. If V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC CHARACTERISTICS" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 metre. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any HCMOS device type; instead, use input voltages of V_{CC} (for the HIGH state) and 0 V (for the LOW state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILmax} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic LOW. However, typically a **higher** V_{IL} will also be recognized as a logic LOW. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

For 74HCMOS, unlike TTL, no output HIGH short-circuit current is specified. The use of this current, for example, to calculate propagation delays with capacitive loads, is covered by the HCMOS graphs showing the output drive capability and those showing the dependence of propagation delay on load capacitance.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors. It is measured with the inputs at V_{CC} or GND and is typically a few nA.

AC CHARACTERISTICS

The "AC CHARACTERISTICS" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveforms section.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground-plane) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for 74HC and 0 V to 3 V for 74HCT; a 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time and removal time. f_{max} is also tested with 6 ns input rise and fall times, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.

I_S Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.

V_{IH} HIGH level input voltage ; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.

V_{OH} HIGH level output voltage ; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON} ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.

ΔR_{ON} ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

C_S Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

t_h Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_r, t_f Clock input rise and fall times; 10% and 90% values.

AC switching parameters (continued)

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V points for the 74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V point for the 74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC and 74HCU devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).

t_{PLZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).

t_{PZH} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).

t_{PZL} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).

t_{rem} Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74HC devices and the 1.3 V points for the 74HCT devices on both input voltage waveforms.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the coltrol input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74HC and 74HCU devices and at the 1.3 V points for 74HCT devices.

DEVICE DATA

QUAD 2-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT00 provide the 2-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

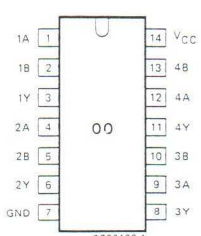


Fig. 1 Pin configuration.

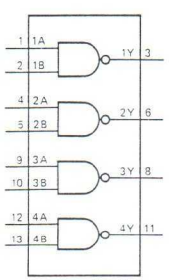


Fig. 2 Logic symbol.

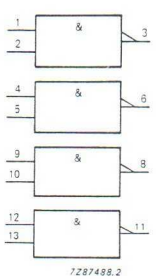


Fig. 3 IEC logic symbol.

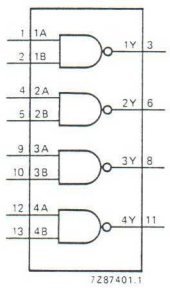


Fig. 4 Functional diagram.

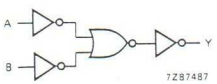


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications"

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		12	19		24		29	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

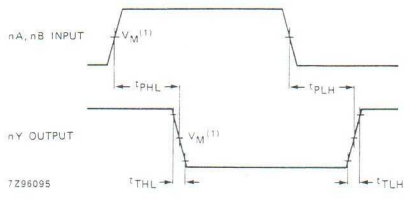


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT NOR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT02 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT02 provide the 2-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 5 V	7	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

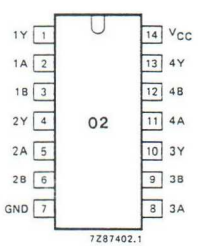


Fig. 1 Pin configuration.

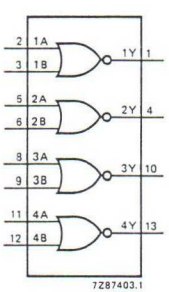


Fig. 2 Logic symbol.

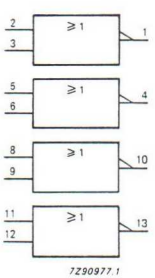


Fig. 3 IEC logic symbol.

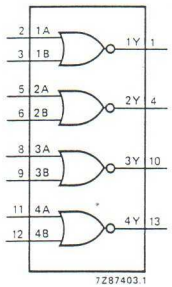


Fig. 4 Functional diagram.

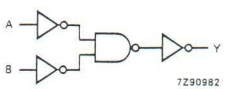


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		11	19		24		29	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

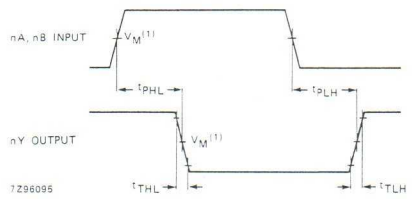


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT NAND GATE

FEATURES

- Level shift capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PLZ}	propagation delay	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to detemine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) +$$

$$+ \Sigma (V_O^2/R_L) \times \text{duty factor LOW, where:}$$

f_i = input frequency in MHz
f_o = output frequency in MHz
V_O = output voltage in V
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
$\Sigma (V_O^2/R_L)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
R_L = pull-up resistor in MΩ

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V
3. The given value of C_{PD} is obtained with:
   C_L = 0 pF and R_L = ∞

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

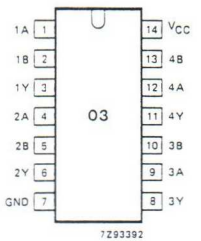


Fig. 1 Pin configuration.

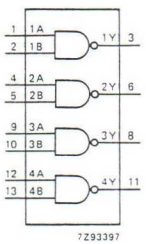


Fig. 2 Logic symbol.

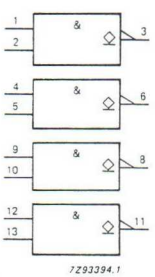


Fig. 3 IEC logic symbol.

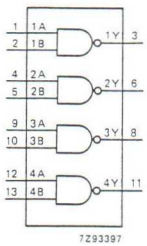


Fig. 4 Functional diagram.

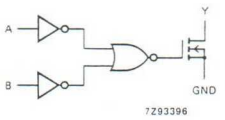


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_O	DC output voltage	−0.5	+7	V	
I_{IK}	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$-I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V
$-I_O$	DC output sink current		25	mA	for -0.5 V $< V_O$
$\pm I_{CC}$; $\pm I_{GND}$	DC VCC or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range; −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are refereced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	$V_O = V_{O(max)}$* or GND

* The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are refereced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	4.5 to 5.5	V_{IL}	$V_O = V_{O(max)}$* or GND

* The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB, to nY		12	24		30		36	ns	4.5	Fig. 6
t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

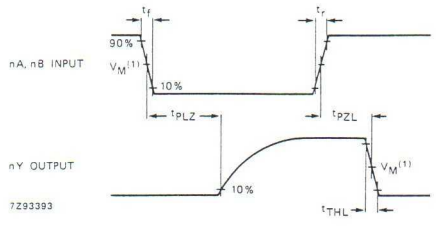


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

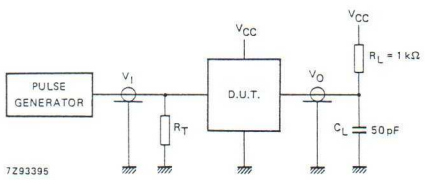


Fig. 7 Test circuit (open drain)

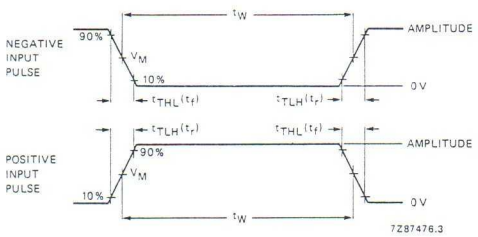


Fig. 8 Input pulse definitions.

Definitions for Figs. 7 and 8:

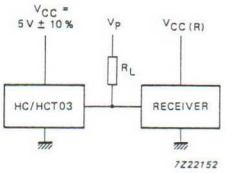
C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

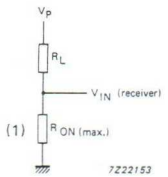
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

APPLICATION INFORMATION





(1) $R_{ON(max)} = \frac{0.26\ V}{4\ mA} = 65\ \Omega$ (at 25 °C)

(a) (b)

Fig. 9 Pull-up configuration.

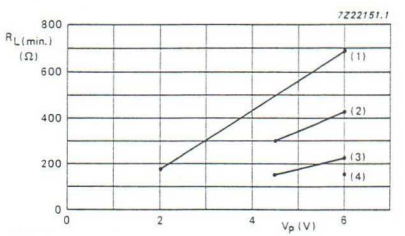


Fig. 10 Minimum resistive load as a function of the pull-up voltage.

Notes to Figs 9 and 10

If $V_P - V_{CC}$ (R) > 0.5 V a positive current will flow into the receiver (as described in the USER GUIDE; input/output protection), this will not affect the receiver provided the current does not exceeds 20 mA. At $V_{CC} < 4.5$ V, $R_{ON(max)}$ is not guaranteed; $R_{ON(max)}$ can be estimated using Figs 33 and 34 in the USER GUIDE.

Notes to Fig. 10

1. V_{CC} (R) = 2.0 V; V_{IL} = 0.5 V.
2. V_{CC} (R) = 5.0 V; V_{IL} = 0.8 V.
3. V_{CC} (R) = 4.5 V; V_{IL} = 1.35 V.
4. V_{CC} (R) = 6.0 V; V_{IL} = 1.8 V.

Note to Application information

All values given are typical unless otherwise specified.

HEX INVERTER

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT04 provide six inverting buffers.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

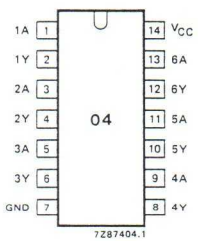


Fig. 1 Pin configuration.

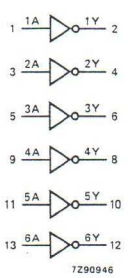


Fig. 2 Logic symbol.

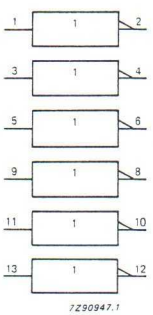


Fig. 3 IEC logic symbol.

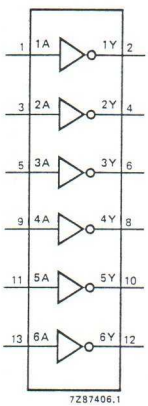


Fig. 4 Functional diagram.

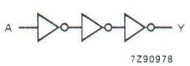


Fig. 5 Logic diagram (one inverter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	1.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY		10	19		24		29	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

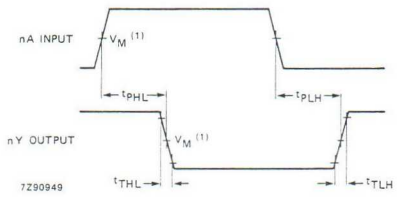


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX INVERTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HCU04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per inverter	note 1	10	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

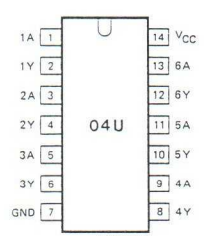


Fig. 1 Pin configuration.

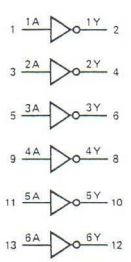


Fig. 2 Logic symbol.

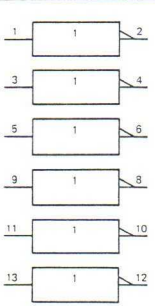


Fig. 3 IEC logic symbol.

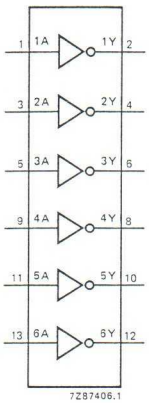


Fig. 4 Functional diagram.

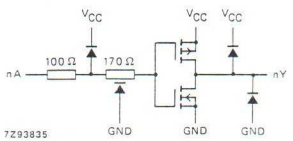


Fig. 5 Schematic diagram (one inverter).

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU								V_{CC} V	V_I	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU									
		+25			-40 to +85		-40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		19 7 6	70 14 12		90 18 15		105 21 18	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

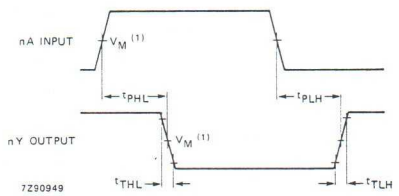


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

TYPICAL TRANSFER CHARACTERISTICS

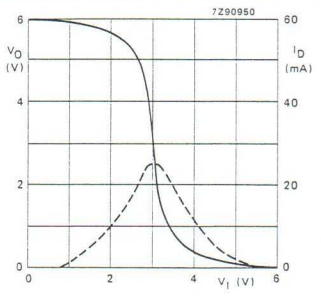


Fig. 7

—— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 6.0 V.

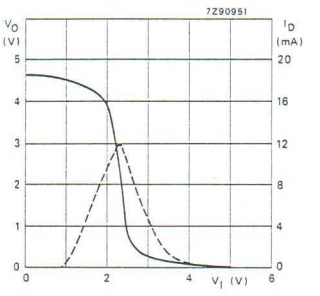


Fig. 8

—— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 4.5 V.

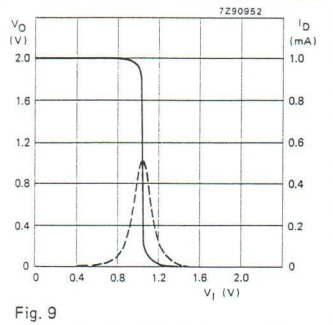


Fig. 9

—— V_O; – – – – I_D (drain current)
I_O = 0; V_{CC} = 2.0 V.

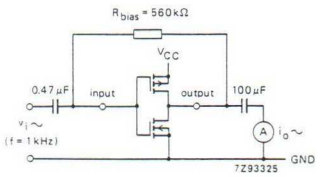


Fig. 10 Test set-up for measuring forward transconductance $g_{fs} = di_O/dv_i$ at v_O is constant (see also graph Fig. 11).

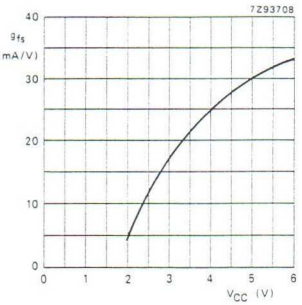


Fig. 11 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

APPLICATION INFORMATION

Some applications for the "HCU04" are:

- Linear amplifier (see Fig. 12)
- In crystal oscillator designs (see Fig. 13)
- Astable multivibrator (see Fig. 14)

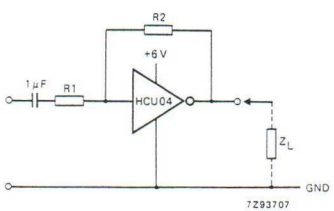


Fig. 12 HCU04 used as a linear amplifier.

Note to Fig. 12

$Z_L > 10$ kΩ; $A_{OL} = 20$ (typ.)

$$A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})};$$

$V_{O\ max\ (p\text{-}p)} \approx V_{CC} - 2$ V centered at ½ V_{CC}

3 kΩ ≤ R1, R2 ≤ 1 MΩ
Typical unity gain bandwidth product is 5 MHz.
C_I (see Fig. 15)
A_{OL} = open loop amplification
A_u = voltage amplification

APPLICATION INFORMATION (Cont'd)

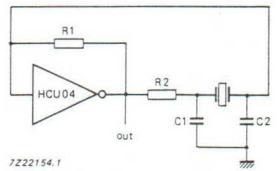


Fig. 13 Crystal oscillator configuration.

Note to Fig. 13

C_1 = 47 pF (typ.)
C_2 = 33 pF (typ.)
R_1 = 1 to 10 MΩ (typ.)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 5 mA at V_{CC} = 5 V and f = 10 MHz).

OPTIMUM VALUE FOR R_2

FREQUENCY (MHz)	R_2 (kΩ)	OPTIMUM FOR
3	2 8	minimum required I_{CC} minimum influence due to change in V_{CC}
6	1 4.7	minimum I_{CC} minimum influence by V_{CC}
10	0.5 2	minimum I_{CC} minimum influence by V_{CC}
14	0.5 1	minimum I_{CC} minimum influence by V_{CC}
> 14	replace R_2 by C_3 with a typical value of 35 pF	

EXTERNAL COMPONENTS FOR RESONATOR (f < 1 MHz)

FREQUENCY (kHz)	R_1 (MΩ)	R_2 (kΩ)	C_1 (pF)	C_2 (pF)
10 to 15.9	22	220	56	20
16 to 24.9	22	220	56	10
25 to 54.9	22	100	56	10
55 to 129.9	22	100	47	5
130 to 199.9	22	47	47	5
200 to 349.9	10	47	47	5
350 to 600	10	47	47	5

Where:

All values given are typical and must be used as an initial set-up.

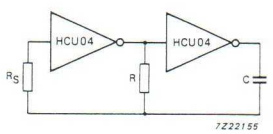


Fig. 14 HCU04 used as an astable multivibrator

Note to Fig. 14

$f = \frac{1}{T} \approx \frac{1}{2.2\ RC}$.

$R_S \approx 2 \times R$.

The average I_{CC} (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V_{CC} = 5.0 V (for more information refer to DESIGNERS GUIDE).

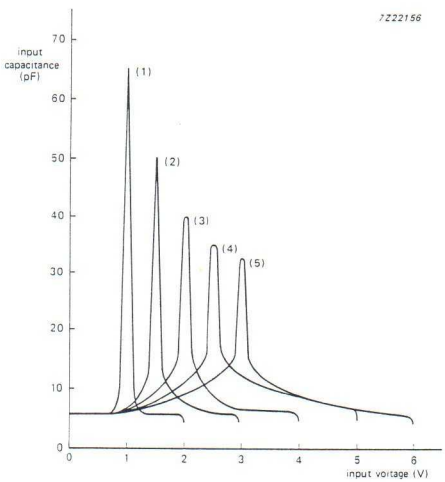


Fig. 15 Typical input capacitance as a function of input voltage.

Note to Fig. 15

1. V_{CC} = 2.0 V.
2. V_{CC} = 3.0 V.
3. V_{CC} = 4.0 V.
4. V_{CC} = 5.0 V.
5. V_{CC} = 6.0 V.

Note to Application information

All values given are typical unless otherwise specified.

QUAD 2-INPUT AND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT08 provide the 2-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

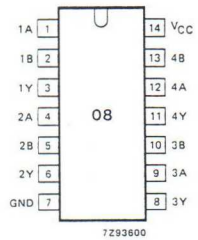


Fig. 1 Pin configuration.

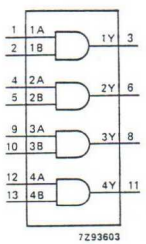


Fig. 2 Logic symbol.

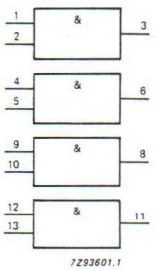


Fig. 3 IEC logic symbol.

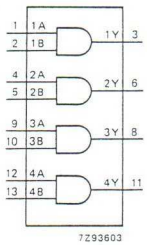


Fig. 4 Functional diagram.

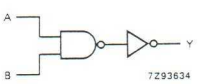


Fig. 5 HC logic diagram (one gate).

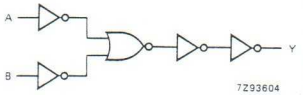


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

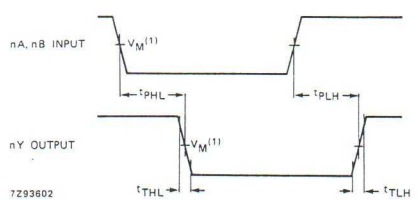


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRIPLE 3-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT10 provide the 3-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	12	14	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

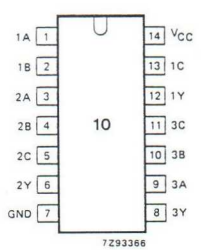


Fig. 1 Pin configuration.

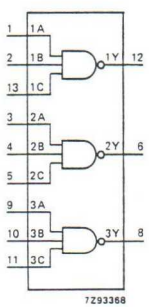


Fig. 2 Logic symbol.

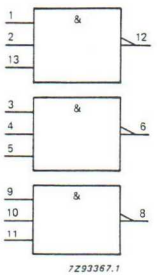


Fig. 3 IEC logic symbol.

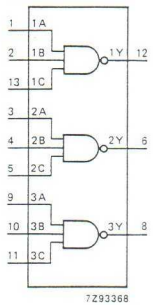


Fig. 4 Functional diagram.

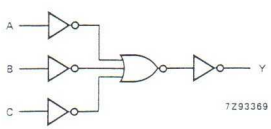


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY		14	24		30		36	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

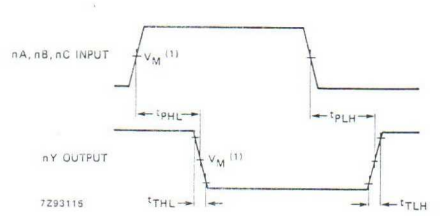


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRIPLE 3-INPUT AND GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT11 provide the 3-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	10	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data inputs
14	V_{CC}	positive supply voltage

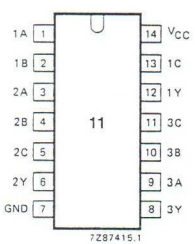


Fig. 1 Pin configuration.

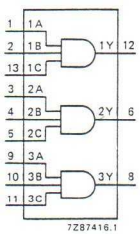


Fig. 2 Logic symbol.

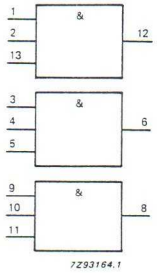


Fig. 3 IEC logic symbol.

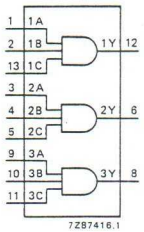


Fig. 4 Functional diagram.

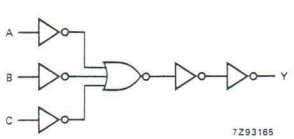


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications"

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		32 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition times		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY		16	24		30		36	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition times		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

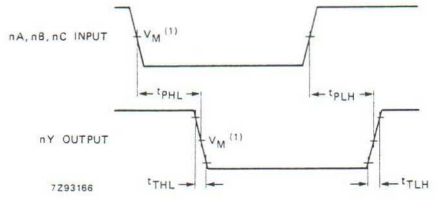


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX INVERTING SCHMITT TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	12	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	7	8	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

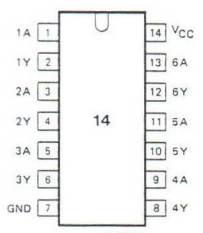


Fig. 1 Pin configuration.

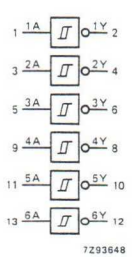


Fig. 2 Logic symbol.

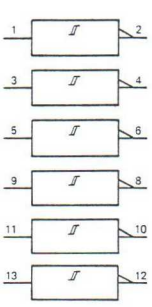


Fig. 3 IEC logic symbol.

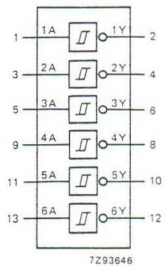


Fig. 4 Functional diagram.

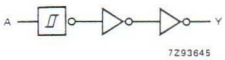


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.7 1.7 2.1	1.18 2.38 3.14	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.3 0.9 1.2	0.52 1.40 1.89	0.90 2.00 2.60	0.3 0.90 1.20	0.90 2.00 2.60	0.30 0.90 1.2	0.90 2.00 2.60	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6	0.66 0.98 1.25	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	1.2 1.4	1.41 1.59	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4	0.56 0.60	– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		20	34		43		51	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 8

TRANSFER CHARACTERISTIC WAVEFORMS

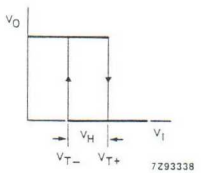


Fig. 6 Transfer characteristic.

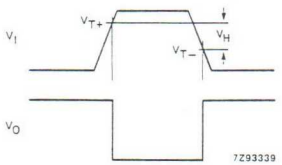


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

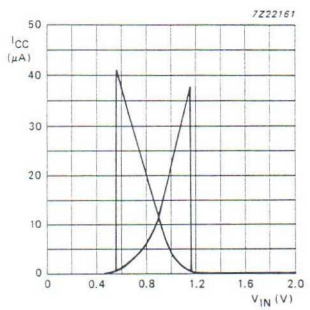


Fig. 8 Typical HC transfer characteristics; V_{CC} = 2 V.

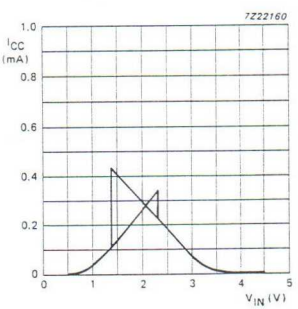


Fig. 9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

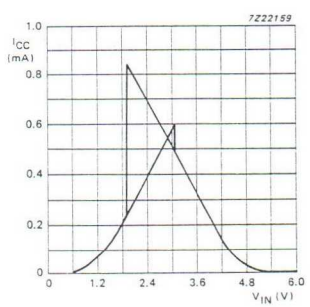


Fig. 10 Typical HC transfer characteristics; V_{CC} = 6 V.

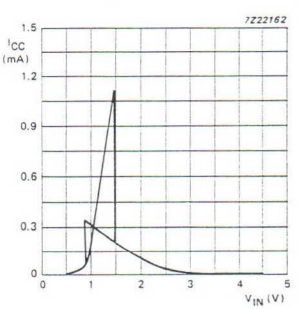


Fig. 11 Typical HCT transfer characteristics; V_{CC} = 4.5 V.

TRANSFER CHARACTERISTIC WAVEFORMS (Cont'd)

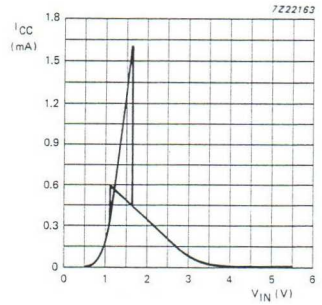


Fig. 12 Typical HCT transfer characteristics; V_{CC} = 5.5 V.

AC WAVEFORMS

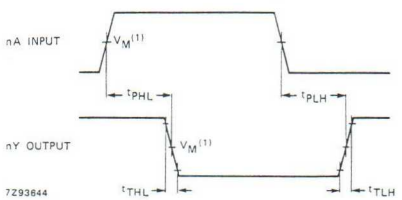


Fig. 13 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (μs); 10% – 90%
t_f = input fall time (μs); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figs 14 and 15.

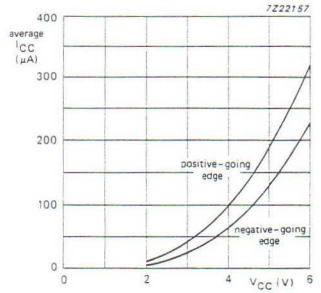


Fig. 14 Average I_{CC} for HC Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

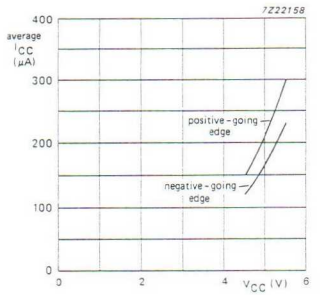


Fig. 15 Average I_{CC} for HCT Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

HC/HCT14 used in a relaxation oscillator circuit, see Fig. 16.

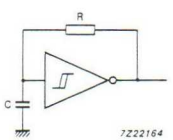


Fig. 16 Relaxation oscillator using HC/HCT14.

Note to Fig. 16

HC : $f = \frac{1}{T} \approx \frac{1}{0.8\ RC}$

HCT: $f = \frac{1}{T} \approx \frac{1}{0.67\ RC}$

Note to Application information

All values given are typical unless otherwise specified.

DUAL 4-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT20 provide the 4-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

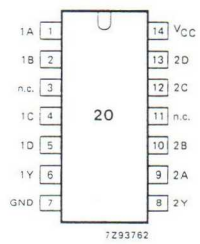


Fig. 1 Pin configuration.

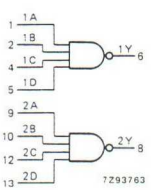


Fig. 2 Logic symbol.

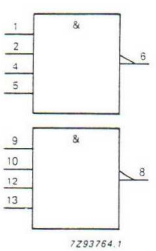


Fig. 3 IEC logic symbol.

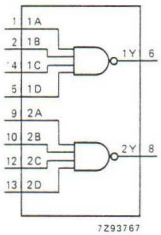


Fig. 4 Functional diagram.

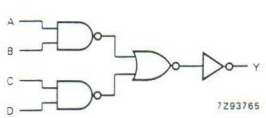


Fig. 5 HC logic diagram (one gate).

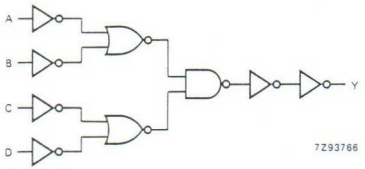


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.3

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY		16	28		35		42	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

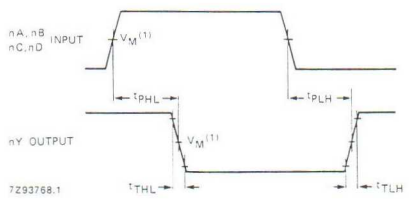


Fig. 7 Waveforms showing the enable input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-INPUT AND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT21 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT21 provide the 4-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	15	16	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

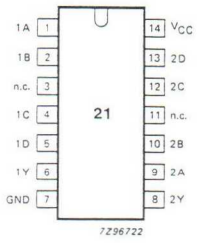


Fig. 1 Pin configuration.

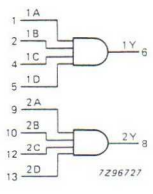


Fig. 2 Logic symbol.

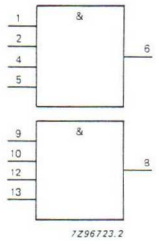


Fig. 3 IEC logic symbol.

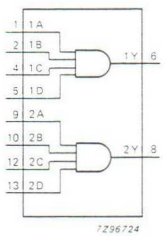


Fig. 4 Functional diagram.

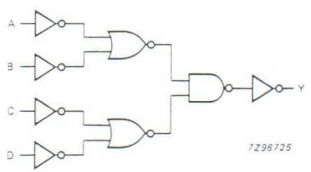


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	1.50 1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		15	27		34		41	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

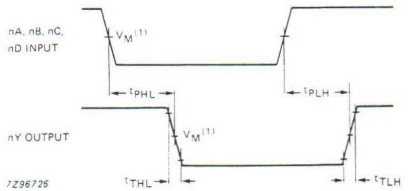


Fig. 6 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRIPLE 3-INPUT NOR GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT27 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT27 provide the 3-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
14	V_{CC}	positive supply voltage

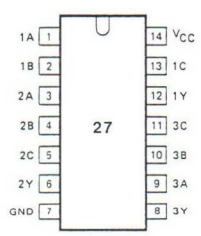


Fig. 1 Pin configuration.

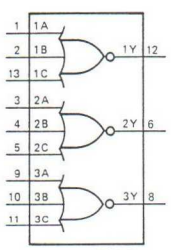


Fig. 2 Logic symbol.

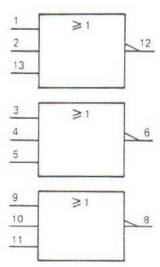


Fig. 3 IEC logic symbol.

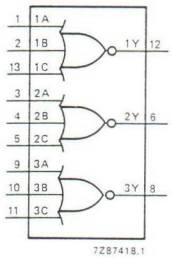


Fig. 4 Functional diagram.

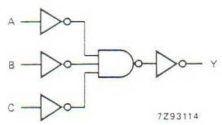


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY		12	21		26		32	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

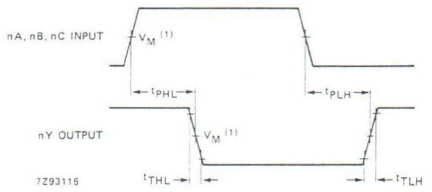


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT30 provide the 8-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y	C_L = 15 pF; V_{CC} = 5 V	12	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	15	15	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A	data input
2	B	data input
3	C	data input
4	D	data input
5	E	data input
6	F	data input
7	GND	ground (0 V)
8	Y	data output
9, 10, 13	n.c.	not connected
11	G	data input
12	H	data input
14	V_{CC}	positive supply voltage

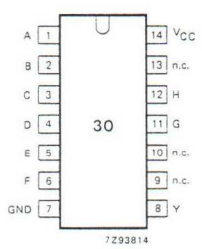


Fig. 1 Pin configuration.

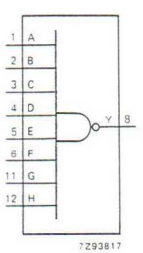


Fig. 2 Logic symbol.

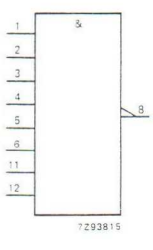


Fig. 3 IEC logic symbol.

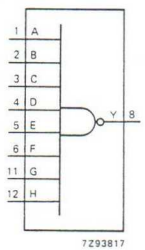


Fig. 4 Functional diagram;
$Y = \overline{ABCDEFGH}$.

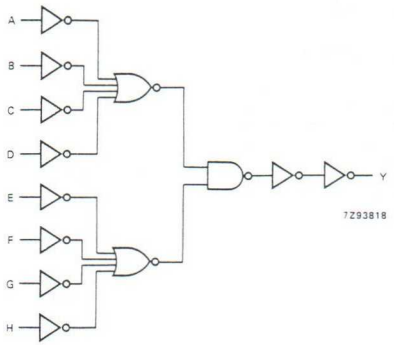


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A, B, C, D, E, F, G, H	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y		16	28		35		42	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

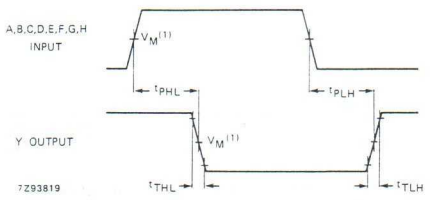


Fig. 6 Waveforms showing the input (A, B, C, D, E, F, G, H) to output (Y) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT OR GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT32 provide the 2-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	6	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

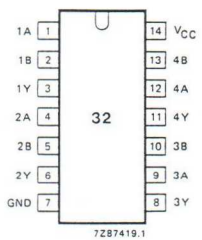


Fig. 1 Pin configuration.

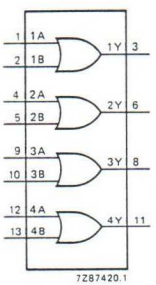


Fig. 2 Logic symbol.

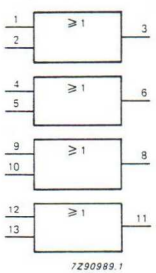


Fig. 3 IEC logic symbol.

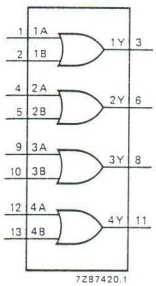


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

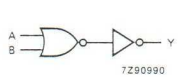


Fig. 5 Logic diagram 74HC (one gate).

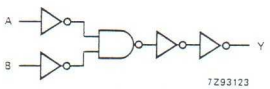


Fig. 6 Logic diagram 74HCT (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC}	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		11	24		30		36	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

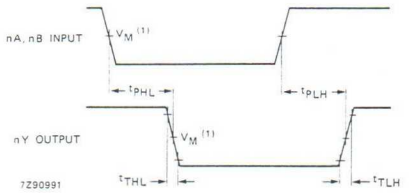


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

BCD TO DECIMAL DECODER (1-OF-10)

FEATURES

- Mutually exclusive outputs
- 1-of-8 demultiplexing capability
- Outputs disabled for input codes above nine
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT42 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT42 decoders accept four active HIGH BCD inputs and provide 10 mutually exclusive active LOW outputs. The active LOW outputs facilitate addressing other MSI circuits with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input (A_3) produces a useful inhibit function when the "42" is used as a 1-of-8 decoder. The A_3 input can also be used as the data input in an 8-output demultiplexer application.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	14	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	37	37	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 9, 10, 11	$\overline{Y}_0$ to $\overline{Y}_9$	multiplexer outputs
8	GND	ground (0 V)
15, 14, 13, 12	A_0 to A_3	data inputs
16	V_{CC}	positive supply voltage

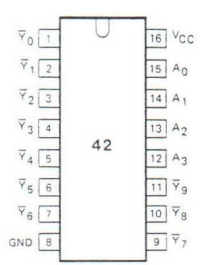


Fig. 1 Pin configuration.

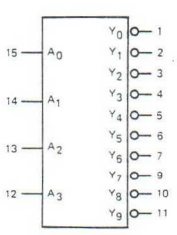


Fig. 2 Logic symbol.

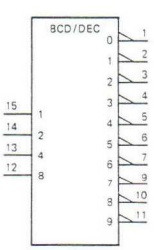


Fig. 3 IEC logic symbol.

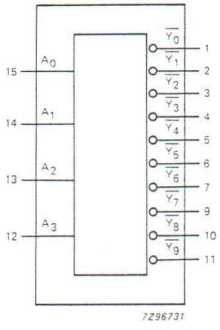


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

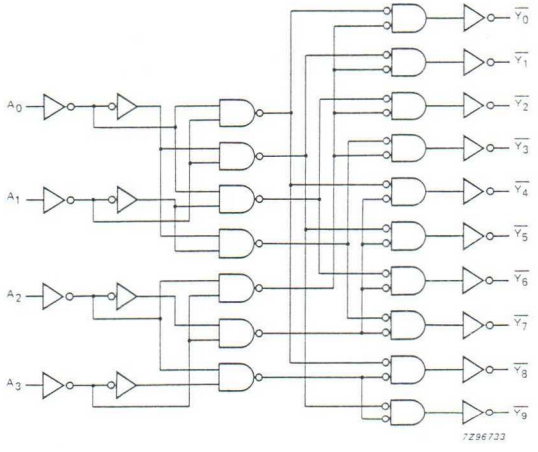


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		20	35		44		53	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

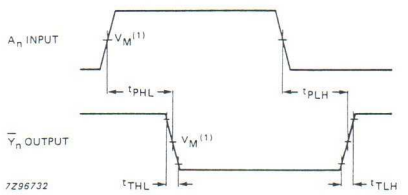


Fig. 6 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL AND-OR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC58 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The "58" provides two sections of AND-OR gates. One section contains a 2-wide, 3-input (1A to 1F) AND-OR gate and the second section contains a 2-wide, 2-input (2A to 2D) AND-OR gate.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay 1n to 1Y 2n to 2Y	C_L = 15 pF V_{CC} = 5 V	 11 9	 ns ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

GND = 0 V; T_{amb} = 15 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 12, 13, 9, 10, 11	1A to 1F	data inputs
2, 3, 4, 5	2A to 2D	data inputs
8, 6	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

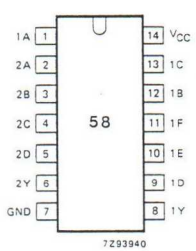


Fig. 1 Pin configuration.

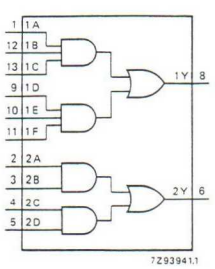


Fig. 2 Logic symbol.

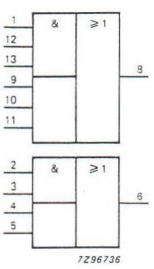


Fig. 3 IEC logic symbol.

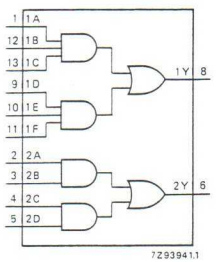


Fig. 4 Functional diagram.

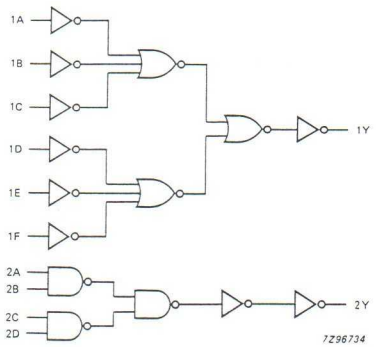


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
L	X	X	L	X	X	L
L	X	X	X	L	X	L
L	X	X	X	X	L	L
X	L	X	L	X	X	L
X	L	X	X	L	X	L
X	L	X	X	X	L	L
X	X	L	L	X	X	L
X	X	L	X	L	X	L
X	X	L	X	X	L	L
X	X	X	H	H	H	H
H	H	H	X	X	X	H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
L	X	L	X	L
L	X	X	L	L
X	L	L	X	L
X	L	X	L	L
X	X	H	H	H
H	H	X	X	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay 1A,1B,1C,1D,1E,1F to 1Y		36 13 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay 2A,2B,2C,2D to 2Y		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

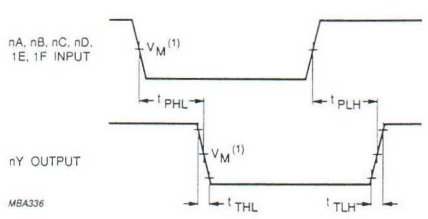


Fig. 6 Waveforms showing the input (nA, nB, nC, nD, 1E, 1F) to output (nY) propagation delays and the output transition times.

Note to AC waveforms
(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- **Output capability: standard**
- **I_{CC} category: flip-flops**

GENERAL DESCRIPTION

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ	C_L = 15 pF, V_{CC} = 5 V	16	15	ns
	propagation delay $n\overline{CP}$ to $n\overline{Q}$		16	18	ns
	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		15	15	ns
f_{max}	maximum clock frequency		77	79	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
2, 6	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
4	V_{CC}	positive supply voltage
11	GND	ground (0 V)
12, 9	1Q, 2Q	true flip-flop outputs
13, 8	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2

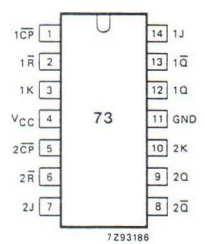


Fig. 1 Pin configuration.

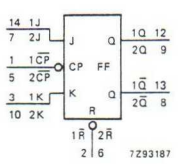


Fig. 2 Logic symbol.

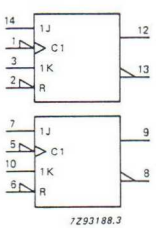


Fig. 3 IEC logic symbol.

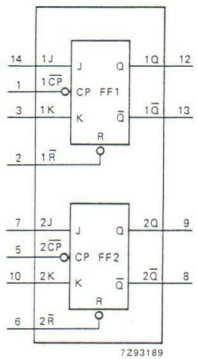


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

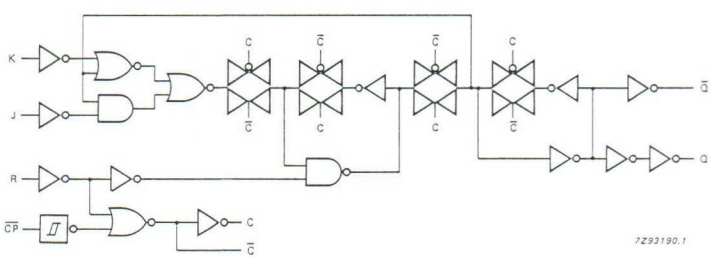


Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	reset pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nK	0.60
$n\overline{R}$	0.65
$n\overline{CP}$, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74 HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		18	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		21	36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		20	34		43		51	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t_W	reset pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	14	8		18		21		ns	4.5	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	12	6		15		18		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	3	−2		3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

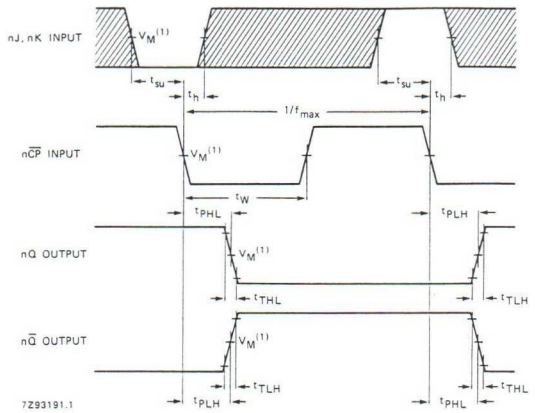


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ) propagation delays, the clock pulse width, the J and K to nCP set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

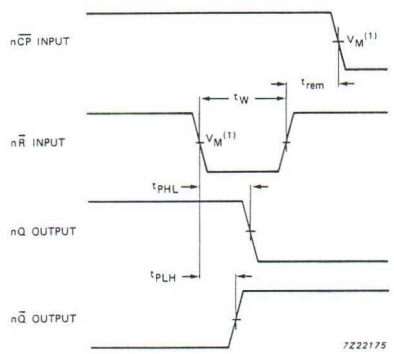


Fig. 7 Waveforms showing the reset (nR) input to output (nQ, nQ) propagation delays and the reset pulse width and the nR to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, nQ̄ n$\overline{S}_D$ to nQ, nQ̄ n$\overline{R}_D$ to nQ, nQ̄	C_L = 15 pF V_{CC} = 5 V	14 15 16	15 18 18	ns ns ns
f_{max}	maximum clock frequency		76	59	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1Q̄, 2Q̄	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

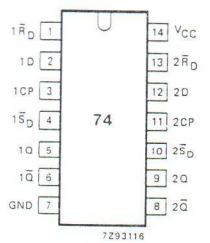


Fig. 1 Pin configuration.

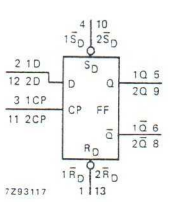


Fig. 2 Logic symbol.

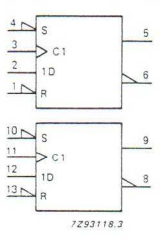


Fig. 3 IEC logic symbol.

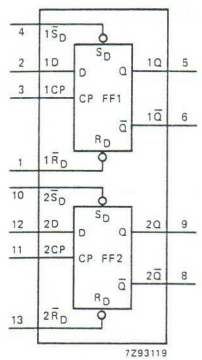


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

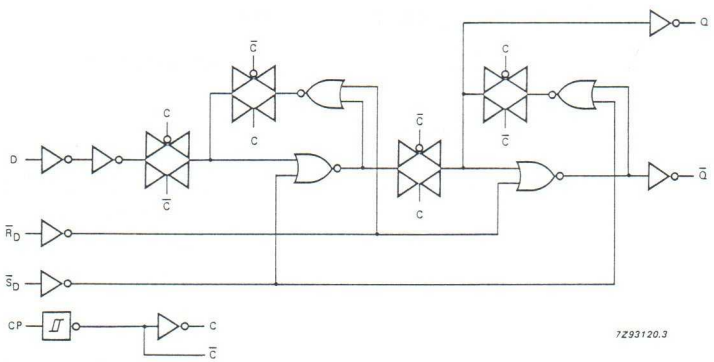


Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$		50 18 14	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$		52 19 15	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time set or reset	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nD to nCP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nD to nCP	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 69 82		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.70
$n\overline{R}_D$	0.70
$n\overline{S}_D$	0.80
nCP	0.80

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$		18	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		23	40		50		60	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		24	40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6
t_W	set or reset pulse width LOW	16	9		20		24		ns	4.5	Fig. 7
t_{rem}	removal time set or reset	6	1		8		9		ns	4.5	Fig. 7
t_{su}	set-up time nD to nCP	12	5		15		18		ns	4.5	Fig. 6
t_h	hold time nD to nCP	3	−3		3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	27	54		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

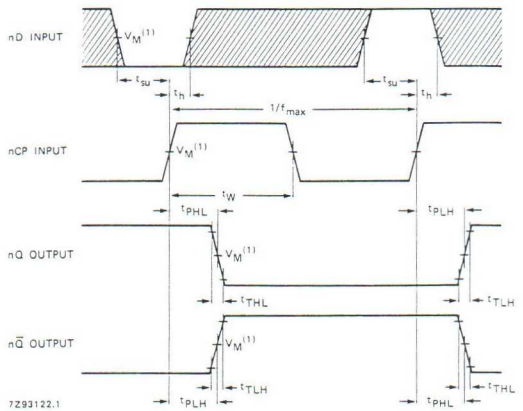


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

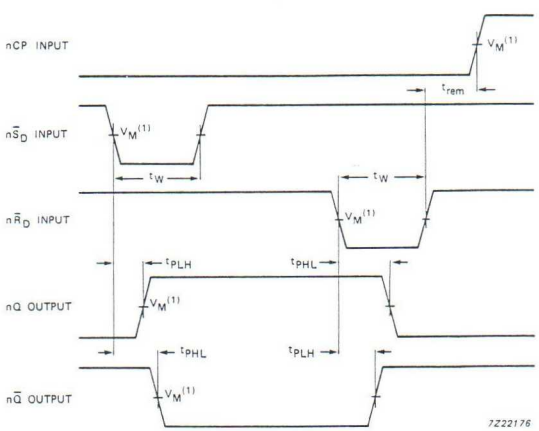


Fig. 7 Waveforms showing the set (nS̄D) and reset (nR̄D) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nR̄D to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BISTABLE TRANSPARENT LATCH

FEATURES

- Complementary Q and $\overline{Q}$ outputs
- V_{CC} and GND on the centre pins
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE_{1-2} and LE_{3-4}). When LE_{n-n} is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE_{n-n} is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE_{n-n} will be stored in the latches. The latched outputs remain stable as long as the LE_{n-n} is LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nD to nQ, n$\overline{Q}$ LE_{n-n} to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	11 11	12 11	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	1$\overline{Q}$ to 4$\overline{Q}$	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE_{3-4}	latch enable input, latches 3 and 4 (active HIGH)
5	V_{CC}	positive supply voltage
12	GND	ground (0 V)
13	LE_{1-2}	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs

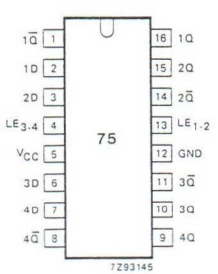


Fig. 1 Pin configuration.

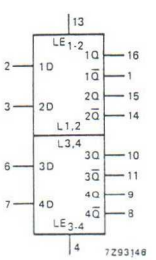


Fig. 2 Logic symbol.

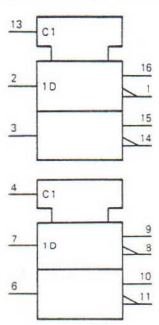


Fig. 3 IEC logic symbol.

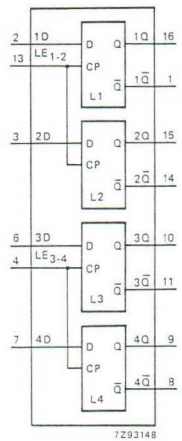


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS		OUTPUTS	
	LE_{n-n}	nD	nQ	$n\overline{Q}$
data enabled	H H	L H	L H	H L
data latched	L	X	q	$\overline{q}$

H = HIGH voltage level
L = LOW voltage level
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LE_{n-n} transition
X = don't care

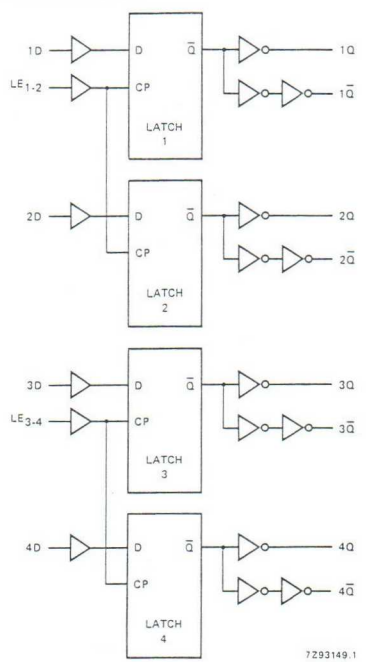


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nD to n$\overline{Q}$		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to nQ		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to n$\overline{Q}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t_W	enable pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time nD to $LE_{n\text{-}n}$	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time nD to $LE_{n\text{-}n}$	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.75
$LE_{n\text{-}n}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nD to $n\overline{Q}$		15	28		35		42	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to nQ		13	28		35		42	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $LE_{n\text{-}n}$ to $n\overline{Q}$		15	30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t_W	enable pulse width HIGH	16	4		20		24		ns	4.5	Fig. 8
t_{su}	set-up time nD to $LE_{n\text{-}n}$	12	4		15		18		ns	4.5	Fig. 9
t_h	hold time nD to $LE_{n\text{-}n}$	3	−2		3		3		ns	4.5	Fig. 9

AC WAVEFORMS

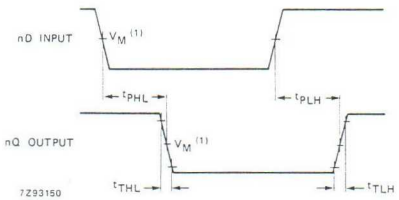


Fig. 6 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

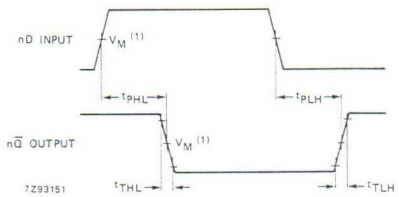


Fig. 7 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

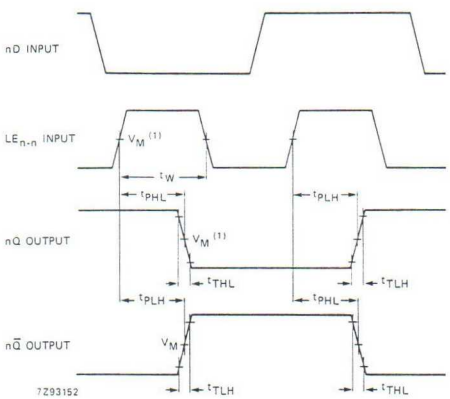


Fig. 8 Waveforms showing the latch enable input (LE_{n-n}) pulse width, the latch enable input to outputs (nQ, nQ̄) propagation delays and the output transition times.

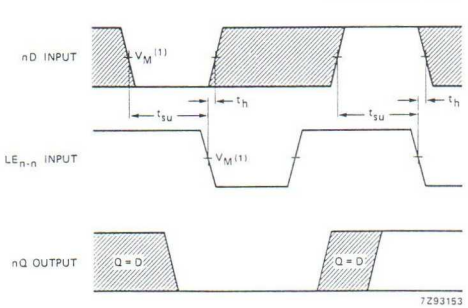


Fig. 9 Waveforms showing the data set-up and hold times for nD input to LE_{n-n} input.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT MAGNITUDE COMPARATOR

FEATURES

- Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ($Q_{A>B}$, $Q_{A=B}$ and $Q_{A<B}$). The 4-bit inputs are weighted (A_0 to A_3 and B_0 to B_3), where A_3 and B_3 are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs ($I_{A>B}$, $I_{A=B}$ and $I_{A<B}$) to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} =$ = LOW and $I_{A=B}$ = HIGH.
For words greater than 4-bits, units can be cascaded by connecting outputs $Q_{A<B}$, $Q_{A>B}$ and $Q_{A=B}$ to the corresponding inputs of the significant comparator.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$, $Q_{A<B}$	C_L = 15 pF; V_{CC} = 5 V	20	22	ns
	A_n, B_n to $Q_{A=B}$		18	20	ns
	$I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$		15	15	ns
	$I_{A=B}$ to $Q_{A=B}$		11	15	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	$I_{A<B}$	A < B expansion input
3	$I_{A=B}$	A = B expansion input
4	$I_{A>B}$	A > B expansion input
5	$Q_{A>B}$	A > B output
6	$Q_{A=B}$	A = B output
7	$Q_{A<B}$	A < B output
8	GND	ground (0 V)
9, 11, 14, 1,	B_0 to B_3	word B inputs
10, 12, 13, 15	A_0 to A_3	word A inputs
16	V_{CC}	positive supply voltage

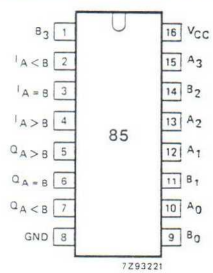


Fig. 1 Pin configuration.

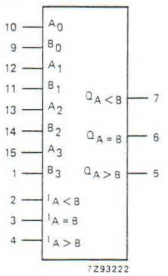


Fig. 2 Logic symbol.

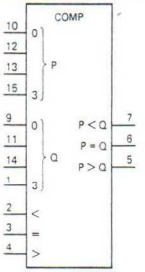


Fig. 3 IEC logic symbol.

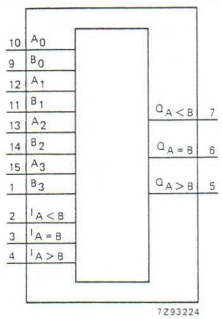


Fig. 4 Functional diagram.

APPLICATIONS

- Process controllers
- Servo-motor control

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$Q_{A>B}$	$Q_{A<B}$	$Q_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

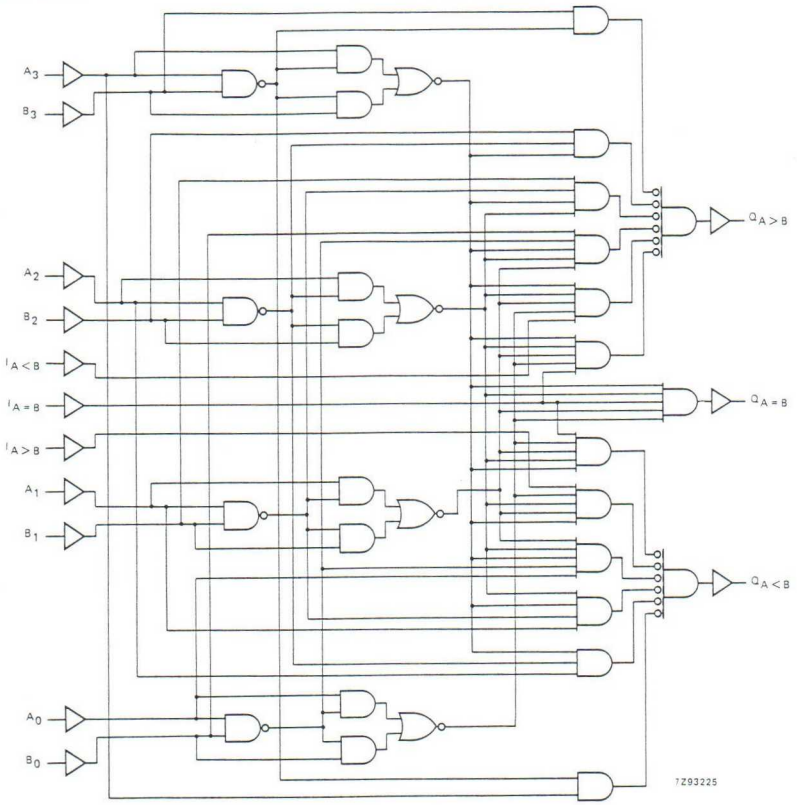


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A=B}$		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$		50 18 14	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A=B}$ to $Q_{A=B}$		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$I_{A<B}$	1.00
$I_{A>B}$	1.00
$I_{A=B}$	1.50
A_n, B_n	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$		26	44		55		66	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $Q_{A=B}$		24	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ to $Q_{A<B}$, $Q_{A>B}$		18	31		39		47	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $I_{A=B}$ to $Q_{A=B}$		18	31		39		47	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

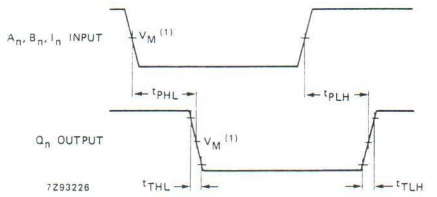


Fig. 6 Waveforms showing the word A inputs (A_n), word B inputs (B_n) and expansion inputs (I_n) to the outputs (Q_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

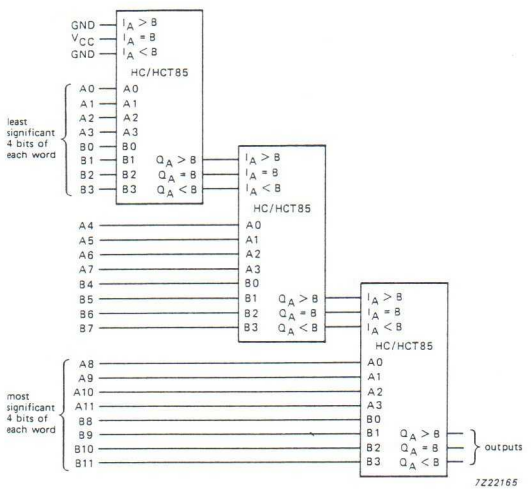


Fig. 7 Series cascading; comparing 12-bit words.

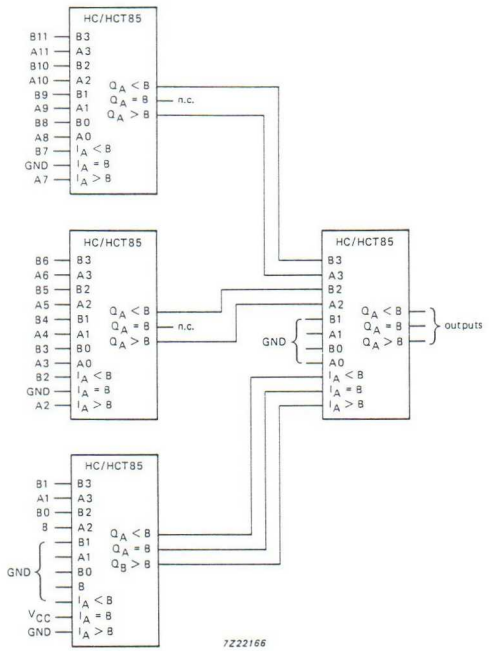


Fig. 8 Parallel cascading; comparing 12-bit words.

QUAD 2-INPUT EXCLUSIVE–OR GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT86 provide the EXCLUSIVE–OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	14	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

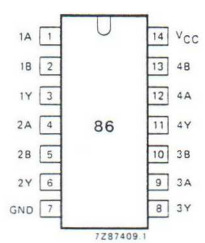


Fig. 1 Pin configuration.

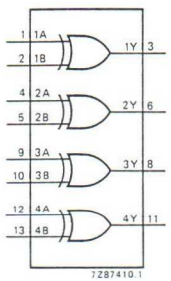


Fig. 2 Logic symbol.

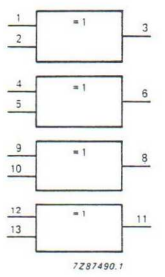


Fig. 3 IEC logic symbol.

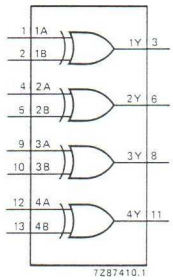


Fig. 4 Functional diagram.

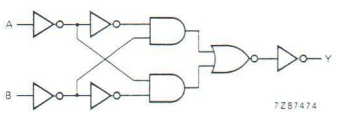


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		17	32		40		48	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

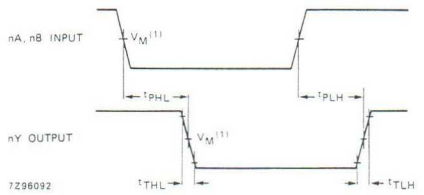


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT BINARY RIPPLE COUNTER

FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP}_0$ and $\overline{CP}_1$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR_1 and MR_2) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.
In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to clock input $\overline{CP}_0$. Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$.
Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	12	15	ns
f_{max}	maximum clock frequency		100	77	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}_1$	clock input 2nd, 3rd and 4th section (HIGH-to-LOW, edge-triggered)
2, 3	MR_1, MR_2	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	V_{CC}	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	Q_0 to Q_3	flip-flop outputs
14	$\overline{CP}_0$	clock input 1st section (HIGH-to-LOW, edge-triggered)

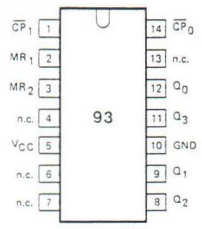


Fig. 1 Pin configuration.

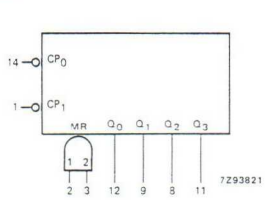


Fig. 2 Logic symbol.

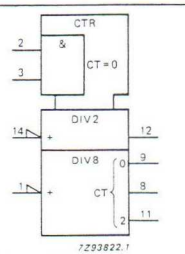


Fig. 3 IEC logic symbol.

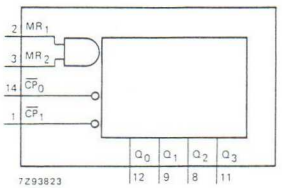


Fig. 4 Functional diagram.

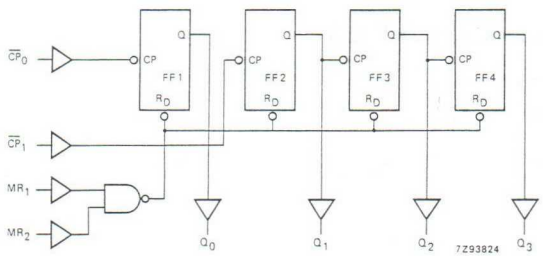


Fig. 5 Logic diagram.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

Note to function table

Output Q_0 connected to $\overline{CP}_1$.

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_1$ to Q_1		49 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_1$ to Q_2		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_1$ to Q_3		80 29 23	245 49 42		305 61 52		370 71 63	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR_n to Q_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_{rem}	removal time MR_n to $\overline{CP}_0$, $\overline{CP}_1$	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t_W	pulse width $\overline{CP}_0$, $\overline{CP}_1$	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width MR_n	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency $\overline{CP}_0$, $\overline{CP}_1$	6.0 30 35	30 91 108		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_0$, $\overline{CP}_1$	0.60
MR_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0		18	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_1		18	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_2		24	46		58		69	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_3		30	58		73		87	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR_n to Q_n		17	33		41		50	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_{rem}	removal time MR_n to $\overline{CP}_0$, $\overline{CP}_1$	10	3		13		15		ns	4.5	Fig. 7
t_W	pulse width $\overline{CP}_0$, $\overline{CP}_1$	16	7		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width MR_n	16	5		20		24		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency $\overline{CP}_0$, $\overline{CP}_1$	30	70		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

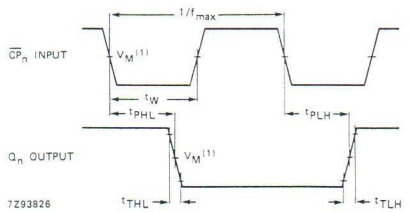


Fig. 6 Waveforms showing the clock ($\overline{CP}_n$) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

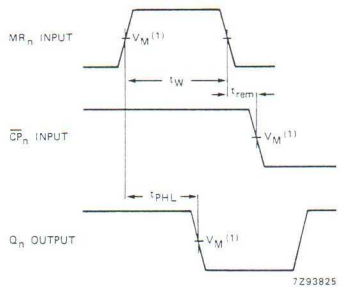


Fig. 7 Waveforms showing the master reset (MR_n) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}_n$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ	C_L = 15 pF; V_{CC} = 5 V	16	16	ns
	propagation delay $n\overline{CP}$ to $n\overline{Q}$		16	18	ns
	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		16	17	ns
f_{max}	maximum clock frequency		78	73	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
3, 5	1Q, 2Q	true flip-flop outputs
7	GND	ground (0 V)
12, 9	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
13, 10	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
14	V_{CC}	positive supply voltage

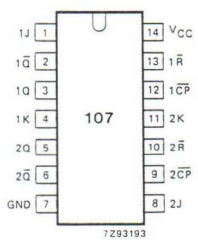


Fig. 1 Pin configuration.

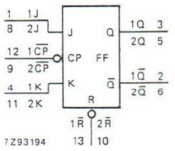


Fig. 2 Logic symbol.

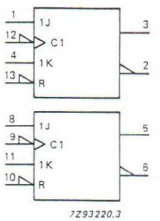


Fig. 3 IEC logic symbol.

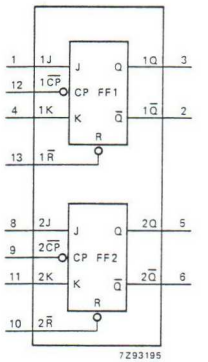


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

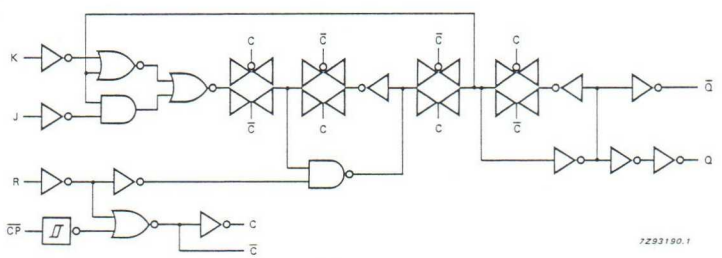


Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		52 19 15	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	60 12 10	19 7 6		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 85		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{K}$	0.60
$n\overline{R}$	0.65
$n\overline{CP}$, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		19	36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		21	36		45		54	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		20	38		48		57	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6
t_W	reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	14	8		18		21		ns	4.5	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	20	7		25		30		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	5	−2		5		5		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30	66		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

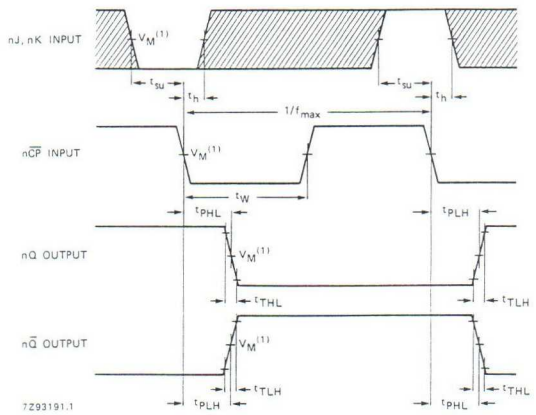


Fig. 6 Waveforms showing the clock (n$\overline{CP}$) to output (nQ, nQ̄) propagation delays, the clock pulse width, the J and K to n$\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

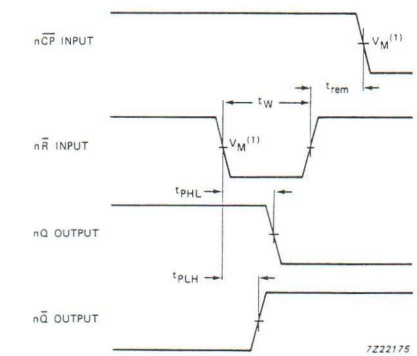


Fig. 7 Waveforms showing the reset (n$\overline{R}$) input to output (nQ, nQ̄) propagation delays, the reset pulse width and the n$\overline{R}$ to n$\overline{CP}$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL J$\overline{K}$ FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, $\overline{K}$ inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT109 are dual positive-edge triggered, J$\overline{K}$ flip-flops with individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.

The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	15 12 12	17 14 15	ns ns ns
f_{max}	maximum clock frequency		75	61	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

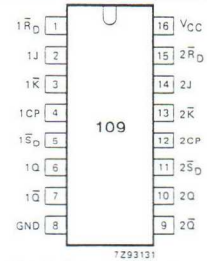


Fig. 1 Pin configuration.

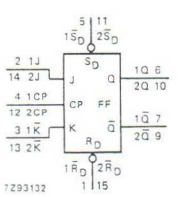


Fig. 2 Logic symbol.

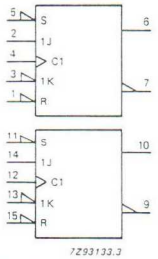


Fig. 3 IEC logic symbol.

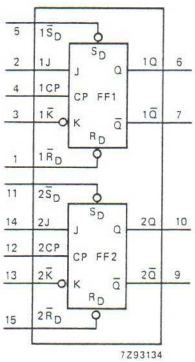


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	$\underline{L}$
hold "no change"	H	H	↑	l	h	q	$\underline{\overline{q}}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

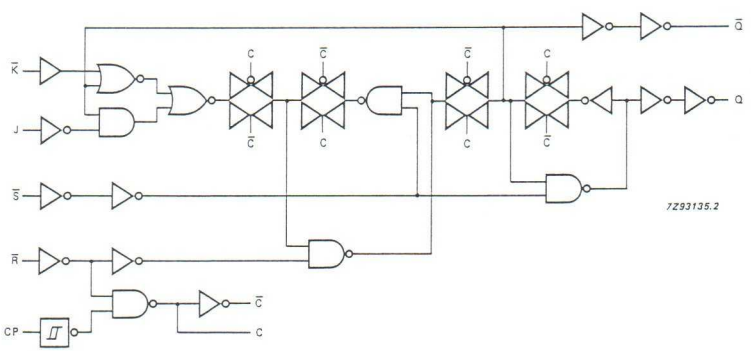


Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PLH}	propagation delay n$\overline{S}_D$ to nQ		30 11 9	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay n$\overline{S}_D$ to n$\overline{Q}$		41 15 12	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay n$\overline{R}_D$ to nQ		41 15 12	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t_{PLH}	propagation delay n$\overline{R}_D$ to n$\overline{Q}$		39 14 11	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time n$\overline{S}_D$, n$\overline{R}_D$ to nCP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, n$\overline{K}$ to nCP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, n$\overline{K}$ to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		5.0 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nJ, $n\overline{K}$	0.35
$n\overline{R}_D$	0.35
$n\overline{S}_D$	0.35
nCP	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$		20	35		44		53	ns	4.5	Fig. 6
t_{PLH}	propagation delay $n\overline{S}_D$ to nQ		13	26		33		39	ns	4.5	Fig. 7
t_{PHL}	propagation delay $n\overline{S}_D$ to $n\overline{Q}$		19	35		44		53	ns	4.5	Fig. 7
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		19	35		44		53	ns	4.5	Fig. 7
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		16	32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6
t_W	set or reset pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	16	8		20		24		ns	4.5	Fig. 7
t_{su}	set-up time nJ, $n\overline{K}$ to nCP	18	8		23		27		ns	4.5	Fig. 6
t_h	hold time nJ, $n\overline{K}$ to nCP	3	−3		3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

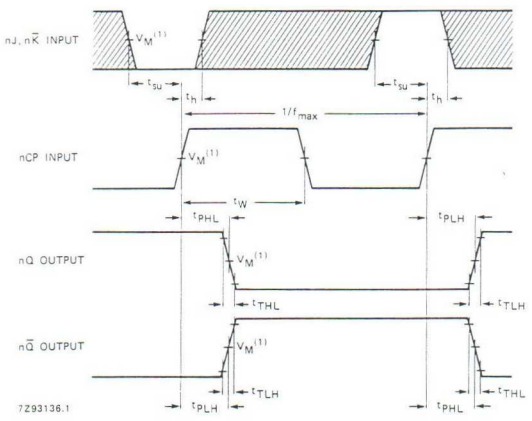


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK̄ to nCP set-up, the nCP to nJ, nK̄ hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

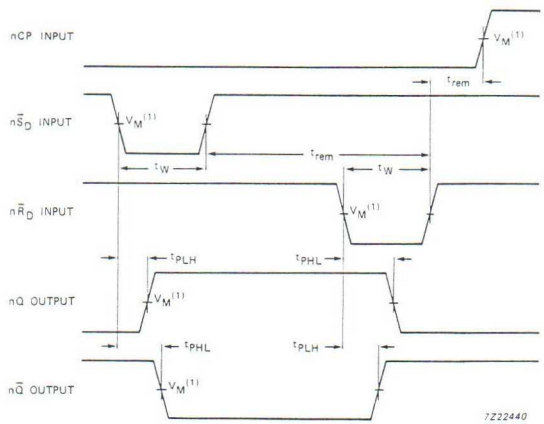


Fig. 7 Waveforms showing the set (nS̄D) and reset (nR̄D) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nR̄D, nS̄D to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL JK FLIP-FLOP WITH SET AND RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Asynchronous set and reset
- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT112 are dual negative-edge triggered JK-type flip-flops featuring individual nJ, nK, clock ($n\overline{CP}$), set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) inputs. The set and reset inputs, when LOW, set or reset the outputs as shown in the function table regardless of the levels at the other inputs.

A HIGH level at the clock ($n\overline{CP}$) input enables the nJ and nK inputs and data will be accepted. The nJ and nK inputs control the state changes of the flip-flops as shown in the function table. The nJ and nK inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Output state changes are initiated by the HIGH-to-LOW transition of $n\overline{CP}$.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		15	15	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		18	19	ns
f_{max}	maximum clock frequency		66	70	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	V_{CC}	positive supply voltage

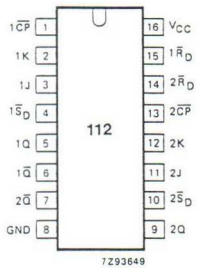


Fig. 1 Pin configuration.

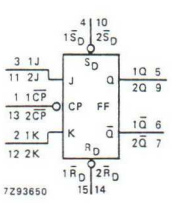


Fig. 2 Logic symbol.

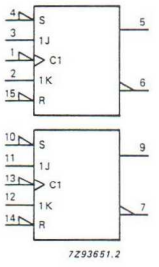


Fig. 3 IEC logic symbol.

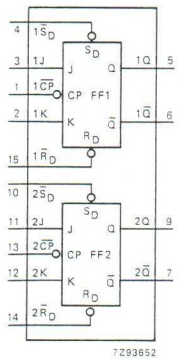


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	L
toggle	H	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	H	↓	l	h	L	H
load "1" (set)	H	H	↓	h	l	H	L
hold "no change"	H	H	↓	l	l	q	$\overline{q}$

Note to function table

If $n\overline{S}_D$ and $n\overline{R}_D$ simultaneously go from LOW to HIGH, the output states will be unpredictable.

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

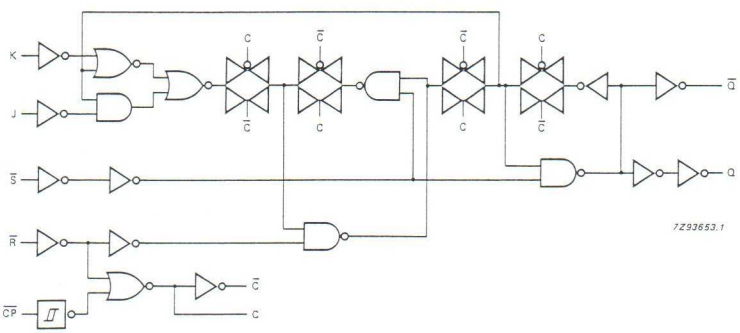


Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		50 18 14	155 31 26		295 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	80 16 14	−19 −7 −6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1\overline{S}_D$, $2\overline{S}_D$	0.5
1K, 2K	0.6
$1\overline{R}_D$, $2\overline{R}_D$	0.65
1J, 2J	1
$1\overline{CP}$, $2\overline{CP}$	1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		21	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		23	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		22	37		46		56	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		18	32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t_W	set or reset pulse width LOW	18	10		23		27		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	20	11		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	20	−8		25		30		ns	4.5	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	16	7		20		24		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	0	−7		0		0		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

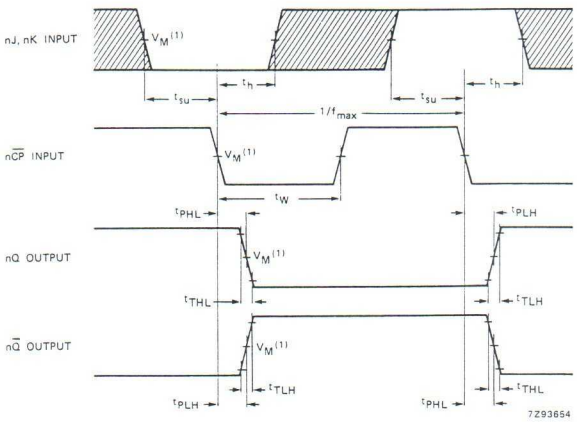


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ) propagation delays, the clock pulse width, the nJ, nK to nCP set-up times, the nCP to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

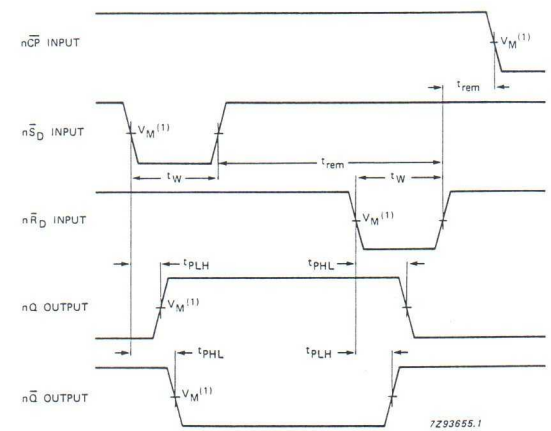


Fig. 7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ) propagation delays, the set and reset pulse width and the $n\overline{R}_D$ and $n\overline{S}_D$ to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	26 20	26 23	ns ns
	$n\overline{R}_D$ to nQ, $n\overline{Q}$				
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per monostable	notes 1 and 2	54	56	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   D = duty factor in %
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   C_{EXT} = timing capacitance in pF
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

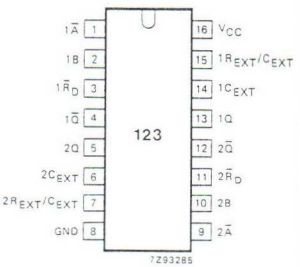


Fig. 1 Pin configuration.

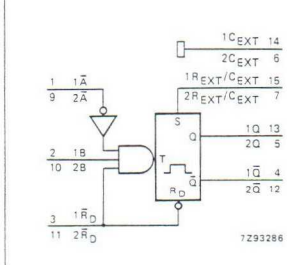


Fig. 2 Logic symbol.

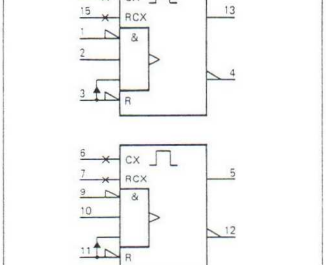


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset LOW and trigger action at positive edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

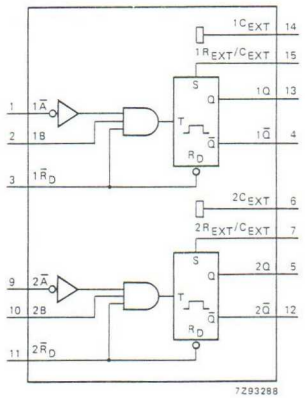


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd)

An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positive-going signal at input $n\overline{R}_D$ as shown in the function table. Figures 7 and 8 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. For pulse widths, when $C_{EXT} < 10\,000$ pF, see Fig. 9.

When $C_{EXT} > 10\,000$ pF, the typical output pulse width is defined as:

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

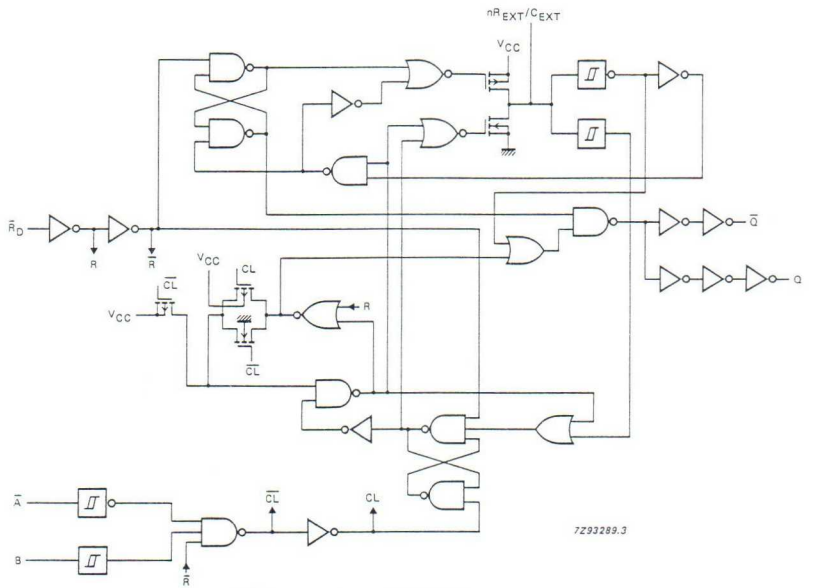
The '123' is identical to the '423' but can be triggered via the reset input.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L*	H*
X	X	L	L*	H*
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴
↑	L	H	⎍	⎴

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎴ = one LOW level output pulse

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.



(1) For minimum noise generation, it is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Fig. 5 Logic diagram.

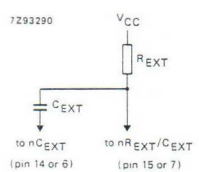


Fig. 6 Timing component connections.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $n\overline{R}_D$, $n\overline{A}$, nB to $n\overline{Q}$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$, $n\overline{A}$, nB to nQ		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ (reset)		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$ (reset)		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t_W	trigger pulse width $n\overline{A}$ = LOW	100 20 17	8 3 2		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	100 20 17	14 5 4		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		26		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	10 2		1000 1000	–		–		kΩ	2.0 5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{A}$, nB	0.35
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $n\overline{R}_D$, nA, nB to $n\overline{Q}$		30	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$, nA, nB to nQ		28	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ (reset)		27	46		58		69	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$ (reset)		23	46		58		69	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	
t_W	trigger pulse width $n\overline{A}$ = LOW	20	3		25		30		ns	4.5	Fig. 7
t_W	trigger pulse width nB = HIGH	20	5		25		30		ns	4.5	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	20	7		25		30		ns	4.5	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		110		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

Notes to AC characteristics

1. For other R_{EXT} and C_{EXT} combinations see Fig. 9.

   If $C_{EXT} > 10$ nF, the next formula is valid:

   $$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.

   The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

   If $C_{EXT} > 10$ pF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

   $$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

AC WAVEFORMS

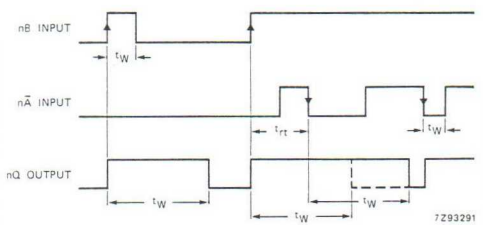


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

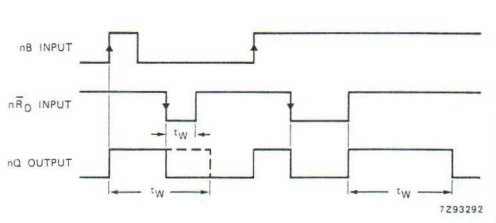


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.

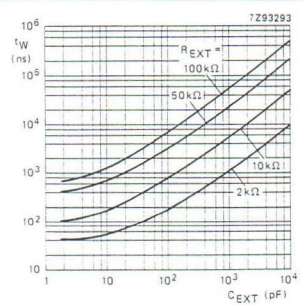


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

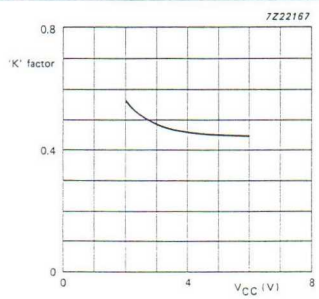


Fig. 10 HCT typical "k" factor as a function of V_{CC}; C_X = 10 nF; R_X = 10 kΩ to 100 kΩ.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_X, this output pulse can be eliminated using the circuit shown in Fig. 11.

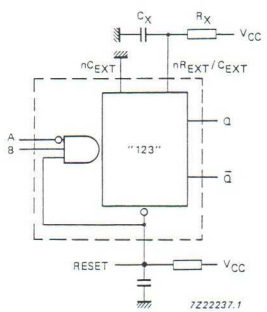


Fig. 11 Power-up output pulse elimination circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 12.

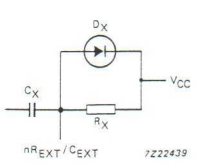


Fig. 12 Power-down protection circuit.

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	9	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

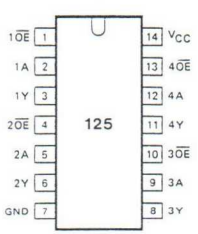


Fig. 1 Pin configuration.

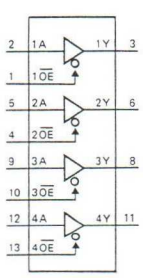


Fig. 2 Logic symbol.

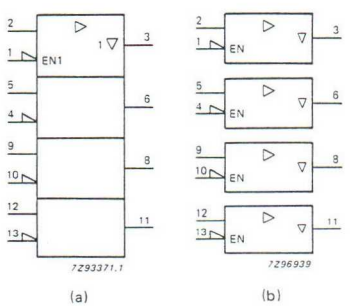


Fig. 3 IEC logic symbol.

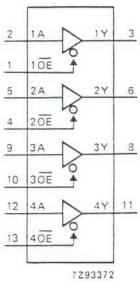


Fig. 4 Functional diagram.

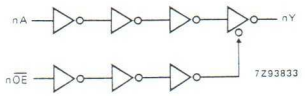


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, n$\overline{OE}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY		15	25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nY		15	28		35		42	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nY		15	25		31		38	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

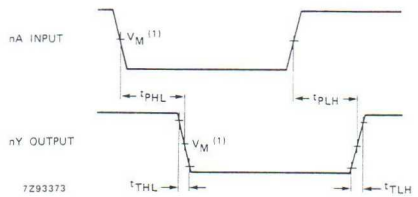


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

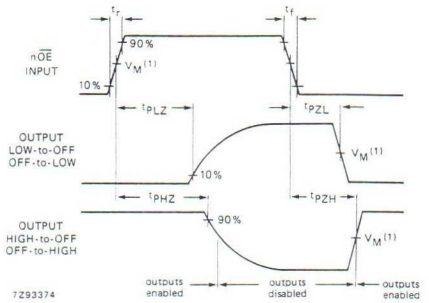


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	23	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

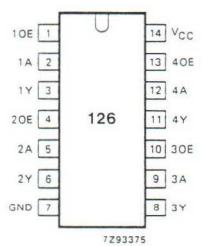


Fig. 1 Pin configuration.

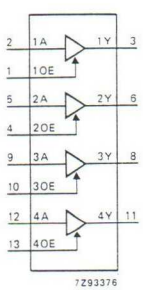


Fig. 2 Logic symbol.

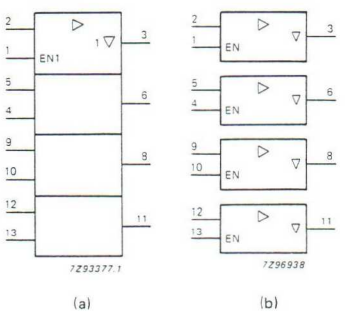


Fig. 3 IEC logic symbol.

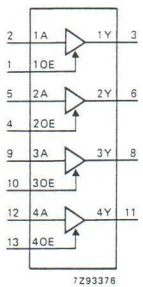


Fig. 4 Functional diagram.

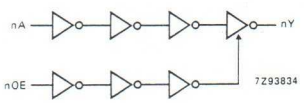


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY		14	24		30		36	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY		13	25		31		38	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY		18	28		35		42	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

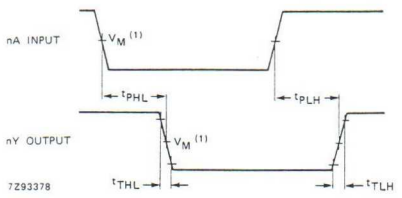


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

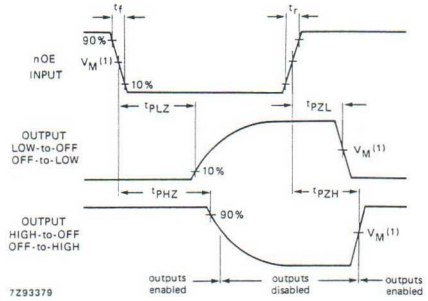


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT NAND SCHMITT TRIGGER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

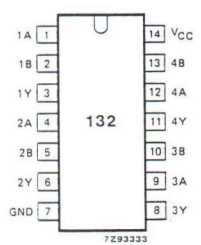


Fig. 1 Pin configuration.

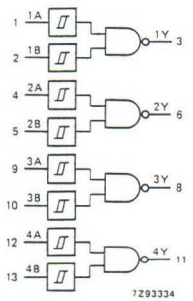


Fig. 2 Logic symbol.

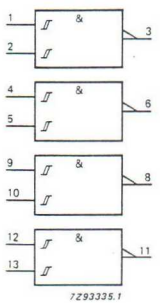


Fig. 3 IEC logic symbol.

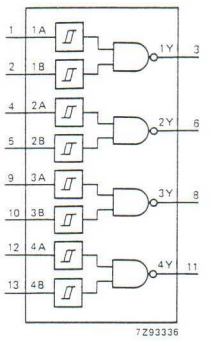


Fig. 4 Functional diagram.

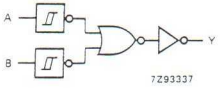


Fig. 5 Logic diagram (one Schmitt trigger).

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.7 1.7 2.1	1.18 2.38 3.14	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.3 0.9 1.2	0.63 1.67 2.26	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6	0.55 0.71 0.88	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 13

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	1.2 1.4	1.41 1.59	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4	0.56 0.60	– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		20	33		41		50	ns	4.5	Fig. 13
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 13

TRANSFER CHARACTERISTIC WAVEFORMS

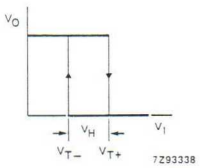


Fig. 6 Transfer characteristic.

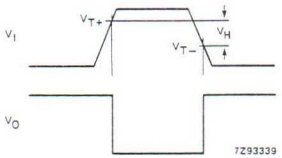


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

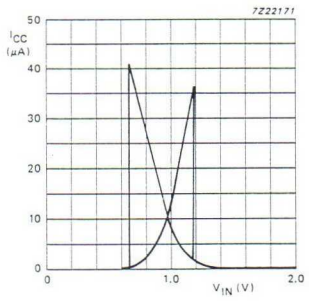


Fig. 8 Typical HC transfer characteristics; V_{CC} = 2 V.

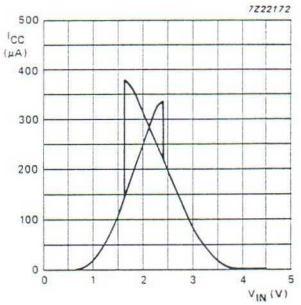


Fig. 9 Typical HC transfer characteristics; V_{CC} = 4.5 V.

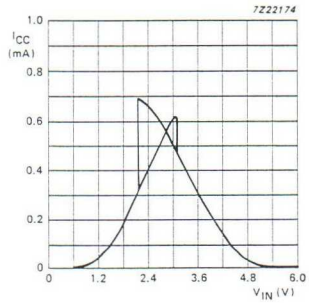


Fig. 10 Typical HC transfer characteristics; V_{CC} = 6 V.

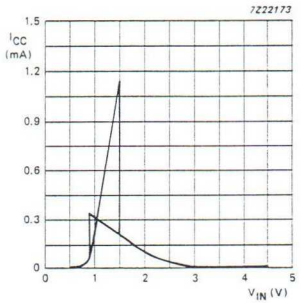


Fig. 11 Typical HCT transfer characteristics; V_{CC} = 4.5 V.

TRANSFER CHARACTERISTIC WAVEFORMS (Cont'd)

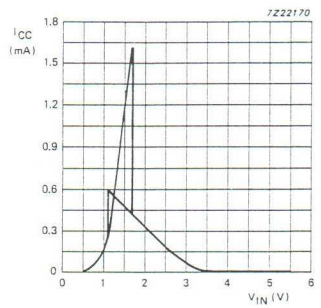


Fig. 12 Typical HCT transfer characteristics; V_{CC} = 5.5 V.

AC WAVEFORMS

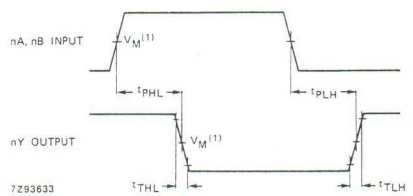


Fig. 13 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figs 14 and 15.

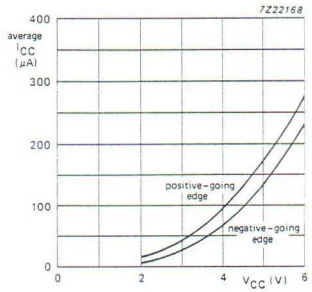


Fig. 14 Average I_{CC} for HC Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

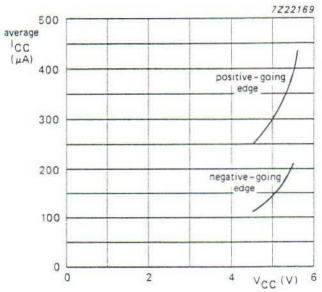


Fig. 15 Average I_{CC} for HCT Schmitt trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

HC/HCT132 used in a relaxation oscillator circuit, see Fig. 16.

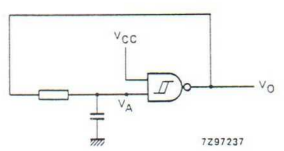


Fig. 16 Relaxation oscillator using HC/HCT132.

Note to Fig. 16

HC : $f = \frac{1}{T} \approx \frac{1}{0.8\ RC}$

HCT: $f = \frac{1}{T} \approx \frac{1}{0.67\ RC}$

Note to Application information

All values given are typical unless otherwise specified.

13-input NAND gate | 74HC133

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The HC133 is an high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC133 provides the 13-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A..M to Y	C_L = 15 pF V_{CC} = 5 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation per gate	notes 1 and 2	19	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For HC the condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74HC133N	16	DIL	plastic	SOT38
74HC133D	16	SO	plastic	SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1..7, 10..15	A..G, H..M	data input
8	GND	ground (0 V)
9	Y	data output
16	V_{CC}	positive supply voltage

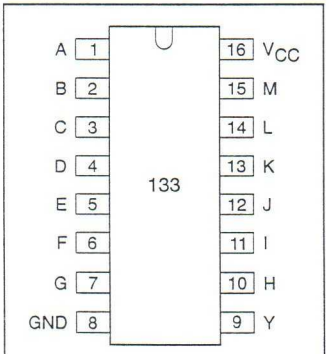


Fig.1 Pin configuration.

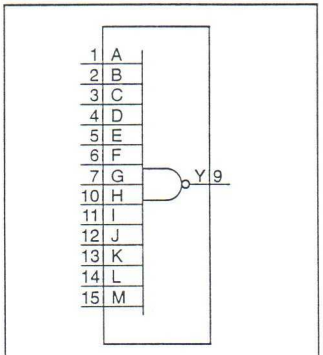


Fig.2 Logic symbol.

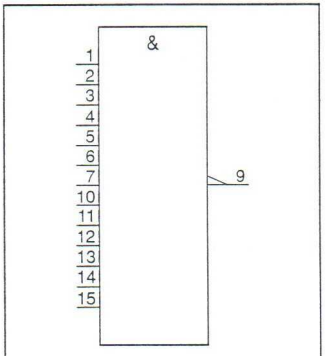


Fig.3 IEC logic symbol.

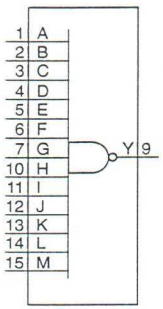


Fig.4 Functional diagram;
$Y = \overline{ABCDEFGHIJKLM}$.

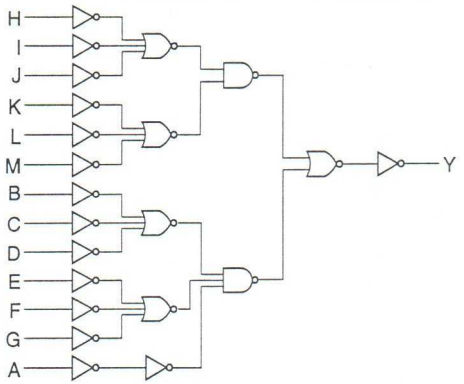


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS													OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	M	Y
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	X	X	X	L	X	X	X	X	X	X	X	H
X	X	X	X	X	X	L	X	X	X	X	X	X	H
X	X	X	X	X	X	X	L	X	X	X	X	X	H
X	X	X	X	X	X	X	X	L	X	X	X	X	H
X	X	X	X	X	X	X	X	X	L	X	X	X	H
X	X	X	X	X	X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A..M to Y	–	36	110	–	140	–	165	ns	2.0	Fig.6
		–	13	22	–	28	–	33		4.5	
		–	10	19	–	23	–	28		6.0	
t_{THL}/t_{TLH}	output transition time	–	19	75	–	95	–	110	ns	2.0	Fig.6
		–	7	15	–	19	–	22		4.5	
		–	6	13	–	16	–	19		6.0	

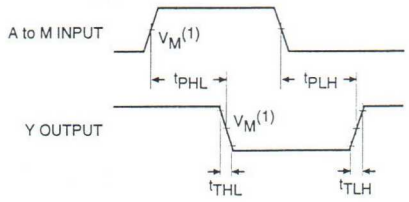


Fig.6 Waveforms showing the input (A, B, C, D, E, F, G, H, I, J, K, L, M) to output (Y) propagation delays and the output transition times.

Note to the AC waveforms

(1) HC: V_M = 50%; V_I = GND to V_{CC}.

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES; INVERTING

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The "137" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the "137" acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$ $\overline{LE}$ to $\overline{Y}_n$ $\overline{E}_1$ to $\overline{Y}_n$ E_2 to $\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	 18 17 15 15	 19 21 17 15	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	57	59	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E_2	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	multiplexer outputs
16	V_{CC}	positive supply voltage

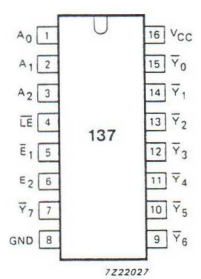


Fig. 1 Pin configuration.

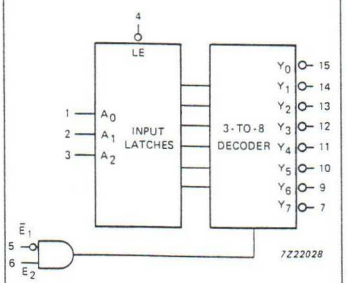


Fig. 2 Logic symbol.

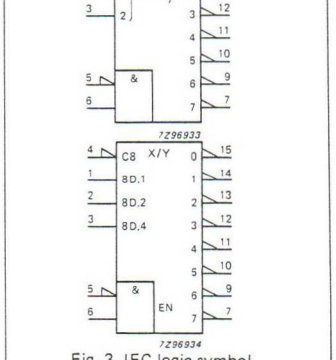


Fig. 3 IEC logic symbol.

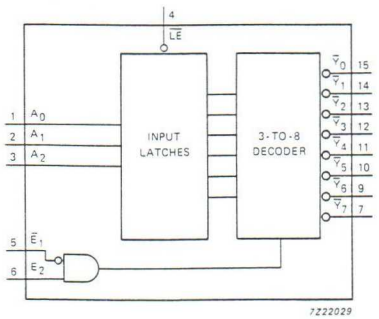


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

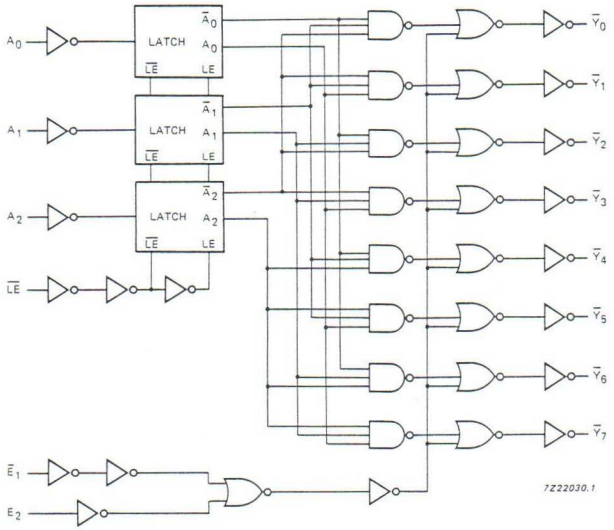


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to $\overline{Y}_n$		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_1$ to $\overline{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay E_2 to $\overline{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{LE}$ pulse width HIGH	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time A_n to $\overline{LE}$	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time A_n to $\overline{LE}$	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{E}_1$	1.50
E_2	1.50
$\overline{LE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to $\overline{Y}_n$		25	44		55		66	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_1$ to $\overline{Y}_n$		20	37		46		56	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay E_2 to $\overline{Y}_n$		18	35		44		53	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	$\overline{LE}$ pulse width HIGH	10	5		13		15		ns	4.5	Fig. 8
t_{su}	set-up time A_n to $\overline{LE}$	10	2		13		15		ns	4.5	Fig. 8
t_h	hold time A_n to $\overline{LE}$	7	2		9		11		ns	4.5	Fig. 8

AC WAVEFORMS

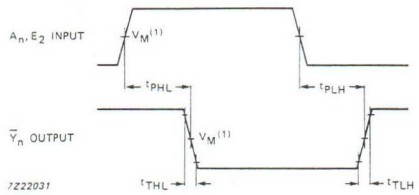


Fig. 6 Waveforms showing the address input (A_n) and enable inputs (E_2) to output ($\overline{Y}_n$) propagation delays and the output transition times.

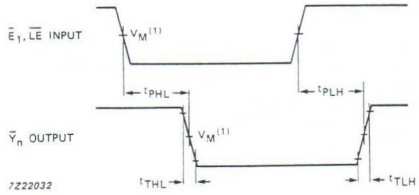


Fig. 7 Waveforms showing the enable input ($\overline{E}_1$, $\overline{LE}$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

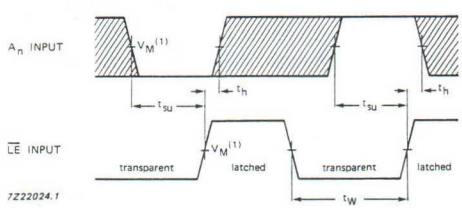


Fig. 8 Waveforms showing the data set-up, hold times for A_n input to $\overline{LE}$ input and the latch enable pulse width.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

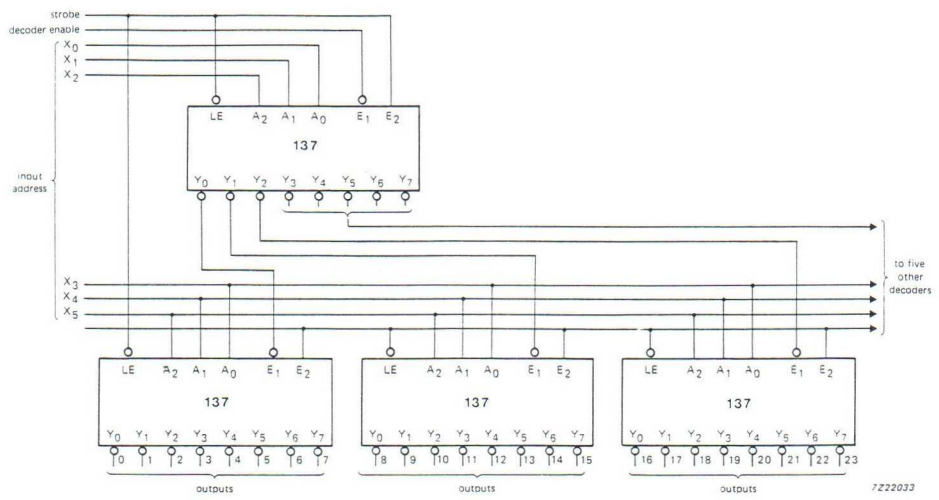


Fig. 9 6-to-64 line decoder with input address storage.

3-TO-8 LINE DECODER/DEMULTIPLEXER; INVERTING

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).
The "138" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	17	ns
t_{PHL}/t_{PLH}	E_3 to $\overline{Y}_n$; $\overline{E}_n$ to $\overline{Y}_n$		14	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

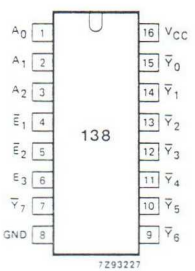


Fig. 1 Pin configuration.

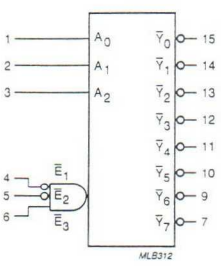


Fig. 2 Logic symbol.

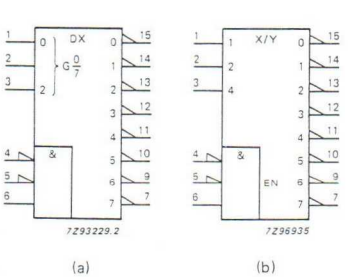


Fig. 3 IEC logic symbol.

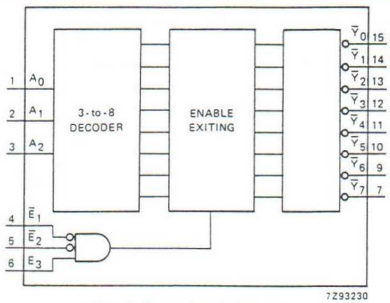


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

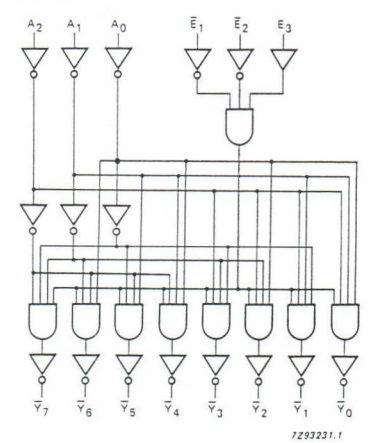


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay E_3 to $\overline{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{E}_n$	1.25
E_3	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		20	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$		18	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		19	40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

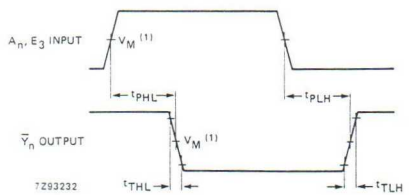


Fig. 6 Waveforms showing the address input (A_n) and enable input (E_3) to output ($\overline{Y}_n$) propagation delays and the output transition times.

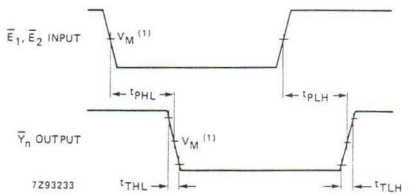


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT139 are high-speed, dual 2-to-4 line decoder/demultiplexers. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

The "139" is identical to the HEF4556 of the HE4000B family.

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$ $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	11 10	13 13	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	42	44	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

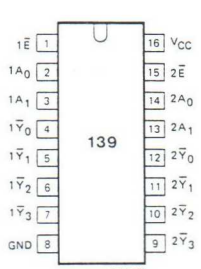


Fig. 1 Pin configuration.

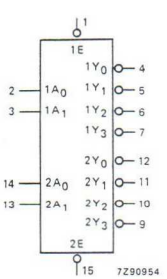


Fig. 2 Logic symbol.

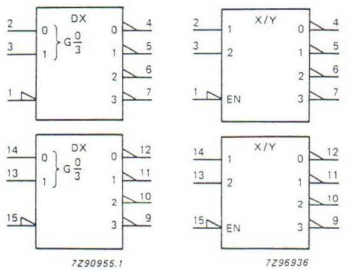


Fig. 3 IEC logic symbol.

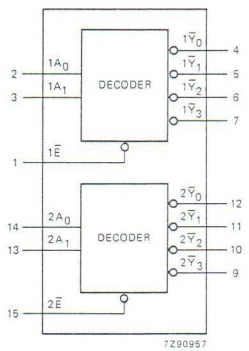


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

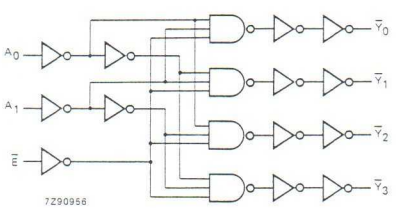


Fig. 5 Logic diagram (one decoder/demultiplexer).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA_n to $\overline{Y}_n$		39 14 11	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to $n\overline{Y}_n$		33 12 10	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1A_n$	0.70
$2A_n$	0.70
$n\bar{E}$	1.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA_n to $\bar{Y}_n$		16	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\bar{E}$ to $n\bar{Y}_n$		16	34		43		51	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

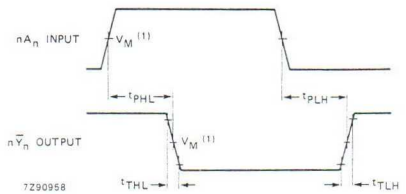


Fig. 6 Waveforms showing the address input (nA$_n$) to output (n$\overline{Y}_n$) propagation delays and the output transition times.

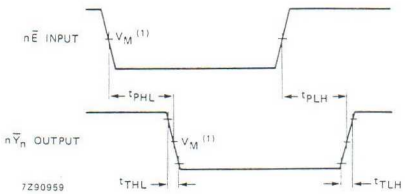


Fig. 7 Waveforms showing the enable input (n$\overline{E}$) to output (n$\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

10-TO-4 LINE PRIORITY ENCODER

FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT147 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT147 9-input priority encoders accept data from nine active LOW inputs ($\overline{A}_0$ to $\overline{A}_8$) and provide a binary representation on the four active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_3$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{A}_8$ having the highest priority.

The devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	15	17	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	33	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 14	$\overline{Y}_0$ to $\overline{Y}_3$	BCD address outputs (active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	$\overline{A}_0$ to $\overline{A}_8$	decimal data inputs (active LOW)
15	n.c.	not connected
16	V_{CC}	positive supply voltage

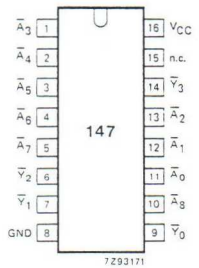


Fig. 1 Pin configuration.

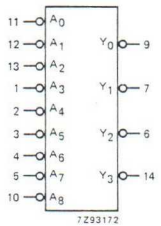


Fig. 2 Logic symbol.

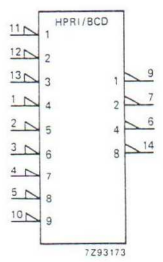


Fig. 3 IEC logic symbol.

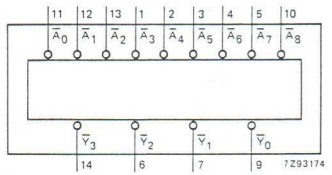


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_8$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

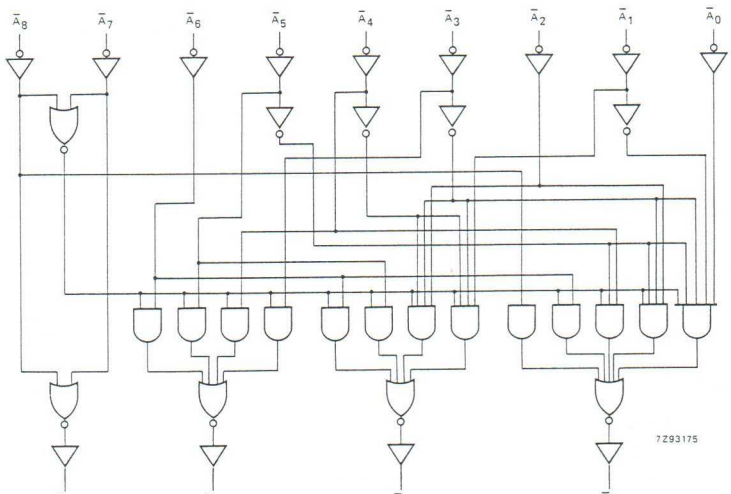


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{A}_3$, $\overline{A}_4$, $\overline{A}_7$, $\overline{A}_8$	1.50
$\overline{A}_5$, $\overline{A}_6$, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{Y}_n$		20	35		44		53	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

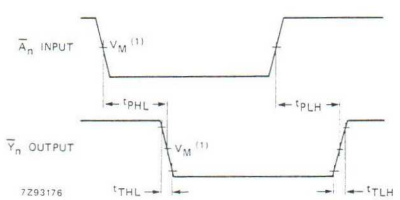


Fig. 6 Waveforms showing the decimal data inputs ($\overline{A}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-INPUT MULTIPLEXER

FEATURES

- True and complement outputs
- Multifunction capability
- Permits multiplexing from n lines to 1 line
- Non-inverting data path
- See the "251" for the 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Y, $\overline{Y}$ S_n to Y, $\overline{Y}$ $\overline{E}$ to Y $\overline{E}$ to $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	 17 19 12 14	 19 20 13 18	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

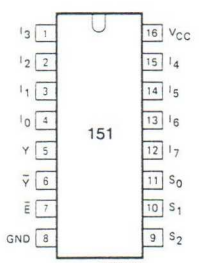


Fig. 1 Pin configuration.

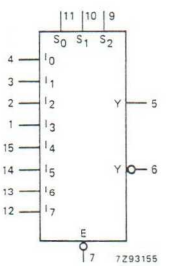


Fig. 2 Logic symbol.

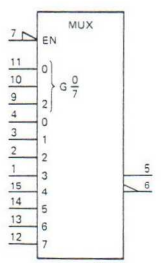


Fig. 3 IEC logic symbol.

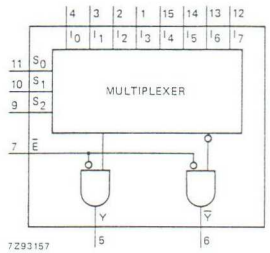


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\bar{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

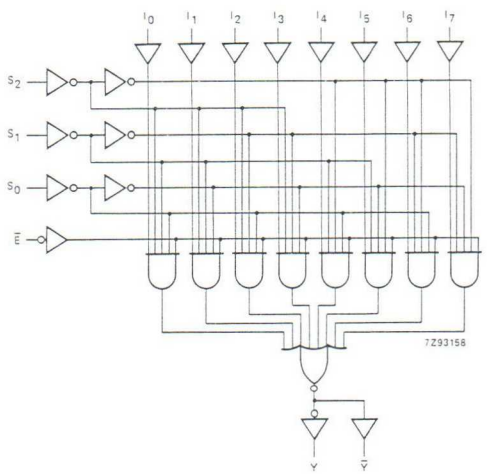


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I_n to Y		52 19 15	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay I_n to $\overline{Y}$		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay S_n to Y		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay S_n to $\overline{Y}$		61 22 18	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to Y		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to $\overline{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	0.45
S_n	1.50
$\overline{E}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y		23	41		51		62	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$		25	43		54		65	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Y		16	29		36		44	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Y}$		21	36		45		54	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

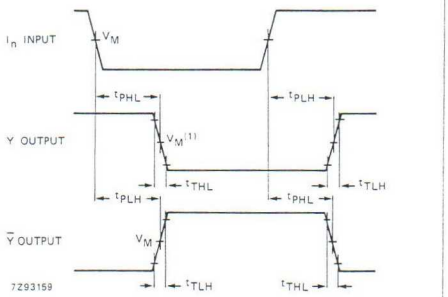


Fig. 6 Waveforms showing the multiplexer input (I_n) to outputs (Y and $\overline{Y}$) propagation delays and the output transition times.

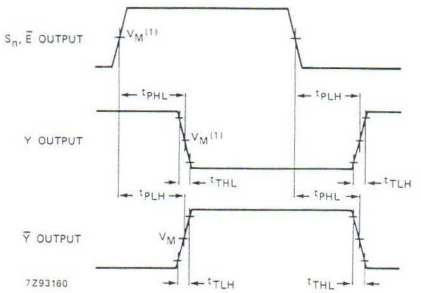


Fig. 7 Waveforms showing the select input (S_n) and enable input ($\overline{E}$) to outputs (Y and $\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-INPUT MULTIPLEXER

FEATURES

- Non-inverting outputs
- Separate enable for each output
- Common select inputs
- See '253" for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{E}$, $2\overline{E}$) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:

$$1Y = 1\overline{E}.(1I_0.\overline{S_1}.\overline{S_0}+1I_1.\overline{S_1}.S_0+ +1I_2.S_1.\overline{S_0}+1I_3.S_1.S_0)$$

$$2Y = 2\overline{E}.(2I_0.\overline{S_1}.\overline{S_0}+2I_1.\overline{S_1}.S_0+ +2I_2.S_1.\overline{S_0}+2I_3.S_1.S_0)$$

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY S_n to nY $n\overline{E}$ to nY	C_L = 15 pF V_{CC} = 5 V	14 15 10	16 17 11	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
7	1Y	multiplexer output from source 1
8	GND	ground (0 V)
9	2Y	multiplexer output from source 2
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

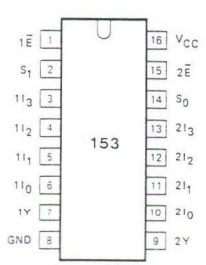


Fig. 1 Pin configuration.

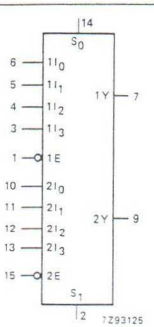


Fig. 2 Logic symbol.

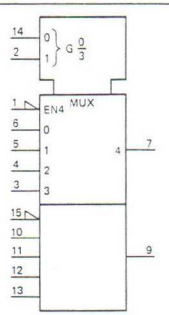


Fig. 3 IEC logic symbol.

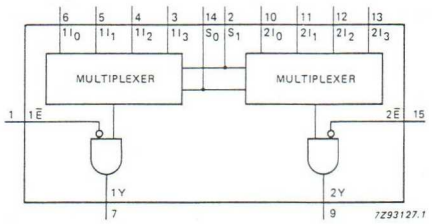


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The "153" is similar to the "253" but has standard outputs.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\bar{E}$	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

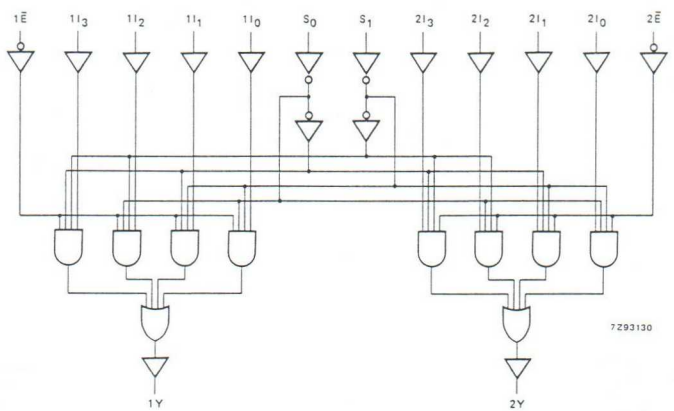


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to nY		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1I_n$, $2I_n$	0.45
$n\overline{E}$	0.60
S_n	1.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay $1I_n$ to nY; $2I_n$ to nY		19	34		43		51	ns	4.5	Fig. 6
t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		13	24		30		36	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay S_n to nY		20	34		43		51	ns	4.5	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay $n\overline{E}$ to nY		14	27		34		41	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

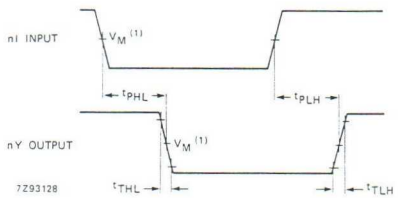


Fig. 6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.

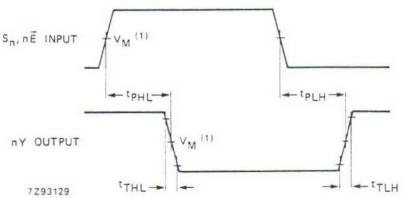


Fig. 7 Waveforms showing the select input (S_0, S_1) and the output enable input ($\bar{E}$) to output (1Y, 2Y) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-TO-16 LINE DECODER/DEMULTIPLEXER

FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.
The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, $\overline{E}_n$ to $\overline{Y}_n$	C_L = 15 pF V_{CC} = 5 V	11	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	60	60	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\overline{Y}_0$ to $\overline{Y}_{15}$	outputs (active LOW)
18, 19	$\overline{E}_0$, $\overline{E}_1$	enable inputs (active LOW)
12	GND	ground (0 V)
23, 22, 21, 20	A_0 to A_3	address inputs
24	V_{CC}	positive supply voltage

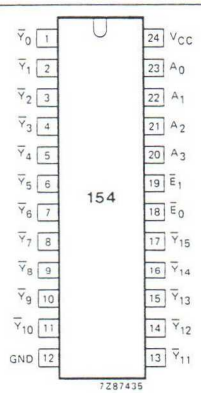


Fig. 1 Pin configuration.

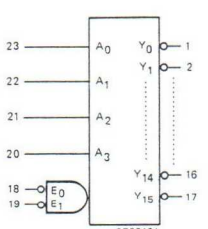


Fig. 2 Logic symbol.

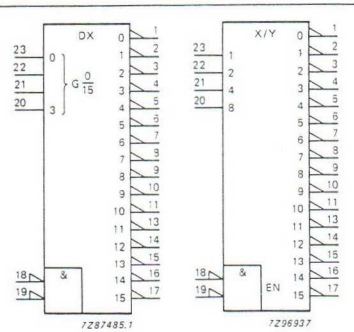


Fig. 3 IEC logic symbol.

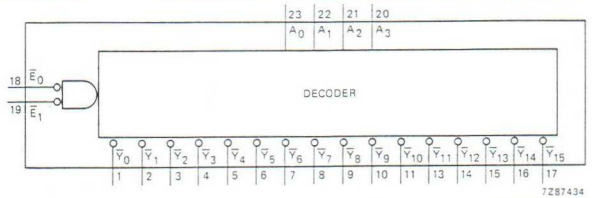


Fig. 4 Functional diagram.

FUNCTION TABLE

		INPUTS				OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$	$\overline{Y}_{10}$	$\overline{Y}_{11}$	$\overline{Y}_{12}$	$\overline{Y}_{13}$	$\overline{Y}_{14}$	$\overline{Y}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = HIGH voltage level L = LOW voltage level X = don't care

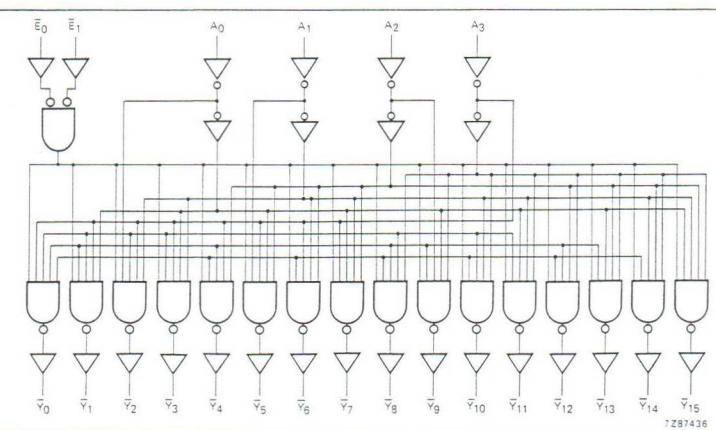


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.0
$\overline{E}_n$	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		16	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		15	32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

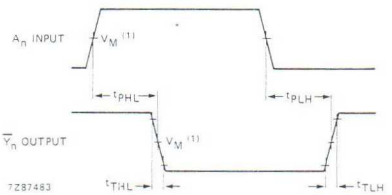


Fig. 6 Waveforms showing the address input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

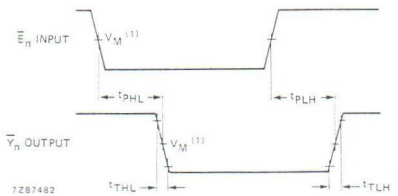


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

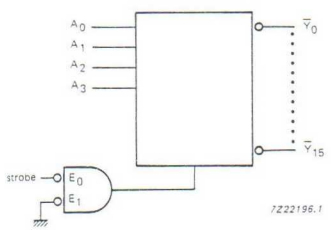


Fig. 8 1-of-16 decoder; LOW level output is selected.

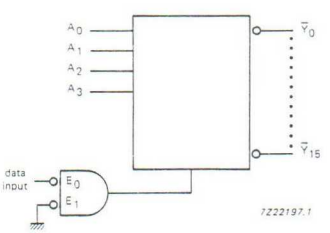


Fig. 9 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.

QUAD 2-INPUT MULTIPLEXER

FEATURES

- Non-inverting data path
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is usefull for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$1Y = \overline{E}.(1I_1.S + 1I_0.\overline{S})$

$2Y = \overline{E}.(2I_1.S + 2I_0.\overline{S})$

$3Y = \overline{E}.(3I_1.S + 3I_0.\overline{S})$

$4Y = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

The "157" is identical to the "158" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY $\overline{E}$ to nY S to nY	C_L = 15 pF V_{CC} = 5 V	11 11 12	13 12 19	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	70	70	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

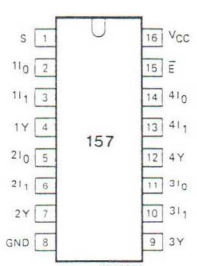


Fig. 1 Pin configuration.

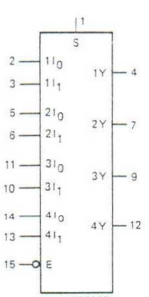


Fig. 2 Logic symbol.

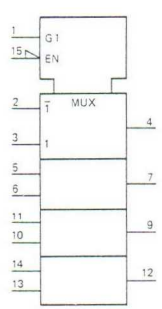


Fig. 3 IEC logic symbol.

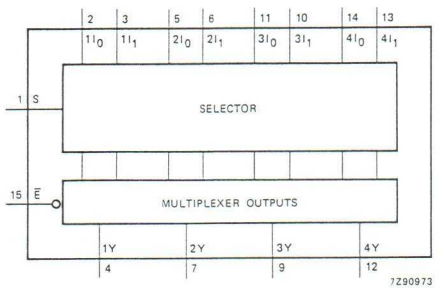


Fig. 4 Functional diagram.

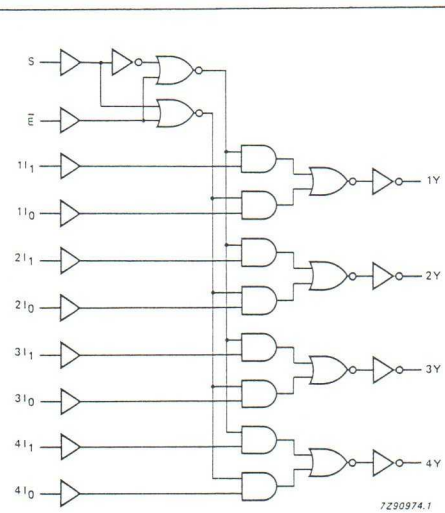


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nI_0	1.00
nI_1	1.00
$\overline{E}$	0.60
S	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		16	27		34		41	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY		15	26		33		39	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY		22	37		46		56	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

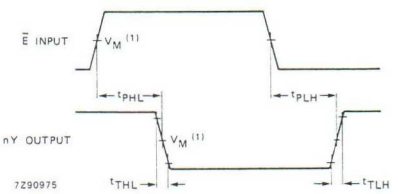


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output (nY) propagation delays and the output transition times.

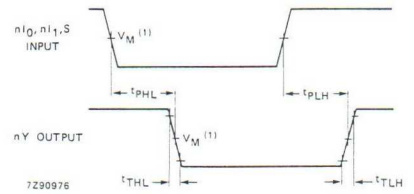


Fig. 7 Waveforms showing the data inputs (nI_n) and common data select input (S) to output (nY) propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT MULTIPLEXER; INVERTING

FEATURES

- Inverting data path
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input ($\overline{E}$) is active LOW.

When $\overline{E}$ is HIGH, all the outputs ($1\overline{Y}$ to $4\overline{Y}$) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$1\overline{Y} = \overline{E}.(1I_1.S + 1I_0.\overline{S})$
$2\overline{Y} = \overline{E}.(2I_1.S + 2I_0.\overline{S})$
$3\overline{Y} = \overline{E}.(3I_1.S + 3I_0.\overline{S})$
$4\overline{Y} = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

The "158" is identical to the "157" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$ $\overline{E}$ to $n\overline{Y}$ S to $n\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	12 14 14	13 16 16	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	$1\overline{Y}$ to $4\overline{Y}$	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

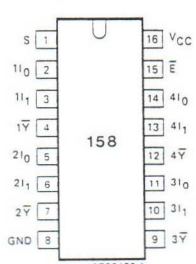


Fig. 1 Pin configuration.

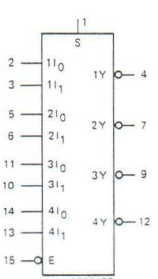


Fig. 2 Logic symbol.

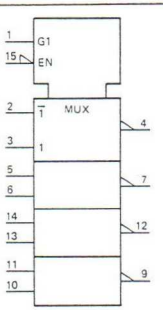


Fig. 3 IEC logic symbol.

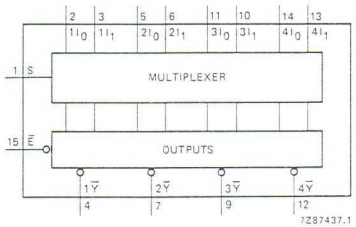


Fig. 4 Functional diagram.

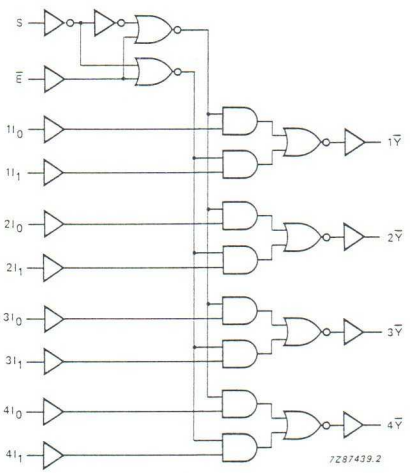


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nI_0	0.40
nI_1	0.40
S	2.80
$\overline{E}$	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$		16	30		38		45	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$		19	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$		19	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

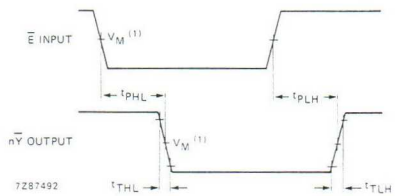


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output ($n\overline{Y}$) propagation delays and the output transition times.

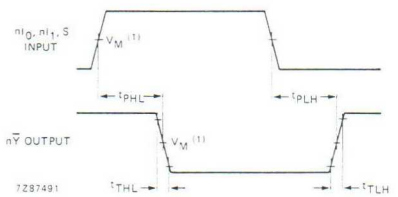


Fig. 7 Waveforms showing the data input (nI_0, nI_1) to output ($n\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; ASYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT160 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 19 21 21 21 14	 21 24 23 26 14	 ns ns ns ns ns
t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC		 19 21 14	 21 20 7	 ns ns ns
f_{max}	maximum clock frequency		61	31	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	39	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

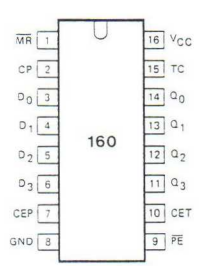


Fig. 1 Pin configuration.

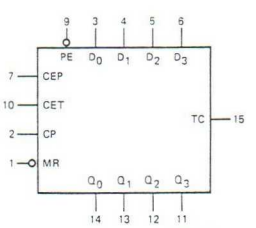


Fig. 2 Logic symbol.

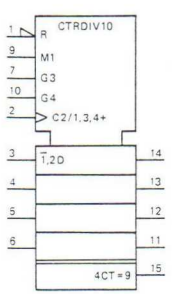


Fig. 3 IEC logic symbol.

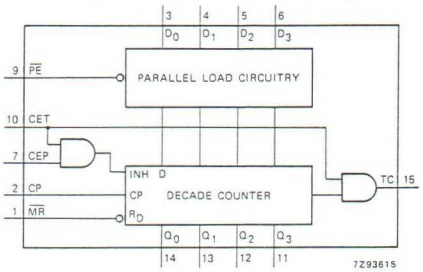


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H H	↑ ↑	X X	X X	l l	l h	L H	L *
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H H	X X	l X	X l	h h	X X	q_n q_n	* L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\,(\text{CP to TC}) + t_{SU}\,(\text{CEP to CP})}$$

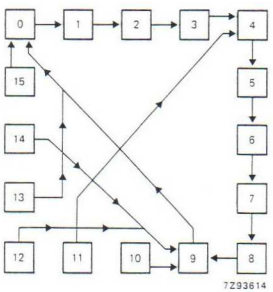


Fig. 5 State diagram.

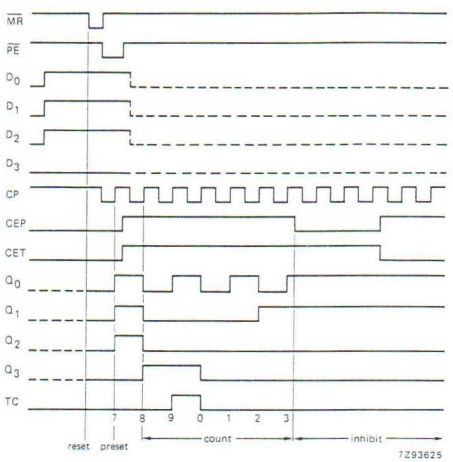


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

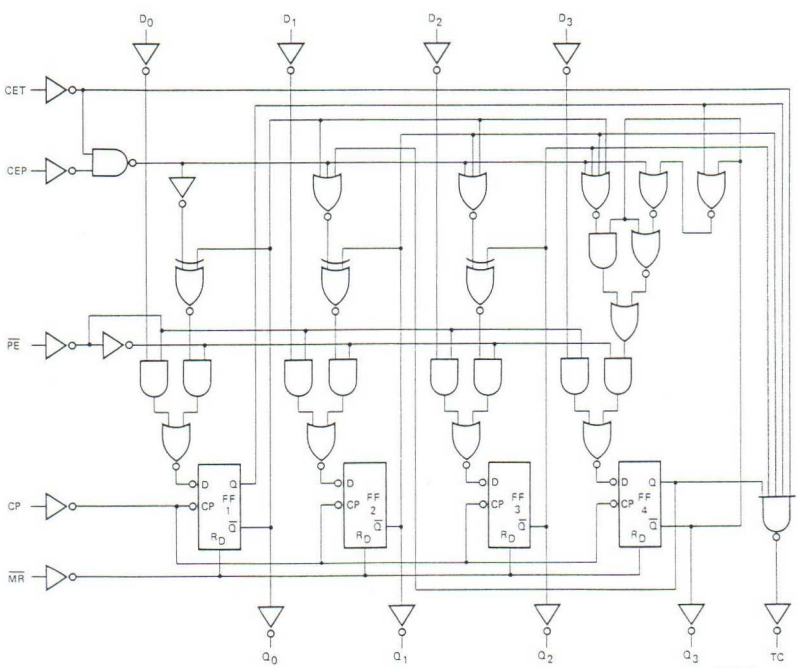


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		69 25 20	215 43 31		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width LOW	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	135 27 23	41 15 12		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time CEP, CET to CP	200 40 34	63 23 18		250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
t_h	hold time $\overline{PE}$ to CP	0 0 0	−41 −15 −12		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
t_h	hold time CEP, CET to CP	0 0 0	−58 −21 −17		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency	6.0 30 35	18 55 66		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	1.05
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		25	43		54		65	ns	4.5	Fig. 8
t_{PHL}	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
t_{PLH}	propagation delay CP to TC		23	39		49		59	ns	4.5	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		27	50		63		75	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC		30	50		63		75	ns	4.5	Fig. 9
t_{PHL}	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
t_{PLH}	propagation delay CET to TC		9	17		21		26	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 8
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	20	9		25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	18	10		25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	30	18		44		53		ns	4.5	Fig. 11
t_{su}	set-up time CEP, CET to CP	50	30		63		75		ns	4.5	Fig. 12

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to CP	0	−8		0		0		ns	4.5	Figs 11 and 12
t_h	hold time $\overline{PE}$ to CP	0	−13		0		0		ns	4.5	Figs 11 and 12
t_h	hold time CEP, CET to CP	0	−21		0		0		ns	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency	16	28		13		11		MHz	4.5	Fig. 8

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; ASYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 19 21 20 20 10	 20 24 25 26 14	 ns ns ns ns ns
f_{max}	maximum clock frequency		44	45	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

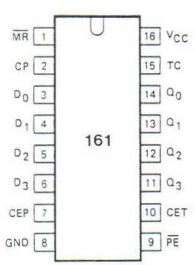


Fig. 1 Pin configuration.

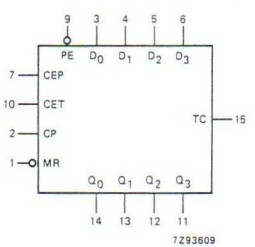


Fig. 2 Logic symbol.

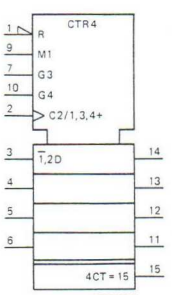


Fig. 3 IEC logic symbol.

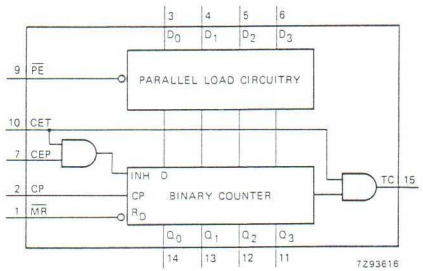


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold	H	X	l	X	h	X	q_n	*
(do nothing)	H	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\,(\text{CP to TC}) + t_{SU}\,(\text{CEP to CP})}$$

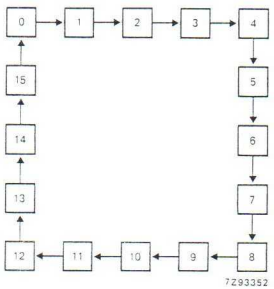


Fig. 5 State diagram.

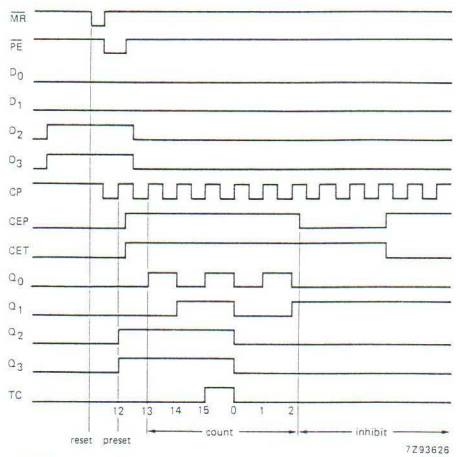


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

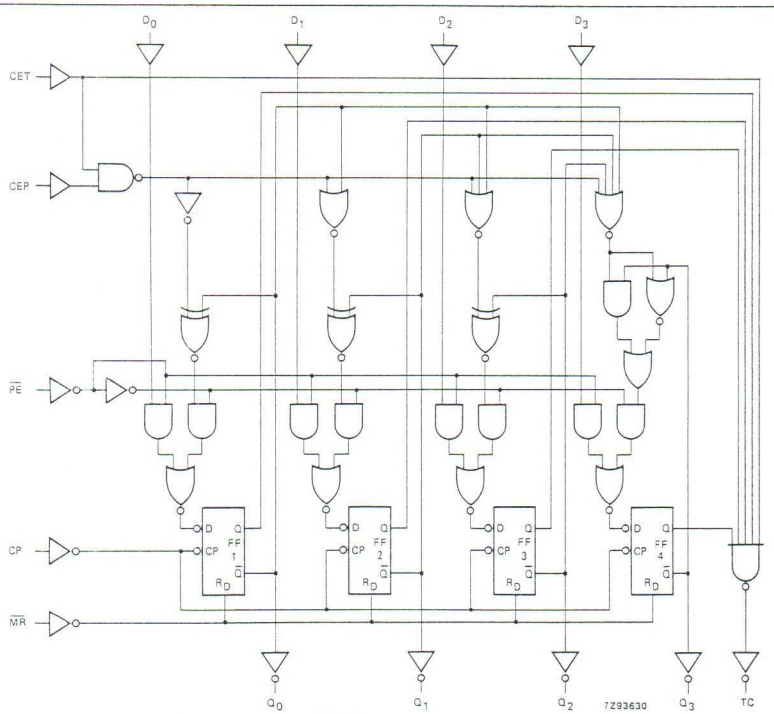


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width; LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time CEP, CET to CP	170 34 29	47 17 14		215 43 37		255 51 43		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency	4.6 23 27	13 40 48		3.6 18 21		3.0 15 18		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	1.10
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	0.75
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		23	43		54		65	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		29	46		58		69	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC		30	51		64		77	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
t_W	master reset pulse width; LOW	20	10		25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	20	6		25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	18	8		23		27		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	30	17		38		45		ns	4.5	Fig. 11
t_{su}	set-up time CEP, CET to CP	40	17		50		60		ns	4.5	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0	−7		0		0		ns	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency	23	41		18		15		MHz	4.5	Fig. 8

AC WAVEFORMS

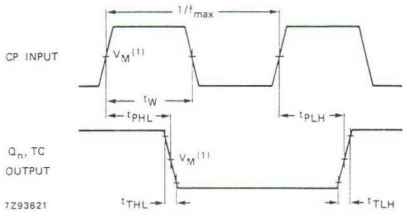


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

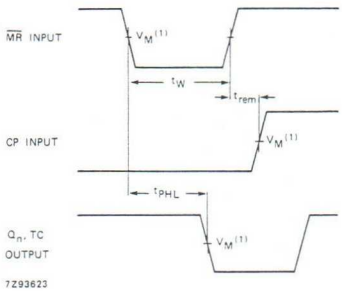


Fig. 9 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal time.

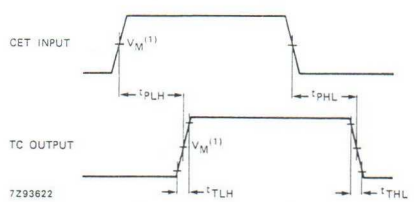


Fig. 10 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

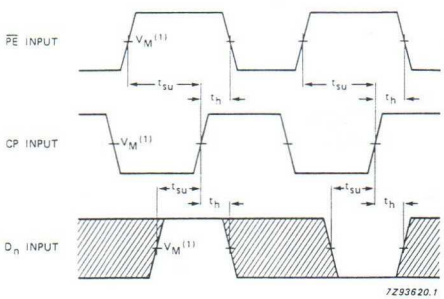


Fig. 11 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input $\overline{PE}$.

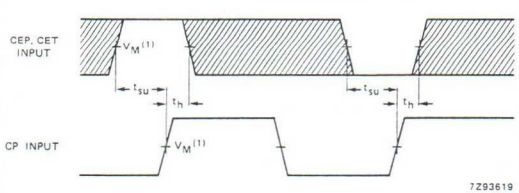


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT162 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "162" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 19 21 11	 20 26 15	 ns ns ns
t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC		 19 21 11	 20 19 10	 ns ns ns
f_{max}	maximum clock frequency		63	32	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	37	37	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

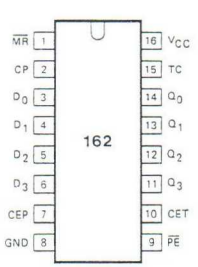


Fig. 1 Pin configuration.

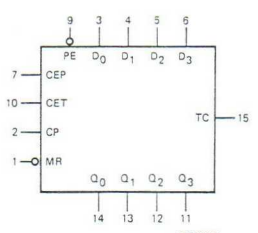


Fig. 2 Logic symbol.

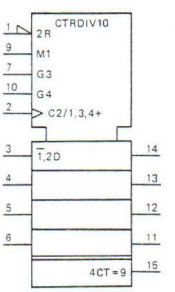


Fig. 3 IEC logic symbol.

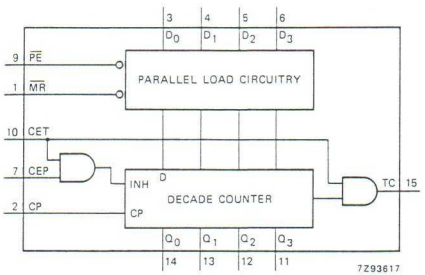


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\,(\text{CP to TC}) + t_{SU}\,(\text{CEP to CP})}$$

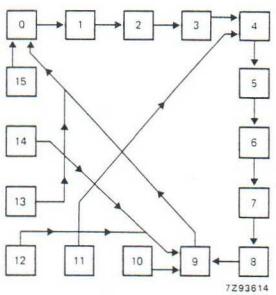


Fig. 5 State diagram.

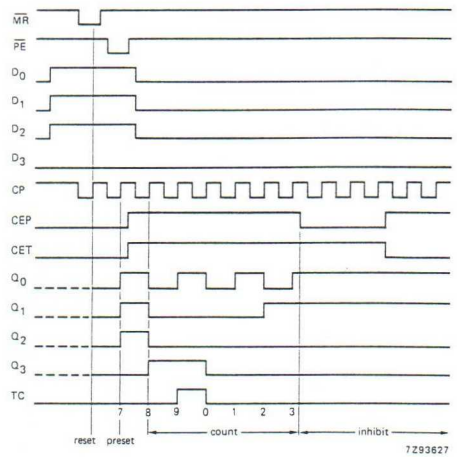


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

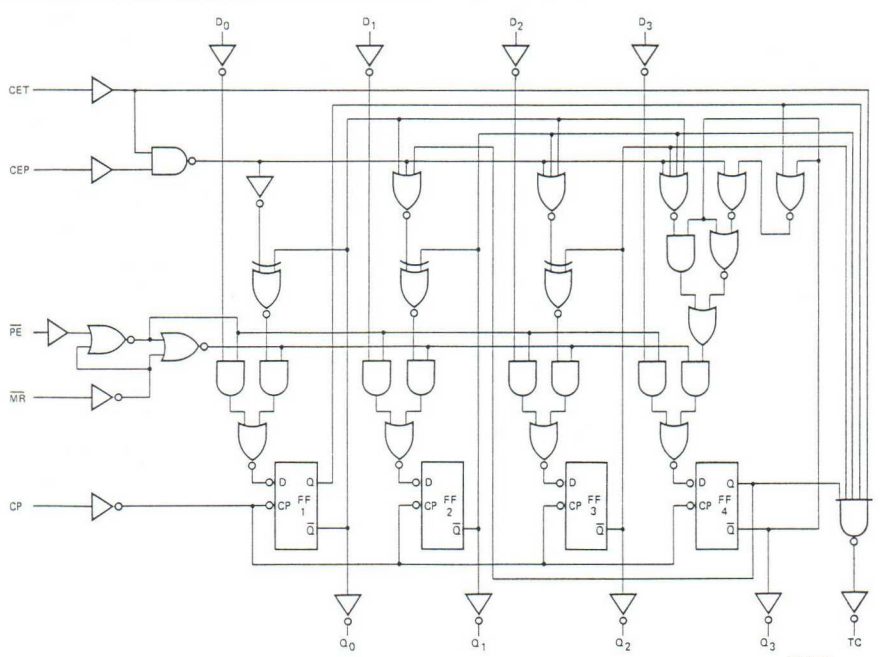


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		58 21 17	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CET to TC		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	135 27 23	39 14 11		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time CEP, CET to CP	200 40 34	69 25 20		250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	1.05
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		24	43		54		65	ns	4.5	Fig. 8
t_{PHL}	propagation delay CP to TC		30	51		64		77	ns	4.5	Fig. 8
t_{PLH}	propagation delay CP to TC		22	45		56		68	ns	4.5	Fig. 8
t_{PHL}	propagation delay CET to TC		18	35		44		53	ns	4.5	Fig. 9
t_{PLH}	propagation delay CET to TC		12	24		30		36	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	20	9		25		30		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	35	16		44		53		ns	4.5	Fig. 10
t_{su}	set-up time CEP, CET to CP	40	23		50		60		ns	4.5	Fig. 12
t_{su}	set-up time $\overline{MR}$ to CP	20	12		25		30		ns	4.5	Fig. 11
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0	−10		0		0		ns	4.5	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	17	29		14		11		MHz	4.5	Fig. 8

AC WAVEFORMS

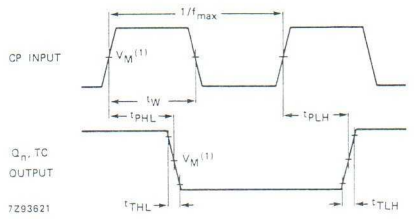


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

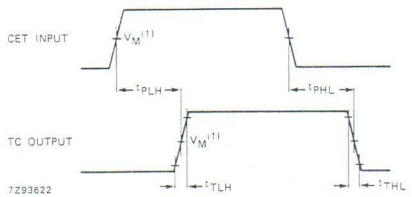


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

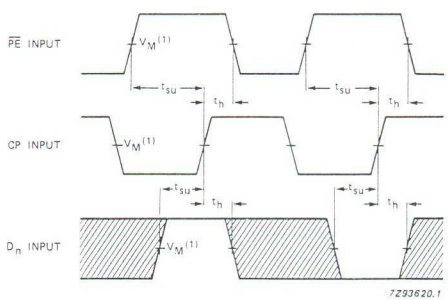


Fig. 10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).

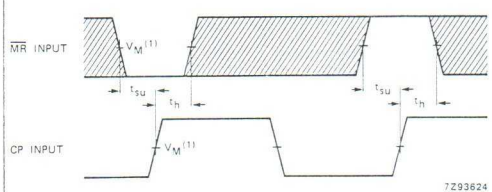


Fig. 11 Waveforms showing the $\overline{MR}$ set-up and hold times.

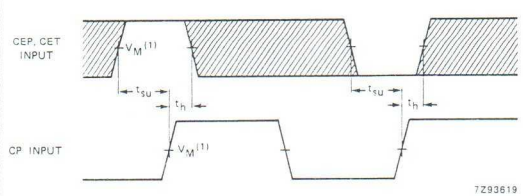


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

The HC/HCT162 facilitate designing counters of any modulus with minimal external logic.
The output is glitch-free due to the synchronous reset.

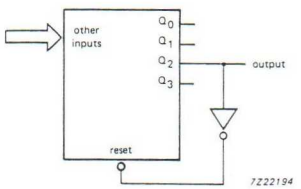


Fig. 13 Modulo-5 counter.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 17 21 11	 20 25 14	 ns ns ns
f_{max}	maximum clock frequency		51	50	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

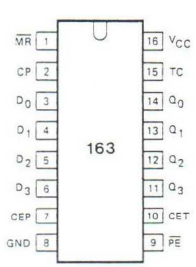


Fig. 1 Pin configuration.

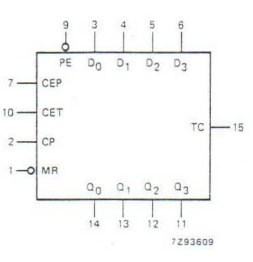


Fig. 2 Logic symbol.

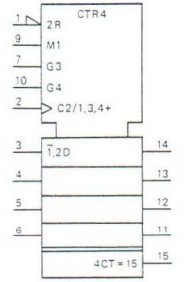


Fig. 3 IEC logic symbol.

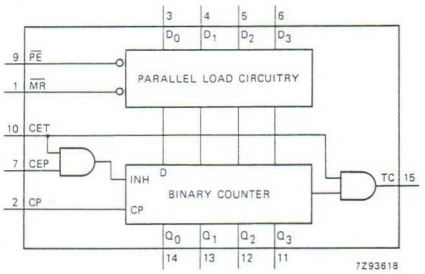


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd)

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\,(\text{CP to TC}) + t_{SU}\,(\text{CEP to CP})}$$

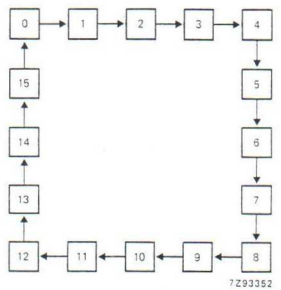


Fig. 5 State diagram.

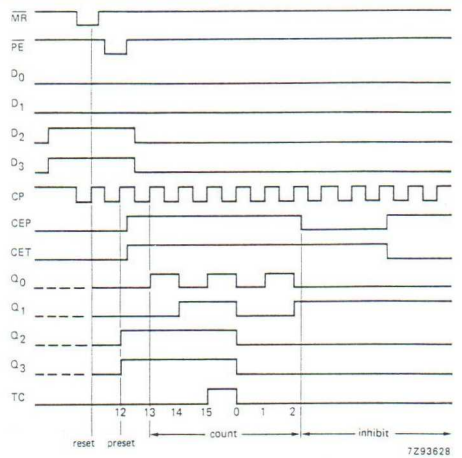


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

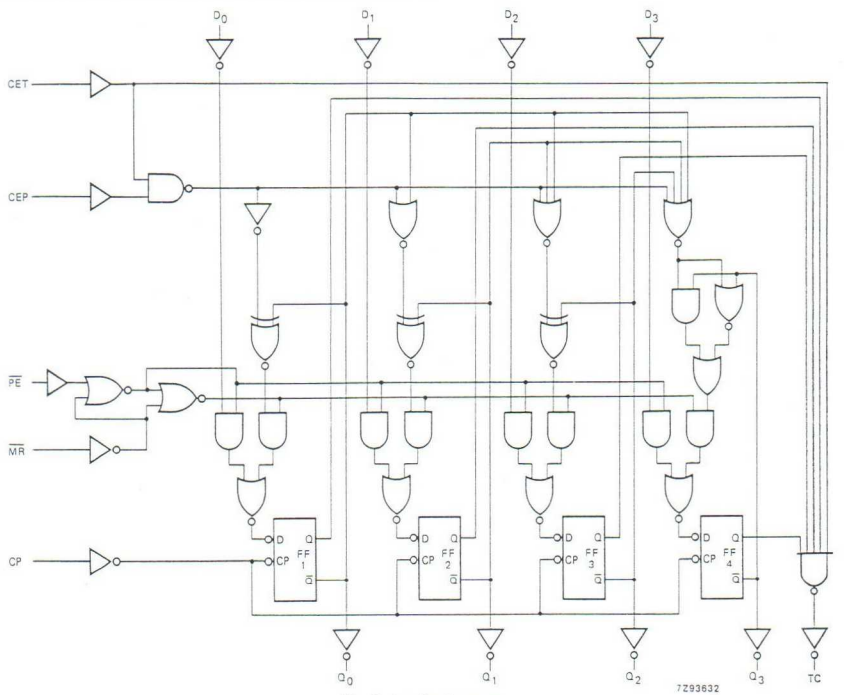


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		55 20 16	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		320 65 55	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CET to TC		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time CEP, CET to CP	175 35 30	58 21 17		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	5 27 32	15 46 55		4 22 26		4 18 21		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	1.10
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	0.75
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		23	39		49		59	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC		29	49		61		74	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CET to TC		17	32		44		48	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	20	9		25		30		ns	4.5	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	20	11		25		30		ns	4.5	Fig. 10
t_{su}	set-up time CEP, CET to CP	40	24		50		60		ns	4.5	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0	−5		0		0		ns	4.5	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	26	45		21		17		MHz	4.5	Fig. 8

AC WAVEFORMS

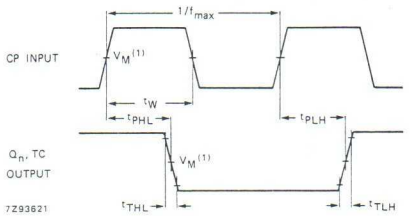


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

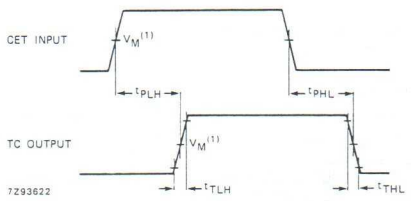


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

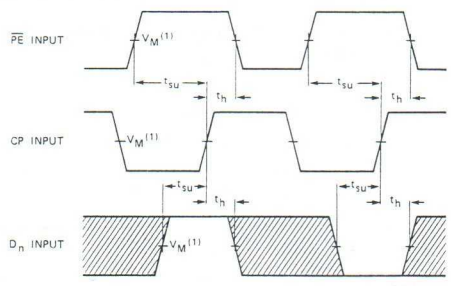


Fig. 10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).

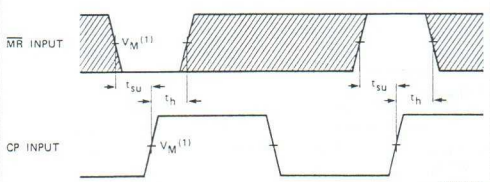


Fig. 11 Waveforms showing the $\overline{MR}$ set-up and hold times.

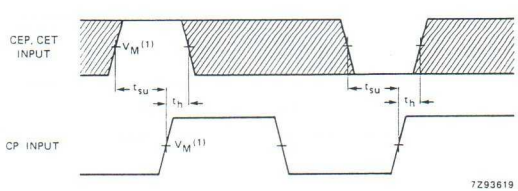


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

The HC/HCT163 facilitate designing counters of any modulus with minimal external logic.
The output is glitch-free due to the synchronous reset.

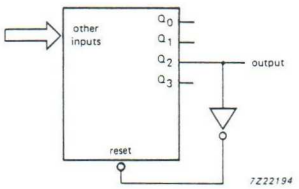


Fig. 13 Modulo-5 counter.

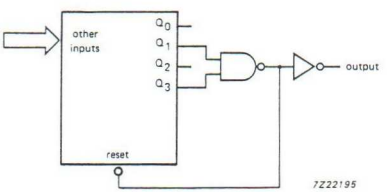


Fig. 14 Modulo-11 counter.

8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT164 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages.

Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	12 11	14 16	ns ns
f_{max}	maximum clock frequency		78	61	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D_{sa}, D_{sb}	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V_{CC}	positive supply voltage

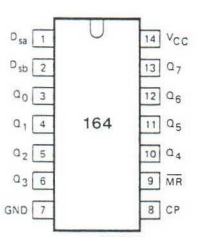


Fig. 1 Pin configuration.

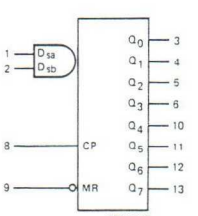


Fig. 2 Logic symbol.

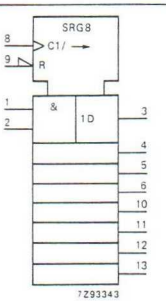


Fig. 3 IEC logic symbol.

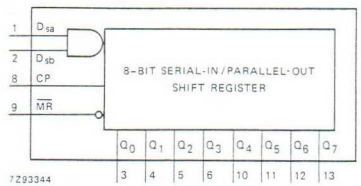


Fig. 4 Functional diagram.

APPLICATIONS

- Serial data transfer

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
reset (clear)	L	X	X	X	L	L — L
shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

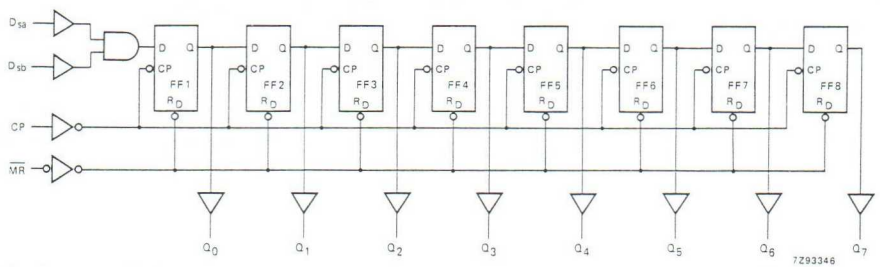


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		41 15 12	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_{sa}, D_{sb} to CP	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_{sa}, D_{sb} to CP	4 4 4	−6 −2 −2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35	23 71 85		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_{sa}, D_{sb}	0.25
CP	0.60
$\overline{MR}$	0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		17	36		45		54	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		19	38		48		57	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18	7		23		27		ns	4.5	Fig. 6
t_W	master reset pulse width; LOW	18	10		23		27		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	16	7		20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_{sa}, D_{sb} to CP	12	6		15		18		ns	4.5	Fig. 8
t_h	hold time D_{sa}, D_{sb} to CP	4	−2		4		4		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

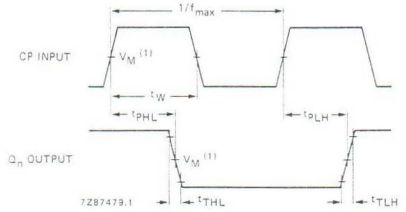


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

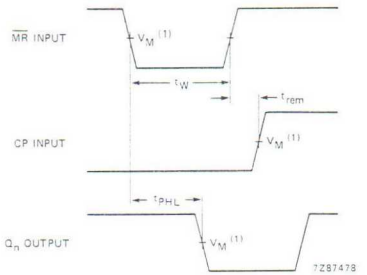


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

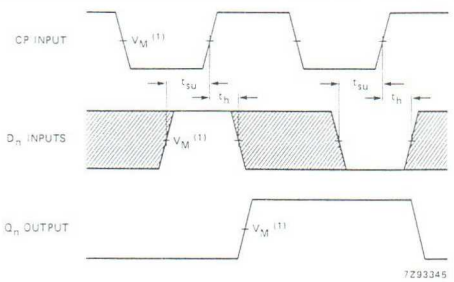


Fig. 8 Waveforms showing the data set-up and hold times for D_n inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q_7 and $\overline{Q_7}$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously.

When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is activated.

APPLICATIONS

- Parallel-to-serial data conversion

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_7, $\overline{Q_7}$ $\overline{PL}$ to Q_7, $\overline{Q_7}$ D_7 to Q_7, $\overline{Q_7}$	C_L = 15 pF V_{CC} = 5 V	 16 15 11	 14 17 11	 ns ns ns
f_{max}	maximum clock frequency		56	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
7	$\overline{Q_7}$	complementary output from the last stage
9	Q_7	serial output from the last stage
2	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
10	D_S	serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	parallel data inputs
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	positive supply voltage

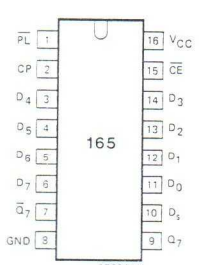


Fig. 1 Pin configuration.

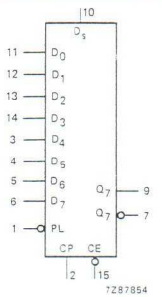


Fig. 2 Logic symbol.

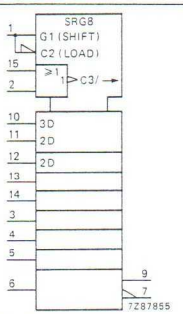


Fig. 3 IEC logic symbol.

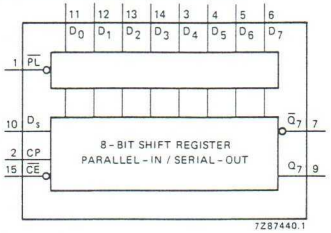


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_s	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q}_7$
parallel load	L L	X X	X X	X X	L H	L H	L - L H - H	L H	H L
serial shift	H H	L L	↑ ↑	l h	X X	L H	q_0-q_5 q_0-q_5	q_6 q_6	$\overline{q}_6$ $\overline{q}_6$
hold "do nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	q_7

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

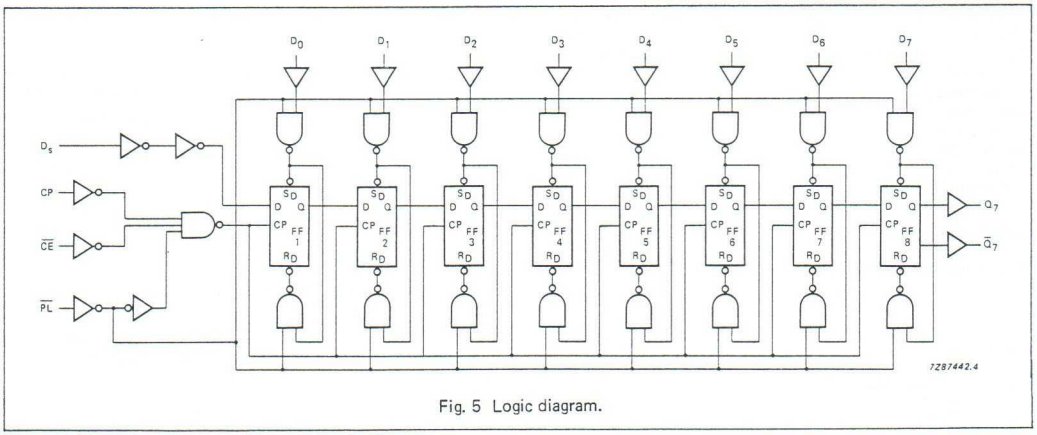


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_7 to Q_7, $\overline{Q}_7$		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	parallel load pulse width; LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{PL}$ to CP, $\overline{CE}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_s to CP, $\overline{CE}$	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to $\overline{PL}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_s to CP, $\overline{CE}$ D_n to $\overline{PL}$	5 5 5	6 2 2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time $\overline{CE}$ to CP CP to $\overline{CE}$	5 5 5	−17 −6 −5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6 30 35	17 51 61		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
D_s	0.35
$\overline{CP}$	0.65
$\overline{CE}$	0.65
$\overline{PL}$	0.65

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$		17	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$		20	40		50		60	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_7 to Q_7, $\overline{Q}_7$		14	28		35		42	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 6
t_W	parallel load pulse width; LOW	20	9		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{PL}$ to CP, $\overline{CE}$	20	8		25		30		ns	4.5	Fig. 7
t_{su}	set-up time D_s to CP, $\overline{CE}$	20	2		25		30		ns	4.5	Fig. 9
t_{su}	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	20	7		25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to $\overline{PL}$	20	10		25		30		ns	4.5	Fig. 10
t_h	hold time D_s to CP, $\overline{CE}$; D_n to $\overline{PL}$	7	−1		9		11		ns	4.5	Fig. 9
t_h	hold time $\overline{CE}$ to CP, CP to $\overline{CE}$	0	−7		0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig. 6

AC WAVEFORMS

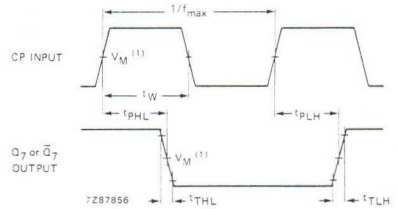


Fig. 6 Waveforms showing the clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

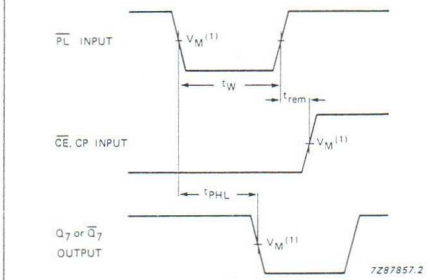


Fig. 7 Waveforms showing the parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.

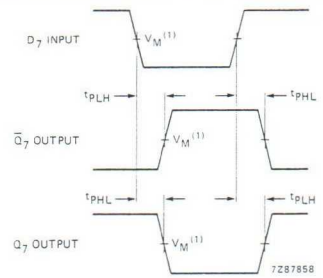


Fig. 8 Waveforms showing the data input (D_n) to output (Q_7 or $\overline{Q}_7$) propagation delays when $\overline{PL}$ is LOW.

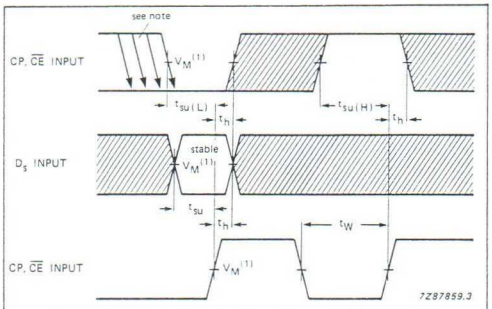


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_s) to the clock (CP) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).

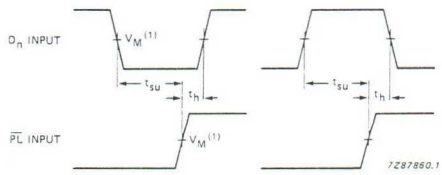


Fig. 10 Waveforms showing the set-up and hold times from the data inputs (D_n) to the parallel load input ($\overline{PL}$).

Note to Figs 6 and 7

The changing to output assumes internal Q_6 opposite state from Q_7.

Note to Fig. 9

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- For asynchronous parallel data load see "165"
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by an active LOW parallel enable ($\overline{PE}$) input. When $\overline{PE}$ is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into the internal bit position Q_0 from serial data input (D_s), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition.

This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_s input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP is HIGH for predictable operation. A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_7 $\overline{MR}$ to Q_7	C_L = 15 pF V_{CC} = 5 V	15 14	20 19	ns ns
f_{max}	maximum clock frequency		63	50	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	41	41	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	D_s	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D_0 to D_7	parallel data inputs
6	$\overline{CE}$	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
13	Q_7	serial output from the last stage
15	$\overline{PE}$	parallel enable input (active LOW)
16	V_{CC}	positive supply voltage

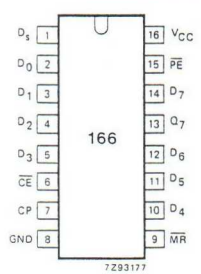


Fig. 1 Pin configuration.

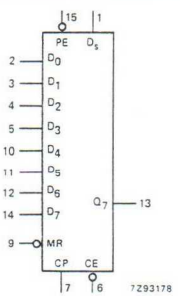


Fig. 2 Logic symbol.

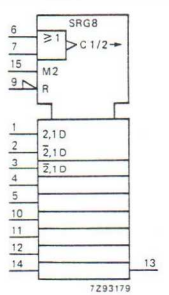


Fig. 3 IEC logic symbol.

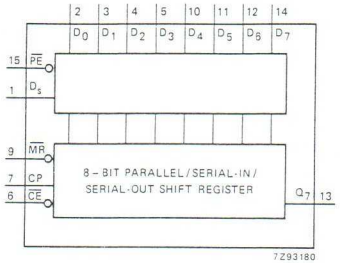


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_s	D_0-D_7	Q_0	Q_1-Q_6	Q_7
parallel load	l	l	↑	X	l - l	L	L - L	L
	l	l	↑	X	h - h	H	H - H	H
serial shift	h	l	↑	l	X - X	L	q_0 - q_5	q_6
	h	l	↑	h	X - X	H	q_0 - q_5	q_6
hold "do nothing"	X	h	X	X	X - X	q_0	q_1 - q_6	q_7

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

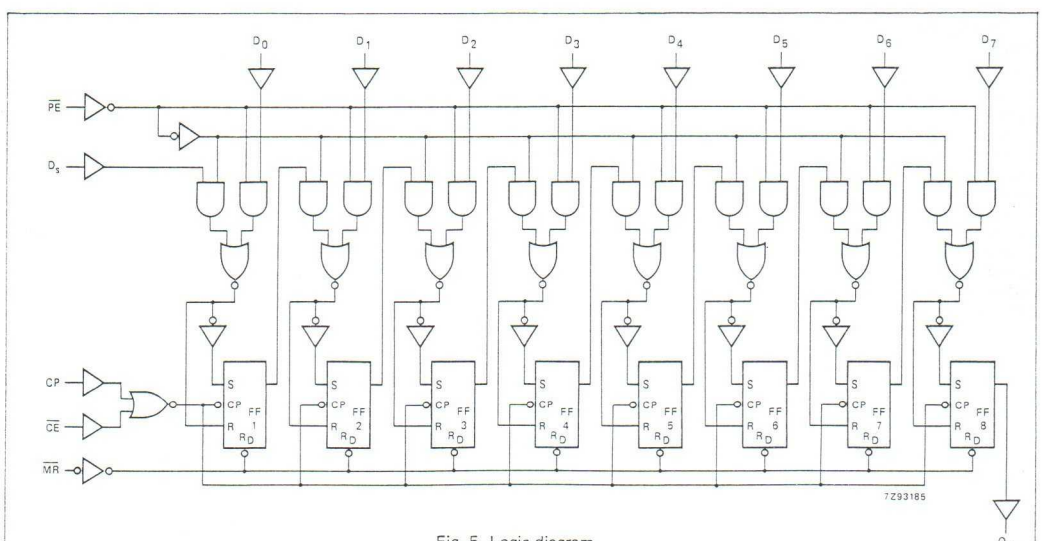


Fig. 5 Logic diagram.

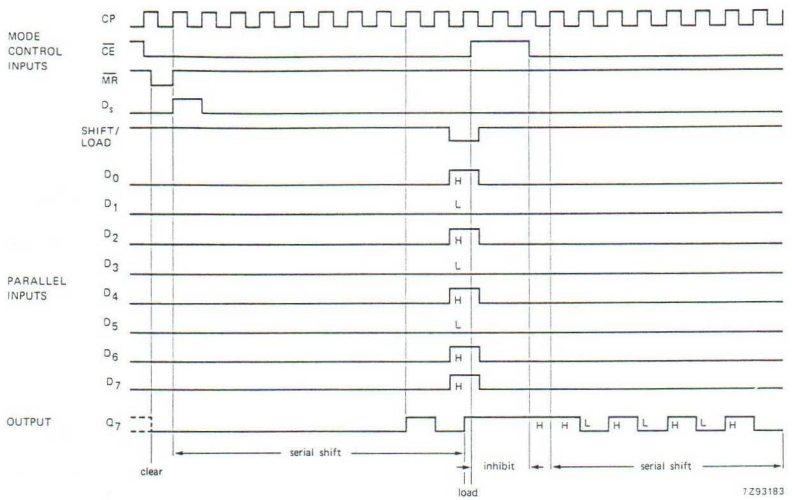


Fig. 6 Typical clear, shift, load, inhibit, and shift sequences.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_7		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_7		47 17 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n, $\overline{CE}$ to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time $\overline{PE}$ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n, $\overline{CE}$ to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time $\overline{PE}$ to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_0 to D_7	0.35
D_S	0.35
$\overline{CP}$	0.80
$\overline{CE}$	0.80
$\overline{MR}$	0.40
$\overline{PE}$	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_7		23	40		50		60	ns	4.5	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_7		22	40		50		60	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	20	9		25		30		ns	4.5	Fig. 7
t_W	master reset pulse width LOW	25	11		31		38		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	0	−7		0		0		ns	4.5	Fig. 8
t_{su}	set-up time D_n, $\overline{CE}$ to CP	16	8		20		24		ns	4.5	Fig. 9
t_{su}	set-up time $\overline{PE}$ to CP	30	15		38		45		ns	4.5	Fig. 8
t_h	hold time D_n, $\overline{CE}$ to CP	0	−3		0		0		ns	4.5	Fig. 9
t_h	hold time $\overline{PE}$ to CP	0	−13		0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse width	25	45		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

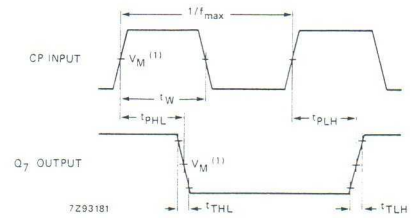


Fig. 7 Waveforms showing the clock (CP) to output (Q_7) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

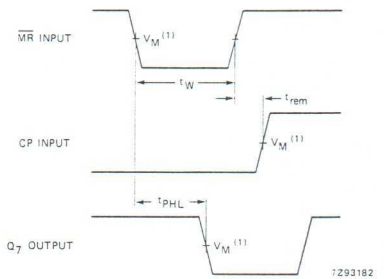


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_7) propagation delay and the master reset to clock (CP) removal time.

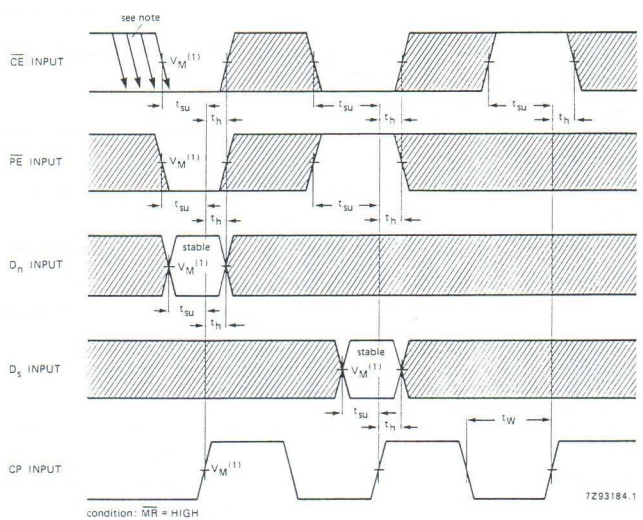


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D_S), the data inputs (D_n), the clock enable input (LOW $\overline{CE}$), the clock enable input $\overline{CE}$ and the parallel enable input to the clock (CP).

Note to Fig. 7

The changing to output assumes internal Q_6 opposite state from Q_7.

Note to Figs 7, 8 and 9

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the function table.

Note to Fig. 9

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.
HCT: $V_M = 1.3$ V; V_I = GND to 3 V.

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n MR to Q_n	C_L = 15 pF V_{CC} = 5 V	17 13	17 17	ns ns
f_{max}	maximum clock frequency		88	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

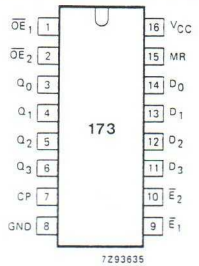


Fig. 1 Pin configuration.

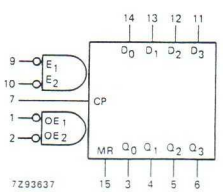


Fig. 2 Logic symbol.

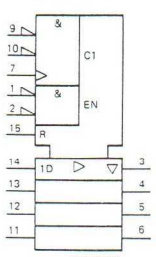


Fig. 3 IEC logic symbol.

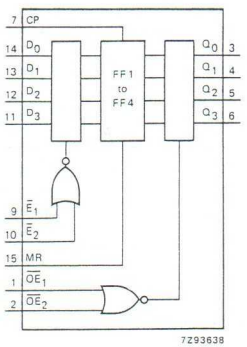


Fig. 4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L L	↑ ↑	l l	l l	l h	L H
hold (no change)	L L	X X	h X	X h	X X	q_n q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L H	L L	L L	L H	L H	L H	L H
disabled	X X	H X	X H	Z Z	Z Z	Z Z	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

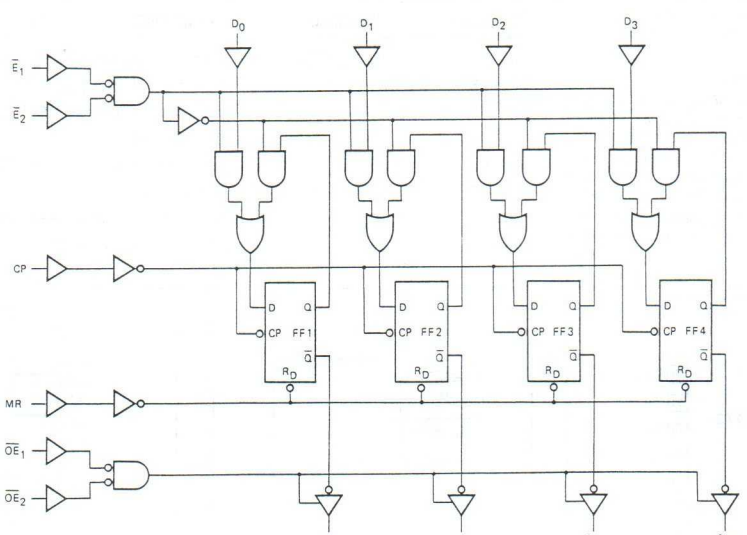


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR to Q_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time MR to CP	60 12 10	−8 −3 −2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to CP	1 1 1	−11 −4 −3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$, $\overline{OE}_2$	0.50
MR	0.60
$\overline{E}_1$, $\overline{E}_2$	0.40
D_n	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		20	40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR to Q_n		20	37		46		56	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		20	35		44		53	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		19	30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		5	12		15		19	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width; HIGH	15	6		19		22		ns	4.5	Fig. 7
t_{rem}	removal time MR to CP	12	−2		15		18		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	22	13		28		33		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	12	7		15		18		ns	4.5	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0	−6		0		0		ns	4.5	Fig. 9
t_h	hold time D_n to CP	0	−3		0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

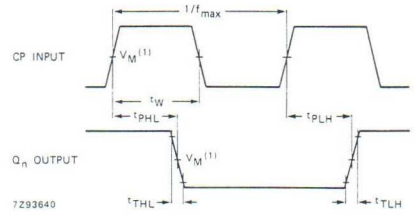


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

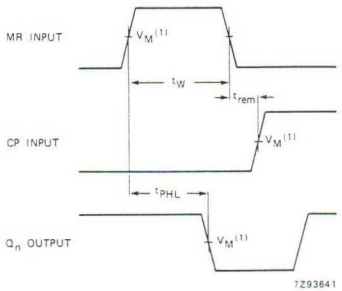


Fig. 7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

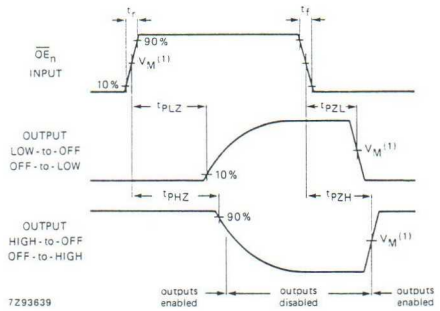


Fig. 8 Waveforms showing the 3-state enable and disable times.

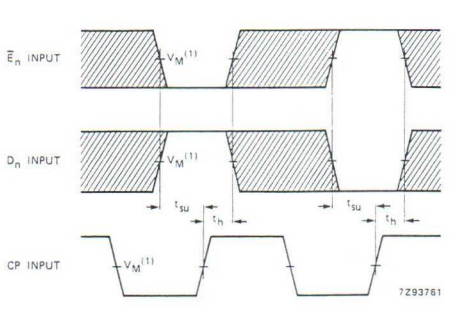


Fig. 9 Waveforms showing the data set-up and hold times from input ($\overline{E}_n$, D_n) to clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

HEX D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Six edge-triggered D-type flip-flops
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT174 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	17 13	18 17	ns ns
f_{max}	maximum clock frequency		99	69	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

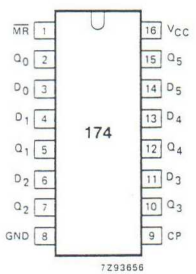
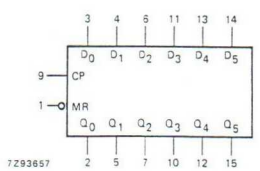


Fig. 1 Pin configuration.



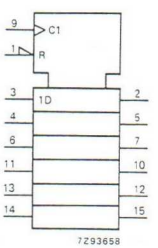


Fig. 3 IEC logic symbol.

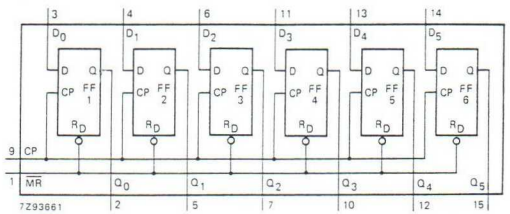


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

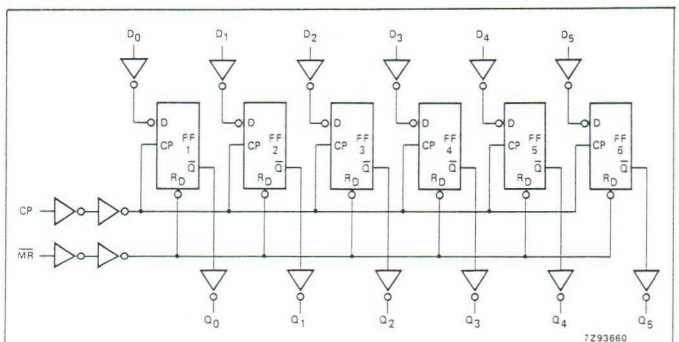


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; LOW	80 16 14	12 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5	−11 −4 −3		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
$\overline{CP}$	1.30
$\overline{MR}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		21	35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		20	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width; LOW	20	7		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	12	−3		15		18		ns	4.5	Fig. 7
t_{su}	set-up time D_n to CP	16	4		20		24		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5	−3		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	63		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

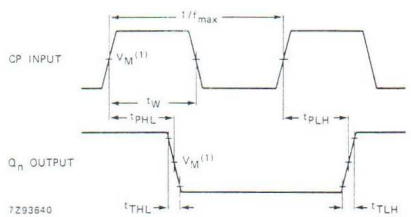


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

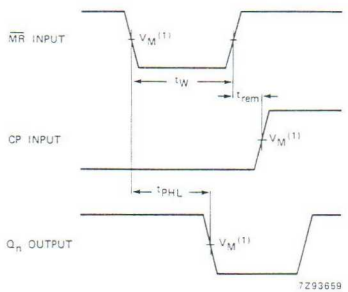


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

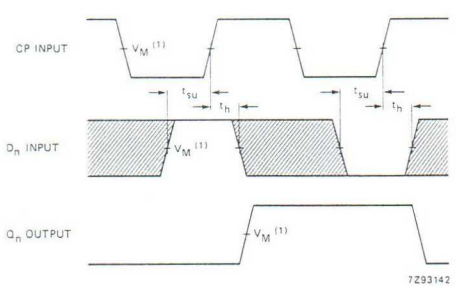


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Four edge-triggered D flip-flops
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs.

The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$ $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	17 15	16 19	ns ns
t_{PLH}	propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$ $\overline{MR}$ to $\overline{Q}_n$		17 15	16 16	ns ns
f_{max}	maximum clock frequency		83	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

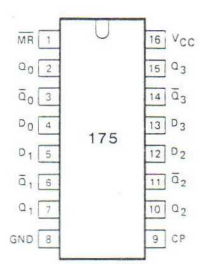


Fig. 1 Pin configuration.

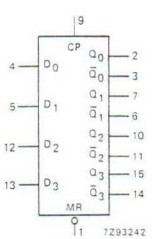


Fig. 2 Logic symbol.

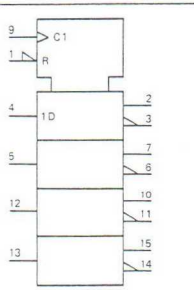


Fig. 3 IEC logic symbol.

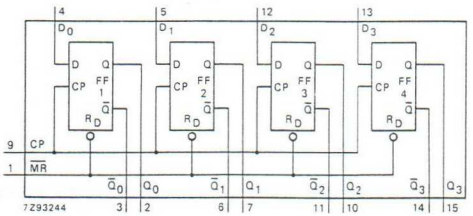


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care

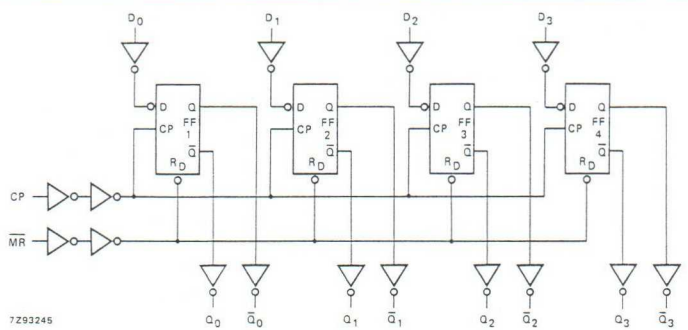


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5	−33 −12 −10		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	80 16 14	3 1 1		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time CP to D_n	25 5 4	2 0 0		30 6 5		40 8 7		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	25 75 89		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	1.00
CP	0.60
D_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		19	33		41		50	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		22	38		48		57	ns	4.5	Fig. 8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20	12		25		30		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5	−10		5		5		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	16	5		20		24		ns	4.5	Fig. 7
t_h	hold time CP to D_n	5	0		5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

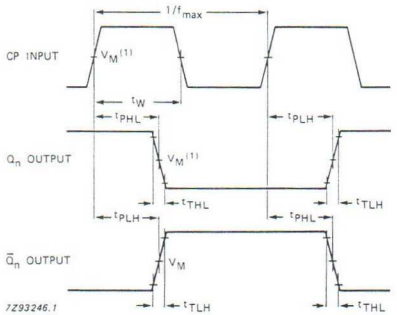


Fig. 6 Waveforms showing the clock (CP) to outputs (Q_n, $\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

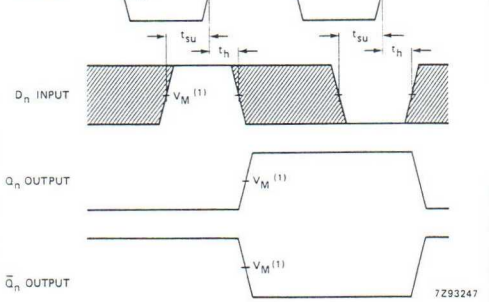


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

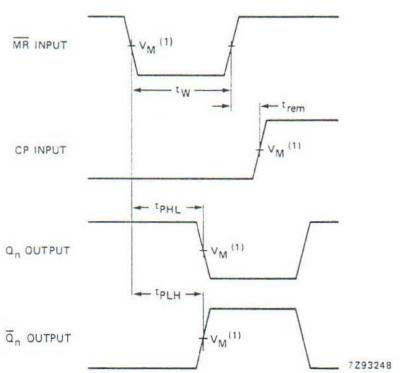


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delays and the master reset to clock (CP) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- Full carry look-ahead for high-speed arithmetic operation on long words
- Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others
- Provides all 16 logic operations of two variables: EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations
- Output capability: standard, A=B open drain
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (S_0 to S_3) and the mode control input (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table).

When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When M is LOW, the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A=B C_n to C_{n+4}	C_L = 15 pF V_{CC} = 5 V	28 17	30 21	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per L package	notes 1 and 2	90	92	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

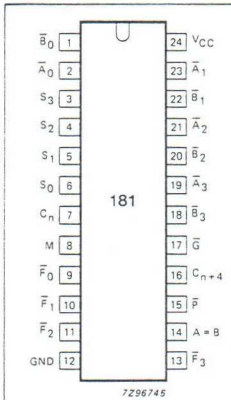


Fig. 1 Pin configuration.

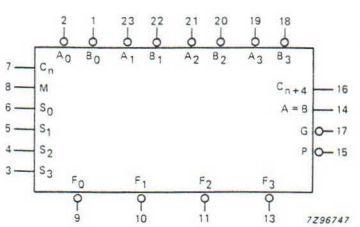


Fig. 2 Logic symbol.

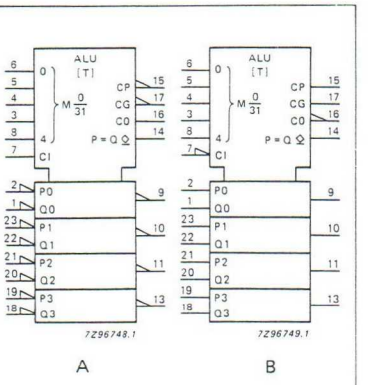


Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION (Cont'd)

either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the carry propagation ($\overline{P}$) and carry generate ($\overline{G}$) signals. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output (A=B) of the device goes HIGH when all four function outputs ($\overline{F}_0$ to $\overline{F}_3$) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. A=B is an open collector output and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The open drain output A=B should be used with an external pull-up resistor in order to establish a logic HIGH level. The A=B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B}_0$ to $\overline{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\overline{A}_0$ to $\overline{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S_0 to S_3	select inputs
7	C_n	carry input
8	M	mode control input
9, 10, 11, 13	$\overline{F}_0$ to $\overline{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\overline{P}$	carry propagate output (active LOW)
16	C_{n+4}	carry output
17	$\overline{G}$	carry generate output (active LOW)
24	V_{CC}	positive supply voltage

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands.

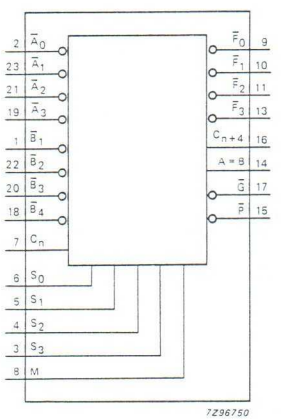
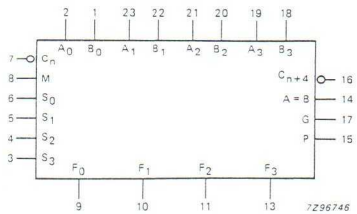


Fig. 4 Functional diagram.

Active HIGH operands



Active LOW operands

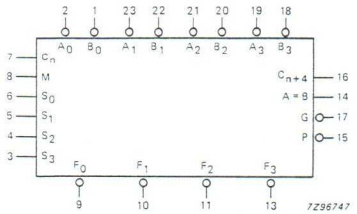


Fig. 5 Active HIGH operands – active LOW operands.

FUNCTION TABLES

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC** (M=L; C_n=H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	A$\overline{B}$	A$\overline{B}$ minus 1
H	L	L	L	$\overline{A} + B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC** (M=L; C_n=L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

Notes to the function tables

* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

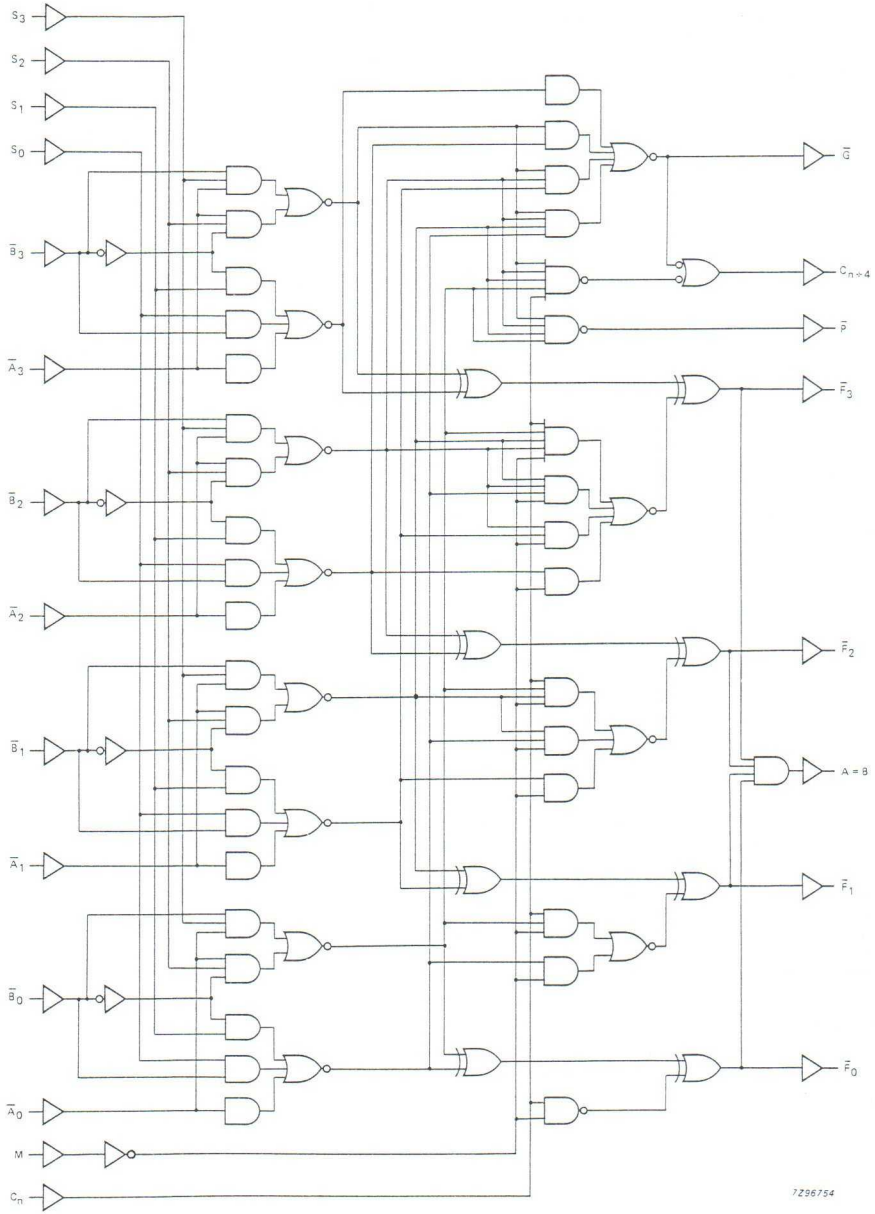


Fig. 6 Logic diagram.

TABLE 1 SUM MODE TEST

Function inputs $S_0 = S_3 = 4.5$ V, $M = S_1 = S_2 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}/t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}/t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}/t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}/t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}/t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	remaining $\overline{B}$	remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}/t_{PHL}	C_n	none	none	all $\overline{A}$	all $\overline{B}$	any $\overline{F}$ or C_{n+4}

TABLE 2 DIFFERENTIAL MODE TEST

Function inputs $S_1 = S_2 = 4.5$ V, $M = S_0 = S_3 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{A}$	remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$	remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/t_{PHL}	$\overline{A}_i$	none	$\overline{B}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}/t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH}/t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLZ}/t_{PZL}	$\overline{A}_i$	none	$\overline{B}_i$	remaining $\overline{A}$	remaining $\overline{B}$, C_n	A=B
t_{PLZ}/t_{PZL}	$\overline{B}_i$	$\overline{A}_i$	none	remaining $\overline{A}$	remaining $\overline{B}$, C_n	A=B
t_{PLH}/t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH}/t_{PHL}	$\overline{B}_i$	none	$\overline{A}_i$	none	remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH}/t_{PHL}	C_n	none	none	all $\overline{A}$ and $\overline{B}$	none	any $\overline{F}$ or C_{n+4}

TABLE 3 LOGIC MODE TEST

Function inputs $M = S_1 = S_2 = 4.5$ V, $S_0 = S_3 = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH}/t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}/t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	none	none	remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$

RATINGS (for A=B output only)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_O	DC output voltage	−0.5	+7.0	V	
$-I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V
$-I_O$	DC output source or sink current		25	mA	for $-0.5\ V < V_O$

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain output (A=B). They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{IL}	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	note 1 V_O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	MODE	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay C_n to C_{n+4}		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t_{PHL}/t_{PLH}	propagation delay C_n to $\overline{F}_n$		69 25 20	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		72 26 21	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		76 26 21	215 43 37		270 54 46		320 65 55	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		77 28 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		85 31 25	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		83 31 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig. 8; Table 3
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	logic	M = 4.5 V; Fig. 8; Table 3

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		80 29 23	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 8; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		80 29 23	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 8; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 10; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		85 31 25	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 10; Table 2
t_{PZL}/t_{PLZ}	propagation delay $\overline{A}_n$ to A=B		80 29 23	245 49 42		305 61 52		370 74 63	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 11; Table 2
t_{PZL}/t_{PLZ}	propagation delay $\overline{B}_n$ to A=B		88 32 26	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 11; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		88 32 26	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0		note 1; Figs 7 and 11

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain output (A=B). They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_{IL}	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	note 1; V_O = 0 or 6 V

Note to the DC characteristics

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C_n, M	0.50
$\overline{A}_n$, $\overline{B}_n$	0.75
S_n	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay C_n to C_{n+4}		25	42		53		63	ns	4.5	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay C_n to $\overline{F}_n$		28	48		60		72	ns	4.5	sum diff	M = 0 V; Fig. 9; Tables 1 and 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		32	54		68		81	ns	4.5	sum	M = S_1 = S_2 = 0 V; S_0 = S_3 = 4.5 V; Fig. 7; Table 1
t_{PHL}/ t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2
t_{PHL}/ t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{G}$		31	54		68		81	ns	4.5	diff	M = S_0 = S_3 = 0 V; S_1 = S_2 = 4.5 V; Fig. 8; Table 2

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	MODE	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		23	41		51		62	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		24	41		51		62	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{P}$		23	40		50		60	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{P}$		23	40		50		60	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		33	58		73		87	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		34	58		73		87	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		33	57		71		86	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		33	57		71		86	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_i$ to $\overline{F}_i$		29	54		68		81	ns	4.5	logic	$M = 4.5$ V; Fig. 8; Table 3
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_i$ to $\overline{F}_i$		33	54		68		81	ns	4.5	logic	$M = 4.5$ V; Fig. 8; Table 3
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		30	53		66		80	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 8; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		31	53		66		80	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 8; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to C_{n+4}		30	55		69		83	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 10; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to C_{n+4}		34	55		69		83	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 10; Table 2
t_{PZL}/t_{PLZ}	propagation delay $\overline{A}_n$ to A=B		34	60		75		90	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 11; Table 2
t_{PZL}/t_{PLZ}	propagation delay $\overline{B}_n$ to A=B		35	60		75		90	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 11; Table 2

AC CHARACTERISTICS (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	MODE	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{B}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	sum	$M = S_1 = S_2 = 0$ V; $S_0 = S_3 = 4.5$ V; Fig. 7; Table 1
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		32	56		70		84	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{F}_n$		33	56		70		84	ns	4.5	diff	$M = S_0 = S_3 = 0$ V; $S_1 = S_2 = 4.5$ V; Fig. 8; Table 2
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5		Figs 7 and 11; [1] note 1

Note to the AC characteristics

1. For the open drain output (A=B) only t_{THL} is valid.

AC WAVEFORMS

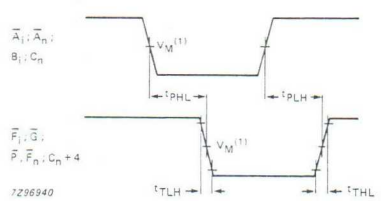


Fig. 7 Propagation delays for carry input to carry output, carry input to function outputs, operands to carry generate operands, propagation outputs and output transition lines.

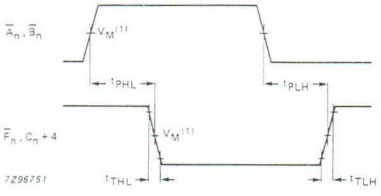


Fig. 9 Propagation delays for operands to carry output and function outputs.

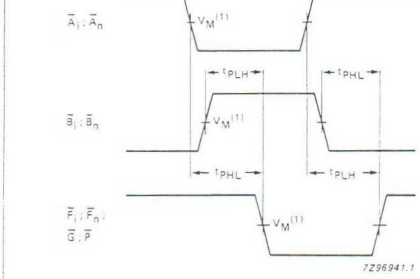


Fig. 8 Propagation delays for operands to carry generate, propagate outputs and function outputs.

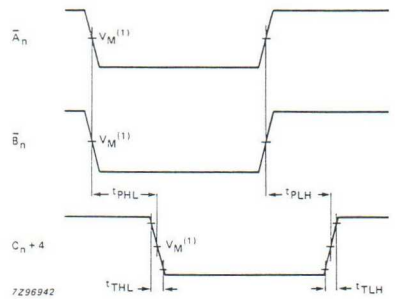


Fig. 10 Propagation delays for operands to carry output.

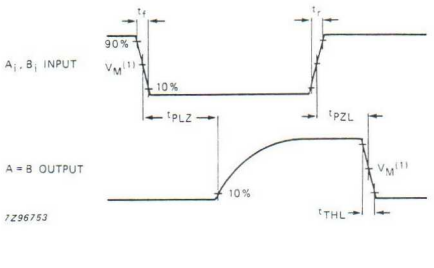


Fig. 11 Waveforms showing the input (A_i, B_i) to output (A=B) propagation delays and output transition time of the open drain output (A=B).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

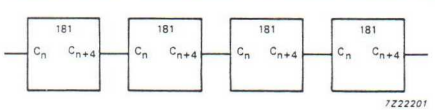


Fig. 12 Application example showing 16-bit ALU ripple-carry configuration.

Note to Fig. 12

A and B inputs and F outputs of "181" are not shown.

LOOK-AHEAD CARRY GENERATOR

FEATURES

- **Provides carry look-ahead across a group of four ALU's**
- **Multi-level look-ahead for high-speed arithmetic operation over long word length**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders.

The "182" also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$ C_n to any output $\overline{P}_n$ or $\overline{G}_n$ to any output	C_L = 15 pF V_{CC} = 5 V	11 17 14	14 21 17	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	50	50	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C_{n+z}	function output
10	$\overline{G}$	carry generate output (active LOW)
11	C_{n+y}	function output
12	C_{n+x}	function output
13	C_n	carry input (active HIGH)
16	V_{CC}	positive supply voltage

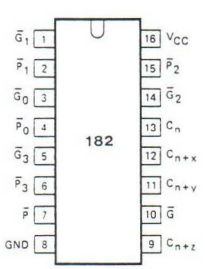


Fig. 1 Pin configuration.

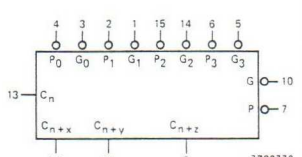


Fig. 2 Logic symbol.

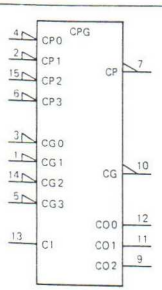


Fig. 3 IEC logic symbol.

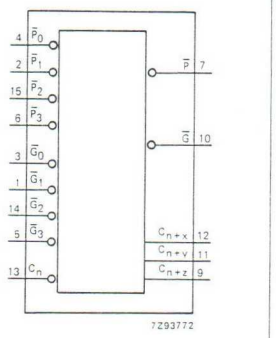


Fig. 4 Functional diagram.

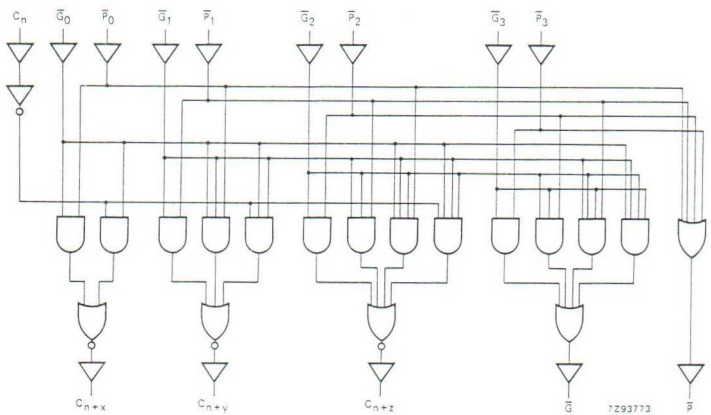


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	L	X						L			
X	X	X	X	L						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	H	H	H	H					L		
X	X	H	H	H	H	X					L		
L	H	X	H	X	X	X					L		
X	X	X	L	L	L	L					H		
X	X	X	X	L	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	L	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$		30 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{G}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to C_{n+n}		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to C_{n+n}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to $\overline{G}$		41 15 12	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{G}_0$, $\overline{G}_1$, $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$	1.50
$\overline{G}_3$	0.30
$\overline{G}_2$, $\overline{P}_3$, C_n	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$		17	28		35		42	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output		26	43		54		65	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{G}$		20	33		41		50	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to C_{n+n}		20	33		41		50	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to C_{n+n}, $\overline{G}_n$ to $\overline{G}$		18	32		40		48	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

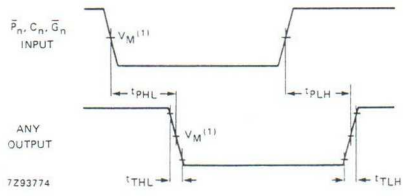


Fig. 6 Waveforms showing the input ($\overline{P}_n$, C_n, $\overline{G}_n$) to any output propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

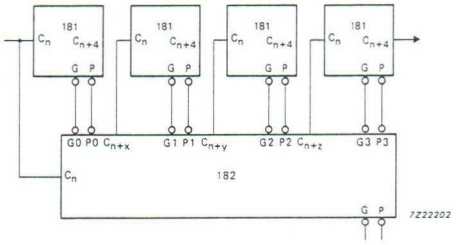


Fig. 7 16-bit ALU two-level look-ahead.

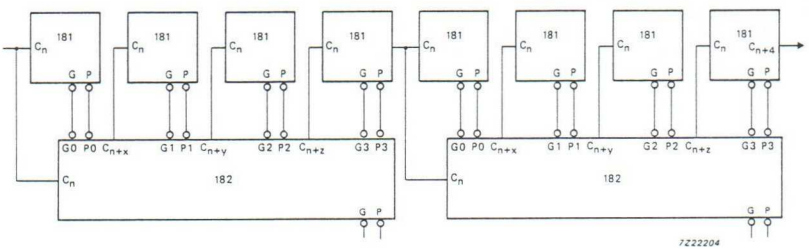


Fig. 8 32-bit ALU two-level look-ahead over 16-bit groups.

APPLICATION INFORMATION (Cont'd)

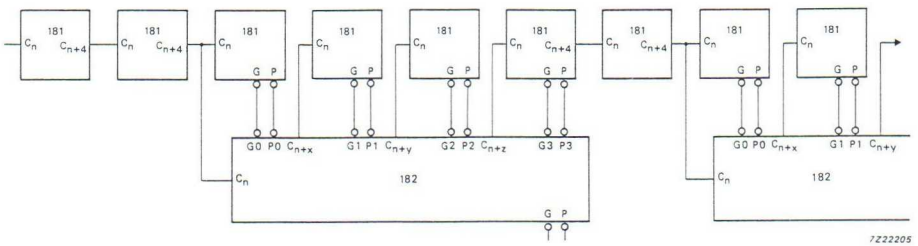


Fig. 9 Combined two-level look-ahead and ripple-carry ALU.

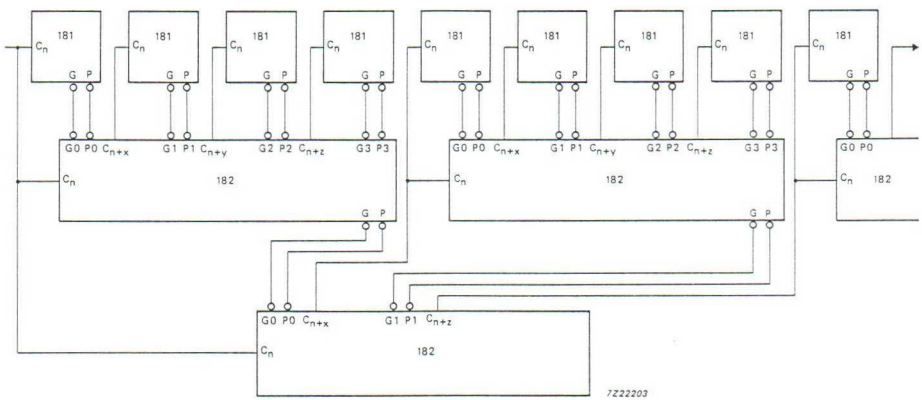


Fig. 10 64-bit ALU full-carry three-level look-ahead.

Note to Figs 7 to 10

A and B inputs and F outputs of "181" are not shown.

PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT190 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	22	24	ns
f_{max}	maximum clock frequency		28	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	36	38	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}/D$	up/down input
8	GND	ground (0 V)
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

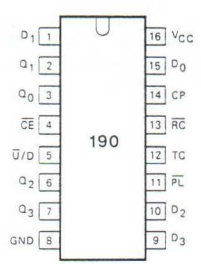


Fig. 1 Pin configuration.

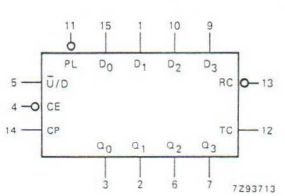


Fig. 2 Logic symbol.

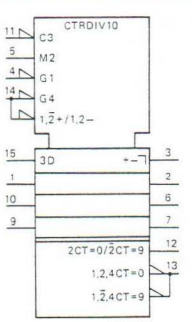


Fig. 3 IEC logic symbol.

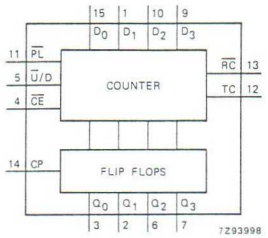


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
parallel load	L L	X X	X X	X X	L H	L H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND RC FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓⊔	H	X	X	H	⊓	⊓⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓⊔	L	L	L	L	⊓	⊓⊔

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition
⊓⊔ = one LOW level pulse
⊓ = TC goes LOW on a LOW-to-HIGH CP transition

GENERAL DESCRIPTION

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig. 5, each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

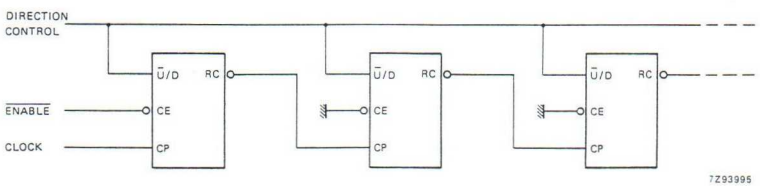


Fig. 5 N-stage ripple counter using ripple clock.

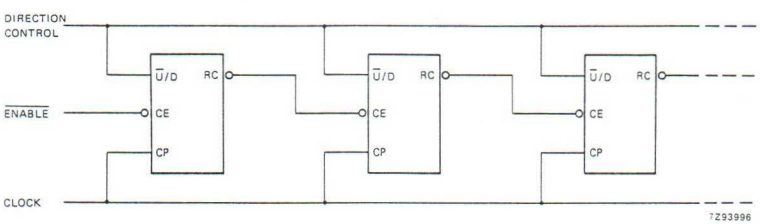


Fig. 6 Synchronous n-stage counter using ripple carry/borrow.

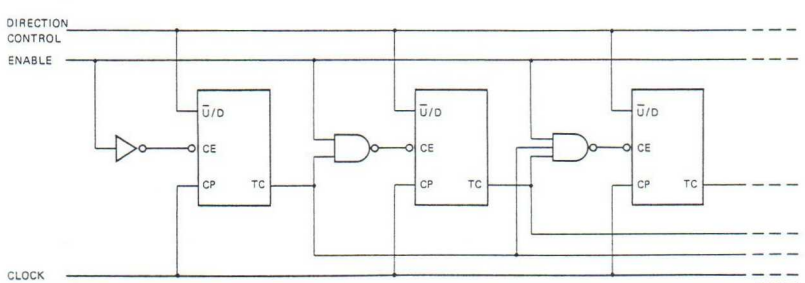
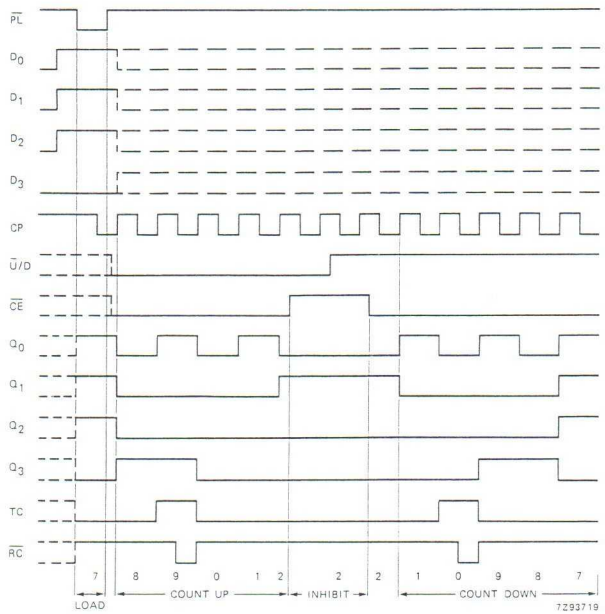


Fig. 7 Synchronous n-stage counter with parallel gated carry/borrow.



Sequence

Load (preset) to BCD seven;

count up to eight, nine, zero, one and two;

inhibit;

count down to one, zero, nine, eight and seven.

Fig. 8 Typical load, count and inhibit sequence.

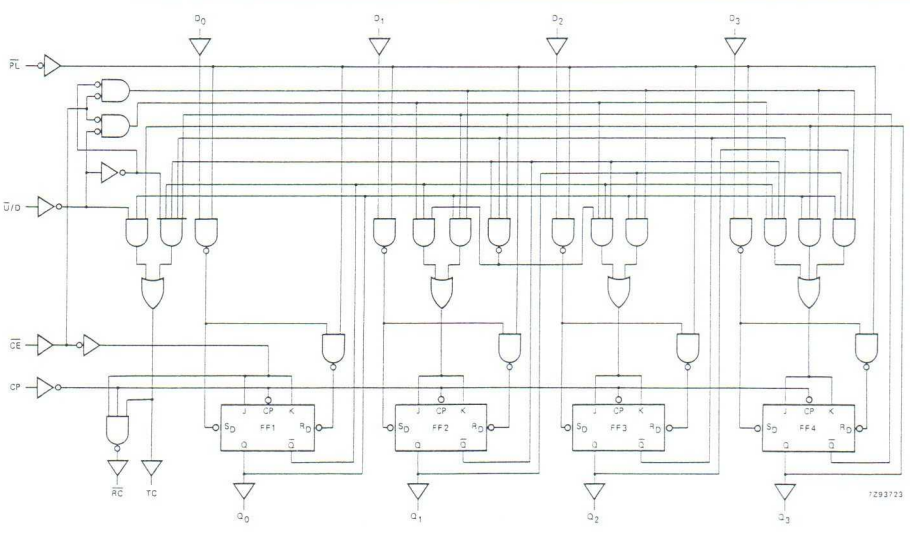


Fig. 9 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to TC		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{RC}$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{RC}$		33 12 10	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to TC		44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to $\overline{RC}$		50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15
t_W	clock pulse width HIGH or LOW	155 31 26	28 10 8		195 39 33		235 47 40		ns	2.0 4.5 6.0	Fig. 10
t_W	parallel load pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 15
t_{rem}	removal time $\overline{PL}$ to CP	35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 15

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time $\overline{U}/D$ to CP	205 41 35	61 22 18		255 51 43		310 62 53		ns	2.0 4.5 6.0	Fig. 17
t_{su}	set-up time D_n to $\overline{PL}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 16
t_{su}	set-up time $\overline{CE}$ to CP	140 28 24	39 14 11		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 17
t_h	hold time $\overline{U}/D$ to CP	0 0 0	−44 −16 −13		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 17
t_h	hold time D_n to $\overline{PL}$	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 16
t_h	hold time $\overline{CE}$ to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 17
f_{max}	maximum clock pulse frequency	3.0 15 18	8.3 25 30		2.4 12 14		2.0 10 12		MHz	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.5
$\overline{CP}$	0.65
$\overline{U}/D$	1.15
$\overline{CE}$, $\overline{PL}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		28	48		60		72	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to TC		34	58		73		87	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{RC}$		20	35		44		53	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{RC}$		18	33		41		50	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		24	44		55		66	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		29	49		61		74	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to TC		24	45		56		68	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to $\overline{RC}$		26	45		56		68	ns	4.5	Fig. 14
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 15
t_W	clock pulse width HIGH or LOW	25	10		31		38		ns	4.5	Fig. 10
t_W	parallel load pulse width LOW	22	12		28		33		ns	4.5	Fig. 15
t_{rem}	removal time $\overline{PL}$ to CP	7	1		9		11		ns	4.5	Fig. 15
t_{su}	set-up time $\overline{U}/D$ to CP	42	25		53		63		ns	4.5	Fig. 17
t_{su}	set-up time D_n to $\overline{PL}$	20	10		25		30		ns	4.5	Fig. 16
t_{su}	set-up time $\overline{CE}$ to CP	31	18		39		47		ns	4.5	Fig. 17
t_h	hold time $\overline{U}/D$ to CP	0	−18		0		0		ns	4.5	Fig. 17
t_h	hold time D_n to $\overline{PL}$	0	−6		0		0		ns	4.5	Fig. 16
t_h	hold time $\overline{CE}$ to CP	0	−10		0		0		ns	4.5	Fig. 17
f_{max}	maximum clock pulse frequency	16	27		13		11		MHz	4.5	Fig. 10

AC WAVEFORMS

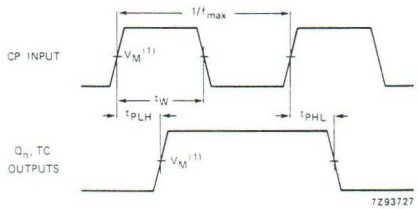


Fig. 10 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

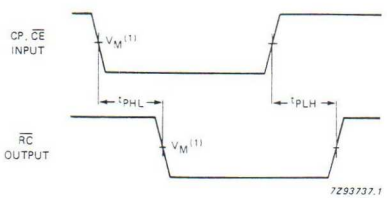


Fig. 11 Waveforms showing the clock and count enable inputs (CP, $\overline{CE}$) to ripple clock output ($\overline{RC}$) propagation delays.

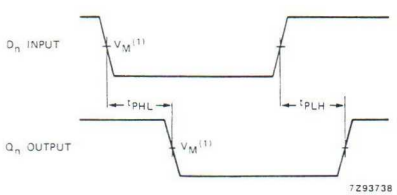


Fig. 12 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

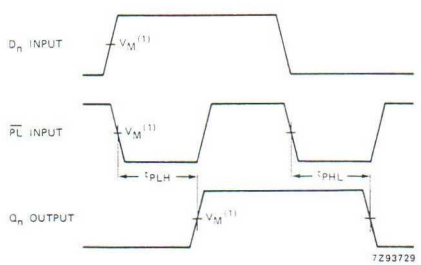


Fig. 13 Waveforms showing the input ($\overline{PL}$) to output (Q_n) propagation delays.

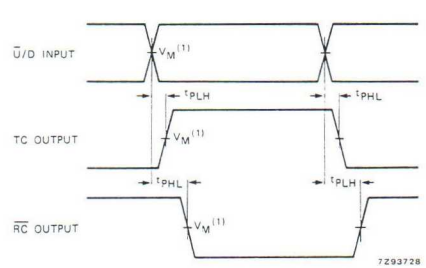


Fig. 14 Waveforms showing the up/down count input ($\overline{U}/D$) to terminal count and ripple clock output (TC, $\overline{RC}$) propagation delays.

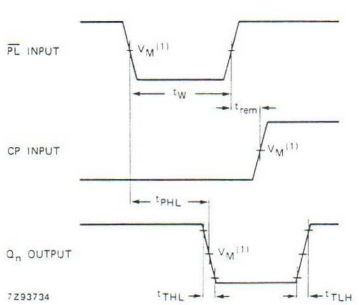


Fig. 15 Waveforms showing the parallel load input ($\overline{PL}$) pulse width, removal time to clock (CP) and the output (Q_n) transition times.

AC WAVEFORMS (Continued)

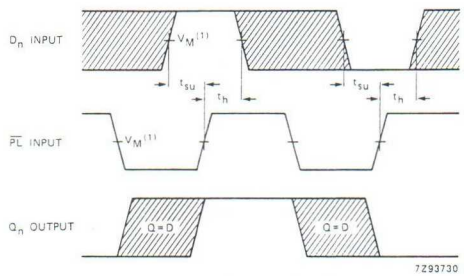


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input ($\overline{PL}$) to the data input (D_n).

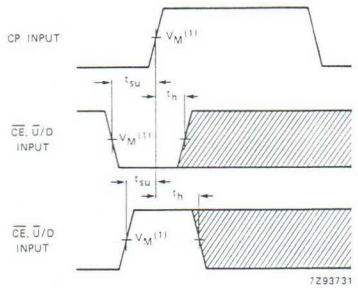


Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ($\overline{CE}$, $\overline{U}$/D) to the clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Figs 16 and 17

The shaded areas indicate when the input is permitted to change for predictable output performance.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	22	22	ns
f_{max}	maximum clock frequency		36	36	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	31	33	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}/D$	up/down input
8	GND	ground (0 V)
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

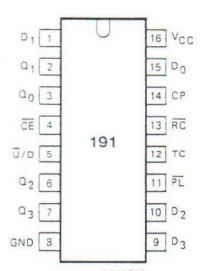


Fig. 1 Pin configuration.

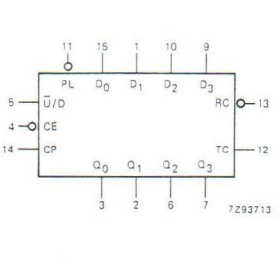


Fig. 2 Logic symbol.

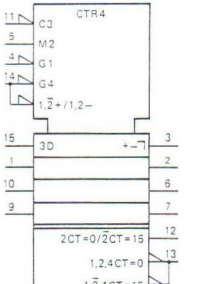


Fig. 3 IEC logic symbol.

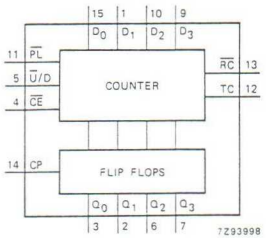


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
parallel load	L L	X X	X X	X X	L H	L H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND RC FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓⊔	H	H	H	H	⊓	⊓⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓⊔	L	L	L	L	⊓	⊓⊔

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition
⊓⊔ = one LOW level pulse
⊓ = TC goes LOW on a LOW-to-HIGH CP transition

GENERAL DESCRIPTION

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig. 5, each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

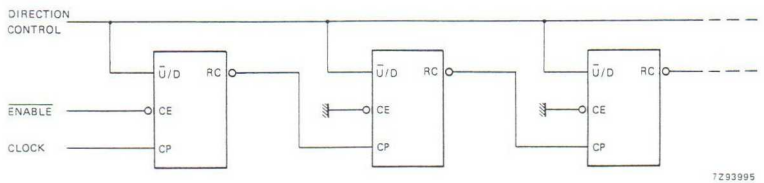


Fig. 5 N-stage ripple counter using ripple clock.

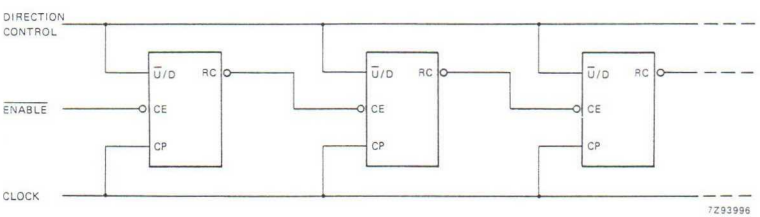


Fig. 6 Synchronous n-stage counter using ripple carry/borrow.

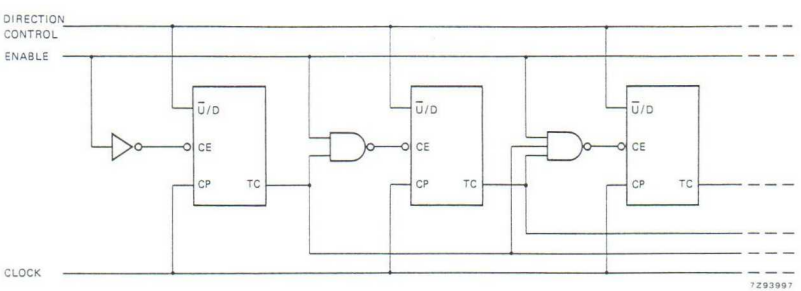
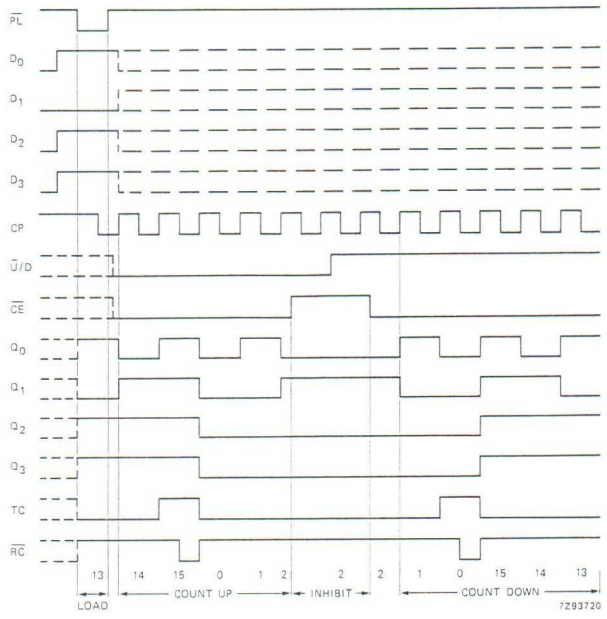


Fig. 7 Synchronous n-stage counter with parallel gated carry/borrow.



Sequence

Load (preset) to binary thirteen;
count up to fourteen, fifteen, zero, one and two;
inhibit;
count down to one, zero, fifteen, fourteen and thirteen.

Fig. 8 Typical load, count and inhibit sequence.

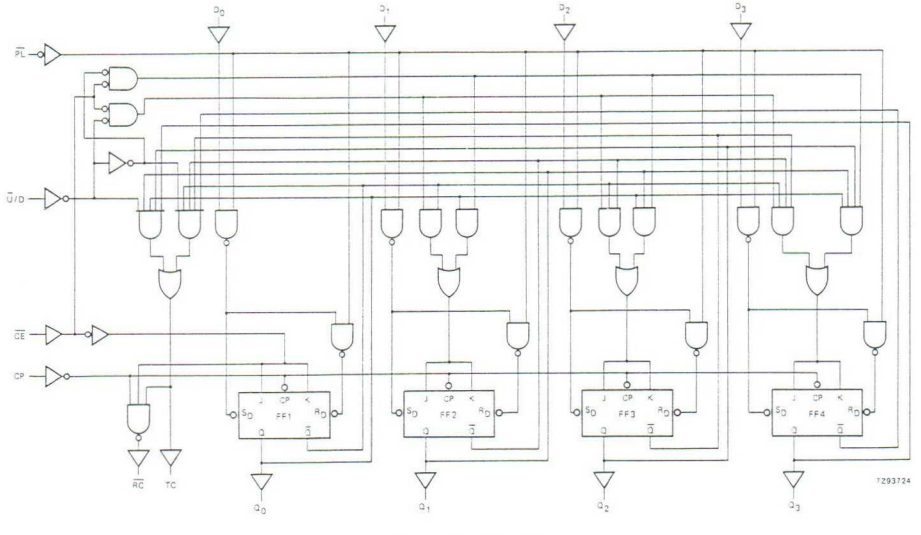


Fig. 9 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to TC		83 30 24	255 51 43		320 64 54		395 77 65	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{RC}$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{RC}$		33 12 10	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to TC		44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to $\overline{RC}$		50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15
t_W	clock pulse width HIGH or LOW	125 25 21	28 10 8		155 31 26		195 39 33		ns	2.0 4.5 6.0	Fig. 10
t_W	parallel load pulse width LOW	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 15
t_{rem}	removal time $\overline{PL}$ to CP	35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 15

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time $\overline{U}/D$ to CP	205 41 35	50 18 14		255 51 43		310 62 53		ns	2.0 4.5 6.0	Fig. 17
t_{su}	set-up time D_n to $\overline{PL}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 16
t_{su}	set-up time $\overline{CE}$ to CP	140 28 24	44 16 13		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 17
t_h	hold time $\overline{U}/D$ to CP	0 0 0	−39 −14 −11		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 17
t_h	hold time D_n to $\overline{PL}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 16
t_h	hold time $\overline{CE}$ to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 17
f_{max}	maximum clock pulse frequency	4.0 20 24	11 33 39		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.5
$\overline{CP}$	0.65
$\overline{U}/D$	1.15
$\overline{CE}$, $\overline{PL}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		26	48		60		72	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to TC		32	51		64		77	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{RC}$		19	35		44		53	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{RC}$		19	33		41		50	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		22	44		55		66	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		27	46		58		69	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to TC		23	45		56		68	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay $\overline{U}/D$ to $\overline{RC}$		24	45		56		68	ns	4.5	Fig. 14
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 15
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 10
t_W	parallel load pulse width LOW	22	11		28		33		ns	4.5	Fig. 15
t_{rem}	removal time $\overline{PL}$ to CP	7	1		9		11		ns	4.5	Fig. 15
t_{su}	set-up time $\overline{U}/D$ to CP	41	20		51		62		ns	4.5	Fig. 17
t_{su}	set-up time D_n to $\overline{PL}$	20	9		25		30		ns	4.5	Fig. 16
t_{su}	set-up time $\overline{CE}$ to CP	30	18		38		45		ns	4.5	Fig. 17
t_h	hold time $\overline{U}/D$ to CP	0	−18		0		0		ns	4.5	Fig. 17
t_h	hold time D_n to $\overline{PL}$	0	−5		0		0		ns	4.5	Fig. 16
t_h	hold time $\overline{CE}$ to CP	0	−10		0		0		ns	4.5	Fig. 17
f_{max}	maximum clock pulse frequency	20	33		16		13		MHz	4.5	Fig. 10

AC WAVEFORMS

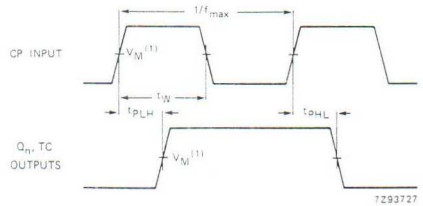


Fig. 10 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

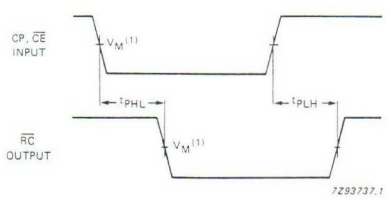


Fig. 11 Waveforms showing the clock and count enable inputs (CP, $\overline{CE}$) to ripple clock output ($\overline{RC}$) propagation delays.

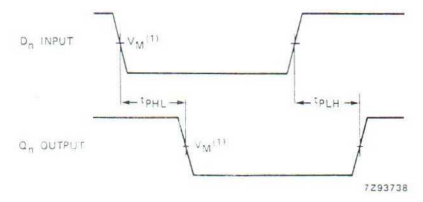


Fig. 12 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

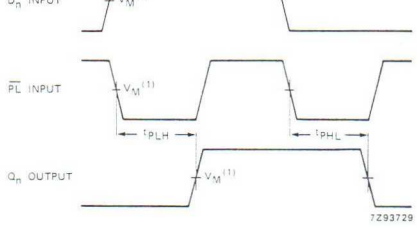


Fig. 13 Waveforms showing the input ($\overline{PL}$) to output (Q_n) propagation delays.

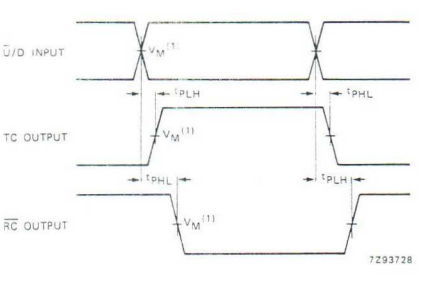


Fig. 14 Waveforms showing the up/down count input ($\overline{U}/D$) to terminal count and ripple clock output (TC, $\overline{RC}$) propagation delays.

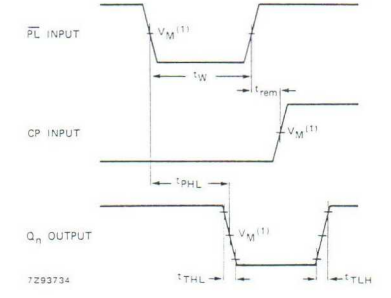


Fig. 15 Waveforms showing the parallel load input ($\overline{PL}$) pulse width, removal time to clock (CP) and the output (Q_n) transition times.

AC WAVEFORMS (Continued)

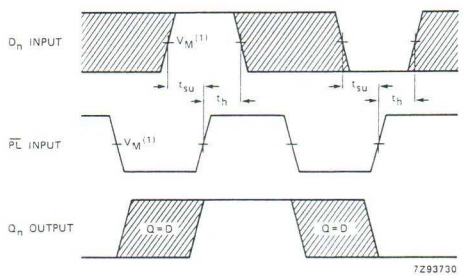


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input ($\overline{PL}$) to the data input (D_n).

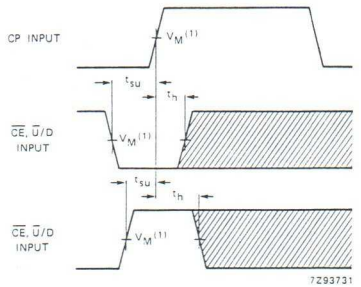


Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ($\overline{CE}$, U/D) to the clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Figs 16 and 17

The shaded areas indicate when the input is permitted to change for predictable output performance.

PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT192 are synchronous BCD up/down counters.
Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "192" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_D, CP_U to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	20	ns
f_{max}	maximum clock frequency		40	45	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input*
5	CP_U	count up clock input*
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

* LOW-to-HIGH, edge triggered

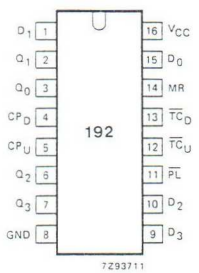


Fig. 1 Pin configuration.

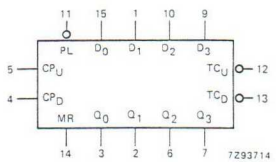


Fig. 2 Logic symbol.

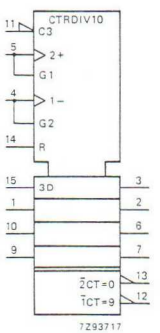


Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION (Continued)

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.
$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

* $\overline{TC}_U = CP_U$ at terminal count up (HLLH)
** $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

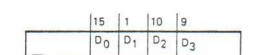
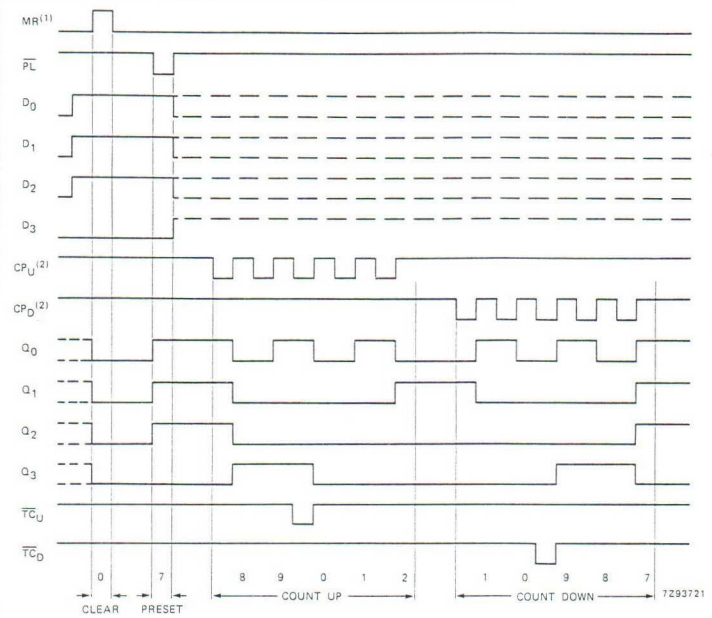


Fig. 4 Functional diagram.



(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input (CP_D) must be HIGH, when counting down the count up clock input (CP_U) must be HIGH.

Sequence

Clear (reset outputs to zero);

load (preset) to BCD seven;

count up to eight, nine, terminal count up, zero, one and two;

count down to one, zero, terminal count down, nine, eight, and seven.

Fig. 5 Typical clear, load and count sequence.

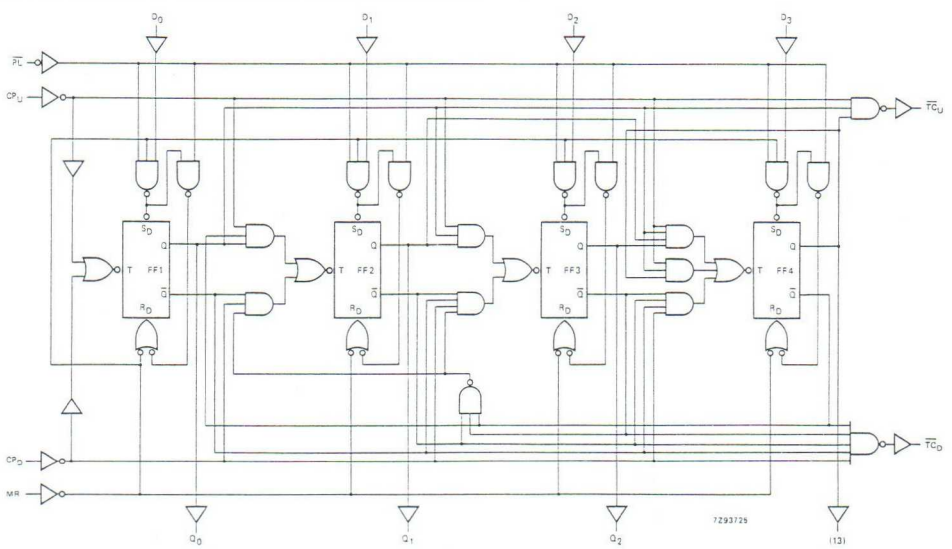


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_U, CP_D to Q_n		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP_U to TC_U		33 12 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP_D to TC_D		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay MR to Q_n		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}	propagation delay D_n to Q_n		91 33 26	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{PLH}	propagation delay D_n to Q_n		80 29 23	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$		102 37 30	315 63 54		395 79 67		475 95 81	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		96 35 28	285 57 48		355 71 60		430 86 73	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{TC}_U$, D_n to $\overline{TC}_D$		83 30 24	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 12
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t_W	up clock pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7
t_W	down clock pulse width HIGH or LOW	140 28 24	50 18 14		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_W	parallel load pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{PL}$ to CP_U, CP_D	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time MR to CP_U, CP_D	50 10 9	0 0 0		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time D_n to $\overline{PL}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11 note: $CP_U = CP_D$ = HIGH
t_h	hold time D_n to $\overline{PL}$	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time CP_U to CP_D, CP_D to CP_U	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
f_{max}	maximum up, down clock pulse frequency	4.0 20 24	12 36 43		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
CP_U, CP_D	1.40
$\overline{PL}$	0.65
MR	1.05

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_U, CP_D to Q_n		23	43		54		65	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP_U to $\overline{TC}_U$		16	30		38		45	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP_D to $\overline{TC}_D$		17	30		38		45	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		28	46		58		69	ns	4.5	Fig. 9
t_{PHL}	propagation delay MR to Q_n		24	40		50		60	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		36	62		78		93	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$		36	64		80		96	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		36	64		80		96	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{TC}_U$, D_n to $\overline{TC}_D$		33	58		73		87	ns	4.5	Fig. 12
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 10
t_W	up, down clock pulse width HIGH or LOW	25	14		31		38		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig. 10
t_W	parallel load pulse width LOW	20	10		25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{PL}$ to CP_U, CP_D	10	1		13		15		ns	4.5	Fig. 9
t_{rem}	removal time MR to CP_U, CP_D	10	2		13		15		ns	4.5	Fig. 10
t_{su}	set-up time D_n to $\overline{PL}$	16	8		20		24		ns	4.5	Fig. 11 note: $CP_U = CP_D$ = HIGH
t_h	hold time D_n to $\overline{PL}$	0	−6		0		0		ns	4.5	Fig. 11
t_h	hold time CP_U to CP_D, CP_D to CP_U	20	9		25		30		ns	4.5	Fig. 13
f_{max}	maximum up, down clock pulse frequency	20	41		16		13		MHz	4.5	Fig. 7

AC WAVEFORMS

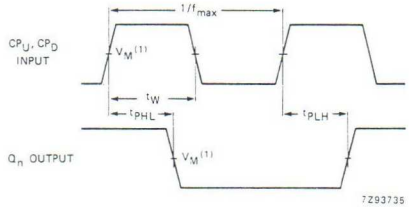


Fig. 7 Waveforms showing the clock (CP_U, CP_D) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

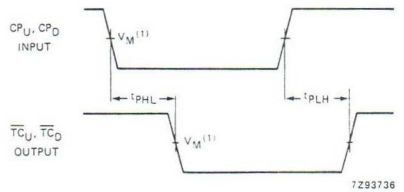


Fig. 8 Waveforms showing the clock (CP_U, CP_D) to terminal count output ($\overline{TC}_U$, $\overline{TC}_D$) propagation delays.

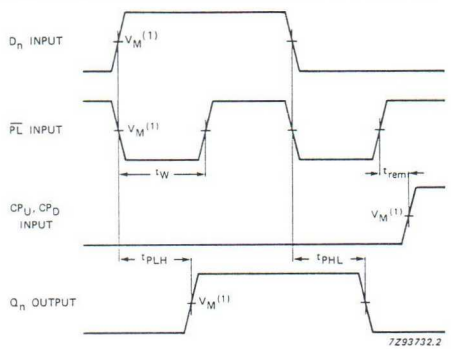


Fig. 9 Waveforms showing the parallel load input ($\overline{PL}$) and data (D_n) to Q_n output propagation delays and $\overline{PL}$ removal time to clock input (CP_U, CP_D).

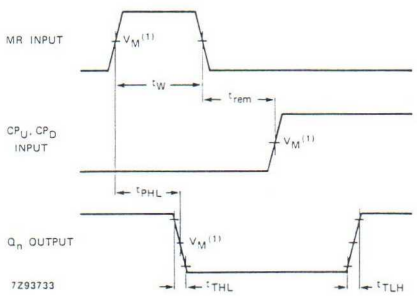


Fig. 10 Waveforms showing the master reset input (MR) pulse width, MR to Q_n propagation delays, MR to CP_U, CP_D removal time and output transition times.

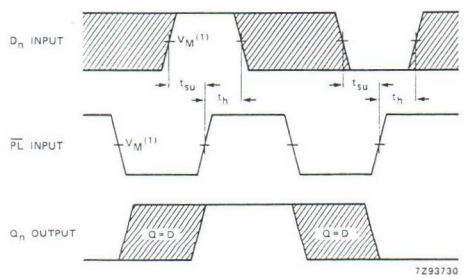


Fig. 11 Waveforms showing the data input (D_n) to parallel load input ($\overline{PL}$) set-up and hold times.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS (Continued)

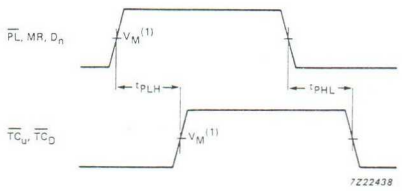


Fig. 12 Waveforms showing the data input (D_n), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TC_U}$, $\overline{TC_D}$) propagation delays.

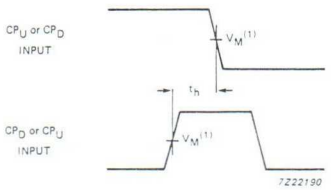


Fig. 13 Waveforms showing the CP_U to CP_D or CP_D to CP_U hold times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

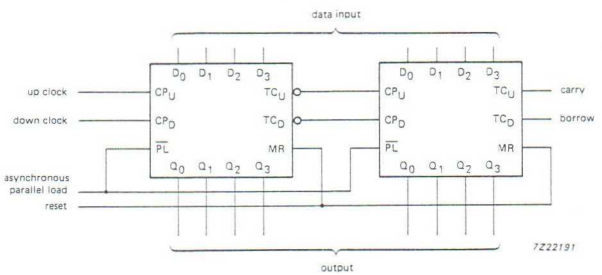


Fig. 14 Cascaded up/down counter with parallel load.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_D, CP_U to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	20	ns
f_{max}	maximum clock frequency		45	47	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	26	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input*
5	CP_U	count up clock input*
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

* LOW-to-HIGH, edge triggered

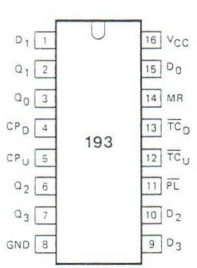


Fig. 1 Pin configuration.

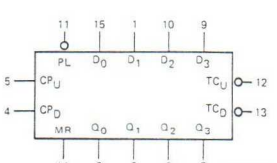


Fig. 2 Logic symbol.

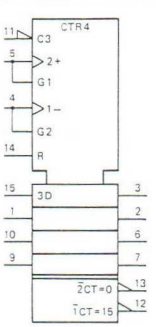


Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.
$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

* $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
** $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

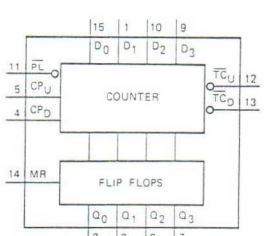
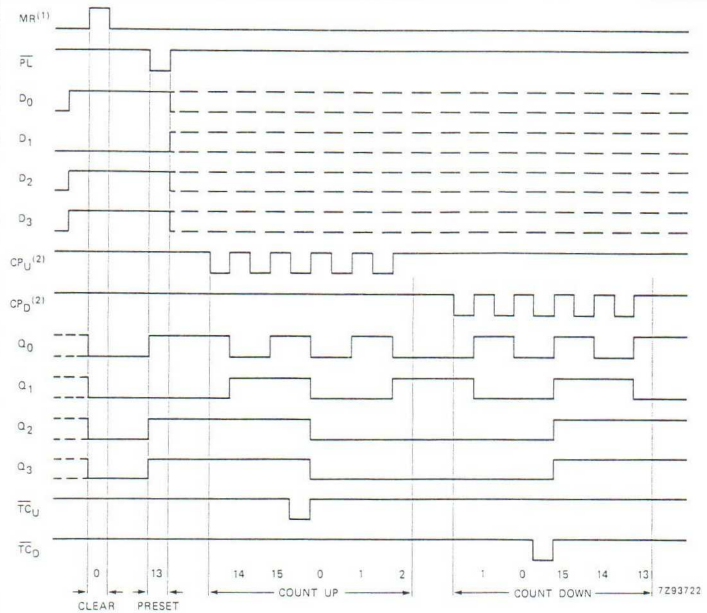


Fig. 4 Functional diagram.



(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input (CP_D) must be HIGH, when counting down the count up clock input (CP_U) must be HIGH.

Sequence

Clear (reset outputs to zero);

load (preset) to binary thirteen;

count up to fourteen, fifteen, terminal count up, zero, one and two;

count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Fig. 5 Typical clear, load and count sequence.

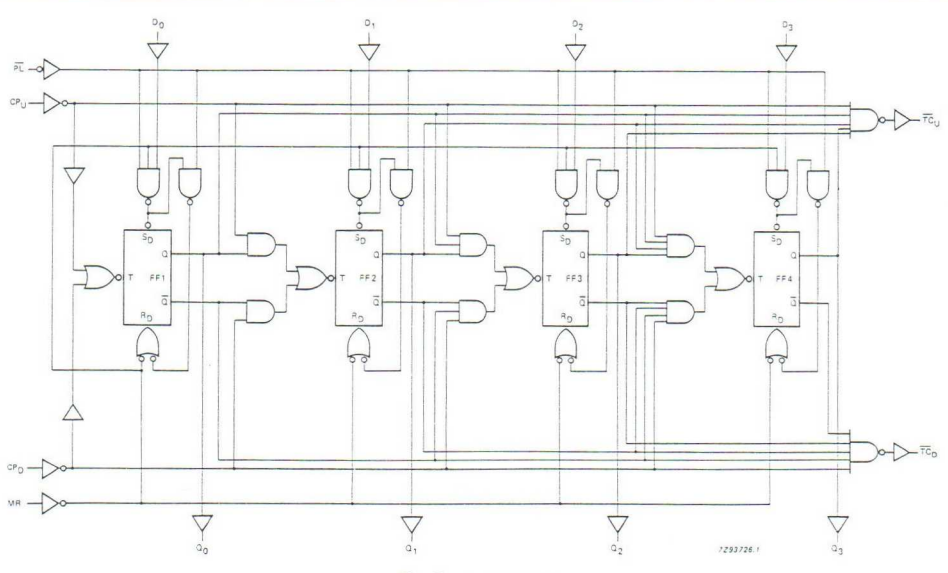


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_U, CP_D to Q_n		63 23 18	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP_U to $\overline{TC}_U$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP_D to $\overline{TC}_D$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay MR to Q_n		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$		80 29 23	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		74 27 22	285 57 48		355 71 60		430 86 73	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{TC}_U$, D_n to $\overline{TC}_D$		80 29 23	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 12
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t_W	up, down clock pulse width HIGH or LOW	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width HIGH	100 20 17	25 9 7		125 25 21		150 30 26		2 ns	2.0 4.5 6.0	Fig. 10
t_W	parallel load pulse width LOW	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{rem}	removal time $\overline{PL}$ to CP_U, CP_D	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time MR to CP_U, CP_D	50 10 9	0 0 0		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time D_n to $\overline{PL}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11 note: $CP_U = CP_D$ = HIGH
t_h	hold time D_n to $\overline{PL}$	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time CP_U to CP_D, CP_D to CP_U	80 16 8	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
f_{max}	maximum up, down clock pulse frequency	4.0 20 24	13.5 41 49		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
CP_U, CP_D	1.40
$\overline{PL}$	0.65
MR	1.05

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_U, CP_D to Q_n		23	43		54		65	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP_U to $\overline{TC}_U$		15	27		34		41	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP_D to $\overline{TC}_D$		15	27		34		41	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_n		26	46		58		69	ns	4.5	Fig. 9
t_{PHL}	propagation delay MR to Q_n		22	40		50		60	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		27	46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$		31	55		69		83	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		29	55		69		83	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{TC}_U$, D_n to $\overline{TC}_D$		32	58		73		87	ns	4.5	Fig. 12
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 10
t_W	up, down clock pulse width HIGH or LOW	25	11		31		38		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	20	7		25		30		ns	4.5	Fig. 10
t_W	parallel load pulse width LOW	20	8		25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{PL}$ to CP_U, CP_D	10	2		13		15		ns	4.5	Fig. 9
t_{rem}	removal time MR to CP_U, CP_D	10	0		13		15		ns	4.5	Fig. 10
t_{su}	set-up time D_n to $\overline{PL}$	16	8		20		24		ns	4.5	Fig. 11 note: $CP_U = CP_D$ = HIGH
t_h	hold time D_n to $\overline{PL}$	0	−6		0		0		ns	4.5	Fig. 11
t_h	hold time CP_U to CP_D, CP_D to CP_U	16	7		20		24		ns	4.5	Fig. 13
f_{max}	maximum up, down clock pulse frequency	20	43		16		13		MHz	4.5	Fig. 7

AC WAVEFORMS

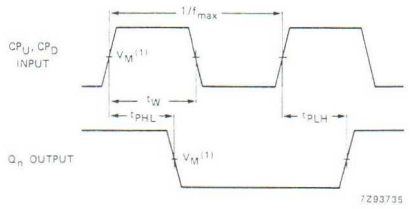


Fig. 7 Waveforms showing the clock (CP_U, CP_D) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

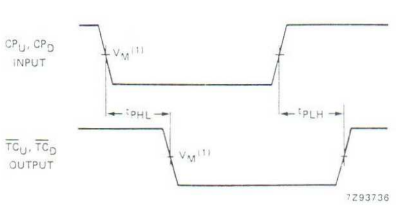


Fig. 8 Waveforms showing the clock (CP_U, CP_D) to terminal count output ($\overline{TC}_U$, $\overline{TC}_D$) propagation delays.

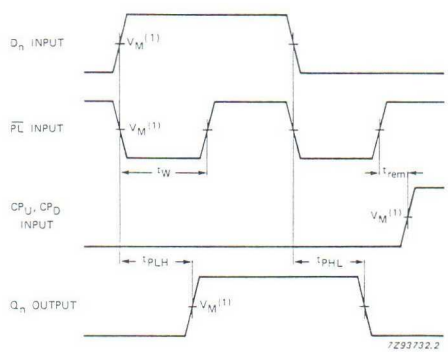


Fig. 9 Waveforms showing the parallel load input ($\overline{PL}$) and data (D_n) to Q_n output propagation delays and $\overline{PL}$ removal time to clock input (CP_U, CP_D).

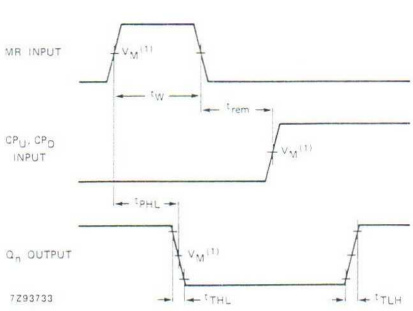


Fig. 10 Waveforms showing the master reset input (MR) pulse width, MR to Q_n propagation delays, MR to CP_U, CP_D removal time and output transition times.

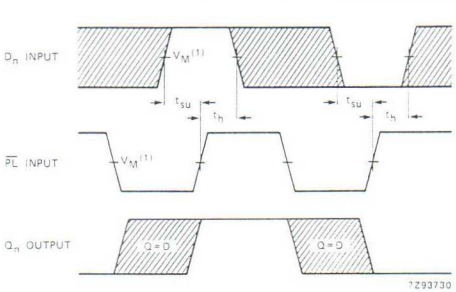


Fig. 11 Waveforms showing the data input (D_n) to parallel load input ($\overline{PL}$) set-up and hold times.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS (Cont'd)

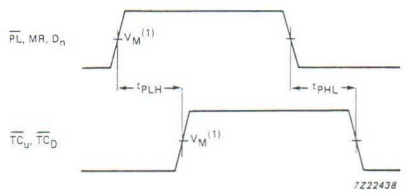


Fig. 12 Waveforms showing the data input (D_n), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TC_U}$, $\overline{TC_D}$) propagation delays.

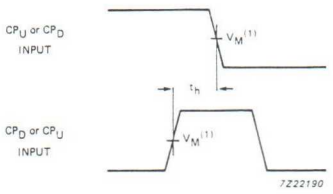


Fig. 13 Waveforms showing the CP_U to CP_D or CP_D to CP_U hold times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

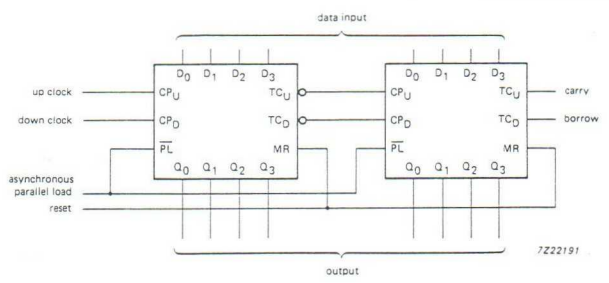


Fig. 14 Cascaded up/down counter with parallel load.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

FEATURES

- Shift-left and shift-right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold ("do nothing") mode
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs (S_0, S_1). As shown in the mode select table, data can be entered and shifted from left to right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) or, right to left ($Q_3 \rightarrow Q_2 \rightarrow Q_1$, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	14	15	ns
t_{PHL}	$\overline{MR}$ to Q_n		11	15	ns
f_{max}	maximum clock frequency		102	77	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset input (active LOW)
2	D_{SR}	serial data input (shift right)
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data input (shift left)
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	parallel outputs
16	V_{CC}	positive supply voltage

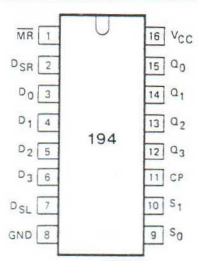


Fig. 1 Pin configuration.

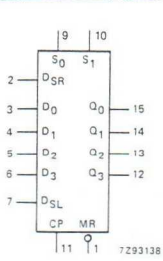


Fig. 2 Logic symbol.

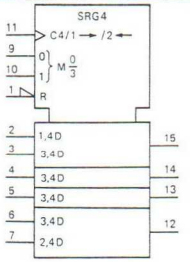


Fig. 3 IEC logic symbol.

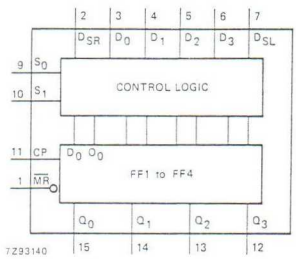


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
shift left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
shift right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

GENERAL DESCRIPTION (Cont'd.)

inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D_0 to D_3) are D-type inputs. Data appearing on the D_0 to D_3 inputs, when S_0 and S_1 are HIGH, is transferred to the Q_0 to Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

The "194" is similar in operation to the "195" universal shift register, with added features of shift-left without external connections and hold ("do nothing") modes of operation.

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

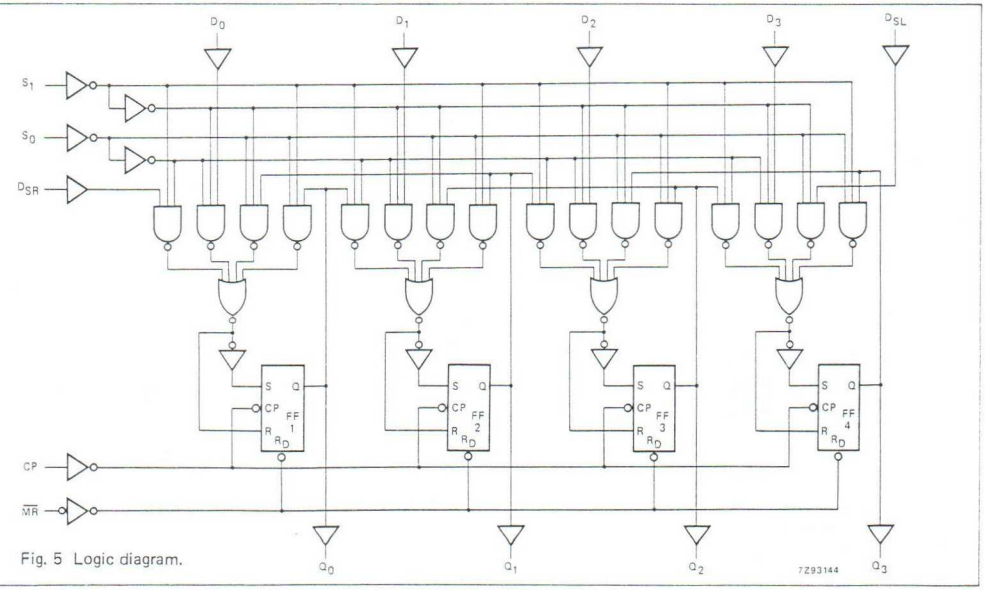


Fig. 5 Logic diagram.

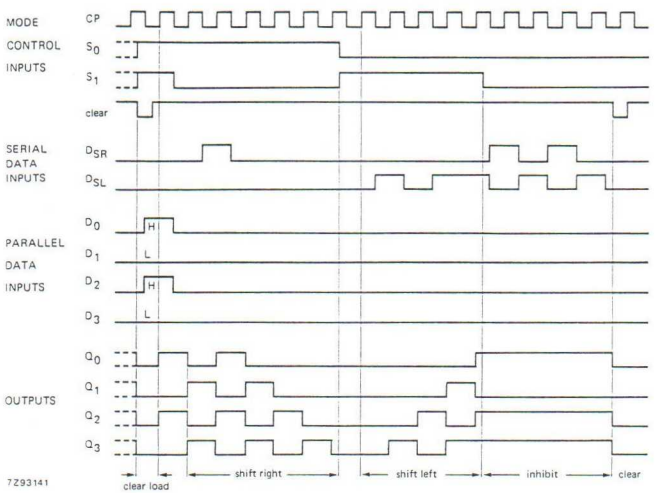


Fig. 6 Typical clear, clear-load, shift-right, shift-left, inhibit and clear timing sequences.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width; LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time S_0, S_1 to CP	80 16 12	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time D_{SR}, D_{SL} to CP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	
t_h	hold time D_n to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time S_0, S_1 to CP	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_{SR}, D_{SL} to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	
f_{max}	maximum clock pulse frequency	6.0 30 35	31 93 111		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.15
D_{SR}, D_{SL}	0.15
$\overline{CP}$	0.50
$\overline{MR}$	0.45
S_n	0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		18	32		40		48	ns	4.5	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		18	32		40		48	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
t_W	master reset pulse width; LOW	16	7		20		24		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	12	6		15		18		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	14	7		18		21		ns	4.5	Fig. 9
t_{su}	set-up time S_0, S_1 to CP	20	10		25		30		ns	4.5	Fig. 10
t_{su}	set-up time D_{SR}, D_{SL} to CP	14			18		21		ns	4.5	Fig. 9
t_h	hold time D_n to CP	0	−7		0		0		ns	4.5	Fig. 9
t_h	hold time S_0, S_1 to CP	0	−5		0		0		ns	4.5	Fig. 10
t_h	hold time D_{SR}, D_{SL} to CP	0	−7		0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	30	70		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

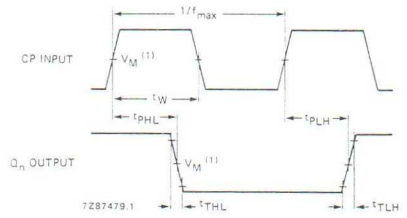


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

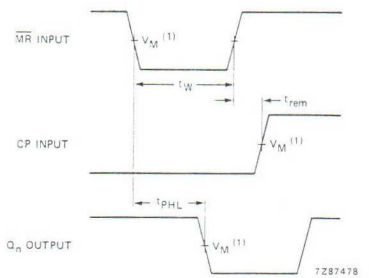


Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

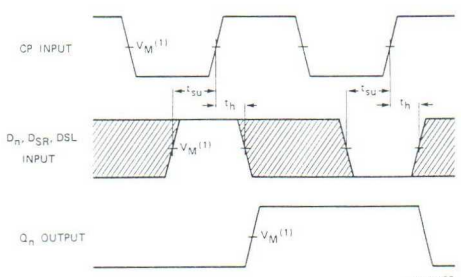


Fig. 9 Waveforms showing the set-up and hold times from the data inputs (D_n, D_{SR} and D_{SL}) to the clock (CP).

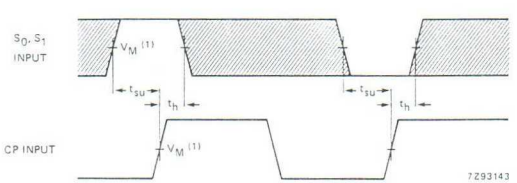


Fig. 10 Waveforms showing the set-up and hold times from the mode control inputs (S_n) to the clock input (CP).

Note to Figs 9 and 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT PARALLEL ACCESS SHIFT REGISTER

FEATURES

- Asynchronous master reset
- J, $\overline{K}$, (D) inputs to the first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complement output from the last stage
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-to-serial data transfer at very high speeds. The "195" operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the parallel load enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH and shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the $J\overline{K}$ type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW.

After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 to D_3) is transferred to the respective Q_0 to Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	15	ns
f_{max}	maximum clock frequency		57	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	105	105	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1,5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2	J	first stage J-input (active HIGH)
3	$\overline{K}$	first stage $\overline{K}$-input (active LOW)
4, 5, 6, 7	D_0 to D_3	parallel data inputs
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	$\overline{Q}_3$	inverted output from the last stage
15, 14, 13, 12	Q_0 to Q_3	parallel outputs
16	V_{CC}	positive supply voltage

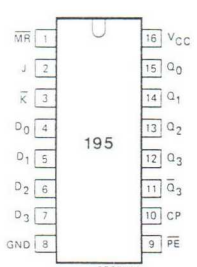


Fig. 1 Pin configuration.

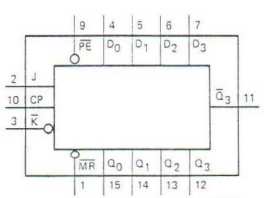


Fig. 2 Logic symbol.

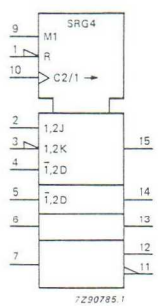


Fig. 3 IEC logic symbol.

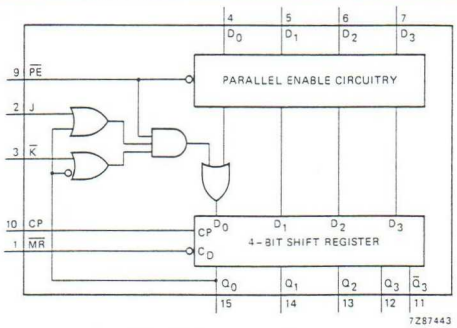


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition.
There is no restriction on the activity of the J, $\overline{K}$, D_n and $\overline{PE}$ inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

APPLICATIONS

- **Serial data transfer**
- **Parallel data transfer**
- **Serial-to-parallel data transfer**
- **Parallel-to-serial data transfer**

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

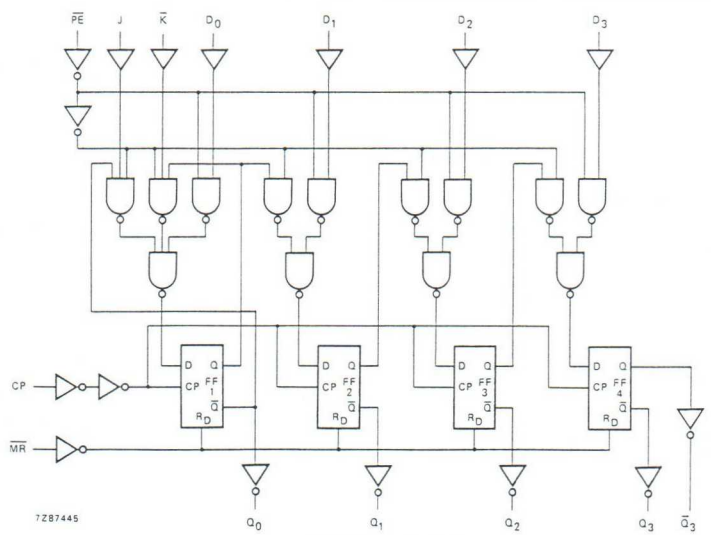


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time J to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 8 and 9
t_{su}	set-up time $\overline{K}$, $\overline{PE}$, D_n to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 8 and 9
t_h	hold time J, $\overline{K}$, $\overline{PE}$, D_n to CP	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Figs 8 and 9
f_{max}	maximum clock pulse frequency	6 30 35	17 52 62		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{PE}$	0.65
all others	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		18	32		40		48	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		17	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	16	6		20		24		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	16	6		20		24		ns	4.5	Fig. 7
t_{su}	set-up time J, $\overline{K}$, $\overline{PE}$ to CP	20	12		25		30		ns	4.5	Figs 8 and 9
t_{su}	set-up time D_n to CP	16	6		20		24		ns	4.5	Figs 8 and 9
t_h	hold time J, $\overline{K}$, $\overline{PE}$, D_n to CP	3	−5		3		3		ns	4.5	Figs 8 and 9
f_{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

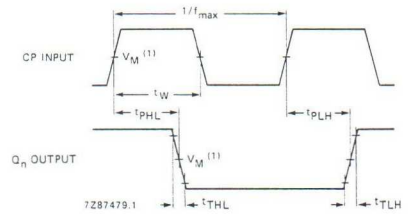


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

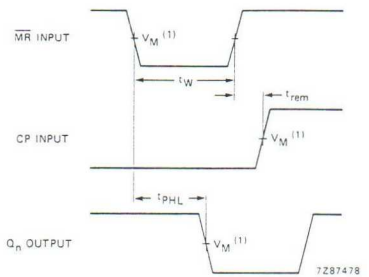


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time

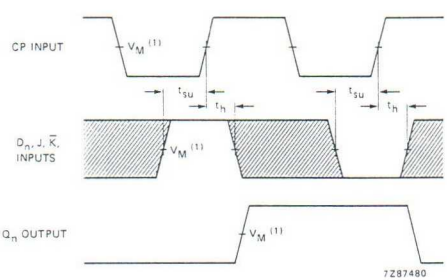


Fig. 8 Waveforms showing the data set-up and hold times for J, $\overline{K}$ and D_n inputs.

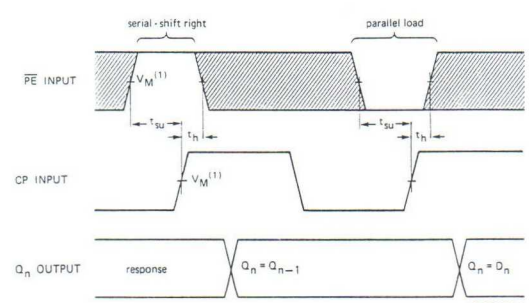


Fig. 9 Waveforms showing the set-up and hold times from the parallel enable input ($\overline{PE}$) to the clock (CP).

Note to Figs. 8 and 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

SUPERSEDES DATA OF APRIL 1988

DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- Pulse width variance is typically less than ± 5%
- Pin-out identical to "123"
- Overriding reset terminates output pulse
- nB inputs have hysteresis for improved noise immunity
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT221 are dual non-retriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input ($n\overline{A}$) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs (nQ, $n\overline{Q}$) are independent of further transitions of $n\overline{A}$ and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs ($n\overline{R}_D$). Input pulses may be of any duration relative to the output pulse.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	propagation delay $n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$ $n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 5 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	29 35	32 36	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	90	96	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.33 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 28 \times V_{CC}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_{EXT} = timing capacitance in pF
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   D = duty factor in %
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

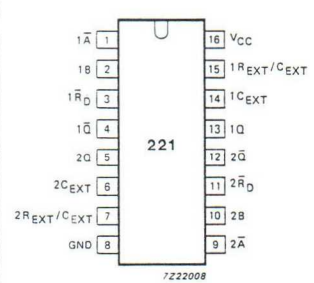


Fig. 1 Pin configuration.

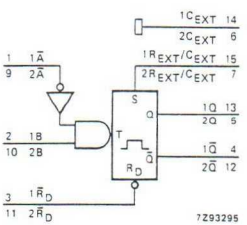


Fig. 2 Logic symbol.

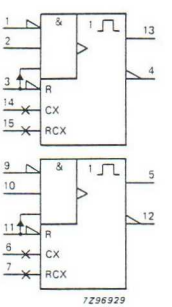


Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION

The output pulse width is defined by the following relationship:

$t_W = C_{EXT}R_{EXT}\ln 2$
$t_W = 0.7C_{EXT}R_{EXT}$

Pin assignments for the "221" are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{EXT} and/or C_{EXT}.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L (1)	H (1)
X	X	L	L (1)	H (1)
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍ (2)	⎍ (2)

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level
↓ = HIGH-to-LOW level
⎍ = one HIGH-level output pulse
⎍ = one LOW-level output pulse

Notes to the function table

1. If the monostable was triggered before this condition was established the pulse will continue as programmed.
2. For this combination the reset input must be LOW and the following sequence must be used: pin 1 (or 9) must be set HIGH or pin 2 (or 10) set LOW; then pin 1 (or 9) must be LOW and pin 2 (or 10) set HIGH. Now the reset input goes from LOW-to-HIGH and the device will be triggered.

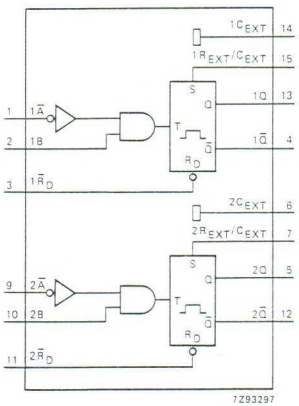


Fig. 4 Functional diagram.

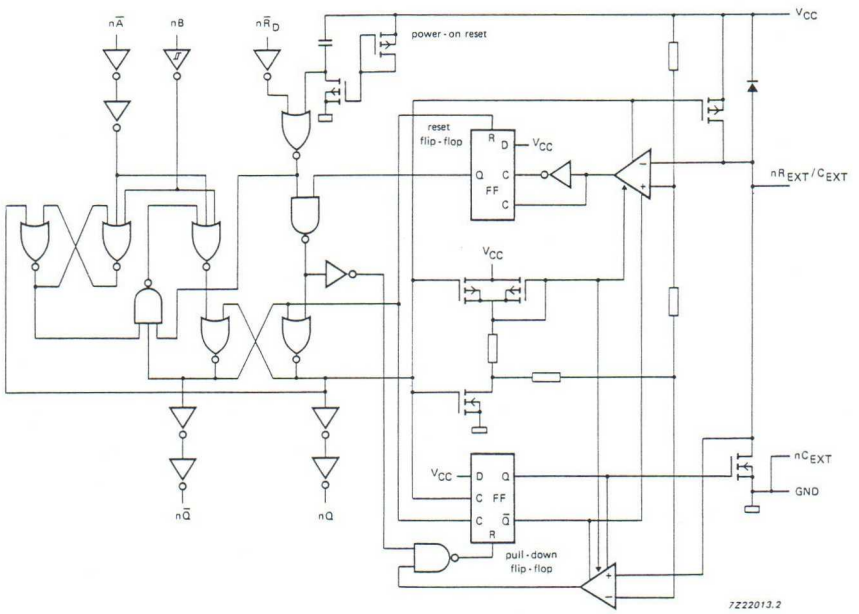


Fig. 5 Logic diagram.

Note

It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

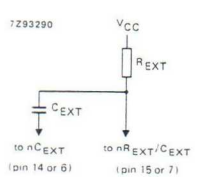


Fig. 6 Timing component connections.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except nR_{EXT}/C_{EXT})
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay (trigger) $n\bar{A}$, nB to nQ		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (trigger) $n\bar{R}_D$ to nQ		80 29 23	245 49 42		305 61 52		370 74 63	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\bar{A}$, nB to $n\bar{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\bar{R}_D$ to $n\bar{Q}$		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6,0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (reset) $n\bar{R}_D$ to $n\bar{Q}$		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{PHL}	propagation delay (reset) $n\bar{R}_D$ to nQ		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t_W	trigger pulse width $n\bar{A}$ = LOW	75 15 13	25 9 7		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	90 18 15	30 11 9		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width $n\bar{R}_D$ = LOW	75 15 13	25 9 7		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width $n\bar{Q}$ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	output pulse width nQ or $n\bar{Q}$		140		–		–		ns	2.0 4.5 6.0	C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; Fig. 10
t_W	output pulse width nQ or $n\bar{Q}$		1.5		–		–		μs	2.0 4.5 6.0	C_{EXT} = 1 nF; R_{EXT} = 2 kΩ; Fig. 10
t_W	output pulse width nQ or $n\bar{Q}$		7		–		–		μs	2.0 4.5 6.0	C_{EXT} = 1 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	pulse width match between circuits in the package		±2		–		–		%	4.5 to 5.5	C_{EXT} = 1000 pF; R_{EXT} = 10 kΩ

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{A}$ or nB	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
R_{EXT}	external timing resistor	10 2		1000 1000	– –		– –		kΩ	2.0 5.0	Fig. 12 Fig. 13
C_{EXT}	external timing capacitor	no limits							pF	2.0 5.0	Fig. 12 Fig. 13

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nB	0.30
$n\overline{A}$	0.50
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay (trigger) nA, $n\overline{R}_D$ to nQ		30	50		63		75	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PLH}	propagation delay (trigger) nB to nQ		24	42		53		63	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) nA to $n\overline{Q}$		26	44		55		66	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) nB to $n\overline{Q}$		21	35		44		53	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (trigger) $n\overline{R}_D$ to $n\overline{Q}$		26	43		54		65	ns	4.5	C_{EXT} = 0 pF R_{EXT} = 5 kΩ; Fig. 10
t_{PHL}	propagation delay (reset) $n\overline{R}_D$ to nQ		26	43		54		65	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11
t_{PLH}	propagation delay (reset) $n\overline{R}_D$ to $n\overline{Q}$		31	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig. 11

AC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 10
t_W	trigger pulse width nA = LOW	20	13		25		30		ns	4.5	Fig. 10
t_W	trigger pulse width nB = HIGH	20	13		25		30		ns	4.5	Fig. 10
t_W	pulse width $n\overline{R}_D$ = LOW	22	13		28		33		ns	4.5	Fig. 8
t_W	output pulse width $n\overline{Q}$ = LOW nQ = HIGH	630	700	770	602	798	595	805	μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		140		–		–		ns	4.5	C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		1.5		–		–		μs	4.5	C_{EXT} = 1 nF; R_{EXT} = 2 kΩ; Fig. 10
t_W	trigger pulse width nQ or $n\overline{Q}$		7		–		–		μs	4.5	C_{EXT} = 1 nF; R_{EXT} = 10 kΩ; Fig. 10
t_{rem}	removal time $n\overline{R}_D$ to nA or nB	20	12		25		30		ns	4.5	Fig. 9
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig. 13
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 13

AC WAVEFORMS

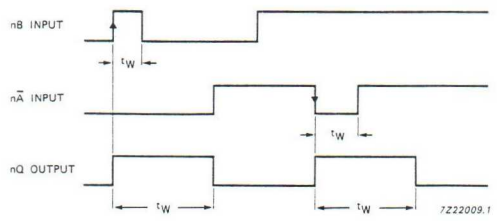


Fig. 7 Output pulse control; $n\overline{R}_D$ = HIGH.

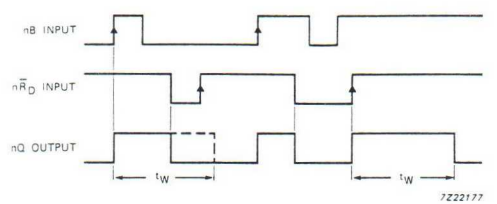


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; nĀ = LOW.

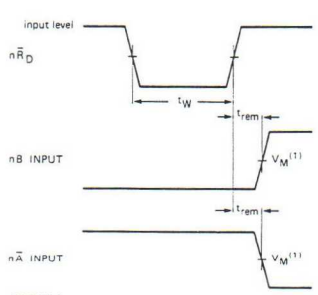


Fig. 9 Waveforms showing the removal times; $n\overline{R}_D$ to nĀ or nB.

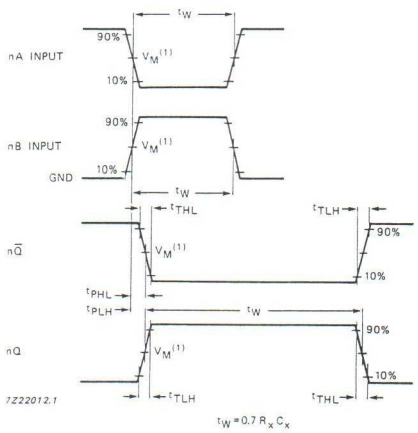


Fig. 10 Waveforms showing the triggering of One Shot by input nĀ or input nB for one period (t_W) and minimum pulse widths of the trigger inputs nĀ and nB.

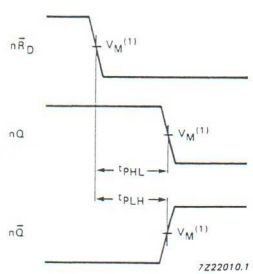


Fig. 11 Waveforms showing the reset to nQ and nQ̄ output propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

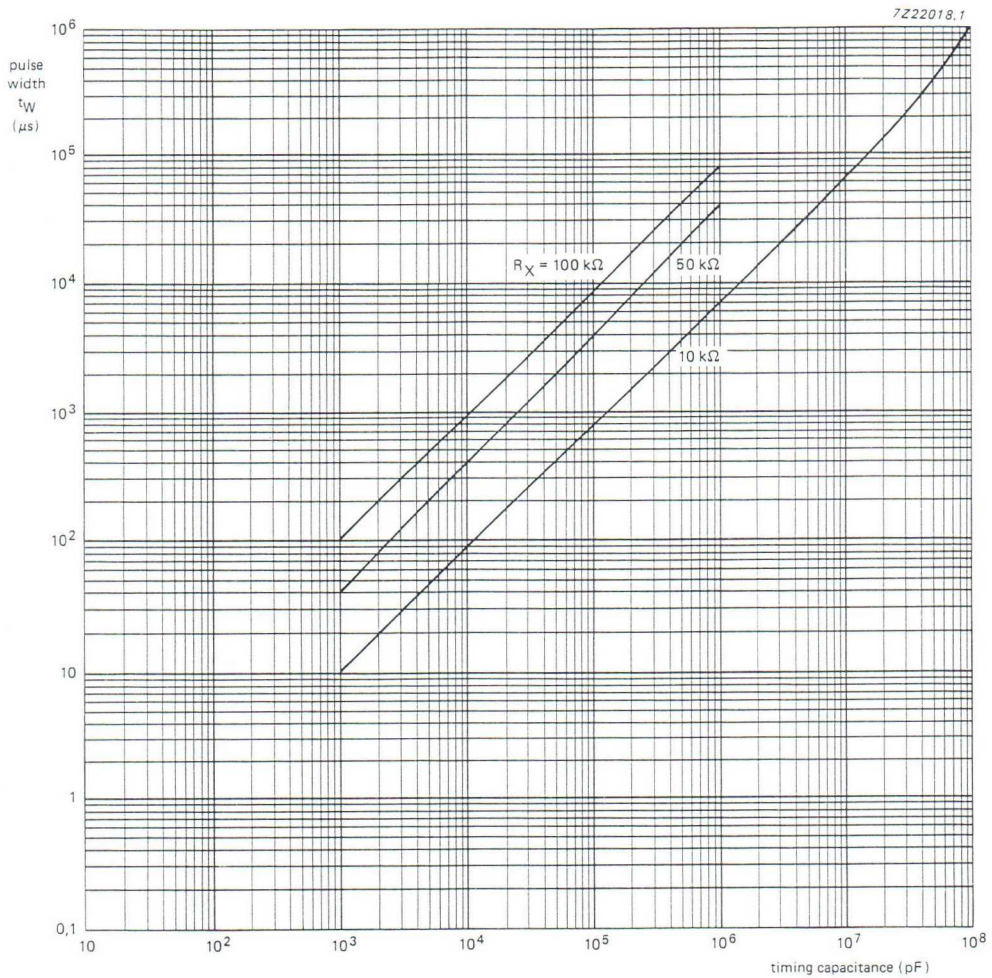


Fig. 12 HC typical output pulse width as a function of timing capacitance (V_{CC} = 2 V).

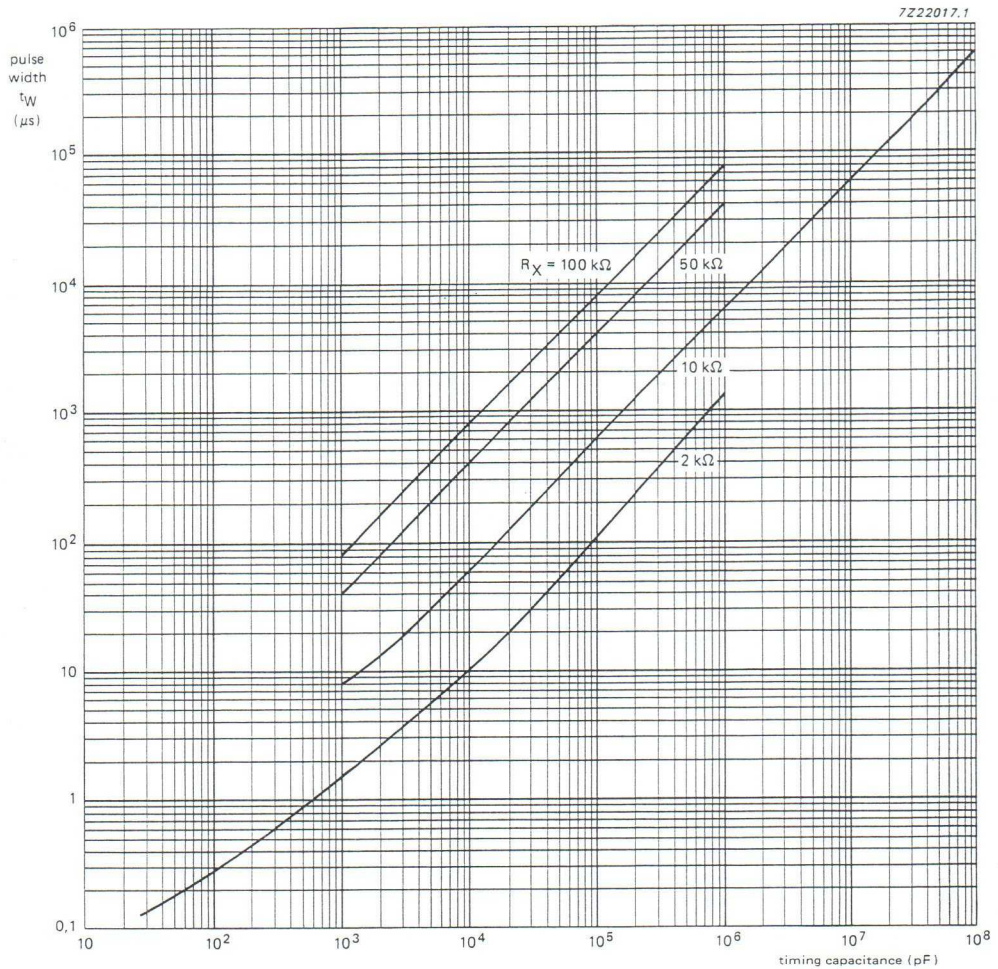


Fig. 13 HC/HCT typical output pulse width as a function of timing capacitance (V_{CC} = 4.5 V).

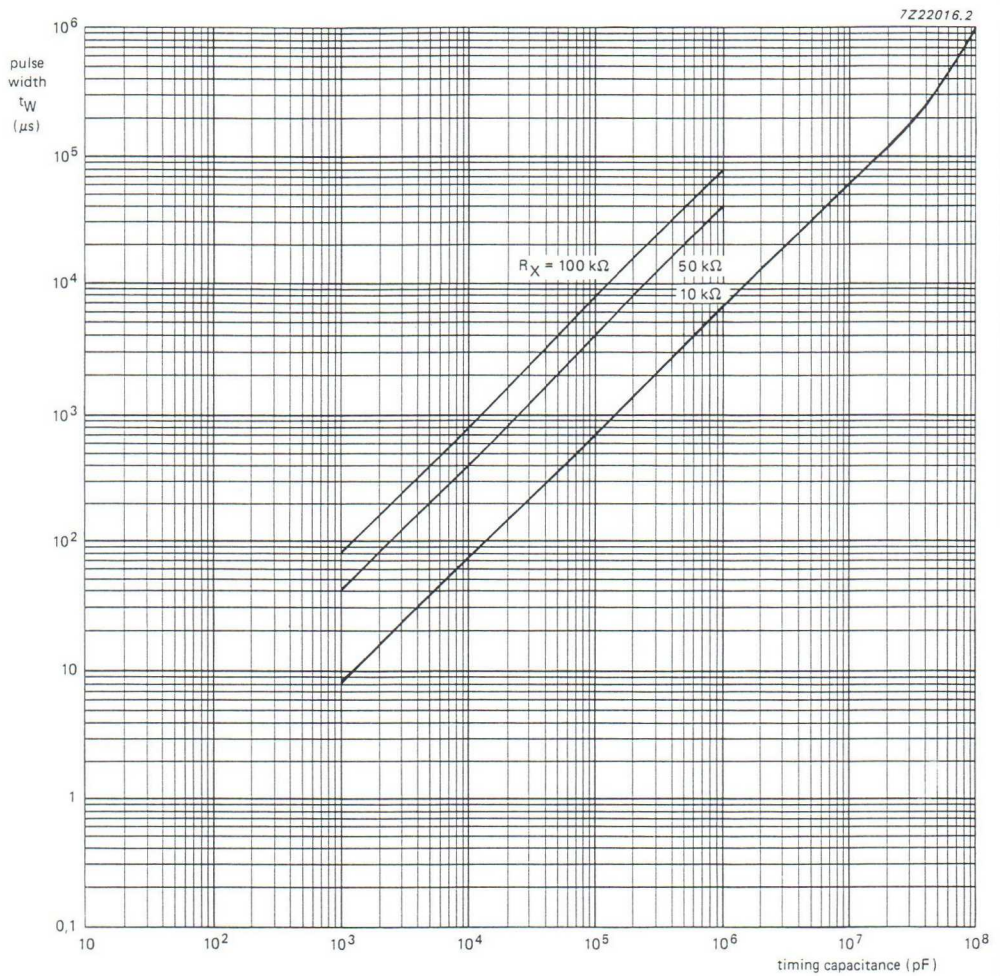


Fig. 14 HC typical output pulse width as a function of timing capacitance (V_{CC} = 6 V).

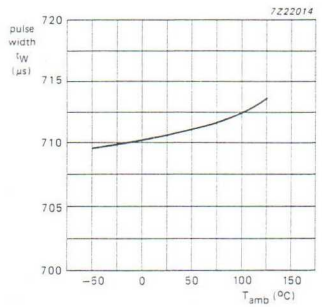


Fig. 15 Typical output pulse width as a function of temperature; C_X = 0.1 μF; R_X = 10 KΩ; V_{CC} = 5 V.

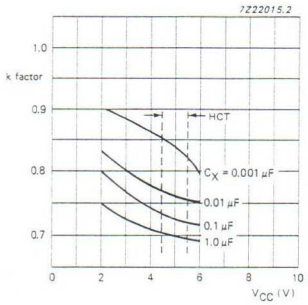


Fig. 16 k factor as a function of supply voltage; R_X = 10 KΩ; T_{amb} = 25 °C.

Power-down consideration

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 17.

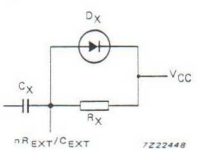


Fig. 17 Power-down protection circuit.

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT237 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT237 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The "237" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the "237" acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E_2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH.

The "237" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n $\overline{LE}$ to Y_n $\overline{E}_1$ to Y_n E_2 to Y_n	C_L = 15 pF V_{CC} = 5 V	 16 19 14 14	 19 21 17 17	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	60	63	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E_2	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	multiplexer outputs
16	V_{CC}	positive supply voltage

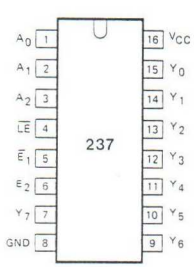


Fig. 1 Pin configuration.

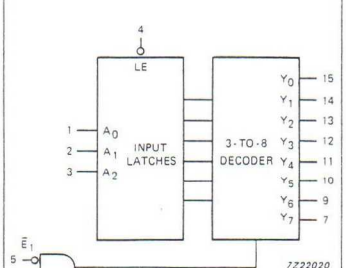


Fig. 2 Logic symbol.

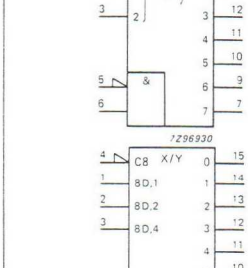


Fig. 3 IEC logic symbol.

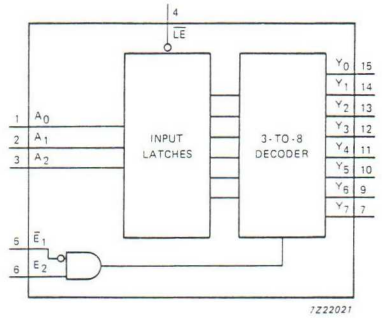


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

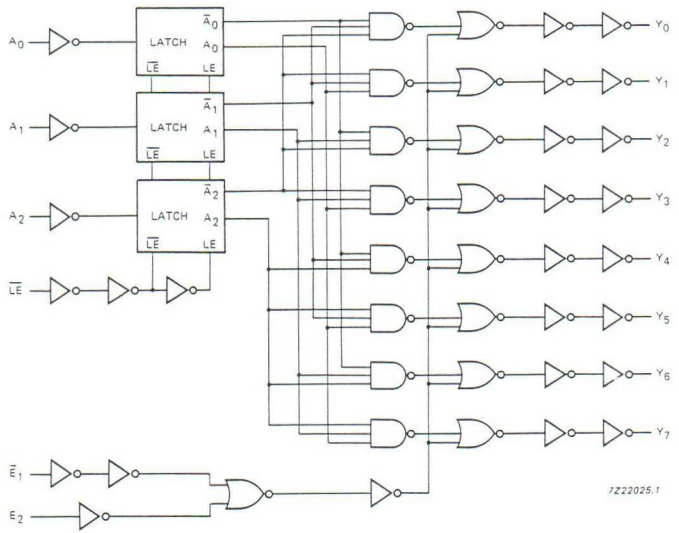


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y_n		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_1$ to Y_n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay E_2 to Y_n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{LE}$ pulse width LOW	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time A_n to $\overline{LE}$	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time A_n to $\overline{LE}$	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{E}_1$	1.50
E_2	1.50
$\overline{LE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y_n		25	42		53		63	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_1$ to Y_n		20	35		44		53	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay E_2 to Y_n		20	33		41		50	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	$\overline{LE}$ pulse width HIGH	10	5		13		15		ns	4.5	Fig. 8
t_{su}	set-up time A_n to $\overline{LE}$	10	2		13		15		ns	4.5	Fig. 8
t_h	hold time A_n to $\overline{LE}$	5	0		5		5		ns	4.5	Fig. 8

AC WAVEFORMS

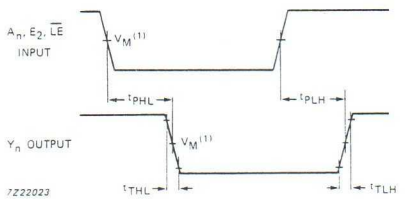


Fig. 6 Waveforms showing the address input (A_n) and enable inputs (E_2, $\overline{LE}$) to output (Y_n) propagation delays and the output transition times.

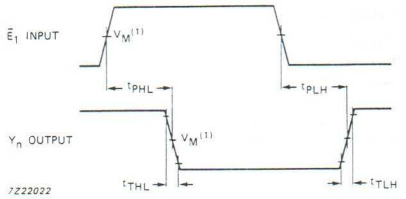


Fig. 7 Waveforms showing the enable input ($\overline{E}_1$) to output (Y_n) propagation delays and the output transition times.

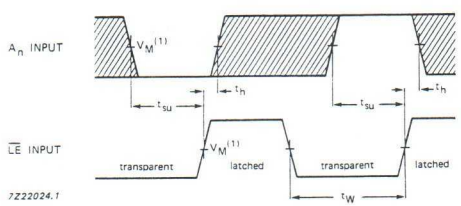


Fig. 8 Waveforms showing the data set-up, hold times for A_n input to $\overline{LE}$ input and the latch enable pulse width.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

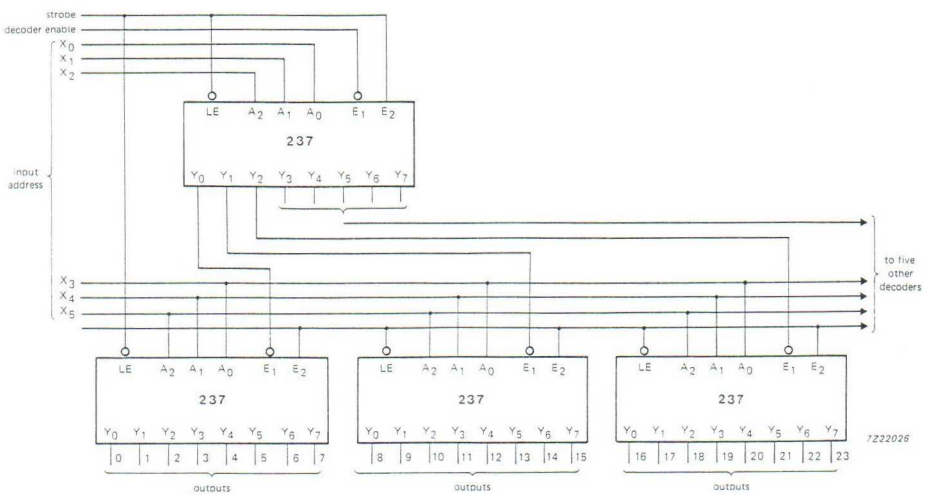


Fig. 9 6-to-64 line decoder with input address storage.

3-TO-8 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).
The "238" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be LOW unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n E_3 to Y_n $\overline{E}_n$ to Y_n	C_L = 15 pF V_{CC} = 5 V	14 16 17	18 20 21	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	72	76	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

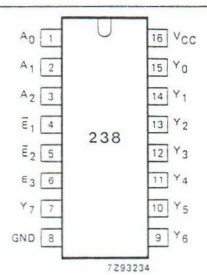


Fig. 1 Pin configuration.

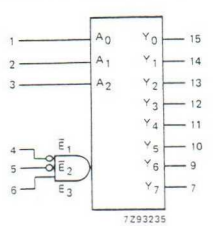
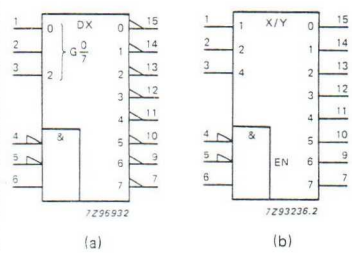


Fig. 2 Logic symbol.



(a) (b)

Fig. 3 IEC logic symbol.

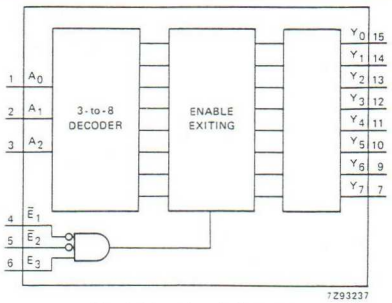


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

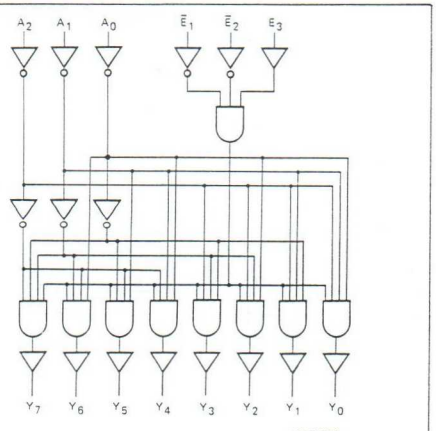


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay E_3 to Y_n		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to Y_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.70
$\overline{E}_n$	0.40
E_3	1.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay A_n to Y_n		21	35		44		53	ns	4.5	Fig. 6
t_{PLH}	propagation delay A_n to Y_n		17	35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay E_3 to Y_n		22	37		46		56	ns	4.5	Fig. 6
t_{PLH}	propagation delay E_3 to Y_n		18	37		46		56	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{E}_n$ to Y_n		21	35		44		53	ns	4.5	Fig. 7
t_{PLH}	propagation delay $\overline{E}_n$ to Y_n		18	35		44		53	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

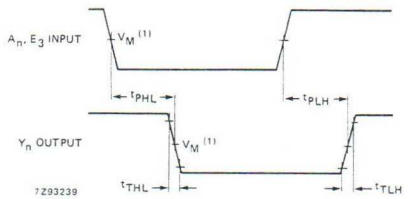


Fig. 6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times.

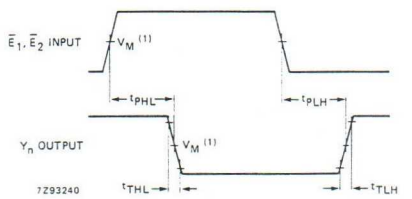


Fig. 7 Waveforms showing the enable input ($\overline{E}_n$) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

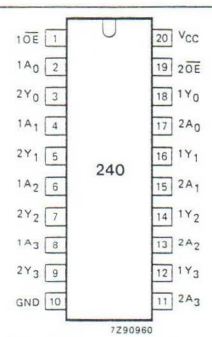


Fig. 1 Pin configuration.

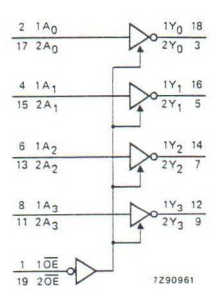


Fig. 2 Logic symbol.

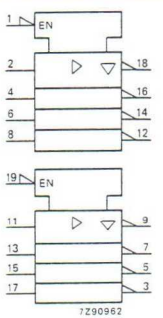


Fig. 3 IEC logic symbol.

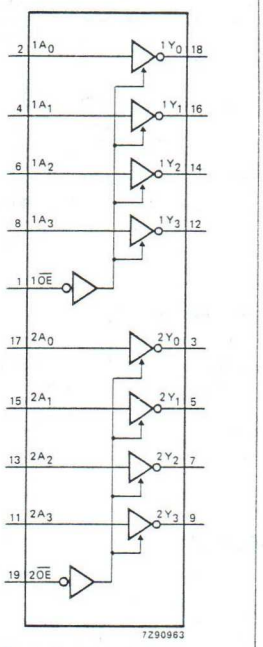


Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$1A_n$	1.50
$2A_n$	1.50
$1\overline{OE}$	0.70
$2\overline{OE}$	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		11	20		25		30	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		13	30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		13	25		31		38	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

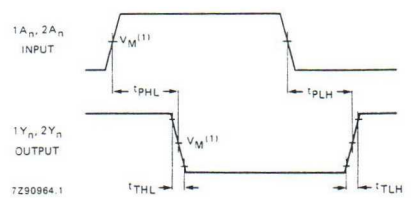


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

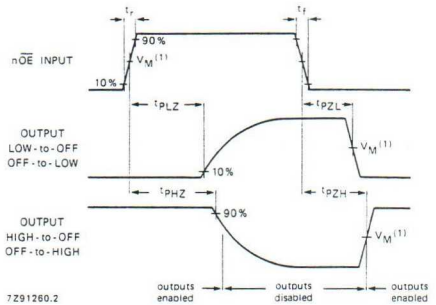


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT241 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT241 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	2OE	output enable input (active HIGH)
20	V_{CC}	positive supply voltage

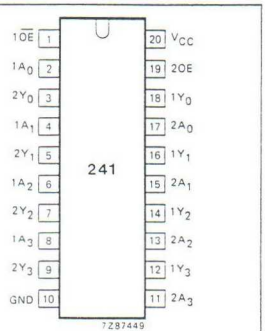


Fig. 1 Pin configuration.

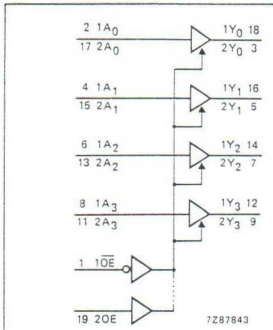


Fig. 2 Logic symbol.

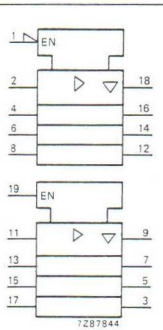


Fig. 3 IEC logic symbol.

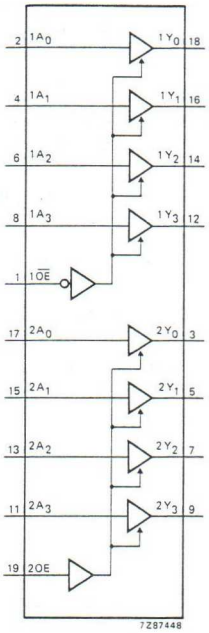


Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		25 9 7	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1A_n$	0.70
$2A_n$	0.70
$1\overline{OE}$	0.70
2OE	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		13	22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$		15	30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$		18	30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

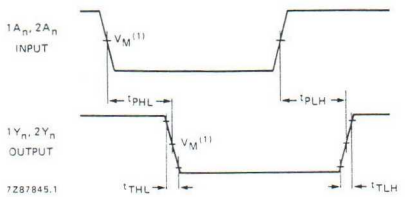


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

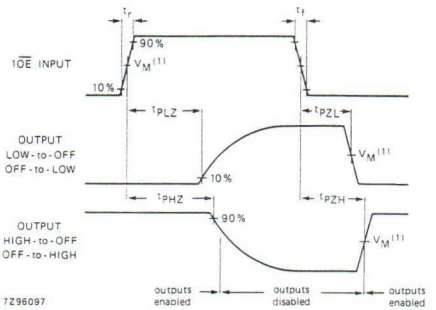


Fig. 6 Waveform showing the 3-state enable and disable times for input $1\overline{OE}$.

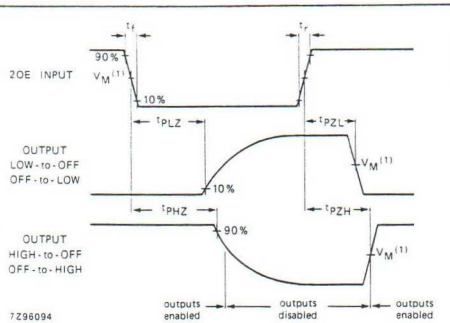


Fig. 7 Waveform showing the 3-state enable and disable times for input 2OE.

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.
HCT: $V_M = 1.3$ V; V_I = GND to 3 V.

QUAD BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT242 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT242 are quad bus transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{OE}_A$ and OE_B) can be used to isolate the buses.

The "242" is similar to the "243" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	29	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A_0 to A_3	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B_0 to B_3	data inputs/outputs
13	OE_B	output enable input
14	V_{CC}	positive supply voltage

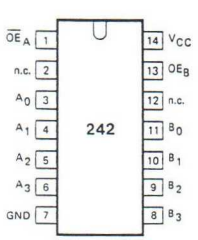


Fig. 1 Pin configuration.

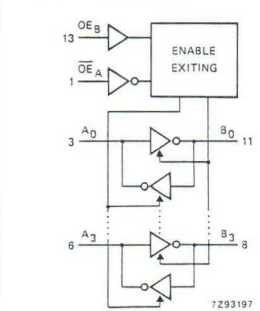


Fig. 2 Logic symbol.

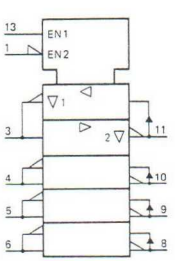


Fig. 3 IEC logic symbol.

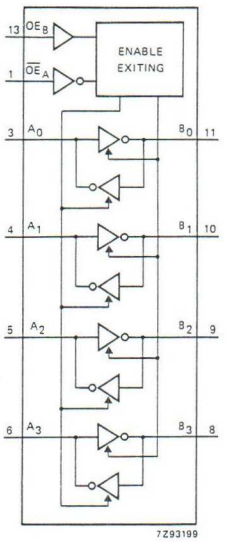


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	inputs	$B = \overline{A}$
H	L	Z	Z
L	H	Z	Z
H	H	$A = \overline{B}$	inputs

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.10
B_n	1.10
$\overline{OE}_A$	1.00
OE_B	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n		12	20		25		30	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		16	34		43		51	ns	4.5	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		22	35		44		53	ns	4.5	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

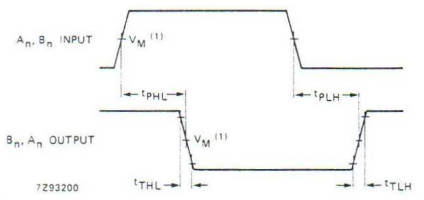


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

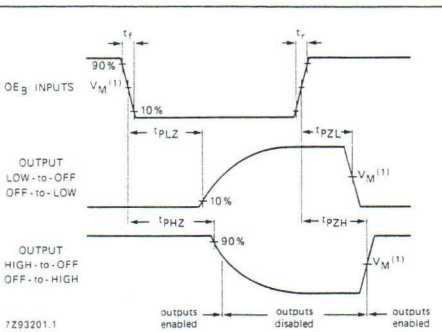


Fig. 6 Waveforms showing the 3-state enable and disable times for input OE_B.

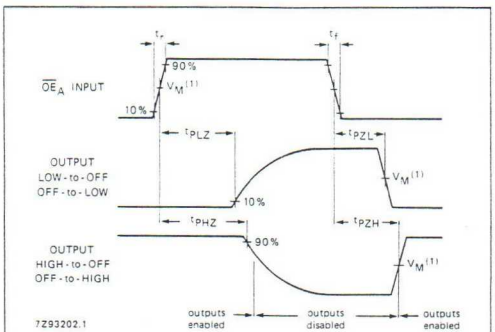


Fig. 7 Waveforms showing the 3-state enable and disable times for input $\overline{OE}_A$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BUS TRANSCEIVER; 3-STATE

FEATURES

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{OE}_A$ and OE_B) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	6	11	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	26	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A_0 to A_3	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B_0 to B_3	data inputs/outputs
13	OE_B	output enable input
14	V_{CC}	positive supply voltage

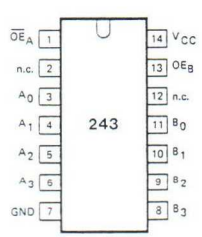


Fig. 1 Pin configuration.

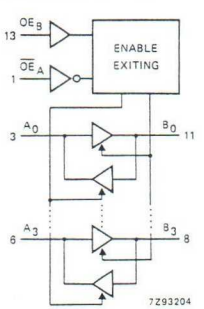


Fig. 2 Logic symbol.

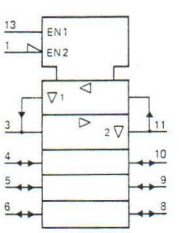


Fig. 3 IEC logic symbol.

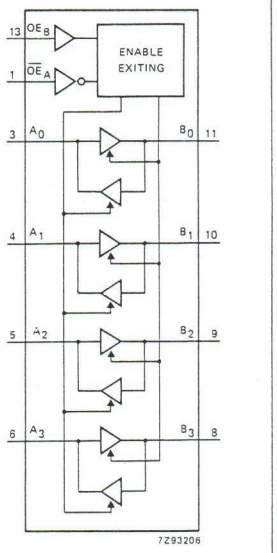


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	inputs	B = A
H	L	Z	Z
L	H	Z	Z
H	H	A = B	inputs

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND =0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		61 22 18	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Figs 6 and 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.10
B_n	1.10
$\overline{OE}_A$	1.00
OE_B	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n		13	22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		18	34		43		51	ns	4.5	Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_A$ to A_n or B_n; OE_B to A_n or B_n		23	35		44		53	ns	4.5	Figs 6 and 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

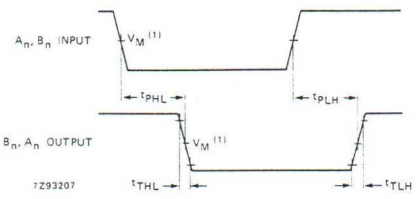


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

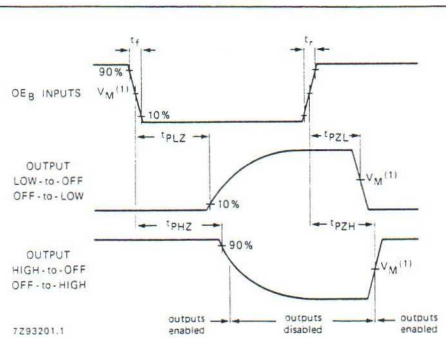


Fig. 6 Waveforms showing the 3-state enable and disable times for input OE_B.

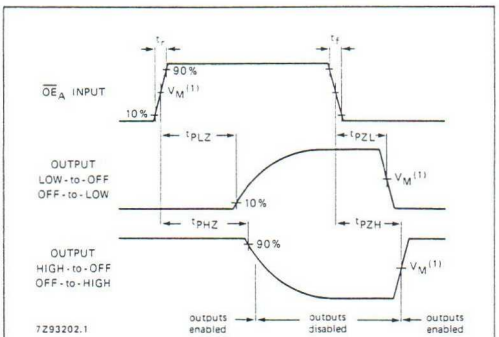


Fig. 7 Waveforms showing the 3-state enable and disable times for input $\overline{OE}_A$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

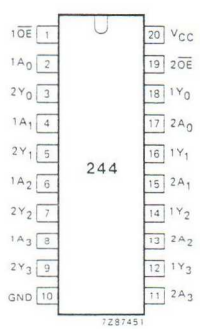


Fig. 1 Pin configuration.

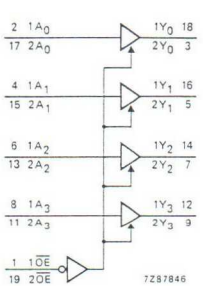


Fig. 2 Logic symbol.

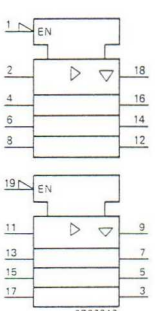


Fig. 3 IEC logic symbol.

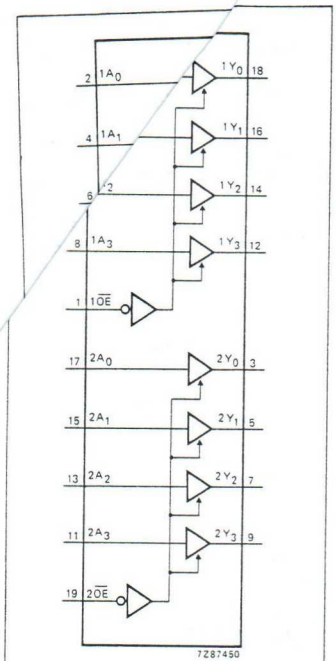


Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		30 11 9	110 22 19		145 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1A_n$	0.70
$2A_n$	0.70
$1\overline{OE}$	0.70
$2\overline{OE}$	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$		13	22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		15	30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		15	25		31		38	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

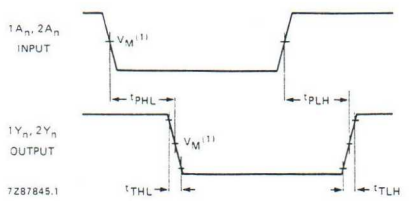


Fig. 5 Waveforms showing th input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

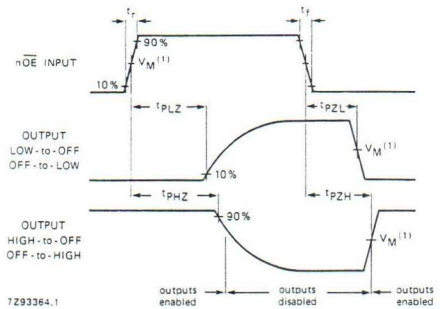


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS TRANSCEIVER; 3-STATE

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
The "245" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "245" is similar to the "640" but has true (non-inverting) outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

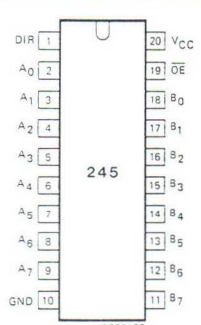


Fig. 1 Pin configuration.

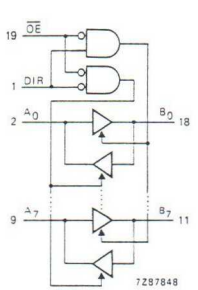


Fig. 2 Logic symbol.

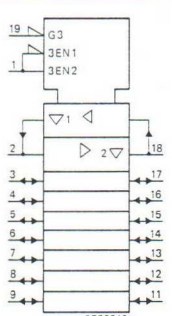


Fig. 3 IEC logic symbol.

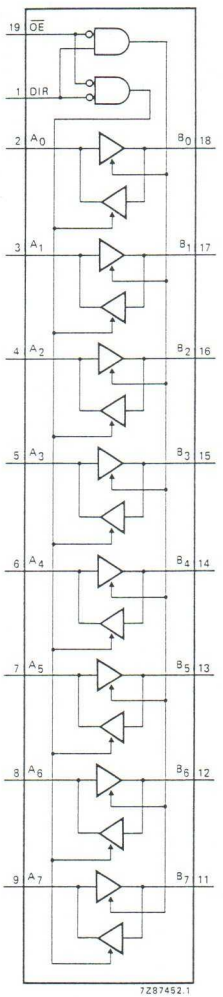


Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n signalname DIR		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n signalname DIR		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.40
B_n	0.40
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n		12	22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n signalname DIR		16	30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n signalname DIR		16	30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

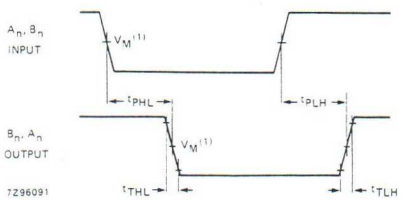


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

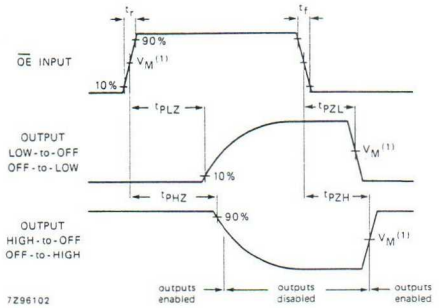


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-INPUT MULTIPLEXER; 3-STATE

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions.

Assertion (Y) and negation ($\overline{Y}$) outputs are both provided.

The output enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE}.(I_0.\overline{S}_0.\overline{S}_1.\overline{S}_2 + I_1.S_0.\overline{S}_1.\overline{S}_2 + I_2.\overline{S}_0.S_1.\overline{S}_2 + I_3.S_0.S_1.\overline{S}_2 + I_4.\overline{S}_0.\overline{S}_1.S_2 + I_5.S_0.\overline{S}_1.S_2 + I_6.\overline{S}_0.S_1.S_2 + I_7.S_0.S_1.S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Y I_n to $\overline{Y}$ S_n to Y S_n to $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	15 17 20 21	19 19 20 21	ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{OE}$	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

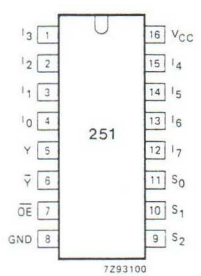


Fig. 1 Pin configuration.

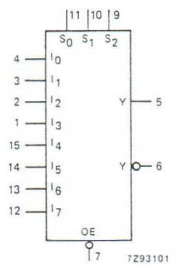


Fig. 2 Logic symbol.

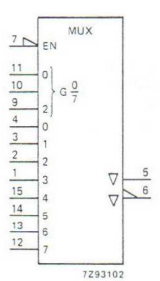


Fig. 3 IEC logic symbol.

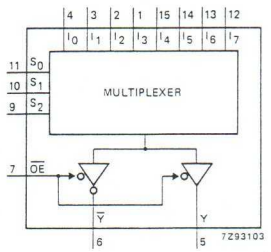


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

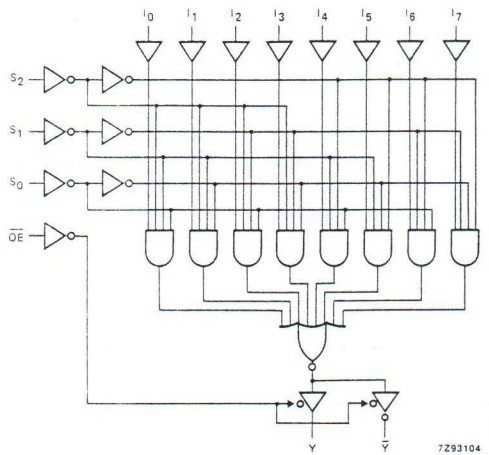


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y		50 18 14	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_n to Y		66 24 19	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$		69 25 20	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$		36 13 10	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$		39 14 11	140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	1.00
S_0	1.50
S_1, S_2	1.50
$\overline{OE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I_n to Y		22	35		44		53	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay I_n to $\overline{Y}$		22	35		44		53	ns	4.5	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay S_n to Y		24	44		55		66	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay S_n to $\overline{Y}$		25	44		55		66	ns	4.5	Fig. 7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$		13	28		35		42	ns	4.5	Fig. 8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$		14	28		35		42	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

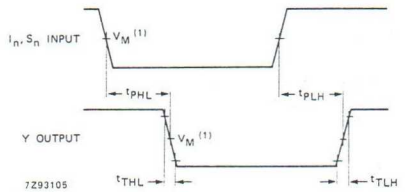


Fig. 6 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays and the output transition times.

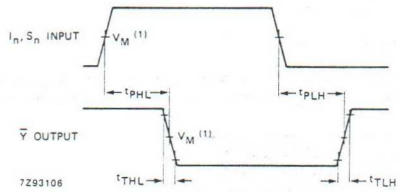


Fig. 7 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output ($\overline{Y}$) propagation delays and the output transition times.

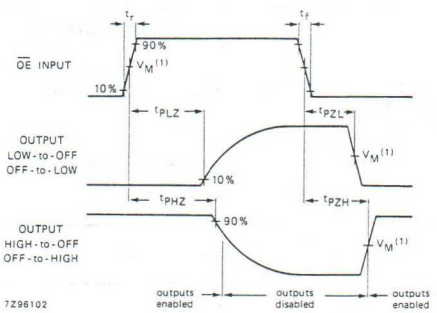


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S_0, S_1).

When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state.

The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:

$1Y = 1\overline{OE}(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0+ +1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$

$2Y = 2\overline{OE}(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0+ +2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$

APPLICATIONS

- Data selectors
- Data multiplexers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY; S_n to nY	C_L = 15 pF V_{CC} = 5 V	17 18	17 19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

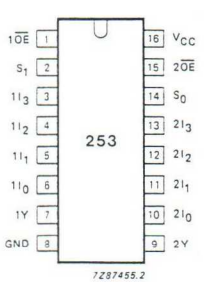


Fig. 1 Pin configuration.

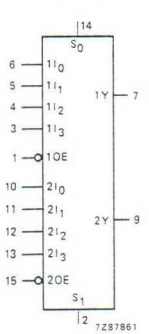


Fig. 2 Logic symbol.

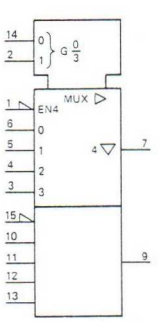


Fig. 3 IEC logic symbol.

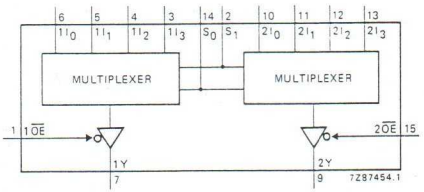


Fig. 4 Functional diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\overline{OE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

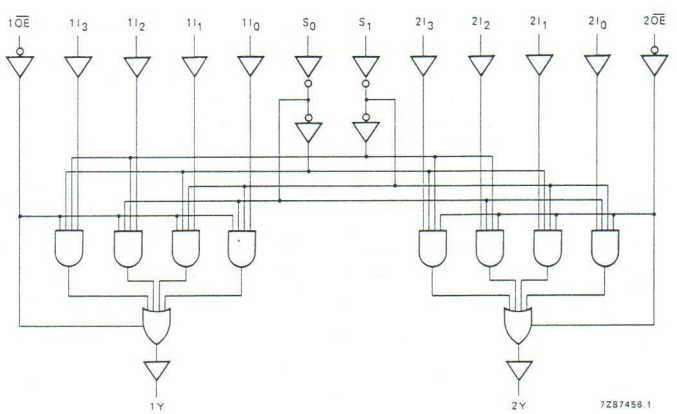


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay S_n to nY		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1I_n$	0.40
$2I_n$	0.40
$n\overline{OE}$	1.10
S_0	1.10
S_1	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		20	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY		22	40		50		60	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		14	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		13	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

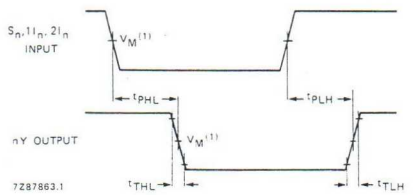


Fig. 6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.

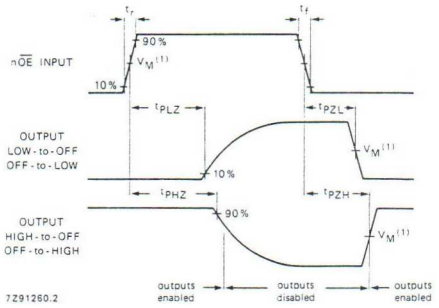


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH.

Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE}.(1I_1.S + 1I_0.\overline{S})$

$2Y = \overline{OE}.(2I_1.S + 2I_0.\overline{S})$

$3Y = \overline{OE}.(3I_1.S + 3I_0.\overline{S})$

$4Y = \overline{OE}.(4I_1.S + 4I_0.\overline{S})$

The "257" is identical to the "258" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	C_L = 15 pF V_{CC} = 5 V	11 14	13 17	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	45	45	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 13, 10	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

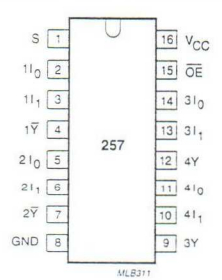


Fig. 1 Pin configuration.

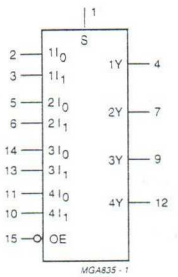


Fig. 2 Logic symbol.

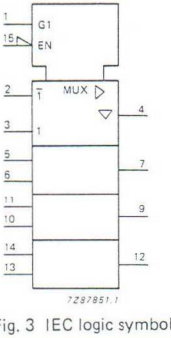


Fig. 3 IEC logic symbol.

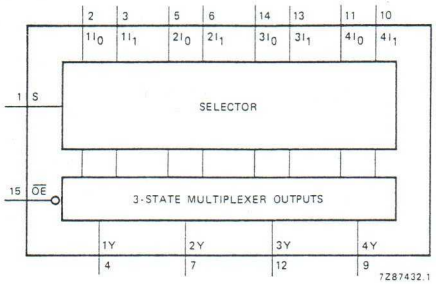


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

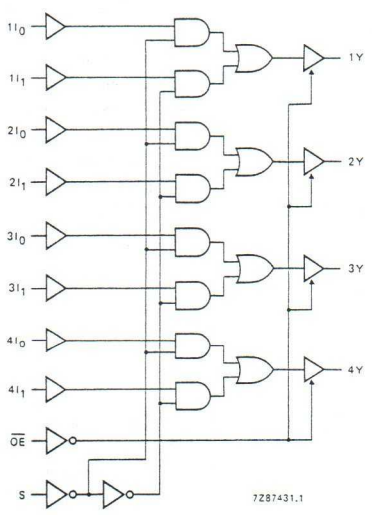


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nI_0	0.40
nI_1	0.40
$\overline{OE}$	1.35
S	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		16	30		38		45	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to nY		20	35		44		53	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY		15	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY		16	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

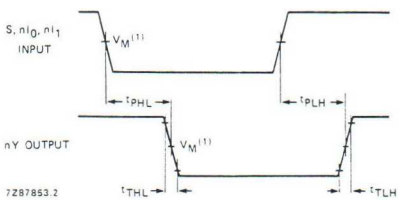


Fig. 6 Waveforms showing the input (nI_0, nI_1) to output (nY) propagation delays and the output transition times.

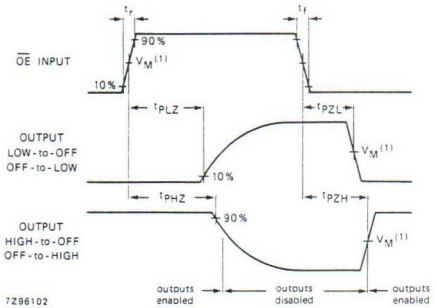


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT MULTIPLEXER; 3-STATE; INVERTING

FEATURES

- Inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT258 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT258 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH.

Data appears at the outputs ($1\overline{Y}$ to $4\overline{Y}$) in inverted form from the select inputs.

The "258" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$$1\overline{Y} = \overline{\overline{OE}.(1I_1.S + 1I_0.\overline{S})}$$
$$2\overline{Y} = \overline{\overline{OE}.(2I_1.S + 2I_0.\overline{S})}$$
$$3\overline{Y} = \overline{\overline{OE}.(3I_1.S + 3I_0.\overline{S})}$$
$$4\overline{Y} = \overline{\overline{OE}.(4I_1.S + 4I_0.\overline{S})}$$

The "258" is identical to the "257" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$ S to $n\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	9 14	13 16	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	38	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 13, 10	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 12, 9	$1\overline{Y}$ to $4\overline{Y}$	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

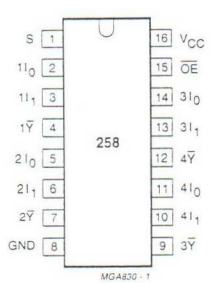


Fig. 1 Pin configuration.

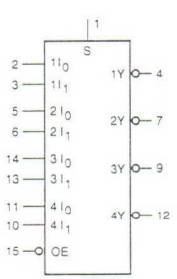


Fig. 2 Logic symbol.

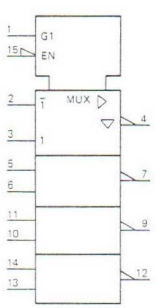


Fig. 3 IEC logic symbol.

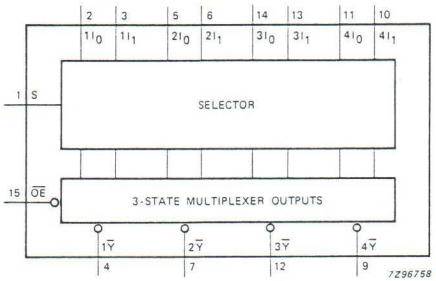


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

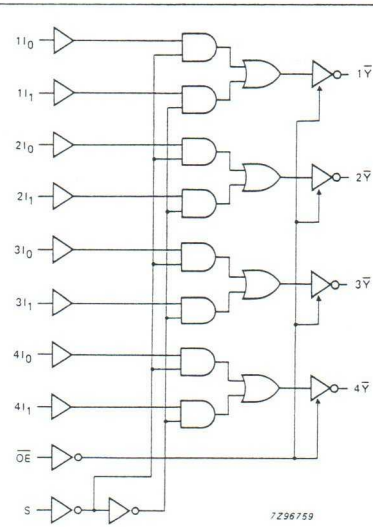


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to $n\overline{Y}$; nI_1 to $n\overline{Y}$		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$		47 17 14	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $n\overline{Y}$		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $n\overline{Y}$		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nI_0	0.50
nI_1	0.50
$\overline{OE}$	1.50
S	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to $n\overline{Y}$; nI_1 to $n\overline{Y}$		16	27		34		41	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S to $n\overline{Y}$		19	34		43		51	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $n\overline{Y}$		18	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $n\overline{Y}$		17	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

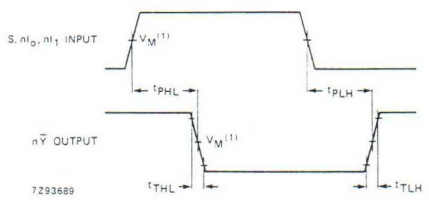


Fig. 6 Waveforms showing input (nI_0, nI_1, S) to output ($n\overline{Y}$) propagation delays and the output transition times.

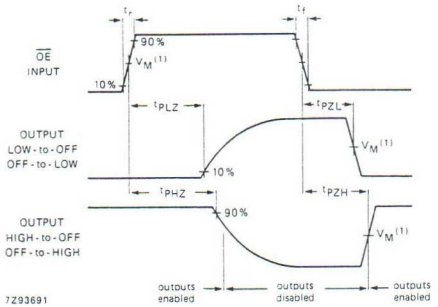


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT ADDRESSABLE LATCH

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.

The "259" also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D to Q_n	C_L = 15 pF; V_{CC} = 5 V	18	20	ns
	propagation delay A_n, $\overline{LE}$ to Q_n		17	20	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		15	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q_0 to Q_7	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V_{CC}	positive supply voltage

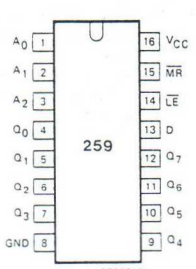


Fig. 1 Pin configuration.

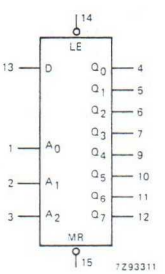


Fig. 2 Logic symbol.

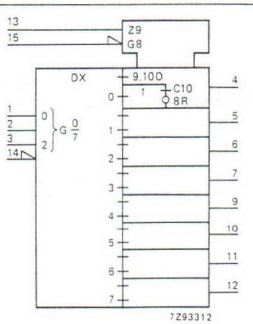


Fig. 3 IEC logic symbol.

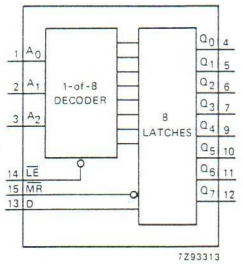


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

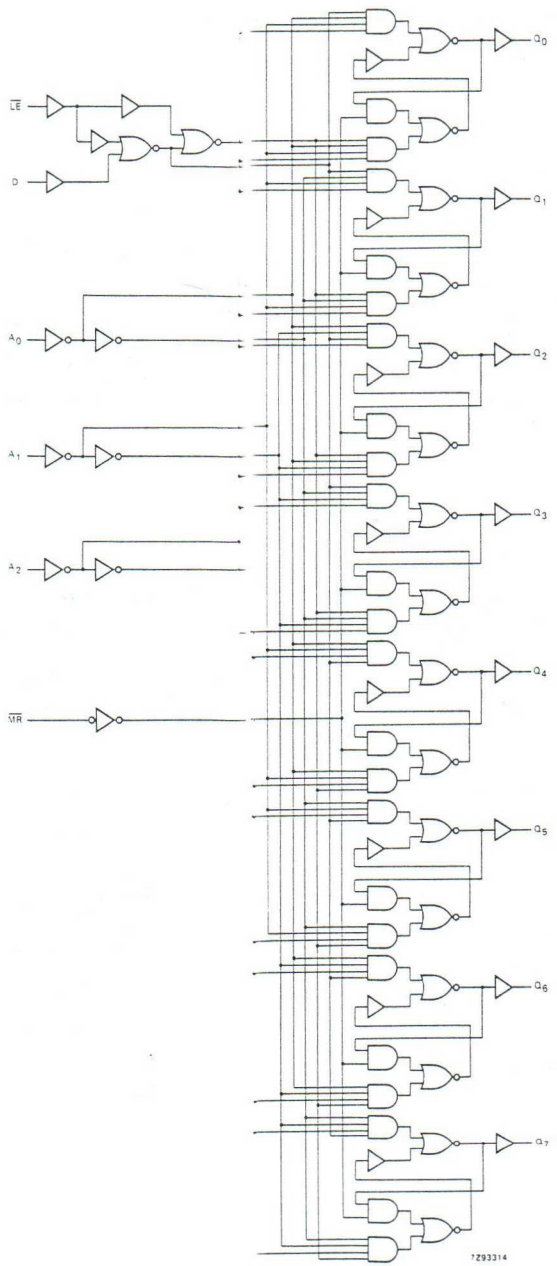


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D to Q_n		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q_n		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t_W	$\overline{LE}$ pulse width HIGH or LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{MR}$ pulse width LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D, A_n to $\overline{LE}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t_h	hold time D to $\overline{LE}$	0 0 0	−19 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time A_n to $\overline{LE}$	2 2 2	−11 −4 −3		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
$\overline{LE}$	1.50
D	1.20
$\overline{MR}$	0.75

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D to Q_n		23	39		49		59	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		25	41		51		62	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q_n		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		23	39		49		59	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t_W	$\overline{LE}$ pulse width LOW	19	11		24		29		ns	4.5	Fig. 6
t_W	$\overline{MR}$ pulse width LOW	18	10		23		27		ns	4.5	Fig. 9
t_{su}	set-up time D to $\overline{LE}$	17	10		21		26		ns	4.5	Fig. 10
t_{su}	set-up time A_n to $\overline{LE}$	17	10		21		26		ns	4.5	Fig. 11
t_h	hold time D to $\overline{LE}$	0	−8		0		0		ns	4.5	Fig. 10
t_h	hold time A_n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig. 11

AC WAVEFORMS

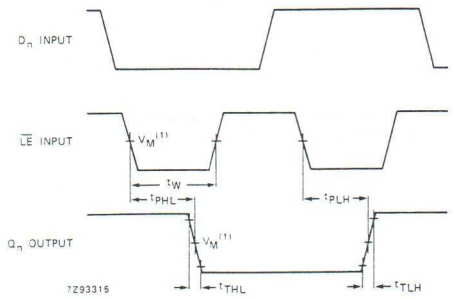


Fig. 6 Waveforms showing the enable input ($\overline{LE}$) to output (Q_n) propagation delays, the enable input pulse width and the output transition times.

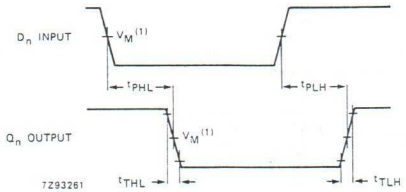


Fig. 7 Waveforms showing the data input (D) to output (Q_n) propagation delays and the output transition times.

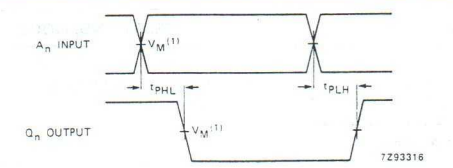


Fig. 8 Waveforms showing the address inputs (A_n) to outputs (Q_n) propagation delays and the output transition times.

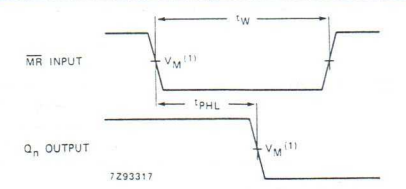


Fig. 9 Waveforms showing the conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.

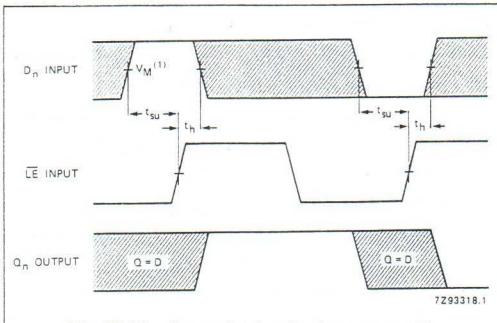


Fig. 10 Waveforms showing the data set-up and hold times for D input to $\overline{LE}$ input.

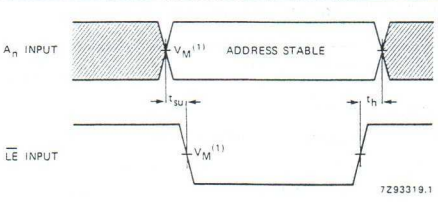


Fig. 11 Waveforms showing the address set-up and hold times for A_n inputs to $\overline{LE}$ input.

Note to Figs 10 and 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See "377" for clock enable version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability; standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	15 15	15 20	ns ns
f_{max}	maximum clock frequency		66	36	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

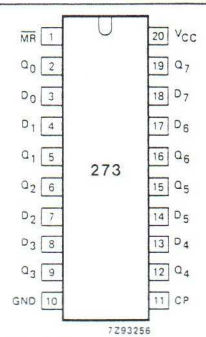


Fig. 1 Pin configuration.

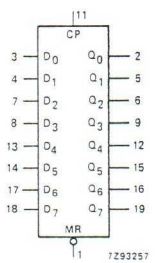


Fig. 2 Logic symbol.

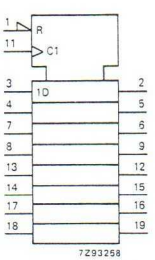


Fig. 3 IEC logic symbol.

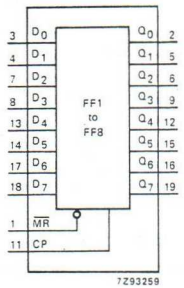


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH transition
X = don't care

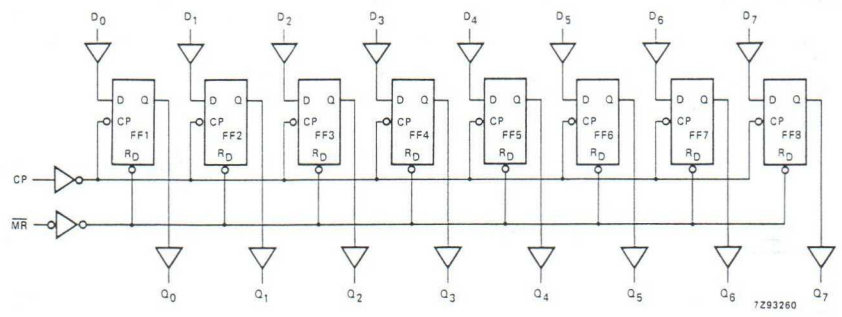


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		41 15 13	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		44 16 14	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 15		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	50 10 9	−6 −2 −2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to CP	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	20.6 103 122		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	1.00
CP	1.75
D_n	0.15

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		16	30		38		45	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		23	34		43		51	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	16	8		20		24		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	10	−2		13		15		ns	4.5	Fig. 7
t_{su}	set-up time D_n to CP	12	5		15		18		ns	4.5	Fig. 8
t_h	hold time D_n to CP	3	−4		3		3		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	56		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

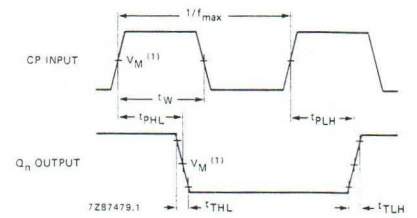


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

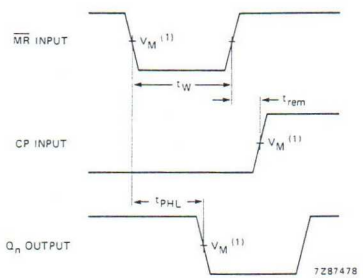


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

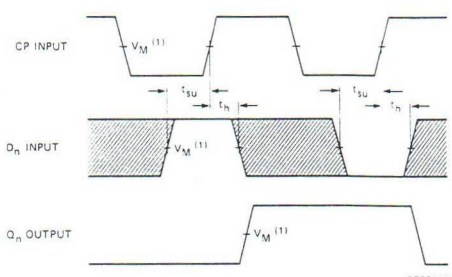


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

FEATURES

- Word-length easily expanded by cascading
- Similar pin configuration to the "180" for easy system up-grading
- Generates either odd or even parity for nine data bits
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT280 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT280 are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits.

The even parity output (Σ_E) is HIGH when an even number of data inputs (I_0 to I_8) are HIGH. The odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the even outputs (Σ_E) of up to nine parallel devices to the data inputs of the final stage.
For a single-chip 16-bit even/odd parity generator/checker, see PC74HC/HCT7080.

APPLICATIONS

- 25-line parity generator/checker
- 81-line parity generator/checker

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_E I_n to Σ_O	C_L = 15 pF V_{CC} = 5 V	17 20	18 22	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	65	65	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 9, 10, 11, 12, 13, 1, 2, 4	I_0 to I_8	data inputs
5, 6	Σ_E, Σ_O	parity outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

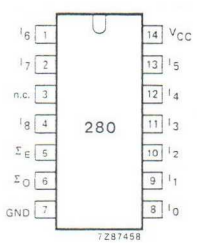


Fig. 1 Pin configuration.

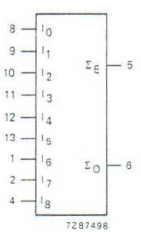


Fig. 2 Logic symbol.

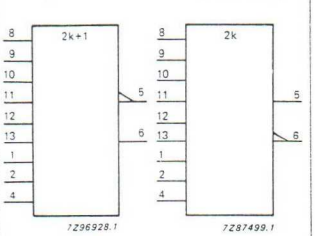


Fig. 3 IEC logic symbol.

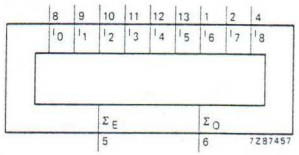


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS	OUTPUTS	
number of HIGH data inputs (I_0 to I_8)	Σ_E	Σ_O
even	H	L
odd	L	H

H = HIGH voltage level
L = LOW voltage level

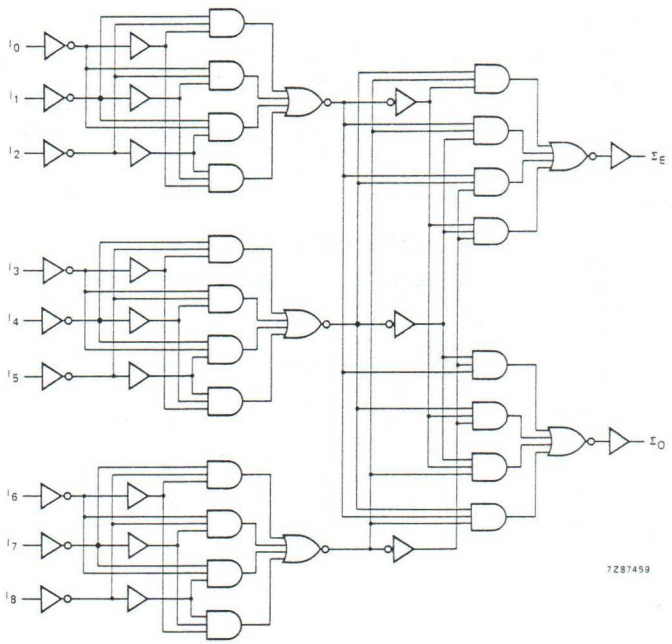


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I_n to Σ_E		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay I_n to Σ_O		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_E		21	42		53		63	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay I_n to Σ_O		26	45		56		68	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

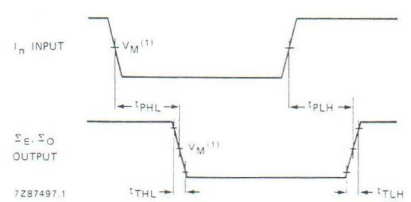


Fig. 6 Waveforms showing the data input (I_n) to parity outputs (Σ_E, Σ_O) propagation delays and the output transition time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

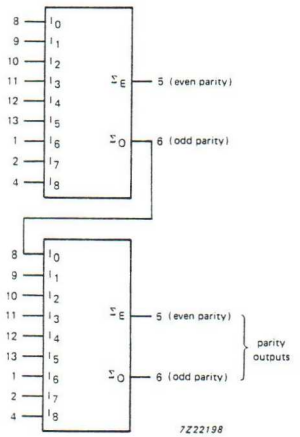


Fig. 7 Cascaded 17-bit odd/even parity generator/checker.

Note to Fig. 7

For a single-chip 16-bit even/odd parity generator/checker, see PC74HC/HCT7080.

4-BIT BINARY FULL ADDER WITH FAST CARRY

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 to Σ_4) and the out-going carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ_1 to Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can be assigned arbitrarily to pins 5, 6, 7, etc.

See the "583" for the BCD version.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay C_{IN} to Σ_1 C_{IN} to Σ_2 C_{IN} to Σ_3 C_{IN} to Σ_4 A_n or B_n to Σ_n C_{IN} to C_{OUT} A_n or B_n to C_{OUT}	C_L = 15 pF V_{CC} = 5 V	 16 18 20 23 21 20 20	 15 21 23 27 25 23 24	 ns ns ns ns ns ns ns
C_I	input capacitance		3,5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	88	92	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A_1 to A_4	A operand inputs
6, 2, 15, 11	B_1 to B_4	B operand inputs
7	C_{IN}	carry input
8	GND	ground (0 V)
9	C_{OUT}	carry output
16	V_{CC}	positive supply voltage

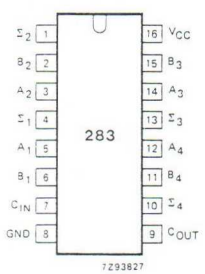


Fig. 1 Pin configuration.

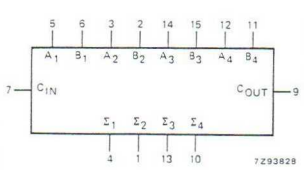


Fig. 2 Logic symbol.

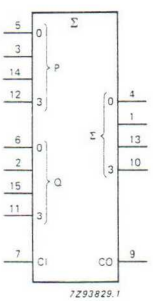


Fig. 3 IEC logic symbol.

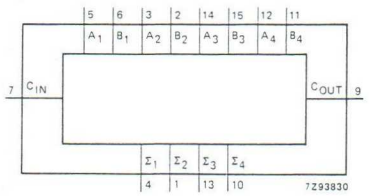


Fig. 4 Functional diagram.

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	EXAMPLE
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(a)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(b)

H = HIGH voltage level
L = LOW voltage level

Example
1001
1010
10011

(a) for active HIGH, example = (9 + 10 = 19)

(b) for active LOW, example = (carry + 6 + 5 = 12)

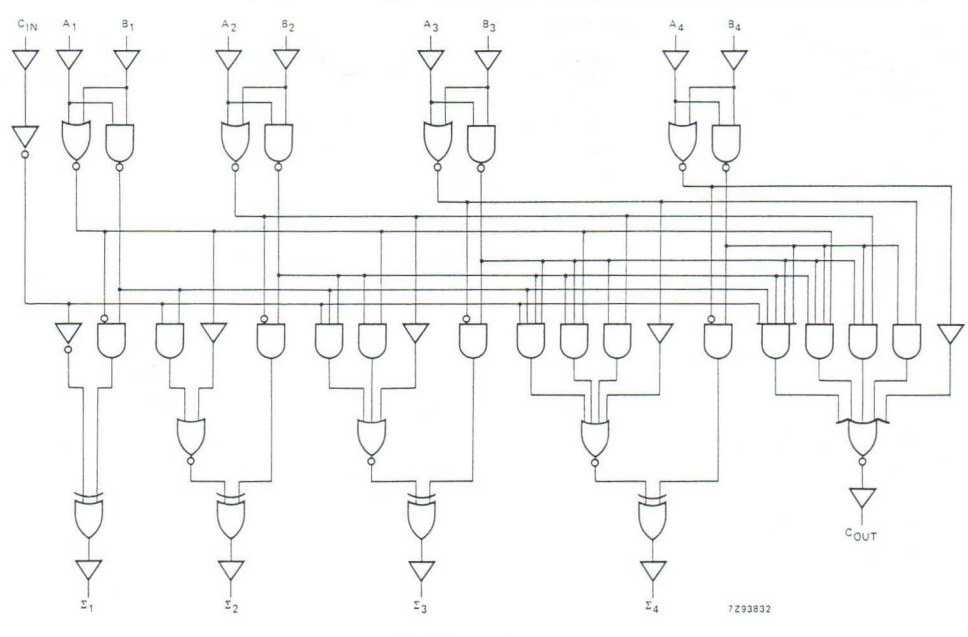


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_4		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to C_{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C_{IN}	1.50
B_2, A_2, A_1	1.00
B_1	0.40
B_4, A_4, A_3, B_3	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay C_{IN} to Σ_1		18	31		39		47	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay C_{IN} to Σ_2		25	43		54		65	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay C_{IN} to Σ_3		27	46		58		69	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay C_{IN} to Σ_4		31	53		66		80	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n or B_n to Σ_n		29	49		61		74	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay C_{IN} to C_{OUT}		27	46		58		69	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay A_n or B_n to C_{OUT}		28	48		60		72	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

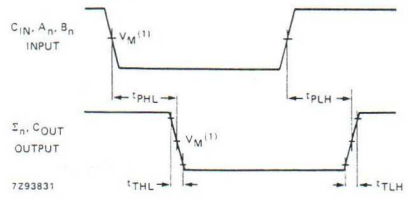


Fig. 6 Waveforms showing the inputs (C_{IN}, A_n, B_n) to the outputs (Σ_n, C_{OUT}) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

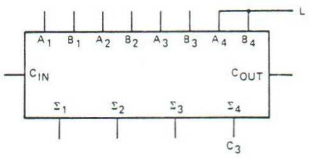


Fig. 7 3-bit adder.

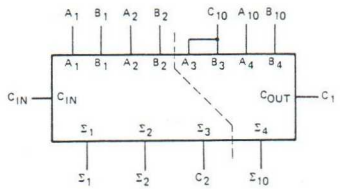


Fig. 8 2-bit and 1-bit adder.

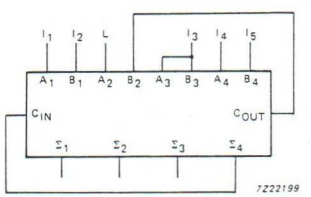


Fig. 9 5-input encoder.

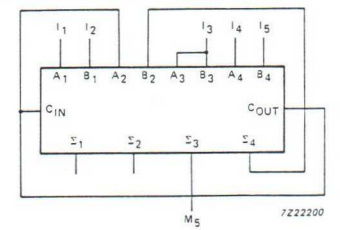


Fig. 10 5-input majority gate.

Note to Figs 7 to 10

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used simply as means of transfering the carry into the fourth stage (via A_2 and B_2) and transfering the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, HIGH or LOW, they do not influence Σ_2. Similary, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 produce a binary number equal to the number inputs (I_1 to I_5) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I_1 to I_5) are HIGH, the output M_5 is HIGH.

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency range:
  DC to 55 MHz typical (K-clock)
  DC to 35 MHz typical (I/D-clock)
- Dynamically variable bandwidth
- Very narrow bandwidth attainable
- Power-on reset
- Output capability: standard/bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT} ϕA_1, ϕB to $XORPD_{OUT}$ ϕB, ϕA_2 to $ECPD_{OUT}$	C_L = 15 pF V_{CC} = 5 V	 15 13 19	 18 13 19	ns
f_{max}	maximum clock frequency K_{CP} I/D_{CP}		 63 41	 68 40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

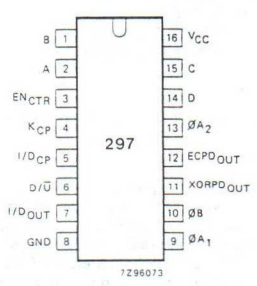


Fig. 1 Pin configuration.

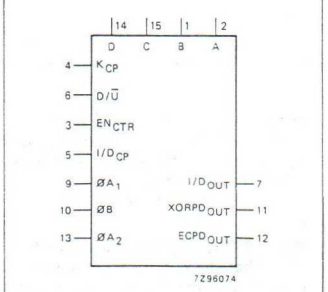


Fig. 2 Logic symbol.

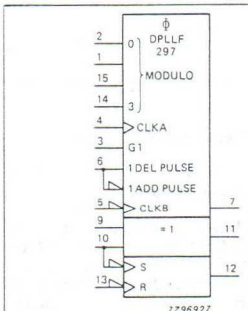


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1, 15, 14	A, B, C, D	modulo control inputs
3	EN_{CTR}	K-counter enable input
4	K_{CP}	K-counter clock input (LOW-to-HIGH, edge-triggered)
5	I/D_{CP}	increment/decrement clock input (HIGH-to-LOW, edge-triggered)
6	$D/\overline{U}$	down/up control
7	I/D_{OUT}	increment/decrement bus output
8	GND	ground (0 V)
9, 10, 13	ϕA_1, ϕB, ϕA_2	phase inputs
11	$XORPD_{OUT}$	EXCLUSIVE-OR phase detector output
12	$ECPD_{OUT}$	edge-controlled phase detector output
16	V_{CC}	positive supply voltage

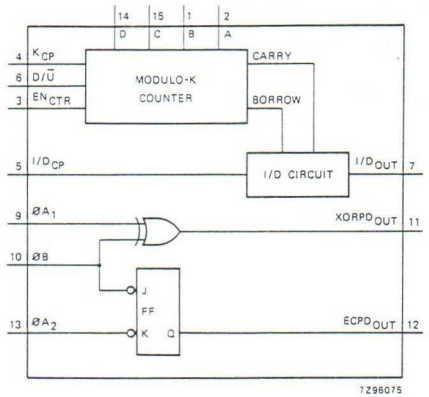


Fig. 4 Functional diagram.

K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE

D	C	B	A	MODULO (K)
L	L	L	L	inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE

ϕA_1	ϕB	$XORPD_{OUT}$
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR TABLE

ϕA_2	ϕB	$ECPD_{OUT}$
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level
L = LOW voltage level
↓ = HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

GENERAL DESCRIPTION

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With, A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwith by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error ($\phi_{IN} - \phi_{OUT}$). Within these limits the phase detector output varies linearly with the input phase

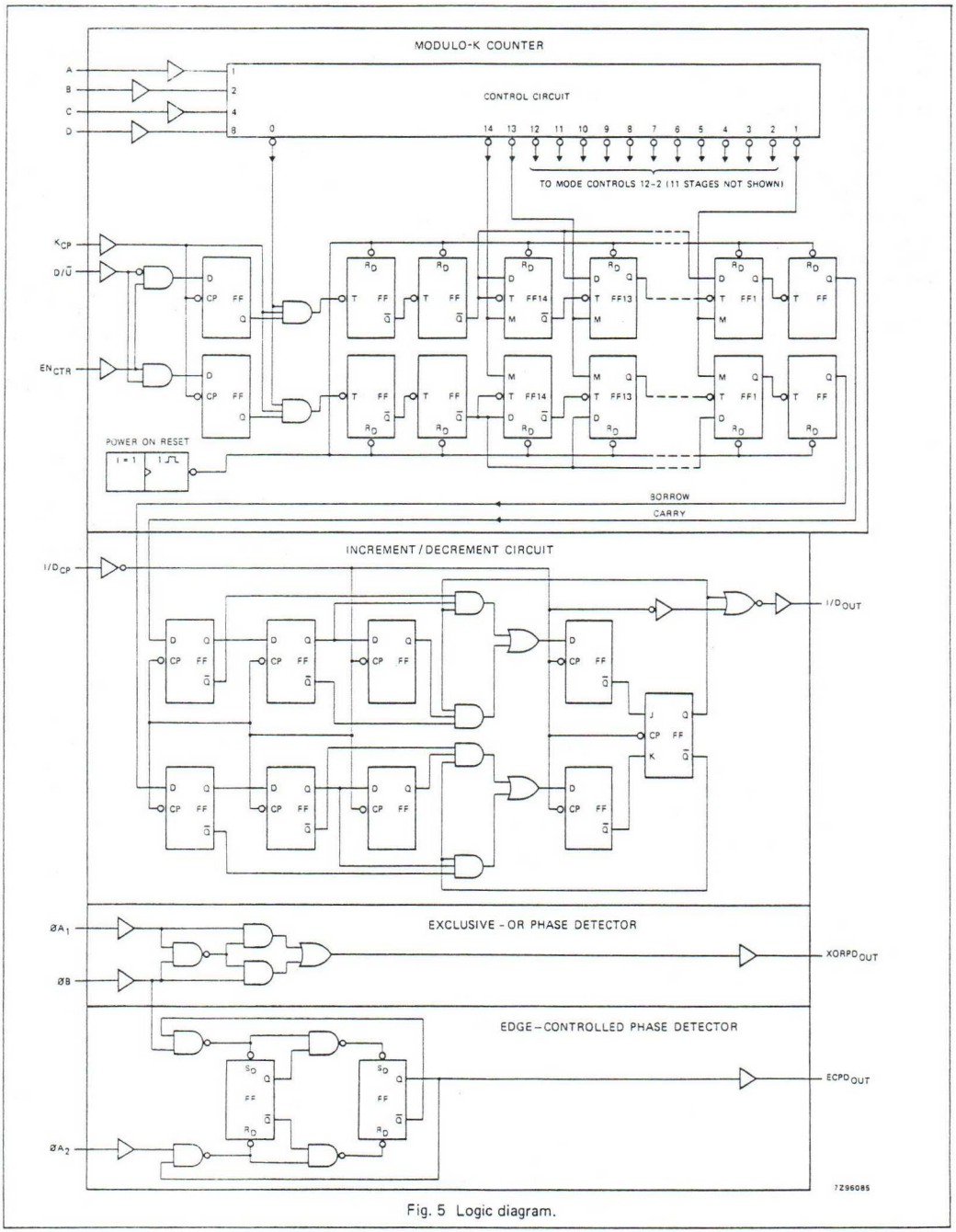


Fig. 5 Logic diagram.

GENERAL DESCRIPTION

error according to the gain k_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\,\text{HIGH} - \%\,\text{LOW}}{100}.$$

The output of the phase detector will be $k_d\phi_e$, where the phase error $\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (k_d) for an XORPD is 4 because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of 1/4 cycle.

Similarly, k_d for the ECPD is 2 since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 6 ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD, ϕ_e = 0 when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop centre frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(k_d\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is 1/2 of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c \pm (k_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (k_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

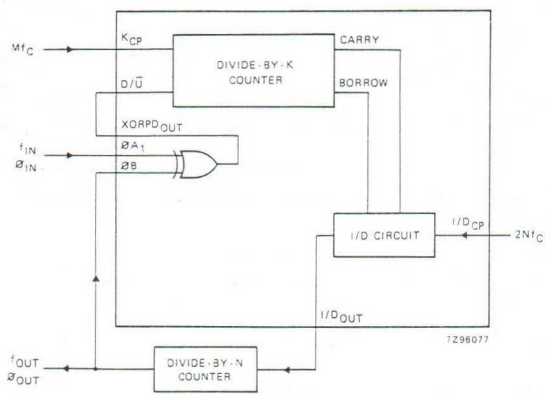


Fig. 6 DPLL using EXCLUSIVE-OR phase detection.

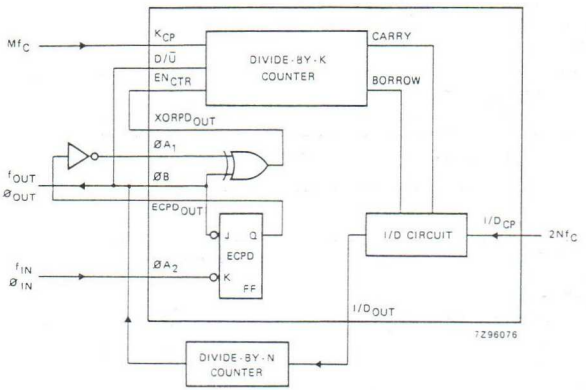


Fig. 7 DPLL using both phase detectors in a ripple-cancelation scheme.

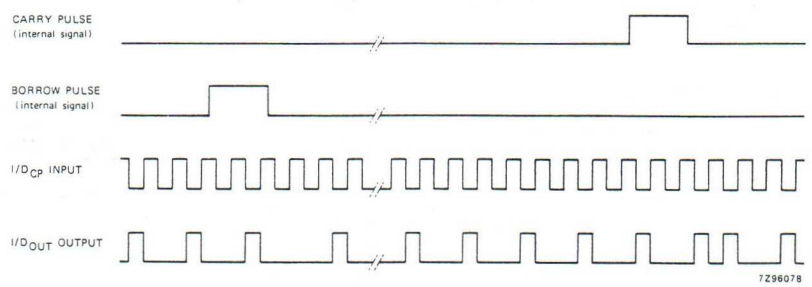


Fig. 8 Timing diagram: I/D$_{OUT}$ in-lock condition.

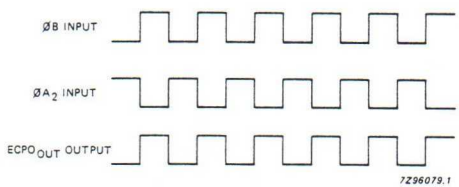


Fig. 9 Timing diagram: edge-controlled phase comparator waveforms.

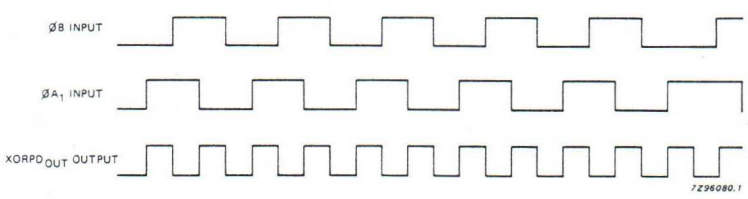


Fig. 10 Timing diagram: EXCLUSIVE-OR phase detector waveforms.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/ t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/ t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/ t_{TLH}	output transition time: bus driver output; I/D_{OUT} (pin 7)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 11
t_{THL}/ t_{TLH}	output transition time: standard outputs; $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12 and 13
t_W	clock pulse width K_{CP}	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14
t_W	clock pulse width I/D_{CP}	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	120 24 20	33 12 10		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	4.0 20 24	12 37 44		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
EN_{CTR}, $D/\overline{U}$	0.3
A, B, C, D, K_{CP}, ϕA_2	0.6
I/D_{CP}, ϕA_1, ϕB	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V, $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} V	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		21	35		44		53	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		16	32		40		48	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		22	44		55		66	ns	4.5	Fig. 13
t_{THL}/t_{TLH}	output transition time bus driver output I/D_{OUT} (pin 7)		5	12		15		18	ns	4.5	Fig. 11
t_{THL}/t_{TLH}	output transition time standard outputs $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		7	15		19		22	ns	4.5	Figs 12 and 13
t_W	clock pulse width K_{CP}	16	8		20		24		ns	4.5	Fig. 14
t_W	clock pulse width I/D_{CP}	25	13		31		38		ns	4.5	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	24	13		30		36		ns	4.5	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0	−8		0		0		ns	4.5	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	30	62		24		20		MHz	4.5	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	20	36		16		13		MHz	4.5	Fig. 11

AC WAVEFORMS

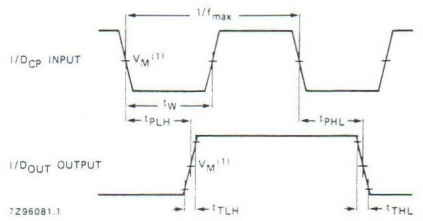


Fig. 11 Waveforms showing the clock (I/D_{CP}) to output (I/D_{OUT}) propagation delays, the clock pulse width, output transition times and maximum clock pulse frequency.

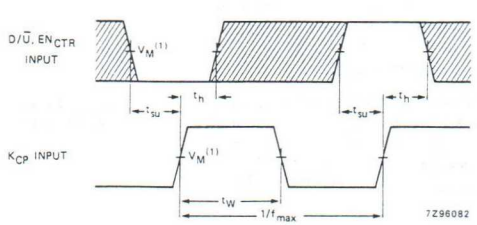


Fig. 14 Waveforms showing the clock (K_{CP}) pulse width and the maximum clock pulse frequency, and the input (D/U, EN_{CTR}) to clock (K_{CP}) set-up and hold times.

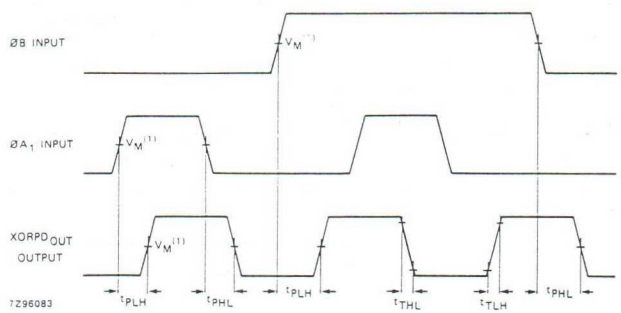


Fig. 12 Waveforms showing the phase input (ϕB, ϕA_1) to output ($XORPD_{OUT}$) propagation delays and output transition times.

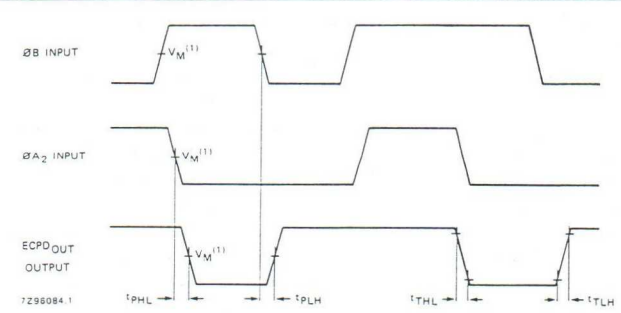


Fig. 13 Waveforms showing the phase input (ϕB, ϕA_2) to output ($ECPD_{OUT}$) propagation delays and output transition times.

Note to Fig. 14

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes: shift left
  shift right
  hold (store)
  load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability:
  bus driver (parallel I/Os)
  standard (serial outputs)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S_0 and S_1), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O_0 to I/O_7) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q_0 and Q_7) are used for expansion in serial shifting of longer words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7	C_L = 15 pF; V_{CC} = 5 V	20	19	ns
	CP to I/O_n		20	19	ns
t_{PHL}	$\overline{MR}$ to Q_0, Q_7 or I/O_n		20	23	ns
f_{max}	maximum clock frequency		50	46	MHz
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	120	125	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

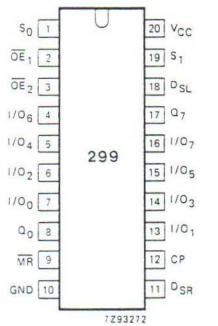


Fig. 1 Pin configuration.

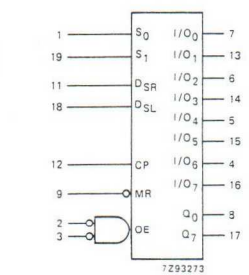


Fig. 2 Logic symbol.

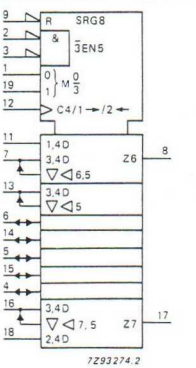


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S_0, S_1	mode select inputs
2, 3	$\overline{OE}_1$, $\overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O_0 to I/O_7	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q_0, Q_7	serial outputs (standard output)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D_{SR}	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D_{SL}	serial data shift-left input
20	V_{CC}	positive supply voltage

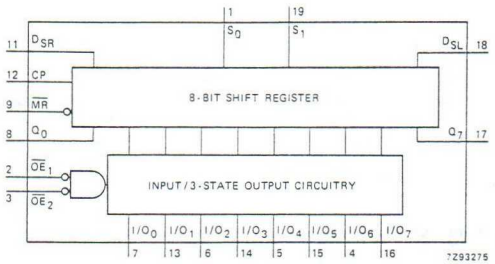


Fig. 4 Functional diagram.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	asynchronous reset; Q_0-Q_7 = LOW
H	H	H	↑	parallel load; $I/O_n \rightarrow Q_n$
H	L	H	↑	shift right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$ etc.
H	H	L	↑	shift left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$ etc.
H	L	L	X	hold

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION

A LOW signal on the asynchronous master reset input ($\overline{MR}$) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ($\overline{OE}_1$ or $\overline{OE}_2$) disables the 3-state buffers and the I/O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1, when in preparation for a parallel load operation.

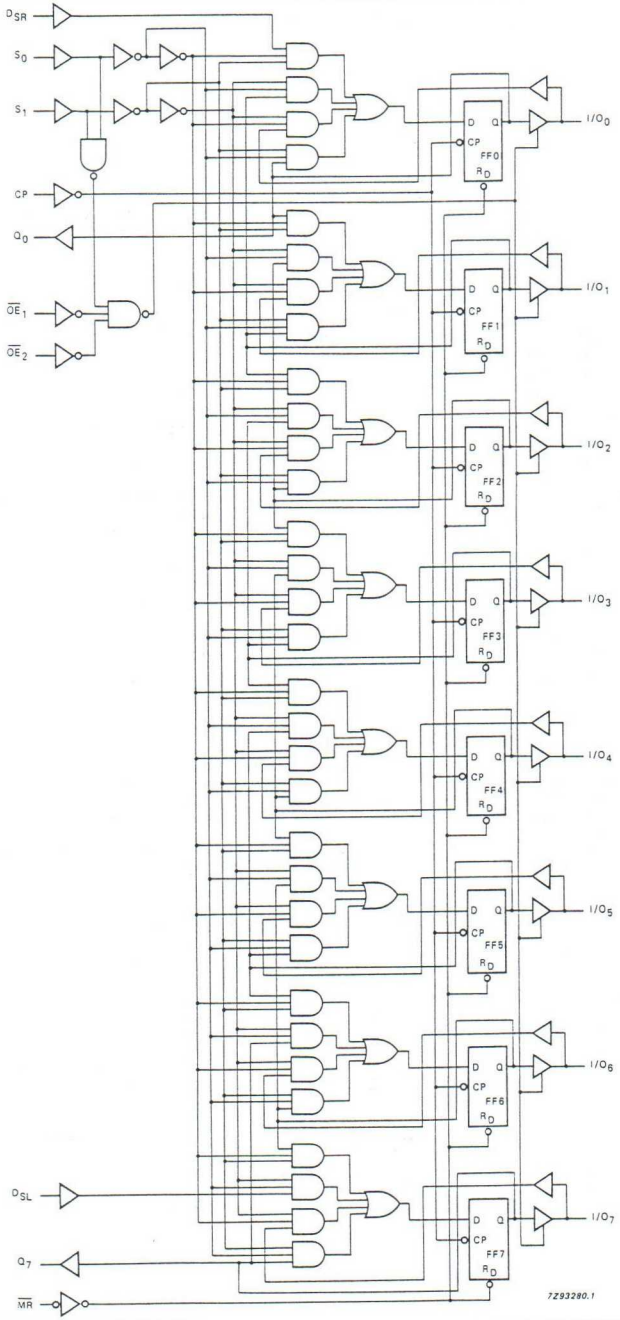


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os)
standard (serial outputs)

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP to I/O_n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}	3-state output enable time $\overline{OE}_n$ to I/O_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9
t_{PZL}	3-state output enable time $\overline{OE}_n$ to I/O_n		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		66 24 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time bus driver (I/O_n)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time standard (Q_0, Q_7)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5	−14 −5 −4		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time D_{SR}, D_{SL} to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time S_0, S_1 to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time I/O_n to CP	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time S_0, S_1 to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	5.0 25 29	15 45 54		4.0 20 24		3.4 17 20		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os)
standard (serial outputs)
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I/O_n	0.25
D_{SR}, D_{SL}	0.25
CP, S_0	0.60
$\overline{MR}$, S_1	0.25
$\overline{OE}_n$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7		22	37		46		56	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP to I/O_n		22	37		46		56	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n		27	46		58		69	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to I/O_n		19	30		38		45	ns	4.5	Fig. 9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		24	37		46		56	ns	4.5	Fig. 9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		20	32		40		48	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time bus driver (I/O_n)		5	12		15		18	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time standard (Q_0, Q_7)		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	10	2		9		11		ns	4.5	Fig. 7
t_{su}	set-up time I/O_n, D_{SR}, D_{SL} to CP	25	14		31		38		ns	4.5	Fig. 6
t_{su}	set-up time S_0, S_1 to CP	32	18		40		48		ns	4.5	Fig. 8
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0	−11		0		0		ns	4.5	Fig. 6
t_h	hold time S_0, S_1 to CP	0	−17		0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	25	42		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

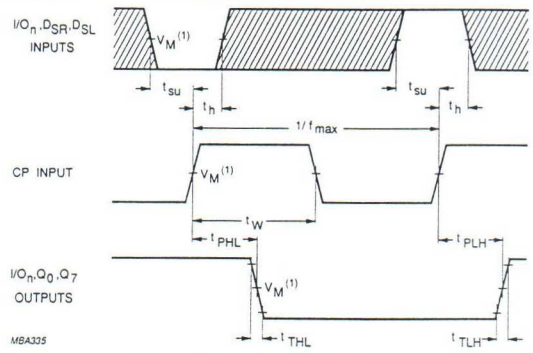


Fig. 6 Waveforms showing the clock (CP) to output (I/O_n, Q_0, Q_7) propagation delays, the clock pulse width, the I/O_n, D_{SR} and D_{SL} to CP set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

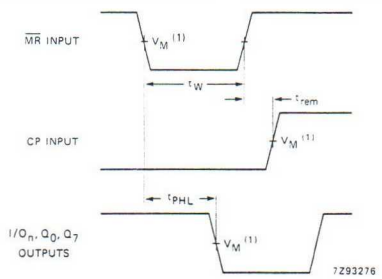


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width (LOW), the master reset to output (I/O_n, Q_0, Q_7) propagation delays and the master reset to clock (CP) removal time.

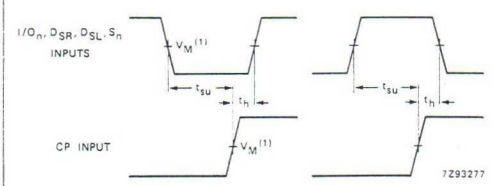


Fig. 8 Waveforms showing the set-up and hold times from the mode control inputs (S_0, S_1) to the clock (CP).

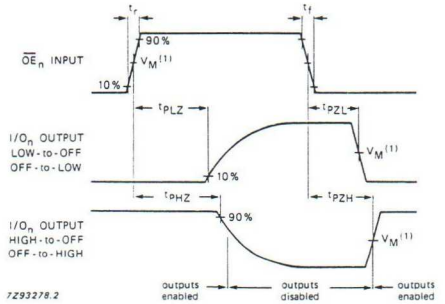


Fig. 9 Waveforms showing the 3-state enable and disable times for $\overline{OE}_n$ inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input ($\overline{LE}$).

The transparent 8-bit data latches are enabled when the active LOW data enable input ($\overline{E}$) is LOW.
When the output enable input $\overline{OE}_1$ = HIGH, $\overline{OE}_2$ = HIGH or OE_3 = LOW, the outputs go to the high impedance OFF-state.
Operation of these output enable inputs does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n, $\overline{E}$ to Y, $\overline{Y}$ S_n, $\overline{LE}$ to Y, $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	20 24	22 27	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

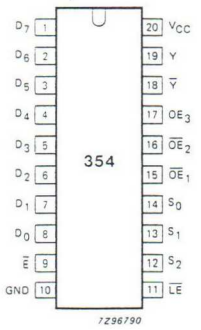


Fig. 1 Pin configuration.

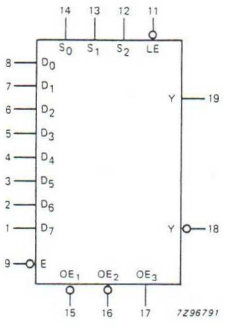


Fig. 2 Logic symbol.

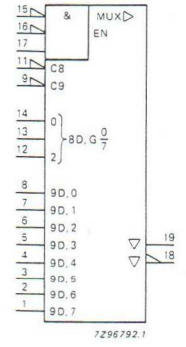


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D_0 to D_7	data inputs
9	$\overline{E}$	data enable input (active LOW)
10	GND	ground (0 V)
11	$\overline{LE}$	address latch enable input (active LOW)
14, 13, 12	S_0, S_1, S_2	select inputs
15, 16	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
17	OE_3	output enable input (active HIGH)
18	$\overline{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS *				OUTPUT ENABLE					
S_2	S_1	S_0	$\overline{E}$	$\overline{OE}_1$	$\overline{OE}_2$	OE_3	Y	$\overline{Y}$	
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D_0	$\overline{D}_0$	data latch is transparent
L	L	H	L	L	L	H	D_1	$\overline{D}_1$	
L	H	L	L	L	L	H	D_2	$\overline{D}_2$	
L	H	H	L	L	L	H	D_3	$\overline{D}_3$	
H	L	L	L	L	L	H	D_4	$\overline{D}_4$	
H	L	H	L	L	L	H	D_5	$\overline{D}_5$	
H	H	L	L	L	L	H	D_6	$\overline{D}_6$	
H	H	H	L	L	L	H	D_7	$\overline{D}_7$	
L	L	L	H	L	L	H	D_{0n}	$\overline{D}_{0n}$	data is latched
L	L	H	H	L	L	H	D_{1n}	$\overline{D}_{1n}$	
L	H	L	H	L	L	H	D_{2n}	$\overline{D}_{2n}$	
L	H	H	H	L	L	H	D_{3n}	$\overline{D}_{3n}$	
H	L	L	H	L	L	H	D_{4n}	$\overline{D}_{4n}$	
H	L	H	H	L	L	H	D_{5n}	$\overline{D}_{5n}$	
H	H	L	H	L	L	H	D_{6n}	$\overline{D}_{6n}$	
H	H	H	H	L	L	H	D_{7n}	$\overline{D}_{7n}$	

D_0 to D_7 = data at inputs D_0 to D_7
D_{0n} to D_{7n} = data at inputs D_0 to D_7 before the most recent LOW-to-HIGH transition of $\overline{E}$

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

* This column shows the input address set-up with $\overline{LE}$ = LOW (address latch is transparent).

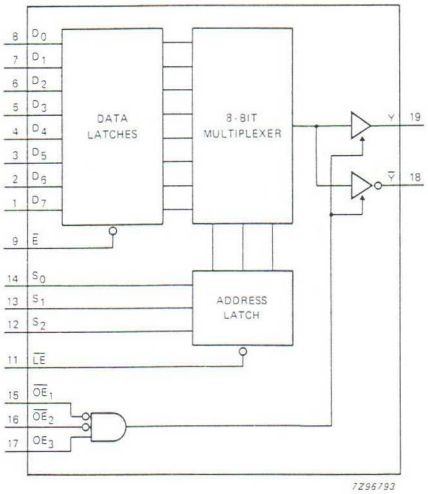


Fig. 4 Functional diagram.

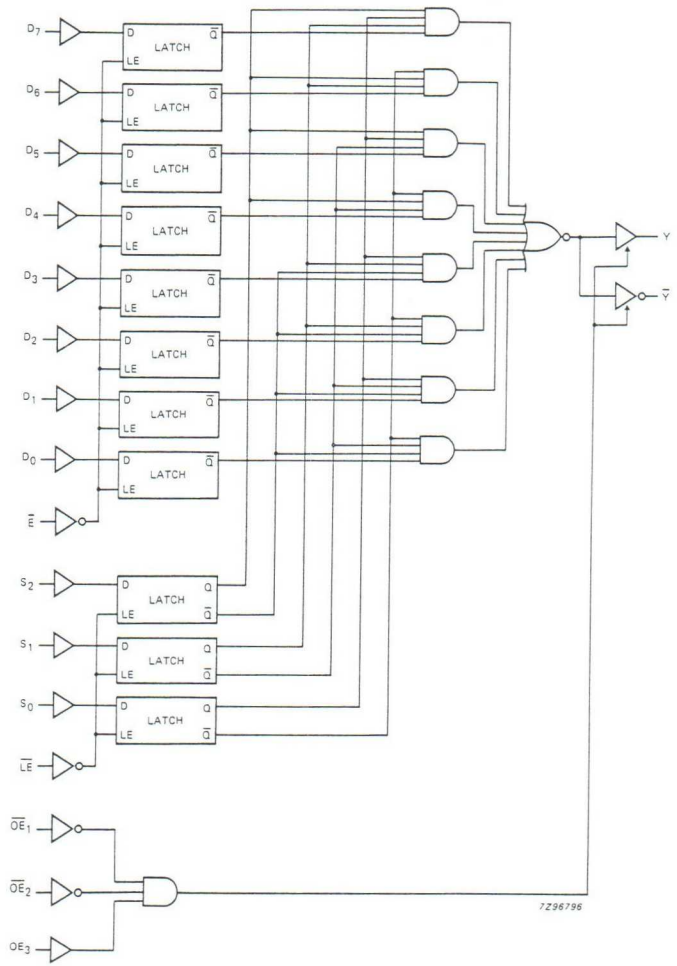


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Y, $\overline{Y}$		61 22 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Y, $\overline{Y}$		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y, $\overline{Y}$		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y, $\overline{Y}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 12
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, $\overline{Y}$		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y, $\overline{Y}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, $\overline{Y}$		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9
t_W	data enable pulse width $\overline{E}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	latch enable pulse width $\overline{LE}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to $\overline{E}$	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time S_n to $\overline{LE}$	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to $\overline{E}$	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time S_n to $\overline{LE}$	5 5 5	−8 −3 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n, S_n	0.2
$\overline{OE}_3$	0.25
$\overline{LE}$	0.5
$\overline{E}$, $\overline{OE}_n$	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Y, $\overline{Y}$		25	47		59		71	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Y, $\overline{Y}$		26	54		68		81	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y, $\overline{Y}$		30	59		74		89	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		31	63		79		95	ns	4.5	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y, $\overline{Y}$		18	34		43		51	ns	4.5	Fig. 12
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, $\overline{Y}$		18	34		43		51	ns	4.5	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y, $\overline{Y}$		18	33		41		50	ns	4.5	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, $\overline{Y}$		21	39		49		59	ns	4.5	Fig. 12
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9
t_W	data enable pulse width $\overline{E}$ LOW	16	6		20		24		ns	4.5	Fig. 6
t_W	latch enable pulse width $\overline{LE}$ LOW	16	6		20		24		ns	4.5	Fig. 9
t_{su}	set-up time D_n to $\overline{E}$	10	4		13		15		ns	4.5	Fig. 11
t_{su}	set-up time S_n to $\overline{LE}$	10	5		13		15		ns	4.5	Fig. 10
t_h	hold time D_n to $\overline{E}$	9	0		11		14		ns	4.5	Fig. 11
t_h	hold time S_n to $\overline{LE}$	9	−3		11		14		ns	4.5	Fig. 10

AC WAVEFORMS

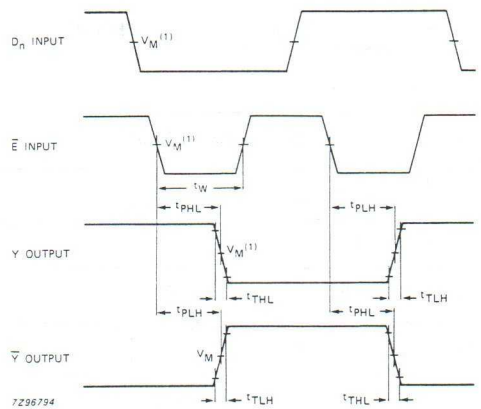


Fig. 6 Waveforms showing the data enable input ($\overline{E}$) pulse width, the data enable to output (Y, $\overline{Y}$) propagation delays and the output transition times.

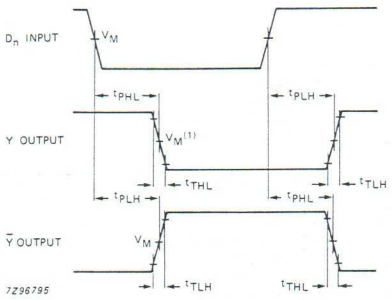


Fig. 7 Waveforms showing the data input (D_n) to output (Y, $\overline{Y}$) propagation delays and the output transition times ($\overline{E}$ = LOW).

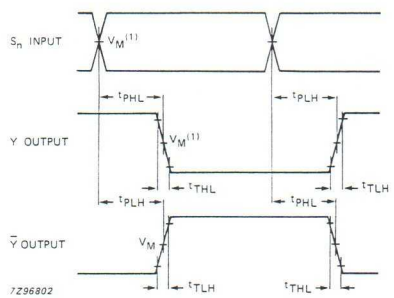


Fig. 8 Waveforms showing the select input (S_n) to output (Y, $\overline{Y}$) propagation delays and the output transition times ($\overline{LE}$ = LOW).

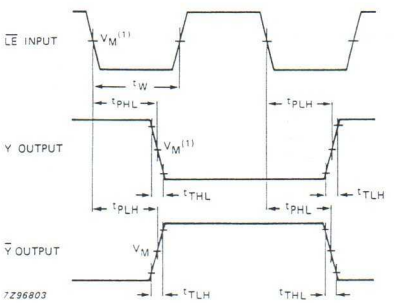


Fig. 9 Waveforms showing the address latch enable input ($\overline{LE}$) pulse width, the address latch enable input to output (Y, $\overline{Y}$) propagation delays and the output transition times.

AC WAVEFORMS (Cont'd)

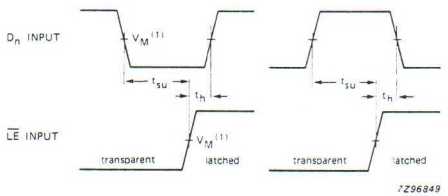


Fig. 10 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input ($\overline{LE}$).

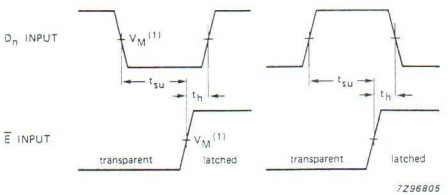


Fig. 11 Waveforms showing the set-up and hold times for the data input (D_n) to the data enable input ($\overline{E}$).

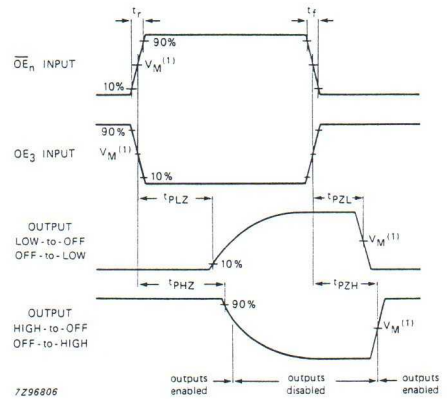


Fig. 12 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-INPUT MULTIPLEXER/REGISTER; 3-STATE

FEATURES

- Non-transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT356 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT356 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input $\overline{LE}$.

Data on the 8 input lines (D_0 to D_7) is clocked into a edge-triggered data register by a LOW-to-HIGH transition of the clock (CP).

When the output enable input $\overline{OE}_1$ = HIGH, $\overline{OE}_2$ = HIGH or OE_3 = LOW, the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches and register.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay S_n, $\overline{LE}$ to Y, $\overline{Y}$ CP to Y, $\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	24 20	25 22	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	123	125	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

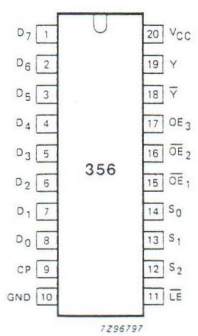


Fig. 1 Pin configuration.

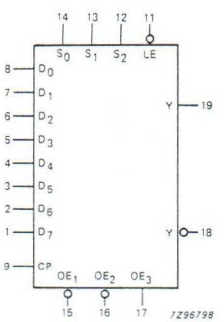


Fig. 2 Logic symbol.

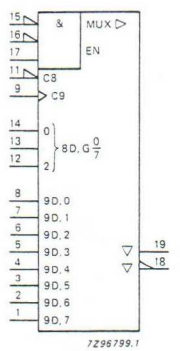


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D_0 to D_7	data inputs
9	CP	clock input data (LOW-to-HIGH, edge-triggered)
10	GND	ground (0 V)
11	$\overline{LE}$	address latch enable input (active LOW)
14, 13, 12	S_0, S_1, S_2	select inputs
15, 16	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
17	OE_3	output enable input (active HIGH)
18	$\overline{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS *				OUTPUT ENABLE					
S_2	S_1	S_0	CP	$\overline{OE}_1$	$\overline{OE}_2$	OE_3	Y	$\overline{Y}$	
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↑	L	L	H	D_{0n}	$\overline{D}_{0n}$	data is clocked into latch
L	L	H	↑	L	L	H	D_{1n}	$\overline{D}_{1n}$	
L	H	L	↑	L	L	H	D_{2n}	$\overline{D}_{2n}$	
L	H	H	↑	L	L	H	D_{3n}	$\overline{D}_{3n}$	
H	L	L	↑	L	L	H	D_{4n}	$\overline{D}_{4n}$	
H	L	H	↑	L	L	H	D_{5n}	$\overline{D}_{5n}$	
H	H	L	↑	L	L	H	D_{6n}	$\overline{D}_{6n}$	
H	H	H	↑	L	L	H	D_{7n}	$\overline{D}_{7n}$	
L	L	L	**	L	L	H	D_{0p}	$\overline{D}_{0p}$	outputs do not change states
L	L	H	**	L	L	H	D_{1p}	$\overline{D}_{1p}$	
L	H	L	**	L	L	H	D_{2p}	$\overline{D}_{2p}$	
L	H	H	**	L	L	H	D_{3p}	$\overline{D}_{3p}$	
H	L	L	**	L	L	H	D_{4p}	$\overline{D}_{4p}$	
H	L	H	**	L	L	H	D_{5p}	$\overline{D}_{5p}$	
H	H	L	**	L	L	H	D_{6p}	$\overline{D}_{6p}$	
H	H	H	**	L	L	H	D_{7p}	$\overline{D}_{7p}$	

D_{0n} to D_{7n} = data present at inputs D_0 to D_7 when the data latch clock made the transition from LOW-to-HIGH

D_{0p} to D_{7p} = data previously latched into the data latch by the LOW-to-HIGH transition of the data latch clock

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Z = high impedance OFF-state

* This column shows the input address set-up with $\overline{LE}$ = LOW (address latch is transparent).
** CP is HIGH, LOW or ↓.

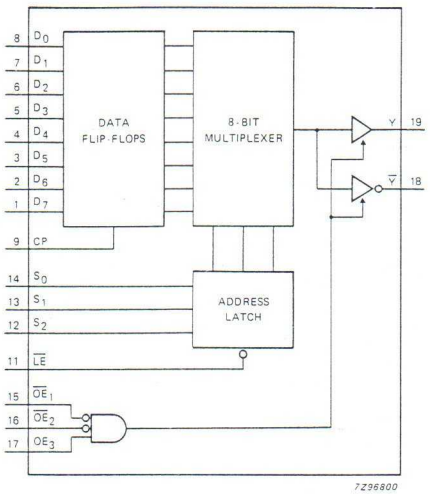


Fig. 4 Functional diagram.

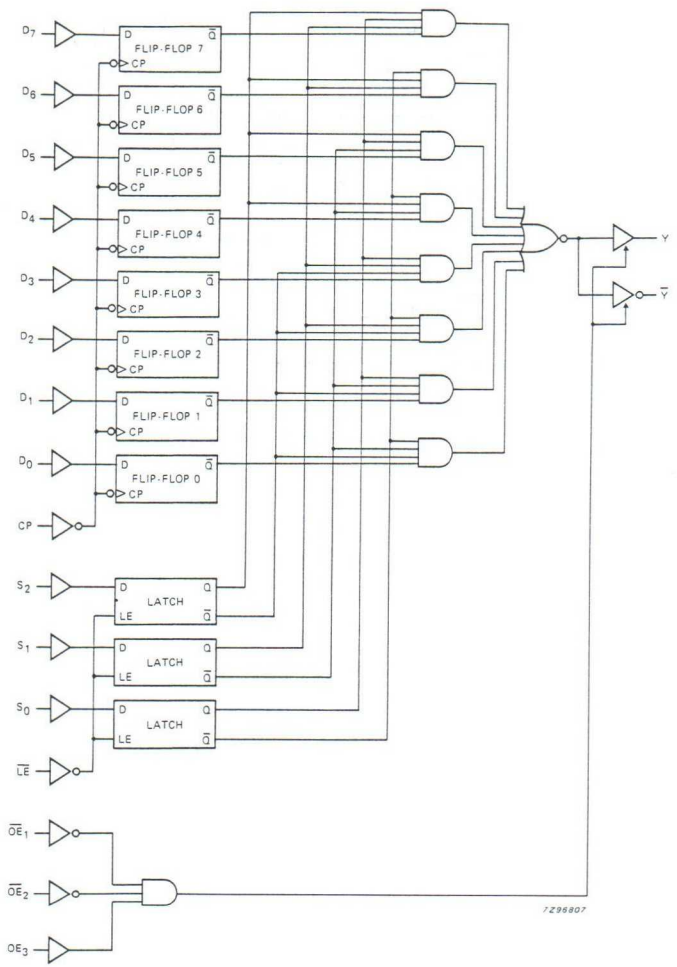


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Y, $\overline{Y}$		66 24 19	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y, $\overline{Y}$		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y, $\overline{Y}$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 11
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, $\overline{Y}$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 11
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y, $\overline{Y}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 11
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, $\overline{Y}$		58 21 17	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 11
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6, 7 and 8
t_W	clock pulse width CP HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	latch enable pulse width $\overline{LE}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time S_n to $\overline{LE}$	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to CP	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time S_n to $\overline{LE}$	5 5 5	−8 −3 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n, S_n	0.2
$\overline{OE}_3$	0.25
$\overline{LE}$	0.5
$\overline{OE}_n$, CP	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Y, $\overline{Y}$		26	51		64		77	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y, $\overline{Y}$		28	59		74		89	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		29	63		79		95	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y, $\overline{Y}$		17	34		43		51	ns	4.5	Fig. 11
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, $\overline{Y}$		18	34		43		51	ns	4.5	Fig. 11
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y, $\overline{Y}$		17	33		41		50	ns	4.5	Fig. 11
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, $\overline{Y}$		20	33		41		50	ns	4.5	Fig. 11
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6, 7 and 8
t_W	clock pulse width CP HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t_W	latch enable pulse width $\overline{LE}$ LOW	16	6		20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	10	4		13		15		ns	4.5	Fig. 10
t_{su}	set-up time S_n to $\overline{LE}$	10	5		13		15		ns	4.5	Fig. 9
t_h	hold time D_n to CP	5	0		5		5		ns	4.5	Fig. 10
t_h	hold time S_n to $\overline{LE}$	5	−2		5		5		ns	4.5	Fig. 9

AC WAVEFORMS

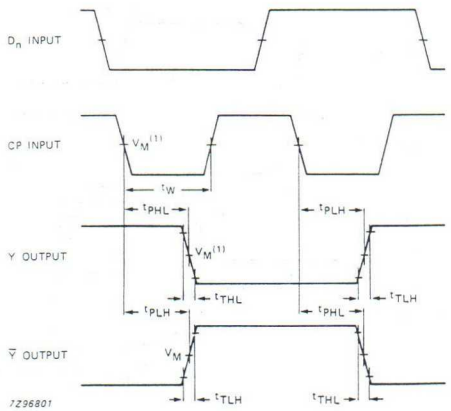


Fig. 6 Waveforms showing the clock (CP) to the output (Y, $\overline{Y}$) propagation delays, the clock pulse width and the output transition times.

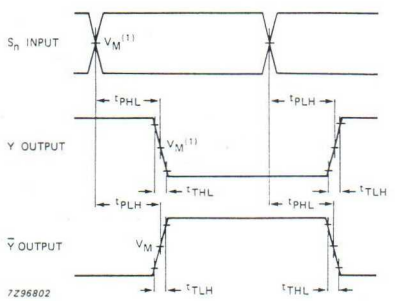


Fig. 7 Waveforms showing the select input (S_n) to output (Y, $\overline{Y}$) propagation delays and the output transition times ($\overline{LE}$ = LOW).

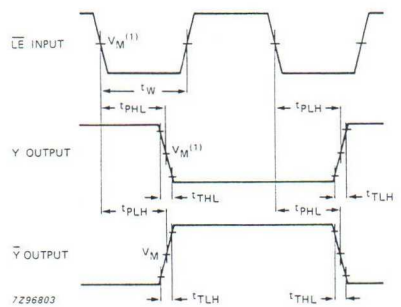


Fig. 8 Waveforms showing the address latch enable input ($\overline{LE}$) pulse width, the latch enable input to output (Y, $\overline{Y}$) propagation delays and the output transition times.

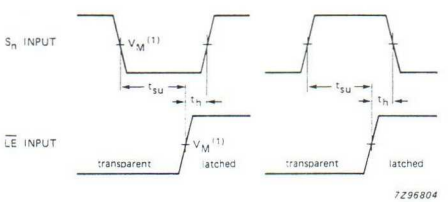


Fig. 9 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input ($\overline{LE}$).

AC WAVEFORMS

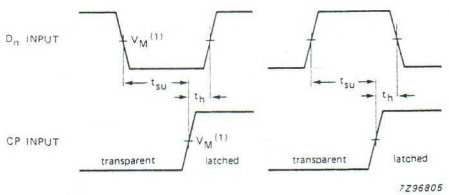


Fig. 10 Waveforms showing the set-up and hold times for the data input (D_n) to the clock (CP).

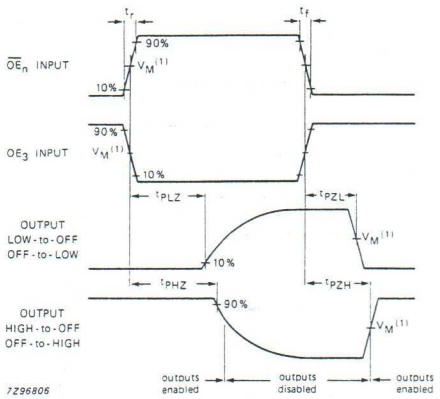


Fig. 11 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}_1$, $\overline{OE}_2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "365" is identical to the "366" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3,5	3,5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

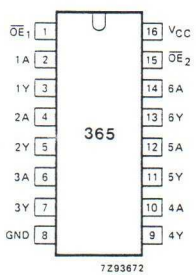
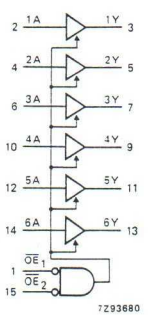


Fig. 1 Pin configuration.



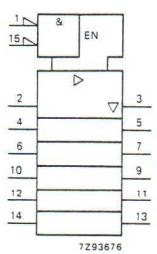


Fig. 3 IEC logic symbol.

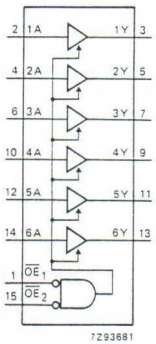


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

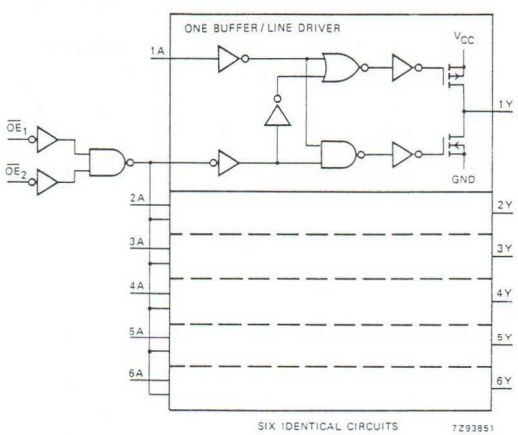


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to nY		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to nY		61 22 18	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.00
$\overline{OE}_2$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to nY		18	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to nY		23	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

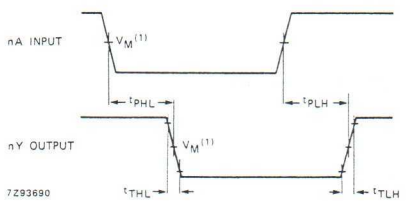


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

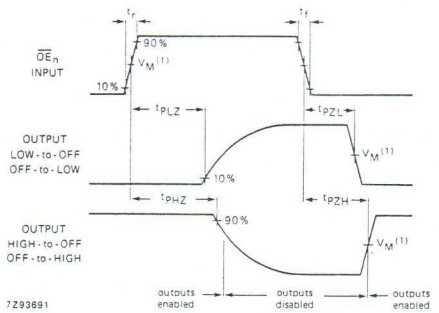


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT366 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT366 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}_1$, $\overline{OE}_2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "366" is identical to the "365" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to $n\overline{Y}$	C_L = 15 pF; V_{CC} = 5 V	10	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\overline{Y}$ to $6\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

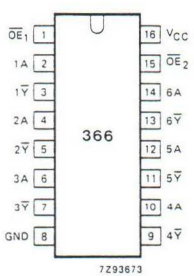


Fig. 1 Pin configuration.

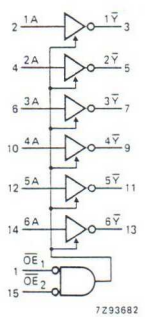


Fig. 2 Logic symbol.

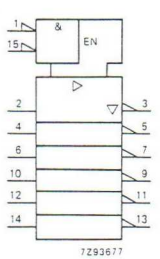


Fig. 3 IEC logic symbol.

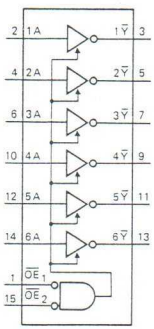


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	n$\overline{Y}$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

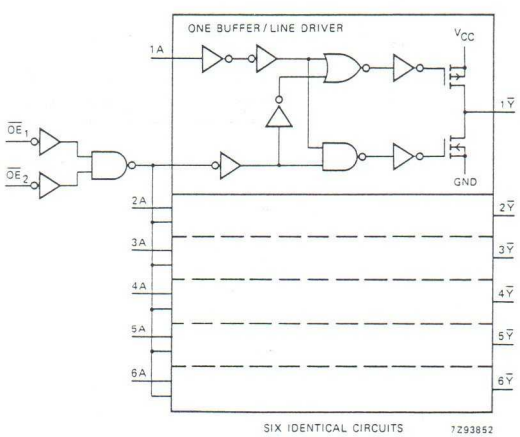


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to n$\overline{Y}$		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to n$\overline{Y}$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to n$\overline{Y}$		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.00
$\overline{OE}_2$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$		13	24		30		36	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to n$\overline{Y}$		16	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to n$\overline{Y}$		20	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

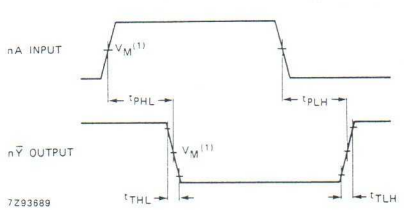


Fig. 6 Waveforms showing the input (nA) to output (n$\overline{Y}$) propagation delays and the output transition times.

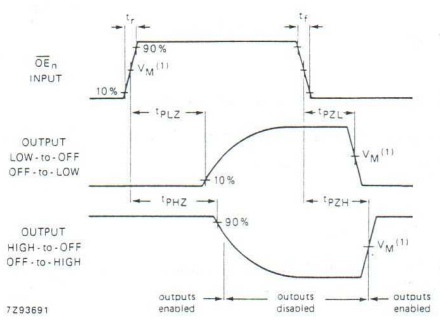


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "367" is identical to the "368" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

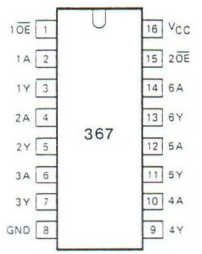


Fig. 1 Pin configuration.

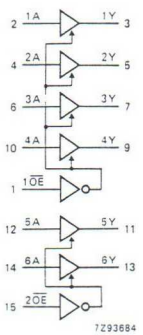


Fig. 2 Logic symbol.

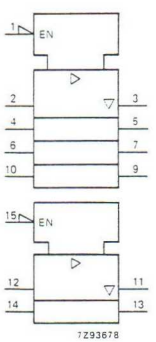


Fig. 3 IEC logic symbol.

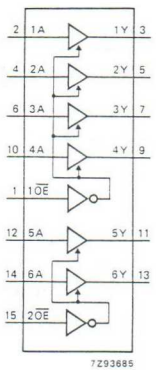


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

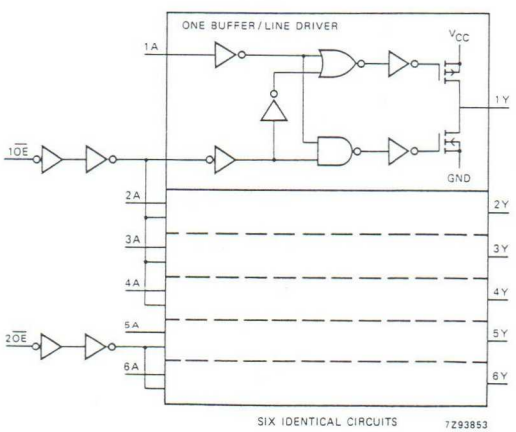


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1\overline{OE}$	1.00
$2\overline{OE}$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to + 85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		16	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		21	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

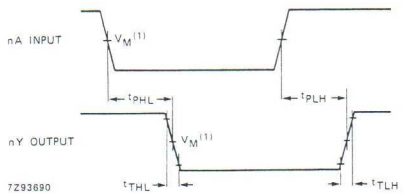


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

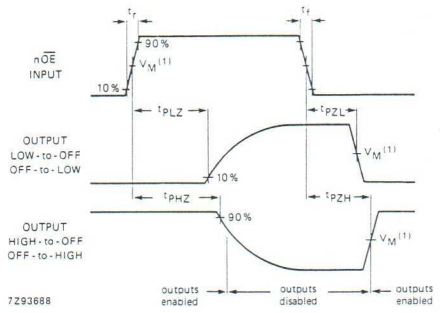


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs ($n\overline{Y}$) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to $n\overline{Y}$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\overline{Y}$ to $6\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

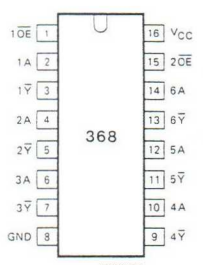


Fig. 1 Pin configuration.

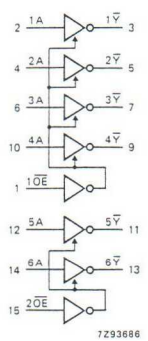


Fig. 2 Logic symbol.

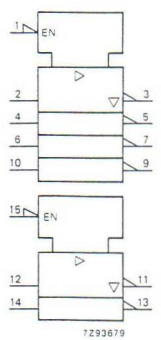


Fig. 3 IEC logic symbol.

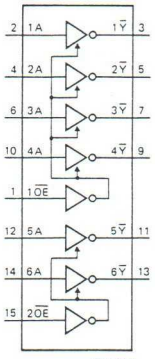


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
n$\overline{OE}$	nA	n$\overline{Y}$
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

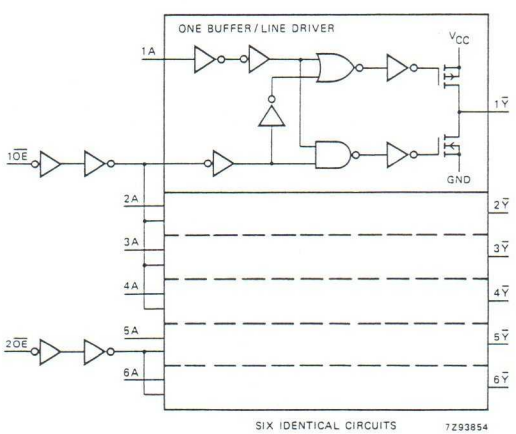


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to n$\overline{Y}$		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time n$\overline{OE}$ to n$\overline{Y}$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time n$\overline{OE}$ to n$\overline{Y}$		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1$\overline{OE}$	1.00
2$\overline{OE}$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$		13	24		30		36	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to n$\overline{Y}$		17	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to n$\overline{Y}$		20	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

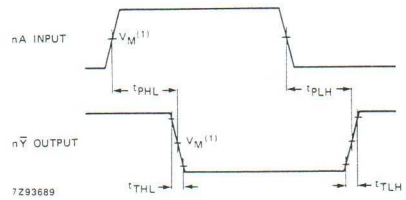


Fig. 6 Waveforms showing the input (nA) to output (n$\overline{Y}$) propagation delays and the output transition times.

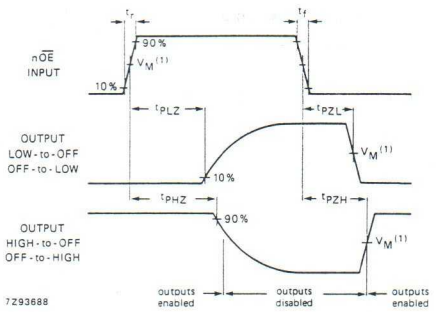


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563", "573" and "533"
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "373" is functionally identical to the "533", "563" and "573", but the "563" and "533" have inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LE to Q_n	C_L = 15 pF V_{CC} = 5 V	12 15	14 13	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	45	41	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

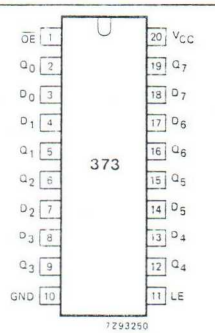


Fig. 1 Pin configuration.

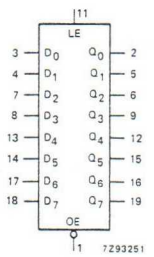


Fig. 2 Logic symbol.

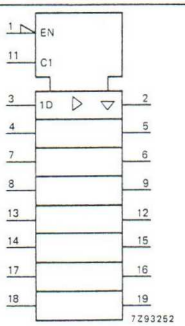


Fig. 3 IEC logic symbol.

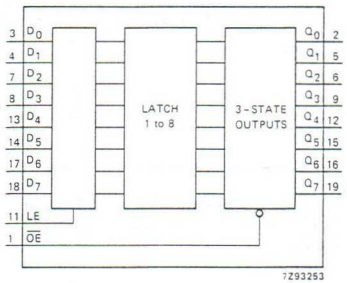


Fig. 4 Functional diagram.

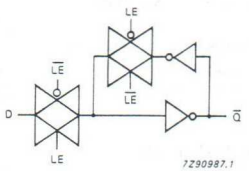


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	X X	X X	X X	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

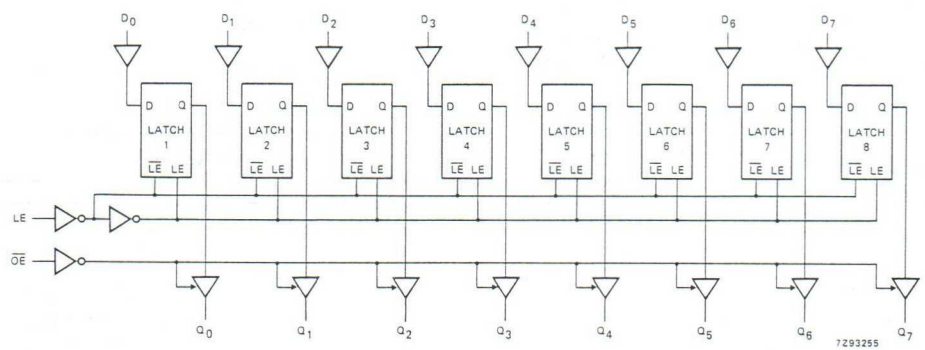


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t_W	LE pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to LE	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_n to LE	5 5 5	−8 −3 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.30
$\overline{LE}$	1.50
$\overline{OE}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74CHT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		17	30		38		45	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		16	32		40		48	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		19	32		40		48	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	30		38		45	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 7
t_W	LE pulse width HIGH	16	4		20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to LE	12	6		15		18		ns	4.5	Fig. 10
t_h	hold time D_n to LE	4	−1		4		4		ns	4.5	Fig. 10

AC WAVEFORMS

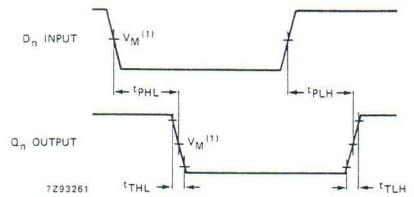


Fig. 7 Waveforms showing the input (D_n) to output (Q_n) propagation delays and the output transition times.

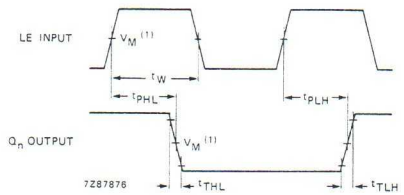


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

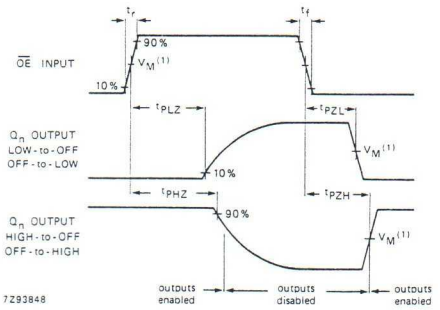


Fig. 9 Waveforms showing the 3-state enable and disable times.

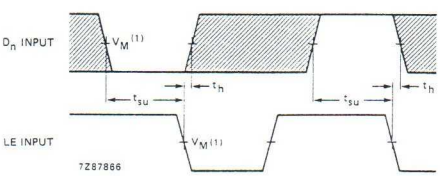


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.
A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	13	ns
f_{max}	maximum clock frequency		77	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

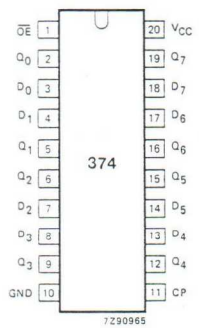


Fig. 1 Pin configuration.

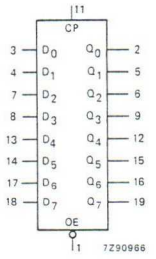


Fig. 2 Logic symbol.

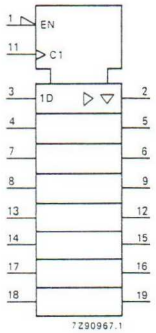


Fig. 3 IEC logic symbol.

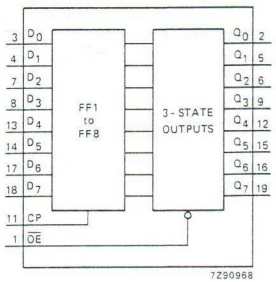


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP–FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

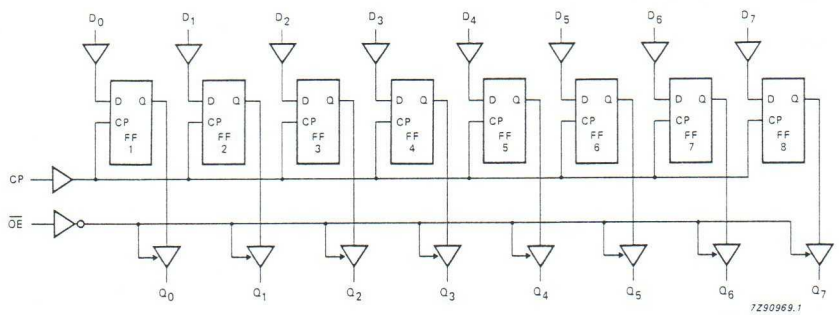


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1.25
CP	0.90
D_n	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		16	32		40		48	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		16	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	28		35		42	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12	7		15		18		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5	−3		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig. 6

AC WAVEFORMS

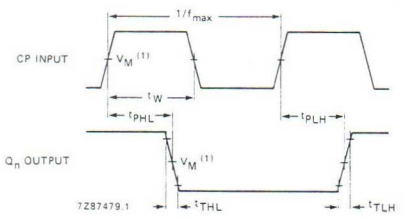


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

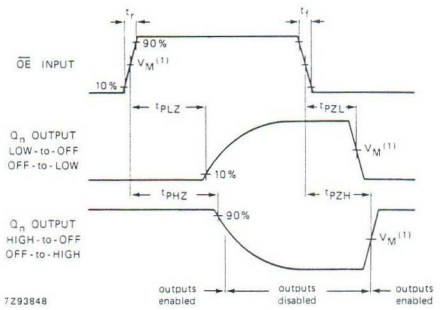


Fig. 7 Waveforms showing the 3-state enable and disable times.

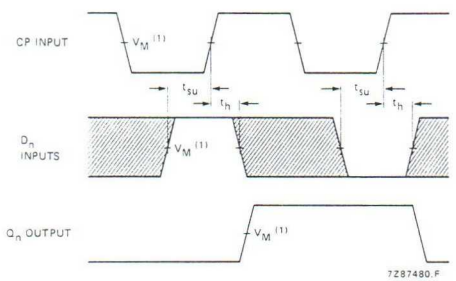


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.
HCT: $V_M = 1.3$ V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP WITH DATA ENABLE; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See "273" for master reset version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

A common clock (CP) input loads all flip-flops simultaneously when the data enable ($\overline{E}$) is LOW.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	13	14	ns
f_{max}	maximum clock frequency		77	53	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

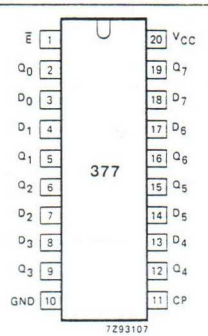


Fig. 1 Pin configuration.

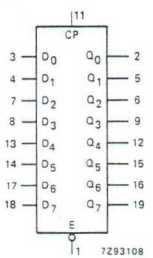


Fig. 2 Logic symbol.

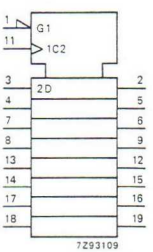


Fig. 3 IEC logic symbol.

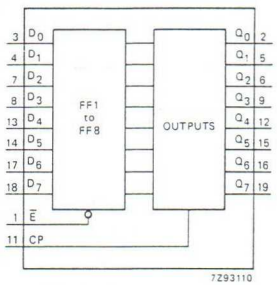
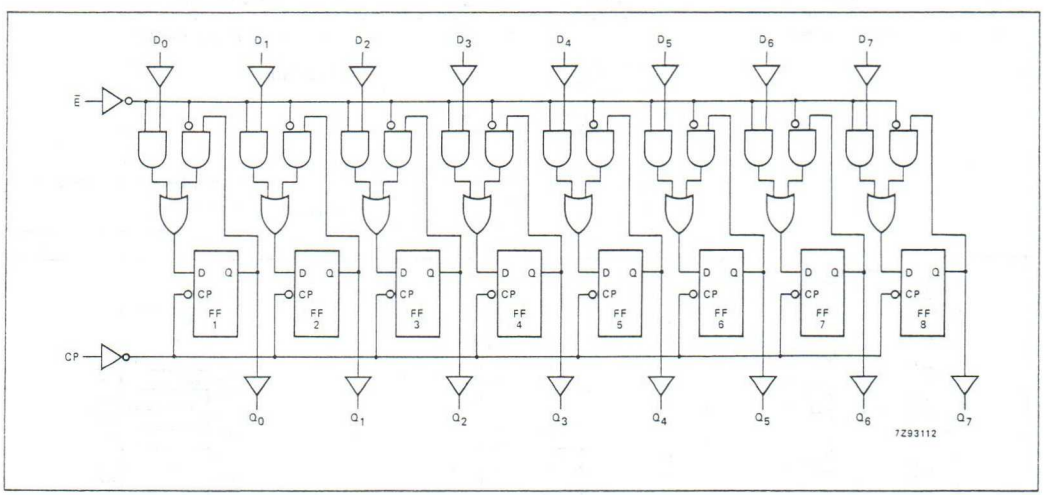


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	$\bar{E}$	D_n	Q_n
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{E}$ to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time D_n to CP	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time $\overline{E}$ to CP	4 4 4	−3 −1 −1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 35	23 70 83		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}$	1.50
CP	0.50
D_n	0.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		17	32		40		48	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20	8		25		30		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12	4		15		18		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{E}$ to CP	22	12		28		33		ns	4.5	Fig. 7
t_h	hold time D_n to CP	2	−4		2		2		ns	4.5	Fig. 7
t_h	hold time $\overline{E}$ to CP	3	−2		3		3		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

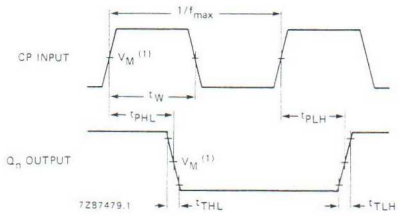


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

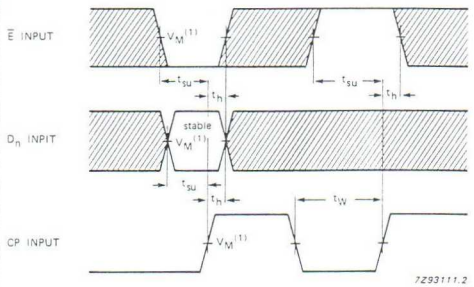


Fig. 7 Waveforms showing the data set-up and hold times from the data input (D_n) and from the data enable input ($\overline{E}$) to the clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

DUAL DECADE RIPPLE COUNTER

FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks ($n\overline{CP}_0$ and $n\overline{CP}_1$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0 $n\overline{CP}_1$ to nQ_1 $n\overline{CP}_1$ to nQ_2 $n\overline{CP}_1$ to nQ_3 nMR to Q_n	C_L = 15 pF V_{CC} = 5 V	 14 15 23 15 16	 18 19 26 19 18	 ns ns ns ns ns
f_{max}	maximum clock frequency $n\overline{CP}_0$, $n\overline{CP}_1$		66	61	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	20	21	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

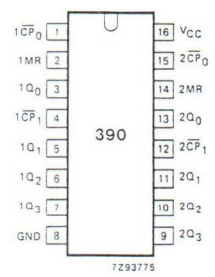


Fig. 1 Pin configuration.

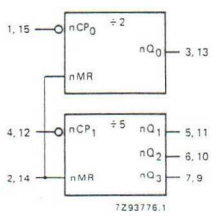


Fig. 2 Logic symbol.

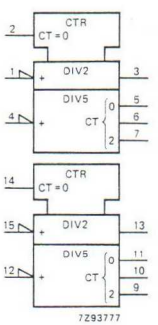


Fig. 3 IEC logic symbol.

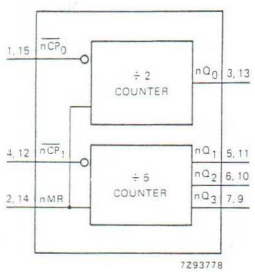


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ($n\overline{CP}_0$ and $n\overline{CP}_1$).
For BCD decade operation, the nQ_0 output is connected to the $n\overline{CP}_1$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ_3 output is connected to the $n\overline{CP}_0$ input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0$, $2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1$, $2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note

Output Q_0 connected to $n\overline{CP}_1$ with counter input on $n\overline{CP}_0$.

H = HIGH voltage level
L = LOW voltage level

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

Output Q_3 connected to $n\overline{CP}_0$ with counter input on $n\overline{CP}_1$.

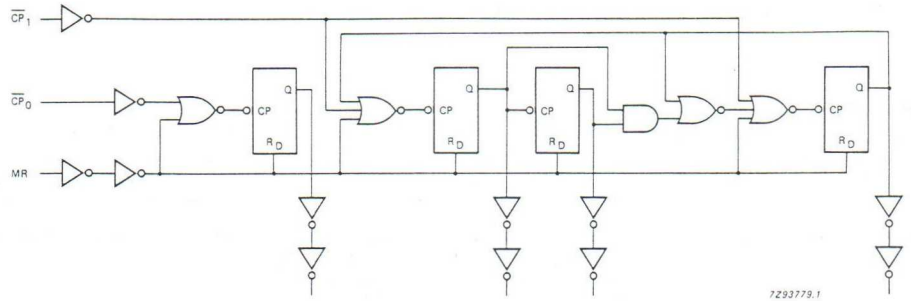


Fig. 5 Logic diagram (one counter).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2		74 27 22	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay nMR to nQ_n		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width HIGH	80 17 14	28 10 8		105 21 18		130 26 22		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time nMR to $n\overline{CP}_n$	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{CP}_0$	0.45
$n\overline{CP}_1$, nMR	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0		21	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2		30	51		64		77	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3		22	38		48		57	ns	4.5	Fig. 6
t_{PHL}	propagation delay nMR to nQ_n		21	36		45		54	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	18	8		23		27		ns	4.5	Fig. 6
t_W	master reset pulse width HIGH	17	10		21		26		ns	4.5	Fig. 7
t_{rem}	removal time nMR to $n\overline{CP}_n$	15	8		19		22		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

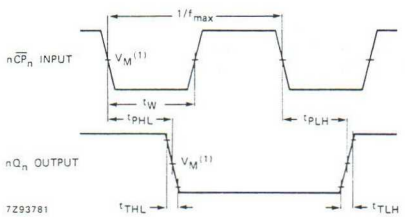


Fig. 6 Waveforms showing the clock ($n\overline{CP}_n$) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

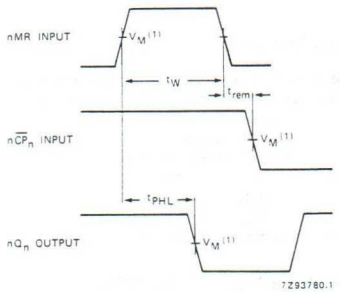


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delays and the master reset to clock ($n\overline{CP}_n$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-BIT BINARY RIPPLE COUNTER

FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks ($1\overline{CP}$ and $2\overline{CP}$) and master reset (1MR and 2MR) inputs to each counter.
The operation of each half of the "393" is the same as the "93" except no external clock connections are required.
The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.
A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0 nQ to nQ_{n+1} nMR to nQ_n	C_L = 15 pF V_{CC} = 5 V	 12 5 11	 20 6 15	 ns ns ns
f_{max}	maximum clock frequency		99	53	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	23	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	$1Q_0$ to $1Q_3$, $2Q_0$ to $2Q_3$	flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

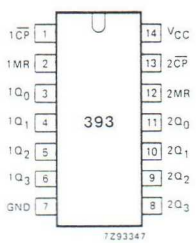


Fig. 1 Pin configuration.

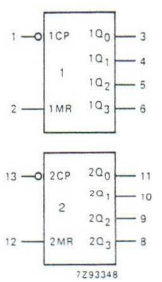


Fig. 2 Logic symbol.

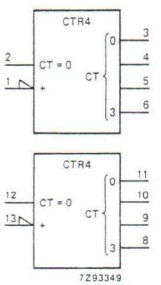


Fig. 3 IEC logic symbol.

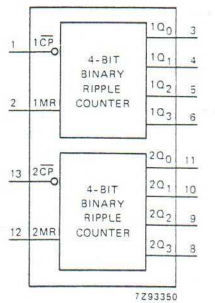


Fig. 4 Functional diagram.

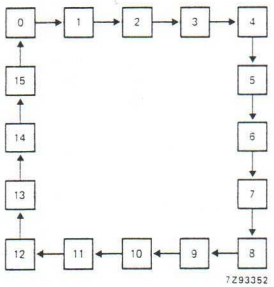


Fig. 5 State diagram.

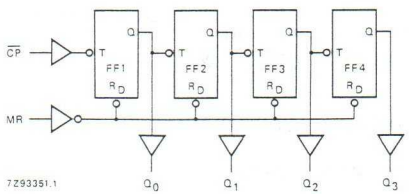


Fig. 6 Logic diagram (one counter).

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}		14 5 4	45 9 8		55 11 9		70 14 12	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay nMR to nQ_n		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time nMR to $n\overline{CP}$	5 5 5	3 1 1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1\overline{CP}$	0.4
$2\overline{CP}$	0.4
1MR	1.0
2MR	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0		15	25		31		38	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}		6	10		13		15	ns	4.5	Fig. 7
t_{PHL}	propagation delay nMR to nQ_n		18	32		40		48	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig. 7
t_W	master reset pulse width; HIGH	16	6		20		24		ns	4.5	Fig. 8
t_{rem}	removal time nMR to $n\overline{CP}$	5	0		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 7

AC WAVEFORMS

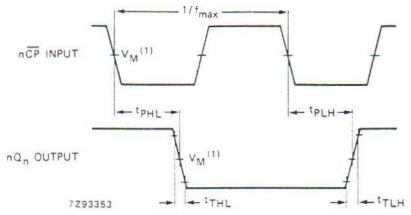


Fig. 7 Waveforms showing the clock ($n\overline{CP}$) to output ($1Q_n$, $2Q_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

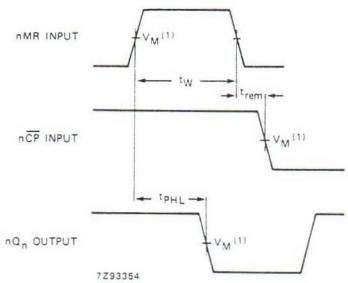


Fig. 8 Waveforms showing the master reset (nMR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($n\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT423 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT423 are dual retriggerable monostable multivibrators with output pulse width control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse periode (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. When $n\overline{R}_D$ is LOW, it forces the nQ output LOW, the $n\overline{Q}$ output HIGH and also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V; R_{EXT} = 5 kΩ; C_{EXT} = 0 pF	25	26	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		20	22	ns
C_I	input capacitance		3.5	3.5	pF
t_W	minimum output pulse width nQ, $n\overline{Q}$	notes 1 and 2	75	75	ns

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + + D \times 16 \times V_{CC}$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
D = duty factor in %
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
C_{EXT} = timing capacitance in pF

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset action (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

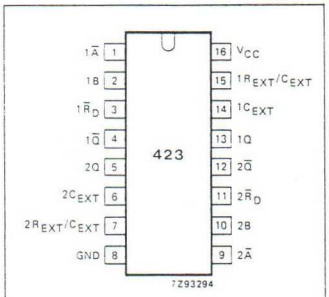
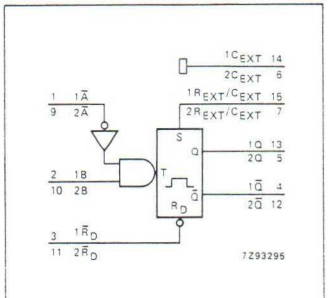


Fig. 1 Pin configuration.



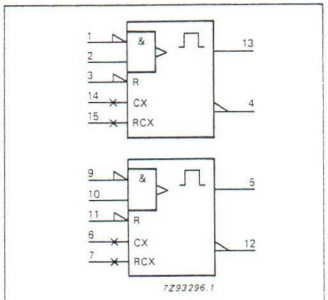


Fig. 3 IEC logic symbol.

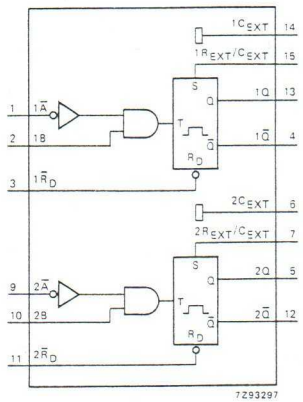


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.

GENERAL DESCRIPTION (Cont'd)

Figures 7 and 8 illustrate pulse control by reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.
For pulse widths, when $C_{EXT} < 10\,000$ pF, see Fig. 9.
When $C_{EXT} > 10\,000$ pF, the typical output pulse width is defined as:

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The "423" is identical to the "123" but cannot be triggered via the reset input.

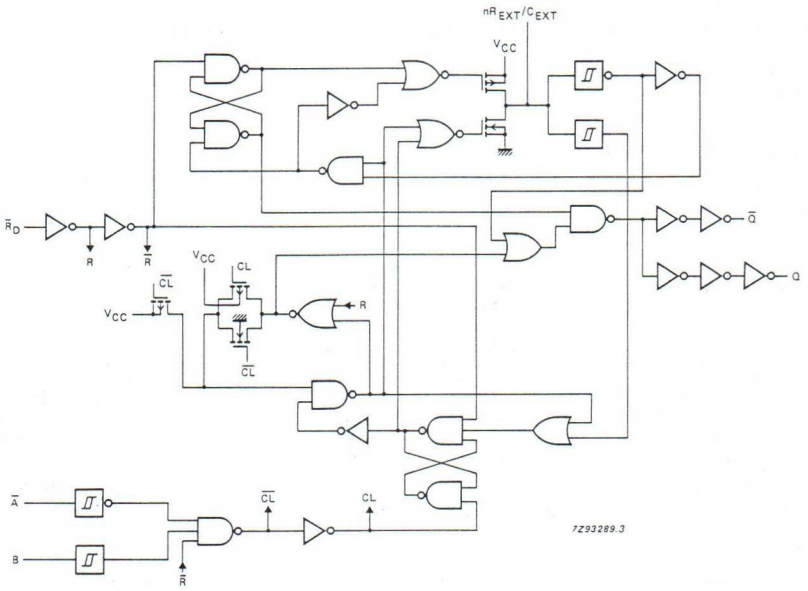


Fig. 5 Logic diagram.

Note to Fig. 5

It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

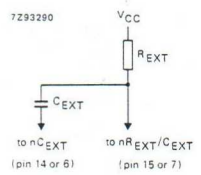


Fig. 6 Timing component connections.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS/NOTES
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$, nQ		80 29 23	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t_W	trigger pulse width $n\overline{A}$ = LOW	100 20 17	11 4 3		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	100 20 17	14 5 4		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		110		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	10 2		1000 1000	–		–		kΩ	2.0 5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{A}$, nB	0.35
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS/NOTES
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$, nQ		30	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		26	48		60		72	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	
t_W	trigger pulse width $n\overline{A}$ = LOW	20	5		25		30		ns	4.5	Fig. 7
t_W	trigger pulse width nB = HIGH	20	5		25		30		ns	4.5	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	20	7		25		30		ns	4.5	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		41		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig 9; note 3

Notes to AC characteristics

1. For other R_{EXT} and C_{EXT} combinations see Fig. 9.

   If $C_{EXT} > 10$ pF, the next formula is valid:

   $$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0 V and 0.55 for V_{CC} = 2.0 V.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.

   The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

   If $C_{EXT} > 10$ pF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:

   $$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.

   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

AC WAVEFORMS

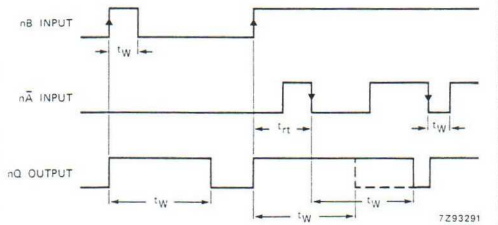


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

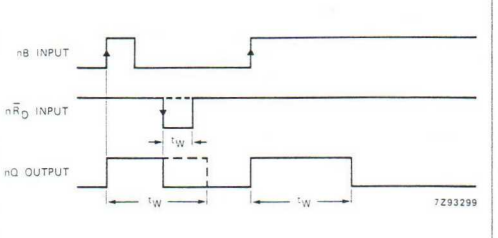


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; nĀ = LOW.

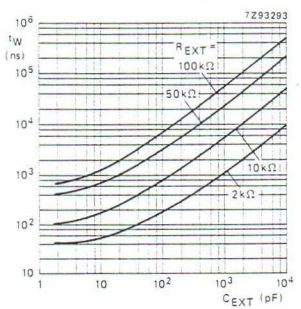


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

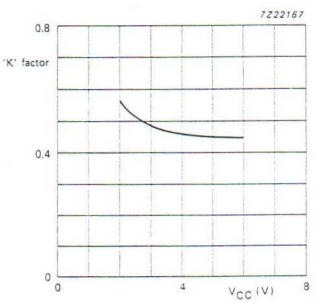


Fig. 10 Typical 'K' factor; external capacitance = 10 nF, external resistance = 10 kΩ to 100 kΩ and T_{amb} = 25 °C.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_X, this output pulse can be eliminated using the circuit shown in Fig. 11.

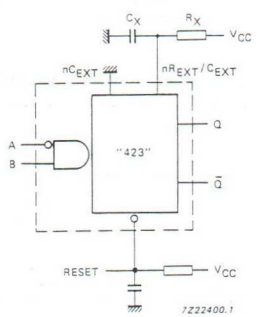


Fig. 11 Power-up output pulse elimination circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky-type diode able to withstand large current surges and connect as shown in Fig. 12.

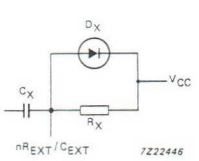


Fig. 12 Power-down protection circuit.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT533 are octal D-type transparent latches f eaturing separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$ LE to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	14 18	16 19	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	34	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

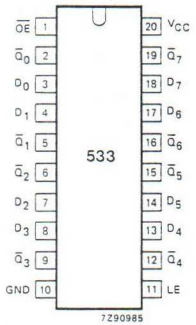


Fig. 1 Pin configuration.

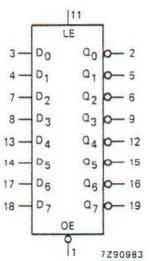


Fig. 2 Logic symbol.

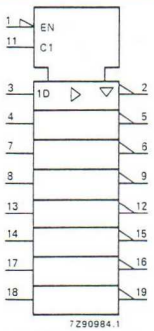


Fig. 3 IEC logic symbol.

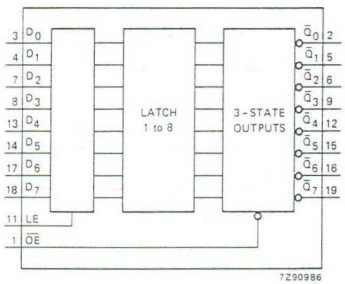


Fig. 4 Functional diagram.

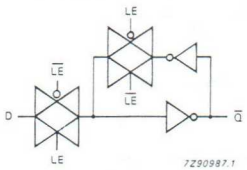


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register (transparent mode)	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	X	X	X	Z
	H	X	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level ont set-up prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

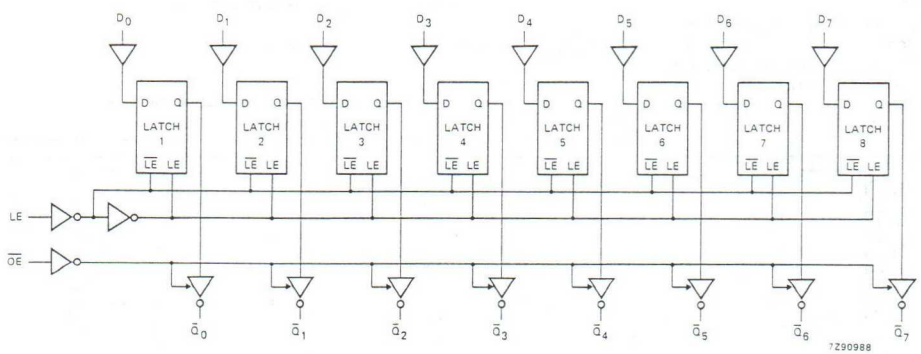


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t_W	LE pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to LE	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D_n to LE	35 7 6	3 1 1		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.15
$\overline{LE}$	0.30
$\overline{OE}$	0.55

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$		19	34		43		51	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		22	38		48		57	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 7
t_W	LE pulse width HIGH	16	5		20		24		ns	4.5	Fig. 8
t_{su}	set-up time D_n to LE	10	3		13		15		ns	4.5	Fig. 10
t_h	hold time D_n to LE	8	2		10		12		ns	4.5	Fig. 10

AC WAVEFORMS

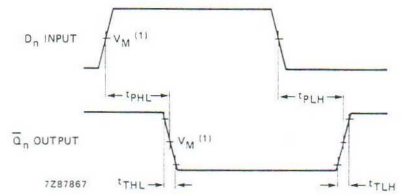


Fig. 7 Waveforms showing the data input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

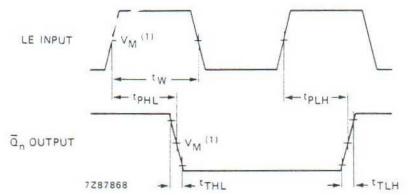


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

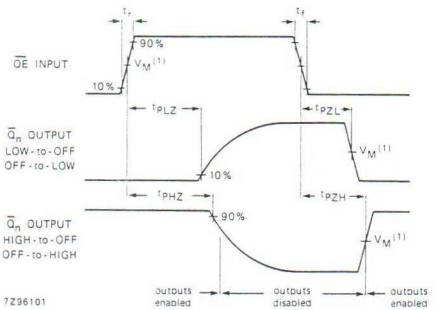


Fig. 9 Waveforms showing the 3-state enable and disable times.

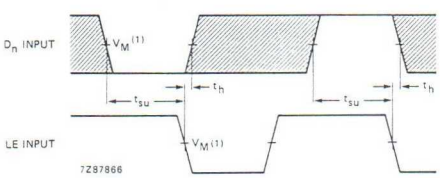


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT534 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "534" is functionally identical to the "374", but has inverted outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
f_{max}	maximum clock frequency		61	40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	19	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

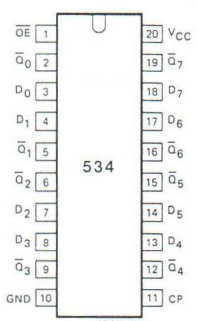


Fig. 1 Pin configuration.

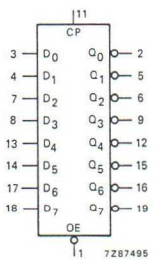


Fig. 2 Logic symbol.

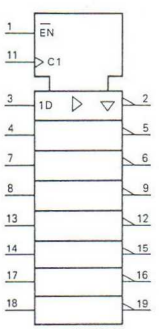


Fig. 3 IEC logic symbol.

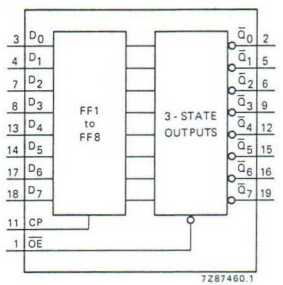


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

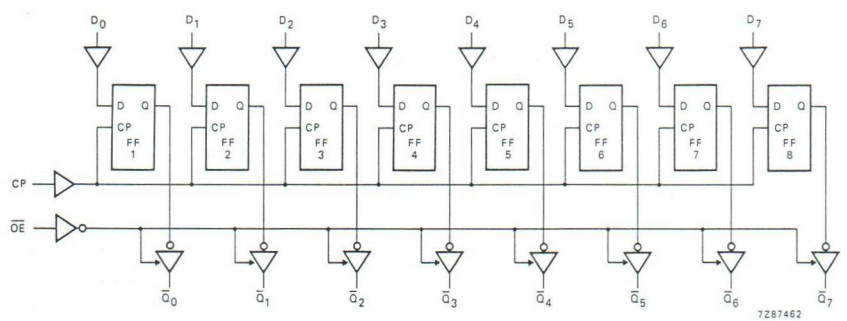


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$		41 15 12	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	5 5 5	−3 −1 −1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	18 55 66		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1.25
CP	0.90
D_n	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	23	14		29		35		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12	4		15		18		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5	−1		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	22	36		18		15		MHz	4.5	Fig. 6

AC WAVEFORMS

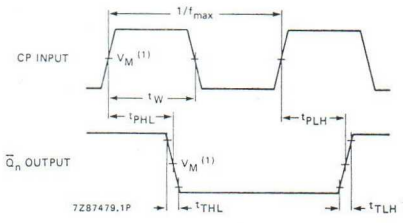


Fig. 6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

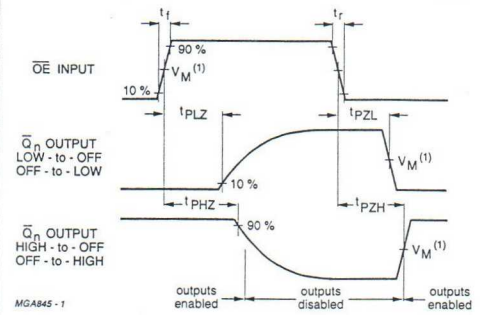


Fig. 7 Waveforms showing the 3-state enable and disable times.

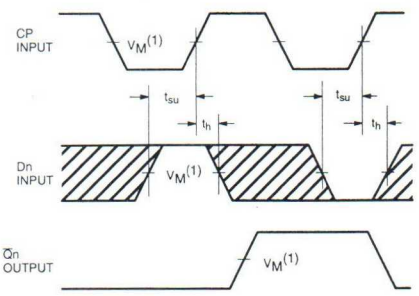


Fig. 8 Waveforms showing the data set-up and hold times for D_n input

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance

SK00017

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.
HCT : $V_M = 1.3V$; V_I = GND to 3V.

OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$. A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "540" is identical to the "541" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	39	44	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V_{CC}	positive supply voltage

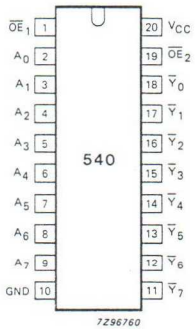


Fig. 1 Pin configuration.

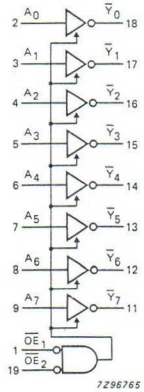


Fig. 2 Logic symbol.

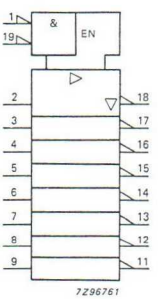


Fig. 3 IEC logic symbol.

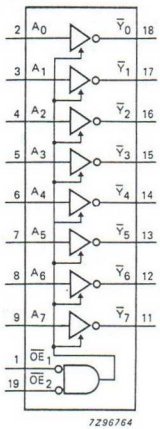


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

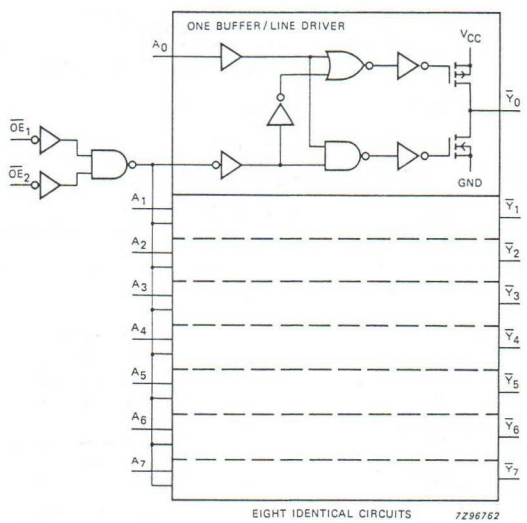


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		61 22 18	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.50
$\overline{OE}_2$	1.00
A_n	1.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		13	24		30		36	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		22	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		23	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

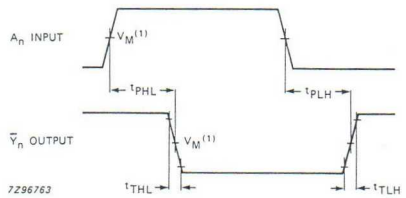


Fig. 6 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

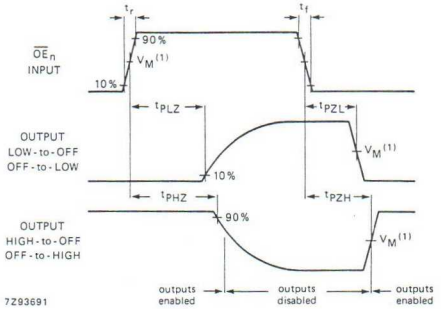


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT541 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "541" is identical to the "540" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	39	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

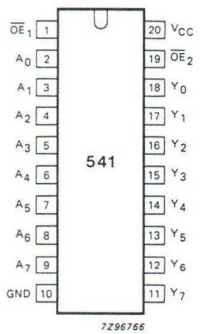


Fig. 1 Pin configuration.

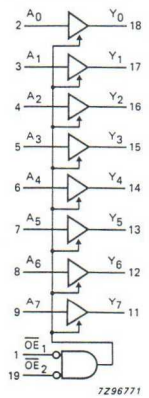


Fig. 2 Logic symbol.

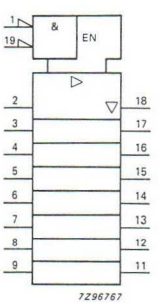


Fig. 3 IEC logic symbol.

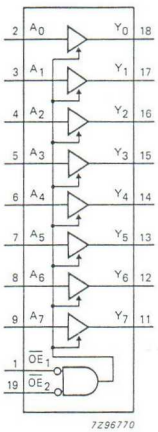


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

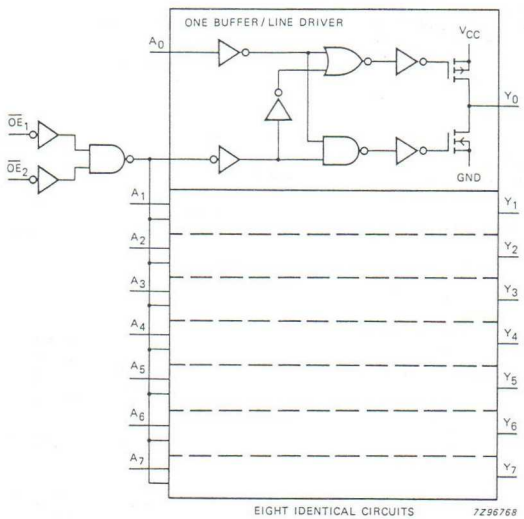


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		33 12 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y_n		55 20 16	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y_n		61 22 18	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.50
$\overline{OE}_2$	1.00
A_n	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n		15	28		35		42	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y_n		21	35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y_n		21	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

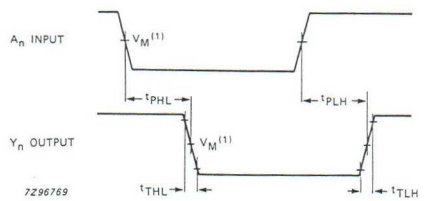


Fig. 6 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

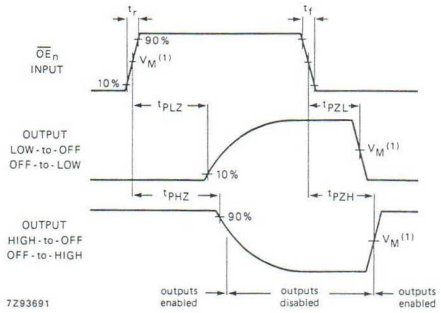


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.
A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and $\overline{OE}$ are common to all latches.
When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.
When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n, LE to $\overline{Q}_n$	C_L = 15 pF V_{CC} = 5 V	14	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
20	V_{CC}	positive supply voltage

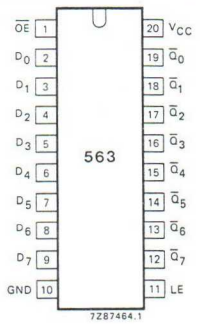


Fig. 1 Pin configuration.

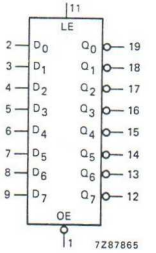


Fig. 2 Logic symbol.

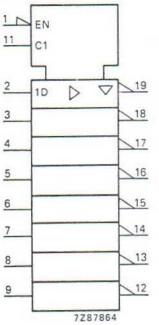


Fig. 3 IEC logic symbol.

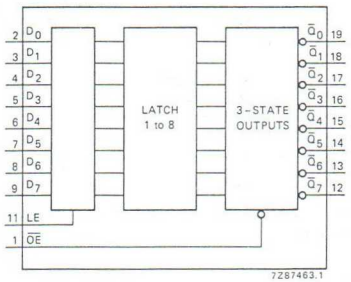


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state

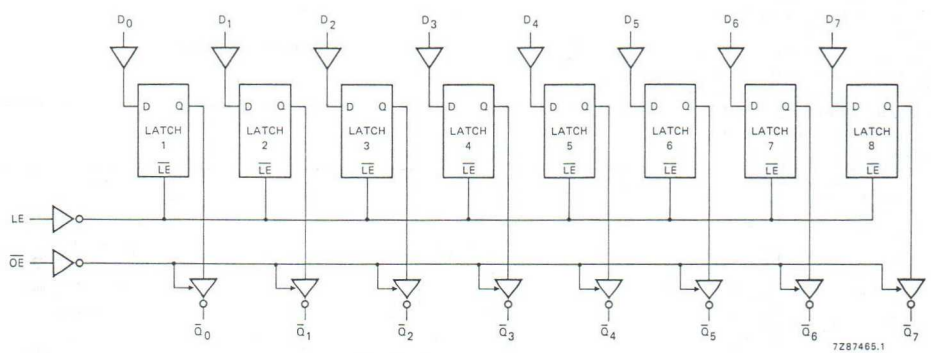


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to LE	4 4 4	−6 −2 −2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
$\overline{LE}$	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		20	35		44		53	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		22	35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_n to LE	10	3		13		15		ns	4.5	Fig. 9
t_h	hold time D_n to LE	5	−1		5		5		ns	4.5	Fig. 9

AC WAVEFORMS

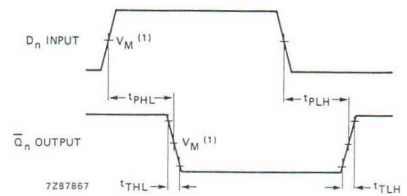


Fig. 6 Waveforms showing the data input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

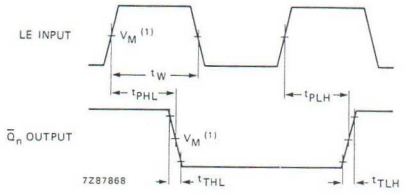


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

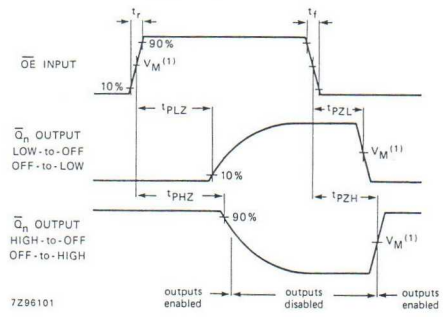


Fig. 8 Waveforms showing the 3-state enable and disable times.

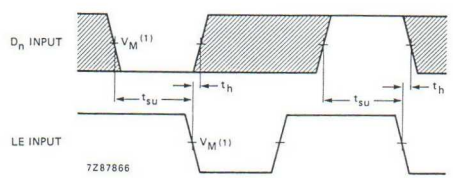


Fig. 9 Waveforms showing the data set-up and hold times for D_n input to LE input

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.
When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574", but has inverting outputs.
The "564" is functionally identical to the "534", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	15	16	ns
f_{max}	maximum clock frequency		127	62	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state flip-flop outputs
20	V_{CC}	positive supply voltage

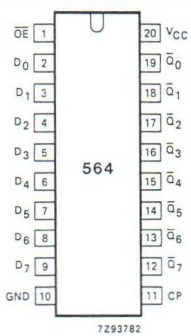


Fig. 1 Pin configuration.

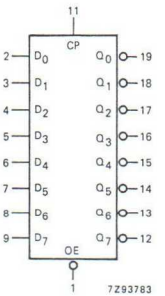


Fig. 2 Logic symbol.

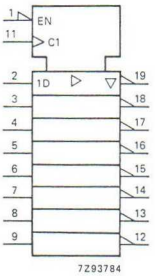


Fig. 3 IEC logic symbol.

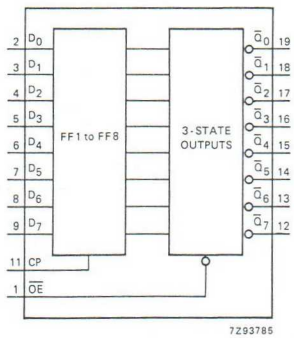


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

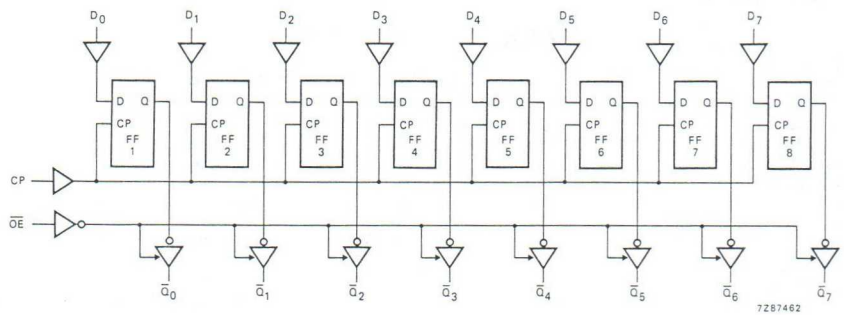


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		50 18 14	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time D_n to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	38 115 137		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.80
D_0 to D_7	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		19	30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18	8		23		27		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12	3		15		18		ns	4.5	Fig. 7
t_h	hold time D_n to CP	3	−2		3		3		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	27	56		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

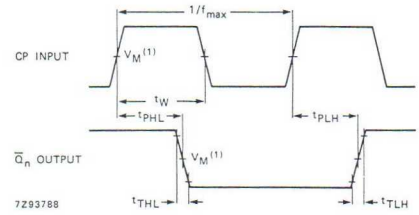


Fig. 6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

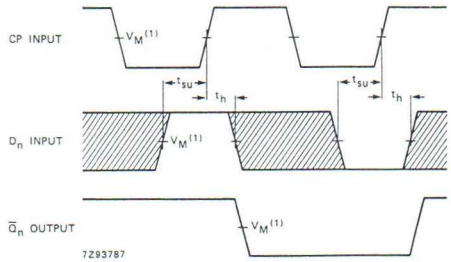


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

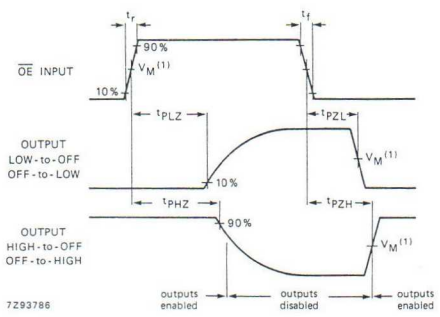


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LE to Q_n	C_L = 15 pF V_{CC} = 5 V	14 15	17 15	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	26	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
20	V_{CC}	positive supply voltage

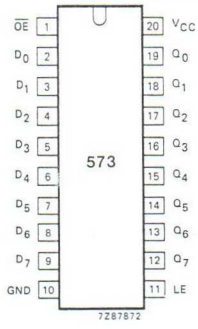


Fig. 1 Pin configuration.

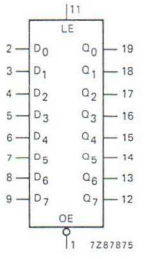


Fig. 2 Logic symbol.

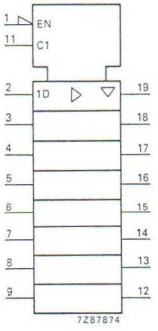


Fig. 3 IEC logic symbol.

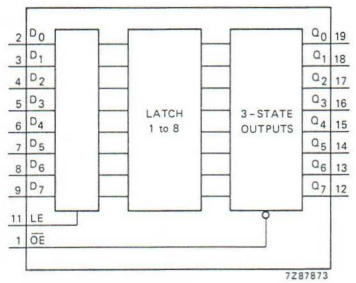


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

Z = high impedance OFF-state

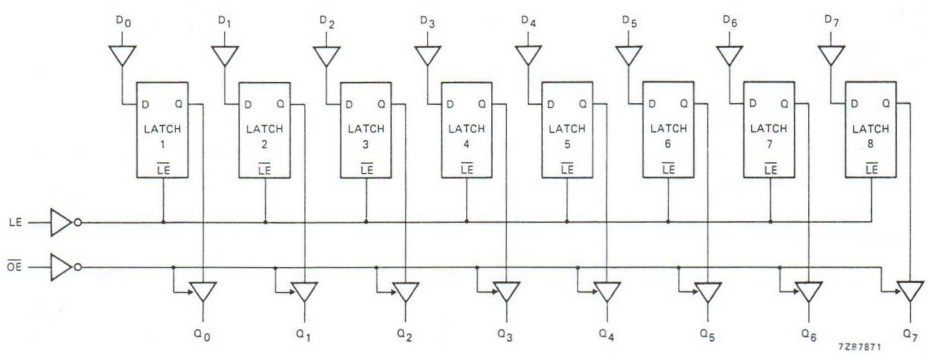


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to LE	5 5 5	3 1 1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
LE	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		20	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		18	35		44		53	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		17	30		38		45	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7
t_{su}	set-up time D_n to LE	13	7		16		20		ns	4.5	Fig. 9
t_h	hold time D_n to LE	9	4		11		14		ns	4.5	Fig. 9

AC WAVEFORMS

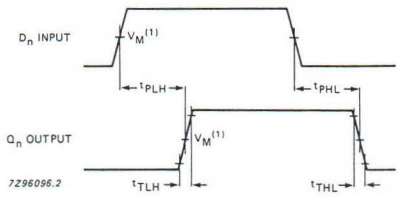


Fig. 6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

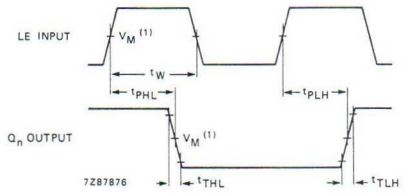


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

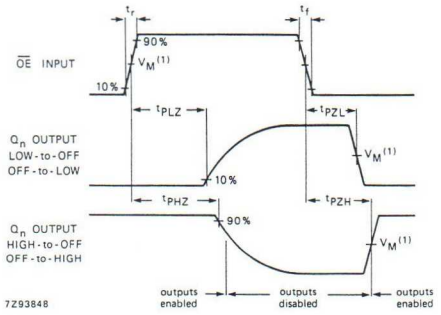


Fig. 8 Waveforms showing the 3-state enable and disable times.

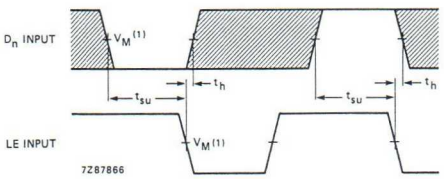


Fig. 9 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT574 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.
When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "574" is functionally identical to the "564", but has non-inverting outputs. The "574" is functionally identical to the "374", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	14	15	ns
f_{max}	maximum clock frequency		123	76	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	22	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state flip-flop outputs
20	V_{CC}	positive supply voltage

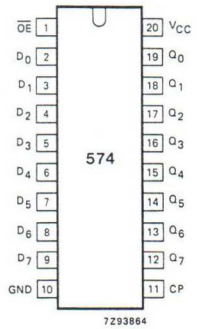


Fig. 1 Pin configuration.

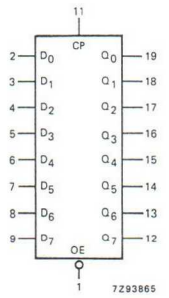


Fig. 2 Logic symbol.

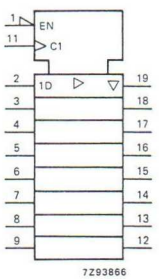


Fig. 3 IEC logic symbol.

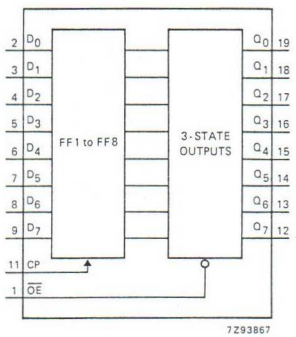


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

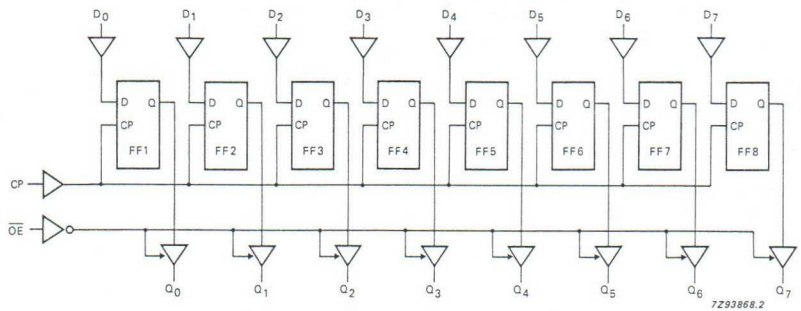


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		47 17 14	150 30 26		190 35 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	37 112 133		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.5
$\overline{OE}$	1.25
CP	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		18	33		41		50	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		19	33		41		50	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		16	28		35		42	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	12	3		15		18		ns	4.5	Fig. 8
t_h	hold time D_n to CP	5	−1		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	69		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

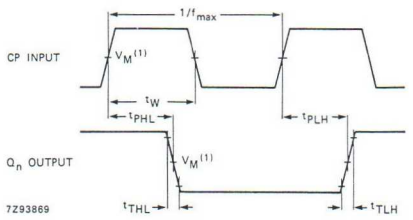


Fig. 6 Waveforms showing the clock input (CP) pulse width, the CP input to output (Q_n) propagation delays, the output transition times and the maximum clock pulse frequency.

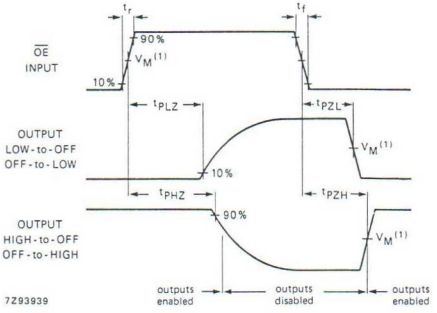


Fig. 7 Waveforms showing the 3-state enable and disable times.

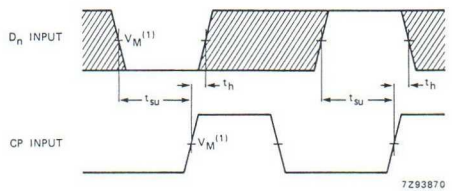


Fig. 8 Waveforms showing the data set-up and hold times for D_n input to CP input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT FULL ADDER WITH FAST CARRY

FEATURES

- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT583 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JECEC standard no. 7A.

The 74HC/HCT583 are high-speed 4-bit BCD full adders with internal carry look-ahead. They accept two 4-bit decimal numbers (A_0 to A_3 and B_0 to B_3) and a carry input (C_{IN}).

The "583" generates the decimal sum outputs (Σ_0 to Σ_3) and a carry output (C_{n+4}) if the sum is greater than 9.

If an addition of two BCD numbers produce a number greater than 9, a valid BCD number and a carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading "583s".

See the "283" for the binary version.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay C_{IN} to C_{n+4} A_n, B_n to C_{n+4}	C_L = 15 pF V_{CC} = 5 V	20 23	23 27	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	116	120	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5	C_{IN}	carry input
6	C_{n+4}	carry output
8	GND	ground (0 V)
11, 10, 7, 9	Σ_0 to Σ_3	sum outputs
12, 1, 2, 3	B_0 to B_3	B operand inputs
13, 14, 15, 4	A_0 to A_3	A operand inputs
16	V_{CC}	positive supply voltage

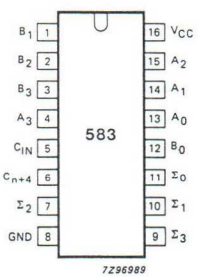


Fig. 1 Pin configuration.

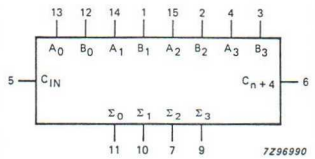


Fig. 2 Logic symbol.

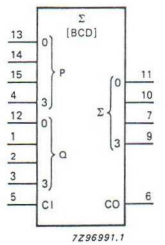


Fig. 3 IEC logic symbol.

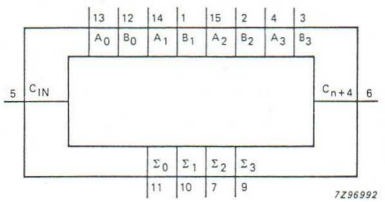


Fig. 4 Functional diagram.

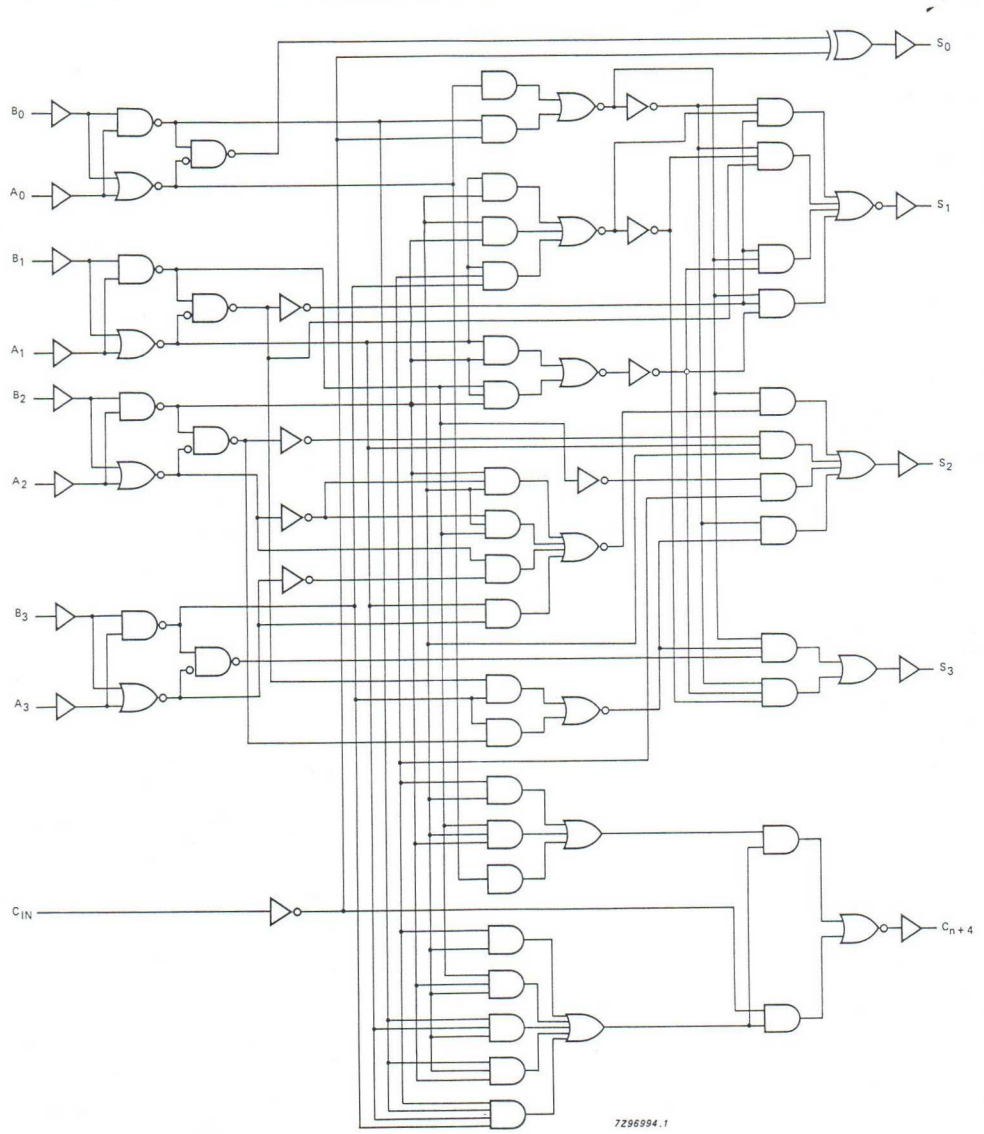


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_0		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		113 41 33	350 70 60		440 88 75		525 105 90	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		100 36 29	305 61 52		380 76 65		460 92 78	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		110 40 32	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_0		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_1		120 43 34	365 73 62		455 91 77		550 110 94	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_2		105 38 30	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_3		116 42 34	355 71 60		445 89 76		535 107 91	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{n+4}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n to C_{n+4}		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay B_n to C_{n+4}		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time standard outputs		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n, B_n	0.4
C_{IN}	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_0		20	34		43		51	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		40	68		85		102	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		38	65		81		98	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		38	65		81		98	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_0		22	37		46		56	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_1		43	73		91		110	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_2		40	68		85		102	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_3		41	70		88		105	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{n+4}		27	46		58		69	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay A_n to C_{n+4}		31	53		66		80	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay B_n to C_{n+4}		30	51		64		77	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

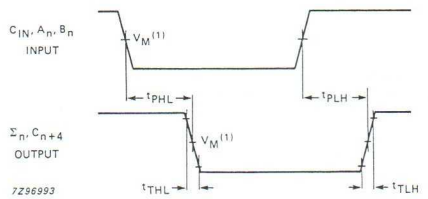


Fig. 6 Waveforms showing the inputs (C_{IN}, A_n, B_n) to the outputs (Σ_n, C_{n+4}) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-bit shift register with output register

74HC/HCT594

FEATURES

- Synchronous serial input and output
- 8-bit parallel output
- Shift and storage register have independent direct clear and clocks
- 100 MHz (typ.)
- Output capability:
  - parallel outputs: bus driver
  - serial outputs: standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to parallel data conversion
- Remote control holding register

DESCRIPTION

The 74HC/HCT594 are high-speed, Si-gate CMOS devices, and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74HC/HCT594 contain an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided on both the shift and storage registers. A serial output (Q_7') is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	SH_{CP} to Q_7'		13	15	ns
	ST_{CP} to Q_n		13	15	ns
	$\overline{SH}_R$ to Q_n		11	14	ns
	$\overline{ST}_R$ to Q_n		11	14	ns
f_{max}	maximum clock frequency SH_{CP}, ST_{CP}		100	100	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	84	89	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW). $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$, where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in V.
2. For HC, the condition is V_I = GND to V_{CC}.
   For HCT, the condition is V_I = GND to $_{VCC}$ – 1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
PC74HC/HCT594P	16	DIL	plastic	SOT38C, P
PC74HC/HCT594T	16	SO	plastic	SOT109A

8-bit shift register with output register

74HC/HCT594

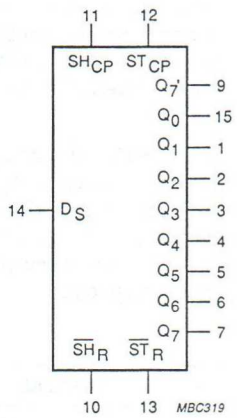


Fig.1 Logic symbol.

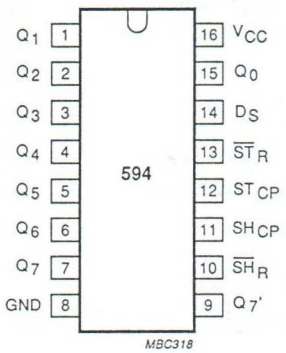


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
Q_0 to Q_7	15 & 1 to 7	parallel data outputs
GND	8	ground (0 V)
Q_7'	9	serial data output
$\overline{SH}_R$	10	shift register reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{ST}_R$	13	storage register reset active (LOW)
D_S	14	serial data input
V_{CC}	16	supply voltage

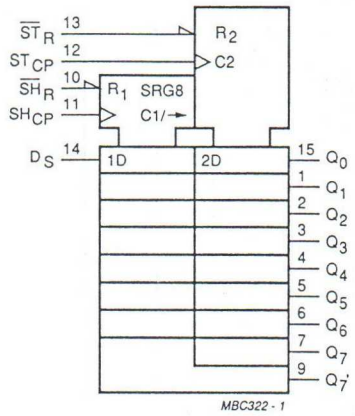


Fig.3 IEC logic symbol.

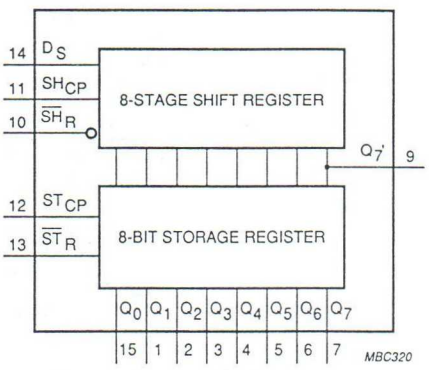


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{SH}_R$	$\overline{ST}_R$	D_S	Q_7'	Q_n	
X	X	L	X	X	L	NC	a LOW level on $\overline{SH}_R$ only affects the shift registers.
X	X	X	L	X	NC	L	a LOW level on $\overline{ST}_R$ only affects the storage registers.
X	↑	L	H	X	L	L	empty shift register loaded into storage register.
↑	X	H	X	H	Q_6'	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on the serial output (Q_7').
X	↑	H	H	X	NC	Q_n'	contents of shift register stages (internal Q_n') are transferred to the storage register and parallel output stages.
↑	↑	H	H	X	Q_6n	Q_n'	contents of shift register shifted through. Previous contents of shift register transferred to the storage register and the parallel output stages.

H = HIGH voltage level

L = LOW voltage level

↑ = LOW-to-HIGH transition

NC = no change

X = don't care.

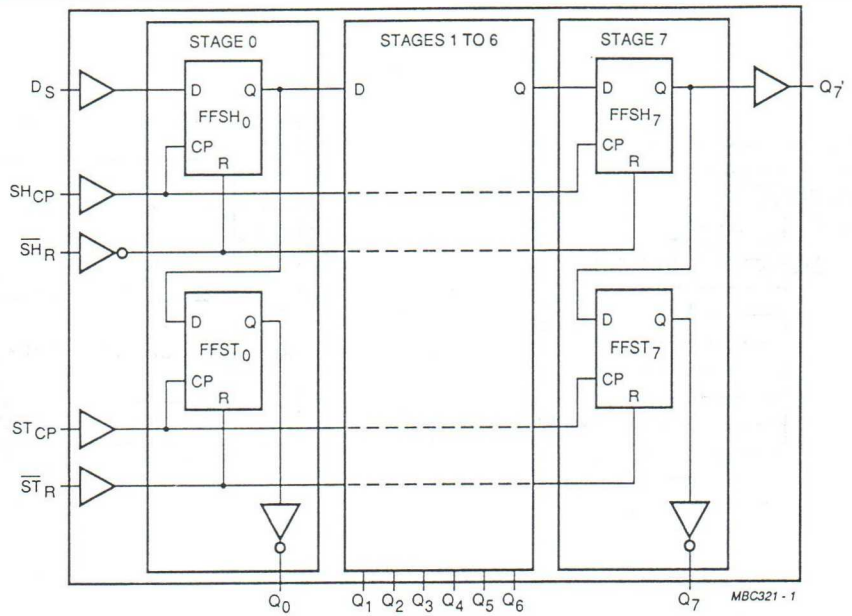


Fig.5 Logic diagram.

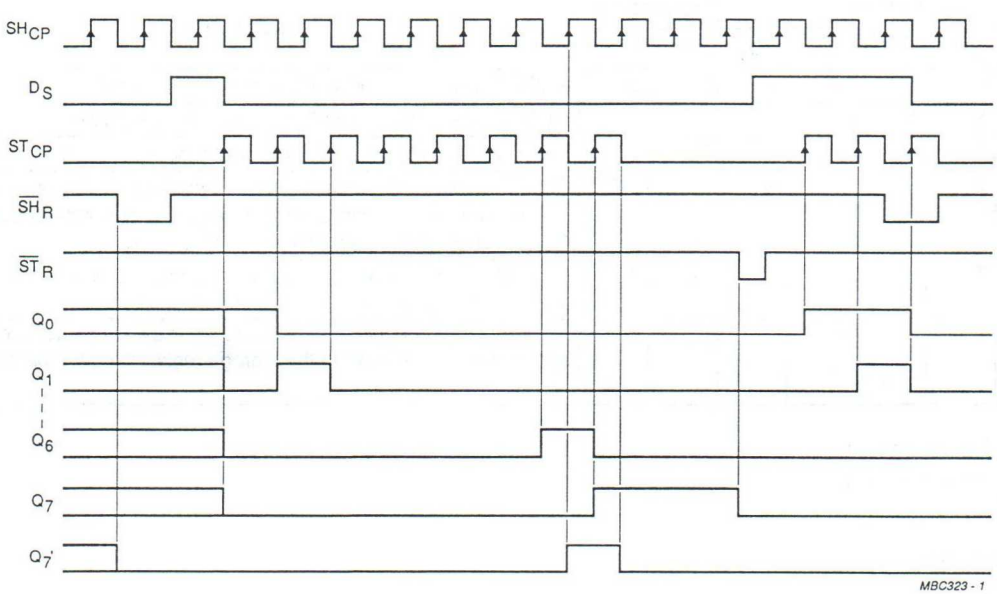


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics, see chapter 'HCMOS family characteristics', section 'Family specifications'.

Output capability: parallel outputs, bus driver; serial output, standard.

I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVE-FORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	44	150	–	185	–	225	ns	2.0	Fig.7
		–	16	30	–	37	–	45	ns	4.5	
		–	14	26	–	31	–	38	ns	6.0	
	propagation delay ST_{CP} to Q_n	–	44	150	–	185	–	225	ns	2.0	Fig.8
		–	16	30	–	37	–	45	ns	4.5	
		–	14	26	–	31	–	38	ns	6.0	
t_{PHL}	propagation delay $\overline{SH}_R$ to Q_7'	–	39	150	–	185	–	225	ns	2.0	Fig.11
		–	14	30	–	37	–	45	ns	4.5	
		–	12	26	–	31	–	38	ns	6.0	
	propagation delay $\overline{ST}_R$ to Q_n	–	39	125	–	155	–	185	ns	2.0	Fig.12
		–	14	25	–	31	–	37	ns	4.5	
		–	12	21	–	26	–	31	ns	6.0	
t_W	shift clock pulse width HIGH or LOW	80	10	–	100	–	120	–	ns	2.0	Fig.7
		16	4	–	20	–	24	–	ns	4.5	
		14	3	–	17	–	20	–	ns	6.0	
	storage clock pulse width HIGH or LOW	80	10	–	100	–	120	–	ns	2.0	Fig.8
		16	4	–	20	–	24	–	ns	4.5	
		14	3	–	17	–	20	–	ns	6.0	
	shift and storage reset pulse width HIGH or LOW	80	14	–	100	–	120	–	ns	2.0	Figs 11 and 12
		16	5	–	20	–	24	–	ns	4.5	
		14	4	–	17	–	20	–	ns	6.0	
t_{su}	set-up time D_S to SH_{CP}	100	10	–	125	–	150	–	ns	2.0	Fig.9
		20	4	–	25	–	30	–	ns	4.5	
		17	3	–	21	–	26	–	ns	6.0	
	set-up time $\overline{SH}_R$ to ST_{CP}	100	14	–	125	–	150	–	ns	2.0	Fig.10
		20	5	–	25	–	30	–	ns	4.5	
		17	4	–	21	–	26	–	ns	6.0	
	set-up time SH_{CP} to ST_{CP}	100	17	–	125	–	150	–	ns	2.0	Fig.8
		20	6	–	25	–	30	–	ns	4.5	
		17	5	–	21	–	26	–	ns	6.0	

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVE-FORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_h	hold time D_S to SH_{CP}	25	−8	−	30	−	35	−	ns	2.0	Fig.9
		5	−3	−	6	−	7	−	ns	4.5	
		4	−2	−	5	−	6	−	ns	6.0	
t_{rem}	removal time $\overline{SH}_R$ to SH_{CP}, $\overline{ST}_R$ to ST_{CP}	50	−14	−	65	−	75	−	ns	2.0	Figs 11 and 12
		10	−5	−	13	−	15	−	ns	4.5	
		9	−4	−	11	−	13	−	ns	6.0	
f_{max}	maximum clock frequency SH_{CP} or ST_{CP}	6.0	30	−	4.8	−	4.0	−	MHz	2.0	Figs 7 and 8
		30	92	−	24	−	20	−	MHz	4.5	
		35	109	−	28	−	24	−	MHz	6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics, see chapter 'HCMOS family characteristics', section 'Family specifications'.

Output capability: parallel outputs, bus driver; serial output, standard.

I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
$\overline{SH}_R$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{ST}_R$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVE-FORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	18	32	–	40	–	48	ns	4.5	Fig.7
	propagation delay ST_{CP} to Q_n	–	18	32	–	40	–	48	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{SH}_R$ to Q_7'	–	17	30	–	38	–	45	ns	4.5	Fig.11
	propagation delay $\overline{ST}_R$ to Q_n	–	17	30	–	38	–	45	ns	4.5	Fig.12
t_W	shift clock pulse width HIGH or LOW	16	4	–	20	–	24	–	ns	4.5	Fig.7
	storage clock pulse width HIGH or LOW	16	4	–	20	–	24	–	ns	4.5	Fig.8
	shift and storage reset pulse width HIGH or LOW	16	6	–	20	–	24	–	ns	4.5	Figs 11 and 12
t_{su}	set-up time D_S to SH_{CP}	20	4	–	25	–	30	–	ns	4.5	Fig.9
	set-up time $\overline{SH}_R$ to ST_{CP}	20	6	–	25	–	30	–	ns	4.5	Fig.10
	set-up time SH_{CP} to ST_{CP}	20	7	–	25	–	30	–	ns	4.5	Fig.8
t_h	hold time D_S to SH_{CP}	5	−3	–	6	–	7	–	ns	4.5	Fig.9
t_{rem}	removal time $\overline{SH}_R$ to SH_{CP}, $\overline{ST}_R$ to ST_{CP}	10	−5	–	13	–	15	–	ns	4.5	Figs 11 and 12
f_{max}	maximum clock frequency SH_{CP} or ST_{CP}	30	92	–	24	–	20	–	MHz	4.5	Figs 7 and 8

AC WAVEFORMS

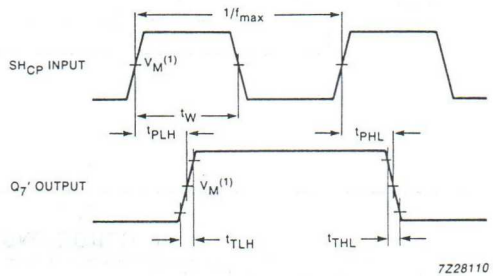


Fig.7 Waveforms showing the shift clock (SH_{CP}) to output (Q_7') propagation delays, the shift clock pulse width and the maximum shift clock frequency.

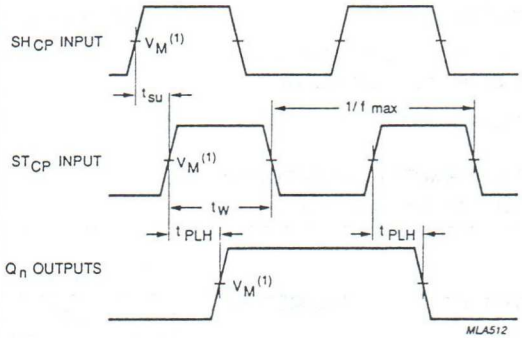


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width, maximum storage clock frequency and the shift clock to storage clock set-up time.

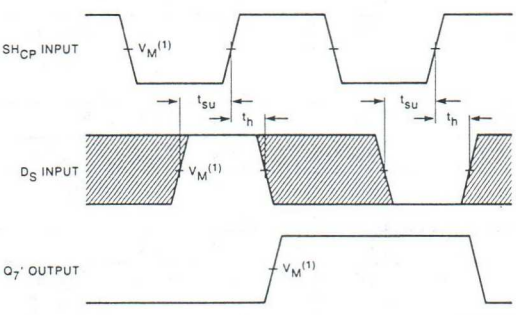


Fig.9 Waveforms showing the data set-up and hold times for the D_S input.

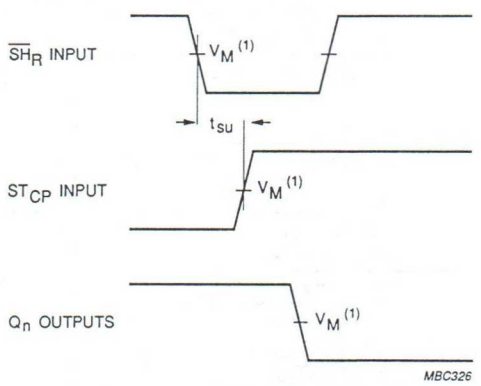


Fig.10 Waveforms showing the set-up time from shift reset ($\overline{SH}_R$) to storage clock (ST_{CP}).

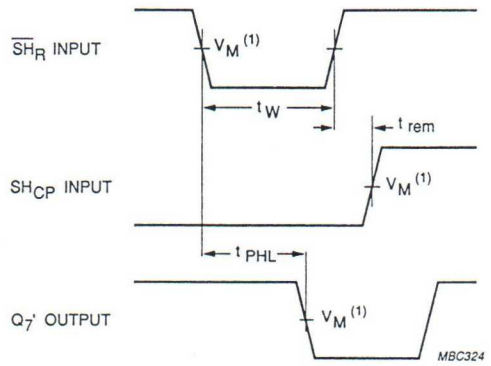


Fig.11 Waveforms showing the shift reset ($\overline{SH}_R$) pulse width, the shift reset to output (Q_7') propagation delay and the shift reset to shift clock (SH_{CP}) removal time.

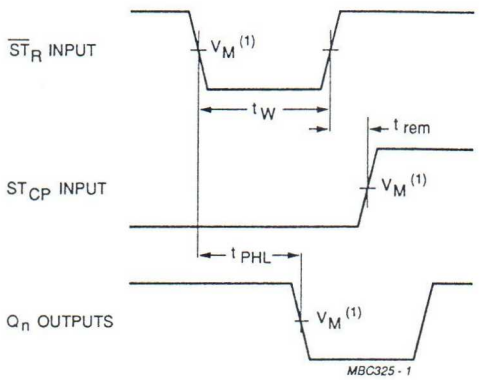


Fig.12 Waveforms showing the storage reset ($\overline{ST}_R$) pulse width, the storage reset to outputs (Q_n) propagation delay and the storage reset to storage clock (ST_{CP}) removal time.

Note (1)

HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- I_{CC} category: MSI.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The "595" is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7' ST_{CP} to Q_n $\overline{MR}$ to Q_7'	C_L = 15 pF V_{CC} = 5 V	16 17 14	21 20 19	ns ns ns
f_{max}	maximum clock frequency SH_{CP}, ST_{CP}		100	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

Notes

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz C_L = output load capacitance in pF

f_o = output frequency in MHz V_{CC} = supply voltage in V

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} - 1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT595N	16	DIL	plastic	SOT38Z
74HC/HCT595D	16	SO16	plastic	SOT109A

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

PINNING

SYMBOL	PIN	DESCRIPTION
Q_0 - Q_7	15, 1 - 7	parallel data output
GND	8	ground (0 V)
Q_7'	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{OE}$	13	output enable (active LOW)
D_S	14	serial data input
V_{CC}	16	positive supply voltage

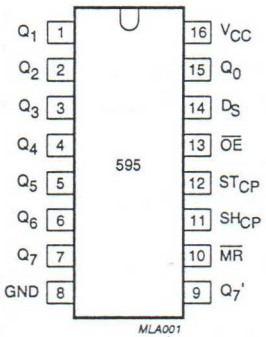


Fig.1 Pin configuration.

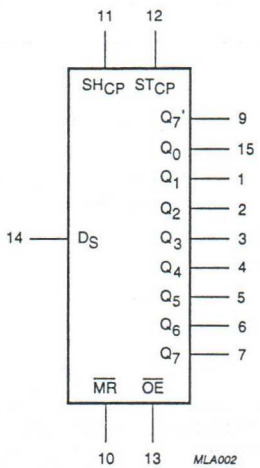


Fig.2 Logic symbol.

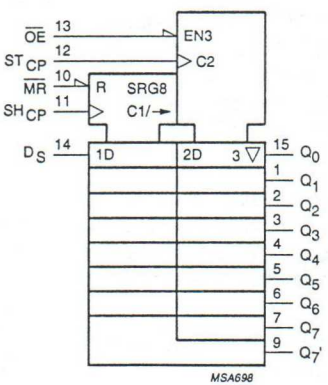


Fig.3 IEC logic symbol.

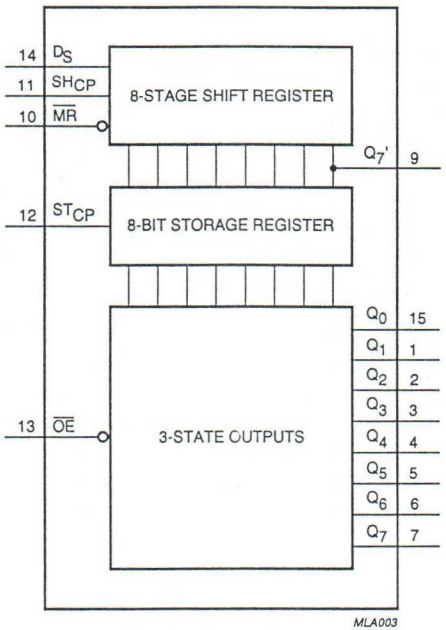


Fig.4 Functional diagram.

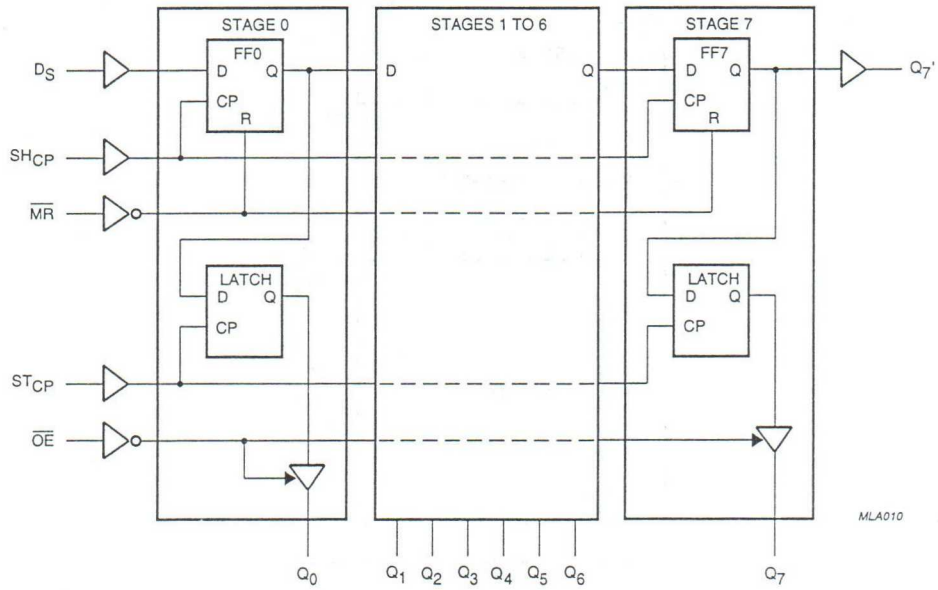


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS					OUPTUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	Q_7'	Q_n	
X	X	L	↓	X	L	NC	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q_6'	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on the serial output (Q_7')
X	↑	L	H	X	NC	Q_n'	contents of shift register stages (internal Q_n') are transferred to the storage register andparallel output stages
↑	↑	L	H	X	Q_6'	Q_n'	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
Z = high-impedance OFF-state
NC = no change
X = don't care.

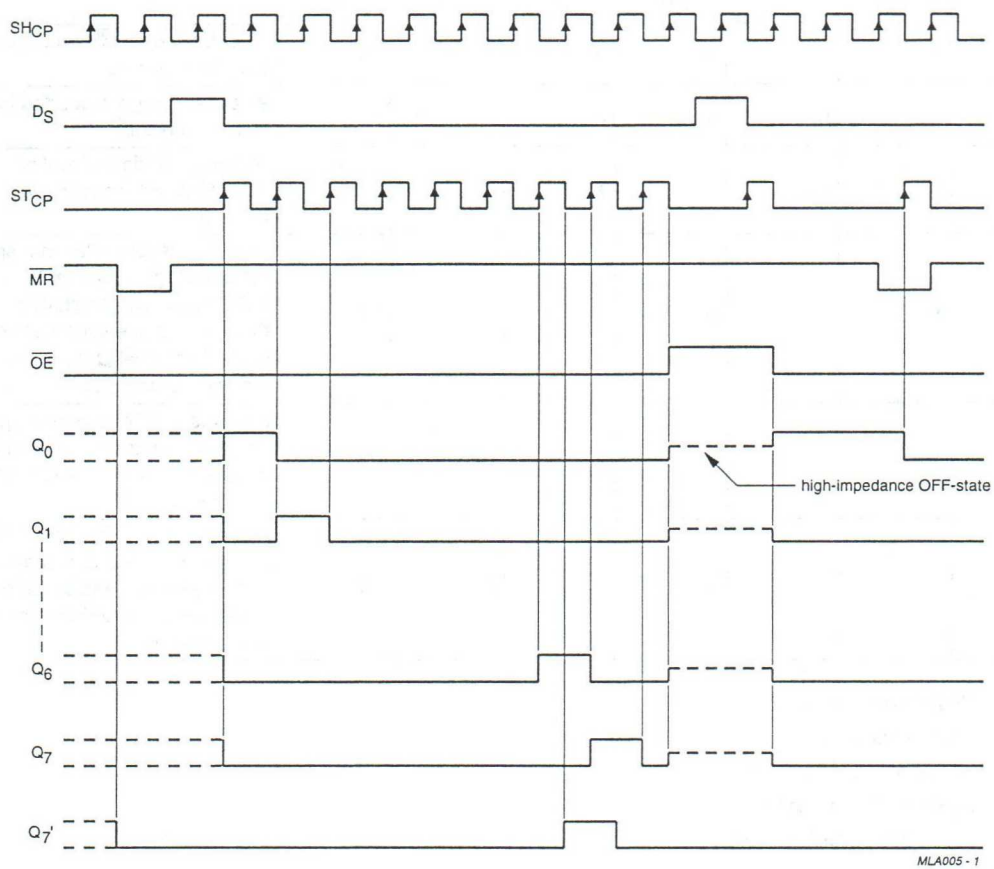


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	52	160	–	200	–	240	ns	2.0	Fig.7
		–	19	32	–	40	–	48	ns	4.5	
		–	15	27	–	34	–	41	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q_n	–	55	175	–	220	–	265	ns	2.0	Fig.8
		–	20	35	–	44	–	53	ns	4.5	
		–	16	30	–	37	–	45	ns	6.0	
t_{PHL}	propagation delay $\overline{MR}$ to Q_7'	–	47	175	–	220	–	265	ns	2.0	Fig.10
		–	17	35	–	44	–	53	ns	4.5	
		–	14	30	–	37	–	45	ns	6.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	47	150	–	190	–	225	ns	2.0	Fig.11
		–	17	30	–	38	–	45	ns	4.5	
		–	14	26	–	33	–	38	ns	6.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	41	150	–	190	–	225	ns	2.0	Fig.11
		–	15	30	–	38	–	45	ns	4.5	
		–	12	26	–	33	–	38	ns	6.0	
t_W	shift clock pulse width HIGH or LOW	75	17	–	95	–	110	–	ns	2.0	Fig.7
		15	6	–	19	–	22	–	ns	4.5	
		13	5	–	16	–	19	–	ns	6.0	
t_W	storage clock pulse width HIGH or LOW	75	11	–	95	–	110	–	ns	2.0	Fig.8
		15	4	–	19	–	22	–	ns	4.5	
		13	3	–	16	–	19	–	ns	6.0	
t_W	master reset pulse width LOW	75	17	–	95	–	110	–	ns	2.0	Fig.10
		15	6.0	–	19	–	22	–	ns	4.5	
		13	5.0	–	16	–	19	–	ns	6.0	
t_{su}	set-up time D_S to SH_{CP}	50	11	–	65	–	75	–	ns	2.0	Fig.9
		10	4.0	–	13	–	15	–	ns	4.5	
		9.0	3.0	–	11	–	13	–	ns	6.0	
t_{su}	set-up time SH_{CP} to ST_{CP}	75	22	–	95	–	110	–	ns	2.0	Fig.8
		15	8	–	19	–	22	–	ns	4.5	
		13	7	–	16	–	19	–	ns	6.0	
t_h	hold time D_S to SH_{CP}	3	−6	–	3	–	3	–	ns	2.0	Fig.9
		3	−2	–	3	–	3	–	ns	4.5	
		3	−2	–	3	–	3	–	ns	6.0	
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	50	−19	–	65	–	75	–	ns	2.0	Fig.10
		10	−7	–	13	–	15	–	ns	4.5	
		9	−6	–	11	–	13	–	ns	6.0	

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	6	30	–	4.8	–	4	–	MHz	2.0	Figs 7 and 8
		30	91	–	24	–	20	–	MHz	4.5	
		35	108	–	28	–	24	–	MHz	6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard
I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
$\overline{MR}$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{OE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	25	42	–	53	–	63	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q_n	–	24	40	–	50	–	60	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_7'	–	23	40	–	50	–	60	ns	4.5	Fig.10
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	21	35	–	44	–	53	ns	4.5	Fig.11
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	18	30	–	38	–	45	ns	4.5	Fig.11
t_W	shift clock pulse width HIGH or LOW	16	6	–	20	–	24	–	ns	4.5	Fig.7
t_W	storage clock pulse width HIGH or LOW	16	5	–	20	–	24	–	ns	4.5	Fig.8
t_W	master reset pulse width LOW	20	8	–	25	–	30	–	ns	4.5	Fig.10
t_{su}	set-up time D_S to SH_{CP}	16	5	–	20	–	24	–	ns	4.5	Fig.9
t_{su}	set-up time SH_{CP} to ST_{CP}	16	8	–	20	–	24	–	ns	4.5	Fig.8
t_h	hold time D_S to SH_{CP}	3	–2	–	3	–	3	–	ns	4.5	Fig.9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	10	–7	–	13	–	15	–	ns	4.5	Fig.10
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	30	52	–	24	–	20	–	MHz	4.5	Figs 7 and 8

AC WAVEFORMS

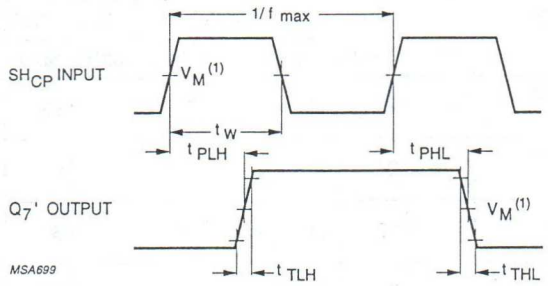


Fig.7 Waveforms showing the clock (SH_{CP}) to output (Q_7') propagation delays, the shift clock pulse width and maximum shift clock frequency.

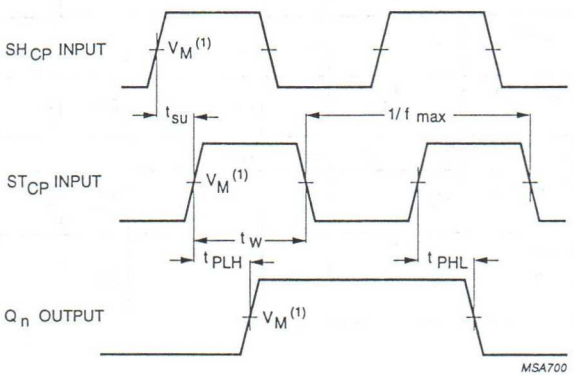


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

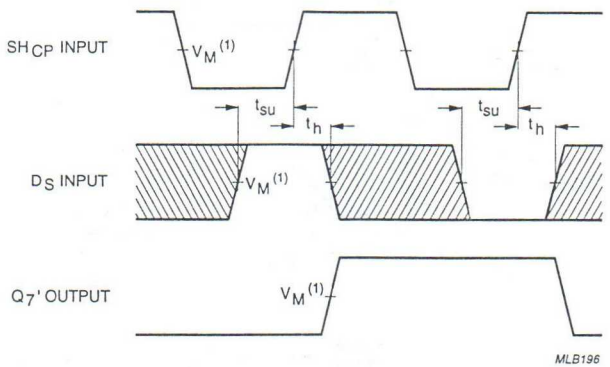


Fig.9 Waveforms showing the data set-up and hold times for the D_S input.

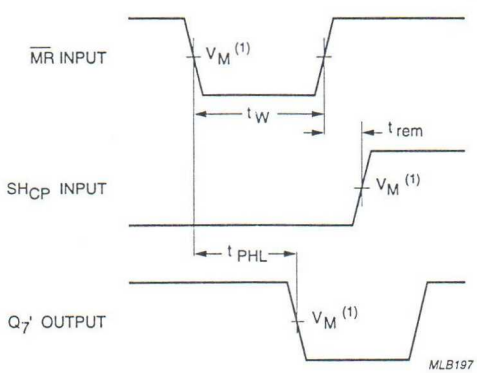


Fig.10 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_7') propagation delay and the master reset to shift clock (SH_{CP}) removal time.

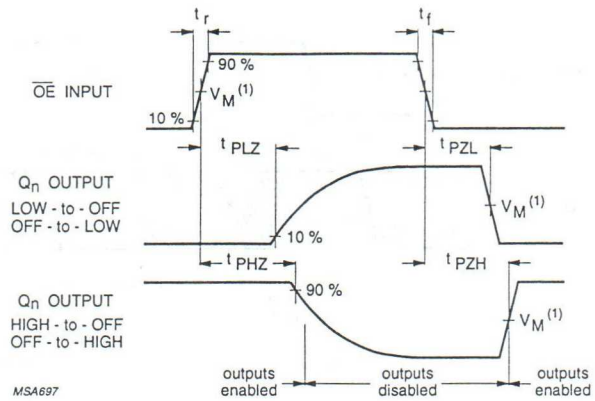


Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT SHIFT REGISTER WITH INPUT FLIP-FLOPS

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky (TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q ST_{CP} to Q $\overline{PL}$ to Q	C_L = 15 pF V_{CC} = 5 V	17 25 21	20 29 26	ns ns ns
f_{max}	maximum clock frequency SH_{CP}		96	83	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	29	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

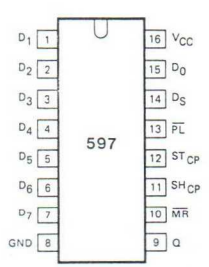


Fig. 1 Pin configuration.

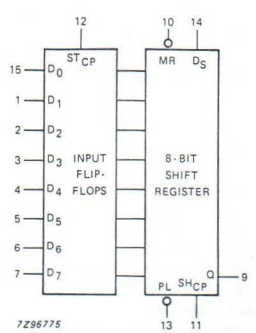


Fig. 2 Logic symbol.

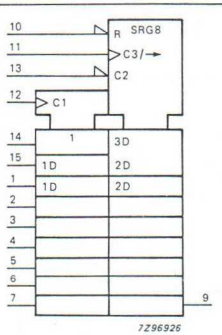


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH_{CP}	shift clock input (LOW-to-HIGH, edge-triggered)
12	ST_{CP}	storage clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	parallel load input (active LOW)
14	D_S	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D_0 to D_7	parallel data inputs
16	V_{CC}	positive supply voltage

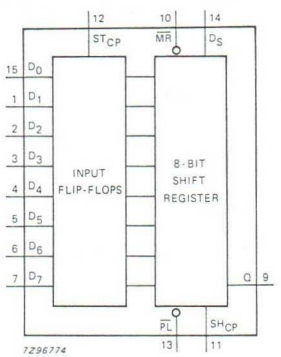


Fig. 4 Functional diagram.

FUNCTION TABLE

ST_{CP}	SH_{CP}	$\overline{PL}$	$\overline{MR}$	FUNCTION
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

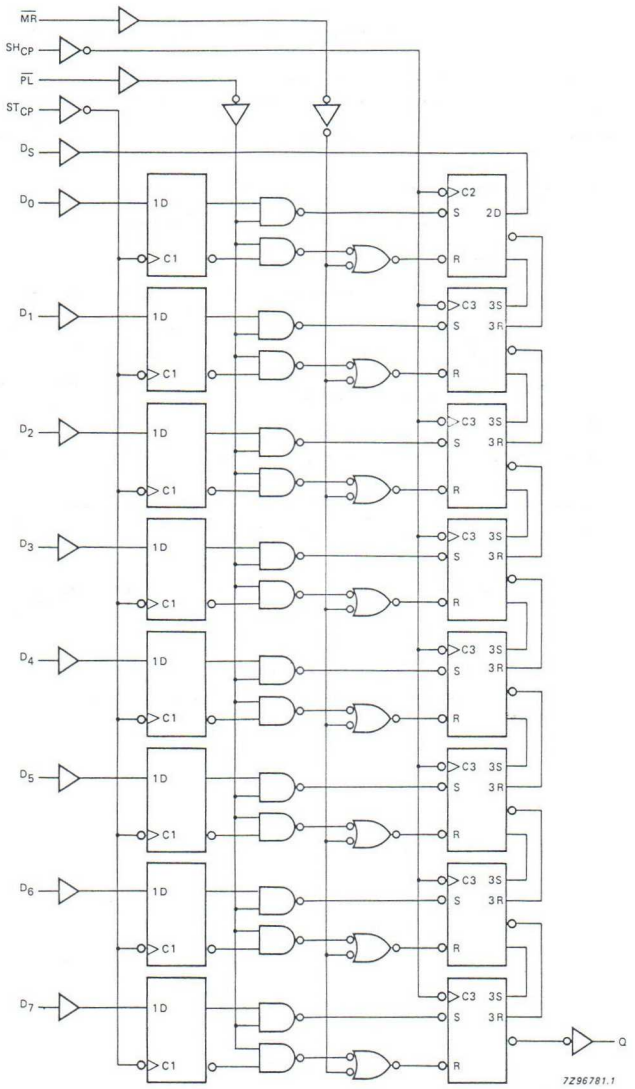


Fig. 5 Logic diagram.

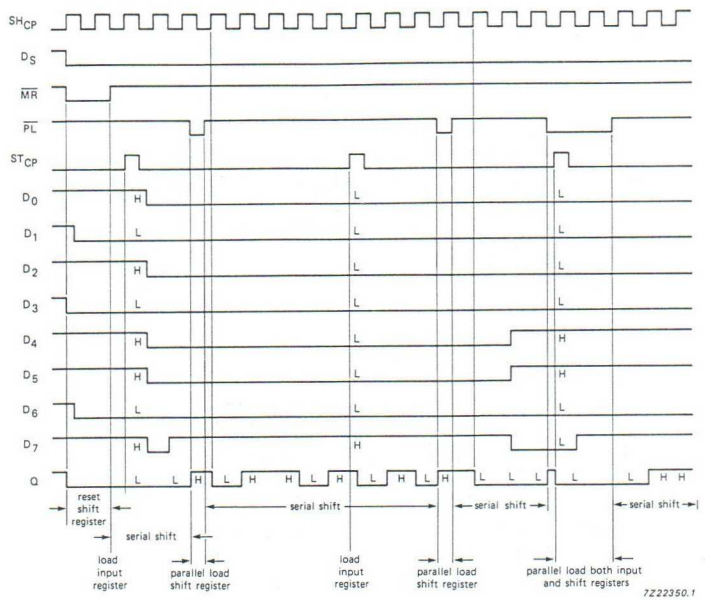


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	ST_{CP} pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	SH_{CP} pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	$\overline{MR}$ pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	$\overline{PL}$ pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	60 12 10	−3 −1 −1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time D_n to ST_{CP}	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time D_S to SH_{CP}	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 12

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to ST_{CP}	5 5 5	−3 −1 −1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{PL}$, D_S to SH_{CP}	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 11
f_{max}	maximum pulse frequency SH_{CP}	6.0 30 35	29 87 104		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
D_n	0.30
$\overline{PL}$, $\overline{MR}$	1.50
ST_{CP}, SH_{CP}	1.50

AC WAVEFORMS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q		23	40		50		60	ns	4.5	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q		28	49		61		74	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q		33	57		71		86	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q		30	52		65		78	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	SH_{CP} pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
t_W	ST_{CP} pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 7
t_W	$\overline{MR}$ pulse width LOW	25	14		31		38		ns	4.5	Fig. 8
t_W	$\overline{PL}$ pulse width LOW	20	10		25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	12	−2		15		18		ns	4.5	Fig. 10
t_{su}	set-up time D_n to ST_{CP}	12	5		15		18		ns	4.5	Fig. 11
t_{su}	set-up time D_S to SH_{CP}	12	2		15		18		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	12	4		15		18		ns	4.5	Fig. 12
t_h	hold time D_n to ST_{CP}	5	−1		5		5		ns	4.5	Fig. 11
t_h	hold time $\overline{PL}$, D_S to SH_{CP}	5	−2		5		5		ns	4.5	Fig. 11
f_{max}	maximum pulse frequency SH_{CP}	30	75		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

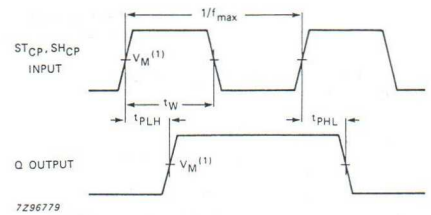


Fig. 7 Waveforms showing the SH_{CP} and ST_{CP} inputs to Q output propagation delays, the SH_{CP} and ST_{CP} pulse widths and maximum clock pulse frequency.

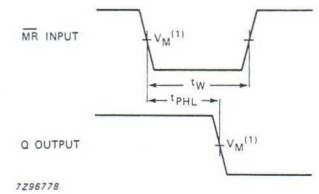


Fig. 8 Waveforms showing the $\overline{MR}$ input to Q output propagation delays and the $\overline{MR}$ pulse width.

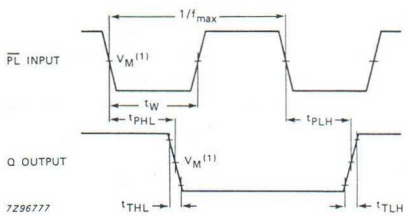


Fig. 9 Waveforms showing the $\overline{PL}$ input to Q output propagation delays, $\overline{PL}$ pulse width and output transition times.

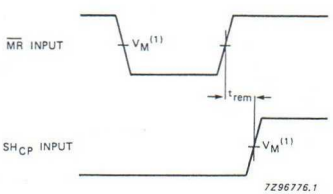


Fig. 10 Waveforms showing the $\overline{MR}$ input to SH_{CP}, ST_{CP} removal times.

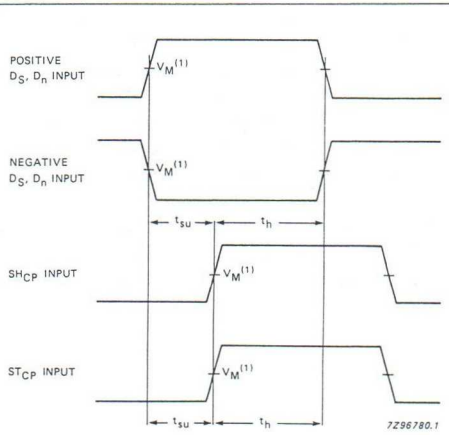


Fig. 11 Waveforms showing hold and set-up times for D_S, D_n inputs to SH_{CP}, ST_{CP} inputs.

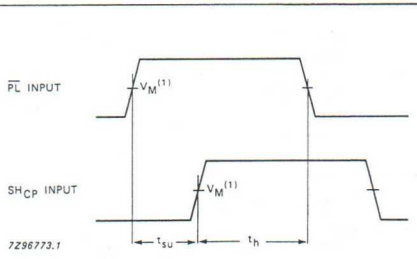


Fig. 12 Waveforms showing set-up times for $\overline{PL}$ input to SH_{CP} input.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS TRANSCEIVER; 3-STATE; INVERTING

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The "640" is similar to the "245" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	9	9	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

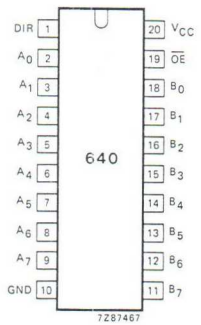


Fig. 1 Pin configuration.

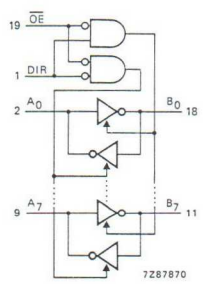


Fig. 2 Logic symbol.

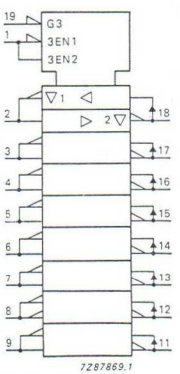


Fig. 3 IEC logic symbol.

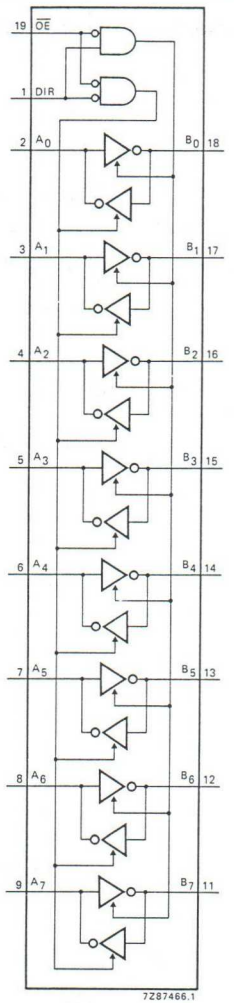


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

FUNCTION TABLE

inputs		inputs/outputs	
$\overline{OE}$	DIR	A_n	B_n
L	L	A=$\overline{B}$	inputs
L	H	inputs	B=$\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	1.50
B_n	1.50
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n		11	22		28		33	ns	4.5	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		18	30		38		45	ns	4.5	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		19	30		38		45	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

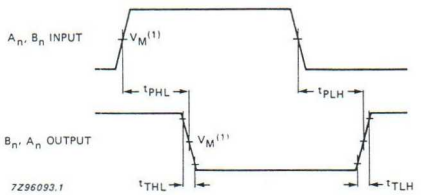


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

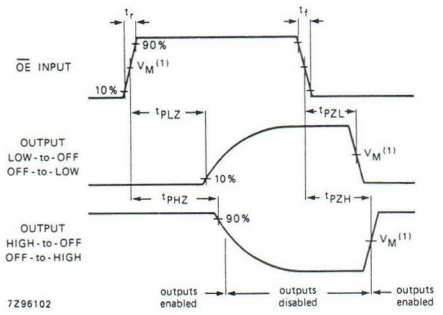


Fig. 6 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS TRANSCEIVER; 3-STATE; TRUE/INVERTING

FEATURES

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; inverting B_n to A_n; true	C_L = 15 pF V_{CC} = 5 V	7 8	8 11	ns ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

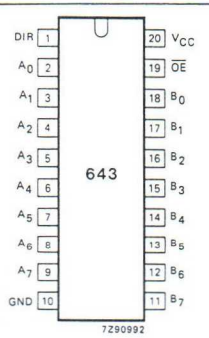


Fig. 1 Pin configuration.

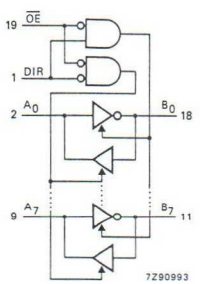


Fig. 2 Logic symbol.

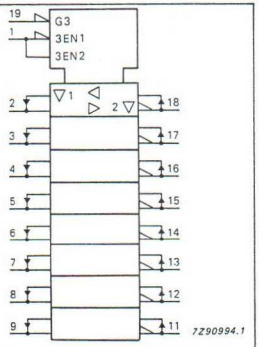


Fig. 3 IEC logic symbol.

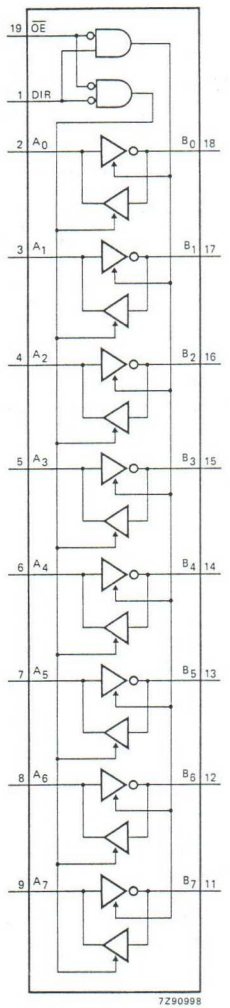


Fig. 4 Functional diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; inverting		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t_{PHL}/ t_{PLH}	propagation delay B_n to A_n; non-inverting (true)		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 5 and 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A_n	1.50
B_n	0.40
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; inverting		10	20		25		30	ns	4.5	Fig. 5
t_{PHL}/t_{PLH}	propagation delay B_n to A_n; non-inverting (true)		13	23		29		35	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		16	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n		17	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 5 and 6

AC WAVEFORMS

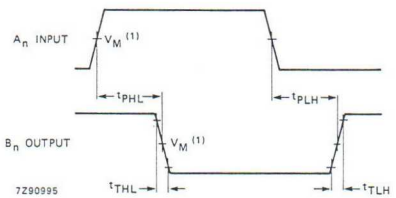


Fig. 5 Waveforms showing the input (A_n) to output (B_n) propagation delays and the output transition times.

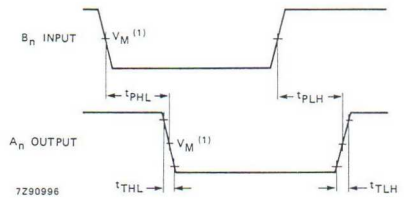


Fig. 6 Waveforms showing the input (B_n) to output (A_n) propagation delays and the output transition times.

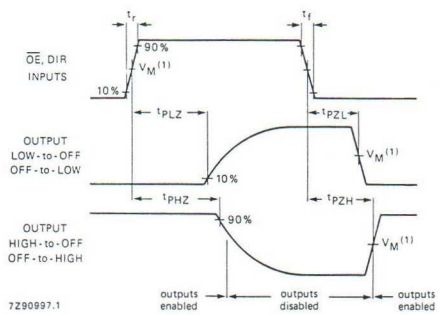


Fig. 7 Waveforms showing the 3-state enable and disable times for $\overline{OE}$ and DIR inputs.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT646 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT646 consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 15 pF; V_{CC} = 5 V	11	13	ns
f_{max}	maximum clock frequency		69	85	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per channel	notes 1 and 2	30	33	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

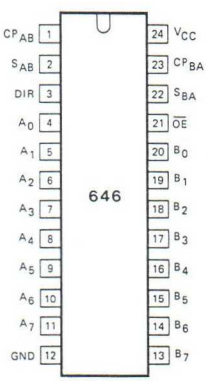


Fig. 1 Pin configuration.

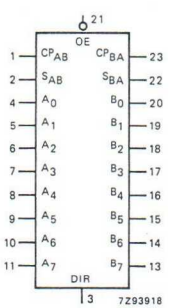


Fig. 2 Logic symbol.

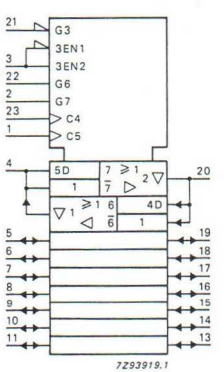


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	A data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	B data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S_{BA}	select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

GENERAL DESCRIPTION

When an output function is disabled, the input function is still enabled and may be used to store and transmit data.
Only one of the two buses, A or B, may be driven at a time.

The "646" is functionally identical to the "648", but has non-inverting data paths.

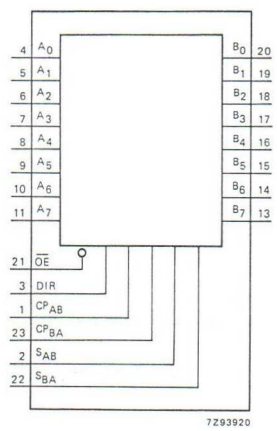


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
H H	X X	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

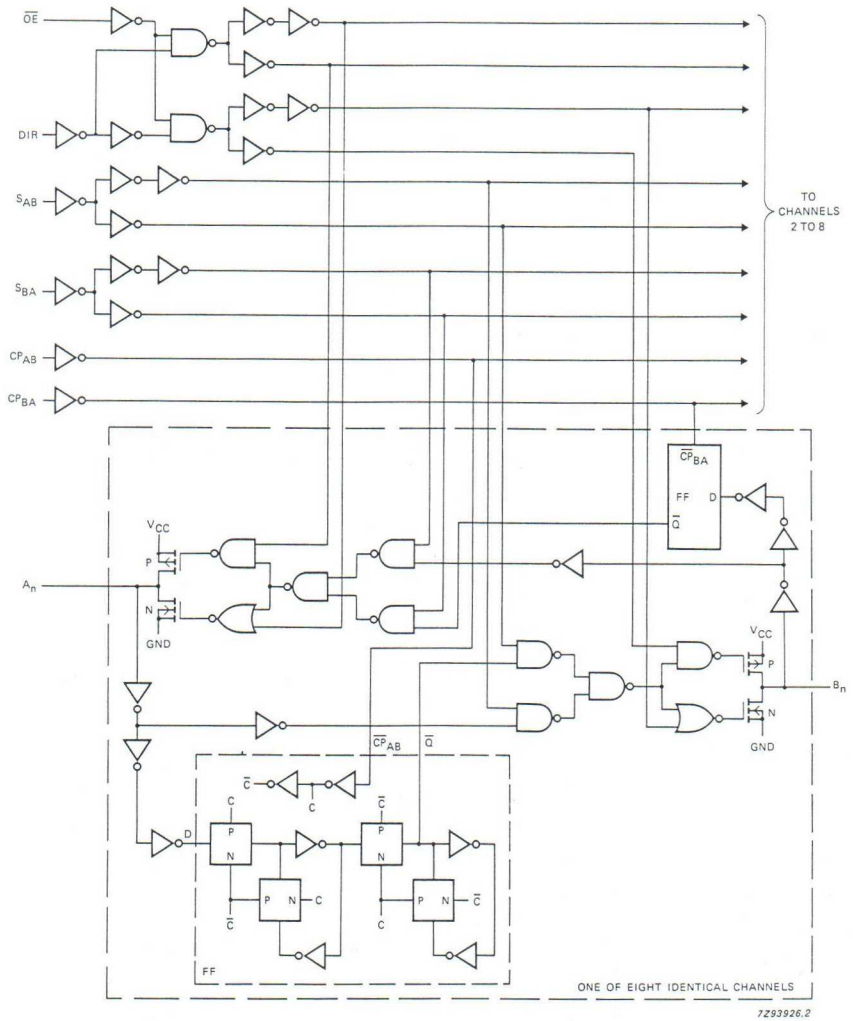


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n,B_n to B_n,A_n		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP_{AB},CP_{BA} to B_n,A_n		66 24 19	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_{AB},S_{BA} to B_n,A_n		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n,B_n		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n,B_n		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n,B_n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n,B_n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	80 16 14	25 9 7		100 24 20		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time A_n,B_n to CP_{AB},CP_{BA}	60 12 10	−3 −1 −1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time A_n,B_n to CP_{AB},CP_{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	21 63 75		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_{AB}, S_{BA} A_0 to A_7 and B_0 to B_7	0.60 0.75

INPUT	UNIT LOAD COEFFICIENT
CP_{AB}, CP_{BA}	1.50
$\overline{OE}$	1.50
DIR	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n,B_n to B_n,A_n		16	30		38		45	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP_{AB},CP_{BA} to B_n,A_n		23	44		55		66	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_{AB},S_{BA} to B_n,A_n		26	46		58		69	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n,B_n		21	40		50		60	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n,B_n		20	35		44		53	ns	4.5	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n,B_n		21	40		50		60	ns	4.5	Fig. 10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n,B_n		21	35		44		53	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	16	8		20		24		ns	4.5	Fig. 7
t_{su}	set-up time A_n,B_n to CP_{AB},CP_{BA}	12	3		15		18		ns	4.5	Fig. 7
t_h	hold time A_n,B_n to CP_{AB},CP_{BA}	5	1		5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	30	77		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

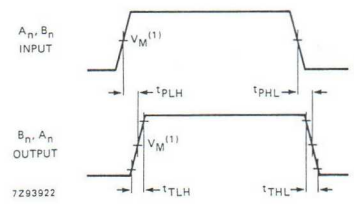


Fig. 6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

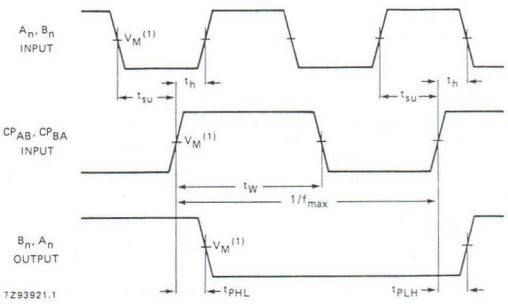


Fig. 7 Waveforms showing the A_n,B_n to CP_{AB},CP_{BA} set-up and hold times, clock CP_{AB},CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB},CP_{BA} to output B_n,A_n propagation delays.

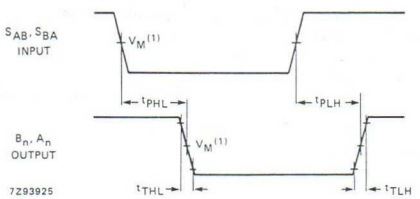


Fig. 8 Waveforms showing the input S_{AB},S_{BA} to output B_n,A_n propagation delays and output transition times.

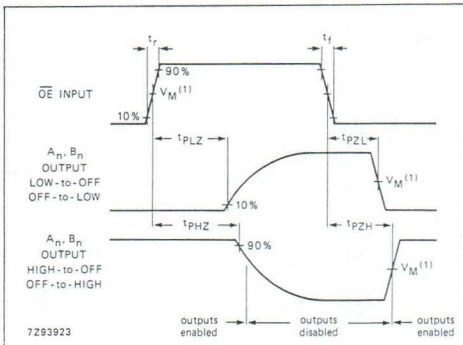


Fig. 9 Waveforms showing the input $\overline{OE}$ to output A_n,B_n 3-state enable and disable times.

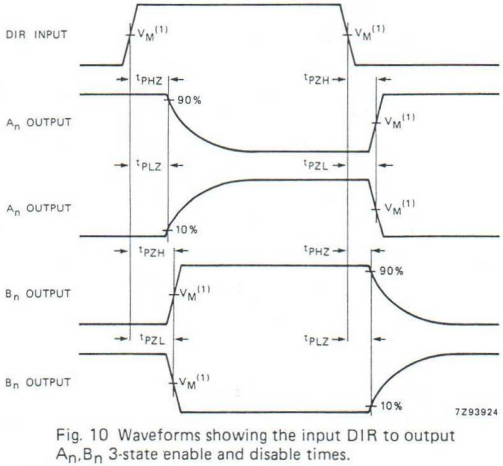


Fig. 10 Waveforms showing the input DIR to output A_n,B_n 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

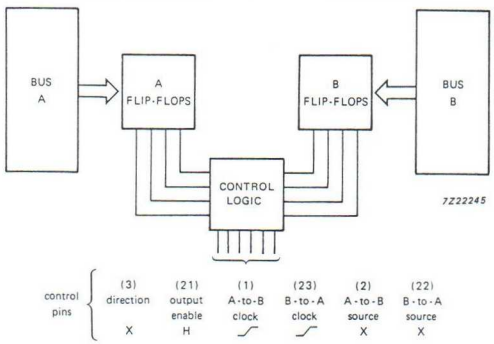


Fig. 11 Data storage from A and/or B bus.

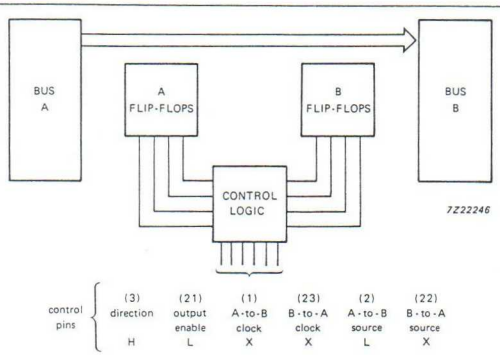


Fig. 12 Real-time transfer from bus A to bus B.

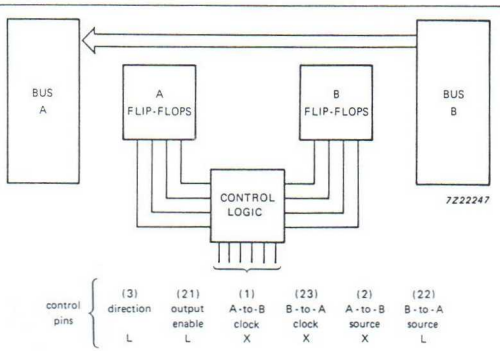


Fig. 13 Real-time transfer from bus B to bus A.

OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE; INVERTING

FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP_{AB} and CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), "$\overline{A}$" data may be stored in the "B" register and/or "$\overline{B}$" data may be stored in the "A" register.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	C_L = 15 pF; V_{CC} = 5 V	11	11	ns
f_{max}	maximum clock frequency		75	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per channel	notes 1 and 2	30	31	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

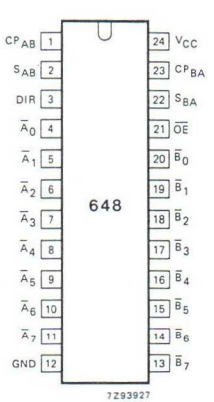


Fig. 1 Pin configuration.

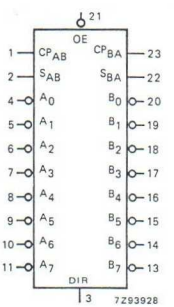


Fig. 2 Logic symbol.

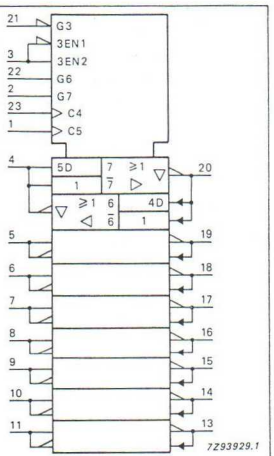


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\overline{A}_0$ to $\overline{A}_7$	$\overline{A}$ data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	$\overline{B}_0$ to $\overline{B}_7$	$\overline{B}$ data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S_{BA}	select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

When an output function is disabled, the input function is still enabled and may be used to store and transmit data.
Only one of the two buses, A or B, may be driven at a time.

The "648" is functionally identical to the "646", but has inverting data paths.

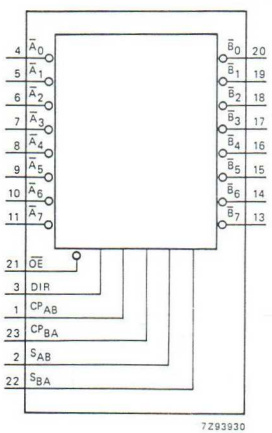


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
H	X	H or L	H or L	X	X	input	input	isolation
H	X	↑	↑	X	X			store $\overline{A}$ and $\overline{B}$ data
L	L	X	X	X	L	output	input	real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			stored $\overline{B}$ data to A bus
L	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

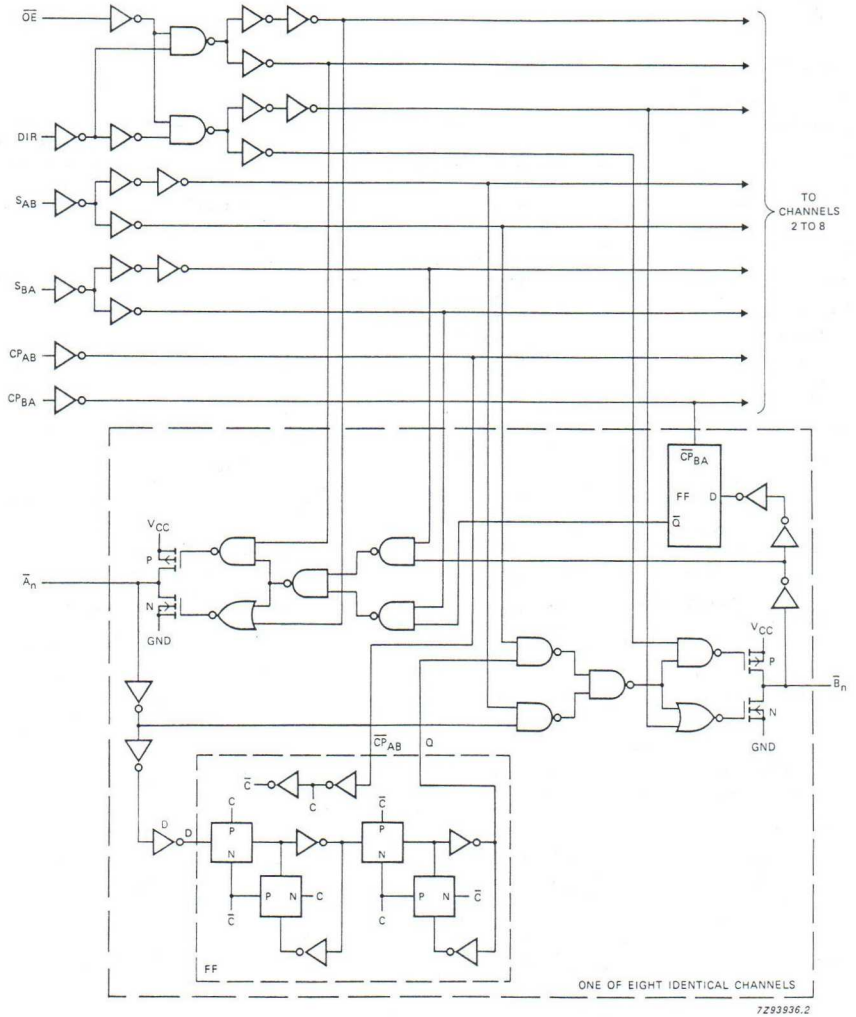


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n,\overline{B}_n$ to $\overline{B}_n,\overline{A}_n$		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP_{AB},CP_{BA} to $\overline{B}_n,\overline{A}_n$		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_{AB},S_{BA} to $\overline{B}_n,\overline{A}_n$		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n,\overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n,\overline{B}_n$		61 22 18	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time DIR to $\overline{A}_n,\overline{B}_n$		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to $\overline{A}_n,\overline{B}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{A}_n,\overline{B}_n$ to CP_{AB},CP_{BA}	60 12 10	0 0 0		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time $\overline{A}_n,\overline{B}_n$ to CP_{AB},CP_{BA}	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{S}_{AB}$, $\overline{S}_{BA}$	0.60
$\overline{A}_0$ to $\overline{A}_7$ and $\overline{B}_0$ to $\overline{B}_7$	0.75

INPUT	UNIT LOAD COEFFICIENT
CP_{AB}, CP_{BA}	1.50
$\overline{OE}$	1.50
DIR	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n,\overline{B}_n$ to $\overline{B}_n,\overline{A}_n$		14	27		34		41	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay CP_{AB},CP_{BA} to $\overline{B}_n,\overline{A}_n$		25	46		58		69	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay S_{AB},S_{BA} to $\overline{B}_n,\overline{A}_n$		20	38		48		57	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n,\overline{B}_n$		21	40		50		60	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n,\overline{B}_n$		20	35		44		53	ns	4.5	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time DIR to $\overline{A}_n,\overline{B}_n$		20	40		50		60	ns	4.5	Fig. 10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to $\overline{A}_n,\overline{B}_n$		21	35		44		53	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	16	7		20		24		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{A}_n,\overline{B}_n$ to CP_{AB},CP_{BA}	12	2		15		18		ns	4.5	Fig. 7
t_h	hold time $\overline{A}_n,\overline{B}_n$ to CP_{AB},CP_{BA}	5	0		5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

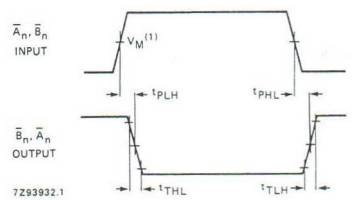


Fig. 6 Waveforms showing the input $\overline{A}_n$,$\overline{B}_n$ to output $\overline{B}_n$,$\overline{A}_n$ propagation delays and the output transition times.

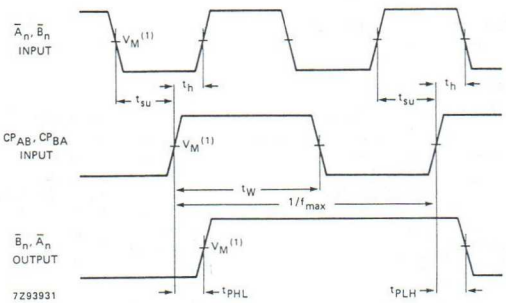


Fig. 7 Waveforms showing the $\overline{A}_n$,$\overline{B}_n$ to CP_{AB},CP_{BA} set-up and hold times, clock CP_{AB},CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB},CP_{BA} to output $\overline{B}_n$,$\overline{A}_n$ propagation delays.

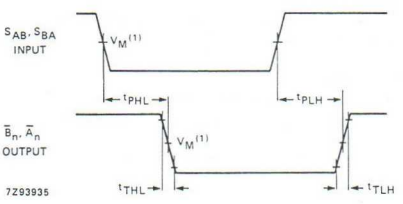


Fig. 8 Waveforms showing the input S_{AB},S_{BA} to output $\overline{B}_n$,$\overline{A}_n$ propagation delays and output transition times.

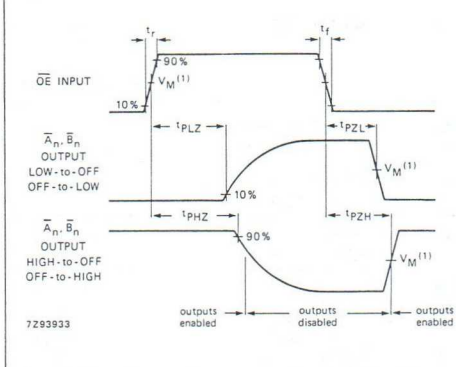


Fig. 9 Waveforms showing the input $\overline{OE}$ to output $\overline{A}_n$,$\overline{B}_n$ 3-state enable and disable times.

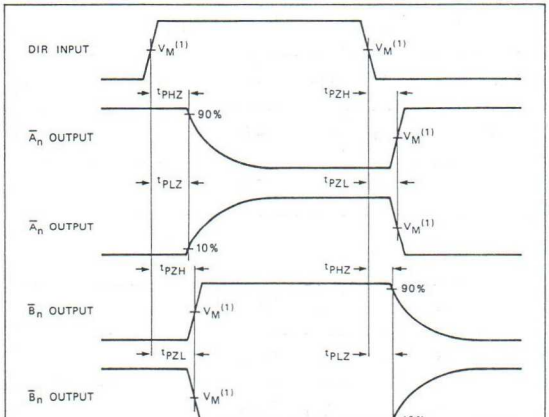


Fig. 10 Waveforms showing the input DIR to output $\overline{A}_n$,$\overline{B}_n$ 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

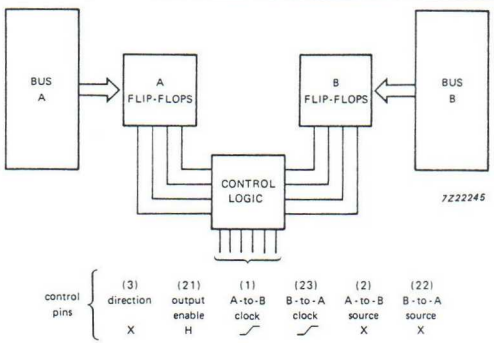


Fig. 11 Data storage from A and/or B bus.

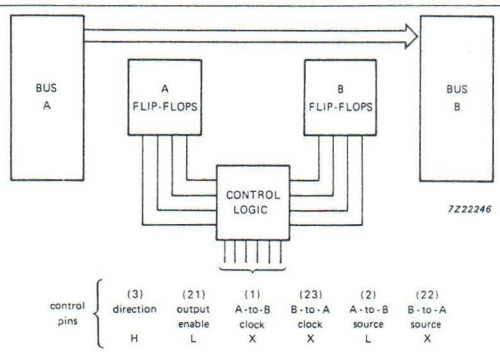


Fig. 12 Real-time transfer from bus A to bus B.

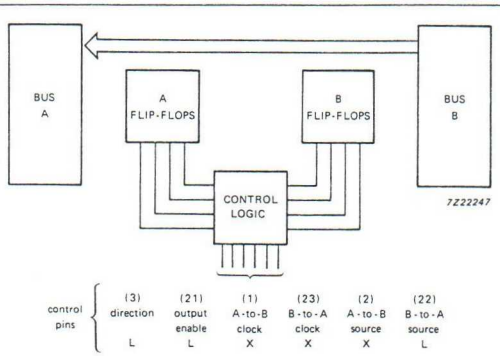


Fig. 13 Real-time transfer from bus B to bus A.

Octal bus transceiver/register; 3-state | 74HC/HCT652

FEATURES

- Multiplexed real-time and stored data
- Independent register for A and B buses
- Independent enables for A and B buses
- 3-state
- Output capability: Bus driver
- Low power consumption by CMOS technology
- I_{CC} category: MSI.

APPLICATIONS

- Bus interfaces.

DESCRIPTION

The 74HC/HCT652 are high-speed SI-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with Jedec standard no. 7A.

The 74HC/HCT652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and central circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock pins (CP_{AB} or CP_{BA}) regardless of the select pins (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control pins. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the output enable pins this operating mode permits. The output enable pins OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns; V_{CC} = 4.5 V; C_L = 50 pF.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PLH}/t_{PHL}	propagation delay A_n/B_n to B_n/A_n	C_L = 15 pF V_{CC} = 5 V	13	13	ns
	propagation delay CP_{AB}/CP_{BA} to B_n/A_n		18	20	ns
	propagation delay S_{AB}/S_{BA} to B_n/A_n		20	23	ns
t_{PZH}/t_{PZL}	3-state output enable time $OE_{AB}/\overline{OE}_{BA}$ to B_n/A_n		14	15	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $OE_{AB}/\overline{OE}_{BA}$ to B_n/A_n		12	13	ns
f_{max}	maximum clock frequency		92	92	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per channel	notes 1 and 2	26	28	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT652N	24	DIL	plastic	SOT101L
74HC/HCT652D	24	SO	plastic	SOT137A

D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high-impedance, each set of the bus lines will remain at its last state. This type differs from the HC/HCT646 in one extra bus-management function. This is the possibility to transfer stored "A" data to the "B" bus and transfer stored "B" data to the "A" bus at the same time. The examples at the application information demonstrate all bus management functions. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

PINNING

SYMBOL	PIN	DESCRIPTION
CP_{AB}	1	A to B clock input
S_{AB}	2	select A to B source input
OE_{AB}	3	output enable A to B input
$A_0..A_7$	4..11	A data inputs/outputs
GND	12	ground (0 V)
$B_7..B_0$	13..20	B data inputs/outputs
$\overline{OE}_{BA}$	21	output enable B to A input
S_{BA}	22	select B to A source input
CP_{BA}	23	B to A clock input
V_{CC}	24	positive supply voltage

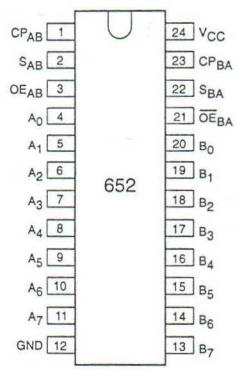


Fig.1 Pin configuration.

Fig.2 Logic symbol.

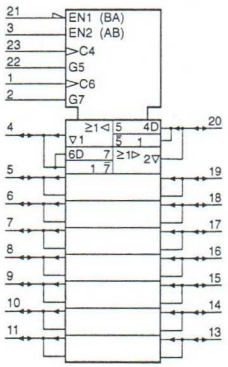


Fig.3 IEC Logic symbol.

FUNCTION TABLE

INPUTS						DATA I/O *		OPERATION OR FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_1 THRU A_8	B_1 THRU B_8	HC/HCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will de stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

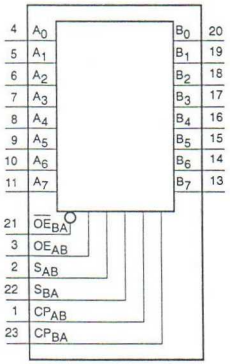


Fig.4 Functional diagram.

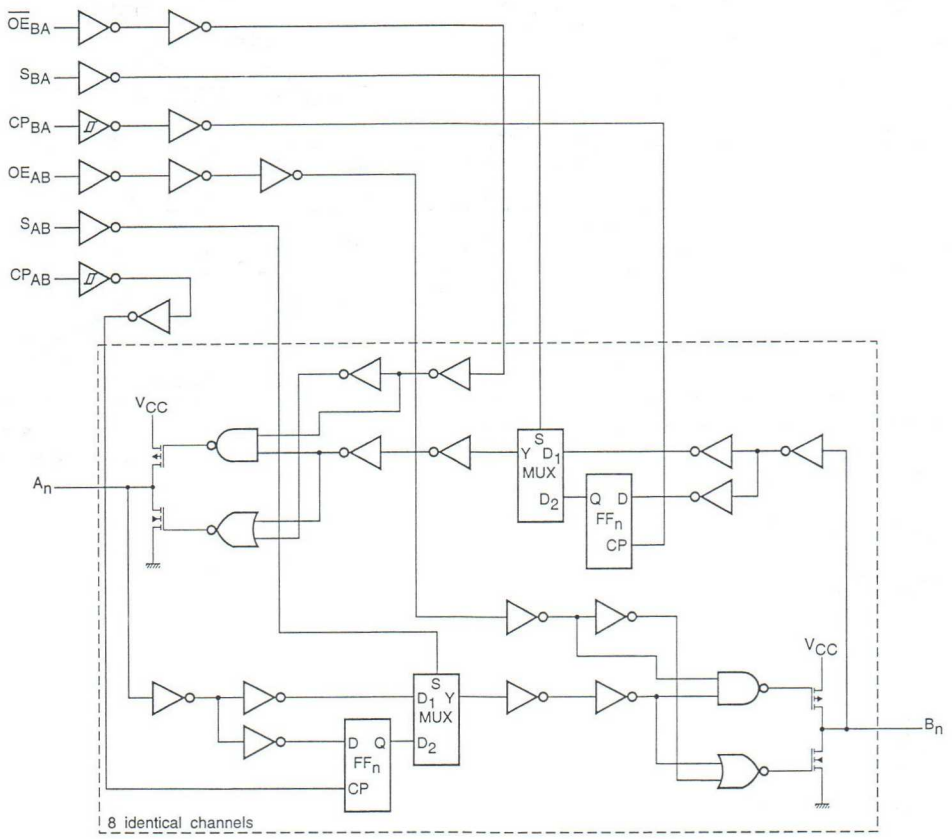


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	44	135	–	170	–	205	ns	2.0	Fig.6
		–	16	27	–	34	–	41		4.5	
		–	13	23	–	29	–	35		6.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	61	190	–	240	–	285	ns	2.0	Fig.7
		–	22	38	–	48	–	57		4.5	
		–	18	32	–	41	–	48		6.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	63	195	–	245	–	295	ns	2.0	Fig.8
		–	23	39	–	49	–	59		4.5	
		–	18	33	–	42	–	50		6.0	
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	47	150	–	190	–	225	ns	2.0	Fig.9
		–	17	30	–	38	–	45		4.5	
		–	14	26	–	33	–	38		6.0	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	41	150	–	190	–	225	ns	2.0	Fig.9
		–	15	30	–	38	–	45		4.5	
		–	12	26	–	33	–	38		6.0	
t_{THL}/t_{TLH}	output transition time	–	14	60	–	75	–	90	ns	2.0	Figs 6, 8
		–	5	12	–	15	–	18		4.5	
		–	4	10	–	13	–	15		6.0	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	80	17	–	100	–	120	–	ns	2.0	Fig.7
		16	6	–	20	–	24	–		4.5	
		14	5	–	17	–	20	–		6.0	
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	100	17	–	125	–	150	–	ns	2.0	Fig.7
		20	6	–	25	–	30	–		4.5	
		17	5	–	21	–	26	–		6.0	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	25	−8	–	30	–	35	–	ns	2.0	Fig.7
		5	−3	–	6	–	7	–		4.5	
		4	−2	–	5	–	6	–		6.0	
f_{max}	maximum clock pulse frequency	6.0	16	–	4.8	–	4.0	–	MHz	2.0	Fig.7
		30	83	–	24	–	20	–		4.5	
		35	98	–	28	–	24	–		6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI.

Note to the HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_{AB}, S_{BA}	0.75
A_0 to A_7 and B_0 to B_7	0.75
CP_{AB}, CP_{BA}	1.50
OE_{AB}	1.50
$\overline{OE}_{BA}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	16	27	–	34	–	41	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	23	39	–	49	–	59	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	27	46	–	55	–	66	ns	4.5	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	18	33	–	41	–	50	ns	4.5	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	16	35	–	44	–	53	ns	4.5	Fig.9
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.6, 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	16	6	–	20	–	24	–	ns	4.5	Fig.7
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	10	5	–	13	–	15	–	ns	4.5	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	5	−2	–	6	–	8	–	ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	83	–	24	–	20	–	MHz	4.5	Fig.7

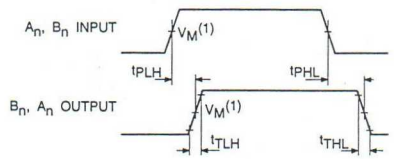


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delay times and the output transition times.

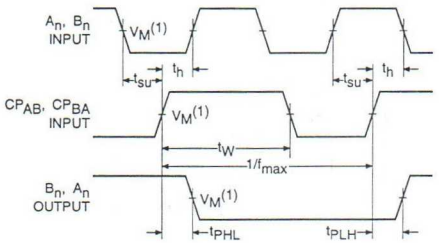


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

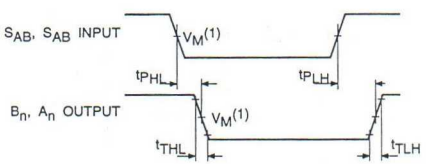


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and the output transition times.

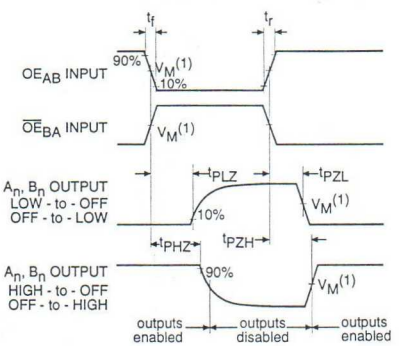
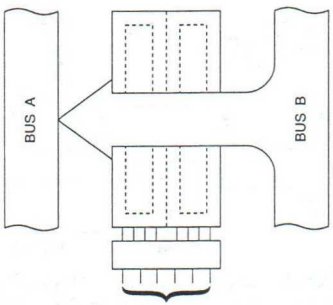


Fig.9 Waveforms showing the output enable inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

Note to the AC waveforms

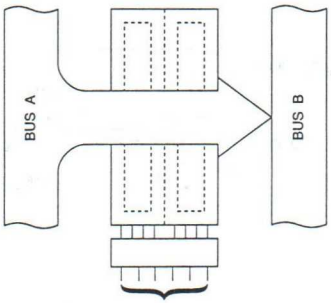
(1) HC: $V_M = 50\%$; V_I = GND to V_{CC}.
HCT: $V_M = 1.3$ V; V_I = GND to 3 V.

APPLICATION INFORMATION



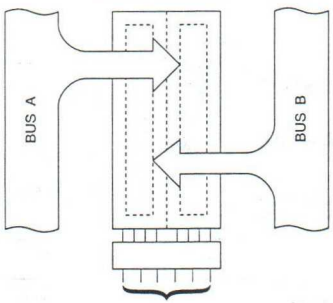
(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
L	L	X	X	X	L

Real-time transfer bus B to bus A



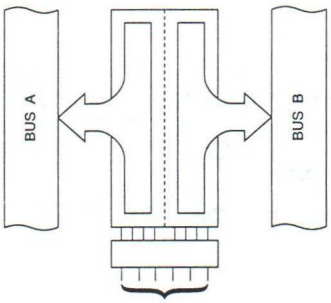
(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	X	X	L	X

Real-time transfer bus A to bus B



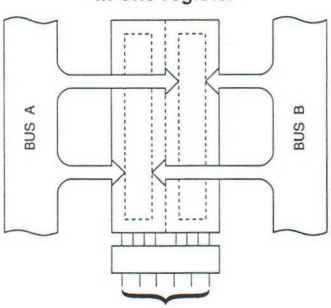
(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Store A, B or A and B in one register



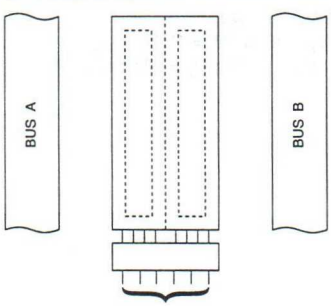
(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Transfer A stored data to B bus or B stored data to A bus or both at the same time



(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Store bus A in both registers or store bus B in both registers



(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
L	H	H or L	H or L	X	X

Isolation

4 x 4 REGISTER FILE; 3-STATE

FEATURES

- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R_A, R_B and W_A, W_B) and enable inputs ($\overline{RE}$ and $\overline{WE}$) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D_0 to D_3). The W_A and W_B inputs determine the location of the stored word. When the $\overline{WE}$ input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ input is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs (Q_0 to Q_3). D_n and W_n inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R_A and R_B). The addressed word appears at the four outputs when the $\overline{RE}$ is LOW. Data outputs are in the high impedance OFF-state when $\overline{RE}$ is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	23	23	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	122	124	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4	R_A, R_B	read address inputs
8	GND	ground (0 V)
10, 9, 7, 6	Q_0 to Q_3	data outputs
11	$\overline{RE}$	3-state output read enable input (active LOW)
12	$\overline{WE}$	write enable input (active LOW)
14, 13	W_A, W_B	write address inputs
15, 1, 2, 3	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

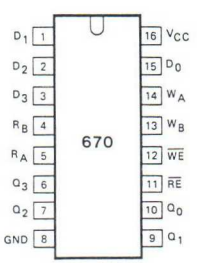


Fig. 1 Pin configuration.

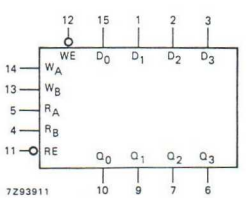


Fig. 2 Logic symbol.

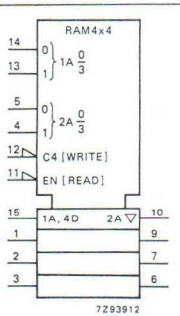


Fig. 3 IEC logic symbol.

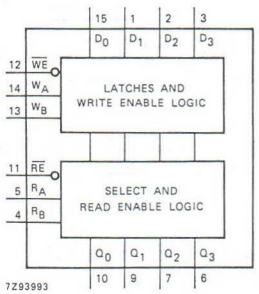


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd)

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES*
	$\overline{WE}$	D_n	
write data	L	L	L
	L	H	H
data latched	H	X	no change

* The write address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES**	Q_n
read	L	L	L
	L	H	H
disabled	H	X	Z

** The selection of the "internal latches" by read address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

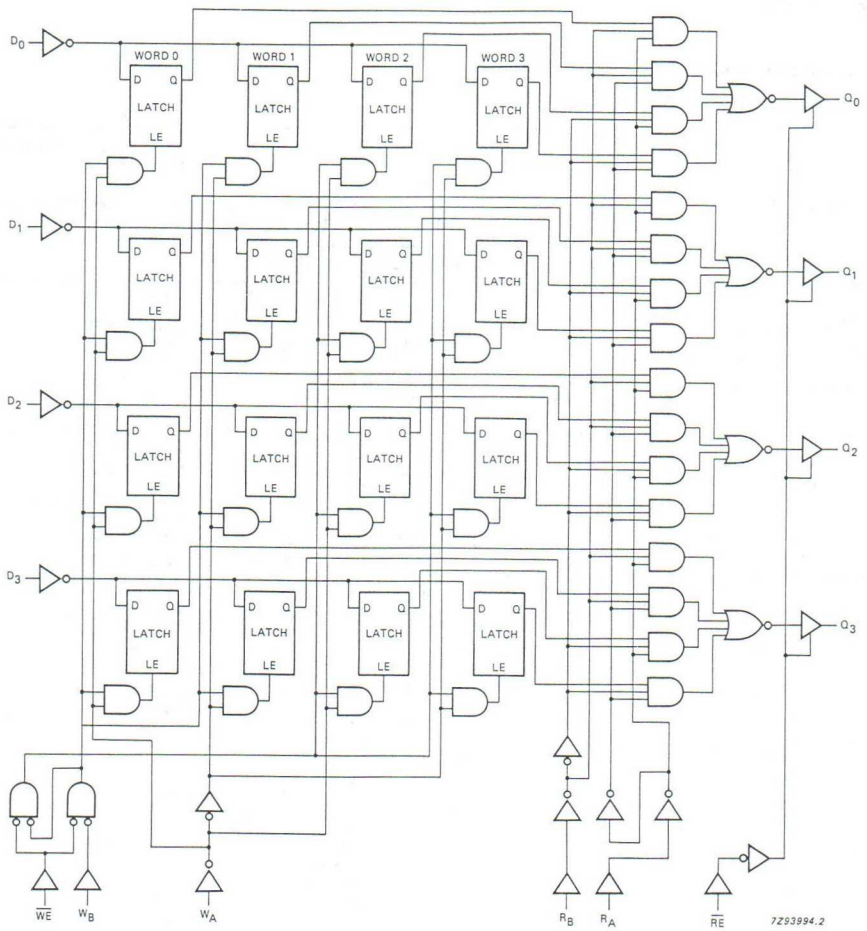


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay R_A, R_B to Q_n		58 21 17	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{WE}$ to Q_n		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		74 27 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{RE}$ to Q_n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{RE}$ to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	write enable pulse width LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to $\overline{WE}$	60 12 10	3 1 1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time W_A, W_B to $\overline{WE}$	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time W_A, W_B to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{latch}	latch time $\overline{WE}$ to R_A, R_B	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
$\overline{WE}$, W_A	0.40
W_B	0.60

INPUT	UNIT LOAD COEFFICIENT
R_A	0.70
R_B	1.10
$\overline{RE}$	1.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay R_A, R_B to Q_n		21	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{WE}$ to Q_n		28	50		63		75	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		27	50		63		75	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{RE}$ to Q_n		18	35		44		53	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{RE}$ to Q_n		19	35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	write enable pulse width LOW	18	9		23		27		ns	4.5	Fig. 8
t_{su}	set-up time D_n to $\overline{WE}$	12	4		15		18		ns	4.5	Fig. 8
t_{su}	set-up time W_A, W_B to $\overline{WE}$	12	−2		15		18		ns	4.5	Fig. 8
t_h	hold time D_n to $\overline{WE}$	5	−1		5		5		ns	4.5	Fig. 8
t_h	hold time W_A, W_B to $\overline{WE}$	5	0		5		5		ns	4.5	Fig. 8
t_{latch}	latch time $\overline{WE}$ to R_A, R_B	25	11		31		38		ns	4.5	Fig. 8

AC WAVEFORMS

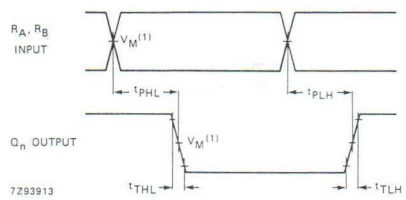


Fig. 6 Waveforms showing the read address input (R_A, R_B) to output (Q_n) propagation delays and output transition times.

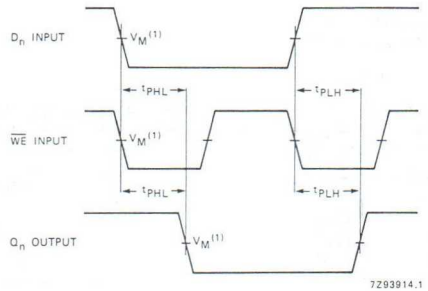
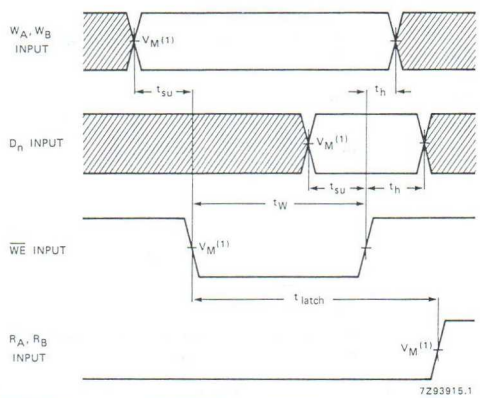


Fig. 7 Waveforms showing the write enable input ($\overline{WE}$) and data input (D_n) to output (Q_n) propagation delays, and the write enable pulse width.



Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

The time allowed for the internal output of the latch to assume the state of the new data (t_{latch}) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B, $\overline{RE}$ must be LOW.

Fig. 8 Waveforms showing the write address input (W_A, W_B) and data input (D_n) to write enable ($\overline{WE}$) set-up, hold and latch times.

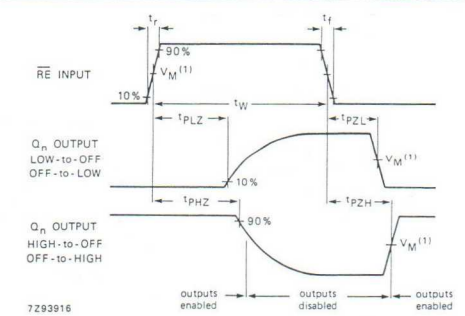


Fig. 9 Waveforms showing the read enable ($\overline{RE}$) to output (Q_n) enable and disable times, and the read enable pulse width.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT MAGNITUDE COMPARATOR

FEATURES

- Compare two 8-bit words
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words.
The output provides $\overline{P = Q}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\overline{P = Q}$ E to $\overline{P = Q}$	C_L = 15 pF V_{CC} = 5 V	17 8	17 12	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P_0 to P_7	word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q_0 to Q_7	word inputs
10	GND	ground (0 V)
19	$\overline{P = Q}$	equal to output
20	V_{CC}	positive supply voltage

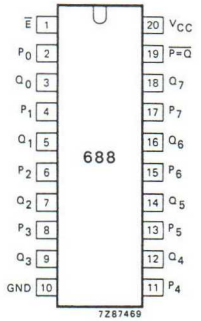


Fig. 1 Pin configuration.

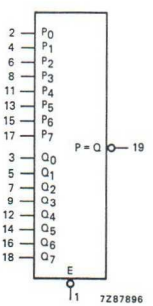


Fig. 2 Logic symbol.

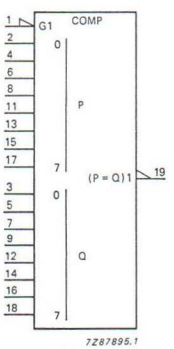


Fig. 3 IEC logic symbol.

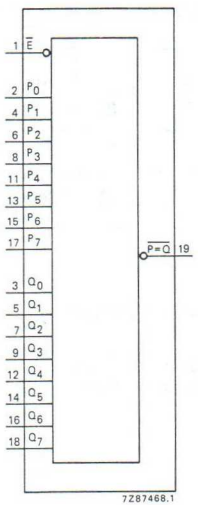


Fig. 4 Functional diagram.

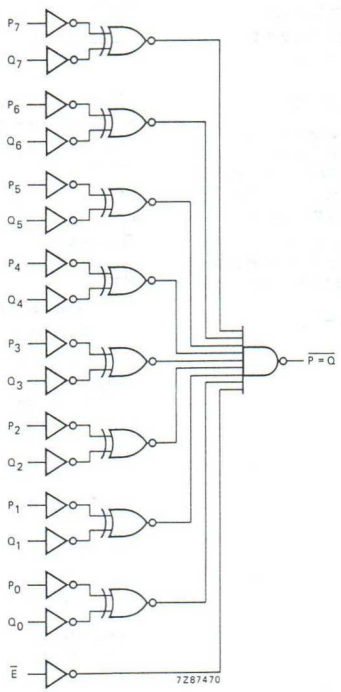


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P_n, Q_n	ENABLE $\bar{E}$	$\overline{P = Q}$
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay P_n, Q_n to $\overline{P = Q}$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to $\overline{P = Q}$		28 10 8	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
P_n	0.35
Q_n	0.35
$\overline{E}$	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay P_n, Q_n to $\overline{P} = \overline{Q}$		20	34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{P} = \overline{Q}$		18	24		30		36	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

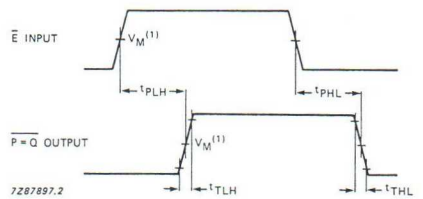


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to the equal to output ($\overline{P = Q}$) propagation delays and the output transition times.

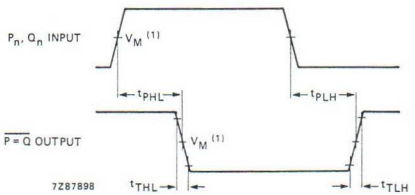


Fig. 7 Waveforms showing the word inputs (P_n, Q_n) to the equal to output ($\overline{P = Q}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits. An example is shown in Fig. 8.

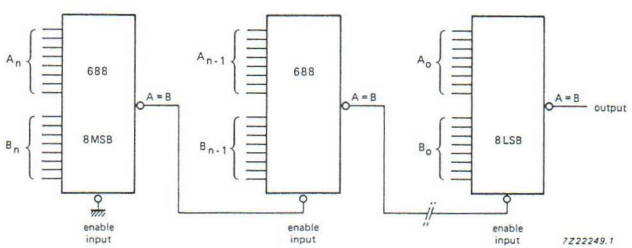


Fig. 8 Binary or BCD comparator.

DUAL 4-INPUT NOR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4002 are high-speed Si-gate CMOS devices and are pin compatible with "4002" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4002 provide the 4-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1Y, 2Y	data outputs
2, 9	1A, 2A	data inputs
3, 10	1B, 2B	data inputs
4, 11	1C, 2C	data inputs
5, 12	1D, 2D	data inputs
6, 8	n.c.	not connected
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

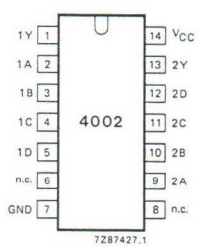


Fig. 1 Pin configuration.

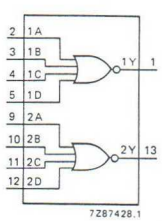


Fig. 2 Logic symbol.

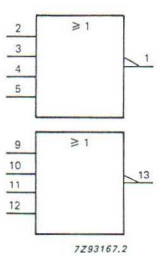


Fig. 3 IEC logic symbol.

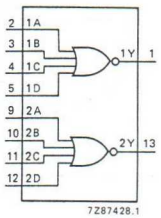


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

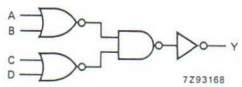


Fig. 5 Logic diagram 74HC4002 (one gate).

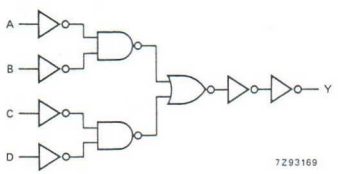


Fig. 6 Logic diagram 74HCT4002 (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY		13	22		28		33	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

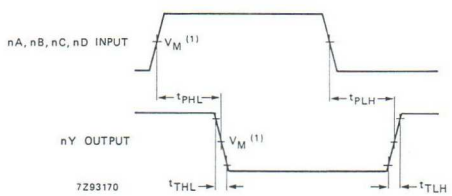


Fig. 7 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The74HC/HCT4015 are dual edge-triggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs ($1Q_0$ to $1Q_3$ and $2Q_0$ to $2Q_3$) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces nQ_0 to nQ_3 to LOW, independent of nCP and nD.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ_n	C_L = 15 pF; V_{CC} = 5 V	16	18	ns
f_{max}	maximum clock frequency		110	74	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per register	notes 1 and 2	35	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4, 3, 10	$1Q_0$ to $1Q_3$	flip-flop outputs
6, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
7, 15	1D, 2D	serial data inputs
8	GND	ground (0 V)
9, 1	1CP, 2CP	clock inputs (LOW-to-HIGH, edge-triggered)
13, 12, 11, 2	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

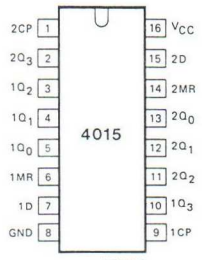


Fig. 1 Pin configuration.

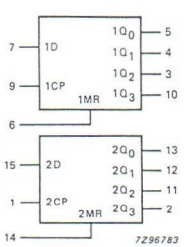


Fig. 2 Logic symbol.

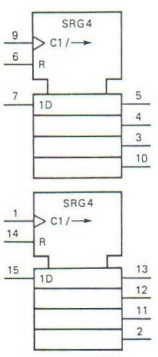


Fig. 3 IEC logic symbol.

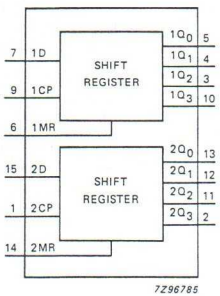


Fig. 4 Functional diagram.

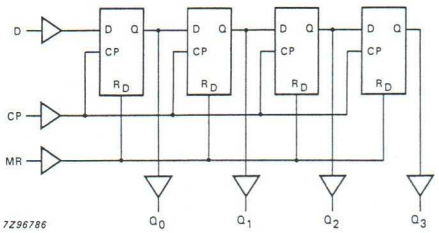


Fig. 5 Logic diagram (one 4-bit serial-in/parallel-out shift register).

FUNCTION TABLE

INPUTS				OUTPUTS			
n	nCP	nD	nMR	nQ_0	nQ_1	nQ_2	nQ_3
1	↑	D_1	L	D_1	X	X	X
2	↑	D_2	L	D_2	D_1	X	X
3	↑	D_3	L	D_3	D_2	D_1	X
4	↑	D_4	L	D_4	D_3	D_2	D_1
	↓	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition
n = number of clock pulse transitions
D_n = either HIGH or LOW

APPLICATIONS

- Serial-to-parallel converter
- Buffer stores
- General purpose register

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ_n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay nMR to nQ_n		44 16 13	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time nMR to nCP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nD to nCP	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time nD to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	33 100 119		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.30
nMR	1.50
nCP	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ_n		21	35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay nMR to nQ_n		18	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7
t_{rem}	removal time nMR to nCP	20	10		25		30		ns	4.5	Fig. 7
t_{su}	set-up time nD to nCP	12	4		15		18		ns	4.5	Fig. 8
t_h	hold time nD to nCP	5	−2		5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	67		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

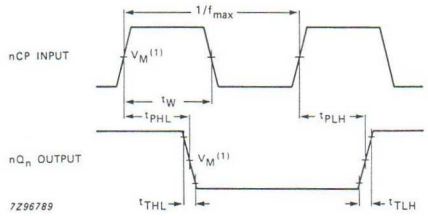


Fig. 6 Waveforms showing the clock (nCP) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

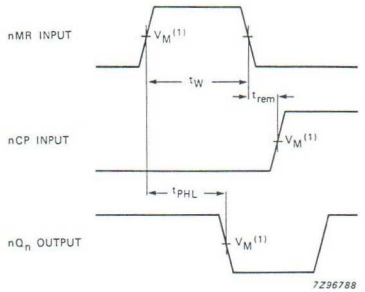


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delay and the master reset to clock (nCP) removal time.

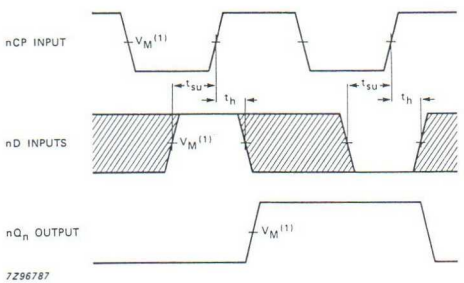


Fig. 8 Waveforms showing the data set-up and hold times for nD inputs.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance:
  160 Ω (typ.) at V_{CC} = 4.5 V
  120 Ω (typ.) at V_{CC} = 6.0 V
  80 Ω (typ.) at V_{CC} = 9.0 V
- Individual switch controls
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the "4016" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4016 have four independent analog switches (transmission gates).
Each switch has two input/output terminals (Y_n, Z_n) and an active HIGH enable input (E_n). When E_n is connected to V_{CC}, a low bidirectional path between Y_n and Z_n is established (ON condition). When E_n is connected to ground (GND), the switch is disabled and a high impedance between Y_n and Z_n is established (OFF condition).

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \geqslant (V_Y, V_Z) \geqslant$ GND.
Inputs Y_n and Z_n are electrically equivalent terminals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time E_n to V_{OS}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 5 V	16	17	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time E_n to V_{OS}		14	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	12	12	pF
C_S	max. switch capacitance		5	5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	Y_0 to Y_3	independent inputs/outputs
7	GND	ground (0 V)
2, 3, 9, 10	Z_0 to Z_3	independent inputs/outputs
13, 5, 6, 12	E_0 to E_3	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

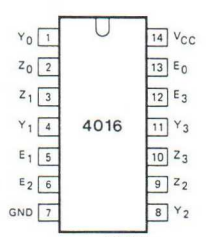


Fig. 1 Pin configuration.

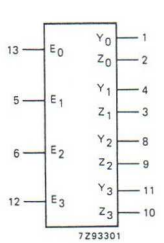


Fig. 2 Logic symbol.

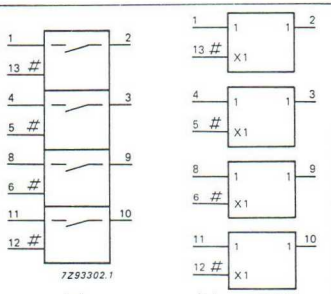


Fig. 3 IEC logic symbol.

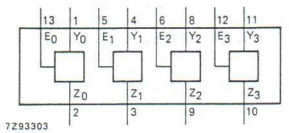


Fig. 4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

FUNCTION TABLE

INPUT E_n	CHANNEL IMPEDANCE
L	high
H	low

H = HIGH voltage level
L = LOW voltage level

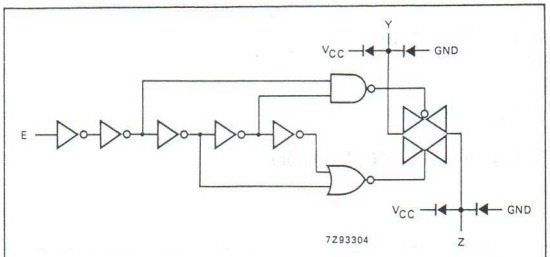


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT											
		+25			–40 to +85		–40 to +125			V_{CC} V	I_S μA	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.					
R_{ON}	ON resistance (peak)		– 160 120 85	– 320 240 170		– 400 300 213		– 480 360 255	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC} to GND	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		160 80 70 60	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		170 90 80 65	– 180 160 135		– 225 200 170		– 270 240 205	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 16 12 9						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V_{CC} to GND	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 6.

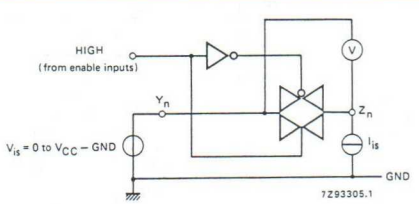


Fig. 6 Test circuit for measuring R_{ON}.

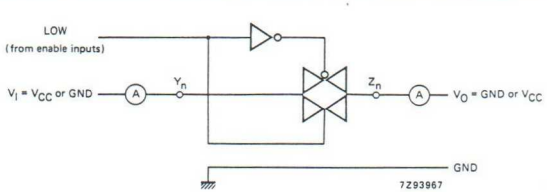


Fig. 7 Test circuit for measuring OFF-state current.

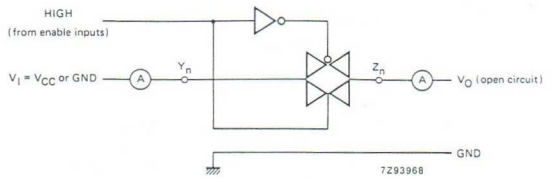


Fig. 8 Test circuit for measuring ON-state current.

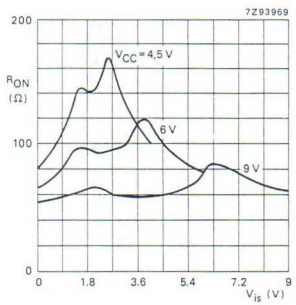


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC}.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig. 7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig. 8)
I_{CC}	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μA	6.0 10.0	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+ 25			−40 to + 85		−40 to + 125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R_L = ∞; C_L = 50 pF (see Fig. 16)
t_{PZH}/ t_{PZL}	turn "ON" time E_n to V_{os}		52 19 15 11	190 38 32 28		240 48 41 35		235 57 48 42	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time E_n to V_{os}		47 17 14 13	145 29 25 22		180 36 31 28		220 44 38 33	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} – GND (see Fig. 7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} – GND (see Fig. 8)
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	4.5 to 5.5	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} -2.1 V	other inputs at V_{CC} or GND

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E_n	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		6	12		15		18	ns	4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 16)
t_{PZH}	turn "ON" time E_n to V_{os}		19	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PZL}	turn "ON" time E_n to V_{os}		20	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PHZ}/t_{PLZ}	turn "OFF" time E_n to V_{os}		23	35		44		53	ns	4.5	R_L= 1 kΩ; C_L = 50 pF (see Figs 17 and 18)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f =1 kHz	0.80 0.40	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	–50 –50	dB dB	4.5 9.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Figs 10 and 15)
	crosstalk between any two switches	–60 –60	dB dB	4.5 9.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (E_n, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 13)
f_{max}	minimum frequency response (–3dB)	150 160	MHz MHz	4.5 9.0	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 11 and 14)
C_S	maximum switch capacitance	5	pF			

Notes to AC characteristics

General note

V_{is} is the input voltage at a Y_n or Z_n terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Y_n or Z_n terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

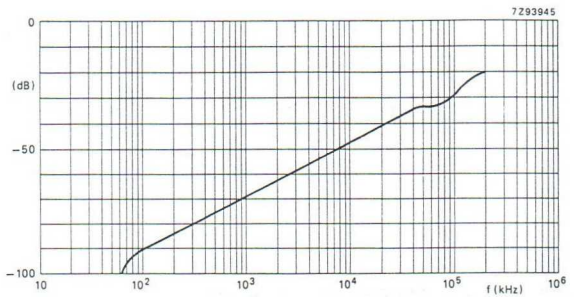
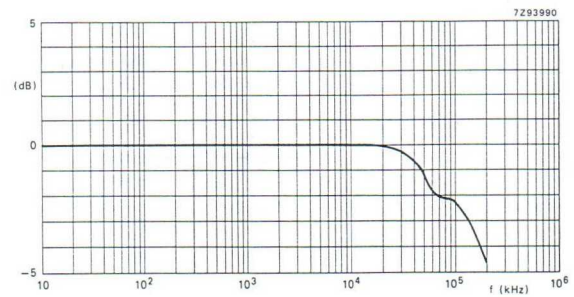


Fig. 10 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 10 and 11

Test conditions:
V_{CC} = 4.5 V; GND = 0 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 11 Typical frequency response.

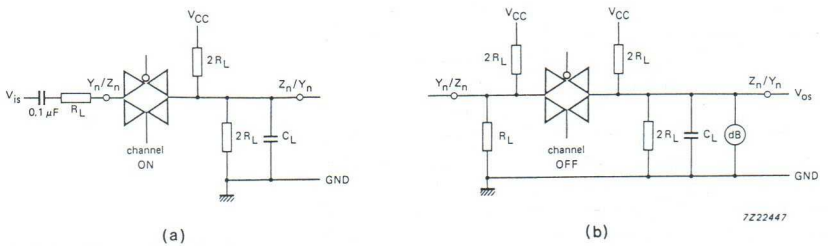


Fig. 12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

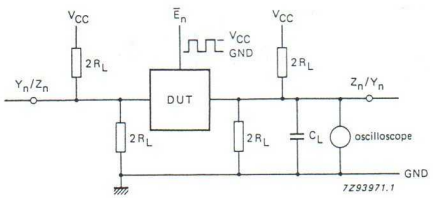
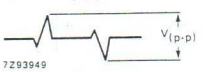


Fig. 13 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 13

The crosstalk is defined as follows (oscilloscope output):



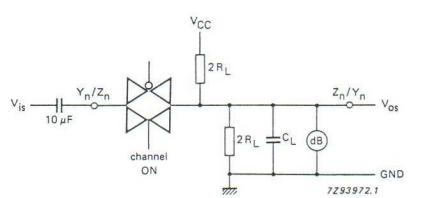


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

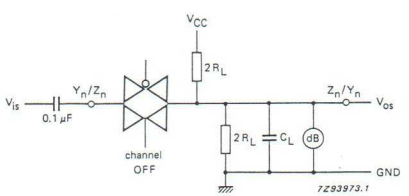


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

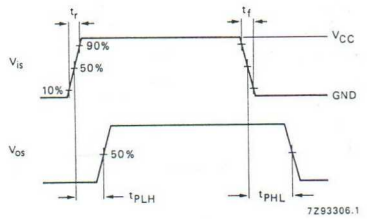


Fig. 16 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

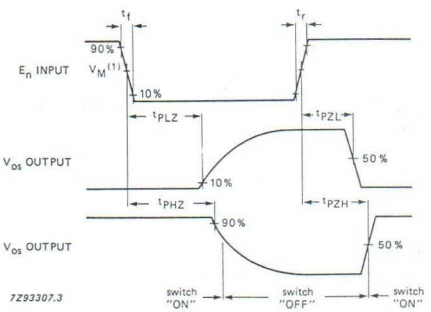
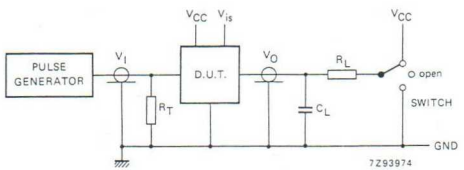


Fig. 17 Waveforms showing the turn-ON and turn-OFF times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V_{is}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

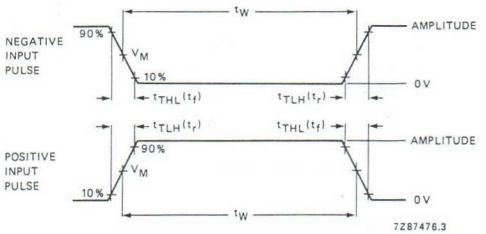


Fig. 19 Input pulse definitions.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q_0 to Q_9), an active LOW output from the most significant flip-flop ($\overline{Q}_{5\text{-}9}$), active HIGH and active LOW clock inputs (CP_0 and $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{Q}_{5\text{-}9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($Q_0 = \overline{Q}_{5\text{-}9}$ = HIGH; Q_1 to Q_9 = LOW) independent of the clock inputs (CP_0 and $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_0, $\overline{CP}_1$ to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	21	ns
f_{max}	maximum clock frequency		77	67	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	35	36	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q_0 to Q_9	decoded outputs
8	GND	ground (0 V)
12	$\overline{Q}_{5\text{-}9}$	carry output (active LOW)
13	$\overline{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP_0	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

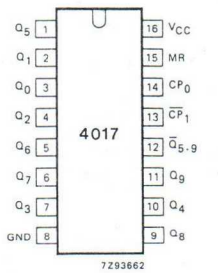


Fig. 1 Pin configuration.

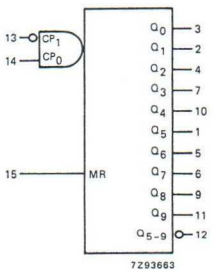


Fig. 2 Logic symbol.

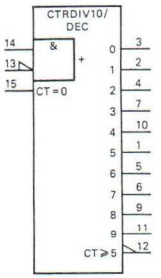


Fig. 3 IEC logic symbol.

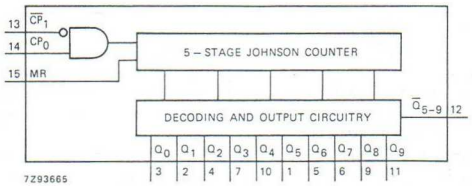


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	OPERATION
H	X	X	$Q_0 = Q_{5-9} = H$; Q_1 to $Q_9 = L$
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

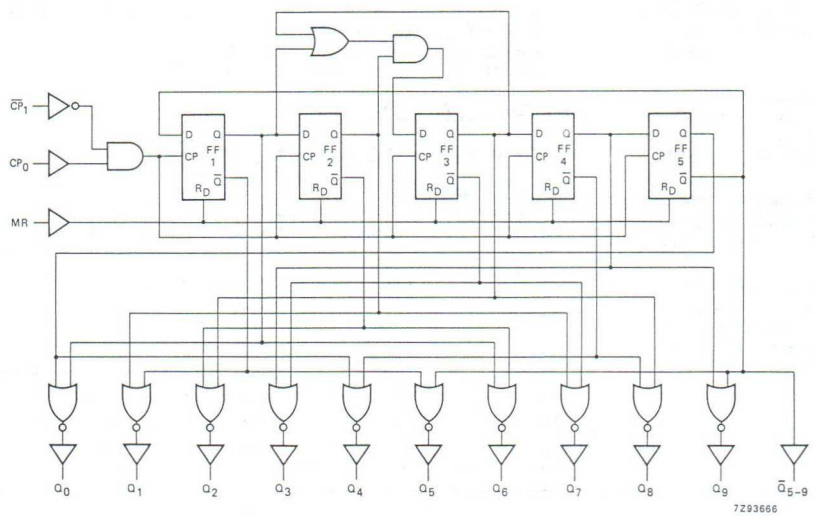


Fig. 5 Logic diagram.

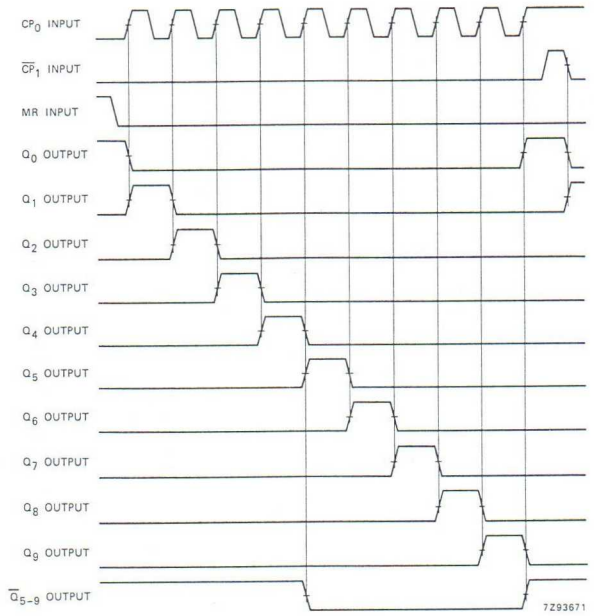


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_0 to Q_n		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5\text{-}9}$		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5\text{-}9}$		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay MR to Q_{1-9}		52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay MR to $\overline{Q}_{5\text{-}9}$, Q_0		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5 5 5	−17 −6 −5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	50 10 9	−8 −3 −2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time CP_0 to $\overline{CP}_1$; $\overline{CP}_1$ to CP_0	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_1$	0.40
CP_0	0.25
MR	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_0 to Q_n		25	46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5\text{-}9}$		25	46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n		25	50		63		75	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5\text{-}9}$		25	50		63		75	ns	4.5	Fig. 9
t_{PHL}	propagation delay MR to Q_{1-9}		22	46		58		69	ns	4.5	Fig. 8
t_{PLH}	propagation delay MR to $\overline{Q}_{5\text{-}9}$, Q_0		20	46		58		69	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
t_W	master reset pulse width; HIGH	16	4		20		24		ns	4.5	Fig. 8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5	−5		5		5		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	10	−3		13		15		ns	4.5	Fig. 7
t_h	hold time CP_0 to $\overline{CP}_1$; $\overline{CP}_1$ to CP_0	10	6		13		15		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	30	61		24		20		MHz	4.5	Fig. 8

AC WAVEFORMS

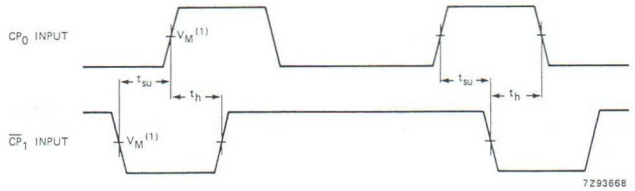


Fig. 7 Waveforms showing hold and set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.

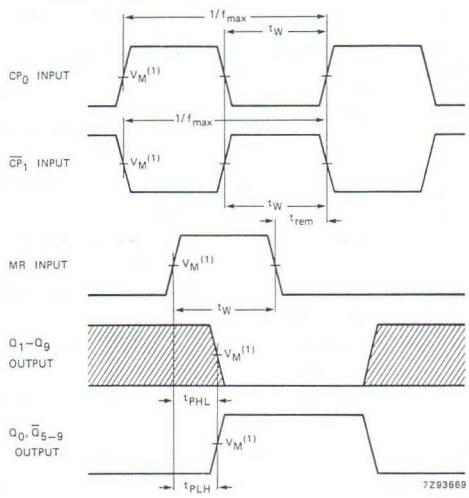


Fig. 8 Waveforms showing the minimum pulse widths for CP_0, $\overline{CP}_1$ and MR inputs; the recovery time for MR and the propagation delays for MR to Q_n and $\overline{Q}_{5\text{-}9}$ outputs.

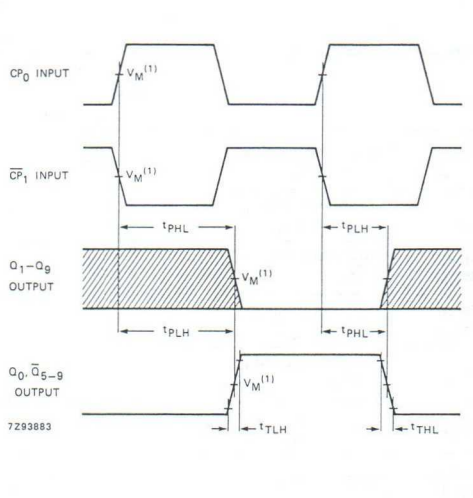


Fig. 9 Waveforms showing the propagation delays for CP_0, $\overline{CP}_1$ to Q_n, $\overline{Q}_{5\text{-}9}$ outputs and the output transition times.

Note to Figs 8 and 9

Conditions:
$\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017".
Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

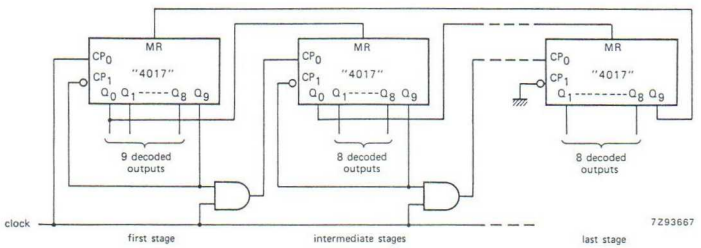


Fig. 10 Counter expansion

Note to Fig. 10

It is essential not to enable the counter on $\overline{CP}_1$ when CP_0 is HIGH, or on CP_0 when $\overline{CP}_1$ is LOW, as this would cause an extra count.

Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one "4017". Since "4017" has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.

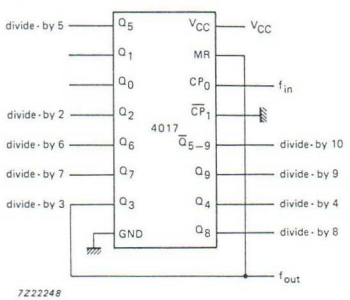


Fig. 11 Divide-by 2 through divide-by 10.

14-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0, Q_3 to Q_{13}).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	C_L = 15 pF V_{CC} = 5 V	11 6 17	15 6 19	ns ns ns
f_{max}	maximum clock frequency		101	52	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	19	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q_0, Q_3 to Q_{13}	parallel outputs
8	GND	ground (0 V)
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

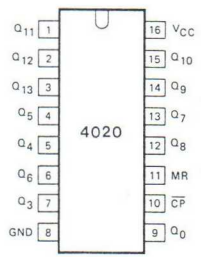


Fig. 1 Pin configuration.

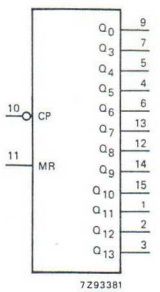


Fig. 2 Logic symbol.

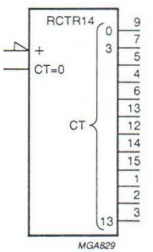


Fig. 3 IEC logic symbol.

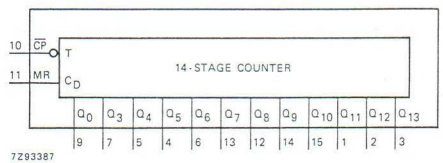


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

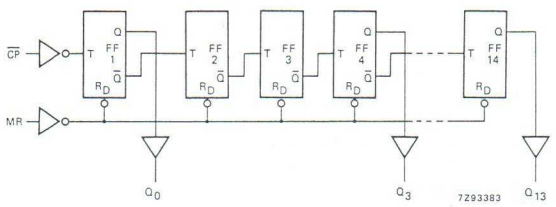


Fig. 5 Logic diagram.

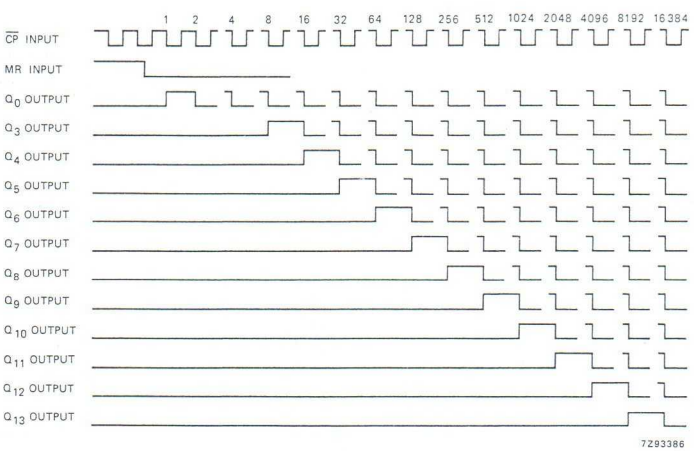


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		22 8 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n		55 20 16	170 34 29		215 43 37		225 51 43	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to $\overline{CP}$	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	30 92 109		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		18	36		45		54	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		8	15		19		22	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n		22	45		56		68	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	20	7		25		30		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	20	8		25		30		ns	4.5	Fig. 8
t_{rem}	removal time MR to $\overline{CP}$	10	2		13		15		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	25	47		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

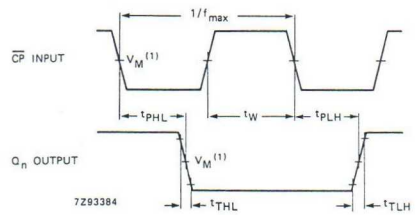


Fig. 7 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

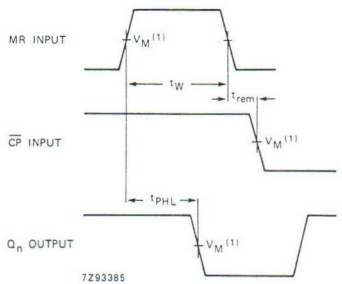


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

7-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the "4024" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4024 are 7-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q_0 to Q_6).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

APPLICATIONS

- Frequency dividing circuits
- Time delay circuits

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	14	14	ns
f_{max}	maximum clock frequency		90	70	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	25	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q_0 to Q_6	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	V_{CC}	positive supply voltage

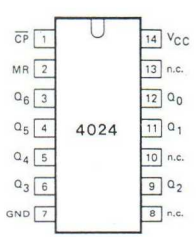


Fig. 1 Pin configuration.

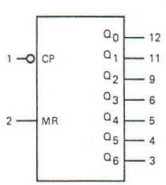


Fig. 2 Logic symbol.

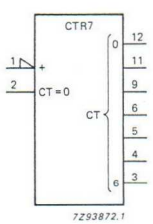


Fig. 3 IEC logic symbol.

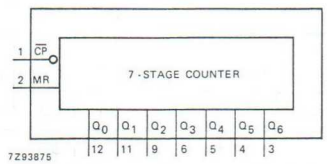


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

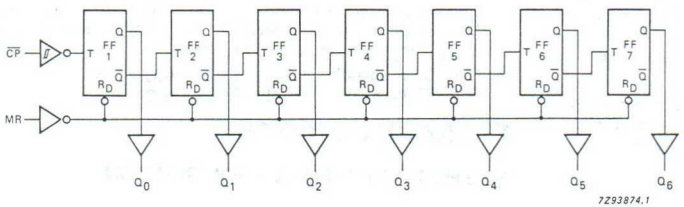


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR to Q_0		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		25 9 7	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{rem}	removal time MR to $\overline{CP}$	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.75
MR	0.85

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		17	35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR to Q_0		21	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		9	16		20		24	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig. 6
t_{rem}	removal time MR to $\overline{CP}$	10	0		13		15		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

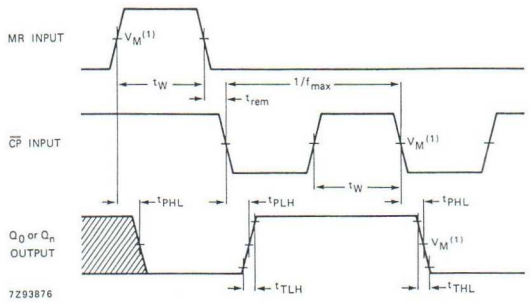


Fig. 6 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

Also showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

12-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q_0 to Q_{11}).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- **Frequency dividing circuits**
- **Time delay circuits**
- **Control counters**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1}	C_L = 15 pF V_{CC} = 5 V	14 8	16 8	ns ns
f_{max}	maximum clock frequency		90	79	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	parallel outputs
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

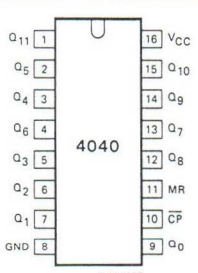


Fig. 1 Pin configuration.

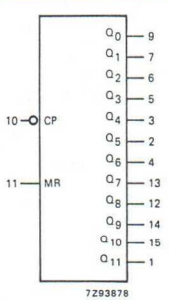


Fig. 2 Logic symbol.

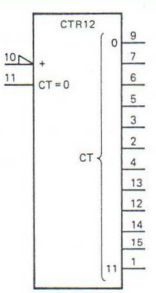


Fig. 3 IEC logic symbol.

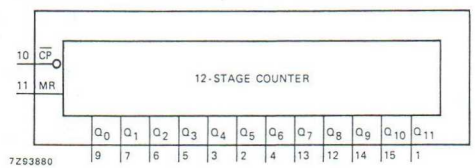


Fig. 4 Functional diagram.

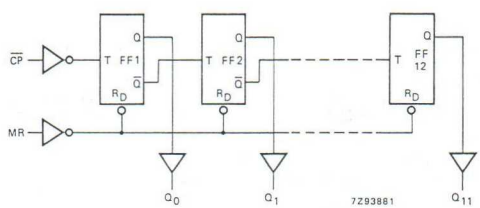


Fig. 5 Logic diagram.

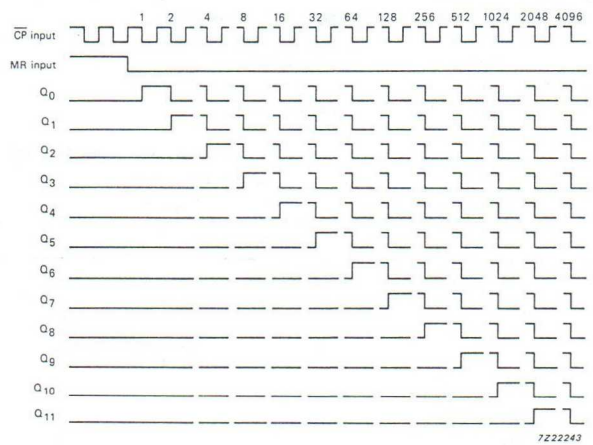


Fig. 6 Timing diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width; HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time MR to $\overline{CP}$	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0		19	40		50		60	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		10	20		25		30	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n		23	45		56		68	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
t_W	master reset pulse width; HIGH	16	6		20		24		ns	4.5	Fig. 7
t_{rem}	removal time MR to $\overline{CP}$	10	2		13		15		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

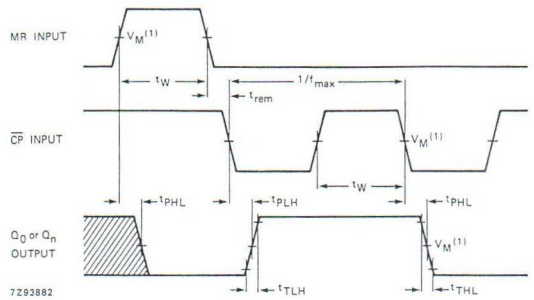


Fig. 7 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

Also showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PHASE-LOCKED-LOOP WITH VCO

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

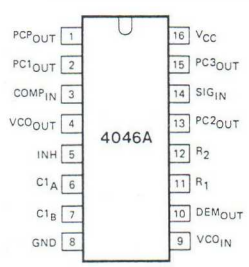


Fig. 1 Pin configuration.

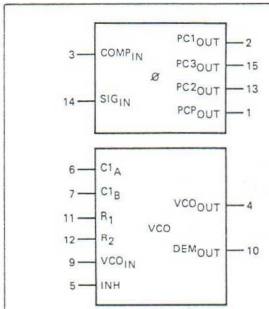


Fig. 2 Logic symbol.

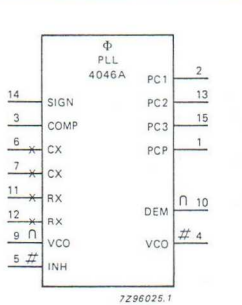


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

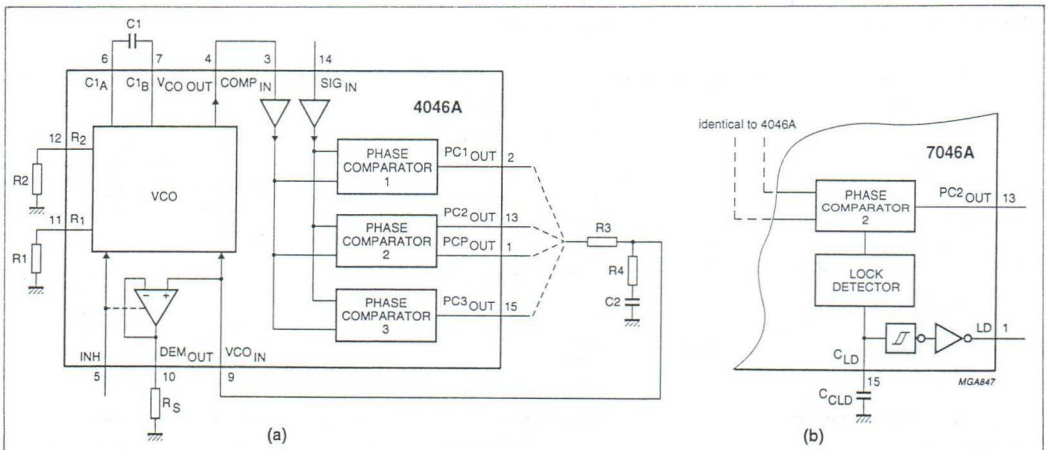


Fig. 4 Functional diagram.

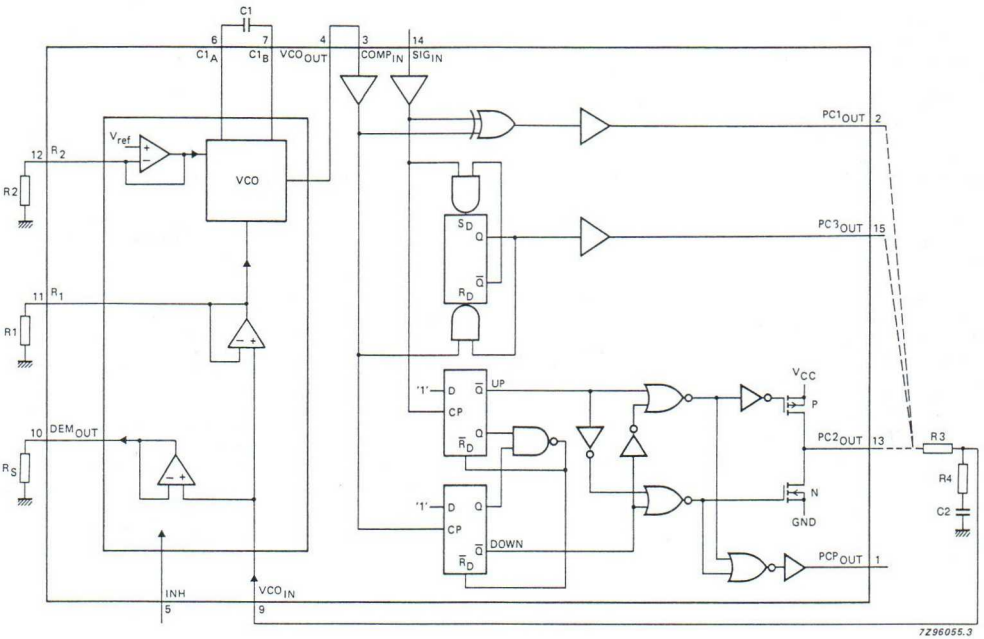


Fig. 5 Logic diagram.

The phase comparator gain is:

$K_p = \frac{V_{CC}}{\pi}$ (V/r).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

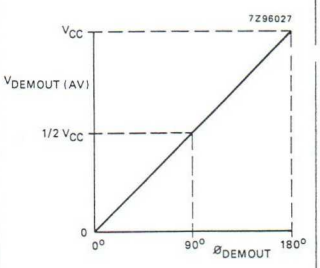


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC1OUT} =$

$\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

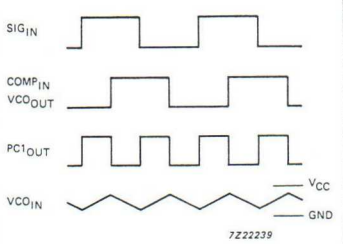


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

GENERAL DESCRIPTION (Cont'd)

Phase comparators (Cont'd)

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} \text{ (V/r)}.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding tc the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

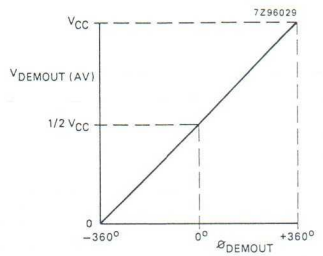


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC2OUT} =$

$\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

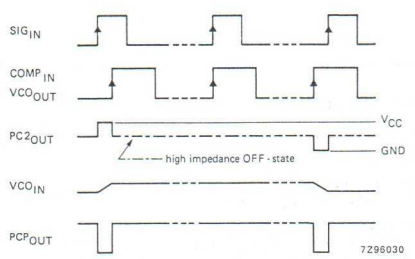


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{2\pi} \text{ (V/r)}.$$

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 10. Typical waveforms for the PC3 loop locked at f_o are shown in Fig. 11.

The phase-to-output response characteristic of PC3 (Fig. 10) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC3, to its lowest frequency.

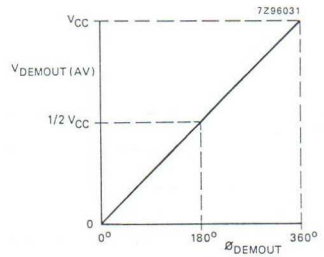


Fig. 10 Phase comparator 3: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC3OUT} =$

$\frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

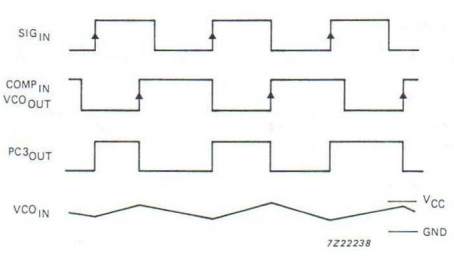


Fig. 11 Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		750	mW	for temperature range: −40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ	3.0 4.5 6.0	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HC (Cont'd)

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 5.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 17
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 16
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18
f_o	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2\ V_{CC}$; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		250						kΩ	4.5	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		23	40		50		60	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		35	68		85		102	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		28	54		68		81	ns	4.5	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		30	56		70		84	ns	4.5	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		36	65		81		98	ns	4.5	Fig. 17
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 16
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

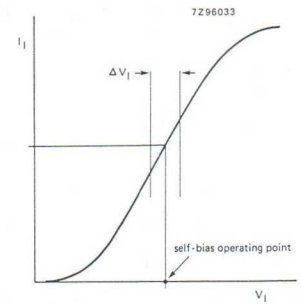


Fig. 12 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

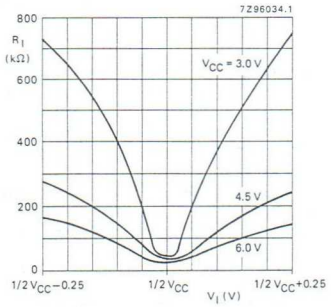


Fig. 13 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

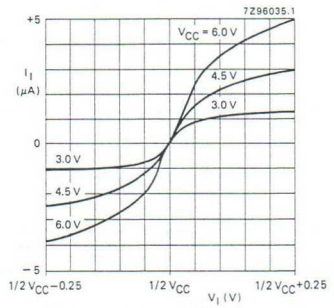
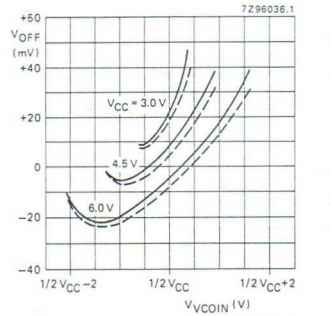


Fig. 14 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



— R_S = 50 kΩ
- - - R_S = 300 kΩ

Fig. 15 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

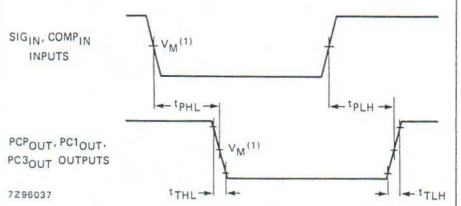


Fig. 16 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.

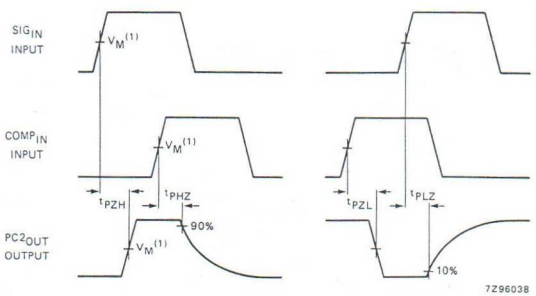


Fig. 17 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

AC WAVEFORMS (Continued)

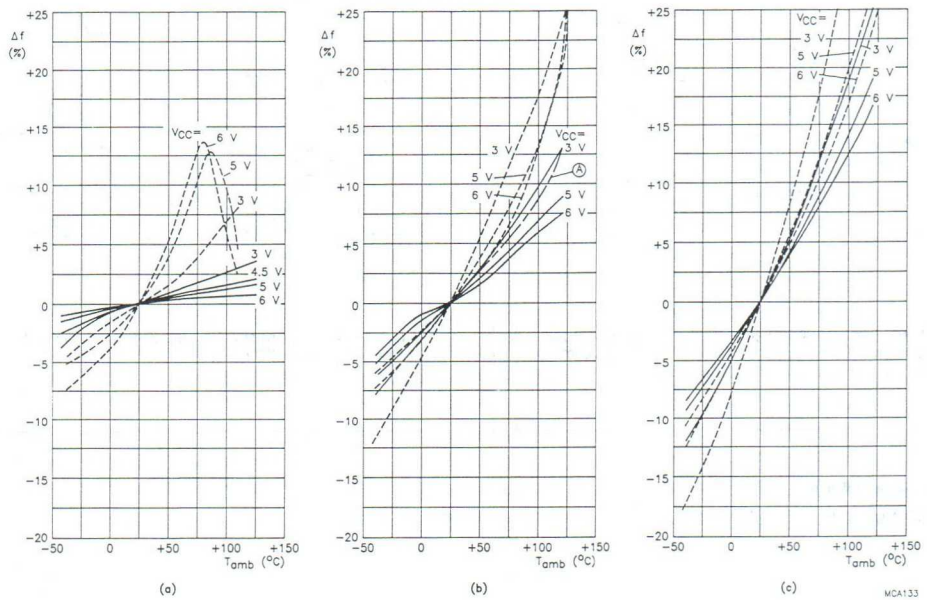
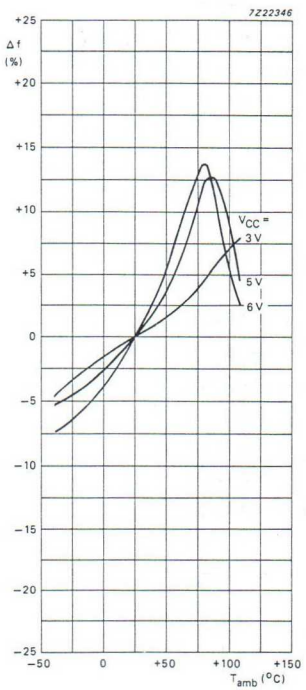
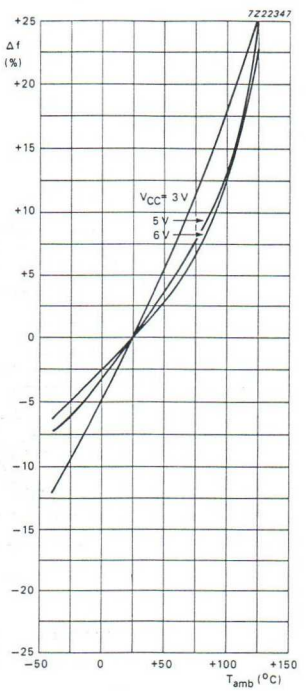


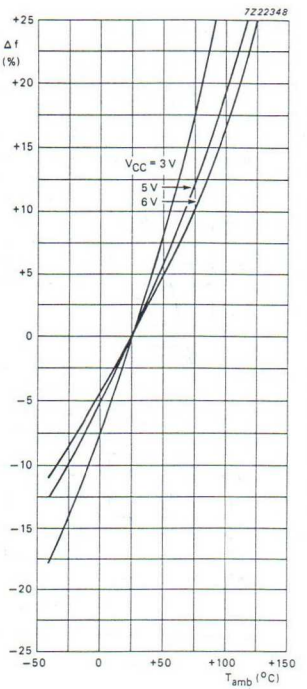
Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
——— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability cuves. C1 = 100 pF; $V_{VCO\ IN} = 0.5\ V_{CC}$.



(d) $R_2 = 3\ k\Omega$
$R_1 = \infty$



(e) $R_2 = 10\ k\Omega$
$R_1 = \infty$



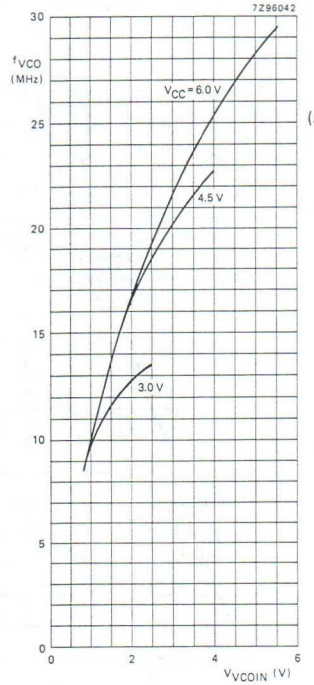
(f) $R_2 = 300\ k\Omega$
$R_1 = \infty$

Fig. 18 Continued.

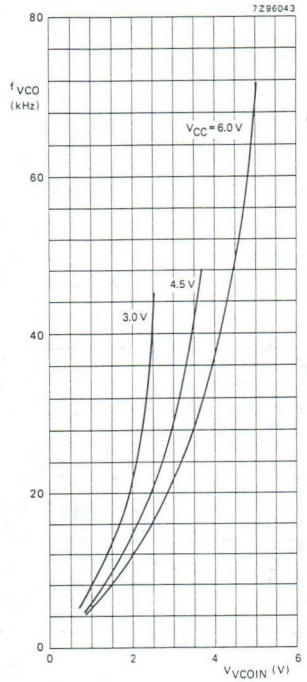
Note to Fig. 18

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

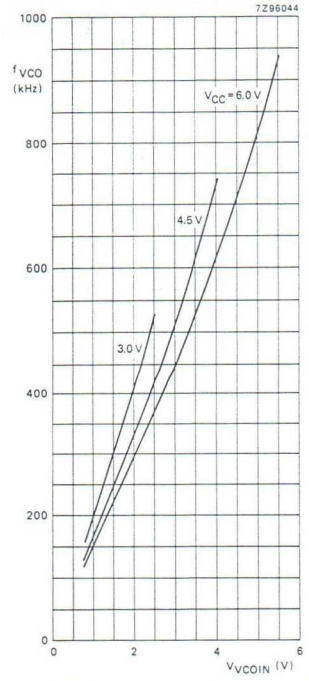
AC WAVEFORMS (Continued)



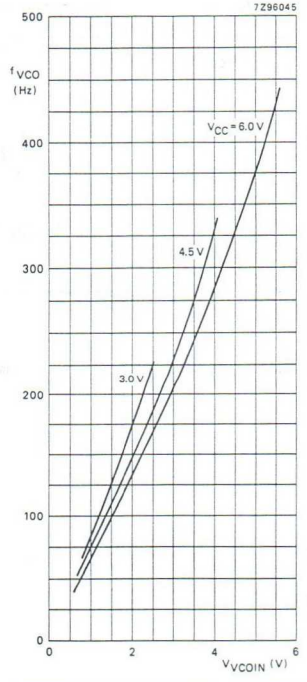
(a) R1 = 3 kΩ; C1 = 40 pF



(b) R1 = 3 kΩ; C1 = 100 nF



(c) R1 = 300 kΩ; C1 = 40 pF



(d) R1 = 300 kΩ; C1 = 100 nF

Fig. 19 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

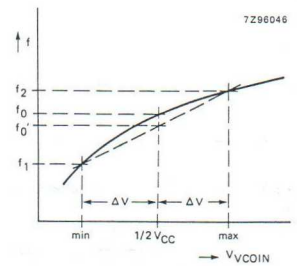


Fig. 20 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the V_{CC} range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2},$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

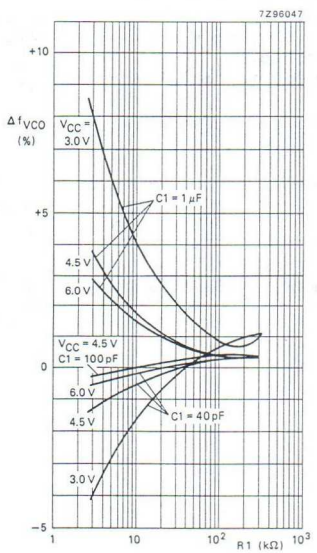
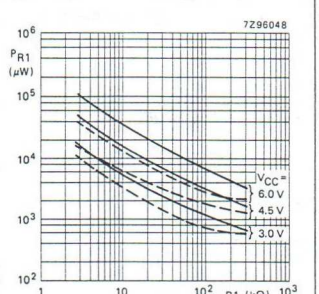
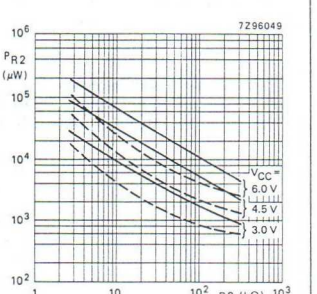


Fig. 21 Frequency linearity as a function of R1, C1 and V_{CC}: $R2 = \infty$ and $\Delta V = 0.5$ V.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 22 Power dissipation versus the value of R1: $C_L = 50$ pF; $R2 = \infty$; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 23 Power dissipation versus the value of R2: $C_L = 50$ pF; $R1 = \infty$; $V_{VCOIN} = GND = 0$ V; $T_{amb} = 25$ °C.

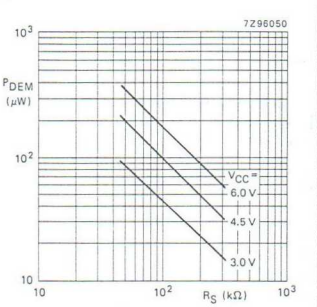


Fig. 24 Typical dc power dissipation of demodulator sections as a function of R_S: $R1 = R2 = \infty$; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

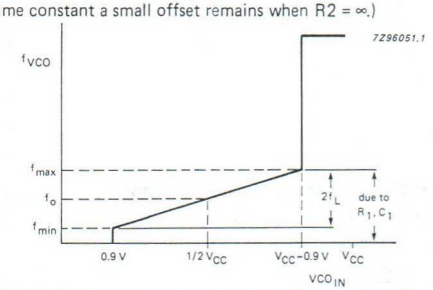
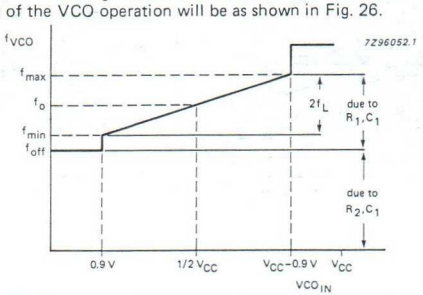
APPLICATION INFORMATION

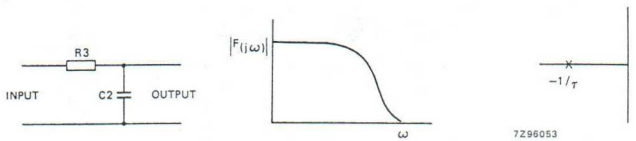
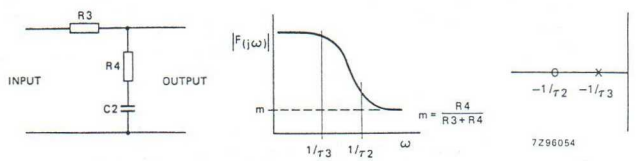
This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs 29, 30 and 31 as indicated in the table.

Values of the selected components should be within the following ranges:

R1 between 3 kΩ and 300 kΩ;
R2 between 3 kΩ and 300 kΩ;
R1 + R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 25. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  Fig. 25 Frequency characteristic of VCO operating without offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig. 29.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 29, use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 26.  Fig. 26 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig. 31. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig. 30. Calculate the value of R1 from the value of C1 and the product R1C1.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig. 6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 8).
	PC3	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 10).
PLL frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx 1/\pi\ (\sqrt{2\pi f_L/\tau})$ Fig. 27 Simple loop filter for PLL **without** offset; R3 ⩾ 500 Ω.  (a) τ_1 = R3 x C2; τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 (b) amplitude characteristic (c) pole-zero diagram Fig. 28 Simple loop filter for PLL **with** offset; R3 + R4 ⩾ 500 Ω.
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°
	PC3	$f_r = f_i$, large ripple content at ϕ_{DEMOUT} = 180°

APPLICATION INFORMATION (Continued)

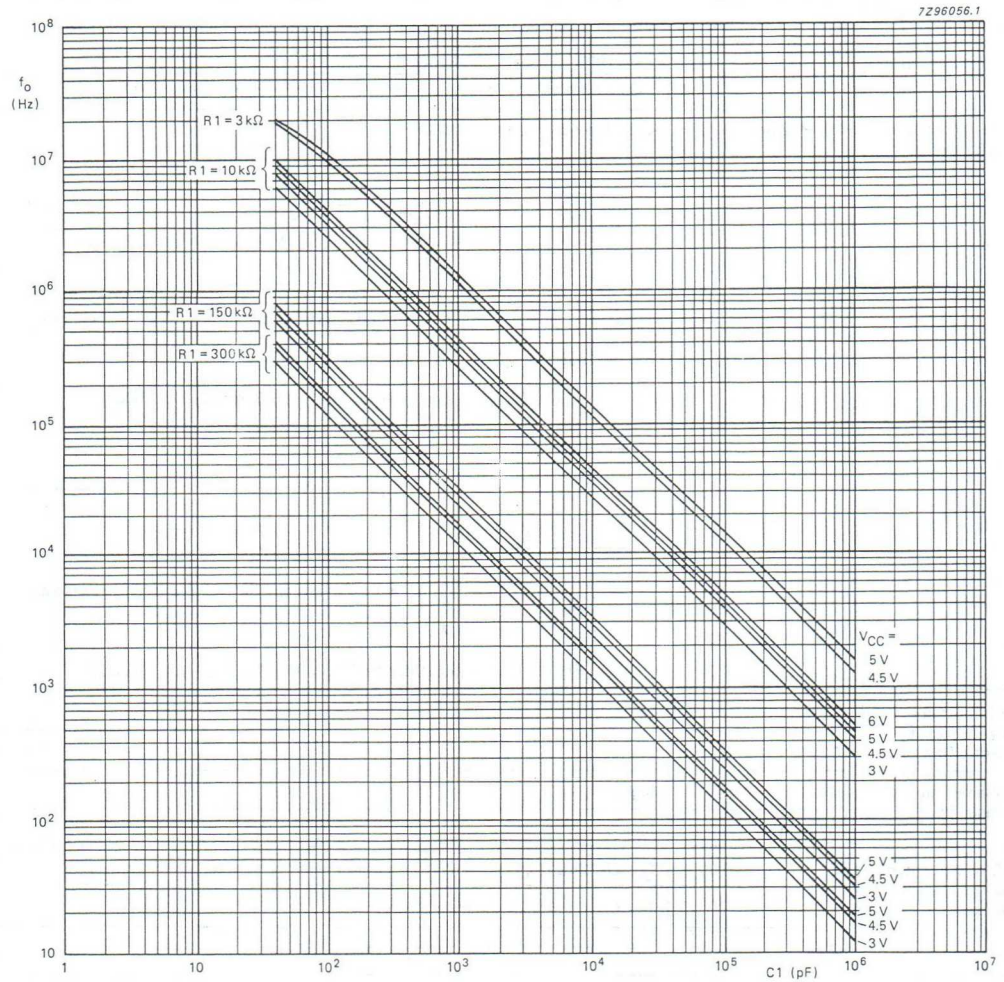


Fig. 29 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 29

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

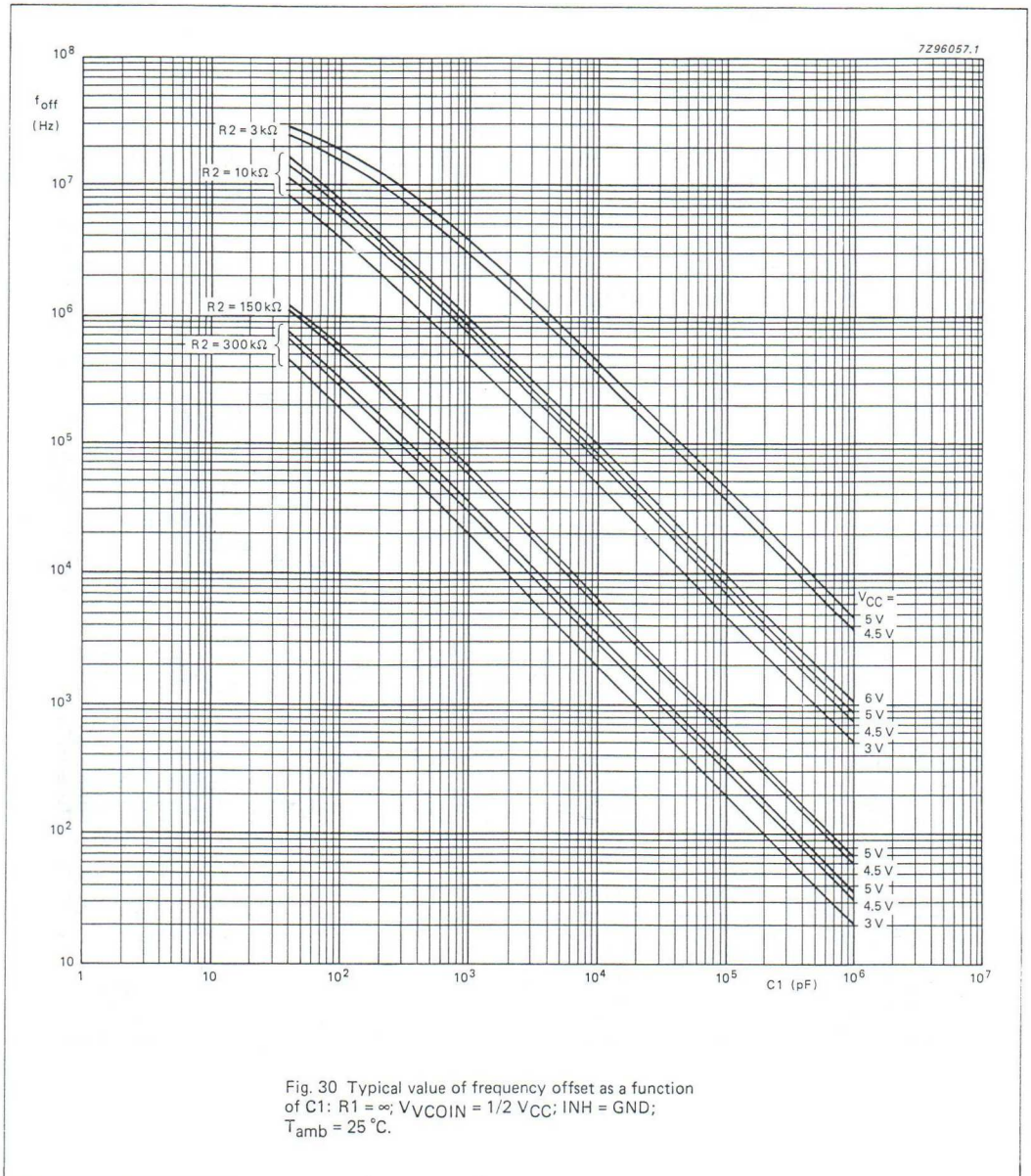


Fig. 30 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 30

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R2 can be easily calculated because, a constant R2C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION (Continued)

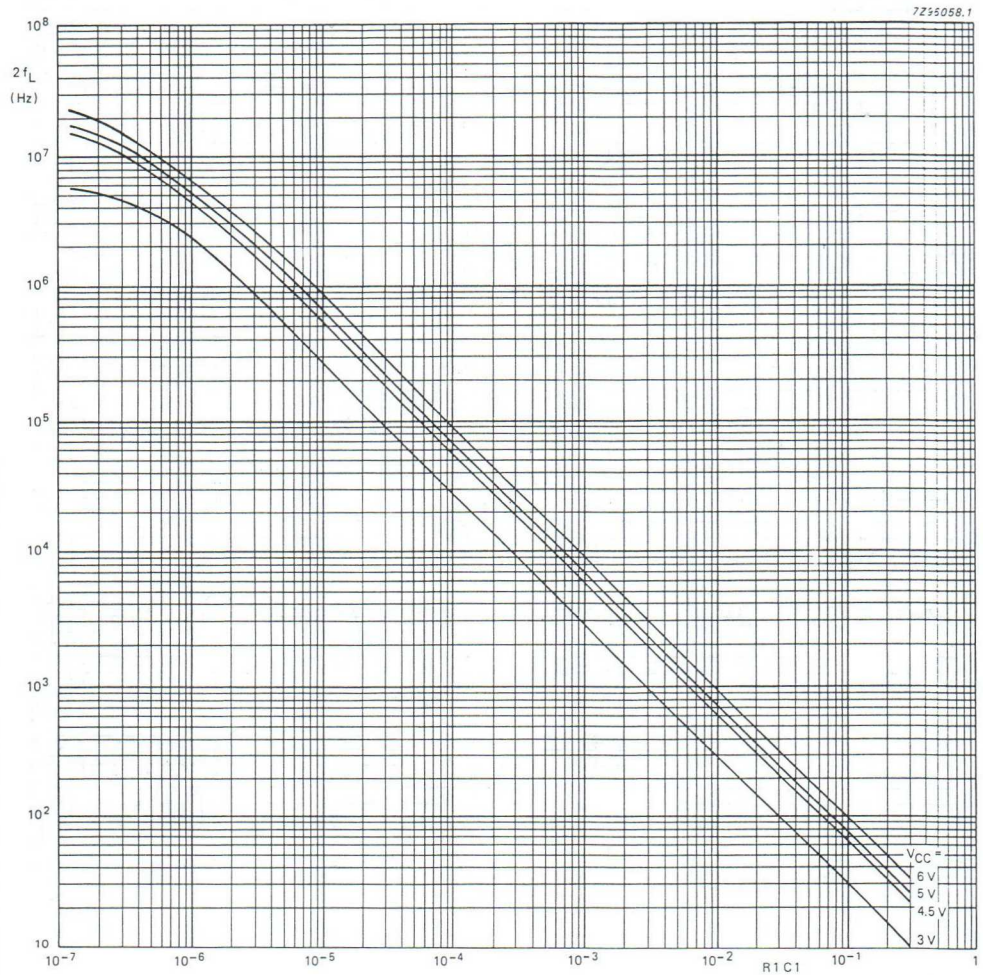


Fig. 31 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to ($V_{CC} - 0.9$) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN\ range}} 2\pi \text{ (r/s/V)}.$$

PLL design example

The frequency synthesizer, used in the design example shown in Fig. 32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : < 20%

The open-loop gain is H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
$K_o = K_v/s$ VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable).
The values can be determined using the information in the section "DESIGN CONSIDERATIONS".
With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/V$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}.$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:

$1 + H(s) \times G(s) = 0$.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ξ is defined as follows:

$$\xi = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}.$$

In Fig. 33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. From Fig. 33 it can be seen that the damping ratio ξ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \xi - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

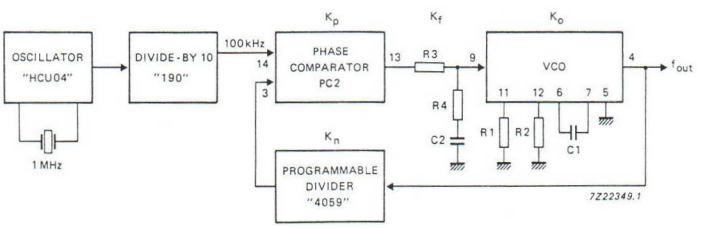


Fig. 32 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION (Continued)

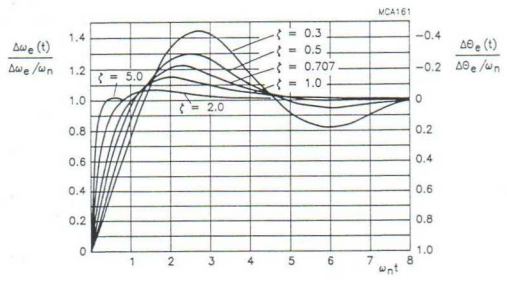


Fig. 33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

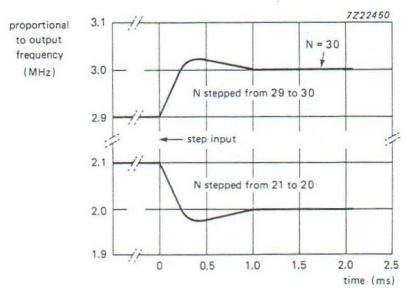


Fig. 34 Frequency compared to the time response.

HEX INVERTING HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC4049 is a high-speed Si-gate CMOS device and is pin compatible with the "4049" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4049 provides six inverting buffers with a modified input protection structure, which has no diode connected to V_{CC}. Input voltages of up to 15 V may therefore be used.
This feature enables the inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics. At the same time each part can be used as a simple inverter without level translation.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic.**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	note 1	14	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6ns

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1$\overline{Y}$ to 6$\overline{Y}$	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

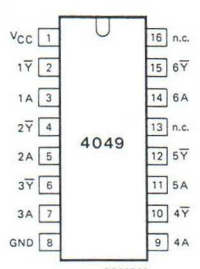


Fig. 1 Pin configuration.

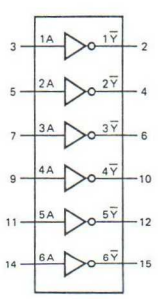


Fig. 2 Logic symbol.

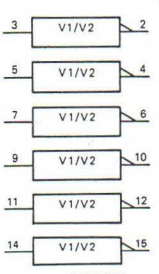


Fig. 3 IEC logic symbol.

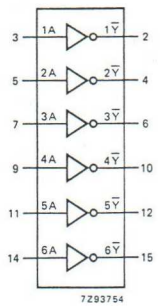


Fig. 4 Functional diagram.

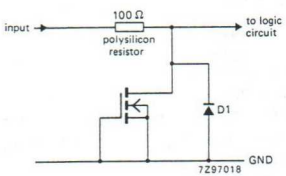


Fig. 5 Input protection for HC4049. Single sided thick oxide field effect metal gate transistor as input protection.

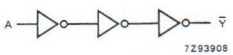


Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nȲ
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_{IK}	DC input voltage range	−0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: - standard outputs		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		750	mW	for temperature range: −40 to +125 °C 74HC above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	GND	—	15	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC characteristics
T_{amb}	operating ambient temperature range	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 650 1000	ns	V_{CC} = 2.0 V; V_{IN} = 2.0 V V_{CC} = 4.5 V; V_{IN} = 4.5 V V_{CC} = 6.0 V; V_{IN} = 6.0 V V_{CC} = 6.0 V; V_{IN} = 10.0 V V_{CC} = 6.0 V; V_{IN} = 15.0 V

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
± I_I	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to n$\overline{Y}$		28 10 8	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC WAVEFORMS

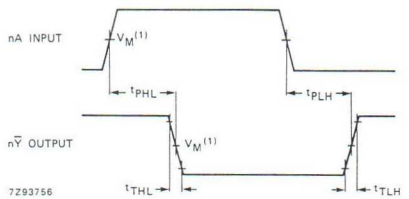


Fig. 7 Waveforms showing the input (nA) to output (nȲ) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC4050 is a high-speed Si-gate CMOS device and is pin compatible with the "4050" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4050 provides six non-inverting buffers with a modified input protection structure, which has no diode connected to V_{CC}. Input voltages of up to 15 V may therefore be used. This feature enables the non-inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic.**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	note 1	14	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

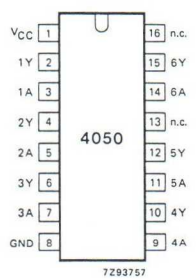


Fig. 1 Pin configuration.

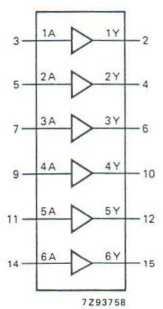


Fig. 2 Logic symbol.

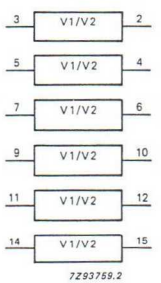


Fig. 3 IEC logic symbol.

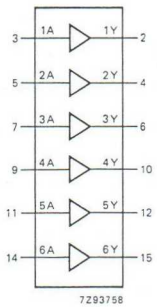


Fig. 4 Functional diagram.

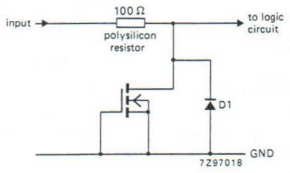


Fig. 5 Input protection for HC4050. Single sided thick oxide field effect metal gate transistor as input protection.

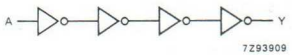


Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L H	L H

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_{IK}	DC input voltage range	−0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for $-0.5\ V < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: - standard outputs		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		750	mW	for temperature range: −40 to +125 °C 74HC above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	GND	–	15	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC characteristics
T_{amb}	operating ambient temperature range	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 650 1000	ns	V_{CC} = 2.0 V; V_{IN} = 2.0 V V_{CC} = 4.5 V; V_{IN} = 4.5 V V_{CC} = 6.0 V; V_{IN} = 6.0 V V_{CC} = 6.0 V; V_{IN} = 10.0 V V_{CC} = 6.0 V; V_{IN} = 15.0 V

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
± I_I	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC WAVEFORMS

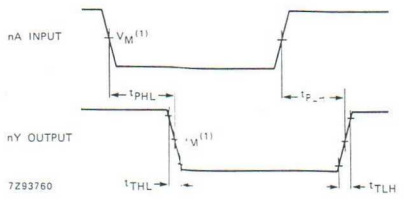


Fig. 7 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Wide analog input voltage range: ± 5 V.
- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4051 are high-speed Si-gate CMOS devices and are pin compatible with the "4051" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4051 are 8-channel analog multiplexers/demultiplexers with three digital select inputs (S_0 to S_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{OS}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	22	22	ns
	turn "ON" time S_n to V_{OS}		20	24	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{OS}		18	16	ns
	turn "OFF" time S_n to V_{OS}		19	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	25	25	pF
C_S	max. switch capacitance independent (Y)		5	5	pF
	max. switch capacitance common (Z)		25	25	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	independent inputs/outputs
16	V_{CC}	positive supply voltage

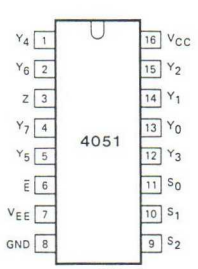


Fig. 1 Pin configuration.

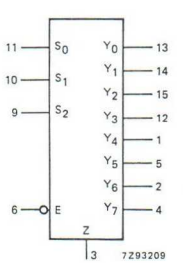


Fig. 2 Logic symbol.

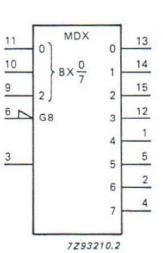


Fig. 3 IEC logic symbol.

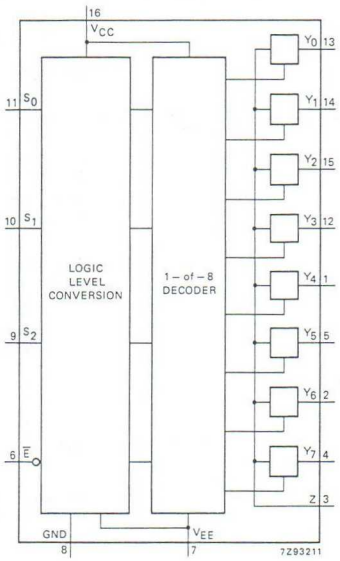


Fig. 4 Functional diagram.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS				channel ON
$\bar{E}$	S_2	S_1	S_0	
L	L	L	L	$Y_0 - Z$
L	L	L	H	$Y_1 - Z$
L	L	H	L	$Y_2 - Z$
L	L	H	H	$Y_3 - Z$
L	H	L	L	$Y_4 - Z$
L	H	L	H	$Y_5 - Z$
L	H	H	L	$Y_6 - Z$
L	H	H	H	$Y_7 - Z$
H	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

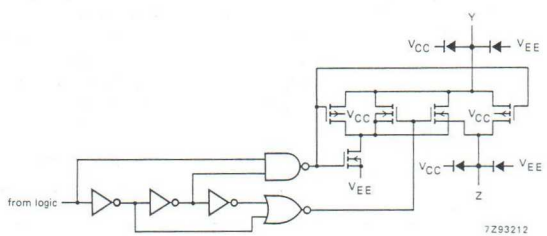


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

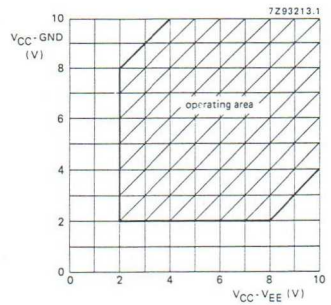


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4051.

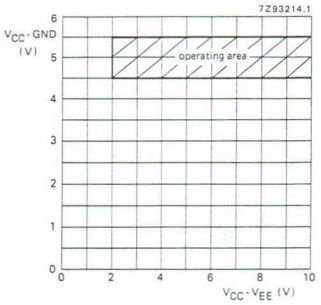


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4051.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT												
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 17)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		72 29 21 18	345 69 59 51		430 86 73 64		520 104 88 77	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		66 28 19 16	345 69 59 51		430 86 73 64		520 104 88 77	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		58 31 17 18	290 58 49 42		365 73 62 53		435 87 74 72	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		61 25 18 18	290 58 49 42		365 73 62 53		435 87 74 72	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_n	0.50
$\overline{E}$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 17)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		26 16	55 39		69 49		83 59	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		28 16	55 39		69 49		83 59	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		19 16	45 32		56 40		68 48	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		23 16	45 32		56 40		68 48	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18, 19 and 20)

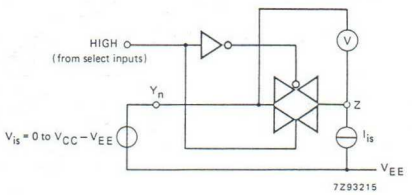


Fig. 8 Test circuit for measuring R_{ON}.

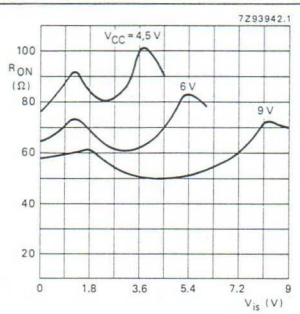


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

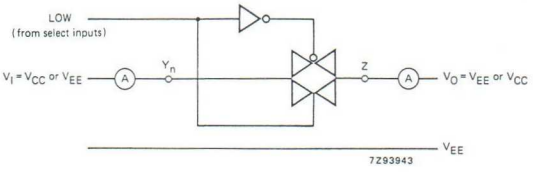


Fig. 10 Test circuit for measuring OFF-state current.

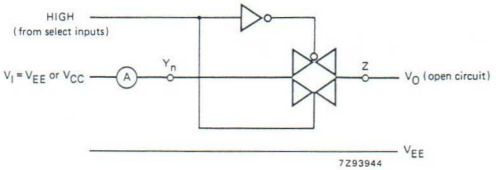


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF (see Figs 12 and 15)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 16)
f_{max}	minimum frequency response (−3dB)	170 180	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	 5 25	 pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at a Y_n or Z terminal. whichever is assigned as an input.
V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

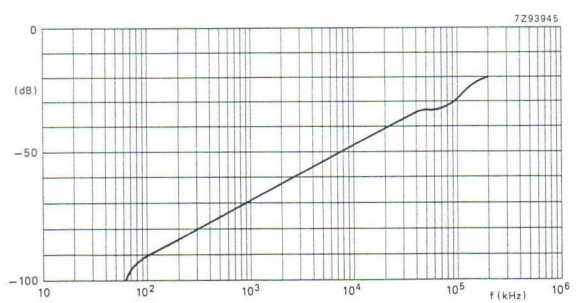
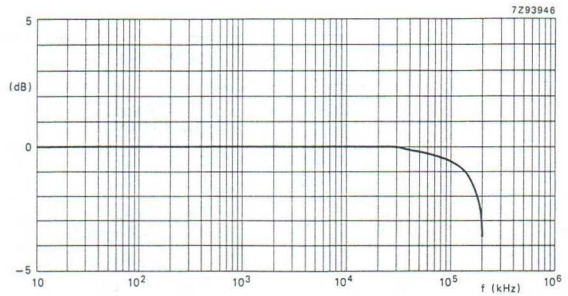


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ

Fig. 13 Typical frequency response.

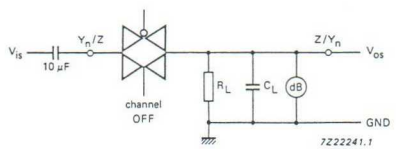


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

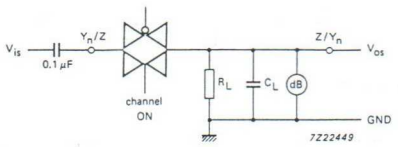


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

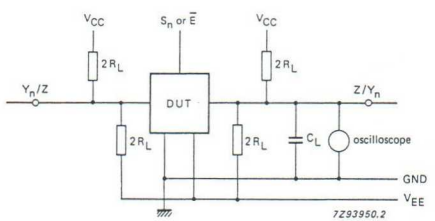
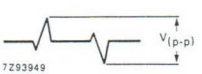


Fig. 16 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 16

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

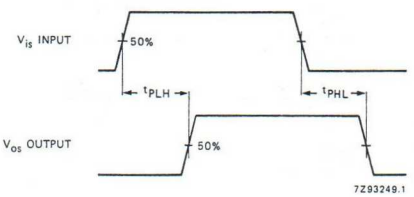


Fig. 17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

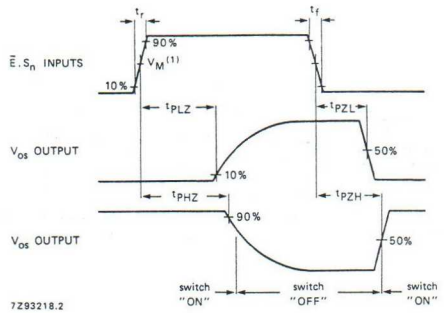


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

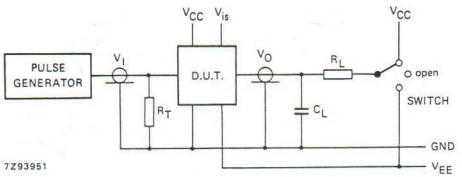


Fig. 19 Test circuit for measuring AC performance.

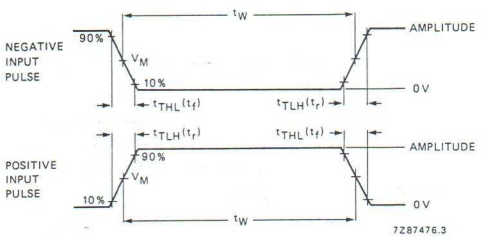


Fig. 20 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 19 and 20:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r, t_f with 50% duty factor.

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Wide analog input voltage range: ± 5 V.
- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}$).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 and S_1, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ or S_n to V_{OS}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 5 V	28	18	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ or S_n to V_{OS}		21	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
C_S	max. switch capacitance independent (Y)		5	5	pF
	common (Z)		12	12	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	$2Y_0$ to $2Y_3$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
10, 9	S_0, S_1	select inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	V_{CC}	positive supply voltage

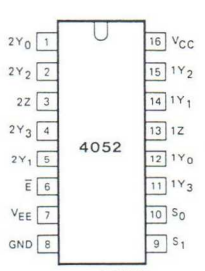


Fig. 1 Pin configuration.

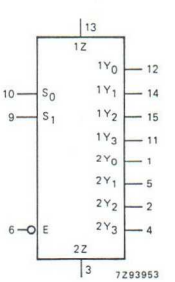


Fig. 2 Logic symbol.

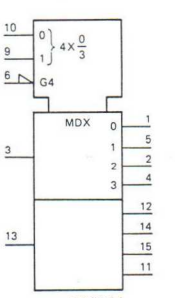


Fig. 3 IEC logic symbol.

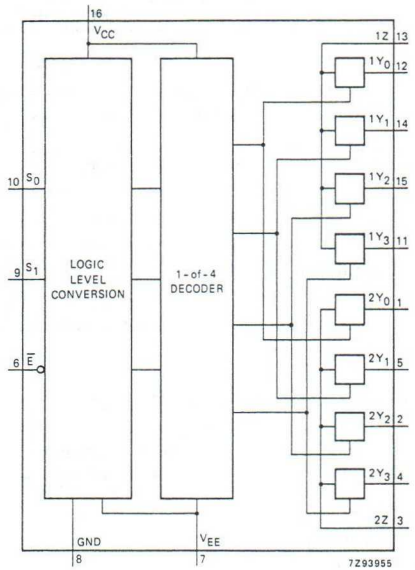


Fig. 4 Functional diagram.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and
- demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S_1	S_0	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

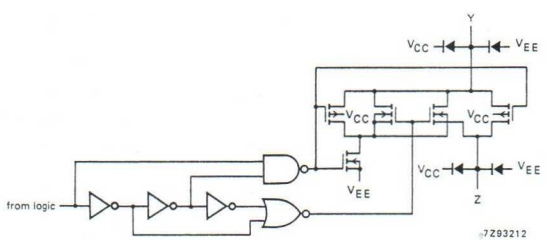


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

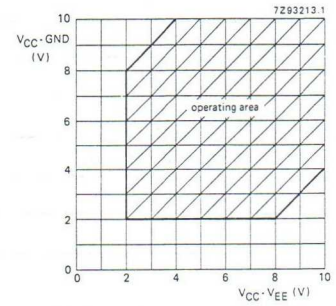


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4052.

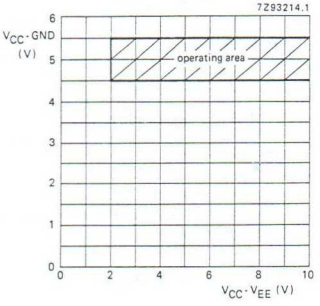


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT												
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IN} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum ΔON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}		105 38 30 26	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		74 27 22 22	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_n	0.45
$\overline{E}$	0.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}		41 28	70 48		88 60		105 72	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		26 21	50 38		63 48		75 57	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

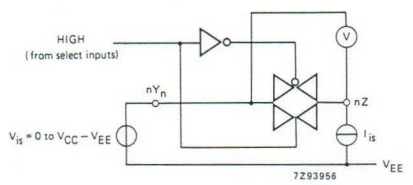


Fig. 8 Test circuit for measuring R_{ON}.

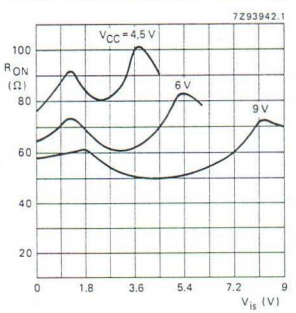


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

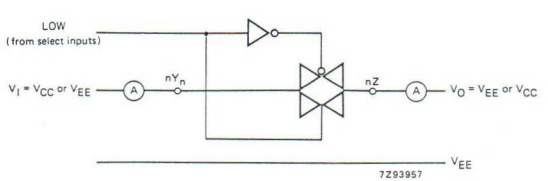


Fig. 10 Test circuit for measuring OFF-state current.

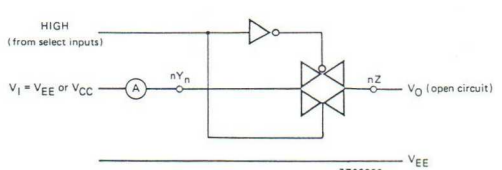


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3dB)	170 180	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 50 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	 5 12	 pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

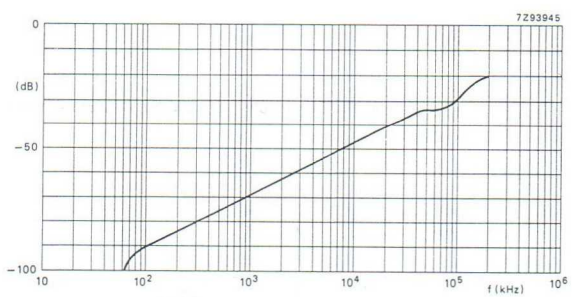
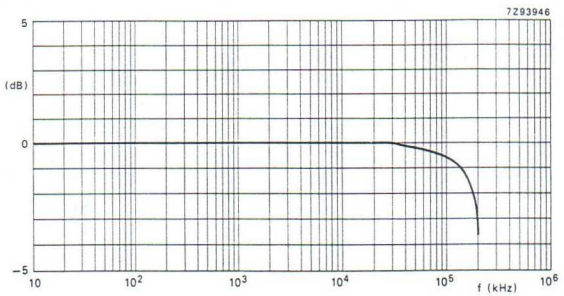


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

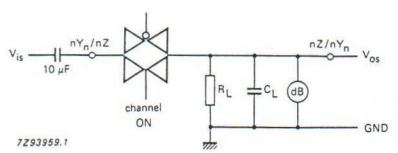


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

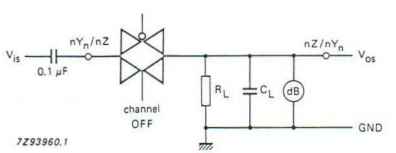


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

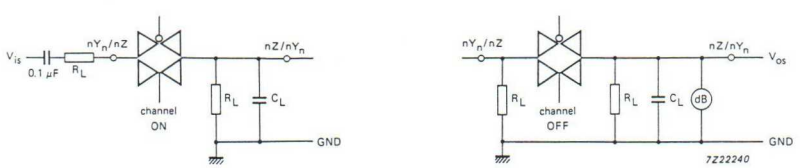


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

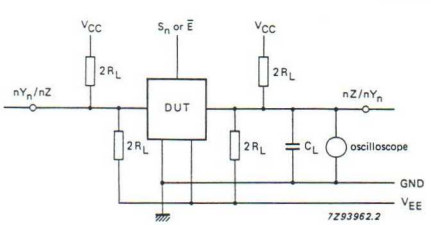
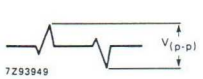


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

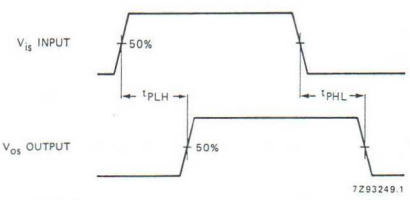


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

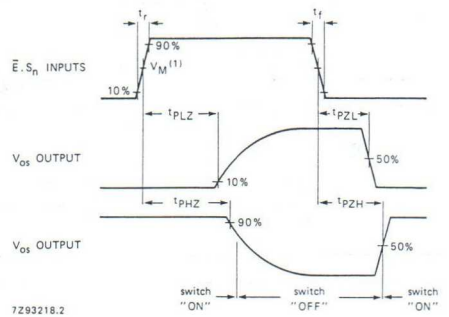


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

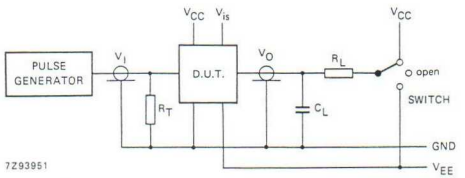


Fig. 20 Test circuit for measuring AC performance.

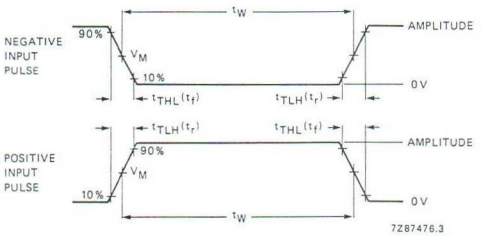


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r, t_f with 50% duty factor.

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and three digital select inputs (S_1 to S_3).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_1 to S_3. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_1 to S_3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1 to S_3, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 and nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	17 21	23 21	ns ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{OS} S_n to V_{OS}		18 17	20 19	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	36	36	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 8	5 8	pF pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

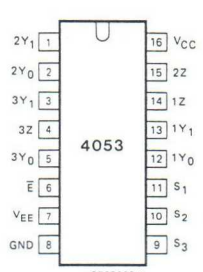


Fig. 1 Pin configuration.

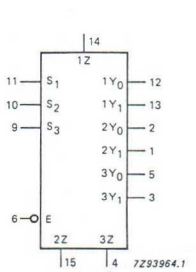


Fig. 2 Logic symbol.

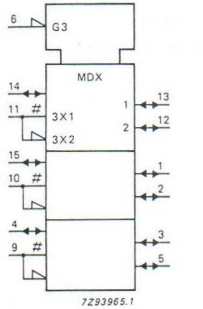


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	$2Y_0$, $2Y_1$	independent inputs/outputs
5, 3	$3Y_0$, $3Y_1$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_1 to S_3	select inputs
12, 13	$1Y_0$, $1Y_1$	independent inputs/outputs
14, 15, 4	1Z to 3Z	common inputs/outputs
16	V_{CC}	positive supply voltage

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

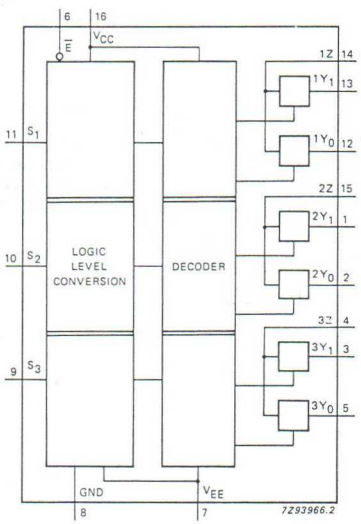


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	S_n	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

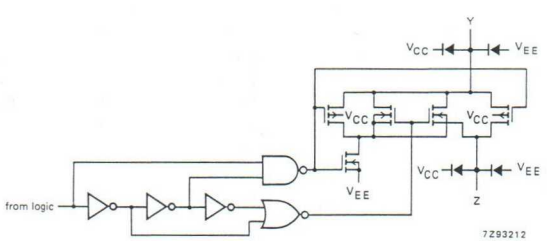


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

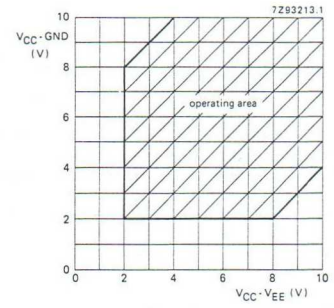


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4053.

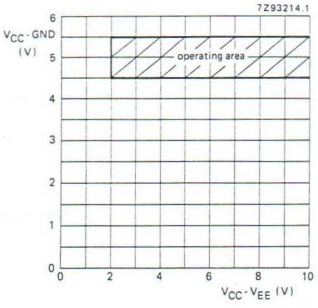


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4053.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT								V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		+25			–40 to +85		–40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC											
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} =$ V_{CC} or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_{EE} V	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		15 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		60 20 16 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		75 25 20 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		63 21 17 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		60 20 16 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			–40 to +85		–40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} -2.1 V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_n	0.50
$\overline{E}$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 –4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		27 16	48 34		60 43		72 51	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		25 16	48 34		60 43		72 51	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		24 15	44 31		55 39		66 47	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		22 15	44 31		55 39		66 47	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

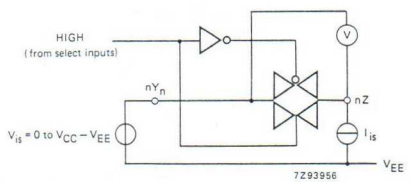


Fig. 8 Test circuit for measuring R_{ON}.

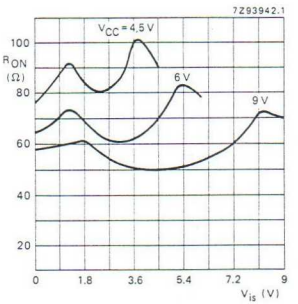


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

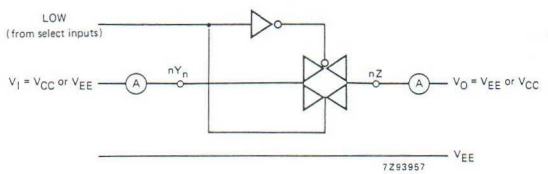


Fig. 10 Test circuit for measuring OFF-state current.

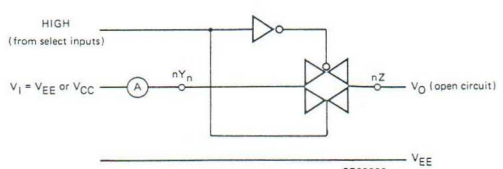


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3dB)	160 170	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 8	pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

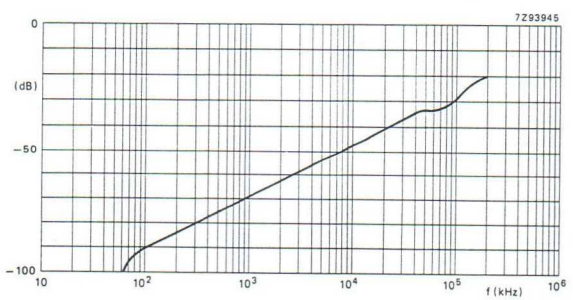
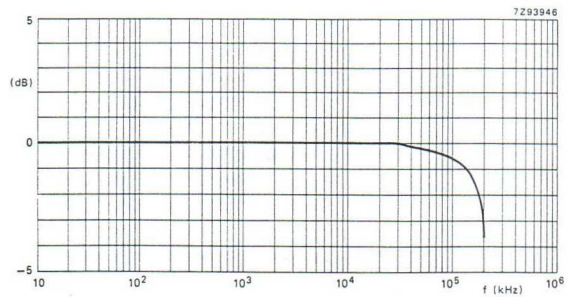


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

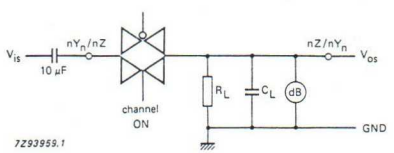


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

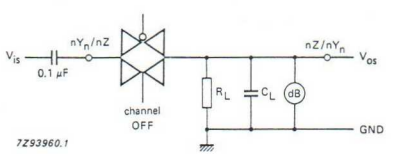


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

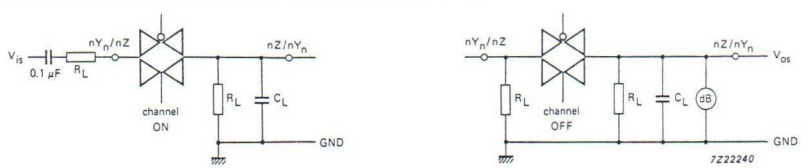


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

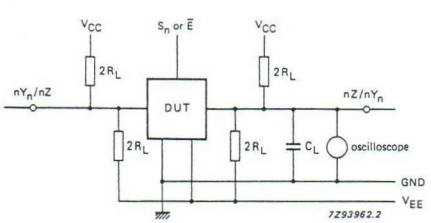
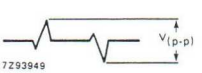


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

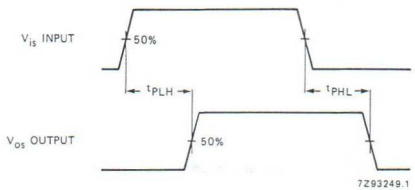


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

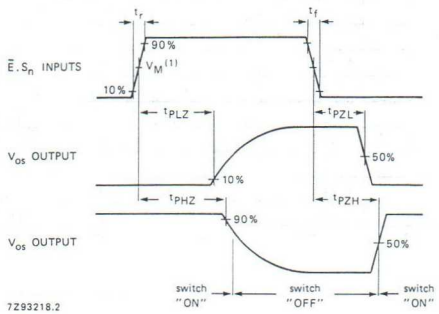


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

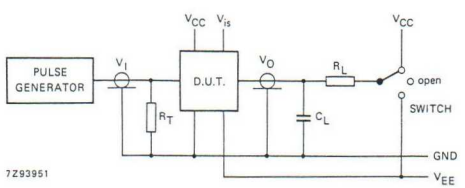


Fig. 20 Test circuit for measuring AC performance.

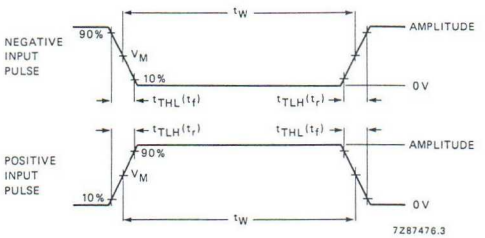


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

PROGRAMMABLE DIVIDE-BY-N COUNTER

FEATURES

- Synchronous programmable divide-by-n counter
- Presettable down counter
- Fully static operation
- Mode select control of initial decade counting function (divide-by-10, 8, 5, 4 and 2)
- Master preset initialization
- Latchable output
- Easily cascadable with other counters
- Four operating modes:
  timer
  divide-by-n
  divide-by-10 000
  master preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4059 are high-speed Si-gate CMOS devices and are pin compatible with the "4059" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4059 are divide-by-n counters which can be programmed to divide an input frequency by any number (n) from 3 to 15 999. There are four operating modes, timer, divide-by-n, divide-by-10 000 and master preset, which are defined by the mode select inputs (K_a to K_c) and the latch enable input (LE) as shown in the Function table.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q	C_L = 15 pF, V_{CC} = 5 V	18	20	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

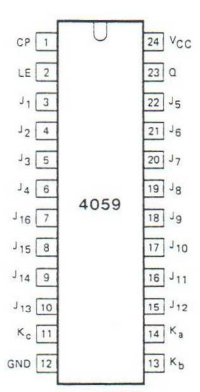


Fig. 1 Pin configuration.

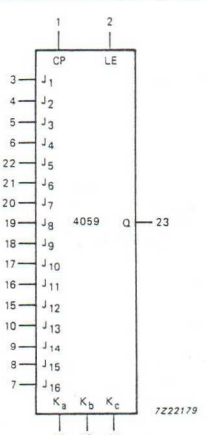


Fig. 2 Logic symbol.

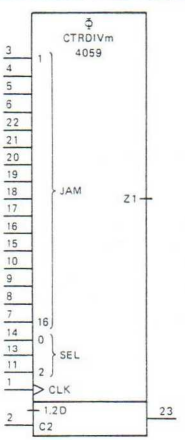


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	LE	latch enable (active HIGH)
3, 4, 5, 6, 22, 21, 20, 19, 18, 17, 16, 15, 10, 9, 8, 7	J_1 to J_{16}	programmable JAM inputs (BCD)
12	GND	ground (0 V)
14, 13, 11	K_a to K_c	mode select inputs
23	Q	divide-by-n output
24	V_{CC}	positive supply voltage

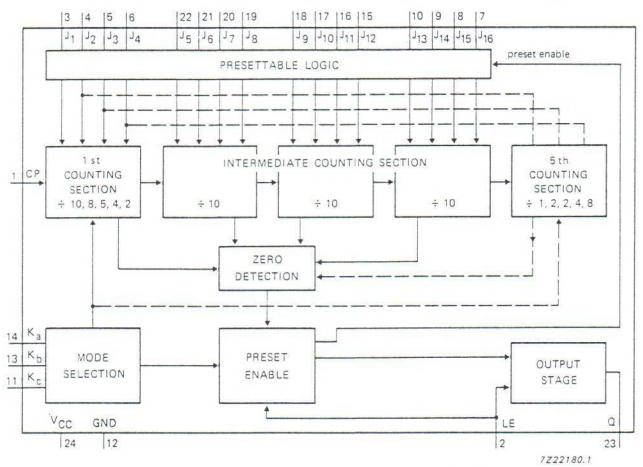


Fig. 4 Functional block diagram.

APPLICATIONS

- Frequency synthesizer, ideally suited for use with PC74HC/HCT4046A and PC74HC/HCT7046A (PLLs)
- Fixed or programmable frequency division
- "Time out" timer

GENERAL DESCRIPTION (Cont'd)

The complete counter consists of a first counting stage, an intermediate counting stage and a fifth counting stage. The first counter stage consists of four independent flip-flops. Depending on the divide-by-mode, at least one flip-flop is placed at the input of the intermediate stage (the remaining flip-flops are placed at the fifth stage with a place value of thousands). The intermediate stage consists of three cascaded decade counters, each containing four flip-flops.

All flip-flops can be preset to a desired state by means of the JAM inputs (J_1 to J_{16}), during which the clock input (CP) will cause all stages to count from n to zero. The zero-detect circuit will then cause all stages to return to the JAM count, during which an output pulse is generated. In the timer mode, after an output pulse is generated, the output pulse remains HIGH until the latch input (LE) goes LOW. The counter will advance, even if LE is HIGH and the output is latched in the HIGH state. In the divide-by-n mode, a clock cycle wide pulse is generated with a frequency rate equal to the input frequency divided by n.

The function of the mode select and JAM inputs are illustrated in the following examples. In the divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. This counting mode is selected when K_a to K_c are set HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

If the divide-by-10 mode is desired for the first section, K_a and K_b are set HIGH and K_c is set LOW. The JAM inputs J_1 to J_4 are used to preset the first counting section (there is no last counting section). The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters, presettable by means of the JAM inputs J_5 to J_{16}.

GENERAL DESCRIPTION

The preset of the counter to a desired divide-by-n is achieved as follows:

n = (MODE*) (1 000 x decade 5 preset
+ 100 x decade 4 preset
+ 10 x decade 3 preset
+ 1 x decade 2 preset)
+ decade 1 preset

* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any "n" count, divide the "n" count by the selected mode. The resultant is the corresponding preset value of the 5th to the 2nd decade with the remainder being equal to the 1st decade value; preset value = n/mode.

If n = 8 479, and the selected mode = 5, the preset value = 8 479/5 = 1 695 with a remainder of 4, thus the JAM inputs must be set as shown in Table 1.

To verify the results, use the given equation:

n = 5 (1 000 x 1 + 100 x 6 + 10 x 9
+ 1 x 5) + 4

n = 8 479.

If n = 12 382 and the selected mode = 8, the preset value = 12 382/8 = 1 547 with a remainder of 6, thus the JAM inputs must be set as shown in Table 2.

To verify:

n = 8 (1 000 x 1 + 100 x 5 + 10 x 4
+ 1 x 7) + 6

n = 12 382.

If n = 8 479 and the selected mode = 10, the preset value = 8 479/10 with a remainder of 9, thus the JAM inputs must be set as shown in Table 3.

To verify:

n = 10 (1 000 x 0 + 100 x 8 + 10 x 4
+ 1 x 7) + 9

n = 8 479.

The three decades of the intermediate counting section can be preset to a binary 15 instead of a BCD 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 counting pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the divide-by-8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade: 1 500
2nd decade: 150
1st decade: 15

The last counting section can be preset to a maximum of 1, with a place value of 1 000. The first counting section can be preset to a maximum of 7. To calculate n:

n = 8 (1 000 x 1 + 100 x 15 + 10 x 15
+ 1 x 15) + 7

n = 21 327.

(continued on next page)

FUNCTION TABLE

LATCH ENABLE INPUT	MODE SELECT INPUTS			FIRST COUNTING SECTION DECADE 1			LAST COUNTING SECTION DECADE 5			COUNTER RANGE		OPERATION
LE	K_a	K_b	K_c	MODE	MAX. PRESET STATE	JAM INPUTS USED	DIVIDE BY	MAX. PRESET STATE	JAM INPUTS USED	BCD MAX.	BINARY MAX.	
H	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	timer mode
H	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
H	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
H	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
H	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	divide-by-n mode
L	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
L	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
L	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
L	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
H	L	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	L	H	L	preset inhibited			preset inhibited			fixed 10 000	–	divide-by-10 000 mode
X	X	L	L	master preset			master preset			–	–	master preset mode

Where:

H = HIGH voltage level
L = LOW voltage level
X = don't care

Note

It is recommended that the device is in the master preset mode (K_b = K_c = logic 0) in order to correctly initialize the device prior to start-up. An example of a suitable external circuit is shown in Fig. 14.

Table 1

4			1	5				9				6			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

Table 2

6			1	7				4				5			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	H	H	H	H	H	H	L	L	L	H	L	H	L	H	L

Table 3

9				7				4				8			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
H	L	L	H	H	H	H	L	L	L	H	L	L	L	L	H

GENERAL DESCRIPTION (Cont'd)

21 327 is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the Function table, in the column entitled "binary counter range".

The mode select inputs permit, when used with decimal programming, a non-BCD least significant digit. For example, the channel spacing in a radio is 12.5 kHz, it may be convenient to program the counter in decimal steps of 100 kHz subdivided into 8 steps of 12.5 kHz controlled by the least significant digit. Also frequency synthesizer channel separations of 10, 12.5, 20, 25 and 50 parts can be chosen by the mode select inputs. This is called "Fractional extension". A similar extension called "Half channel offset" can be obtained in modes 2, 4, 6 and 8, if the JAM inputs are switched between zero and 1, 2, 3 and 4 respectfully. This is illustrated in Fig. 5.

This features is used primarily is cases where radio channels are allocated according to the following formula:

Channel frequency = channel spacing x (N + 0.5)

N is an integer.

Control inputs K_b and K_c can be used to initiate and lock the counter in the "master preset" mode. In this condition the flip-flops in the counter are preset in accordance with the JAM inputs and the counter remains in that mode as long as K_b and K_c both remain LOW. The counter begins to count down from the preset state when a counting mode other than the "master preset" mode is selected.

Whenever the "master preset" mode is used, control signals $K_b = K_c$ = LOW must be applied for at least 2 full clock pulses. After the "master preset" mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down begins on the second positive-going clock transition. Thus, after a "master preset" mode, there is always one extra count before the output goes HIGH. Figure 6 illustrates the operation of the counter in the divide-by-8 mode starting from the preset state 3.

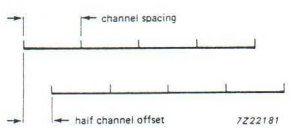


Fig. 5 Half channel offset.

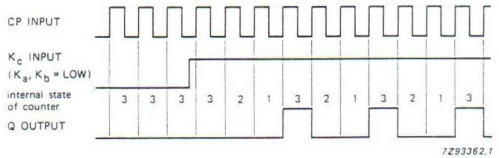


Fig. 6 Total count of 3.

If the "master preset" mode is started two clock cycles or less before an output pulse, the output pulse will appear at the correct moment. When the output pulse appears and the "master preset" mode is not selected, the counter is preset according to the states of the JAM inputs.

When K_a, K_b, K_c and LE are LOW, the counter operates in the "preset inhibit" mode, during which the counter divides at a fixed rate of 10 000, independent of the state of the JAM inputs. However, the first cycle length after leaving the "master preset" mode is determined by the JAM inputs.

When K_a, K_b and K_c are LOW and input LE = HIGH, the counter operates in the normal divide-by-10 mode, however, without the latch operation at the output.

This device is particularly advantageous in digital frequency synthesizer circuits (VHF, UHF, FM, AM etc.) for communication systems, where programmable divide-by-"n" counters are an integral part of the synthesizer phase-locked-loop sub-system. The 74HC/HCT4059 can also be used to perform the synthesizer "fixed divide-by-n" counting function, as well as general purpose counting for instrumentation functions such as totalizers, production counters and "time out" timers.

Schmitt-trigger action at the clock input makes the circuit highly tolerant to slower clock rise and fall times.

DC CHARACTERISTIC FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay LE to Q		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width CP	90 18 15	7 6 5		115 23 90		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time K_b, K_c to CP	75 15 13	19 7 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 9; note 1
f_{max}	maximum clock pulse frequency	4.2 21 25	12 36 43		3.4 17 20		2.8 14 17		MHz	2.0 4.5 6.0	Fig. 7

Note to the characteristic table

1. From master preset mode to any other mode.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP	0.65
LE	0.65
J_n	0.50
K_a	1.00
K_b	1.50
K_c	0.85

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q		24	46		58		69	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q		24	46		58		69	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width CP	20	7		25		30		ns	4.5	Fig. 7
t_{rem}	removal time K_b, K_c to CP	15	7		9		22		ns	4.5	Fig. 9; note 1
f_{max}	maximum clock pulse frequency	21	36		17		14		MHz	4.5	Fig. 7

Note to the characteristic table

1. From master preset mode to any other mode.

AC WAVEFORMS

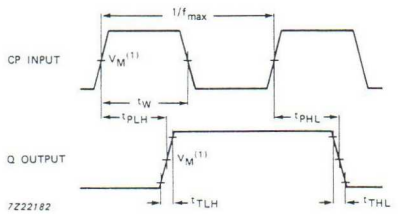


Fig. 7 Waveforms showing the clock (CP) to output (Q) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

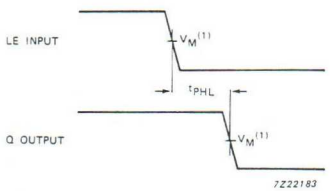


Fig. 8 Waveforms showing the LE input to Q output propagation delay.

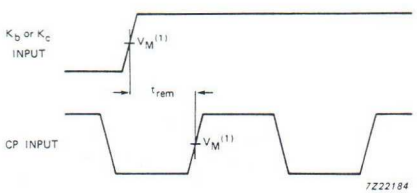


Fig. 9 Waveforms showing the K_b or K_c removal times, when the operating mode is switched from master preset to any other mode.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

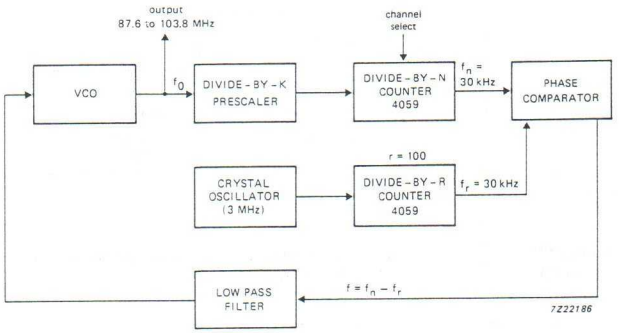


Fig. 10 Example showing the application of the PC74HC/HCT4059 in a phase-locked-loop (PL) for a FM band synthesizer.

Calculating the minimum and maximum divide-by-n values:

Output frequency range = 87.6 to 103.8 MHz (CCIR band 2)

Channel spacing frequency (f_c) = 300 kHz

Division factor prescaler (k) = 10

Reference frequency (f_r) =

$$\frac{f_c}{k} = \frac{300}{10} = 30 \text{ kHz}$$

Maximum divide-by-n value =

$$\frac{103.8 \text{ MHz}}{300 \text{ kHz}} = 346$$

Minimum divide-by-n value =

$$\frac{87.6 \text{ MHz}}{300 \text{ kHz}} = 292$$

Fixed divide-by-n value = $\frac{3 \text{ MHz}}{30 \text{ kHz}} = 100$

Application of the "4059" as divide-by-n counter allows programming of the channel spacing (shown in equations as 300 kHz). A channel in the CCIR band 2 is selected by the divide-by-n counter as follows:

channel = n – 290

Figure 11 shows a BCD switch compatible arrangement suitable for divide-by-5 and divide-by-8 modes, which can be adapted (with minimal changes) to the other divide-by-modes. In order to be able to preset to any number from 3 to 256 000, while preserving the BCD switch compatible character of the JAM inputs, a rather complex cascading scheme is necessary because the "4059" can never be preset to count less than 3. Logic circuitry is required to detect a condition where one of the numbers to be preset in the "4059" is < 3. In order to simplify the detection logic, only that condition is detected where the JAM inputs to terminals 6, 7 and 9 would be LOW during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2 000 times the divide-by-mode) and jams the same 2 000 into the "4059" by forcing pins 6, 7 and 9 HIGH.

The general circuit in Fig. 11 can be simplified considerably if the range of the cascaded counters do not start at a very low value.

Figure 12 shows an arrangement in the divide-by-4 mode, where the counting range extends in a BCD switch compatible manner from 99 003 to 114 999. The arrangement shown in Fig. 12 is easy to follow; once during every cycle the programmed digits are jammed in (15 616 in this example) and then a round number of 11 000 is jammed in, nine times in succession, by forcing the JAM inputs via AND/OR gates.

Numbers larger than the extended counter range can also be produced by cascading the PC74HC/HCT4059 with some other counting devices. Figure 13 shows such an arrangement where only one fixed divide-by number is desired. The dual flip-flop wired to produce a divide-by-3 count can be replaced by other counters such as the "190", "191", "192", "193", "4017", "4510" and "4516".

In Fig. 13 the divide-by-n sub-system is preset once to a number which represents the least significant digits of the divide-by number (15 690 in the example shown in Fig. 13). The sub-system is then preset twice to a round number (8 000 in the example shown in Fig. 13) and multiplied by the number of the divide-by mode (2 in the example shown in Fig. 13).

To verify:

15 690 + 2 x 8 000 x 2 = 47 690.

It is important that the second counting device has an output that is HIGH or LOW during only one of its counting states.

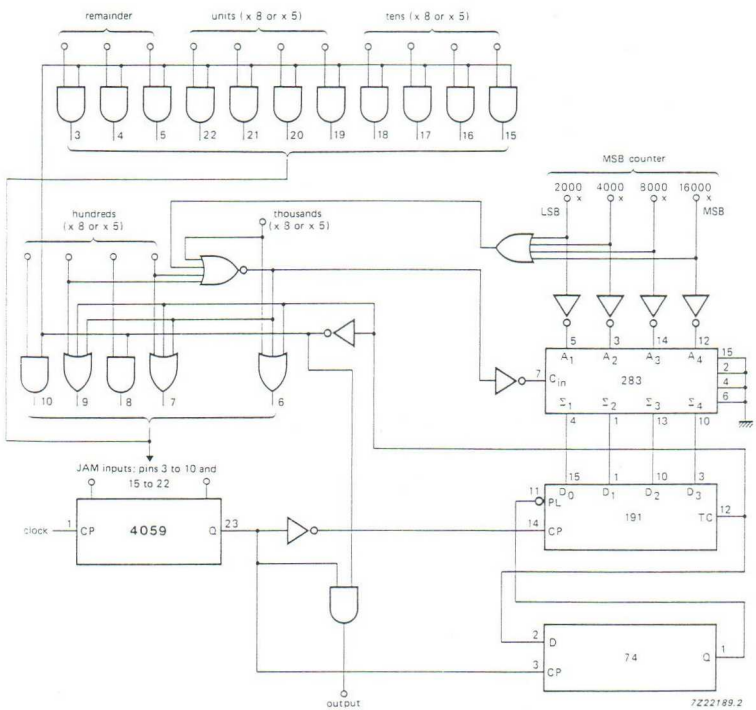


Fig. 11 BCD switch compatible divide-by-n system suitable for divide-by-5 and divide-by-8 mode. Divides by any number from 3 to 256 000.

Note to Fig. 11

Each AND gate is 1/4 of PC74HC/HCT08.
Each OR gate is 1/3 of PC74HC/HCT4075.
Each NOR gate is 1/2 of PC74HC/HCT4002.
Each inverter is 1/6 of PC74HC/HCT04.

APPLICATION INFORMATION (Cont'd)

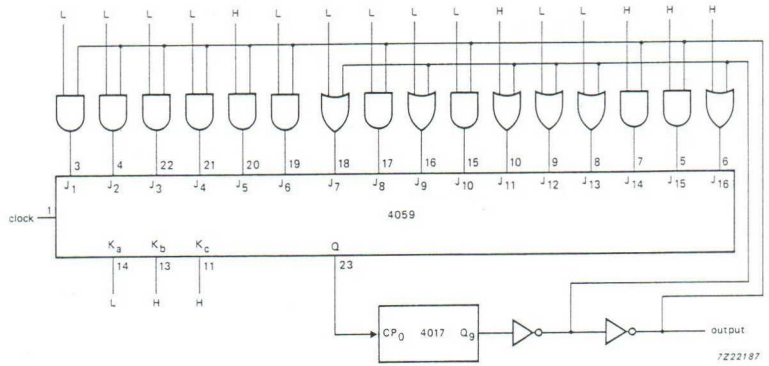


Fig. 12 Dividing-by any number from 99 003 to 114 999 (in this example n = 114 616).

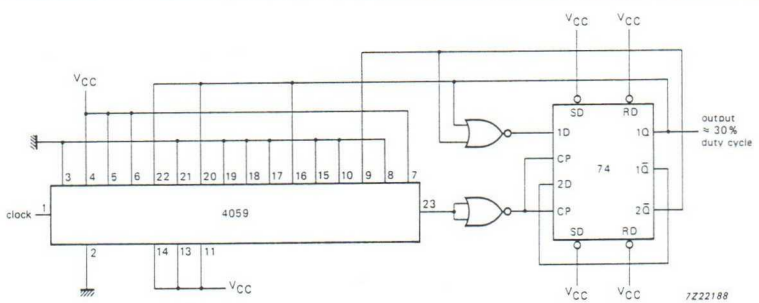


Fig. 13 Division by 47 690 in divide-by-2 mode.

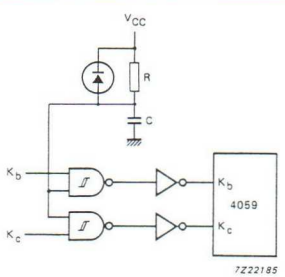


Fig. 14 External circuit for master preset at start-up.

Notes to Fig. 14

1. $RC \geqslant \frac{1}{0.2 \times f_{CP}\ (Hz)}$
2. It is assumed that the f_{CP} starts directly after the power-on. Any additional delay in starting f_{CP} must be added to the RC time.

14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR

FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay RS to Q_3	C_L = 15 pF, V_{CC} = 5 V	31	31	ns
	Q_n to Q_{n+1}		6	6	ns
t_{PHL}	MR to Q_n		17	18	ns
f_{max}	maximum clock frequency		87	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V
3. For formula on dynamic power dissipation see next page.

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q_{11} to Q_{13}	counter outputs
7, 5, 4, 6, 14, 13, 15	Q_3 to Q_9	counter outputs
8	GND	ground (0 V)
9	C_{TC}	external capacitor connection
10	R_{TC}	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V_{CC}	positive supply voltage

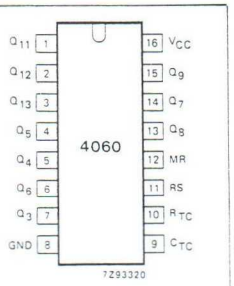


Fig. 1 Pin configuration.

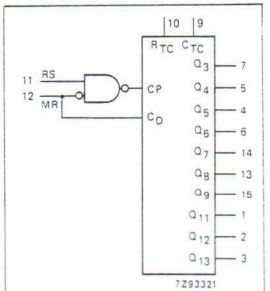


Fig. 2 Logic symbol.

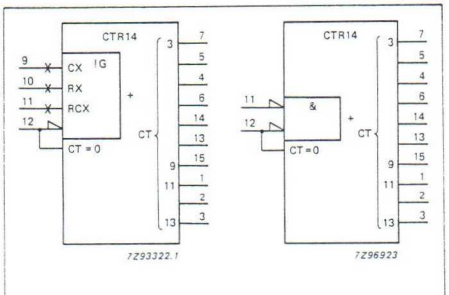


Fig. 3 IEC logic symbol.

DYNAMIC POWER DISSIPATION FOR 74HC

PARAMETER	V_{CC} V	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$
	6.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3\,800 \times V_{CC}$

GND = 0 V; T_{amb} = 25 °C

DYNAMIC POWER DISSIPATION FOR 74HCT

PARAMETER	V_{CC} V	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$

GND = 0 V; T_{amb} = 25 °C

Notes

1. Where: f_o = output frequency in MHz
   f_{osc} = oscillator frequency in MHz
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   C_t = timing capacitance in pF
   V_{CC} = supply voltage in V

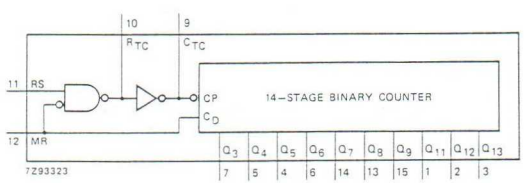


Fig. 4 Functional diagram.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

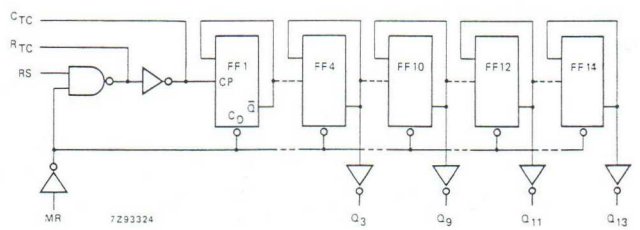


Fig. 5 Logic diagram.

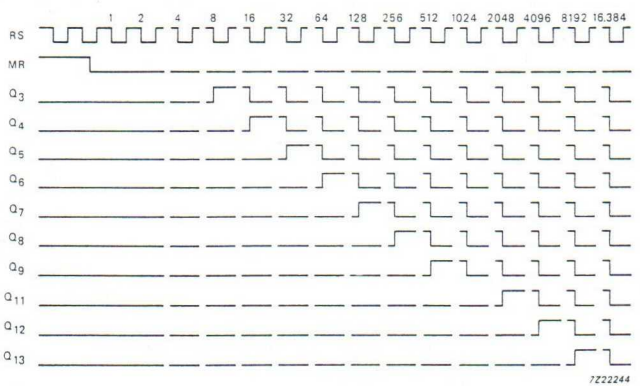


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

Output capability: standard (except for R_{TC} and C_{TC})
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} V	V_I	OTHER
V_{IH}	HIGH level input voltage MR input	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage MR input		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{IH}	HIGH level input voltage RS input	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage RS input			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage R_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=GND and MR=GND	$-I_O$ = 2.6 mA $-I_O$ = 3.3 mA
		3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 0.65 mA $-I_O$ = 0.85 mA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=GND and MR=GND	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{IH} and MR=V_{IL}	$-I_O$ = 3.2 mA $-I_O$ = 4.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4		4.5 6.0	RS=V_{CC} and MR=GND	I_O = 2.6 mA I_O = 3.3 mA
			0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	RS=V_{CC} and MR=GND	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage C_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	RS=V_{IL} and MR=V_{IH}	I_O = 3.2 mA I_O = 4.2 mA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OL}	LOW level output voltage except R_{TC} output		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay RS to Q_3		99 36 29	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		22 8 6	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}	propagation delay MR to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12
t_W	clock pulse width RS; HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t_W	master reset pulse width MR; HIGH	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
t_{rem}	removal time MR to RS	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 13
f_{max}	maximum clock pulse frequency	6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 12

DC CHARACTERISTICS FOR 74HCT

Output capability: standard (except for R_{TC} and C_{TC})
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		note 2
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		note 2
V_{OH}	HIGH level output voltage R_{TC} output	3.98			3.84		3.7		V	4.5	RS=GND and MR=GND	$-I_O$ = 2.6 mA
		3.98			3.84		3.7		V	4.5	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 0.65 mA
		4.4	4.5		4.4		4.4		V	4.5	RS=GND and MR=GND	$-I_O$ = 20 μA
		4.4	4.5		4.4		4.4		V	4.5	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98			3.84		3.7		V	4.5	RS=V_{IH} and MR=V_{IL}	$-I_O$ = 3.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26		0.33		0.4	V	4.5	RS=V_{CC} and MR=GND	I_O = 2.6 mA
			0	0.1		0.1		0.1	V	4.5	RS=V_{CC} and MR=GND	I_O = 20 μA
V_{OL}	LOW level output voltage C_{TC} output			0.26		0.33		0.4	V	4.5	RS=V_{IL} and MR=V_{IH}	I_O = 3.2 mA
V_{OL}	LOW level output voltage except R_{TC} output		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	

DC CHARACTERISTICS FOR 74HCT (continued)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Notes to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.
2. Only input MR (pin 12) has TTL input switching levels for the HCT versions.

INPUT	UNIT LOAD COEFFICIENT
MR	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay RS to Q_3		33	66		83		99	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}		8	16		20		24	ns	4.5	Fig. 14
t_{PHL}	propagation delay MR to Q_n		21	44		55		66	ns	4.5	Fig. 13
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 12
t_W	clock pulse width RS; HIGH or LOW	16	6		20		24		ns	4.5	Fig. 12
t_W	master reset pulse width MR; HIGH	16	6		20		24		ns	4.5	Fig. 13
t_{rem}	removal time MR to RS	26	13		33		39		ns	4.5	Fig. 13
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 12

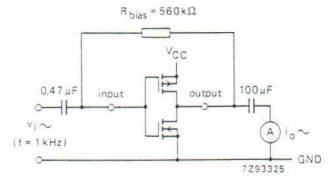


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_O/dv_i$ at v_O is constant (see also graph Fig. 8); MR = LOW.

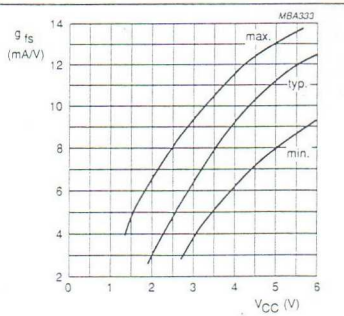


Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

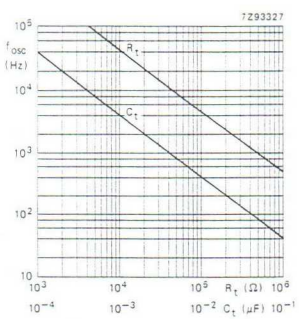


Fig. 9 RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2.0 to 6.0 V; T_{amb} = 25 °C.
C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.
R_t curve at C_t = 1 nF; R2 = 2 x R_t.

RC OSCILLATOR

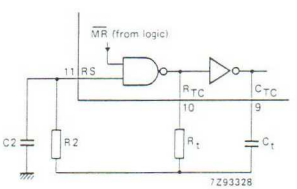


Fig. 10 Example of a RC oscillator.
Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

TIMING COMPONENT LIMITATIONS

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ 2R_t and R2C2 ≪ R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is 280 Ω at V_{CC} = 2.0 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6.0 V.
The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t > 50$ pF, up to any practical value,

10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, $R_t \geqslant 1$ kΩ.

TYPICAL CRYSTAL OSCILLATOR

In Fig. 11, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

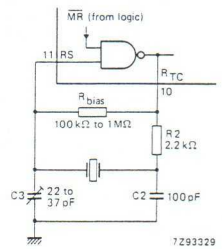


Fig. 11 External components connection for a crystal oscillator.

AC WAVEFORMS

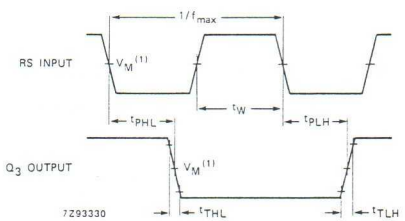


Fig. 12 Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

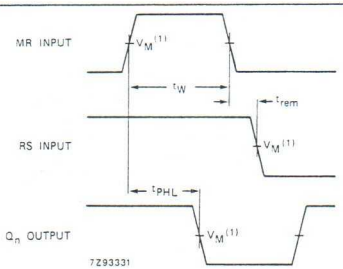


Fig. 13 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.

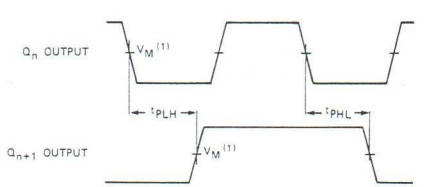


Fig. 14 Waveforms showing the output (Q_n) to Q_{n+1} propagation delays.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BILATERAL SWITCHES

FEATURES

- Very low "ON" resistance:
  50 Ω (typ.) at V_{CC} = 4.5 V
  45 Ω (typ.) at V_{CC} = 6.0 V
  35 Ω (typ.) at V_{CC} = 9.0 V
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4066" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4066 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The "4066" is pin compatible with the "4016" but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn-on time nE to V_{os}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 5 V	11	12	ns
t_{PHZ}/ t_{PLZ}	turn-off time nE to V_{os}		13	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	11	12	pF
C_S	max. switch capacitance		8	8	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1,5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
7	GND	ground (0 V)
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

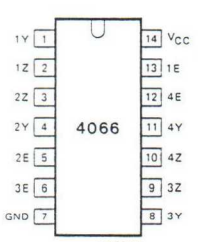


Fig. 1 Pin configuration.

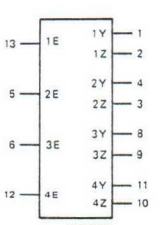
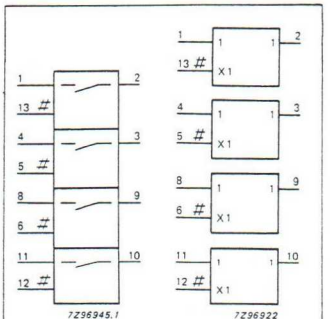


Fig. 2 Logic symbol.



(a) (b)

Fig. 3 IEC logic symbol.

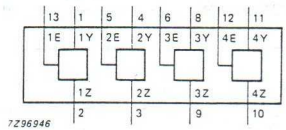


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUT nE	SWITCH
L	off
H	on

H = HIGH voltage level
L = LOW voltage level

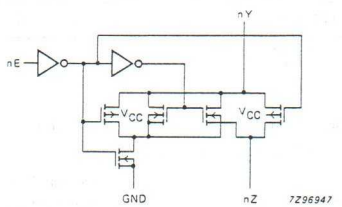


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to the Ratings

To avoid drawing V_{CC} current out of terminal nZ, when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT								V_{CC} V	I_S μA	V_{is}	V_I
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
R_{ON}	ON-resistance (peak)		– 54 42 32	– 95 84 70		– 118 105 88		– 142 126 105	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC} to GND	V_{IH} or V_{IL}
R_{ON}	ON-resistance (rail)		80 35 27 20	– 75 65 55		– 95 82 70		– 115 100 85	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND	V_{IH} or V_{IL}
R_{ON}	ON-resistance (rail)		100 42 35 27	– 80 75 60		– 106 94 78		– 128 113 95	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum variation of ON-resistance between any two channels		– 5 4 3						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V_{CC} to GND	V_{IH} or V_{IL}

Note to DC characteristics

1. At supply voltages approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

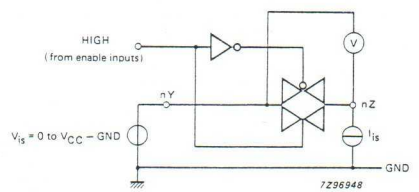


Fig. 6 Test circuit for measuring ON-resistance (R_{ON}).

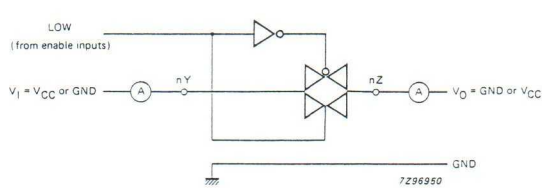


Fig. 7 Test circuit for measuring OFF-state current.

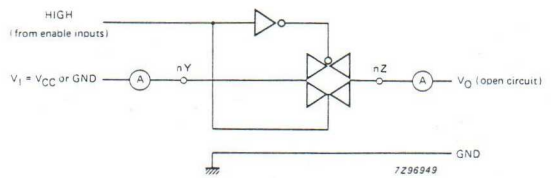


Fig. 8 Test circuit for measuring ON-state current.

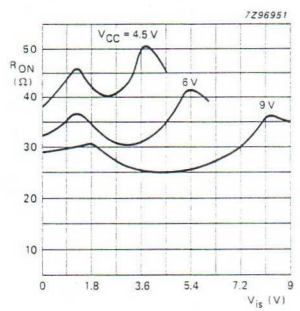


Fig. 9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}.

DC CHARACTERISTICS FOR 74HC

Voltage are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 8)
I_{CC}	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μA	6.0 10.0	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		8 3 2 2	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	$R_L = \infty$; C_L = 50 pF (see Fig. 17)
t_{PZH}/ t_{PZL}	turn-on time nE to V_{os}		36 13 10 8	100 20 17 13		125 25 21 16		150 30 26 20	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 18 and 19)
t_{PHZ}/ t_{PLZ}	turn-off time nE to V_{os}		44 16 13 16	150 30 26 24		190 38 33 16		225 45 38 20	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 18 and 19)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 8)
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	4.5 to 5.5	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} -2.1 V	other inputs at V_{CC} or GND

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nE	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		3	12		15		18	ns	4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 17)
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}		12	24		30		36	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18 and 19)
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}		20	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 18 and 19)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 15)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 15)
	switch "OFF" signal feed-through	−50 −50	dB dB	4.5 9.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Figs 10 and 16)
	crosstalk between any two switches	−60 −60	dB dB	4.5 9.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (nE, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 13)
f_{max}	minimum frequency response (−3 dB)	180 200	MHz MHz	4.5 9.0	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 11 and 14)
C_S	maximum switch capacitance	8	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

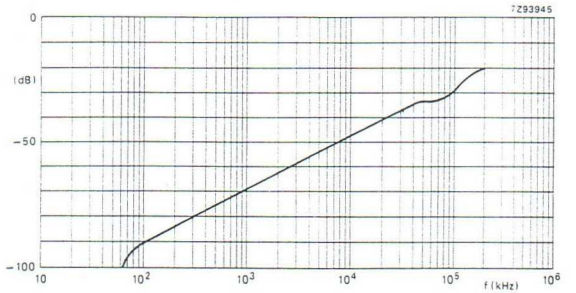


Fig. 10 Typical switch "OFF" signal feed-through as a function of frequency.

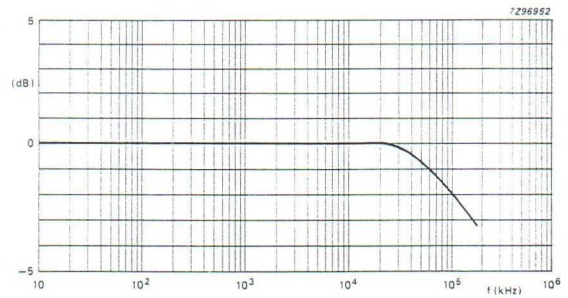


Fig. 11 Typical frequency response.

Note to Figs 10 and 11

Test conditions:
V_{CC} = 4.5 V; GND = 0 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

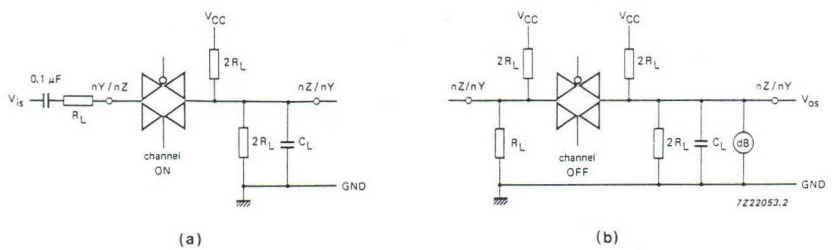


Fig. 12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

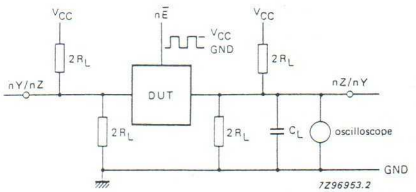
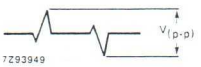


Fig. 13 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 13

The crosstalk is defined as follows (oscilloscope output):



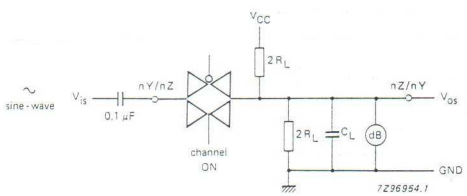


Fig. 14 Test circuit for measuring minimum frequency response.

Note to Fig. 14

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

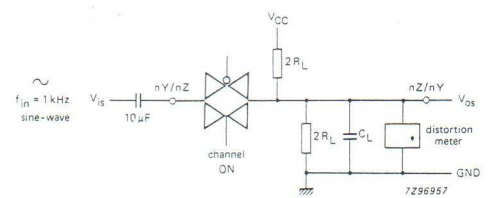


Fig. 15 Test circuit for measuring sine-wave distortion.

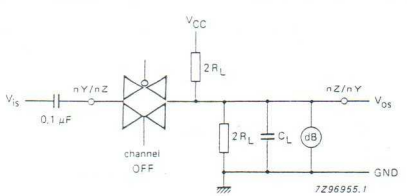


Fig. 16 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

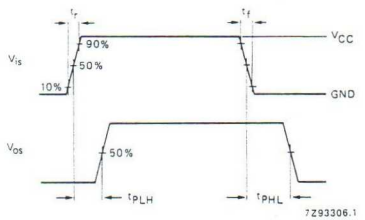


Fig. 17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

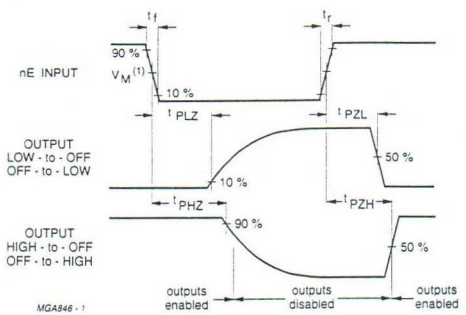
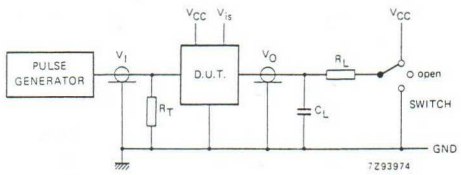


Fig. 18 Waveforms showing the turn-on and turn-off times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



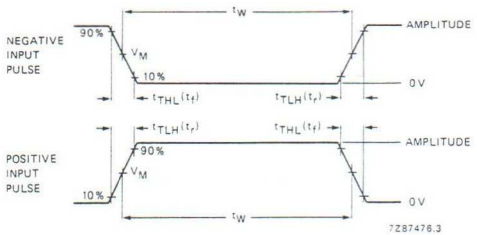


Fig. 20 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
others	open	pulse

Fig. 19 Test circuit for measuring AC performance.

Definitions for Figs 19 and 20:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance:
  80 Ω (typ.) at V_{CC} = 4.5 V
  70 Ω (typ.) at V_{CC} = 6.0 V
  60 Ω (typ.) at V_{CC} = 9.0 V
  typical "break before make" built-in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S_0 to S_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by S_0 to S_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_3.

The analog inputs/outputs (Y_0 to Y_{15}, and Z) can swing between V_{CC} as a positive limit and GND as a negative limit. V_{CC} to GND may not exceed 10 V.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PZH}	turn-on time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	26 29	32 33	ns ns
t_{PLZ}/ t_{PHZ}	turn-off time $\overline{E}$ to V_{OS} S_n to V_{OS}		27 29	26 30	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	29	29	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 45	5 45	pF pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} −1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

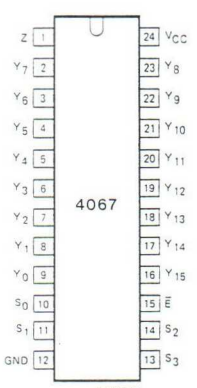


Fig. 1 Pin configuration.

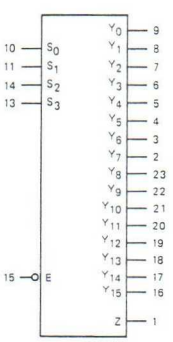


Fig. 2 Logic symbol.

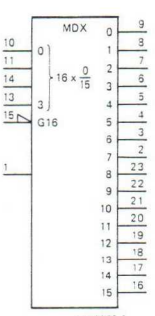


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Z	common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y_0 to Y_{15}	independent inputs/outputs
10, 11, 14, 13	S_0 to S_3	address inputs
12	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

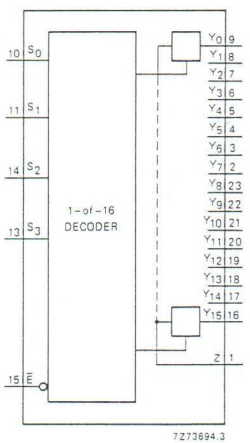


Fig. 4 Functional diagram.

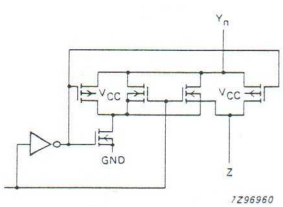


Fig. 5 Schematic diagram (one switch).

FUNCTION TABLE

INPUTS					CHANNEL ON
$\overline{E}$	S_3	S_2	S_1	S_0	
L	L	L	L	L	Y_0 – Z
L	L	L	L	H	Y_1 – Z
L	L	L	H	L	Y_2 – Z
L	L	L	H	H	Y_3 – Z
L	L	H	L	L	Y_4 – Z
L	L	H	L	H	Y_5 – Z
L	L	H	H	L	Y_6 – Z
L	L	H	H	H	Y_7 – Z
L	H	L	L	L	Y_8 – Z
L	H	L	L	H	Y_9 – Z
L	H	L	H	L	Y_{10} – Z
L	H	L	H	H	Y_{11} – Z
L	H	H	L	L	Y_{12} – Z
L	H	H	L	H	Y_{13} – Z
L	H	H	H	L	Y_{14} – Z
L	H	H	H	H	Y_{15} – Z
H	X	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

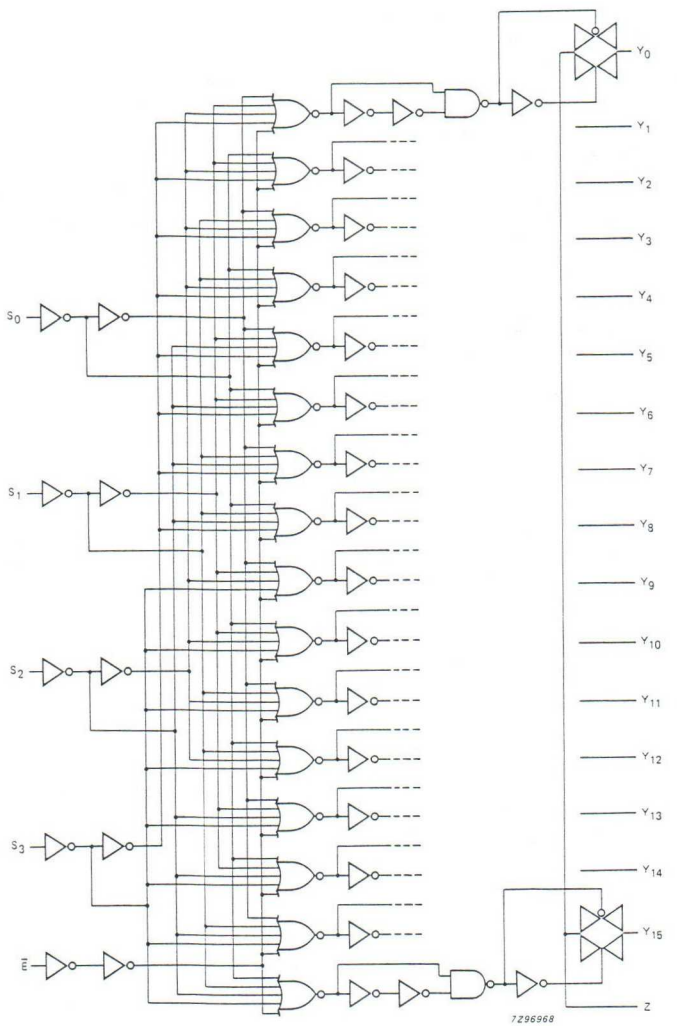


Fig. 6 Logic diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT											
		+25			–40 to +85		–40 to +125			V_{CC} V	I_S μA	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.					
R_{ON}	ON-resistance (peak)		– 110 95 75	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC} to GND	V_{IH} or V_{IL}
R_{ON}	ON-resistance (rail)		150 90 80 70	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND or V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum variation of ON-resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V_{CC} to GND	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – GND) approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 7.

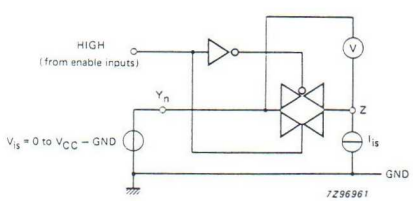


Fig. 7 Test circuit for measuring ON-resistance (R_{ON}).

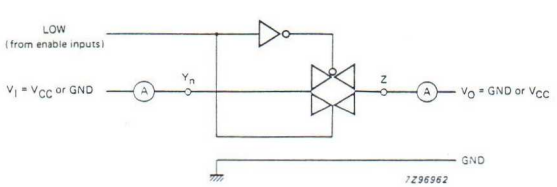


Fig. 8 Test circuit for measuring OFF-state current.

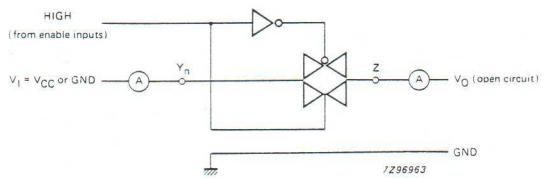


Fig. 9 Test circuit for measuring ON-state current.

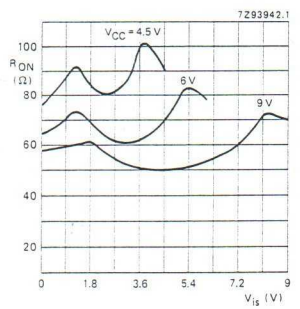


Fig. 10 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC} – GND.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 8)
$\pm I_S$	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 9)
$\pm I_S$	analog switch ON-state current			0.8		8.0		8.0	μA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 9)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160		160 320	μA	6.0 10.0	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}; Y_n to Z		25 9 7 5	75 15 13 9		95 19 16 11		110 22 19 14	ns	2.0 4.5 6.0 9.0	$R_L = \infty$; C_L = 50 pF (see Fig. 16)
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}; Z to Y_n		18 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	
t_{PHZ}/ t_{PLZ}	turn-off time $\overline{E}$ to Y_n		74 27 22 20	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Fig. 17)
t_{PHZ}/ t_{PLZ}	turn-off time S_n to Y_n		83 30 24 21	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0	
t_{PHZ}/ t_{PLZ}	turn-off time $\overline{E}$ to Z		85 31 25 24	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t_{PHZ}/ t_{PLZ}	turn-off time S_n to Z		94 34 27 25	290 58 47 45		365 73 62 56		435 87 74 68	ns	2.0 4.5 6.0 9.0	
t_{PZH}/ t_{PZL}	turn-on time $\overline{E}$ to Y_n		80 29 23 17	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t_{PZH}/ t_{PZL}	turn-on time S_n to Y_n		88 32 26 18	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0	
t_{PZH}/ t_{PZL}	turn-on time $\overline{E}$ to Z		85 31 25 18	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t_{PZH}/ t_{PZL}	turn-on time S_n to Z		94 34 27 19	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0	

Note to AC characteristics for 74HC

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 8)
$\pm I_S$	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 9)
$\pm I_S$	analog switch ON-state current			0.8		8.0		8.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ (see Fig. 9)
I_{CC}	quiescent supply current			8.0		80.0		160	μA	4.5 to 5.5	V_{CC} or GND	$V_{is} = GND$ or V_{CC}; $V_{os} = V_{CC}$ or GND
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} -2.1 V	other inputs at V_{CC} or GND

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}$	0.6
S_n	0.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}; Y_n to Z		9	15		19		22	ns	4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 16)
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}; Z to Y_n		6	12		15		18	ns	4.5	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ to Y_n		26	55		69		83	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 17)
t_{PHZ}/t_{PLZ}	turn-off time S_n to Y_n		31	55		69		83	ns	4.5	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ to Z		30	60		75		90	ns	4.5	
t_{PHZ}/t_{PLZ}	turn-off time S_n to Z		35	60		75		90	ns	4.5	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ to Y_n		32	60		75		90	ns	4.5	
t_{PZH}/t_{PZL}	turn-on time S_n to Y_n		35	60		75		90	ns	4.5	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ to Z		38	65		81		98	ns	4.5	
t_{PZH}/t_{PZL}	turn-on time S_n to Z		38	65		81		98	ns	4.5	

Note to the AC characteristics

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	4.5 9.0	note 1	R_L = 600 Ω; C_L = 50 pF f = 1 MHz (see Figs 11 and 15)
f_{max}	minimum frequency response (−3 dB)	90 100	MHz MHz	4.5 9.0	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 12 and 13)
C_S	maximum switch capacitance independent (Y) common (Z)	 5 45	 pF pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at Y_n or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at Y_n or Z terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

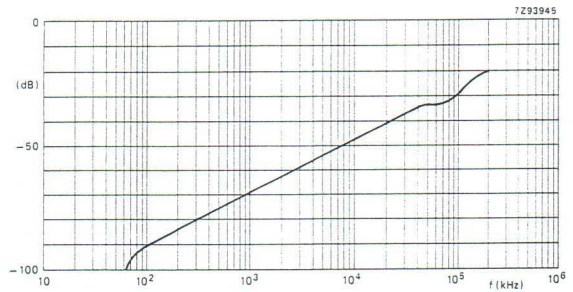


Fig. 11 Typical switch "OFF" signal feed-through as a function of frequency.

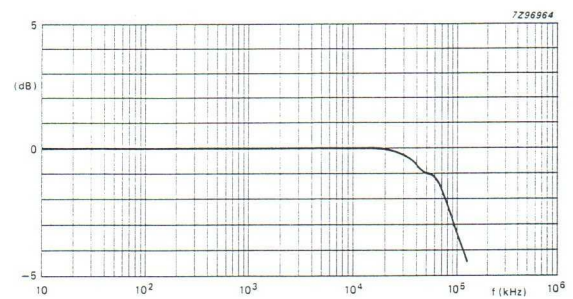


Fig. 12 Typical frequency response.

Note to Figs 11 and 12

Test conditions:
V_{CC} = 4.5 V; GND = 0 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

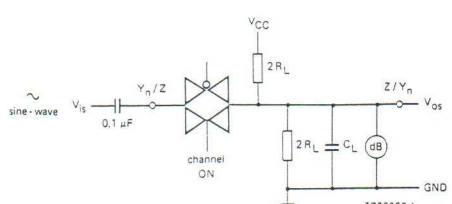


Fig. 13 Test circuit for measuring minimum frequency response.

Note to Fig. 13

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

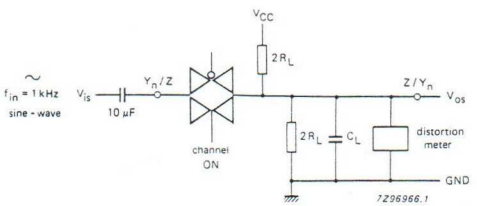


Fig. 14 Test circuit for measuring sine-wave distortion.

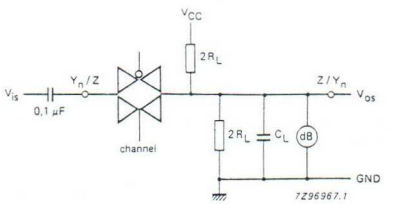


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

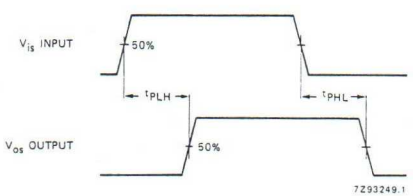


Fig. 16 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

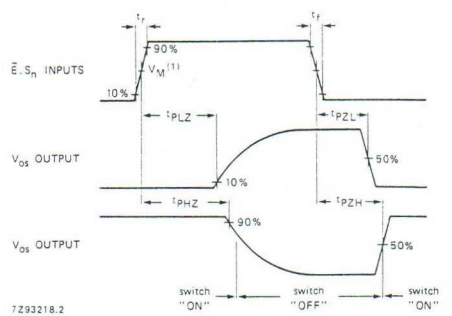
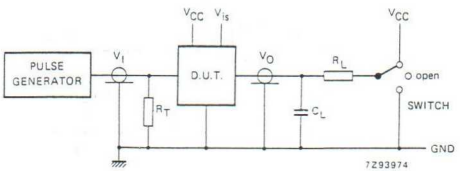


Fig. 17 Waveforms showing the turn-on and turn-off times.

Note to Fig. 17

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V_{is}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

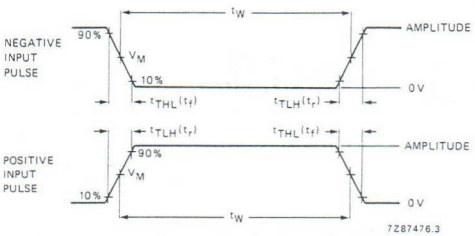


Fig. 19 Input pulse definitions.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

TRIPLE 3-INPUT OR GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the "4075" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4075 provide the 3-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	28	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	data inputs
4, 2, 12	1B to 3B	data inputs
5, 8, 13	1C to 3C	data inputs
6, 9, 10	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

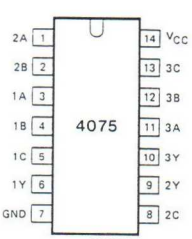


Fig. 1 Pin configuration.

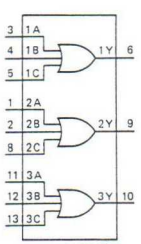


Fig. 2 Logic symbol.

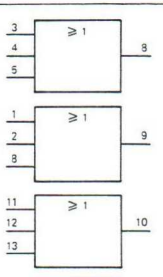


Fig. 3 IEC logic symbol.

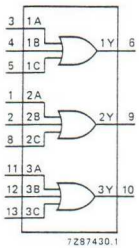


Fig. 4 Functional diagram.

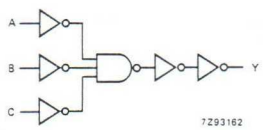


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY		12	24		30		36	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

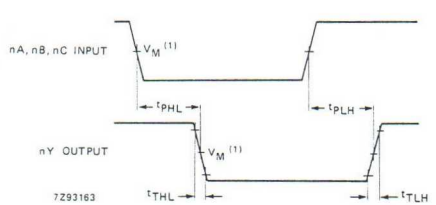


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES

- Ouput capability: standard
- I_{CC} catagory: MSI

GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS_1 and QS_2) are available for cascading a number of "4094" devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS_2 on the next negative-going clock edge and is for cascading "4094" devices when the clock rise time is slow.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to QS_1 CP to QS_2 CP to QP_n STR to QP_n	C_L = 15 pF V_{CC} = 5 V	 15 13 20 18	 19 18 21 19	 ns ns ns ns
f_{max}	maximum clock frequency		95	86	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	83	92	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	parallel outputs
8	GND	ground (0 V)
9, 10	QS_1, QS_2	serial outputs
15	OE	output enable input
16	V_{CC}	positive supply voltage

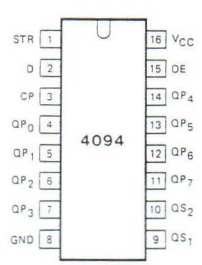


Fig. 1 Pin configuration.

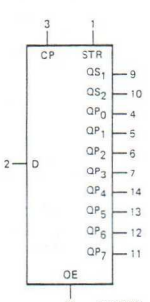


Fig. 2 Logic symbol.

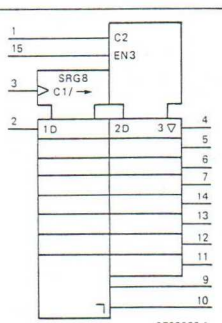


Fig. 3 IEC logic symbol.

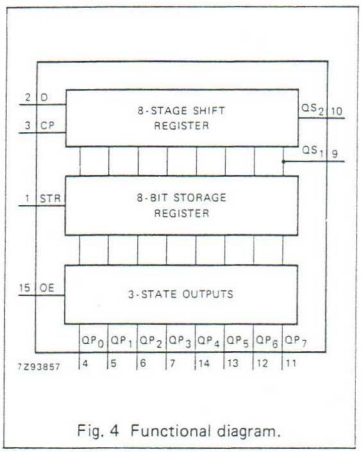


Fig. 4 Functional diagram.

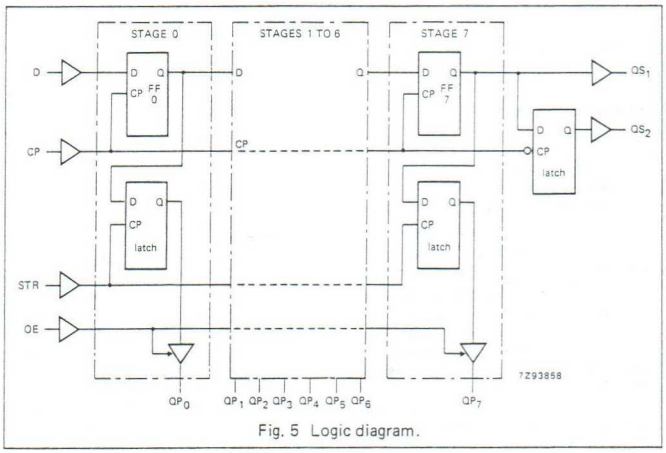


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge

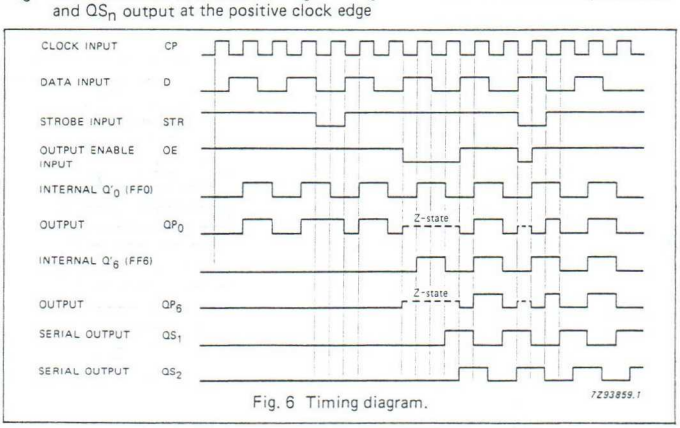


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	strobe pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time CP to STR	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D to CP	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time CP to STR	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	28 87 103		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE, CP	1.50
D	0.40
STR	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1		23	39		49		59	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2		21	36		45		54	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n		25	43		54		65	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n		22	39		49		59	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n		20	35		44		53	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n		21	35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
t_W	strobe pulse width HIGH	16	5		20		24		ns	4.5	Fig. 8
t_{su}	set-up time D to CP	10	4		13		15		ns	4.5	Fig. 10
t_{su}	set-up time CP to STR	20	9		25		30		ns	4.5	Fig. 8
t_h	hold time D to CP	4	0		4		4		ns	4.5	Fig. 10
t_h	hold time CP to STR	0	−4		0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

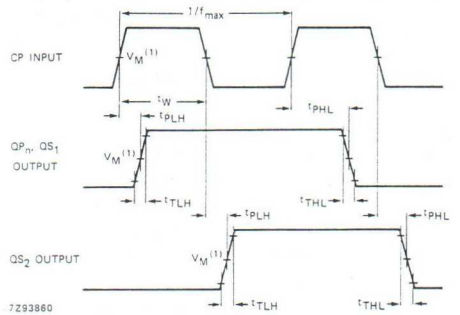


Fig. 7 Waveforms showing the clock (CP) to output (QP_n, QS_1, QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

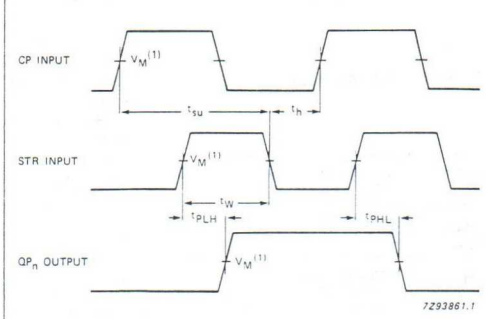


Fig. 8 Waveforms showing the strobe (STR) to output (QP_n) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

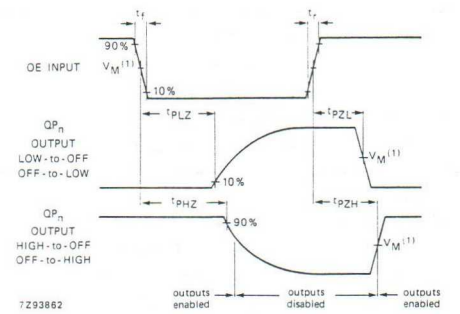


Fig. 9 Waveforms showing the 3-state enable and disable times for input OE.

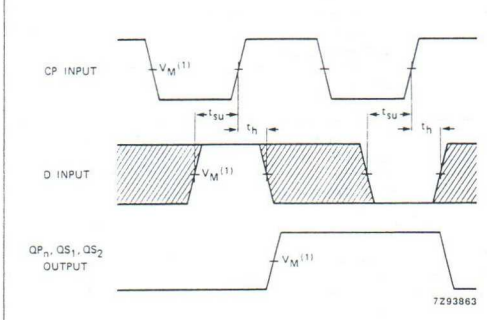


Fig. 10 Waveforms showing the data set-up and hold times for the data input (D).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance:
  160 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  120 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \geqslant (V_Y, V_Z) \geqslant V_{EE}$.
Inputs nY and nZ are electrically equivalent terminals.

V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT.
The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.
$V_{CC} - V_{EE}$ may not exceed 10.0 V.

See the "4016" for the version without logic level translation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}	turn "ON" time $\overline{E}$ to V_{OS} nS to V_{OS}	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	 19 16	 19 17	 ns ns
t_{PZL}	turn "ON" time $\overline{E}$ to V_{OS} nS to V_{OS}		 19 16	 24 21	 ns ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{OS} nS to V_{OS}		 20 16	 21 19	 ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	13	14	pF
C_S	max. switch capacitance		5	5	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

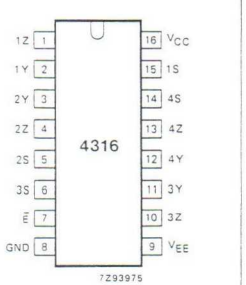


Fig. 1 Pin configuration.

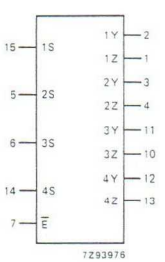


Fig. 2 Logic symbol.

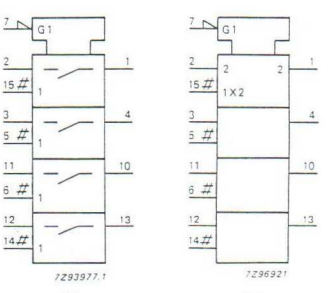


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
9	V_{EE}	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS		SWITCH
$\overline{E}$	nS	
L	L	off
L	H	on
H	X	off

H = HIGH voltage level
L = LOW voltage level
X = don't care

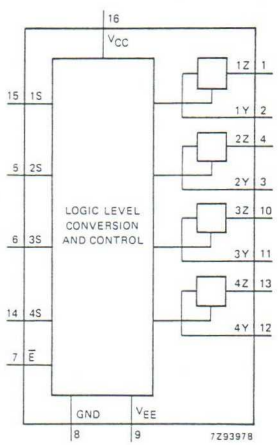


Fig. 4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

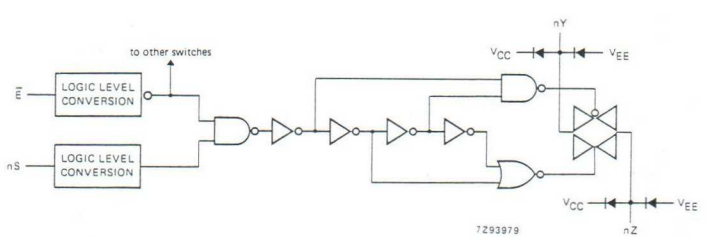


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminal Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

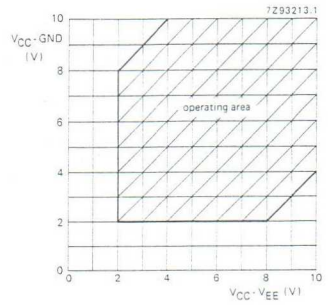


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4316.

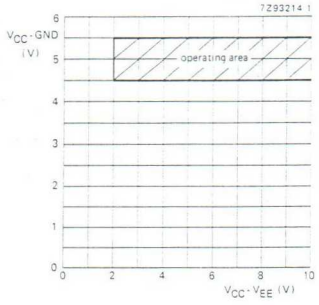


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4316.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND = 4.5 and 5.5 V; V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT								V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		+25			–40 to +85		–40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 160 120 85	– 320 240 170		– 400 300 215		– 480 360 255	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		160 80 70 60	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		170 90 80 65	– 180 160 135		– 225 200 170		– 270 240 205	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 16 9 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			–40 to +85		–40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_{EE} V	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		61 22 18 19	205 41 35 37		255 51 43 47		310 62 53 56	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PZH}/ t_{PZL}	turn "ON" time nS to V_{os}		52 19 15 17	175 35 30 34		220 44 37 43		265 53 45 51	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		63 23 18 21	220 44 37 39		275 55 47 49		330 66 56 59	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time nS to V_{os}		55 20 16 18	175 35 30 36		220 44 37 45		265 53 45 54	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1 V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nS	0.50
$\overline{E}$	0.50

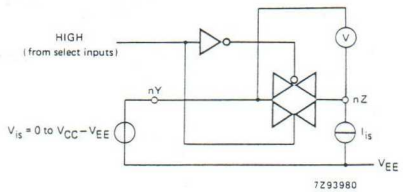


Fig. 8 Test circuit for measuring R_{ON}.

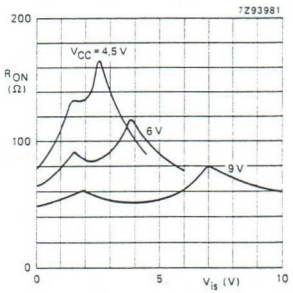


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC} − V_{EE}.

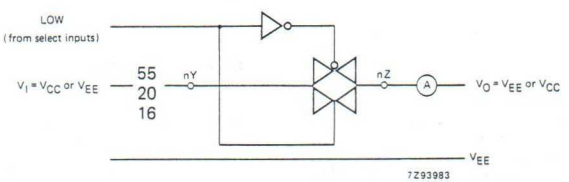


Fig. 10 Test circuit for measuring OFF-state current.

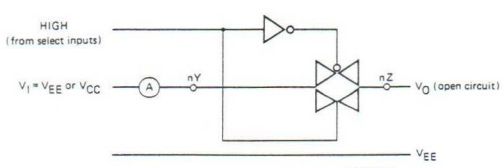


Fig. 11 Test circuit for measuring ON-state current.

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}	turn "ON" time $\overline{E}$ to V_{os}		22 21	44 42		55 53		66 63	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PZL}	turn "ON" time $\overline{E}$ to V_{os}		28 21	56 42		70 53		84 63	ns	4.5 4.5	0 −4.5	
t_{PZH}	turn "ON" time nS to V_{os}		20 17	40 34		53 43		60 51	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PZL}	turn "ON" time nS to V_{os}		25 17	50 34		63 43		75 51	ns	4.5 4.5	0 −4.5	
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os}		25 23	50 46		63 58		75 69	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time nS to V_{os}		22 20	44 40		55 50		66 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF (see Figs 12 and 15)
	crosstalk between any two switches	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz; (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or nS, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3 dB)	150 160	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance	5	pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

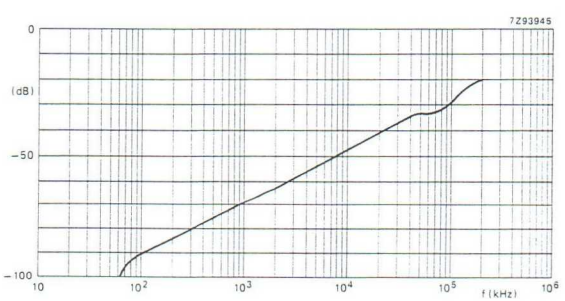
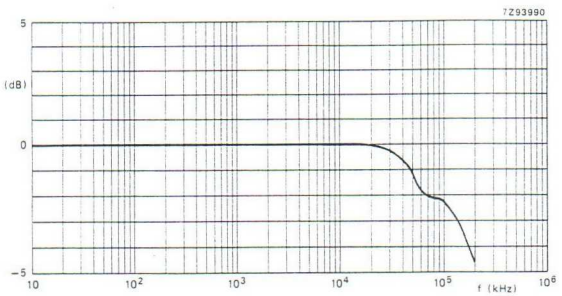


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

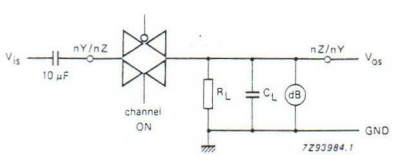


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

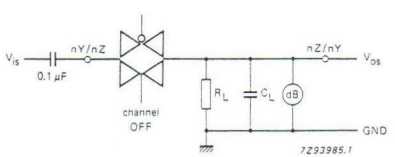


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

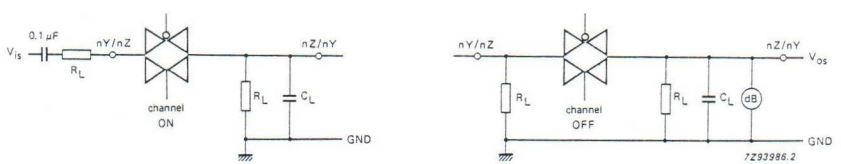


Fig. 16 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

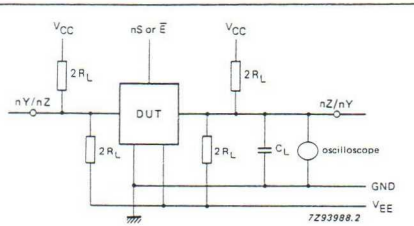
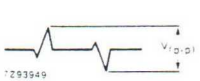


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

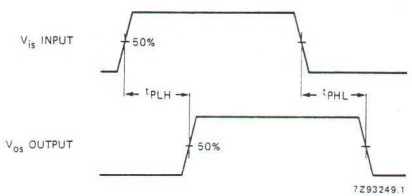


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

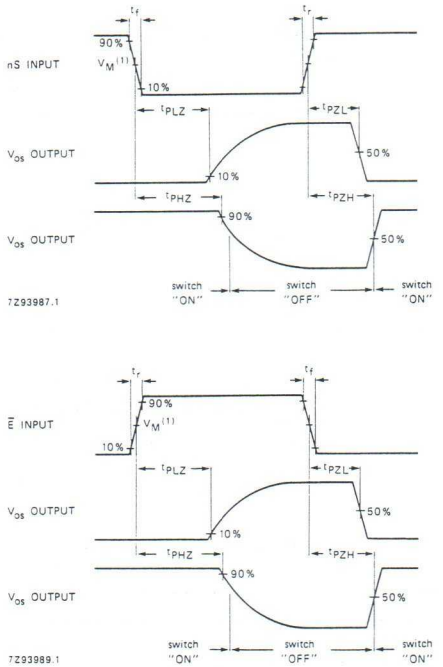


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Notes to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

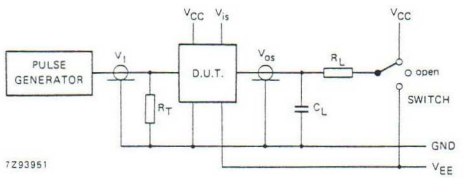


Fig. 20 Test circuit for measuring AC performance.

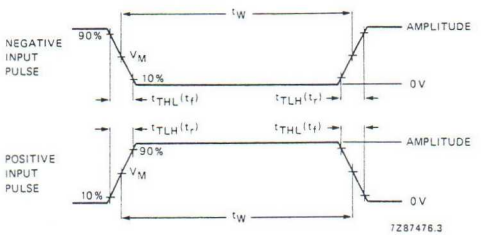


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4351 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4351 are 8-channel analog multiplexers/demultiplexers with three select inputs (S_0 to S_2), two enable inputs ($\overline{E}_1$ and E_2), a latch enable input ($\overline{LE}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With $\overline{E}_1$ LOW and E_2 is HIGH, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all 8 analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$, E_2 or S_n to V_{OS}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 5 V	27	35	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$, E_2 or S_n to V_{OS}		21	23	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	25	25	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 25	5 25	pF pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

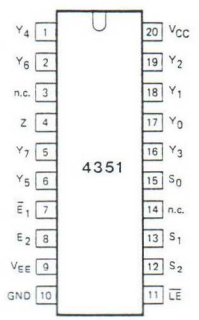
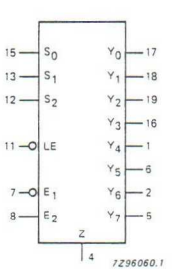


Fig. 1 Pin configuration.



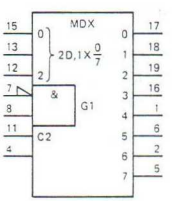


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4	Z	common
3, 14	n.c.	not connected
7	$\overline{E}_1$	enable input (active LOW)
8	E_2	enable input (active HIGH)
9	V_{EE}	negative supply voltage
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
15, 13, 12	S_0 to S_2	select inputs
17, 18, 19, 16, 1, 6, 2, 5	Y_0 to Y_7	independent inputs/outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS						CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_2	S_1	S_0	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	Y_0
L	H	H	L	L	H	Y_1
L	H	H	L	H	L	Y_2
L	H	H	L	H	H	Y_3
L	H	H	H	L	L	Y_4
L	H	H	H	L	H	Y_5
L	H	H	H	H	L	Y_6
L	H	H	H	H	H	Y_7
L	H	L	X	X	X	*
X	X	↓	X	X	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

APPLICATIONS

- **Analog multiplexing and demultiplexing**
- **Digital multiplexing and demultiplexing**
- **Signal gating**

GENERAL DESCRIPTION

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

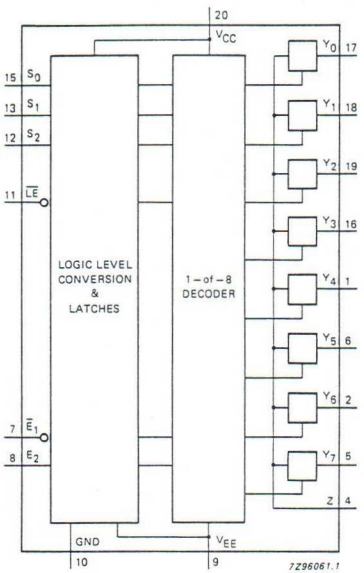


Fig. 4 Functional diagram.

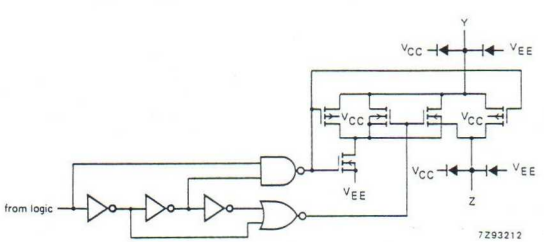


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

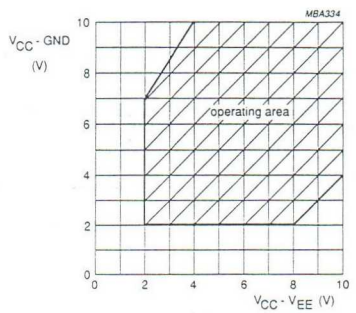


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4351.

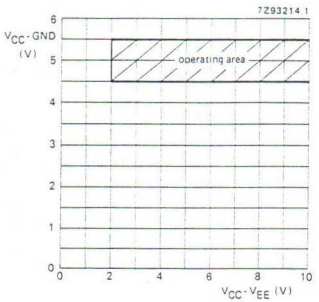


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4351.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT								V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (rail)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IN} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum ΔON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_{EE} V	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = ∞; C_L = 50 pF (see Fig. 17)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$ to V_{os}		85 31 25 28	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time E_2 to V_{os}		85 31 25 25	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{LE}$ to V_{os}		91 33 26 27	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		88 32 26 25	300 60 51 50		375 75 64 63		450 90 77 75	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$ to V_{os}		69 25 20 20	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time E_2 to V_{os}		72 26 21 19	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{LE}$ to V_{os}		83 30 24 26	275 55 47 45		345 69 59 56		415 83 71 68	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		80 29 23 24	275 55 47 48		345 69 59 60		415 83 71 72	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{su}	set-up time S_n to $\overline{LE}$	60 12 10 18	17 6 5 9			75 15 13 23		90 18 15 27	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_h	hold time S_n to $\overline{LE}$	5 5 5 5	–8 –3 –2 –4			5 5 5 5		5 5 5 5	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_W	$\overline{LE}$ minimum pulse width HIGH	100 20 17 25	11 1 3 7			125 25 21 31		150 30 26 38	ns	2.0 4.5 6.0 4.5	0 0 0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}_1$, E_2	0.50
S_n	0.50
$\overline{LE}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 17)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$ to V_{os}		40 31	75 60		94 75		113 90	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time E_2 to V_{os}		35 26	70 50		88 63		105 75	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{LE}$ to V_{os}		42 37	75 60		94 75		113 90	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		39 30	75 60		94 75		113 90	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$ to V_{os}		27 20	55 40		69 50		83 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time E_2 to V_{os}		32 26	60 50		75 63		90 75	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{LE}$ to V_{os}		33 30	60 55		75 69		90 83	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		33 29	65 55		81 69		98 83	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 18)
t_{su}	set-up time S_n to $\overline{LE}$	12 14	6 7			15 18		18 21	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_h	hold time S_n to $\overline{LE}$	5 5	−1 −2			5 5		5 5	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_W	$\overline{LE}$ minimum pulse width HIGH	25 25	13 13			31 31		38 38	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)

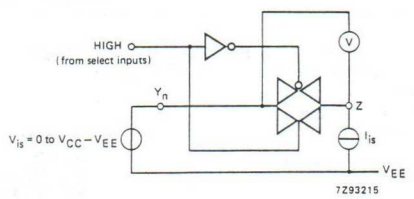


Fig. 8 Test circuit for measuring R_{ON}.

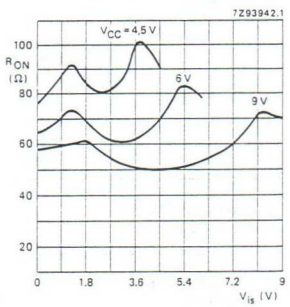


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC} − V_{EE}.

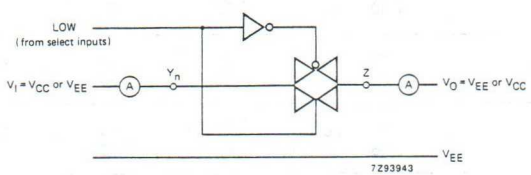


Fig. 10 Test circuit for measuring OFF-state current.

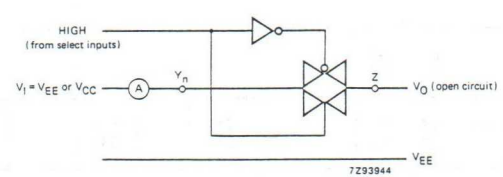


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF (see Figs 12 and 15)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	120 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}_1$, $\overline{E}_2$ or S_n, square-wave between V_{CC} and GND, t_r = t_f = 6 ns) (see Fig. 16)
f_{max}	minimum frequency response (−3dB)	160 170	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 25	pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

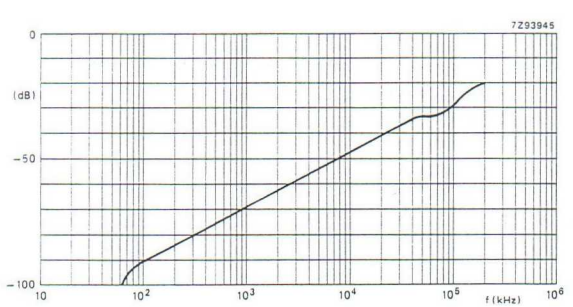
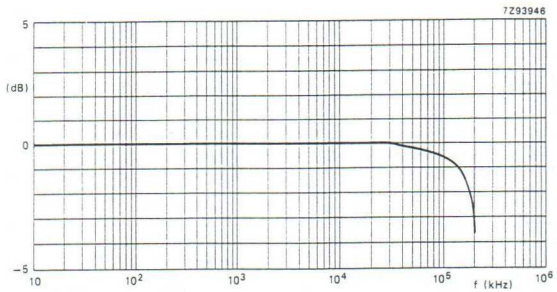


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

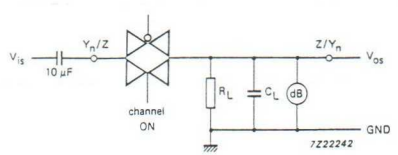


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

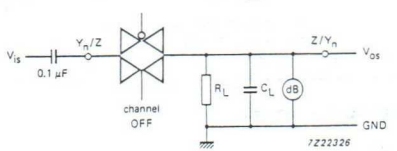


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

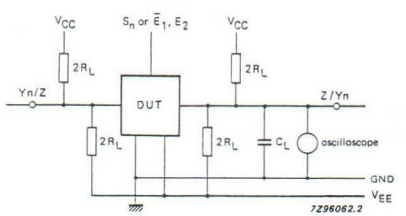
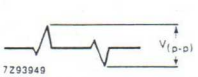


Fig. 16 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 16

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

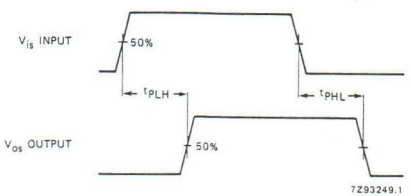


Fig. 17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

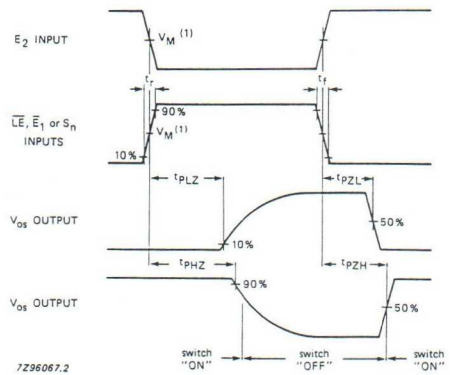


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

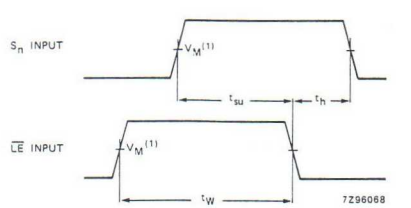


Fig. 19 Waveforms showing the set-up and hold times from S_n inputs to $\overline{LE}$ input, and minimum pulse width of $\overline{LE}$.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

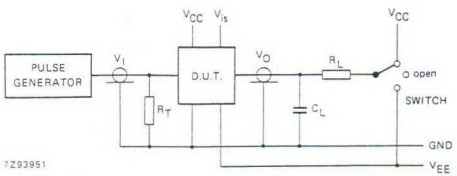


Fig. 20 Test circuit for measuring AC performance.

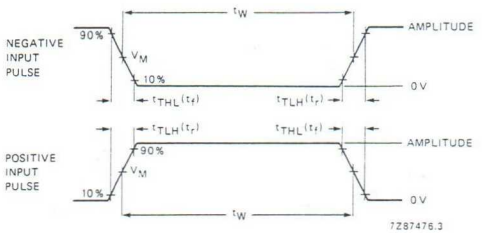


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	$t_r; t_f$	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4352 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ).

The common channel select logics include two select inputs (S_0 and S_1), an active LOW enable input ($\overline{E}_1$), an active HIGH enable input (E_2) and a latch enable input ($\overline{LE}$).

With $\overline{E}_1$ LOW and E_2 HIGH, one of the four switches is selected (low impedance ON-state) by S_0 and S_1. The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$, E_2 or S_n to V_{os}	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	31	33	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$, E_2 or S_n to V_{os}		20	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	55	55	pF
C_S	max. switch capacitance independent (Y) common (Z)		 5 12	 5 12	 pF pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

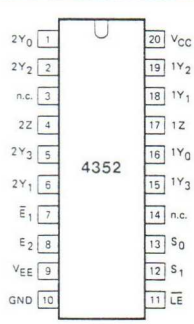


Fig. 1 Pin configuration.

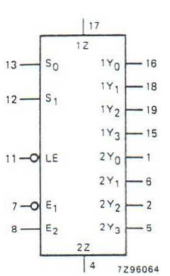


Fig. 2 Logic symbol.

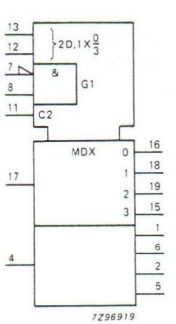


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 6, 2, 5	$2Y_0$ to $2Y_3$	independent inputs/outputs
3, 14	n.c.	not connected
7	$\overline{E}_1$	enable input (active LOW)
8	E_2	enable input (active HIGH)
9	V_{EE}	negative supply voltage
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
13, 12	S_0, S_1	select inputs
16, 18, 19, 15	$1Y_0$ to $1Y_3$	independent inputs/outputs
17, 4	1Z, 2Z	common inputs/outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS					CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_1	S_0	
H	X	X	X	X	none
X	L	X	X	X	none
L	H	H	L	L	$nY_0 - nZ$
L	H	H	L	H	$nY_1 - nZ$
L	H	H	H	L	$nY_2 - nZ$
L	H	H	H	H	$nY_3 - nZ$
L	H	L	X	X	*
X	X	↓	X	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0, S_1, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

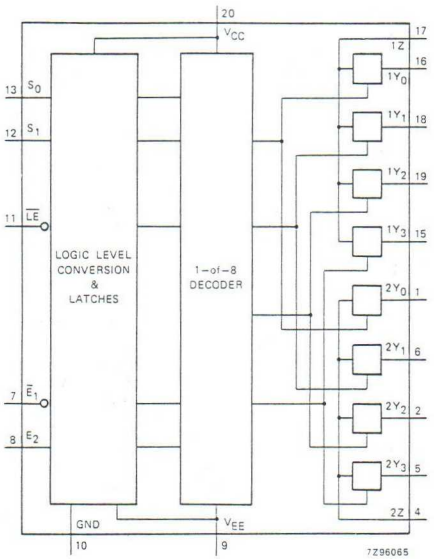


Fig. 4 Functional diagram.

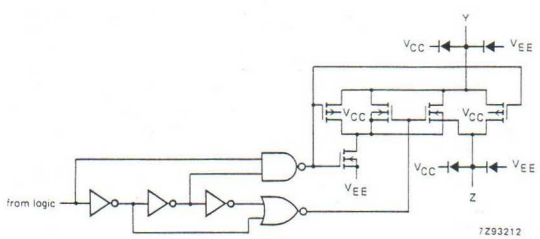


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 6 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

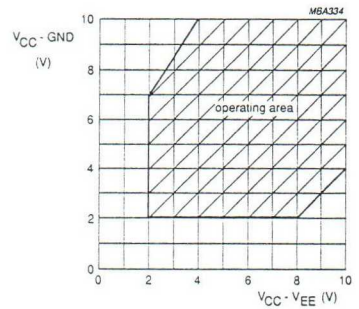


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4352.

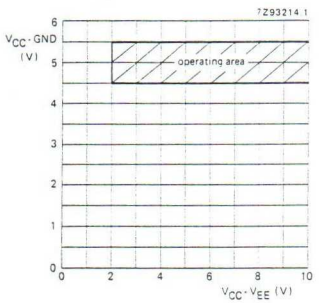


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4352.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT												
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IN} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 –4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 5	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}_1$; E_2 to V_{os} $\overline{LE}$ to V_{os}		99 36 29 25	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/t_{PZL}	turn "ON" time S_n to V_{os}		99 36 29 25	325 65 55 46		405 81 69 58		490 98 80 69	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}_1$; E_2 to V_{os} $\overline{LE}$ to V_{os}		58 21 17 21	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/t_{PLZ}	turn "OFF" time S_n to V_{os}		63 23 18 24	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{su}	set-up time S_n to $\overline{LE}$	90 18 15 18	17 6 5 9		115 23 20 23		135 27 23 27		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_h	hold time S_n to $\overline{LE}$	5 5 5 5	−6 −2 −2 −3		5 5 5 5		5 5 5 5		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_W	$\overline{LE}$ minimum pulse width HIGH	80 16 14 16	11 4 3 4		100 20 17 20		120 24 20 24		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1 V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}_1$, E_2	0.50
S_n	0.50
$\overline{LE}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			–40 to +85		–40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		6 5	12 8		15 10		18 12	ns	4.5 4.5	0 –4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$; E_2 to V_{os} $\overline{LE}$ to V_{os}		38 28	65 46		81 58		98 69	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		38 27	65 46		81 58		98 69	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$ to V_{os} $\overline{LE}$ to V_{os}		20 20	40 40		50 50		60 60	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_2$, S_n to V_{os}		25 25	43 43		54 54		65 65	ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{su}	set-up time S_n to $\overline{LE}$	16 18	7 9		20 23		24 27		ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_h	hold time S_n to $\overline{LE}$	5 5	–1 –1		5 5		5 5		ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_W	$\overline{LE}$ minimum pulse width HIGH	16 16	3 4		20 20		24 24		ns	4.5 4.5	0 –4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)

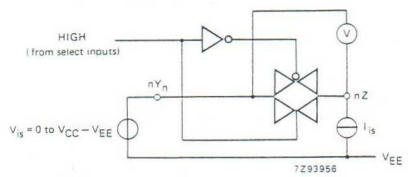


Fig. 8 Test circuit for measuring R_{ON}.

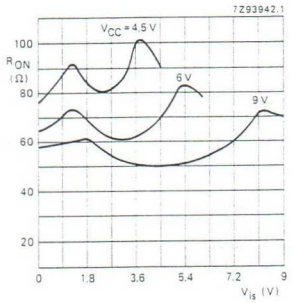


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

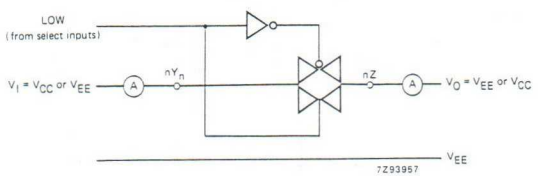


Fig. 10 Test circuit for measuring OFF-state current.

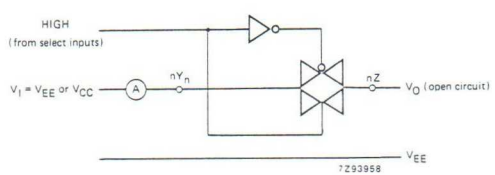


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\bar{E}_1$, $\bar{E}_2$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3dB)	160 170	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

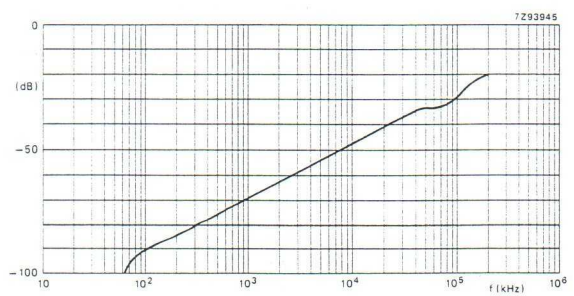
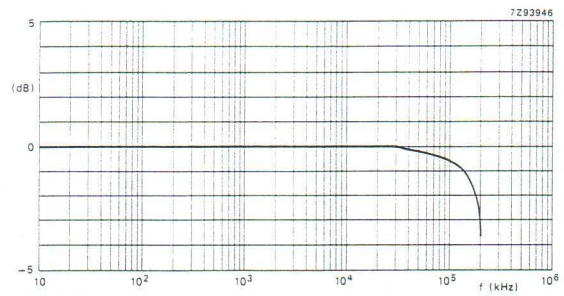


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

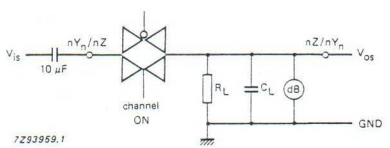


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

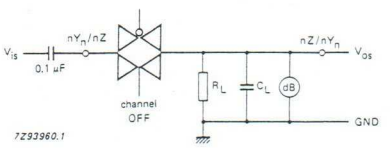


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

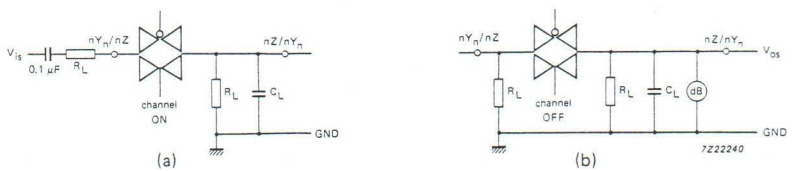


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

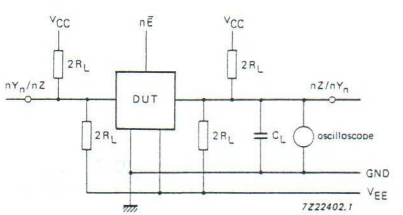
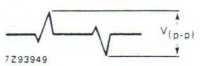


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

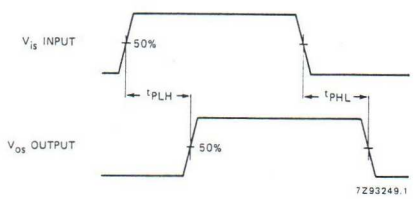


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

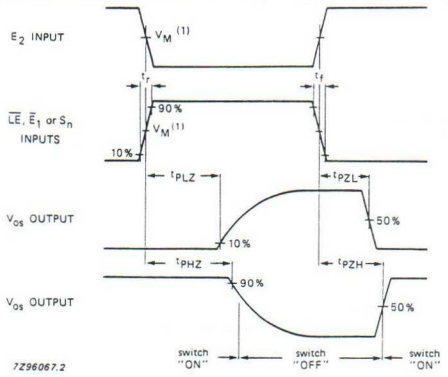


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

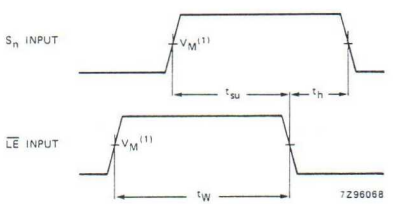


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to $\overline{LE}$ input, and minimum pulse width of $\overline{LE}$.

Note to Fig. 20

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

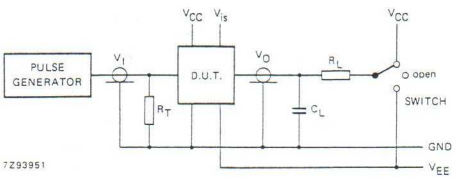


Fig. 21 Test circuit for measuring AC performance.

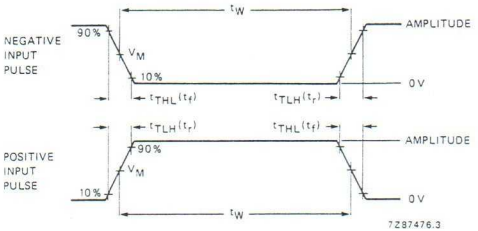


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance:
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4353 are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4353 are triple 2-channel analog multiplexers/demultiplexers with two common enable inputs ($\overline{E}_1$ and E_2) and a latch enable input ($\overline{LE}$). Each multiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and select inputs (S_1 to S_3).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$, E_2 or S_n to V_{os}	C_L = 50 pF; R_L = 1 kΩ; V_{CC} = 5 V	29	21	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$, E_2 or S_n to V_{os}		20	22	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	23	23	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 8	5 8	pF pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

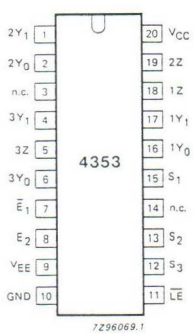


Fig. 1 Pin configuration.

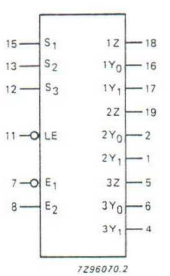


Fig. 2 Logic symbol.

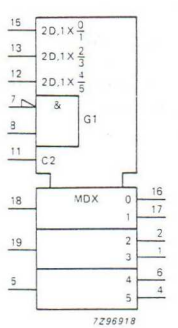


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	$2Y_0$, $2Y_1$	independent inputs/outputs
5	3Z	common input/output
6, 4	$3Y_0$, $3Y_1$	independent inputs/outputs
3, 14	n.c.	not connected
7	$\overline{E}_1$	enable input (active LOW)
8	E_2	enable input (active HIGH)
9	V_{EE}	negative supply voltage
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
15, 13, 12	S_1 to S_3	select inputs
16, 17	$1Y_0$, $1Y_1$	independent inputs/outputs
18	1Z	common input/output
19	2Z	common input/output
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}_1$	E_2	$\overline{LE}$	S_n	
H	X	X	X	none
X	L	X	X	none
L	H	H	L	nY_0 – nZ
L	H	H	H	nY_1 – nZ
L	H	L	X	*
X	X	↓	X	**

H = HIGH voltage level
L = LOW voltage level
X = don't care
↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".
** Selected channels latched.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY_0 and nY_1) and the other side connected to a common input/output (nZ).

With $\overline{E}_1$ LOW and E_2 HIGH, one of the two switches is selected (low impedance ON-state) by S_1 to S_3.
The data at the select inputs may be latched by using the active LOW latch enable input ($\overline{LE}$). When $\overline{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\overline{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1 to S_3, $\overline{LE}$, $\overline{E}_1$ and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 and nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

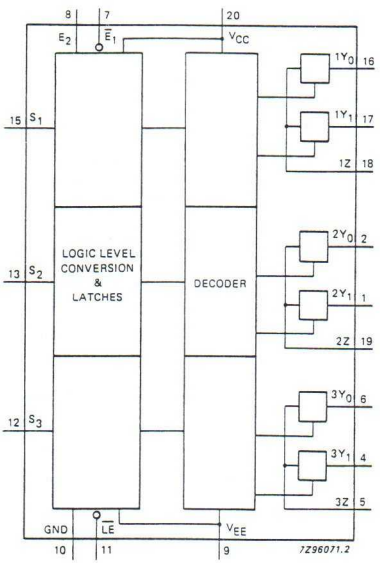


Fig. 4 Functional diagram.

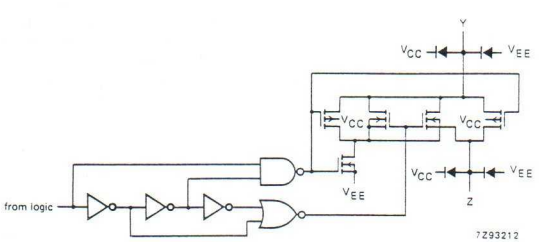


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

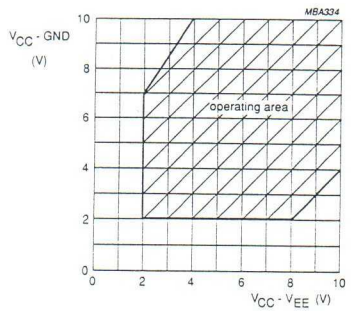


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4353.

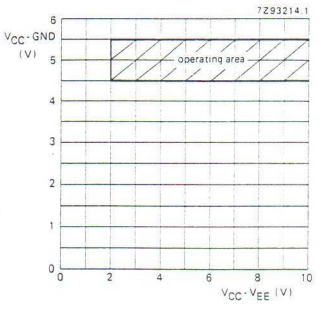


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4353.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC/HCT								V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R_{ON}	ON resistance (peak)		– 100 90 70	– 180 160 130		– 225 200 165		– 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IN} or V_{IL}
R_{ON}	ON resistance (rail)		150 80 70 60	– 140 120 105		– 175 150 130		– 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}
R_{ON}	ON resistance		150 90 80 65	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum Δ ON resistance between any two channels		– 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 −4.5		V_{CC} to V_{EE}	V_{IH} or V_{IL}

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC								V_{CC} V	V_{EE} V	V_I	OTHER
		+25			–40 to +85		–40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$; E_2 to V_{os}		61 22 18 18	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{CE}$ to V_{os}		55 20 16 17	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		61 22 18 17	225 45 38 40		280 56 48 50		340 68 58 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$; E_2 to V_{os}		66 24 19 19	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}; $\overline{CE}$ to V_{os}		55 20 16 19	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{su}	set-up time S_n to $\overline{CE}$	60 12 10 18	17 6 5 8		75 15 13 23		90 18 15 27		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_h	hold time S_n to $\overline{CE}$	5 5 5 5	−6 −2 −2 −3		5 5 5 5		5 5 5 5		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_W	$\overline{CE}$ minimum pulse width HIGH	80 16 14 16	11 4 3 6		100 20 17 20		120 24 20 24		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} =$ V_{CC} or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} −2.1 V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}_1$, E_2	0.50
S_n	0.50
$\overline{LE}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_{EE} V	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}_1$ to V_{os}		26 22	55 45		69 56		83 68	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time E_2 to V_{os}		22 18	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{LE}$ to V_{os}		21 17	45 40		56 50		68 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PZH}/ t_{PZL}	turn "ON" time S_n to V_{os}		25 19	50 45		63 56		75 68	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}_1$ to V_{os}		23 19	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time E_2 to V_{os}		27 23	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{LE}$ to V_{os}		19 19	40 40		50 50		60 60	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{PHZ}/ t_{PLZ}	turn "OFF" time S_n to V_{os}		22 22	45 45		56 56		68 68	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 19)
t_{su}	set-up time S_n to $\overline{LE}$	12 15	7 9		15 19		18 22		ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_h	hold time S_n to $\overline{LE}$	5 5	0 −2		5 5		5 5		ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)
t_W	$\overline{LE}$ minimum pulse width HIGH	16 16	3 5		20 20		24 24		ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Fig. 20)

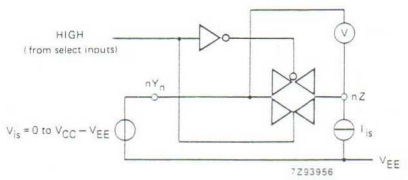


Fig. 8 Test circuit for measuring R_{ON}.

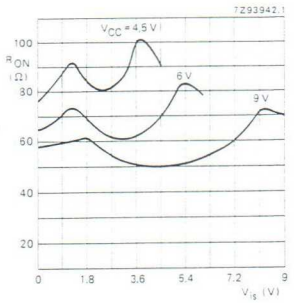


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC} − V_{EE}.

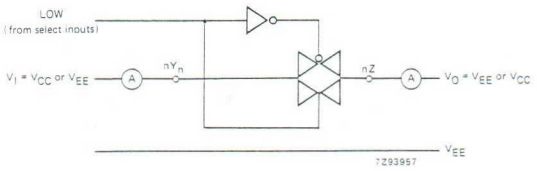


Fig. 10 Test circuit for measuring OFF-state current.

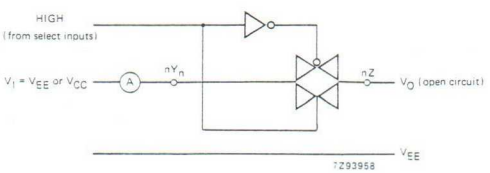


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}_1$, $\overline{E}_2$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3dB)	160 170	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

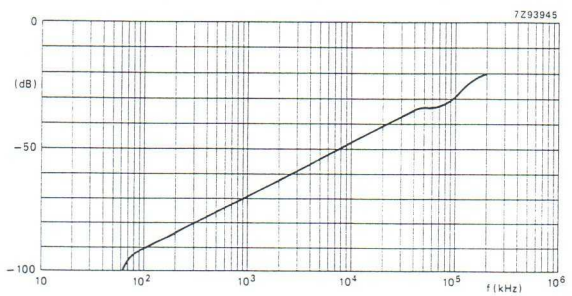
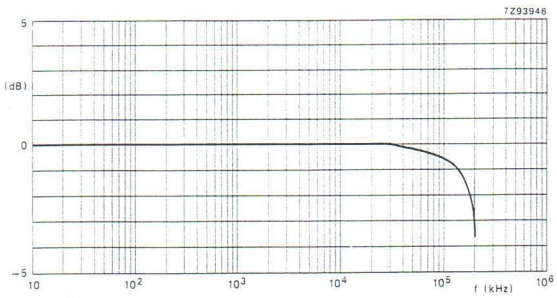


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

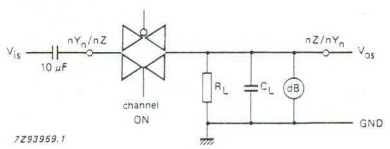


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

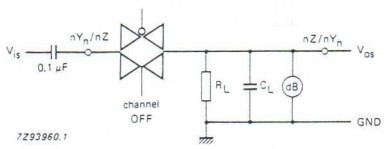


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

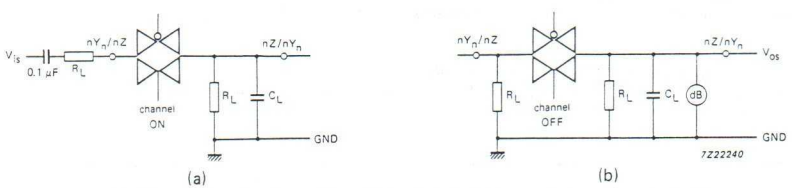


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

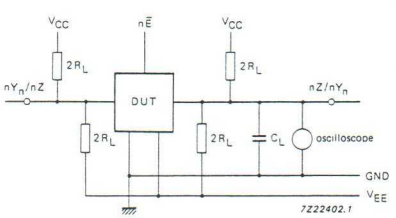


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):

AC WAVEFORMS

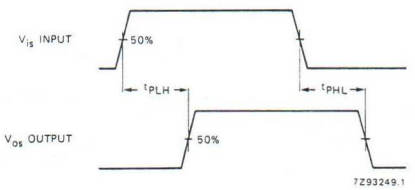


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

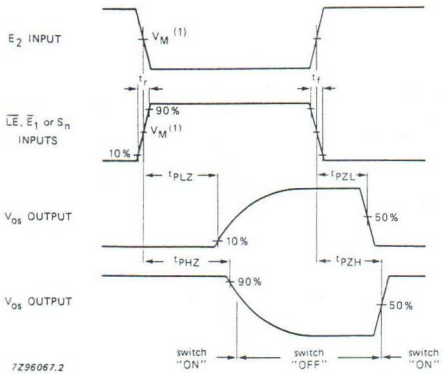


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

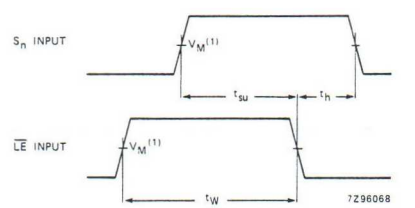


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to $\overline{LE}$ input, and minimum pulse width of $\overline{LE}$.

Note to Fig. 20

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

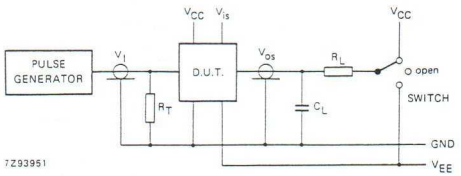


Fig. 21 Test circuit for measuring AC performance.

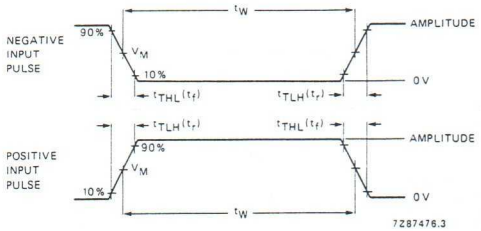


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

BCD UP/DOWN COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the "4510" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D_0 to D_3), four parallel outputs (Q_0 to Q_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q_0 and Q_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q_0 to Q_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \cdot \{ (UP/\overline{DN}) \cdot Q_0 \cdot Q_3 + \overline{(UP/\overline{DN}) \cdot \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3} \}}$$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	21	23	ns
f_{max}	maximum clock frequency		57	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	50	53	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D_0 to D_3	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q_0 to Q_3	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/$\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

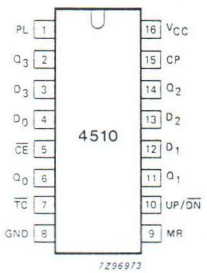


Fig. 1 Pin configuration.

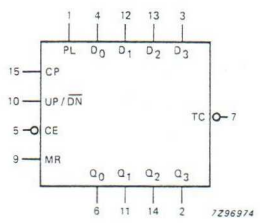


Fig. 2 Logic symbol.

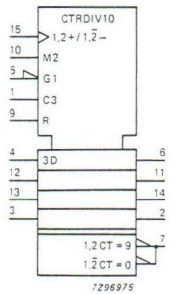


Fig. 3 IEC logic symbol.

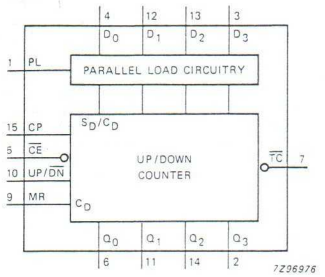


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

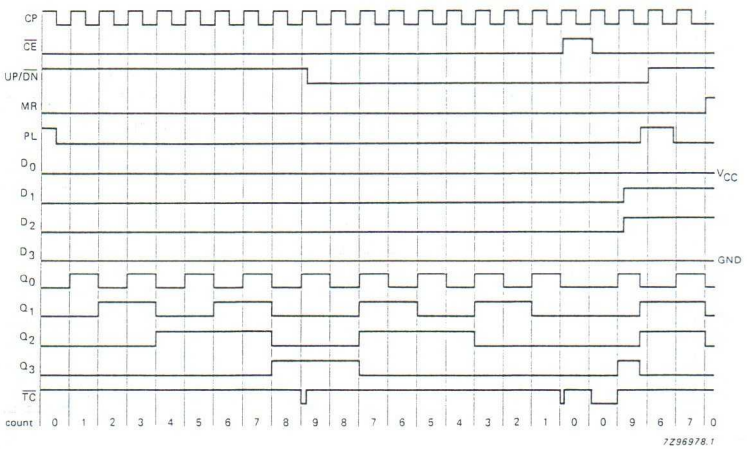


Fig. 5 Timing diagram.

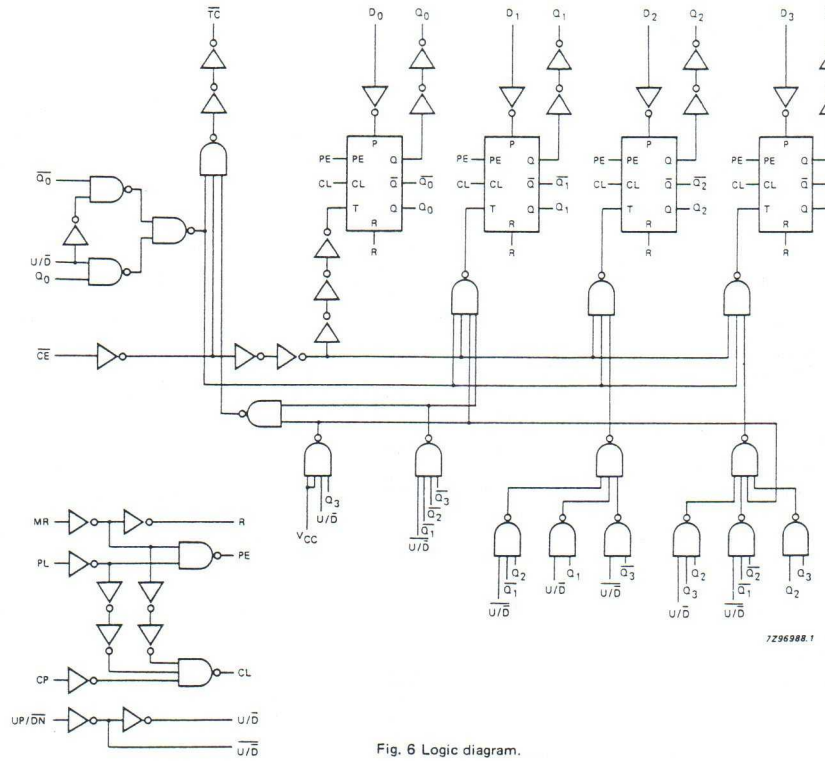


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		74 27 22	260 52 44		325 65 55		395 78 66	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay PL to $\overline{TC}$		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	pulse width CP, $\overline{CE}$ HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	parallel load pulse width HIGH	80 16 14	22 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_W	master reset pulse width HIGH	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time PL to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time UP/$\overline{DN}$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to PL	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{CE}$ to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to PL	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time UP/$\overline{DN}$ to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	17 52 62		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.75
PL, $\overline{CE}$	1.00
UP/$\overline{DN}$	1.00
CP	1.25
MR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		27	50		63		75	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n		25	42		53		63	ns	4.5	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		28	53		66		80	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		29	58		73		87	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		17	31		39		47	ns	4.5	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		31	50		63		75	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay PL to $\overline{TC}$		35	68		85		102	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	pulse width CP, $\overline{CE}$ HIGH or LOW	16	9		20		24		ns	4.5	Fig. 7
t_W	parallel load pulse width HIGH	16	6		20		24		ns	4.5	Fig. 10
t_W	master reset pulse width HIGH	20	4		25		30		ns	4.5	Fig. 10
t_{rem}	removal time MR to CP	23	13		29		35		ns	4.5	Fig. 10
t_{rem}	removal time PL to CP	17	10		21		26		ns	4.5	Fig. 10
t_{su}	set-up time UP/$\overline{DN}$ to CP	20	12		25		30		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	20	6		25		30		ns	4.5	Fig. 8
t_{su}	set-up time D_n to PL	20	6		25		30		ns	4.5	Fig. 11
t_h	hold time $\overline{CE}$ to CP	5	0		5		5		ns	4.5	Fig. 8
t_h	hold time D_n to PL	5	0		5		5		ns	4.5	Fig. 11
t_h	hold time UP/$\overline{DN}$ to CP	0	−5		0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	53		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

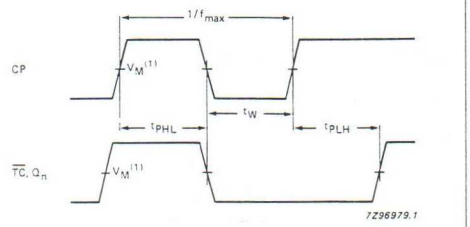


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) and terminal count ($\overline{TC}$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

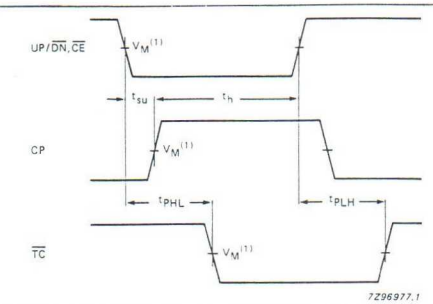


Fig. 8 Waveforms showing the set-up and hold times from count enable ($\overline{CE}$) and up/down (UP/$\overline{DN}$) control inputs to the clock pulse (CP), the propagation delays from UP/$\overline{DN}$, $\overline{CE}$ to $\overline{TC}$.

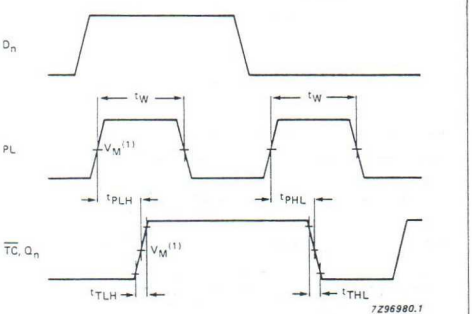


Fig. 9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.

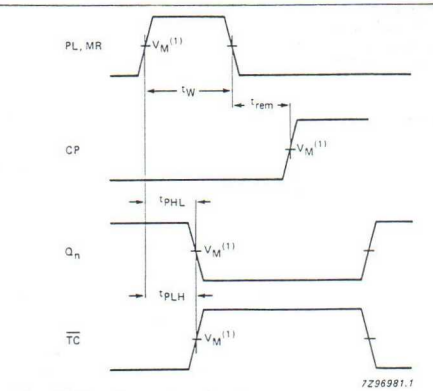


Fig. 10 Waveforms showing the master reset pulse, master reset to terminal count and Q_n delay and master reset to clock removal time.

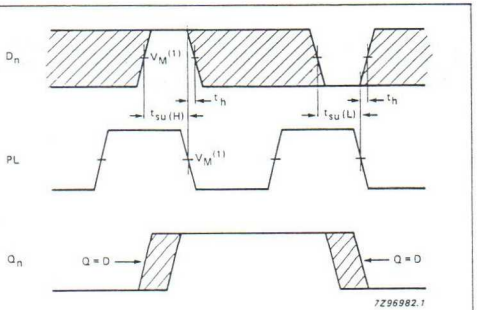


Fig. 11 Waveforms showing the data set-up and hold times to parallel load (PL).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

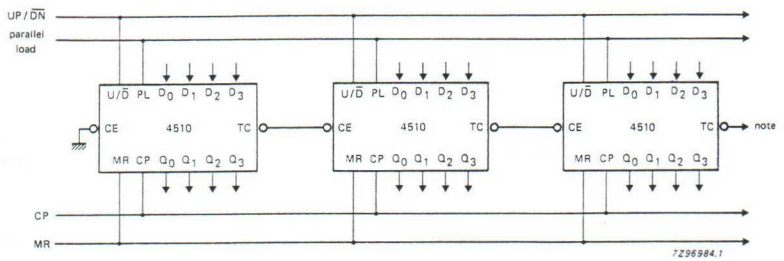


Fig. 12 Cascading counter packages (parallel clocking).

Note to Fig. 12

Terminal count ($\overline{TC}$) lines at the 2nd, 3rd, etc. stages may have a negative-going glitch pulse resulting from differential delays of different 4510s. These negative-going glitches do not affect proper 4510 operation. However, if the terminal count signals are used to trigger other edge sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.

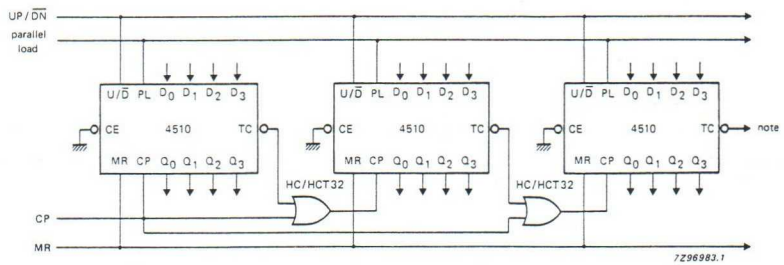
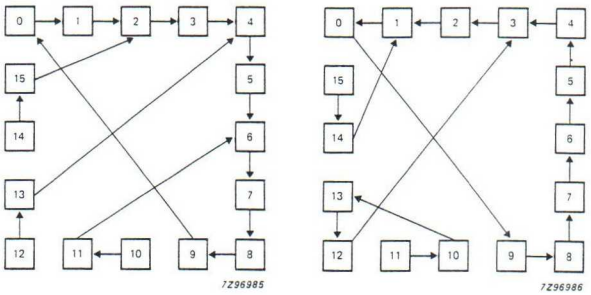


Fig. 13 Cascading counter packages (ripple clocking).

Note to Fig. 13

Ripple clocking mode: the UP/$\overline{DN}$ control can be changed at any count. The only restriction on changing the UP/$\overline{DN}$ control is that the clock input to the first counting stage must be HIGH. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and $\overline{TC}$ is connected directly to the CP input of the next stage with $\overline{CE}$ grounded.



Count-up mode.

Count-down mode.

Notes to Fig. 14

Count-up mode: illegal states in BCD counters corrected in one count.
Count-down mode: illegal states in BCD counters corrected in one or two counts.

Fig. 14 State diagrams.

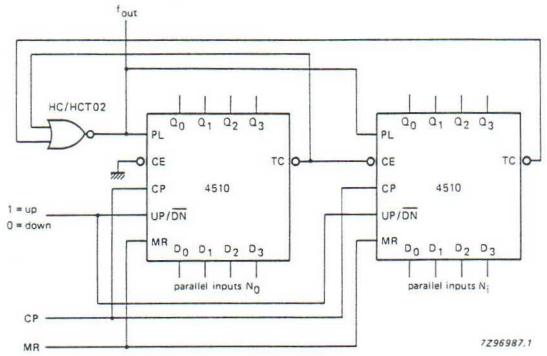


Fig. 15 Programmable cascaded frequency divider.

Note to Fig. 15

Use the following formulae to calculate N_{total}:

$$N_{total} = \left\{ \sum_{1}^{i} \pi(10 \times N_i) \right\} + N_0$$

$$f_{out} = \frac{f_{in}}{N_{total}}$$

Formulae are only applicable if legal data is provided to the parallel inputs.

parallel inputs				count-up	count-down
D_3	D_2	D_1	D_0	n	n
0	0	0	0	9	*
0	0	0	1	8	1
0	0	1	0	7	2
0	0	1	1	6	3
0	1	0	0	5	4
0	1	0	1	4	5
0	1	1	0	3	6
0	1	1	1	2	7
1	0	0	0	1	8
1	0	0	1	*	9

* no count; f_{out} is HIGH

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D_1 to D_4), an active LOW latch enable input ($\overline{LE}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH segment outputs (Q_a to Q_g).

When $\overline{LE}$ is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D_1 to D_4.
When $\overline{LE}$ goes HIGH, the last data present on D_1 to D_4 are stored in the latches and the segment outputs remain stable.
When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n $\overline{LE}$ to Q_n $\overline{BI}$ to Q_n $\overline{LT}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	 24 23 19 12	 24 24 20 13	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	$\overline{LT}$	lamp test input (active LOW)
4	$\overline{BI}$	ripple blanking input (active LOW)
5	$\overline{LE}$	latch enable input (active LOW)
7, 1, 2, 6	D_1 to D_4	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q_a to Q_g	segments outputs
16	V_{CC}	positive supply voltage

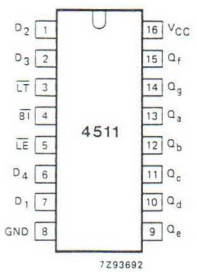


Fig. 1 Pin configuration.

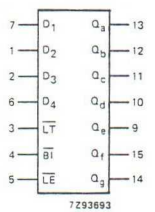


Fig. 2 Logic symbol.

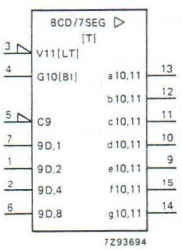


Fig. 3 IEC logic symbol.

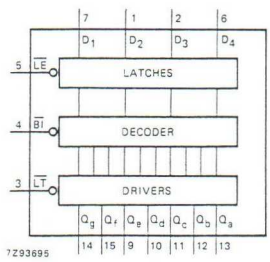


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_4	D_3	D_2	D_1	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	*							*

* Depends upon the BCD-code applied during the LOW-to-HIGH transition of $\overline{LE}$.

H = HIGH voltage level
L = LOW voltage level
X = don't care

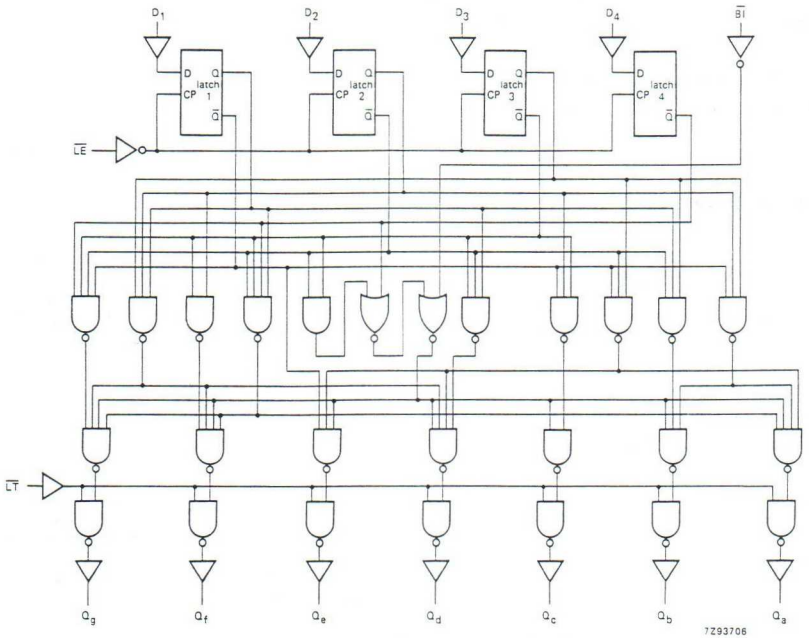


Fig. 5 Logic diagram.

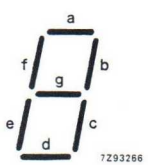


Fig. 6 Segment designation.

Fig. 7 Display.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I	$-I_O$ mA
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0
V_{OH}	HIGH level output voltage	5.60 5.48 4.80			5.45 5.34 4.50		5.35 5.20 4.20		V	6.0	V_{IH} or V_{IL}	7.5 10.0 15.0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		77 28 22	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BI}$ to Q_n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to $\overline{LE}$	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time D_n to $\overline{LE}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I	$-I_O$ mA
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{LT}$, $\overline{LE}$	1.50
$\overline{BI}$, D_n	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		28	60		75		90	ns	4.5	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		27	54		68		81	ns	4.5	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BI}$ to Q_n		23	44		55		66	ns	4.5	Fig. 10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n		16	30		38		45	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig. 9
t_{su}	set-up time D_n to $\overline{LE}$	12	5		15		18		ns	4.5	Fig. 11
t_h	hold time D_n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig. 11

AC WAVEFORMS

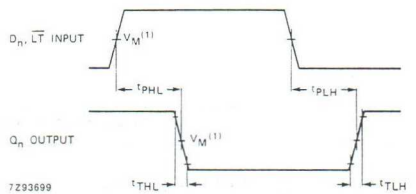


Fig. 8 Waveforms showing the input (D_n, $\overline{LT}$) to output (Q_n) propagation delays and the output transition times.

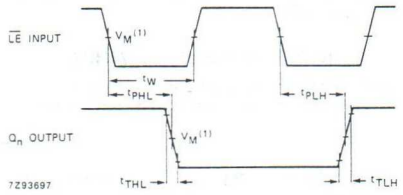


Fig. 9 Waveforms showing the input ($\overline{LE}$) to output (Q_n) propagation delays and the latch enable pulse width.

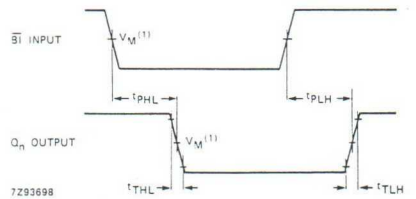


Fig. 10 Waveforms showing the input ($\overline{BI}$) to output (Q_n) propagation delays.

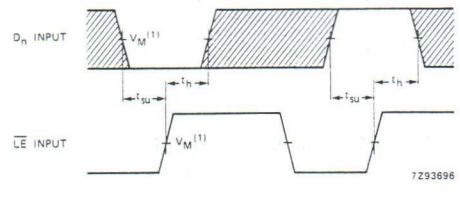


Fig. 11 Waveforms showing the data set-up and hold times for D_n input to $\overline{LE}$ input.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION DIAGRAMS

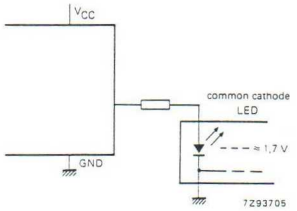


Fig. 12 Connection to common cathode LED display readout.

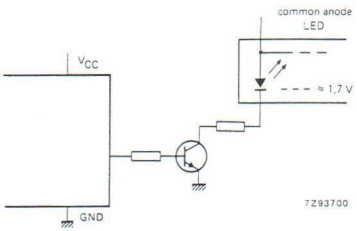
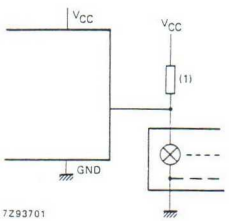


Fig. 13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig. 14 Connection to incandescent display readout.

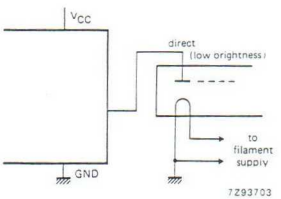


Fig. 15 Connection to fluorescent display readout.

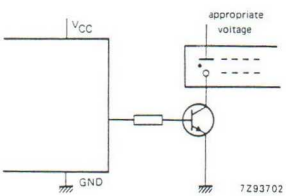


Fig. 16 Connection to gas discharge display readout.

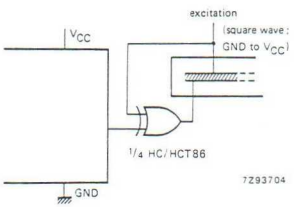


Fig. 17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).

4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES

FEATURES

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), with latches, a latch enable input (LE), and an active LOW enable input ($\overline{E}$). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch.

When the "4514" is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	23	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	45	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q_0 to Q_{15}	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

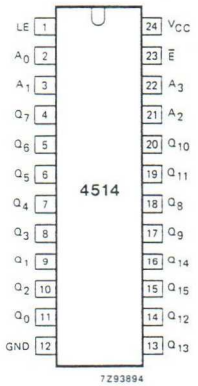


Fig. 1 Pin configuration.

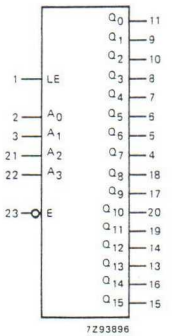


Fig. 2 Logic symbol.

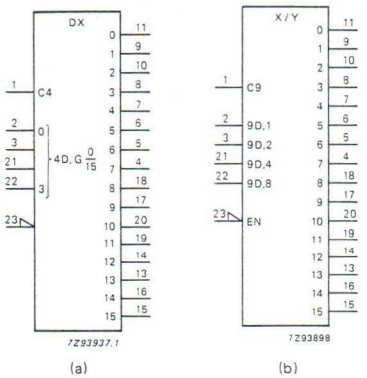


Fig. 3 IEC logic symbol.

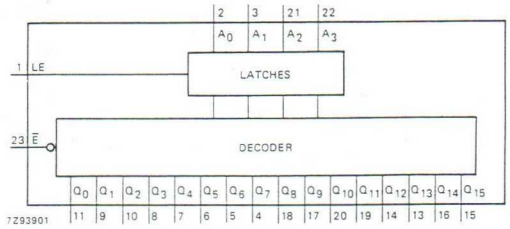


Fig. 4 Functional diagram.

APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

INPUTS					OUTPUTS													
$\overline{E}$	A_0	A_1	A_2	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

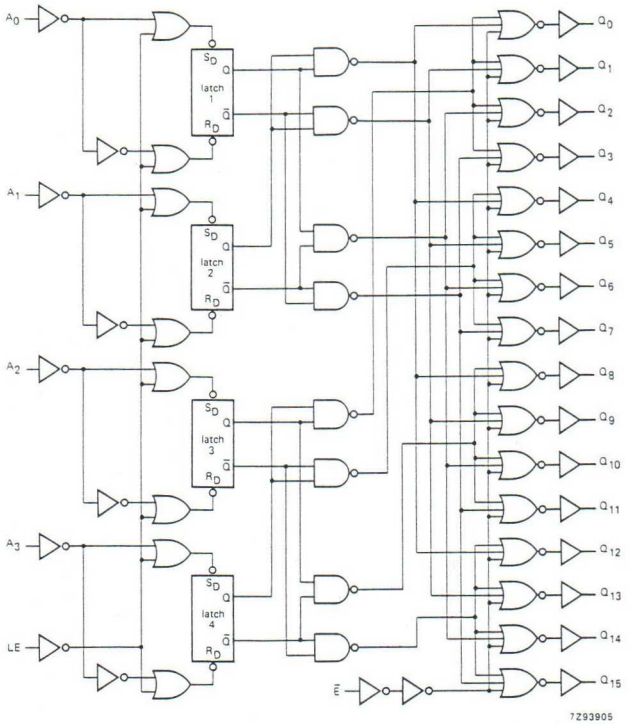


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Q_n		41 15 12	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time A_n to LE	90 18 15	25 9 7		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time A_n to LE	1 1 1	−11 −4 −3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.65
LE	1.40
$\overline{E}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		30	55		69		83	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		29	50		63		75	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to Q_n		17	40		50		60	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig. 7
t_{su}	set-up time A_n to LE	18	9		23		27		ns	4.5	Fig. 7
t_h	hold time A_n to LE	3	−3		3		3		ns	4.5	Fig. 7

AC WAVEFORMS

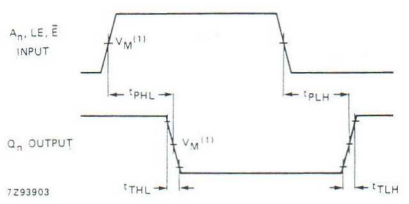


Fig. 6 Waveforms showing the input (A_n, LE, $\overline{E}$) to output (Q_n) propagation delays and the output transition times.

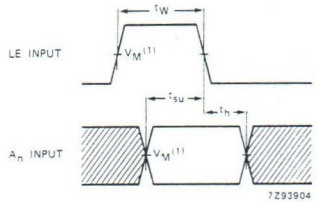


Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n. Set-up and hold times are shown as positive values but may be specified as negative values.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION

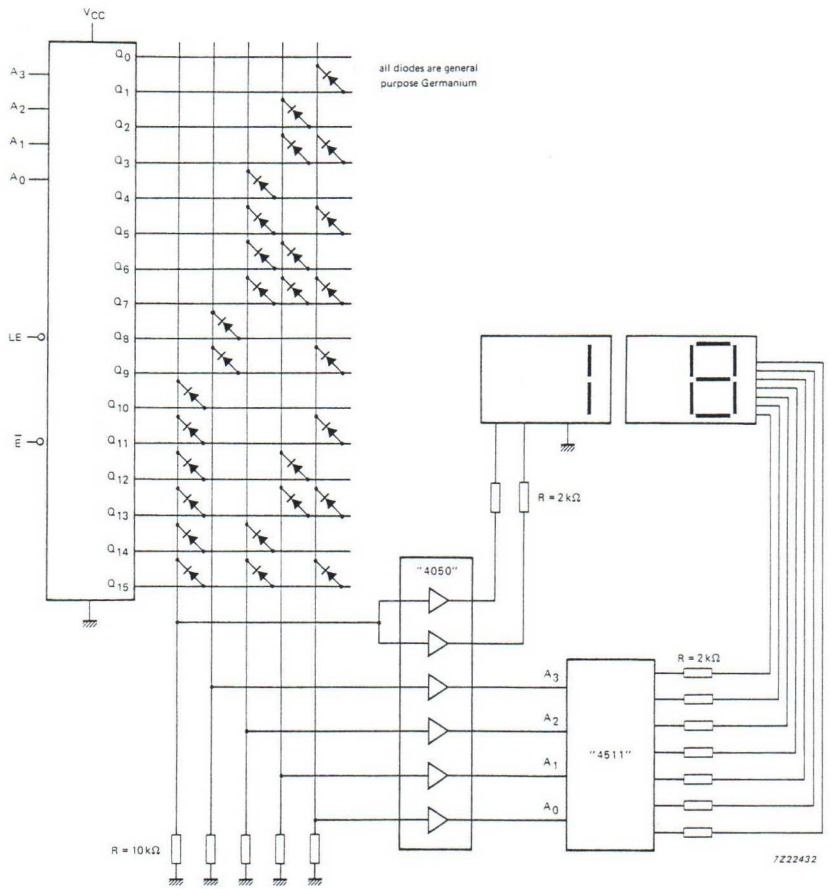


Fig. 8 Code-to-code conversion; hexadecimal to BCD.

4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES; INVERTING

FEATURES

- Inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3) with latches, a latch enable input (LE), and an active LOW enable input ($\overline{E}$). The 16 inverting outputs ($\overline{Q}_0$ to $\overline{Q}_{15}$) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is LOW. When $\overline{E}$ is HIGH, all outputs are HIGH. The enable input ($\overline{E}$) does not affect the state of the latch.

When the "4515" is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	25	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{Q}_0$ to $\overline{Q}_{15}$	multiplexer outputs (active LOW)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

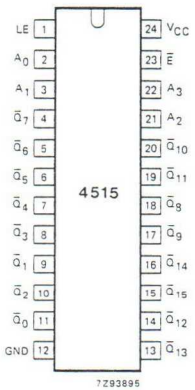


Fig. 1 Pin configuration.

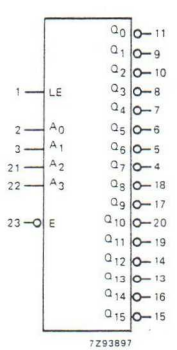


Fig. 2 Logic symbol.

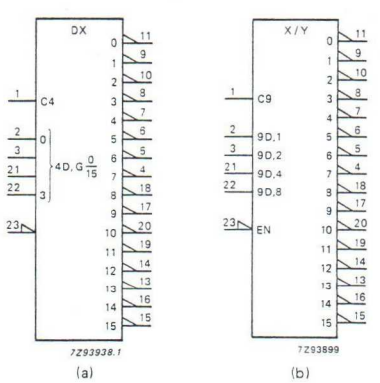


Fig. 3 IEC logic symbol.

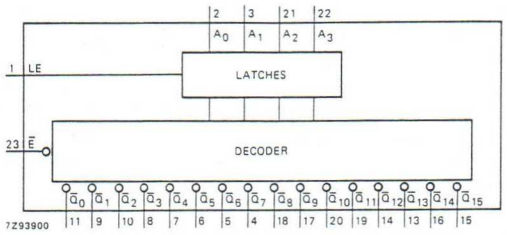


Fig. 4 Functional diagram.

APPLICATIONS

- Digital mutliplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

INPUTS					OUTPUTS														
$\bar{E}$	A_0	A_1	A_2	A_3	$\bar{Q}_0$	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	$\bar{Q}_6$	$\bar{Q}_7$	$\bar{Q}_8$	$\bar{Q}_9$	$\bar{Q}_{10}$	$\bar{Q}_{11}$	$\bar{Q}_{12}$	$\bar{Q}_{13}$	$\bar{Q}_{14}$	$\bar{Q}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

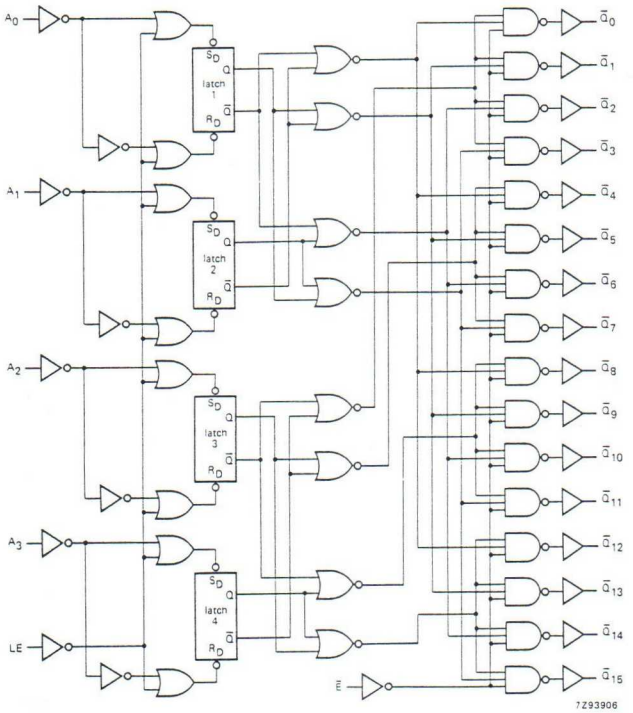


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		66 24 19	225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Q}_n$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	latch enable pulse width HIGH	75 15 13	14 5 4		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time A_n to LE	90 18 15	28 10 8		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time A_n to LE	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.65
LE	1.40
$\overline{E}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$		30	55		69		83	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		29	50		63		75	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Q}_n$		18	40		50		60	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	latch enable pulse width HIGH	16	3		20		24		ns	4.5	Fig. 7
t_{su}	set-up time A_n to LE	18	9		23		27		ns	4.5	Fig. 7
t_h	hold time A_n to LE	3	−2		3		3		ns	4.5	Fig. 7

AC WAVEFORMS

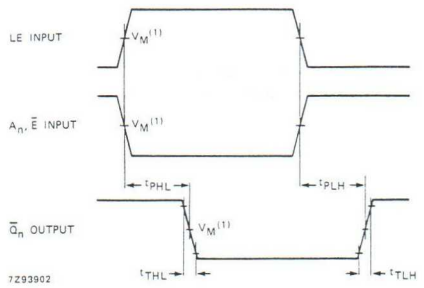


Fig. 6 Waveforms showing the input (A_n, LE, $\overline{E}$) to output ($\overline{Q}_n$) propagation delays and the output transition times.

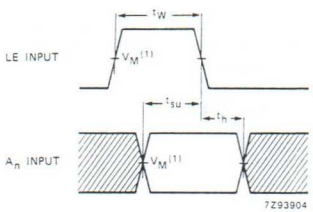


Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n. Set-up and hold times are shown as positive values but may be specified as negative values.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

BINARY UP/DOWN COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4516 are high-speed Si-gate CMOS devices and are pin compatible with the "4516" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4516 are edge-triggered synchronous up/down 4-bit binary counters with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D_0 to D_3), four parallel outputs (Q_0 to Q_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW-to-HIGH transition of CP. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q_0 to Q_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q_0 to Q_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \cdot \{(UP/\overline{DN}) \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 + \overline{(UP/\overline{DN}) \cdot \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3}\}}$$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	19	19	ns
f_{max}	maximum clock frequency		45	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	59	61	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D_0 to D_3	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q_0 to Q_3	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/$\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

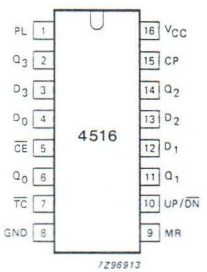
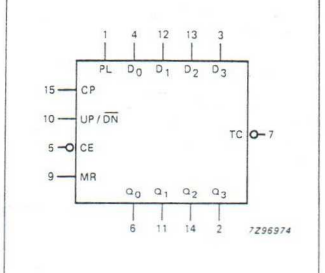


Fig. 1 Pin configuration.



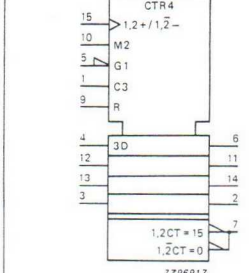


Fig. 3 IEC logic symbol.

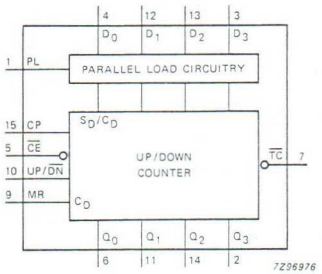


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level
L = LOW voltage level
X = dont't care
↑ = LOW-to-HIGH clock transition

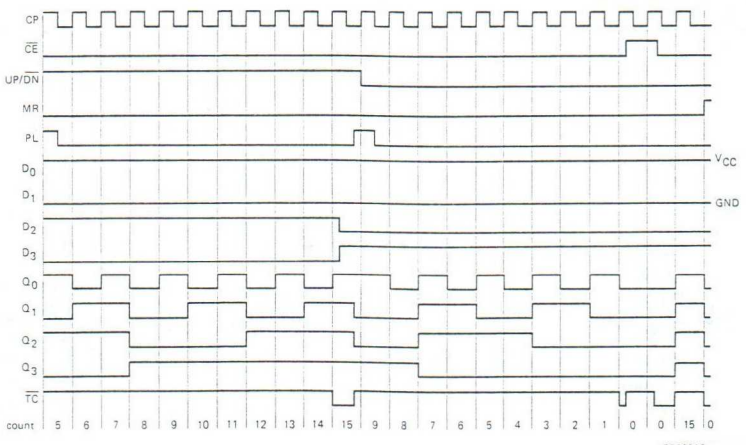


Fig. 5 Timing diagram.

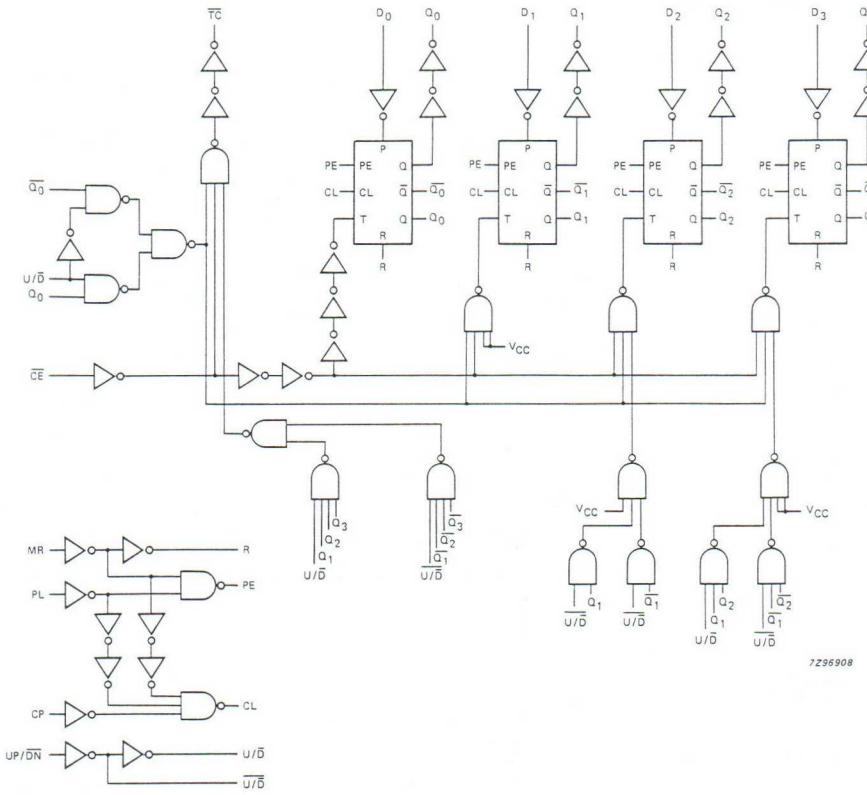


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		83 30 24	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		74 27 22	260 52 44		325 65 55		395 78 66	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to $\overline{TC}$		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 9
t_{TLH}/t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width CP, $\overline{CE}$ HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	parallel load pulse width HIGH	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_W	master rest pulse width HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time PL to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time UP/$\overline{DN}$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to PL	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{CE}$ to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to PL	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time UP/$\overline{DN}$ to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	16 49 58		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.75
PL, $\overline{CE}$	1.00
UP/$\overline{DN}$	1.00
CP	1.25
MR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		28	50		63		75	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n		24	42		53		63	ns	4.5	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		32	53		66		80	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		29	58		73		87	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		18	31		39		47	ns	4.5	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		31	50		63		75	ns	4.5	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to $\overline{TC}$		34	68		85		102	ns	4.5	Fig. 9
t_{TLH}/t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	clock pulse width CP, $\overline{CE}$ HIGH or LOW	16	9		20		24		ns	4.5	Fig. 7
t_W	parallel load pulse width HIGH	16	8		20		24		ns	4.5	Fig. 10
t_W	master rest pulse width HIGH	20	5		25		30		ns	4.5	Fig. 10
t_{rem}	removal time MR to CP	23	14		29		35		ns	4.5	Fig. 10
t_{rem}	removal time PL to CP	17	10		21		26		ns	4.5	Fig. 10
t_{su}	set-up time UP/$\overline{DN}$ to CP	20	11		25		30		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	20	9		25		30		ns	4.5	Fig. 8
t_{su}	set-up time D_n to PL	20	9		25		30		ns	4.5	Fig. 11
t_h	hold time $\overline{CE}$ to CP	10	9		13		15		ns	4.5	Fig. 8
t_h	hold time D_n to PL	5	−6		5		5		ns	4.5	Fig. 11
t_h	hold time UP/$\overline{DN}$ to CP	0	−5		0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	52		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

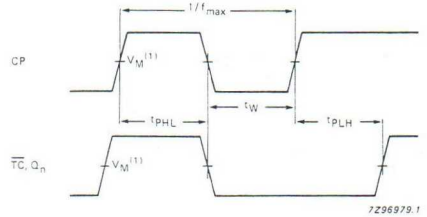


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) and terminal count ($\overline{TC}$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

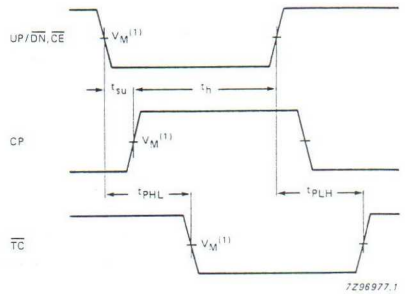


Fig. 8 Waveforms showing the set-up and hold times form count enable ($\overline{CE}$) and up/down (UP/$\overline{DN}$) control inputs to the clock pulse (CP), the propagation delays from UP/$\overline{DN}$, $\overline{CE}$ to $\overline{TC}$.

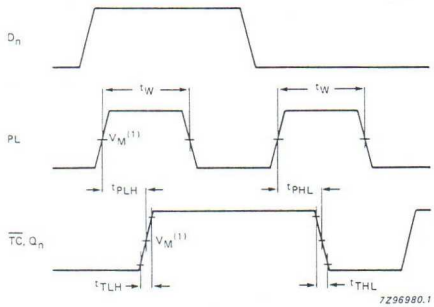


Fig. 9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.

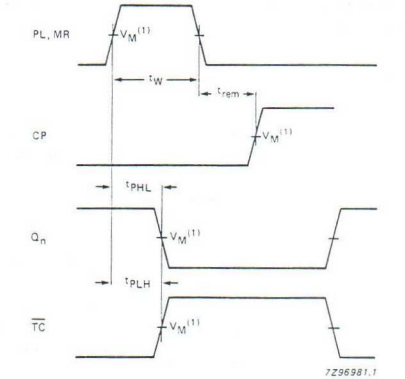


Fig. 10 Waveforms showing the master reset pulse, master reset to terminal count and Q_n delay and master reset to clock removal time.

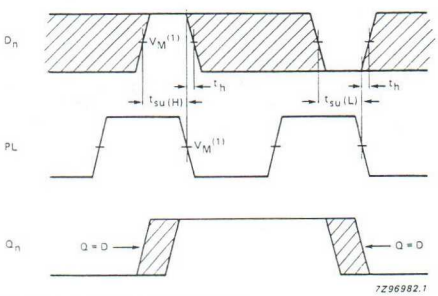


Fig. 11 Waveforms showing the data set-up and hold times to parallel load (PL).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

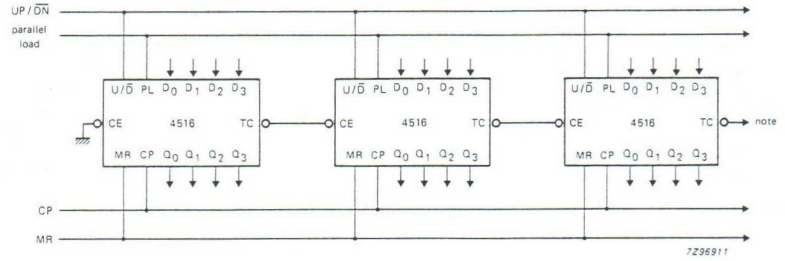


Fig. 12 Cascading counter packages (parallel clocking).

Note to Fig. 12

Terminal count ($\overline{TC}$) lines at the 2nd 3rd etc. Stages may have a negative-going glitch pulse resulting from differential delays of different 4516s. These negative-going glitches do not affect proper 4516 operation. However, if the terminal count signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.

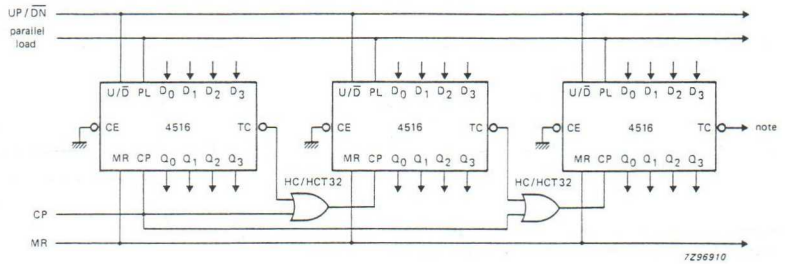


Fig. 13 Cascading counter packages (ripple clocking).

Note to Fig. 13

Ripple clocking mode: the UP/$\overline{DN}$ control can be changed at any count. The only restriction on changing the UP/$\overline{DN}$ control is that the clock input to the first counting stage must be "HIGH". For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and $\overline{TC}$ is connected directly to the CP input of the next stage with $\overline{CE}$ grounded.

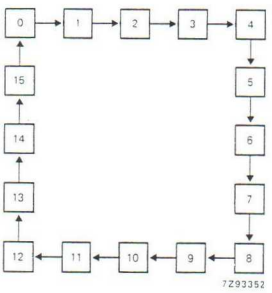


Fig. 14 State diagram.

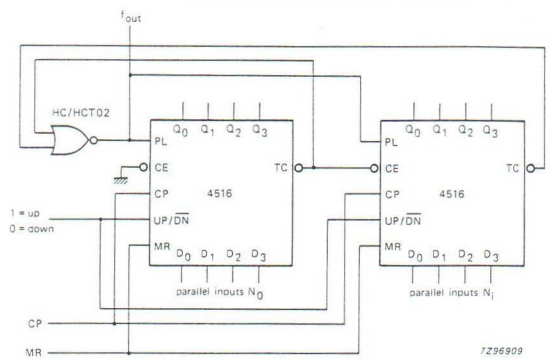


Fig. 15 Programmable cascaded frequency divider.

Note to Fig. 15

Use the following formulae to calculate N_{total}:

$$N_{total} = \left(\sum_{1}^{i} (16 \times N_i) \right) + N_0$$

$$f_{out} = f_{in}/N_{total}$$

parallel inputs				count-up	count-down
D_3	D_2	D_1	D_0	n	n
0	0	0	0	15	*
0	0	0	1	14	1
0	0	1	0	13	2
0	0	1	1	12	3
0	1	0	0	11	4
0	1	0	1	10	5
0	1	1	0	9	6
0	1	1	1	8	7
1	0	0	0	7	8
1	0	0	1	6	9
1	0	1	0	5	10
1	0	1	1	4	11
1	1	0	0	3	12
1	1	0	1	2	13
1	1	1	0	1	14
1	1	1	1	*	15

* no count; f_{out} is HIGH.

DUAL SYNCHRONOUS BCD COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n	C_L = 15 pF; V_{CC} = 5 V	20	24	ns
t_{PHL}	propagation delay nMR to nQ_n		13	14	ns
f_{max}	maximum clock frequency		61	55	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	29	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

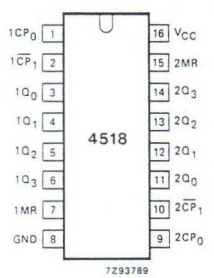


Fig. 1 Pin configuration.

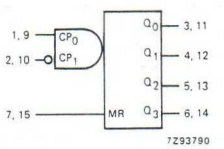


Fig. 2 Logic symbol.

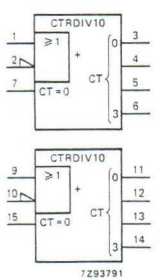


Fig. 3 IEC logic symbol.

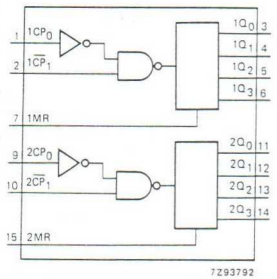


Fig. 4 Functional diagram.

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

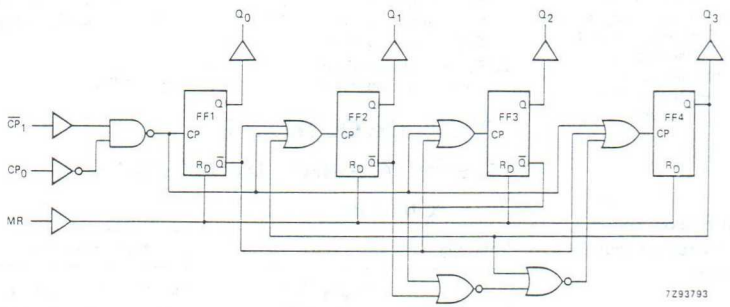


Fig. 5 Logic diagram (one counter).

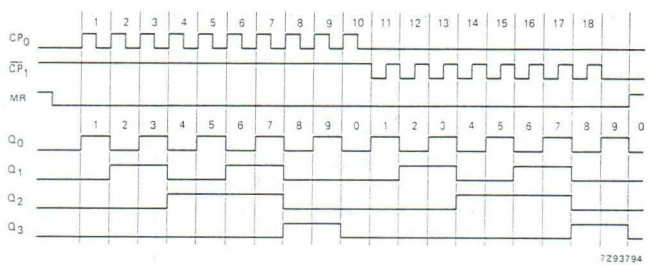


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n		66 24 19	210 42 36		265 53 45		315 63 59	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay nMR to nQ_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width HIGH	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0 0 0	−22 −8 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency nCP_0, $n\overline{CP}_1$	6.0 30 35	18 55 66		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP_0, $n\overline{CP}_1$	0.80
nMR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n		28	53		66		80	ns	4.5	Fig. 9
t_{PHL}	propagation delay nMR to nQ_n		17	35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	clock pulse width HIGH or LOW	20	11		25		30		ns	4.5	Fig. 8
t_W	master reset pulse width HIGH	20	11		25		30		ns	4.5	Fig. 8
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0	−11		0		0		ns	4.5	Fig. 8
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	16	5		20		24		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency nCP_0, $n\overline{CP}_1$	25	50		20		17		MHz	4.5	Fig. 8

AC WAVEFORMS

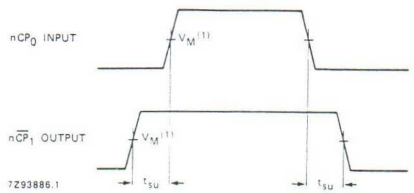


Fig. 7 Waveforms showing hold and set-up times for nCP_0 to $n\overline{CP}_1$ and $n\overline{CP}_1$ to nCP_0.

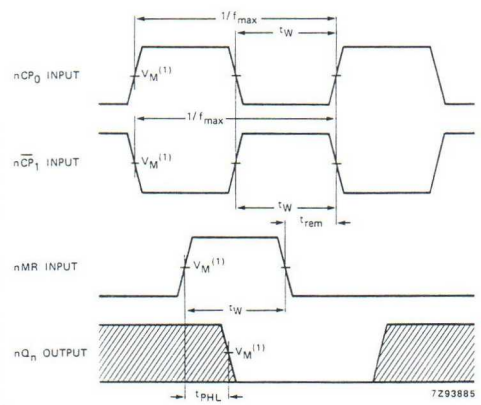


Fig. 8 Waveforms showing the minimum pulse widths for nCP_0, $n\overline{CP}_1$ and nMR inputs; the removal time for nMR and the propagation delay for nMR to nQ_n outputs and the maximum clock pulse frequency.

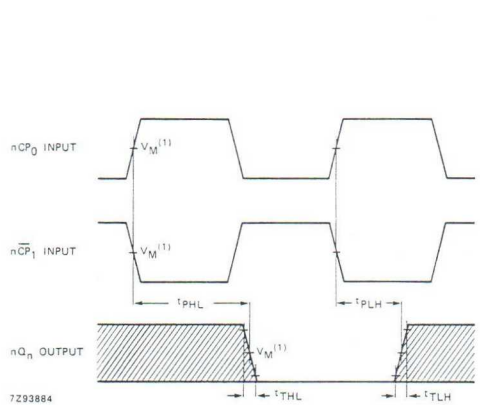


Fig. 9 Waveforms showing the propagation delays for nCP_0, $n\overline{CP}_1$ to nQ_n outputs and the output transition times.

Note to Fig. 8 and Fig. 9

Conditions:
$n\overline{CP}_1$ = HIGH while nCP_0 is triggered on a LOW-to-HIGH transition and nCP_0 = LOW, while $n\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-BIT SYNCHRONOUS BINARY COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n	C_L = 15 pF; V_{CC} = 5 V	24	24	ns
t_{PHL}	propagation delay nMR to nQ_n		13	13	ns
f_{max}	maximum clock frequency		68	64	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	29	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

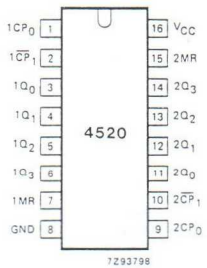


Fig. 1 Pin configuration.

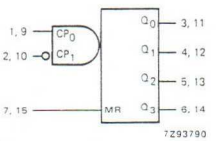


Fig 2 Logic symbol.

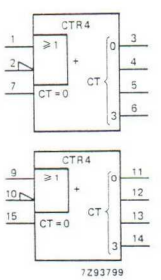


Fig. 3 IEC logic symbol.

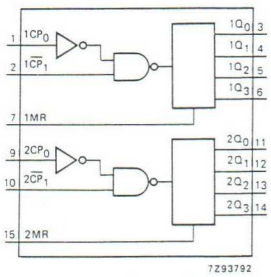


Fig. 4 Functional diagram.

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

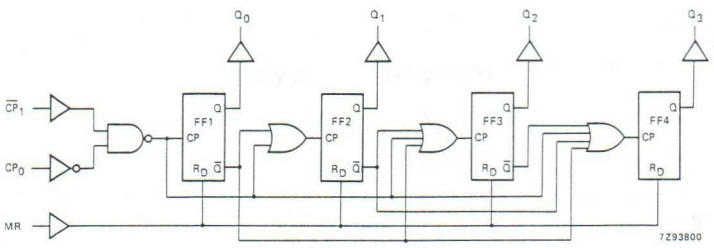


Fig. 5 Logic diagram (one counter).

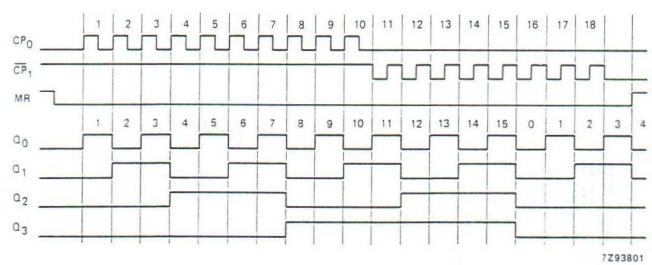


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0 to nQ_n		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay nMR to nQ_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width HIGH	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time nMR to nCP_0; $n\overline{CP}_1$	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	19 58 69		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP_0, $n\overline{CP}_1$	0.80
nMR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0 to nQ_n		28	53		66		80	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n		25	53		66		80	ns	4.5	Fig. 8
t_{PHL}	propagation delay nMR to nQ_n		16	35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 8
t_W	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	20	12		25		30		ns	4.5	Fig. 7
t_{rem}	removal time nMR to nCP_0; $n\overline{CP}_1$	0	−8		0		0		ns	4.5	Fig. 7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	16	6		20		24		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	58		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

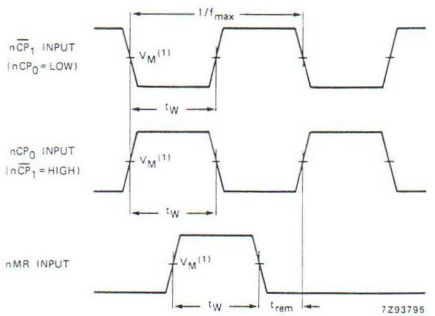


Fig. 7 Waveforms showing removal time for nMR; minimum nCP_0, $n\overline{CP}_1$, nMR pulse widths and maximum clock pulse frequency.

Conditions:

$n\overline{CP}_1$ = HIGH while nCP_0 is triggered on a LOW-to-HIGH transition; t_W and t_{rem} also apply when nCP_0 = LOW and $n\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

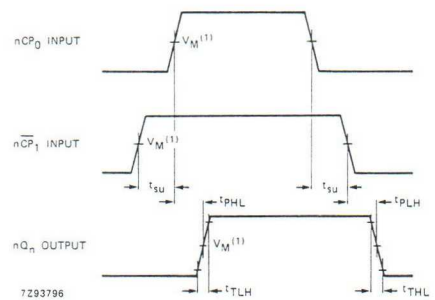


Fig. 8 Waveforms showing set-up times for nCP_0 to $n\overline{CP}_1$ and $n\overline{CP}_1$ to nCP_0, propagation delays and output transition times.

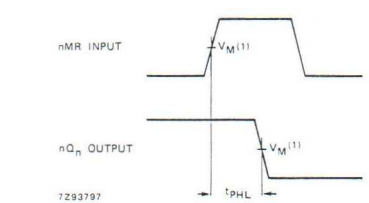


Fig. 9 Waveforms showing propagation delay from nMR to nQ_n output.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC};
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I_{CC} category: MSI
- Power-on reset on-chip

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ($n\overline{A}_0$), an active HIGH trigger/retrigger input (nA_1), an overriding active LOW direct reset input ($n\overline{R}_D$), an output (nQ) and its complement ($n\overline{Q}$), and two pins (nC_{TC} and nRC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ± 0.2%.

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $0.7 \times R_t \times C_t$. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at $n\overline{R}_D$ terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	27	30	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multivibrator	notes 1 and 2	136	138	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) +$$
$$+ 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC} \text{ where:}$$

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
D = duty factor in %
C_{EXT} = timing capacitance in pF

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}$, $2C_{TC}$	external capacitor connections
2, 14	$1RC_{TC}$, $2RC_{TC}$	external resistor/capacitor connections
3, 13	$1\overline{R}_D$, $2\overline{R}_D$	direct reset inputs (active LOW)
4, 12	$1A_1$, $2A_1$	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{A}_0$, $2\overline{A}_0$	trigger inputs (HIGH-to-LOW, edge-triggered)
6, 10	1Q, 2Q	pulse outputs
7, 9	$1\overline{Q}$, $2\overline{Q}$	complementary pulse outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

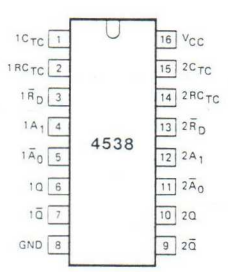


Fig. 1 Pin configuration.

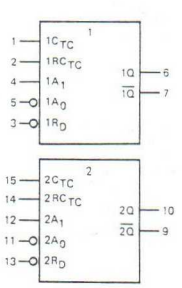


Fig. 2 Logic symbol.

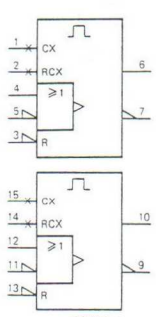


Fig. 3 IEC logic symbol.

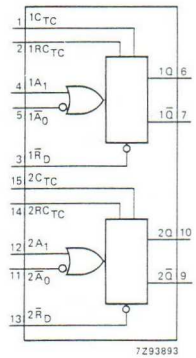
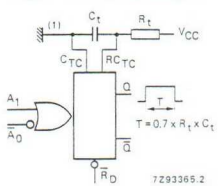


Fig. 4 Functional diagram.



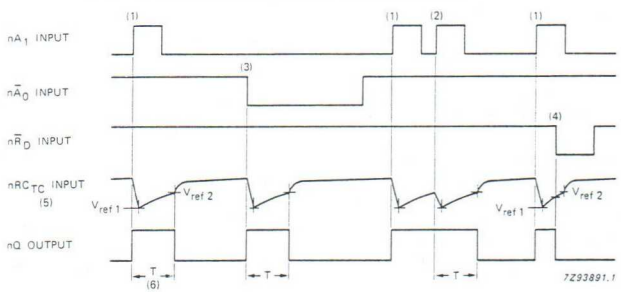
(1) Connect C_{TC} (pins 1 and 15) to GND (pin 8).

Fig. 5 Connection of the external timing components R_t and C_t.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{A}_0$	nA_1	$n\bar{R}_D$	nQ	$n\bar{Q}$
↓	L	H	⎍	⎍
H	↑	H	⎍	⎍
X	X	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse



(1) Positive edge triggering.
(2) Positive edge retriggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) V_{ref1} and V_{ref2} are internal reference voltages.
(6) $T = 0.7 \times R_t \times C_t$ (see also Fig. 5).

Fig. 6 Timing diagram.

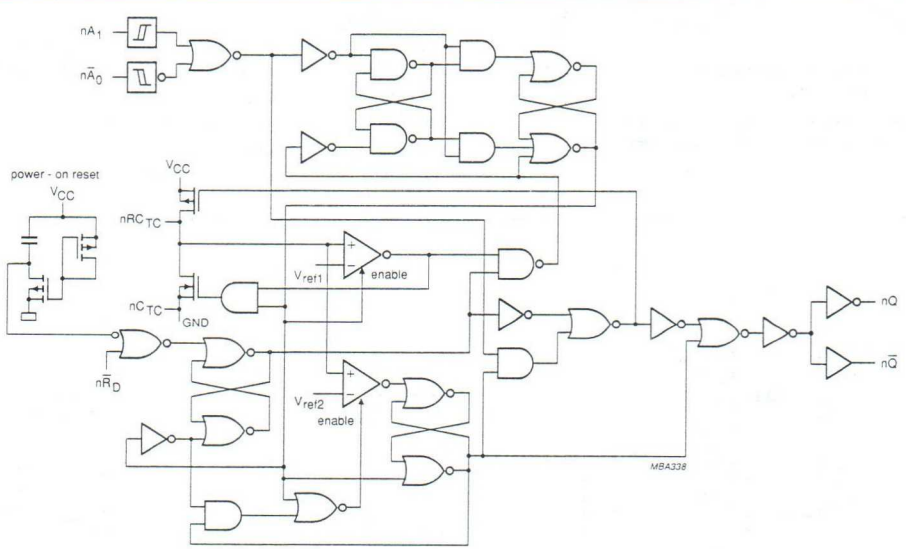


Fig. 7 Logic diagram (V_{ref1} and V_{ref2} are internal reference voltages).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $n\overline{A}_0$, nA_1 to $n\overline{Q}$		83 30 24	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		80 29 23	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		83 30 24	265 53 45		340 68 58		400 80 68	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8
t_W	$n\overline{A}_0$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	nA_1 pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	$n\overline{R}_D$ pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	nQ, $n\overline{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig. 8; R_t = 10 kΩ; C_t = 0.1 μF
t_{rem}	removal time $\overline{R}_D$ to $n\overline{A}_0$, nA_1	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 8
t_{rt}	retrigger time $n\overline{A}_0$, nA_1	– – –	455+X 80+X 55+X		– – –		– – –		ns	2.0 4.5 6.0	Fig. 8 X = C_{EXT}/(4.5 x V_{CC})
R_{EXT}	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0	
C_{EXT}	external timing capacitor	no limits							pF	5.0	

NON-STANDARD DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
$\pm I_I$	input leakage current nRC_{EXT}			0.5		5.0		10.0	μA	6.0	2.0 or GND	V_{CC} or GND; note 1

Note

1. This measurement can only be carried out after a trigger pulse is applied.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\bar{A}_0$, nA_1	0.50
$n\bar{R}_D$	0.65

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PLH}	propagation delay $n\overline{A}_0$, nA_1 to nQ		35	60		75		90	ns	4.5	Fig. 8
t_{PHL}	propagation delay $n\overline{A}_0$, nA_1 to $n\overline{Q}$		35	60		75		90	ns	4.5	Fig. 8
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		35	60		75		90	ns	4.5	Fig. 8
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		35	60		75		90	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time		7	15		19		21	ns	4.5	Fig. 8
t_W	$n\overline{A}_0$ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t_W	nA_1 pulse width HIGH	16	5		20		24		ns	4.5	Fig. 8
t_W	$n\overline{R}_D$ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t_W	nQ, $n\overline{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig. 8; R_t = 10 kΩ; C_t = 0.1 μF
t_{rem}	removal time $\overline{R}_D$ to $n\overline{A}_0$, nA_1	7	2		9		11		ns	4.5	Fig. 8
t_{rt}	retrigger time $n\overline{A}_0$, nA_1	–	80+X		–		–		ns	4.5	Fig. 8 X = C_{EXT}/(4.5 x V_{CC})
R_{EXT}	external timing resistor	2		1000					kΩ	5.0	
C_{EXT}	external timing capacitor	no limits							pF	5.0	

NON-STANDARD DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I V	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$\pm I_I$	input leakage current nRC_{EXT}			0.5		5.0		10.0	μA	5.5	2.0 or GND	V_{CC} or GND; note 1

Note

1. This measurement can only be carried out after a trigger pulse is applied.

AC WAVEFORMS

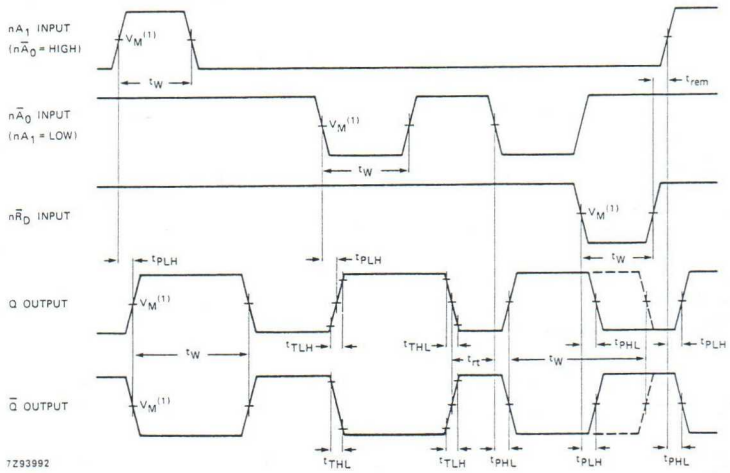
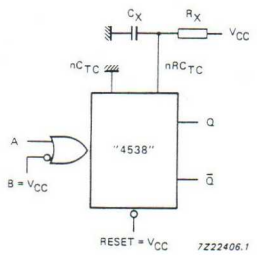


Fig. 8 Waveforms showing the input (nA_1, $n\bar{A}_0$, $n\bar{R}_D$) to output (nQ, $n\bar{Q}$) propagation delays, the output transition times, the input and output pulse widths, the removal time from direct reset ($n\bar{R}_D$) to input (nA_1, $n\bar{A}_0$), and the input retrigger time.

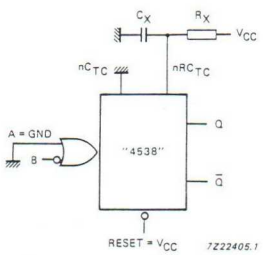
Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

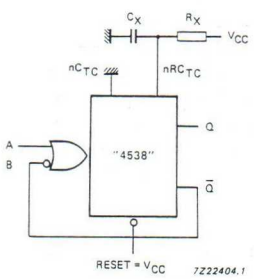


(a)

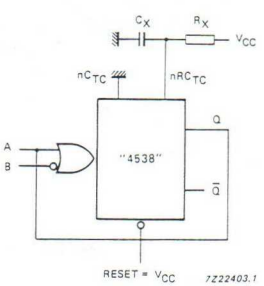


(b)

Fig. 9 Retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.



(a)



(b)

Fig. 10 Non-retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.

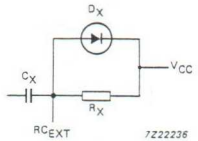


Fig. 11 Power-down protection circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes.
To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 11.

APPLICATION INFORMATION (Continued)

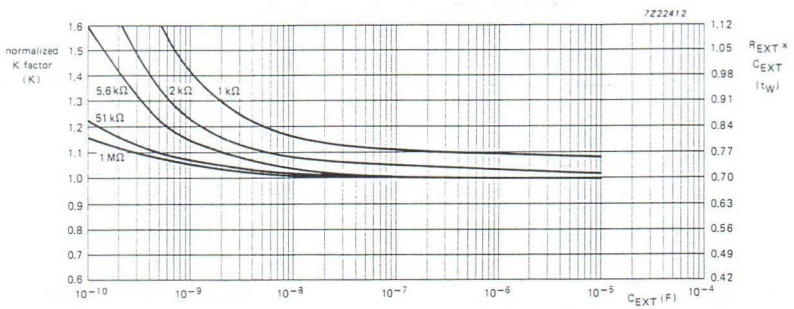


Fig. 12 Typical pulse width accuracy versus external capacitance; V_{CC} = 4.5 V; T_{amb} = 25 °C.

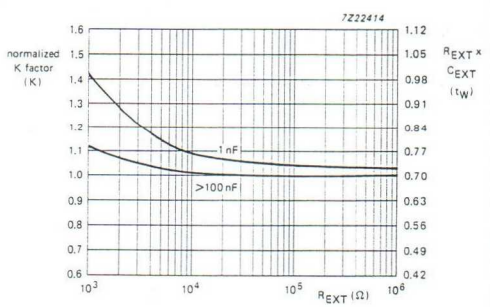


Fig. 13 Typical pulse width accuracy versus external resistance; V_{CC} = 4.5 V; T_{amb} = 25 °C.

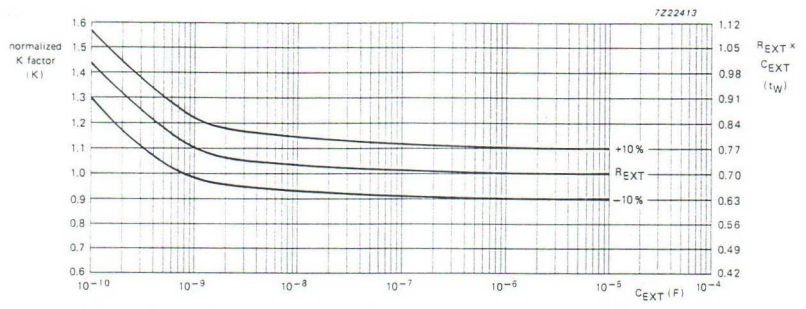


Fig. 14 Typical pulse width accuracy versus external capacitance; R_{EXT} = 10 kΩ; V_{CC} = 4.5 V; T_{amb} = 25 °C.

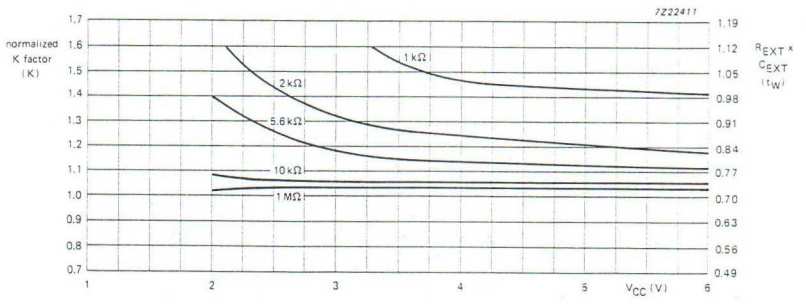


Fig. 15 Typical pulse width accuracy versus power supply; C_{EXT} = 1 nF; T_{amb} = 25 °C.

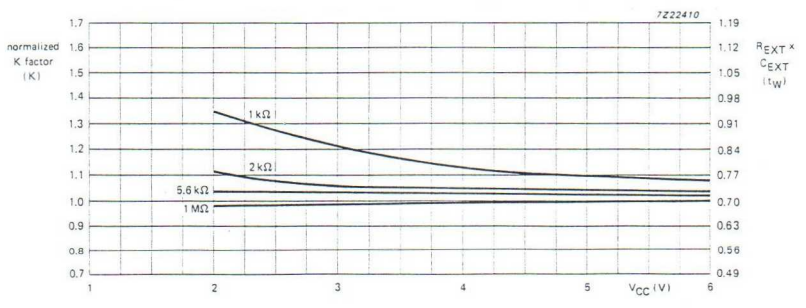


Fig. 16 Typical pulse width accuracy versus power supply; C_{EXT} = 100 nF; T_{amb} = 25 °C.

APPLICATION INFORMATION (Continued)

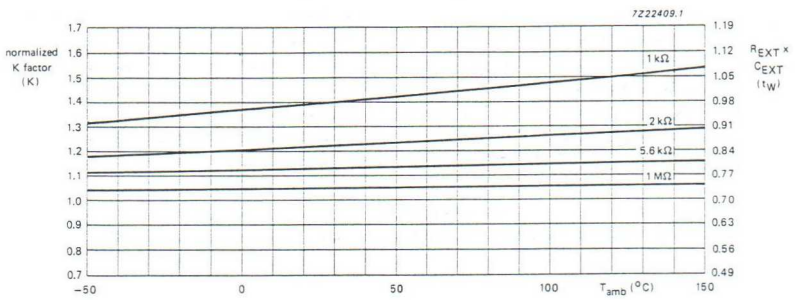


Fig. 17 Typical pulse width accuracy versus temperature; C_{EXT} = 1 nF; V_{CC} = 4.5 V.

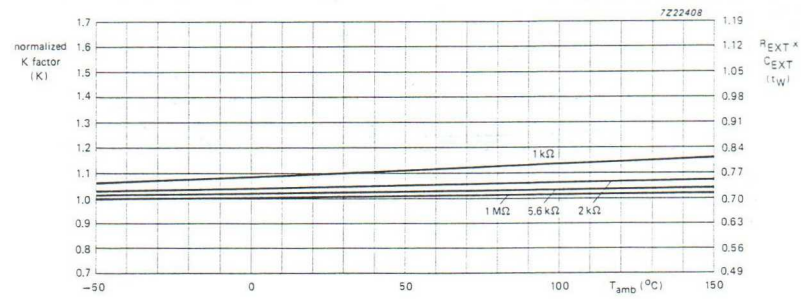


Fig. 18 Typical pulse width accuracy versus temperature; C_{EXT} = 1 μF; V_{CC} = 4.5 V.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D_0 to D_3), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_g).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LD to Q_n BI to Q_n	C_L = 15 pF V_{CC} = 5 V	 29 32 20	 33 31 28	 ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D_0 to D_3	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12 13, 15, 14	Q_a to Q_g	segment outputs
16	V_{CC}	positive supply voltage

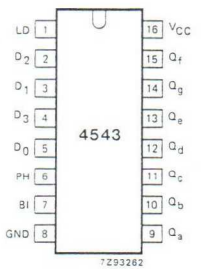


Fig. 1 Pin configuration.

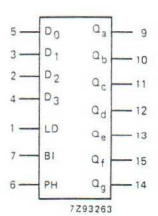


Fig. 2 Logic symbol.

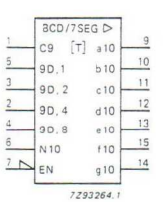


Fig. 3 IEC logic symbol.

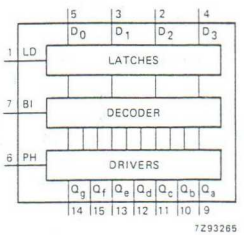


Fig. 4 Functional diagram.

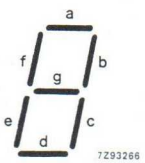


Fig. 5 Segment designation.

APPLICATIONS

- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH*	D_3	D_2	D_1	D_0	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

* For liquid crystal displays, apply a square-wave to PH.

** Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level
L = LOW voltage level
X = don't care

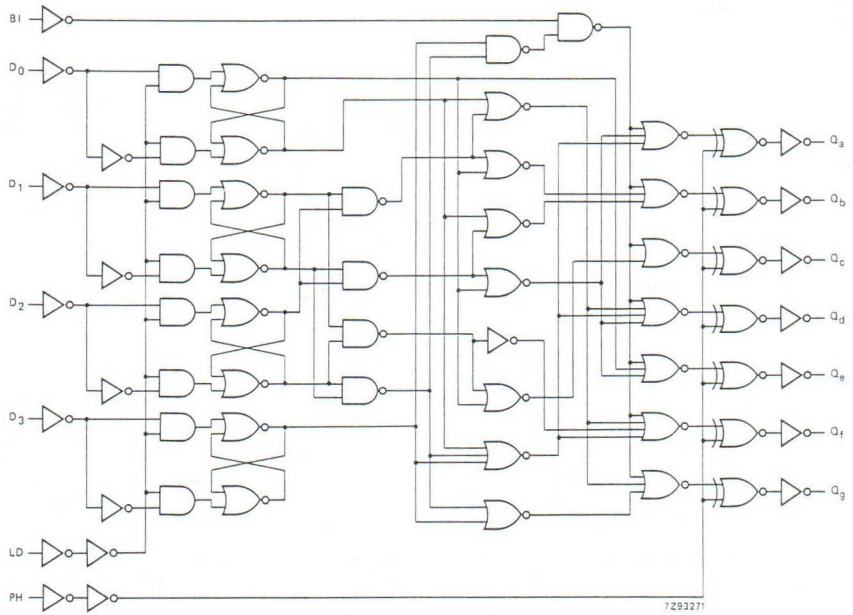


Fig. 6 Logic diagram.

Fig. 7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
For RATINGS see chapter "HCMOS family characteristics", section "Family specifications", standard outputs.

DC CHARACTERISTICS FOR 74HC

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 1.0 mA $-I_O$ = 1.3 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 1.0 mA I_O = 1.3 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		91 33 26	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		102 37 30	370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		66 24 19	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	
t_{THL}/t_{TLH}	output transition time		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	35 7 6	11 4 3		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time D_n to LD	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 15
t_h	hold time D_n to LD	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 15

DC CHARACTERISTICS FOR 74HCT

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 1.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 1.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_0, D_1, D_2	1.00
D_3	0.50
BI	0.50
LD	1.50
PH	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		38	80		100		120	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		36	68		85		102	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		32	66		83		99	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		24	66		83		99	ns	4.5	
t_{THL}/t_{TLH}	output transition time		23	50		63		75	ns	4.5	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	10	4		13		15		ns	4.5	Fig. 13
t_{su}	set-up time D_n to LD	12	4		15		18		ns	4.5	Fig. 15
t_h	hold time D_n to LD	8	2		10		12		ns	4.5	Fig. 15

APPLICATION DIAGRAMS

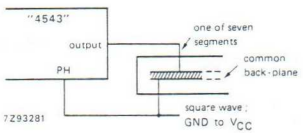


Fig. 8 Connection to liquid crystal (LCD) display readout.

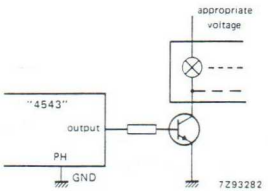


Fig. 9 Connection to incandescent display readout.

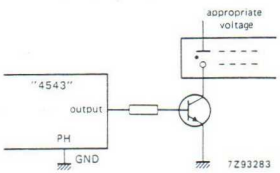


Fig. 10 Connection to gas discharge display readout.

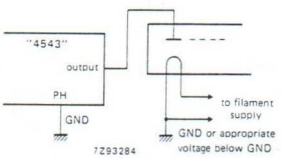


Fig. 11 Connection to fluorescent display readout.

AC WAVEFORMS

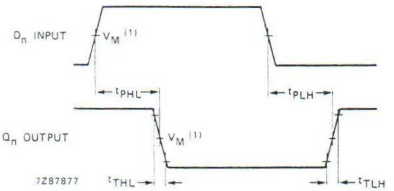


Fig. 12 Waveforms showing the address input (D_n) to output (Q_n) propagation delays and the output transition times.

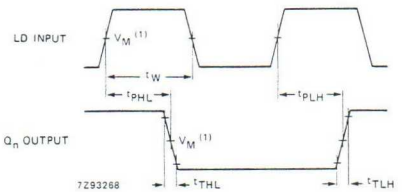


Fig. 13 Waveforms showing the latch disable input (LD) to output (Q_n) propagation delays and the output transition times.

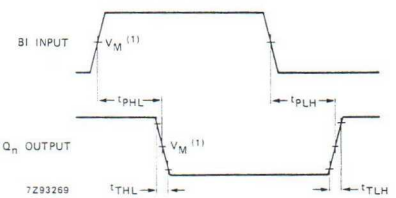


Fig. 14 Waveforms showing the blanking (BI) to output (Q_n) propagation delays and the output transition times.

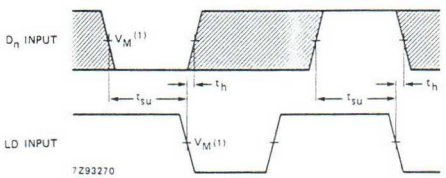


Fig. 15 Waveforms showing the address (D_n) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Programmable delay timer with oscillator

74HC/HCT5555

FEATURES

- Positive and negative edge triggered
- Retriggerable or non-retriggerable
- Programmable delay

  minimum: 100 ns

  maximum: depends on input frequency and division ratio
- Divide-by range of 2 to 2^{24}
- Direct reset terminates output pulse
- Very low power consumption in triggered start mode
- 3 oscillator operating modes:
  - RC oscillator
  - Crystal oscillator
  - External oscillator
- Device is unaffected by variations in temperature and V_{CC} when using an external oscillator
- Automatic power-ON reset
- Schmitt trigger action on both trigger inputs
- Direct drive for a power transistor
- Low power consumption in active mode with respect to TTL type timers
- High precision due to digital timing
- Output capability: 20 mA
- I_{CC} category: MSI.

APPLICATIONS

- Motor control
- Attic fan timers
- Delay circuits
- Automotive applications
- Precision timing
- Domestic appliances.

GENERAL DESCRIPTION

The 74HC/HCT5555 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT5555 are precision programmable delay timers which consist of:

- 24-stage binary counter
- integrated oscillator (using external timing components)
- retriggerable/non-retriggerable monostable
- automatic power-ON reset
- output control logic
- oscillator control logic
- overriding assynchronous master reset (MR).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
t_{PHL}/t_{PLH}	propagation delay A, $\overline{B}$ to Q/$\overline{Q}$ MR to Q/$\overline{Q}$ RS to Q/$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	24 19 26	24 20 28	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	23	36	pF

Notes

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} - 1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT5555N	16	DIL	plastic	SOT38Z
74HC/HCT5555D	16	SO16	plastic	SOT109A

PINNING

SYMBOL	PIN	DESCRIPTION
RS	1	clock input/oscillator pin
R_{TC}	2	external resistor connection
C_{TC}	3	external capacitor connection
A	4	trigger input (positive-edge triggered)
$\overline{B}$	5	trigger input (negative-edge triggered)
RTR/$\overline{RTR}$	6	retriggerable/non-retriggerable input (active HIGH/active LOW)
$\overline{Q}$	7	pulse output (active LOW)
GND	8	ground (0 V)
Q	9	pulse output (active HIGH)
S_0 - S_3	10, 11, 12, 13	programmable input
OSC CON	14	oscillator control
MR	15	master reset input (active HIGH)
V_{CC}	16	positive supply voltage

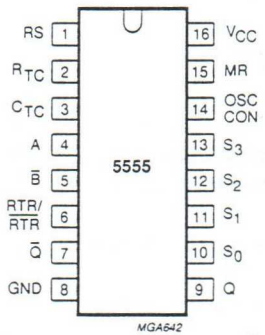


Fig.1 Pin configuration.

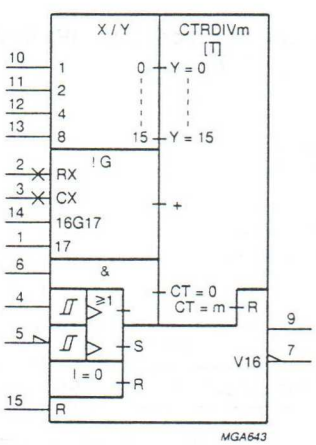


Fig.2 IEC logic diagram.

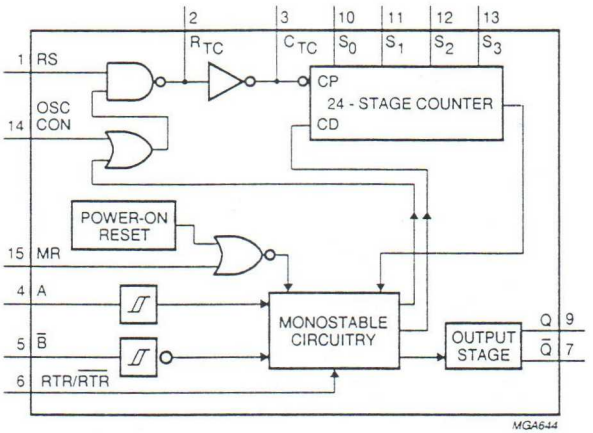


Fig.3 Functional diagram.

FUNCTIONAL DESCRIPTION

The oscillator configuration allows the design of RC or crystal oscillator circuits. The device can operate from an external clock signal applied to the RS input (R_{TC} and C_{TC} must not be connected). The oscillator frequency is determined by the external timing components (R_T and C_T), within the frequency range 1 Hz to 4 MHz (32 kHz to 20 MHz with crystal oscillator).

In the HCT version the MR input is TTL compatible but the RS input has CMOS input switching levels. The RS input can be driven by TTL input levels if RS is tied to V_{CC} via a pull-up resistor.

The counter divides the frequency to obtain a long pulse duration. The 24-stage is digitally programmed via the select inputs (S_0 to S_3). Pin S_3 can also be used to select the test mode, which is a convenient way of functionally testing the counter.

The "5555" is triggered on either the positive-edge, negative-edge or both.

- Trigger pulse applied to input A for positive-edge triggering
- Trigger pulse applied input $\overline{B}$ for negative-edge triggering
- Trigger pulse applied to inputs A and $\overline{B}$ (tied together) for both positive-edge and negative triggering.

The Schmitt trigger action in the trigger inputs, transforms slowly changing input signals into sharply defined jitter-free output signals and provides the circuit with excellent noise immunity.

The OSC CON input is used to select the oscillator mode, either continuously running (OSC CON = HIGH) or triggered start mode (OSC CON = LOW). The continuously running mode is selected where a start-up delay is an undesirable feature and the triggered start mode is selected where very low power consumption is the primary concern.

The start of the programmed time delay occurs when output Q goes HIGH (in the triggered start mode, the previously disabled oscillator will start-up). After the programmed time delay, the flip-flop stages are reset and the output returns to its original state.

An internal power-on reset is used to reset all flip-flop stages.

The output pulse can be terminated by the assynchronous overriding master reset (MR), this results in all flip-flop stages being reset. The output signal is capable of driving a power transistor. The output time delay is calculated using the following formula (minimum time delay is 100 ns):

$$\frac{1}{f_i} \times \text{division ratio (s)}.$$

Once triggered, the output width may be extended by retriggering the gated, active HIGH-going input A or the active LOW-going input $\overline{B}$. By repeating this process, the output pulse period (Q = HIGH, $\overline{Q}$ = LOW) can be made as long as desired. This mode is selected by RTR/$\overline{RTR}$ = HIGH. A LOW on RTR/$\overline{RTR}$ makes, once triggered, the outputs (Q, $\overline{Q}$) independent of further transitions of inputs A and $\overline{B}$.

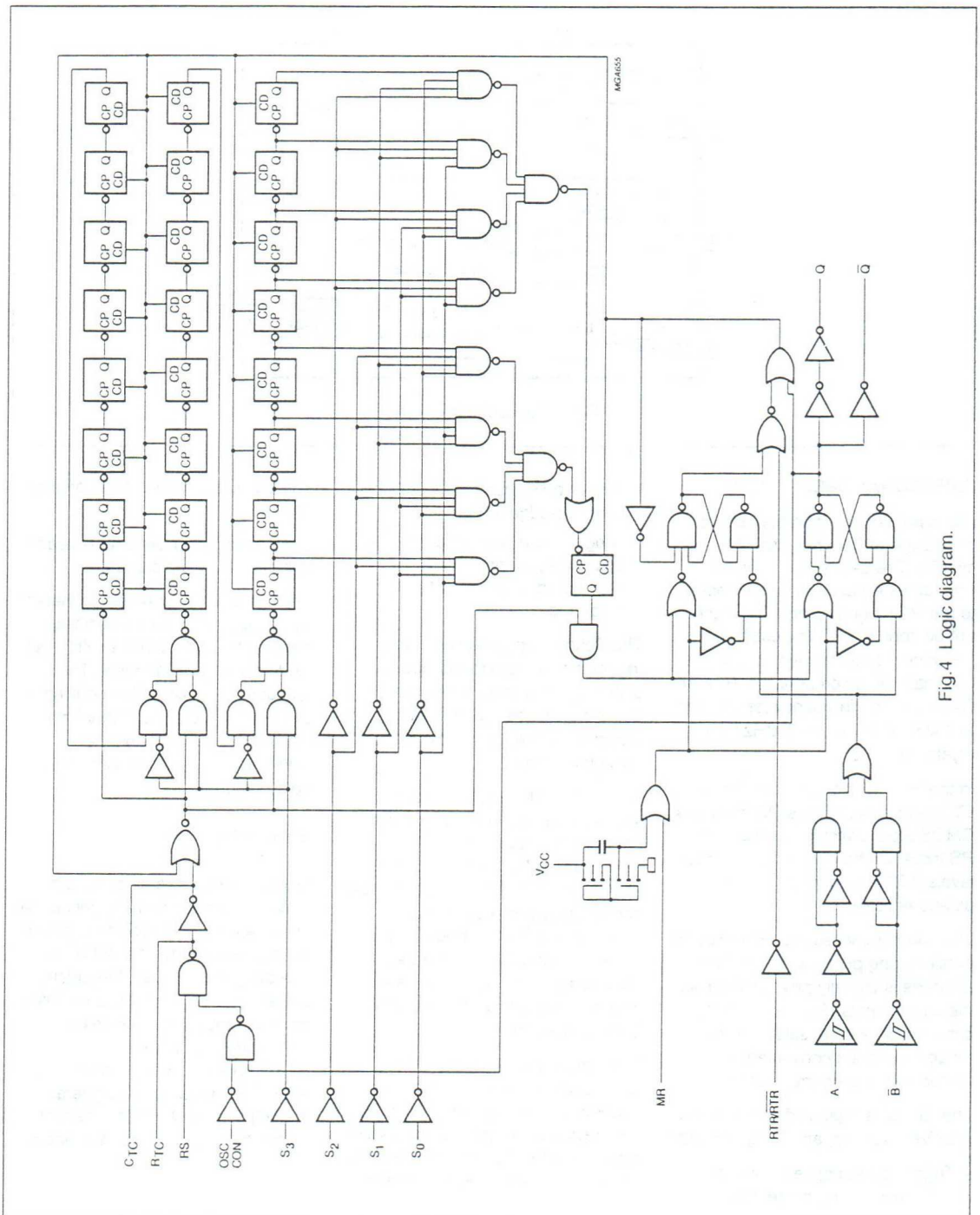


Fig.4 Logic diagram.

TEST MODE

Set S_3 to a logic LOW level, this will divide the 24 stage counter into three, parallel clocking, 8-stage counters. Set S_0, S_1 and S_2 to a logic HIGH level, this programs the counter to divide-by 2^8 (256). Apply a trigger pulse and clock in 255 pulses, this sets all flip-flop stages to a logic HIGH level. Set S_3 to a logic HIGH level, this causes the counter to divide-by 2^{24}. Clock one more pulse into the RS input, this causes a logic 0 to ripple through the counter and output $Q/\overline{Q}$ goes from HIGH-to-LOW level. This method of testing the delay counter is faster than clocking in 2^{24} (16 777 216) clock pulses.

FUNCTION TABLE

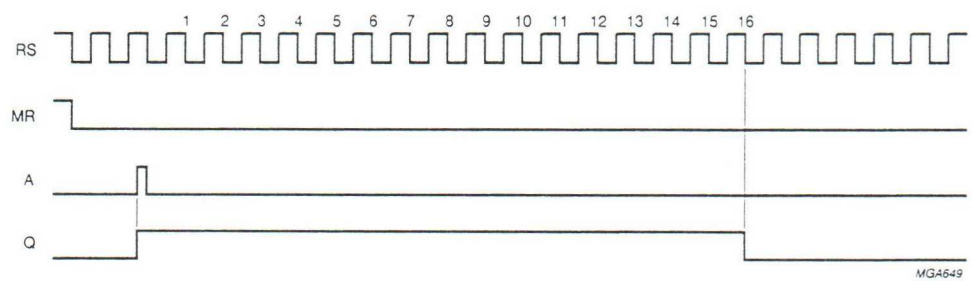
INPUTS			OUTPUTS	
MR	A	$\overline{B}$	Q	$\overline{Q}$
H	X	X	L	H
L	↑	X	one HIGH level output pulse	one LOW level output pulse
L	X	↓	one HIGH level output pulse	one LOW level output pulse

Notes

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition.

DELAY TIME SELECTION

SELECT INPUTS				OUTPUT Q/$\overline{Q}$ (FREQUENCY DIVIDING)	
S_3	S_2	S_1	S_0	BINARY	DECIMAL
L	L	L	L	2^1	2
L	L	L	H	2^2	4
L	L	H	L	2^3	8
L	L	H	H	2^4	16
L	H	L	L	2^5	32
L	H	L	H	2^6	64
L	H	H	L	2^7	128
L	H	H	H	2^8	256
.	.	.	.	.	.
H	L	L	L	2^{17}	131 072
H	L	L	H	2^{18}	262 144
H	L	H	L	2^{19}	524 288
H	L	H	H	2^{20}	1 048 576
H	H	L	L	2^{21}	2 097 152
H	H	L	H	2^{22}	4 194 304
H	H	H	L	2^{23}	8 388 608
H	H	H	H	2^{24}	16 777 216



Timing example shown for S_3, S_2, S_1, S_0 = 0011 (binary 2^4, decimal 16).

Fig.5 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI.

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	1.9 4.4 5.9	2 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0		I_O = −20 μA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.98 5.48	4.32 5.81	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0		I_O = −6.0 mA I_O = −7.8 mA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.3 4.8	– –	– –	3 4.5	– –	2.7 4.2	– –	V V	4.5 6.0		I_O = −20 mA I_O = −20 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0		I_O = 20 μA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– –	0.15 0.15	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	V V	4.5 6.0		I_O = 6.0 mA I_O = 7.8 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– –	– –	0.9 0.9	– –	1.14 1.14	– –	1.34 1.34	V V	4.5 6.0		I_O = 20 mA I_O = 25 mA
V_{IH}	HIGH level input voltage RS input	1.7 3.6 4.8	– – –	– – –	1.7 3.6 4.8	– – –	1.7 3.6 4.8	– – –	V V V	2 4.5 6.0		
V_{IL}	LOW level input voltage RS input	– – –	– – –	0.3 0.9 1.2	– – –	0.3 0.9 1.2	– – –	0.3 0.9 1.2	V V V	2.0 4.5 6.0		

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage R_{TC} output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = GND; OSC CON = V_{CC}	I_o = −2.6 mA I_o = −3.3 mA
		3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = V_{CC}; OSC CON = GND; untriggered	I_o = −0.65mA I_o = −0.85mA
		1.9 4.4 5.9	2.0 4.5 6	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	RS = V_{CC}; OSC CON = V_{CC}	I_o = −20 µA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2 4.5 6.0	RS = V_{CC}; OSC CON = GND; untriggered	I_o = −20 µA
V_{OH}	HIGH level output voltage C_{TC} output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = V_{IH}; OSC CON = V_{IH}	I_o = −3.2 mA I_o = −4.2 mA
V_{OL}	LOW level output voltage R_{TC} output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6	RS = V_{CC}; OSC CON = V_{CC}	I_o = 2.6 mA I_o = 3.3 mA
		– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6	RS = V_{CC}; OSC CON = V_{CC}	I_o = 20 µA
V_{OL}	LOW level output voltage C_{TC} output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	RS = V_{IL}; OSC CON = V_{IL}; untriggered	I_o = 3.2 mA I_o = 4.2 mA

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PLH}/t_{PHL}	propagation delay A, $\overline{B}$ to Q, $\overline{Q}$	– – –	77 28 22	240 48 41	– – –	300 60 51	– – –	360 72 61	ns ns ns	2.0 4.5 6.0	Fig.6
t_{PLH}/t_{PHL}	propagation delay MR to Q, $\overline{Q}$	– – –	61 22 18	185 37 31	– – –	230 46 39	– – –	280 56 48	ns ns ns	2.0 4.5 6.0	Fig.7
t_{PLH}/t_{PHL}	propagation delay RS to Q, $\overline{Q}$	– – –	83 30 24	250 50 43	– – –	315 63 54	– – –	375 75 64	ns ns ns	2.0 4.5 6.0	Fig.8; note 1
t_{THL}/t_{TLH}	output transition time	– – –	19 7 6	75 15 13	– – –	95 19 16	– – –	110 22 19	ns ns ns	2.0 4.5 6.0	Fig.6
t_W	trigger pulse width A = HIGH $\overline{B}$ = LOW	70 14 12	17 6 5	– – –	90 18 15	– – –	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width HIGH	70 14 12	19 7 6	– – –	90 18 15	– –	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.7
t_W	clock pulse width RS; HIGH or LOW	80 16 14	25 9 7	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.8
t_W	minimum output pulse width Q = HIGH, $\overline{Q}$ = LOW	– – –	275 100 80	– – –	– – –	– – –	– – –	– – –	ns ns ns	2.0 4.5 6.0	Fig.6; note 1
t_{rt}	retrigger time A, $\overline{B}$	– – –	0 0 0	– – –	– – –	– – –	– – –	– – –	ns ns ns	2.0 4.5 6.0	Fig.10; note 2
R_{EXT}	external timing resistor	5 1	– –	1000 1000	– –	– – –	– –	– – –	kΩ kΩ	2.0 5.0	Fig.13
C_{EXT}	external timing capacitor	50 50	no limits						pF pF	2.0 5.0	Fig.13
t_{rem}	removal time MR to A, $\overline{B}$	120 24 20	39 14 11	– – –	150 30 26	– – –	180 36 31	– – –	ns ns ns	2.0 4.5 6.0	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f_{max}	maximum clock pulse frequency	2	5.9	–	1.8	–	1.3	–	MHz	2.0	Fig.8; note 3
		10	18	–	8	–	6.6	–	MHz	4.5	
		12	21	–	10	–	8	–	MHz	6.0	
f_{max}	maximum clock pulse frequency	6	24.8	–	4.8	–	4	–	MHz	2.0	Fig.9; note 4
		30	75	–	24	–	20	–	MHz	4.5	
		35	89	–	28	–	24	–	MHz	6.0	

Notes to the AC Characteristics

1. One stage selected.
2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
3. One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specification".

Output capability: non-standard; bus driver with extended specification on V_{OH} and V_{OL}
I_{CC} category: MSI.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	4.4	4.5	–	4.4	–	4.4	–	V	4.5		I_O = −20 µA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.98	4.32	–	3.84	–	3.7	–	V	4.5		I_O = −6 mA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.3	–	–	3	–	2.7	–	V	4.5		I_O = −20 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	0	0.1	–	0.1	–	0.1	V	4.5		I_O = 20 µA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	0.15	0.26	–	0.33	–	0.40	V	4.5		I_O = 6 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	–	0.9	–	1.14	–	1.34	V	4.5	–	I_O = 20 mA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage R_{TC} output	3.98	–	–	3.84	–	3.7	–	V	4.5	RS = GND; OSC CON = V_{CC}	I_o = −2.6 mA
		3.98	–	–	3.84	–	3.7	–	V	4.5	RS = V_{CC}; OSC CON = GND; untriggered	I_o = −0.65 mA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = −20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	RS = V_{CC}; OSC CON = GND; untriggered	I_o = −20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98	–	–	3.84	–	3.7	–	V	4.5	RS = V_{IH}; OSC CON = V_{IH}	I_o = −3.2 mA
V_{OL}	LOW level output voltage R_{TC} output	–	–	0.26	–	0.33	–	0.4	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = 2.6 mA
		–	0	0.1	–	0.1	–	0.1	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = 20 μA
V_{OL}	LOW level output voltage C_{TC} output	–	–	0.26	–	0.33	–	0.4	V	4.5	RS = V_{IL}; OSC CON = V_{IL}; untriggered	I_o = 3.2 mA

Notes to HCT DC Characteristics

1. The RS input has CMOS input switching levels.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
MR	0.35
A	0.69
$\overline{B}$	0.50
RTR/$\overline{RTR}$	0.35
OSC CON	1.20
S_0 - S_2	0.65
S_3	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PLH}/t_{PHL}	propagation delay A, $\overline{B}$ to Q, $\overline{Q}$	–	28	48	–	60	–	72	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay MR to Q, $\overline{Q}$	–	24	41	–	51	–	62	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay RS to Q, $\overline{Q}$	–	32	54	–	68	–	81	ns	4.5	Fig.8; note 1
t_{THL}/t_{TLH}	output transition time	–	7	15	–	19	–	22	ns	4.5	Fig.6
t_W	trigger pulse width A = HIGH $\overline{B}$ = LOW	21	12	–	26	–	32	–	ns	4.5	Fig.6
t_W	master reset pulse width HIGH	14	5	–	18	–	21	–	ns	4.5	Fig.7
t_W	clock pulse width RS; HIGH or LOW	16	9	–	20	–	24	–	ns	4.5	Fig.8
t_W	minimum output pulse width Q = HIGH, $\overline{Q}$ = LOW	–	100	–	–	–	–	–	ns	4.5	Fig.6
t_{rt}	retrigger time A, $\overline{B}$	–	0	–	–	–	–	–	ns	4.5	Fig.10; note 2

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
R_{EXT}	external timing resistor	1	–	1000	–	–	–	–	kΩ	4.5	Fig.13
C_{EXT}	external timing capacitor	50	no limits						pF	4.5	Fig.13
t_{rem}	removal time MR to A, $\overline{B}$	24	14	–	30	–	36	–	ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	10	18	–	8	–	6.6	–	MHz	4.5	Fig.8; note 3
f_{max}	maximum clock pulse frequency	30	75	–	24	–	20	–	MHz	4.5	Fig.9; note 4

Notes to HCT AC characteristics

1. One stage selected.
2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
3. One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

AC WAVEFORMS

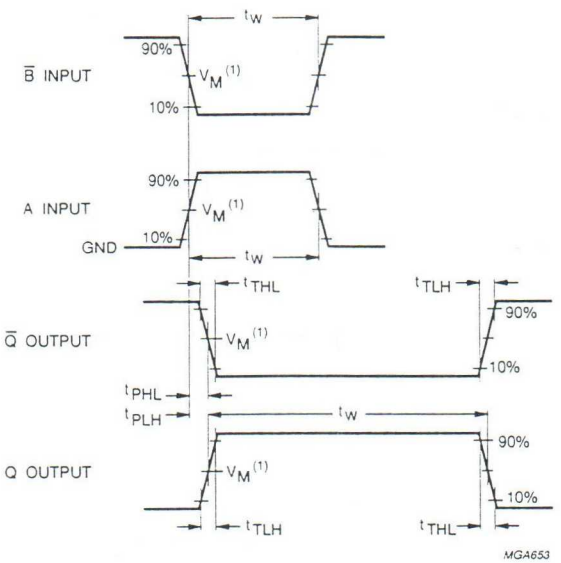


Fig.6 Waveforms showing the triggering of the delay timer by input A or $\overline{B}$, the minimum pulse widths of the trigger inputs A and $\overline{B}$, the output pulse width and output transition times.

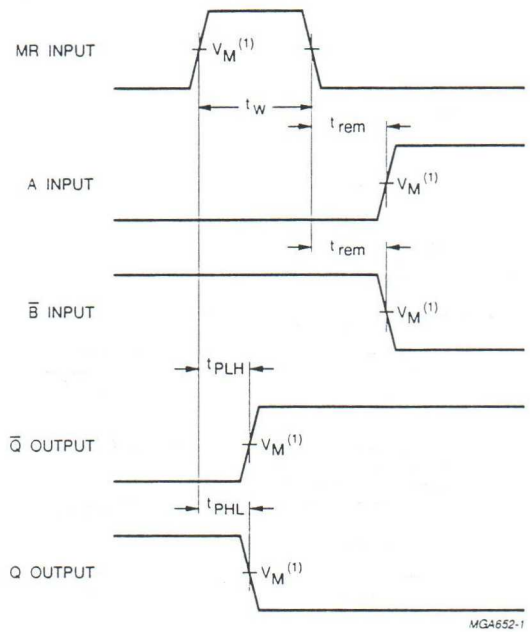


Fig.7 Waveforms showing the master reset (MR) pulse width, the master reset to outputs (Q and $\overline{Q}$) propagation delays and the master reset to trigger inputs (A and $\overline{B}$) removal time.

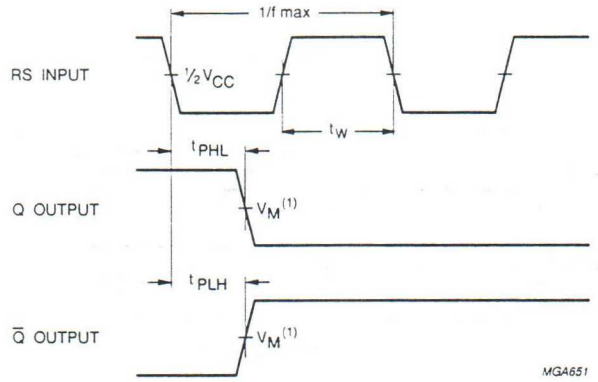


Fig.8 Waveforms showing the clock (RS) to outputs (Q and $\overline{Q}$) propagation delays, the clock pulse width and the maximum clock frequency.

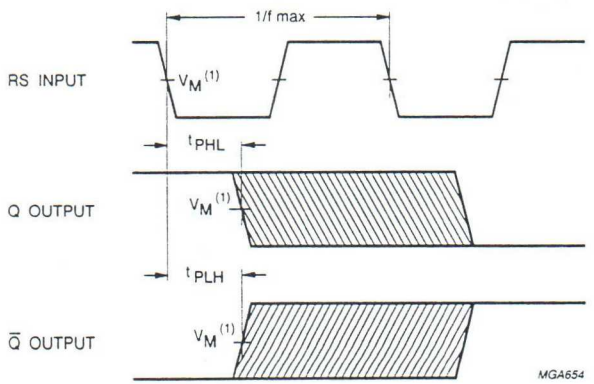


Fig.9 Waveforms showing the clock (RS) to outputs (Q and $\overline{Q}$) propagation delays, the clock pulse width and the maximum clock frequency (Output waveforms are not synchronized with respect to the RS waveform).

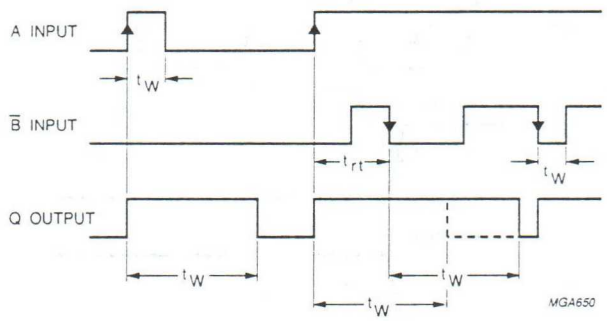


Fig.10 Output pulse control using retrigger pulse (RTR/$\overline{RTR}$ = HIGH).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

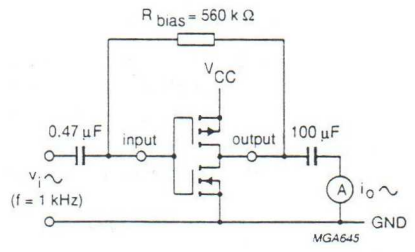


Fig.11 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see Fig.12) and MR = LOW.

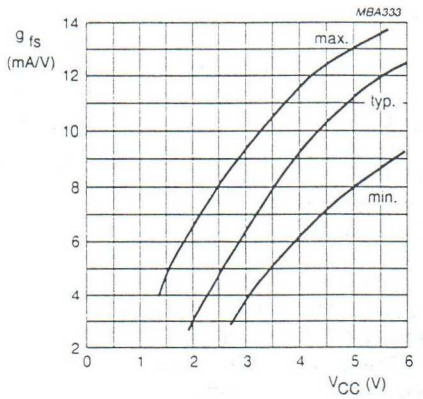
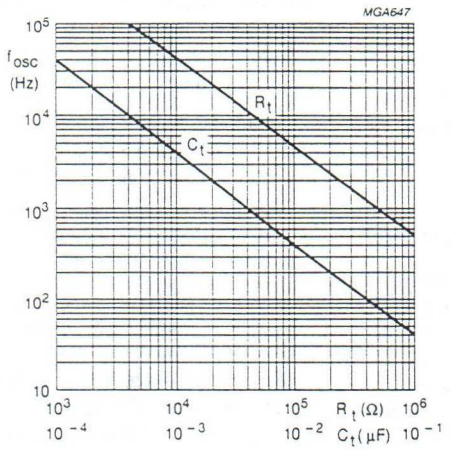


Fig.12 Typical forward transconductance g_{fs} as a function of the supply voltage at V_{CC} at T_{amb} = 25 °C.

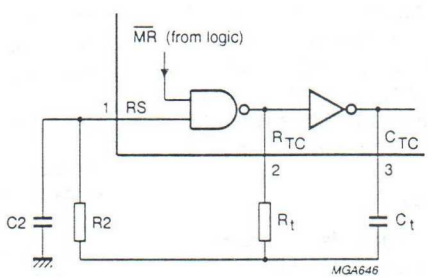


C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.

R_t curve at C_t = 1 nF; R2 = 2 x R_t.

RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2 to 6 V; T_{amb} = 25 °C.

Fig.13 Application information.



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

Fig.14 Example of an RC oscillator.

Timing Component Limitations

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ $2R_t$ and $R2C2 \ll R_tC_t$. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is 280 Ω at V_{CC} = 2 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6 V. The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t > 50$ pF, up to any practical value, 10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, $R_t \gg 1$ kΩ.

Typical Crystal Oscillator

In Fig.15, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ. Above 14 MHz it is recommended replacement of R2 by a capacitor with a typical value of 35 pF.

Accuracy

Device accuracy is very precise for long time delays and has an accuracy of better than 1% for short time delays (1% applies to values ≥400 ns). Tolerances are dependent on the external components used, either RC network or crystal oscillator.

Start-up Using External Clock

The start of the timing pulse is initiated directly by the trigger pulse (assynchronously with respect to the oscillator clock). Triggering on a clock HIGH or clock LOW results in the following:

- clock = HIGH; the timing pulse may be lengthened by a maximum of $t_w/2$ (t_w = clock pulse width)
- clock = LOW; the timing pulse may be shortened by a maximum of $t_w/2$ (t_w = clock pulse width).

This effect can be minimized by selecting more delay stages. When using only one or two delay stages, it is recommended to use an external time base that is synchronized with the negative-edge of the clock.

Start-up Using RC Oscillator

The first clock cycle is ≈35% of a time period too long. This effect can also be minimized by selecting more delay stages.

Start-up Using Crystal Oscillator

A crystal oscillator requires at least two clock cycles to start-up plus an unspecified period (ms) before the amplitude of the clock signal increases to its expected level. Although this device also operates at lower clock amplitudes, it is recommended to select the continuously running mode (OSC CON = HIGH) to prevent start-up delays.

Termination of the Timing Pulse

The end of the timing pulse is synchronized with the falling edge of the oscillator clock. The timing pulse may lose synchronization under the following conditions:

- high clock frequency and large number of stages are selected. This depends on the dynamic relationship that exists between the clock frequency and the ripple through delay of the subsequent stages.

Synchronization

When frequencies higher than those specified in the Table 'Synchronization limits' are used, the termination of timing pulse will lose synchronization with the falling edge of the oscillator. The unsynchronized timing pulse introduces errors, which can be minimized by increasing the number of stages used e.g. A 20 MHz clock frequency using all 24 stages will result in a frequency division of 16 777 225 instead of 16 777 216, an error of 0.0005%.

The amount of error increases at high clock frequencies as the number of stages decrease. A clock frequency of 40 MHz and 4 stages selected results in a division of 18 instead of 16, a 12.5% error. Application example:

- If a 400 ns timing pulse was required it would be more accurate to utilize a 5 MHz clock frequency using 1 stage or a 10 MHz clock frequency using 2 stages (due to synchronization with falling edge of the oscillator) than a 40 MHz clock frequency and 4 stages (synchronization is lost).

Minimum Output Pulse Width

The minimum output pulse width is determined by the minimum clock pulse width, plus the maximum propagation delay of A, $\overline{B}$ to Q. The rising edge of Q is dominated by the A, $\overline{B}$ to Q propagation delay, while the falling edge of Q is dominated by RS to Q propagation delay. These propagation delays are not equal.

The RS to Q propagation delay is some what longer, resulting in inaccurate outputs for extremely short pulses. The propagation delays are listed in the section 'AC Characteristics'. With these numbers it is possible to calculate the maximum deviation (an example is shown in Fig.16). Figure 16 is valid for an external clock where the trigger is synchronized to the falling edge of the clock only. The graph shows that the minimum programmed pulse width of 100 ns is:

- minimum of 4% too long
- typically 7% too long
- maximum of 10% too long.

SYNCHRONIZATION LIMITS

NUMBER OF STAGES SELECTED	CLOCK FREQUENCY (TYPICAL)
1	18 MHz
2	14 MHz
3	11 MHz
4	9.6 MHz
5	8.3 MHz
6	7.3 MHz
7	6.6 MHz
8	6 MHz
.	.
17	3.2 MHz
18	3.0 MHz
19	2.9 MHz
20	2.8 MHz
21	2.7 MHz
22	2.6 MHz
23	2.5 MHz
24	2.4 MHz

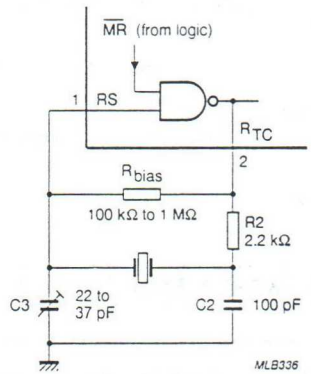


Fig.15 External components configuration for a crystal oscillator.

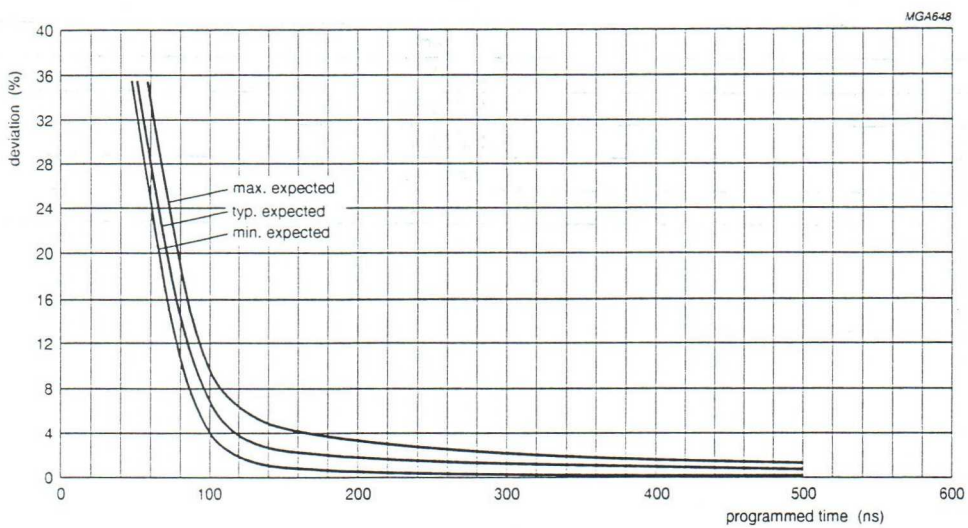


Fig.16 Graphic representation of short time delay accuracy; one stage selected; V_{CC} = 4.5 V.

Programmable ripple counter with oscillator; 3-state

74HC/HCT6323A

FEATURES

- 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 50 MHz (V_{CC} = 5 V ± 10%)
- 3-state output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3 to 6 V
- Oscillator stop function ($\overline{MR}$)
- Output capability: bus driver → (15 LSTTL)
- I_{CC} category: MSI.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation.

GENERAL DESCRIPTION

The HC/HCT6323A are high-speed Si-gate CMOS devices.
They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT6323A are oscillators designed for quartz crystal combined with a programmable 3-state counter, a 3-state output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-by-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator and sets the output buffer in the 3-state condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive. In the HCT version, the $\overline{MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay X1 to OUT (S1 = S2 = LOW)	C_L = 15 pF; V_{CC} = 5 V	17	17	ns
f_{max}	maximum clock frequency		90	90	MHz
C_I	input capacitance except X1 and X2		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	÷1; notes 1 and 2	54	54	pF
		÷2; notes 1 and 2	42	42	pF
		÷4; notes 1 and 2	36	36	pF
		÷8; notes 1 and 2	33	33	pF

Notes

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$$

where:

f_i = input frequency in MHz.
f_o = output frequency in MHz.
V_{CC} = supply voltage in V.
C_L = output load capacitance in pF.
$I_{pull\text{-}up}$ = pull-up currents in µA.

For HC and HCT an external clock is applied to X1 with:
$t_r = t_f \leq 6$ ns, V_i is GND to V_{CC}, $\overline{MR}$ = HIGH
$I_{pull\text{-}up}$ is the summation of $-I_I$ (µA) of S1 and S2 inputs at the LOW state.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT6323AD	8	SO	plastic	SOT96

Programmable ripple counter with oscillator; 3-state

74HC/HCT6323A

PINNING

SYMBOL	PIN	DESCRIPTION
OUT	1	counter output
S1 - S2	3, 2	mode select inputs for divide by 1, 2, 4 or 8
GND	4	ground (0 V)
$\overline{MR}$	5	master reset (active LOW)
X2	6	oscillator pin
X1	7	clock input/oscillator pin
V_{CC}	8	positive supply

FUNCTION TABLE

INPUTS		OUTPUTS
S1	S2	OUT
0	0	f_i
0	1	$f_i/2$
1	0	$f_i/4$
1	1	$f_i/8$

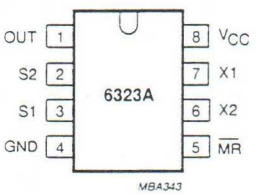


Fig.1 Pin configuration.

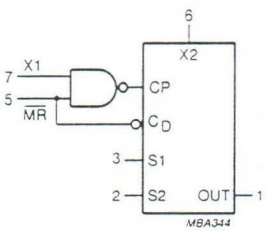


Fig.2 IEC logic symbol.

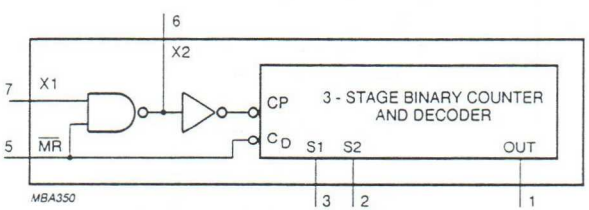
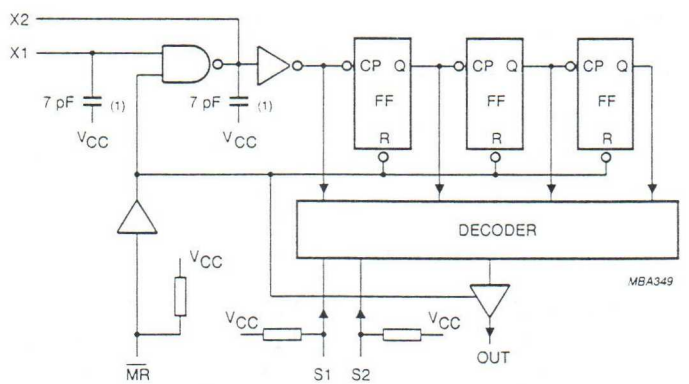


Fig.3 Functional diagram.



Internal capacitors typical 7 pF each. Including stray capacitors on pin X1 and X2, total capacitance will be typical 12 pF per pin.

Fig.4 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family Characteristics", section "Family Specifications".

Output capability: non-standard; bus driver (except for X2)
I_{CC} category: MSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	HIGH level input voltage $\overline{MR}$, X1 input	1.5	1.2	–	1.5	–	1.50	–	V	2.0		
		3.15	2.4	–	3.15	–	3.15	–	V	4.5		
		4.2	3.2	–	4.2	–	4.20	–	V	6.0		
V_{IL}	LOW level input voltage $\overline{MR}$, X1 input	–	0.8	0.5	–	0.5	–	0.5	V	2.0		
		–	2.1	1.35	–	1.35	–	1.35	V	4.5		
		–	2.8	1.80	–	1.8	–	1.8	V	6.0		

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage X2 output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = −2.6 mA I_O = −3.3 mA
		3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −2.6 mA I_O = −3.3 mA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	X1 = GND and $\overline{MR}$ = V_{CC}	$-I_O$ = 20 µA I_O = −20 µA I_O = −20 µA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −20 µA I_O = −20 µA I_O = −20 µA
V_{OH}	HIGH level output voltage OUT	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = −20 µA I_O = −20 µA I_O = −20 µA
V_{OH}	HIGH level output voltage OUT	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = −6 mA I_O = −7.8 mA
V_{OL}	LOW level output voltage X2 output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 2.6 mA I_O = 3.3 mA
		– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 20 µA I_O = 20 µA I_O = 20 µA
V_{OL}	LOW level ouput voltage OUT	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 µA I_O = 20 µA I_O = 20 µA
V_{OL}	LOW level output voltage OUT	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = 6 mA I_O = 7.8 mA
$\pm I_{LI}$	input leakage current X1	–	–	0.1	–	1	–	1	µA	6.0	$\overline{MR}$ = V_{CC} S1 = V_{CC} S2 = V_{CC}	
$-I_I$	input pull-up current S1, S2 and $\overline{MR}$	5	30	100	–	–	–	–	µA	6.0	GND	see Fig.11 and Fig.12
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	µA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 1	–	61	185	–	230	–	275	ns	2.0	Fig.7	S1 = GND S2 = GND
		–	22	37	–	46	–	55	ns	4.5		
		–	19	31	–	39	–	47	ns	6.0		
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 2	–	74	235	–	290	–	350	ns	2.0	Fig.7	S1 = GND S2 = V_{CC}
		–	27	47	–	58	–	70	ns	4.5		
		–	23	40	–	49	–	60	ns	6.0		
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 4	–	91	285	–	355	–	425	ns	2.0	Fig.7	S1 = V_{CC} S2 = GND
		–	33	57	–	71	–	85	ns	4.5		
		–	28	48	–	60	–	72	ns	6.0		
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide by 8	–	105	335	–	415	–	500	ns	2.0	Fig.7	S1 = V_{CC} S2 = V_{CC}
		–	38	67	–	83	–	100	ns	4.5		
		–	32	57	–	71	–	85	ns	6.0		
t_{PLZ}/t_{PHZ}	3-state output disable time $\overline{MR}$ to OUT	–	75	150	–	185	–	225	ns	2.0	Fig.8	
		–	15	30	–	37	–	45	ns	4.5		
		–	13	26	–	31	–	38	ns	6.0		
t_{PZL}	3-state output enable time $\overline{MR}$ to OUT	–	36	150	–	185	–	225	ns	2.0	Fig.8	
		–	13	30	–	37	–	45	ns	4.5		
		–	11	26	–	31	–	38	ns	6.0		
t_{PZH}	3-state output enable time $\overline{MR}$ to OUT	–	61	200	–	250	–	300	ns	2.0	Fig.8	note 1
		–	22	40	–	50	–	60	ns	4.5		
		–	19	34	–	43	–	51	ns	6.0		
t_{THL}/t_{TLH}	output transition time	–	14	60	–	75	–	90	ns	2.0	Fig.7	
		–	5	12	–	15	–	19	ns	4.5		
		–	4	10	–	13	–	15	ns	6.0		
t_W	clock pulse width X1, HIGH or LOW	50	17	–	60	–	75	–	ns	2.0	Fig.7	
		10	6.0	–	12	–	15	–	ns	4.5		
		9	5	–	10	–	13	–	ns	6.0		
t_W	master reset pulse width $\overline{MR}$; LOW	80	22	–	100	–	120	–	ns	2.0	Fig.9	
		16	8	–	20	–	24	–	ns	4.5		
		14	7	–	17	–	20	–	ns	6.0		
t_{rem}	removal time $\overline{MR}$ to X1	100	19	–	125	–	150	–	ns	2.0	Fig.9	
		20	7	–	25	–	30	–	ns	4.5		
		17	6.0	–	21	–	26	–	ns	6.0		
f_{max}	maximum clock pulse frequency	10	17	–	8	–	6.6	–	MHz	2.0	Fig.7	
		50	85	–	40	–	33	–	MHz	4.5		
		59	100	–	47	–	39	–	MHz	6.0		

Note to the 74HC AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications".

Output capability: bus driver (except for X2).

I_{CC} category: MS1.

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	HIGH level input voltage $\overline{MR}$, S1 and S2 inputs	2.0	–	–	2.0	–	2.0	–	V	4.5 to 5.5		
V_{IL}	LOW level input voltage $\overline{MR}$, S1 and S2 inputs	–	–	0.8	–	0.8	–	0.8	V	4.5 to 5.5		
V_{IH}	HIGH level input voltage X1 input	3.15 3.85	– –	– –	3.15 3.85	– –	3.15 3.85	– –	V V	4.5 5.5		
V_{IL}	LOW level input voltage X1 input	– –	– –	1.35 1.65	– –	1.35 1.65	– –	1.35 1.65	V V	4.5 5.5		
V_{OH}	HIGH level output voltage X2 output	3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = −2.6 mA
		3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −2.6 mA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	X1 = GND and $\overline{MR}$ = V_{CC}	I_O = −20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	X1 = V_{CC} and $\overline{MR}$ = GND	I_O = −20 mA
V_{OH}	HIGH level output voltage OUT	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage OUT	3.98	–	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −6 mA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OL}	LOW level output voltage X2 output	–	–	0.26	–	0.33	–	0.4	V	4.5	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 2.6 mA
		–	0	0.1	–	0.1	–	0.1	V	4.5	X1 = V_{CC} and $\overline{MR}$ = V_{CC}	I_O = 20 μA
V_{OL}	LOW level output voltage OUT	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage OUT	–	–	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6 mA
$\pm I_{LI}$	input leakage current	–	–	0.1	–	1.0	–	1.0	μA	5.5	$\overline{MR}$ = V_{CC}; S1 = V_{CC}; S2 = V_{CC}	
$-I_I$	input pull-up current S1, S2 and $\overline{MR}$	5	25	100	–	–	–	–	μA	5.5	GND	see Fig.11 and Fig.12
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1	–	100	360	–	450	–	490	μA	5.5	V_{CC} or GND	other inputs at V_{CC} or GND; I_O = 0; (note 1)

Note to the HCT DC Characteristics

1. The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$, S1, S2	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-1	–	24	40	–	50	–	60	ns	4.5	Fig.7	S1 = GND S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 to OUT divide-by-2	–	29	50	–	62	–	75	ns	4.5	Fig.7	S1 = GND S2 = V_{CC}
t_{PHL}/t_{PLH}	propagation delay X1 OUT to divide-by-4	–	35	60	–	75	–	90	ns	4.5	Fig.7	S1 = V_{CC} S2 = GND
t_{PHL}/t_{PLH}	propagation delay X1 OUT to divide-by-8	–	40	70	–	87	–	105	ns	4.5	Fig.7	S1 = V_{CC} S2 = V_{CC}
t_{PLZ}/t_{PHZ}	3-state output disable time $\overline{MR}$ to OUT	-	21	35	–	43	–	52	ns	4.5	Fig.8	
t_{PZ}	3-state output enable time $\overline{MR}$ to OUT	–	16	30	–	37	–	45	ns	4.5	Fig.8	
t_{PZH}	3-state output enable time $\overline{MR}$ to OUT	–	22	38	–	47	–	57	ns	4.5	Fig.8	see note 1
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	19	ns	4.5	Fig.7	
t_W	clock pulse width X1, HIGH or LOW	10	6	–	12	–	15	–	ns	4.5	Fig.7	
t_W	master reset pulse width $\overline{MR}$; LOW	16	8	–	20	–	24	–	ns	4.5	Fig.9	
t_{rem}	removal time $\overline{MR}$ to X1	24	12	–	30	–	36	–	ns	4.5	Fig.9	
f_{max}	maximum clock pulse frequency	50	85	–	40	–	33	–	MHz	4.5	Fig.7	

Note to the 74HCT AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

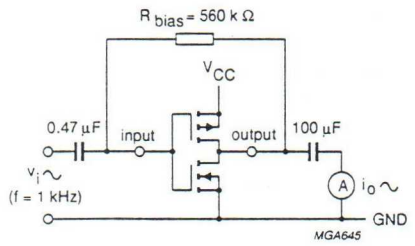


Fig.5 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also Fig.6); $\overline{MR}$ = HIGH.

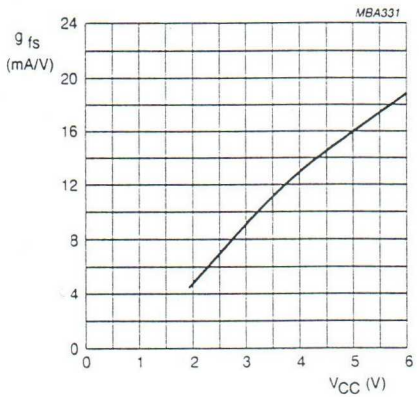


Fig.6 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

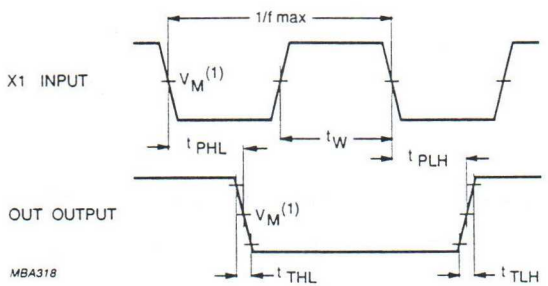


Fig.7 Waveforms showing the clock (X1) to output (OUT) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

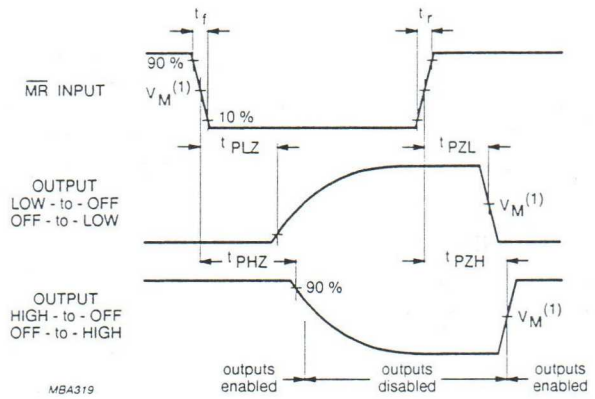


Fig.8 Waveforms showing the input $\overline{MR}$ to output OUT, 3-state enable and disable times.

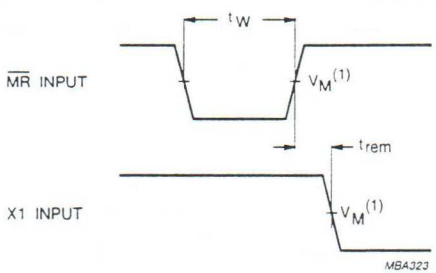
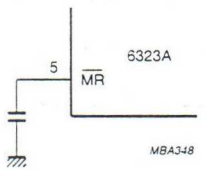


Fig.9 Waveforms showing the $\overline{MR}$ minimum pulse width and $\overline{MR}$ to X1 removal time.

Note to the AC waveforms

1. HC : V_M = 50%; V_I = GND to V_{CC}.
   HCT : V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION



The input pull-up current is used to create a power-on delay time at $\overline{MR}$.

Fig.10 Power-on reset.

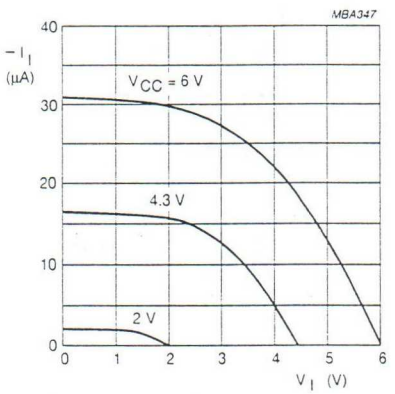


Fig.11 Typical input pull-up current as a function of the input voltage (V_I).

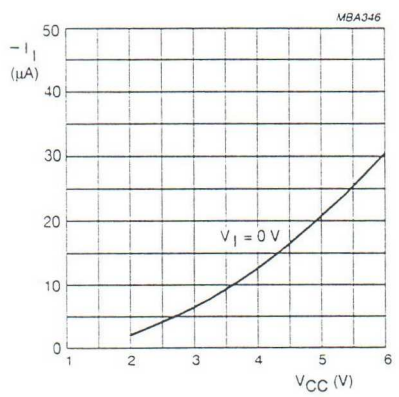


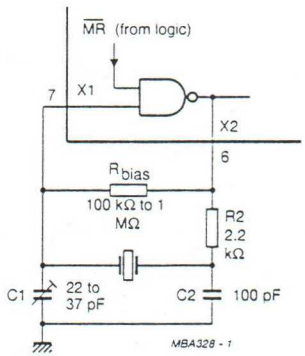
Fig.12 Typical input pull-up current as a function of the supply voltage (V_{CC}).

Table 1 Typical application values

f (MHz)	R2 (KΩ)	C1 (pF)	C2 (pF)
1	4.7	47 to 68	
10	2.2	47 to 68	
25	1	33	33

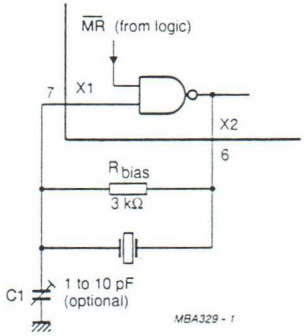
Table 2 Typical Application Values

f(MHz)	R_{bias} (KΩ)	C1(pF)
50	3.0	4.7



Above 5 MHz replace R2 by a capacitor of half the value of C2.
C_L at which a crystal is specified (or adjusted) equals for this application C1 . C2/C1 + C2.

Fig.13 Typical setup for a crystal oscillator operating in the fundamental mode (1 MHz to 25 MHz).



Applicable for third overtone crystals (lower damping resistance at the third harmonic frequency) at typical 50 MHz. For lower frequencies extra load capacitors must be supplied, or increase bias resistor.

Fig.14 Typical set-up for a crystal oscillator operating in the third overtone mode without the use of an inductor.

Typical Crystal Oscillator

In Fig.13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 KΩ.

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external components. There are two on-chip capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to run the oscillator in the third overtone without external capacitors applied. If a certain frequency is chosen, the IC parameters, as forward transconductance, and the crystal parameters such as the motional resistances R1 (fundamental), R3 (third overtone) and R5 (fifth overtone), are of paramount importance. Also the values of the external components as R_s (series resistance) and the crystal load capacitances play an important role. Especially in overtone mode oscillations, R_b (bias resistance) and the load capacitance values are very important.

Considerations for Fundamental Oscillator:

In the fundamental oscillator mode, the R_b has only the function of biasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. 100 kΩ up to 10 MΩ. The load capacitors C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load capacitance. C1 can be used to trim the oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in the crystal. R_s also suppresses overtone oscillations and introduces a phase shift over a broad frequency range. This is of less concern provided R_s is not too high a value.

Note

A combination of a small load capacitor value and a small series resistance, may cause a third overtone oscillation.

Considerations for Third-overtone Oscillator:

In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for third overtone can be too small for oscillation. A simple solution to suppress the fundamental oscillation, is to spoil the crystal fundamental activity. By dramatically reducing the value of the bias resistor of the inverting stage, and applying small load capacitors, it is possible to have an insufficient phase in the total loop for fundamental oscillation. However the phase for third overtone is good. It can be explained by the $R_b \times C_l$ time constant. During oscillation the crystal with the load capacitors cause a phase shift of 180°. Because R_b is parallel with the crystal (no R_s), R_b spoils the phase for fundamental. $R_b \times C_l$ must be of a value, that it is not spoiling the phase for third overtone too much. Because third overtone is a 3 times higher frequency than the fundamental, the $R_b \times C_l$ cannot 'maintain' the higher third overtone frequency, which results in a less spoiled overtone phase.

Hex non-inverting precision Schmitt-trigger — 74HC7014

FEATURES

- Operating voltage 3 to 6 V
- Output capability: standard
- category: SSI

APPLICATIONS

- Wave and pulse shapers for highly noisy environments

DESCRIPTION

The 74HC7014 is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no. 7A.

The 74HC7014 provides six precision Schmitt-triggers with non-inverting buffers. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. The precisely defined trigger levels are lying in a window between 0.55 x V_{CC} and 0.65 x V_{CC}. This makes the circuit suitable to operate in a highly noisy environment. Input shorts are allowed to −1.5 V and 16 V without disturbing other channels.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	L
H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
V_{T+}	positive going threshold	C_L = 50 pF; V_{CC} = 5 V	3.1	V
V_{T-}	negative going threshold		2.9	V
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	9	pF
I_{CC}	DC supply current		3.0	mA

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For HC the condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC7014P	14	DIL	plastic	SOT27
74HC7014T	14	SO	plastic	SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

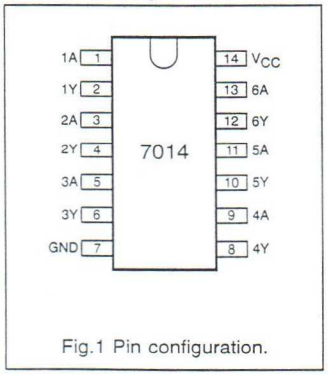


Fig.1 Pin configuration.

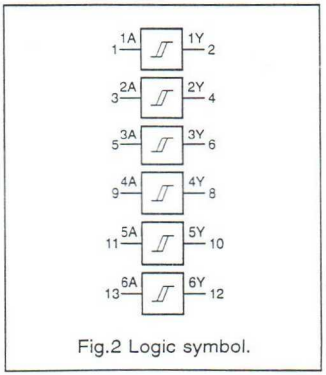


Fig.2 Logic symbol.

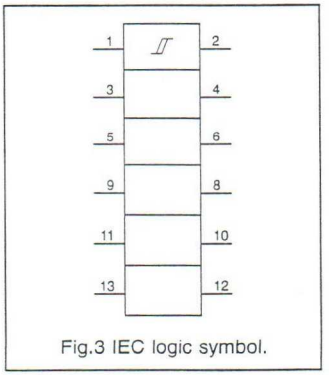


Fig.3 IEC logic symbol.

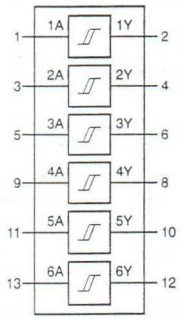


Fig.4 Functional diagram.

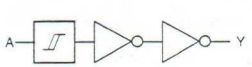


Fig.5 Logic diagram (one Schmitt-trigger).

DC CHARACTERISTICS FOR 74HC

For the DC output characteristics see chapter "HCMOS family characteristics", section "Family specifications". Except for recommended operating conditions the'7014' has a DC supply voltage from minimum 3 V to maximum 6 V.
Transfer characteristics are given below.

Output capability: standard
Category: SSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{T+}	positive-going threshold	–	1.86	1.95	–	1.95	–	1.95	V	3.00		Figs.6 and 7
		–	2.94	3.08	–	3.08	–	3.08		4.75		
		–	3.10	3.25	–	3.25	–	3.25		5.00		
		–	3.25	3.41	–	3.41	–	3.41		5.25		
		–	3.72	3.90	–	3.90	–	3.90		6.00		
V_{T-}	negative-going threshold	1.65	1.74	–	1.65	–	1.65	–	V	3.00		Figs.6 and 7
		2.62	2.76	–	2.62	–	2.62	–		4.75		
		2.75	2.90	–	2.75	–	2.75	–		5.00		
		2.89	3.05	–	2.89	–	2.89	–		5.25		
		3.30	3.48	–	3.30	–	3.30	–		6.00		
V_H	hysteresis ($V_{T+} - V_{T-}$)	50	120	–	50	–	50	–	mV	3.00		Figs.6 and 7
		100	180	–	100	–	100	–		4.75		
		120	200	–	120	–	120	–		5.00		
		130	210	–	130	–	130	–		5.25		
		160	240	–	160	–	160	–		6.00		
$\pm I_I$	input leakage current	–	–	0.1	–	1.0	–	1.0	µA	V_{CC} or GND		
		–	–	0.5	–	5.0	–	5.0	µA	16 V or GND		
I_{CC}	DC supply current	–	0.7	1.4	–	1.8	–	2.1	mA	3.00		
		–	3.0	6.0	–	7.5	–	7.5		5.25		
		–	3.7	7.4	–	10.0	–	13.0		6.00		

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}	propagation delay nA, nB to nY	–	95	475	–	600	–	715	ns	3.00	Fig.8
		–	38	115	–	145	–	175		4.75	
		–	27	73	–	93	–	112		6.00	
t_{PLH}	propagation delay nA, nB to nY	–	47	175	–	220	–	260	ns	3.00	Fig.8
		–	23	52	–	65	–	78		4.75	
		–	18	46	–	58	–	70		6.00	
t_{THL}/t_{TLH}	output transition time	–	12	20	–	25	–	30	ns	3.00	Fig.8
		–	7	15	–	19	–	22		4.75	
		–	6	13	–	16	–	19		6.00	

TRANSFER CHARACTERISTIC WAVEFORMS

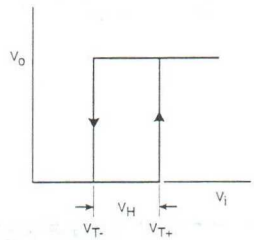


Fig.6 Transfer characteristic.

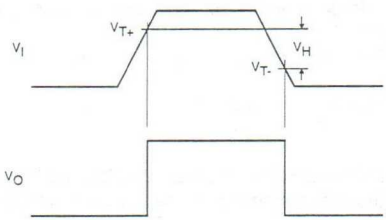


Fig.7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

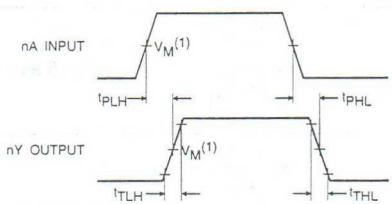


Fig.8 Waveforms showing the input (nA) to output (nY) propagation delay and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

9-BIT x 64-WORD FIFO REGISTER; 3-STATE

FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- Master-reset input to clear control functions
- 33 MHz (typ.) shift-in, shift-out rates with or without flags
- Very low power consumption
- Cascadable to 25 MHz (typ.)
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: standard
- I_{CC} category: LSI

GENERAL DESCRIPTION

The 74HC/HCT7030 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 33 MHz data-rate makes it ideal for high-speed applications. Even at high frequencies, the I_{CC} dynamic is very low (f_{max} = 18 MHz; V_{CC} = 5 V produces a dynamic I_{CC} of 80 mA). If the device is not continuously operating at f_{max}, then I_{CC} will decrease proportionally.

With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$) and an output enable input ($\overline{OE}$). Flags for data-in-ready (DIR) and data-out-ready (DOR) indicate the status of the device.

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $\overline{MR}$ to DIR and DOR $\overline{SO}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	21 36	26 40	ns ns
f_{max}	maximum clock frequency SI and $\overline{SO}$		33	29	MHz
C_I	input capacitance		3.5	3.5	pF
C_P	power dissipation capacitance per package	notes 1 and 2	660	660	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

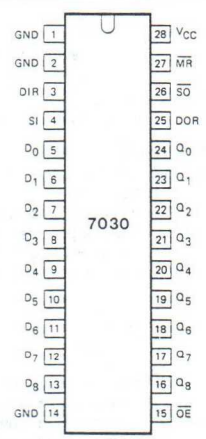


Fig. 1 Pin configuration.

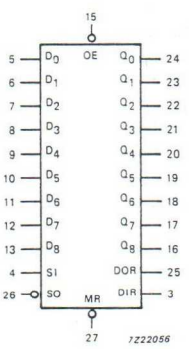


Fig. 2 Logic symbol.

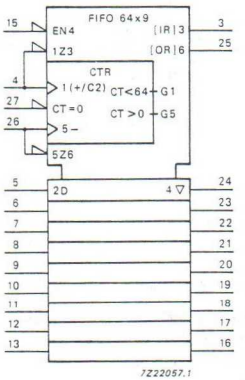


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 14	GND	ground (0 V)
3	DIR	data-in-ready output
4	SI	shift-in input (LOW-to-HIGH, edge-triggered)
5, 6, 7, 8, 9, 10, 11, 12, 13	D_0 to D_8	parallel data inputs
15	$\overline{OE}$	output enable input (active LOW)
24, 23, 22, 21, 20, 19, 18, 17, 16	Q_0 to Q_8	3-state parallel data outputs
25	DOR	data-out-ready output
26	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
27	$\overline{MR}$	asynchronous master-reset input (active LOW)
28	V_{CC}	positive supply voltage

Note to the pin description

Pin 14 must be connected to GND. Pins 1 and 2 can be left floating or connected to GND, however it is not allowed to let current flow in either direction between pins 1, 2 and 14.

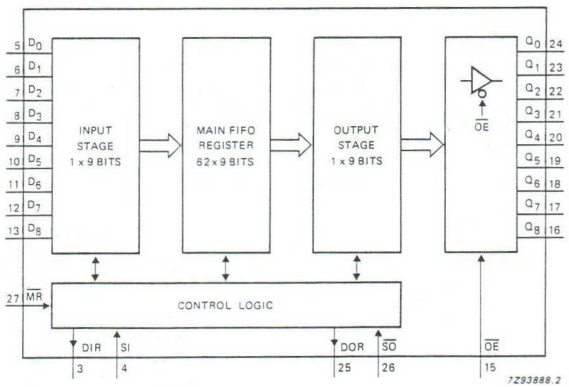


Fig. 4 Functional diagram.

APPLICATIONS

- High-speed disc or tape controller
- Video timebase correction
- A/D output buffers
- Voice synthesis
- Input/output formatter for digital filters and FFTs
- Bit-rate smoothing

GENERAL DESCRIPTION

INPUTS AND OUTPUTS

Data inputs (D_0 to D_8)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration, i.e. 8 x 64, 7 x 64, down to 1 x 64, by tying unused data input pins to V_{CC} or GND.

Data outputs (Q_0 to Q_8)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset ($\overline{MR}$)

When $\overline{MR}$ is LOW, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

DIR = HIGH indicates the input stage is empty and ready to accept valid data;

DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy);

DOR = HIGH assures valid data is present at the outputs Q_0 to Q_8 (does not indicate that new data is awaiting transfer into the output stage);

DOR = LOW indicates the output stage is busy or there is no valid data.

Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the rising edge of the $\overline{MR}$ signal.

Shift-out control ($\overline{SO}$)

A LOW-to-HIGH transition of $\overline{SO}$ causes the DOR flags to go LOW. A HIGH-to-LOW transition of $\overline{SO}$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

(continued on next page)

Output enable ($\overline{OE}$)

The outputs Q_0 to Q_8 are enabled when $\overline{OE}$ = LOW. When $\overline{OE}$ = HIGH the outputs are in the high impedance OFF-state.

FUNCTIONAL DESCRIPTION

Data input

Following power-up, the master-reset ($\overline{MR}$) input is pulsed LOW to clear the FIFO memory (see Fig. 8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D_0 to D_8 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until SI is set to LOW. With SI = LOW data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out ($\overline{SO}$) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI again goes LOW (see Fig. 7).

Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q_0 to Q_8). The initial master-reset at power-on ($\overline{MR}$ = LOW) sets DOR to LOW (see Fig. 8). After $\overline{MR}$ = HIGH, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the $\overline{SO}$ control input. With $\overline{SO}$ = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When $\overline{SO}$ is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW (see Fig. 9). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_8.

With the FIFO empty, the $\overline{SO}$ input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The $\overline{SO}$ control must be made LOW before additional data can be shifted out (see Fig. 10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).
- $\overline{SO}$ is held HIGH when the FIFO is full, some additional logic is required to produce a composite DOR pulse (see Figs 10 and 18).

Due to the part-to-part spread of the ripple through time, the flag signals of $FIFO_A$ and $FIFO_B$ will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig. 18.

The "7030" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words x 9-bits (see Fig. 19).

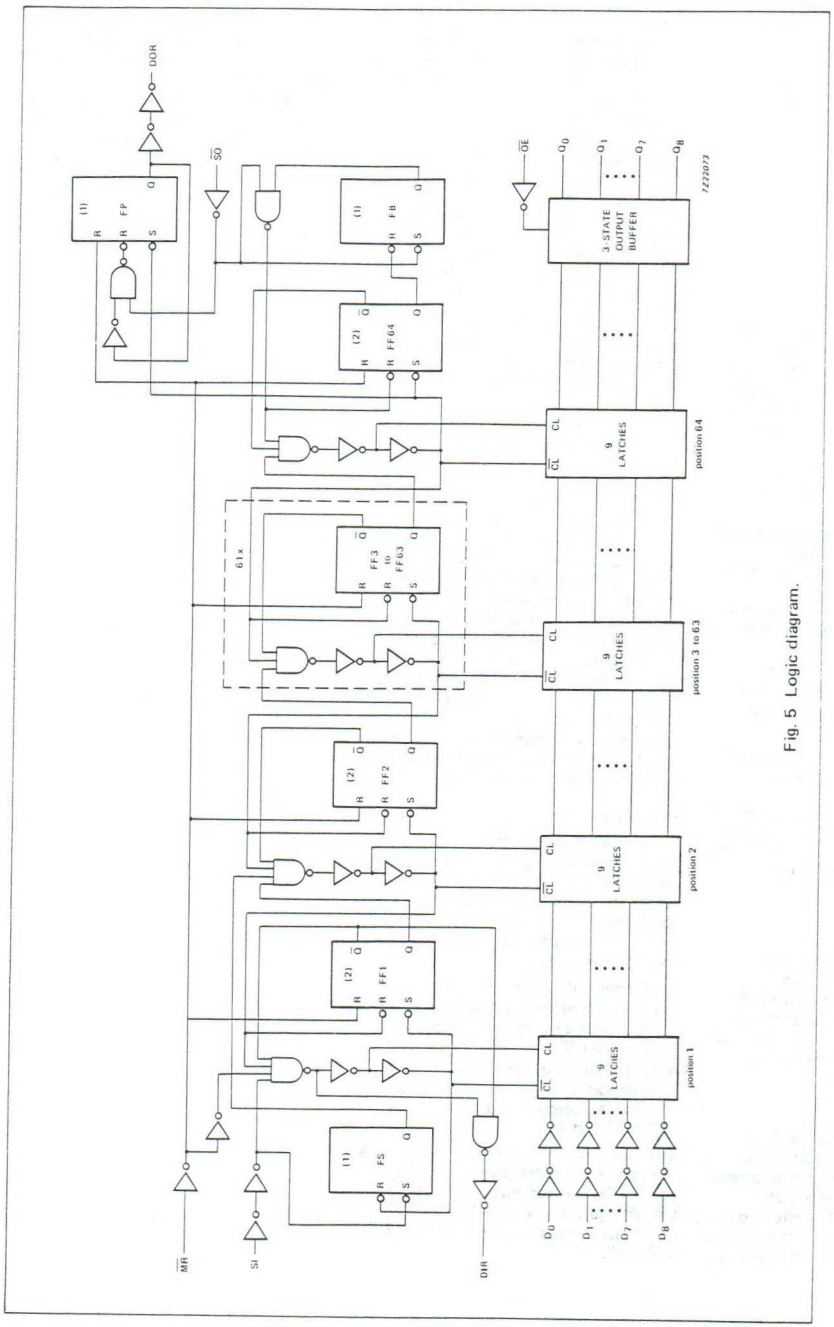


Fig. 5 Logic diagram.

Notes to Fig. 5 (see control flip-flops)

1. LOW on $\overline{S}$ input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on $\overline{R}$ input.
2. LOW on $\overline{R}$ input to FF1 to FF64 will set Q output to LOW independent of state on $\overline{S}$ input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: LSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay SI to DIR		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR		102 37 30	315 63 54		395 79 67		475 95 81	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n		11 4 3	35 7 6		45 9 8		55 11 9	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n		113 41 33	345 69 59		430 86 73		520 104 88	ns	2.0 4.5 6.0	Fig. 14
t_{PLH}	propagation delay/ripple through delay SI to DOR		2.5 0.9 0.7	8.0 1.6 1.3		10 2.0 1.6		12 2.4 1.9	μs	2.0 4.5 6.0	Fig. 10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		3.3 1.2 1.0	10.0 2.0 1.6		12 2.5 2.0		15 3.0 2.4	μs	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 16
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 16
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14
t_W	SI pulse width HIGH or LOW	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{SO}$ pulse width HIGH or LOW	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	DIR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig. 7
t_W	DOR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig. 10
t_W	$\overline{MR}$ pulse width LOW	70 14 12	22 8 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to SI	80 16 14	24 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 15
t_{su}	set-up time D_n to SI	−35 −7 −6	−36 −13 −10		−45 −9 −8		−55 −11 −9		ns	2.0 4.5 6.0	Fig. 13
t_h	hold time D_n to SI	135 27 23	44 16 13		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded		7.6 23 27		2.2 11 13		1.8 9.2 11		MHz	2.0 4.5 6.0	Figs 6 and 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: LSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1.00
SI	1.50
D_n	0.75
$\overline{MR}$	1.50
$\overline{SO}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR		30	51		53		63	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay SI to DIR		29	49		61		74	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR		39	67		84		101	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n		46	78		98		117	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n		7	12		15		18	ns	4.5	Fig. 10
t_{PLH}	propagation delay/ripple through delay SI to DOR		0.9	1.6		2.0		2.4	μs	4.5	Fig. 10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		1.2	2.0		2.5		3.0	μs	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n		20	35		44		53	ns	4.5	Fig. 16
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n		19	35		44		53	ns	4.5	Fig. 16
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 14
t_W	SI pulse width HIGH or LOW	12	6		15		18		ns	4.5	Fig. 6
t_W	$\overline{SO}$ pulse width HIGH or LOW	15	9		19		22		ns	4.5	Fig. 9
t_W	DIR pulse width HIGH	7	22	37	6	46	6	56	ns	4.5	Fig. 7
t_W	DOR pulse width HIGH	6	20	35	5	44	5	53	ns	4.5	Fig. 10
t_W	$\overline{MR}$ pulse width LOW	18	10		23		27		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to SI	18	10		23		27		ns	4.5	Fig. 15
t_{su}	set-up time D_n to SI	−5	−16		−4		−4		ns	4.5	Fig. 13
t_h	hold time D_n to SI	30	18		38		45		ns	4.5	Fig. 13

AC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	15	26		12		10		MHz	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	15	26		12		10		MHz	4.5	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	13	22		10		8.6		MHz	4.5	Figs 6 and 9

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

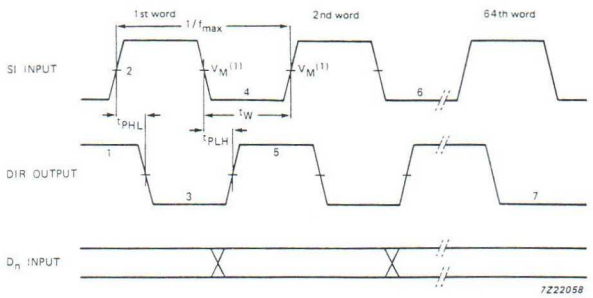


Fig. 6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig. 6

1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage "busy".
4. SI set LOW; data from first location "ripple through".
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd word through to 64th word into FIFO.
7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

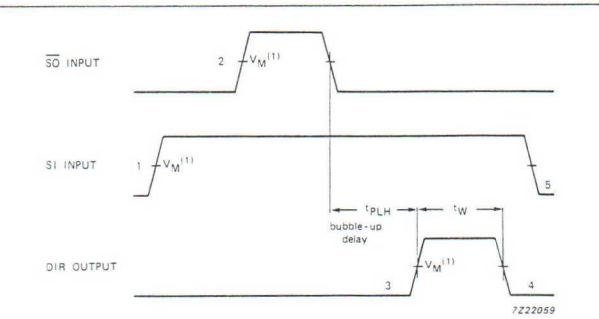


Fig. 7 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig. 7

1. FIFO is initially full, shift-in is held HIGH.
2. $\overline{SO}$ pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
4. DIR returns to LOW; FIFO is full again.
5. SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

AC WAVEFORMS

Master reset applied with FIFO full

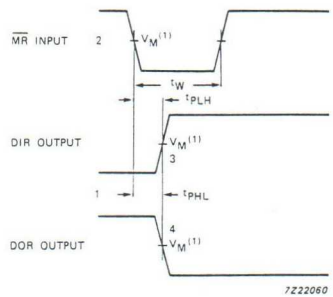


Fig. 8 Waveforms showing the $\overline{MR}$ input to DIR, DOR output propagation delays and the $\overline{MR}$ pulse width.

Notes to Fig. 8

1. DIR LOW, output ready HIGH; assume FIFO is full.
2. $\overline{MR}$ pulse LOW; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty

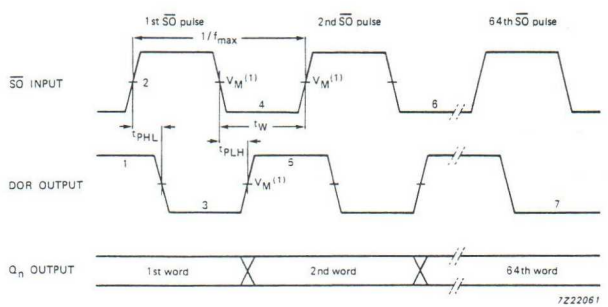


Fig. 9 Waveforms showing the $\overline{SO}$ input to DIR output propagation delay. The $\overline{SO}$ pulse width and $\overline{SO}$ maximum pulse frequency.

Notes to Fig. 9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2. $\overline{SO}$ set HIGH; results in DOR going LOW.
3. DOR drops LOW; output stage "busy".
4. $\overline{SO}$ is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
6. Repeat process to unload the 3rd through to the 64th word from FIFO.
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation

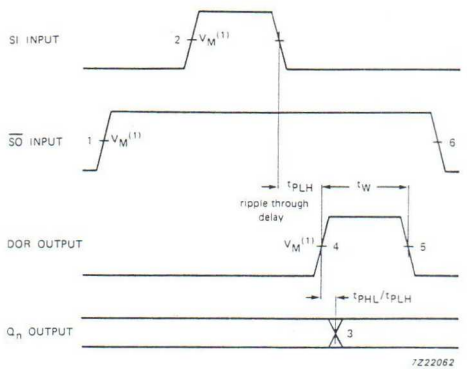


Fig. 10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig. 10

1. FIFO is initially empty, $\overline{SO}$ is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. DOR flag signals the arrival of valid data at the output stage.
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
5. DOR goes LOW; FIFO is empty again.
6. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode

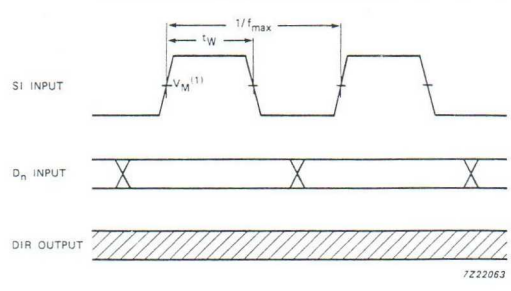


Fig. 11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig. 11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

AC WAVEFORMS

Shift-out operation; high-speed burst mode

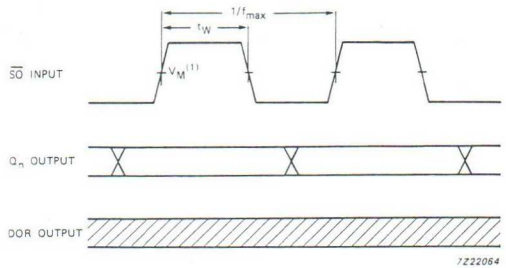


Fig. 12 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig. 12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a $\overline{SO}$ pulse can be applied without regard to the flag.

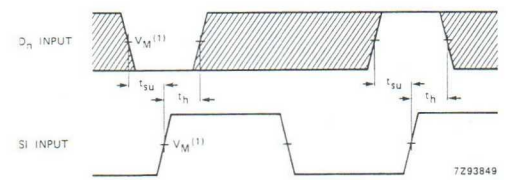


Fig. 13 Waveforms showing hold and set-up times for D_n input to SI input.

Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.

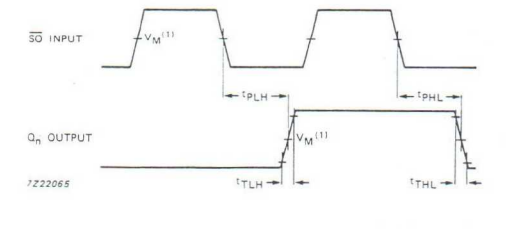


Fig. 14 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

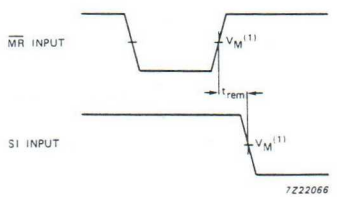


Fig. 15 Waveforms showing the $\overline{MR}$ input to SI input removal time.

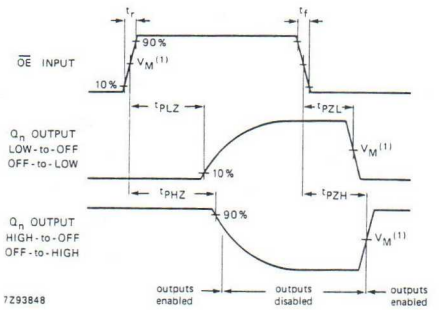


Fig. 16 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

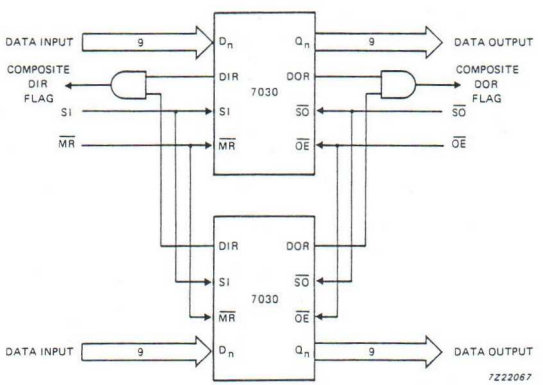


Fig. 17 Expanded FIFO for increased word length; 64 words x 18 bits.

Note to Fig. 17

The PC74HC/HCT7030 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

APPLICATION INFORMATION

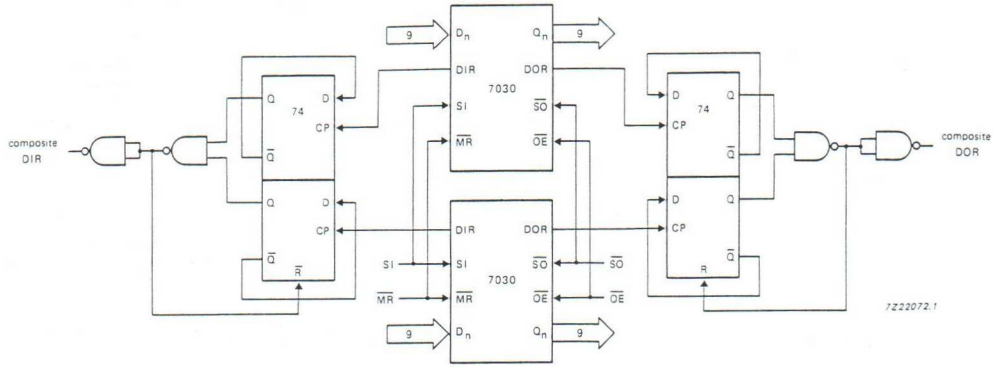


Fig. 18 Expanded FIFO for increased word length.

Note to Fig. 18

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

Expanded format

Fig. 19 shows two cascaded FIFOs providing a capacity of 128 words x 9 bits.
Fig. 20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are intially empty. After a rippled through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.
Fig. 21 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH.
Fig. 22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

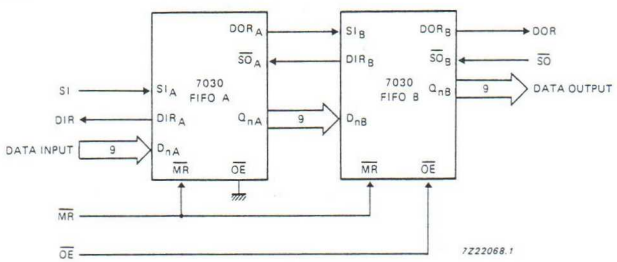


Fig. 19 Cascading for increased word capacity; 128 words x 9 bits.

Note to Fig. 19

The PC74HC/HCT7030 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 to 19 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Fig. 22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

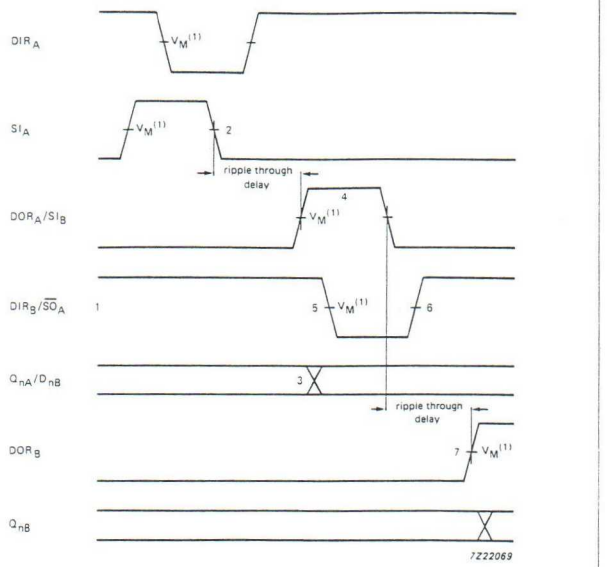


Fig. 20 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig. 20

1. FIFO$_A$ and FIFO$_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data.
2. Load one word into FIFO$_A$; SI pulse applied, results in DIR pulse.
3. Data out $_A$/data in $_B$ transition; valid data arrives at FIFO$_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO$_B$.
4. DOR$_A$ and SI$_B$ pulse HIGH; (ripple through delay after SI$_A$ LOW) data is unloaded from FIFO$_A$ as a result of the data output ready pulse, data is shifted into FIFO$_B$.
5. DIR$_B$ and $\overline{SO}_A$ go LOW; flag indicates input stage of FIFO$_B$ is busy, shift-out of FIFO$_A$ is complete.
6. DIR$_B$ and $\overline{SO}_A$ go HIGH automatically; the input stage of FIFO$_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data.
7. DOR$_B$ goes HIGH; (ripple through delay after SI$_B$ LOW) valid data is present one propagation delay later at the FIFO$_B$ output stage.

APPLICATION INFORMATION

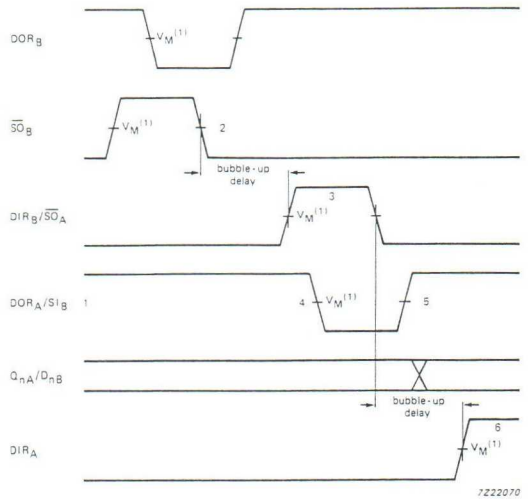


Fig. 21 FIFO to FIFO communication; output timing under full condition.

Note to Fig. 21

1. FIFO$_A$ and FIFO$_B$ initially full, SI$_B$ held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word from FIFO$_B$; $\overline{SO}$ pulse applied, results in DOR pulse.
3. DIR$_B$ and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into FIFO$_B$ as a result of the DIR pulse, data is shifted out of FIFO$_A$.
4. DOR$_A$ and SI$_B$ go LOW; flag indicates the output stage of FIFO$_A$ is busy, shift-in to FIFO$_B$ is complete.
5. DOR$_A$ and SI$_B$ go HIGH; flag indicates valid data is again available at FIFO$_A$ output stage, SI$_B$ is held HIGH, awaiting bubble-up of empty location.
6. DIR$_A$ goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of FIFO$_A$.

Note to application waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

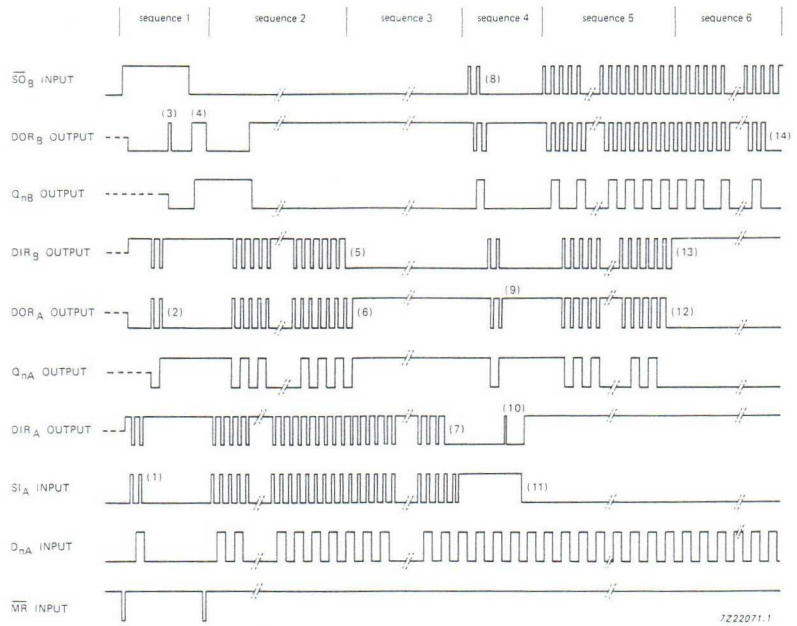


Fig. 22 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig. 19).

Note to Fig. 22

Sequence 1 (Both FIFOs empty, starting shift-in process):
After a $\overline{MR}$ pulse has been applied $FIFO_A$ and $FIFO_B$ are empty. The DOR flags of $FIFO_A$ and $FIFO_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of $FIFO_A$ and to the input stage of $FIFO_B$ (2). When data arrives at the output of $FIFO_B$, a DOR_B pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full):
After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full):
When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process):
SI_A is held HIGH and two $\overline{SO}_B$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty):
At the start of sequence 5 $FIFO_A$ contains 63 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of $\overline{SO}_B$ pulses are applied. After 63 $\overline{SO}_B$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty):
After the next $\overline{SO}_B$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty (13). After another 63 $\overline{SO}_B$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO}_B$ pulses have no effect. The last word remains available at the output Q_n.

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range:
  VCO section 3.0 to 6.0 V
  digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. Applies to the phase comparator section only (VCO disabled).
   For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). The value of the C_{LD} capacitor can be determined, using information supplied in Fig. 32

The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

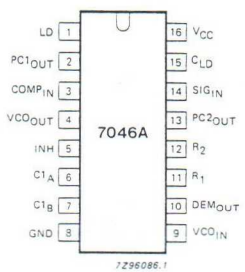


Fig. 1 Pin configuration.

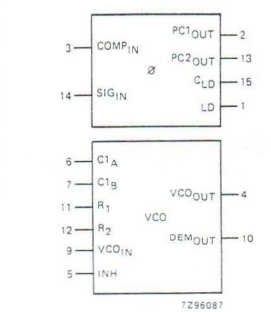


Fig. 2 Logic symbol.

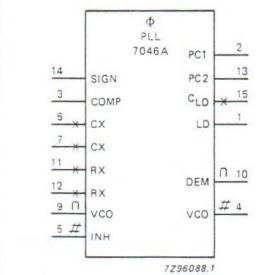


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	lock detector output (active HIGH)
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	C_{LD}	lock detector capacitor input
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

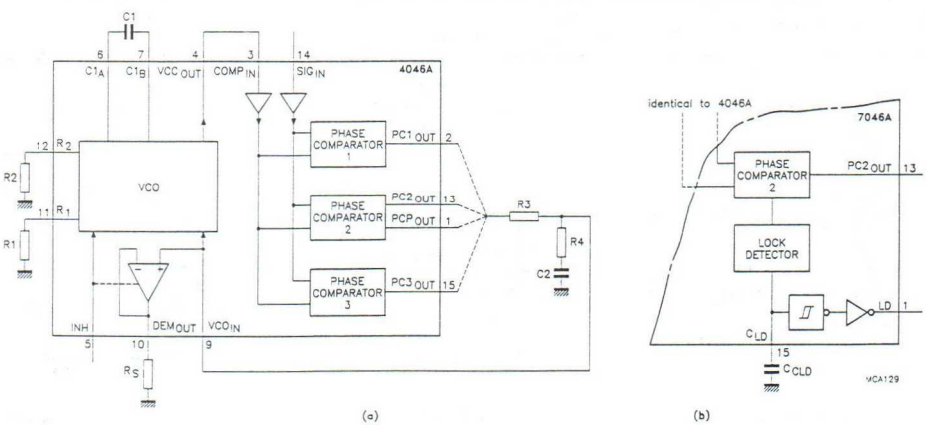


Fig. 4 Functional diagram.

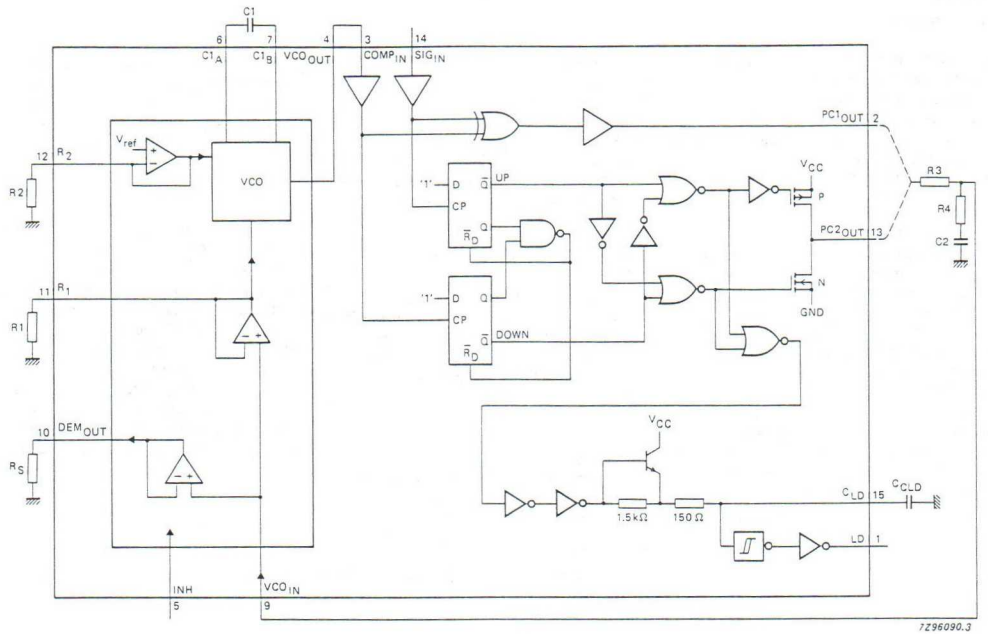


Fig. 5 Logic diagram.

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{\pi} \text{ (V/r)}.$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

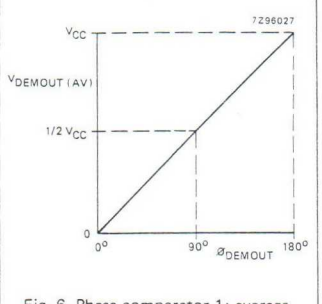


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

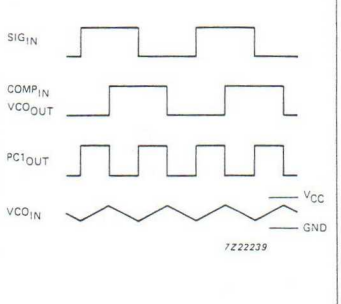


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

GENERAL DESCRIPTION

Phase comparators

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} \text{ (V/r)}.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference ($\phi DEMOUT$). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

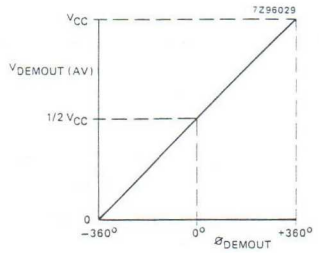


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC2OUT} =$

$\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi DEMOUT = (\phi_{SIGIN} - \phi_{COMPIN})$.

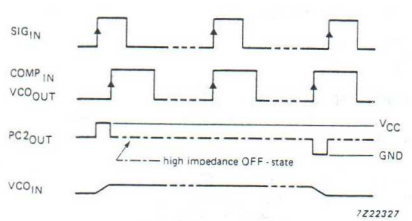


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	V_O = V_{CC} or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ	3.0 4.5 6.0	V_I at self-bias operating point; ΔV_I = 0.5 V; see Figs 10, 11 and 12	

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 4.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 18 and 19.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

DC CHARACTERISTICS FOR 74HC

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 13
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 14
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		74 27 22	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 15
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		96 35 28	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 15
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 16
f_o	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 17
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		250						kΩ	4.5	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 10, 11 and 12	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 18 and 19.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 13
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		21	40		50		60	ns	4.5	Fig. 14
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		27	56		70		84	ns	4.5	Fig. 15
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		35	65		81		98	ns	4.5	Fig. 15
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 14
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	OTHER
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 16b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 17
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

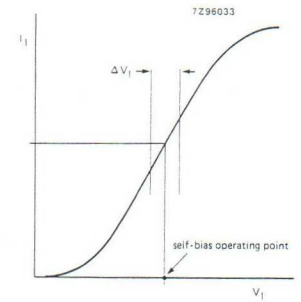


Fig. 10 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

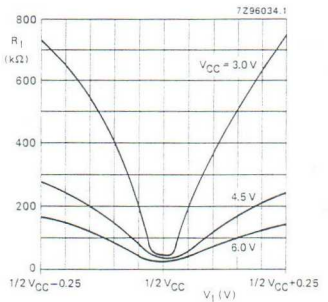


Fig. 11 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

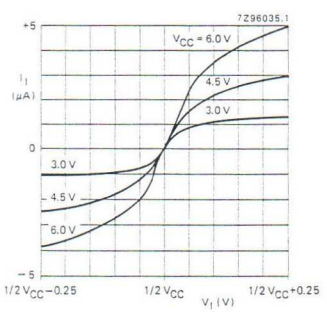
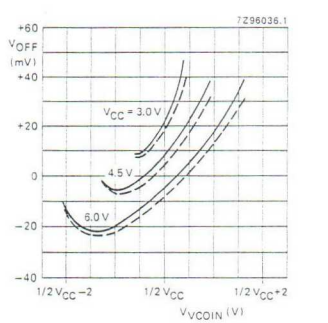


Fig. 12 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



— R_S = 50 kΩ
- - - R_S = 300 kΩ

Fig. 13 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

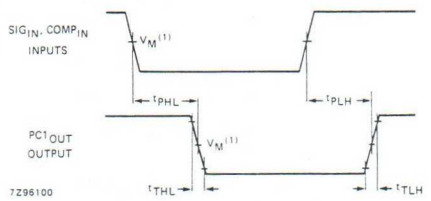


Fig. 14 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output ($PC1_{OUT}$) propagation delays and the output transition times.

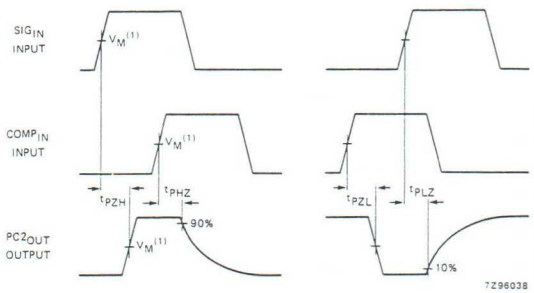


Fig. 15 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

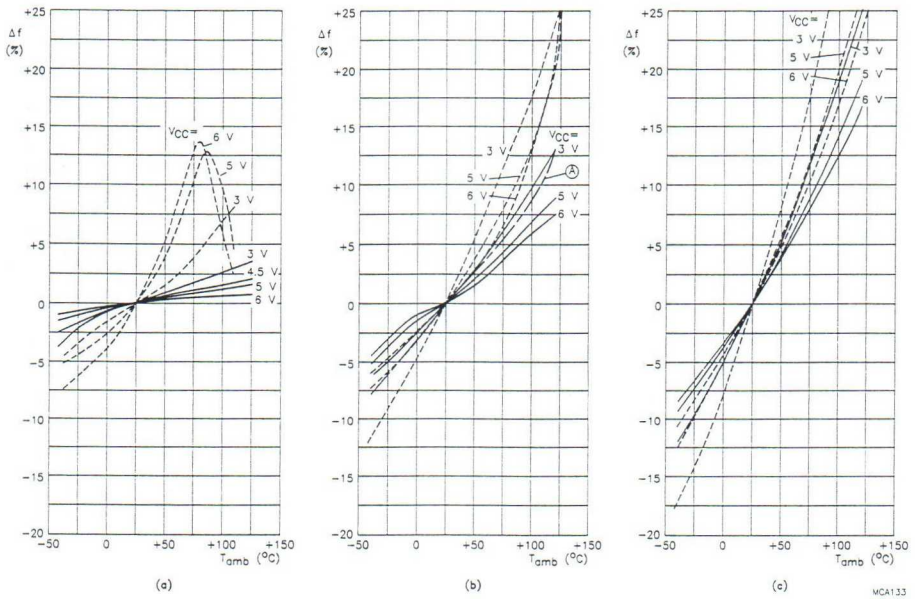
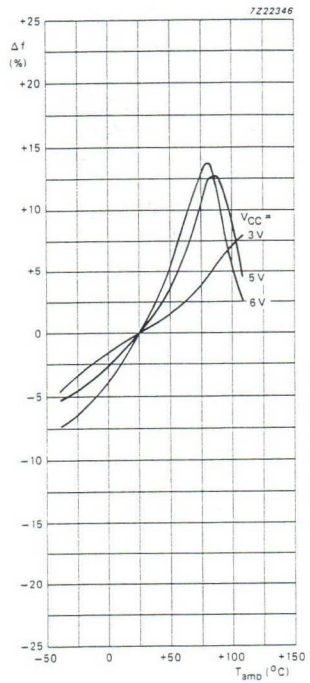
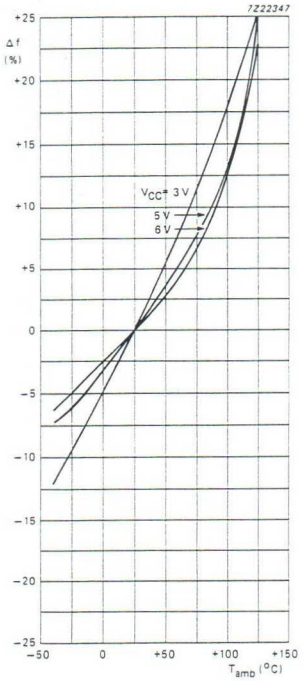


Fig.16 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
——— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO\ IN} = 0.5\ V_{CC}$.

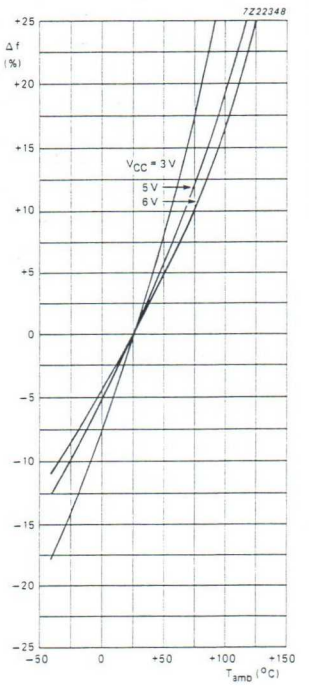
AC WAVEFORMS



(d) R2 = 3 kΩ
R1 = ∞



(e) R2 = 10 kΩ
R1 = ∞

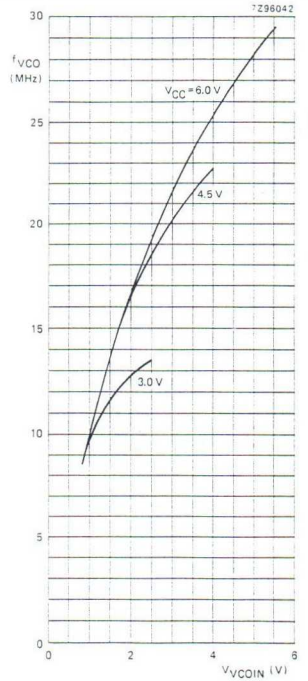


(f) R2 = 300 kΩ
R1 = ∞

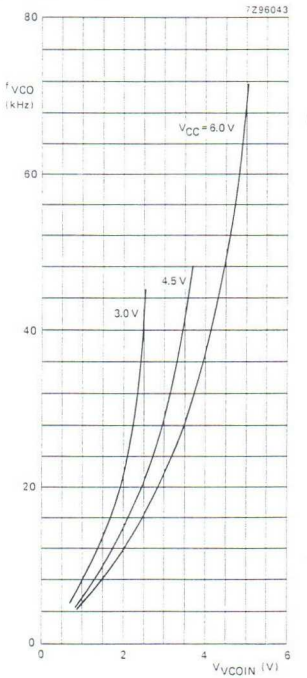
Fig. 16 Continued.

Note to Fig. 16

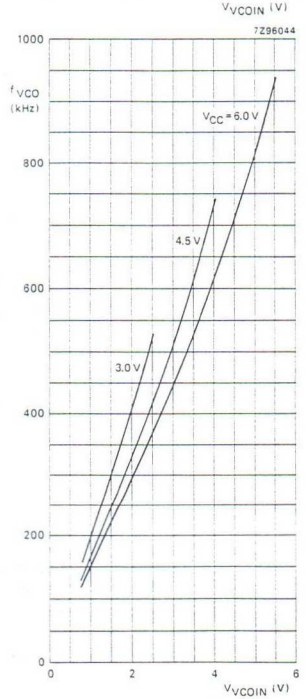
To obtain optimum temperature stability, C_1 must be as small as possible, but larger than 100 pF.



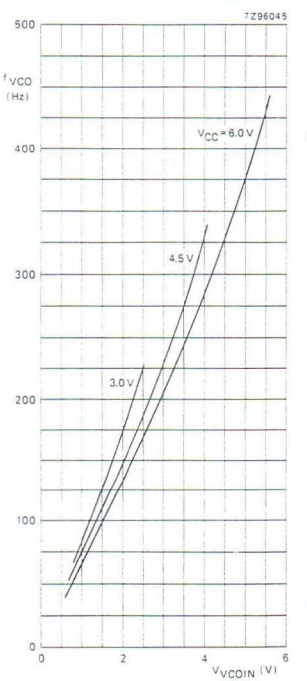
(a) R1 = 3 kΩ; C1 = 40 pF



(b) R1 = 3 kΩ; C1 = 100 nF



(c) R1 = 300 kΩ; C1 = 40 pF



(d) R1 = 300 kΩ; C1 = 100 nF

Fig. 17 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

AC WAVEFORMS

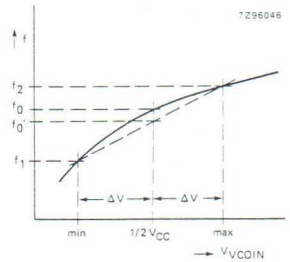


Fig. 18 Definition of VCO frequency linearity:
$\Delta V = 0.5$ V over the V_{CC} range:
for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2},$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

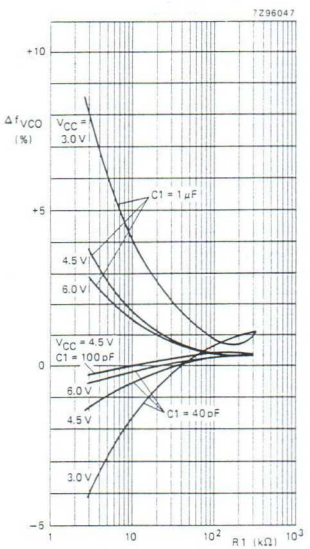
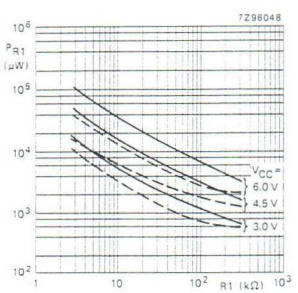
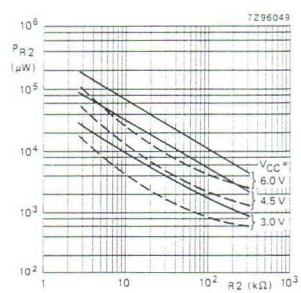


Fig. 19 Frequency linearity as a function of R1, C1 and V_{CC}: $R2 = \infty$ and $\Delta V = 0.5$ V.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 20 Power dissipation versus the value of R1: $C_L = 50$ pF; $R2 = \infty$; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 21 Power dissipation versus the value of R2: $C_L = 50$ pF; R1 = ∞; $V_{VCOIN} = GND = 0$ V; $T_{amb} = 25$ °C.

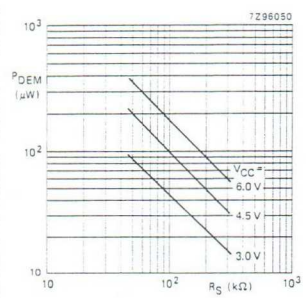


Fig. 22 Typical dc power dissipation of demodulator section as a function of R_S: $R1 = R2 = \infty$; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046 in a phase-lock-loop system.

References should be made to Figs 27, 28 and 29 as indicated in the table.

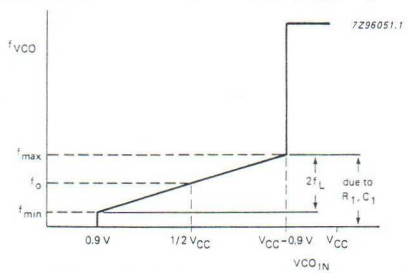
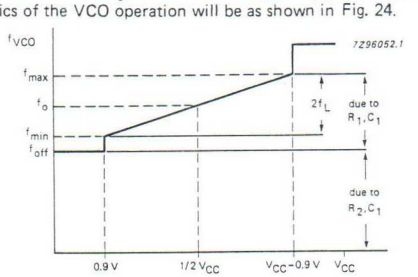
Values of the selected components should be within the following ranges:

R1 between 3 kΩ and 300 kΩ;

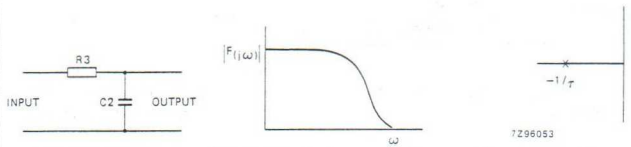
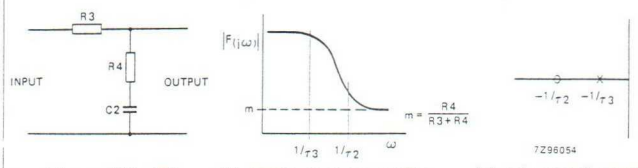
R2 between 3 kΩ and 300 kΩ;

R1 + R2 parallel value > 2.7 kΩ;

C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 23. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  Fig. 23 Frequency characteristic of VCO operating without offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig. 27.
	PC2	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 27, use Fig. 29 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 24.  Fig. 24 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig. 29. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig. 28. Calculate the value of R1 from the value of C1 and the product R1C1.

APPLICATION INFORMATION

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig. 6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = − 360° and V_{VCOIN} = min. (see Fig. 8).
PLL frequency capture range	PC1, PC2	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx 1/\pi\ (\sqrt{2\pi f_L/\tau})$ Fig. 25 Simple loop filter for PLL **without** offset; R3 ⩾ 500 Ω.  (a) τ_1 = R3 x C2; τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 (b) amplitude characteristic (c) pole-zero diagram Fig. 26 Simple loop filter for PLL **with** offset; R3 + R4 ⩾ 500 Ω.
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°

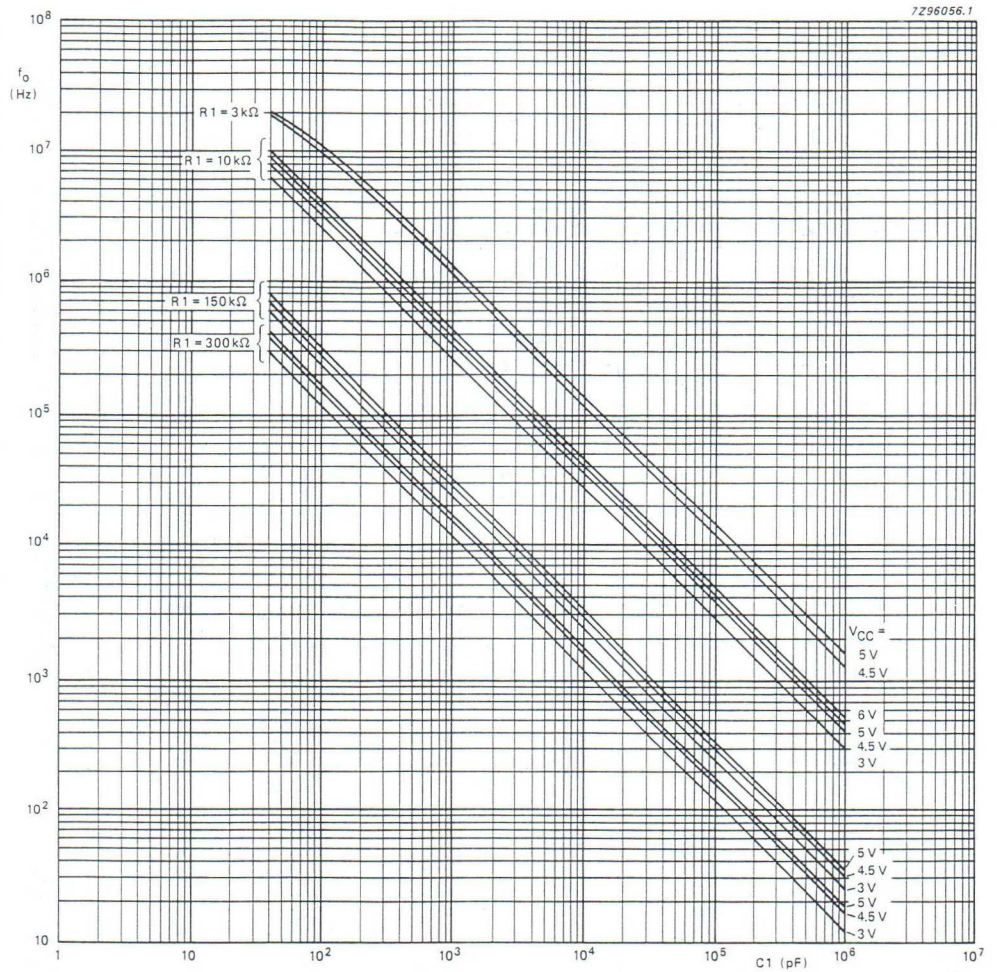


Fig. 27 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 27

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION

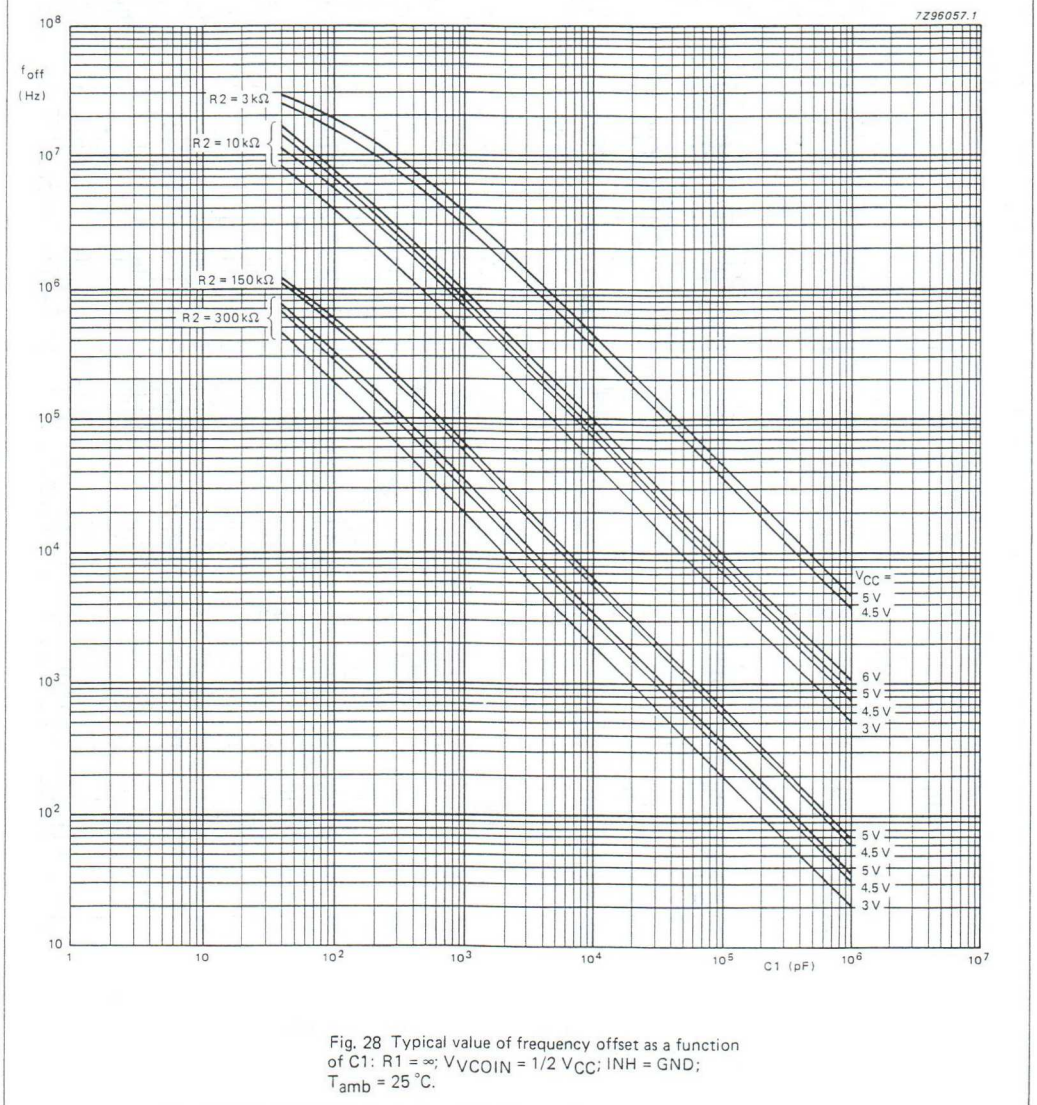


Fig. 28 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 28

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R2 can be easily calculated because, a constant R2C2 product will produce almost the same VCO output frequency.

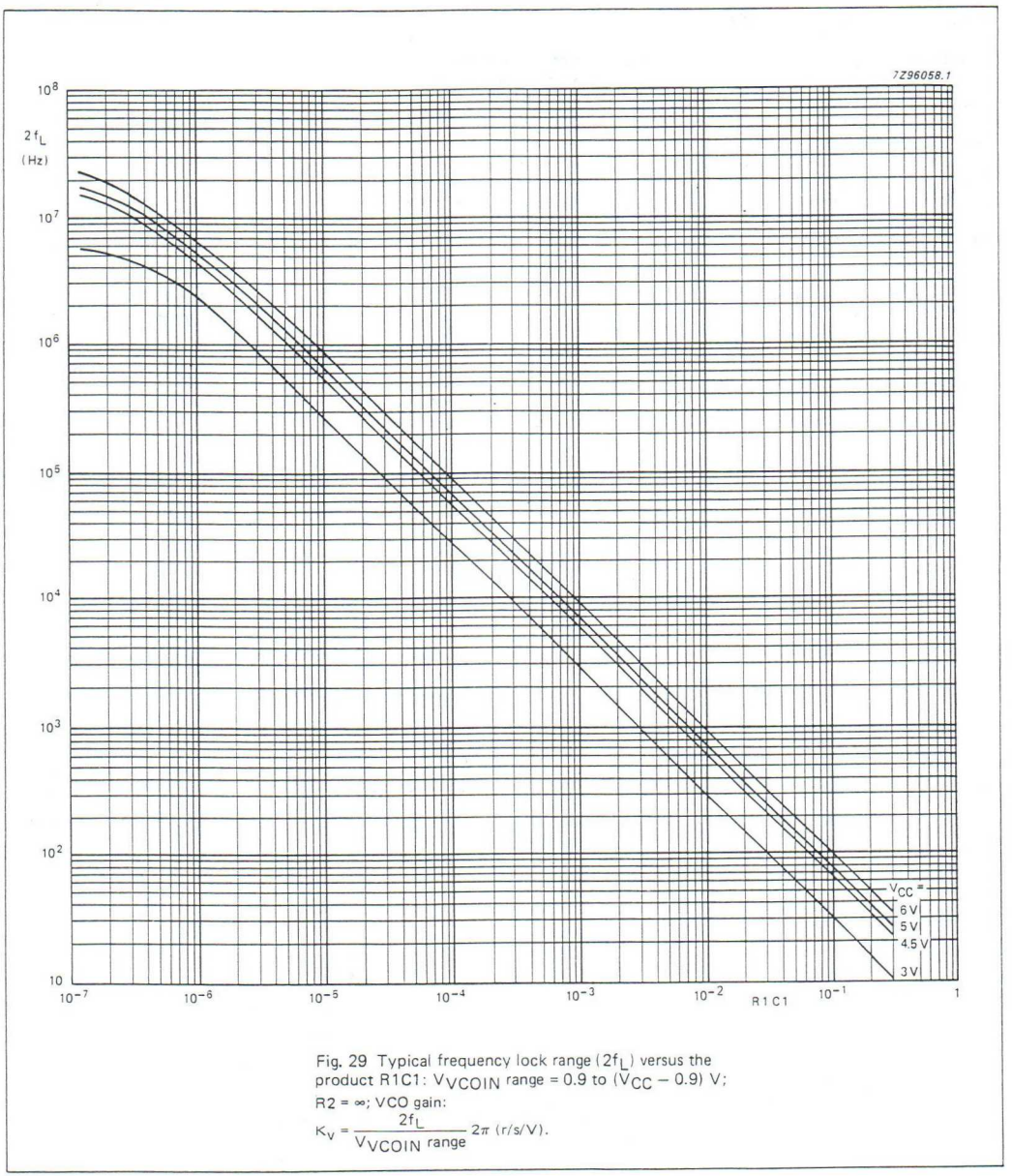


Fig. 29 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to (V_{CC} − 0.9) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN\ range}} 2\pi \text{ (r/s/V)}.$$

APPLICATION INFORMATION

Lock-detection circuit

The built-in lock-detection circuit will only work when used in conjunction with the phase comparator PC2. The lock-indication is derived from the phase error between SIG_{IN} and $COMP_{IN}$. The PC2 has a typical phase error of zero degrees over the entire VCO operating range. However, to remain in-lock the circuit requires some small adjustments. The variation is dependent on the loop parameters and back-lash time (typically 5 ns). Depending on the application, the phase error can be defined as the limit, a phase error of greater magnitude would be considered out-of-lock. An example of an in-lock detection circuit using the "7046A" is shown in Fig. 30.

If the PLL is in-lock, only very small pulses will come from the "up" or "down" connections of PC2. These pulses are filtered out by a RC network. A Schmitt trigger produces a steady state level, a HIGH level indicates an in-lock condition and a pulsed output indicates an out-of-lock condition as shown in Fig. 31.

Note to Fig. 30

(1) See Fig. 31 for input waveform.

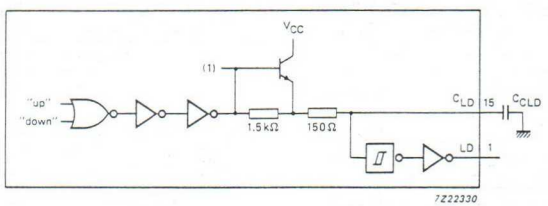


Fig. 30 An example of an in-lock detection circuit using the "7046A".

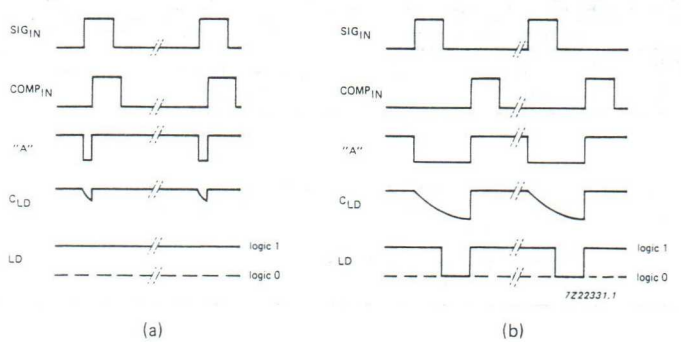


Fig. 31 Waveforms showing the lock detection process; (a) in-lock; (b) out-of-lock.

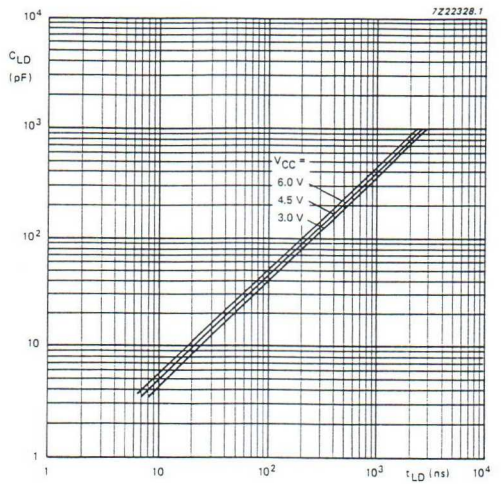


Fig. 32 C_{LD} capacitor value versus typical t_{LD}.

Where:

C_{LD} = capacitor connected to pin 15
(includes the parasitic input capacitance of the IC, approximately 3.5 pF).

t_{LD} = phase difference between SIG_{IN} and $COMP_{IN}$ (positive-going edges).

APPLICATION INFORMATION

The maximum permitted phase error must be defined, before t_{LD} can be defined using the following formula:

$$t_{LD} = \frac{\phi max}{360} \times \frac{1}{f_{IN}}.$$

Using this calculated value in Fig. 32, it is possible to define the value of C_{LD}, e.g. assuming the phase error is 36° and f_{IN} = 2 MHz:

$$t_{LD} = \frac{36°}{360} \times \frac{1}{2\ MHz} = 50\ ns,$$

and using Fig. 32, it can be seen that C_{LD} is 26 pF.

With the addition of one retriggerable monostable (e.g. "123", "423" or "4538") a steady state LOW and HIGH indication can be obtained, as shown in Fig. 33.

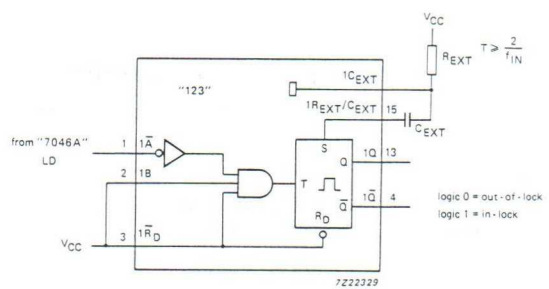


Fig. 33 Steady state signal for lock indication.

PLL design example

The frequency synthesizer, used in the design example shown in Fig. 34, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : < 20%

The open-loop gain is H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
K_o = K_v/s VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable).
The values can be determined using the information in the section "DESIGN CONSIDERATIONS".
With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/v$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:

1 + H (s) x G (s) = 0.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ξ is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{\tau_1 + \tau_2}.$$

The overshoot and settling time percentages are now used to determine ω_n. From Fig. 35 it can be seen that the damping ratio ζ = 0.8 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 4.5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n} = 790\ \Omega.$$

R3 is calculated using the damping ratio equation:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

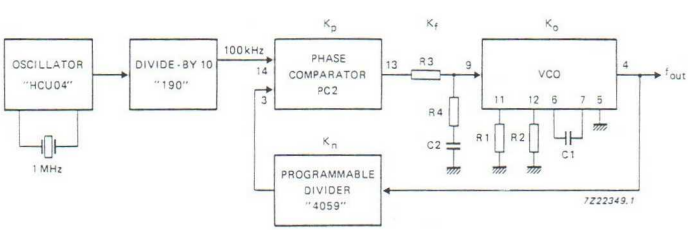


Fig. 34 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION

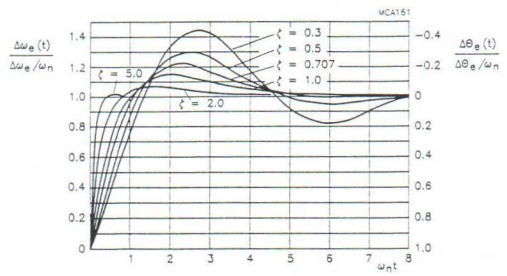


Fig. 35 Type 1, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

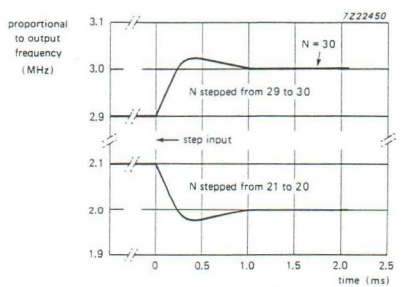


Fig. 36 Frequency compared to the time response.

16-BIT EVEN/ODD PARITY GENERATOR/CHECKER

FEATURES

- Word-length easily expanded by cascading
- Generates either even or odd parity for 16-data bits
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7080 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7080 are 16-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems.

The even and odd parity output is available for generating or checking even/odd parity up to 16-bits.

The even/odd parity output ($E/\overline{O}$) is HIGH when an even number of data inputs (I_0 to I_{15}) are HIGH and the cascade/even-odd-changing input ($\overline{X}$) is HIGH.

Expansion to larger word sizes is accomplished by connecting the even/odd parity output ($E/\overline{O}$) to the cascade/even-odd-changing input ($\overline{X}$) of the final stage.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to $E/\overline{O}$ $\overline{X}$ to $E/\overline{O}$	C_L = 15 pF V_{CC} = 5 V	29 12	32 15	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{X}$	cascade/even-odd-changing input
2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18	I_0 to I_{15}	data inputs
10	GND	ground (0 V)
19	$E/\overline{O}$	even/odd parity output
20	V_{CC}	positive supply voltage

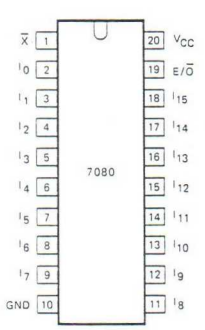


Fig. 1 Pin configuration.

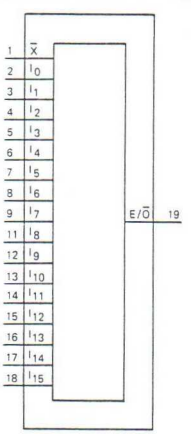


Fig. 2 Logic symbol.

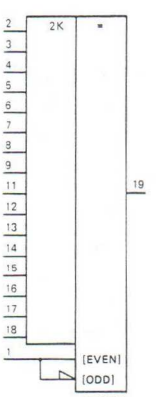


Fig. 3 IEC logic symbol.

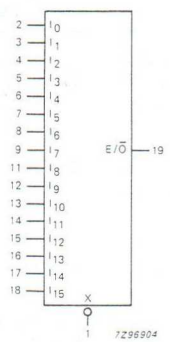


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
I_n	$\overline{X}$	E/$\overline{O}$
$\Sigma = E$	H	H
	L	L
$\Sigma \neq E$	H	L
	L	H

H = HIGH voltage level
L = LOW voltage level
E = even

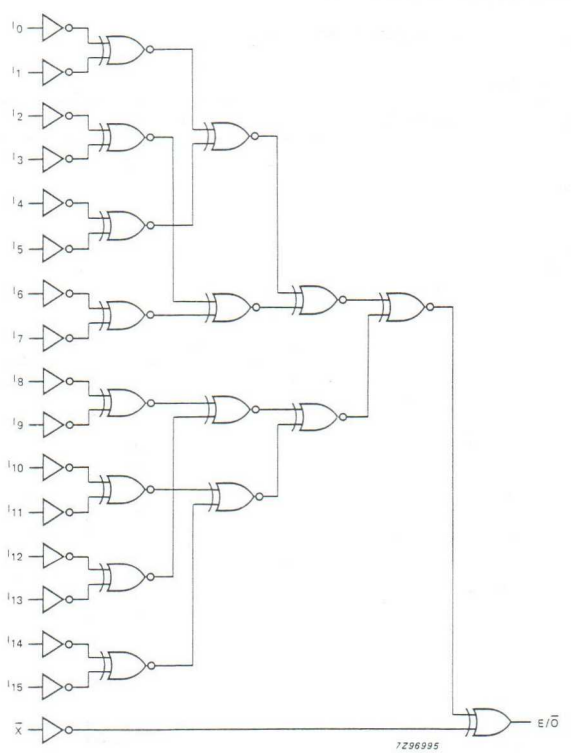


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to $E/\overline{O}$		91 33 26	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{X}$ to $E/\overline{O}$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	1.0
$\overline{X}$	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I_n to $E/\overline{O}$		37	63		79		95	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{X}$ to $E/\overline{O}$		18	32		40		48	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

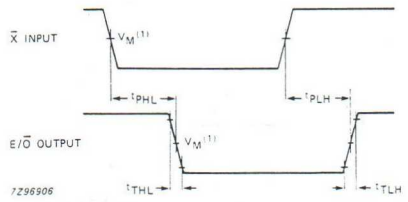


Fig. 6 Waveforms showing the cascade/even-odd-changing input ($\overline{X}$) to the even/odd parity output (E/$\overline{O}$) propagation delays and the output transition times.

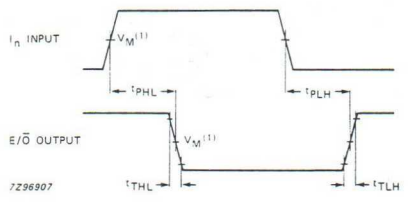


Fig. 7 Waveforms showing the data inputs (I_n) to the even/odd parity output (E/$\overline{O}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

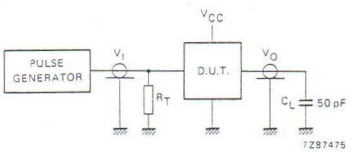


Fig. 8 Test circuit for measuring AC performance.

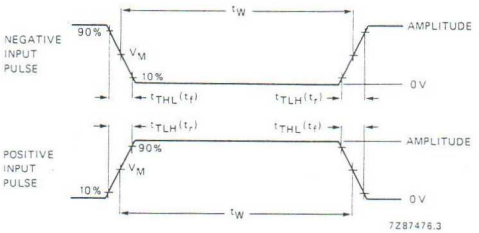


Fig. 9 Input pulse definitions.

Definitions for Figs 8 and 9:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132

FEATURES

- Precision inputs
- 2 operation modes: PAST and comparator
- In PAST mode: Inverting outputs in view of the precision oscillator application
- In comparator mode: Non-inverting outputs to simplify the design of an external hysteresis network
- 3-state outputs for bus oriented applications
- Output capability: Bus driver
- I_{CC} category: MSI

APPLICATIONS

- Precision oscillators
- Signal reconditioning
- Level conversion
- Process control (temperature, pressure, power e.g.)
- Accurate level detectors
- Time delays
- Overvoltage, overcurrent protection
- Bargraph display with LED's
- Battery charge control
- Analog to digital conversion

DESCRIPTION

The 74HC/HCT7132 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7132 contain 4 comparators with two common reference inputs V_{rH} and V_{rL} and four separate signal inputs V_{in0} to V_{in3}. The circuits can be applied in two modes:

1) The PAST (precision adjustable Schmitt-trigger) mode at which a voltage level equal to the wanted V_{T+} must be applied to the V_{rH} input and a voltage level equal to the wanted V_{T-} to the V_{rL} input.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
V_{rH}	High trip level	PAST mode; V_{CC} = 3 to 6 V	1.15 to V_{CC} − 1.2	V
	reference level	Comparator mode; V_{CC} = 3 to 6 V	0.6 to V_{CC}	V
V_{rL}	Low trip level	PAST mode; V_{CC} = 3 to 6 V	1.10 to V_{CC} − 1.25	V
δV_t	DC inaccuracy	V_{CC} = 3 to 6 V	±20	mV
C_{PD}	power dissipation capacitance per function	V_{CC} = 5 V PAST mode Comparator mode	 100 30	 pF pF
P_d	Total DC power dissipation	Comparator mode; V_{CC} = 4.5 V; $V_{rL} = V_{INn}$ = 0 V; V_{rH} = 2.25 V	8	mW
t_{rmin}/t_{fmin}	Minimum rise and fall time for optimum operation	PAST mode; V_{CC} = 4.5 V; V_{rH} = 3 V; V_{rL} = 1.5 V	180	ns
t_{PHL}/t_{PLH}	propagation delay V_{inn} to Q	PAST mode; V_{CC} = 4.5 V	40/60	ns

Notes to the quick reference data:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + C_L \times V_{CC}^2 \times f_o$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7132P	14	DIL	plastic	SOT27
74HC/HCT7132T	14	SO	plastic	SOT108

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132

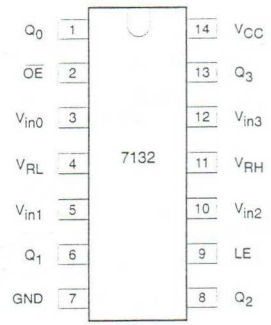


Fig.1 Pin configuration.

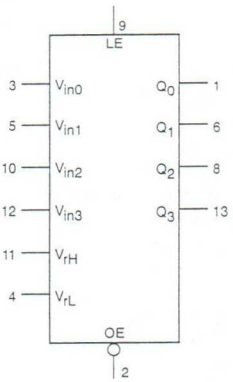


Fig.2 Logic symbol.

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 6, 8, 13	Q_0 to Q_3	3-state latch outputs
2	$\overline{OE}$	3-state output enable input (active LOW)
3, 5, 10, 12	V_{in0} to V_{in3}	signal inputs
4	V_{rL}	low reference voltage input
7	GND	ground (0 V)
9	LE	latch enable input (active HIGH)
11	V_{rH}	high reference voltage input
14	V_{CC}	positive supply voltage

FUNCTION TABLE for PAST mode (table 1)

V_{inn} (rising edge)	LE	$\overline{OE}$	Q_n
$V_{inn} < V_{LL}$	L	L	H
$V_{LL} < V_{inn} < V_{rH}$	L	L	H
$V_{HH} > V_{inn} > V_{rH}$	L	L	L
$V_{inn} > V_{HH}$	L	L	L
V_{inn} (falling edge)	**LE**	**$\overline{OE}$**	**Q_n**
$V_{HH} > V_{inn} > V_{rL}$	L	L	L
$V_{LL} < V_{inn} < V_{rL}$	L	L	H
$V_{inn} < V_{LL}$	L	L	H
$V_{inn} = X$	H	L	Q_{t-1}
$V_{inn} = X$	X	H	Z

2) The comparator mode at which the V_{rL} input must be connected to GND and the V_{rH} input is the active reference level input. In this mode a few resistors must be added to achieve a small hysteresis in order to avoid oscillations. The operation in both modes will be further explained by means of the logic diagram of fig.5.

DETAILED DESCRIPTION

The mode selector.

See fig.5 for logic diagram. The circuit can be applied in two modes that are selected by the mode selector on bases of the level on the V_{rL} input. When the level on this input is in the operating area of the PAST mode (V_{rL} > 1 V) the true output of the mode detector is "0" which means that the PAST mode is selected. When the V_{rL} input is at GND level the true output of the mode detector is "1" by which the comparator mode is selected. This mode needs only one reference input being the V_{rH} input.

The Power-on Detector

The power-on detector selects a window typically between V_{INn} = 1 V

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
Q_{t-1} = initial state

and $V_{INn} = V_{CC} - 1$ V in which in case of the PAST mode the power of the analog part (comparator)is switched on. When operating in the comparator mode the power is always switched on by means of an OR gate.

The digital detector

The digital detector is a Flip-Flop which output is set to LOW when

Quad precision adjustable Schmitt-trigger/comparator with output latches; 3-state

74HC/HCT7132

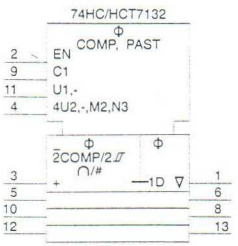


Fig.3 IEC Logic symbol.

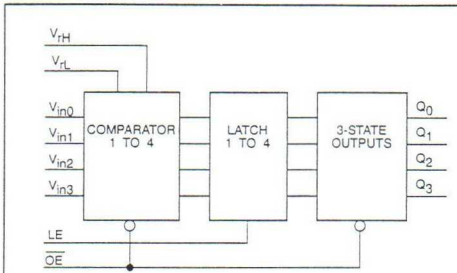


Fig.4 Functional diagram.

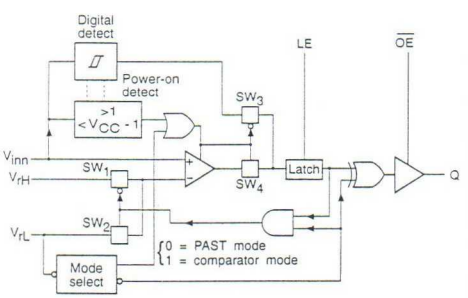


Fig.5 Logic diagram.

V_{INn} < 1 V and to HIGH when V_{INn} > V_{CC} – 1 V. This detector controls the output stage in the cases that the power of the comparator is switched off. This is performed by means of the switches SW_3 and SW_4.

The latch

The output information can be stored in a latch on activating the LE input. In the PAST mode this latch is also used to control the reference input of the comparator which is either connected to the V_{rH} input via SW, or to the V_{rL} input via SW_2. In case of the comparator mode the reference input is always connected to the V_{rH} input. This is done by means of an AND gate.

The exclusive OR gate

By means of this function the output stage is switched between inverting and non-inverting. In the PAST mode the inverting output of the mode selector is "1" so the exclusive OR is inverting. In the comparator mode this output is "0" so the exclusive OR is non-inverting.

The operation in the PAST mode

The operation in the PAST mode will be further outlined with the aid of Fig.5 and 9. and table 1. When the level of V_{INn} is 0 V the power of the comparator is switched OFF and the output circuit is controlled by the digital detector which output is LOW in that situation. So the output of the transparent latch is LOW. As the output stage is inverting now Q_n is HIGH. In this condition the reference input of the comparator is connected to the $+V_{rH}$ input. When starting from 0 V the level at V_{inn} is increased, at about the V_{LL} level (≈1 V) the DC power of the comparator is switched ON. The control of the output circuit is switched over from the digital detector output to the comparator output, when after a delay the voltage at this node is stabilised. During this operation the output level of the latch output remains LOW and the level of Q_n HIGH. When the level at V_{inn} reaches the V_{rH} level the output level of the comparator turns to HIGH and so the output level of the transparent latch. The level at Q_n turns to LOW. In this instant the reference input of the comparator is switched over from V_{rH} to V_{rL} leaving the output voltage at Q_n constant. When the level at V_{inn} reaches the V_{HH} level (≈V_{CC} – 1 V) the DC power of the comparator is switched OFF. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is HIGH in this situation. During this action the level at Q_n remains LOW. When the level at the V_{inn} input is decreased starting at V_{CC} level, at the V_{HH} level (≈V_{CC} – 1 V) the power of the comparator will be switched on again. The control of the output circuit

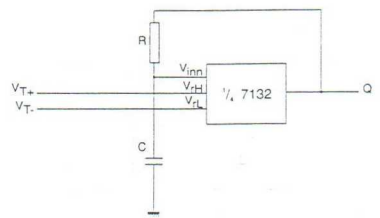


Fig.6 $^1/_4$ 7132 Precision oscillator application.

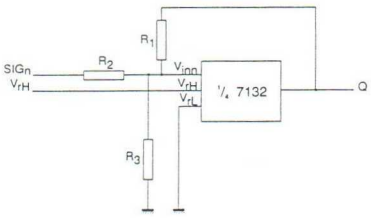


Fig.7 $^1/_4$ 7132 Comparator application.

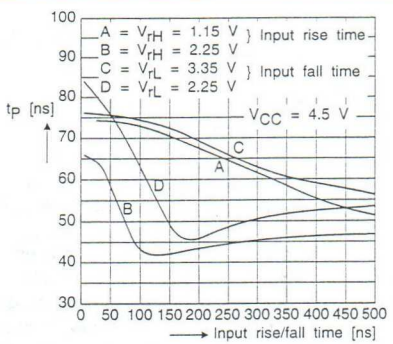


Fig.8 Waveforms applied during measurements see fig.13.

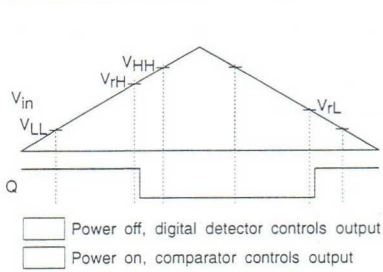


Fig.9 Input voltage switching levels.

is switched over from the digital detector output to the comparator output when after a delay the voltage at this node is stabilised. As the comparator output level is HIGH in this situation the output level of the latch remains HIGH and the Q_n output LOW. When the level at V_{inn} reaches the V_{rL} level the output level of the comparator turns to LOW and so the output level of the transparent latch. The level at Q_n turns to HIGH. In this instant the reference input of the comparator is switched over from V_{rL} to V_{rH} leaving the output voltage at Q_n constant. When the level at V_{inn} reaches about 1 V the DC power of the comparator is switched OFF again. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is LOW in this situation. During this action the level at Q_n remains HIGH. The function of the circuit is a Schmitt-Trigger of which the V_{T+} and V_{T-} levels can be set at the V_{rH} and V_{rL} inputs. These levels can be varied from ≈1 V up to ≈V_{CC} – 1 V. so the maximum obtainable hysteresis is ≈V_{CC} – 2 V. The on-and off switching of the power and the stabilisation of the comparator needs time, therefore the minimum applicable rise- and fall time of the input signal are limited when the maximum accuracy is required. When during the rise time of the input signal the input level has past the V_{LL} level, the power starts to switch on. Only when the comparator is stable at the moment that the input signal passes the V_{rH} level the comparator has its true delay and its optimal accuracy. When the V_{rH} level is passed before the comparator is stable an extra delay occurs due to the switching of the power and the accuracy of the comparator is less. At the positive going edge, this extra delay depends on the difference between V_{LL} and V_{rH} and the rise time of the signal. This is shown in Fig.8, where by means of curves A and B t_{PHL} is plotted at V_{rH} is 1.15 V and 2.25 V respectively and V_{CC} = 4.5 V. As with curve a V_{rH} is very close to V_{LL} the part of the input edge that is available for switching the power on is very small. This causes that only at a rise time > 500 ns/V the delay will be equal to the true delay of the comparator. At V_{rH} = 2.25 V this situation is reached already at a rise time of 120 ns/V. At a very short rise time, the major part of the propagation delay is due to the switching

(Continued)

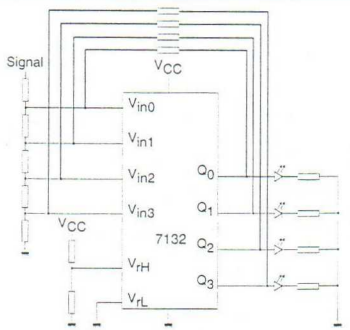


Fig. 10 Possible circuit for a bargraph.

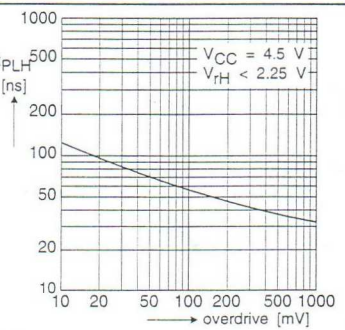


Fig.11 Curve showing the t_{PLH}/t_{PHL} as a function of the overdrive for the comparator application. Waveforms applied during measurements see fig.13.

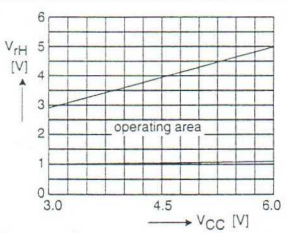


Fig.12 Operating area for V_{rH} in comparator mode.

time of the power. At the negative going edge, the power is switched on when the level V_{HH} is passed so the extra delay depends on the difference between V_{HH} and V_{rL} and the fall time of the signal. This situation is referred to with curves C and D where t_{PLH} is drawn against the fall time of the input signal. With curve C V_{rL} is 3.25 V which is on the edge of the operating region. Curve D corresponds with a V_{rL} value of 2.25 V. For linear input edges the recommended minimum rise time at V_{CC} = 4.5 V or 6 V is 100 ns/V and at V_{CC} = 3 V, 300 ns/V. For non-linear input signals, during the rising edge there must be a delay between the time at which the V_{LL} level is passed and the time at which the V_{rH} level is passed. This delay will be dependent on the V_{CC} level and the amplitude of the overdrive of V_{LL}. There is no limitation on the signal slope during the passing of the levels. For the same reasons, during the falling edge there must be a delay between the time at which the V_{HH} level is passed and the time at which the V_{rL} level is passed.

A possible application of the circuit is as precision oscillator see Fig.6. The operating frequency is:

$$f = \frac{1}{t_{RC} + 2 \times (t_{PLH} + t_{PHL})} \text{ where } t_{RC} = 2 \times \ln\left(\frac{V_{CC} - V_{rL}}{V_{CC} - V_{rH}}\right) \times RC$$

The operation in the comparator mode

The IC can be applied as a comparator by connecting the V_{rL} input to GND and adjusting the level at V_{rH} to the wanted detection level see Fig.7. In this mode the DC power of the comparator is always on and the output stage is set to non-inverting. The function table for this operation mode is given in table 2.

FUNCTION TABLE for Comparator mode (table 2)

INPUT	LE	$\overline{OE}$	Q_n
$V_{inn} < V_{ref}$	L	L	L
$V_{inn} > V_{ref}$	L	L	H
V_{inn} = X	H	L	Q_{n-1}
V_{inn} = X	X	H	Z

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care

The fact that the power is always on offers the feature of a more extended operation region of the V_{rH} input voltage which is at a V_{CC} of 4.5 V from 1.1 V up to 4.2 V see also Fig.12. A hysteresis of about 50 mV is required to overcome oscillations. This has to be performed by means of a few external resistors. The DC power in this operation mode at V_{CC} = 4.5 V is typical 2 mW per function. A curve showing t_{PD} as a function of the overdrive is given in Fig.11. A possible diagram for a bargraph display is shown in Fig.10.

DC CHARACTERISTICS FOR 74HC

Output capability: Bus driver
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{CC}	DC supply voltage	3.0	–	6.0	3.0	6.0	3.0	6.0	V			
V_{err}	Error on trip level	–	±20	–	–	–	–	–	mV	3.0 to 6.0		over V_{ref} range
V_{LL}	V_{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V	3.0 to 6.0		Fig.9
V_{HH}	V_{IN} at which power for comparator is switched OFF	V_{CC} - 1.1	V_{CC} - 0.9	V_{CC} - 0.5	V_{CC} - 1.1	V_{CC} - 0.5	V_{CC} - 1.1	V_{CC} - 0.5	V	3.0 to 6.0		Fig.9
I_{CC}	active supply current. Comparator mode	–	2.0	3.4	–	–	–	–	mA	4.5		V_{rH} = 2.25 V V_{rL} = 0 V
I_{CC}	supply current. PAST mode	–	30	50	–	–	–	–	µA	4.5		V_{rH} = 3 V V_{rL} = 1.5 V
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	µA	6.0		$V_{rH} = V_{rL} = V_{CC}$ V_{IN} = 0 V

PAST mode

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{rH}	HIGH reference level, (V_{T+})	1.15	–	V_{CC} – 1.2	1.15	V_{CC} - 1.2	1.15	V_{CC} - 1.2	V	3.0 to 6.0		
V_{rL}	LOW reference level, (V_{T-})	1.1	–	V_{CC} – 1.25	1.1	V_{CC} – 1.25	1.1	V_{CC} – 1.25	V	3.0 to 6.0		
V_{Hmin}	Minimum hysteresis voltage, ($V_{rH} - V_{rL}$)	–	50	–	–	–	–	–	mV	3.0 to 6.0		

COMPARATOR mode

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{rHmin}	minimum reference level	–	0.6	–	–	–	–	–	V	4.5		over V_{ref} range
V_{rHmax}	maximum reference level	–	V_{CC}	–	–	–	–	–	V	4.5		over V_{ref} range

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_{rH}	V_{rL}	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.					
t_{PHL}	propagation delay V_{inn} to Q_n; PAST mode	–	80	–	–	–	–	–	ns	3.0	1.67	1.50	t_r = 300 ns/V
		–	50	–	–	–	–	–		4.5	3.00	1.50	t_r = 100 ns/V
		–	40	–	–	–	–	–		6.0	4.00	2.00	t_r = 100 ns/V Fig.13
t_{PLH}	propagation delay V_{inn} to Q_n; PAST mode	–	80	–	–	–	–	–	ns	3.0	1.67	1.50	t_r = 300 ns/V
		–	50	–	–	–	–	–		4.5	3.00	1.50	t_r = 100 ns/V
		–	40	–	–	–	–	–		6.0	4.00	2.00	t_r = 100 ns/V Fig.13
t_{PHL}	propagation delay V_{inn} to Q_n; Comparator mode	–	100	–	–	–	–	–	ns	3.0	$V_{CC}/2$	0.00	Fig.14, overdrive: 100 mV
		–	60	–	–	–	–	–		4.5			
		–	50	–	–	–	–	–		6.0			
t_{PLH}	propagation delay V_{inn} to Q_n; Comparator mode	–	80	–	–	–	–	–	ns	3.0	$V_{CC}/2$	0.00	Fig.14, overdrive: 100 mV
		–	50	–	–	–	–	–		4.5			
		–	40	–	–	–	–	–		6.0			
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	–	35	–	–	–	–	–	ns	3.0			Fig.15
		–	23	–	–	–	–	–		4.5			
		–	18	–	–	–	–	–		6.0			
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	22	–	–	–	–	–	ns	3.0			Fig.17
		–	15	–	–	–	–	–		4.5			
		–	13	–	–	–	–	–		6.0			
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	22	–	–	–	–	–	ns	3.0			Fig.17
		–	17	–	–	–	–	–		4.5			
		–	14	–	–	–	–	–		6.0			
t_{THL}/t_{TLH}	output transition time	–	25	–	–	–	–	–	ns	3.0			Fig.13
		–	10	–	–	–	–	–		4.5			
		–	9	–	–	–	–	–		6.0			
t_W	LE pulse width LOW	–	12	–	–	–	–	–	ns	3.0			Fig.15
		–	6	–	–	–	–	–		4.5			
		–	5	–	–	–	–	–		6.0			
t_{su}	set-up time V_{inn} to LE	–	30	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns
t_h	hold time V_{inn} to LE	–	−30	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns
										6.0			

DC CHARACTERISTICS FOR 74HCT

Output capability: Bus driver
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{CC}	DC supply voltage	4.5	–	5.5	4.5	5.5	4.5	5.5	V			
V_{arr}	Error on trip level	–	±20	–	–	–	–	–	mV	4.5 to 5.5		over V_{ref} range
V_{LL}	V_{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V	4.5		Fig.9
V_{HH}	V_{IN} at which power for comparator is switched OFF	3.4	3.6	4.0	3.4	4.0	3.4	4.0	V	4.5		Fig.9
I_{CC}	active supply current. Comparator mode	–	2.0	3.4	–	–	–	–	mA	4.5		V_{rH} = 2.25 V V_{rL} = 0 V
I_{CC}	supply current. PAST mode	–	30	50	–	–	–	–	µA	4.5		V_{rH} = 3 V V_{rL} = 1.5 V
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	µA	4.5		$V_{rH} = V_{rL} = V_{CC}$ V_{IN} = 0 V

PAST mode

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{rH}	HIGH reference level, (V_{T+})	1.05	–	V_{CC} − 1.20	1.05	V_{CC} − 1.20	1.05	V_{CC} − 1.20	V	4.5 to 5.5		
V_{rL}	LOW reference level, (V_{T-})	1.00	–	V_{CC} − 1.25	1.00	V_{CC} − 1.25	1.00	V_{CC} − 1.25	V	4.5 to 5.5		
V_{Hmin}	Minimum hysteresis voltage, ($V_{rH} - V_{rL}$)	–	50	–	–	–	–	–	mV	4.5 to 5.5		

COMPARATOR mode

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{rHmin}	minimum reference level	–	0.6	–	–	–	–	–	V	4.5		over V_{ref} range
V_{rHmax}	maximum reference level	–	V_{CC}	–	–	–	–	–	V	4.5		over V_{ref} range

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_{rH}	V_{rL}	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.					
t_{PHL}	propagation delay V_{inn} to Q_n; PAST mode	–	50	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.13, t_r = 100 ns/V
t_{PLH}	propagation delay V_{inn} to Q_n; PAST mode	–	50	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.13, t_f = 100 ns/V
t_{PHL}	propagation delay V_{inn} to Q_n; Comparator mode	–	60	–	–	–	–	–	ns	4.5	$V_{CC}/2$	0.00	Fig.14, overdrive: 100 mV
t_{PLH}	propagation delay V_{inn} to Q_n; Comparator mode	–	50	–	–	–	–	–	ns	4.5	$V_{CC}/2$	0.00	Fig.14, overdrive: 100 mV
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	–	28	–	–	–	–	–	ns	4.5			Fig.15
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	20	–	–	–	–	–	ns	4.5			Fig.17
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	22	–	–	–	–	–	ns	4.5			Fig.17
t_{THL}/t_{TLH}	output transition time	–	10	–	–	–	–	–	ns	4.5			Fig.13
t_W	LE pulse width LOW	–	6	–	–	–	–	–	ns	4.5			Fig.15
t_{su}	set-up time V_{inn} to LE	–	25	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns
t_h	hold time V_{inn} to LE	–	−25	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns

AC WAVEFORMS

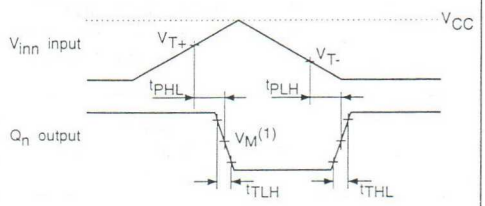


Fig.13 Waveforms showing the input (V_{inn}) to output Q_n propagation delays for PAST mode.

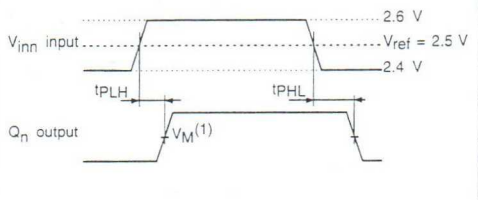


Fig.14 Waveforms showing the input (V_{inn}) to output Q_n propagation delays for Comparator mode at V_{rL} = 0 V and V_{ref} = $^1/_2V_{CC}$.

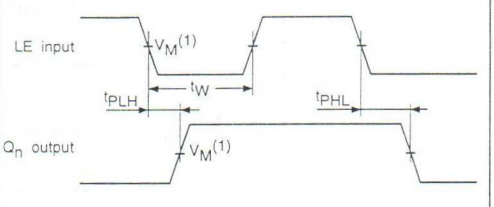


Fig.15 Waveforms showing the input (LE) to output Q_n propagation delays for Comparator mode.

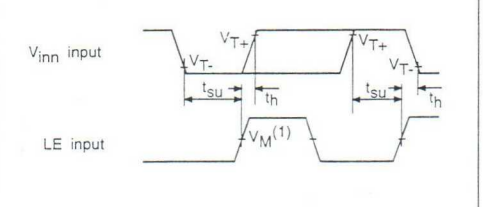


Fig.16 Waveforms showing the input set-up and hold times for V_{inn} input to LE input.

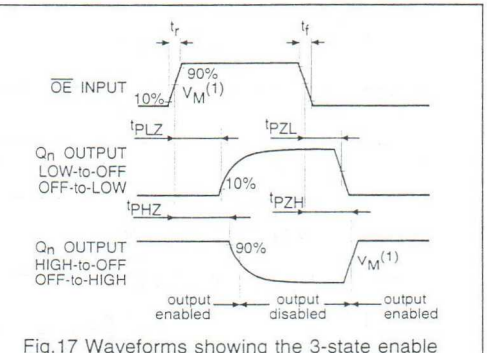


Fig.17 Waveforms showing the 3-state enable and disable times.

Note to the AC waveforms

(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL BUS SCHMITT-TRIGGER TRANSCEIVER; 3-STATE

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI
- Schmitt-trigger action on all data inputs

GENERAL DESCRIPTION

The 74HC/HCT7245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
The "7245" features and output enable ($\overline{OE}$) input for easy cascading and a send/receive input (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated. The 74HC/HCT7245 have Schmitt-trigger inputs. These inputs are capable of transforming slowly changing input signals into sharply defined jitter-free output signals.

The "7245" is identical to the "245" but has hysteresis on the data inputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	C_L = 15 pF; V_{CC} = 5 V	8	12	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

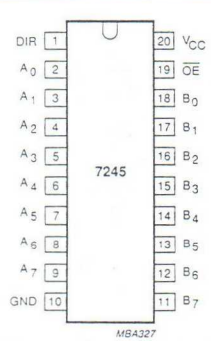


Fig. 1 Pin configuration.

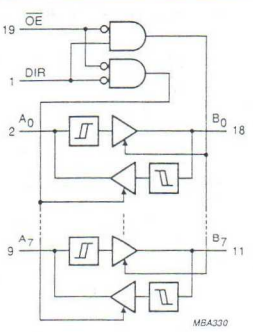


Fig. 2 Functional diagram.

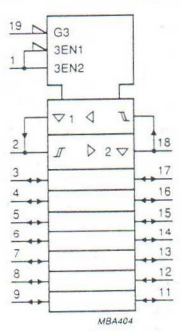


Fig. 3 IEC logic symbol.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			1.50 3.15 4.20		1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs. 4 and 5
V_{T-}	negative-going threshold	0.30 1.35 1.80			0.30 1.35 1.80		0.30 1.35 1.80		V	2.0 4.5 6.0	Figs. 4 and 5
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.1 0.25 0.3	0.2 0.4 0.5		0.1 0.25 0.3		0.1 0.25 0.3		V	2.0 4.5 6.0	Figs. 4 and 5

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n		47 17 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n		52 19 16	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.33
B_n	0.33
$\overline{OE}$	1.50
DIR	1.00

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			2.0 2.1		2.0 2.1		2.0 2.1	V	4.5 5.5	Figs. 4 and 5
V_{T-}	negative-going threshold	0.7 0.8			0.64 0.74		0.6 0.7		V	4.5 5.5	Figs. 4 and 5
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.17 0.17	0.23 0.23						V	4.5 5.5	Figs. 4 and 5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to B_n; B_n to A_n		17	30		37		45	ns	4.5	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n		19	32		40		48	ns	4.5	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n		19	32		40		48	ns	4.5	Fig. 7
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

TRANSFER CHARACTERISTIC WAVEFORMS

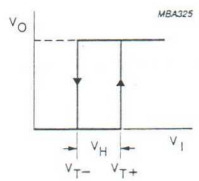


Fig. 4 Transfer characteristic.

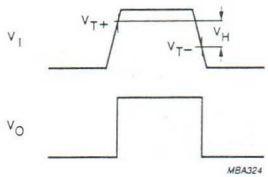


Fig. 5 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

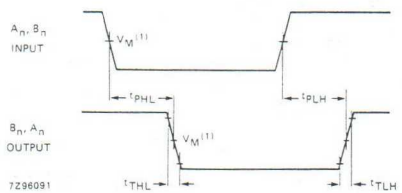


Fig. 6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

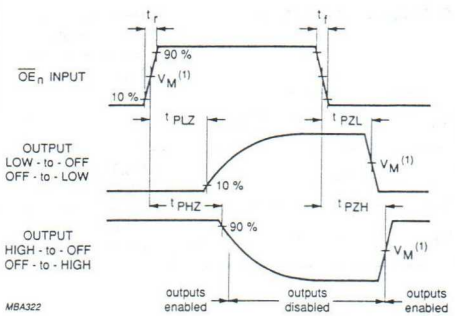


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT EXCLUSIVE-NOR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC7266 provide the EXCLUSIVE-NOR function with active push-pull output.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	note 1	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 8, 12	1A to 4A	data inputs
2, 6, 9, 13	1B to 4B	data inputs
3, 4, 10, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

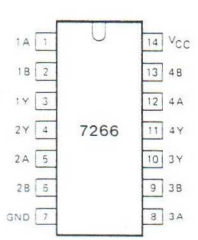


Fig. 1 Pin configuration.

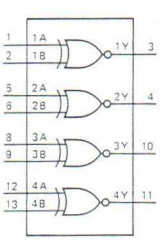


Fig. 2 Logic symbol.

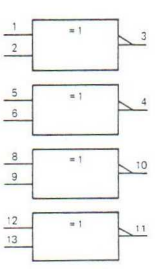


Fig. 3 IEC logic symbol.

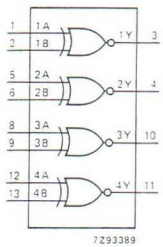


Fig. 4 Functional diagram.

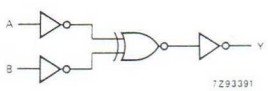


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

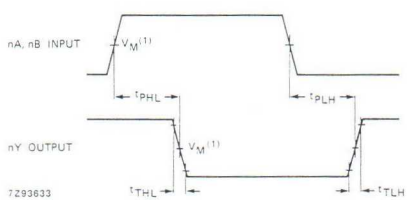


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

4-Bit × 64-word FIFO register; 3-state

74HC/HCT7403

FEATURES

- Synchronous or assynchronous operation
- 3-state outputs
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- I_{CC} category: LSI.

APPLICATIONS

- High-speed disc or tape controller
- Communications buffer.

GENERAL DESCRIPTION

The 74HC/HCT7403 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no.7A.

The "7403" is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 4 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$), an output enable input ($\overline{OE}$) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$, SI to DIR and DOR	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
f_{max}	maximum clock frequency		30	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	note 1	475	490	pF

Note

For HC the condition is V_I = GND to V_{CC}.
For HCT the condition is V_I = GND to V_{CC} −1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7403N	16	DIL	plastic	SOT38Z
74HC/HCT7403D	16	SO16L	plastic	SOT162

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
D_0 to D_3	4, 5, 6, 7	parallel data input
GND	8	ground
$\overline{MR}$	9	assynchronous master-reset input (active LOW)
Q_3 to Q_0	10, 11, 12, 13	data output
DOR	14	data-out-ready output
$\overline{SO}$	15	shift-out input (active LOW)
V_{CC}	16	positive supply voltage

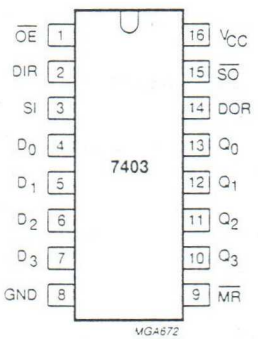


Fig.1 Pin configuration.

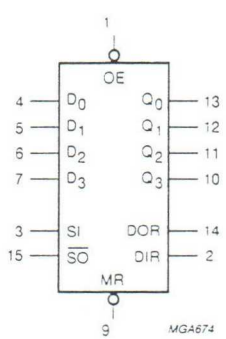


Fig.2 Logic symbol.

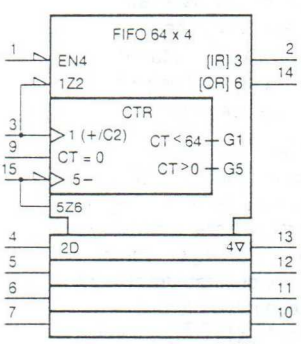


Fig.3 IEC logic symbol.

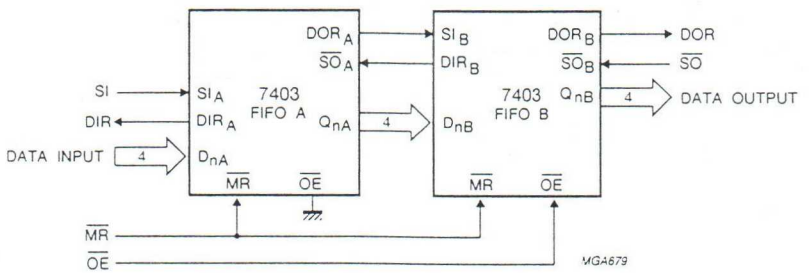


Fig.4 Functional diagram.

FUNCTIONAL DESCRIPTION

A DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D_0 to D_3 is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When $\overline{SO}$ and DOR are HIGH, data is available at the outputs (Q_0 to Q_3). When $\overline{SO}$ is set LOW new data may be shifted into the output stage, once complete DOR is set HIGH.

Expanded format (see Fig.17)

The DOR and DIR signals are used to allow the "7403" to be cascaded. Both parallel and serial expansion is possible.
Serial expansion is only possible with typical devices.

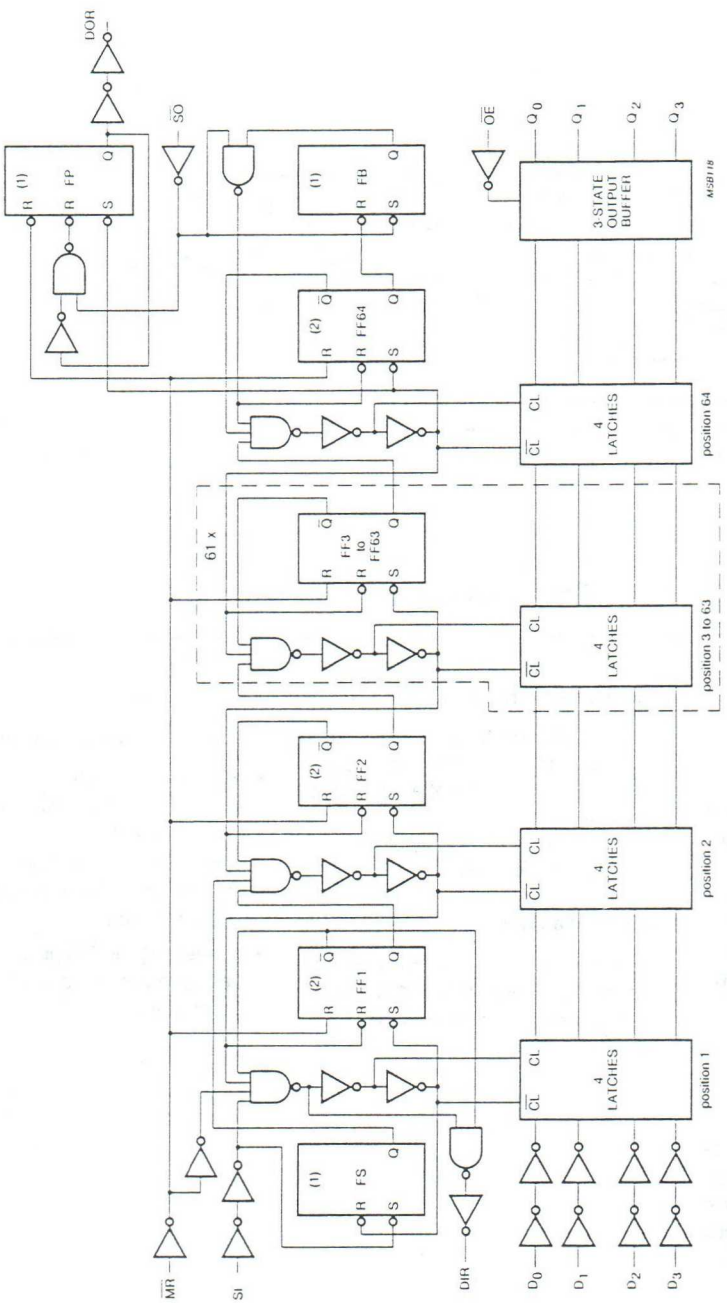
Parallel expansion

Parallel expansion is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

Serial expansion

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the $\overline{SO}$ pin of the first device to the DIR pin of the second device.



(see control flip-flops)
LOW on $\overline{S}$ input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on $\overline{R}$ input.
LOW on $\overline{R}$ input of FF1 to FF64 will set Q output to LOW independent of state on $\overline{S}$ input.

Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family specifications", except that V_{OH} and V_{OL} are not valid for driver output.
They are replaced by the values given below.

Output capability: driver 8 mA
I_{CC} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage driver outputs	3.98 5.48	4.32 5.81	– –	3.84 5.34	– –	3.70 5.20	– –	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = −8 mA I_O = −10 mA
V_{OL}	LOW level output voltage all outputs	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage driver outputs	– –	0.15 0.15	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = 8 mA I_O = 10 mA

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		−25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	–	69	210	–	265	–	315	ns	2.0	Fig.8
		–	25	42	–	53	–	63	ns	4.5	
		–	20	36	–	45	–	54	ns	6.0	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	52	160	–	200	–	240	ns	2.0	Fig.8
		–	19	32	–	40	–	48	ns	4.5	
		–	15	27	–	34	–	41	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay SI to DIR	–	66	205	–	255	–	310	ns	2.0	Fig.6
		–	24	41	–	51	–	62	ns	4.5	
		–	19	35	–	43	–	53	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	–	94	290	–	365	–	435	ns	2.0	Fig.9
		–	34	58	–	73	–	87	ns	4.5	
		–	27	49	–	62	–	74	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	–	11	35	–	45	–	55	ns	2.0	Fig.10
		–	4	7	–	9	–	11	ns	4.5	
		–	3	6.0	–	8	–	9	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	–	105	325	–	406	–	488	ns	2.0	Fig.14
		–	38	65	–	81	–	98	ns	4.5	
		–	30	55	–	69	–	83	ns	6.0	
t_{PLH}	propagation delay/ripple through delay SI to DOR	–	2.2	7	–	8.8	–	10.5	µs	2.0	Fig.10
		–	0.8	1.4	–	1.8	–	2.1	µs	4.5	
		–	0.6	1.2	–	1.5	–	1.8	µs	6.0	
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	2.8	9	–	11.2	–	13.5	µs	2.0	Fig.7
		–	1.0	1.8	–	2.2	–	2.7	µs	4.5	
		–	0.8	1.5	–	1.9	–	2.3	µs	6.0	
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n	–	44	150	–	190	–	225	ns	2.0	Fig.16
		–	16	30	–	38	–	45	ns	4.5	
		–	13	26	–	32	–	38	ns	6.0	
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n	–	50	150	–	190	–	225	ns	2.0	Fig.16
		–	18	30	–	38	–	45	ns	4.5	
		–	14	26	–	33	–	38	ns	6.0	
t_{THL}/t_{TLH}	output transition time	–	14	60	–	75	–	90	ns	2.0	Fig.16
		–	5	12	–	15	–	18	ns	4.5	
		–	4	10	–	13	–	15	ns	6.0	
t_W	SI pulse width HIGH or LOW	35	11	–	45	–	55	–	ns	2.0	Fig.6
		7	4	–	9	–	11	–	ns	4.5	
		6.0	3	–	8	–	9	–	ns	6.0	

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	$\overline{SO}$ pulse width HIGH or LOW	70	22	–	90	–	105	–	ns	2.0	Fig.9
		14	8	–	18	–	21	–	ns	4.5	
		12	6.0	–	15	–	18	–	ns	6.0	
t_W	DIR pulse width HIGH	10	41	130	8	165	8	195	ns	2.0	Fig.7
		5	15	26	4	33	4	39	ns	4.5	
		4	12	22	3	28	3	33	ns	6.0	
t_W	DOR pulse width HIGH	14	52	160	12	200	12	240	ns	2.0	Fig.10
		7	19	32	6	40	6.0	48	ns	4.5	
		6.0	15	27	5	34	5.0	41	ns	6.0	
t_W	$\overline{MR}$ pulse width LOW	120	39	–	150	–	180	–	ns	2.0	Fig.8
		24	14	–	30	–	36	–	ns	4.5	
		20	11	–	26	–	31	–	ns	6.0	
t_{rem}	removal time $\overline{MR}$ to SI	80	24	–	100	–	120	–	ns	2.0	Fig.15
		16	8	–	20	–	24	–	ns	4.5	
		14	7	–	17	–	20	–	ns	6.0	
t_{su}	set-up time D_n to SI	−8	−36	–	−6	–	−6	–	ns	2.0	Fig.13
		−4	−13	–	−3	–	−3	–	ns	4.5	
		−3	−10	–	−3	–	−3	–	ns	6.0	
t_h	hold time D_n to SI	135	44	–	170	–	205	–	ns	2.0	Fig.13
		27	16	–	34	–	41	–	ns	4.5	
		23	13	–	29	–	35	–	ns	6.0	
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	3.6	9.9	–	2.8	–	2.4	–	MHz	2.0	Figs 11 and 12
		18	30	–	14	–	12	–	MHz	4.5	
		21	36	–	16	–	14	–	MHz	6.0	
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	3.6	9.9	–	2.8	–	2.4	–	MHz	2.0	Figs 6 and 9
		18	30	–	14	–	12	–	MHz	4.5	
		21	36	–	16	–	14	–	MHz	6.0	
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	–	7.6	–	–	–	–	–	MHz	2.0	Figs 6 and 9
		–	23	–	–	–	–	–	MHz	4.5	
		–	27	–	–	–	–	–	MHz	6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications", except that V_{OH} and V_{OL} are not valid for driver output.
They are replaced by the values given below.

Output capability: driver 8 mA.
I_{CC} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage all outputs	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage driver outputs	3.98	4.32	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −8 mA
V_{OL}	LOW level output voltage all outputs	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage driver outputs	–	0.15	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = 8 mA

Notes to the HCT DC Characteristics

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
2. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1
SI	1.5
D_n	0.75
$\overline{MR}$	1.5
$\overline{SO}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		−25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	–	30	51	–	53	–	63	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	22	38	–	48	–	57	ns	4.5	Fig.8
t_{PHL}/t_{PLH}	propagation delay SI to DIR	–	25	43	–	54	–	65	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	–	36	61	–	76	–	92	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	–	42	72	–	90	–	108	ns	4.5	Fig.14
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	–	7	12	–	15	–	18	ns	4.5	Fig.10
t_{PLH}	propagation delay/ripple through delay SI to DOR	–	0.8	1.4	–	1.75	–	2.1	µs	4.5	Fig.10
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	1	1.8	–	2.25	–	2.7	µs	4.5	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	16	30	–	38	–	45	ns	4.5	Fig.16
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	19	30	–	38	–	45	ns	4.5	Fig.16
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.16
t_W	SI pulse width HIGH or LOW	9	5	–	6	–	8	–	ns	4.5	Fig.6
t_W	$\overline{SO}$ pulse width HIGH or LOW	14	8	–	18	–	21	–	ns	4.5	Fig.9

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	DIR pulse width HIGH	5	17	29	4	36	4	44	ns	4.5	Fig.7
t_W	DOR pulse width HIGH	7	21	36	6.0	45	6.0	54	ns	4.5	Fig.10
t_W	$\overline{MR}$ pulse width LOW	26	15	–	33	–	39	–	ns	4.5	Fig.8
t_{rem}	removal time $\overline{MR}$ to SI	18	10	–	23	–	27	–	ns	4.5	Fig.15
t_{su}	set-up time D_n to SI	−5	−16	–	−4	–	−4	–	ns	4.5	Fig.13
t_h	hold time D_n to SI	30	18	–	38	–	45	–	ns	4.5	Fig.13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	18	30	–	14	–	12	–	MHz	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	18	30	–	14	–	12	–	MHz	4.5	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	–	23	–	–	–	–	–	MHz	4.5	Figs 6 and 9

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

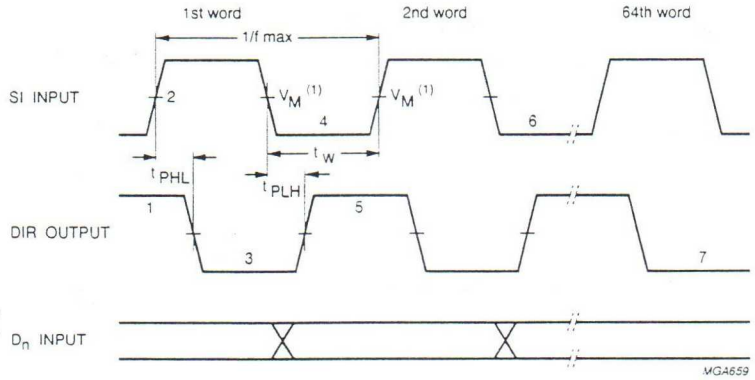


Fig.6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig.6

1. DIR initially HIGH; FIFO is prepared for valid data
2. SI set HIGH; data loaded into input stage
3. DIR goes LOW, input stage "busy"
4. SI set LOW; data from first location "ripple through"
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
6. Repeat process to load 2nd word through to 64th word into FIFO
   DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

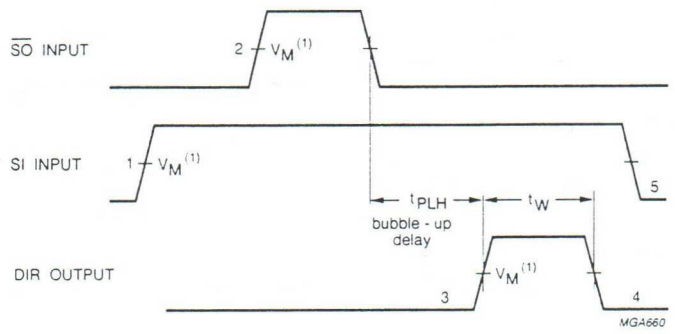


Fig.7 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig.7

1. FIFO is initially full, shift-in is held HIGH
2. $\overline{SO}$ pulse; data in the output stage is unloaded, "bubble-up" process of empty location begins
3. DIR HIGH; when empty location reaches input stage, flage indicates FIFO is prepared for data input
4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again
5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

Master reset applied with FIFO full

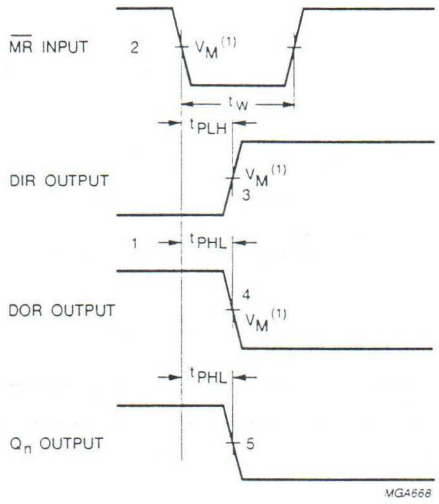


Fig.8 Waveforms showing the $\overline{MR}$ input to DIR, DOR and Q_n output propagation delays and the $\overline{MR}$ pulse width.

Notes to Fig.8

1. DIR LOW, output ready HIGH; assume FIFO is full
2. $\overline{MR}$ pulse LOW; clears FIFO
3. DIR goes HIGH; flag indicates input prepared for valid data
4. DOR goes LOW; flag indicates FIFO empty
5. Q_n outputs go LOW (only last bit will be reset).

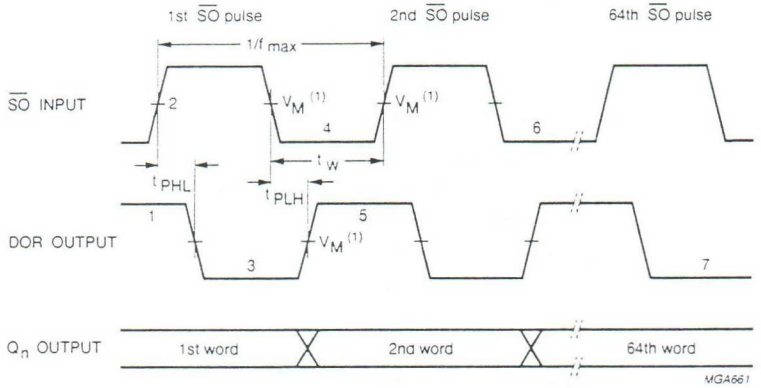


Fig.9 Waveforms showing the $\overline{SO}$ input to DOR output propagation delay. The $\overline{SO}$ pulse widths and maximum pulse frequency.

Notes to Fig.9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage
2. $\overline{SO}$ set HIGH; results in DOR going LOW
3. DOR goes LOW; output stage "busy"
4. $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
6. Repeat process to unload the 3rd through to the 64th word from FIFO
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation

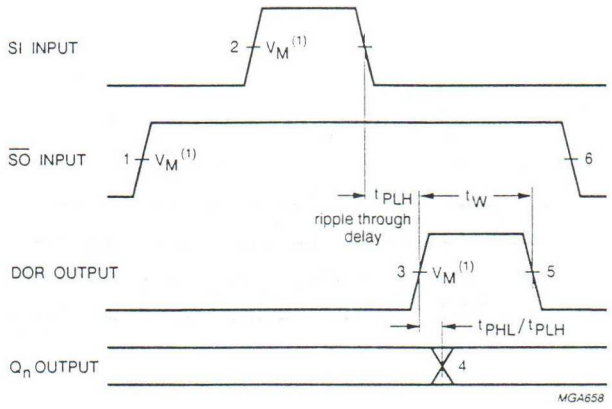


Fig.10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig.10

1. FIFO is initially empty, $\overline{SO}$ is held HIGH
2. SI pulse; loads data into FIFO and initiates ripple through process
3. DOR flag signals the arrival of valid data at the output stage
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output
5. DOR goes LOW; data shift-out is complete, FIFO is empty again
6. $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode

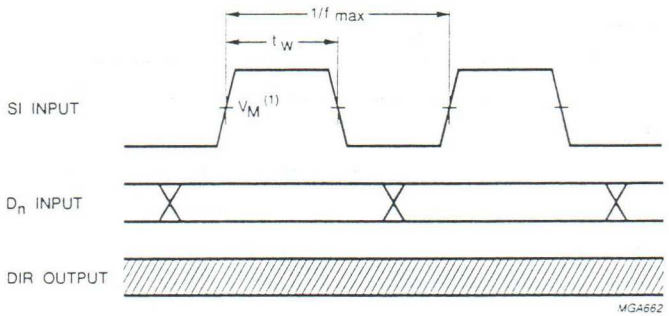


Fig.11 Waveforms showing SI minimum pulse width and maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig.11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

Shift-out operation; high-speed burst mode

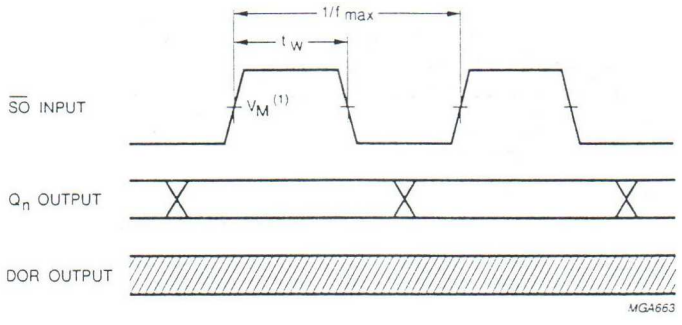
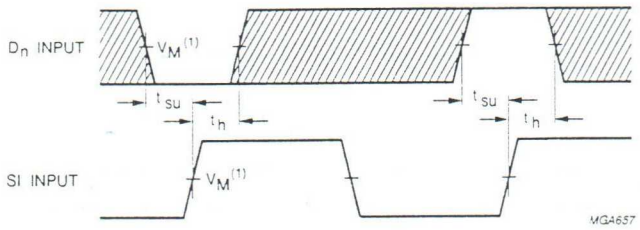


Fig.12 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig.12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an $\overline{SO}$ pulse can be applied without regard to the flag.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.13 Waveforms showing hold and set-up times for D_n input to SI input.

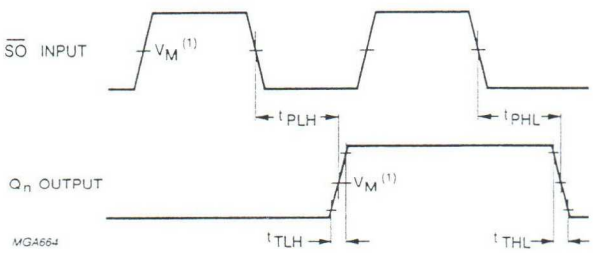


Fig.14 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

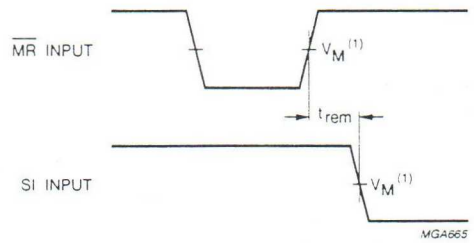


Fig.15 Waveform showing the $\overline{MR}$ input to SI input removal time.

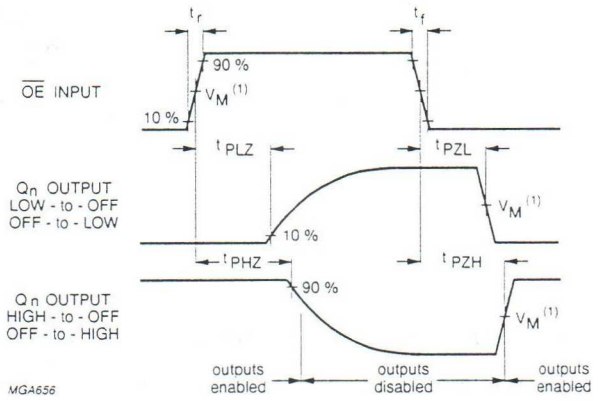


Fig.16 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

HC : VM = 50%; V_I = GND to V_{CC}.
HCT: VM = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

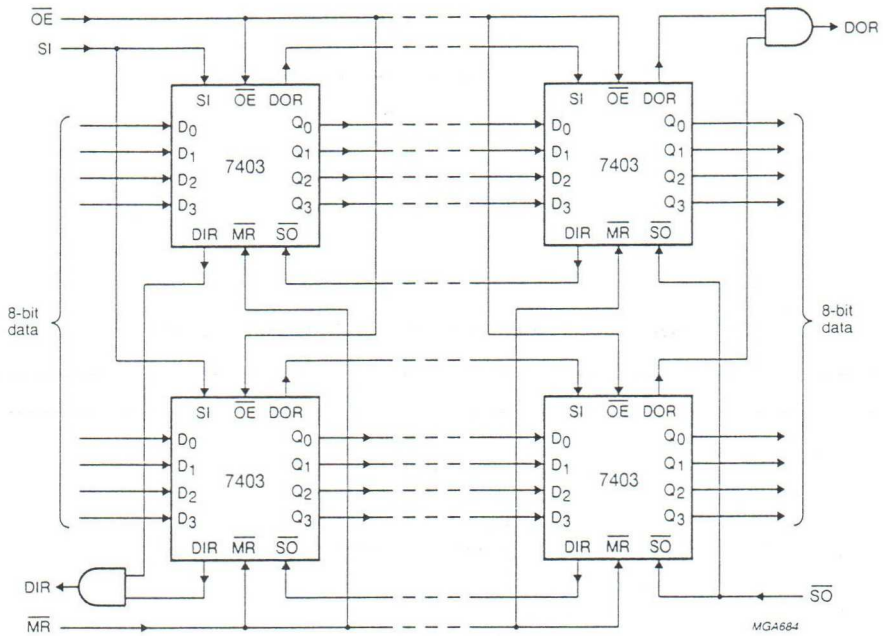


Fig.17 Expanded FIFO (parallel and serial) for increased word length; 8 bits wide x 64 n-bits.

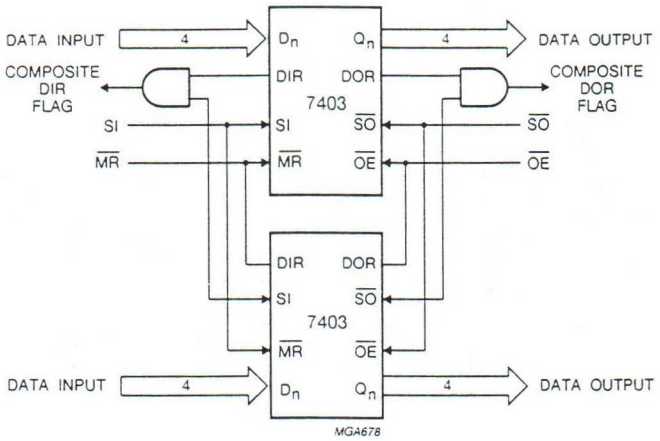


Fig.18 Expanded FIFO for increased word length; 64 words x 10 bits.

Note to Fig.18

The "7403" is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

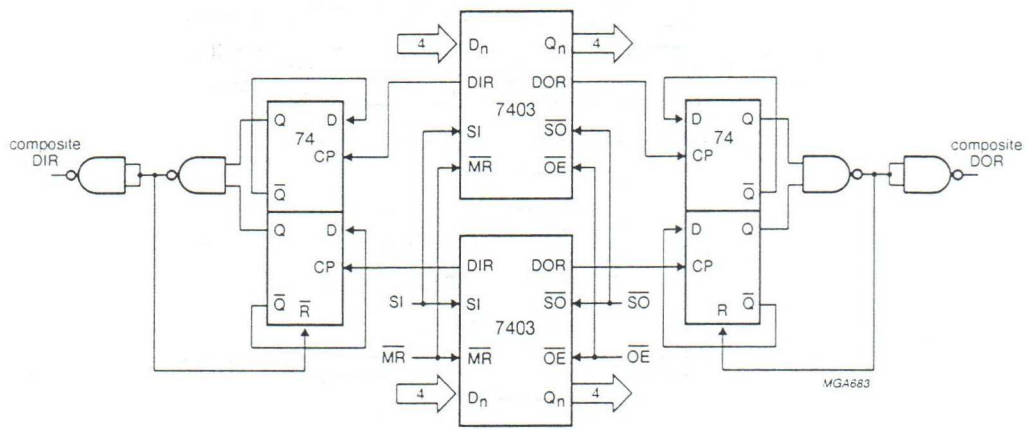


Fig.19 Expanded FIFO for increased word length.

Note to Fig.19

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

Expanded format

Figure 20 shows two cascaded FIFOs providing a capacity of 128 words x 4 bits. Figure 21 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR_A pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.

Figure 22 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH. Figure 23 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

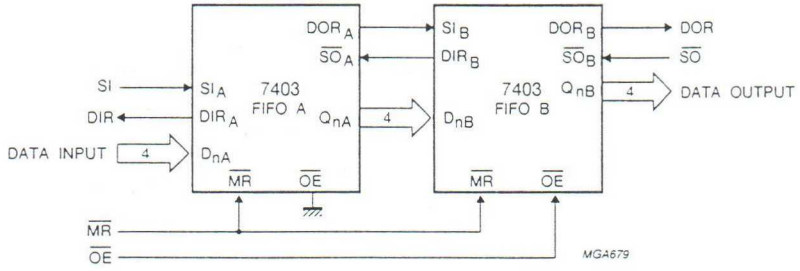


Fig.20 Cascading for increased word capacity; 128 words x 4 bits.

Note to Fig.20

The "7404" is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 21 and 22 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Figure 23 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

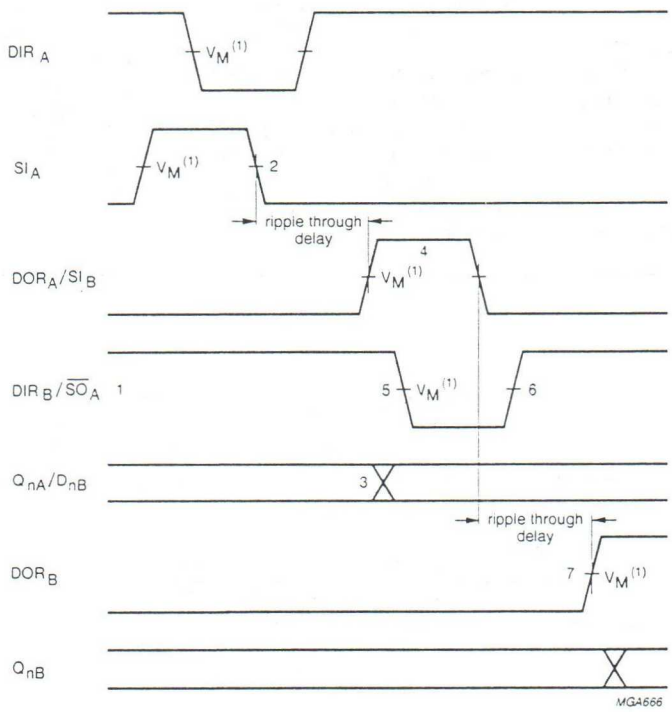


Fig.21 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig.21

1. $FIFO_A$ and $FIFO_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data
2. Load one word into $FIFO_A$; SI pulse applied, results in DIR pulse
3. Data-out $_A$/data-in $_B$ transition; valid data arrives at $FIFO_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of $FIFO_B$
4. DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from $FIFO_A$ as a result of the data output ready pulse, data is shifted into $FIFO_B$
5. DIR_B and $\overline{SO}_A$ go LOW; flag indicates input stage of $FIFO_B$ is busy, shift-out of $FIFO_A$ is complete
6. DIR_B and $\overline{SO}_A$ go HIGH automatically; the input stage of $FIFO_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data
7. DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the $FIFO_B$ output stage.

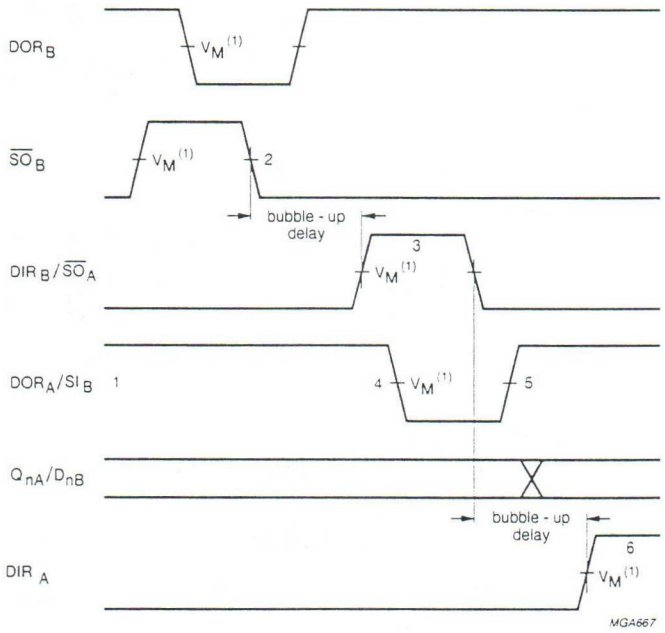


Fig.22 FIFO to FIFO communication; output timing under full condition.

Notes to Fig.22

1. $FIFO_A$ and $FIFO_B$ initially full, SI_B held HIGH in anticipation of shifting in new data as an empty location bubbles-up
2. Unload one word from $FIFO_B$; $\overline{SO}$ pulse applied, results in DOR pulse
3. DIR_B and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into $FIFO_B$ as a result of the DIR pulse, data is shifted out of $FIFO_A$
4. DOR_A and SI_B go LOW; flag indicates the output stage of $FIFO_A$ is busy, shift-in to $FIFO_B$ is complete
5. DOR_A and SI_B go HIGH; flag indicates valid data is again available at $FIFO_A$ output stage, SI_B is held HIGH, awaiting bubble-up of empty location
6. DIR_A goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of $FIFO_A$.

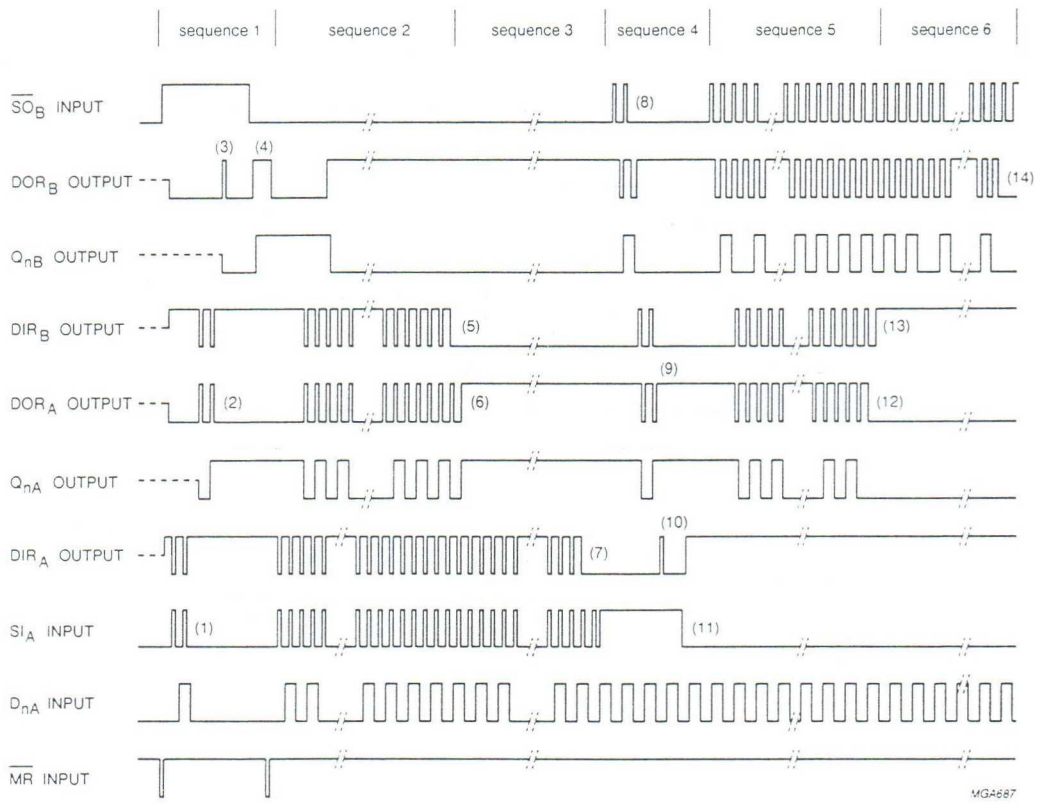


Fig.23 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig.18).

Note to Fig.23

Sequence 1 (both FIFOS empty, starting SHIFT-IN process)

After a $\overline{MR}$ pulse has been applied $FIFO_A$ and $FIFO_B$ are empty. The DOR flags of $FIFO_A$ and $FIFO_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of $FIFO_A$ and to the input stage of $FIFO_B$ (2). When data arrives at the output of $FIFO_B$, a DOR_B pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full)

After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full)

When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Squence 4 (both FIFOs full, starting SHIFT-OUT process)

SI_A is held HIGH and two $\overline{SO}_B$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty)

At the start of sequence 5 $FIFO_A$ contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of $\overline{SO}_B$ pulses are applied. After 63 $\overline{SO}_B$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty)

After the next $\overline{SO}_B$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty. After another 63 $\overline{SO}_B$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO}_B$ pulses have no effect. The last word remains available at the output Q_n.

5-Bit × 64-word FIFO register; 3-state 74HC/HCT7404

FEATURES

- Synchronous or assynchronous operation
- 3-state outputs
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- I_{CC} category: LSI.

APPLICATIONS

- High-speed disc or tape controller
- Communications buffer.

GENERAL DESCRIPTION

The 74HC/HCT7404 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no.7A.

The "7404" is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 5 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$), an output enable input ($\overline{OE}$) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$, SI to DIR and DOR	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
f_{max}	maximum clock frequency		30	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	note 1	475	490	pF

Note

For HC the condition is V_I = GND to V_{CC}.
For HCT the condition is V_I = GND to V_{CC} −1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7404N	18	DIL	plastic	SOT102
74HC/HCT7404D	20	SO20	plastic	SOT163A

PINNING (SOT102)

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
D_0 to D_4	4, 5, 6, 7, 8	parallel data inputs
GND	9	ground
$\overline{MR}$	10	assynchronous master-reset input (active LOW)
Q_4 to Q_0	11, 12, 13, 14, 15	data outputs
DOR	16	data-out-ready output
$\overline{SO}$	17	shift-out input (active LOW)
V_{CC}	18	positive supply voltage

PINNING (SOT163A)

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
n.c.	4	not connected
D_0 to D_4	5, 6, 7, 8, 9	parallel data inputs
GND	10	ground
$\overline{MR}$	11	Assynchronous master-reset input (active LOW)
Q_4 to Q_0	12, 13, 14, 15, 16	data outputs
n.c.	17	not connected
DOR	18	data-out ready output
n.c.	19	not connected
V_{CC}	20	positive supply voltage

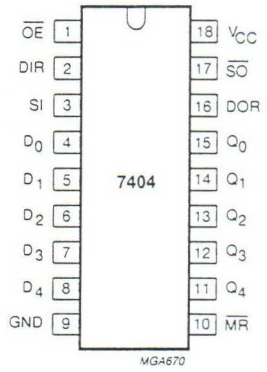


Fig.1 Pin configuration (SOT102).

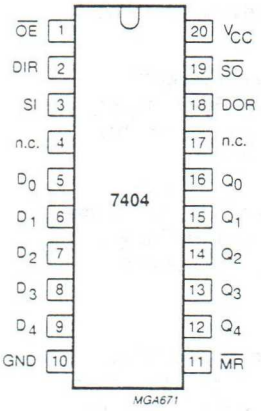
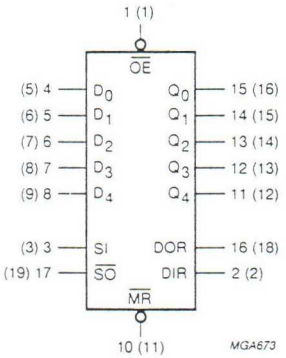
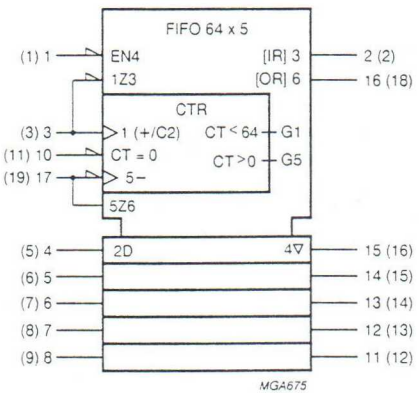


Fig.2 Pin configuration (SOT163).



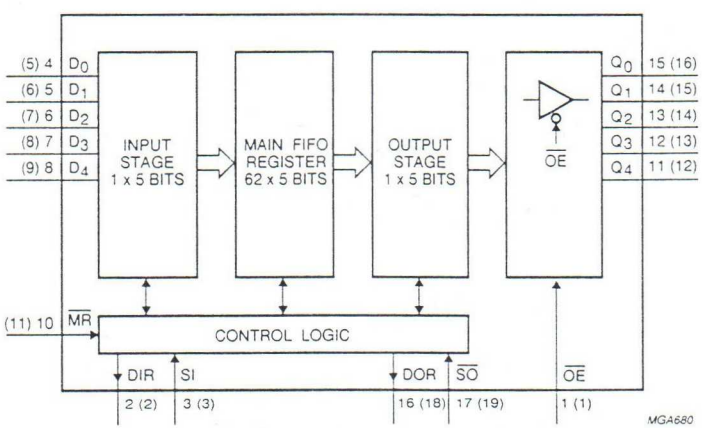
Pin numbers between parentheses refer to the SO package.

Fig.3 Logic symbol.



Pin numbers between parentheses refer to the SO package.

Fig.4 IEC logic symbol.



Pin numbers between parentheses refer to the SO package.

Fig.5 Functional diagram.

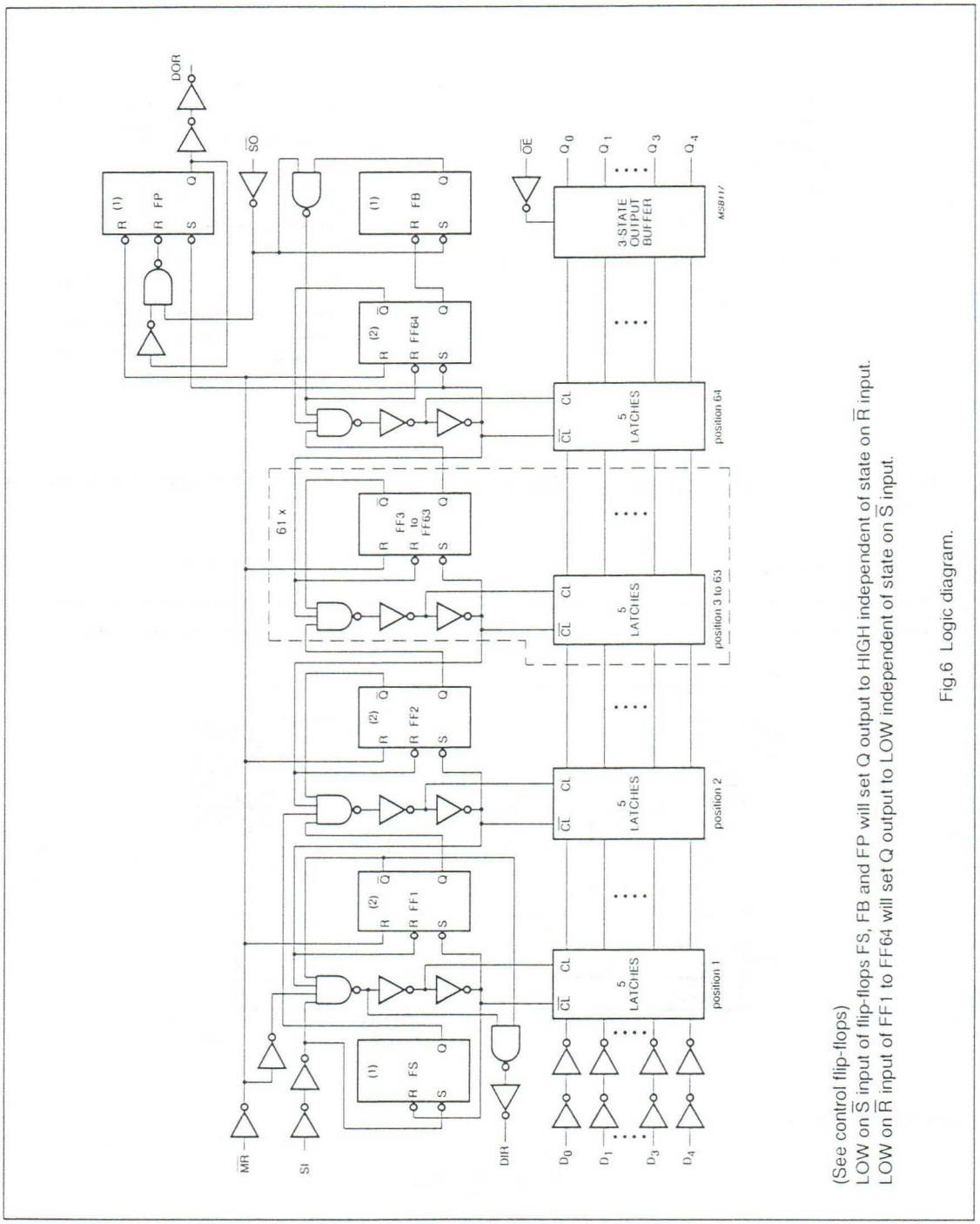


Fig.6 Logic diagram.

(See control flip-flops)
LOW on $\overline{S}$ input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on $\overline{R}$ input.
LOW on $\overline{R}$ input of FF1 to FF64 will set Q output to LOW independent of state on $\overline{S}$ input.

FUNCTIONAL DESCRIPTION

The DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D_0 to D_4 is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When $\overline{SO}$ and DOR are HIGH, data is available at the outputs (Q_0 to Q_4). When $\overline{SO}$ is LOW new data may be shifted into the output stage, once complete DOR is set LOW.

Expanded Format (see Fig.18)

The DOR and DIR signals are used to allow the "7404" to be cascaded. Both parallel and serial expansion is possible. Serial expansion is only possible with typical devices.

Parallel Expansion

Parallel expansion is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

Serial Expansion

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the $\overline{SO}$ pin of the first device to the DIR pin of the second device.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI

Output capability: driver 8 mA
I_{CC} category: LSI

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81	– –	3.84 5.34	– –	3.70 5.20	– –	V V	4.5 6	V_{IH} or V_{IL}	I_O = −8 mA I_O = −10 mA
V_{OL}	LOW level output voltage	– –	0.15 0.15	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6	V_{IH} or V_{IL}	I_O = 8 mA I_O = 10 mA

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	–	69	210	–	265	–	315	ns	2.0	Fig.9
		–	25	42	–	53	–	63	ns	4.5	
		–	20	36	–	45	–	54	ns	6.0	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	52	160	–	200	–	240	ns	2.0	Fig.9
		–	19	32	–	40	–	48	ns	4.5	
		–	15	27	–	34	–	41	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay SI to DIR	–	66	205	–	255	–	310	ns	2.0	Fig.7
		–	24	41	–	51	–	62	ns	4.5	
		–	19	35	–	43	–	53	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	–	94	290	–	365	–	435	ns	2.0	Fig.10
		–	34	58	–	73	–	87	ns	4.5	
		–	27	49	–	62	–	74	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	–	11	35	–	45	–	55	ns	2.0	Fig.11
		–	4	7	–	9	–	11	ns	4.5	
		–	3	6.0	–	8	–	9	ns	6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	–	105	325	–	406	–	488	ns	2.0	Fig.15
		–	38	65	–	81	–	98	ns	4.5	
		–	30	55	–	69	–	83	ns	6.0	
t_{PLH}	propagation delay/ripple through delay SI to DOR	–	2.2	7.0	–	8.8	–	10.5	µs	2.0	Fig.16
		–	0.8	1.4	–	1.8	–	2.1	µs	4.5	
		–	0.6	1.2	–	1.5	–	1.8	µs	6.0	
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	2.8	9.0	–	11.2	–	13.5	µs	2.0	Fig.8
		–	1.0	1.8	–	2.2	–	2.7	µs	4.5	
		–	0.8	1.5	–	1.9	–	2.3	µs	6.0	
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n	–	44	150	–	190	–	225	ns	2.0	Fig.17
		–	16	30	–	38	–	45	ns	4.5	
		–	13	26	–	32	–	38	ns	6.0	
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n	–	50	150	–	190	–	225	ns	2.0	Fig.17
		–	18	30	–	38	–	45	ns	4.5	
		–	14	26	–	33	–	38	ns	6.0	
t_{THL}/t_{TLH}	output transition time	–	14	60	–	75	–	90	ns	2.0	Fig.17
		–	5	12	–	15	–	18	ns	4.5	
		–	4	10	–	13	–	15	ns	6.0	
t_W	SI pulse width HIGH or LOW	35	11	–	45	–	55	–	ns	2.0	Fig.7
		7	4	–	9	–	11	–	ns	4.5	
		6	3	–	8	–	9	–	ns	6.0	

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	$\overline{SO}$ pulse width HIGH or LOW	70 14 12	22 8 6	– – –	90 18 15	– – –	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.10
t_W	DIR pulse width HIGH	10 5 4	41 15 12	130 26 22	8 4 3	165 33 28	8 4 3	195 39 33	ns ns ns	2.0 4.5 6.0	Fig.8
t_W	DOR pulse width HIGH	14 7 6	52 19 15	160 32 27	12 6 5	200 40 34	12 6 5	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.11
t_W	$\overline{MR}$ pulse width LOW	120 24 20	39 14 11	– – –	150 30 26	– – –	180 36 31	– – –	ns ns ns	2.0 4.5 6.0	Fig.9
t_{rem}	removal time $\overline{MR}$ to SI	80 16 14	24 8 7	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.16
t_{su}	set-up time D_n to SI	−8 −4 −3	−36 −13 −10	– – –	−6 −3 −3	– – –	−6 −3 −3	– – –	ns ns ns	2.0 4.5 6.0	Fig.14
t_h	hold time D_n to SI	135 27 23	44 16 13	– – –	170 34 29	– – –	205 41 35	– – –	ns ns ns	2.0 4.5 6.0	Fig.14
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	3.6 18 21	9.9 30 36	– – –	2.8 14 16	– – –	2.4 12 14	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 12 and 13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	3.6 18 21	9.9 30 36	– – –	2.8 14 16	– – –	2.4 12 14	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 7 and 10
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	– – –	7.6 23 27	– – –	– – –	– – –	– – –	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 7 and 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS Family Characteristics", section "Family Specifications", except that V_{OH} and V_{OL} are not valid for driver output. They are replaced by the values given below.

Output capability: driver 8 mA
I_{CC} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage	3.98	4.32	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −8 mA
V_{OL}	LOW level output voltage	–	0.15	0.26	–	0.33	–	0.40	V	4.5	V_{IH} or V_{IL}	I_O = 8 mA

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1
SI	1.5
D_n	0.75
$\overline{MR}$	1.5
$\overline{SO}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	–	30	51	–	53	–	63	ns	4.5	Fig.9
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	22	38	–	48	–	57	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay SI to DIR	–	25	43	–	54	–	65	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	–	36	61	–	76	–	92	ns	4.5	Fig.10
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	–	42	72	–	90	–	108	ns	4.5	Fig.15
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	–	7	12	–	15	–	18	ns	4.5	Fig.11
t_{PLH}	propagation delay/ripple through delay SI to DOR	–	0.8	1.4	–	1.75	–	2.1	µs	4.5	Fig.11
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	1	1.8	–	2.25	–	2.7	µs	4.5	Fig.8
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n	–	16	30	–	38	–	45	ns	4.5	Fig.17
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n	–	19	30	–	38	–	45	ns	4.5	Fig.17
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.17
t_W	SI pulse width HIGH or LOW	9	5	–	6	–	8	–	ns	4.5	Fig.7
t_W	$\overline{SO}$ pulse width HIGH or LOW	14	8	–	18	–	21	–	ns	4.5	Fig.10

SYMBOL	PARAMETER	T_{amb} °C							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	DIR pulse width HIGH	5	17	29	4	36	4	44	ns	4.5	Fig.8
t_W	DOR pulse width HIGH	7	21	36	6	45	6	54	ns	4.5	Fig.11
t_W	$\overline{MR}$ pulse width LOW	26	15	–	33	–	39	–	ns	4.5	Fig.9
t_{rem}	removal time $\overline{MR}$ to SI	18	10	–	23	–	27	–	ns	4.5	Fig.16
t_{su}	set-up time D_n to SI	−5	−16	–	−4	–	−4	–	ns	4.5	Fig.14
t_h	hold time D_n to SI	30	18	–	38	–	45	–	ns	4.5	Fig.14
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	18	30	–	14	–	12	–	MHz	4.5	Figs 12 and 13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	18	30	–	14	–	12	–	MHz	4.5	Figs 7 and 10
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	–	23	–	–	–	–	–	MHz	4.5	Figs 7 and 10

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

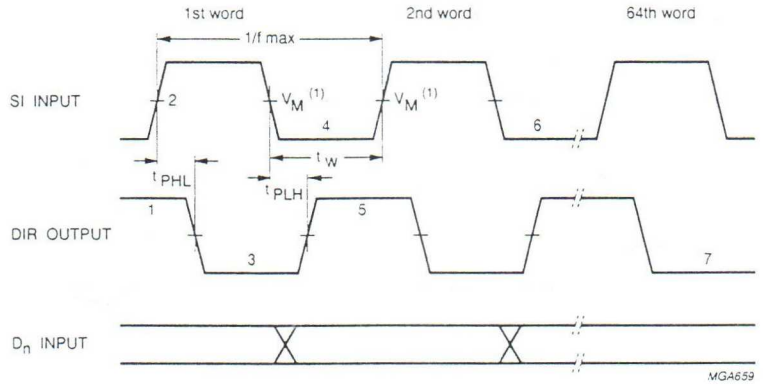


Fig.7 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig.7

1. DIR initially HIGH; FIFO is prepared for valid data
2. SI set HIGH; data loaded into input stage
3. DIR goes LOW, input stage "busy"
4. SI set LOW; data from first location "ripple through"
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
6. Repeat process to load 2nd word through to 64th word into FIFO
   DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

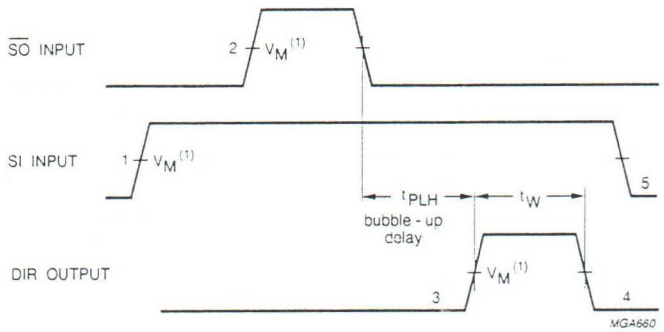


Fig.8 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig.8

1. FIFO is initially full, shift-in is held HIGH
2. $\overline{SO}$ pulse; data in the output stage is unloaded, "bubble-up" process of empty location begins
3. DIR HIGH; when empty location reaches input stage, flag indicates FIFO is prepared for data input
4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again
5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

Master reset applied with FIFO full

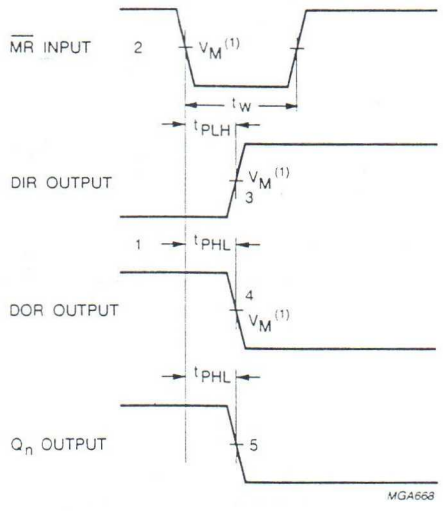


Fig.9 Waveforms showing the $\overline{MR}$ input to DIR, DOR and Q_n output propagation delays and the $\overline{MR}$ pulse width.

Notes to Fig.9

1. DIR LOW, output ready HIGH; assume FIFO is full
2. $\overline{MR}$ pulse LOW; clears FIFO
3. DIR goes HIGH; flag indicates input prepared for valid data
4. DOR goes LOW; flag indicates FIFO empty
5. Q_n outputs go LOW (only last bit will be reset).

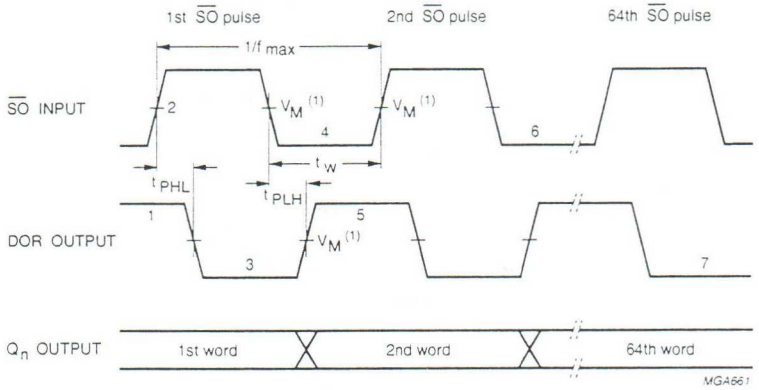


Fig.10 Waveforms showing the $\overline{SO}$ input to DOR output propagation delay. The $\overline{SO}$ pulse widths and maximum pulse frequency.

Notes to Fig.10

1. DOR HIGH; no data transfer in progress, valid data is present at output stage
2. $\overline{SO}$ set HIGH; results in DOR going LOW
3. DOR goes LOW; output stage "busy"
4. $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
6. Repeat process to unload the 3rd through to the 64th word from FIFO.
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation

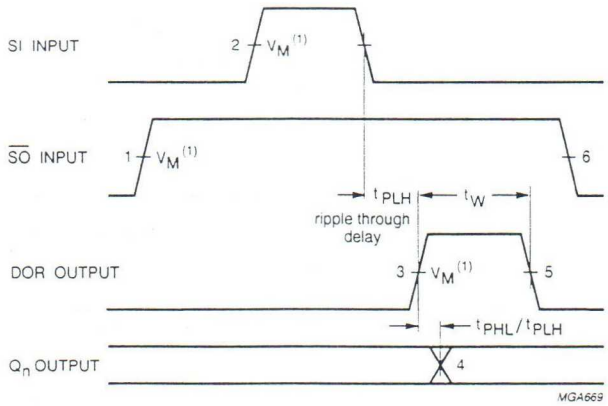


Fig.11 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig.11

1. FIFO is initially empty, $\overline{SO}$ is held HIGH
2. SI pulse; loads data into FIFO and initiates ripple through process
3. DOR flag signals the arrival of valid data at the output stage
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output
5. DOR goes LOW; data shift-out is complete, FIFO is empty again
6. $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode

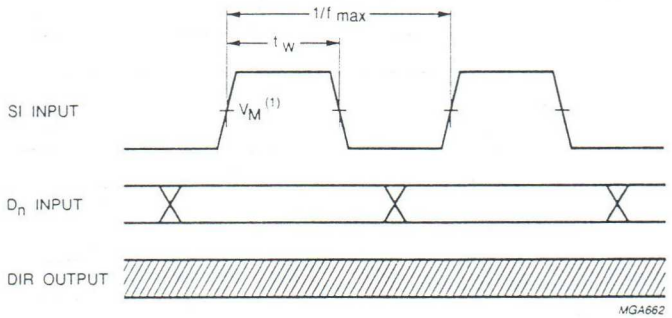


Fig.12 Waveforms showing SI minimum pulse width and maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig.12

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

Shift-out operation; high-speed burst mode

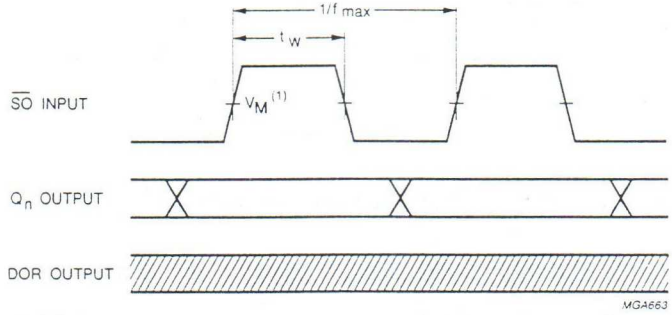
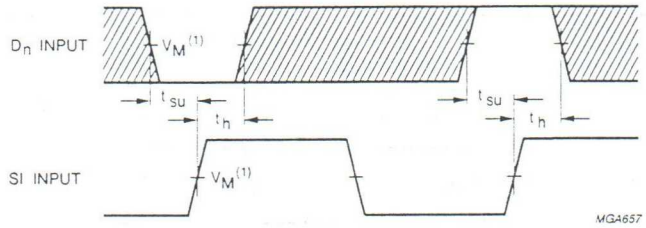


Fig.13 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig.13

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an $\overline{SO}$ pulse can be applied without regard to the flag.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.14 Waveforms showing hold and set-up times for D_n input to SI input.

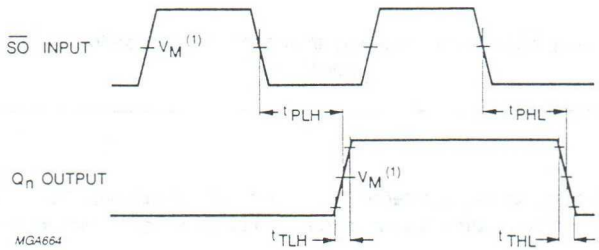


Fig.15 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

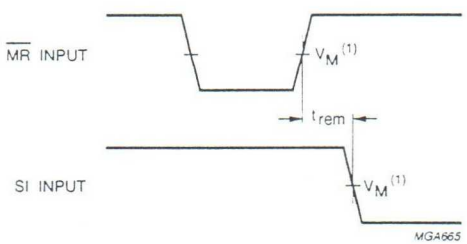


Fig.16 Waveform showing the $\overline{MR}$ input to SI input removal time.

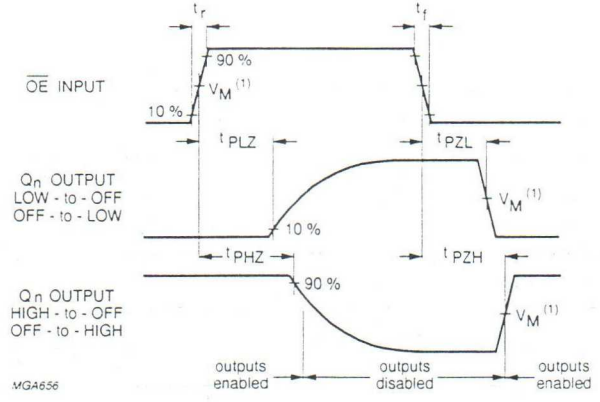


Fig.17 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC Waveforms

HC : VM = 50%; V_I = GND to V_{CC}.

HCT : VM = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

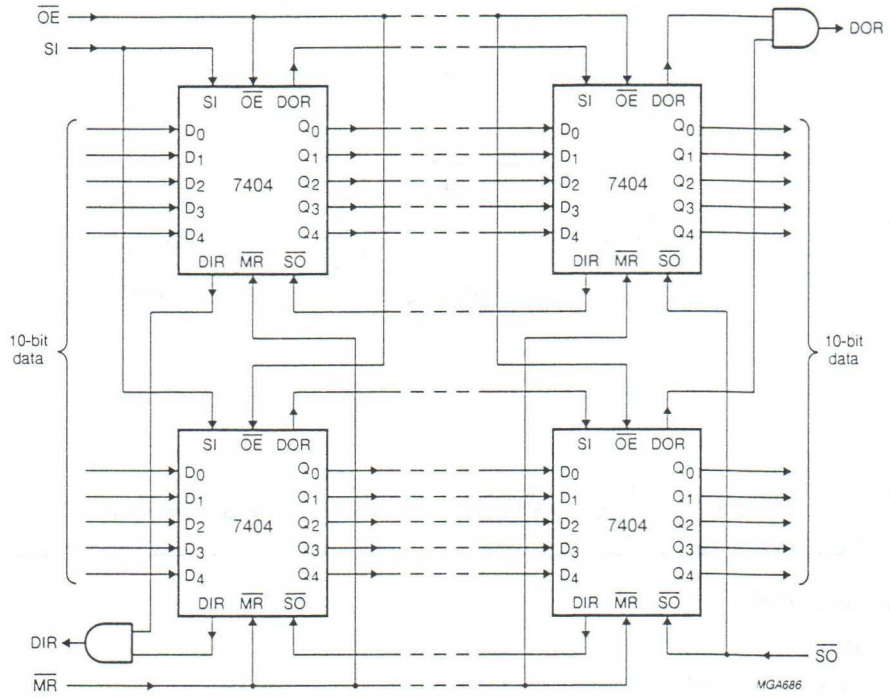


Fig.18 Expanded FIFO (parallel and serial) for increased word length; 10 bits wide x 64 n-bits.

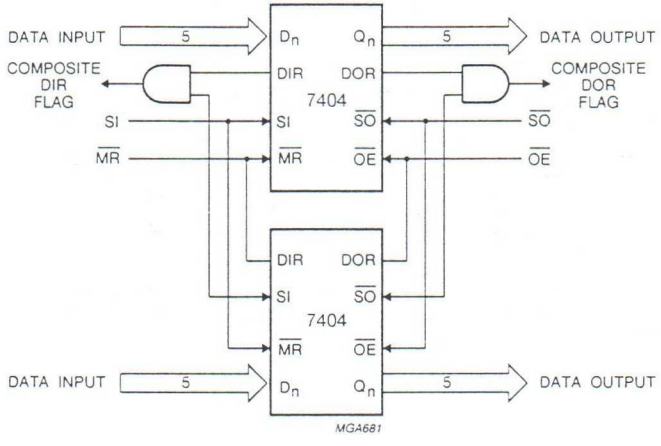


Fig.19 Expanded FIFO for increased word length; 64 words x 10 bits.

Note to Fig.19

The "7404" is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

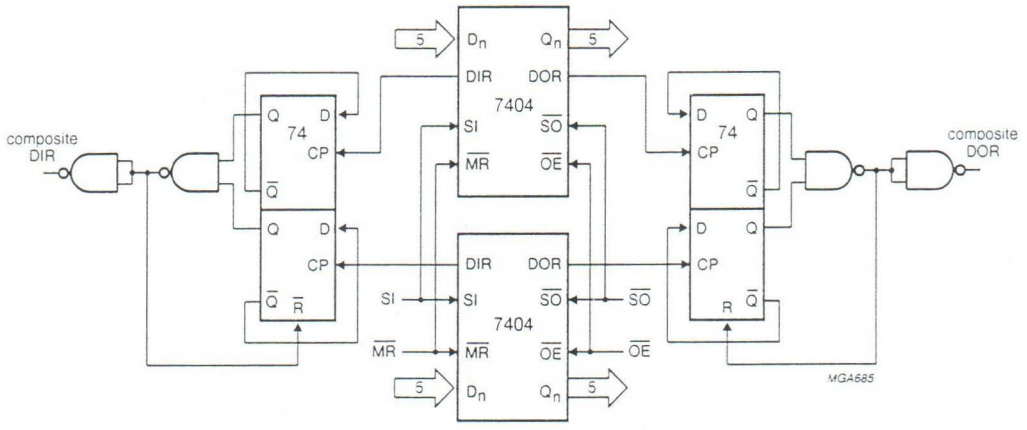


Fig.20 Expanded FIFO for increased word length.

Note to Fig.20

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 8 and 10).

Expanded format

Figure 21 shows two cascaded FIFOs providing a capacity of 128 words x 5 bits. Figure 22 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR_A pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.

Figure 23 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH. Figure 24 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

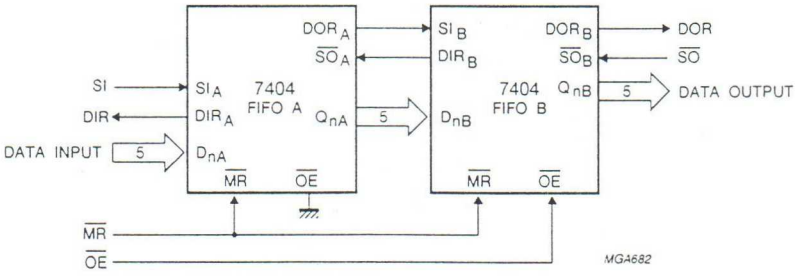


Fig.21 Cascading for increased word capacity; 128 words x 5 bits.

Note to Fig.21

The "7404" is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 22 and 23 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Figure 24 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

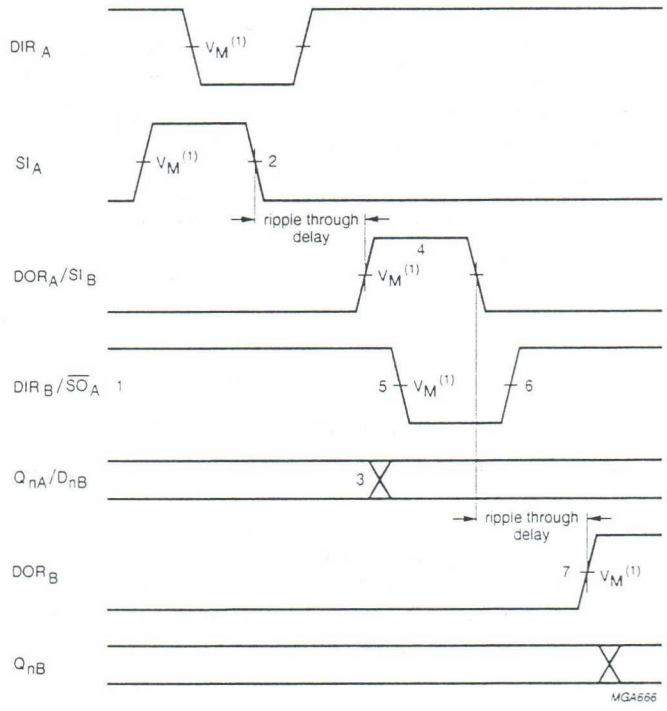


Fig.22 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig.22

1. $FIFO_A$ and $FIFO_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data
2. Load one word into $FIFO_A$; SI pulse applied, results in DIR pulse
3. Data-out $_A$/data-in $_B$ transition; valid data arrives at $FIFO_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of $FIFO_B$
4. DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from $FIFO_A$ as a result of the data output ready pulse, data is shifted into $FIFO_B$
5. DIR_B and $\overline{SO}_A$ go LOW; flag indicates input stage of $FIFO_B$ is busy, shift-out of $FIFO_A$ is complete
6. DIR_B and $\overline{SO}_A$ go HIGH automatically; the input stage of $FIFO_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data
7. DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the $FIFO_B$ output stage.

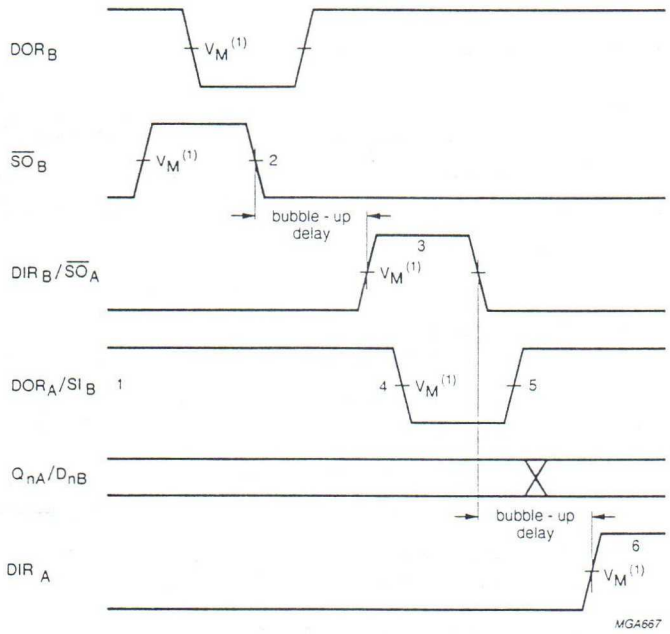


Fig.23 FIFO to FIFO communication; output timing under full condition.

Notes to Fig.23

1. $FIFO_A$ and $FIFO_B$ initially full, SI_B held HIGH in anticipation of shifting in new data as an empty location bubbles-up
2. Unload one word from $FIFO_B$; $\overline{SO}$ pulse applied, results in DOR pulse
3. DIR_B and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into $FIFO_B$ as a result of the DIR pulse, data is shifted out of $FIFO_A$
4. DOR_A and SI_B go LOW; flag indicates the output stage of $FIFO_A$ is busy, shift-in to $FIFO_B$ is complete
5. DOR_A and SI_B go HIGH; flag indicates valid data is again available at $FIFO_A$ output stage, SI_B is held HIGH, awaiting bubble-up of empty location
6. DIR_A goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of $FIFO_A$.

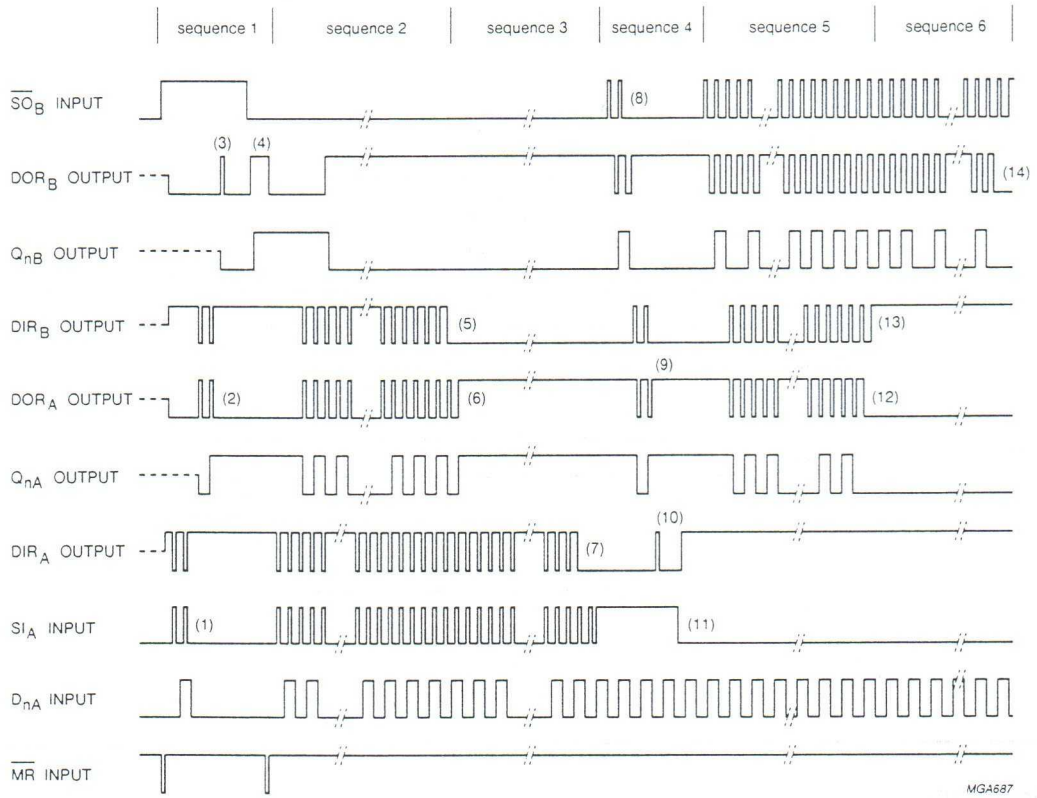


Fig.24 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig.19).

Note to Fig.24

Sequence 1 (both FIFOS empty, starting SHIFT-IN process)

After a $\overline{MR}$ pulse has been applied $FIFO_A$ and $FIFO_B$ are empty. The DOR flags of $FIFO_A$ and $FIFO_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of $FIFO_A$ and to the input stage of $FIFO_B$ (2). When data arrives at the output of $FIFO_B$, a DOR_B pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full)

After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full)

When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Squence 4 (both FIFOs full, starting SHIFT-OUT process)

SI_A is held HIGH and two $\overline{SO_B}$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty)

At the start of sequence 5 $FIFO_A$ contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of $\overline{SO_B}$ pulses are applied. After 63 $\overline{SO_B}$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty)

After the next $\overline{SO_B}$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty. After another 63 $\overline{SO_B}$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO_B}$ pulses have no effect. The last word remains available at the output Q_n.

SUPERSEDES DATA OF MARCH 1988

OCTAL SCHMITT TRIGGER BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Schmitt trigger action on all data inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7540 are octal Schmitt trigger inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The Schmitt trigger action in the data inputs transforms slowly changing input signals into sharply defined jitter-free output signals.

The "7540" is identical to the "540" but has hysteresis on the data inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	11	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	29	31	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

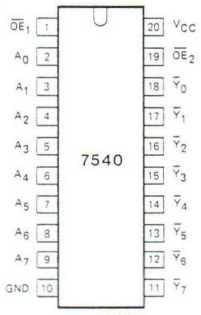


Fig. 1 Pin configuration.

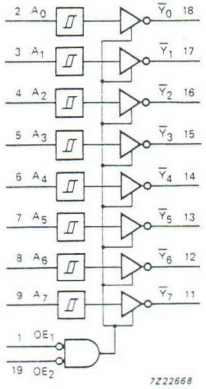


Fig. 2 Logic symbol.

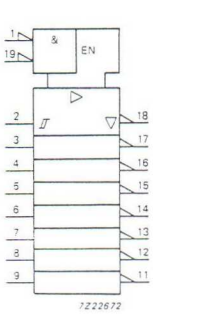


Fig. 3 IEC logic symbol.

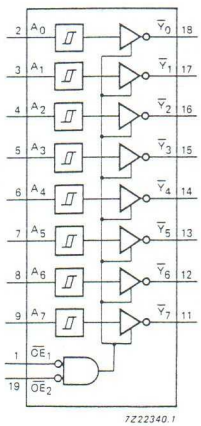


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	A_n	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

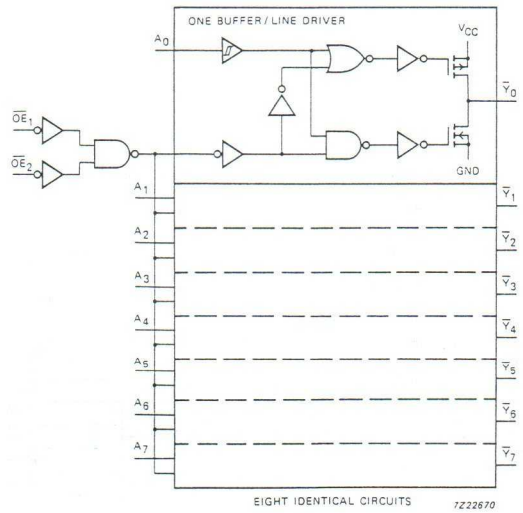


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below (not applicable for $\overline{OE}_n$ inputs).

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 8

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			1.50 3.15 4.20		1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.30 1.35 1.80			0.30 1.35 1.80		0.30 1.35 1.80		V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.10 0.25 0.30	0.20 0.40 0.50		0.10 0.25 0.30		0.10 0.25 0.30		V	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below (not applicable for $\overline{OE}_n$ inputs).

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.30
$\overline{OE}_2$	1.30
A_n	0.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$		19	32		40		48	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		19	32		40		48	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		20	32		40		48	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 8

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			2.0 2.1		2.0 2.1		2.0 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.70 0.80			0.64 0.74		0.60 0.70		V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.17 0.17	0.23 0.23						V	4.5 5.5	Figs 6 and 7

TRANSFER CHARACTERISTIC WAVEFORMS

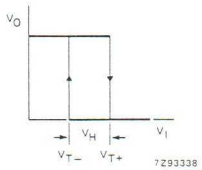


Fig. 6 Transfer characteristic.

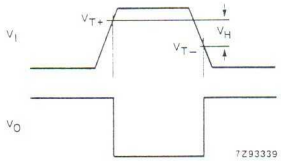


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

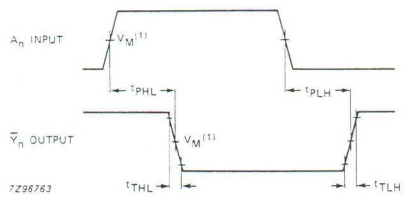


Fig. 8 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

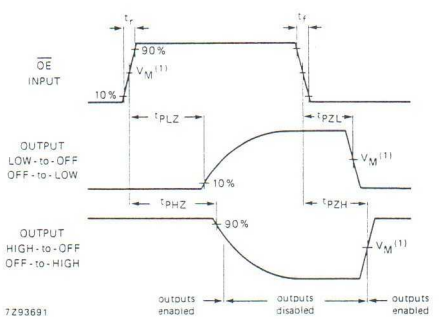


Fig. 9 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

SUPERSEDES DATA OF MARCH 1988

OCTAL SCHMITT TRIGGER BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Schmitt trigger action on all data inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7541 are octal Schmitt trigger non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The Schmitt trigger action in the data inputs transforms slowly changing input signals into sharply defined jitter-free output signals.

The "7541" is identical to the "541" but has hysteresis on the data inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	10	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

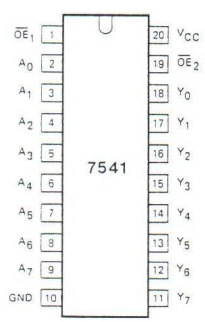


Fig. 1 Pin configuration.

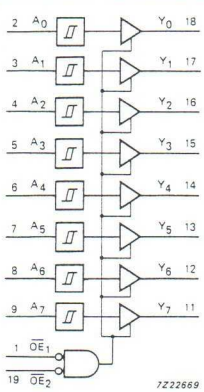


Fig. 2 Logic symbol.

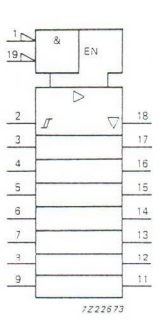


Fig. 3 IEC logic symbol.

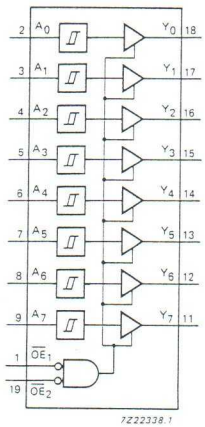


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

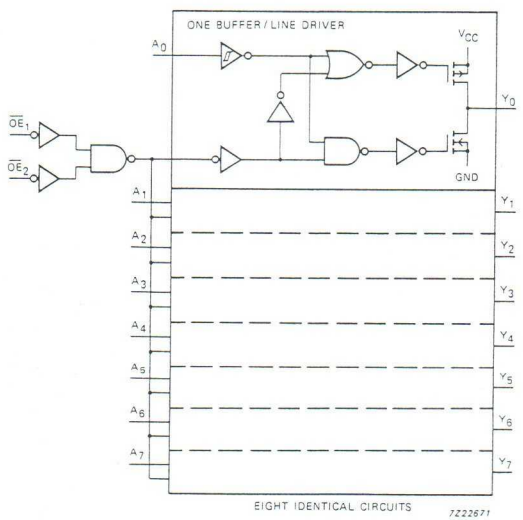


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below (not applicable for $\overline{OE}_n$ inputs).

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		39 14 11	120 24 20		150 30 26		180 36 32	ns	2.0 4.5 6.0	Fig. 8
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y_n		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y_n		58 21 17	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 8

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			1.50 3.15 4.20		1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.30 1.35 1.80			0.30 1.35 1.80		0.30 1.35 1.80		V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.10 0.25 0.30	0.20 0.40 0.50		0.10 0.25 0.30		0.10 0.25 0.30		V	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below (not applicable for $\overline{OE}_n$ inputs).

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.30
$\overline{OE}_2$	1.30
A_n	0.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n		19	32		40		48	ns	4.5	Fig. 8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y_n		18	32		40		48	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y_n		20	32		40		48	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 8

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold			2.0 2.1		2.0 2.1		2.0 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.70 0.80			0.64 0.74		0.60 0.70		V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.17 0.17	0.23 0.23						V	4.5 5.5	Figs 6 and 7

TRANSFER CHARACTERISTIC WAVEFORMS

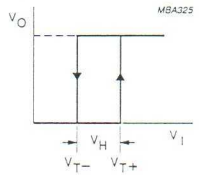


Fig. 6 Transfer characteristic.

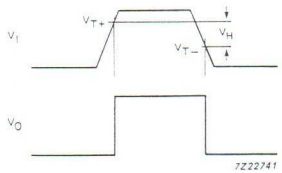


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

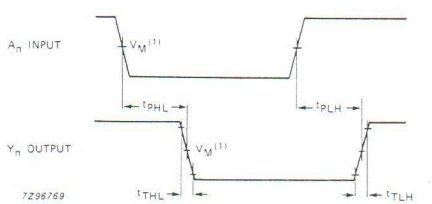


Fig. 8 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

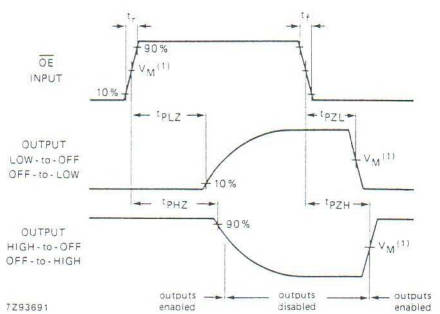


Fig. 9 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT SHIFT REGISTER WITH INPUT LATCHES

FEATURES

- 8-bit parallel input latches
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7597 both consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register.

When $\overline{LE}$ is LOW, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When $\overline{LE}$ is HIGH the latches store the information that was present at the D-inputs, a set-up time preceding the LOW-to-HIGH transition of $\overline{LE}$.

The shift register has a positive edge-triggered clock, direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
	propagation delay $\overline{LE}$ to Q		22	27	ns
	propagation delay $\overline{PL}$ to Q		20	23	ns
	propagation delay D_7 to Q		20	24	ns
f_{max}	maximum clock frequency SH_{CP}		99	79	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package		29	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH_{CP}	shift clock input (LOW-to-HIGH, edge-triggered)
12	$\overline{LE}$	latch enable input (active LOW)
13	$\overline{PL}$	parallel load input (active LOW)
14	D_S	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D_0 to D_7	parallel data inputs
16	V_{CC}	positive supply voltage

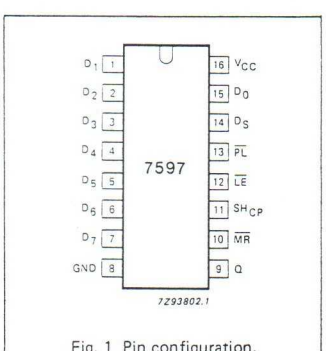


Fig. 1 Pin configuration.

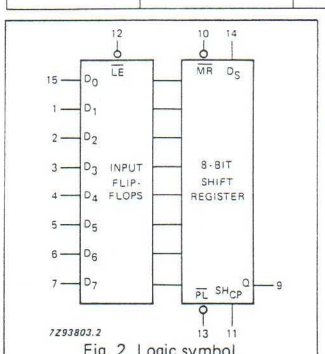


Fig. 2 Logic symbol.

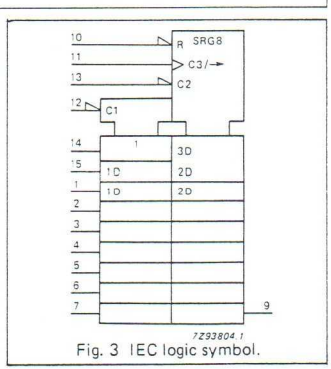


Fig. 3 IEC logic symbol.

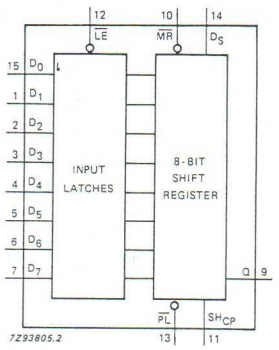


Fig. 4 Functional diagram.

FUNCTION TABLE

$\overline{LE}$	SH_{CP}	$\overline{PL}$	$\overline{MR}$	FUNCTION
L	X	X	X	data enabled to input latches (transparent)
H	X	X	X	data stored into latches (non-transparent)
X	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

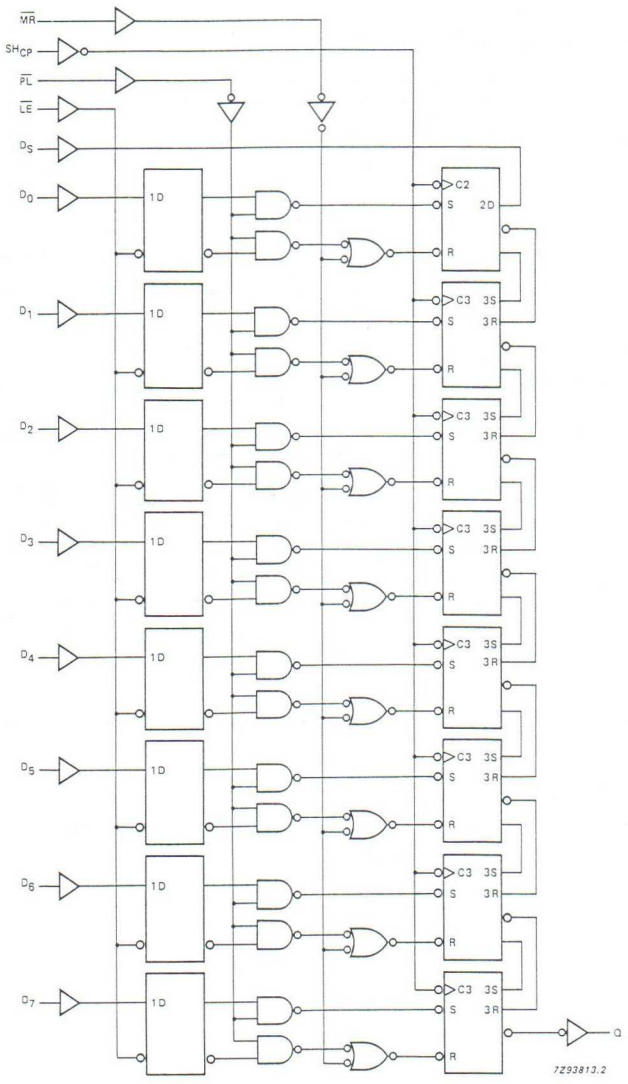


Fig. 5 Logic diagram.

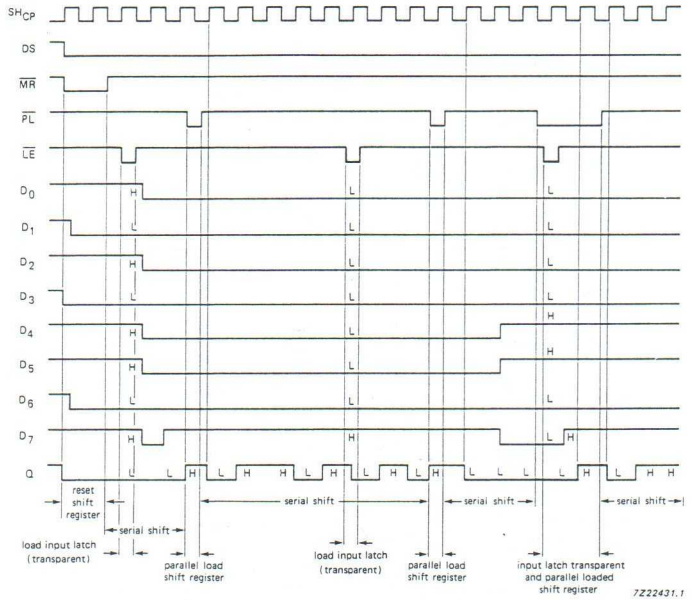


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q		72 26 21	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay D_7 to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 11
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t_W	SH_{CP} pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	$\overline{LE}$ pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_W	$\overline{MR}$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	$\overline{PL}$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	50 10 9	−3 −1 −1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 12
t_{rem}	removal time $\overline{MR}$ to $\overline{PL}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
t_{su}	set-up time D_n to $\overline{LE}$	80 16 14	6 2 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time D_S to SH_{CP}	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	80 16 14	8 3 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14

AC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to $\overline{LE}$	4 4 4	−3 −1 −1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 13
t_h	hold time D_S to SH_{CP}	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 13
t_h	hold time $\overline{PL}$ to SH_{CP}	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 14
f_{max}	maximum pulse frequency SH_{CP}	6.0 30 35	30 90 107		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
D_n	0.40
$\overline{PL}$, $\overline{MR}$	1.50
$\overline{LE}$, SH_{CP}	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q		20	35		44		53	ns	4.5	Fig. 7
t_{PHL}	propagation delay $\overline{MR}$ to Q		25	42		53		63	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q		31	53		66		80	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q		27	46		58		69	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay D_7 to Q		28	49		61		74	ns	4.5	Fig. 11
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 10
t_W	SH_{CP} pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 7
t_W	$\overline{LE}$ pulse width LOW	16	7		20		24		ns	4.5	Fig. 9
t_W	$\overline{MR}$ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t_W	$\overline{PL}$ pulse width LOW	18	9		23		27		ns	4.5	Fig. 10
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	10	−1		13		15		ns	4.5	Fig. 12
t_{rem}	removal time $\overline{MR}$ to $\overline{PL}$	20	9		25		30		ns	4.5	Fig. 14
t_{su}	set-up time D_n to $\overline{LE}$	16	5		20		24		ns	4.5	Fig. 13
t_{su}	set-up time D_S to SH_{CP}	16	5		20		24		ns	4.5	Fig. 13
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	16	3		20		24		ns	4.5	Fig. 12
t_h	hold time D_n to $\overline{LE}$	4	−2		4		4		ns	4.5	Fig. 13
t_h	hold time D_S to SH_{CP}	2	−4		2		2		ns	4.5	Fig. 13
t_h	hold time $\overline{PL}$ to SH_{CP}	2	−3		2		2		ns	4.5	Fig. 14
f_{max}	maximum pulse frequency SH_{CP}	30	72		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

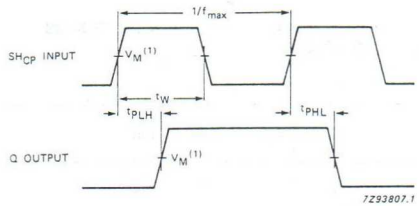


Fig. 7 Waveforms showing the SH_{CP} input to Q output propagation delays, the SH_{CP} pulse width and maximum clock pulse frequency.

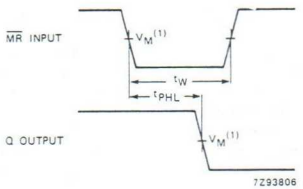


Fig. 8 Waveforms showing the $\overline{MR}$ input to Q output propagation delay and the $\overline{MR}$ pulse width.

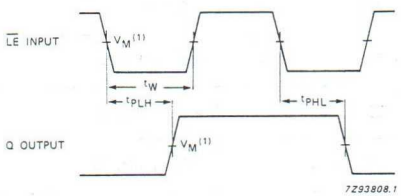


Fig. 9 Waveforms showing the $\overline{LE}$ input to Q output propagation delays and the $\overline{LE}$ pulse width.

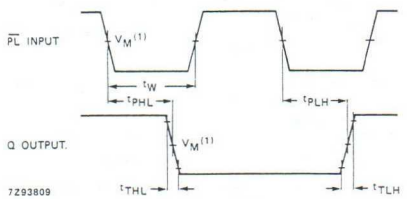


Fig. 10 Waveforms showing the $\overline{PL}$ input to Q output propagation delays, $\overline{PL}$ pulse width and output transition times.

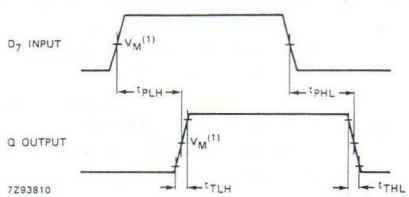


Fig. 11 Waveforms showing the D_7 input to Q output propagation delays and output transition times.

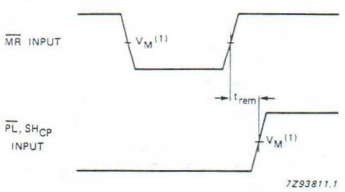


Fig. 12 Waveforms showing the $\overline{MR}$ input to $\overline{PL}$, SH_{CP} removal times.

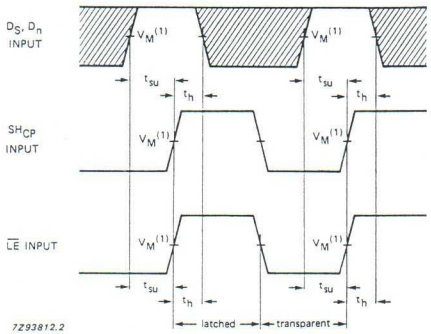


Fig. 13 Waveforms showing hold and set-up times for D_S, D_n inputs to SH_{CP}, $\overline{LE}$ inputs.

Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.

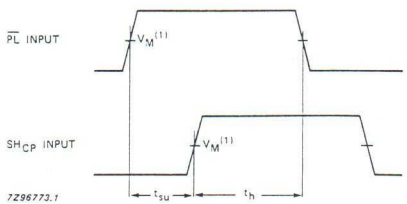


Fig. 14 Waveforms showing set-up and hold times for $\overline{PL}$ input to SH_{CP} input.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Quad 64-bit static shift register 74HC/HCT7731

FEATURES

- Frequency range DC to 100 MHz.
- Separate serial data inputs
- Cascadable
- Functionally compatible with HEF 4731
- Includes recycling mode
- Direct shift out
- Output capability: Standard
- I_{CC} category: LSI.

APPLICATIONS

- Data storage
- Delay line.

GENERAL DESCRIPTION

The HC/HCT7731 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT7731 are quad 64-bit static shift registers with a recycling mode. Each register has separate data inputs D_a to D_d, clock inputs CP_a to CP_d and data outputs Q_a to Q_d. Data shifts one place towards the output, each LOW to HIGH transition of the clock pulse. Each recycling mode input controls two registers REC_{ab} for registers A and B and REC_{cd} for registers C and D. When the REC input is HIGH, the device is in the recycling mode and data at the output is shifted back into the input of the register, so after 64 clock pulses the contents of a register is again in its original position. This enables the user to tap off data from any position. When the REC input is LOW external data can be shifted in.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_{a-d} to Q_{a-d}	C_L = 15 pF V_{CC} = 5 V	15	20	ns
f_{max}	maximum clock frequency		100	100	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per register	notes 1, 2 and 3	58	61	pF

Notes

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$$

where:

f_i = input frequency in MHz.
f_o = output frequency in MHz.
V_{CC} = supply voltage in V.
C_L = output load capacitance in pF.
$I_{pull\text{-}up}$ = pull-up currents in µA.

For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V.

See also power dissipation information.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7731N	16	DIL	plastic	SOT38Z
74HC/HCT7731D	16	SO16	plastic	SOT109A

PINNING

SYMBOL	PIN	DESCRIPTION
Q_a to Q_d	1, 7, 9, 15	data outputs
CP_a to CP_d	2, 6, 10, 14	clock inputs
D_a to D_d	3, 5, 11, 13	data inputs
REC_{ab}, REC_{cd}	4, 12	recycled enable input
GND	8	ground (0 V)
V_{CC}	16	positive supply

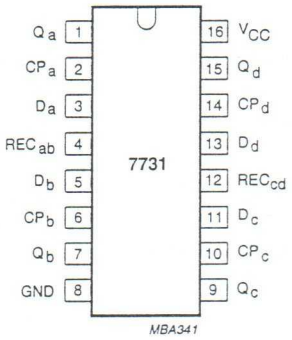


Fig.1 Pin configuration.

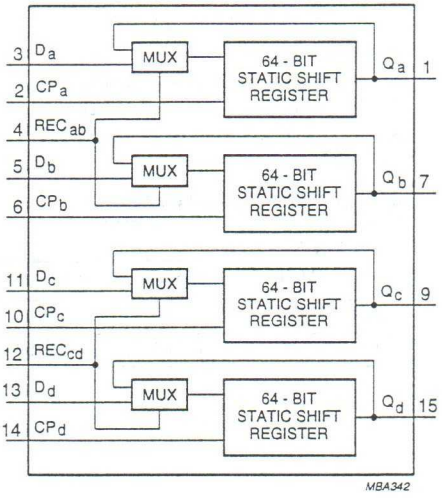


Fig.2 Functional diagram.

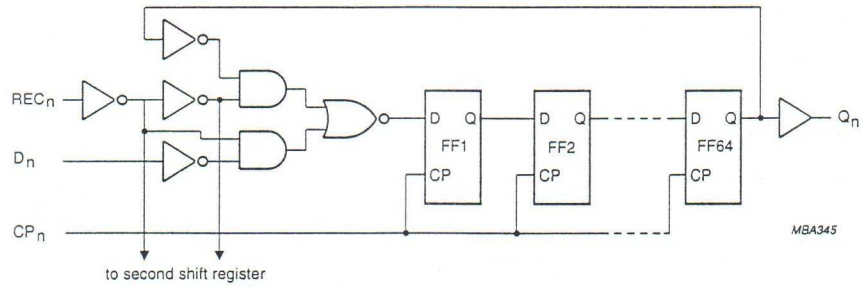


Fig.3 Logic diagram.

FUNCTION TABLE

INPUT		OUTPUT
REC	CP	MODE
L	↑	shift
H	↑	recycle

Notes to Function Table

1. L = LOW voltage level
2. H = HIGH voltage Level
3. ↑ = LOW-to-HIGH CP transistion

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: LSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay time CP to Q_n	–	50	155	–	190	–	230	ns	2.0	Fig.4
		–	18	31	–	38	–	46	ns	4.5	
		–	15	26	–	32	–	39	ns	6.0	
t_{THL}/t_{TLH}	output transistion time	–	19	75	–	90	–	110	ns	2.0	Fig.4
		–	7	15	–	18	–	22	ns	4.5	
		–	6	13	–	15	–	19	ns	6.0	
t_W	clock pulse width HIGH or LOW	80	19	–	100	–	120	–	ns	2.0	Fig.4
		16	7	–	20	–	24	–	ns	4.5	
		14	6	–	17	–	20	–	ns	6.0	
t_{su}	set-up time D_n to CP_n	60	8	–	75	–	90	–	ns	2.0	Fig.4
		12	3	–	15	–	18	–	ns	4.5	
		10	3	–	13	–	15	–	ns	6.0	
t_{su}	set-up time REC_n to CP_n	75	22	–	90	–	110	–	ns	2.0	Fig.5
		15	8	–	18	–	22	–	ns	4.5	
		13	7	–	15	–	19	–	ns	6.0	
t_h	hold time D_n to CP_n	25	−3	–	30	–	35	–	ns	2.0	Fig.4
		5	−1	–	6	–	7	–	ns	4.5	
		4	−1	–	5	–	6	–	ns	6.0	
t_h	hold time REC_n to CP_n	10	−8	–	10	–	15	–	ns	2.0	Fig.5
		2	−3	–	2	–	3	–	ns	4.5	
		2	−3	–	2	–	3	–	ns	6.0	
f_{max}	maximum clock pulse frequency	6	26	–	4.8	–	4	–	MHz	2.0	Fig.4 (note 1)
		30	78	–	24	–	20	–	MHz	4.5	
		35	93	–	28	–	23	–	MHz	6.0	

Note to 74HC AC Characteristics

1. The maximum power dissipation has to be observed. See power dissipation information.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
CP_n	0.7
REC_n	0.4
D_n	0.5

Notes to HCT DC Characteristics

1. The RS input has CMOS input switching levels.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)								TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay time CP to Q_n	–	24	42	–	52	–	63	ns	4.5	Fig.4
t_{THL}/t_{TLH}	output transmission time	–	7	15	–	18	–	22	ns	4.5	Fig.4
t_W	clock pulse width HIGH or LOW	16	7	–	20	–	24	–	ns	4.5	Fig.4
t_{su}	set-up time D_n to CP_n	12	3	–	15	–	18	–	ns	4.5	Fig.4
t_{su}	set-up time REC_n to CP_n	15	6	–	18	–	22	–	ns	2	Fig.5
t_h	hold time D_n to CP_n	5	0	–	6	–	7	–	ns	2	Fig.4
t_h	hold time REC_n to CP_n	2	−3	–	2	–	3	–	ns	4.5	Fig.5
f_{max}	maximum clock pulse frequency	30	80	–	24	–	20	–	MHz	4.5	Fig.4 (note 1)

AC WAVEFORMS

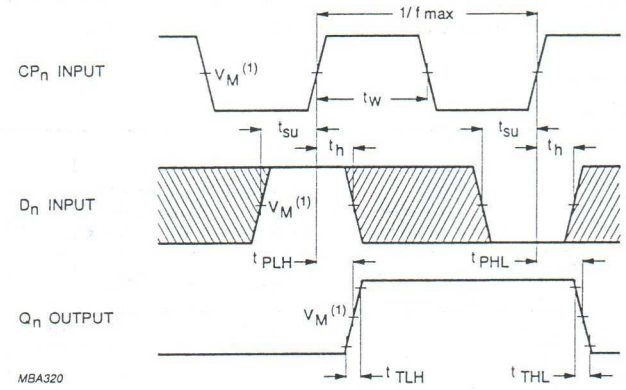


Fig.4 Waveforms showing the clock (CP) and data (D) input to output (Q) propagation delay, set-up, hold and transition times.

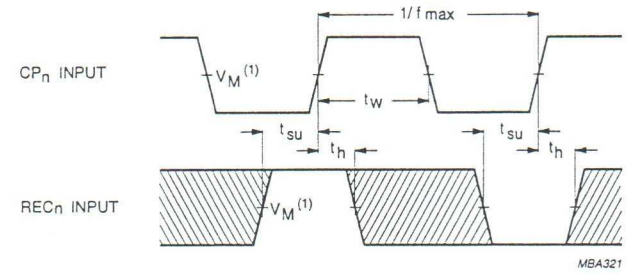


Fig.5 Waveforms showing the clock (CP) to recycle (REC) set-up and hold times.

Note to AC Waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT : V_M = 1.3 V; V_I = GND to 3 V.

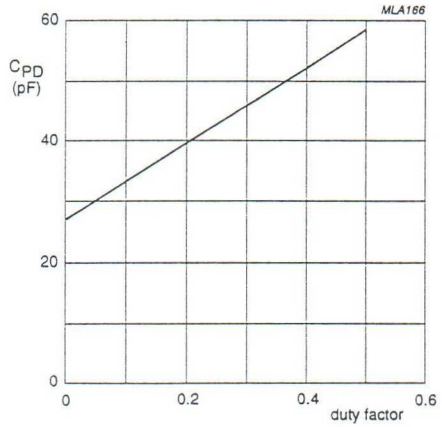


Fig.6 C_{PD} as a function of the duty factor.

POWER DISSIPATION INFORMATION

The power dissipation per register operating at the same frequency is given by:

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$$

f_i = clock input frequency

f_o = data output frequency

C_L = output load capacitance in pF

V_{CC} = power supply voltage in V.

As P_D also depends on the frequency at which the contents of the internal bits are changing, the value of C_{PD} is a function of the duty factor (d_f) being the ration between data and clock frequency, see Fig.6.

Example:

f_i = 12 MHz

f_o = 3 MHz

C_L = 25 pF

V_{CC} = 5 V

d_f = 3/12 = 0.25

C_{PD} = 42.5 pF

$P_D = (42.5 \times 5^2 \times 12) + (25 \times 5^2 \times 3) = 14625\ \mu W$

As the maximum allowable power dissipation in an SO package at T_{amb} = 125 °C is 60 mW, it is allowed to apply 4 registers at the same time under these conditions.

SUPERSEDES DATA OF MARCH 1988

NINE WIDE SCHMITT TRIGGER BUFFER/LINE DRIVER; INVERTING

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9014 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9014 are nine wide Schmitt trigger inverting buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The "9014" is identical to the "9015" but has inverting inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_8	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_8$	data outputs
20	V_{CC}	positive supply voltage

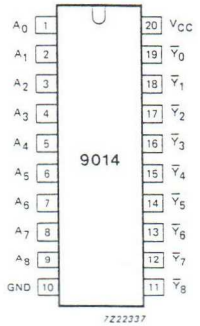


Fig. 1 Pin configuration.

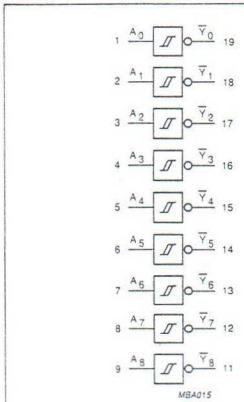


Fig. 2 Logic symbol.

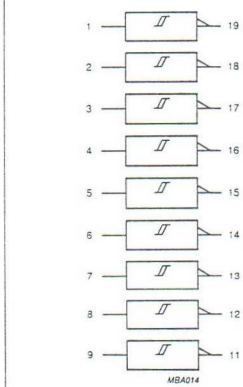


Fig. 3 IEC logic symbol.

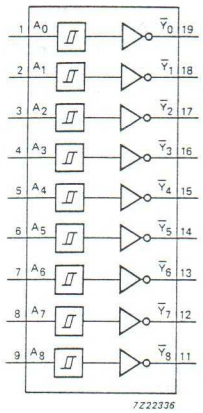


Fig. 4 Functional diagram.

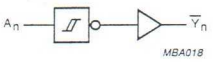


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	$\overline{Y}_n$
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		33 12 10	105 21 18		130 26 22		160 32 27	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		19	32		40		48	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.8

TRANSFER CHARACTERISTIC WAVEFORMS

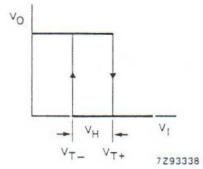


Fig.6 Transfer characteristic.

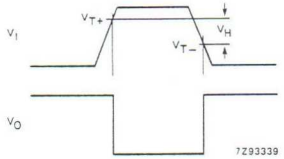


Fig.7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

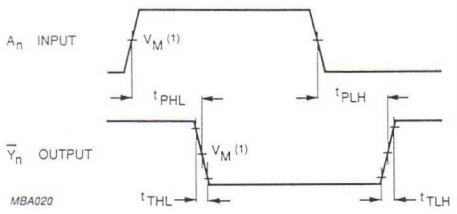


Fig.8 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

SUPERSEDES DATA OF MARCH 1988

NINE WIDE SCHMITT TRIGGER BUFFER/LINE DRIVER

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9015 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9015 are nine wide Schmitt trigger buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The "9015" is identical to the "9014" but has non-inverting inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_8	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_8	data outputs
20	V_{CC}	positive supply voltage

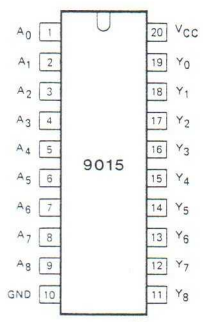


Fig.1 Pin configuration.

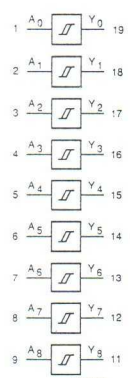


Fig.2 Logic symbol.

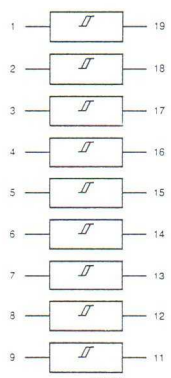


Fig.3 IEC logic symbol.

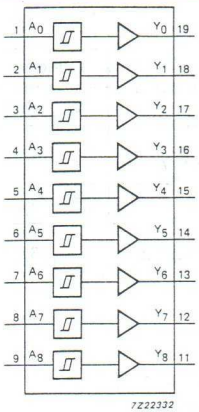


Fig.4 Functional diagram.

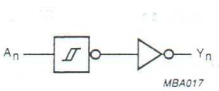


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	Y_n
L	L
H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig.6

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		33 12 10	105 21 18		130 26 22		160 32 27	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74 HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74 HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		18	32		40		48	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.8

TRANSFER CHARACTERISTIC WAVEFORMS

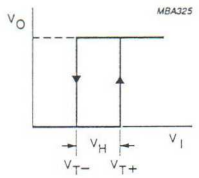


Fig.6 Transfer characteristic.

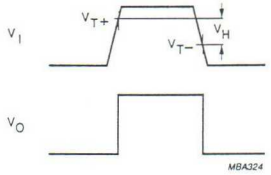


Fig.7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H.

AC WAVEFORMS

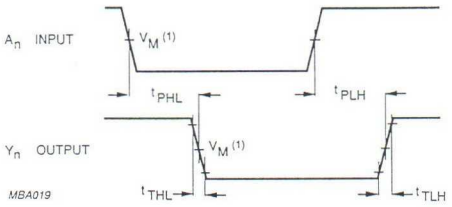


Fig.8 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PLL with bandgap controlled VCO 74HCT9046A

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 5.5 V
- Choice of two phase comparators:
  - EXCLUSIVE-OR (PC1)
  - edge-triggered JK flip-flop (PC2)
- No dead zone of PC2.
- Charge pump output on PC2, whose current is set by an external resistor R_b
- Centre frequency tolerance ±10%
- Excellent VCO linearity
- Low frequency drift with supply voltage and temperature variations
- On chip bandgap reference
- Glitch free operation of VCO, even at very low frequencies
- Inhibit control for ON/OFF keying and for low standby power consumption
- Operation power supply voltage range 4.5 to 5.5 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- ICC category: MSI

APPLICATIONS

- FM modulation and demodulation where a small centre frequency tolerance is essential
- Frequency synthesis and multiplication where a low jitter is required (e.g. Video picture-in-picture)
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

GENERAL DESCRIPTION

The 74HCT9046A is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 6$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
f_o	VCO centre frequency	C_1 = 40 pF R_1 = 4.3 kΩ V_{CC} = 5 V	16	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	pF

Notes

(1) C_PD is used to determine the dynamic power dissipation (P_D in μW)
$P_D = C_PD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

(2) Applies to the phase comparator section only (inhibit = HIGH). For power dissipation of the VCO and demodulator sections see Figs 24 and 25.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HCT9046AP	16	DIL	plastic	DIL16/SOT38Z
74HCT9046AT	16	SO	plastic	SO16/SOT109A

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground (0 V) (phase comparators)
$PC1_{OUT}/PCP_{OUT}$	2	phase comparator 1 output/phase comparator pulse output
$COMP_{IN}$	3	comparator input
VCO_{OUT}	4	VCO output
INH	5	inhibit input
$C1_A$	6	capacitor C1 connection A
$C1_B$	7	capacitor C1 connection B
GND	8	ground (0 V) (VCO)
VCO_{IN}	9	VCO input
DEM_{OUT}	10	demodulator output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
$PC2_{OUT}$	13	phase comparator 2 output (current source adjustable with R_b)
SIG_{IN}	14	signal input
R_b	15	bias resistor (Rb) connection
V_{CC}	16	positive supply voltage

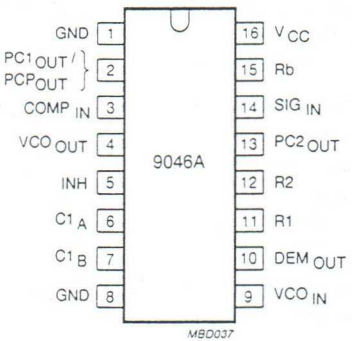


Fig.1 Pin configuration.

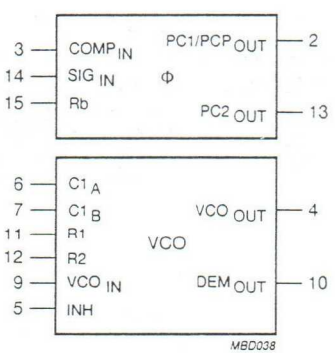


Fig.2 Logic symbol.

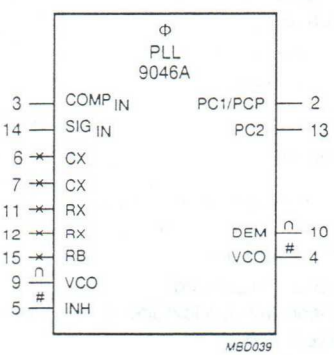


Fig.3 IEC Logic symbol.

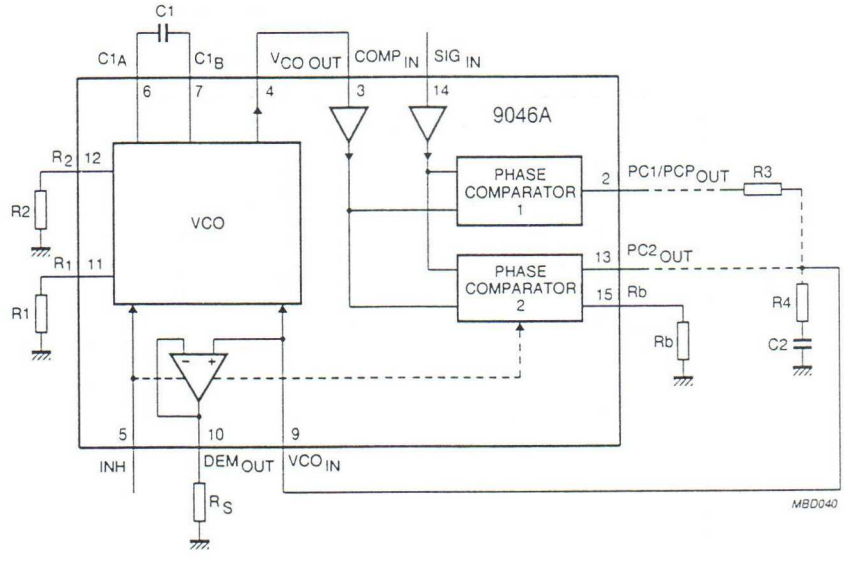


Fig.4 Functional diagram.

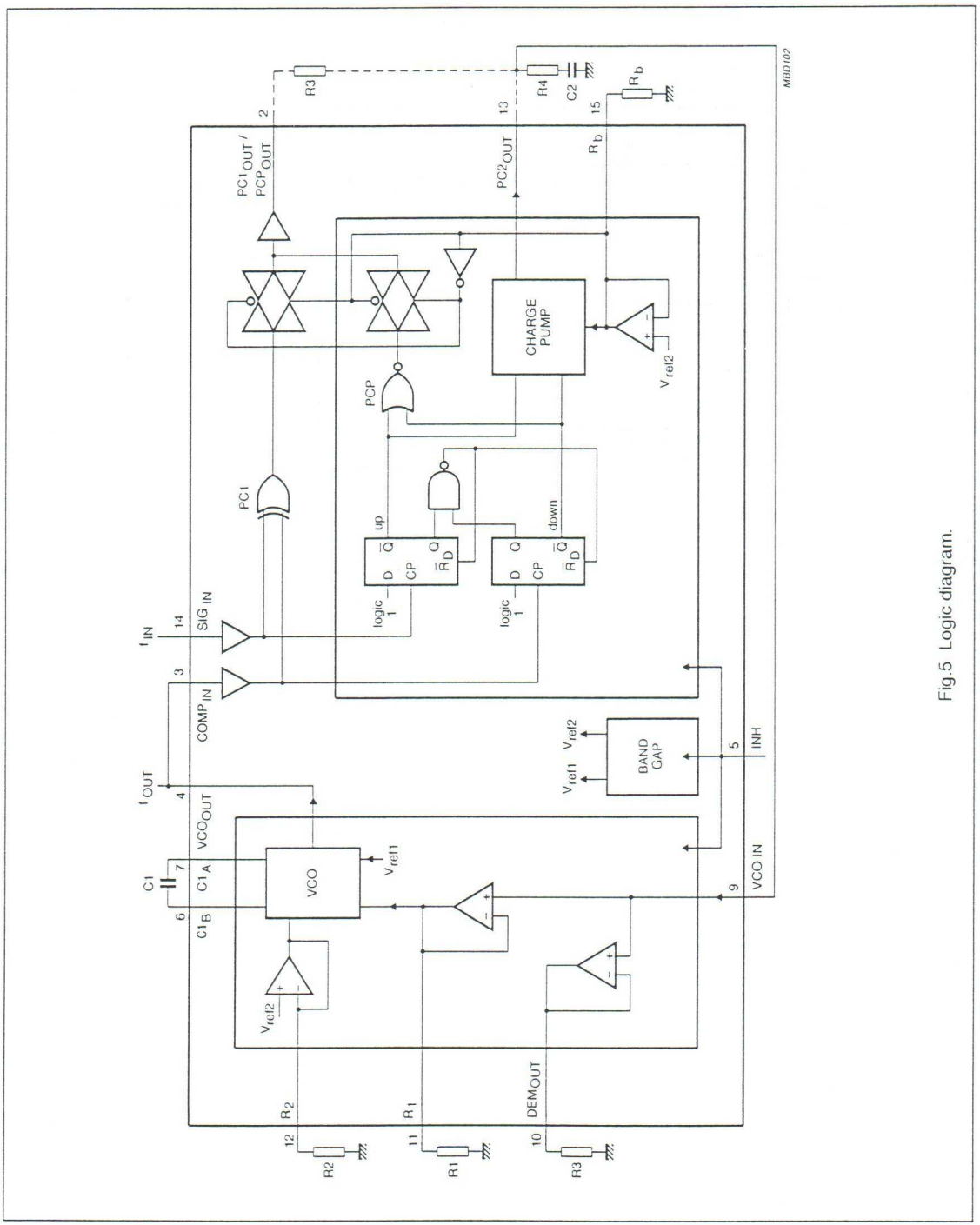


Fig.5 Logic diagram.

FUNCTIONAL DESCRIPTION

The 74HCT9046A is a phase-locked-loop circuit that comprises a linear voltage-controlled-oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input (see Fig.4). The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the '9046A' forms a second-order loop PLL.

The principle of this phase-locked-loop is based on the familiar HCT4046A. However extra features are built in, allowing very high performance phase-locked-loop applications. This is done, at the expense of PC3, which is skipped in this HCT9046A. The PC2 is equipped with a current source output stage here. Further a bandgap is applied for all internal references, allowing a small centre frequency tolerance. The details are summed up in the next section called: 'Differences which respect to the familiar HCT4046A'. If one is familiar with the HCT4046A already, it will do to read this section only.

DIFFERENCES WITH RESPECT TO THE FAMILIAR HCT4046A

- A centre frequency tolerance of maximum ± 10%
- The on board bandgap sets the internal references resulting in a minimal frequency shift at supply voltage variations and temperature variations
- The value of the frequency offset is determined by an internal reference voltage of 2.5 V instead of V_{CC} - 0.7 V. In this way the offset frequency will not shift over the supply voltage range.
- A current switch charge pump output on PC2 allows a virtually ideal performance of PC2. The gain of PC2 is independent of the voltage across the low pass filter. Further a passive low pass filter in the loop achieves an active performance now. The influence of the parasitic capacitance of the PC2 output plays no role here, resulting in a true correspondence of the output correction pulse and the phase difference even up to phase differences as small as a few nanoseconds. Because of its linear peerformance without deadzone, higher impedance values for the filter, hence lower C-values, can now be chosen. Correct operation will not be inflluenced by parasitic capacitances as in the instance with voltage source output of the 4046.
- No PC3 on pin 15 but instead a resistor connected to GND, which sets the load/unload currents of the charge pump (PC2).
- Extra GND pin at pin 1 to allow an excellent FM demodulator performance even at 10 MHz and higher.
- Combined function of pin 2. If pin 15 is tied to V_{CC} (No bias resistor R_b) pin 2 has its familiar function viz. output of PC1. If at pin 15 a resistor (R_b) is connected to GND it is assumed that PC2 has been chosen as phase comparator. Connection of R_b is sensed by internal circuitry and this changes the function of pin 2 into a lock detect output (PCP_{out}) with the same characteristics as PCP_{out} of pin 1 of the well known 74HCT4046A.
- The inhibit function differs. For the HCT4046A a HIGH level at the inhibit input (INH) disables the VCO and demodulator, while a LOW level turns both on. For the 74HCT9046A a HIGH level on the inhibit input disables the whole circuit to allow quiescent supply current testing.

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required (see Fig.5).
The high input impedance of the VCO simplifies the design of the low-pass filters by giving the

designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). The DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from pin 10 to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$3K\sqrt{V_{DEMOUT}} = \frac{V_{CC}}{\pi}(F_{SIGIN} - F_{COMPIN})$$

where $F\Theta V_{PCIN}$ is the demodulator output at pin 10;
$V_{PCIN} = V_{PC1OUT}$ (via low-pass). The phase comparator gain is:

$$Kp = \frac{V_{CC}}{\pi}(V/r)$$

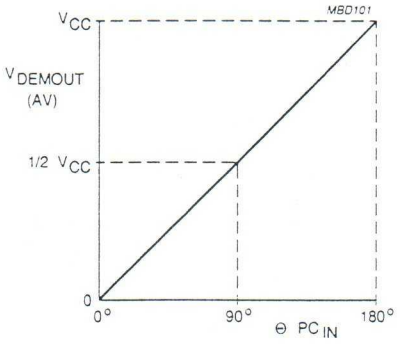
The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig.6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig.7. This figure also shows the actual waveforms across the VCO capacitor at pins 6 and 7 (V_{C1a} and V_{C1b}) to show the relation between these ramps and the VCO_{OUT} voltage.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2F_L$) is defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behaviour of this type of phase comparator is that it may lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{in} and $COMP_{in}$ are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage with sink and source transistors acting as current sources, henceforth called charge pump output of PC2. The circuit functions as an up-down counter, (Fig.5. where SIG_{in} causes an up-count and $COMP_{in}$ a down count. The current switch charge pump output allows a virtually ideal performance of PC2, due to appliance of some pulse overlap of the up and down signals. See Fig.8a.



$$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi} (\Theta_{SIGIN} - \Theta_{COMPIN})$$

$$\Theta_{PCIN} = (\Theta_{SIGIN} - \Theta_{COMPIN}).$$

Fig.6 Phase comparator 1: average output voltage as a function of input phase difference.

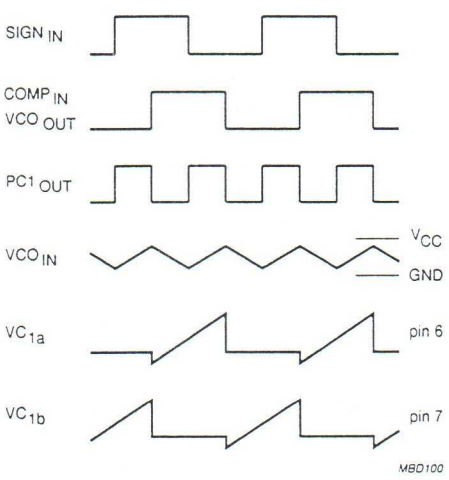


Fig.7 Typical waveforms for PLL using phase comparator 1, loop-locked at f_0.

The pump current I_p is independent from the supply voltage and is set by the internal bandgap reference of 2.5 V.

$$I_p = 17 \times \frac{2.5}{R_b} (A)$$

R_b is the external bias resistor tied to pin 15.

The current and voltage transfer function of PC2 are shown in Fig.9.

The phase comparator gain is:

$$K_p = \frac{|I_p|}{2\pi} (A/r)$$

Typical waveforms for the PC2 loop locked at f_0 are shown in Fig.10.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the up output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (Θ_{PCIN}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the down or sink driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the source output driver is held "ON" for most of the input signal cycle time and for the remainder of the cycle time both drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the sink driver that is held "ON" for most of the cycle. Subsequently the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition the signal at the phase comparator pulse output (PCP_{OUT}) has a minimum output pulse width equal to the overlap time, so can be used for indicating a locked condition.

Thus for PC2 no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both output drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjust, via PC2, to its lowest frequency.

By using current sources as charge pump output on PC2, the dead zone or backlash time could be reduced to zero! Also, the pulse widening due to the parasitic output capacitance plays no role here. This enables a linear transfer function, even in the vicinity of the zero crossing. The differences between a current switch charge pump and voltage switch charge pump are shown in Fig.11.

The design of the low-pass filter is somewhat different when using current sources. The external resistor R3 is no longer present when using PC2 as phase comparator. The current source is set by R_b. A simple capacitor behaves as an ideal integrator now, because the capacitor is charged by a constant current. The transfer function of the voltage switch charge pump may be used. In fact it is even more valid, because the transfer function is no longer restricted for small changes only. Further the current is independent from both the supply voltage and the voltage across the filter. For one that is familiar with the low-pass filter design of the '4046A a relation may show how R_b relates with a fictive series resistance, called R'_3.

This relation can be derived by assuming first that a voltage controlled switch PC2 of the 4046 is connected to the filter capacitance C2 via this fictive R'_3 (see Fig 8b). Then during tthe PC2 output pulse the charge current equals

$$|I_p| = \frac{V_{CC} V_{C20}}{R'_3}.$$

With the initial voltage $VC2_0$ at

$1/2\ V_{CC} = 2.5\ V$, $|I_p| = \frac{2.5}{R'_3}$.

As shown before the charge current of the current switch of the 9046 is

$$|I_p| = 17 \times \frac{2.5}{R_b}.$$

Hence:

$$R'_3 = \frac{R_b}{17} (\Omega)$$

Using this equivalent resistance R'_3 for the filter design the voltage can now be expressed as a transfer function of PC2; assuming ripple ($f_r = f_i$) is suppressed, as:

$$K_{PC2OUT} = \frac{5}{4\pi} ((v/r)$$

Again this illustrates the supply voltage independent behaviour of PC2.

Examples of PC2 combined with a passive filter are shown in Figs 12 and 13. Fig.12 shows that PC2 with only a C2 filter behaves as a high-gain filter. For stability the damped version of Fig.13 with series resistance R4 is preferred.

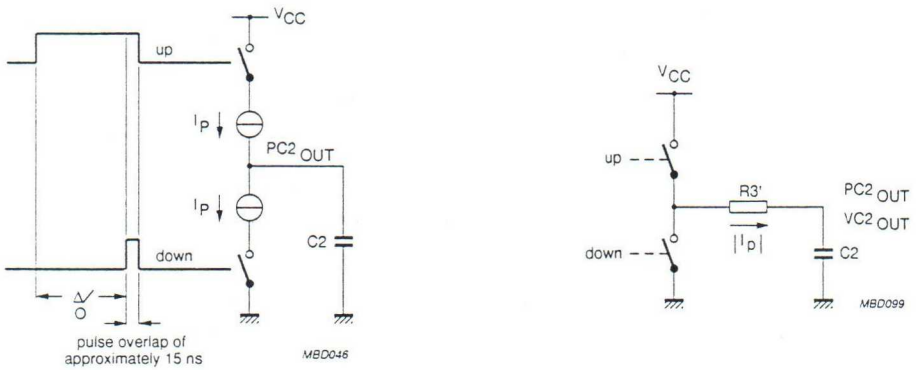
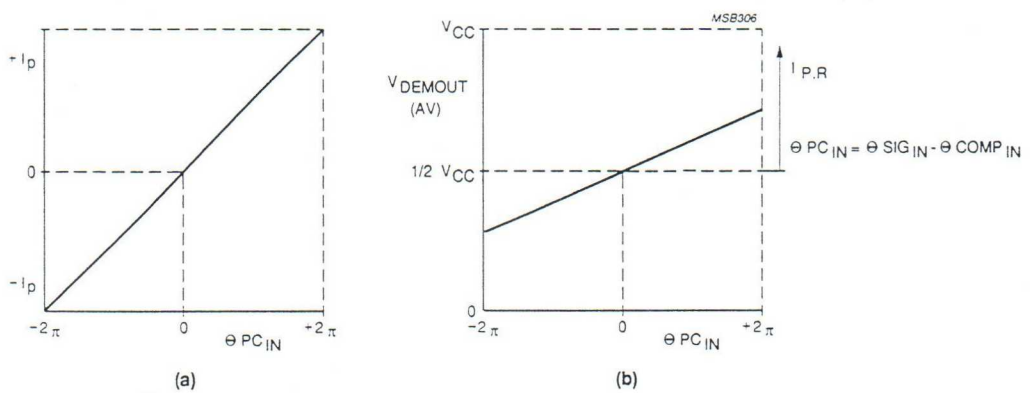


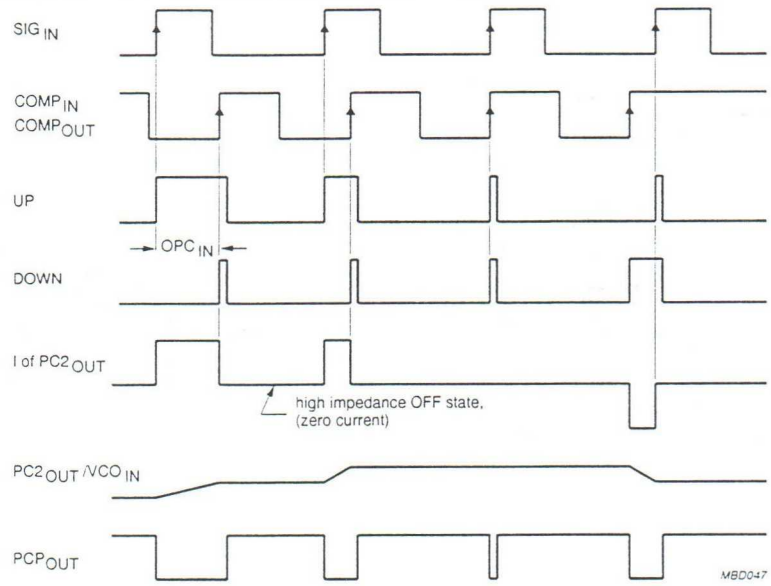
Fig.8 (a) The current switch charge pump output of PC2. At every $\Delta\Theta$, even at zero $\Delta\Theta$ both switches are closed simultaneously for a short period (typically 15 ns). (b) Comparable voltage-controlled switch.



a) pump current $\frac{|I_p|}{2\pi}\Theta PC_{IN}$.

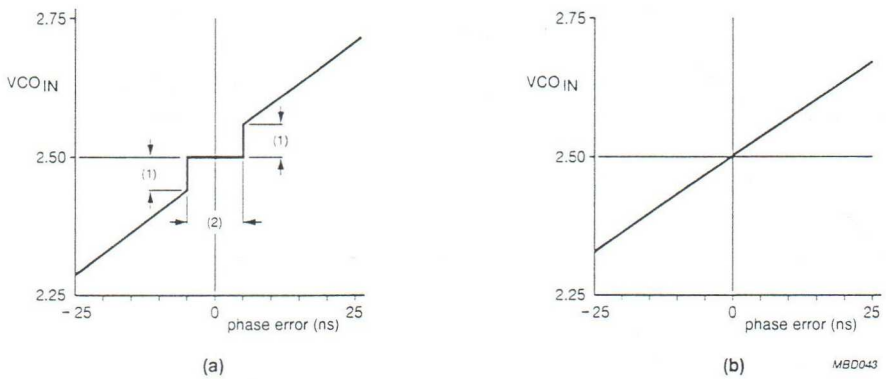
b) $V_{DEMOUT} = VPC2_{OUT} = \frac{5}{4\pi}.\Theta PC_{IN}$.

Fig.9 Phase comparator 2. Two kinds of transfer functions may be regarded: the current transfer (a) and the voltage transfer (b). The voltage transfer can be observed at $PC2_{OUT}$ by connecting first a resistance R = 10 kΩ between $PC2_{OUT}$ and $V_{CC}/2$.



Note the pulse overlap of the up and down signals (typically 15 ns)

Fig.10 Timing diagram for PC2.



(1) due to parasitic capacitance on PC2 output.

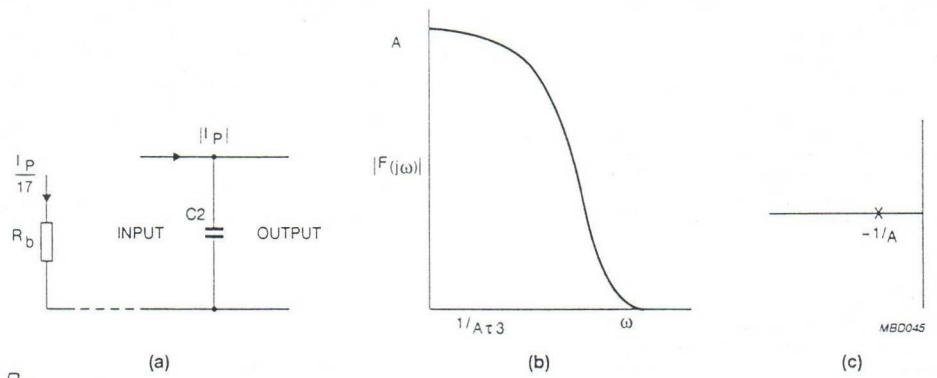
(2) backlash time (dead zone).

(a) response with traditional voltage-switch charge-pump PC2 output (4046).

(b) response with current-switch charge-pump PC2 output as applied in the HCT9046A

Fig.11 The response of a locked-loop in the vicinity of the zero crossing of the phase error.

LOOP FILTER COMPONENT SELECTION



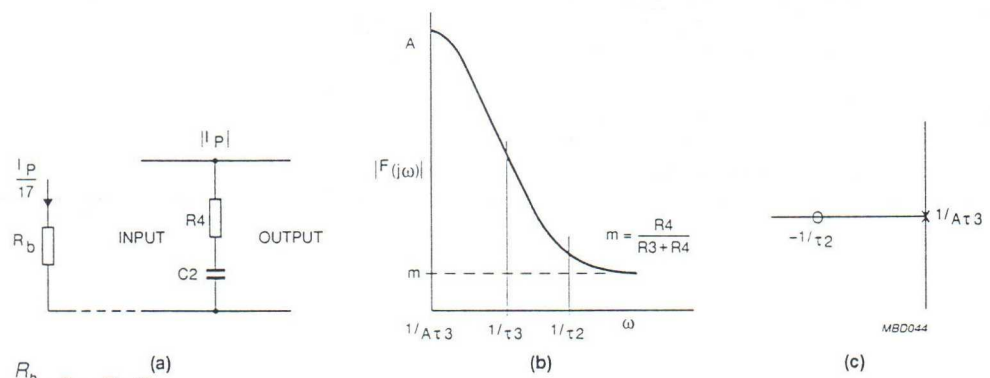
(a) (b) (c)

(a) $\tau_1 = \frac{R_b}{17} \times C_2 = R'_3$

(b) amplitude characteristic, $F(j\omega) = \frac{1}{1/A + j\omega\tau_1} \approx \frac{1}{j\omega\tau_1}$

(c) pole zero diagram

Fig.12 Simple loop filter for PC2 without damping.



(a) (b) (c)

(a) $\tau_1 = \frac{R_b}{17} \times C_2 = R'_3.C_2$

$\tau_2 = R_4 \times C_2$

(b) amplitude characteristic. $F(j\omega) = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1}$

(c) pole zero diagram

A = DC gain limit, due to leakage.

Fig.13 Simple loop filter for PC2 with damping.

RECOMMENDED OPERATING CONDITIONS FOR 74HCT

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage		4.5	5.0	5.5	V
V_I	DC input voltage range		0	–	V_{CC}	V
V_O	DC output voltage range		0	–	V_{CC}	V
T_{amb}	operating ambient temperature range	see DC and AC Characteristics	−40	–	+85	°C
T_{amb}	operating ambient temperature range		−40	–	+125	°C
t_r, t_f	input rise and fall times (pin 5)	V_{CC} = 4.5 V	–	6.0	500	ns

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		−0.5	+7	V
$\pm I_{IK}$	DC input diode current	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	20	mA
$\pm I_{OK}$	DC output diode current	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	–	20	mA
$\pm I_O$	DC output source or sink current	for -0.5 V $< V_O < V_{CC} + 0.5$ V	–	25	mA
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		–	50	mA
T_{stg}	storage temperature range		−65	+150	°C
P_{tot}	power dissipation per package plastic DIL	for temperature range: −40 to +125 °C above +70 °C: derate linearly with 12 mW/K	–	750	mW
	plastic mini-pack (SO)	above +70 °C: derate linearly with 8 mW/K	–	500	mW

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
I_{CC}	quiescent supply current (disabled)	–	–	8.0	–	80.0	–	160.0	μA	5.5	pin 5 at V_{CC}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V	–	100	360	–	450	–	490	μA	4.5 to 5.5	other inputs at V_{CC} or GND.

Note

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the Unit Load Coefficient Table.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4	–	–	–	–	–	V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$	–	2.1	1.35	–	–	–	–	V	4.5		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98	4.32	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −4.0 mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}	–	0.15	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = −4.0 mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$	–	–	30	–	38	–	45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$	–	–	0.5	–	5.0	–	10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$	–	250	–	–	–	–	–	kΩ	4.5	V_I at self-bias operating point; ΔV_I = 0.5 V; see Figs 14, 15, 16	
R_b	resistor range	25	–	250	–	–	–	–	kΩ	4.5		
$\pm I_p$	charge pump current $PC2_{OUT}$	0.53	1.06	2.12	–	–	–	–	mA	4.5	R_3 = 40 kΩ	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{IH}	DC coupled HIGH level input voltage INH	2.0	1.6	–	2.0	–	2.0	–	V	4.5 to 5.5		
V_{IL}	DC coupled LOW level input voltage INH	–	1.2	0.8	–	0.8	–	0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT},	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = −20 μA
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = −4.0 mA
V_{OL}	LOW level output voltage VCO_{OUT}	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = +20 μA
V_{OL}	LOW level output voltage VCO_{OUT}	–	0.15	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = +4.0 mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$	–	–	0.40	–	0.47	–	0.54	V	4.5	V_{IH} or V_{IL}	I_O = +4.0 mA
$\pm I_I$	input leakage current INH, VCO_{IN}	3	–	0.1	–	1.0	–	1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3	–	300	–	–	–	–	kΩ	4.5		
R2	resistor range	3	–	300	–	–	–	–	kΩ	4.5		
C1	Capacitor range	40	–	no limit	–	–	–	–	pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1	–	3.4 3.9 4.4	–	–	–	–	V	4.5 5.0 5.5		over the range specified for R1

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
R_S	resistor range	50	–	300	–	–	–	–	kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}	–	±20	–	–	–	–	–	mV	4.5	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; values taken over R_S range, see Fig.17
R_D	dynamic output resistance at PC_{DEMOUT}	–	25	–	–	–	–	–	Ω	4.5	V_{DEMOUT} = 1/2 V_{CC}

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)								TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}	–	23	40	–	50	–	60	ns	4.5	Fig.18
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}	–	35	68	–	85	–	102	ns	4.5	Fig.18
t_{PZH}/t_{PZL}	3–state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	–	30	56	–	70	–	84	ns	4.5	Fig.19
t_{PHZ}/t_{PLZ}	3–state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	–	36	65	–	81	–	98	ns	4.5	Fig.19
t_{THL}/t_{TLH}	output transition time	–	7	15	–	19	–	22	ns	4.5	Fig.18
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at $SIGN_{IN}$ or $COMP_{IN}$	–	15	–	–	–	–	–	mV	4.5	f_i = 1 MHz

AC CHARACTERISTICS FOR 74HCT

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)								TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
$\Delta f/T$	frequency stability with temperature change	–	–	–	0.06	–	–	–	%/K	4.5	V_{VCOIN} = 1/2 V_{CC}; recommended range: R1 = 10 kΩ R2 = 10 kΩ C1 = 1 nF see Fig.20
Δf_{VCO}	centre frequency tolerance	−10	–	+10	–	–	–	–	%	5.0	R1 = 10 kΩ; R2 = 10 kΩ C1 = 1 nF V_{VCOIN} = 3.9 V
f_o	VCO centre frequency (duty factor = 50%)	11.0	15.0	–	–	–	–	–	MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 4.3 kΩ R2 = ∞ C1 = 40 pF see Fig.21
Δf_{VCO}	VCO frequency linearity	–	0.4	–	–	–	–	–	%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pFsee Figs 22, 23
δVCO	duty factor at VCO_{OUT}	–	50	–	–	–	–	–	%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

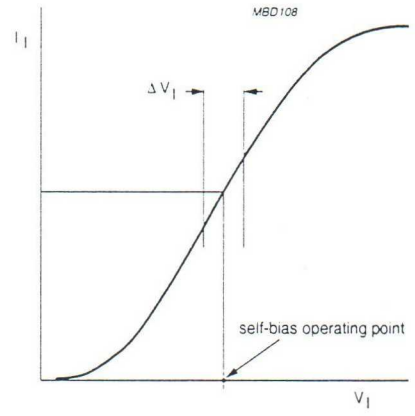


Fig.14 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

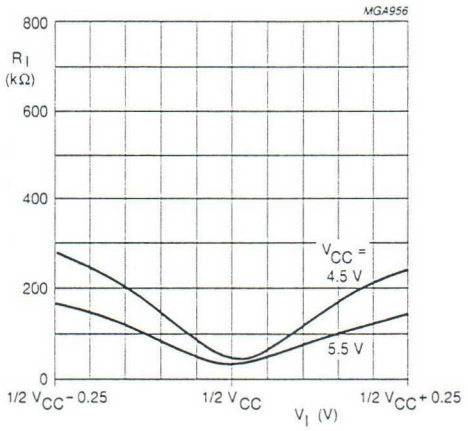


Fig.15 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

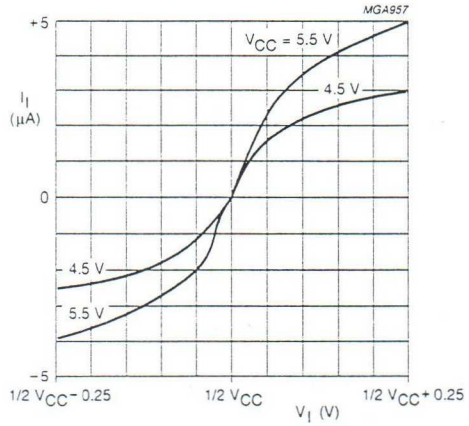


Fig.16 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

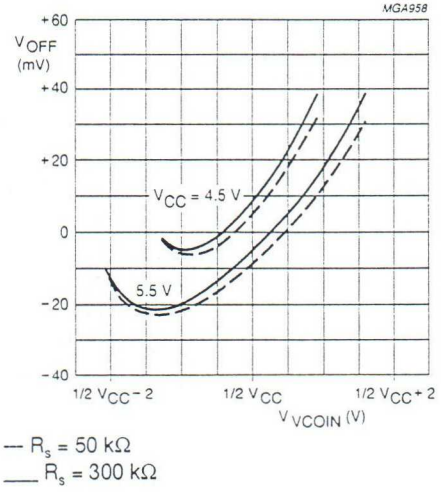


Fig.17 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

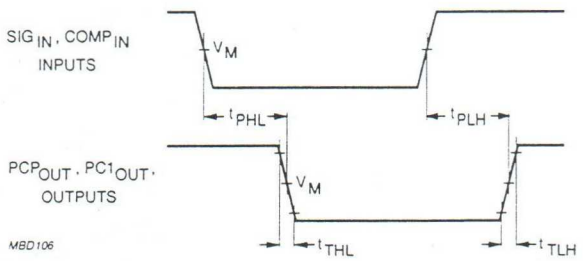


Fig.18 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$) propagation delays and the output transition times.

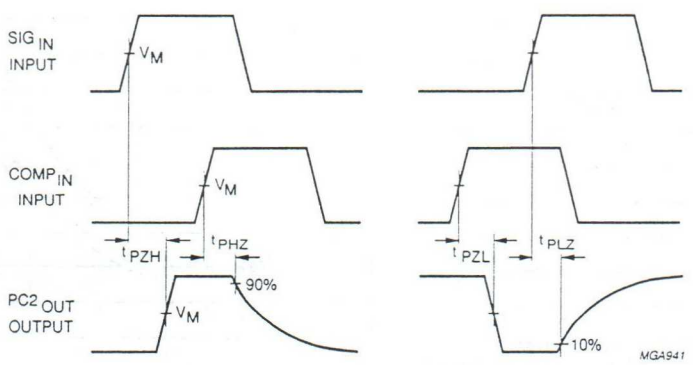
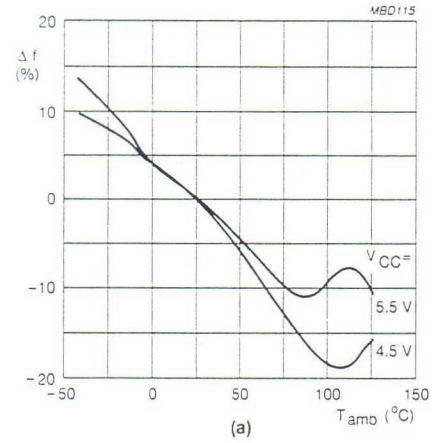


Fig.19 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.



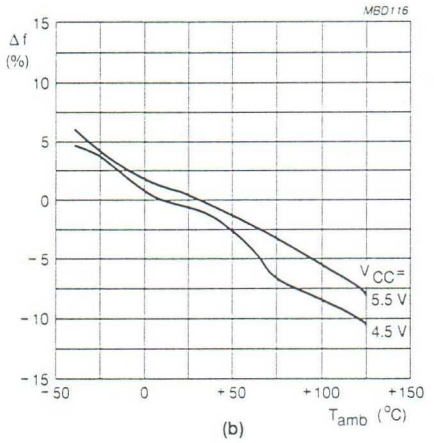
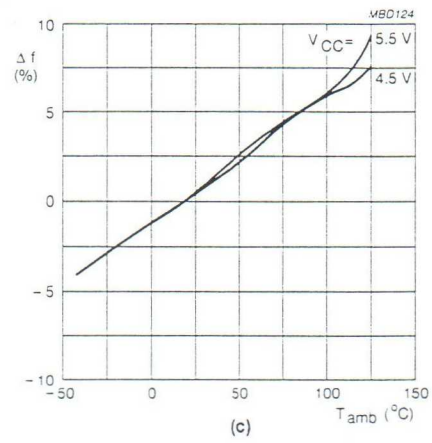


Fig.20 a-b Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.



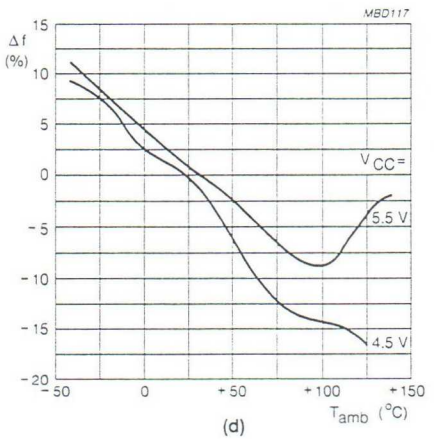
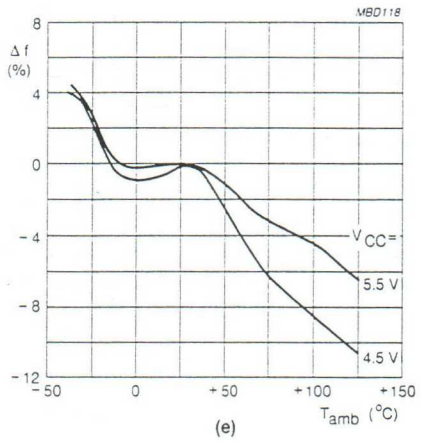


Fig.20 c-d Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.



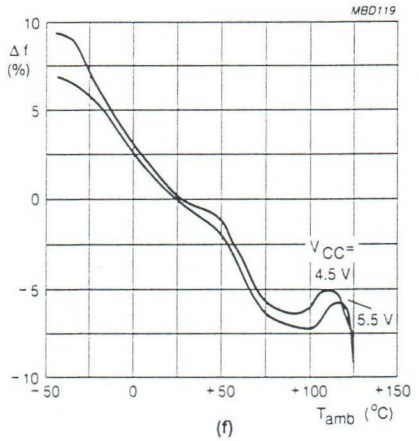
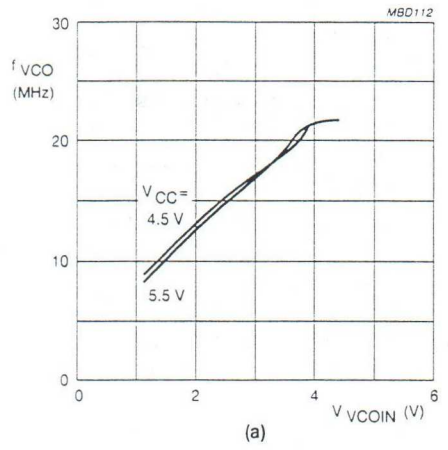
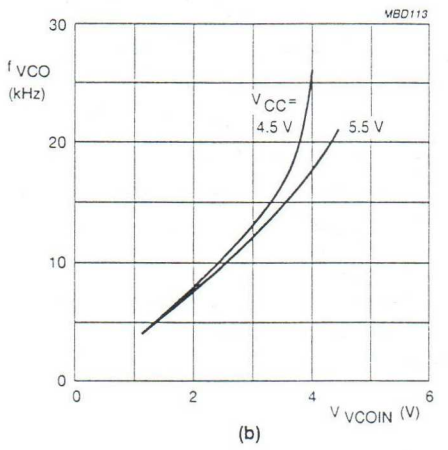


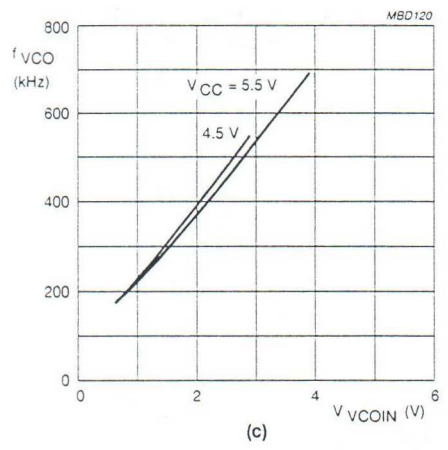
Fig.20 e-f Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

Notes to Fig.20

(a) R1 = 3 kΩ, R2 = ∞, C1 = 100 pF
(b) R1 = 10 kΩ, R2 = ∞, C1 = 100 pF
(c) R1 = 300 kΩ, R2 = ∞, C1 = 100 pF
(d) R1 = ∞, R2 = 3 kΩ, C1 = 100 pF
(e) R1 = ∞, R2 = 10 kΩ, C1 = 100 pF
(f) R1 = ∞, R2 = 300 kΩ, C1 = 100 pF







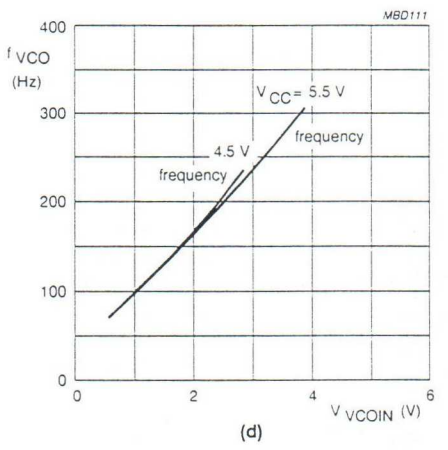
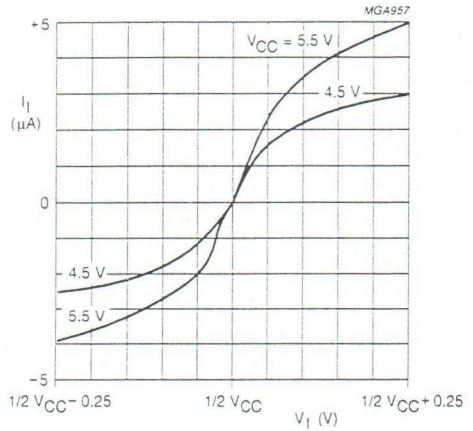


Fig.21 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

Notes to Fig.21

(a) R1 = 3 kΩ, C1 = 39 pF.
(b) R1 = 3 kΩ, C1 = 100 nF.
(c) R_1 = 300 kΩ C1 = 39 pF.
(d) R_1 = 300 kΩ C1 = 100 nF.



$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f_0} \times 100\%$$

Fig.22 Definition of VCO frequency linearity: ΔV = 0.5 V over the V_{CC} range.

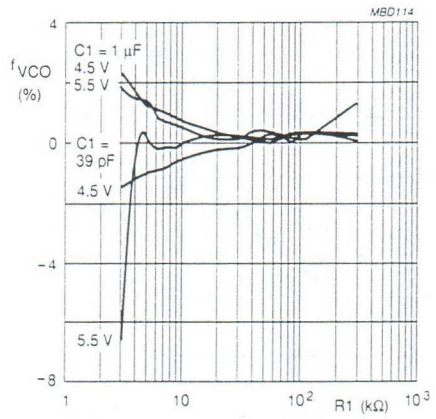
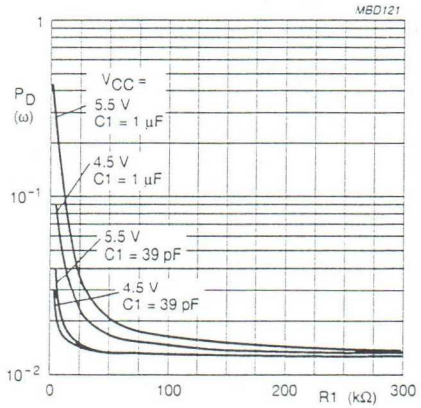
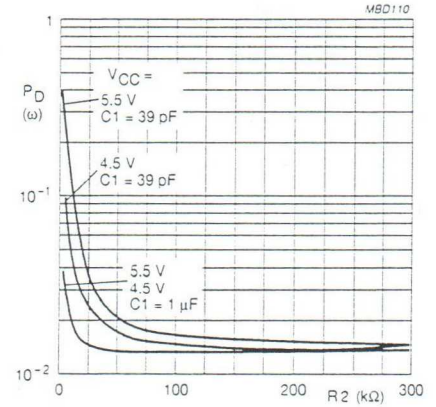


Fig.23 Frequency linearity as a function of R1, C1 and V_{CC}: R2 = ∞. and Delta;V = 0.5 V.



R1 = ∞

Fig.24 Power dissipation as a function of component values.



R2 = ∞

Fig.25 Power dissipation as a function of component values.

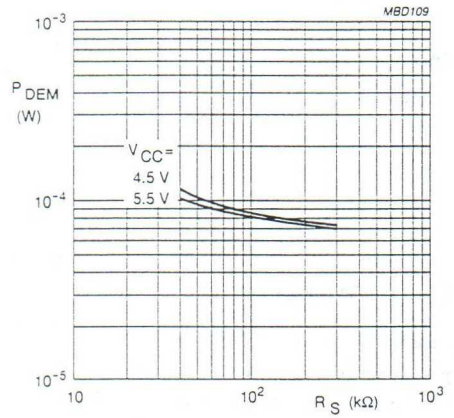


Fig.26 Typical power dissipation.

APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HCT9046A in a phase-lock-loop system.

Values of the selected components should be within the following ranges:

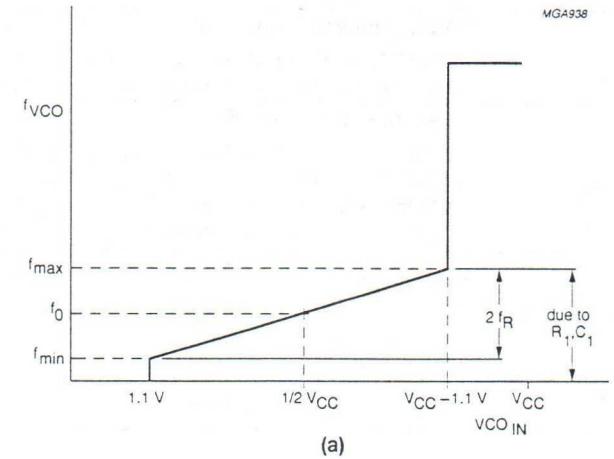
R1 between 3 kΩ and 300 kΩ

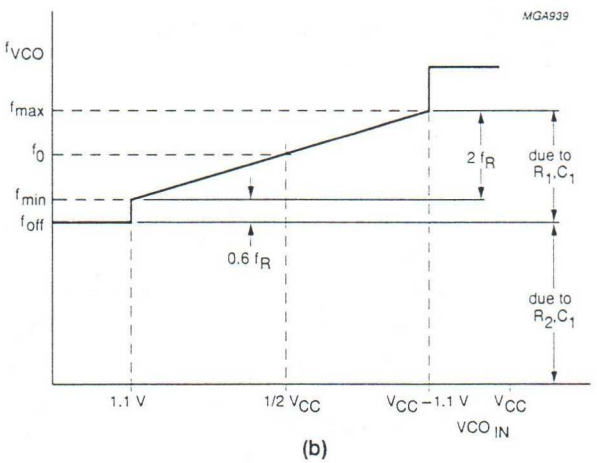
R2 between 3 kΩ and 300 kΩ

R1 + R2 parallel value > 2.7 kΩ

C1 greater than 40 pF

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
VCO frequency **without extra offset**	PC1, PC2	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.27a. (Due to R1, C1 time constant a small offset remains when R2 = ∞).
	PC1	**Selection of R1 and C1** Given f_O, determine the values of R1 and C1 using Fig.29
	PC2	Given f_{max} and f_O determine the values of R1 and C1 using Fig.29; use Fig.31 to obtain $2f_L$ and then use this to calculate f_{min}.





(a) Operating without offset: f_0 = centre frequency: $2f_L$ = frequency lock range.

(b) Operating with offset: f_0 = centre frequency: $2f_L$ = frequency lock range.

Fig.27 Frequency characteristic of VCO.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
VCO frequency **without extra offset**	PC1, PC2	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.27b.
VCO frequency **with extra offset**	PC1, PC2	**Selection of R1, R2 and C1** Given f_O and f_L determine the value of product R1C1 by using Fig.31. Calculate f_{off} from the equation $f_{off} = f_O - 1.6f_L$. Obtain the values of C1 and R2 by using Fig.30. Calculate the value of R1 from the value of C1 and the product R1C1.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_O with Θ_{PCIN} = 90° and V_{VCOIN} = 1/2 V_{CC}.
	PC2	VCO adjusts to f_{offset} with Θ_{PCIN} = −360° and V_{VCOIN} = minimum.

Filter design considerations for PC1 and PC2 of the HCT9046A. Fig.28 shows some examples of passive and active filters to be used with the phase comparators of the HCT9046A. Transfer functions of phase comparators and filters are given in Table 1.

Table 1 Transfer functions of phase comparators and filters.

FIG.28	FILTER TYPE	PHASE COMPARATOR	TRANSFER FUNCTION	NOTE:
(a)	Passive filter without damping	PC1	$F_{j\omega} = \frac{1}{1 + j\omega\tau_1}$;	$K_{PC1} = \frac{V_{CC}}{\pi}$ V/r
(b)	Passive filter with damping	PC1	$F_{j\omega} = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$	$\tau = R_3C_2$ $\tau_2 = R_4C_2$ $\tau_3 = R_4C_3$ $A = 10^5$ = DC gain Ampl.
(c)	Active filter with damping	PC1	$Fj\omega = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$	
(d)	Passive filter with damping	PC2	$Fj\omega = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5$ = limit DC gain	$K_{PC2} = \frac{5}{4\pi}$. V/r $\tau = R_3C_2$ $\tau_2 = R_4C_2$ $\tau_3 = R_4C_3$ $R_3' = Rb/17$
(e)	Active filter with damping	PC2	$Fj\omega = \frac{1 + j\omega\tau_2}{1/4 + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5$ = DC gain ampl	

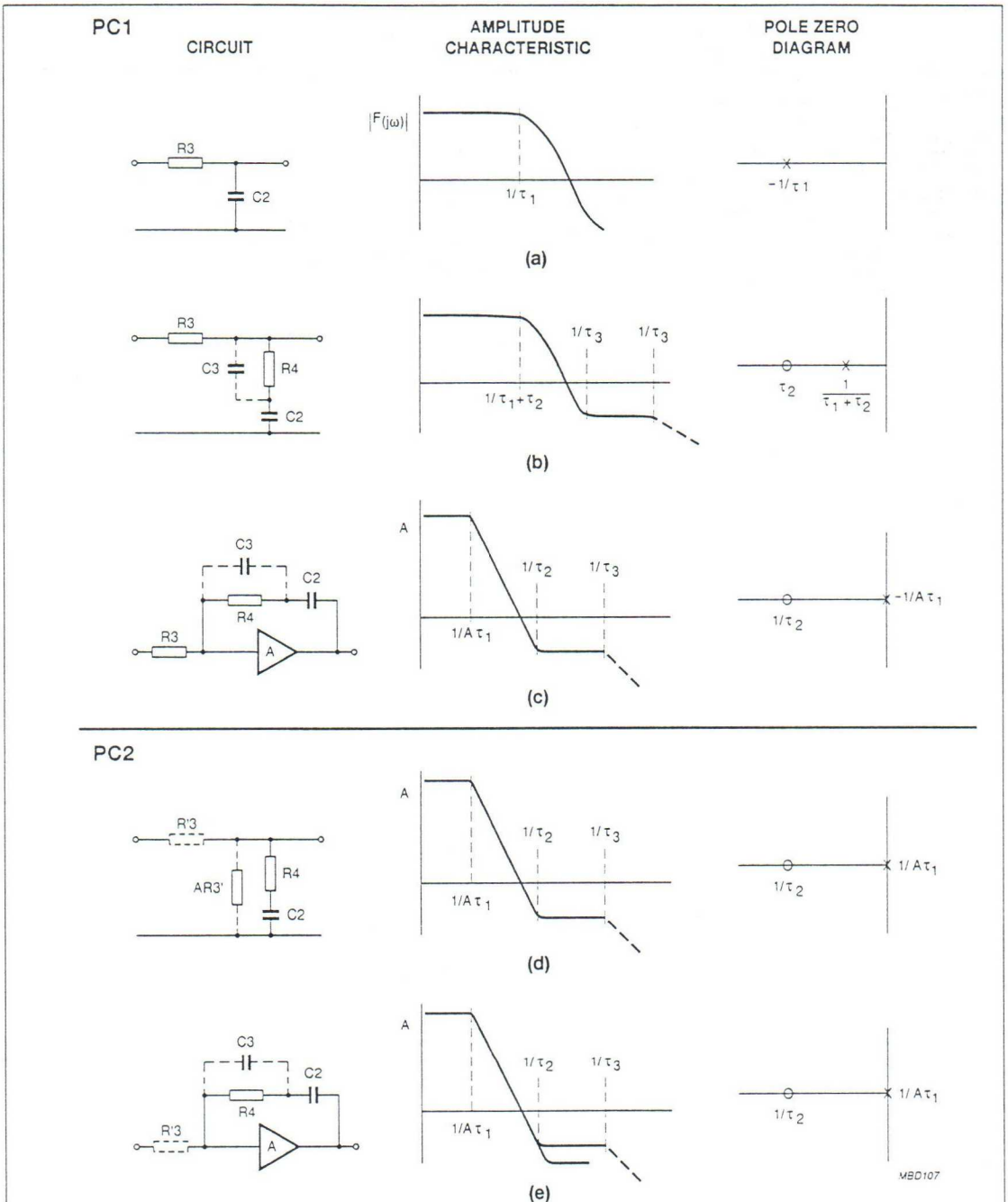


Fig.28 Passive and active filters for HCT9046A.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at $\Theta_{PCIN} = 90°$
	PC2	$f_r = f_i$, small ripple content at $\Theta_{PCIN} = 0°$

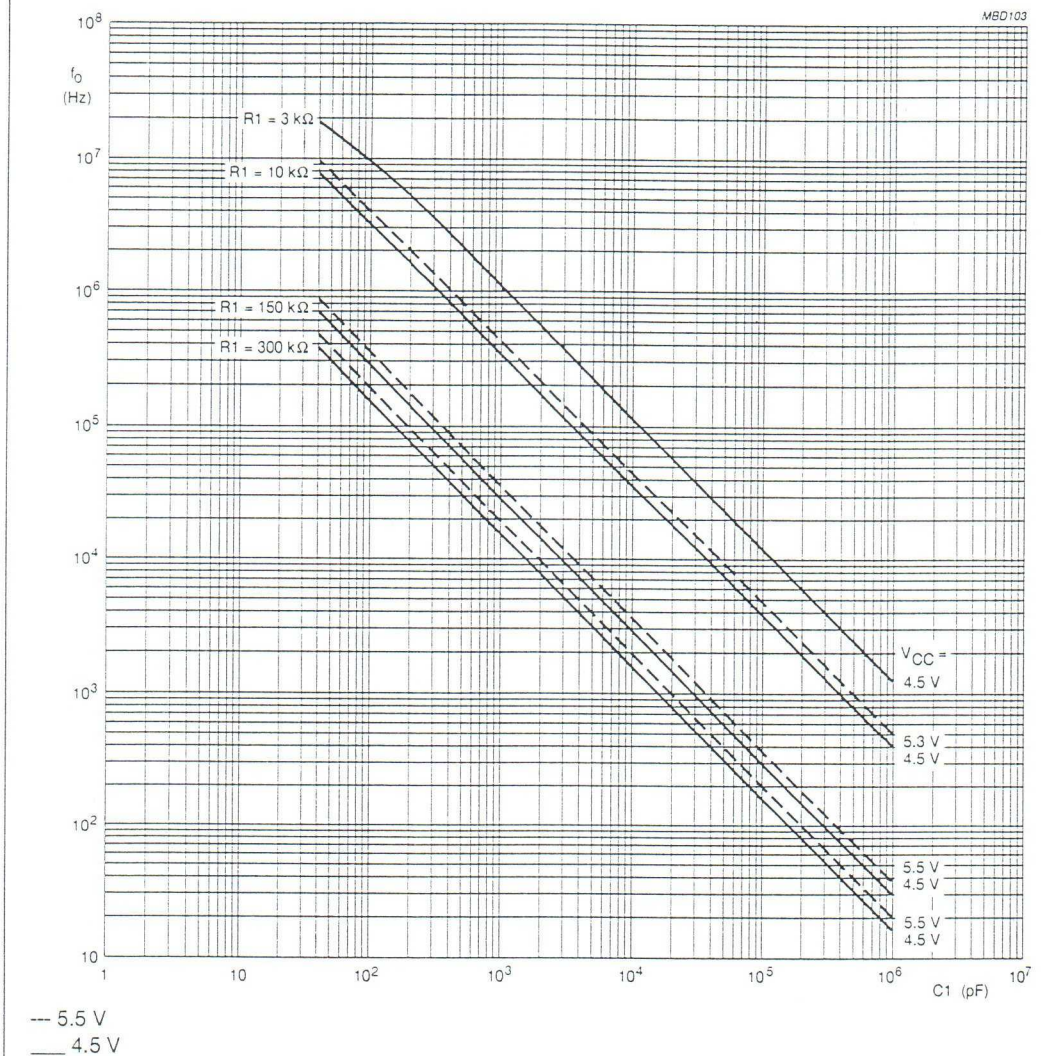


Fig.29 Typical value of VCO centre frequency (f_O) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

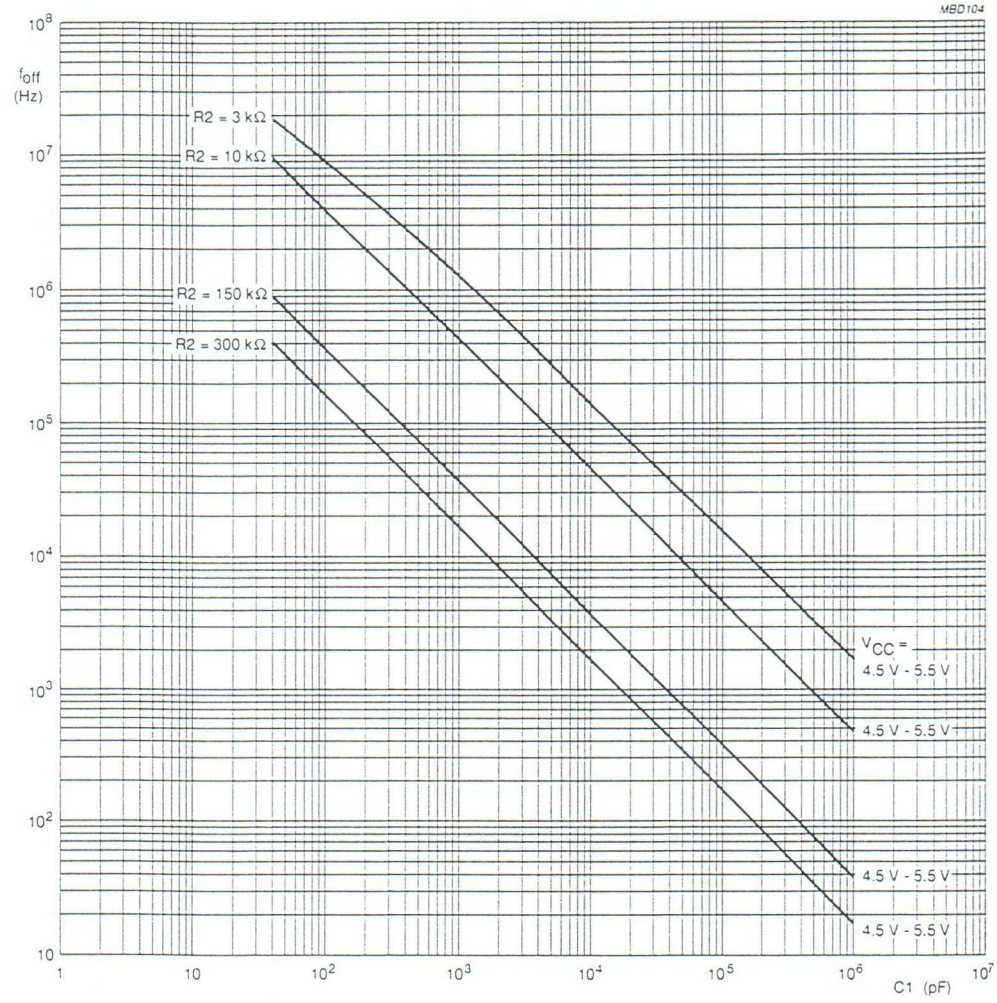
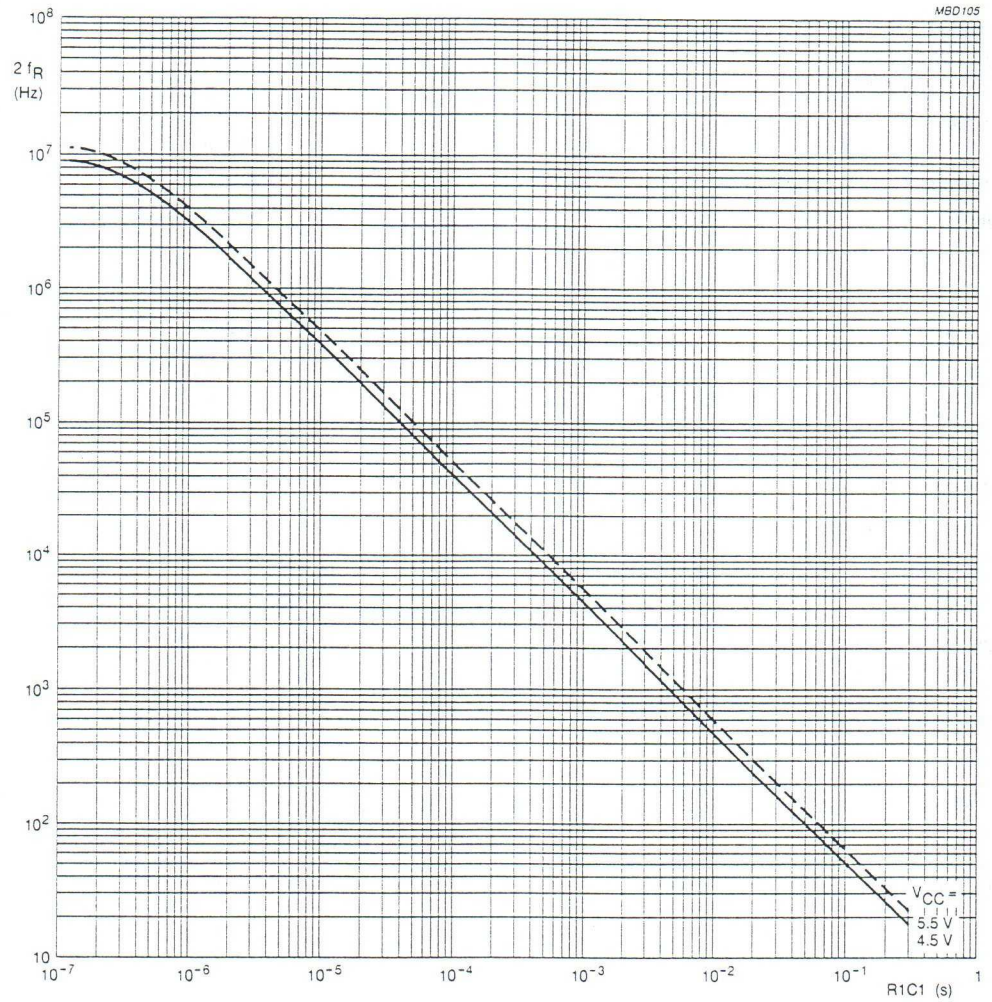


Fig.30 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.



$$K_V = \frac{2f_L}{V_{VCOIN}\ range} 2\pi\ (r/s/V).$$

--- 5.5 V

___ 4.5 V

Fig.31 Typical frequency lock range $2f_L$ as a function of the product R1C1: V_{VCOIN} range = 1.1 to (V_{CC} – 1.1 V) V.

PLL DESIGN EXAMPLE

The frequency synthesizer used in the design example shown in Fig.32 has the following parameters:

output frequency	:	2 MHz to 3 MHz
frequency steps	:	100 kHz
settling time	:	1 ms
overshoot	:	<20%

The open loop gain is H (s) × G (s) =

$K_p \times K_f \times K_o \times K_n$

and the closed loop:

$$\frac{\Theta u}{\Theta i} = \frac{K_p K_f K_o K_n}{1 + K_p K_f K_o K_n}, \text{ where}$$

K_p = phase comparator gain

K_f = low-pass filter transfer gain

K_o = K_v/s VCO gain

K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min} = \frac{f_{out}}{f_{step}} = \frac{2MHz}{100kHz} = 20$$

$$N_{max} = \frac{f_{out}}{f_{step}} = \frac{3MHz}{100kHz} = 30$$

The VCO is set by the values of R1, R2 and C1; R2 = 10 kΩ (adjustable).

The values can be determined using the information in the section: "DESIGN CONSIDERATIONS".

With f_O = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):

R1 = 30 kΩ
R2 = 30 kΩ
C1 = 100 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{(V_{CC} - 1.1) - 1.1}$$

$$= \frac{1MHz}{2.8} \times 2\pi \approx \times 2.24 \,.\, 10^6 \; r/s/V$$

The gain of the phase comparator PC2 is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r.}$$

Using PC2 with the passive filter as shown in Fig.32 results in a high gain loop with the same performance as a loop with an active filter. Hence loop filter equations as for a high gain loop should be used. The current source output of PC2 can be simulated then with a fictive filter resistance $R_3' = \frac{R_b}{17}$.

The transfer functions of the filter is given by:

$$K_p = \frac{1 + s\tau_2}{s\tau_1}$$

Where:

τ_1 = R3, C2 and τ_2 = R4, C2.

The characteristic equation is:

$1 + K_p.K_f.K_o.K_n$

This results in:

$$1 + K_p \left(\frac{1 + s\tau_2}{s\tau_1}\right) \frac{K_v}{s} K_n = 0$$

$$\text{or } s^2 + s\, K_p\, K_v\, K_n \frac{\tau_2}{\tau_1} + K_p K_v K_n / \tau_1 = 0$$

This can be written as

$s^2 + 2\zeta\, \omega_n s + \omega_n^2 = 0$

with the natural frequency ω_n defined as $\omega_n = \sqrt{\frac{K_p K_v K_n}{\tau_1}}$

and the damping value given as $\zeta = 0.5.\tau_2.\omega_n$

In Fig.33 the output frequency response to a step of input frequency is shown.
The overshoot and settling time percentages are now used to determine ω_n. From Fig.33 it can be seen that the damping ratio ζ = 0.707 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \; r/s.$$

Rewriting the equation for natural frequency results in:

$$\tau_1 = \frac{K_p \times K_v \times K_n}{\omega_n^2}$$

The maximum overshoot occurs at N_{max} = 30; hence K_n = 1/30:

$$\tau_1 = \frac{0.4 \times 2.24 \times 10^6}{5000^2 \times 30} = 0.0012$$

When C2 = 470 nF, it follows

$$R_3' = \frac{\tau_1}{C_2} = \frac{0.0012}{470\ 10^{-9}} = 2550\ \Omega$$

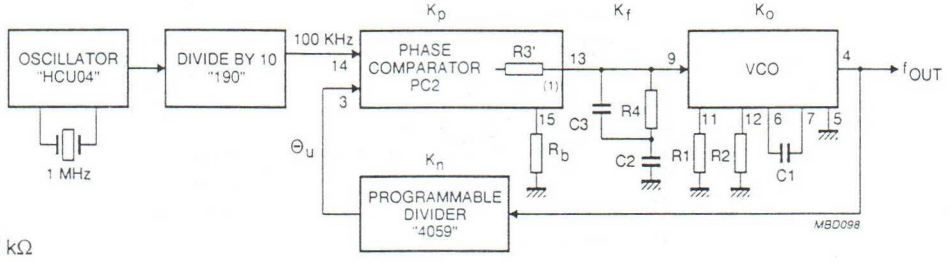
Hence the current source bias resistance R_b = 17 × 2550 = 43 kΩ

With ζ = 0.707 (= 0.5 τ_2 ω_n) it follows

$$\tau_2 = \frac{0.707}{0.5 \times 5000} = 0.00028$$

$$R_4 = \frac{\tau_2}{C_2} = \frac{0.00028}{470.10^{-9}} = 600\ \Omega$$

For extra ripple suppression a capacitor C3 can be connected in parallel with R4, with an extra $\tau_3 = R_4 C_3$.
For stability reasons τ_3 should be < 0.1 τ_2, hence C_3 < 0.1 C_2, or C_3 = 39 nF.



R1 = 30 kΩ
R2 = 30 kΩ
C1 = 100 pF
R_3' = 2550 Ω
R_b = 43 kΩ
R4 = 600 Ω
C2 = 470 nF
C3 = 39 nF

(1) R_3' = fictive

$$R_3' = \frac{R_b}{17}.$$

Fig.32 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011. Also available a computer design program for PLL's ordering number 9398 961 10061.

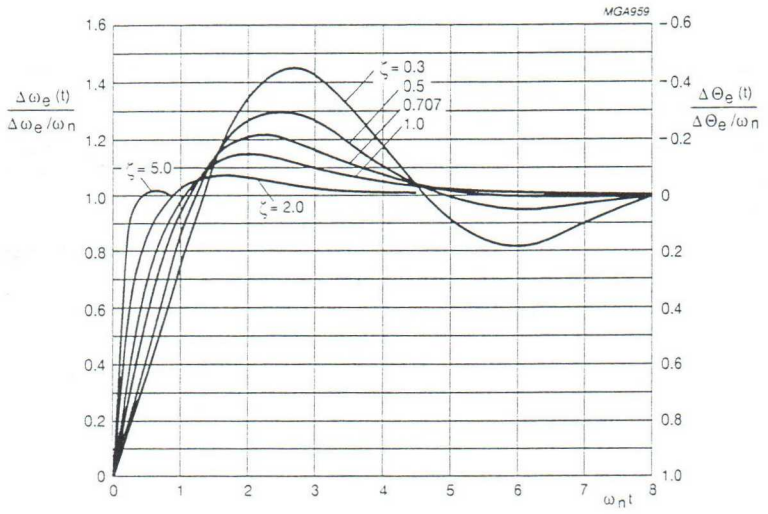


Fig.33 Type 2 second order frequency step response.

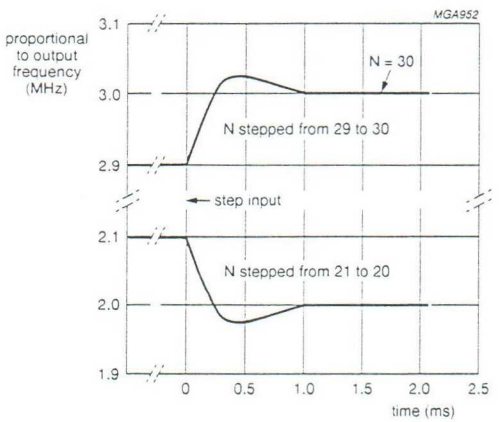


Fig.34 Frequency compared to the time response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared with the phase detector sampling rate but short compared with the PLL response time.

SUPERSEDES DATA OF MARCH 1988

NINE WIDE SCHMITT TRIGGER BUFFER; OPEN DRAIN OUTPUTS; INVERTING

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9114 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9114 are nine wide Schmitt trigger inverting buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9114 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The "9114" is identical to the "9115" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLZ}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_8	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Y}_0$ to $\overline{Y}_8$	data outputs
11		
20	V_{CC}	positive supply voltage

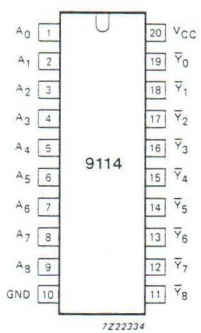


Fig. 1 Pin configuration.

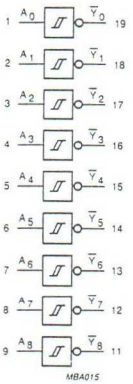


Fig. 2 Logic diagram.

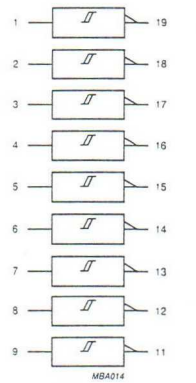


Fig. 3 IEC logic diagram.

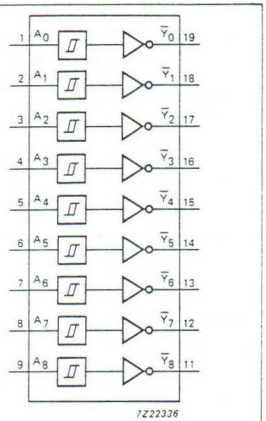


Fig. 4 Functional diagram.

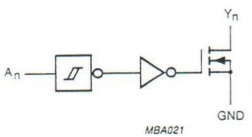


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	$\overline{Y}_n$
L	Z
H	L

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Fig. 6
V_{T-}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig. 6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLZ}	propagation delay A_n to $\overline{Y}_n$		36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Fig. 6
V_{T-}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Fig. 6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Fig. 6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLZ}	propagation delay A_n to $\overline{Y}_n$		17	31		39		47	ns	4.5	Fig. 7
t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig. 7

TRANSFER CHARACTERISTIC WAVEFORMS

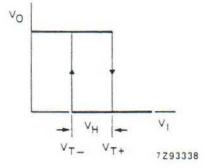


Fig. 6 Transfer characteristic.

AC WAVEFORMS

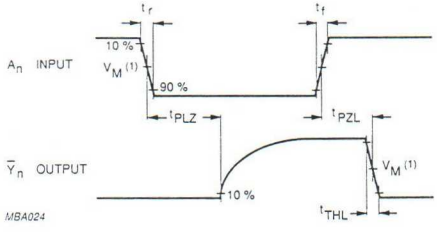


Fig. 7 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

SUPERSEDES DATA OF MARCH 1988

NINE WIDE SCHMITT TRIGGER BUFFER; OPEN DRAIN OUTPUTS

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9115 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9115 are nine wide Schmitt trigger buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9115 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is HIGH, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The "9115" is identical to the "9114" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLZ}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_8	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_8	data outputs
20	V_{CC}	positive supply voltage

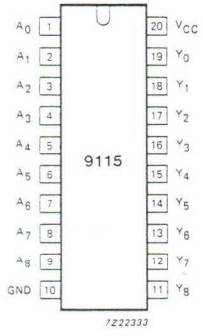


Fig. 1 Pin configuration.

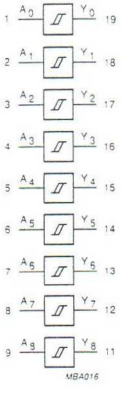


Fig. 2 Logic diagram.

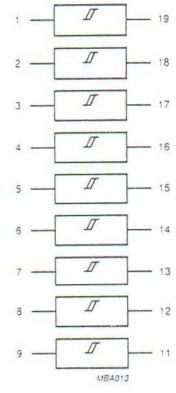


Fig. 3 IEC logic diagram.

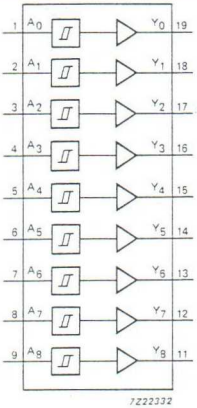


Fig. 4 Functional diagram.

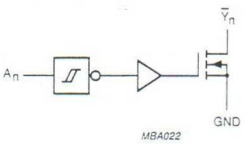


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	Y_n
L	L
H	Z

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Fig. 6
V_{T-}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig. 6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig. 6

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLZ}	propagation delay A_n to Y_n		36 13 10	115 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are refered to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Fig. 6
V_{T-}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Fig. 6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Fig. 6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLZ}	propagation delay A_n to Y_n		18	31		39		47	ns	4.5	Fig. 7
t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig. 7

TRANSFER CHARACTERISTIC WAVEFORMS

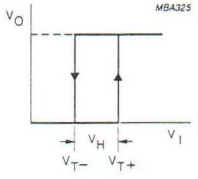


Fig. 6 Transfer characteristic.

AC WAVEFORMS

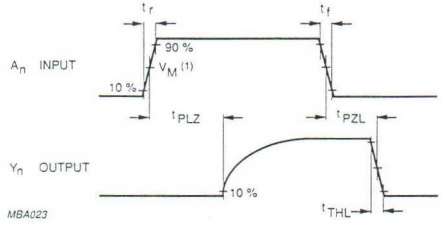


Fig. 7 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT SYNCHRONOUS BCD DOWN COUNTER

FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40102 are high-speed Si-gate CMOS devices and are pin compatible with the "40102" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40102 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40102" is configured as two cascaded 4-bit BCD counters and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.
When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent two 4-bit BCD words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	30	31	ns
f_{max}	maximum clock frequency		30	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	25	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset input (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

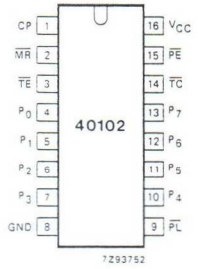


Fig. 1 Pin configuration.

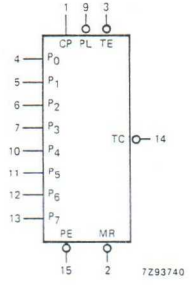


Fig. 2 Logic symbol.

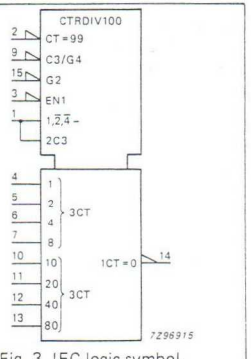


Fig. 3 IEC logic symbol.

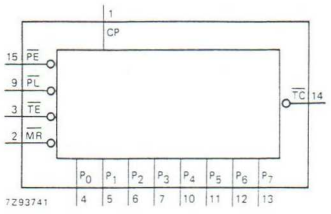


Fig. 4 Functional diagram.

GENERAL DESCRIPTION

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 99) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 clock pulses long.

The "40102" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

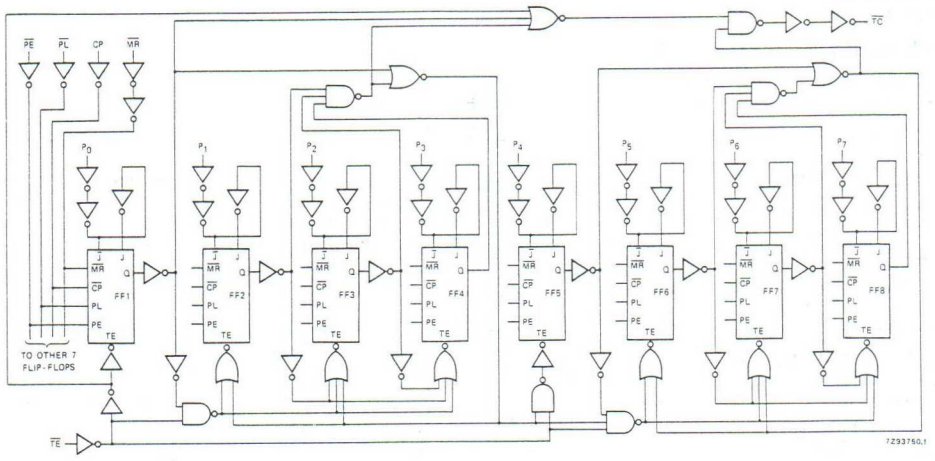


Fig. 5 Logic diagram.

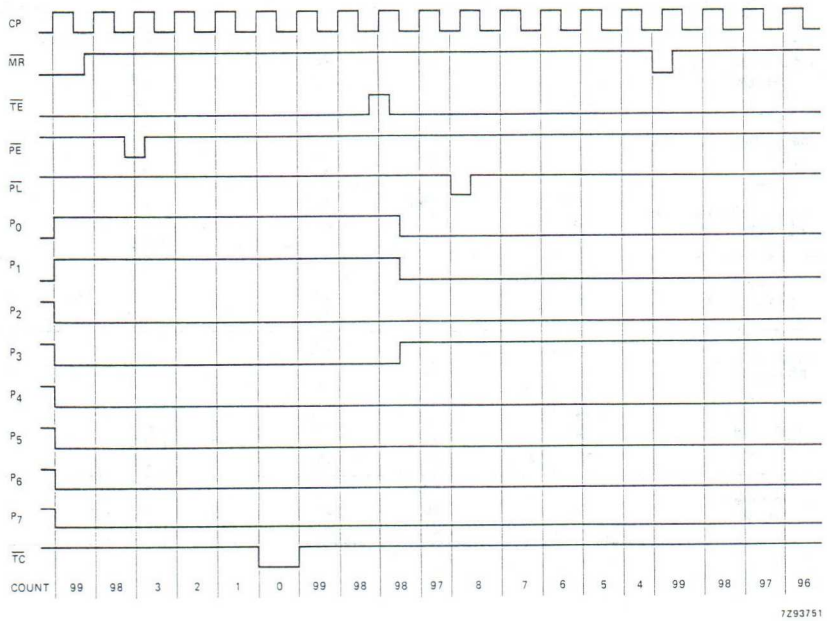


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		96 35 28	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		50 18 14	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay P_n, $\overline{PL}$ to $\overline{TC}$		110 40 32	240 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 9
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{TC}$		83 30 24	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		9 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 7 and 8
t_W	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width LOW	150 30 26	30 11 9		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{PL}$; $\overline{MR}$ to CP	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	100 20 17	36 13 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	175 35 30	50 18 14		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time P_n to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{PE}$ to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{TE}$ to CP	0 0 0	−41 −15 −12		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time P_n to CP	2 2 2	−5 −5 −5		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 12
f_{max}	maximum clock pulse frequency	3 15 18	8.9 27 32		2 12 14		2 10 12		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$, $\overline{PE}$	1.50
$\overline{MR}$	1.00
$\overline{TE}$	0.80
P_n	0.25
$\overline{PL}$	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay P_n; CP to $\overline{TC}$		38	63		79		95	ns	4.5	Figs 7 and 9
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		25	50		63		75	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		49	83		104		125	ns	4.5	Fig. 9
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{TC}$		31	55		69		83	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 7 and 8
t_W	clock pulse width HIGH or LOW	33	11		41		50		ns	4.5	Fig. 7
t_W	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	43	25		54		65		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{PL}$; $\overline{MR}$ to CP	10	1		13		15		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	20	10		25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	40	20		50		60		ns	4.5	Fig. 11
t_{su}	set-up time P_n to CP	20	12		25		30		ns	4.5	Fig. 12
t_h	hold time $\overline{PE}$ to CP	0	−4		0		0		ns	4.5	Fig. 11
t_h	hold time $\overline{TE}$ to CP	0	−15		0		0		ns	4.5	Fig. 11
t_h	hold time P_n to CP	0	−6		0		0		ns	4.5	Fig. 12
f_{max}	maximum clock pulse frequency	15	27		12		10		MHz	4.5	Fig. 7

AC WAVEFORMS

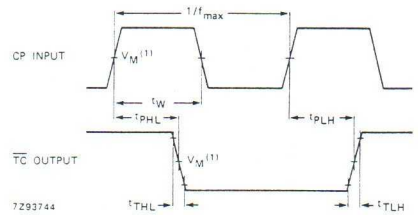


Fig. 7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

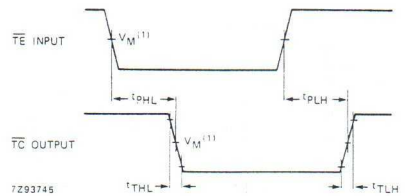


Fig. 8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.

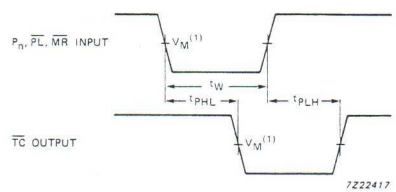


Fig. 9 Waveforms showing $\overline{PL}$, $\overline{MR}$, P_n to $\overline{TC}$ propagation delays.

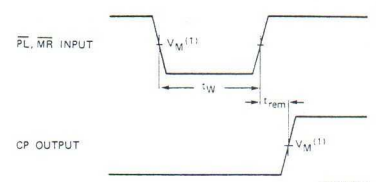


Fig. 10 Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$.

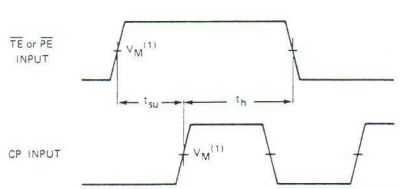


Fig. 11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.

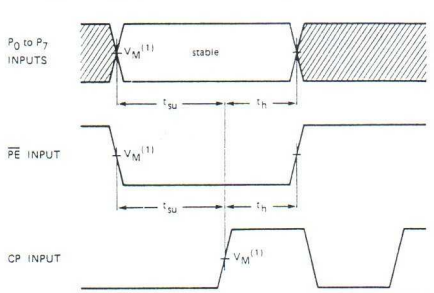


Fig. 12 Waveforms showing hold and set-up times for P_n, $\overline{PE}$ to CP.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION

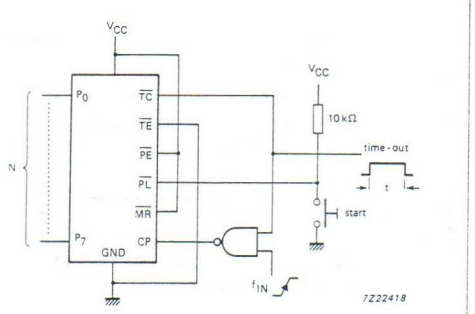


Fig. 13 Programmable timer.

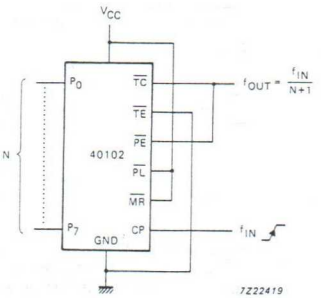


Fig. 14 Divide-by-N counter.

8-BIT SYNCHRONOUS BINARY DOWN COUNTER

FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.

When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent a single 8-bit binary word.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	30	30	ns
f_{max}	maximum clock frequency		32	31	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset input (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

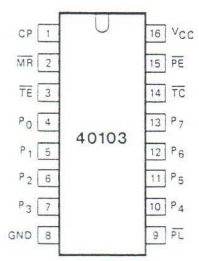


Fig. 1 Pin configuration.

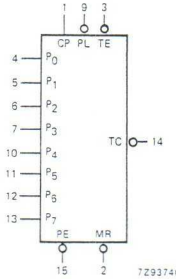


Fig. 2 Logic symbol.

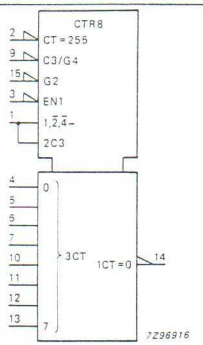


Fig. 3 IEC logic symbol.

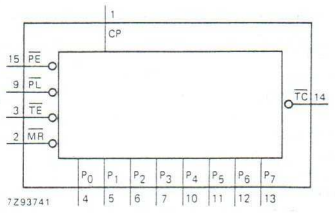


Fig. 4 Functional diagram.

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

GENERAL DESCRIPTION (Cont'd)

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

The "40103" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

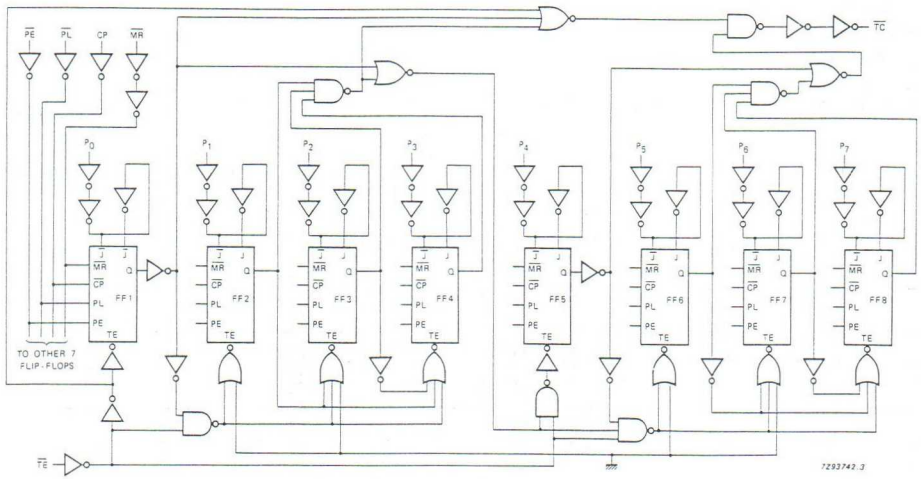


Fig. 5 Logic diagram.

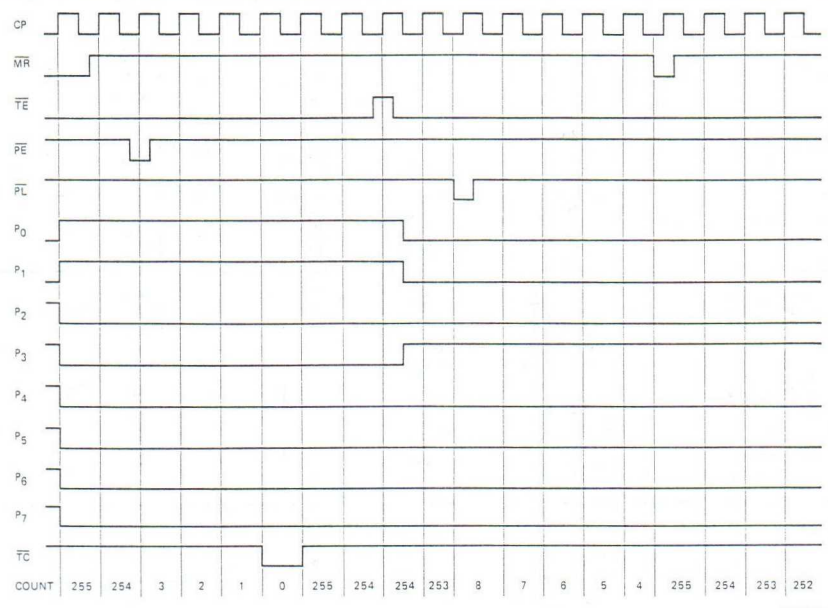


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		96 35 28	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		102 37 30	315 63 53		395 79 40		475 95 81	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$		83 30 24	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 7 and 8
t_W	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	125 25 21	33 12 10		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	150 30 26	44 16 13		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time P_n to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time $\overline{PE}$ to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0 0 0	−30 −11 −9		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time P_n to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 12
f_{max}	maximum clock pulse frequency	3.0 15 18	10 29 35		2.4 12 14		2.0 10 12		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$, $\overline{PE}$	1.50
$\overline{MR}$	1.00
$\overline{TE}$	0.80
$\overline{PL}$	0.35
P_n	0.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		35	60		75		90	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		23	40		50		60	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		44	75		94		112	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$		29	55		69		83	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs. 7 and 8
t_W	clock pulse width HIGH or LOW	33	10		41		50		ns	4.5	Fig. 7
t_W	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	38	22		48		57		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP	10	1		13		15		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	20	11		25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	40	20		50		60		ns	4.5	Fig. 11
t_{su}	set-up time P_n to CP	20	11		25		30		ns	4.5	Fig. 12
t_h	hold time $\overline{PE}$ to CP	2	−3		2		2		ns	4.5	Fig. 11

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0	−10		0		0		ns	4.5	Fig. 11
t_h	hold time P_n to CP	0	−5		0		0		ns	4.5	Fig. 12
f_{max}	maximum clock pulse frequency	15	28		12		10		MHz	4.5	Fig. 7

AC WAVEFORMS

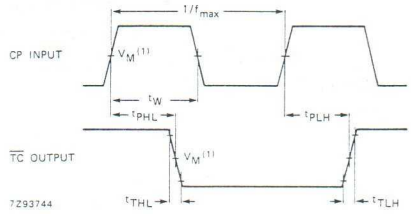


Fig. 7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

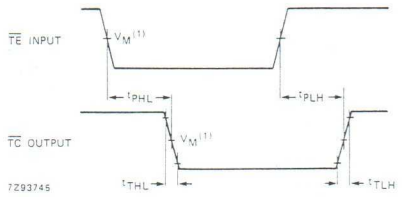


Fig. 8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.

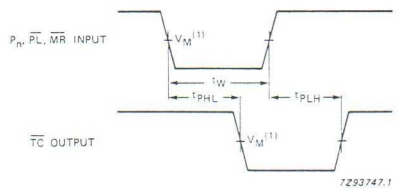


Fig. 9 Waveforms showing $\overline{PL}$, $\overline{MR}$, P_n to $\overline{TC}$ propagation delays.

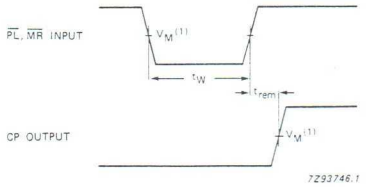


Fig. 10 Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$.

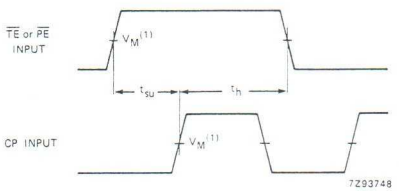


Fig. 11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.

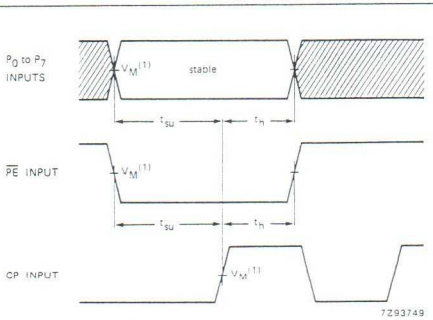


Fig. 12 Waveforms showing hold and set-up times for P_n, $\overline{PE}$ to CP.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION

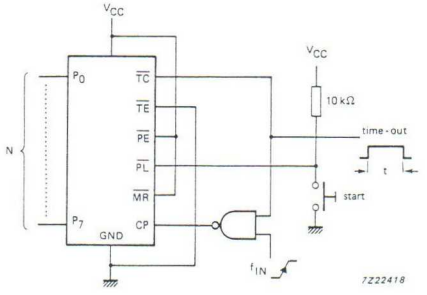


Fig. 13 Programmable timer.

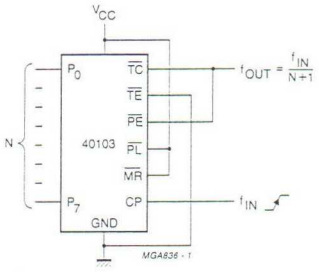


Fig. 14 Divide-by-N counter.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

In the parallel-load mode (S_0 and S_1 are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D_{SR}) and shift-left (D_{SL}) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S_0 and S_1) LOW and clocking the register. When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

APPLICATIONS

- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	13	15	ns
f_{max}	maximum clock frequency		62	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	75	75	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D_{SR}	serial data shift-right input
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data shift-left input
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	3-state parallel outputs
16	V_{CC}	positive supply voltage

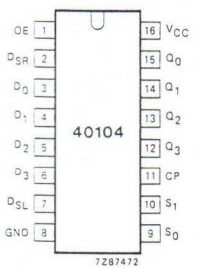


Fig. 1 Pin configuration.

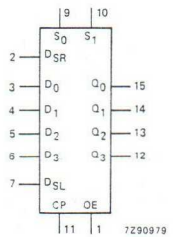


Fig. 2 Logic symbol.

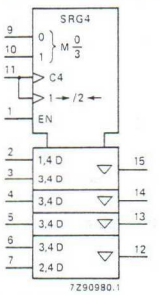


Fig. 3 IEC logic symbol.

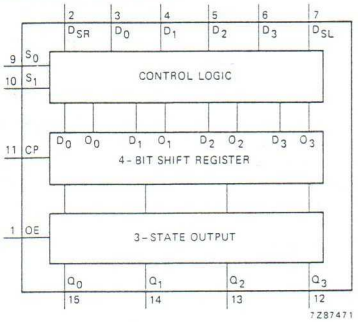


Fig. 4 Functional diagram.

FUNCTION TABLE

H = HIGH voltage level
L = LOW voltage level
X = don't care
t_{n+1} = state after next LOW-to-HIGH transition of CP

OPERATING MODES	INPUTS (OE = HIGH)					OUTPUTS at t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	D_0 to D_3	Q_0	Q_1	Q_2	Q_3
reset	L	L	X	X	X	L	L	L	L
shift left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
shift right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

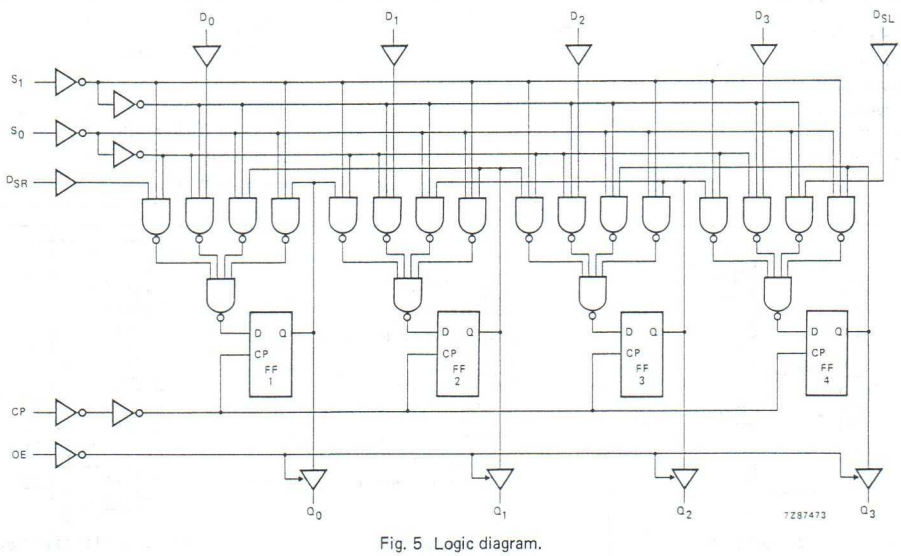


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time OE to Q_n		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time S_0, S_1 to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time S_0, S_1 to CP	2 2 2	−14 −5 −4		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	19 56 67		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_0 to D_3	0.35
D_{SR}, D_{SL}	0.35
CP	0.35
S_0, S_1	0.70
OE	1.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		18	34		43		51	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time OE to Q_n		12	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time OE to Q_n		21	35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	16	8		20		24		ns	4.5	Fig. 8
t_{su}	set-up time S_0, S_1 to CP	20	9		25		30		ns	4.5	Fig. 8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2	−2		2		2		ns	4.5	Fig. 8
t_h	hold time S_0, S_1 to CP	2	−5		2		2		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

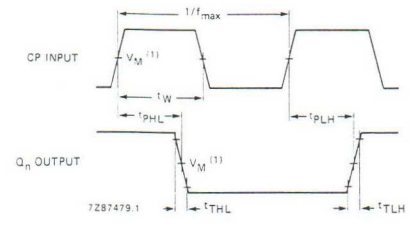


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

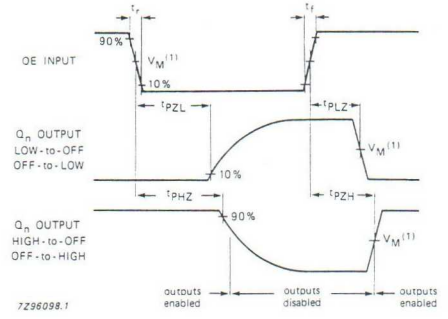


Fig. 7 Waveforms showing the 3-state enable and disable times.

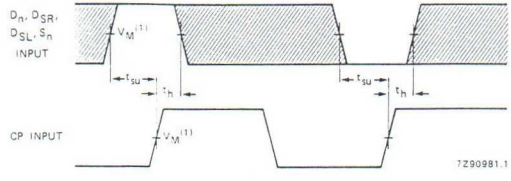


Fig. 8 Waveforms showing the set-up and hold times from the D_n, D_{SR}, D_{SL} and S_n inputs to the clock (CP).

Note to Fig 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

4-BIT X 16-WORD FIFO REGISTER

FEATURES

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay MR to DIR, DOR $\overline{SO}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	16 37	15 35	ns ns
t_{PHL}	propagation delay SI to DIR $\overline{SO}$ to DOR		16 17	18 18	ns ns
f_{max}	maximum clock frequency		33	31	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	134	145	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2	DIR	data-in ready output
3	SI	shift-in input (LOW-to-HIGH, edge-triggered)
4, 5, 6, 7	D_0 to D_3	parallel data inputs
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q_0 to Q_3	3-state data outputs
14	DOR	data-out ready output
15	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
16	V_{CC}	positive supply voltage

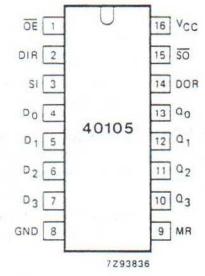


Fig. 1 Pin configuration.

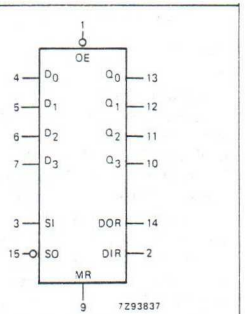


Fig. 2 Logic symbol.

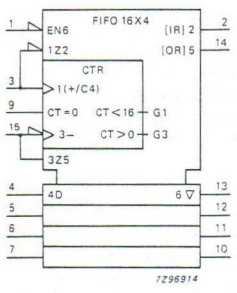


Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION

contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

INPUTS AND OUTPUTS

Data inputs (D_0 to D_3)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration, i.e. 3 x 16, down to 1 x 16, by tying unused data input pins to V_{CC} or GND.

Data outputs (Q_0 to Q_3)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset (MR)

When MR is HIGH, the control functions within the FIFO are cleared, and dat content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

DIR = HIGH indicates the input stage is empty and ready to accept valid data;

DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy);

DOR = HIGH assures valid data is present at the outputs Q_0 to Q_3 (does not indicate that new data is awaiting transfer into the output stage);

DOR = LOW indicates the output stage is busy or there is no valid data.

Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. It also triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the falling edge of the MR signal.

Shift-out control ($\overline{SO}$)

A HIGH-to-LOW transition of $\overline{SO}$ causes the DOR flags to go LOW. A HIGH-to-LOW transition of $\overline{SO}$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

Output enable ($\overline{OE}$)

The outputs Q_0 to Q_3 are enabled when $\overline{OE}$ = LOW. When $\overline{OE}$ = HIGH the outputs are in the high impedance OFF-state.

FUNCTIONAL DESCRIPTION

Data input

Following power-up, the master-reset (MR) input is pulsed HIGH to clear the FIFO memory (see Fig. 8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D_0 to D_3 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until DIR is set to HIGH and data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out ($\overline{SO}$) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI goes LOW (see Fig. 7).

Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q_0 to Q_3). The initial master-reset at power-on (MR = HIGH) sets DOR to LOW (see Fig. 8). After MR = LOW, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the $\overline{SO}$ control input. With $\overline{SO}$ = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When $\overline{SO}$ is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted-out leaving the FIFO empty the DOR flag remains LOW (see Fig. 9). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_3.

With the FIFO empty, the $\overline{SO}$ input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and as shift-out of data occurring. The $\overline{SO}$ control must be made LOW before additional data can be shifted-out (see Fig. 10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).

Due to the part-to-part spread of the ripple through time, the SI signals of $FIFO_A$ and $FIFO_B$ will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig. 18.

The "40105" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 32-words x 4-bits (see Fig. 19).

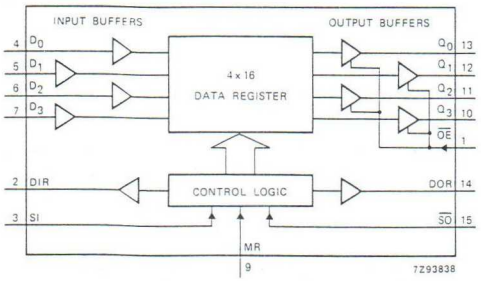


Fig. 4 Functional diagram.

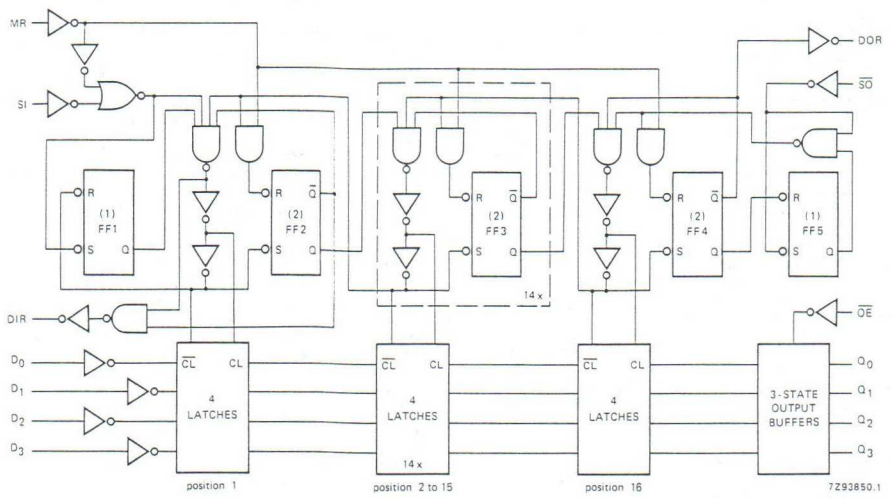


Fig. 5 Logic diagram.

Notes to Fig. 5

(see control flip-flops)

(1) LOW on $\overline{S}$ input of FF1 and FF5 will set Q output to HIGH independent of state on $\overline{R}$ input.

(2) LOW on $\overline{R}$ input of FF2, FF3 and FF4 will set Q output to LOW independent of state on $\overline{S}$ input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay MR to DIR, DOR		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay SI to DIR		52 19 15	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{SO}$ to DOR		55 20 16	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay $\overline{SO}$ to Q_n		116 42 34	400 80 68		500 100 85		600 120 102	ns	2.0 4.5 6.0	Fig. 14
t_{PLH}	propagation delay/ ripple through delay SI to DOR		564 205 165	2000 400 340		2500 500 425		3000 600 510	ns	2.0 4.5 6.0	Fig. 10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		701 255 204	2500 500 425		3125 625 532		3750 750 638	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 16
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		41 15 12	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 16
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14
t_W	SI pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	$\overline{SO}$ pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 9
t_W	DIR pulse width HIGH	12 6 5	58 21 17	180 36 31	10 5 4	225 45 38	10 5 4	270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_W	DOR pulse width LOW	12 6 5	55 20 16	170 34 29	10 5 4	215 43 37	10 5 4	255 51 43	ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 74HC (Cont'd)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	MR pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to SI	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 15
t_{su}	set-up time D_n to SI	−5 −5 −5	−39 −14 −11		−5 −5 −5		−5 −5 −5		ns	2.0 4.5 6.0	Fig. 13
t_h	hold time D_n to SI	125 25 21	44 16 13		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 13
f_{max}	maximum pulse frequency SI, $\overline{SO}$ using flags or burst mode	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6, 9, 11 and 12
f_{max}	maximum pulse frequency SI, $\overline{SO}$ cascaded	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.75
SI	0.40
D_n	0.30
$\overline{MR}$	1.50
$\overline{SO}$	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay MR to DIR, DOR		18	35		44		53	ns	4.5	Fig. 8
t_{PHL}	propagation delay SI to DIR		21	42		53		63	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{SO}$ to DOR		20	42		53		63	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n		40	80		100		120	ns	4.5	Fig. 14
t_{PLH}	propagation delay/ ripple through delay SI to DOR		188	400		500		600	ns	4.5	Fig. 10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		244	500		625		750	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		18	35		44		53	ns	4.5	Fig. 16
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn		15	30		38		45	ns	4.5	Fig. 16
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 14
t_W	SI pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 6
t_W	$\overline{SO}$ pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 9
t_W	DIR pulse width HIGH or LOW	6	20	34	5	43	5	51	ns	4.5	Fig. 7
t_W	DOR pulse width HIGH or LOW	6	19	34	5	43	5	51	ns	4.5	Fig. 9
t_W	MR pulse width HIGH	16	7		20		24		ns	4.5	Fig. 8
t_{rem}	removal time MR to SI	15	7		19		22		ns	4.5	Fig. 15
t_{su}	set-up time D_n to SI	−5	−14		−4		−4		ns	4.5	Fig. 13
t_h	hold time D_n to SI	27	16		34		41		ns	4.5	Fig. 13
f_{max}	maximum pulse frequency SI, $\overline{SO}$ using flags or burst mode		28		12		10		MHz	4.5	Figs 6, 9, 11 and 12
f_{max}	maximum pulse frequency SI, $\overline{SO}$ cascaded		28		12		10		MHz	4.5	Figs 6 and 9

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

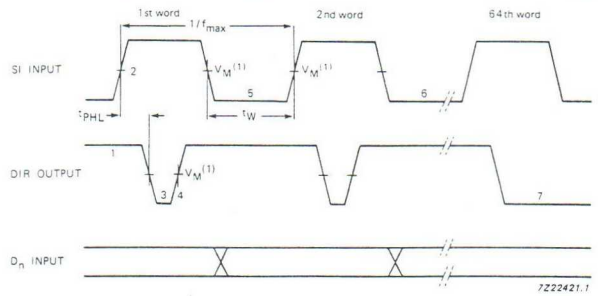


Fig. 6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig. 6

1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage "busy".
4. DIR goes HIGH, status flag indicates FIFO prepared for additional data; data from first location "ripple through".
5. SI set LOW; necessary to complete shift-in process.
6. Repeat process to load 2nd word through to 16th word into FIFO.
7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

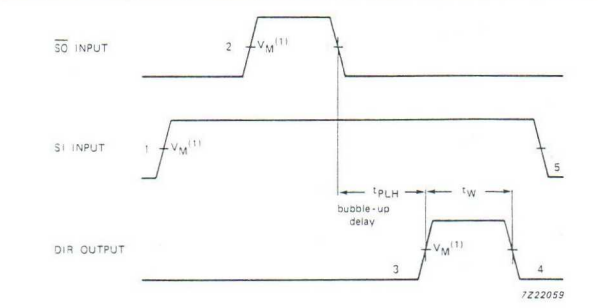


Fig. 7 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig. 7

1. FIFO is intially, shift-in is held HIGH.
2. $\overline{SO}$ pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
4. DIR returns to LOW; FIFO is full again.
5. SI brought LOW; necessary to complete whidt-in process, DIR remains LOW, because FIFO is full.

AC WAVEFORMS

Master reset applied with FIFO full

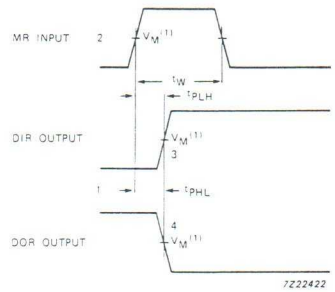


Fig. 8 Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

Notes to Fig. 8

1. DIR LOW, output ready HIGH; assume FIFO is full.
2. MR pulse HIGH; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty

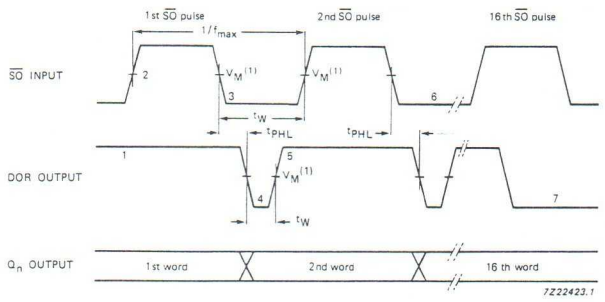


Fig. 9 Waveforms showing the $\overline{SO}$ input to DIR output propagation delay. The $\overline{SO}$ pulse width and $\overline{SO}$ maximum pulse frequency.

Notes to Fig. 9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2. $\overline{SO}$ set HIGH.
3. $\overline{SO}$ is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
4. DOR drops LOW; output stage "busy".
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
6. Repeat process to unload the 3rd through to the 16th word from FIFO.
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation

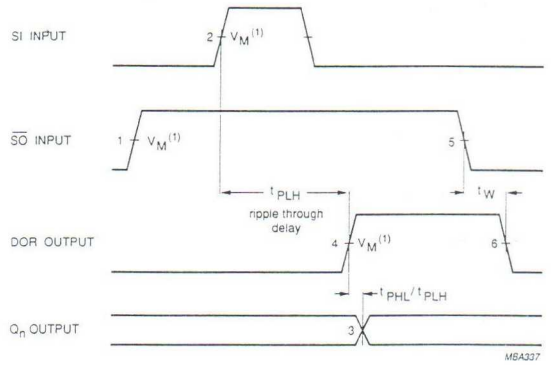


Fig. 10 Waveforms showing ripple through delay SI input to DOR output and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig. 10

1. FIFO is initially empty, $\overline{SO}$ is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. DOR flag signals the arrival of valid data at the output stage.
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
5. $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.
6. DOR goes LOW; FIFO is empty again.

Shift-in operation; high-speed burst mode

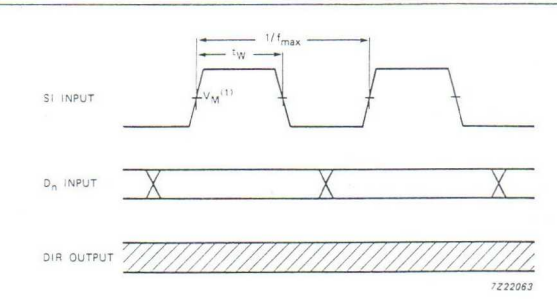


Fig. 11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig. 11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

AC WAVEFORMS

Shift-out operation; high-speed burst mode

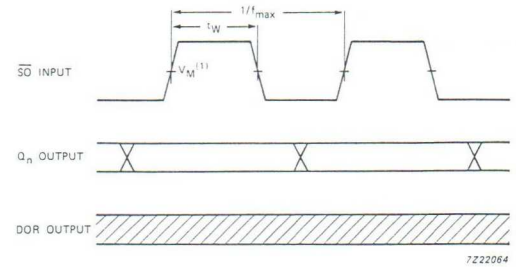


Fig. 12 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig. 12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a $\overline{SO}$ pulse can be applied without regard to the flag.

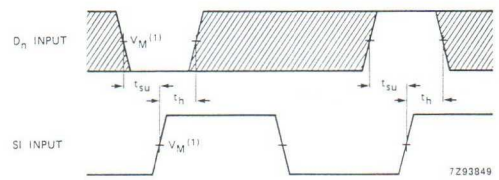


Fig. 13 Waveforms showing hold and set-up times for D_n input to SI input.

Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.

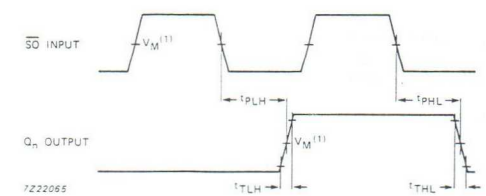


Fig. 14 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

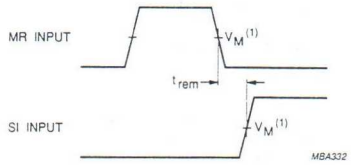


Fig. 15 Waveforms showing the MR input to SI input removal time.

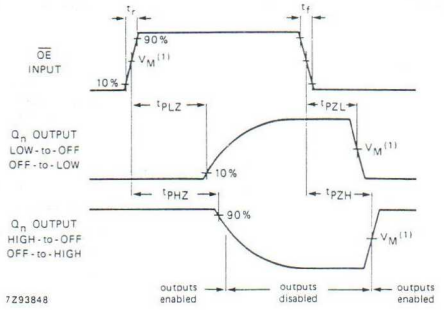


Fig. 16 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

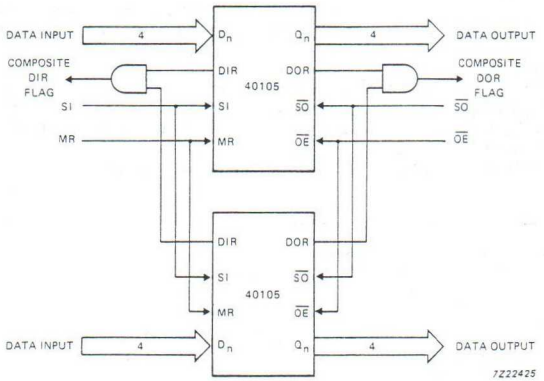


Fig. 17 Expanded FIFO for increased word length; 16 words x 8 bits.

Note to Fig. 17

The PC74HC/HCT40105 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

APPLICATION INFORMATION

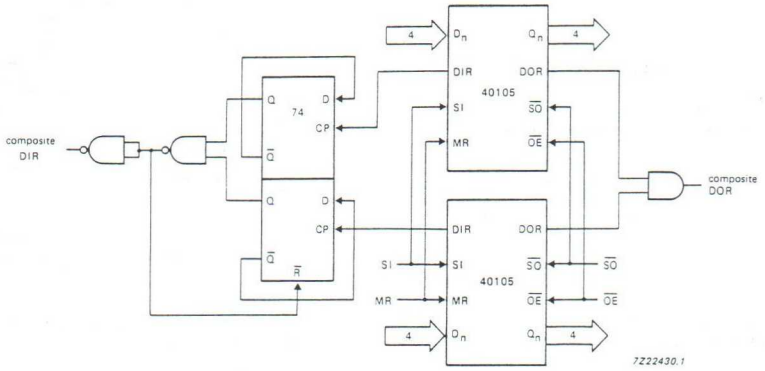


Fig. 18 Expanded FIFO for increased word length.

Note to Fig. 18

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started (see Fig. 7).

Expanded format

Fig. 19 shows two cascaded FIFOs providing a capacity of 32 words x 4 bits.
Fig. 20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.
Fig. 21 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH.
Fig. 22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

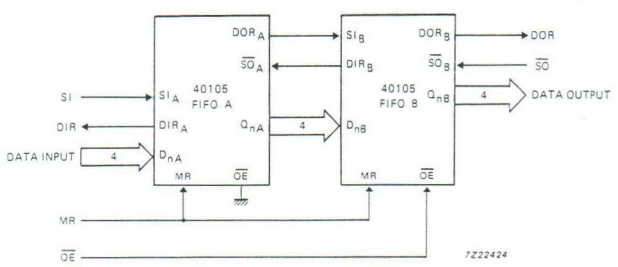


Fig. 19 Cascading for increased word capacity; 32 words x 4 bits.

Note to Fig. 19

The PC74HC/HCT40105 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 and 19 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Fig. 22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

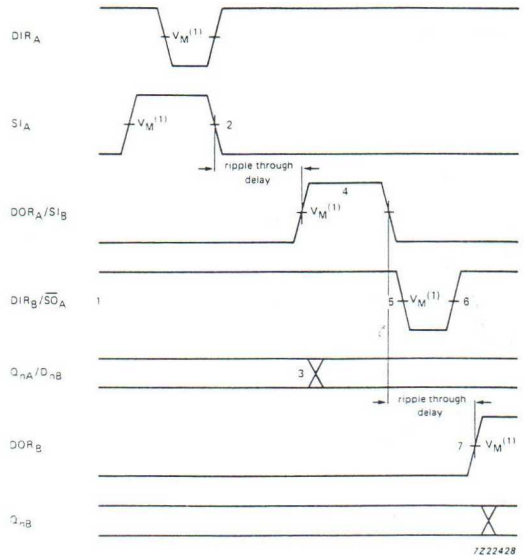


Fig. 20 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig. 20

1. FIFO$_A$ and FIFO$_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data.
2. Load one word into FIFO$_A$; SI pulse applied, results in DIR pulse.
3. Data out $_A$/data in $_B$ transition; valid data arrives at FIFO$_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO$_B$.
4. DOR$_A$ and SI$_B$ pulse HIGH; (ripple through delay after SI$_A$ LOW) data is unloaded from FIFO$_A$ as a result of the data output ready pulse, data is shifted into FIFO$_B$.
5. DIR$_B$ and $\overline{SO}_A$ go LOW; flag indicates input stage of FIFO$_B$ is busy, shift-out of FIFO$_A$ is complete.
6. DIR$_B$ and $\overline{SO}_A$ go HIGH automatically; the input stage of FIFO$_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data.
7. DOR$_B$ goes HIGH; (ripple through delay after SI$_B$ LOW) valid data is present one propagation delay later at the FIFO$_B$ output stage.

APPLICATION INFORMATION

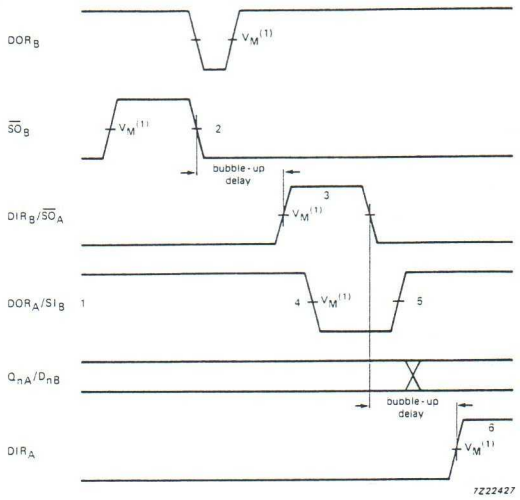


Fig. 21 FIFO to FIFO communication; output timing under full condition.

Notes to Fig. 21

1. FIFO$_A$ and FIFO$_B$ initially full, SI$_B$ held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word from FIFO$_B$; $\overline{SO}$ pulse applied, results in DOR pulse.
3. DIR$_B$ and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into FIFO$_B$ as a result of the DIR pulse, data is shifted out of FIFO$_A$.
4. DOR$_A$ and SI$_B$ go LOW; flag indicates the output stage of FIFO$_A$ is busy, shift-in to FIFO$_B$ is complete.
5. DOR$_A$ and SI$_B$ go HIGH; flag indicates valid data is again available at FIFO$_A$ output stage, SI$_B$ is held HIGH, awaiting bubble-up of empty location.
6. DIR$_A$ goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of FIFO$_A$.

Note to application waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

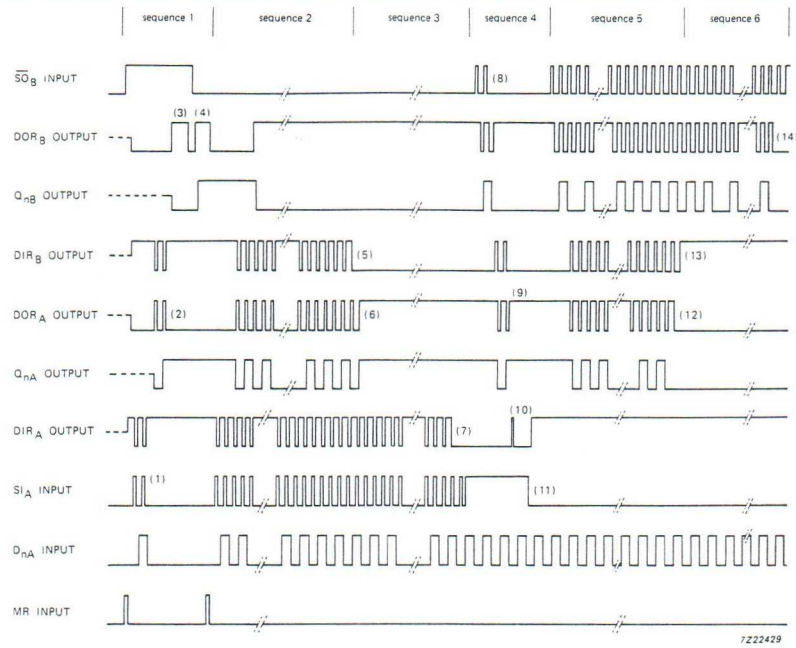


Fig. 22 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig. 19).

Note to Fig. 22

Sequence 1 (Both FIFOs empty, starting shift-in process):
After a MR pulse has been applied $FIFO_A$ and $FIFO_B$ are empty. The DOR flags of $FIFO_A$ and $FIFO_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of $FIFO_A$ and to the input stage of $FIFO_B$ (2). When data arrives at the output of $FIFO_B$, a DOR_B pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full):
After the MR pulse, a series of 16 SI pulses are applied. When 16 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full):
When 17 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 17th data word (6). After the 32th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process):
SI_A is held HIGH and two $\overline{SO}_B$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty):
At the start of sequence 5 $FIFO_A$ contains 15 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of $\overline{SO}_B$ pulses are applied. After 15 $\overline{SO}_B$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty):
After the next $\overline{SO}_B$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty (13). After another 15 $\overline{SO}_B$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO}_B$ pulses have no effect. The last word remains available at the output Q_n.

APPLICATION NOTES

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HANDLING PRECAUTIONS

Electrostatic charges

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is 1 kΩ to 0,5 MΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be earthed via a wrist strap and a resistor.
- All electrical equipment should be connected to the mains via an earth-leakage switch and the equipment cases should be earthed.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

CMOS ICs are packed for despatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the task should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

Assembly

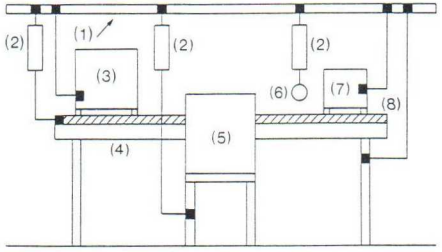
CMOS ICs must be removed from their protective packing with earthed component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail
(2) Resistor (500 kΩ ± 10%, 0,5 W)
(3) Ionizer
(4) Work bench
(5) Chair
(6) Wrist strap
(7) Electrical equipment
(8) Conductive surface/ antistatic sheet

Fig. 1 Protected work station.

POWER SUPPLY LINE LAYOUT AND DECOUPLING RECOMMENDATIONS

Spikes due to output current switching and the charging and discharging of parasitic capacitance, are the two main sources of noise on the power lines of HCMOS logic systems. To minimize noise, the power supply should be decoupled. However, if switching speed is high, not only the voltage dips on the power lines must be considered but also the effects of di/dt radiation. Decoupling requirements are a balance between the precautions necessary to reduce the effects of these two phenomena.

The first requirement for minimizing noise is a well designed power distribution network. For instance, it is essential to have a good ground (GND) connection pattern on a pcb. Even the commonly used GND pattern shown in Fig.1 can cause problems. In Fig.1, an output from IC1 drives an input of IC2, and an output from IC3 drives an input of IC4. Since the signal paths between IC1 and IC2, and between IC3 and IC4 are not coupled, there should be no crosstalk between them. However, IC1 and IC3 share the hatched section of the GND comb, and, when the output of IC1 switches, a spike could be generated on the GND of IC3. This could be transmitted to IC4 via the IC3-IC4 signal connection causing the output of IC4 to switch erroneously. If a double-sided board is used, it is therefore advisable to reduce the length of individual sections of the GND comb by installing links on the opposite side of the board as shown in Fig.2. This is especially important for boards on which high level currents are switched.

It is bad practice to use jumpers to connect GND/V_{CC} pins of ICs to pcb tracks (Fig.3). Jumpers are unlikely to be used on production boards, but they should not be used on prototype or one-off boards either because the inductance they introduce into the lines causes coupling between outputs. Printed connections should therefore be used to interconnect power tracks and IC pins. An even better solution is to use multi-layer boards so that individual layers can be used as a V_{CC} plane and a groundplane. The power supply can then be connected directly to the IC supply pins. Also, the inherent capacitance between the V_{CC} plane and the groundplane will reduce the amplitude of any high frequency noise on the power supply.

This inherent capacitance has the distinct advantage of being free from the inductance associated with discrete decoupling capacitors. A less expensive alternative to a multi-layer board is a multi-wire board which offers the same high frequency noise characteristics. With double-sided boards, it is not possible to dedicate a layer to a V_{CC} plane and a groundplane. Nevertheless, if at all possible, it is still best to have the V_{CC} and ground tracks on opposite sides of the board.

Connectors on any type of pcb should each have at least five ground pins to obtain good distribution of ground current.

The precautions outlined for ground tracks on the pcb are equally applicable to the power (V_{CC}) lines.

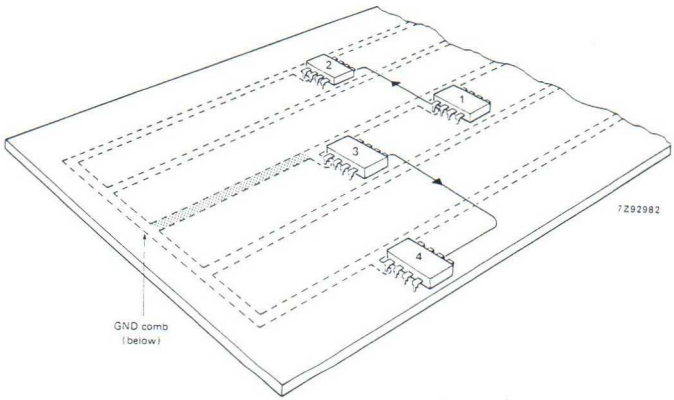


Fig.1 Common ground path on double-sided board

The wide HCMOS power supply range of 2 V to 6 V may suggest that voltage regulation is not necessary, but it must be remembered that supply voltage level variations will influence switching speed, noise immunity and power consumption. Supply voltage differences between ICs must also be avoided because a difference of as little as 0,5 V between power lines can cause unwanted effects. To isolate noise sources and avoid the use of a large voltage stabilizer with its heavy gauge (low impedance) wiring to each board, it is better to have a separate stabilizer for each board. However, care must be taken because a fault on a stabilizer for one board may be transmitted via the HCMOS input structure to other boards, possibly causing damage.

No matter how good the V_{CC} and GND connections are, all line inductance cannot be eliminated. This is where decoupling plays its part.

Ceramic capacitors are best for decoupling because they have very low series inductance. The advantage of using them will, however, be lost if they are connected too far from the IC. The inductance of the long tracks in conjunction with the capacitor will then form a very high-Q LC tuned-circuit, and the oscillations produced will have a worse effect than not having any decoupling at all. If it is impossible to make connections between decoupling capacitors and ICs shorter than 20 mm, then use several tracks connected in parallel and separated by at least one track-width (Fig.4). Some ceramic capacitors have preformed leads as shown in Fig.5(a). These leads introduce unwanted inductance. It is better to use capacitors with straight leads mounted as shown in Fig.5(b).

In general, the minimum requirements for good decoupling are:

- one 47 μF bulk capacitor per Eurocard
- one 1 μF tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal IC and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per 4 packages of SSI logic

An example showing how to determine the value of decoupling capacitor follows. Assume a buffer output sees a 100 Ω dynamic load and the output LOW-to-HIGH transition is 5 V; the current demand is therefore 50 mA per output. For an octal buffer, the current demand would be 0,4 A for 6 ns.

The instantaneous current in the capacitor is:

$$i = \frac{\Delta Q}{\Delta t}$$

$$\text{And } i = \frac{C\Delta V}{\Delta t} \quad (\text{from } Q = CV)$$

$$\text{Therefore, } C = \frac{i\Delta t}{\Delta V}$$

For an octal buffer and a change in V_{CC} of 0,4 V say,

$$C = \frac{0{,}4\ \text{A} \times 6 \times 10^{-9}\ \text{ns}}{0{,}4\ \text{V}} = 6\ \text{nF}.$$

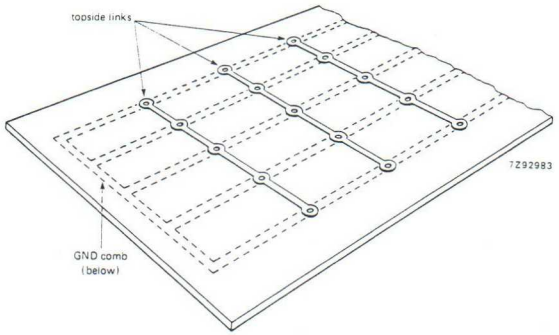


Fig.2 Reducing the length of common ground paths on double-sided board

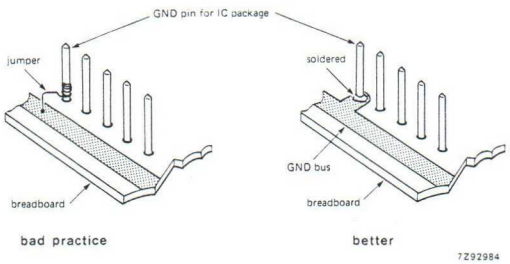


Fig.3 Methods of making ground connections

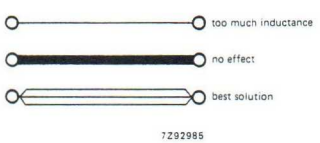


Fig.4 Power supply tracks

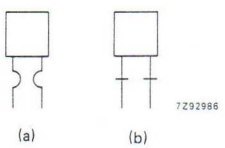


Fig.5 Leads of decoupling capacitors:
(a)unsuitable; (b) preferred

POWER DISSIPATION CONSIDERATIONS

For LSTTL logic ICs operating below 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With HCMOS logic ICs however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it is practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one and two orders of magnitude lower than the system clock frequency and the ICs therefore only draw quiescent current for most of the time. This means that replacing LSTTL ICs with equivalent 74HCT ICs, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

However, total system power dissipation, is the sum of both the quiescent and the dynamic power dissipation of all the ICs and must be determined and minimized during system design. For LSTTL, where the quiescent power dissipation is the most significant contributor to the total power dissipation, the total power dissipation can be simply derived from the product of V_{CC} and I_{CC} given in the data sheets. For HCMOS circuits however, the dynamic power dissipation which is the most significant part of the total power dissipation is influenced by circuit design. It cannot be read direct from the data sheets but must be calculated from the supply voltage, average switching frequency, load capacitance, internal capacitances of the IC, and transient switching currents.

This article explains how our method of specifying HCMOS ICs in the data sheets makes it very simple to calculate their quiescent, dynamic and total power dissipation.

QUIESCENT POWER DISSIPATION

Quiescent power is dissipated by an IC when it is not switching and $V_I = V_{CC}$ or GND. Figure 1(a) will be used to illustrate this power dissipation in HCMOS ICs. In the quiescent state, either the PMOS or the NMOS transistor is fully off and, in theory, no direct MOS transistor channel path exists between V_{CC} and GND. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. This quiescent supply current (I_{CC}) is specified in the published data.

Three factors influence the value of I_{CC}, and therefore the quiescent power dissipation, for a particular IC. They are:

Temperature: increasing temperature causes I_{CC} to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated.

Device Complexity: MSI circuits dissipate more power than SSI circuits because they have a proportionally greater reverse-biased diode junction area.

Supply voltage: the number of minority charge-carriers is linearly related to reverse junction voltage.

Table 1 shows the JEDEC industry standard for the worst-case I_{CC} in HCMOS ICs. It shows the effect of temperature and circuit complexity on I_{CC} at the maximum recommended supply voltage V_{CC}. I_{CC} can be linearly derated for other supply voltages and would be approximately one-third of the value in Table 1 for a 74HC IC with $V_{CC} = 2$ V. Typical I_{CC} values are well below the maximum specified values.

TABLE 1

JEDEC industry standard for d.c. characteristics of HCMOS ICs

DC characteristics for 74HC/HCT

symbol	parameter	T_{amb} (°C) 74HC/HCT +25 min.	+25 typ.	+25 max.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V *	V_I	other
	quiescent supply current										
I_{CC}	SSI	–	–	2,0	20,0	–	40,0	μA	5,5	V_{CC}	$I_O = 0$
I_{CC}	flip-flops	–	–	4,0	40,0	–	80,0	μA	5,5	or	$I_O = 0$
I_{CC}	MSI	–	–	8,0	80,0	–	160,0	μA	5,5	GND	$I_O = 0$

* for HC, $V_{CC} = 6$ V.

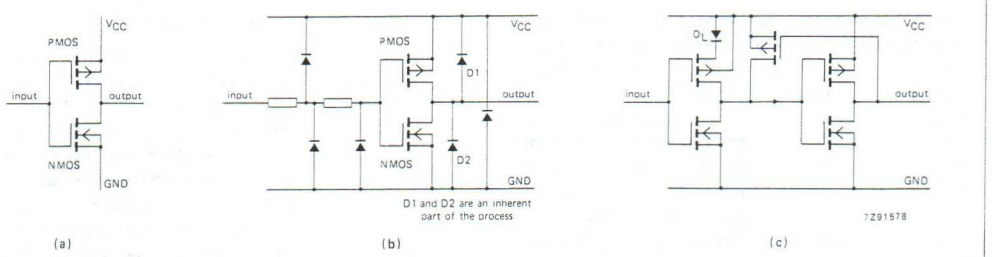


Fig.1 74HC inverter: (a) input structure of 74HC inverter; (b) 74HC inverter with protection circuitry; (c) input structure of 74HCT inverter

Another factor which influences quiescent power dissipation is the steady-state input voltage level which may slightly turn-on one of the input transistors shown in Fig.1(a) and yet not fully turn-off the other. This causes a small additional quiescent supply current (ΔI_{CC}) to flow between V_{CC} and GND. The level of ΔI_{CC} depends on the size of the input transistors and is different for each device.

In a system consisting entirely of 74HC ICs, the additional quiescent supply current ΔI_{CC} is so small that it can be omitted from practical power dissipation calculations. This is because 74HC outputs swing from GND to V_{CC}. The worst-case output levels with $|I_O| = 20\,\mu A$ are $V_{OL} = 0{,}1$ V max. and $V_{OH} = V_{CC} - 0{,}1$ V min., very close to GND and V_{CC} respectively. Figure 2(a) shows that ΔI_{CC} is negligible when these levels are applied to 74HC inputs because they always turn one of the input transistors fully off.

However, if 74HC input levels are held close to the switching threshold (typically $V_{CC}/2$), Fig.2 shows that the additional quiescent supply current (Δ_{CC}) becomes much greater than quiescent supply current I_{CC}. This occurs if the mistake is made of driving a 74HC input from a TTL output. With a minimum TTL V_{OH} of 2,4 V driving a 74HC input, not only will a logic "1" probably not be recognized, but several milliamps of (Δ_{CC}) will flow. To overcome this problem, an external pull-up resistor could be used as shown in Fig.3 but the resistor would dissipate significant power because its value would have to be low to maintain switching speed. 74HCT ICs have TTL input switching levels and should therefore be used instead of 74HC ICs whenever it is necessary to interface HCMOS with TTL logic.

Unlike 74HC ICs, 74HCT ICs can be substituted for LSTTL ICs and/or mixed with LSTTL, ALSTTL, ASTTL or FAST-TTL family ICs in the same system. Under some conditions, they may dissipate somewhat more quiescent power than 74HC ICs. For example, Fig.2(b) shows that a worst-case TTL V_{OL} of 0,5 V max. is close enough to GND

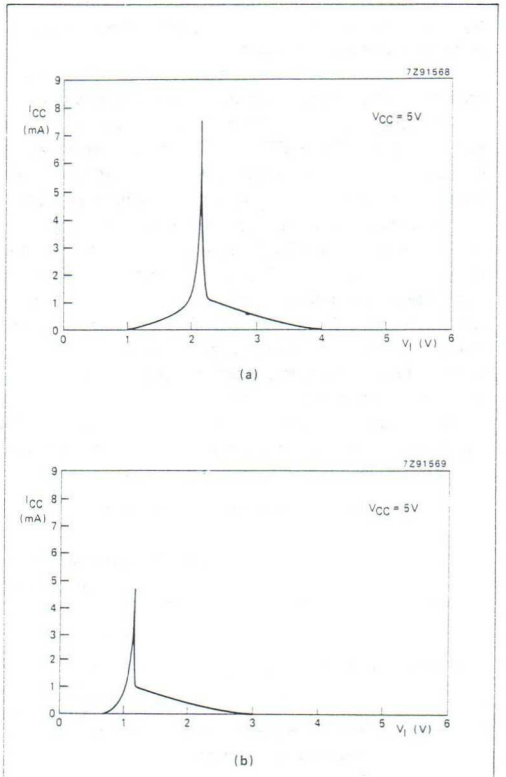


Fig.2 Supply current as a function of input voltage at V_{CC} = 5 V. (a) 74HC; (b) 74HCT

to turn the input NMOS transistor fully off so that ΔI_{CC} is close to zero. However, a worst-case TTL V_{OH} of 2,4 V min. causes some ΔI_{CC} to flow. For this reason, 74HCT data sheets specify I_{CC} at the worst-case input voltage of $V_{CC} - 2{,}1$ V for V_{CC} ranging from 4,5 V to 5,5 V. It is further specified on a per input pin basis to allow more accurate power dissipation calculations if all the functions within an IC are not being used, or are being driven by different input voltage levels.

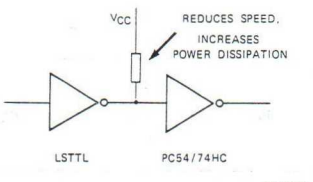


Fig.3 Using a pull-up resistor to interface 74HC ICs with LSTTL

Our proprietary 74HCT input structure shown in Fig.1(c) considerably reduces the additional quiescent supply current ΔI_{CC}. The structure is identical to that for 74HC circuits except for a level-shifting diode between the PMOS transistor and V_{CC}, and the connection of the substrate of the CMOS transistor to V_{CC}. The effect is to reduce the input level switching threshold to 28%V_{CC} instead of 50%V_{CC} as is the case with 74HC ICs. This therefore reduces the additional quiescent current ΔI_{CC} when a TTL minimum HIGH level of 2,4 V is applied to a 74HCT input by ensuring that the PMOS transistor is fully turned off. Figure 2(b) shows that ΔI_{CC} is negligible when a 74HCT input is held at a typical TTL HIGH output level (3,4 V) or LOW output level (0,25 V).

Calculating 74HC quiescent power dissipation

For power-critical applications such as battery-powered equipment, it may be necessary to calculate 74HC quiescent power dissipation as a standby value of battery drain. It is given by:

$$P_{QHC} = V_{CC} I_{CC} \qquad (1)$$

V_{CC} is dependent upon the particular application, we recommend that a ±10% variation be allowed. I_{CC} at $V_{CC\,max}$ is obtained from the data sheet for the particular IC. For critical battery-powered applications, the value of I_{CC} can be linearly derated for any desired V_{CC}; for example, at $V_{CC} = 2$ V, use one-third of the limits shown in Table 1 for 74HC ICs.

Calculating 74HCT quiescent power dissipation

Assume that an LSTTL IC with an output duty factor of 0,5 is switching one gate input in a 74HCT11 (triple 3-input AND gate) with a 5 V supply and an ambient temperature of 25 °C. Quiescent power dissipation is calculated from:

$$P_{QHCT} = V_{CC}(I_{CC} + \delta \Delta I_{CC}) \qquad (2)$$

where δ = switching duty factor.

$\Delta I_{CC\,max}$ is calculated on a unit-load basis from the part of the data sheet reproduced in Table 2:

$\Delta I_{CC\,max} = 360\,\mu$A per input pin x 1 pin x 0,5 unit-load coefficient = 180 μA.

Inserting this current and the values for V_{CC} (5,5 V), $I_{CC} = 2\,\mu$A from Table 2, and δ (0,5) into equation (2) gives:

$$P_{QHCT} = 5{,}5\text{ V } [2\,\mu\text{A} + (0{,}5 \times 180\,\mu\text{A})] = 506\,\mu\text{W}.$$

This is only 2% of the 25,5 mW maximum quiescent power that would be dissipated by the equivalent LSTTL IC. Furthermore, as previously stated, the ΔI_{CC} of 360 μA per input pin quoted in Table 2 for the 74HCT11 IC is based on a worst-case HIGH input level of $V_{CC} - 2{,}1$ V. In a typical application, the TTL HIGH input level driving the IC would be much higher than this, resulting in a reduction of ΔI_{CC} by an order of magnitude.

If all the inputs of a 74HCT IC are driven by 74HC or equivalent CMOS outputs, the input levels are such that the additional quiescent supply current ΔI_{CC} is so small that it can be omitted from 74HCT power dissipation calculations. 74HC quiescent power dissipation equation (1) can then be used to calculate 74HCT quiescent power dissipation.

DYNAMIC POWER DISSIPATION

Unlike quiescent power dissipation, dynamic power dissipation is calculated in the same manner for both 74HC and 74HCT ICs. All equations presented here for dynamic power dissipation are therefore applicable to both 74HC and 74HCT ICs.

Three factors influence the dynamic power dissipation of HCMOS ICs. They are load capacitance, internal capacitance and switching transient currents (through-currents of transistor pairs when both transistors momentarily conduct during logic level transitions).

TABLE 2
Specification of I_{CC}, ΔI_{CC} and unit load coefficient for 74HCT11 triple 3-input AND gate

symbol	parameter	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V	V_I	other
I_{CC}	quiescent supply current			2,0		20,0		40,0	μA	5,5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4,5 to 5,5	V_{CC} −2,1 V	other inputs at V_{CC} or GND: $I_O = 0$

Note:

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in table below.

input	unit load coefficient
nA, nB, nC	0,5

Load capacitance

The first contribution to dynamic power dissipation is caused by the charging and discharging of external capacitive loads. Figure 4 illustrates an HCMOS inverter with a capacitive load and, together with the following equations, will help to illustrate how load capacitance consumes power. The energy dissipated (joules) in charging and discharging the capacitive load is:

$$P_{CL}t = C_L V_{CC}^2 \quad (3)$$

where $t = 1/f_o$ and C_L = total external load capacitance due to interconnections, driven inputs and any sockets that are used.

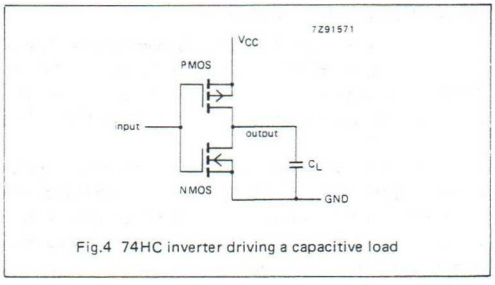


Fig.4 74HC inverter driving a capacitive load

The dynamic power dissipation due to capacitive loads is therefore:

$$P_{CL} = C_L V_{CC}^2 f_o \quad (4)$$

Equation (4) is only applicable if all the outputs are switching the same load. If they are not, the equation becomes:

$$P_{CL} = \Sigma(C_L V_{CC}^2 f_o) \quad (5)$$

For multiple output ICs, it is important to calculate with the appropriate output frequency. For example, at either output from a flip-flop, $f_o = f_i/2$; for a 7-stage binary ripple counter (type 74HC/HCT4024), f_o is halved for each successive output stage so that $f_o = f_i/64$ for the final output stage.

Internal capacitance

All MOS logic ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminium and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the circuit.

HCMOS ICs are manufactured with a self-aligned polysilicon gate process (3 μm gate length) and local oxidation to reduce internal capacitance by minimising gate-to-source

and gate-to-drain capacitances. The junction capacitances, which are proportional to junction area, are smaller than those in HE4000B CMOS ICs because the diffusions are shallower. Figure 5 shows the location of the capacitances in a 74HC inverter.

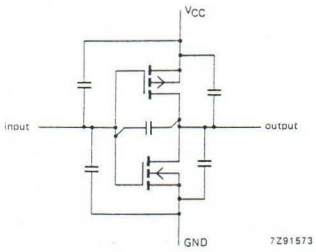


Fig.5 Location of capacitances in a 74HC inverter

For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance C_{PD}. It is defined in the data sheet for each HCMOS IC on a 'per function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within an IC. This allows more accurate power dissipation calculations to be made if logic functions within the same IC are operating at different frequencies.

The published figure for C_{PD} is valid for the worst-case operating mode under typical operating conditions. For example, in the case of a NAND gate, the state of the inputs is assumed to be such that the output is changing state; for a shift register or D-type flip-flop, it is assumed that alternately HIGH/LOW data is being clocked in. The specified value for C_{PD} however is a typical one; nevertheless, some protection will already be built-in to dynamic power dissipation calculations because the assumed worst-case operating modes don't always occur. Although we're not yet prepared to officially publish a maximum value for C_{PD}, a rough guide would be to increase the published figure by 50% for worst-case calculations. The method of measuring C_{PD} is explained in the chapter "User Guide".

Switching transient currents

The final factor that contributes to the dynamic power dissipation of HCMOS is internal switching transient currents. When the output of a basic HCMOS inverter as shown in Fig.6(a) changes state, either from a logic "1" to a logic "0" or vice-versa, there is a brief period during which both transistors conduct. This creates a temporary low-resistance path between V_{CC} and GND as shown in Fig.6(b). In this transistory state, additional supply current (ΔI_{CC}) flows and power is dissipated, so input rise and fall times should be kept short. The average value of this transient current increases linearly with increasing switching frequency. In other words, power dissipation due to switching (like power dissipation due to internal capacitance) increases linearly with increasing switching frequency. However, since it is small compared to the power dissipation due to internal capacitance, its effect is included in the published value of power dissipation capacitance (C_{PD}) which has discussed under the previous heading.

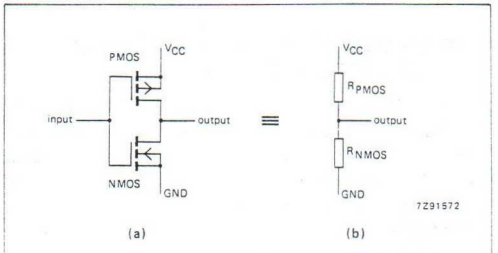


Fig.6 When an HCMOS inverter changes state, both input transistors momentarily conduct: (a) inverter input structure; (b) equivalent circuit when the input level is between logic levels

Total dynamic power dissipation

Since C_{PD} represents the load imposed by both internal capacitance and switching transient currents, the total dynamic power dissipation due to these factors is:

$$P_{DYN} = C_{PD} V_{CC}^2 f_i \quad (6)$$

The total dynamic power dissipation of HCMOS ICs is obtained by adding equation (6) to the power dissipation due to the total external capacitive load (equation 5) and is given by:

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \quad (7)$$

CALCULATING TOTAL POWER DISSIPATION FOR 74HC AND 74HCT ICs

Total HCMOS power dissipation is a summation of the appropriate quiescent and dynamic power dissipation formulae previously described.

For 74HC/HCT ICs driven by CMOS levels:

$$P_{tot} = V_{CC} I_{CC} + C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \quad (8)$$

For 74HCT ICs driven by TTL:

$$P_{tot} = V_{CC} (I_{CC} + \delta \Delta I_{CC}) + C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \quad (9)$$

POWER DISSIPATION IN OSCILLATORS AND ONE-SHOTS

The information presented so far is only valid for ICs switching rapidly between logic levels. Additional quiescent supply current ΔI_{CC} is greater for one-shots, oscillators and gates arranged as oscillators because, in these applications, the input slowly passes through the switching threshold (typically 50%V_{CC} for 74HC ICs and 28%V_{CC} for 74HCT ICs) causing flow-through current as shown in Fig.2.

POWER DISSIPATION COMPARISON BETWEEN HCMOS, LSTTL AND ALSTTL

In any IC, there is a balance between speed and power dissipation. LSTTL logic is relatively fast but the quiescent power dissipated by its bipolar circuitry is considerable. ALSTTL improves upon LSTTL by using advanced wafer fabrication techniques and smaller geometries. These improvements increase speed and approximately halve the quiescent power dissipation.

CMOS ICs dissipate negligible quiescent power compared with all bipolar TTL logic ICs but, until the development of the HCMOS family, CMOS ICs were relatively slow. Use of advanced wafer fabrication techniques and smaller geometries has now made it possible for HCMOS to match the speed of LSTTL and yet retain the substantial power savings afforded by CMOS. Figure 7 shows the speed-power products for today's most popular logic IC technologies.

Figures 8 and 9 compare the dynamic power dissipation of SSI and MSI for 74HC, and LSTTL ICs. These graphs show that 74HC ICs maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL ICs is caused by the many bipolar transistors that continuously conduct.

Figures 8 and 9 also show that, as device complexity increases, the frequency at which HCMOS ICs dissipate the same amount of power as LSTTL ICs also increases. This is because, as LSTTL complexity increases, there are more resistive paths between V_{CC} and GND which carry more quiescent bias current and thus cause more quiescent power dissipation. HCMOS ICs also dissipate more quiescent power as their complexity increases, but the leakage currents which cause it are so small that it can be ignored.

The power dissipation of the different logic IC technologies is translated into total system power as a function of frequency in Fig.10 which is for a small system consisting of one gate and two flip-flops. The graph shows that HCMOS also dissipates substantially less power than LSTTL at the system level.

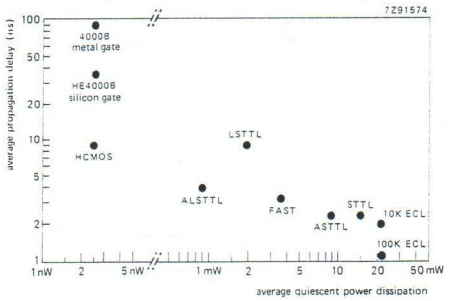


Fig.7 Speed/power products for the most popular logic IC technologies

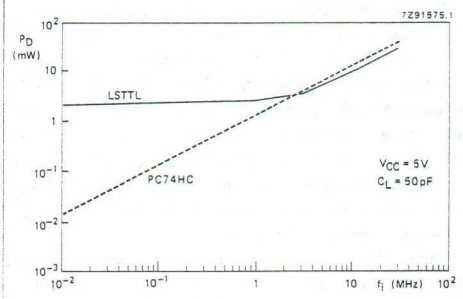


Fig.8 Total power dissipation as a function of switching frequency for gates

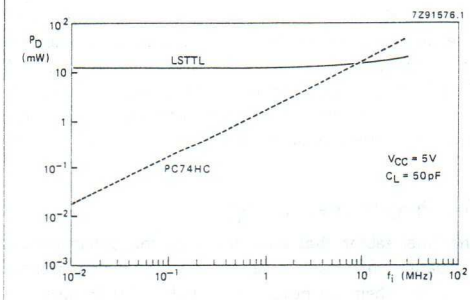


Fig.9 Total power dissipation as a function of frequency for a dual flip-flop with one of the flip-flops toggling

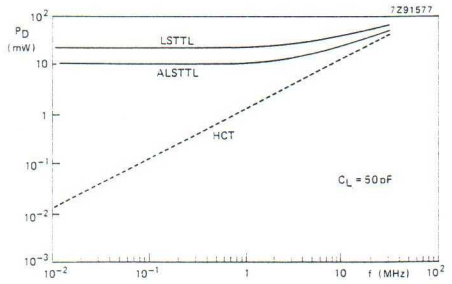


Fig.10 Total power dissipation as a function of frequency for a small system comprising one gate and two flip-flops

INFLUENCE OF HCMOS ICs ON APPLICATIONS

The significantly lower power dissipation in an HCMOS logic system, compared with its LSTTL or ALSTTL equivalent, is *the* primary reason why HCMOS ICs should be used for new system designs and to replace LSTTL or ALSTTL ICs in many existing designs where power consumption and/or dissipation is a problem.

For new designs, HCMOS is the only suitable family of logic ICs for battery-powered portable personal computers. The use of HCMOS is *the* major trend in personal computers using all CMOS microprocessors, RAMs, ROMs, and peripherals. All CMOS designs can be powered-down to 2 V standby to extend battery life.

For non-portable equipment, the use of HCMOS logic and CMOS LSI is also preferred because it not only reduces power dissipation, but also significantly reduces, in order of priority, cost, size, and weight. Cost reductions stem from major reductions of power supply current and regulation, cooling fans, heatsinks, and copper buses.

An equally powerful motivating force for using HCMOS logic ICs with their lower power dissipation is the inherent and proven increase of component and equipment reliability. Equipment life is considerably extended because IC junction temperatures are much reduced and other components are exposed to lower ambient temperatures.

Package Information

PART NUMBER	PIN COUNT	DIL	SO	SSOP	TSSOP
74HC/HCT00	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT02	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT03	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT04	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCTU04	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT08	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT10	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT11	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT14	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT20	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT21	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT27	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT30	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT32	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT42	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC58	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT73	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT74	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT75	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT85	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT86	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT93	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT107	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT109	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT112	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT123	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT125	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT126	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT132	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT133	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT137	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT138	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT139	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT147	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT151	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT153	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT154	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT154N3	24	SOT222-1			

Package Information

PART NUMBER	PIN COUNT	DIL	SO	SSOP	TSSOP
74HC/HCT157	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT158	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT160	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT161	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT162	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT163	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT164	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT165	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT166	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT173	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT174	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT175	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT181	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT181N3	24	SOT222-1			
74HC/HCT182	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT190	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT191	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT192	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT193	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT194	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT195	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT221	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT237	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT238	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT240	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT241	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT242	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT243	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT244	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT245	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT251	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT253	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT257	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT258	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT259	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT273	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT280	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT283	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1

Package Information

PART NUMBER	PIN COUNT	DIL	SO	SSOP	TSSOP
74HC/HCT297	16	SOT38-4	SOT162-1		
74HC/HCT299	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT354	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT356	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT365	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT366	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT367	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT368	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT373	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT374	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT377	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT390	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT393	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT423	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT533	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT534	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT540	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT541	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT563	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT564	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT573	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT574	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT583	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT594	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT595	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT597	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT640	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT643	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT646	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT646N3	24	SOT222-1			
74HC/HCT648	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT648N3	24	SOT222-1			
74HC/HCT652	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT670	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT688	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HCT1284	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT4002	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT4015	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1

Package Information

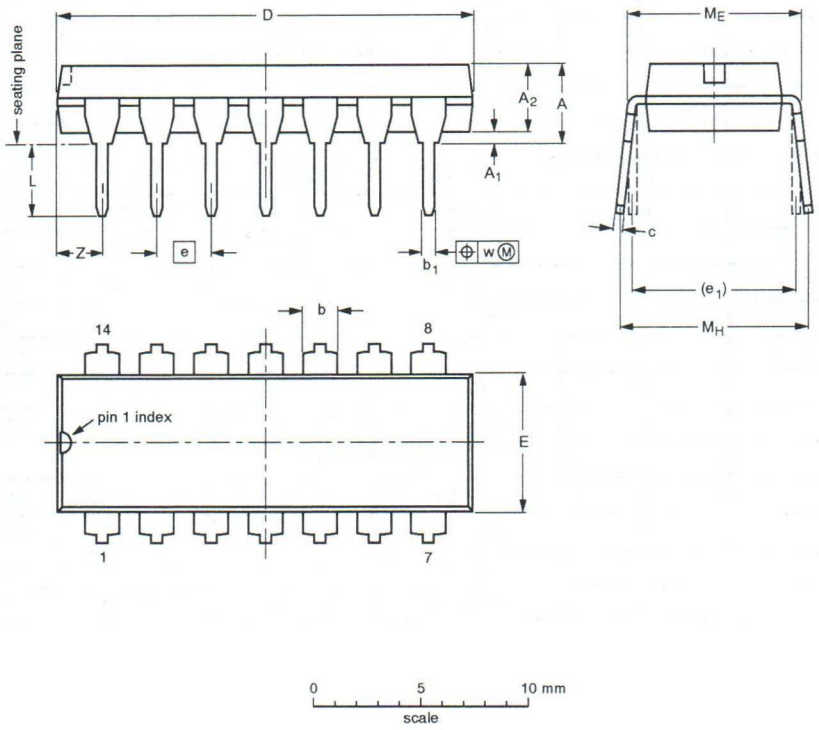
PART NUMBER	PIN COUNT	DIL	SO	SSOP	TSSOP
74HC/HCT4016	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT4017	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4020	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4024	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT4040	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4046A	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC4049	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC4050	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4051	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4052	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4053	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4059	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT4059N3	24	SOT222-1			
74HC/HCT4060	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4066	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT4067	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT4067N3	24	SOT222-1			
74HC/HCT4075	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT4094	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4316	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4351	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT4352	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT4353	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT4510	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4511	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4514	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT4514	24	SOT222-1			
74HC/HCT4515	24	SOT101-1	SOT137-1	SOT340-1	SOT355-1
74HC/HCT4515	24	SOT222-1			
74HC/HCT4516	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4518	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4520	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4538	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT4543	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT5555	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT6323A	8		SOT96-1		
74HC/HCT7014	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT7030	28	SOT117-1	SOT136-1		

Package Information

PART NUMBER	PIN COUNT	DIL	SO	SSOP	TSSOP
74HC/HCT7046A	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT7080	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT7132	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT7245	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT7266	14	SOT27-1	SOT108-1	SOT337-1	SOT402-1
74HC/HCT7403	16	SOT38-4	SOT162-1		
74HC/HCT7404	18	SOT102-1			
74HC/HCT7404	20		SOT163-1		
74HC/HCT7540	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT7541	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT7597	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT7731	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT9014	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT9015	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT9046A	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT9114	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT9115	20	SOT146-1	SOT163-1	SOT339-1	SOT360-1
74HC/HCT9323A	8		SOT96-1		
74HC/HCT40102	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT40103	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT40104	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1
74HC/HCT40105	16	SOT38-4	SOT109-1	SOT338-1	SOT403-1

Package Outline Drawings

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

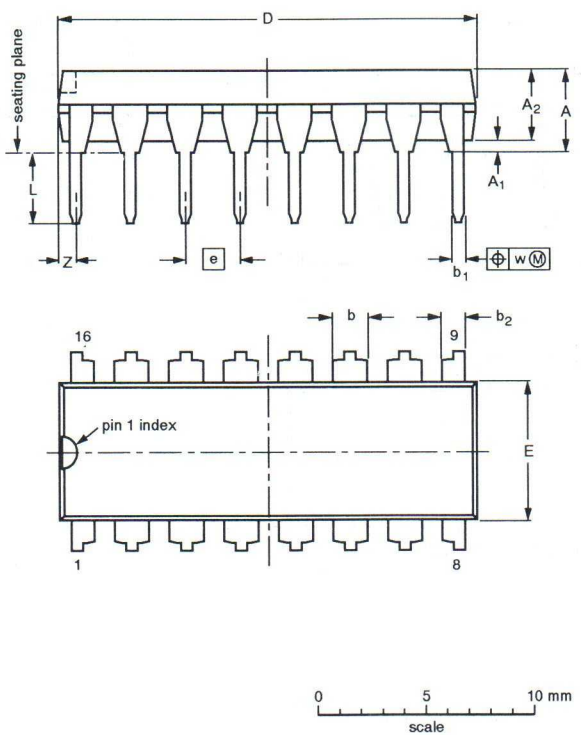
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package Outline Drawings

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

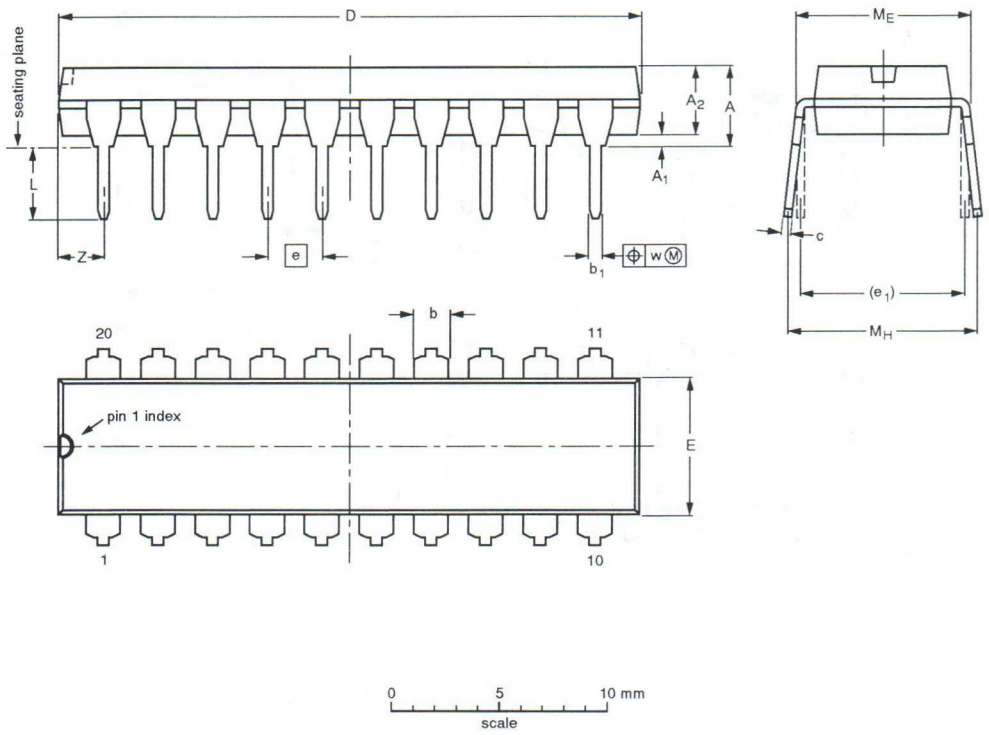
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package Outline Drawings

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

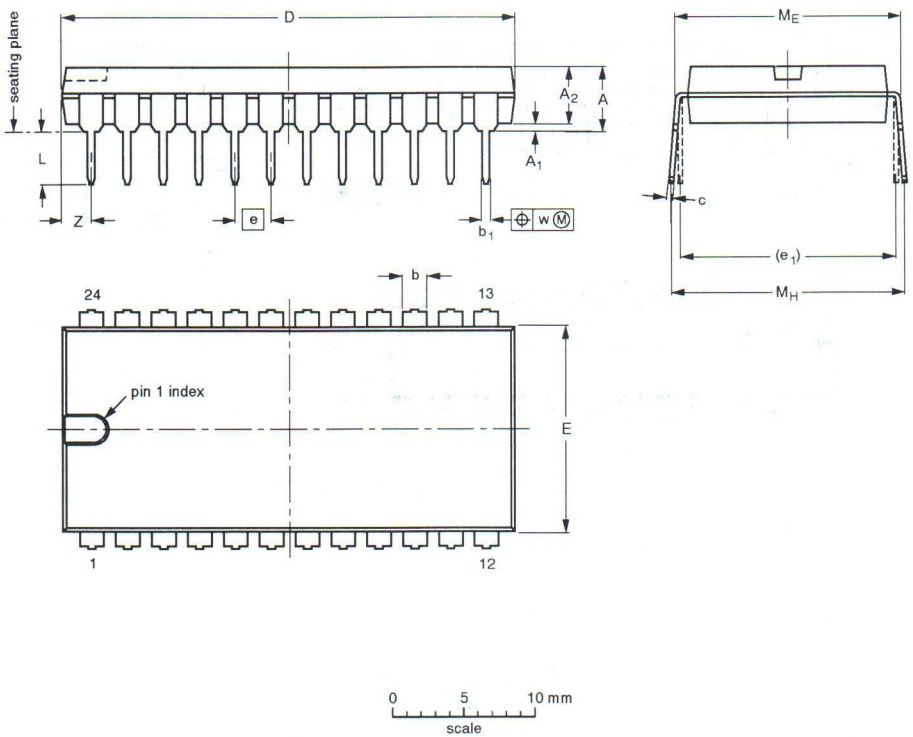
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package Outline Drawings

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

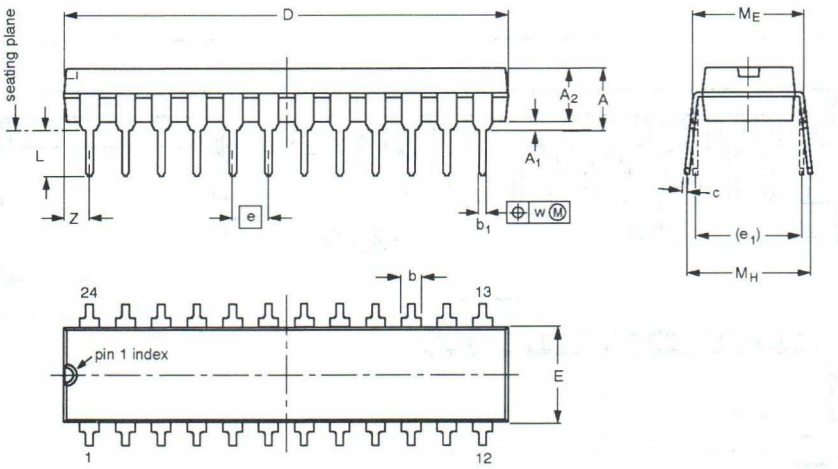
Note

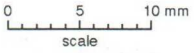
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

Package Outline Drawings

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

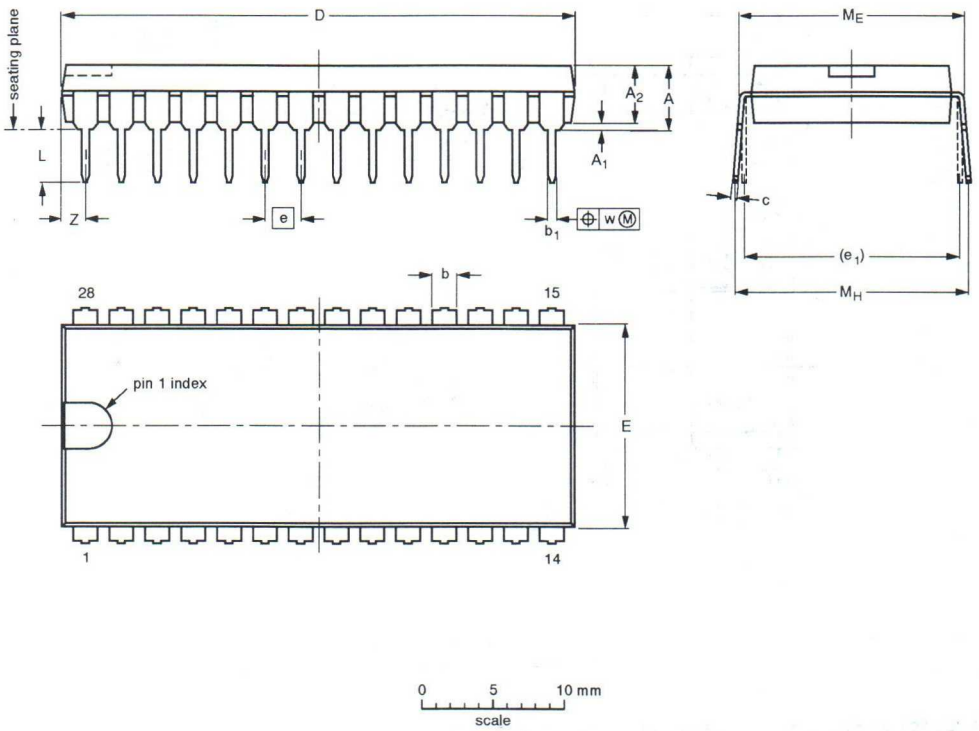
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package Outline Drawings

DIP28: plastic dual in-line package; 28 leads (600 mil) SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

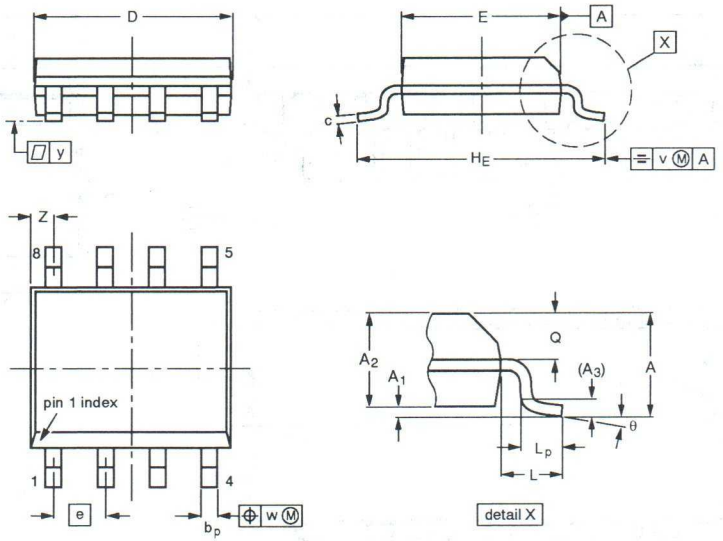
Note

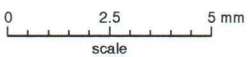
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

Package Outline Drawings

SO8: plastic small outline package; 8 leads; body width 3.9mm — SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

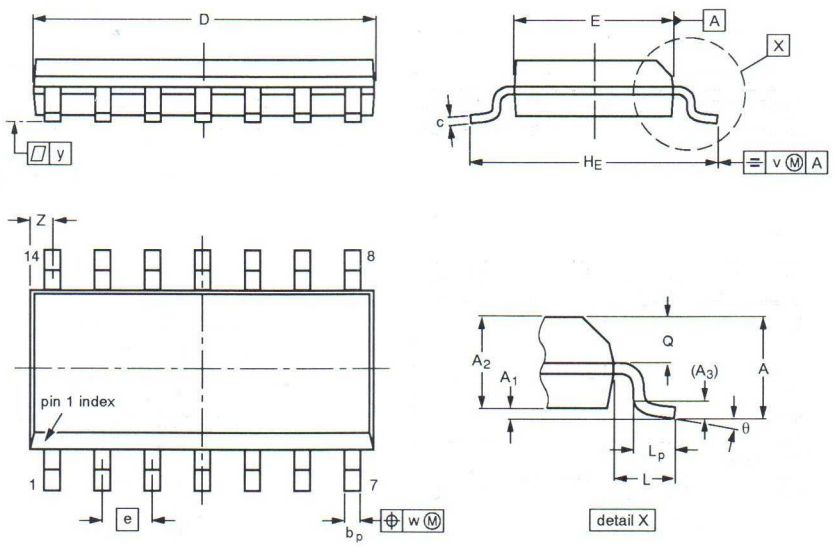
Notes

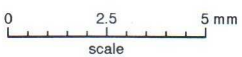
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

Package Outline Drawings

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

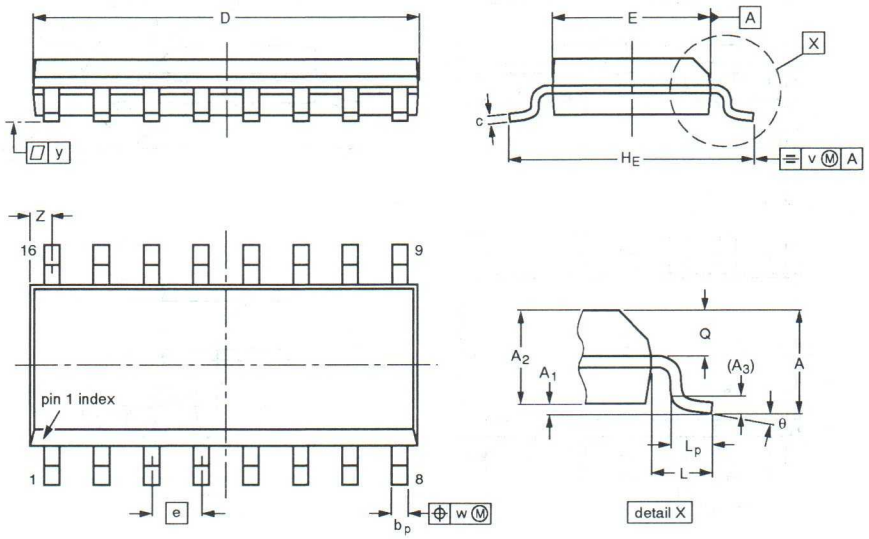
Note

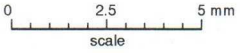
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

Package Outline Drawings

SO16: plastic small outline package; 16 leads; body width 3.9 mm — SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

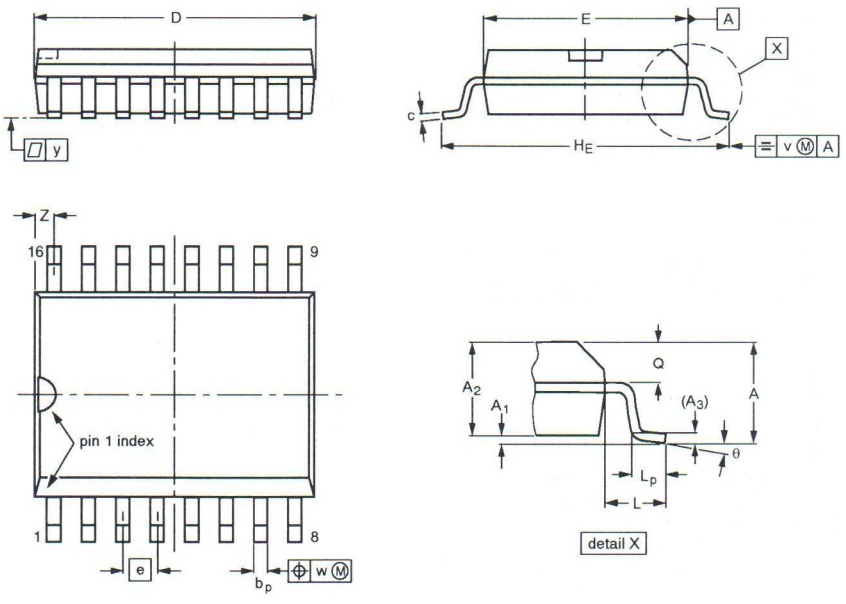
Note

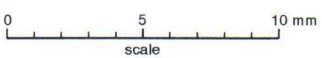
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

Package Outline Drawings

SO16: plastic small outline package; 16 leads; body width 7.5 mm — SOT162-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

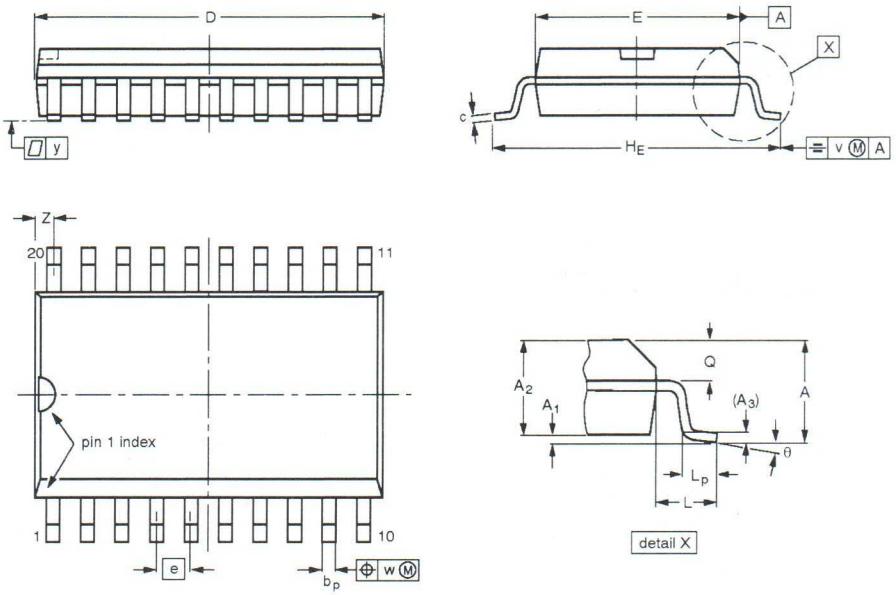
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

Package Outline Drawings

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

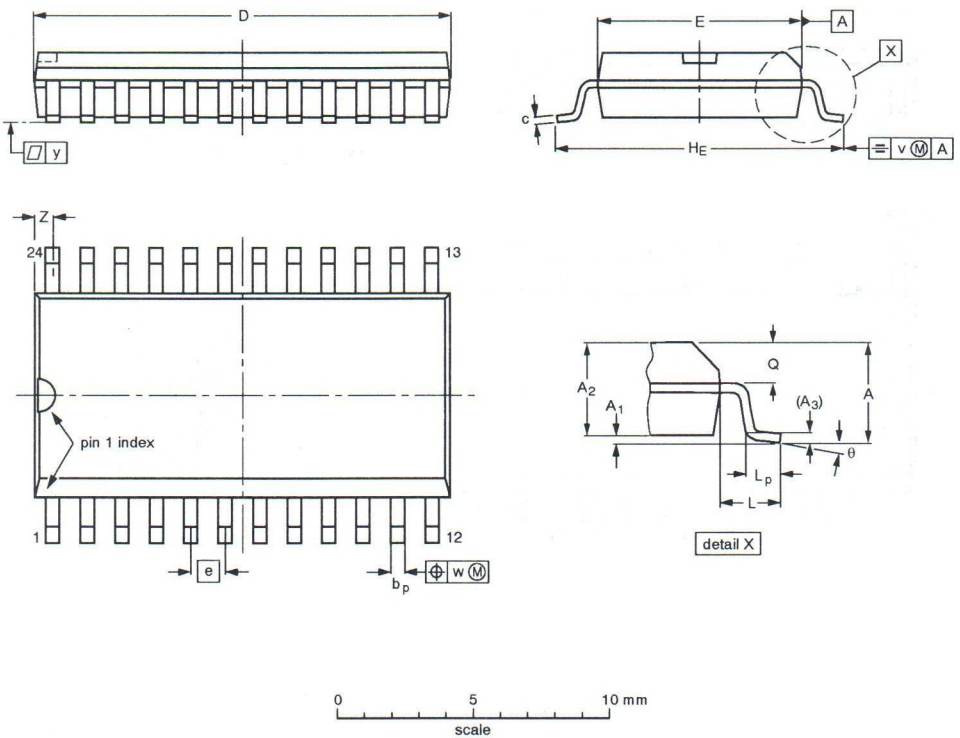
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

Package Outline Drawings

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

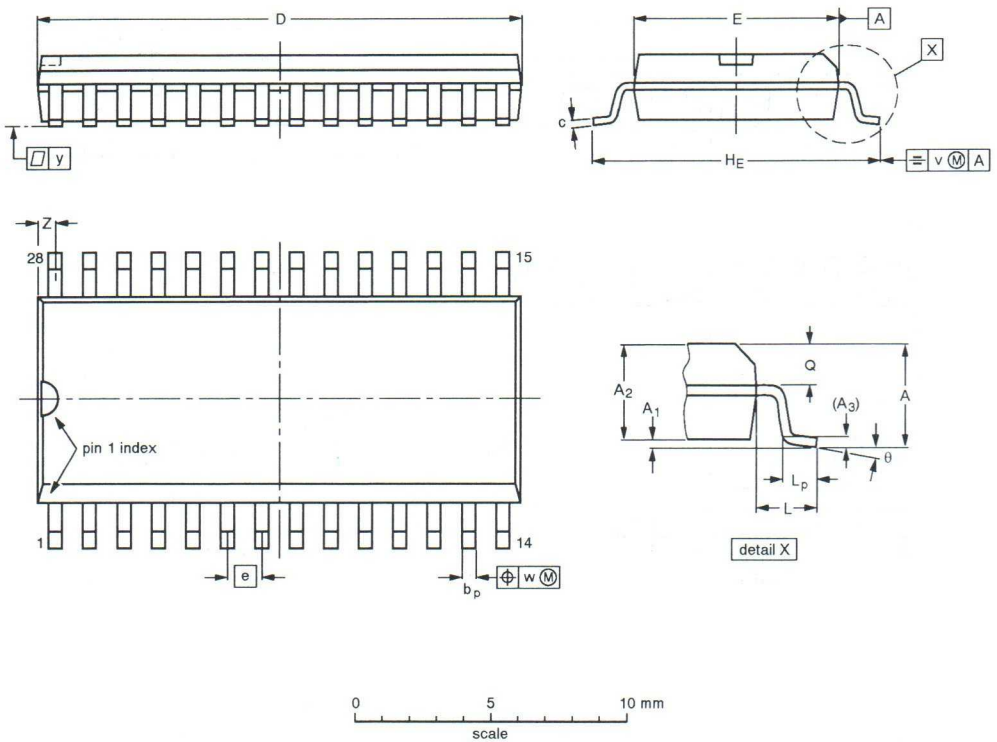
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

Package Outline Drawings

SO28: plastic small outline package; 28 leads; body width 7.5mm — SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

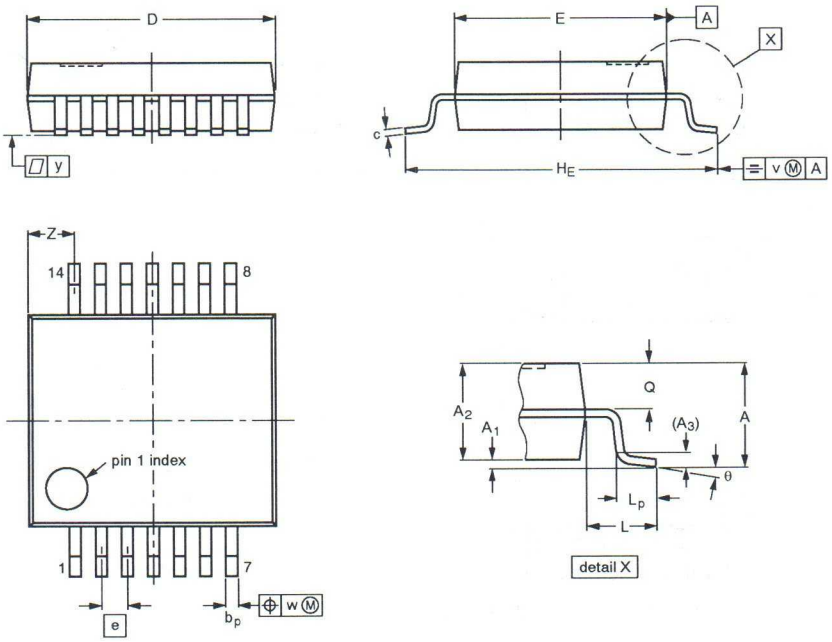
Note

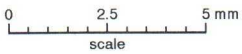
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

Package Outline Drawings

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm — SOT337-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

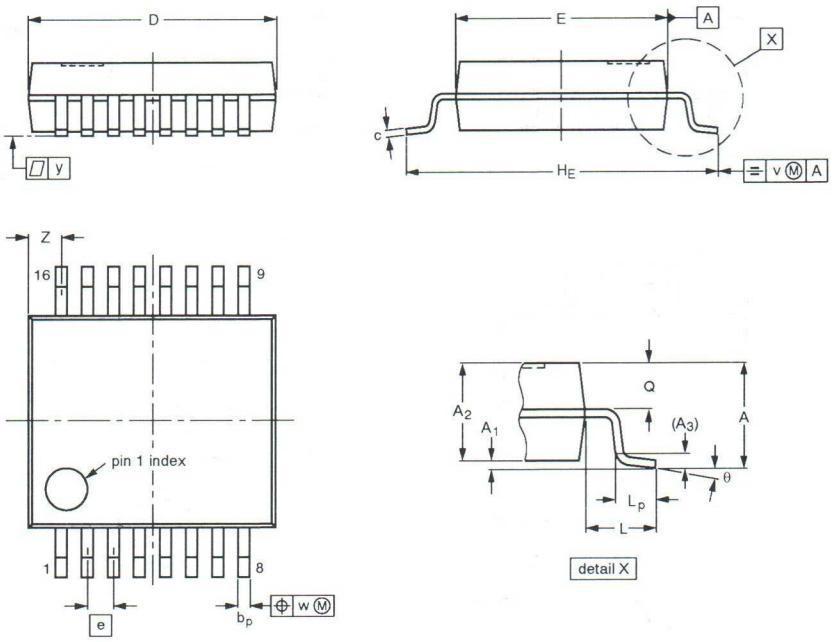
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~94-01-14~~ 95-02-04

Package Outline Drawings

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm — SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

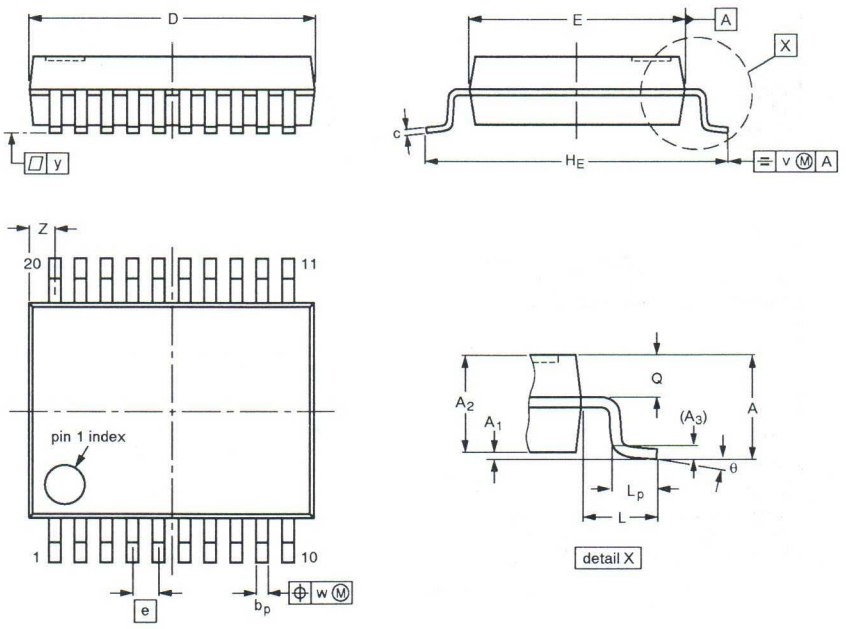
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

Package Outline Drawings

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm — SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

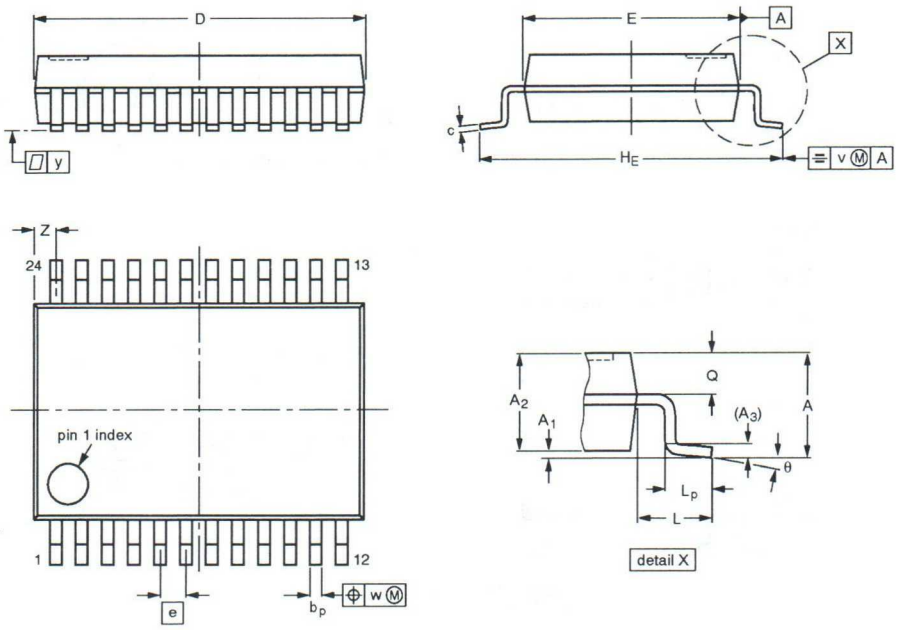
Note

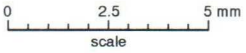
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

Package Outline Drawings

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm — SOT340-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

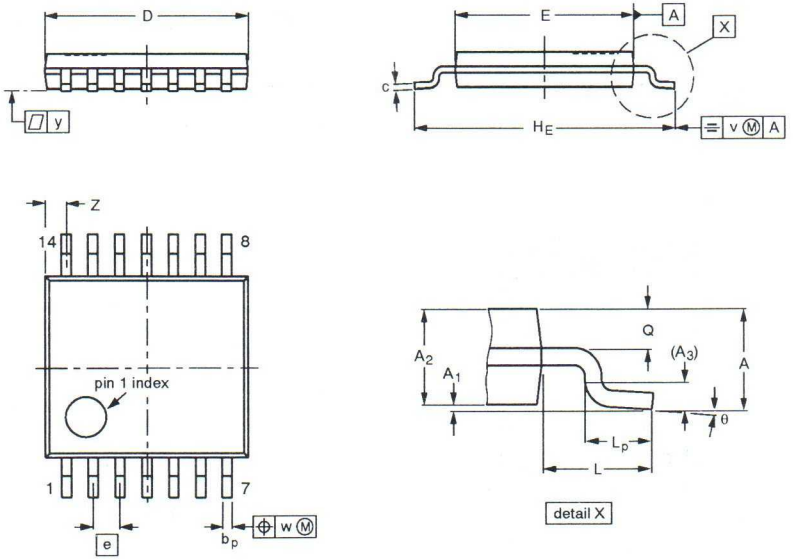
Note

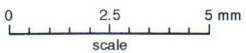
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Package Outline Drawings

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm — SOT402-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

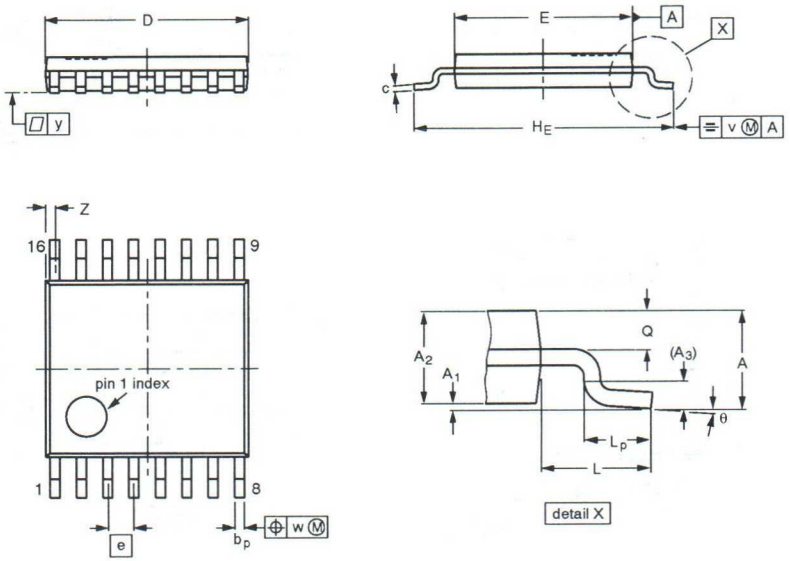
Notes

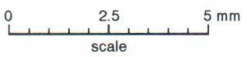
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

Package Outline Drawings

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm — SOT403-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

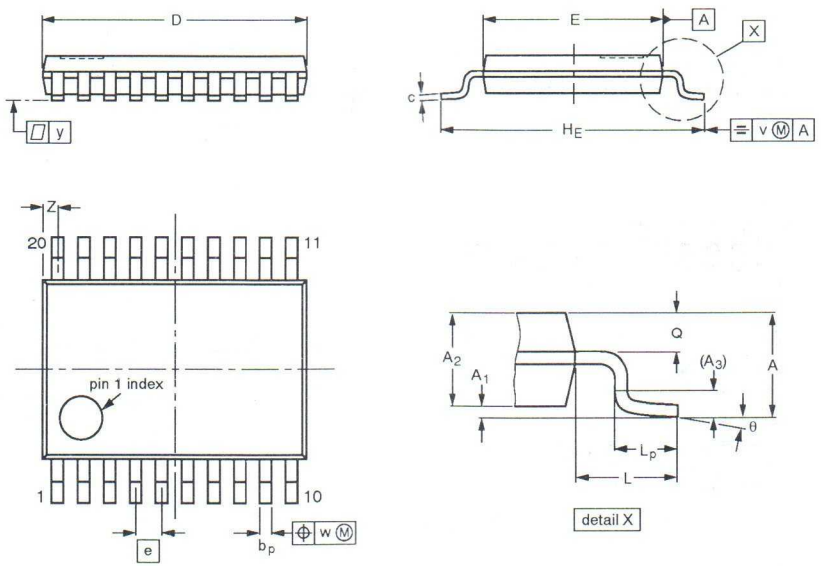
Notes

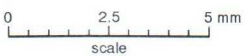
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Package Outline Drawings

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm — SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

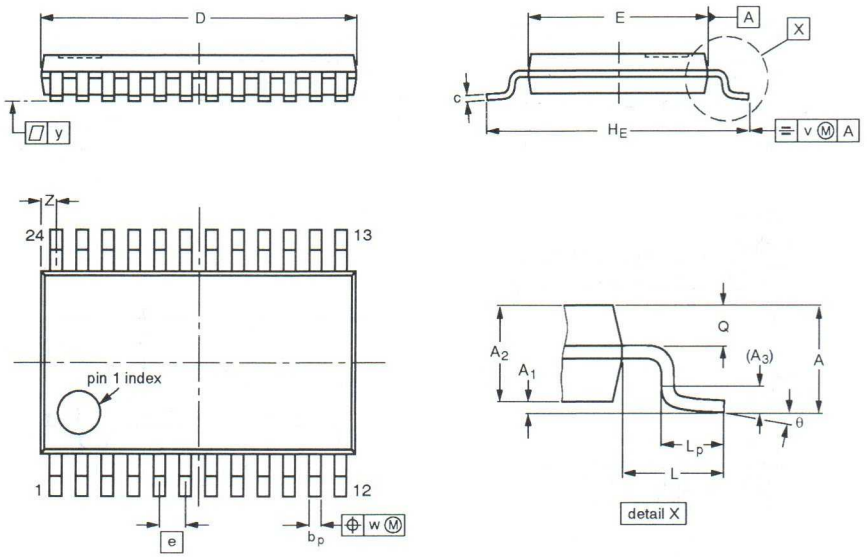
Notes

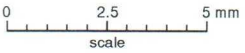
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Package Outline Drawings

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm — SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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