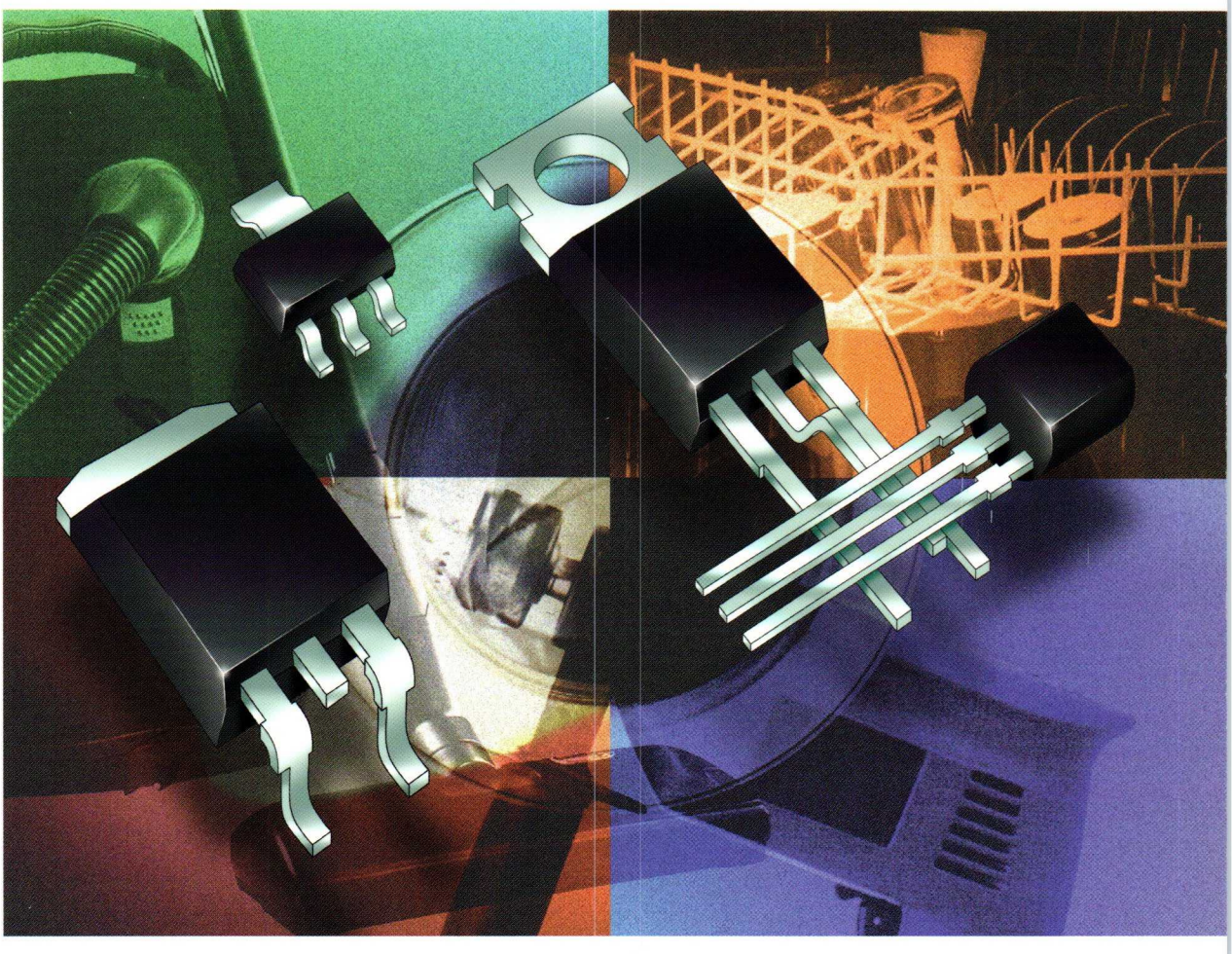
DISCRETE SEMICONDUCTORS

# Power Thyristors and Triacs



1998

Data Handbook SC03

Philips Semiconductors

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PHILIPS

## QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

## PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

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## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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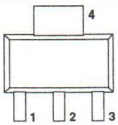
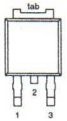
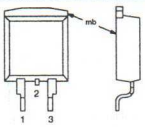
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| Internet WWW home page | 33 |

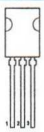
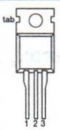
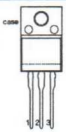
## SILICON BIDIRECTIONAL TRIGGER DEVICES

| $I_{FRM}$ | $V_{(BO)}$ | $I_{(BO)}$ |  SOD27 (DO35) |
|---|---|---|---|
| A | V | μA | |
| 2 | 28 - 36 | 50 | BR100/03 |

**THYRISTORS - Surface Mount Packages**

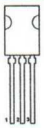
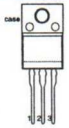
| $I_{T(RMS)}$ | $V_{DRM}$, $V_{RRM}$ | $I_{GT}$ (max) |  SOT223 |  SOT428 (TO252) |  SOT404 (TO263) |
|---|---|---|---|---|---|
| A | V | µA | | | |
| 1 | 200<br>400<br>500<br>600 | 20-200 | BT168BW<br>BT168DW<br>BT168EW<br>BT168GW | | |
| 1 | 200<br>400<br>500<br>600 | 200 | BT169BW<br>BT169DW<br>BT169EW<br>BT169GW | | |
| 1 | 400<br>500<br>600 | 200 | BT148W-400R<br>BT148W-500R<br>BT148W-600R | | |
| 4 | 600<br>600 | 200 | | BT148MZ-600R<br>BT148SZ-600R | |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 200 | | BT150M-500R<br>BT150M-600R<br>BT150M-800R<br>BT150S-500R<br>BT150S-600R<br>BT150S-800R | |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 200 | | BT258M-500R<br>BT258M-600R<br>BT258M-800R<br>BT258S-500R<br>BT258S-600R<br>BT258S-800R | BT258B-500R<br>BT258B-600R<br>BT258B-800R |
| A | V | mA | | | |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 15 | | BT300M-500R<br>BT300M-600R<br>BT300M-800R<br>BT300S-500R<br>BT300S-600R<br>BT300S-800R | BT300B-500R<br>BT300B-600R<br>BT300B-800R |
| 12 | 500<br>650<br>800<br>500<br>650<br>800 | 15 | | BT151M-500R<br>BT151M-650R<br>BT151M-800R<br>BT151S-500R<br>BT151S-650R<br>BT151S-800R | BT151B-500R<br>BT151B-650R<br>BT151B-800R |
| 20 | 400<br>600<br>800 | 32 | | | BT152B-400R<br>BT152B-600R<br>BT152B-800R |

**THYRISTORS - Leaded Packages**

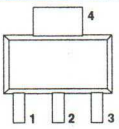
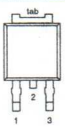
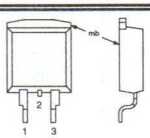
| $I_{T(RMS)}$ | $V_{DRM}$, $V_{RRM}$ | $I_{GT}$ (max) |  SOT54 (TO92) |  SOT82 |  SOT78 (TO220AB) |  SOT186A |
|---|---|---|---|---|---|---|
| A | V | µA | | | | |
| 0.8 | 200<br>400<br>500<br>600 | 200 | BT149B<br>BT149D<br>BT149E<br>BT149G | | | |
| 0.8 | 200<br>400<br>500<br>600 | 20-200 | BT168B<br>BT168D<br>BT168E<br>BT168G | | | |
| 0.8 | 200<br>400<br>500<br>600 | 200 | BT169B<br>BT169D<br>BT169E<br>BT169G | | | |
| 0.8 | 200 | 200 | 2N5064 | | | |
| 4 | 400<br>500<br>600 | 200 | | BT148-400R<br>BT148-500R<br>BT148-600R | | |
| 4 | 500<br>600<br>800 | 200 | | | BT150-500R<br>BT150-600R<br>BT150-800R | |
| 8 | 500<br>600<br>800 | 200 | | | BT258-500R<br>BT258-600R<br>BT258-800R | BT258X-500R<br>BT258X-600R<br>BT258X-800R |

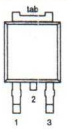
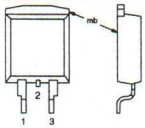
# Power Thyristors and Triacs

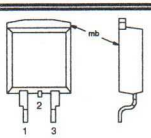


| $I_{T(RMS)}$ | $V_{DRM}$, $V_{RRM}$ | $I_{GT}$ (max) |  SOT82 |  SOT78 (TO220AB) |  SOT186A |
|---|---|---|---|---|---|
| A | V | mA | | | |
| 8 | 500<br>600<br>800 | 15 | | BT300-500R<br>BT300-600R<br>BT300-800R | BT300X-500R<br>BT300X-600R<br>BT300X-800R |
| 9 | 500<br>650<br>800 | 15 | | | BT151X-500R<br>BT151X-650R<br>BT151X-800R |
| 12 | 500<br>650<br>800 | 4 | BTA151-500R<br>BTA151-650R<br>BTA151-800R | | |
| 12 | 500<br>650<br>800 | 15 | | BT151-500R<br>BT151-650R<br>BT151-800R | |
| 20 | 400<br>600<br>800 | 32 | | BT152-400R<br>BT152-600R<br>BT152-800R | BT152X-400R<br>BT152X-600R<br>BT152X-800R |
| 25 | 500<br>600<br>800 | 35 | | BT145-500R<br>BT145-600R<br>BT145-800R | |

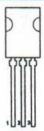
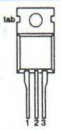
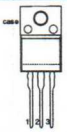
**FOUR QUADRANT TRIACS - Surface Mount Packages**

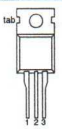
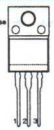
| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: | |  |  |  |
|---|---|---|---|---|---|---|
| | | (i), (ii), (iii) | (iv) | SOT223 | SOT428 (TO252) | SOT404 (TO263) |
| A | V | mA | mA | | | |
| 1 | 500<br>600 | 5 | 10 | BT134W-500D<br>BT134W-600D | | |
| 1 | 500<br>600 | 10 | 25 | BT134W-500E<br>BT134W-600E | | |
| 1 | 500<br>600 | 25 | 70 | BT134W-500F<br>BT134W-600F<br>BT134W-800F | | |
| 1 | 500<br>600<br>800 | 35 | 70 | BT134W-500<br>BT134W-600<br>BT134W-800 | | |
| 1 | 500<br>600<br>800 | 50 | 100 | BT134W-500G<br>BT134W-600G<br>BT134W-800G | | |
| 4 | 500<br>600<br>500<br>600 | 5 | 10 | | BT136M-500D<br>BT136M-600D<br>BT136S-500D<br>BT136S-600D | BT136B-500D<br>BT136B-600D |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 10 | 25 | | BT136M-500E<br>BT136M-600E<br>BT136M-800E<br>BT136S-500E<br>BT136S-600E<br>BT136S-800E | BT136B-500E<br>BT136B-600E<br>BT136B-800E |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 25 | 70 | | BT136M-500F<br>BT136M-600F<br>BT136M-800F<br>BT136S-500F<br>BT136S-600F<br>BT136S-800F | BT136B-500F<br>BT136B-600F<br>BT136B-800F |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 35 | 70 | | BT136M-500<br>BT136M-600<br>BT136M-800<br>BT136S-500<br>BT136S-600<br>BT136S-800 | BT136B-500<br>BT136B-600<br>BT136B-800 |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 50 | 100 | | BT136M-500G<br>BT136M-600G<br>BT136M-800G<br>BT136S-500G<br>BT136S-600G<br>BT136S-800G | BT136B-500G<br>BT136B-600G<br>BT136B-800G |

| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: | |  |  |
|---|---|---|---|---|---|
| | | (i), (ii), (iii) | (iv) | SOT428 (TO252) | SOT404 (TO263) |
| A | V | mA | mA | | |
| 8 | 500<br>600<br>500<br>600 | 5 | 10 | BT137M-500D<br>BT137M-600D<br>BT137S-500D<br>BT137S-600D | BT137B-500D<br>BT137B-600D |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 10 | 25 | BT137M-500E<br>BT137M-600E<br>BT137M-800E<br>BT137S-500E<br>BT137S-600E<br>BT137S-800E | BT137B-500E<br>BT137B-600E<br>BT137B-800E |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 25 | 70 | BT137M-500F<br>BT137M-600F<br>BT137M-800F<br>BT137S-500F<br>BT137S-600F<br>BT137S-800F | BT137B-500F<br>BT137B-600F<br>BT137B-800F |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 35 | 70 | BT137M-500<br>BT137M-600<br>BT137M-800<br>BT137S-500<br>BT137S-600<br>BT137S-800 | BT137B-500<br>BT137B-600<br>BT137B-800 |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 50 | 100 | BT137M-500G<br>BT137M-600G<br>BT137M-800G<br>BT137S-500G<br>BT137S-600G<br>BT137S-800G | BT137B-500G<br>BT137B-600G<br>BT137B-800G |

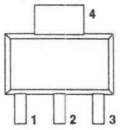
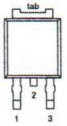
| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: | |   |
|---|---|---|---|---|
| | | (i), (ii), (iii) | (iv) | SOT404 (TO263) |
| A | V | mA | mA | |
| 12 | 500<br>600<br>800 | 10 | 25 | BT138B-500E<br>BT138B-600E<br>BT138B-800E |
| 12 | 500<br>600<br>800 | 25 | 70 | BT138B-500F<br>BT138B-600F<br>BT138B-800F |
| 12 | 500<br>600<br>800 | 35 | 70 | BT138B-500<br>BT138B-600<br>BT138B-800 |
| 12 | 500<br>600<br>800 | 50 | 100 | BT138B-500G<br>BT138B-600G<br>BT138B-800G |
| 16 | 500<br>600<br>800 | 10 | 25 | BT139B-500E<br>BT139B-600E<br>BT139B-800E |
| 16 | 500<br>600<br>800 | 25 | 70 | BT139B-500F<br>BT139B-600F<br>BT139B-800F |
| 16 | 500<br>600<br>800 | 35 | 70 | BT139B-500<br>BT139B-600<br>BT139B-800 |
| 16 | 500<br>600<br>800 | 50 | 100 | BT139B-500G<br>BT139B-600G<br>BT139B-800G |
| 16 | 500<br>600<br>800 | 10-50 | 10-100 | BT139B-500H<br>BT139B-600H<br>BT139B-800H |
| 25 | 500<br>600<br>800 | 35 | 70 | BTA140B-500<br>BTA140B-600<br>BTA140B-800 |

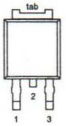
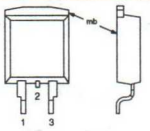
**FOUR QUADRANT TRIACS - Leaded Packages**

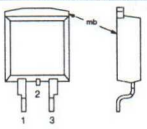
| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: | |  |  |  |  |
|---|---|---|---|---|---|---|---|
| | | (i), (ii), (iii) | (iv) | SOT54 (TO92) | SOT82 | SOT78 (TO220AB) | SOT186A |
| A | V | mA | mA | | | | |
| 1 | 500<br>600 | 3 | 5 | BT131-500<br>BT131-600 | | | |
| 1 | 500<br>600 | 5 | 10 | BT132-500D<br>BT132-600D | | | |
| 4 | 500<br>600 | 5 | 10 | | BT134-500D<br>BT134-600D | BT136-500D<br>BT136-600D | BT136X-500D<br>BT136X-600D |
| 4 | 500<br>600<br>800 | 10 | 25 | | BT134-500E<br>BT134-600E<br>BT134-800E | BT136-500E<br>BT136-600E<br>BT136-800E | BT136X-500E<br>BT136X-600E<br>BT136X-800E |
| 4 | 500<br>600<br>800 | 25 | 70 | | BT134-500F<br>BT134-600F<br>BT134-800F | BT136-500F<br>BT136-600F<br>BT136-800F | BT136X-500F<br>BT136X-600F<br>BT136X-800F |
| 4 | 500<br>600<br>800 | 35 | 70 | | BT134-500<br>BT134-600<br>BT134-800 | BT136-500<br>BT136-600<br>BT136-800 | BT136X-500<br>BT136X-600<br>BT136X-800 |
| 4 | 500<br>600<br>800 | 50 | 100 | | BT134-500G<br>BT134-600G<br>BT134-800G | BT136-500G<br>BT136-600G<br>BT136-800G | BT136X-500G<br>BT136X-600G<br>BT136X-800G |
| 8 | 500<br>600 | 5 | 10 | | | BT137-500D<br>BT137-600D | BT137X-500D<br>BT137X-600D |
| 8 | 500<br>600<br>800 | 10 | 25 | | | BT137-500E<br>BT137-600E<br>BT137-800E | BT137X-500E<br>BT137X-600E<br>BT137X-800E |
| 8 | 500<br>600<br>800 | 25 | 70 | | | BT137-500F<br>BT137-600F<br>BT137-800F | BT137X-500F<br>BT137X-600F<br>BT137X-800F |
| 8 | 500<br>600<br>800 | 35 | 70 | | | BT137-500<br>BT137-600<br>BT137-800 | BT137X-500<br>BT137X-600<br>BT137X-800 |
| 8 | 500<br>600<br>800 | 50 | 100 | | | BT137-500G<br>BT137-600G<br>BT137-800G | BT137X-500G<br>BT137X-600G<br>BT137X-800G |

| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: | |  |  |
|---|---|---|---|---|---|
| | | (i), (ii), (iii) | (iv) | SOT78 (TO220AB) | SOT186A |
| A | V | mA | mA | | |
| 12 | 500<br>600<br>800 | 10 | 25 | BT138-500E<br>BT138-600E<br>BT138-800E | BT138X-500E<br>BT138X-600E<br>BT138X-800E |
| 12 | 500<br>600<br>800 | 25 | 70 | BT138-500F<br>BT138-600F<br>BT138-800F | BT138X-500F<br>BT138X-600F<br>BT138X-800F |
| 12 | 500<br>600<br>800 | 35 | 70 | BT138-500<br>BT138-600<br>BT138-800 | BT138X-500<br>BT138X-600<br>BT138X-800 |
| 12 | 500<br>600<br>800 | 50 | 100 | BT138-500G<br>BT138-600G<br>BT138-800G | BT138X-500G<br>BT138X-600G<br>BT138X-800G |
| 16 | 500<br>600<br>800 | 10 | 25 | BT139-500E<br>BT139-600E<br>BT139-800E | BT139X-500E<br>BT139X-600E<br>BT139X-800E |
| 16 | 500<br>600<br>800 | 25 | 70 | BT139-500F<br>BT139-600F<br>BT139-800F | BT139X-500F<br>BT139X-600F<br>BT139X-800F |
| 16 | 500<br>600<br>800 | 35 | 70 | BT139-500<br>BT139-600<br>BT139-800 | BT139X-500<br>BT139X-600<br>BT139X-800 |
| 16 | 500<br>600<br>800 | 50 | 100 | BT139-500G<br>BT139-600G<br>BT139-800G | BT139X-500G<br>BT139X-600G<br>BT139X-800G |
| 16 | 500<br>600<br>800 | 10-50 | 10-100 | BT139-500H<br>BT139-600H<br>BT139-800H | BT139X-500H<br>BT139X-600H<br>BT139X-800H |
| 25 | 500<br>600<br>800 | 35 | 70 | BTA140-500<br>BTA140-600<br>BTA140-800 | |

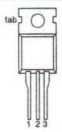
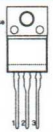
**THREE QUADRANT TRIACS - Surface Mount Packages**

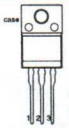
| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: |  |  |
|---|---|---|---|---|
| | | (i), (ii), (iii) | SOT223 | SOT428 (TO252) |
| A | V | mA | | |
| 1 | 500<br>600 | 5 | BTA204W-500D<br>BTA204W-600D | |
| 1 | 500<br>600<br>800 | 10 | BTA204W-500E<br>BTA204W-600E<br>BTA204W-800E | |
| 1 | 500<br>600<br>800 | 25 | BTA204W-500F<br>BTA204W-600F<br>BTA204W-800F | |
| 1 | 500<br>600<br>800 | 35 | BTA204W-500C<br>BTA204W-600C<br>BTA204W-800C | |
| 1 | 500<br>600<br>800 | 50 | BTA204W-500B<br>BTA204W-600B<br>BTA204W-800B | |
| 4 | 500<br>600<br>500<br>600 | 5 | | BTA204M-500D<br>BTA204M-600D<br>BTA204S-500D<br>BTA204S-600D |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 10 | | BTA204M-500E<br>BTA204M-600E<br>BTA204M-800E<br>BTA204S-500E<br>BTA204S-600E<br>BTA204S-800E |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 25 | | BTA204M-500F<br>BTA204M-600F<br>BTA204M-800F<br>BTA204S-500F<br>BTA204S-600F<br>BTA204S-800F |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 35 | | BTA204M-500C<br>BTA204M-600C<br>BTA204M-800C<br>BTA204S-500C<br>BTA204S-600C<br>BTA204S-800C |
| 4 | 500<br>600<br>800<br>500<br>600<br>800 | 50 | | BTA204M-500B<br>BTA204M-600B<br>BTA204M-800B<br>BTA204S-500B<br>BTA204S-600B<br>BTA204S-800B |

| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: |  |  |
|---|---|---|---|---|
| | | (i), (ii), (iii) | SOT428 (TO252) | SOT404 (TO263) |
| A | V | mA | | |
| 8 | 500<br>600<br>500<br>600 | 5 | BTA208M-500D<br>BTA208M-600D<br>BTA208S-500D<br>BTA208S-600D | BTA208B-500D<br>BTA208B-600D |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 10 | BTA208M-500E<br>BTA208M-600E<br>BTA208M-800E<br>BTA208S-500E<br>BTA208S-600E<br>BTA208S-800E | BTA208B-500E<br>BTA208B-600E<br>BTA208B-800E |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 25 | BTA208M-500F<br>BTA208M-600F<br>BTA208M-800F<br>BTA208S-500F<br>BTA208S-600F<br>BTA208S-800F | BTA208B-500F<br>BTA208B-600F<br>BTA208B-800F |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 35 | BTA208M-500C<br>BTA208M-600C<br>BTA208M-800C<br>BTA208S-500C<br>BTA208S-600C<br>BTA208S-800C | BTA208B-500C<br>BTA208B-600C<br>BTA208B-800C |
| 8 | 500<br>600<br>800<br>500<br>600<br>800 | 50 | BTA208M-500B<br>BTA208M-600B<br>BTA208M-800B<br>BTA208S-500B<br>BTA208S-600B<br>BTA208S-800B | BTA208B-500B<br>BTA208B-600B<br>BTA208B-800B |

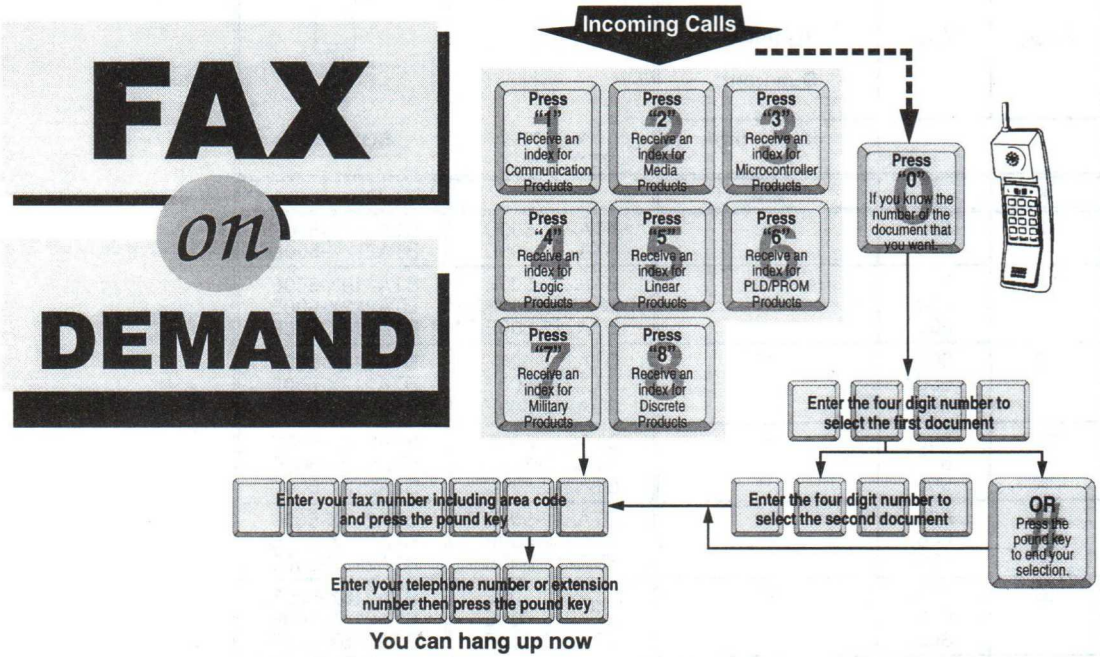
| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: |  |
|---|---|---|---|
| | | (i), (ii), (iii) | SOT404 (TO263) |
| A | V | mA | |
| 12 | 500<br>600 | 5 | BTA212B-500D<br>BTA212B-600D |
| 12 | 500<br>600<br>800 | 10 | BTA212B-500E<br>BTA212B-600E<br>BTA212B-800E |
| 12 | 500<br>600<br>800 | 25 | BTA212B-500F<br>BTA212B-600F<br>BTA212B-800F |
| 12 | 500<br>600<br>800 | 35 | BTA212B-500C<br>BTA212B-600C<br>BTA212B-800C |
| 12 | 500<br>600<br>800 | 50 | BTA212B-500B<br>BTA212B-600B<br>BTA212B-800B |
| 16 | 500<br>600<br>800 | 35 | BTA216B-500C<br>BTA216B-600C<br>BTA216B-800C |
| 16 | 500<br>600<br>800 | 50 | BTA216B-500B<br>BTA216B-600B<br>BTA216B-800B |
| 25 | 500<br>600<br>800 | 35 | BTA225B-500C<br>BTA225B-600C<br>BTA225B-800C |
| 25 | 500<br>600<br>800 | 50 | BTA225B-500B<br>BTA225B-600B<br>BTA225B-800B |

**THREE QUADRANT TRIACS - Leaded Packages**

| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: |  |  |
|---|---|---|---|---|
| | | (i), (ii), (iii) | SOT78 (TO220AB) | SOT186A |
| A | V | mA | | |
| 4 | 500<br>600 | 5 | BTA204-500D<br>BTA204-600D | BTA204X-500D<br>BTA204X-600D |
| 4 | 500<br>600<br>800 | 10 | BTA204-500E<br>BTA204-600E<br>BTA204-800E | BTA204X-500E<br>BTA204X-600E<br>BTA204X-800E |
| 4 | 500<br>600<br>800 | 25 | BTA204-500F<br>BTA204-600F<br>BTA204-800F | BTA204X-500F<br>BTA204X-600F<br>BTA204X-800F |
| 4 | 500<br>600<br>800 | 35 | BTA204-500C<br>BTA204-600C<br>BTA204-800C | BTA204X-500C<br>BTA204X-600C<br>BTA204X-800C |
| 4 | 500<br>600<br>800 | 50 | BTA204-500B<br>BTA204-600B<br>BTA204-800B | BTA204X-500B<br>BTA204X-600B<br>BTA204X-800B |
| 8 | 500<br>600 | 5 | BTA208-500D<br>BTA208-600D | BTA208X-500D<br>BTA208X-600D |
| 8 | 500<br>600<br>800 | 10 | BTA208-500E<br>BTA208-600E<br>BTA208-800E | BTA208X-500E<br>BTA208X-600E<br>BTA208X-800E |
| 8 | 500<br>600<br>800 | 25 | BTA208-500F<br>BTA208-600F<br>BTA208-800F | BTA208X-500F<br>BTA208X-600F<br>BTA208X-800F |
| 8 | 500<br>600<br>800 | 35 | BTA208-500C<br>BTA208-600C<br>BTA208-800C | BTA208X-500C<br>BTA208X-600C<br>BTA208X-800C |
| 8 | 500<br>600<br>800 | 50 | BTA208-500B<br>BTA208-600B<br>BTA208-800B | BTA208X-500B<br>BTA208X-600B<br>BTA208X-800B |

| $I_{T(RMS)}$ | $V_{DRM}$ | $I_{GT}$ (max) Quadrant: |  |  |
|---|---|---|---|---|
| | | (i), (ii), (iii) | SOT78 (TO220AB) | SOT186A |
| A | V | mA | | |
| 12 | 500<br>600 | 5 | BTA212-500D<br>BTA212-600D | BTA212X-500D<br>BTA212X-600D |
| 12 | 500<br>600<br>800 | 10 | BTA212-500E<br>BTA212-600E<br>BTA212-800E | BTA212X-500E<br>BTA212X-600E<br>BTA212X-800E |
| 12 | 500<br>600<br>800 | 25 | BTA212-500F<br>BTA212-600F<br>BTA212-800F | BTA212X-500F<br>BTA212X-600F<br>BTA212X-800F |
| 12 | 500<br>600<br>800 | 35 | BTA212-500C<br>BTA212-600C<br>BTA212-800C | BTA212X-500C<br>BTA212X-600C<br>BTA212X-800C |
| 12 | 500<br>600<br>800 | 50 | BTA212-500B<br>BTA212-600B<br>BTA212-800B | BTA212X-500B<br>BTA212X-600B<br>BTA212X-800B |
| 16 | 500<br>600<br>800 | 10 | BTA216-500E<br>BTA216-600E<br>BTA216-800E | BTA216X-500E<br>BTA216X-600E<br>BTA216X-800E |
| 16 | 500<br>600<br>800 | 25 | BTA216-500F<br>BTA216-600F<br>BTA216-800F | BTA216X-500F<br>BTA216X-600F<br>BTA216X-800F |
| 16 | 500<br>600<br>800 | 35 | BTA216-500C<br>BTA216-600C<br>BTA216-800C | BTA216X-500C<br>BTA216X-600C<br>BTA216X-800C |
| 16 | 500<br>600<br>800 | 50 | BTA216-500B<br>BTA216-600B<br>BTA216-800B | BTA216X-500B<br>BTA216X-600B<br>BTA216X-800B |
| 25 | 500<br>600<br>800 | 35 | BTA225-500C<br>BTA225-600C<br>BTA225-800C | |
| 25 | 500<br>600<br>800 | 50 | BTA225-500B<br>BTA225-600B<br>BTA225-800B | |

# FAX-on-DEMAND System




## What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

## How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
**http://www.semiconductors.philips.com**

## Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

## FAX-on-DEMAND phone numbers:

| | |
|---|---|
| England (United Kingdom, Ireland) | 44-181-730-5020 |
| France | 33-1-40-99-60-60 |
| Italy | 39-167-295502 |
| North America | 1-800-282-2000 |

## Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

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# GENERAL


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Philips Semiconductors is working intensively on bringing new products to the market to meet the requirements of existing and new developing application areas. These are the new products and technologies that appear for the first time in this data handbook.

### 1A Logic level triacs in SOT54 (TO92)

A new range of logic level four quadrant triacs has been introduced which uses the compact and low cost SOT54 leaded package. This package is Philips' equivalent to TO92. The triacs have been designed with very sensitive gates for operation in all four quadrants where gate drive current availability is limited.

Part numbers are BT131-500, BT131-600 and BT132-500D, BT132-600D. Their $I_{GT}$ levels are 3,3,3,7mA and 5,5,5,10mA respectively in quadrants (i), (ii), (iii) and (iv). They are intended for driving small loads such as fan motors, timers and valves. They will find uses in numerous domestic appliances and large white goods, for example washing machines, dishwashers and refrigerators, where many such devices might be used per appliance.

### Surface mount packages

Our surface mount range has been increased dramatically by the addition of two new purpose-designed surface mount packages: SOT428 and SOT404. These are Philips' equivalents to DPAK and $D^2PAK$ respectively. Our full range of thyristors and triacs is now available in these higher power packages, where higher currents combined with surface mount technology become a reality. Device current ratings range from 4A to 25A. Actual current handling is limited only by the degree of heatsinking provided by the substrate.

The SOT428 package is available with two pinout options: standard and reverse. This assures compatability with all existing PCB layouts.

### Additional voltage grades for BT169W

The SOT223 version of the small BT169 thyristor has previously only been available in the 400V grade (BT169DW). It is now available in all voltage grades from 200V to 600V. The full lineup is BT169BW (200V), BT169DW (400V), BT169EW (500V), BT169GW (600V).

### New thyristor with high $V_{GR}$

Some specialist applications require a thyristor with a high gate-cathode reverse breakdown voltage ($V_{GR}$). This is available in the BT148SZ-600R and BT148MZ-600R. These are standard and reverse pinning versions in SOT428. These 4A thyristors possess a $V_{GR}$ of 14V to 20V and an $I_{GT}$ of 200µA.

### Three quadrant triacs

The advantages of Hi-Com triacs will be well known to many. However, although their static and dynamic dV/dt and their dI/dt performances are exemplary, their insensitive gates ($I_{GT}$ = 50mA) can be a problem in applications where gate drive is limited. There are occasions when a compromise between commutation performance and gate sensitivity are required. This is now possible with the introduction of a full range of 3-quadrant triacs. Gate sensitivities now range upwards from 5mA. All of our new surface mount packages, leaded packages and pinning options are available.

### Thyristors in SOT186A

Our range of thyristors is now released in the SOT186A isolated envelope which offers 2,500V RMS isolation from any surrounding metalwork. The part numbers are BT258X-500R, BT258X-600R and BT258X-800R ($I_{T(RMS)}$ = 8A, $I_{GT}$ = 200µA); BT300X-500R, BT300X-600R, BT300X-800R ($I_{T(RMS)}$ = 8A, $I_{GT}$ = 15mA); BT152X-400R, BT152X-600R, BT152X-800R ($I_{T(RMS)}$ = 20A, $I_{GT}$ = 32mA).

### Unencapsulated, passivated, silicon power chips

All the devices in this data handbook are available as unencapsulated dice complete with passivation and metallised contact pads, but without bond wires or any other connections or encapsulation. Contact your Regional or National Sales Office for details.

## PHILIPS THYRISTORS AND TRIACS

### The Phase 2 Process

The basic principle of using a PNPN structure to produce a thyristor, and an NPNPN structure (with two PNPN's in antiparallel) to produce a triac has been known for decades. The factors controlling various important parameters, such as blocking voltages, on-state voltage drop, trigger current, latching and holding current, off-state dV/dt, triac commutation and surge capability are also well known.

The modern challenge of making good thyristors and triacs lies not so much in innovative design concepts as in perfection of manufacturing technology.

Philips products are characterised by the use of well established, stable processes in both diffusion and assembly, giving devices of high quality and reliability. The strengths and special features of these products are outlined below.

Except for those designed for specialist applications such as GTO's and ASCR's, most common thyristors and triacs are specified to have voltage blocking capability in both directions. This means that in the PNPN or NPNPN structures, two opposing PN junctions need to be designed to withstand the rated voltage.

This is normally achieved by starting with a suitably low doped N type silicon wafer into which two P regions are diffused simultaneously from opposite sides, resulting in a symmetric PNP structure where both PN junctions have high voltage blocking capability. Further N-type diffusions are then put into both sides of the structure, (for a triac). The result is an NPNPN structure with a symmetrical blocking voltage. Both of these blocking PN junctions now need to be passivated at the point where they intersect the silicon surface, and there are two common methods for doing this, shown in the diagrams below.

In Philips terminology we call these "Phase 1" and "Phase 2" technologies respectively.

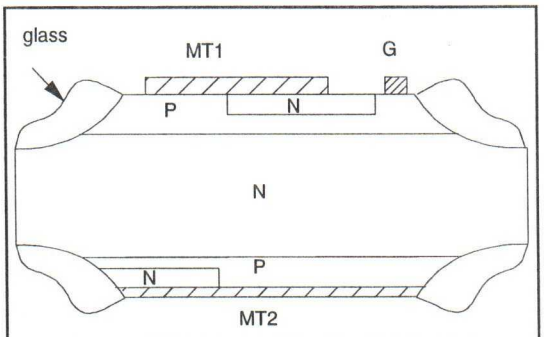



*Fig. 1. Phase 1 structure and passivation.*

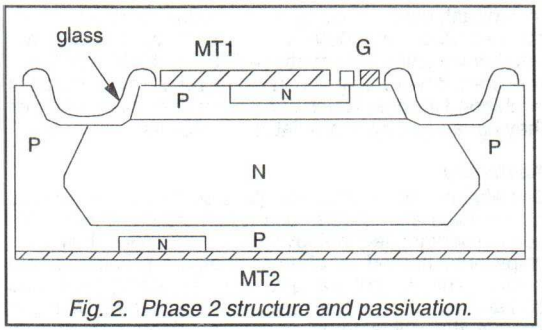



*Fig. 2. Phase 2 structure and passivation.*

As can be seen, Phase 1 passivation requires a simultaneous etching of mesa troughs from both sides followed by the deposition of passivants such as negatively charged glass. The advantages of this technique are small chip size and fewer processing stages. No aluminium isolation diffusion or photolith are required, hence the overall chip cost is lower.

By contrast, the Phase 2 technology requires an aluminium isolation diffusion prior to the fabrication of the PNPN or NPNPN structure, which has the effect of bringing both blocking PN junctions to the top surface. These can then be passivated with trough etching and glass deposition on the top side only.

The main advantage of the Phase 2 technology is a much more mechanically robust structure, due to the fact that the edge of the chip is not reduced in thickness. Minor damage to the edges does not intrude into the active region. A further advantage is that the flat bottom surface is compatible with automatic die bonding in assembly.

The main disadvantage is increased cost in comparison with the Phase 1 process.

Philips has progressed from Phase 1 to Phase 2 passivation technology, despite its higher cost, because of the advantages of mechanical ruggedness and lower vulnerability to handling damage.

It is our belief that Philips thyristors and triacs produced using Phase 2 technology have fewer manufacturing defects, and are more reliable than devices produced using the Phase 1 structure.

### Passivation

The use of the Phase 2 passivation structure coupled with the well developed glass mesa passivation technology at Philips results in devices with high voltage blocking capability and extremely stable characteristics. The structure is also less vulnerable to edge damage compared to the alternative Phase 1 passivation.

The typical off-state breakdown voltage of our thyristors and triacs is in excess of 900V, with a very tight distribution. We would consider any devices with blocking voltages less than 500V to be defective. For example, our 400V grade devices are tested to withstand 500V.

In contrast, devices using Phase 1 passivation and rated at, say, 200V or 400V are more likely to have true breakdown voltages just above 200V or 400V. The lower true breakdown voltages can be the result of glass cracks or chipped corners which can progress to the extent that they cause quality and reliability problems.

**Assembly**

The absence of troughs and glass on the bottom surface of our chips allows us to use automated assembly. We use die bonding technology which involves scrubbing the chips onto heated leadframes that are precoated with solder. This technique gives an excellent, void free contact with low thermal resistance and avoids having to subject the chips to long duration, high temperature furnacing. Compared to our main competitors, our devices have superior die bonds and lower thermal resistance, which means that they operate at a lower junction temperature for the same dissipation, and thus have higher reliability.

Another feature of this assembly method is that, along with the ultrasonic wire bonding used to connect to the top of the chip, it gives our devices a high thermal fatigue capability. Thus they have excellent on-state reliability as well as extremely stable off-state characteristics.

**Unencapsulated Dice**

Because of the advantages of the Philips process and assembly techniques outlined above, our family of triacs and thyristors are ideal for use in unencapsulated form, in applications where space and height are at a premium. The glass passivation protects the otherwise exposed surface regions, giving highly stable device characteristics. The silicon wafers are 100% electrically tested and are normally supplied sawn, on blue film frame carriers. Unsawn wafers can be supplied where necessary.

Philips Semiconductors has a wealth of experience of supplying devices in this form and is able to provide expert advice on the subject of mounting, soldering and attaching bond wires to unpackaged dice.

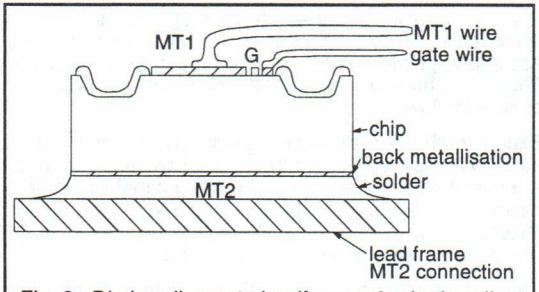



*Fig. 3. Die bonding onto leadframes & wire bonding.*

## Thyristor and Triac Ratings

A rating is a value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

All limiting values quoted in this data handbook are Absolute Maximum Ratings - limiting values of operating and environmental conditions applicable to any device of a specified type, as defined by its published data.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value is exceeded with any device, under the worst probable operating conditions.

### Voltage ratings

$V_{DRM}$, $V_{RRM}$ Repetitive peak off-state voltage. The maximum allowable instantaneous forward or reverse voltage including transients. The rated values of $V_{DRM(max)}$ and $V_{RRM(max)}$ may be applied continuously over the entire operating junction temperature range, provided that the thermal resistance between junction and ambient is kept low enough to avoid the possibility of thermal runaway.

### Current ratings

$I_{T(AV)}$ Average on-state current. The average rated current is that value which under steady state conditions will result in the rated temperature $T_{jmax}$ being reached when the mounting base or heatsink is at a given temperature. Graphs of on-state dissipation versus $I_{T(AV)}$ or $I_{T(RMS)}$ are provided in the data sheets. The right hand scale of each graph shows the maximum allowable mounting base or heatsink temperature for a given dissipation.

$I_{T(RMS)}$ RMS on-state current. For a given average current, the power dissipated at small conduction angles is much higher than at large conduction angles. This is a result of the higher rms currents at small conduction angles. Operating the device at rms currents above the rated value is likely to result in rapid thermal cycling of the chip and the bond wires which can lead to reliability problems.

$I_{TSM}$ Non-repetitive peak on-state current. The maximum allowable non-repetitive peak on-state surge current which may be applied to the device. The data sheet condition assumes a starting junction temperature of 25°C and a sinusoidal surge current at a mains frequency of 50/60 Hz. For a triac, a full sine wave of current is applied. Graphs in the data sheet show the variation of $I_{TSM}$ with surge duration.

$I^2t$ Device fuse rating. For correct circuit protection, the $I^2t$ of a protective fuse must be less than the $I^2t$ of the device. In the data sheets, the device rating is numerically equal to $I_{TSM}^2/200$ and assumes a 10ms fusing time.

$dI_T/dt$ The maximum allowable rate of rise of on-state current after gate triggering. The theory underlying this rating is that, where the rate of rise of main current is very rapid immediately after triggering, local 'hot spot' heating will occur in a small part of the device active area close to the gate, leading to device degradation or complete failure. In practice, true $dI_T/dt$ failures of this kind are very rare. The only conditions where $dI_T/dt$ has been observed to cause failures is in triacs operated in quadrant (iv) (T2-, G+) where a combination of high $dI_T/dt$ and high peak current (in excess of the data sheet ratings), can cause damage to the gate structure. For this reason, operation of our triacs in quadrant IV should be avoided wherever possible.

$V_{BO}$ or $dV_D/dt$ triggered. Where a device is triggered by exceeding the breakdown voltage, or by a high rate of rise of off-state voltage, as opposed to injecting current into the gate, it is necessary to limit the $dI_T/dt$. A note in the data sheet specifies the maximum allowable $dI_T/dt$ for this mode of triggering.

### Thermal ratings

Steady state thermal resistances.

$R_{th\ j\text{-}mb}$ Junction to mounting base is used for the SOT78 (TO220), SOT404 and SOT428 envelopes.

$R_{th\ j\text{-}hs}$ Junction to heatsink is used for full pack, isolated envelopes (e.g. SOT186A).

$R_{th\ j\text{-}sp}$ Junction to solder point is used for the smallest surface mounting envelope, SOT223.

$R_{th\ j\text{-}lead}$ Junction to lead is used for the SOT54 (TO92) small outline.

The maximum value of the thermal resistance is given in the data sheet, and is used to specify the device rating. The average junction temperature rise for a given dissipation is given by multiplying the average dissipation by the thermal resistance.

Note that for triacs, two values of thermal resistance are quoted; one for half cycle operation and one for full cycle operation. This is because only half of the chip carries current in each half cycle allowing the non-conducting half to cool down between conduction periods. The net effect is to reduce the average thermal resistance for full cycle conduction.

$R_{th\ j\text{-}a}$ Typical values of junction to ambient thermal resistance are given in the data sheet. This assumes that, for leaded devices intended for through-hole mounting, the device is mounted vertically on a printed circuit board in free air, and for surface mount packages the device is soldered to a given pad area on given PCB material.

$Z_{th\ j\text{-}mb}$, $Z_{th\ j\text{-}hs}$ Whilst the average junction temperature rise may be found from the thermal resistance figure, the peak junction temperature requires knowledge of the current waveform and the transient thermal impedance. The thermal impedance curves in the data sheets are based on rectangular power pulses. The junction temperature rise due to a rectangular power pulse, is given by multiplying the peak dissipation during the pulse by the thermal impedance $Z_{th\ j\text{-}mb}$ for the given pulse width. Analysis methods for non-rectangular pulses are covered in the Power Semiconductor Applications handbook.

$T_{jmax}$ The maximum operating junction temperature range for all of our thyristors and triacs is 125˚C. This applies in either the on-state or off-state, and for either half cycle or full cycle conduction. It is permissible for the junction temperature to exceed $T_{j\ max}$ for short periods during non-repetitive surges, but for repetitive operation the peak junction temperature must remain below $T_{j\ max}$.

$T_{stg}$ The limiting storage temperature range for all of our thyristors and triacs is -40˚C to 150˚C.

$P_{G(AV)}$, $P_{GM}$, $I_{GM}$, $V_{GM}$ The average and peak gate power dissipation, and the maximum gate voltage and gate current. Exceeding the gate ratings can cause the device to degrade gradually, or fail completely.

## Thyristor and Triac Characteristics

A characteristic is an inherent and measurable property of a device. Such a property may be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

### Static characteristics

$V_T$ On-state voltage. The tabulated value in the data sheet is the maximum, instantaneous on-state voltage measured under pulse conditions to avoid excessive dissipation, at a junction temperature of 25˚C. The data sheet also contains a graph showing the maximum and typical characteristics at 125˚C and the maximum characteristic at 25˚C. The maximum characteristic at 125˚C is used to calculate the dissipation for a given average or rms current, and hence the graph of on-state dissipation versus average or rms current in the data sheet.

The on-state voltage/ current characteristic of a diode, thyristor or triac may be approximated by a piecewise linear model as shown in the figure below; where $R_S$ is the slope of the tangent to the curve at the rated current, and $V_O$ is the voltage axis intercept. The on-state voltage is then $V_T = V_O + I_T.R_S$, and the instantaneous dissipation is $P_T = V_O.I_T + I_T^2.R_S$. where $I_T$ is the instantaneous on-state current.

It can be shown that the average on-state dissipation for any current waveform is: $P_{T(AV)} = V_O.I_{T(AV)} + I_{T(RMS)}^2.R_S$, where $I_{T(AV)}$ is the average on-state current and $I_{T(RMS)}$ is the rms value of the on-state current. Graphs in the published data show on-state dissipation as a function of average current for thyristors and versus rms current for triacs. Sinusoidal current waveforms are assumed and the graphs show dissipation over a range of conduction angles

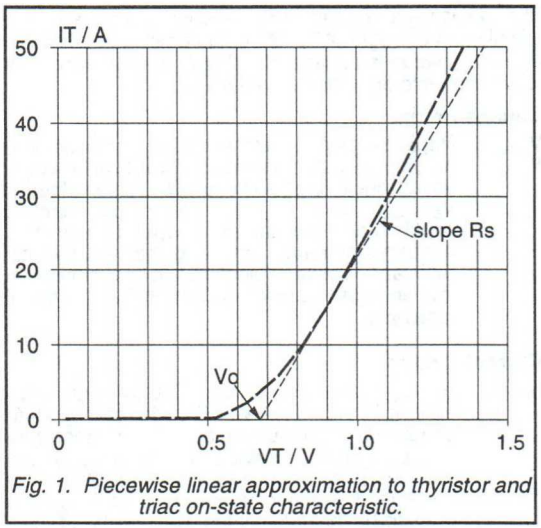



*Fig. 1. Piecewise linear approximation to thyristor and triac on-state characteristic.*

$I_{GT}$ Gate trigger current. The data sheet shows the typical and maximum gate trigger current at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised $I_{GT}$ with temperature.

When designing a triac gate trigger circuit, triggering in quadrant (iv) (T2-, G+) should be avoided if possible. The gate trigger current in this quadrant is much higher than in the other three quadrants and the device is more susceptible to turn-on $dI_T/dt$ failure.

$V_{GT}$ Gate trigger voltage. The data sheet shows the typical and maximum gate trigger voltage at a gate current equal to $I_{GT}$, at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised $V_{GT}$ with temperature.

To ensure that a device will not trigger, the gate voltage must be held below the minimum gate trigger voltage. The data sheet quotes $V_{GT(min)}$ at the maximum junction temperature (125˚C), and the maximum off-state voltage ($V_{DRM(max)}$).

$I_L$ Latching current. The latching current is the value of on-state current required to maintain conduction at the instant when the gate current is removed. A graph in the data sheets shows the variation of normalised $I_L$ with temperature.

To trigger a thyristor or triac, a gate current greater than the maximum device gate trigger current $I_{GT}$ must be applied until the on-state current $I_T$ rises above the maximum latching current $I_L$. This condition must be met at the lowest junction temperature.

$I_H$ Holding current. The holding current is the value of on-state current required to maintain conduction once the device has fully turned on and the gate current has been removed. The on-state current must have previously exceeded the latching current $I_L$. A graph in the data sheet shows the variation of normalised $I_H$ with temperature.

To turn off (commutate) a thyristor or triac, the load current must remain below $I_H$ for sufficient time to allow a return to the off-state. This condition must be met at the highest operating junction temperature (125˚C).

$I_D$, $I_R$ The maximum off-state leakage current, specified at rated $V_{DRM(max)}$, $V_{RRM(max)}$ at 125˚C.

**Dynamic characteristics**

$dV_D/dt$ Critical rate of rise of off-state voltage. Displacement current caused by a high rate of rise of off-state voltage can induce a gate current sufficient to trigger the device. Devices with sensitive gates are particularly susceptible to $dV_D/dt$ triggering, and since gate trigger current decreases as junction temperature increases, the condition is worse when the device is hot. The data sheet figure is specified at 125˚C using an exponential waveform and a maximum applied voltage of 67% $V_{DRM(max)}$. The $dV_D/dt$ is measured to 63% of the maximum voltage.

To prevent sensitive gate devices from false triggering due to high rates of rise of off state voltage, 1 kΩ resistor in parallel with a 10nF capacitor may be fitted between gate and cathode (gate and terminal 1 for a triac). This approach is less effective for standard gate devices. In this case, the preferred option is to fit an RC snubber between anode and cathode (T2 and T1 for a triac) to reduce the $dV_D/dt$ below the critical value.

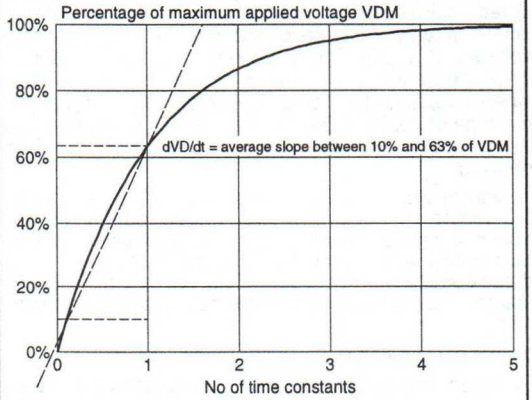



*Fig. 2. Exponential waveform used for measurement of critical off-state $dV_D/dt$. The $dV_D/dt$ is the average slope between 10% and 63% of the maximum applied voltage $V_{DM}$.*

$t_{gt}$ Gate controlled turn-on time. A typical turn on time of 2 µs is specified for all our thyristors and triacs.

$t_q$ Circuit commutated turn-off time. A typical turn off time of 70 µs is specified for standard gate thyristors and 100µs for sensitive gate thyristors.

## Triac Commutation

A triac is an AC conduction device and may be thought of as two thyristors in antiparallel, monolithically integrated onto the same silicon chip. In phase control circuits, the triac often has to be triggered into conduction part way into each half cycle. This means that at the end of each half cycle the on-state current in one direction must drop to zero and not resume in the other direction until the device is triggered again. This commutation turn-off capability is at the heart of triac power control applications. If the triac were truly two separate thyristors in antiparallel, this requirement would not present any problems. However, as the two are on the same piece of silicon there is the possibility that the unrecombined charge of one thyristor as it turns off may act as gate current to trigger the other thyristor as the voltage rises in the opposite direction. This phenomenon is called commutation failure.

There are two components of current which can act as gate current to cause commutation failure. One of these is the displacement current generated by the reapplied $dV_{COM}/dt$. The other is the recombination current, which is mainly determined by the rate of fall of commutating current, $dI_{COM}/dt$. Both tend to create a lateral volt drop in the cathode of the opposing thyristor which triggers the device in the opposite direction to the original current flow.

At low rates of fall of current, $dI_{COM}/dt$, the amount of unrecombined charge is small and commutation failure occurs mainly because of the rate of rise of off-state voltage, $dV_{COM}/dt$. This situation is worse for inductive loads where the rate of rise of voltage can be very high when commutation occurs. The conventional remedy for this type of commutation failure is to fit a snubber across the device to limit the rate of rise of off-state voltage $dV_{COM}/dt$.

At high values of $dI_{COM}/dt$ as would occur with a rectifier-fed DC motor, the recombination current dominates and, above a critical value of $dI_{COM}/dt$, the device will not commutate even at fairly low values of $dV_{COM}/dt$. Under these conditions, a snubber will not prevent commutation failure, and the best option is to use a High Commutation Triac.

**Three Quadrant Triacs**

Philips three quadrant triacs, which include Hi-Com types, attempt to separate the two antiparallel thyristor structures to prevent the unrecombined charge from the conducting half becoming gate current in the other half. This is accomplished by lateral separation of the top and bottom emitters, more extensive emitter and peripheral shorting, and by a modified gate design which prevents triggering in quadrant (iv).

The device design, in addition to giving high immunity to commutation failure, also improves the off-state $dV_D/dt$ capability. They will commutate the full rated current up to 125˚C without the aid of a snubber and will also withstand extremely high rates of rise of off-state voltage, in excess of 1000 V/µs. High commutation triacs can simplify circuit design by eliminating the need for RC snubbers. Typical applications include:
Motor starting, where the triac may be required to commutate the starting current;
Switching of DC operated relay coils or motors, where the time constant of the coil is much greater than the mains period;
Static switching, where it is required to turn the triac off whilst it is carrying an overload current.

$dV_{COM}/dt$ Critical rate of rise of commutating voltage. For conventional, as opposed to high commutation triacs, the data sheet conditions specify a junction temperature of 95˚C and a $dI_{COM}/dt$ given by $2.\sqrt{2}.\pi.f.I_{T(RMS)}$, where f is the mains frequency (assumed to be 50Hz). This value is the maximum rate of change of current which occurs at the zero crossing for a sine wave current equal to the rated rms value, $I_{T(RMS)}$. Graphs in the data sheet show the variation of $dV_{COM}/dt$ and with junction temperature with $dI_{COM}/dt$ as a parameter.

$dI_{COM}/dt$ Critical rate of change of commutating current. High Commutation Triacs are intended for use in circuits where high values of both $dI_{COM}/dt$ and $dV_{COM}/dt$ can occur. Commutation capability is specified in terms of $dI_{COM}/dt$, without a snubber and at the highest junction temperature, $T_{jmax}$ = 125˚C. A graph in the data sheet shows the variation of $dI_{COM}/dt$ with junction temperature.

## Operation up to 150˚C

The maximum operating junction temperature, $T_{jmax}$ of Philips thyristors and triacs is 125˚C. Operation above $T_{jmax}$ for long periods, particularly in the off-state, can give rise to reliability problems due to changes in characteristics which occur as a result of mobile charge in the glass passivation.

Furthermore, as a thyristor or triac gets hot, it becomes more susceptible to false gate triggering, off-state $dV_D/dt$ triggering, thermal runaway and commutation failure.

However, it has become apparent that some customers have applications which require operation of thyristors and triacs at higher junction temperatures.

Recent improvements in Philips glass mesa technology backed up by extensive reliability testing has shown that, for certain applications, our thyristors and triacs can be operated reliably at junction temperatures up to 150˚C.

Typical applications where 150˚C operation may be allowed include:- static switching of resistive loads, power switches for domestic appliances and electric heating applications where the device is mounted on a high temperature substrate.

Extending the upper operating junction temperature to 150˚C depends very much on the application. For this reason we recommend that customers wishing to use our thyristors and triacs at 150˚C contact the Field Applications Engineer at their Regional or National sales office.

Philips Semiconductors publishes many Technical Publications each year on various aspects of power semiconductors. All the publications relevant to thyristors and triacs are reproduced in this chapter. They provide some useful information on the different device types. They also give hints and ideas on how best to use thyristors and triacs.

The technical information contained within these publications always remains relevant. However due to the wide range in their issue dates, product information, where provided, will be historical and might have been superceded. Please bear this fact in mind when reading any selection tables. The up-to-date product information can be found in the selection guide at the front of this data book.

# FACTSHEET 013. UNDERSTANDING Hi-Com TRIACS

Issue date August 1993 Document number 9398 510 21011

Hi-Com triacs from Philips Semiconductors are specifically designed to give superior triac commutation performance in the control of motors for domestic equipment and tools. These devices are suitable for use with a wide variety of motor and inductive loads without the need for a protective snubber. The use of a Hi-Com triac greatly simplifies circuit design and gives significant cost savings to the designer.

This product information sheet explains how the superior characteristics and performance of Hi-Com triacs removes design limitations of standard devices.

## Triac commutation explained

A triac is an AC conduction device and may be thought of as two antiparallel thyristors monolithically integrated onto the same silicon chip.

In phase control circuits the triac often has to be triggered into conduction part way into each half cycle. This means that at the end of each half cycle the on-state current in one direction must drop to zero and not resume in the other direction until the device is triggered again. This "commutation" turn-off capability is at the heart of triac power control applications.

If the triac were truly two separate thyristors this requirement would not present any problems. However, as the two are on the same piece of silicon, there is the possibility that the "reverse recovery current" (due to unrecombined charge carriers) of one thyristor as it turns off may act as gate current to trigger the other thyristor as the voltage rises in the opposite direction. This is described as a "commutation failure" and results in the triac continuing to conduct in the opposite direction instead of blocking.

The probability of any device failing commutation is dependent on the rate of rise of reverse voltage (dV/dt) and the rate of decrease of conduction current (dI/dt). The higher the dI/dt the more unrecombined charge carriers are left at the instant of turn-off. The higher the dV/dt the more probable it is that some of these carriers will act as gate current. Thus the commutation capability of any device is usually specified in terms of the turn-off dI/dt and the re-applied dV/dt it can withstand, at any particular junction temperature.

If a triac has to be operated in an inductive load circuit with a combination of dI/dt and dV/dt that exceeds its specification, it is necessary to use an RC-snubber network in parallel with the device to limit the dV/dt. This is at a penalty of extra circuit complexity and dissipation in the snubber. The "High Commutation" triacs (Hi-Com triacs) are designed to have superior commutation capability, so that even at a high rate of turn-off (dI/dt) and a high rate of re-applied dV/dt, they can be used without the aid of a snubber network, thus greatly simplifying the circuit. The design features of Hi-Com devices that have made this possible are:

### 1. Geometric separation of the two antiparallel thyristors

Commutation failure can be avoided by physically separating the two 'thyristor halves' of a triac. However, separating them into two discrete chips would remove the advantage of a triac being triggerable in both directions by the same gate connection. Within the integrated structure of a Hi-Com triac the two halves of the device are kept further apart by modifying the layout of the chip in order to lessen the chance of conduction in one half affecting the other half.

### 2. Emitter shorting

"Emitter shorts" refer to the on-chip resistive paths between emitter and base of a transistor. A higher degree of emitter shorting means the presence of more such paths and lower resistance values in them. The use of emitter shorts in a triac has two effects on commutation.

Firstly it reduces the gain of the internal transistors that make up the triac. This means there will be fewer carriers left to recombine when the conduction current falls to zero, and therefore a smaller probability that a sufficient number will be available to re-trigger the triac. The second way in which emitter shorts help commutation is that any unrecombined carriers in the conducting thyristor at turn-off will have more chance of flowing out through the emitter shorts (of the opposite thyristor) rather than acting as gate current to trigger that thyristor on.

The Hi-Com triacs have a higher degree of emitter shorting both around the periphery of the device and in the central part of the active area. This both reduces the number of carriers available, and lessens the danger of any available carriers acting as gate current for undesirable triggering.

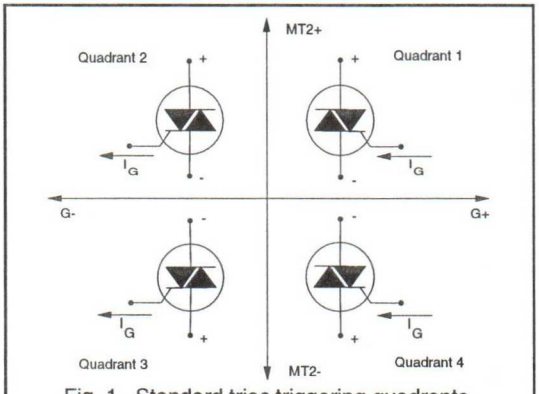



Fig. 1. Standard triac triggering quadrants.

### 3. Modified gate structure

The gate of a triac allows conduction in both directions to be initiated by either a positive or a negative current pulse between gate (G) and main terminal (MT1). The four different modes of triggering are often called 1+, 1-, 3- and 3+ (or sometimes quadrants 1, 2, 3 and 4) and are shown in Fig. 1.

This triggering versatility arises from the fact that the gate consists of some elements which conduct temporarily during the turn-on phase. In particular, one of the triggering modes, 3+ (or quadrant 4), relies on the main terminal 1 supplying electrons to trigger a thyristor element in the gate-MT1 boundary. Conduction then spreads to the main thyristor element from this boundary.

Unfortunately the carrier distribution in this triggering mode of operation is very similar to that existing when the triac is commutating in the 1-to-3 direction (i.e changing from conduction with MT2 positive to blocking with MT1 positive). The presence of the element in the gate to allow 3+ triggering will therefore always also undermine commutation capability in the 1-to 3 direction. For this reason the Hi-Com triacs have a modified gate design to remove this structure. This incurs the penalty that the 3+ trigger mode cannot be used, but it greatly improves the commutation performance of the device.

### Conclusions

By modifications to the internal design and layout of the triac it is possible to achieve a high commutation capability triac for use in inductive and motor load applications. These modifications have been implemented in the Hi-Com range of devices from Philips Semiconductors. The devices can be used in all typical motor control applications without the need for a snubber circuit. The commutation capability of the devices is well in excess of the operating conditions in typical applications.

As the loss of the fourth trigger quadrant can usually be tolerated in most designs, Hi-Com triacs can be used in existing motor control applications without the snubber network required for a standard device. This gives the designer significant savings in design simplicity, board space and system cost.

# FACTSHEET 014. USING Hi-Com TRIACS

Issue date September 1995 Document number 9397 750 00316

Hi-Com triacs from Philips Semiconductors are specifically designed to give superior triac commutation performance in the control of motors for domestic equipment and tools. These devices are suitable for use with a wide variety of motor and inductive loads without the need for a snubber. The use of a Hi-Com triac greatly simplifies circuit design and gives significant cost savings to the designer.

This product information sheet explains how the need for a triac snubber arises and how the superior performance of Hi-Com triacs removes design limitations of standard devices. The Hi-Com range is summarised in Table 1.

## Triac commutation

For resistive loads the device current is in phase with the line voltage. Under such conditions triac turn-off (commutation) occurs at the voltage "zero-crossover" point. This is not a very severe condition for triac commutation: the slow rising $dV_{COM}/dt$ gives time for the triac to turn off (commutate) easily.

The situation is quite different with inductive or motor loads. For these circuits, conduction current lags behind the line voltage as shown in Fig. 1. When triac commutation occurs, the rate of rise of voltage in the opposite direction can be very rapid and is governed by the circuit and device characteristics. This high $dV_{COM}/dt$ means there is a much higher probability of charge carriers in the device re-triggering the triac and causing a commutation failure.

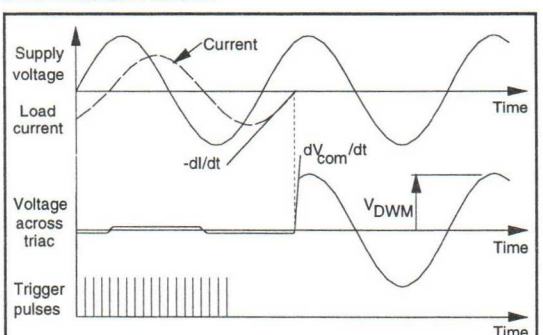



Fig. 1. Triac commutation waveforms (inductive load).

## Hi-Com triacs

Hi-Com triacs are specifically designed for use with AC inductive loads such as motors. As commutation capability is not an issue for resistive load applications then standard triacs are usually the most appropriate devices for these applications. The significant advantage of a Hi-Com triac is that it can withstand a very high rate of rise of reapplied voltage at commutation. This removes the requirement for a snubber circuit in inductive load circuits. An additional advantage of the Hi-Com design is that the off-state (static) $dV_D/dt$ capability of the device is also significantly improved.

When using Hi-Com triacs in inductive load applications, the trigger circuit cannot trigger the device in the fourth (3+) quadrant (Fig. 2). Fortunately the vast majority of circuit designs do not require this mode of operation and so are suitable for use with Hi-Com triacs without modification. The circuit of Fig. 3 is a typical example of the simplest type of trigger circuit. Hi-Com triacs are equally also suitable for use with microcontroller trigger circuits.

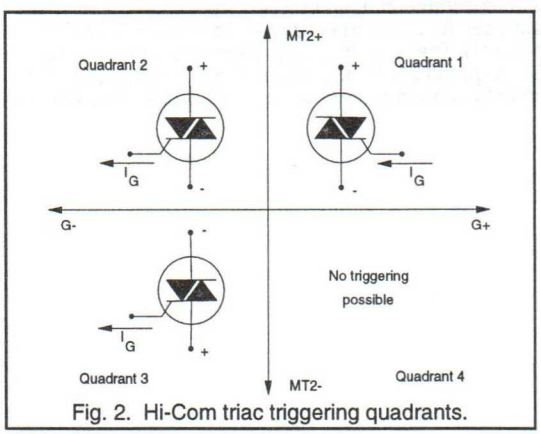



Fig. 2. Hi-Com triac triggering quadrants.

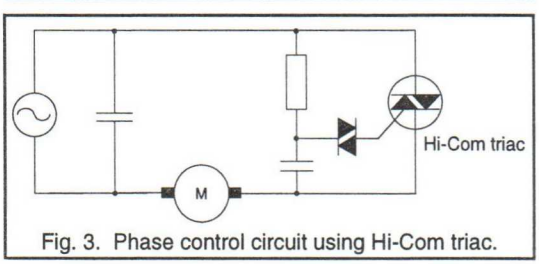



Fig. 3. Phase control circuit using Hi-Com triac.

## Device limiting values

### i) Trigger current, $I_{GT}$

Trigger current for the Hi-Com triacs is in the range 2mA to 50mA. This means that gate currents due to noise that are below 2mA in amplitude can be guaranteed not to trigger the devices. This gives the devices a noise immunity feature that is important in many applications. The trigger current delivered by the trigger circuit must be greater than 50mA under all conditions in order to guarantee triggering of the device when required. As discussed above, triggering is only possible in the 1+, 1- and 3- quadrants.

**ii) Rate of change of current, $dI_{com}/dt$**

Hi-Com triacs do not require a snubber network providing that the rate of change of current prior to commutation is less than the rating specified in the device data sheet. This $dI_{com}/dt$ limit is well in excess of the currents that occur in the device under normal operating condition, during transients such as start-up and faults such as the stalled motor condition.

As an example, for the 12A Hi-Com triacs the limit commutating current is typically 24A/ms at 125°C. This corresponds to an RMS current of 54A at 50Hz. For the 16A Hi-Com triacs the limit commutating current is typically 28A/ms at 125°C. This corresponds to an RMS current of 63A at 50Hz. Typical stall currents for an 800W domestic appliance motor are in the range 15A to 20A and so the commutation capability of the Hi-Com triacs is well above the requirement for this type of application.

**Conclusions**

The Hi-Com range of devices from Philips Semiconductors can be used in all typical motor control applications without the need for a snubber circuit. The commutation capability of the devices is well in excess of the operating conditions in typical applications.

As the loss of the fourth trigger quadrant can usually be tolerated in most designs, Hi-Com triacs can be used in existing motor control applications. By removing the snubber the use of a Hi-Com triac gives the designer significant savings in design simplicity, board space and system cost.

| | $V_{DRM}$ (V) | $I_{T(RMS)}$ (A) | $I_{GT}$ (mA) | $dV_D/dt$ (V/µs) | $dI_{com}/dt$ (A/ms) | $dI_T/dt$ (A/µs) | Package |
|---|---|---|---|---|---|---|---|
| BTA208-600B | 600 | 8 | 2 - 50 | 1000 | 14 | 100 | SOT78 |
| BTA208-800B | 800 | 8 | 2 - 50 | 1000 | 14 | 100 | SOT78 |
| BTA208X-600B | 600 | 8 | 2 - 50 | 1000 | 14 | 100 | SOT186A |
| BTA208X-800B | 800 | 8 | 2 - 50 | 1000 | 14 | 100 | SOT186A |
| BTA212-600B | 600 | 12 | 2 - 50 | 1000 | 24 | 100 | SOT78 |
| BTA212-800B | 800 | 12 | 2 - 50 | 1000 | 24 | 100 | SOT78 |
| BTA212X-600B | 600 | 12 | 2 - 50 | 1000 | 24 | 100 | SOT186A |
| BTA212X-800B | 800 | 12 | 2 - 50 | 1000 | 24 | 100 | SOT186A |
| BTA216-600B | 600 | 16 | 2 - 50 | 1000 | 28 | 100 | SOT78 |
| BTA216-800B | 800 | 16 | 2 - 50 | 1000 | 28 | 100 | SOT78 |
| BTA216X-600B | 600 | 16 | 2 - 50 | 1000 | 28 | 100 | SOT186A |
| BTA216X-800B | 800 | 16 | 2 - 50 | 1000 | 28 | 100 | SOT186A |
| BTA225-600B | 600 | 25 | 2 - 50 | 1000 | 44 | 100 | SOT78 |
| BTA225-800B | 800 | 25 | 2 - 50 | 1000 | 44 | 100 | SOT78 |

Table 1. Hi-Com triac range in leaded packages. (SOT78 <=> TO220.)

# FACTSHEET 067. LOGIC LEVEL AND SENSITIVE GATE TRIACS

Issue date March 1996 Document number 9397 750 00759

## Introduction

Triacs have been available since the early 1970s. They could be regarded as a mature technology. However, they remain an extremely popular power control device for AC mains applications because of their low cost and the simplicity of their control circuits. Nothing can better them in these two respects. There has even been an upsurge in their use in the 1990s due partly to the proliferation of domestic appliances with electronic controls. Common examples of these include air and water heaters, vacuum cleaners, refrigerators, washing machines, dishwashers and most small kitchen appliances.

Despite their maturity, triacs have not "stood still" since their first invention. They have evolved to meet the changing demands of the applications. One important change in triac requirements is the gate sensitivity specification $I_{GT}$. Early triac trigger circuits were built using discrete components which could supply high currents up to 100mA peak or more. Triacs therefore did not require sensitive gates. This is still relevant today for phase control circuits which use a diac such as the BR100/03 to trigger the triac. However, Integrated Circuit control is becoming ever more popular for two main reasons:

1. Stringent Electro Magnetic Compatibility regulations limit the harmonic currents that can be drawn from the mains and also limit the amount of Radio Frequency Interference that can be generated by appliances. This requires the use of either a dedicated zero crossing triac power control IC such as the OM1654 or OM1682 from Philips Australia, or a microcontroller which has been programmed to perform a similar function in which a high harmonic and RFI-generating phase control circuit is replaced by an electrically "quieter" alternative. An example might be Binary Rate Modulation power control, where varying full and half mains cycles are conducted symmetrically to ensure very low harmonic currents and zero DC component in the current waveform.

2. More intelligent appliance controls are now being demanded such as remote control, soft start, variable timing, automatic power ramp-up & ramp-down, and power reduction after full power startup for energy conservation measures (applicable to refrigerator compressors in particular). These would be very complicated, expensive or even impossible to implement using discrete components.

Integrated circuits such as the dedicated triac controller ICs and microcontrollers possess a limited drive current capability which ranges from 10mA to 15mA typically. Moreover, since the IC's supply is usually derived from the mains via a resistive/capacitive dropper and simple half wave rectifier, power dissipation in the resistor can very easily become unacceptably high if the load current is not kept to an absolute minimum. This means that the average current demand from the IC's power supply must usually be minimised. This can impose a limit on the current amplitude and duration available for triggering the triac. This is even more relevant if several triacs are controlled by one microcontroller. Examples where this holds true are fridge freezers and washing machines. This can mean that the drive current available for triac triggering is even less than the 10mA to 15mA suggested above.

Figure 1 shows a simple IC-triac arrangement. The 5.6V zener diode combined with the forward voltage drop of the rectifier diode produce an IC supply close to 5V. The advantages of connecting the zener as shown instead of directly across the IC are that full wave current is drawn from the mains supply (no DC component), and the forward conduction of the zener means that the rectifier never has to support full mains voltage. A cheap, low voltage diode can therefore be used. Attention must be paid, however, to the additional power dissipation in the resistor due to the forward zener current.

These IC-triac power control applications could not be implemented without sensitive triacs. Philips logic level D series and sensitive gate E series triacs are designed to meet fully the requirements in this burgeoning market. For a full selection guide of available types, see Tables 1 and 2.

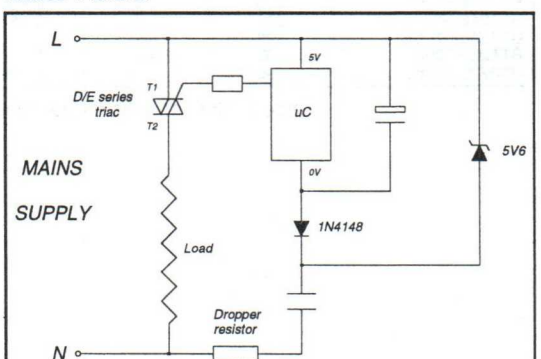



Fig. 1. A typical microcontroller / triac arrangement.

## Gate trigger current $I_{GT}$

Philips D and E series triacs are specified to trigger in all four quadrants. However, a feature of four-quadrant triacs is that they are less sensitive and more difficult to trigger in the 4th (T2-, G+) quadrant. (For example, for the D series, max $I_{GT}$ in quadrant 1,2,3,4 is 5,5,5,10mA, and for the E series it is 10,10,10,25mA.) The ability of triacs to support a high rate of rise of load current ($dI_T/dt$) after turn-on is also limited in the 4th quadrant. ($dI_T/dt$ is 10A/µs compared with 50A/µs in the other three quadrants). For these two reasons, operation in the 4th quadrant is not recommended if it can be avoided.

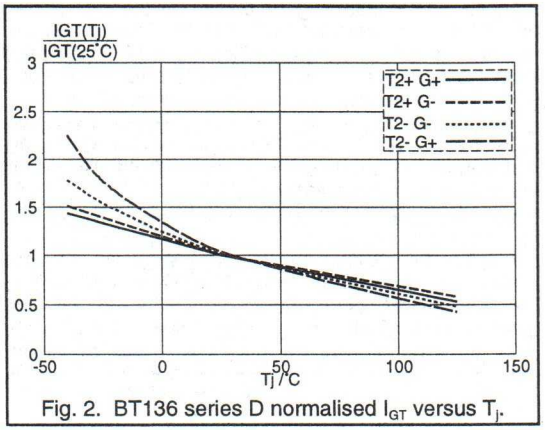



Fig. 2. BT136 series D normalised $I_{GT}$ versus $T_j$.

Since the control IC operates on a single rail supply (usually +5V), its outputs are unipolar. It can be referenced to the mains circuit in order to source current (positive gate drive) or to sink current (negative gate drive). Since 4th quadrant triggering should be avoided, optimum performance will be obtained with negative gate current - i.e operation in the 2nd (T2+, G-) and 3rd (T2-, G-) quadrants (see Fig. 1).

A triac's $I_{GT}$ varies with junction temperature. At lower temperature the $I_{GT}$ increases. It is therefore important to ensure that the circuit supplies enough gate current at the lowest expected operating temperature for guaranteed triggering. Figure 2 shows an example of normalised $I_{GT}$ versus $T_j$ for the BT136 series D.

**Latching current $I_L$**

If the triac is triggered by a gate current at the beginning of a mains half cycle, the load current will build up gradually from zero. The gate current must not be removed before the triac is latched ON otherwise it will return to the blocking state. Latching occurs when the load current reaches $I_L$. The gate pulse must therefore be present until the load current has reached $I_L$.

Just as for $I_{GT}$, $I_L$ also increases at lower temperature. The gate pulse duration must be specified at the lowest expected operating temperature for guaranteed triggering. Figure 3 shows an example of normalised $I_L$ versus $T_j$ for the BT136 series D.

How quickly the load current reaches the triac's $I_L$ will depend on the peak load current and mains frequency. Taken to the extreme case, if the load current is so low that its peak value is equivalent to $I_L$, it will take one quarter cycle, or 5ms for 50Hz mains, before the triac is latched and the gate pulse can cease.

It is also important to be aware that higher current triacs have a higher $I_L$. This could compound problems or even lead to the triac never latching ON if the load current is lower than the triac's $I_L$. So, apart from the higher component cost, it would not be a good idea to use a triac whose current rating is very much higher than the load current when a lower current type is available. Tables 1 and 2 illustrate how $I_L$ varies with the triggering quadrant and triac current rating.

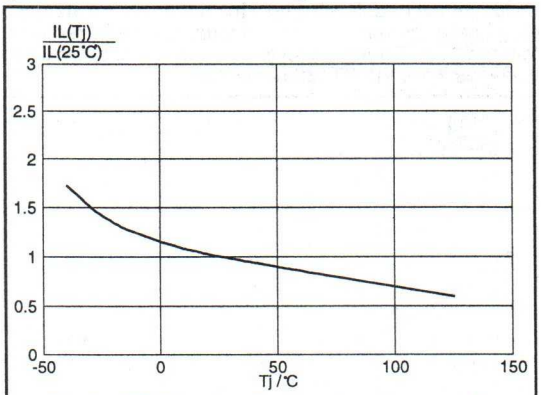



Fig. 3. BT136 series D normalised $I_L$ versus $T_j$.

**Minimum triac drive current calculation**

Because the current demand must be minimised in many IC applications, it is necessary to calculate the gate pulse duration to be just long enough to guarantee triac triggering while avoiding unnecessary burden on the IC's power supply. The time to reach $I_L$, hence the gate pulse duration, can be calculated using the equation:

$I_L = I_{pk} \times \sin(2\pi ft)$. Transposing gives:

$$t = 1/(2\pi f) \times \sin^{-1}(I_L/I_{pk}).$$

The average gate current supplied by the IC is calculated by multiplying its peak gate current with t/T. Hence:

$$I_{G(ave)} = I_{G(pk)} \times t/T.$$

$I_L$ = triac latching current at the lowest expected operating temperature,
$I_{pk}$ = peak load current,
t = gate pulse duration,
T = gate pulse cycle time.

Note:- Since triac latching current is higher in the 2nd and 4th quadrants, and normal operation for IC triggering is in the 2nd and 3rd quadrants, the gate current calculations must always be based on the worst case quadrant 2 $I_L$ condition.

If the load current is very low and the necessary gate pulse duration imposes too great a burden on the IC's power supply, triggering could be delayed for a few degrees to allow the supply voltage to build up a little. The time to reach $I_L$ will then be shortened by the delay time (true for resistive loads). Now that switching occurs further from the zero crossing, there will be a slightly increased risk of RFI generation, even if the load current is very low as in this case. RFI measurements will show if filtering is necessary to meet the relevant EMC legislation.

**Holding current $I_H$**

As the load current reduces towards the end of a mains half cycle, a current, $I_H$, will be reached when the triac is no longer latched. It will cease to conduct in the absence of a gate current. $I_H$ also increases with reducing temperature. Figure 4 shows an example of normalised $I_H$ versus $T_j$ for the BT136 series D.

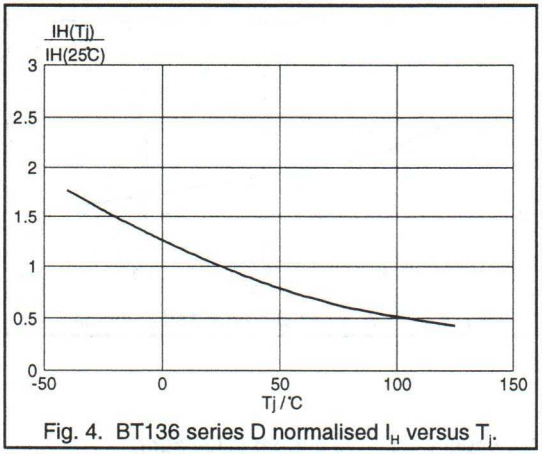



Fig. 4. BT136 series D normalised $I_H$ versus $T_j$.

In some IC applications where the triac is used as a power switch, for example a precision electronic thermostat for a refrigerator compressor, continuous conduction must be maintained through the current zero crossing. (This is essential to prevent glitches and RFI generation.) Continuous conduction is achieved by monitoring the load current and applying a gate pulse before the triac's $I_H$ is reached, and maintaining the pulse until the current has passed through zero and risen to the triac's $I_L$ in the alternate quadrant. This condition must be met at the lowest expected operating temperature for continuous glitch-free conduction under worst case conditions.

$I_H$ increases for the larger E series triacs. The most sensitive D series triacs, however, are designed to maintain a consistent, low $I_H$ of 10mA @ 25°C even for the higher 8A current rating.

Figure 5 illustrates triac load current zero crossing and the minimum gate pulse required for continuous conduction through the max $I_H$ and $I_L$ points. The diagram illustrates how $I_H$ remains constant in different quadrants. The point made earlier about how $I_L$ varies in different quadrants is illustrated by the higher $I_L$ in the 2nd quadrant (T2+, G-). $I_G$ duration must meet this worst case condition.

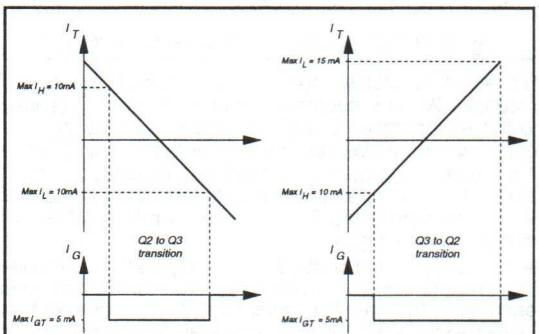



Fig. 5. Relationship between $I_L$, $I_H$ and $I_{GT}$ for BT136 series D at 25°C.

**Selection guide**

| Type number | $I_{T(RMS)}$ (A) | $V_{DRM}$ (V) | $I_{GT}$ max (mA) | $I_L$ max (mA) | $I_H$ max (mA) | Package |
|---|---|---|---|---|---|---|
| BT134W-...D | 1 | 500,600 | 5,5,5,10 | 10,15,10,15 | 10 | SOT223 |
| BT134-...D | 4 | | | | | SOT82 |
| BT136-...D | 4 | | | | | SOT78 |
| BT136F-...D | 4 | | | | | SOT186 |
| BT136X-...D | 4 | | | | | SOT186A |
| BT137-...D | 8 | 500,600 | 5,5,5,10 | 15,20,15,20 | 10 | SOT78 |
| BT137F-...D | 8 | | | | | SOT186 |
| BT137X-...D | 8 | | | | | SOT186A |

Tabe 1. Philips D series logic level triacs.

| Type number | $I_{T(RMS)}$ (A) | $V_{DRM}$ (V) | $I_{GT}$ max (mA) | $I_L$ max (mA) | $I_H$ max (mA) | Package |
|---|---|---|---|---|---|---|
| BT134W-...E | 1 | 500,600 | 10,10,10,25 | 15,20,15,20 | 15 | SOT223 |
| BT134-...E | 4 | 500,600,800 | | | | SOT82 |
| BT136-...E | 4 | | | | | SOT78 |
| BT136F-...E | 4 | | | | | SOT186 |
| BT136X-...E | 4 | | | | | SOT186A |
| BT137-...E | 8 | 500,600,800 | 10,10,10,25 | 25,35,25,35 | 20 | SOT78 |
| BT137F-...E | 8 | | | | | SOT186 |
| BT137X-...E | 8 | | | | | SOT186A |
| BT138-...E | 12 | 500,600,800 | 10,10,10,25 | 30,40,30,40 | 30 | SOT78 |
| BT138F-...E | 12 | | | | | SOT186 |
| BT138X-...E | 12 | | | | | SOT186A |
| BT139-...E | 16 | | | | | SOT78 |
| BT139F-...E | 16 | | | | | SOT186 |
| BT139X-...E | 16 | | | | | SOT186A |

Table 2. Philips E series sensitive gate triacs.

NOTE: SOT78 is equivalent to TO220AB.

# THYRISTORS AND TRIACS - TEN GOLDEN RULES FOR SUCCESS IN YOUR APPLICATION

Issue date May 1996 Document number 9397 750 00812

This Technical Publication aims to provide an interesting, descriptive and practical introduction to the golden rules that should be followed in the successful use of thyristors and triacs in power control applications.

## Thyristor

A thyristor is a controlled rectifier where the unidirectional current flow from anode to cathode is initiated by a small signal current from gate to cathode.

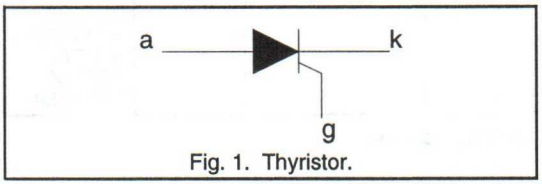



Fig. 1. Thyristor.

The thyristor's operating characteristic is shown in Fig. 2.

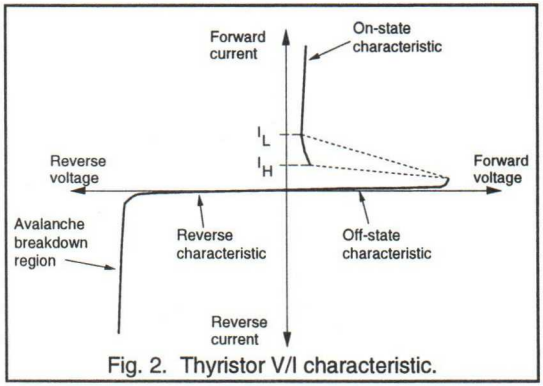



Fig. 2. Thyristor V/I characteristic.

## Turn-on

A thyristor is turned on by making its gate positive with respect to its cathode, thereby causing current flow into the gate. When the gate voltage reaches the threshold voltage $V_{GT}$ and the resulting current reaches the threshold current $I_{GT}$, within a very short time known as the gate-controlled turn-on time, $t_{gt}$, the load current can flow from 'a' to 'k'. If the gate current consists of a very narrow pulse, say less than 1µs, its peak level will have to increase for progressively narrower pulse widths to guarantee triggering.

When the load current reaches the thyristor's latching current $I_L$, load current flow will be maintained even after removal of the gate current. As long as adequate load current continues to flow, the thyristor will continue to conduct without the gate current. It is said to be latched ON.

Note that the $V_{GT}$, $I_{GT}$ and $I_L$ specifications given in data are at 25 °C. These parameters will increase at lower temperatures, so the drive circuit must provide adequate voltage and current amplitude and duration for the lowest expected operating temperature.

*Rule 1. To turn a thyristor (or triac) ON, a gate current ≥ $I_{GT}$ must be applied until the load current is ≥ $I_L$. This condition must be met at the lowest expected operating temperature.*

Sensitive gate thyristors such as the BT150 can be prone to turn-on by anode to cathode leakage current at high temperatures. If the junction temperature $T_j$ is increased above $T_j$ max, a point will be reached where the leakage current will be high enough to trigger the thyristor's sensitive gate. It will then have lost its ability to remain in the blocking state and conduction will commence without the application of an external gate current.

This method of spurious turn-on can be avoided by using one or more of the following solutions:

1. Ensure that the temperature does not exceed $T_j$ max.
2. Use a thyristor with a less sensitive gate such as the BT151, or reduce the existing thyristor's sensitivity by including a gate-to-cathode resistor of 1kΩ or less.
3. If it is not possible to use a less sensitive thyristor due to circuit requirements, apply a small degree of reverse biasing to the gate during the 'off' periods. This has the effect of increasing $I_L$. During negative gate current flow, particular attention should be paid to minimising the gate power dissipation.

## Turn-off (commutation)

In order to turn the thyristor off, the load current must be reduced below its holding current $I_H$ for sufficient time to allow all the mobile charge carriers to vacate the junction. This is achieved by "forced commutation" in DC circuits or at the end of the conducting half cycle in AC circuits. (Forced commutation is when the load circuit causes the load current to reduce to zero to allow the thyristor to turn off.) At this point, the thyristor will have returned to its fully blocking state.

If the load current is not maintained below $I_H$ for long enough, the thyristor will not have returned to the fully blocking state by the time the anode-to-cathode voltage rises again. It might then return to the conducting state without an externally-applied gate current.

Note that $I_H$ is also specified at room temperature and, like $I_L$, it reduces at higher temperatures. The circuit must therefore allow sufficient time for the load current to fall below $I_H$ at the maximum expected operating temperature for successful commutation.

*Rule 2. To turn off (commutate) a thyristor (or triac), the load current must be < $I_H$ for sufficient time to allow a return to the blocking state. This condition must be met at the highest expected operating temperature.*

### Triac

A triac can be regarded as a "bidirectional thyristor" because it conducts in both directions. For standard triacs, current flow in either direction between the main terminals MT1 and MT2 is initiated by a small signal current applied between MT1 and the gate terminal.

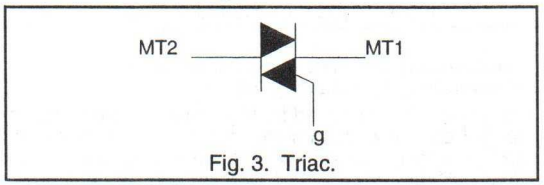


Fig. 3. Triac.

### Turn-on

Unlike thyristors, standard triacs can be triggered by positive or negative current flow between the gate and MT1. (The rules for $V_{GT}$, $I_{GT}$ and $I_L$ are the same as for thyristors. See Rule 1.) This permits triggering in four "quadrants" as summarised in Fig. 4.

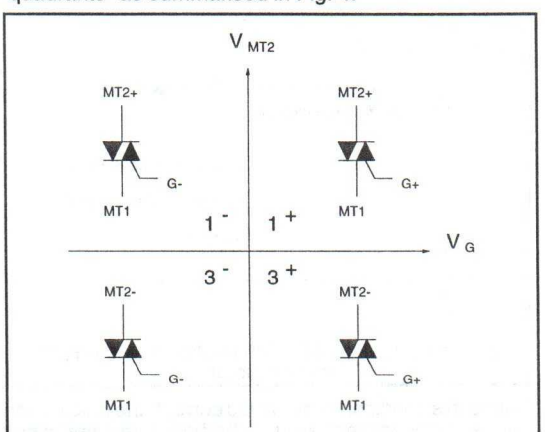


Fig. 4. Triac triggering quadrants.

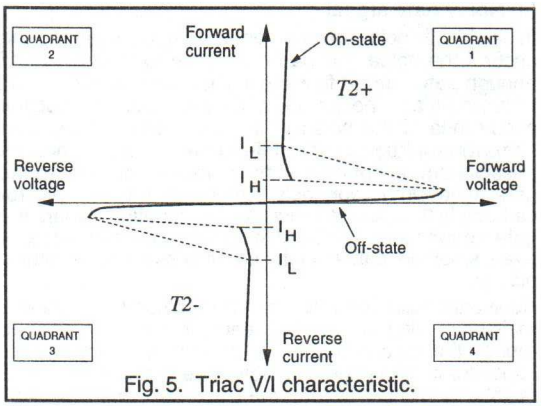


Fig. 5. Triac V/I characteristic.

Where the gate is to be triggered by DC or unipolar pulses at zero-crossing of the load current, negative gate current is to be preferred for the following reasons.

The internal construction of the triac means that the gate is more remote from the main current-carrying region when operating in the $3^+$ quadrant. This results in:

1. Higher $I_{GT}$ -> higher peak $I_G$ required,
2. Longer delay between $I_G$ and the commencement of load current flow -> longer duration of $I_G$ required,
3. Much lower $dI_T/dt$ capability -> progressive gate degradation can occur when controlling loads with high initial dI/dt (e.g. cold incandescent lamp filaments),
4. Higher $I_L$ (also true for $1^-$ operation) -> longer $I_G$ duration might be needed for very small loads when conducting from the beginning of a mains half cycle to allow the load current to reach the higher $I_L$.

In standard AC phase control circuits such as lamp dimmers and domestic motor speed controls, the gate and MT2 polarities are always the same. This means that operation is always in the $1^+$ and $3^-$ quadrants where the triac's switching parameters are the same. This results in symmetrical triac switching where the gate is at its most sensitive.

Note:- The $1^+$, $1^-$, $3^-$ and $3^+$ notation for the four triggering quadrants is used for brevity instead of writing "MT2+, G+" for $1^+$, etc. It is derived from the graph of the triac's V/I characteristic. Positive MT2 corresponds with positive current flow into MT2, and vice versa (see Fig. 5). Hence, operation is in quadrants 1 and 3 only. The + and - superscripts refer to inward and outward gate current respectively.

*Rule 3. When designing a triac triggering circuit, avoid triggering in the $3^+$ quadrant (MT2-, G+) where possible.*

### Alternative turn-on methods

There are undesirable ways a triac can be turned on. Some are benign, while some are potentially destructive.

**(a) Noisy gate signal**

In electrically noisy environments, spurious triggering can occur if the noise voltage on the gate exceeds $V_{GT}$ and enough gate current flows to initiate regenerative action within the triac. The first line of defence is to minimise the occurrence of the noise in the first place. This is best achieved by keeping the gate connections as short as possible and ensuring that the common return from the gate drive circuit connects directly to the MT1 pin (or cathode in the case of a thyristor). In situations where the gate connections are hard wired, twisted pair wires or even shielded cable might be necessary to minimise pickup.

Additional noise immunity can be provided by adding a resistor of 1kΩ or less between the gate and MT1 to reduce the gate sensitivity. If a high frequency bypass capacitor is also used, it is advisable to include a series resistor between it and the gate to minimise peak capacitor currents through the gate and minimise the possibility of overcurrent damage to the triac's gate area. **Alternatively, use a series H triac (e.g. BT139-600H). These are insensitive types with 10mA min $I_{GT}$ specs which are specifically designed to provide a high degree of noise immunity.**

*Rule 4. To minimise noise pickup, keep gate connection length to a minimum. Take the return directly to MT1 (or cathode). If hard wired, use twisted pair or shielded cable. Fit a resistor of 1kΩ or less between gate and MT1. Fit a bypass capacitor in conjunction with a series resistor to the gate.*
*Alternatively, use an insensitive series H triac.*

**(b) Exceeding the max rate of change of commutating voltage $dV_{COM}/dt$**

This is most likely to occur when driving a highly reactive load where there is substantial phase shift between the load voltage and current waveforms. When the triac commutates as the load current passes through zero, the voltage will not be zero because of the phase shift (see Fig. 6). The triac is then suddenly required to block this voltage. The resulting rate of change of commutating voltage can force the triac back into conduction if it exceeds the permitted $dV_{COM}/dt$. This is because the mobile charge carriers have not been given time to clear the junction.

The $dV_{COM}/dt$ capability is affected by two conditions:-
1. The rate of fall of load current at commutation, $dI_{COM}/dt$. Higher $dI_{COM}/dt$ lowers the $dV_{COM}/dt$ capability.
2. The junction temperature $T_j$. Higher $T_j$ lowers the $dV_{COM}/dt$ capability.

If the triac's $dV_{COM}/dt$ is likely to be exceeded, false triggering can be avoided by use of an RC snubber across MT1-MT2 to limit the rate of change of voltage. Common values are 100Ω carbon composition resistor, chosen for its surge current handling, and 100nF. **Alternatively, use a Hi-Com triac.**

Note that the resistor should never be omitted from the snubber because there would then be nothing to prevent the capacitor from dumping its charge into the triac and creating damaging $dI_T/dt$ during unfavourable turn-on conditions.

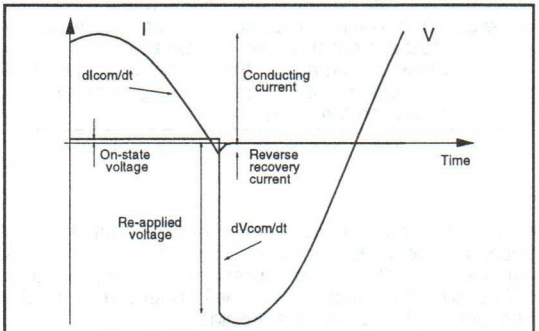



Fig. 6. Triac $dI_{COM}/dt$ and $dV_{COM}/dt$.

**(c) Exceeding the max rate of change of commutating current $dI_{COM}/dt$**

Higher $dI_{COM}/dt$ is caused by higher load current, higher mains frequency (assuming sinewave current) or non sinewave load current. A well known cause of non sinewave load current and high $dI_{COM}/dt$ is rectifier-fed inductive loads. These can often result in commutation failure in standard triacs as the supply voltage falls below the back EMF of the load and the triac current collapses suddenly to zero. The effect of this is illustrated in Fig. 7.

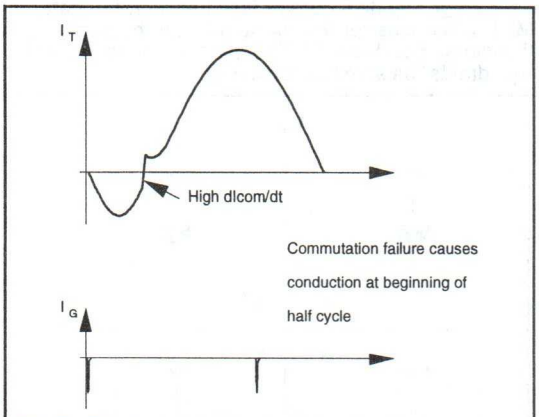



Fig. 7. Effects of rectifier-fed inductive load on phase control circuit.

During this condition of zero triac current, the load current will be "freewheeling" around the bridge rectifier circuit. Loads of this nature can generate such high $dI_{COM}/dt$ that the triac cannot support even the gentle reapplied dV/dt of a 50Hz waveform rising from zero volts. There will then be no benefit in adding a snubber across the triac because

$dV_{COM}/dt$ is not the problem. The $dI_{COM}/dt$ will have to be limited by adding an inductor of a few mH in series with the load. **Alternatively, use a Hi-Com triac.**

**(d) Exceeding the max rate of change of off-state voltage $dV_D/dt$**

If a very high rate of change of voltage is applied across a non-conducting triac (or sensitive gate thyristor in particular) without exceeding its $V_{DRM}$ (see Fig. 8), internal capacitive current can generate enough gate current to trigger the device into conduction. Susceptibility is increased at high temperature.

Where this is a problem, the $dV_D/dt$ must be limited by an RC snubber across MT1 and MT2 (or anode and cathode). **In the case of triacs, using Hi-Com types can yield benefits.**

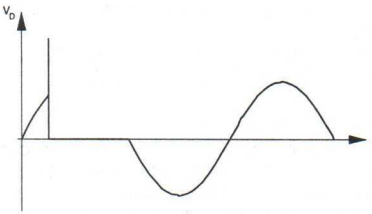



Fig. 8. Triac turn-on by exceeding $dV_D/dt$.

*Rule 5. Where high $dV_D/dt$ or $dV_{COM}/dt$ are likely to cause a problem, fit an RC snubber across MT1 and MT2.*
*Where high $dI_{COM}/dt$ is likely to cause a problem, fit an inductor of a few mH in series with the load.*
*Alternatively, use a Hi-Com triac.*

**(e) Exceeding the repetitive peak off-state voltage $V_{DRM}$**

If the MT2 voltage exceeds $V_{DRM}$ such as might occur during severe and abnormal mains transient conditions, MT2-MT1 leakage will reach a point where the triac will spontaneously break over into conduction (see Fig. 9).

If the load permits high inrush currents to flow, extremely high localised current density can occur in the small area of silicon that is conducting. This can lead to burnout and destruction of the die. Incandescent lamps, capacitive loads and crowbar protection circuits are likely causes of high inrush currents.

Turn-on by exceeding the triac's $V_{DRM}$ or $dV_D/dt$ is not necessarily the main threat to its survival. It's the $dI_T/dt$ that follows which is most likely to cause the damage. Due to the time required for conduction to spread out over the whole junction, the permitted $dI_T/dt$ is lower than if the triac is correctly turned on by a gate signal. If the $dI_T/dt$ can be limited during these conditions to this lower value, which is given in data, the triac is more likely to survive. This could be achieved by fitting a non saturable (air cored) inductor of a few µH in series with the load.

If the above solution is unacceptable or impractical, an alternative solution would be to provide additional filtering and clamping to prevent the spikes reaching the triac. This would probably involve the use of a Metal Oxide Varistor as a "soft" voltage clamp across the supply, with series inductance followed by parallel capacitance upstream of the MOV.

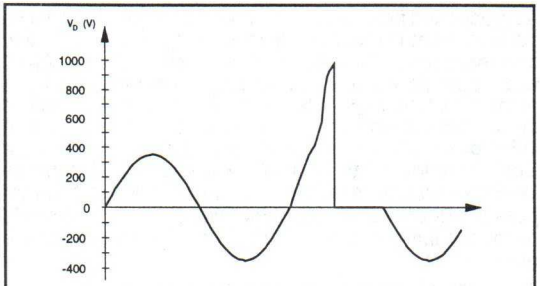



Fig. 9. Triac turn-on by exceeding $V_{DRM}$.

Doubts have been expressed by some manufacturers over the reliability of circuits which use MOVs across the mains, since they have been known to go into thermal runaway in high ambient temperatures and fail catastrophically. This is due to the fact that their operating voltage possesses a marked negative temperature coefficient. However, if the recommended voltage grade of 275V RMS is used for 230V mains, the risk of MOV failure should be negligible. Such failures are more likely if 250V RMS MOVs are used, which are underspecified for 230V RMS use at high ambient temperatures.

*Rule 6. If the triac's $V_{DRM}$ is likely to be exceeded during severe mains transients, employ one of the following measures:*
*Limit high $dI_T/dt$ with a non saturable inductor of a few µH in series with the load;*
*Use a MOV across the mains in combination with filtering on the supply side.*

**Turn-on $dI_T/dt$**

When a triac or thyristor is triggered into conduction by the correct method via its gate, conduction begins in the die area immediately adjacent to the gate, then quickly spreads to cover the whole active area. This time delay imposes a limit on the permissible rate of rise of load current. A $dI_T/dt$ which is too high can cause localised burnout. An MT1-MT2 short will be the result.

If triggering in the $3^+$ quadrant, an additional mechanism further reduces the permitted $dI_T/dt$. It is possible to momentarily take the gate into reverse avalanche breakdown during the initial rapid current rise. This might not lead to immediate failure. Instead, there would be progressive burnout of the gate-MT1 shorting resistance after repeated exposure. This would show itself by a progressive increase in $I_{GT}$ until the triac will no longer trigger. Sensitive triacs are likely to be the most susceptible. Hi-Com triacs are not affected as they do not operate in the 3+ quadrant.

The $dI_T/dt$ capability is affected by how fast the gate current rises ($dI_G/dt$) and the peak value of $I_G$. Higher values of $dI_G/dt$ and peak $I_G$ (without exceeding the gate power ratings) give a higher $dI_T/dt$ capability.

*Rule 7. Healthy gate drive and avoiding 3⁺ operation maximises the triac's $dI_T/dt$ capability.*

As mentioned previously, a common load with a high initial surge current is the incandescent lamp which has a low cold resistance. For resistive loads such as this, the $dI_T/dt$ would be at its highest if conduction commenced at a peak of the mains voltage. If this is likely to exceed the triac's $dI_T/dt$ rating, it should be limited by the inclusion of an inductor of a few µH or even a Negative Temperature Coefficient thermistor in series with the load. Again, the inductor must not saturate during the maximum current peak. If it does, its inductance would collapse and it would no longer limit the $dI_T/dt$. An air cored inductor meets the requirement.

A more elegant solution which could avoid the requirement for a series current-limiting device would be to use zero voltage turn-on. This would allow the current to build up more gradually from the beginning of the sinewave.

Note: It is important to rememember that zero voltage turn-on is only applicable to resistive loads. Using the same method for reactive loads where there is phase shift between voltage and current can cause "halfwaving" or unipolar conduction, leading to possible saturation of inductive loads, damagingly high peak currents and overheating. More advanced control employing zero current switching and / or variable trigger angle is required in this case.

*Rule 8. If the triac's $dI_T/dt$ is likely to be exceeded, an air cored inductor of a few µH or an NTC thermistor should be fitted in series with the load.*
*Alternatively, employ zero voltage turn-on for resistive loads.*

### Turn-off

Since triacs are used in AC circuits, they naturally commutate at the end of each half cycle of load current unless a gate signal is applied to maintain conduction from the beginning of the next half cycle. The rules for $I_H$ are the same as for the thyristor. See Rule 2.

### Hi-Com triac

Hi-Com triacs have a different internal construction to conventional triacs. One of the differences is that the two "thyristor halves" are better separated to reduce the influence that they have on each other. This has yielded two benefits:

1. Higher $dV_{COM}/dt$. This enables them to control reactive loads without the need for a snubber in most cases while still avoiding commutation failure. This reduces the component count, board size and cost, and eliminates snubber power dissipation.

2. Higher $dI_{COM}/dt$. This drastically improves the chances of successfully commutating higher frequency or non sinewave currents without the need for a $dI_{COM}/dt$-limiting inductor in series with the load.

3. Higher $dV_D/dt$. Triacs become more sensitive at high operating temperatures. The higher $dV_D/dt$ of Hi-Com triacs reduces their tendency to spurious dV/dt turn-on when in the blocking state at high temperature. This enables them to be used in high temperature applications controlling resistive loads, such as cooking or heating applications, where conventional triacs could not be used.

The different internal construction also means that 3⁺ triggering is not possible. This should not be a problem in the vast majority of cases because this is the least desirable and least used triggering quadrant, so direct substitution of a Hi-Com for an equivalent conventional triac will almost always be possible.

Hi-Com triacs are fully described in two Philips Factsheets:
Factsheet 013 - Understanding Hi-Com Triacs, and
Factsheet 014 - Using Hi-Com Triacs.

### Triac mounting methods

For small loads or very short duration load current (i.e. less than 1 second), it might be possible to operate the triac in free air. In most cases, however, it would be fixed to a heatsink or heat dissipating bracket.

The three main methods of clamping the triac to a heatsink are clip mounting, screw mounting and riveting. Mounting kits are available from many sources for the first two methods. Riveting is not a recommended method in most cases.

### Clip mounting

This is the preferred method for minimum thermal resistance. The clip exerts pressure on the plastic body of the device. It is equally suitable for the non-isolated packages (SOT82 and SOT78) and the isolated packages (SOT186 F-pack and the more recent SOT186A X-pack). Note: SOT78 is otherwise known as TO220AB.

### Screw mounting

1. An M3 screw mounting kit for the SOT78 package includes a rectangular washer which should be between the screw head and the tab. It should not exert any force on the plastic body of the device.
2. During mounting, the screwdriver blade should never exert force on the plastic body of the device.
3. The heatsink surface in contact with the tab should be deburred and flat to within 0.02mm in 10mm.
4. The mounting torque (with washer) should be between 0.55Nm and 0.8Nm.
5. Where an alternative exists, the use of self-tapping screws should be avoided due to the possible swelling of the heatsink material around the fixing hole. This could be detrimental to the thermal contact between device and heatsink. (See 3 above.) The uncontrollable mounting torque is also a disadvantage with this fixing method.
6. The device should be mechanically fixed before the leads are soldered. This minimises undue stress on the leads.

### Riveting

Pop riveting is not recommended unless great care is taken because the potentially severe forces resulting from such an operation can deform the tab and crack the die, rendering the device useless. In order to minimise rejects, the following rules should be obeyed if pop riveting:

1. The heatsink should present a flat, burr-free surface to the device.
2. The heatsink mounting hole diameter should be no greater than the tab mounting hole diameter.
3. The pop rivet should just be a clearance fit in the tab hole and heatsink mounting hole without free play.
4. The pop rivet should be fitted with its head, not the mandrel, on the tab side.
5. The pop rivet should be fitted at 90 degrees to the tab. (The rivet head should be in contact with the tab around its complete circumference.)
6. The head of the rivet should not be in contact with the plastic body of the device after riveting.
7. Mechanical fixing of the device and heatsink assembly to the PCB should be completed before the leads are soldered to minimise stressing of the leads.

*Rule 9. Avoid mechanical stress to the triac when fitting it to the heatsink. Fix, then solder. Never pop rivet with the rivet mandrel on the tab side.*

### Thermal resistance

Thermal resistance $R_{th}$ is the resistance to the flow of heat away from the junction. It is analogous to electrical resistance;

i.e. just as electrical resistance R = V/I, thermal resistance $R_{th} = T/P$,

where T is the temperature rise in Kelvin and P is the power dissipation in Watts. Therefore $R_{th}$ is expressed in K/W.

For a device mounted vertically in free air, the thermal resistance is dictated by the junction-to-ambient thermal resistance $R_{th\ j\text{-}a}$. This is typically 100K/W for the SOT82 package, 60K/W for the SOT78 package and 55K/W for the isolated F-pack and X-pack.

For a non isolated device mounted to a heatsink, the junction-to-ambient thermal resistance is the sum of the junction-to-mounting base, mounting base-to-heatsink and heatsink-to-ambient thermal resistances.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}mb} + R_{th\ mb\text{-}h} + R_{th\ h\text{-}a} \text{ (non isolated package).}$$

The use of heat transfer compound or sheet between the device and heatsink is always recommended. In the case of isolated packages, there is no reference made to "mounting base", since the $R_{th\ mb\text{-}h}$ is assumed to be constant and optimised with heat transfer compound. Therefore, the junction-to-ambient thermal resistance is the sum of the junction-to-heatsink and heatsink-to-ambient thermal resistances.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}h} + R_{th\ h\text{-}a} \text{ (isolated package).}$$

$R_{th\ j\text{-}mb}$ or $R_{th\ j\text{-}h}$ are fixed and can be found in data for each device.

$R_{th\ mb\text{-}h}$ is also given in the mounting instructions for several options of insulated and non-insulated mounting, with or without heatsink compound.

$R_{th\ h\text{-}a}$ is governed by the heatsink size and the degree of unrestricted air movement past it.

### Calculation of heatsink size

To calculate the required heatsink thermal resistance for a given triac and load current, we must first calculate the power dissipation in the triac using the following equation:

$$P = V_o \times I_{T(AVE)} + R_s \times I_{T(RMS)}^2.$$

Knee voltage $V_o$ and slope resistance $R_s$ are obtained from the relevant $V_T$ graph in data book SC03. If the values are not already provided, they can be obtained from the graph by drawing a tangent to the max $V_T$ curve. The point on the $V_T$ axis where the tangent crosses gives $V_o$, while the slope of the tangent $(V_T/I_T)$ gives $R_s$.

Using the thermal resistance equation given above:

$$R_{th\ j\text{-}a} = T/P.$$

The max allowable junction temperature rise will be when $T_j$ reaches $T_j$ max in the highest ambient temperature. This gives us T.

$R_{th\ j\text{-}a} = R_{th\ j\text{-}mb} + R_{th\ mb\text{-}h} + R_{th\ h\text{-}a}$. SC03 data gives us the values for $R_{th\ j\text{-}mb}$ and $R_{th\ mb\text{-}h}$ for our chosen mounting method, leaving $R_{th\ h\text{-}a}$ as the only unknown.

### Thermal impedance

The above calculations for thermal resistance are applicable to the steady state condition - that is for a duration greater than 1 second. This time is long enough for heat to flow from the junction to the heatsink. For current pulses or transients lasting for shorter than 1 second, however, heatsinking has progressively less effect. The heat is simply dissipated in the bulk of the device with very little reaching the heatsink. For transient conditions such as these, the junction temperature rise is governed by the device's junction-to-mounting base thermal impedance $Z_{th\ j\text{-}mb}$.

$Z_{th\ j\text{-}mb}$ decreases for decreasing current pulse duration due to reduced chip heating. As the duration increases towards 1 second, $Z_{th\ j\text{-}mb}$ increases to the steady state $R_{th\ j\text{-}mb}$ value.

The $Z_{th\ j\text{-}mb}$ curve for bidirectional and unidirectional current down to 10µs duration is shown for each device in the SC03 data book.

*Rule 10. For longterm reliability, ensure that the $R_{th\ j\text{-}a}$ is low enough to keep the junction temperature within $T_j$ max for the highest expected ambient temperature.*

### Range and packaging

Philips thyristors range from 0.8A in SOT54 (TO92) to 25A in SOT78 (TO220AB).

Philips triacs range from 1A in SOT223 to 25A in SOT78. Conventional types (4-quadrant triggering) and Hi-Com types (3-quadrant triggering) are available. SOT54 types are planned for 1996.

The smallest package is the surface mount SOT223 for the smaller thyristors and triacs (Fig. 10). The power dissipation is governed by the degree of heatsinking offered by the PCB onto which it is soldered.

The same respective chips are also available in SOT82 which is a non isolated package (Fig. 12). The improved heat removal of this package when heatsunk allows higher current ratings and improved power dissipations.

Figure 11 shows SOT54 in which the very smallest devices are mounted. Smaller chips than those accommodated by SOT223 go into this package, which offers the most compact non surface mount solution.

SOT78 is the most common non isolated package in which most of our devices are supplied (Fig. 13).

Figure 14 shows SOT186 (F-pack). This has been the traditional Philips isolated package. It offers an isolation voltage of 1,500V peak between device and heatsink under clean conditions.

The more recent SOT186A package (X-pack) shown in Fig. 15 possesses several advantages over the older type.

1. It has the same dimensions as the SOT78 package for pin spacing from the mounting surface, so it can directly replace SOT78 devices to provide isolation without the need for modification of the mounting arrangement.
2. It has no exposed metal at the top of the tab, and creepage distances from pins to heatsink are greater, so it can offer an improved true isolation of 2,500V RMS.
3. It is a fully encapsulated SOT78 replacement.

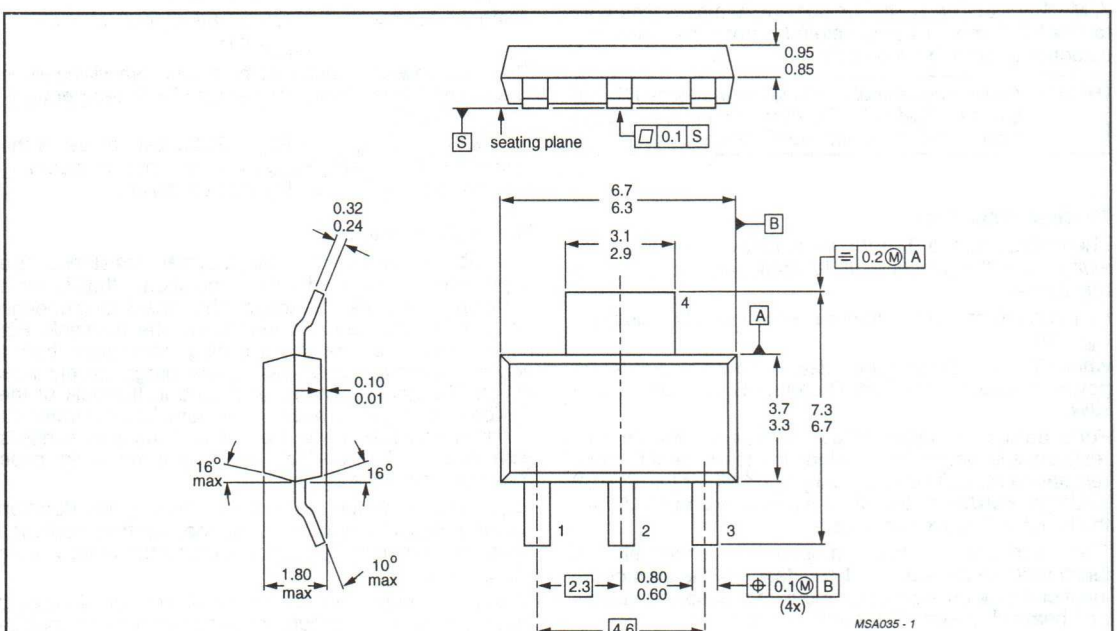



Fig. 10. SOT223.

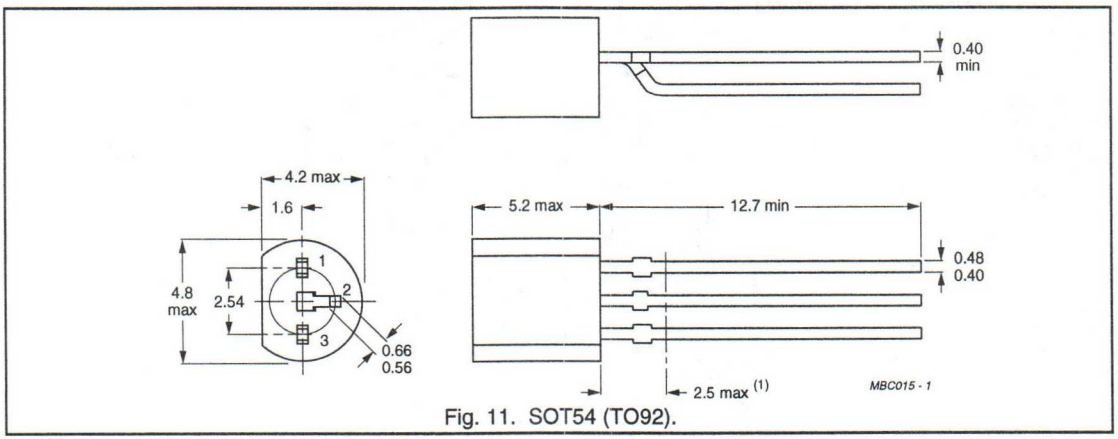



Fig. 11. SOT54 (TO92).

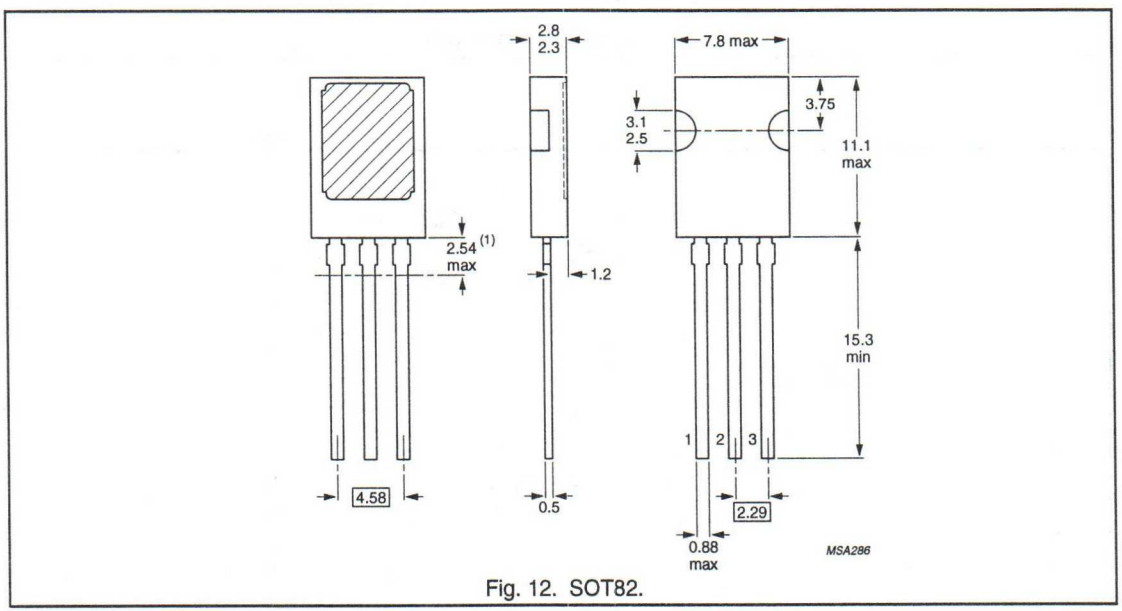



Fig. 12. SOT82.

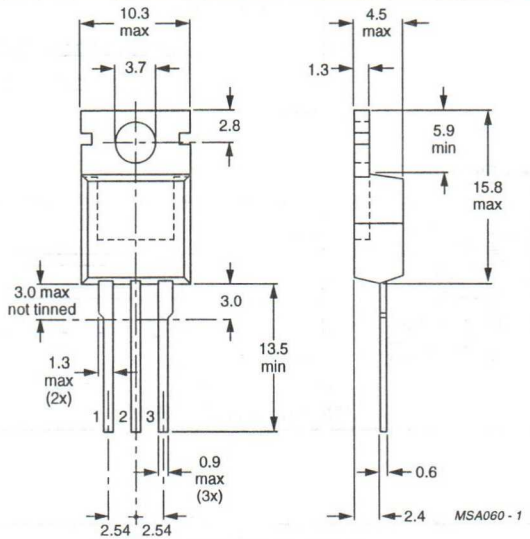



Fig. 13. SOT78 (TO220AB).

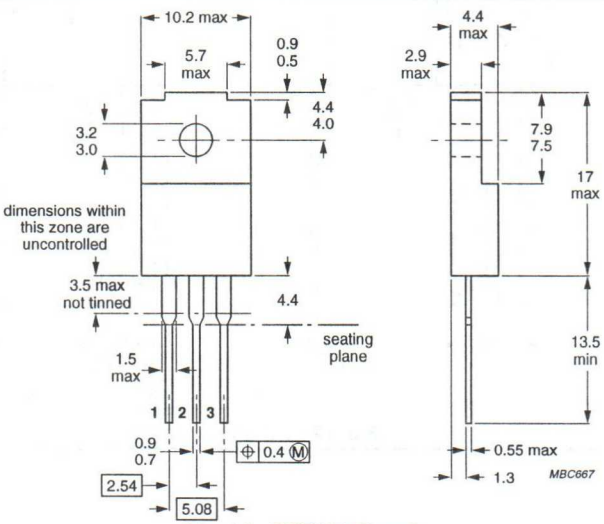



Fig. 14. SOT186 F-pack.

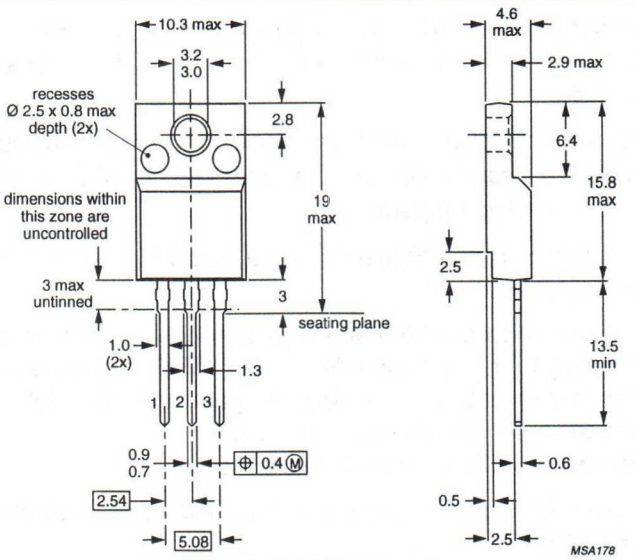



Fig. 15. SOT186A X-pack.

# The Ten Golden Rules Summarised

Rule 1. To turn a thyristor (or triac) ON, a gate current $\geq I_{GT}$ must be applied until the load current is $\geq I_L$. This condition must be met at the lowest expected operating temperature.

Rule 2. To turn off (commutate) a thyristor (or triac), the load current must be $< I_H$ for sufficient time to allow a return to the blocking state. This condition must be met at the highest expected operating temperature.

Rule 3. When designing a triac triggering circuit, avoid triggering in the $3^+$ quadrant (MT2-, G+) where possible.

Rule 4. To minimise noise pickup, keep gate connection length to a minimum. Take the return directly to MT1 (or cathode). If hard wired, use twisted pair or shielded cable. Fit a resistor of 1kΩ or less between gate and MT1. Fit a bypass capacitor in conjunction with a series resistor to the gate.
Alternatively, use an insensitive series H triac.

Rule 5. Where high $dV_D/dt$ or $dV_{COM}/dt$ are likely to cause a problem, fit an RC snubber across MT1 and MT2.
Where high $dI_{COM}/dt$ is likely to cause a problem, fit an inductor of a few mH in series with the load.
Alternatively, use a Hi-Com triac.

Rule 6. If the triac's $V_{DRM}$ is likely to be exceeded during severe mains transients, employ one of the following measures:
Limit high $dI_T/dt$ with a non saturable inductor of a few μH in series with the load;
Use a MOV across the mains in combination with filtering on the supply side.

Rule 7. Healthy gate drive and avoiding $3^+$ operation maximises the triac's $dI_T/dt$ capability.

Rule 8. If the triac's $dI_T/dt$ is likely to be exceeded, an air cored inductor of a few μH or an NTC thermistor should be fitted in series with the load.
Alternatively, employ zero voltage turn-on for resistive loads.

Rule 9. Avoid mechanical stress to the triac when fitting it to the heatsink. Fix, then solder. Never pop rivet with the rivet mandrel on the tab side.

Rule 10. For longterm reliability, ensure that the $R_{th\,j\text{-}a}$ is low enough to keep the junction temperature within $T_j$ max for the highest expected ambient temperature.

# SURFACE MOUNTED TRIACS AND THYRISTORS

Issue date September 1997 Document number 9397 750 02622

# Surface mounted triacs and thyristors

## Introduction

There is an ever growing need in the electronics industry for miniaturisation and cost reduction of the end product. In order to satisfy these requirements, designers are specifying Surface Mount Technology with increasing regularity. At first their attentions were aimed at the low power and small signal components. Now their attentions are turning towards the power devices in order to give them total surface mount solutions.

The increased miniaturisation is possible because surface mounted power semiconductors occupy less board area than through-hole-mounting devices on heatsinks. Cost reduction is possible due to the faster and simpler assembly that result when ALL components are surface mounted.

The availability of a wide range of package sizes permits continuous power dissipations ranging from 0.5 Watts to 2 Watts on standard Printed Circuit Boards. Higher power dissipations are achievable if special heatsinking provisions are made on the PCB. Some examples of these include:

- A grid of solder vias to a pad on the reverse side of the PCB.
- A PCB-mounted heatsink on one or both sides.
- An aluminium-cored PCB.
- Fan-assisted cooling.

## Surface mount solutions from Philips

Philips Semiconductors has developed a full range of surface mount power packages for its entire range of triacs and thyristors. The assembly materials and technology used are not simply adapted from the pre-existing through-hole-mounting package technology; they are unique to SMT.

Every new SMT device is subjected to rigorous testing which originates from stringent automotive requirements. This consists of full reliability testing after three surface mounting operations on printed circuit boards. No failures will be generated. This gives the best assurance of reliable end products.

This Technical Publication will present the surface mount packages and show what thermal performances can be achieved on standard PCBs without special heatsinking arrangements.

## SOT223

SOT223 (Fig. 1) is the smallest SMT power package presented in this publication. The mechanical design has been optimised for maximum ease & versatility of surface mounting, and maximum longterm reliability in the application. It will provide the minimum cost of ownership to the Original Equipment Manufacturer when initial purchase costs, handling costs and final assembly costs are added together.

The three legs and the heatsink tab emerge sideways from the edge of the plastic body, where they are formed to bring them into contact with the PCB for soldering to the pads. The centre leg and the larger heatsink tab on the opposite side of the package are internally connected.

Because the main tab and the three legs emerge from the edge of the plastic package and are formed before they make contact with the PCB, a certain degrée of safe movement of the PCB relative to the device is possible as the assembly expands and contracts during soldering and during circuit operation. Since the device's diepad is not in direct and intimate contact with the PCB solder pad, differential movement caused by different coefficients of expansion can be accommodated without excessive fatigue stress to the solder joints. The more extreme condition of stresses being transmitted to the die, causing it to crack, is also minimised with this package design.

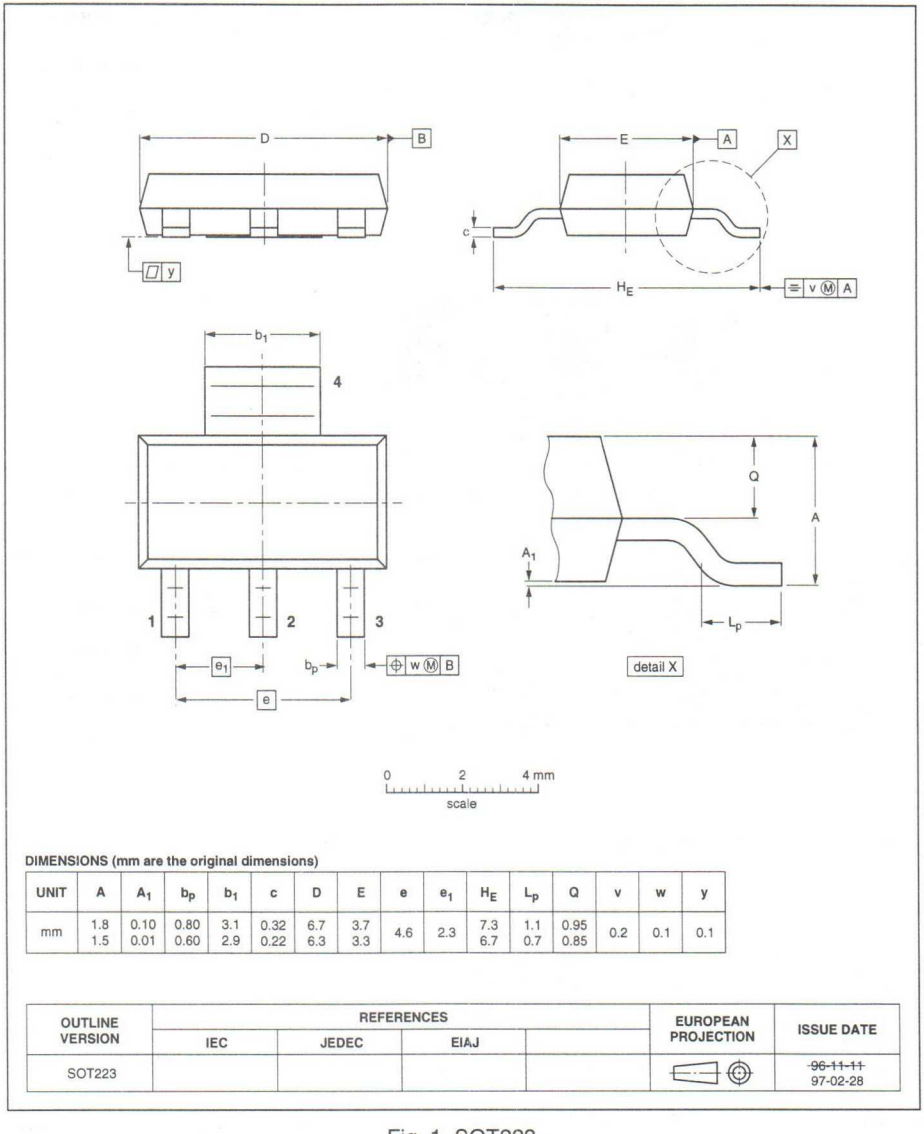
## SOT223 soldering

When soldering most SMT power packages, a reflow process must be used. However, for SOT223, it is also feasible to use wave soldering if required. Wave soldering is possible because the small size of the package minimises the size of the "shadow" on the downstream side of the solder flow. Perhaps more importantly, the exposed nature of the solder connections around the periphery of the package, and their relatively low thermal capacities, mean that

full solder wetting is easily possible with wave soldering. The good visibility of the solder joints allows full inspection for quality after assembly.

Figures 2 and 3 show the recommended SOT223 footprints for reflow soldering and for wave soldering.

**Plastic surface mounted package; collector pad for good heat transfer; 4 leads** **SOT223**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | $b_1$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.8<br>1.5 | 0.10<br>0.01 | 0.80<br>0.60 | 3.1<br>2.9 | 0.32<br>0.22 | 6.7<br>6.3 | 3.7<br>3.3 | 4.6 | 2.3 | 7.3<br>6.7 | 1.1<br>0.7 | 0.95<br>0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT223 | | | | | | ~~96-11-11~~<br>97-02-28 |

Fig. 1. SOT223.

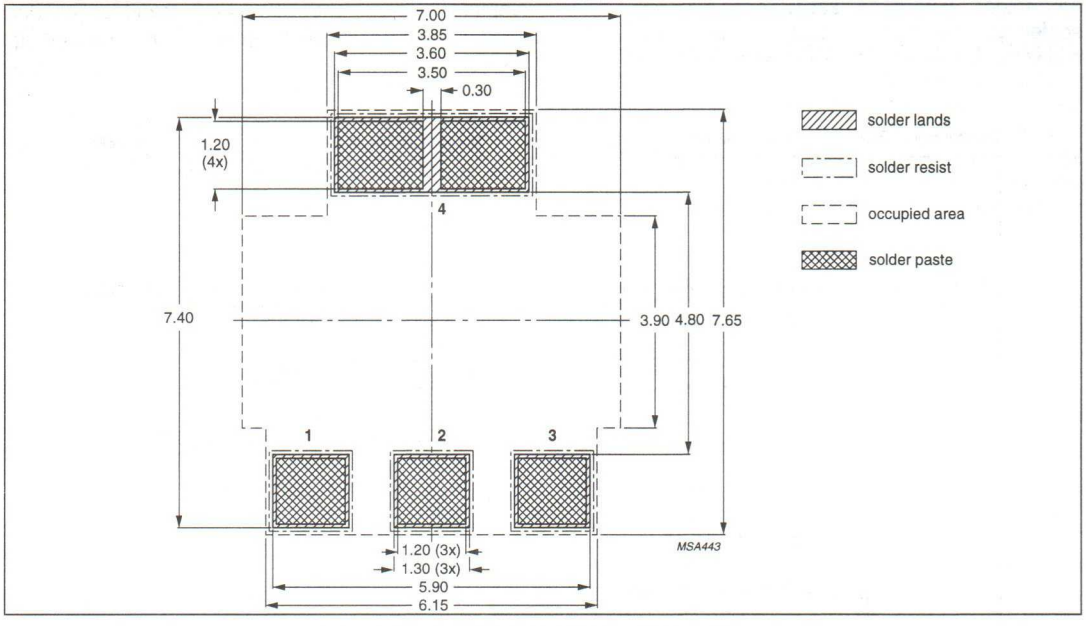



Fig. 2. Reflow soldering footprint for SOT223.

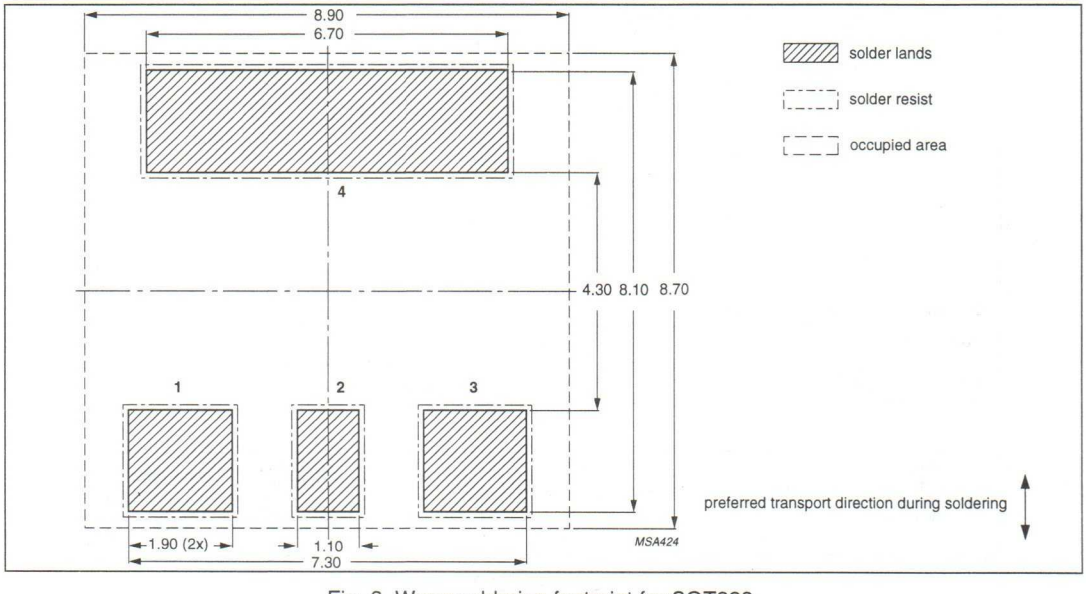


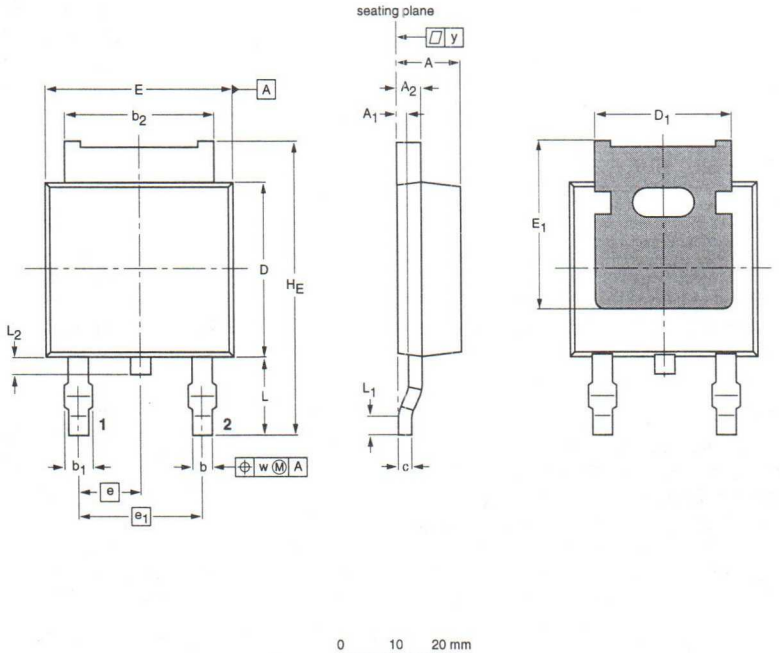

Fig. 3. Wave soldering footprint for SOT223.

## SOT428

SOT428 (also known as TO252 and DPAK) occupies an area on the PCB which is not much larger than the area required for SOT223. Indeed, it can be soldered to a universal SOT223 / SOT428 pad layout. Figures 5 and 6 show the pad and relative component sizes. The main pad area of $20mm^2$ is the minimum practical pad size for SOT428.

SOT428 has three legs which emerge from one edge of the plastic body. The centre leg is cropped off close to the plastic, so it is not used for electrical connection. The "centre leg connection" is made from the device's metal backplate to the main PCB pad. The two outer legs are formed to bring them into contact with the PCB pads for soldering.

**Plastic surface mounted package (Philips version of D-PAK); 2 leads** **SOT428**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ (1) | $A_2$ | b | $b_1$ max. | $b_2$ | c | D max. | $D_1$ max. | E max. | $E_1$ min. | e | $e_1$ | $H_E$ max. | L | $L_1$ min. | $L_2$ | w | y max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.65<br>0.45 | 0.89<br>0.71 | 0.89<br>0.71 | 1.1<br>0.9 | 5.36<br>5.26 | 0.4<br>0.2 | 6.22<br>5.98 | 4.81<br>4.45 | 6.73<br>6.47 | 4.0 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.7<br>0.5 | 0.2 | 0.2 |

**Note**

1. Measured from heatsink back to lead.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT428 | | | | | | 97-06-11 |

Fig. 4. SOT428.

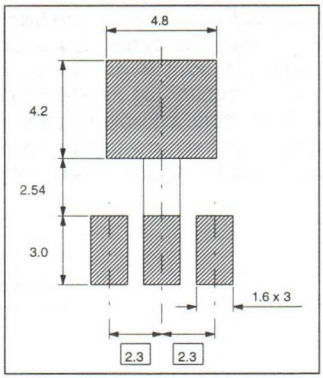



Fig. 5. Universal SOT223 / SOT428 pad layout.

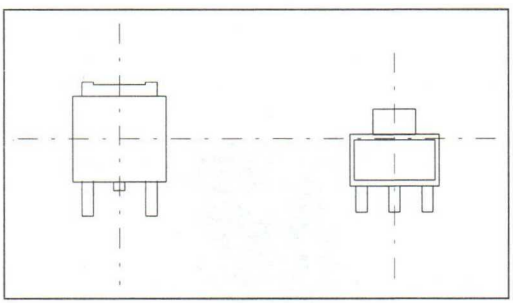


Fig. 6. SOT428 & SOT223 relative sizes.

**SOT428 soldering**

This surface mount package features a relatively large solder area (compared to SOT223) which is hidden after assembly. Because the mating surfaces between the main PCB pad and the device are remote from the outside world, wave soldering cannot be relied upon to wet the joint sufficiently. It is therefore necessary to use a reflow soldering method for packages of this design. Figure 7 shows the SOT428 solder pad dimensions.

**SOT428 design features for surface mountability**

It is well known among power semiconductor manufacturers that the larger a surface mounted power semiconductors is, the more vulnerable it is to die stresses during manufacture and during the surface mounting process. This can result in a significant percentage of rejects due to die cracking. We have learned long ago that it is not possible to use the same manufacturing techniques for surface mount devices as are used for through-hole devices. Unacceptable failure rates will certainly be the result, either during manufacture, during surface mounting or during prolonged thermal cycling in the application.

Philips Semiconductors has spent a long time perfecting its SOT428 package before releasing it onto the market so that these pitfalls can be avoided. Described below are some of the special design features which ensure successful manufacture and longterm reliable operation in the customer's application.

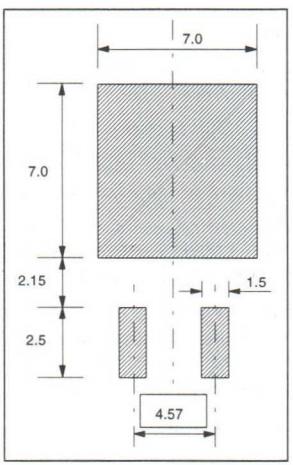



Fig. 7. SOT428 solder pad dimensions.

1. The package is moulded using a low stress epoxy plastic in order to minimise the bending force on the mounting base as curing takes place. Less bending of the mounting base means less die stress.
2. A thick copper mounting base of 0.89mm (0.035 inches) max thickness is used to further inhibit any tendency for bending of the mounting base.
3. A low stress, high lead content soft solder is used for diebonding. The amount of "give" in the solder accommodates differential expansions and minimises die stress.
4. A new technique has been developed to accurately control the thickness and positioning of the die-attach solder on the diepad. This guarantees optimum diebonding over the complete die area every time without unsoldered areas or excess solder. The benefit of this is to offer the best longterm reliability under thermal stress and the minimum junction-to-mounting base thermal resistance.

5. Special locking features are used to lock the epoxy to the metal to improve hermeticity. These features have been carefully optimised to provide good hermeticity without locking the epoxy too rigidly to the diepad, which can result in excess die stress during differential expansion.
6. A bare copper diepad is used for best adhesion of the epoxy to the metal. This promotes good hermeticity.
7. All mating surfaces to be soldered to the PCB pads are tin-lead solder plated for good solderability.
8. The footprint is compatible with JEDEC and Motorola layouts.
9. The coplanarity of leads to seating plane and leads to leads meets stringent industry standards.
10. A fully automatic high volume production line is used which takes in the raw components at its input and delivers assembled, 100% tested, packaged devices at its output.
11. All assembled devices are subjected to an in-line surface mount temperature profile pass to eliminate any remaining possibility, however small, of zero hour defects at the customer.
12. Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

**SOT404**

SOT404 (Fig. 9, also known as TO263 and $D^2PAK$) possesses the same size of plastic body as SOT78 (TO220). The similarity ends there. SOT404 is manufactured without a tab since no mounting hole is required. (It is not merely a cropped TO220!) The centre lead is cropped close to the plastic, so the "centre leg connection" is made via the metal backplate. The two outer leads are formed downwards to bring them into contact with the PCB.

**SOT404 soldering**

As for SOT428, it is also not possible to solder SOT404 using a wave soldering technique. The even larger body and larger hidden solder area would put this method out of the question. Reflow soldering is essential. Figure 8 shows the SOT404 solder pad dimensions.

**SOT404 design features for surface mountability**

In designing and manufacturing the SOT404 package, similar measures must be taken as for SOT428 to ensure a reliable end product. These include:

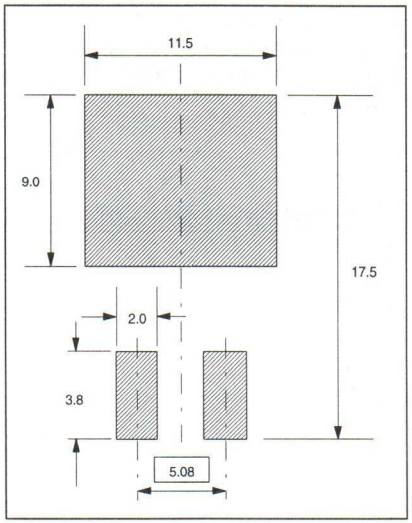



Fig. 8. SOT404 solder pad dimensions.

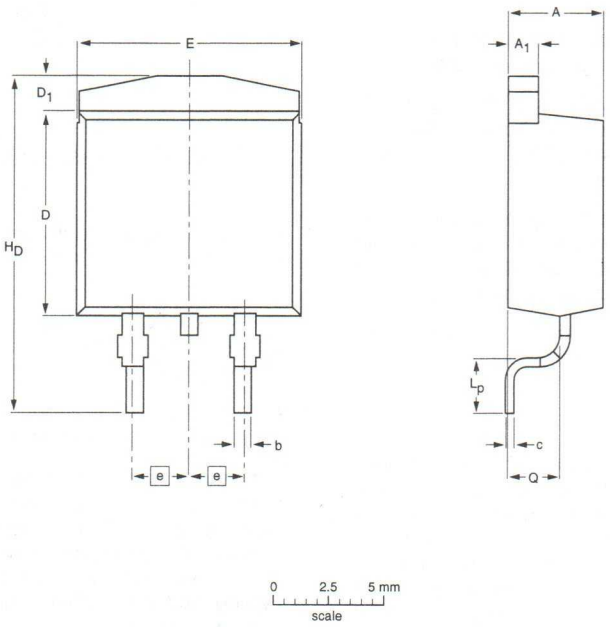
1. A low stress epoxy to minimise bending forces on the mounting base after curing. (Minimises die stress.)
2. A thick copper mounting base of 1.4mm (0.055 inches) max thickness to further minimise any tendency to bend.
3. A low stress, high lead content soft diebond solder. (Minimises die stress.)
4. Accurate dosing and spreading of the die-attach solder prior to diebonding to ensure optimum diebonding over the complete die area every time without unsoldered areas or excess solder. This offers best longterm reliability under thermal cycling and optimum junction-to-mounting base thermal resistance.
5. Optimised locking features to balance the conflicting requirements of good hermeticity with sufficient differential movement to avoid die stress fracture.
6. A bare copper comb to ensure good epoxy-to-metal adhesion for best hermeticity.
7. Tin-lead solder plating of all exposed copper, including all cropped edges, for optimum solderability.
8. Compatibility with the industry standard footprint layout for $D^2PAK$.
9. Coplanarity check on leads to seating plane and leads to leads.

10. A specially designed leadframe to reduce cropping forces as each device is separated from the comb. This avoids die cracking due to shock loading.

11. A surface mount temperature profile pass to eliminate zero hour defects at the customer.

12. Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

**Plastic single-ended package (Philips version of D2-PAK); 2 leads** **SOT404**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | c | D | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 9.65<br>8.65 | 1.6<br>1.2 | 10.3<br>9.7 | 2.54 | 2.9<br>2.1 | 15.4<br>14.8 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | 97-06-16 |

Fig. 9. SOT404.

### Mounting and soldering

The SM footprint drawings define the solder land (pad) areas, the solder resist areas and the area occupied by the package. Since the solder lands must be completely free of solder resist, the areas without the solder resist are always slighty greater than the solder land areas. The solder resist must cover all areas of the PCB that are not soldered to. This includes extended areas of copper used for heatsinking.

The footprints for reflow soldering define the solder paste areas in addition to the areas listed above. Solder paste is applied using a metal stencil which must be accurately aligned to within 0.1mm over the pads. A metal "squeegee" is drawn across the stencil to deposit the paste through the apertures, which must be the same size as the solder paste areas defined on the footprint drawings. With reference to Figs. 2 & 3, it can be seen that the optimum pad areas are different for wave soldering and for reflow soldering.

When wave soldering, surface mount devices must be held in position by a small measured dose of adhesive. A double wave process is used to ensure better wetting of all joints without solder shadows. Wave soldering **must** be used if there are any through-hole components on the PCB.

For reflow soldering, surface mount devices are held in position by the viscosity of the solder paste. When the solder is melted in the reflow oven, the surface tension of the molten solder causes them to self centre on their pads. For self centreing to operate reliably, the pad sizes and configuration are critical.

For PCBs which contain a mixture of SM and through-hole components, both soldering methods are sometimes employed in order to ensure optimum soldering of both technologies.

A more detailed description of the wave and reflow soldering processes is beyond the scope of this Technical Publication. For a more detailed description, please see Data Handbook SC18 entitled SMD Footprint Design and Soldering Guidelines.

## Thermal resistance - a laboratory investigation.

Detailed laboratory tests have been conducted on the junction-to-ambient thermal resistance $R_{th\ j\text{-}a}$ of the SOT223, SOT428 and SOT404 SM packages when mounted to different pad sizes on standard FR4 PCB. Sufficient time was devoted to this work to ensure repeatability of the results and to give a high level of confidence in their validity.

### Theory

It is possible to measure the temperature of a power semiconductor junction by measuring one of its temperature-dependent characteristics. For example, for a MOSFET it might be the forward voltage of the anti-parallel diode and for a thyristor it would be the forward voltage drop $V_T$. In order to heat up the device under test, a heating current is passed through it. When measuring its temperature-dependent characteristic, a much lower calibration current is passed for a very short measurement period. For this investigation, thyristors were used because of the relative ease of their measurement and because they were freely available in all the packages of interest.

The size of the die within any given package will not affect the final $R_{th\ j\text{-}a}$ result appreciably because any differences in the junction-to-case thermal resistance $R_{th\ j\text{-}c}$ will pale into insignificance compared to the case-to-ambient thermal resistance $R_{th\ c\text{-}a}$. It is not critical, therefore, which device is used when measuring package $R_{th}$ in free air or when surface mounted to conventional PCBs with relatively high thermal resistances to ambient.

FR4 fibreglass pcb with 35µm copper (1oz/square foot) was used because it is an industry standard to which everyone can relate. It is the PCB type which is always quoted in power semiconductor manufacturers' data sheets. It has become a "reference standard" by default. Despite this "standard" status, many industries cannot justify its use because of its cost. The home appliance industry prefers to use a lower cost alternative, one example of which is CEM3. This is a resin and paper-based material with fibre on both sides. Fortunately, the thermal performance of the cheaper alternatives is sufficiently close to that of FR4 in many cases to make the results of this investigation valid for those also.

### Equipment

The test PCBs had pad sizes which varied upwards from the minimum recommended for the package. Consistent pad width / height ratios were maintained. The pad was always positioned centrally on the test board to assure consistent heatsinking to the bulk of

the PCB. SOT223 and SOT428 used the same pad layouts, while SOT404 had its own PCBs. Figure 10 shows the second smallest and largest pad size test boards for SOT223 / SOT428, and Fig. 11 shows the smallest and largest pad size test boards for SOT404. Note that these test boards are not shown full scale.

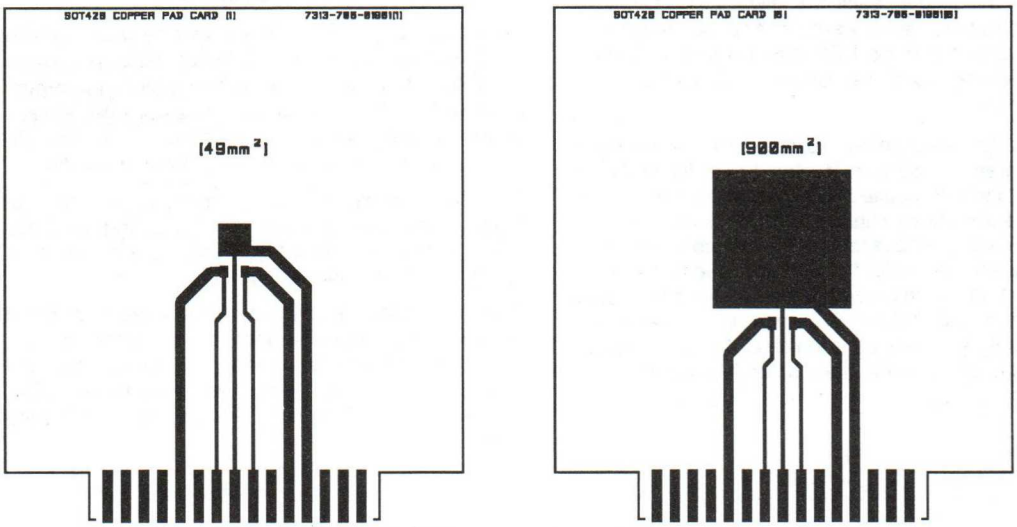



Fig. 10. SOT223 / SOT428 test PCB layout, small and large pad areas.

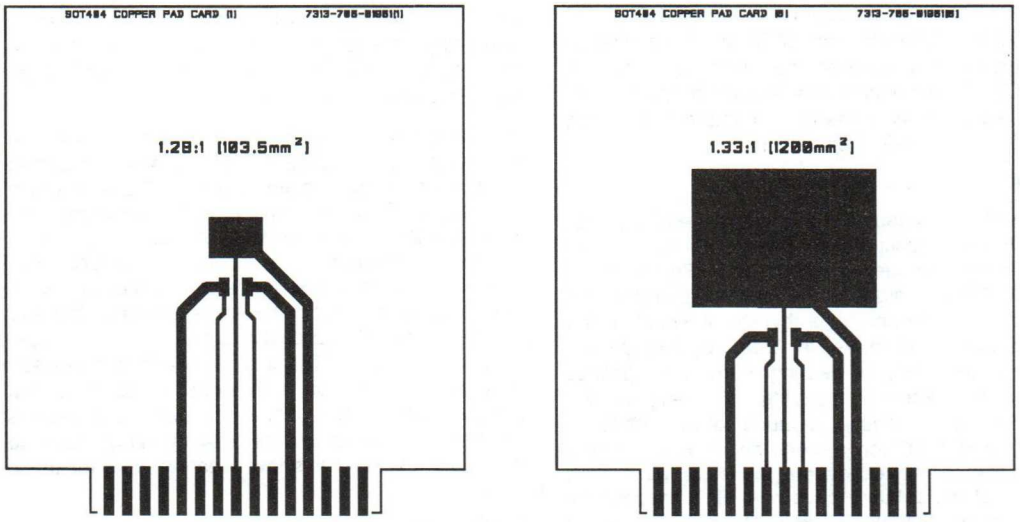



Fig. 11. SOT404 test PCB layout, small and large pad areas.

Separate power and measurement connections were taken via an edge connector to the device. The PCBs were standard fibreglass FR4 with 35μm copper which had been very lightly "tinned" by electrochemical deposition. (Thermal resistance will not be reduced by a thick layer of roller tinning!) The

PCBs were made relatively large at 100mm x 100mm to ensure that $R_{th}$ is controlled by pad area and not by PCB area.

Thyristors were tested using a purpose built thermal resistance test gear. (Thyristors were tested in preference to triacs because they only require one measurement for each power setting, whereas triacs need measuring in both directions with the average power being calculated from the results.)

The most important fact to remember when conducting the tests was that they take a lot of time. It was essential to ensure that thermal equilibrium and stability had been reached before readings were taken at elevated device temperature. Rushing the tests would give incorrect results and improbable graphs. This was learned from experience.

**Results**

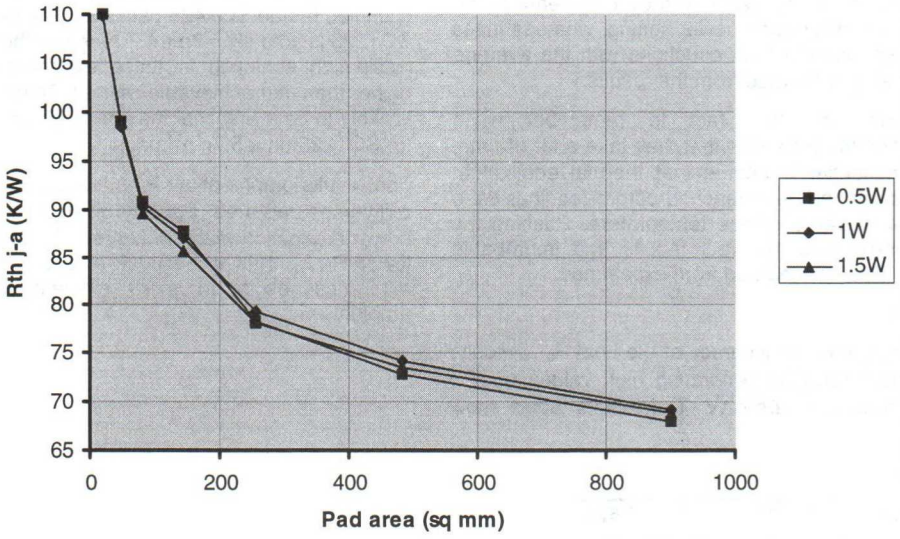
The resolution and accuracy of the final $R_{th\ j\text{-}a}$ results were maximised by generating high values of $\Delta T_j$, hence large measured $\Delta V$. The results tables show $R_{th\ j\text{-}a}$ (K/W) versus power dissipation and pad area. The power levels highlighted by an asterisk indicate a suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB. (In the case of the SOT223 package, the smallest pad area used was 20mm$^2$. This area is fully occupied by the SOT428 package. The minimum for SOT223 is actually 5.7mm$^2$. Therefore the 1W power dissipation achieved in these experiments will be higher than that achievable with a 5.7mm$^2$ pad. 0.5W is likely to be a practical maximum power dissipation for SOT223 on a 5.7mm$^2$ pad.)

The results graphs show $R_{th\ j\text{-}a}$ versus pad area and $\Delta T_j$ versus pad area. For any given package, higher power dissipation leads to higher $\Delta T_j$ which leads to lower $R_{th\ j\text{-}a}$. This is because a larger temperature difference results in more efficient radiation to ambient.

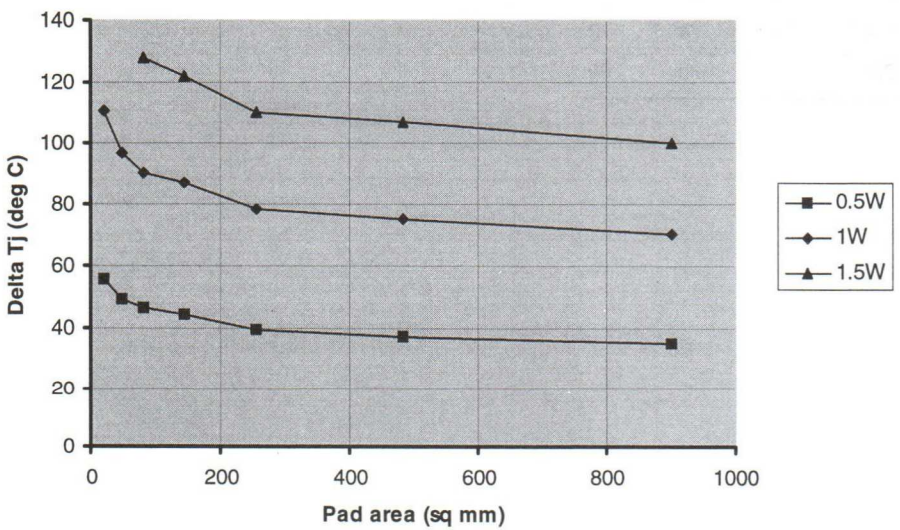
***SOT223***

| *Area (mm$^2$)* | *0.5W* | *1.0W** | *1.5W* |
|---|---|---|---|
| 20 | 110 | 110 | - |
| 49 | 99 | 98 | - |
| 81 | 91 | 90 | 90 |
| 144 | 88 | 87 | 86 |
| 256 | 78 | 79 | 78 |
| 484 | 73 | 74 | 73 |
| 900 | 68 | 69 | 69 |

**SOT223 Rth j-a vs PCB pad area. 100 x 100 mm FR4 PCB positioned vertically in still air.**

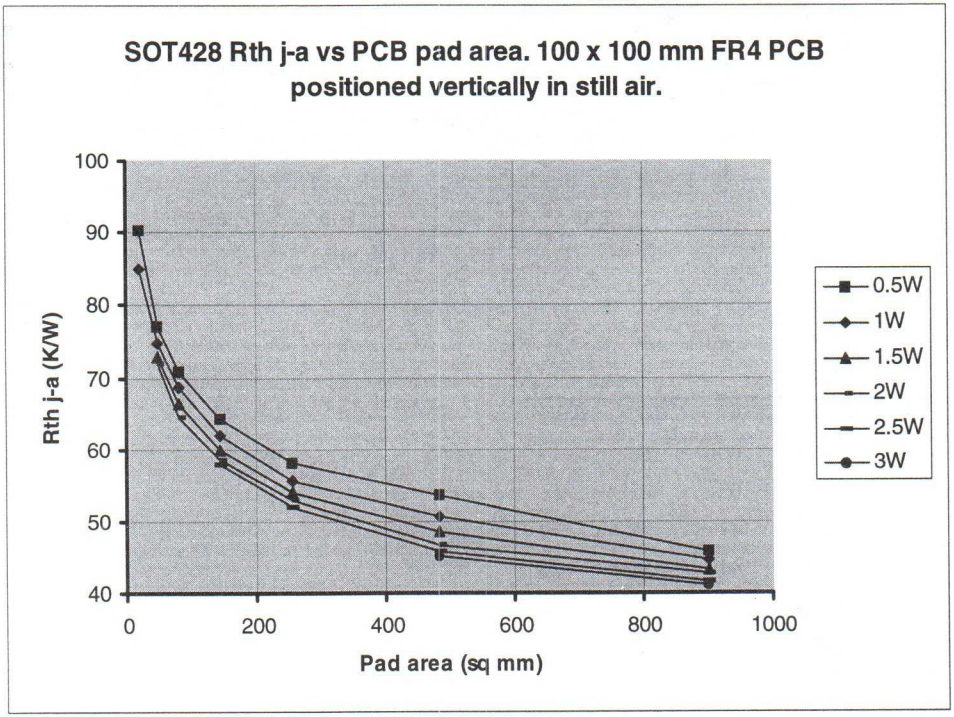


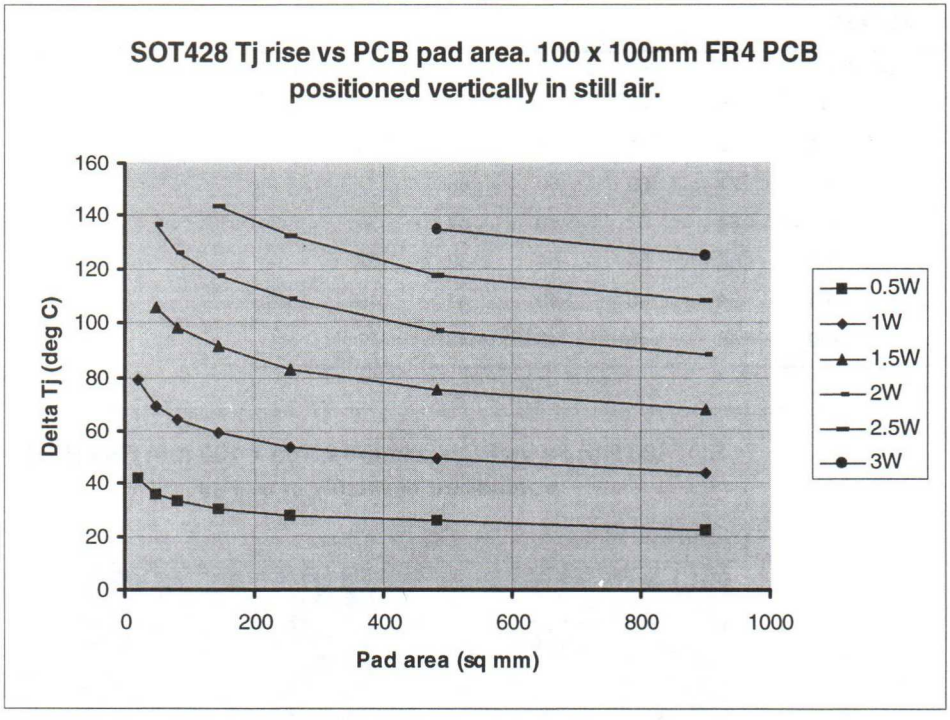

**SOT223 Tj rise vs PCB pad area. 100 x 100mm FR4 PCB positioned vertically in still air.**



***SOT428***

| *Area ($mm^2$)* | *0.5W* | *1.0W** | *1.5W** | *2.0W* | *2.5W* | *3.0W* |
|---|---|---|---|---|---|---|
| 20 | 90 | 85 | - | - | - | - |
| 49 | 77 | 75 | 73 | 72 | - | - |
| 81 | 71 | 69 | 66 | 65 | - | - |
| 144 | 64 | 62 | 60 | 59 | 58 | - |
| 256 | 58 | 56 | 54 | 53 | 52 | - |
| 484 | 54 | 50 | 48 | 47 | 46 | 45 |
| 900 | 46 | 45 | 43 | 43 | 42 | 41 |

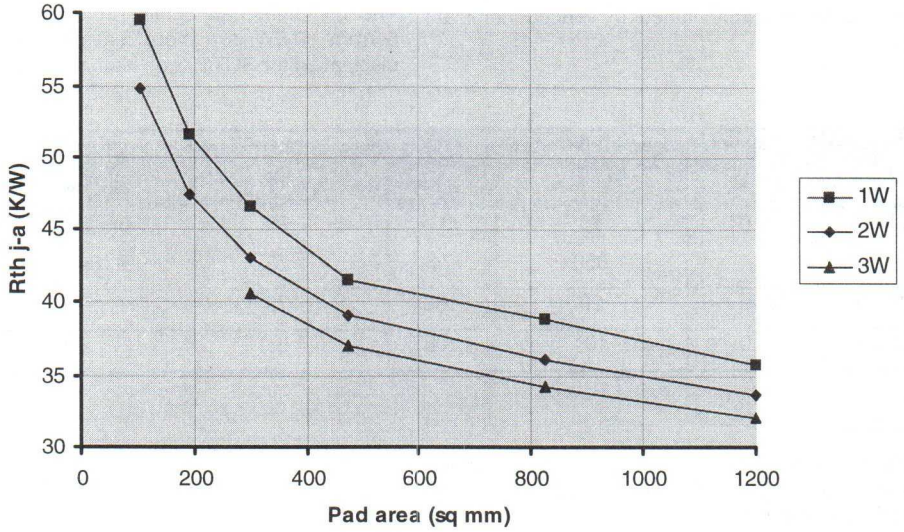




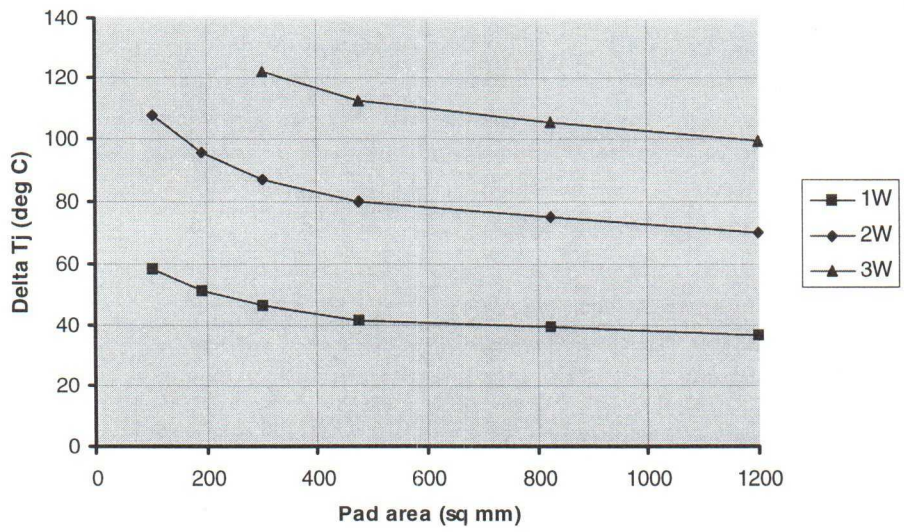

***SOT404***

| *Area ($mm^2$)* | *1.0W* | *2.0W** | *3.0W* |
|---|---|---|---|
| 103.5 | 60 | 55 | - |
| 192 | 52 | 47 | - |
| 300 | 47 | 43 | 41 |
| 475 | 41 | 39 | 37 |
| 825 | 39 | 36 | 34 |
| 1200 | 36 | 34 | 32 |

**SOT404 Rth j-a vs PCB pad area. 100 x 100mm FR4 PCB positioned vertically in still air.**




**SOT404 Tj vs PCB pad area. 100 x 100mm FR4 PCB positioned vertically in still air.**



## Conclusions

The maximum practical power dissipations are summarised below for stagnant ambient conditions at 25°C. These are for standard FR4 PCB or similar without special heatsinking provisions. The 35µm copper had been lightly tinned by electrochemical deposition.

SOT223 and SOT428 can be soldered to common pad layouts. 20mm$^2$ was the absolute minimum pad area for soldering SOT428. A reasonable power dissipation for SOT428 on 20mm$^2$ fell somewhere between 1.0W and 1.5W.

The minimum pad quoted in data for SOT223 is 5.7mm$^2$. 0.5W is a more realistic maximum power dissipation for SOT223 on its minimum pad.

| Package | Pmax (W) | Pad area (mm$^2$) | $\Delta T_j$ (°C) | $R_{th\ j\text{-}a}$ (K/W) (experimental) | $R_{th\ j\text{-}a}$ (K/W) (quoted in data) |
|---|---|---|---|---|---|
| SOT223 | 1.0 | 20 | 97 | 99 | 156 (5.7mm$^2$ pad) |
| | | 650 | 74 | 72 | 70 (648mm$^2$ pad) |
| SOT428 | 1.0<1.5 | 20 | 106 | 73 | 75 |
| SOT404 | 2.0 | 104 | 108 | 55 | 55 |

## Naked dice

All Philips' thyristors and triacs can be supplied as naked dice if required. Please contact your local sales office for details.

## Total Quality Management




Philips Semiconductors is committed to be a world class, customer driven, volume supplier of semiconductors.

To achieve this, we operate a Total Quality Management (TQM) system, based on Continuous Improvement and Quality Assurance in all our business activities, and Partnerships with our customers and suppliers.

The top priority throughout the company is Continuous Improvement.

To focus on this we will:

- Work closely with key customers, as our partners.
- Monitor progress, using customer-driven data, of our product and services.
- Benchmark against the best.

Furthermore, all parts of the organisation must always demonstrate:

- The presence of a strong, management-led improvement structure.
- Commitment and participation in all areas.
- Measurable progress towards our Quality Improvement goals.

### Organisation

An organisation is in place which ensures that personnel with the necessary organisational freedom and authority can identify and solve quality problems, prevent occurrence of product non-conformity and protect the customer from non-conforming product.

### Design control

A comprehensive design and development procedure is in place which ensures that the requirements of good design practice are met.

Particular emphasis is placed on ensuring that the initial specification is agreed by the Customer and the Marketing and Development functions.

There are regular formal reviews of design progress to ensure that the initial specification will be met by the design.

Detailed measurements are made on initial samples to ensure that the initial specification has been met.

### Process control

All processes which directly affect quality are carried out under controlled conditions. Documented work instructions are available for all production processes and the appropriate environmental controls are in place to ensure consistent processing. Monitoring of the product, processes and the environment takes place during production.

Approval exercises are run to ensure that new processes and new equipment perform at an acceptable level.

Written, photographic or visual standards are available at the appropriate points in the production processes.

### Corrective action

Non-conforming product found in process is investigated and the root causes identified. Changes to product or process are then introduced to prevent recurrence of the problem.

### Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE. Our factories are certified to ISO 9000.

### Partnerships with customers

These include: PPM co-operations, design-in agreements, ship-to-stock, just-in-time, self-qualification programmes and application support.

### Partnerships with suppliers

In addition to ISO9000 audits and close monitoring of supplier delivery performance, we operate a Supplier Excellence Award scheme which requires suppliers and their sub-suppliers to use statistical process control, perform gauge studies and use failure mode and effect analysis (FMEA) techniques to identify and correct the root causes of quality and delivery problems.

### Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimizations for the highest built-in product reliability. Highly accelerated tests are applied in order to evaluate the product reliability. Rejects from reliability tests and from customer complaints are submitted to failure analysis and the results applied to improve the product or process.

### Customer responses

Our quality improvement depends on joint action with our customers. We need our customers' inputs and we invite constructive comment on all aspects of our performance. Please contact your local sales representative.

### Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organisations.

## Environmental Policy

Philips Semiconductors is a global company committed to achieving a leading competitive position in the electronics industry through continuous improvements in product innovation, manufacturing excellence, customer service and environmental protection.

Environmental protection is an integral part of our business policy and is based on four principles:

> Sustainable development - development of products and processes that have minimal effect on the quality of the environment today and in the future.

> Prevention is better than cure.

> The total effect on the environment is what counts - embodied in the development of products whose production (including energy usage), operation and disposal at end of life have minimal adverse effect on the environment.

> Open contact with the authorities and customers.

As a leading manufacturer of integrated circuits and discrete semiconductors, Philips Semiconductors regards environmental protection as a major issue. In contrast to many industries, semiconductor manufacture uses relatively few toxic and hazardous materials. Nevertheless it is always our policy to follow working practices that reduce to the absolute minimum any chance of these materials passing into the environment. Every opportunity is taken to refine our manufacturing processes to reduce energy and water consumption and produce as little impact on the surroundings as possible.

### Certification

Philips Semiconductors was among the first companies in the world to implement certifiable Environmental Management Systems in line with the ISO 14001 environmental standard. We expect all of our manufacturing centres to be certified before 1999.

We were also one of the first international companies to introduce an internal Environmental Network meeting ISO 14001 requirements.

### ISO 14001

The essential elements of an Environmental Management System meeting ISO 14001 requirements are:

> An organisation and well-defined procedures for handling environmental issues.

> Clearly-defined areas of responsibility within the organisation and a framework for setting up and reviewing environmental objectives.

> Awareness of environmental factors plus a clear improvement plan prioritising actions on reducing environmental impact.

> A published policy of continuous improvement on environmental issues.

As with Quality standards, companies must be periodically audited, usually by an external party, to verify that they are complying with the requirements.

### Gaining certification

As part of the process of gaining environmental certification such as ISO 14001, the headings below describe just some of the work carried out by the Philips Semiconductors sites worldwide.

#### REDUCING HAZARDOUS MATERIALS

Examples of work carried in this area include:
Replacing nickel leadframes by copper leadframes to reduce the quantity of nickel passing into the environment, both in production and at end-of-life disposal;
Research into finding suitable alternatives to antimony and bromine which are used as flame retardants in semiconductor encapsulations;
Finding suitable alternatives to toxic beryllia in semiconductors, for example aluminium nitride.

#### INVOLVING PARTNERS

We require our suppliers and subcontractors to be environmentally responsible, to have their own environmental policy and improvement plans and to record environmental information on all raw materials supplied to us. Future preferred suppliers will also be required to have ISO 14001 certification.

#### LOW-POWER DESIGNS

Continuing developments in our power semiconductors and integrated circuits produce more efficient operation, leading to lower power dissipation, cooler operation and lower drain on the power supply. This pays dividends whatever the power source. In the case of battery power, fewer batteries mean fewer problems from battery disposal.

#### CUTTING ENERGY CONSUMPTION

Efforts have been made and are ongoing to reduce energy consumption within the company. The overall goal is to improve the efficiency of energy consumption by 25% before the year 2000.

Energy-saving programmes include:
Maintaining clean-air conditions at the work surface by the use of mini-environments within clean-rooms. This can lead to reductions of up to 60% in clean-room energy usage;
Replacing old inefficient lighting with new equipment which uses electronic ballasts and controls;
Making the workforce aware of good energy-saving practices which are as relevant in the home as they are in the workplace.

#### REDUCING CHEMICAL EMISSIONS

Efforts are constantly in progress to reduce chemical emissions. These efforts include:
Improvements to manufacturing processes to reduce the emissions of perfluorinated compounds and volatile organic compounds;
Alternatives introduced for damaging organic materials like ethyl glycol ethers and methanol in photo-lithographic processes.

ODC-FREE

In the elimination of ozone-depleting chemicals from its production processes, Philips Semiconductors can claim major successes. As early as May 1993, all plants had eliminated chloro-fluorocarbons (CFCs) from their manufacturing processes. This led the way to a complete phasing out of all Class I and Class II ODCs (listed in the 1986 Montreal Protocol) from our products and manufacturing processes in compliance with the US Clean Air Act.

RECYCLING

Chemicals and water used in production processes are cleaned and recycled for re-use where, previously, they would have been disposed of. In some cases where we cannot re-use waste materials in our manufacturing processes, they are still of sufficient purity for other industries who buy them for their own manufacturing processes.

Examples of waste product re-use are:
Supplying cleaned water from production processes for landscaping irrigation and for supporting other local industries;
Supplying reject wafers to the aluminium industry to be used as pure silicon additives during aluminium smelting;
Re-using sulphuric acid in-house for cleaning furnace tubes and supplying it to third parties for use in electroplating;
The recycling and re-use on-site of solvents such as acetone, isopropanol and N-methyl pyrrolidone.

PAPER AND CARDBOARD REDUCTION

Our parent company has set a target to reduce the volume of paper and cardboard used in packing materials by 15% by the year 2000. Philips Semiconductors has already passed this target by 1997 with a reduction over the previous 3 years of more than 20%.

REDUCED ENVIRONMENTAL IMPACT OF PACKING

We are reducing the impact of used packing material on the environment by promoting recycling. To make this easier we have switched to "mono material" (for example, from aluminium-lined boxes to carbon-coated boxes)

Other measures include:
Switching from two-piece to one-piece boxes;
Changing from boxes of white cardboard (which require bleach in manufacture) to brown recycled cardboard;
Using water-based inks (without heavy metals) for marking.
All parts are marked with recycling symbols and the material used (for example, "PVC" in the case of plastic device tubes).

We actively promote re-use of reels and trays used for discrete semiconductors and integrated circuits. This is helped by marking the boxes with labels giving an address to contact to arrange collection of used reels and trays. Philips is also cooperating with other manufacturers to establish global standards for these materials.

As a result of these actions, our new packing designs are easier to recycle, use less material and are nearly 40% lighter than old designs.

SEMICONDUCTOR CONTENT

We were the first semiconductor manufacturer to publish full details of the chemical content of its products and packaging. This assists manufacturers who wish to evaluate the environmental impact from initial purchase to end-of-life disposal of using our products.

# DEVICE DATA

in alphanumeric sequence

# Silicon Bi-directional Trigger Device | BR100/03

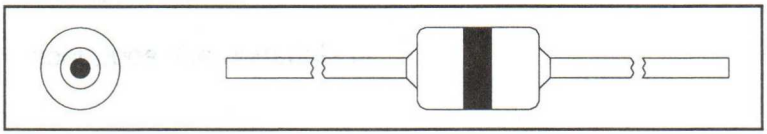
## GENERAL DESCRIPTION

Silicon bidirectional trigger device in a glass envelope intended for use in triac and thyristor trigger circuits.

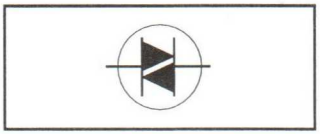
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{(BO)}$ | Breakover voltage | 28 | 36 | V |
| $V_O$ | Output voltage | 7 | - | V |
| $I_{FRM}$ | Repetitive peak forward current | - | 2 | A |

## OUTLINE - SOD27



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $I_{FRM}$ | Repetitive peak forward current | $t \leq 10$ µs, $T_a \leq 50$°C; f = 60 Hz | - | 2 | A |
| $P_{tot}$ | Total power dissipation | $T_a = 50$°C | - | 150 | mW |
| $T_{stg}$ | Storage temperature | | -55 | 125 | °C |
| $T_j$ | Operating junction temperature | | - | 100 | °C |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 330 | - | K/W |
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to leads | | - | 150 | - | K/W |

## CHARACTERISTICS

$T_a = 25$ °C unless otherwise stated.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BO)}$ | Breakover voltage | $I = I_{(BO)}$ | 28 | 32 | 36 | V |
| $\lvert V_{(BO)+} \rvert - \lvert V_{(BO)-} \rvert$ | Breakover voltage symmetry | $I = I_{(BO)}$, see fig: 1 | - | - | 3.5 | V |
| $V_O$ | Output voltage | $R_L = 20\ \Omega$; Circuit of fig: 2 | 7 | - | - | V |
| $I_{(BO)}$ | Breakover current | $V = V_{(BO)}$ | - | - | 50 | µA |
| $dV_{(BO)}/dT$ | Temperature coefficient of $V_{(BO)}$ | | - | 0.1 | - | %/K |
| $t_r$ | Risetime | $I_p = 0.5$ A; Circuit of fig: 2 | - | 1.5 | | µs |

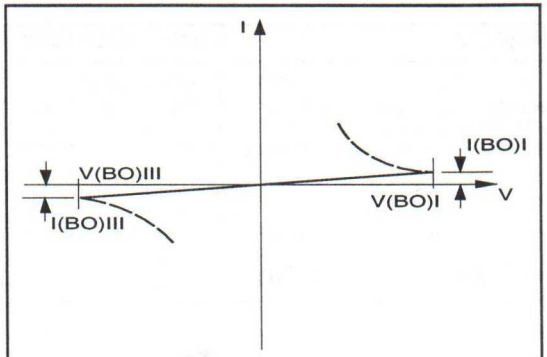



*Fig.1. Current-voltage characteristics*

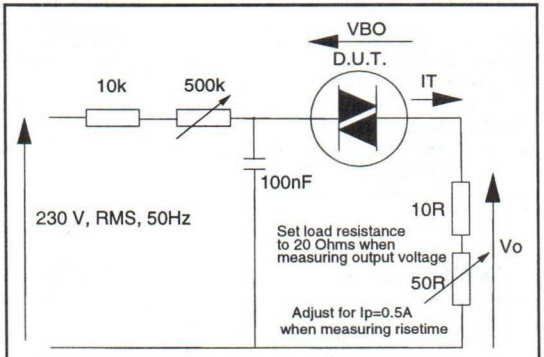



*Fig.2. Test circuit for output voltage and risetime.*

## MECHANICAL DATA

*Dimensions in mm*

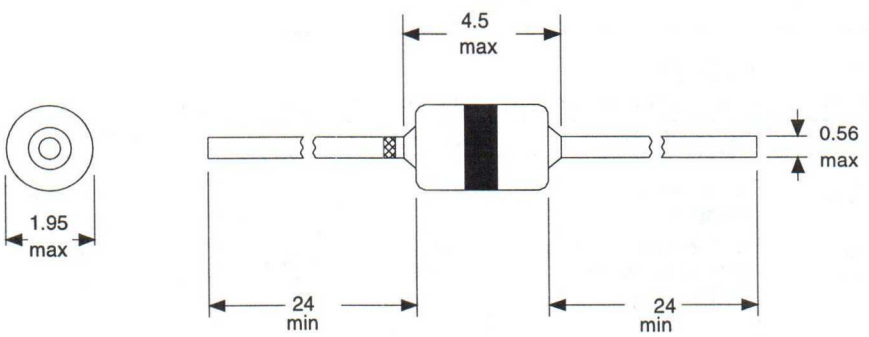



*Fig.3. SOD27.*

# Triacs logic level

# BT131 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

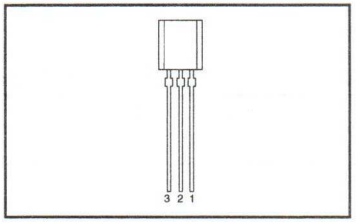
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | | **BT131-** | **500** | **600** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 16 | 16 | A |

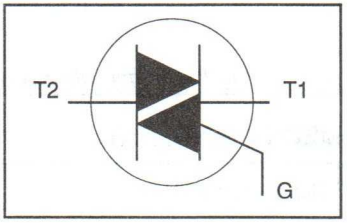
## PINNING - TO92

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 2 |
| 2 | gate |
| 3 | main terminal 1 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq$ TBF °C | - | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | |
| | | t = 20 ms | - | 16 | | A |
| | | t = 16.7 ms | - | 17.6 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 1.28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

# Objective specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to lead | full cycle | - | - | 60 | K/W |
| | | half cycle | - | - | 80 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted;lead length = 4mm | - | 150 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 3 | mA |
| | | | T2+ G- | - | - | 3 | mA |
| | | | T2- G- | - | - | 3 | mA |
| | | | T2- G+ | - | - | 7 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 6 | mA |
| | | | T2+ G- | - | - | 18 | mA |
| | | | T2- G- | - | - | 6 | mA |
| | | | T2- G+ | - | - | 18 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 12 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | TBF | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

# Triacs logic level

# BT132 series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

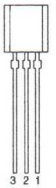
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT132- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 16 | 16 | A |

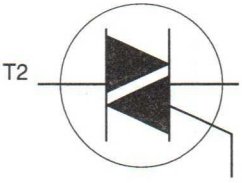
## PINNING - TO92

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 2 |
| 2 | gate |
| 3 | main terminal 1 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | -500 | -600 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 51$ °C | - | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | |
| | | t = 20 ms | - | 16 | | A |
| | | t = 16.7 ms | - | 17.6 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 1.28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to lead | full cycle | - | - | 60 | K/W |
| | | half cycle | - | - | 80 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted;lead length = 4mm | - | 150 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

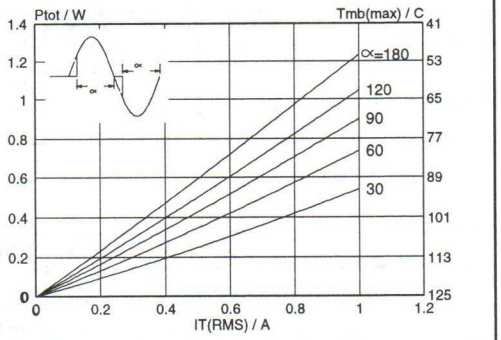



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

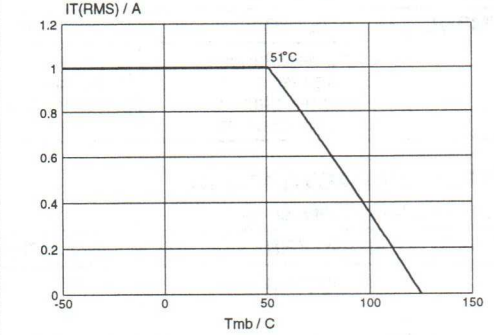



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature $T_{lead}$.*

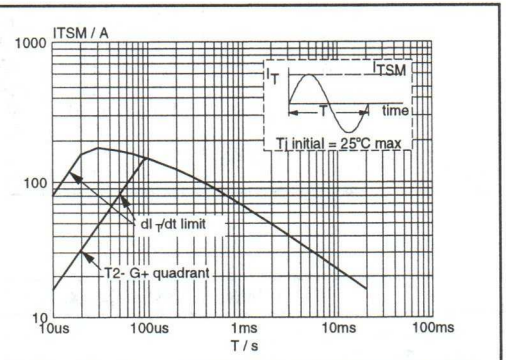



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

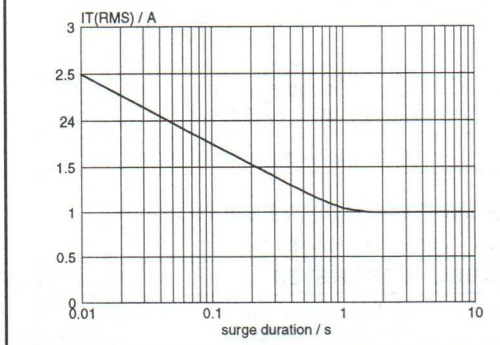



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 51°C$.*

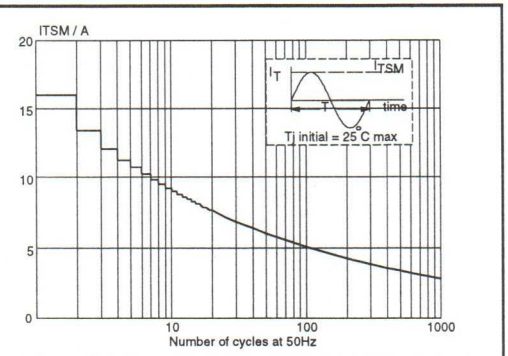



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

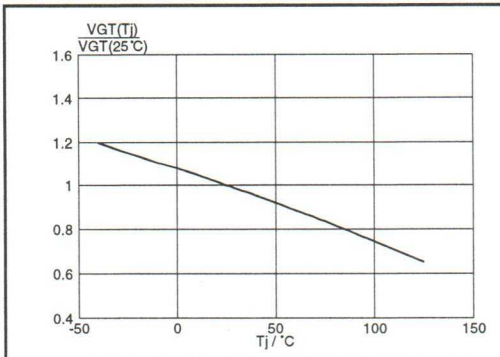



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

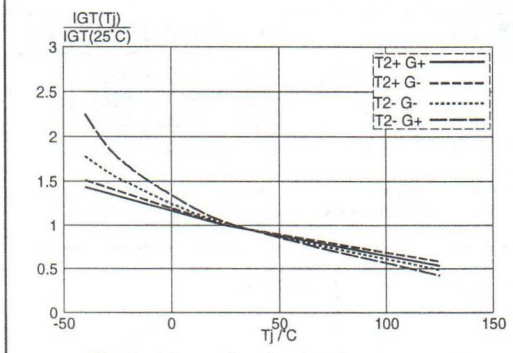



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

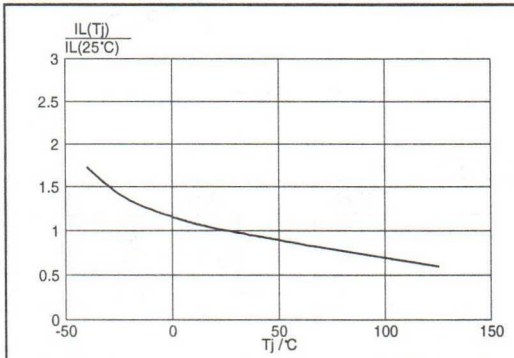



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

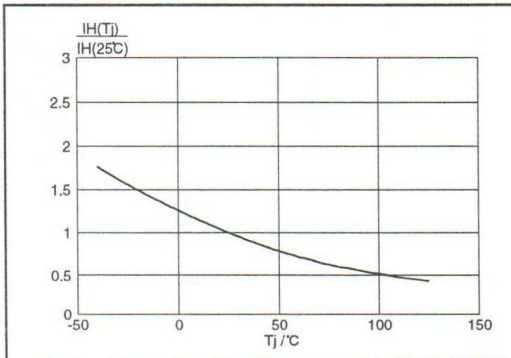



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

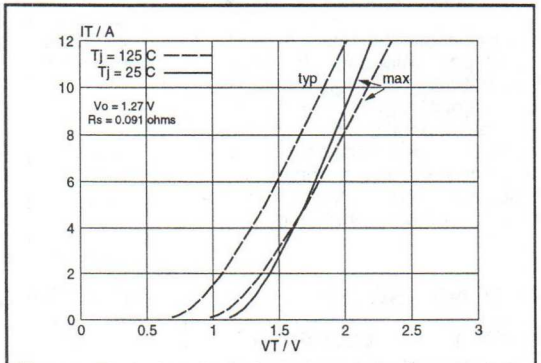



*Fig.10. Typical and maximum on-state characteristic.*

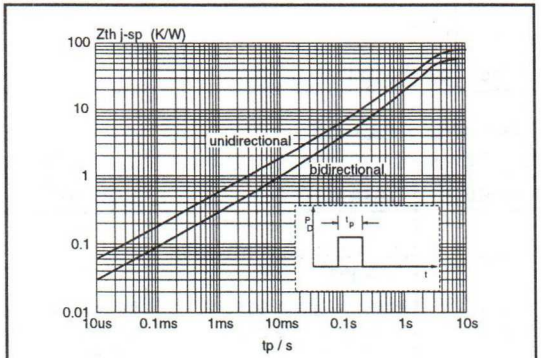



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width $t_p$.*

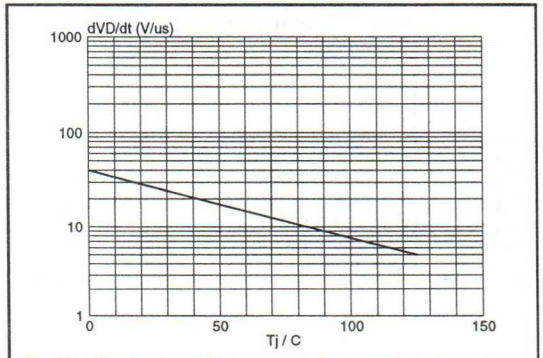



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

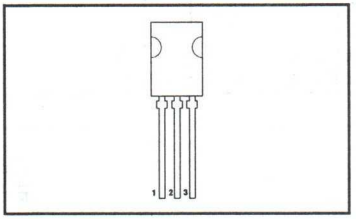
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT134-** | **500** | **600** | **800** | |
| | **BT134-** | **500F** | **600F** | **800F** | |
| | **BT134-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

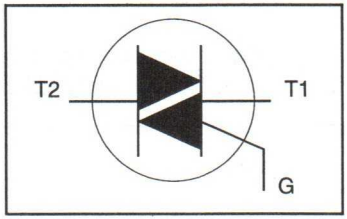
## PINNING - SOT82

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 100 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT134- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.70 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT134- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ =67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 4 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; | - | - | - | 2 | - | µs |

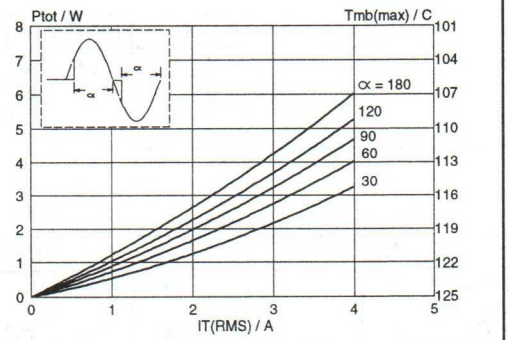



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

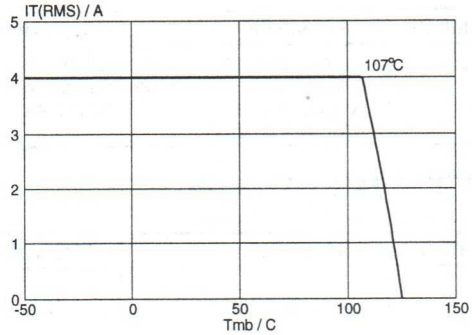



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

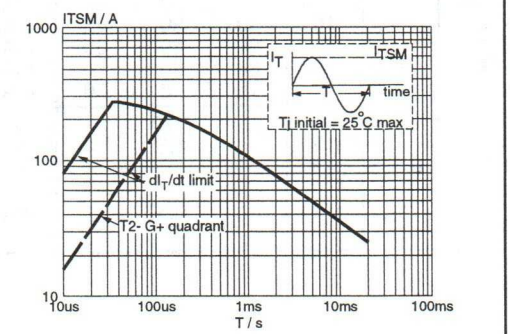



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

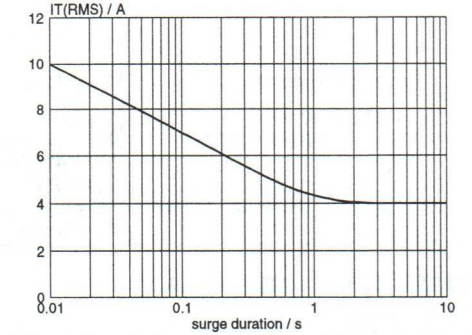



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

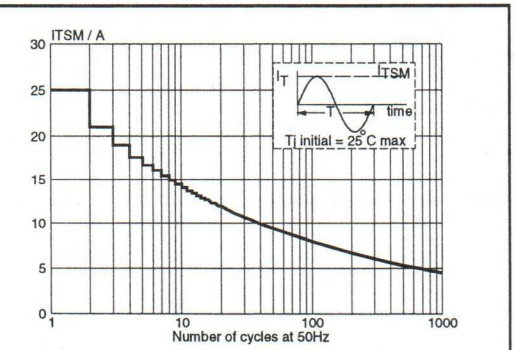



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

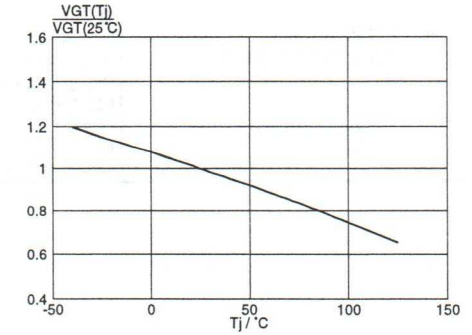



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

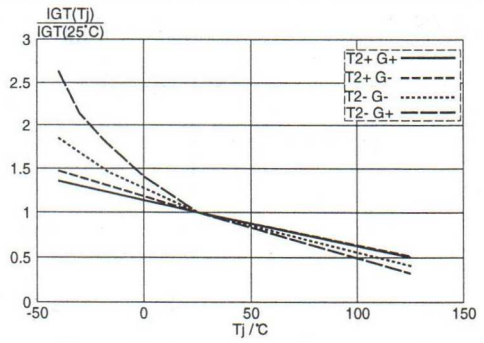



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

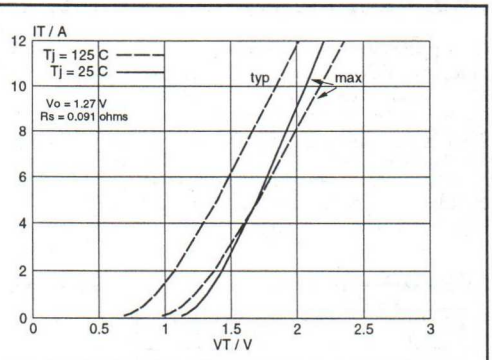



*Fig.10. Typical and maximum on-state characteristic.*

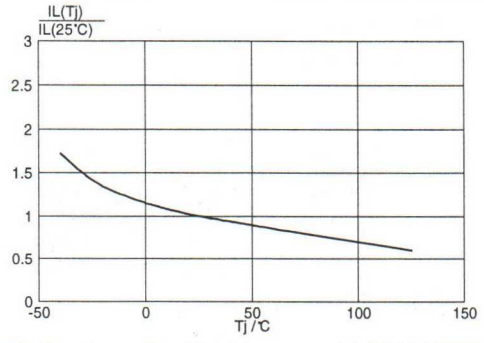



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

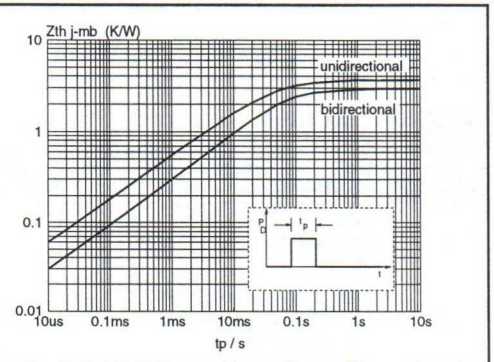



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

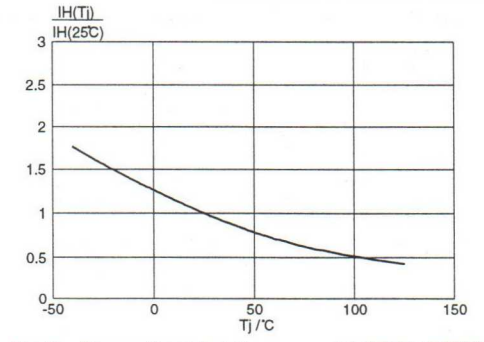



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

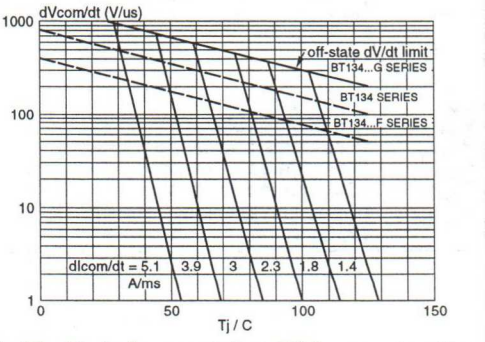



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs logic level

# BT134 series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

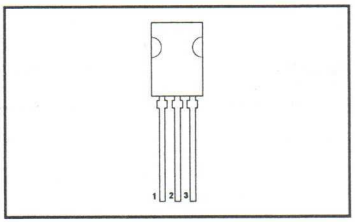
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT134- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | A |

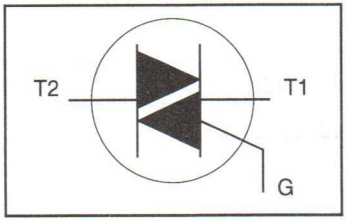
## PINNING - SOT82

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | UNIT |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 25 | | A |
| | | t = 16.7 ms | - | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 100 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

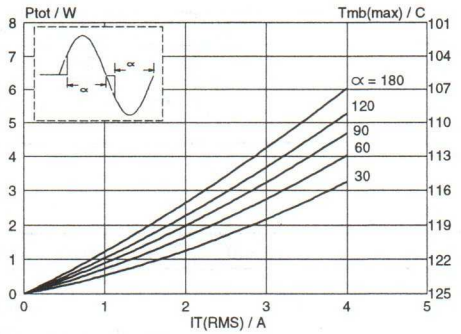



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

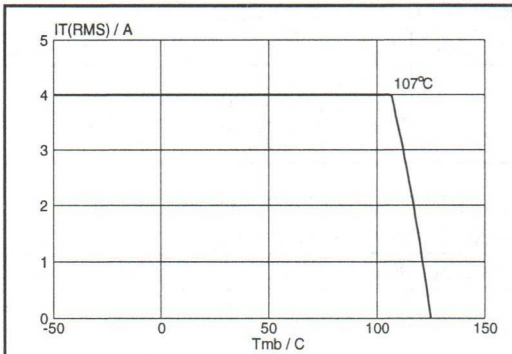



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

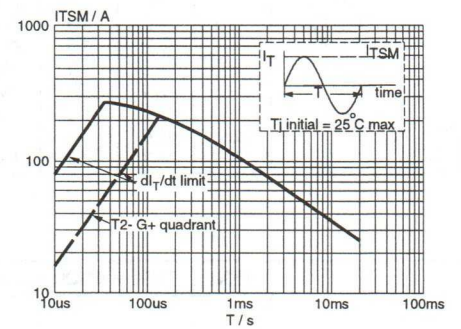



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

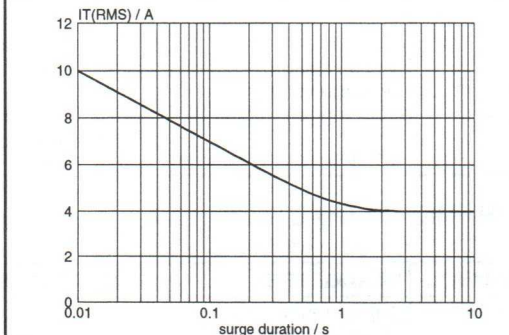



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

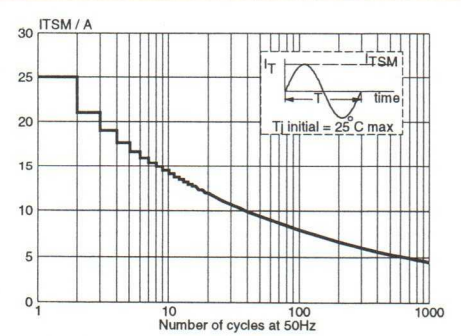



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

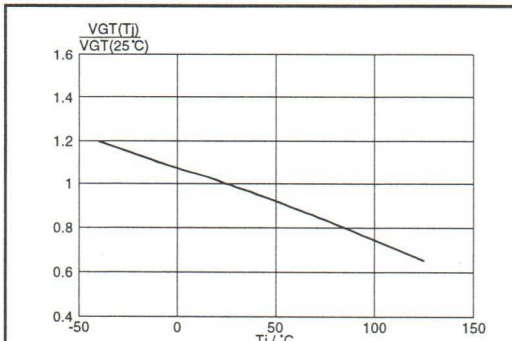



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

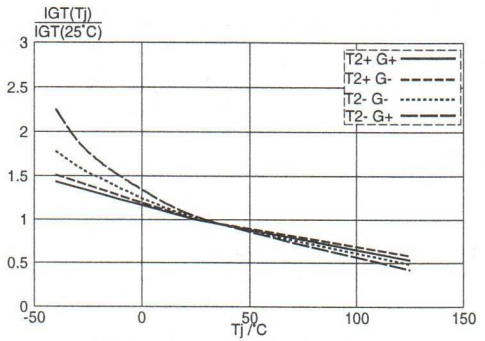



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

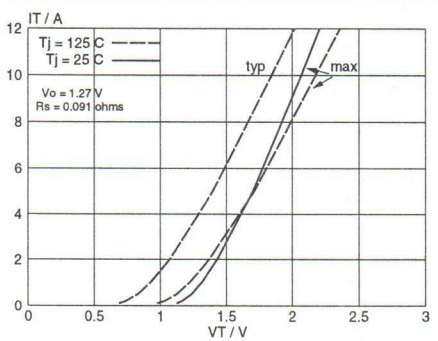



*Fig.10. Typical and maximum on-state characteristic.*

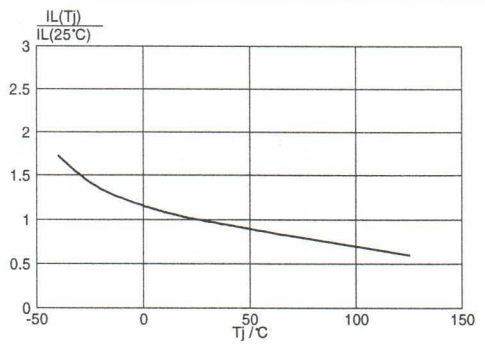



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

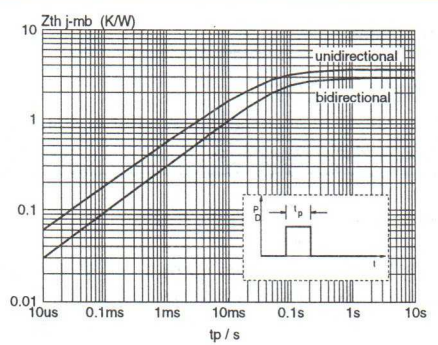



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

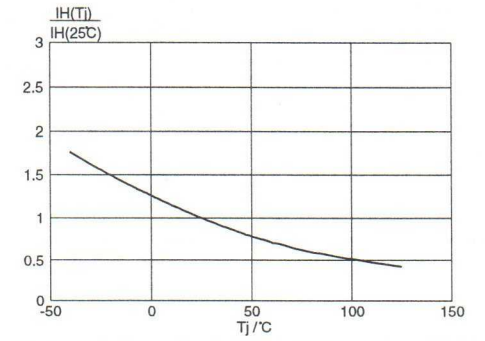



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

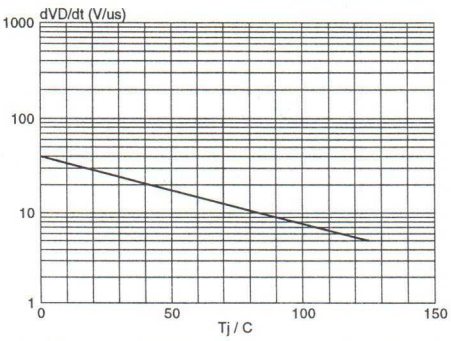



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs sensitive gate

# BT134 series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

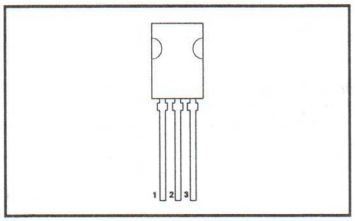
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT134- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

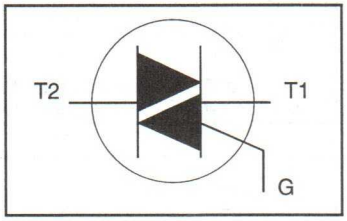
## PINNING - SOT82

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 100 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 15 | mA |
| | | | T2+ G- | - | 10 | 20 | mA |
| | | | T2- G- | - | 2.5 | 15 | mA |
| | | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

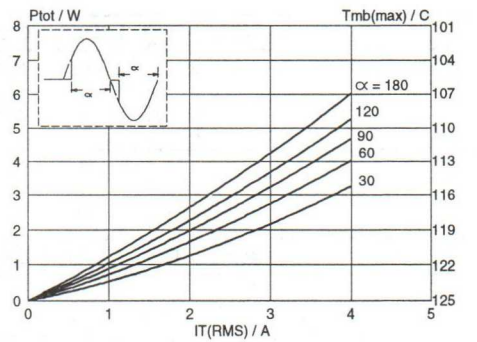



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

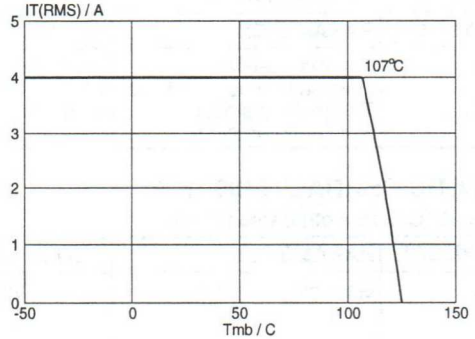



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

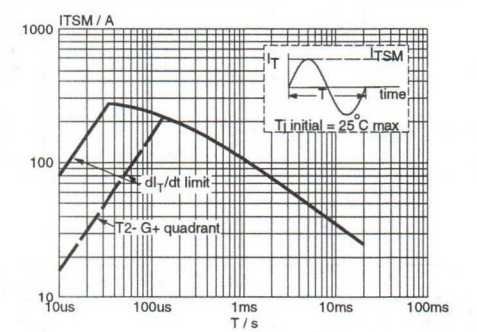



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

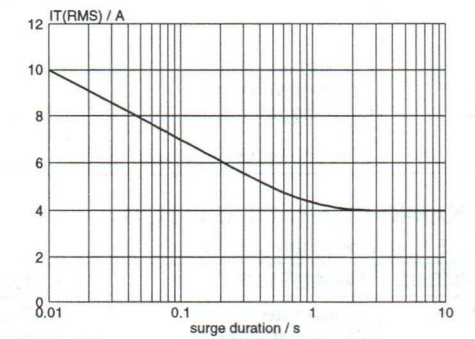



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

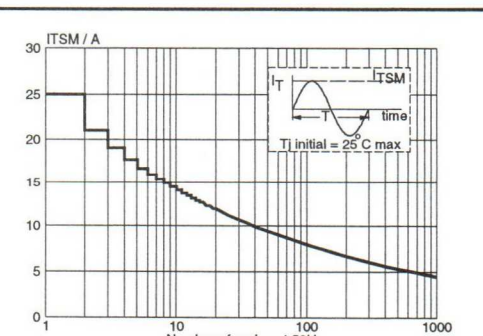



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

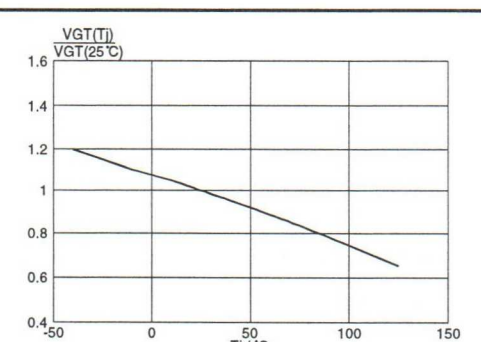



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

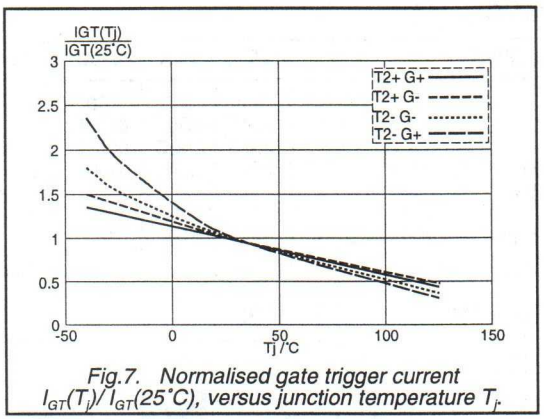



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

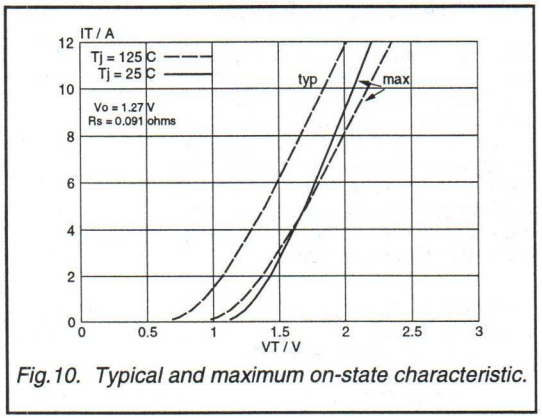



*Fig.10. Typical and maximum on-state characteristic.*

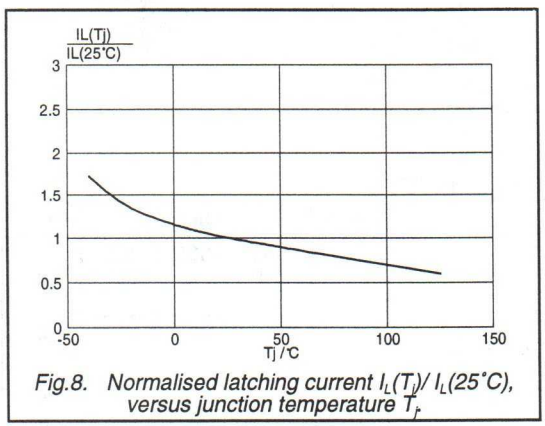



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

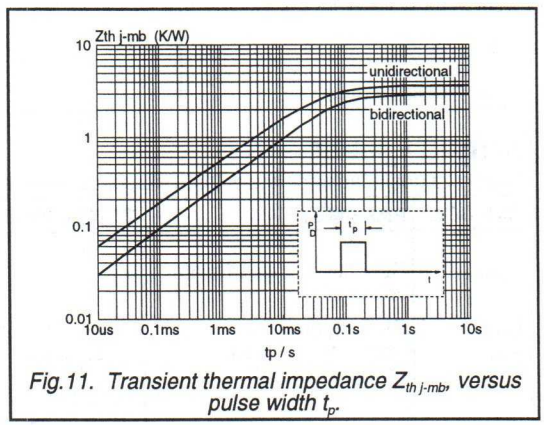



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

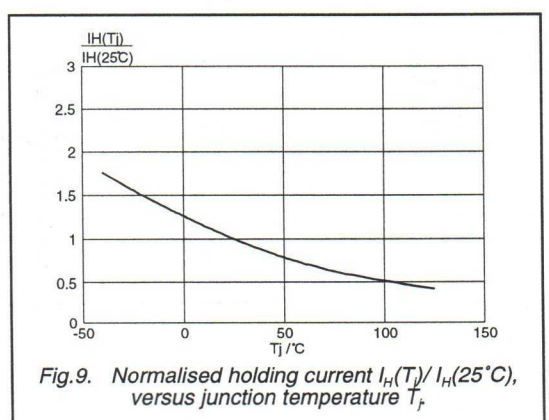



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

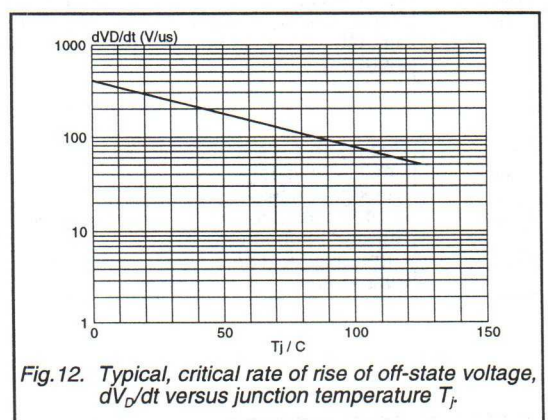



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

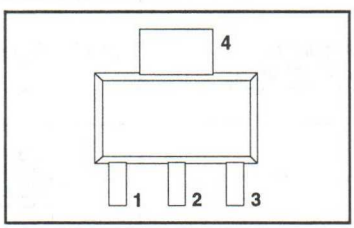
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT134W-** | **500** | **600** | **800** | |
| | **BT134W-** | **500F** | **600F** | **800F** | |
| | **BT134W-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | 10 | A |

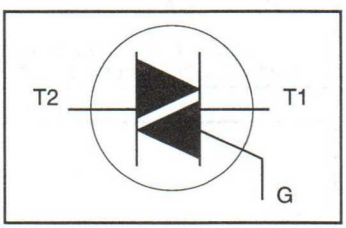
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108$ °C | - | 1 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 10 | | | A |
| | | t = 16.7 ms | - | 11 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.5 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | full or half cycle | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT134W- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.2 | | 1.50 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT134W- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ =67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 1 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 1.5 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; | - | - | - | 2 | - | µs |

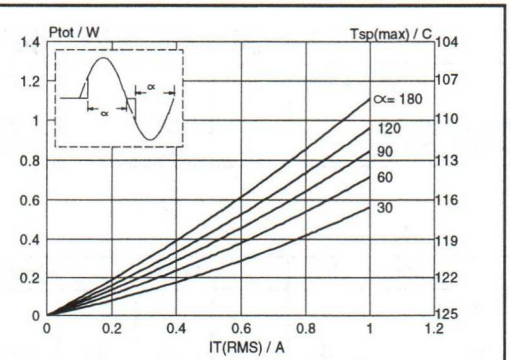



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

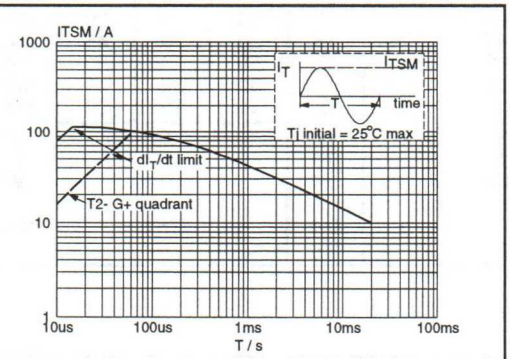



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

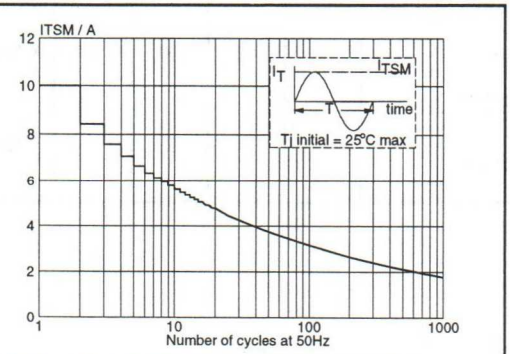



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

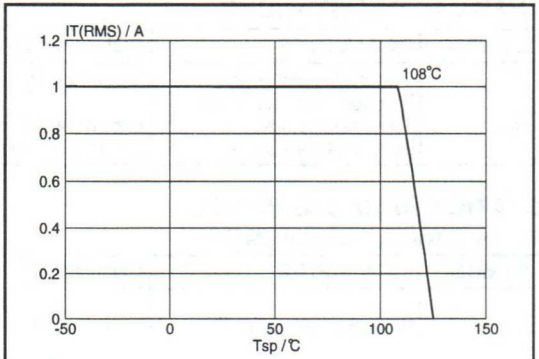



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

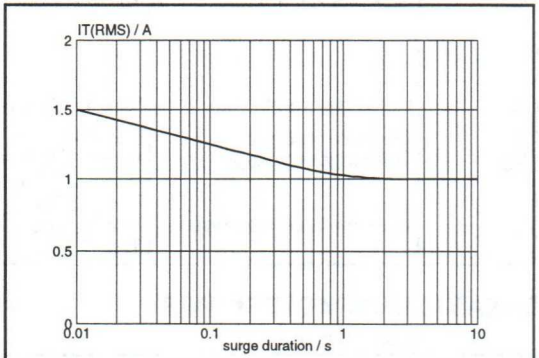



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108°C$.*

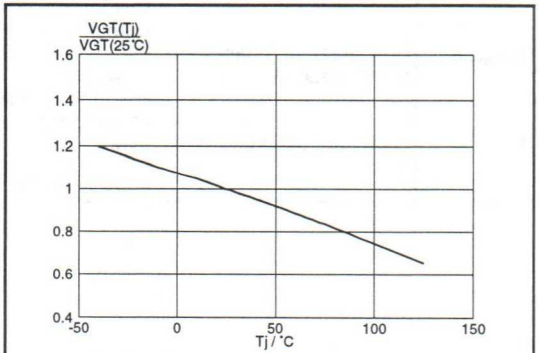



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

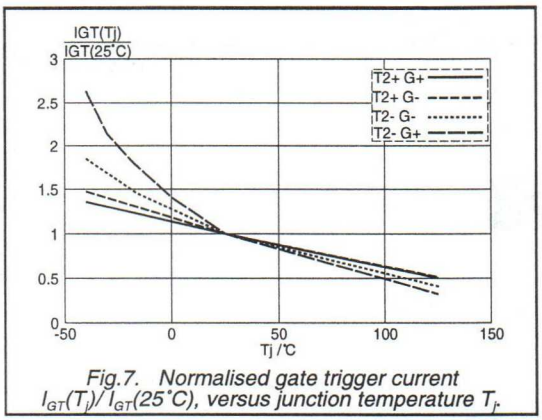



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

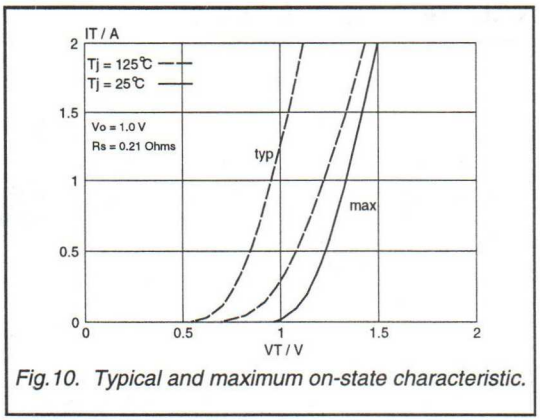



*Fig.10. Typical and maximum on-state characteristic.*

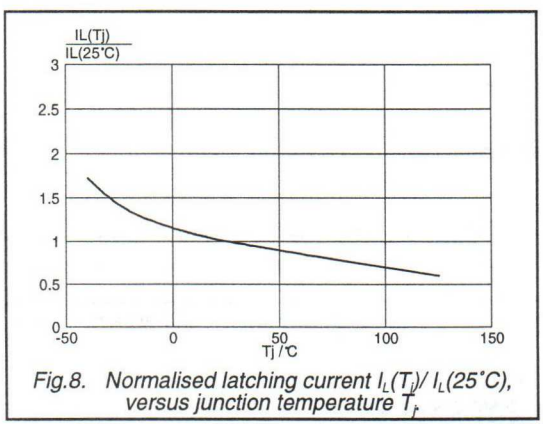



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

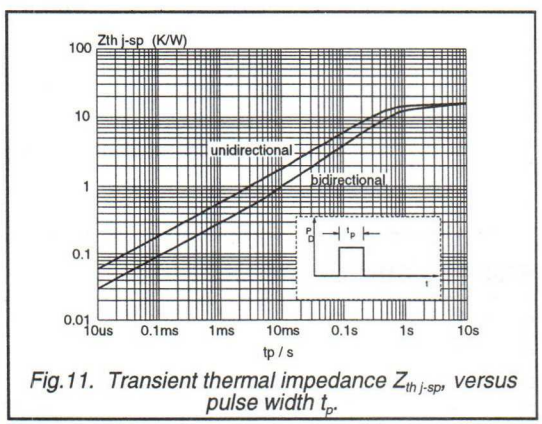



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width $t_p$.*

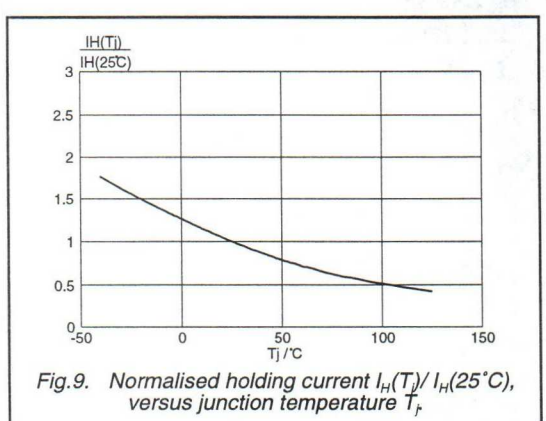



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

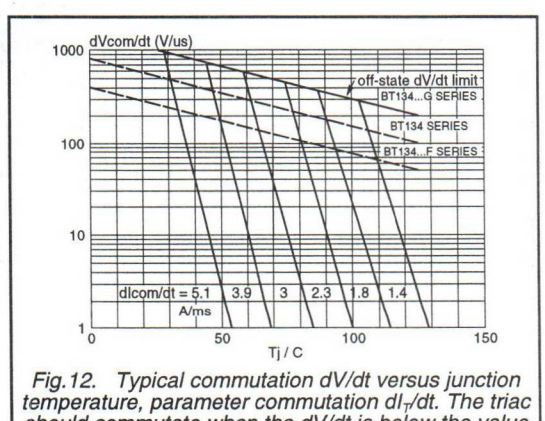



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

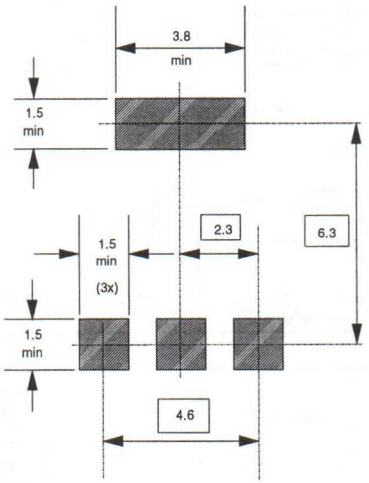



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

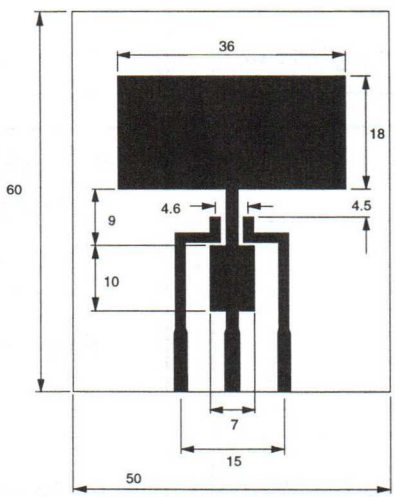



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

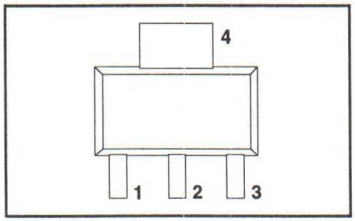
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT134W- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | A |

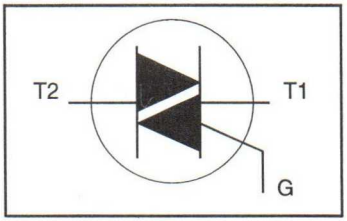
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | -500 | -600 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108$ °C | - | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 10 | | A |
| | | t = 16.7 ms | - | 11 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.5 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 1.5 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | full or half cycle | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of change of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 1.5 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

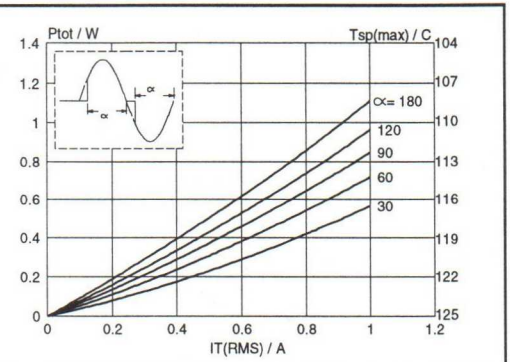



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

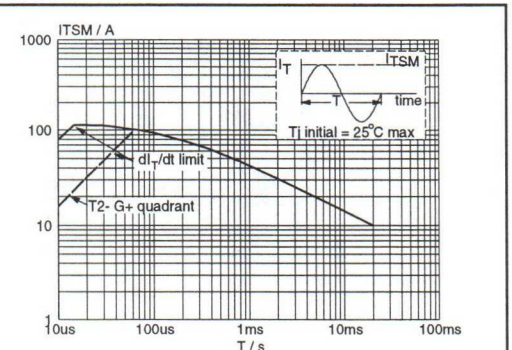



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

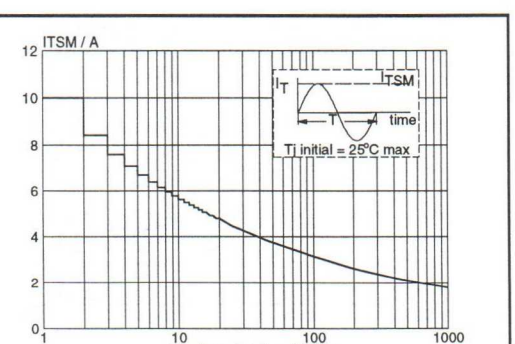



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

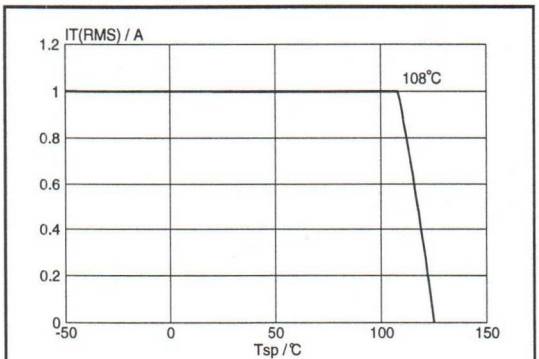



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

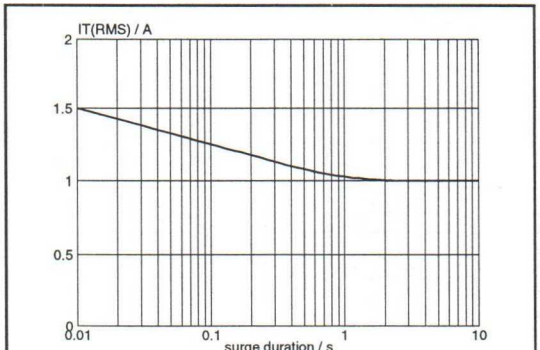



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108°C$.*

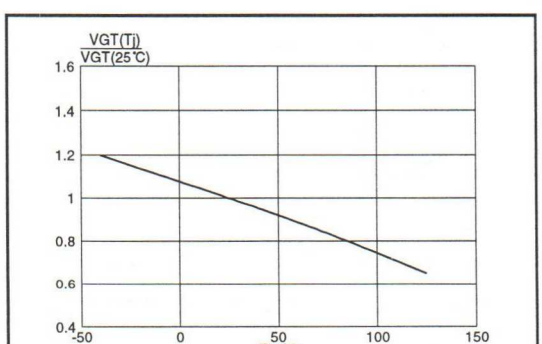



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

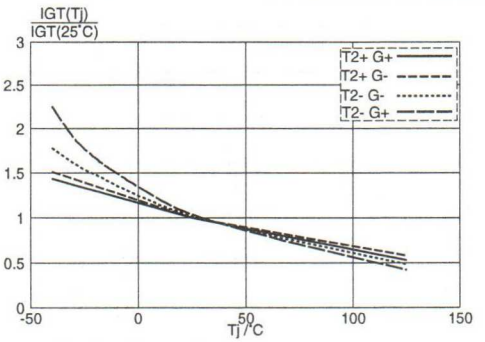



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

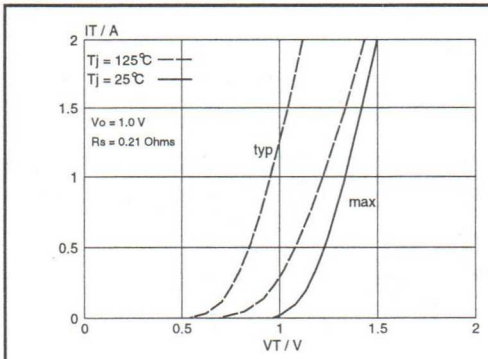



*Fig.10. Typical and maximum on-state characteristic.*

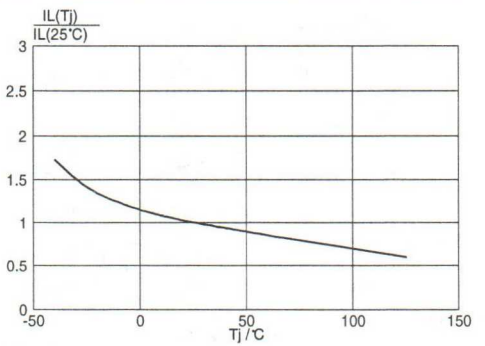



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

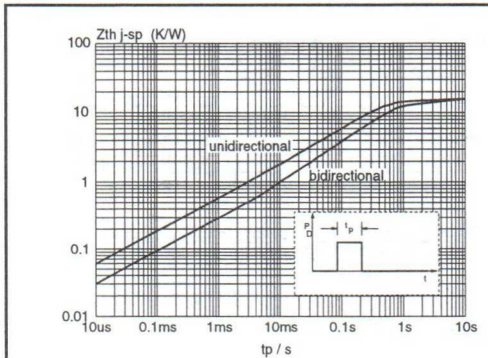



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width $t_p$.*

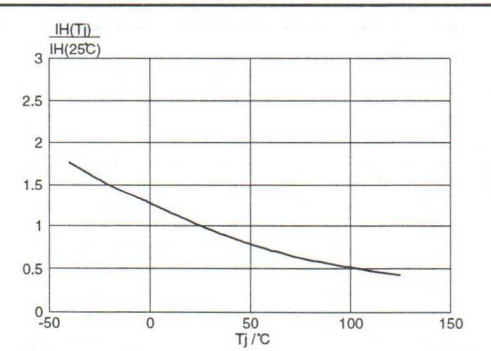



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

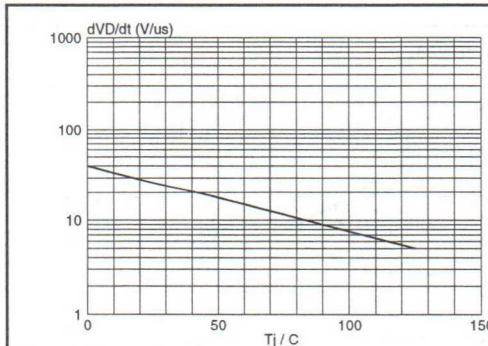



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

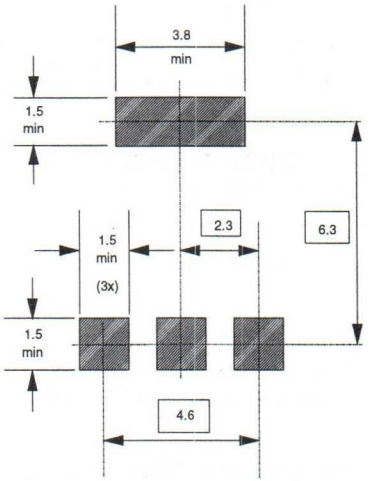



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

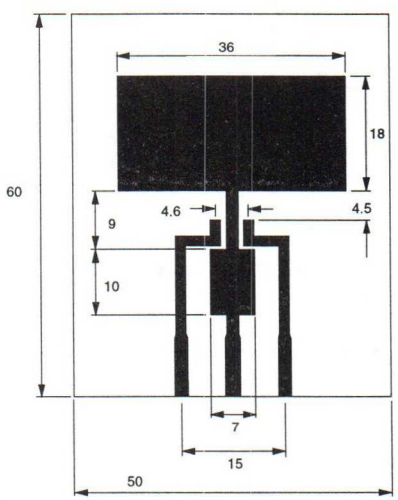



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

# Triacs sensitive gate

# BT134W series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

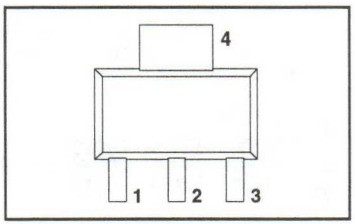
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT134W- | 500E | 600E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | A |

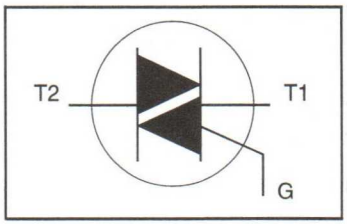
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | -500 | -600 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108$ °C | - | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 10 | | A |
| | | t = 16.7 ms | - | 11 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.5 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | full or half cycle | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 15 | mA |
| | | | T2+ G- | - | 10 | 20 | mA |
| | | | T2- G- | - | 2.5 | 15 | mA |
| | | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 30 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 1.5 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

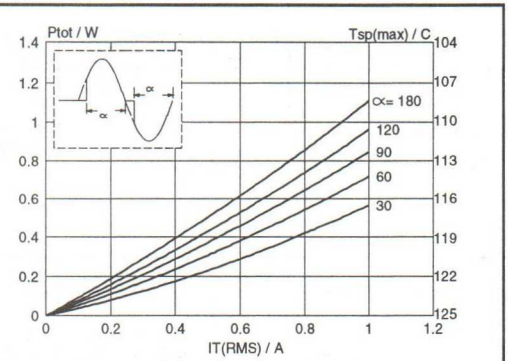



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

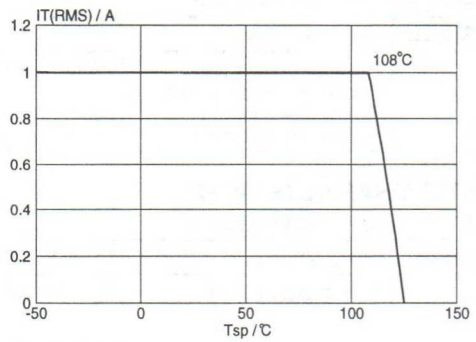



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

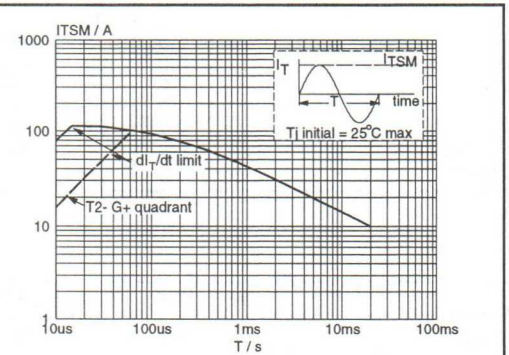



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

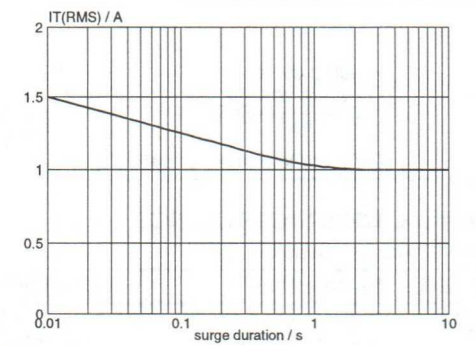



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108°C$.*

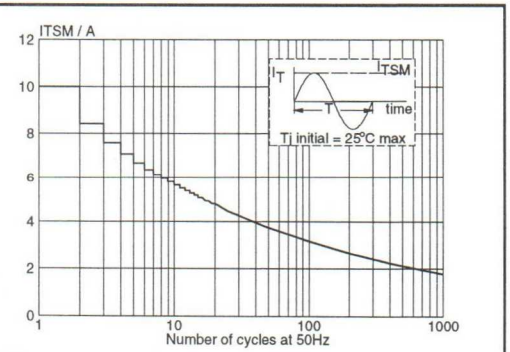



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

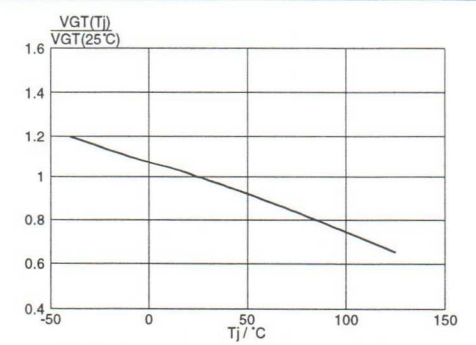



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

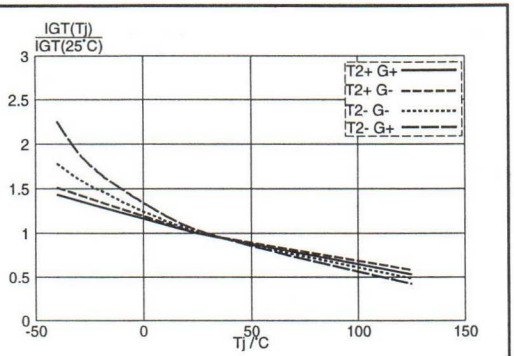



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

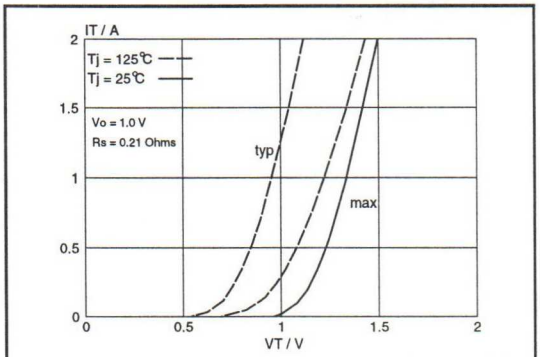



*Fig.10. Typical and maximum on-state characteristic.*

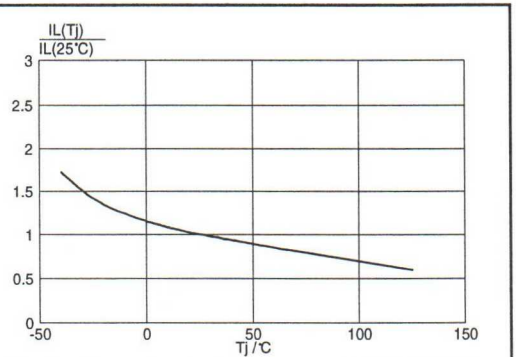



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

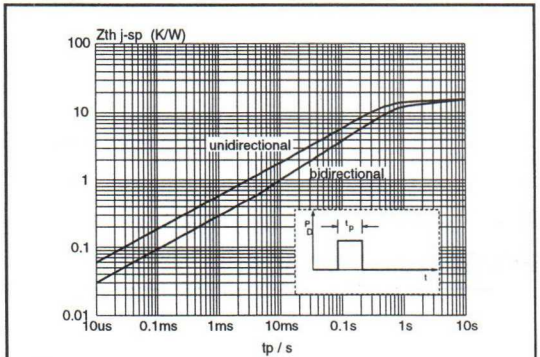



*Fig.11. Transient thermal impedance $Z_{th\,j\text{-}sp}$, versus pulse width $t_p$.*

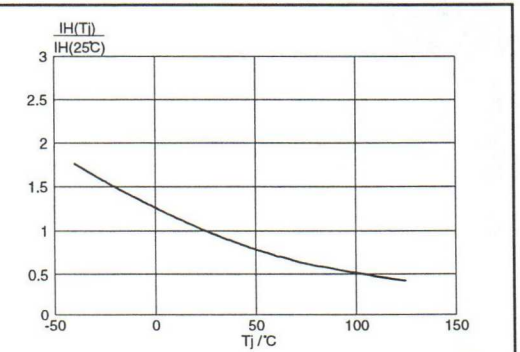



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

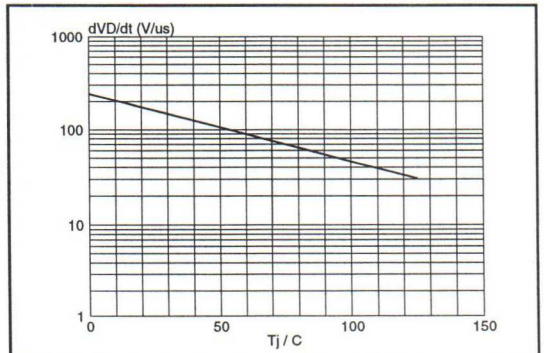



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

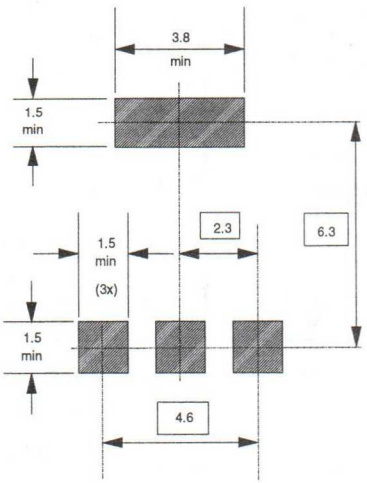



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

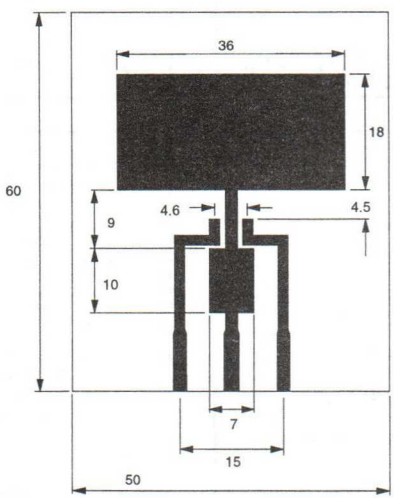



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

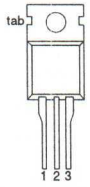
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT136-** | **500** | **600** | **800** | |
| | **BT136-** | **500F** | **600F** | **800F** | |
| | **BT136-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

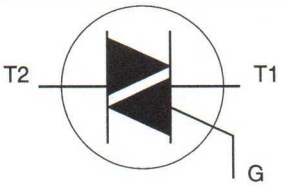
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.70 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 4 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

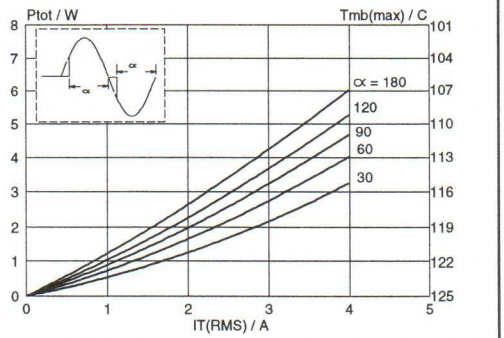



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

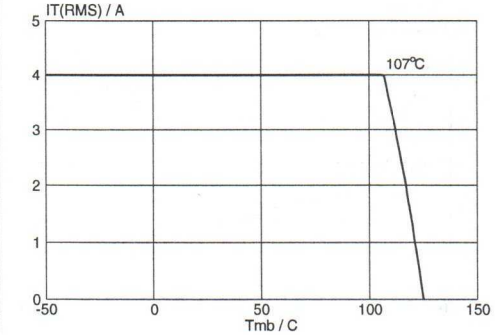



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

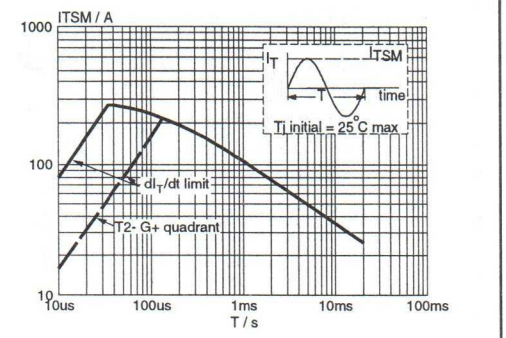



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

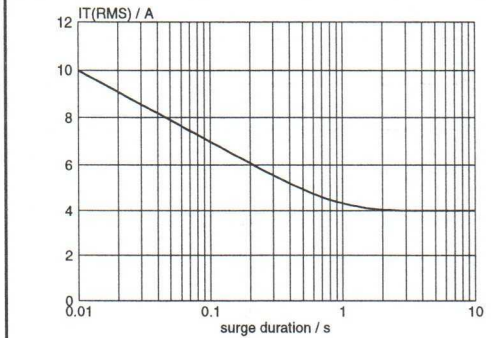



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

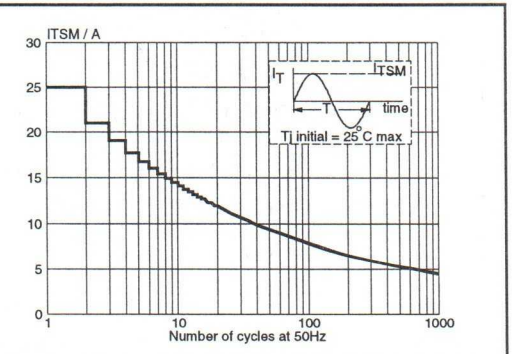



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

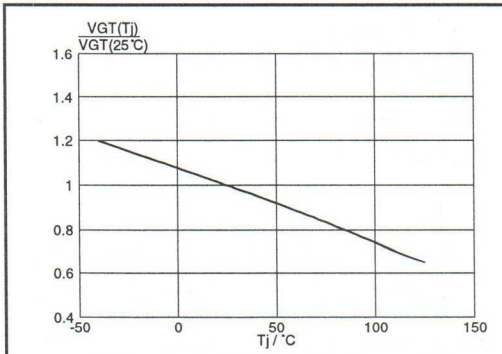



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

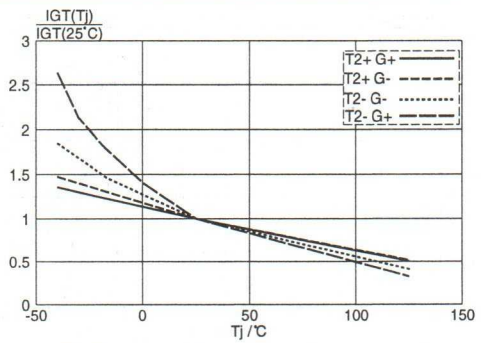



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

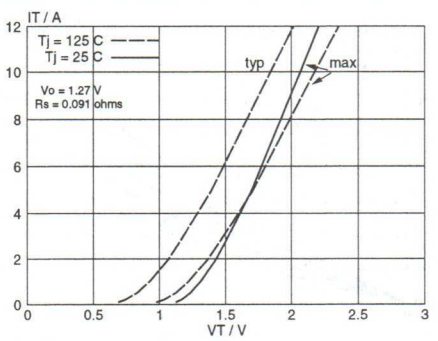



*Fig.10. Typical and maximum on-state characteristic.*

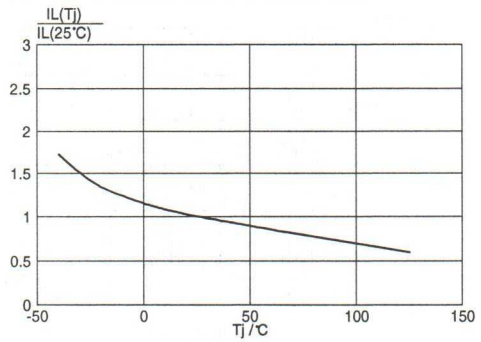



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

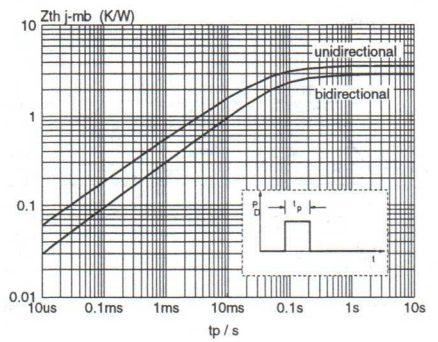



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

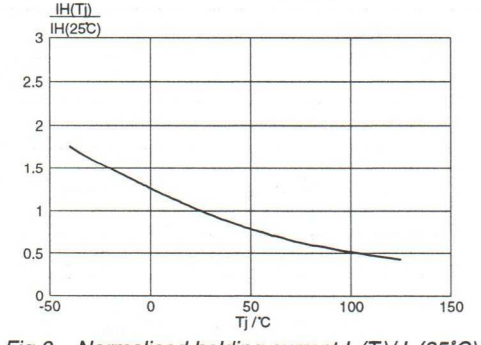



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

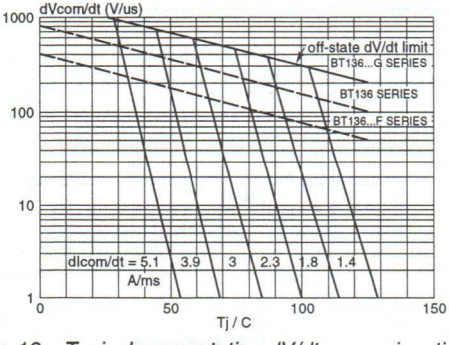



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs logic level

# BT136 series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

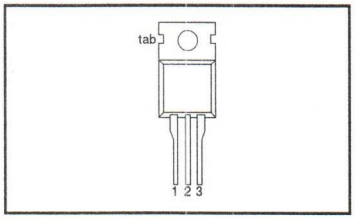
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | **BT136-** | **500D** | **600D** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | A |

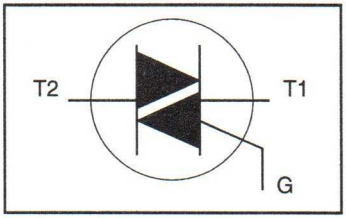
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 25 | | A |
| | | t = 16.7 ms | - | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

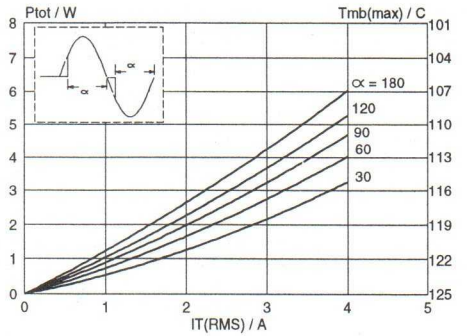



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

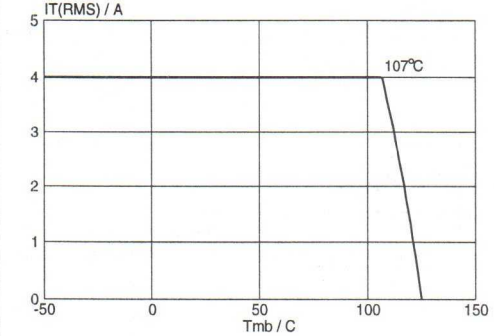



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

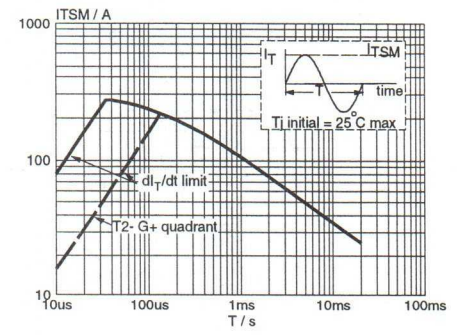



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

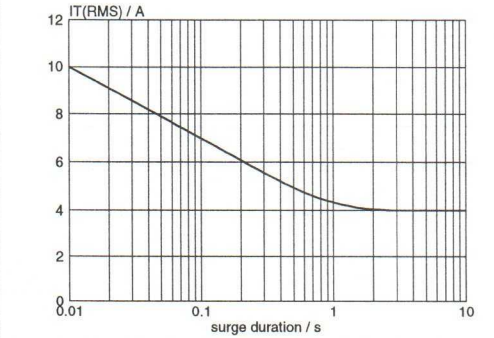



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

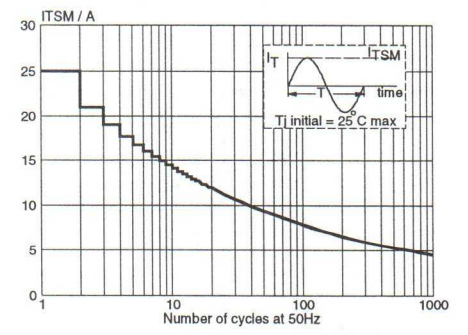



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

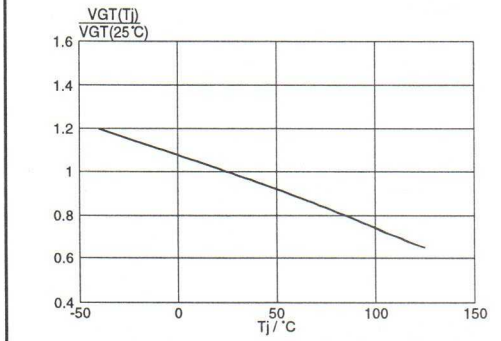



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

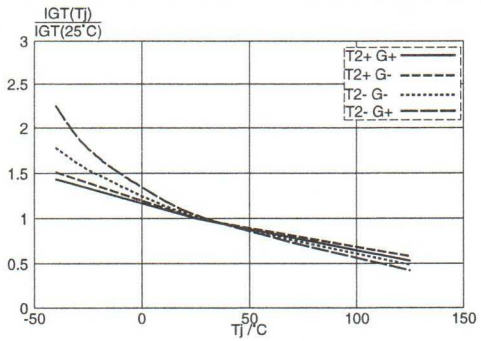



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

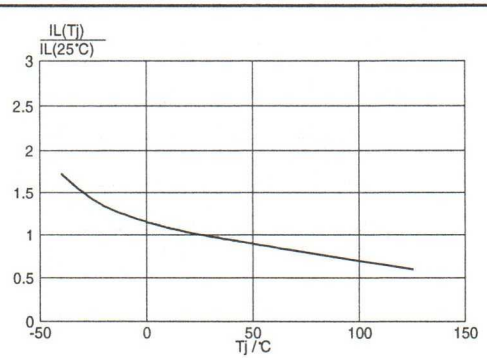



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

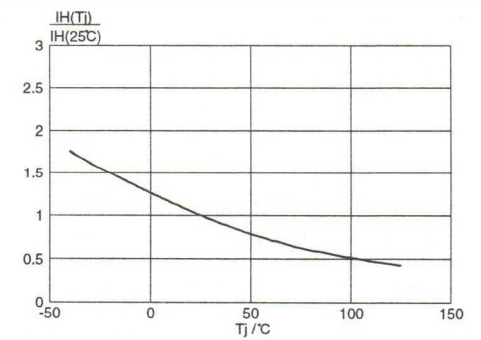



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

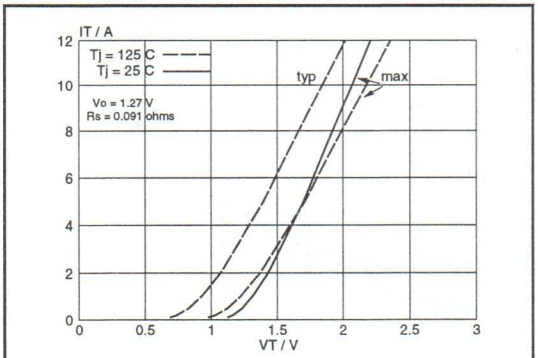



*Fig.10. Typical and maximum on-state characteristic.*

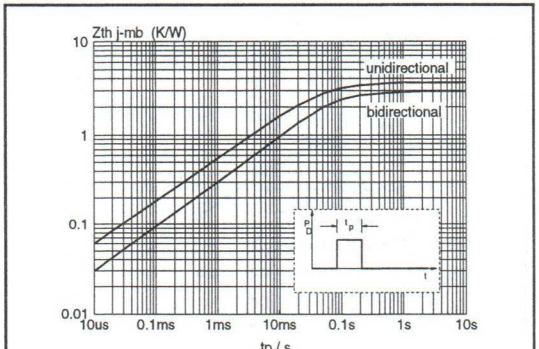



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

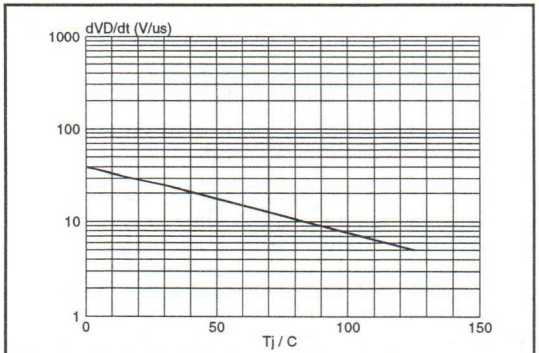



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs sensitive gate

# BT136 series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

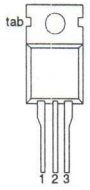
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT136- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

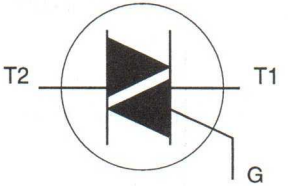
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 15 | mA |
| | | | T2+ G- | - | 10 | 20 | mA |
| | | | T2- G- | - | 2.5 | 15 | mA |
| | | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

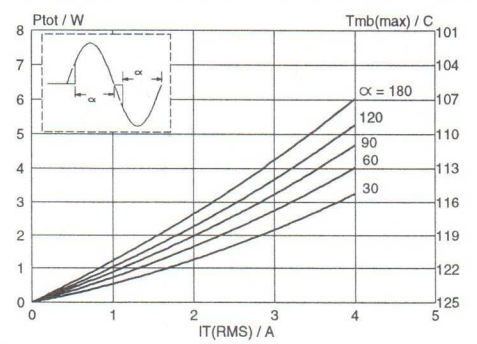



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

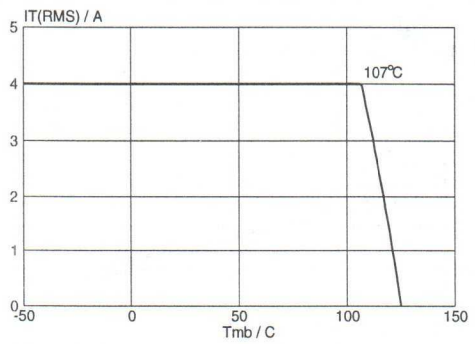



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

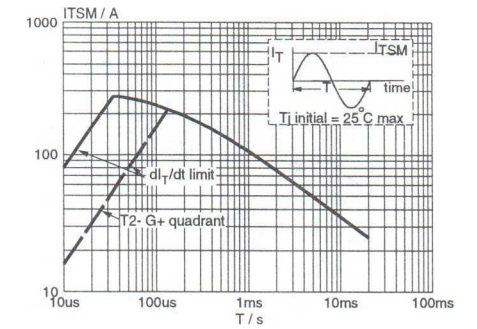



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

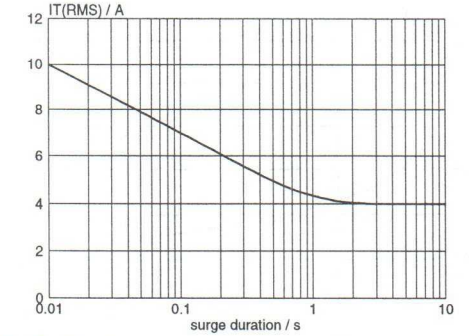



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

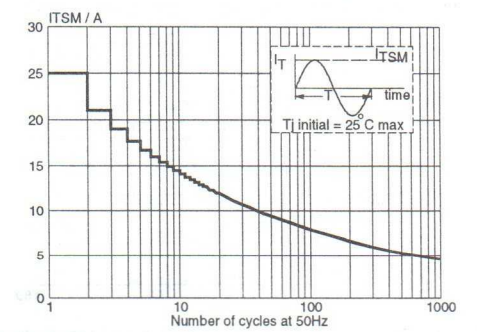



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

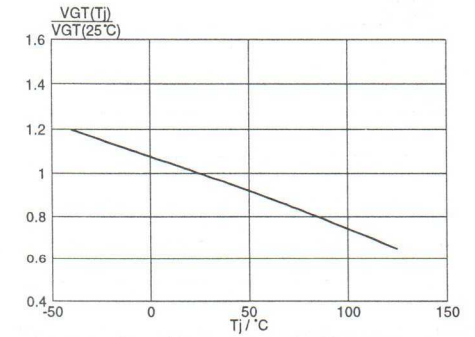



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

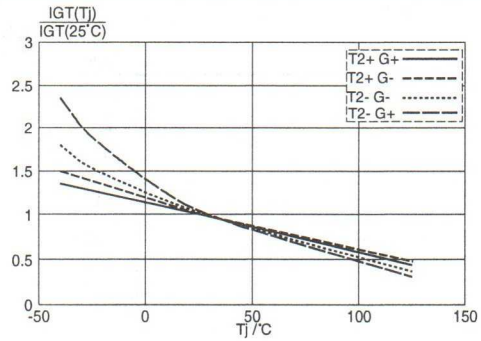



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

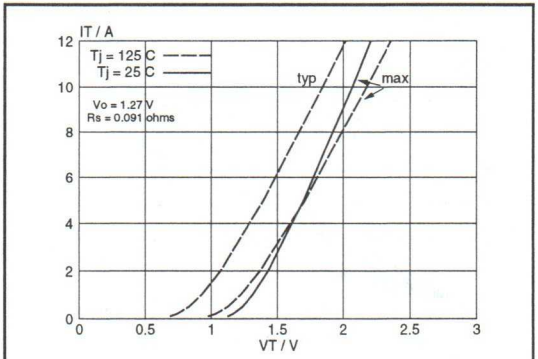



*Fig.10. Typical and maximum on-state characteristic.*

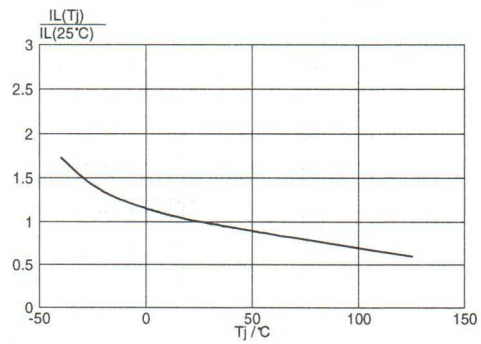



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

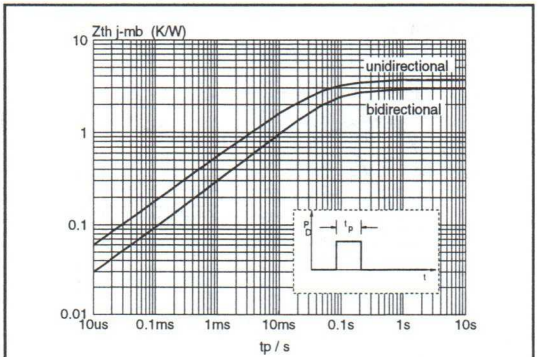



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

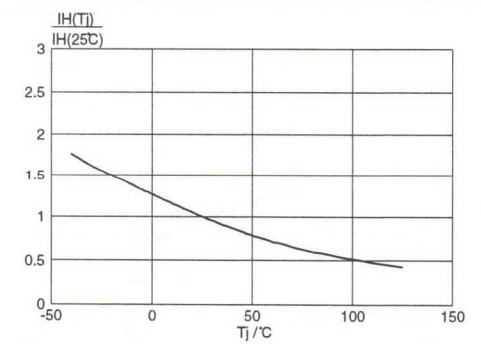



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

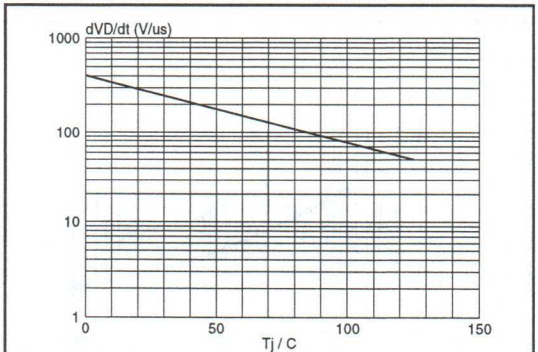



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

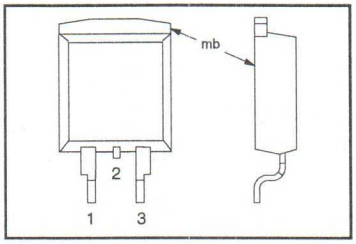
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT136B-** | **500** | **600** | **800** | |
| | **BT136B-** | **500F** | **600F** | **800F** | |
| | **BT136B-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

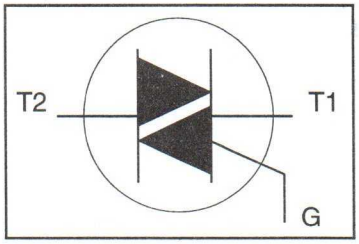
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136B- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.70 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136B- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 4 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

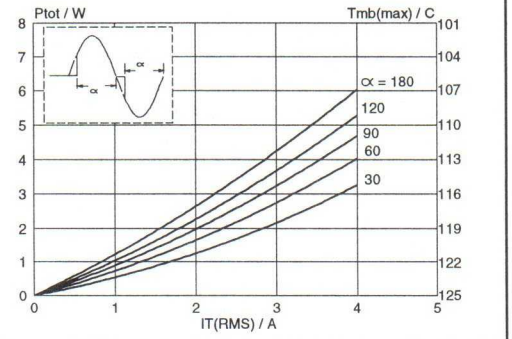



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

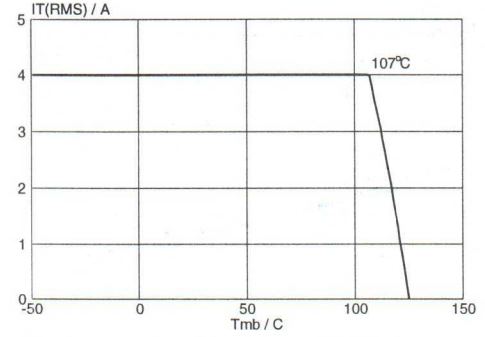



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

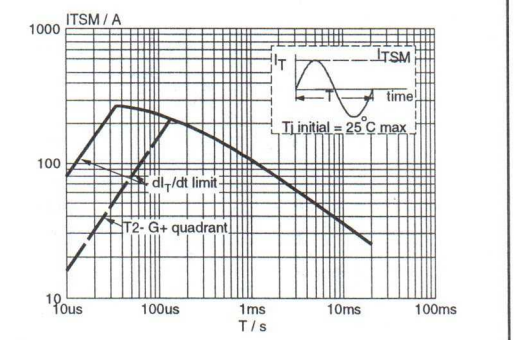



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

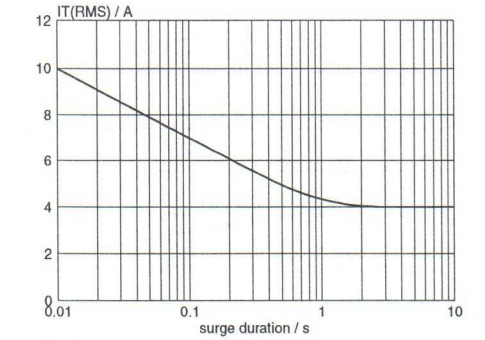



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

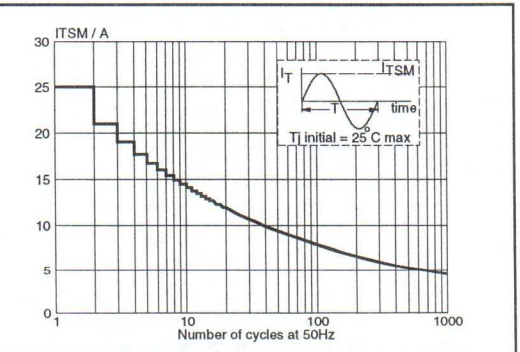



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

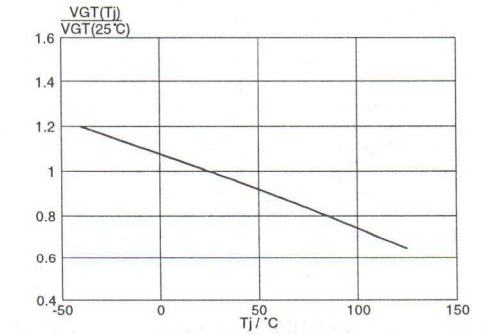



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

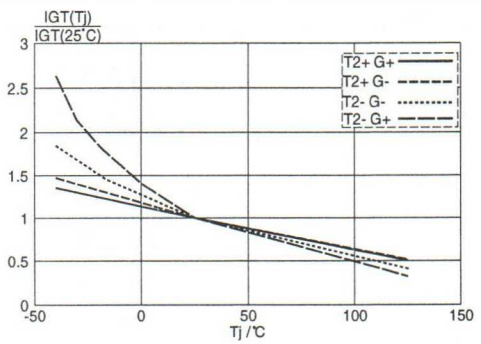



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

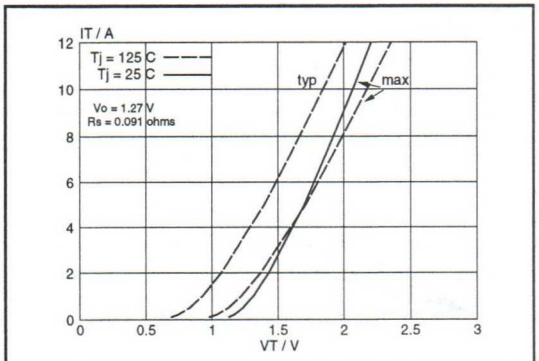



*Fig.10. Typical and maximum on-state characteristic.*

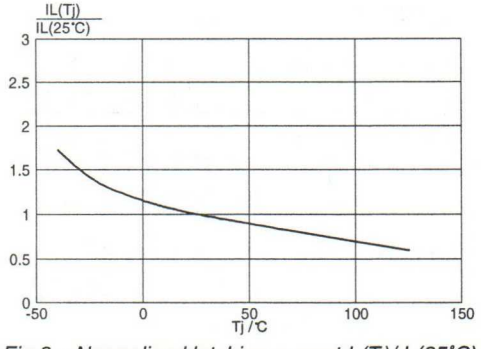



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

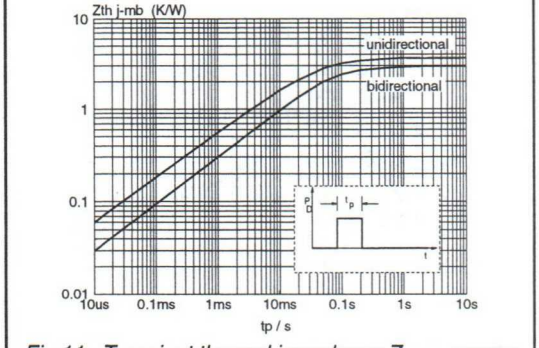



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

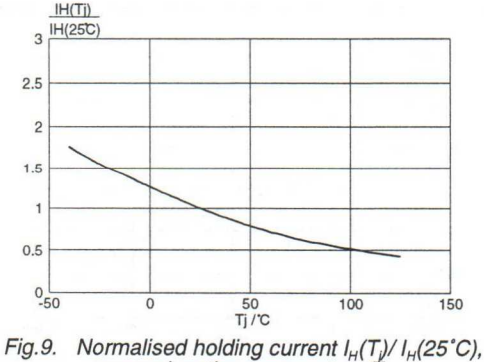



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

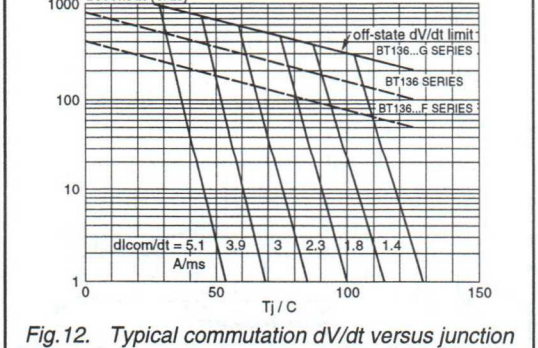



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

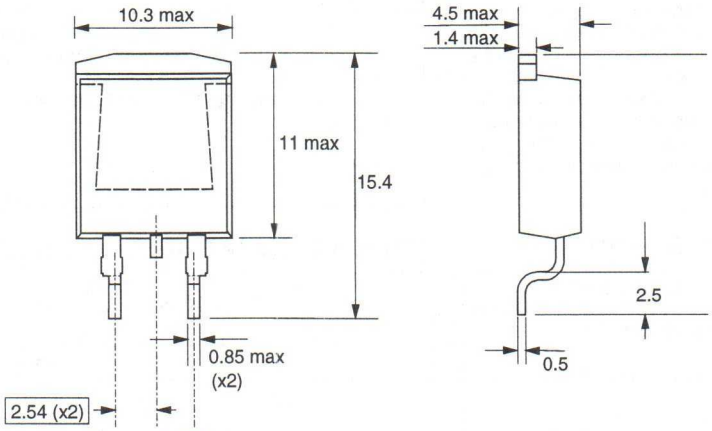



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

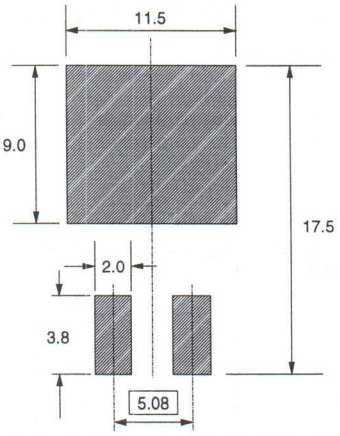



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs logic level

# BT136B series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

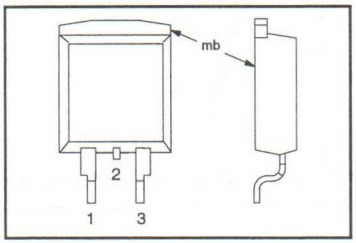
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT136B- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | A |

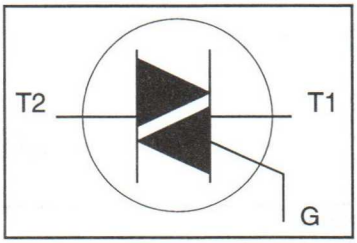
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | UNIT |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 25 | | A |
| | | t = 16.7 ms | - | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

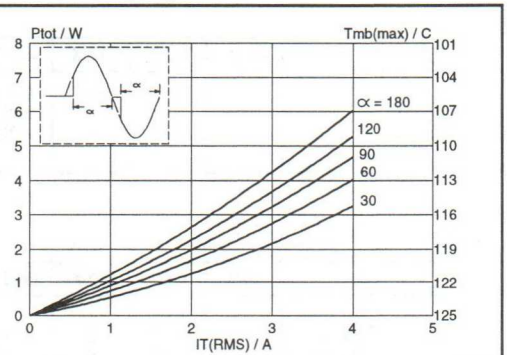



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

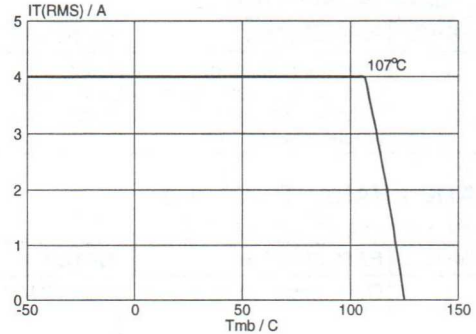



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

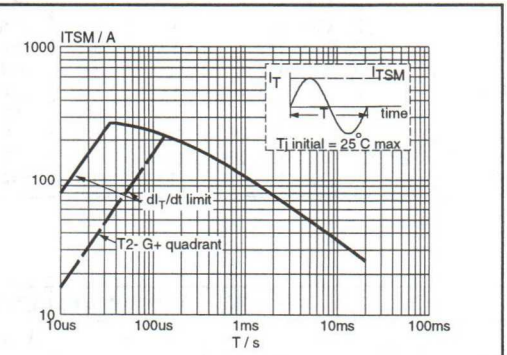



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

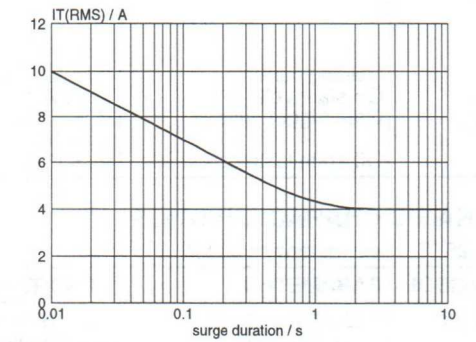



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

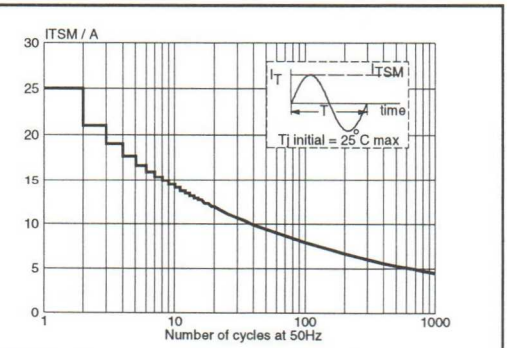



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

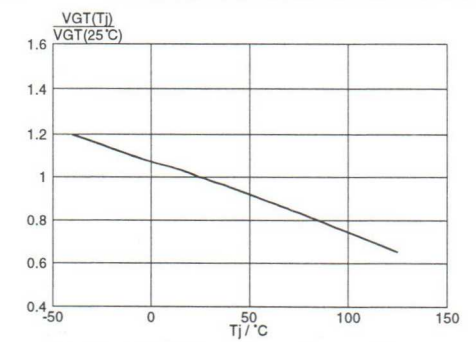



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

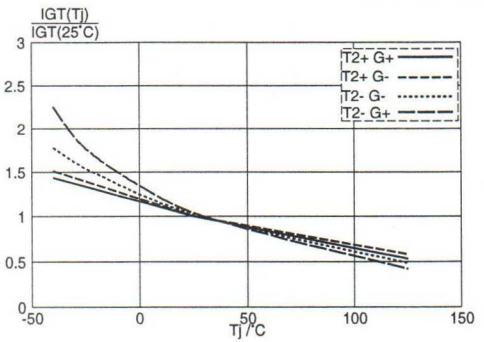



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

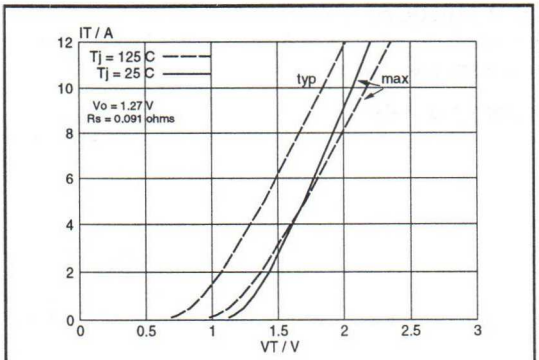



*Fig.10. Typical and maximum on-state characteristic.*

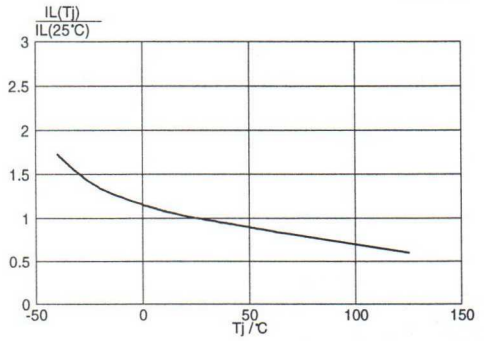



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

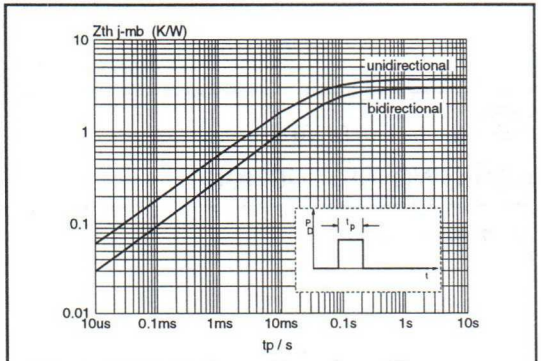



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

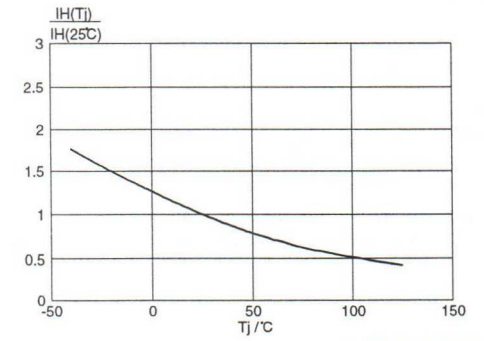



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

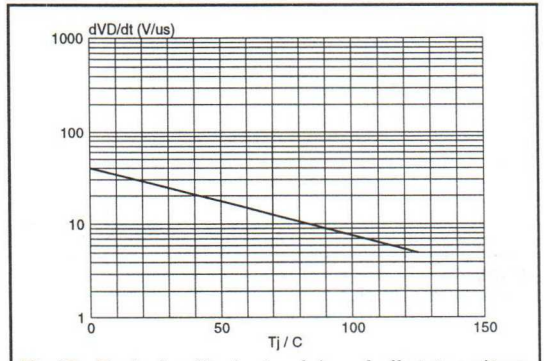



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

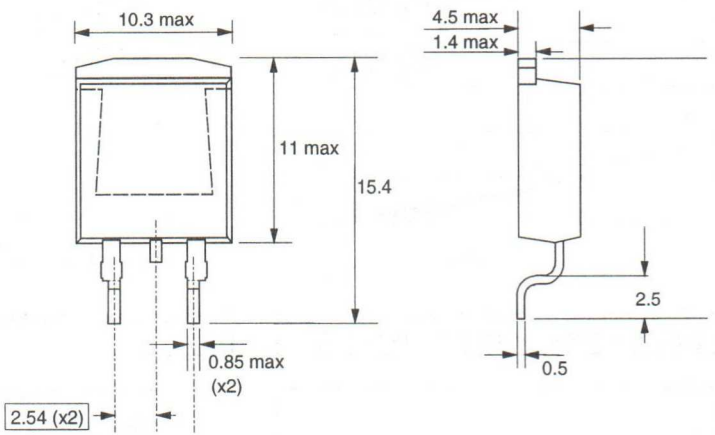



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

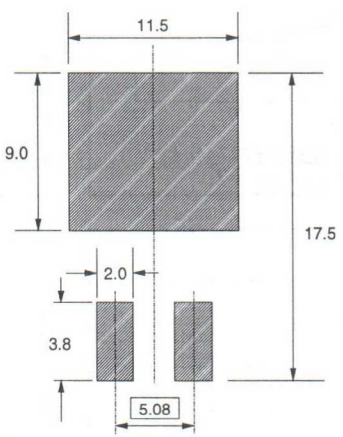



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT136B series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

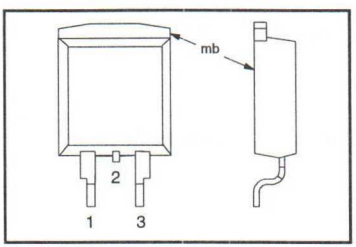
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT136B- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

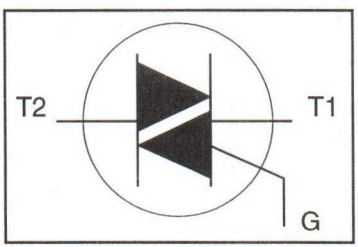
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 15 | mA |
| | | | T2+ G- | - | 10 | 20 | mA |
| | | | T2- G- | - | 2.5 | 15 | mA |
| | | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

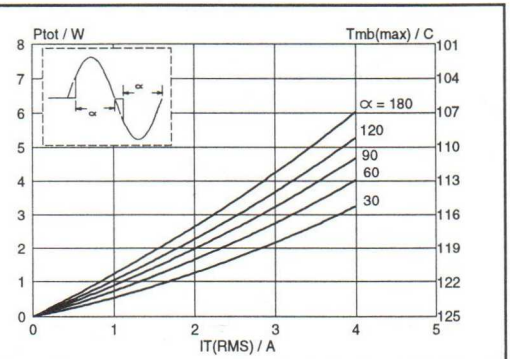



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

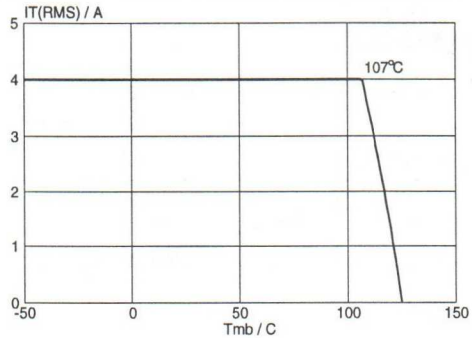



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

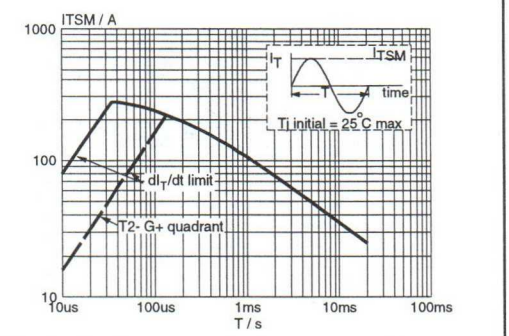



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

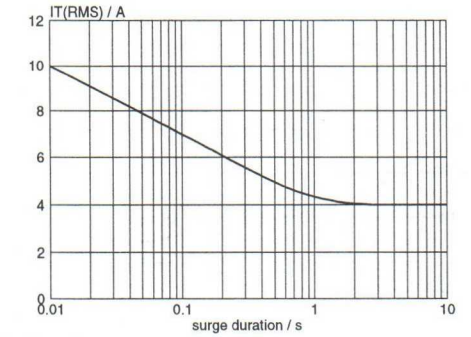



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

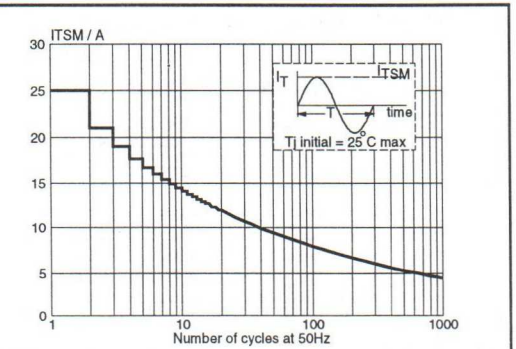



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

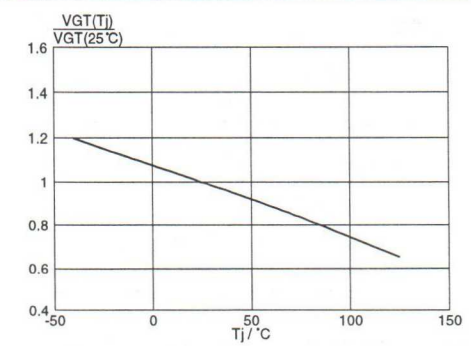



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

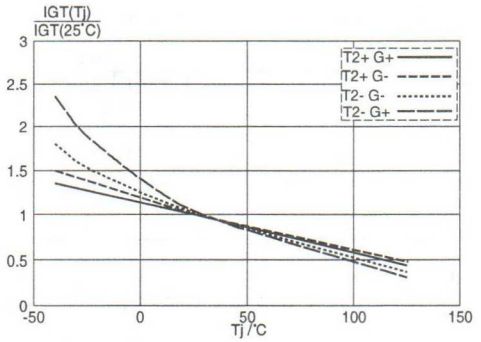



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

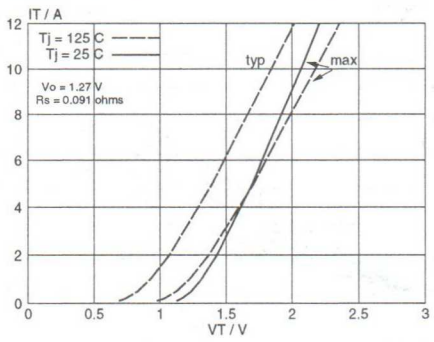



*Fig.10. Typical and maximum on-state characteristic.*

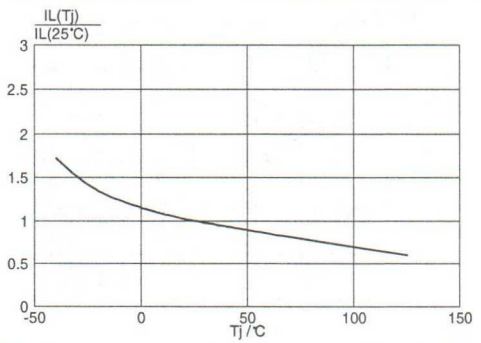



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

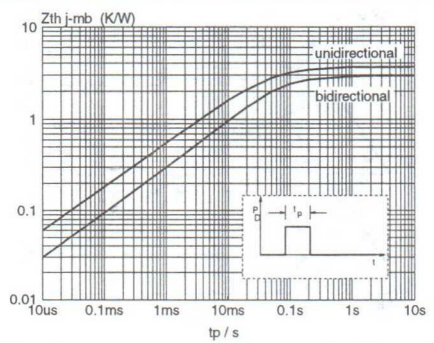



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

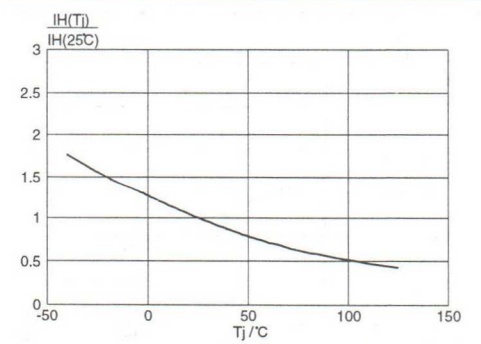



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

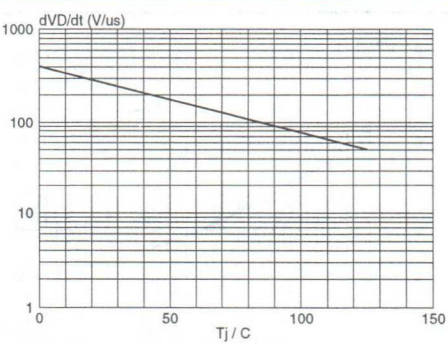



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

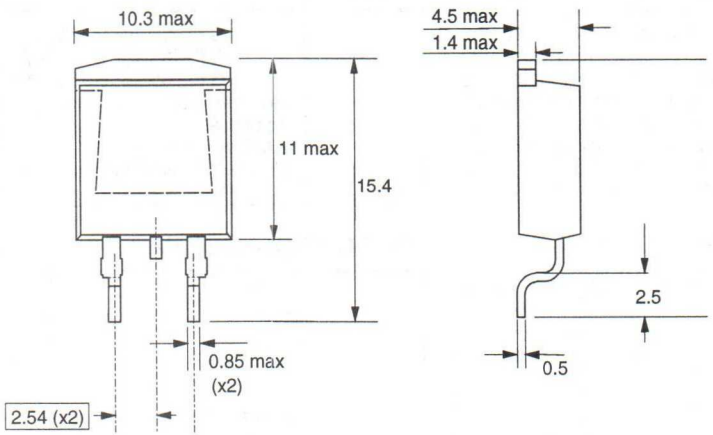



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

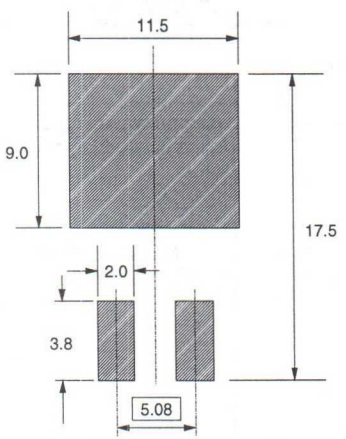



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

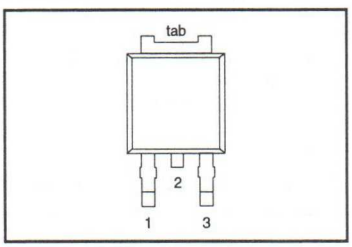
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT136S** (or BT136M)- | **500** | **600** | **800** | |
| | **BT136S** (or BT136M)- | **500F** | **600F** | **800F** | |
| | **BT136S** (or BT136M)- | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

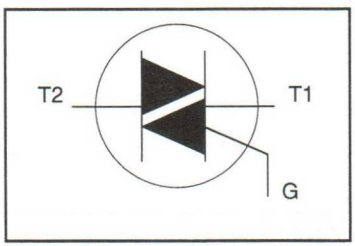
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BT136S-** | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.70 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BT136S** (or BT136M)- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 4 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

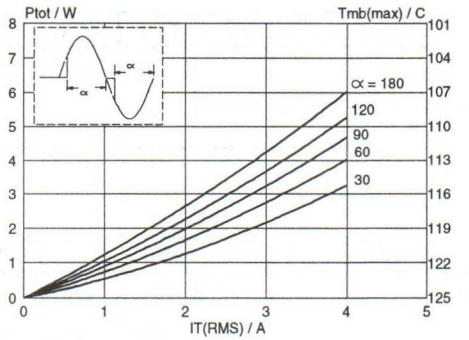



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

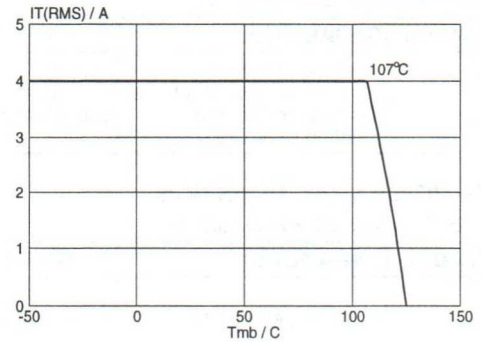



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

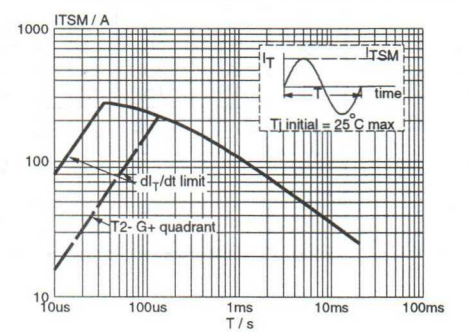



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

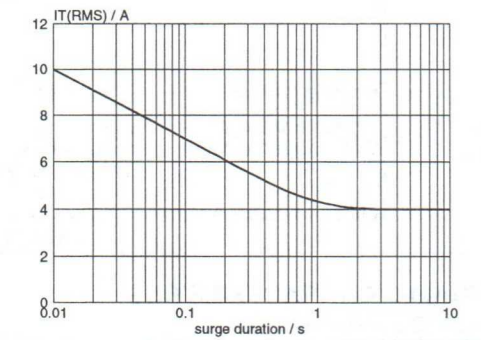



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

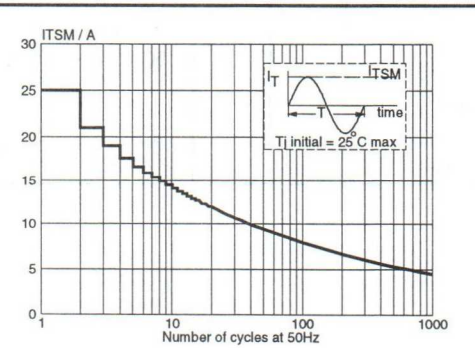



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

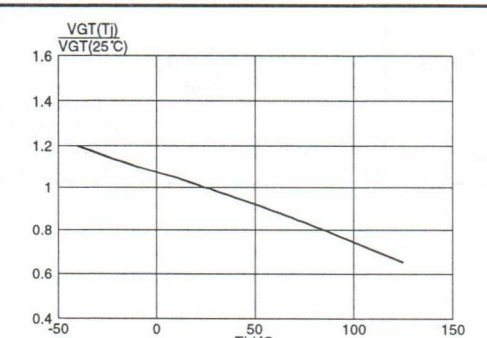



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

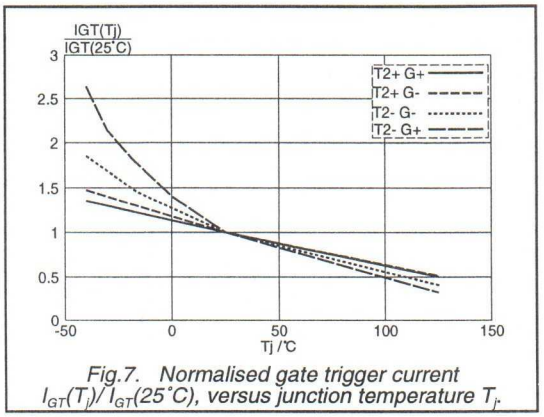



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

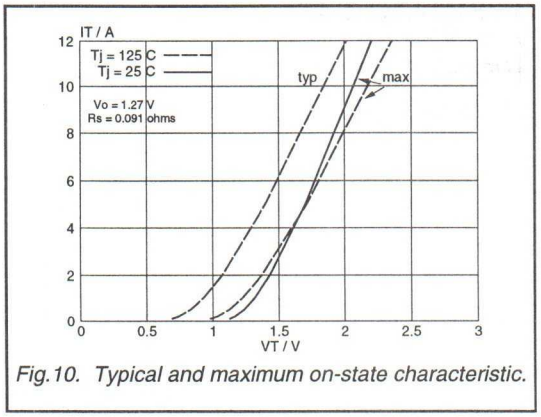



*Fig.10. Typical and maximum on-state characteristic.*

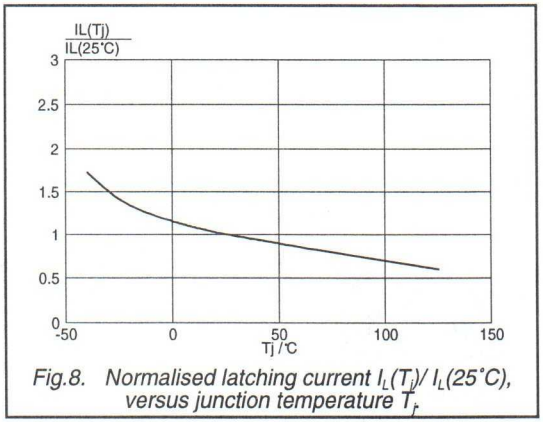



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

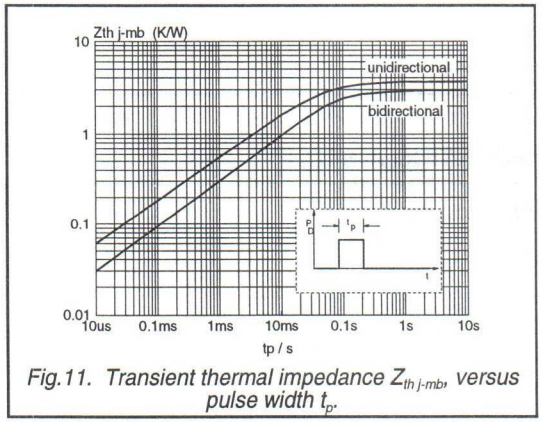



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

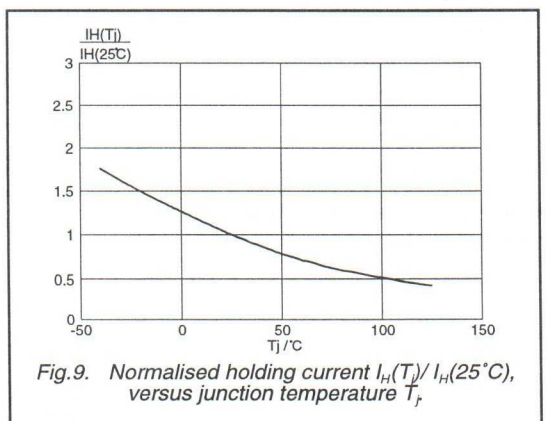



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

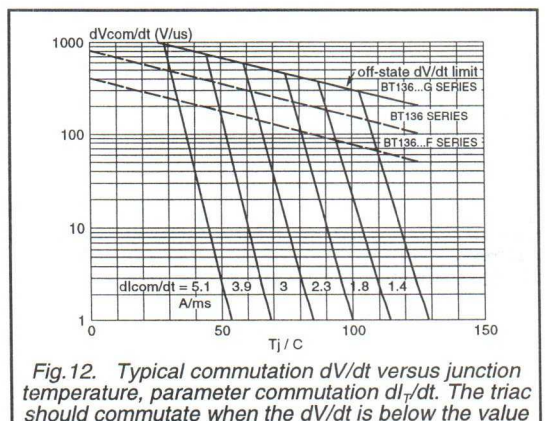



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

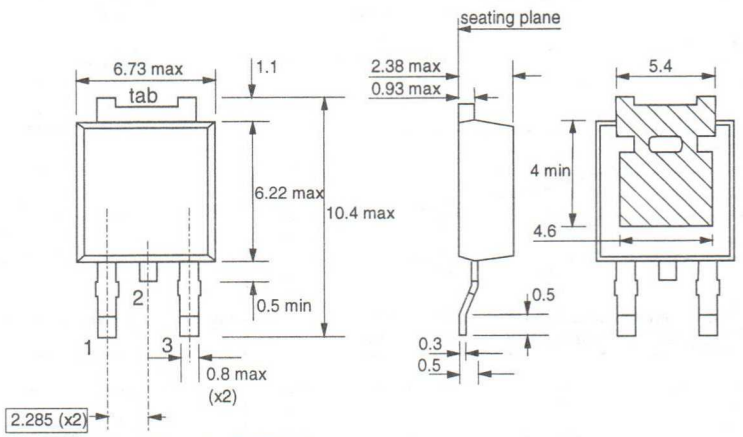



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

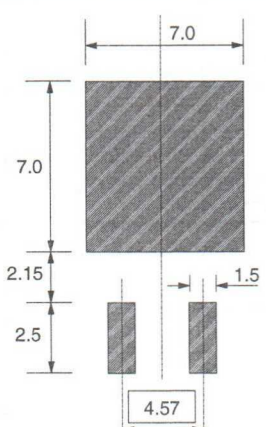



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Triacs logic level

# BT136S series D
BT136M series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

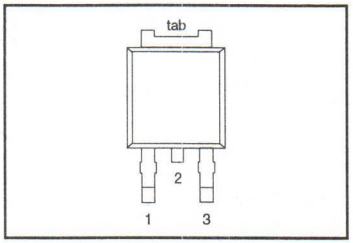
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | **BT136S** (or BT136M)- | **500D** | **600D** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | A |

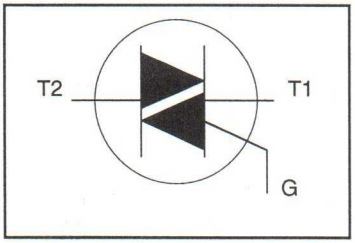
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 25 | | A |
| | | t = 16.7 ms | - | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

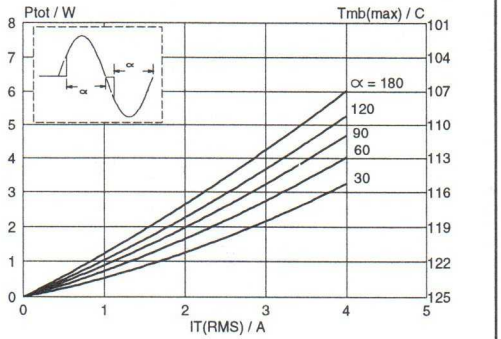



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

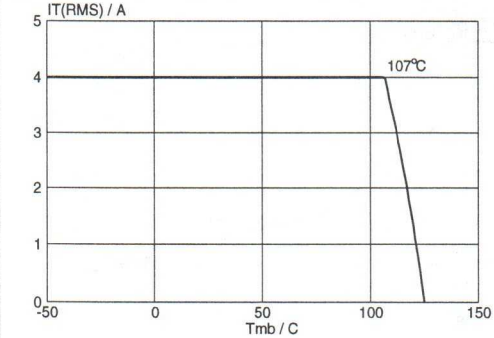



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

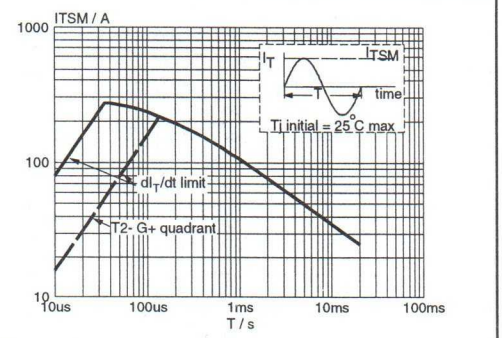



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

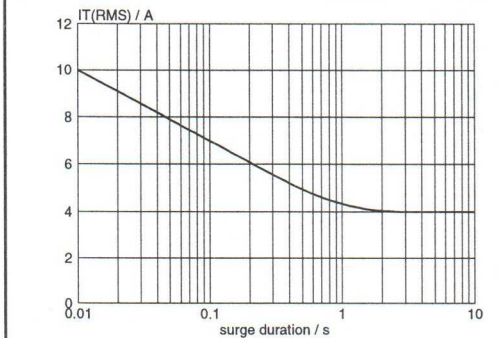



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

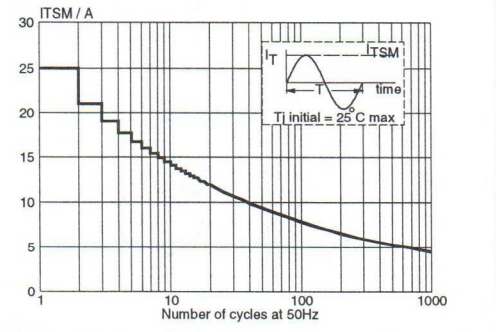



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

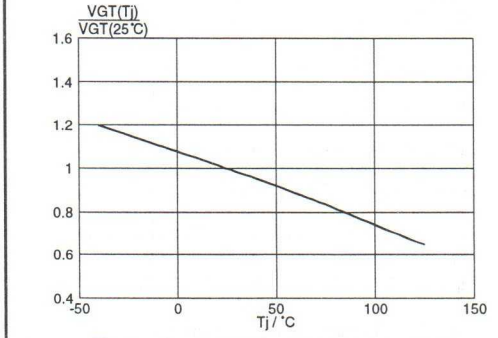



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

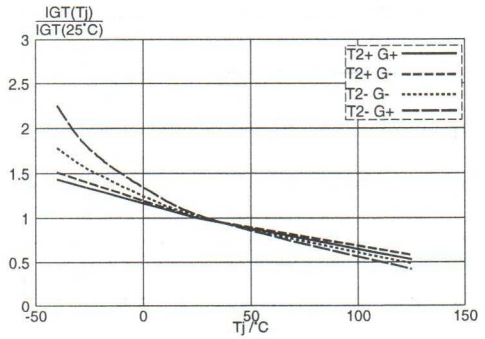



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

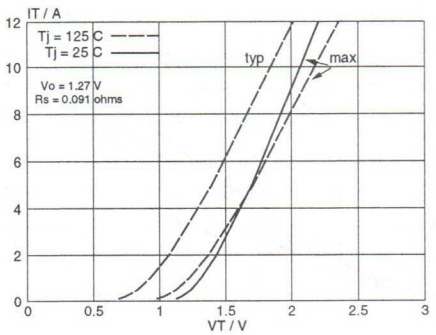



*Fig.10. Typical and maximum on-state characteristic.*

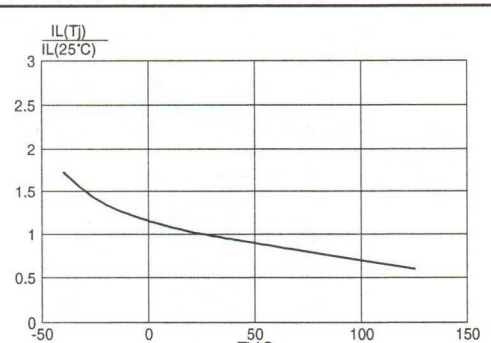



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

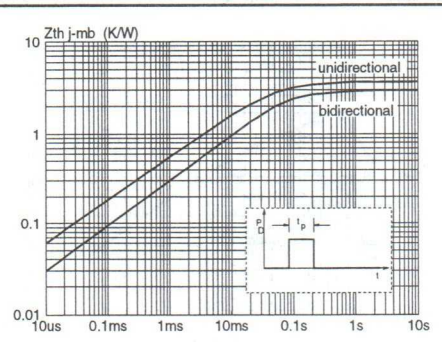



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

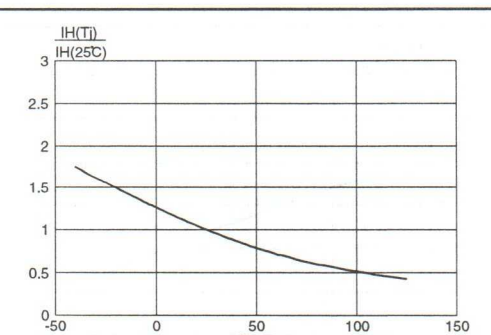



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

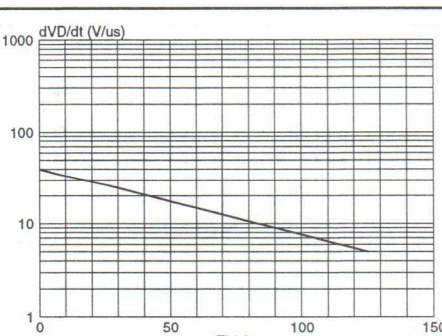



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

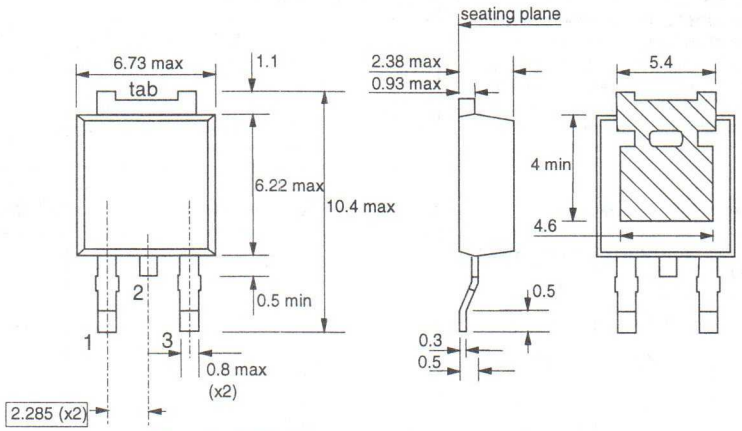



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

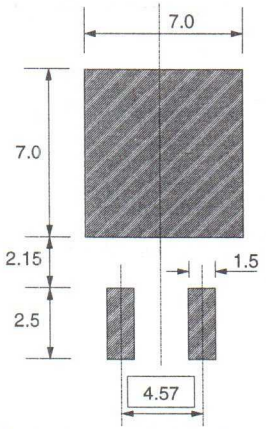



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT136S series E
BT136M series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

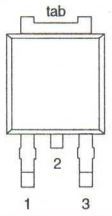
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT136S** (or BT136M)- | **500E** | **600E** | **800E** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

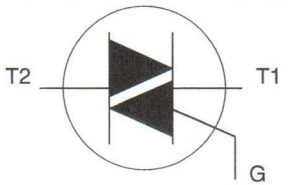
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | - | 2.5 | 10 | mA |
| | | T2+ G- | - | 4.0 | 10 | mA |
| | | T2- G- | - | 5.0 | 10 | mA |
| | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | 3.0 | 15 | mA |
| | | T2+ G- | - | 10 | 20 | mA |
| | | T2- G- | - | 2.5 | 15 | mA |
| | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

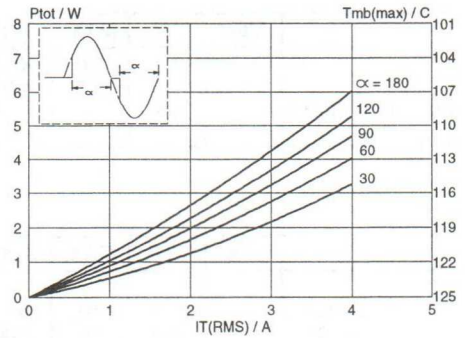



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

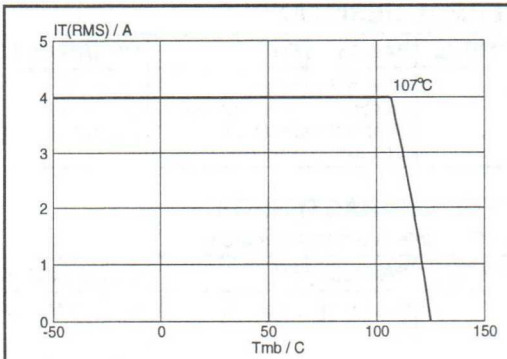



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

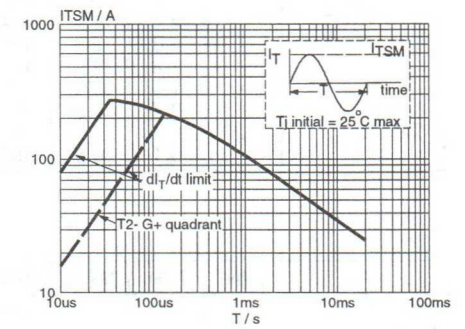



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

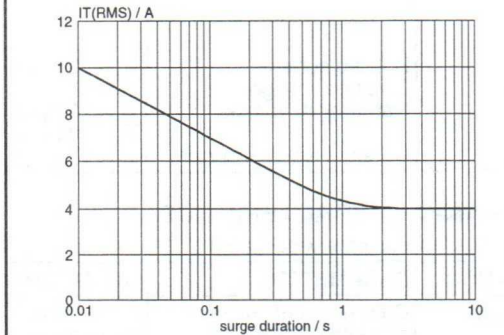



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

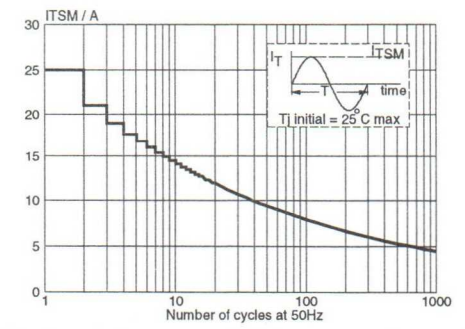



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

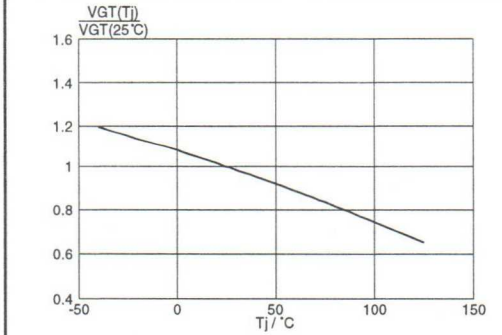



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

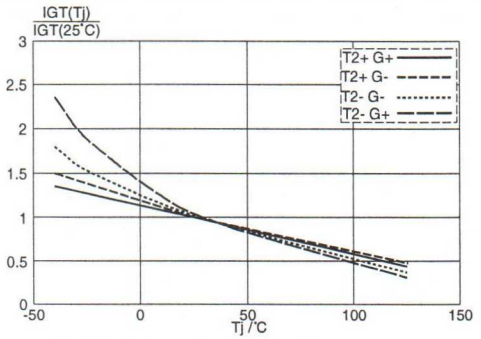



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

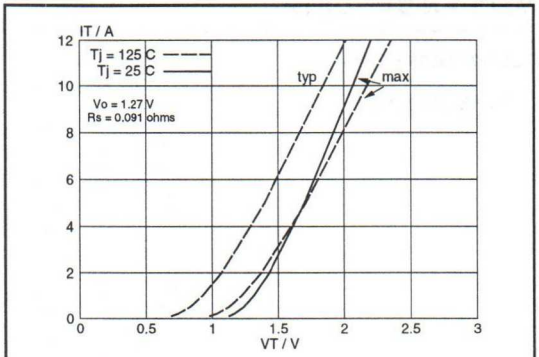



*Fig.10. Typical and maximum on-state characteristic.*

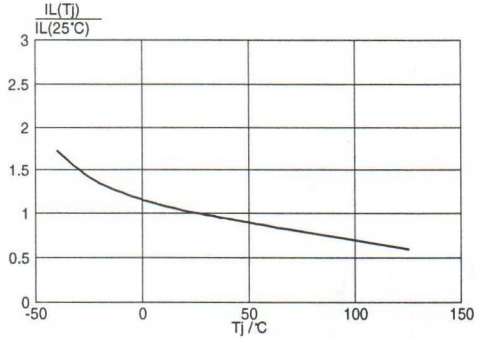



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

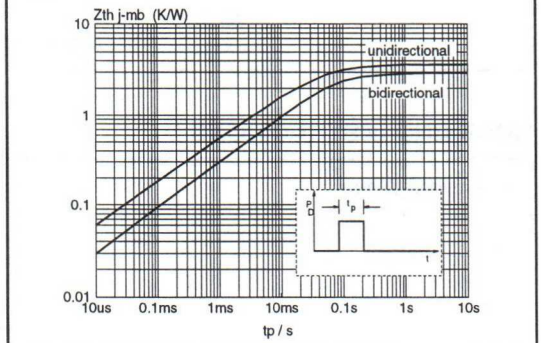



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

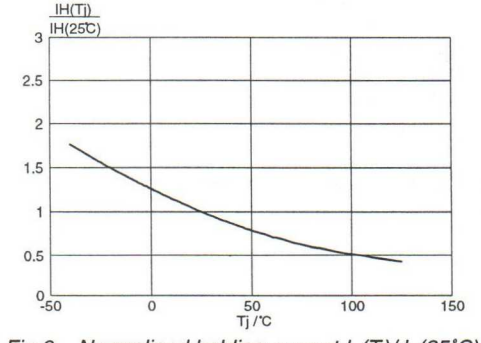



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

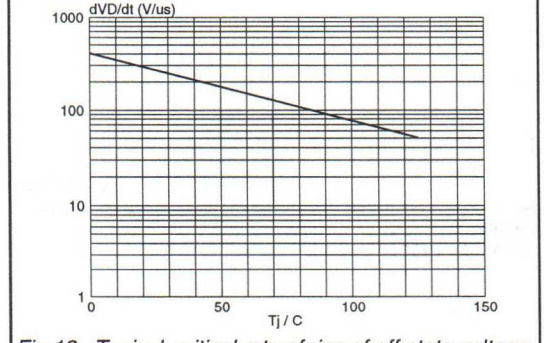



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

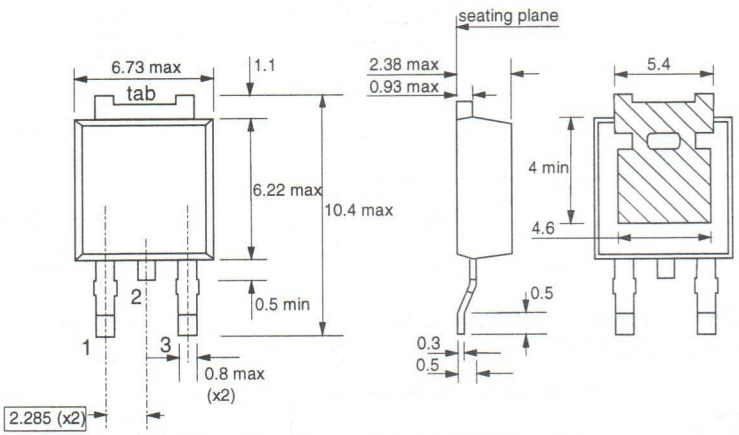



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

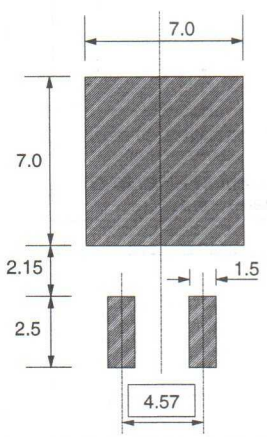



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

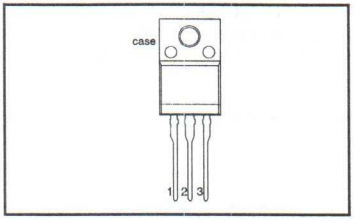
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT136X-** | **500** | **600** | **800** | |
| | **BT136X-** | **500F** | **600F** | **800F** | |
| | **BT136X-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

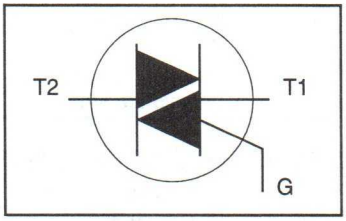
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 92$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 5.5 | K/W |
| | | without heatsink compound | - | - | 7.2 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136X- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 20 | 20 | 30 | mA |
| | | T2+ G- | - | 16 | 30 | 30 | 45 | mA |
| | | T2- G- | - | 5 | 20 | 20 | 30 | mA |
| | | T2- G+ | - | 7 | 30 | 30 | 45 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 15 | 15 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.70 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT136X- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 4 A; $dI_{com}/dt$ = 1.8 A/ms; gate open circuit | - | - | 10 | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

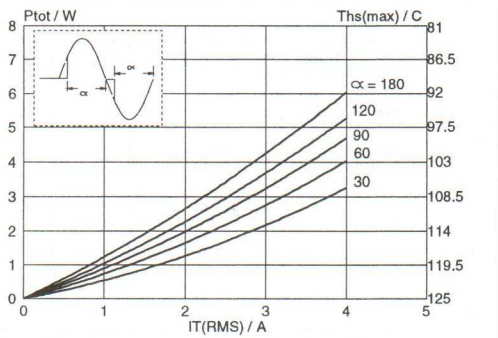



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

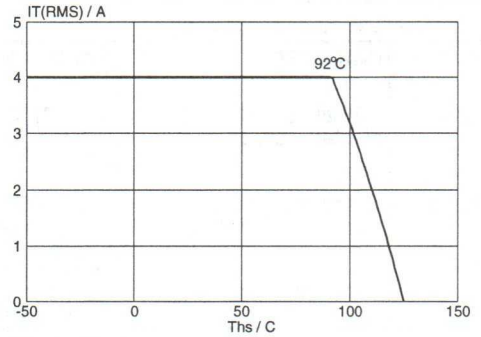



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

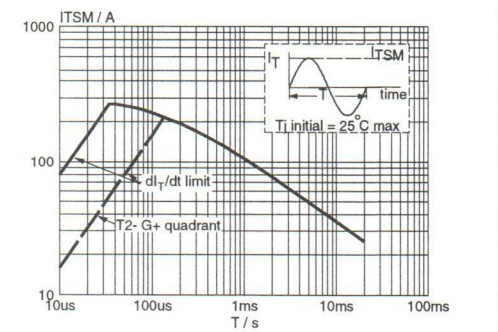



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

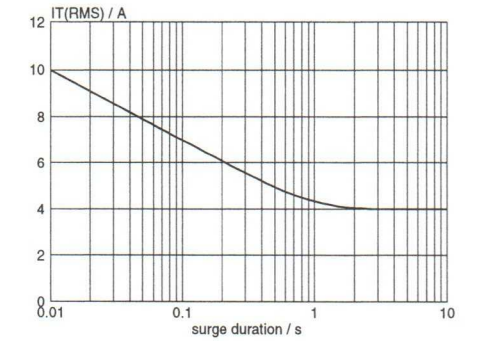



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92°C$.*

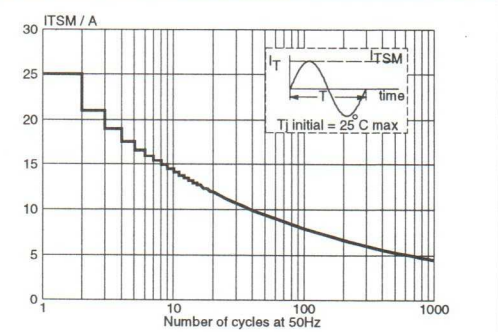



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

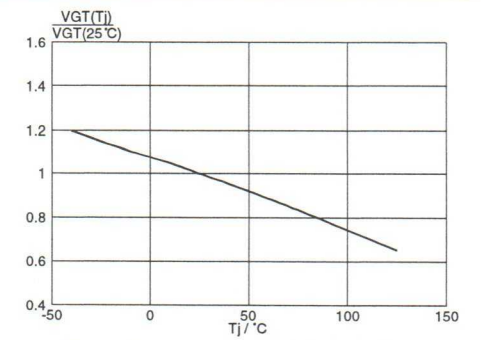



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

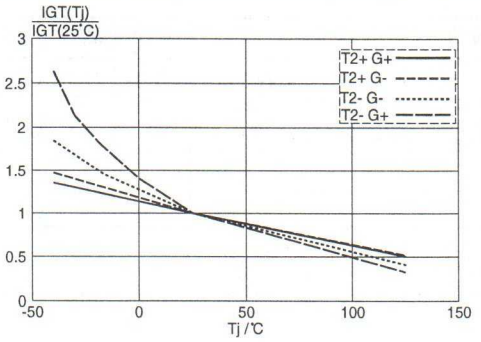



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

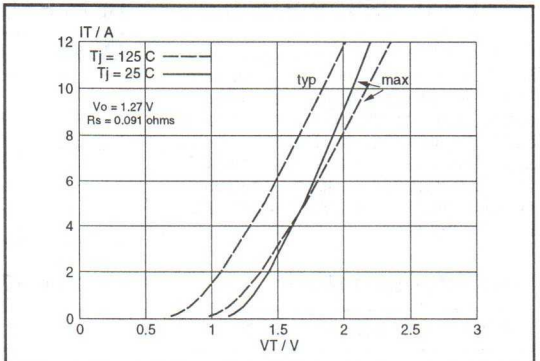



*Fig.10. Typical and maximum on-state characteristic.*

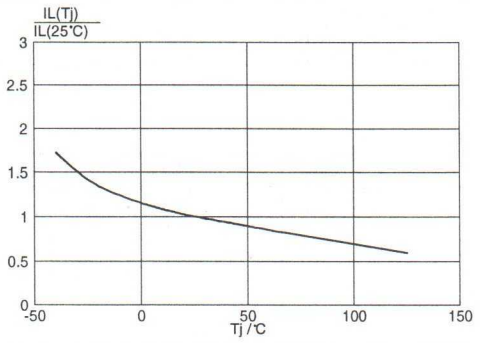



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

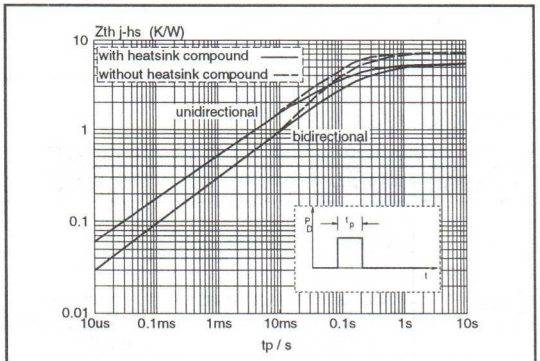



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

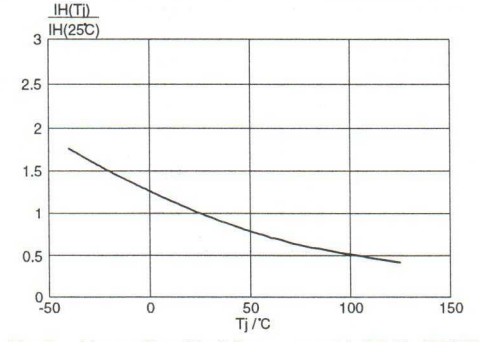



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

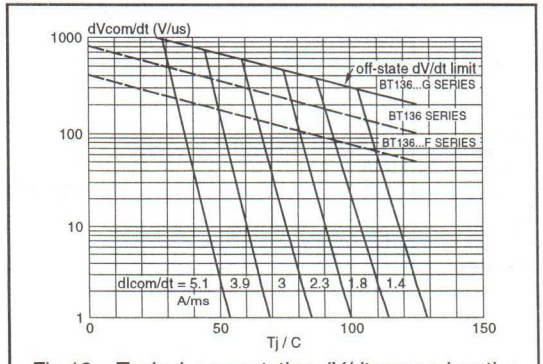



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs logic level

# BT136X series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

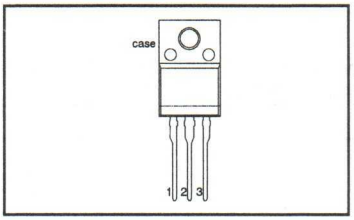
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT136X- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | A |

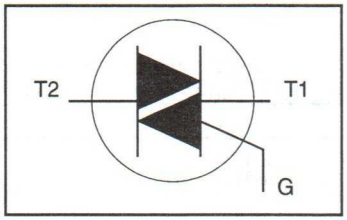
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | -500 | -600 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 92$ °C | - | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 25 | | A |
| | | t = 16.7 ms | - | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 5.5 | K/W |
| | | without heatsink compound | - | - | 7.2 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.0 | 5 | mA |
| | | | T2+ G- | - | 2.5 | 5 | mA |
| | | | T2- G- | - | 2.5 | 5 | mA |
| | | | T2- G+ | - | 5.0 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 10 | mA |
| | | | T2+ G- | - | 4.5 | 15 | mA |
| | | | T2- G- | - | 1.2 | 10 | mA |
| | | | T2- G+ | - | 2.2 | 15 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.2 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

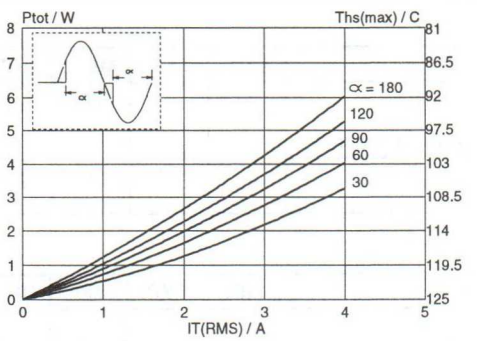



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

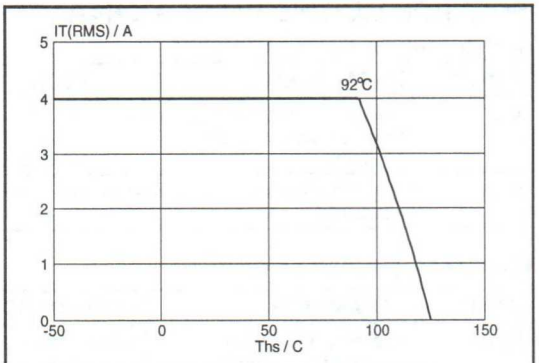



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

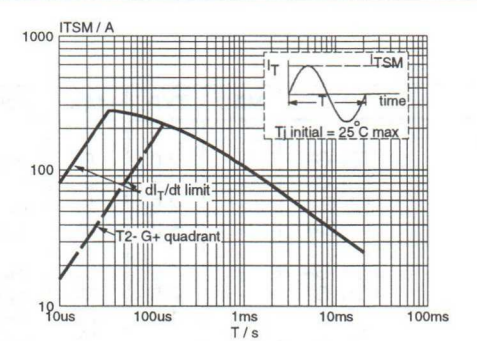



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

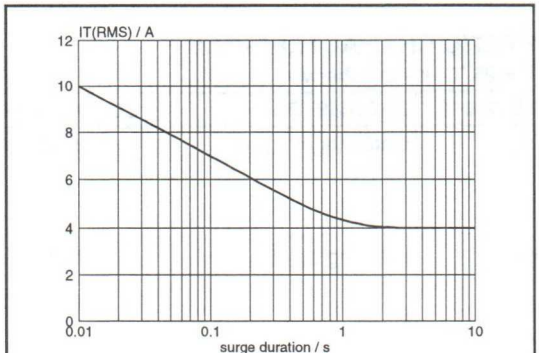



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92°C$.*

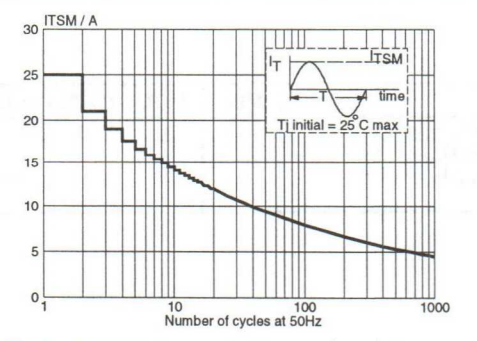



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

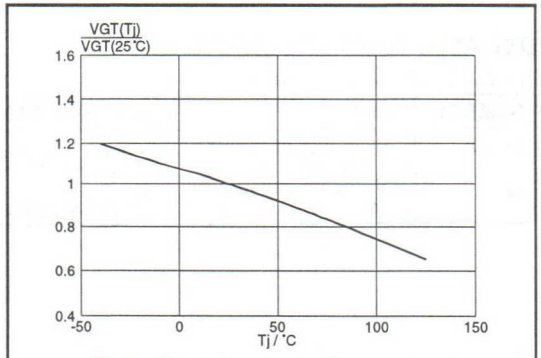



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

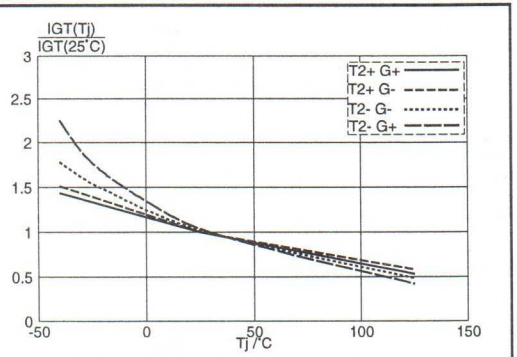



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

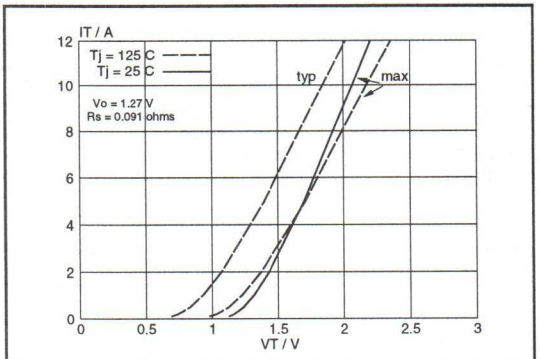



*Fig.10. Typical and maximum on-state characteristic.*

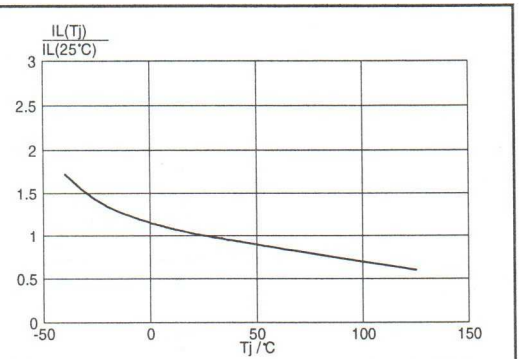



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

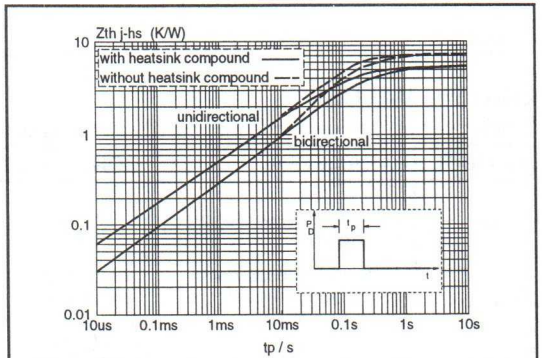



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

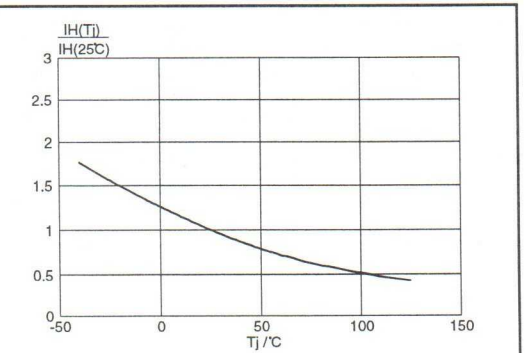



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

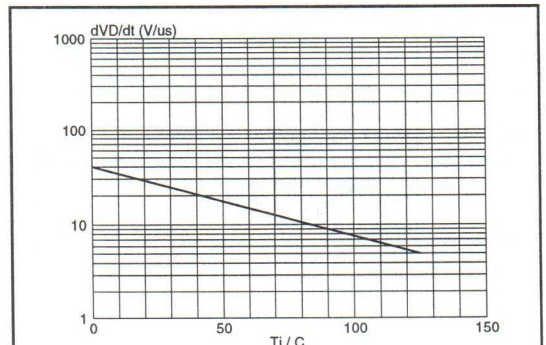



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs sensitive gate

# BT136X series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

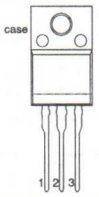
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT136X- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

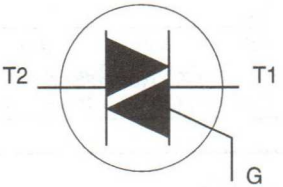
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 92$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 6 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 5.5 | K/W |
| | | without heatsink compound | - | - | 7.2 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 15 | mA |
| | | | T2+ G- | - | 10 | 20 | mA |
| | | | T2- G- | - | 2.5 | 15 | mA |
| | | | T2- G+ | - | 4.0 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.2 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | | - | 1.4 | 1.70 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 6 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

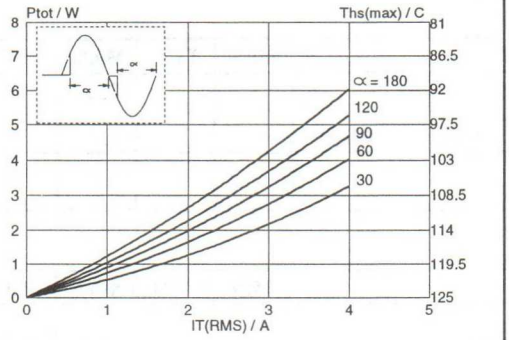



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

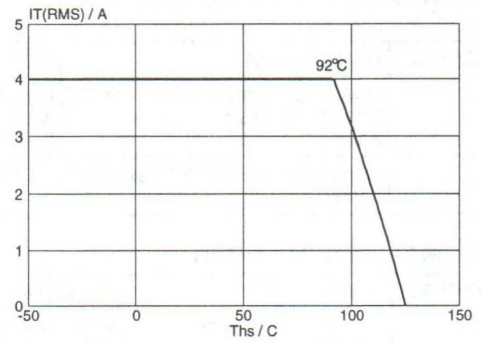



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

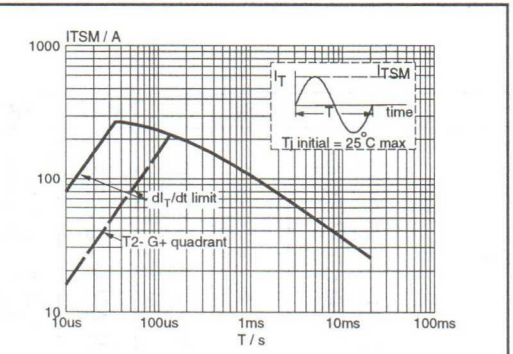



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

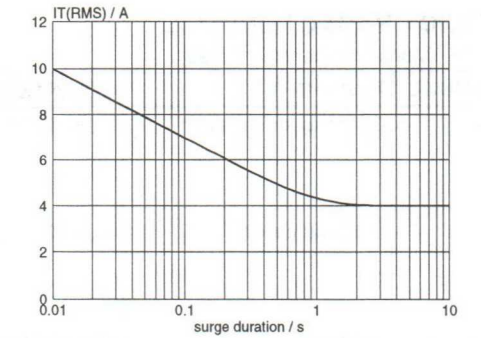



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92°C$.*

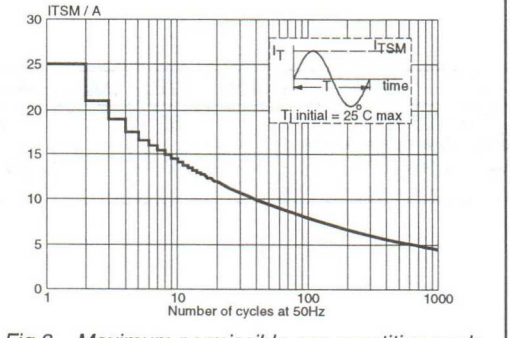



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

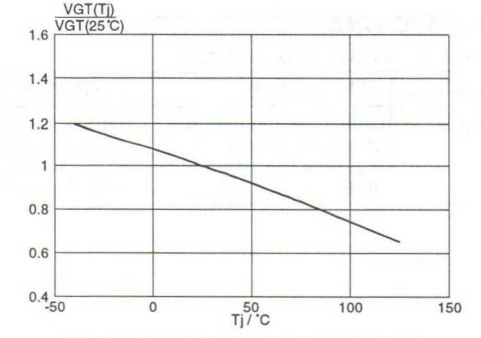



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

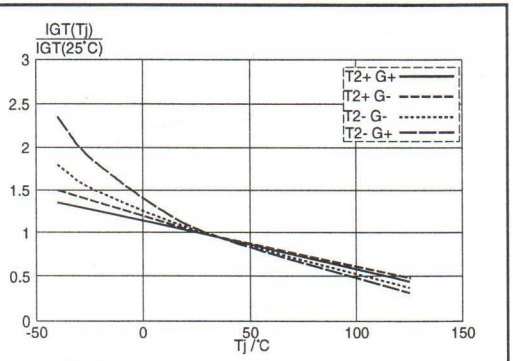



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

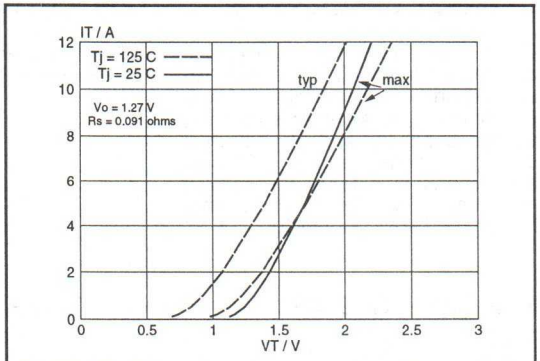



*Fig.10. Typical and maximum on-state characteristic.*

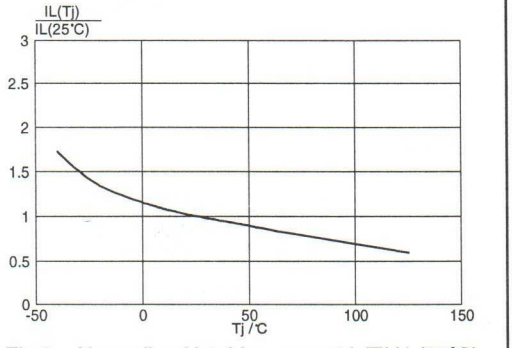



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

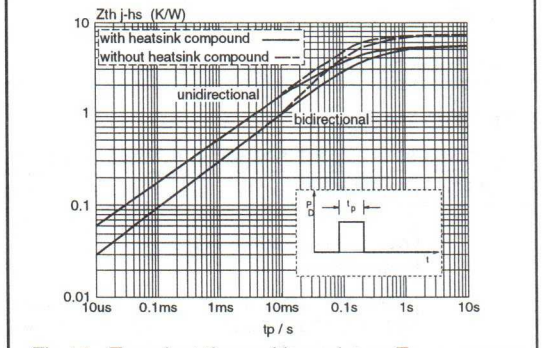



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

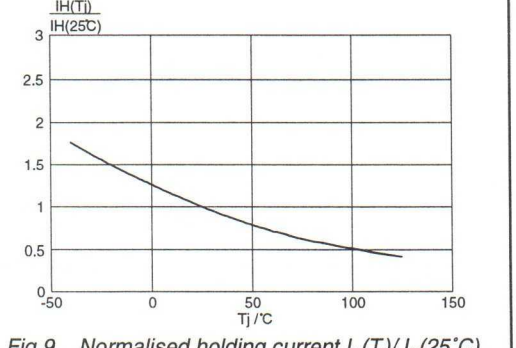



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

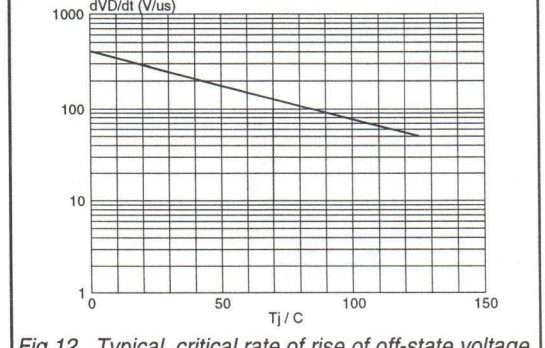



*Fig.12. Typical, critical rate of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

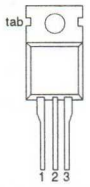
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT137- | 500 | 600 | 800 | |
| | BT137- | 500F | 600F | 800F | |
| | BT137- | 500G | 600G | 800G | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

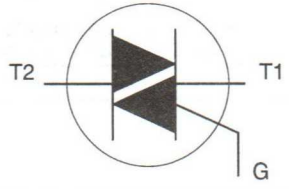
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 30 | 30 | 45 | mA |
| | | T2+ G- | - | 16 | 45 | 45 | 60 | mA |
| | | T2- G- | - | 5 | 30 | 30 | 45 | mA |
| | | T2- G+ | - | 7 | 45 | 45 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 20 | 20 | 40 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 8 A; $dI_{com}/dt$ = 3.6 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

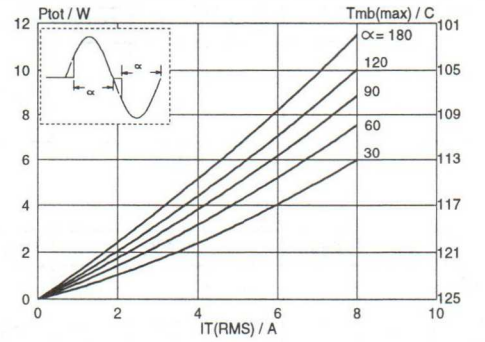



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

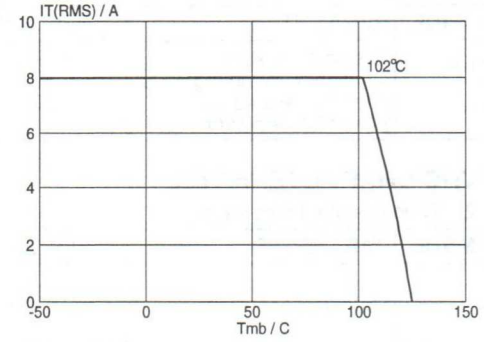



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

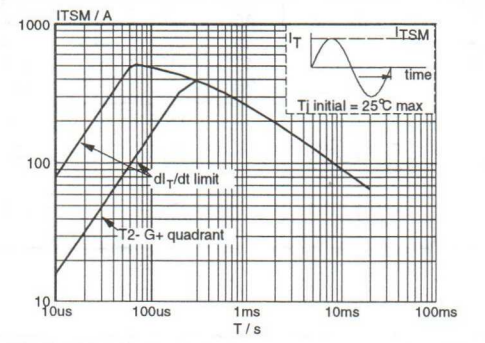



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

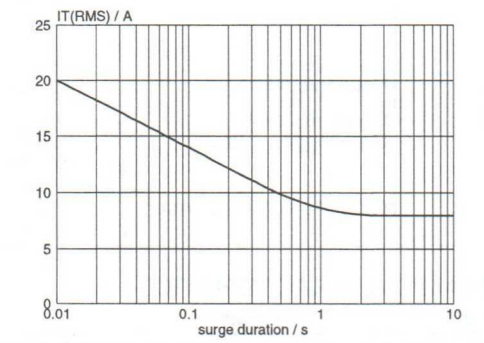



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

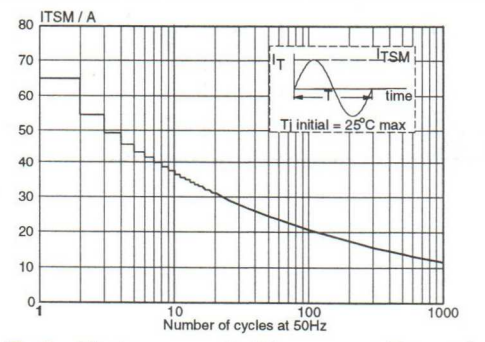



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

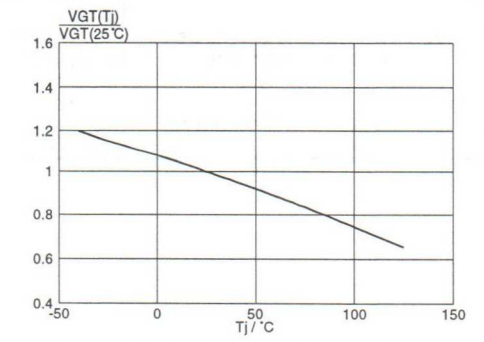



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

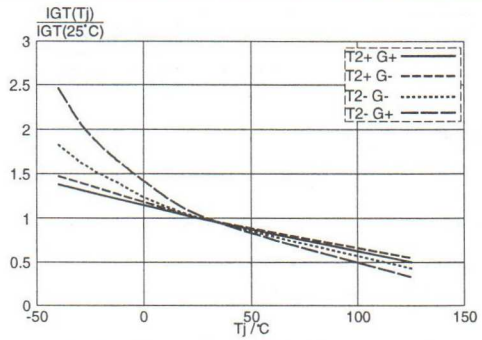



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

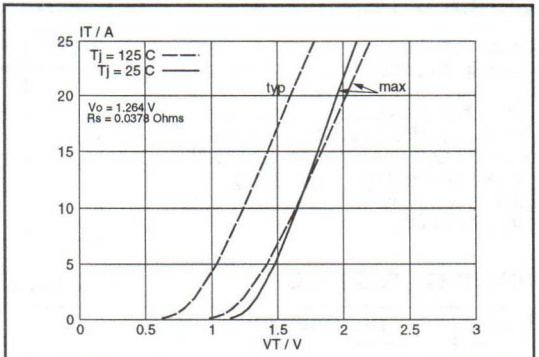



*Fig.10. Typical and maximum on-state characteristic.*

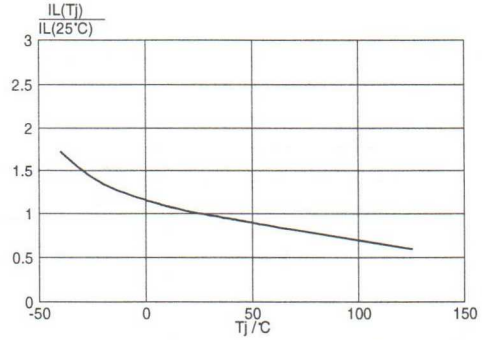



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

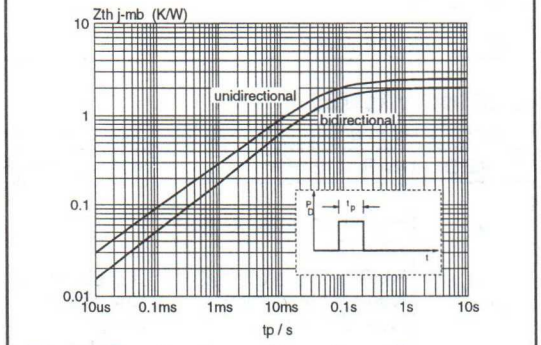



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

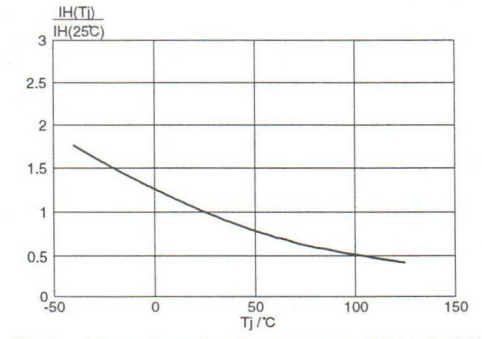



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

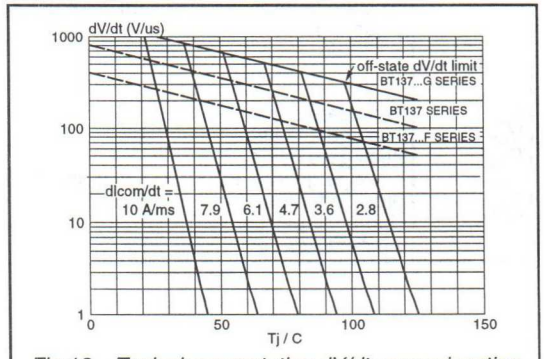



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs logic level

# BT137 series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

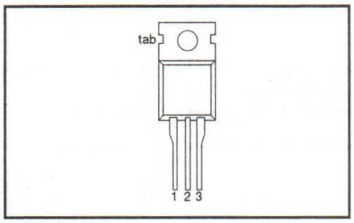
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | BT137- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | A |

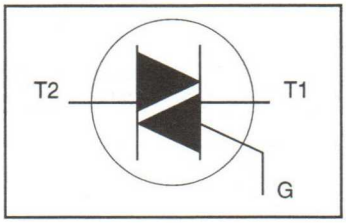
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | UNIT |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 65 | | A |
| | | t = 16.7 ms | - | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 5 | mA |
| | | | T2+ G- | - | 3.5 | 5 | mA |
| | | | T2- G- | - | 3.5 | 5 | mA |
| | | | T2- G+ | - | 6.5 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 15 | mA |
| | | | T2+ G- | - | 8.5 | 20 | mA |
| | | | T2- G- | - | 1.2 | 15 | mA |
| | | | T2- G+ | - | 2.5 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.5 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

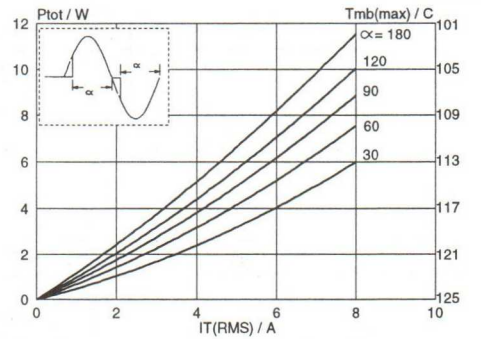



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

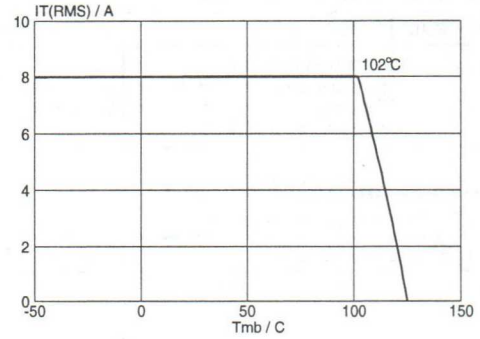



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

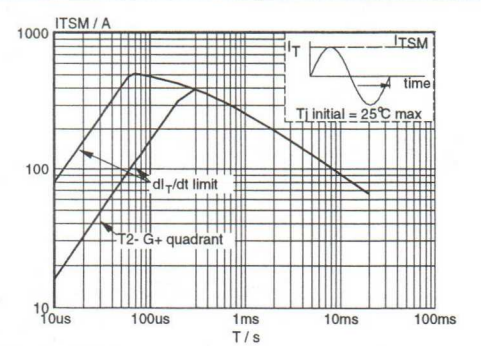



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

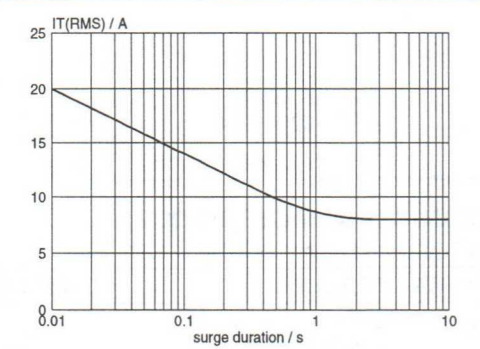



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102^{\circ}C$.*

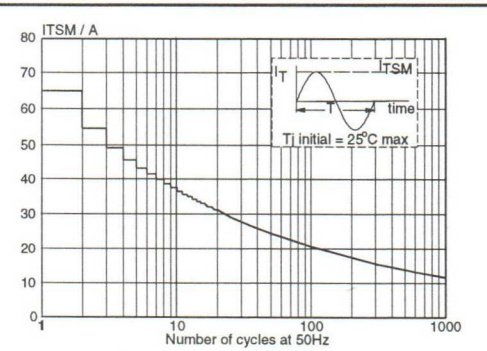



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

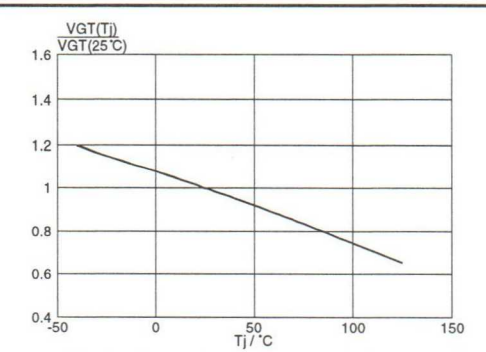



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

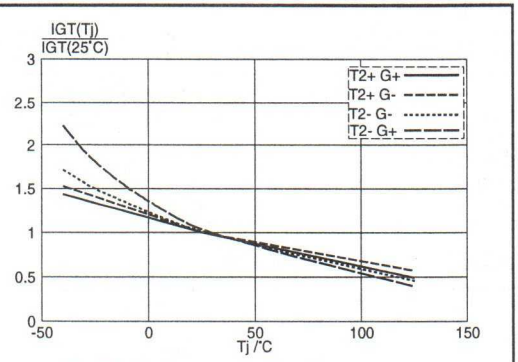



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

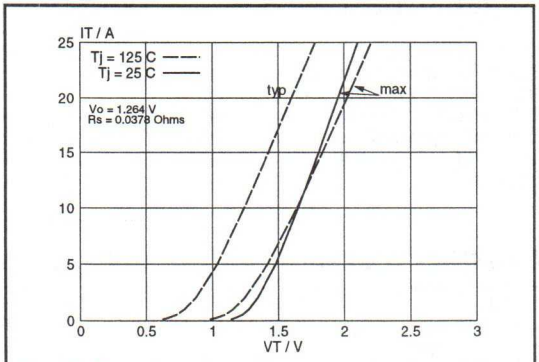



*Fig.10. Typical and maximum on-state characteristic.*

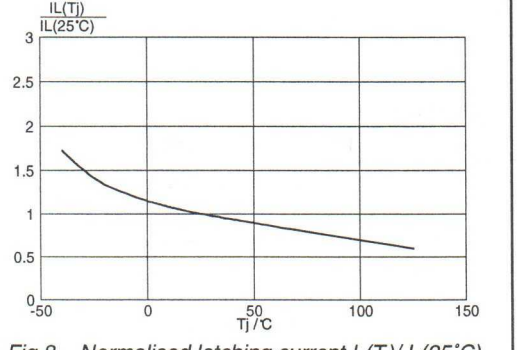



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

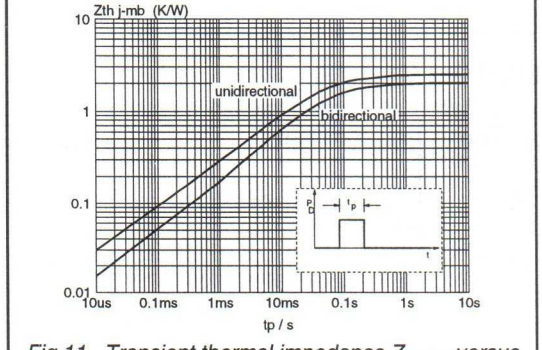



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

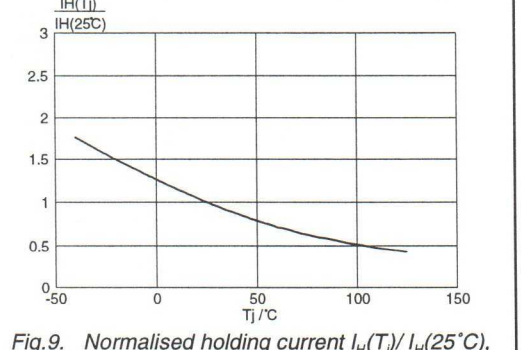



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

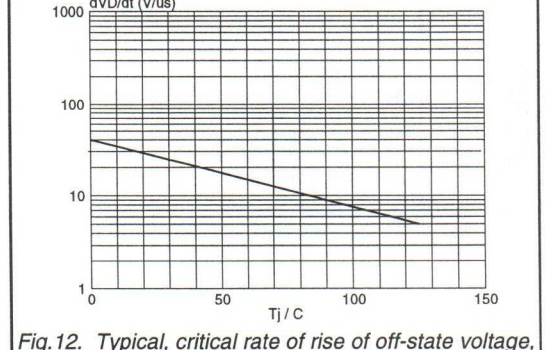



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs sensitive gate

# BT137 series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

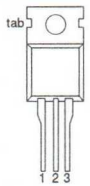
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT137- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

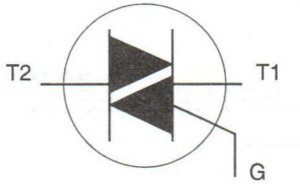
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 25 | mA |
| | | | T2+ G- | - | 14 | 35 | mA |
| | | | T2- G- | - | 3.0 | 25 | mA |
| | | | T2- G+ | - | 4.0 | 35 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.5 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

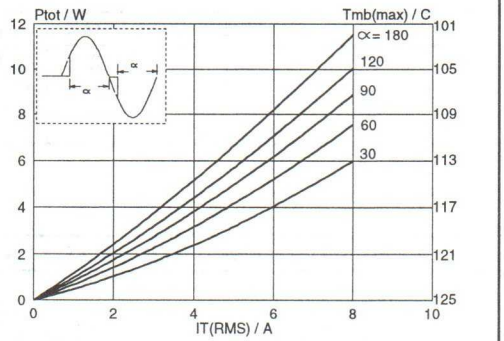



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

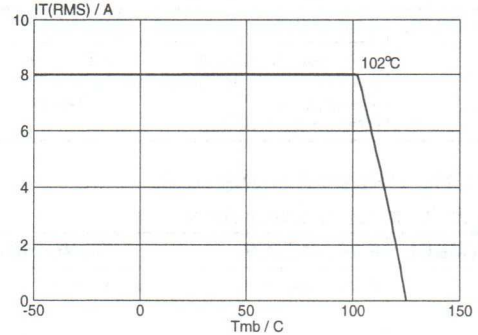



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

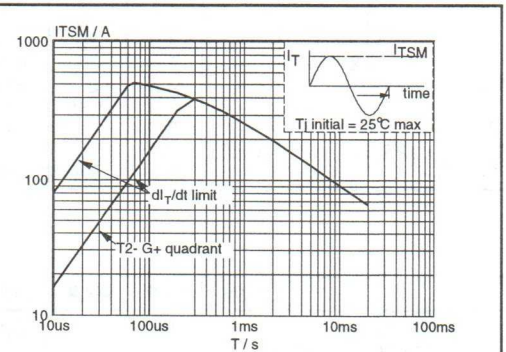



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

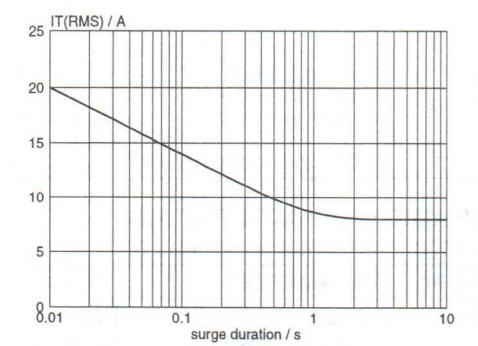



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

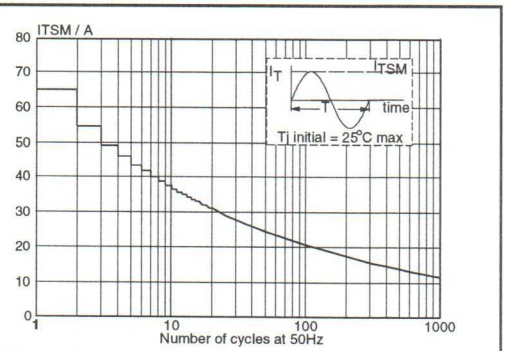



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

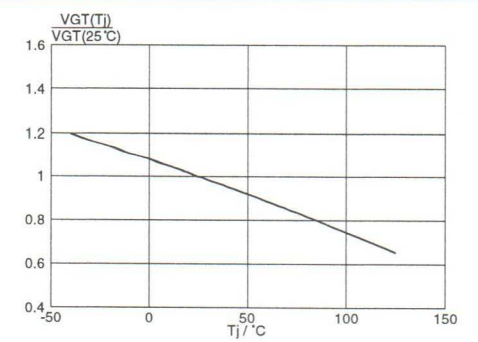



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

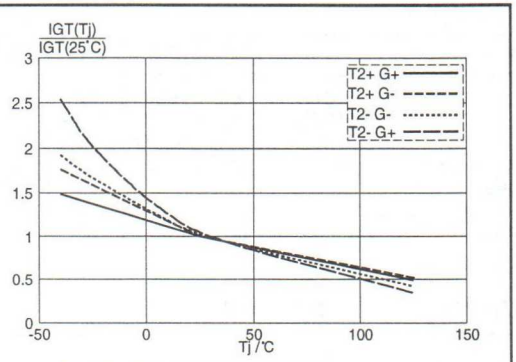



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

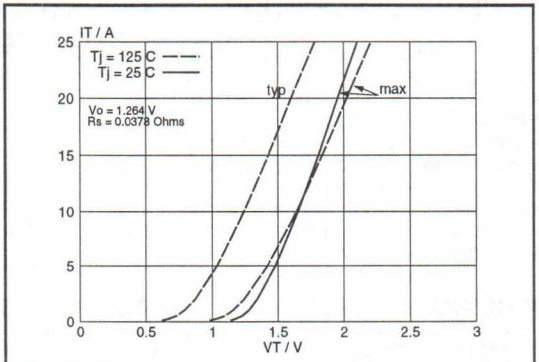



*Fig.10. Typical and maximum on-state characteristic.*

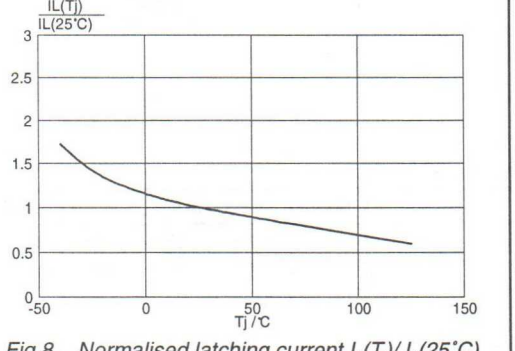



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

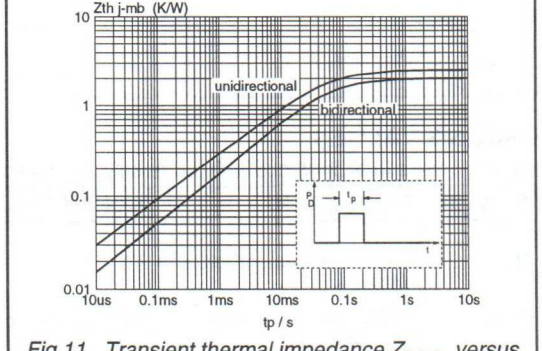



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

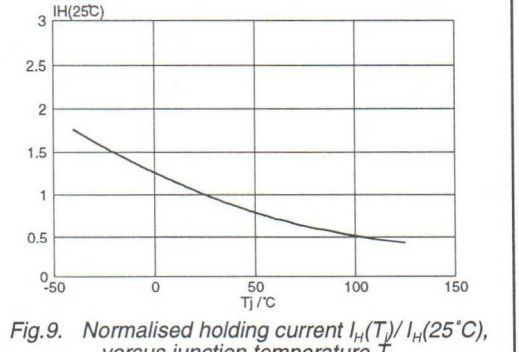



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

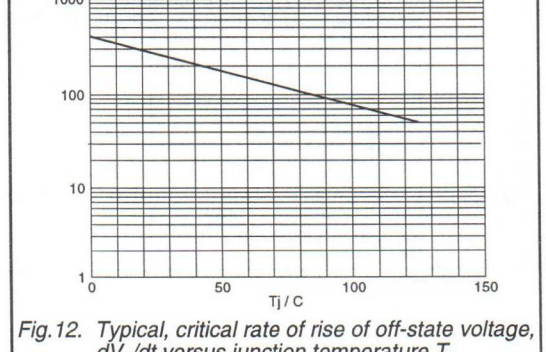



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

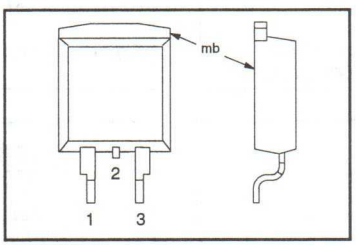
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT137B-** | **500** | **600** | **800** | |
| | **BT137B-** | **500F** | **600F** | **800F** | |
| | **BT137B-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

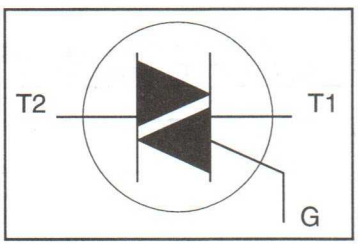
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137B- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 30 | 30 | 45 | mA |
| | | T2+ G- | - | 16 | 45 | 45 | 60 | mA |
| | | T2- G- | - | 5 | 30 | 30 | 45 | mA |
| | | T2- G+ | - | 7 | 45 | 45 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 20 | 20 | 40 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137B- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 8 A; $dI_{com}/dt$ = 3.6 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

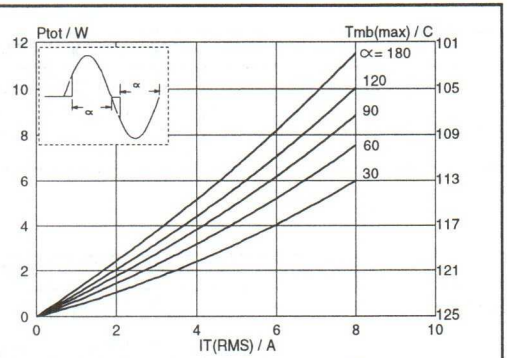



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

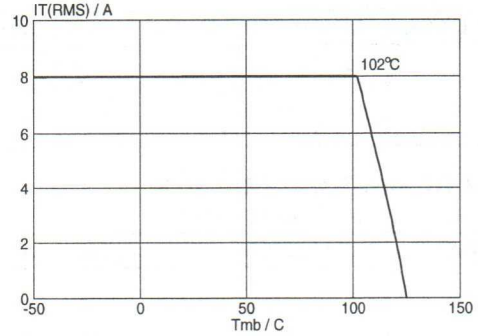



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

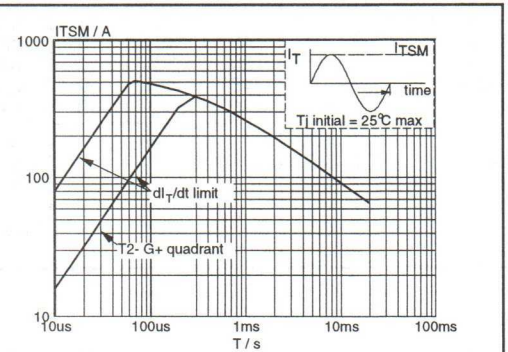



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

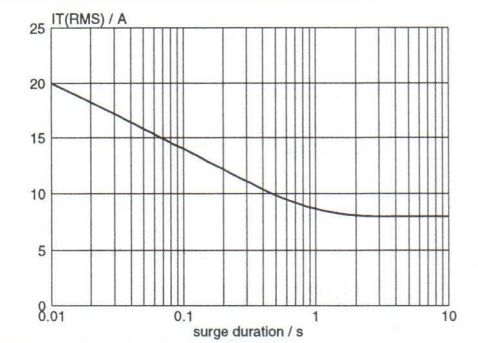



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

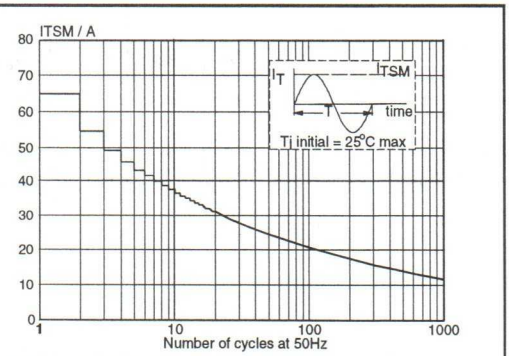



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

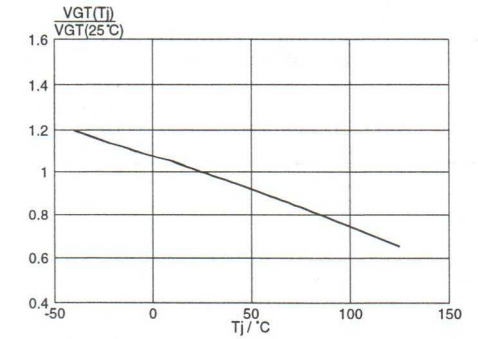



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

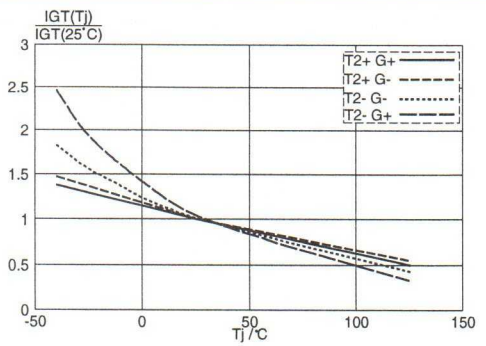



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

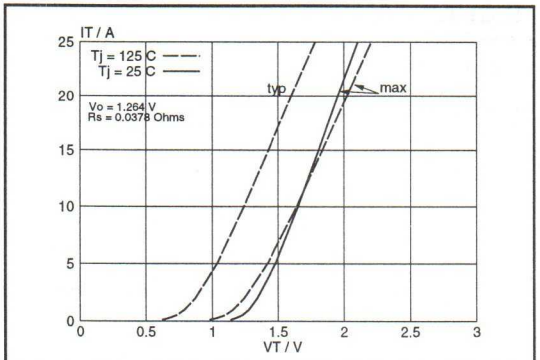



*Fig.10. Typical and maximum on-state characteristic.*

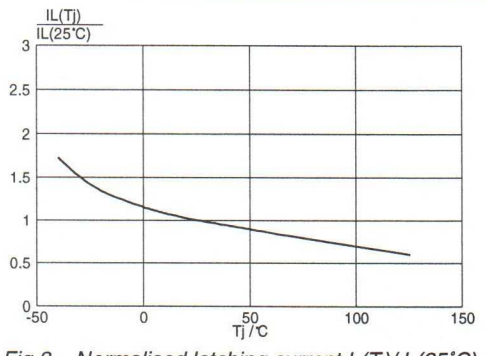



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

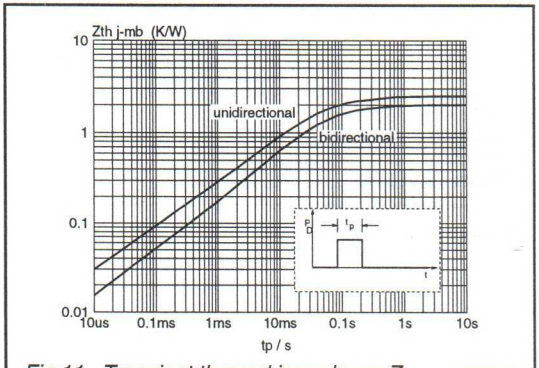



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

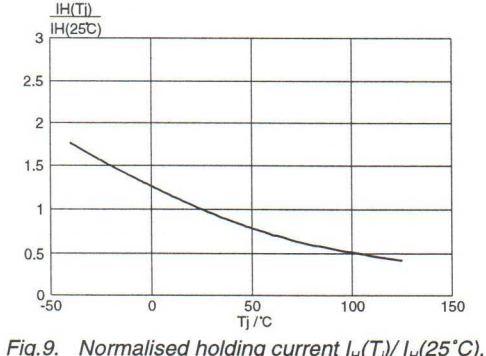



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

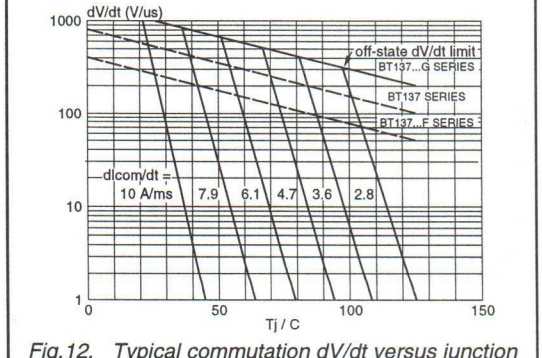



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

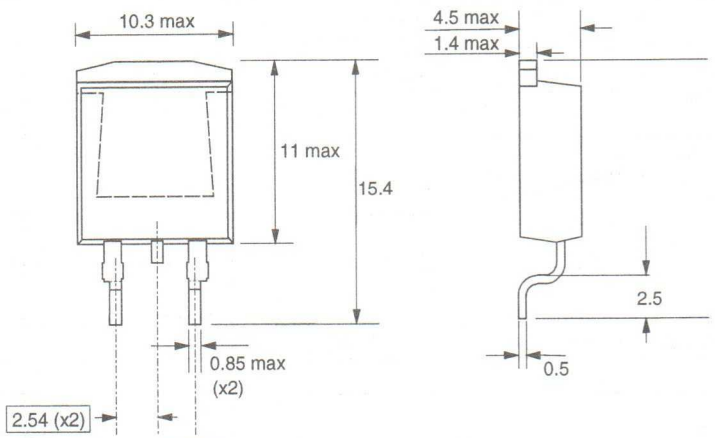



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

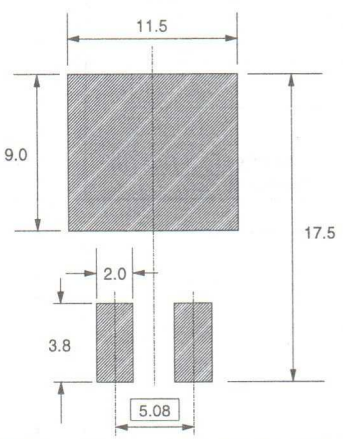



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs logic level

# BT137B series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

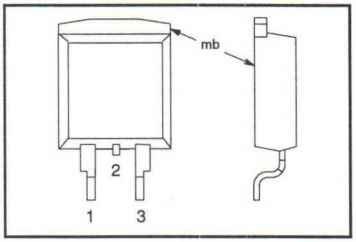
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | **BT137B-** | **500D** | **600D** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | A |

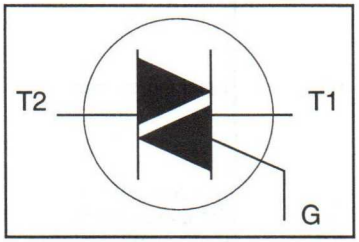
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | UNIT |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 65 | | A |
| | | t = 16.7 ms | - | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 5 | mA |
| | | | T2+ G- | - | 3.5 | 5 | mA |
| | | | T2- G- | - | 3.5 | 5 | mA |
| | | | T2- G+ | - | 6.5 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 15 | mA |
| | | | T2+ G- | - | 8.5 | 20 | mA |
| | | | T2- G- | - | 1.2 | 15 | mA |
| | | | T2- G+ | - | 2.5 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.5 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

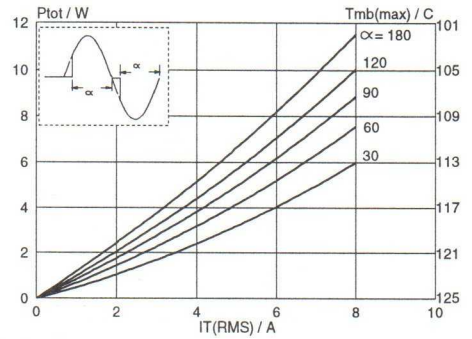



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

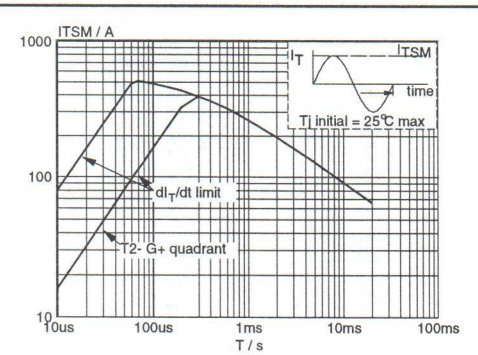



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

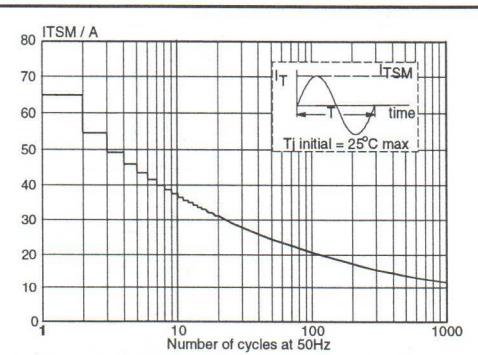



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

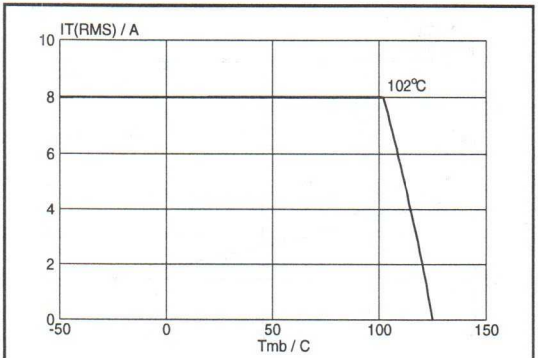



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

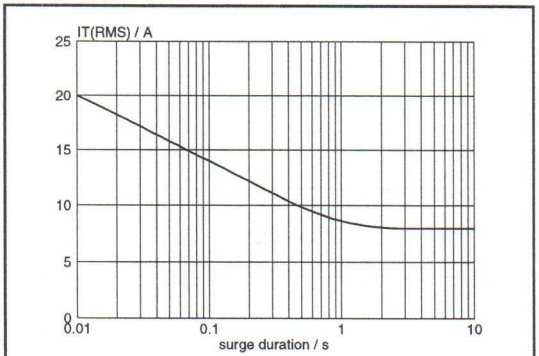



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

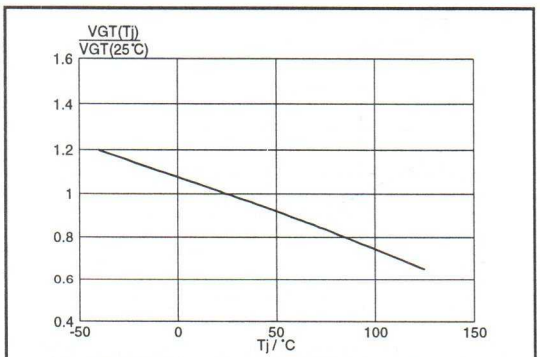



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

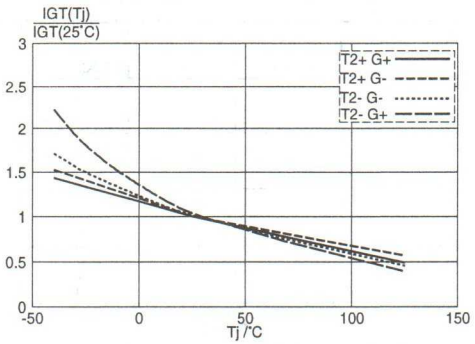



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

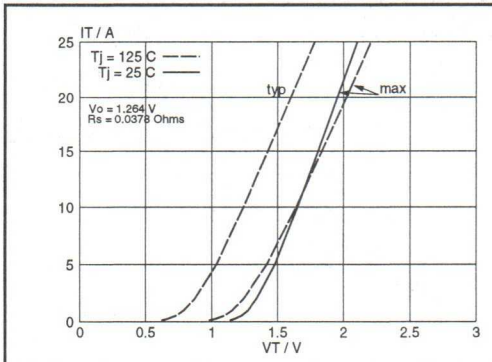



*Fig.10. Typical and maximum on-state characteristic.*

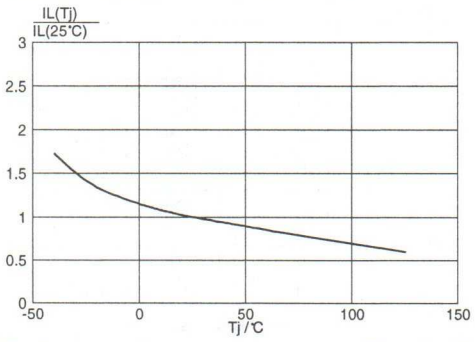



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

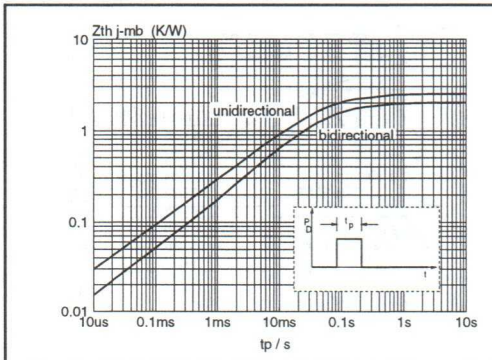



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

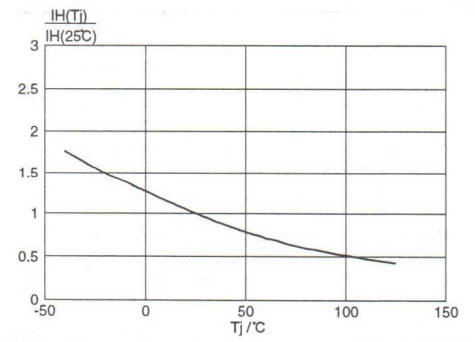



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

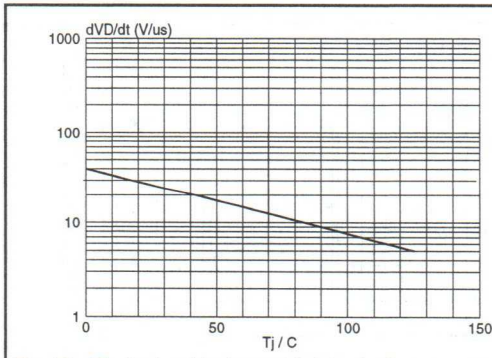



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

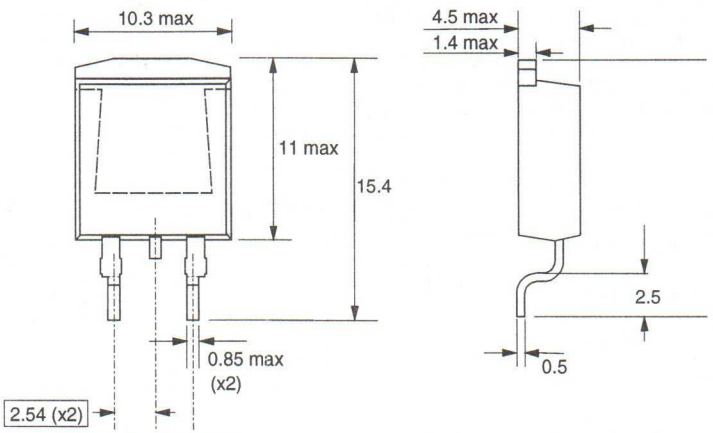



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

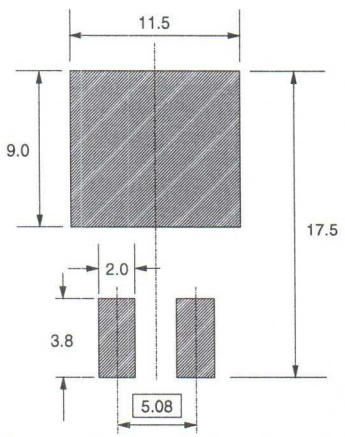



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT137B series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

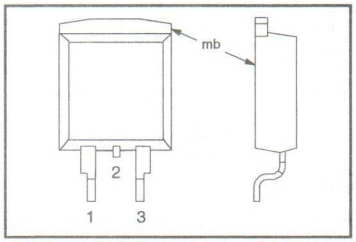
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT137B- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

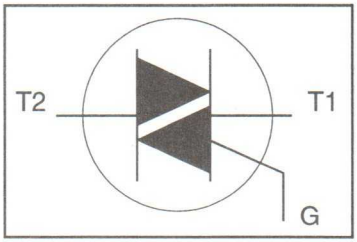
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.0 | 25 | mA |
| | | | T2+ G- | - | 14 | 35 | mA |
| | | | T2- G- | - | 3.0 | 25 | mA |
| | | | T2- G+ | - | 4.0 | 35 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 2.5 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

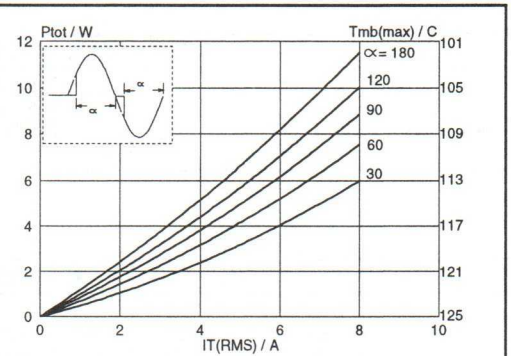



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

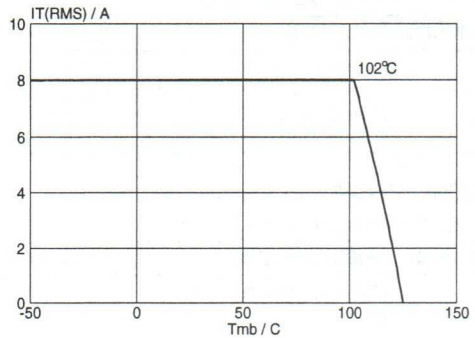



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

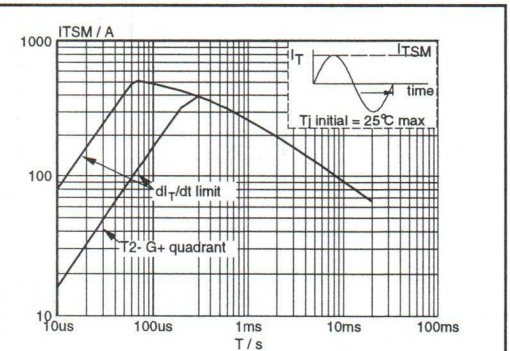



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

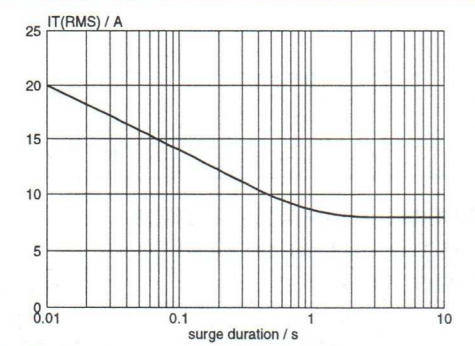



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

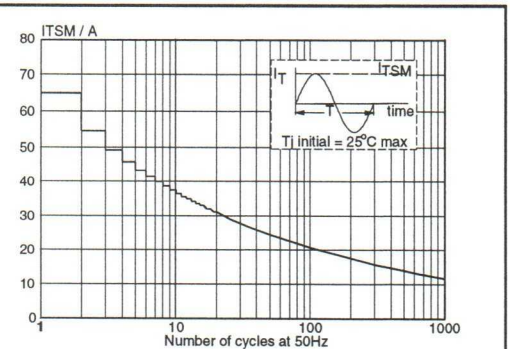



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

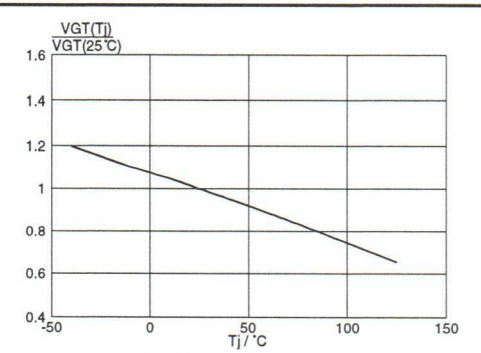



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

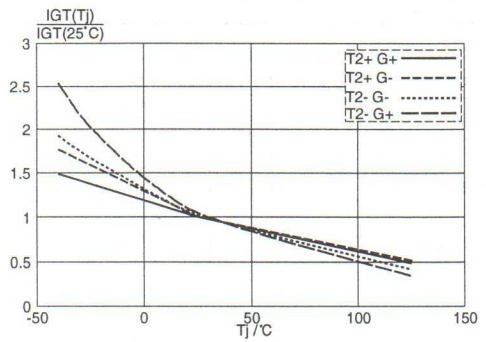



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

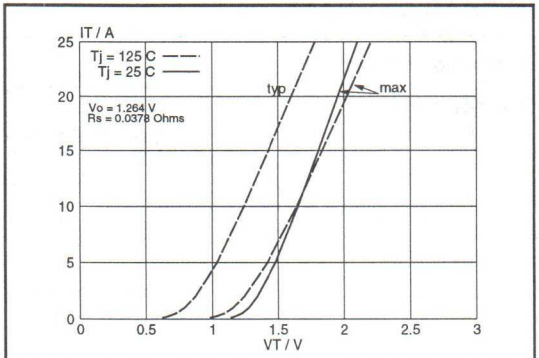



*Fig.10. Typical and maximum on-state characteristic.*

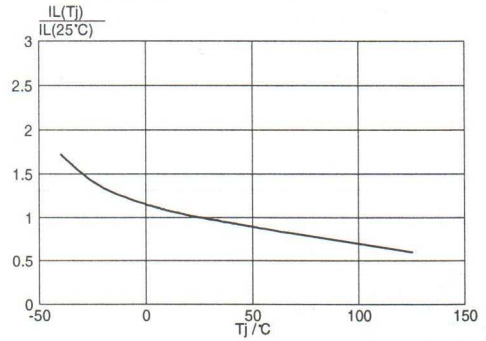



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

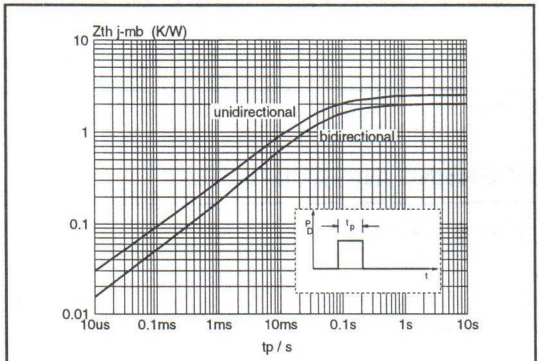



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

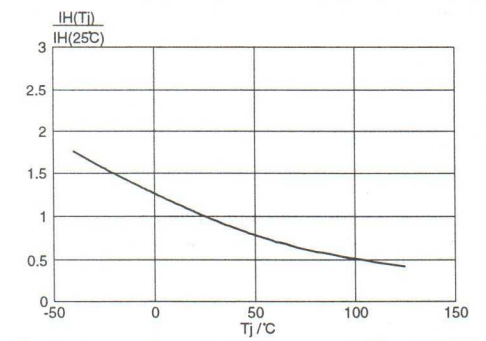



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

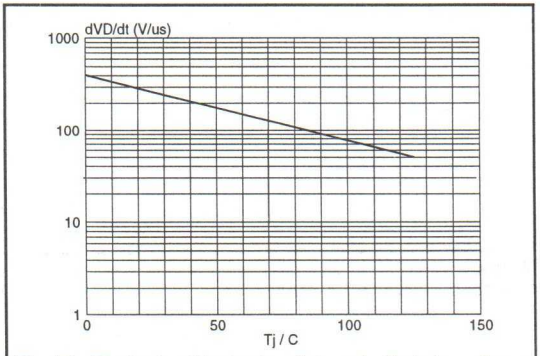



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

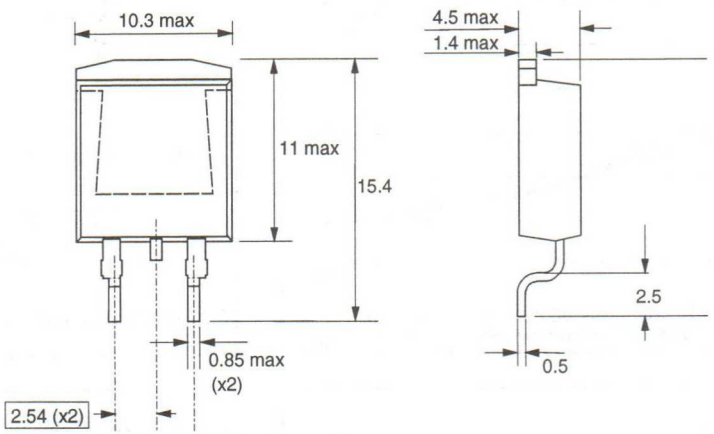



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

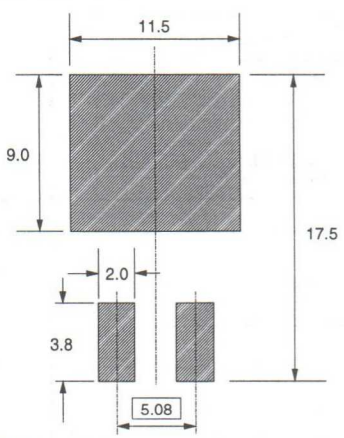



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

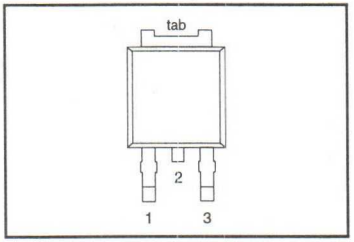
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT137S** (or BT137M)- | **500** | **600** | **800** | |
| | **BT137S** (or BT137M)- | **500F** | **600F** | **800F** | |
| | **BT137S** (or BT137M)- | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

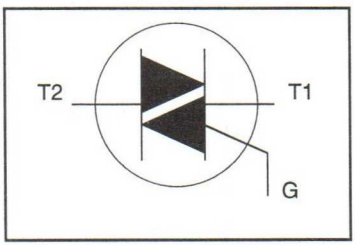
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BT137S-**(or BT137M) | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 30 | 30 | 45 | mA |
| | | T2+ G- | - | 16 | 45 | 45 | 60 | mA |
| | | T2- G- | - | 5 | 30 | 30 | 45 | mA |
| | | T2- G+ | - | 7 | 45 | 45 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 20 | 20 | 40 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BT137S-**(or BT137M) | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 8 A; $dI_{com}/dt$ = 3.6 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

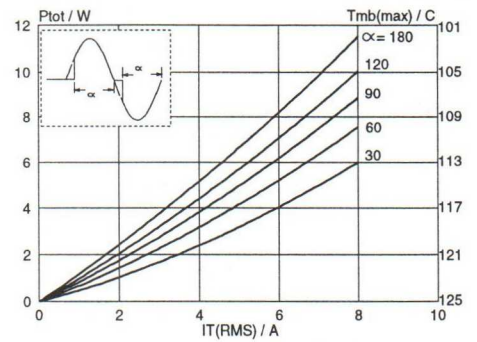



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

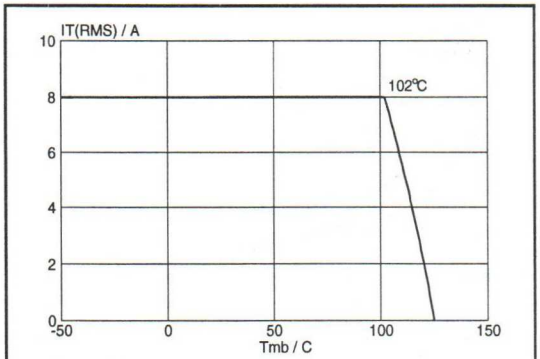



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

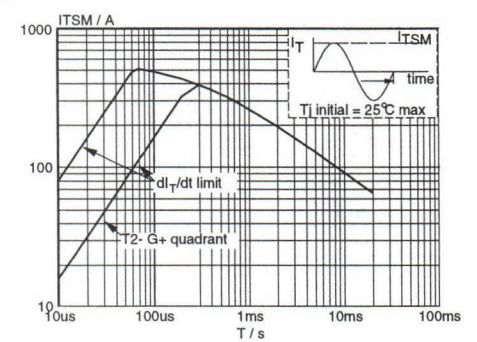



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

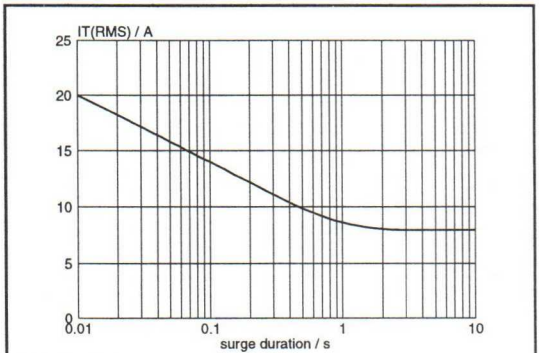



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

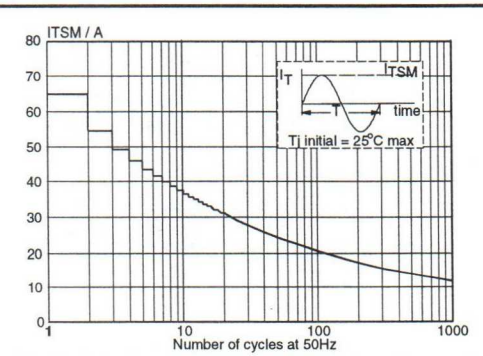



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

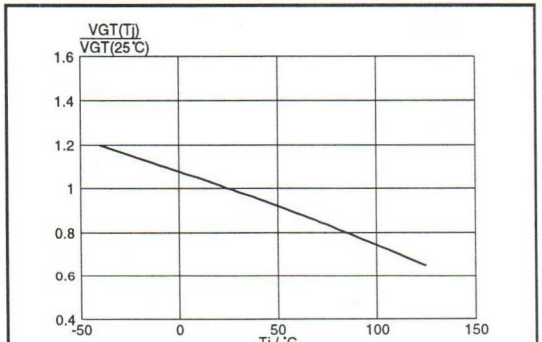



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

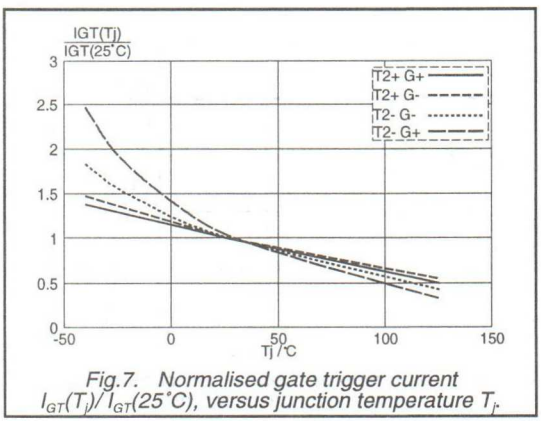



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

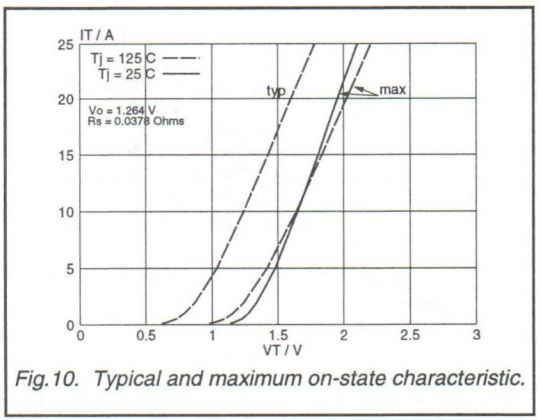



*Fig.10. Typical and maximum on-state characteristic.*

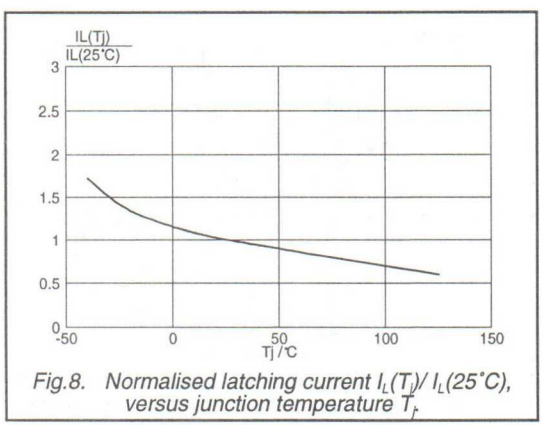



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

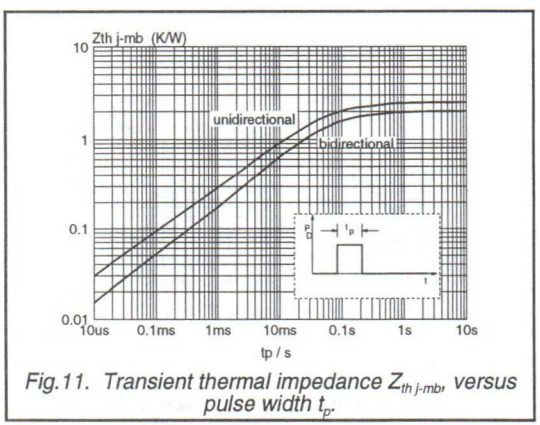



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

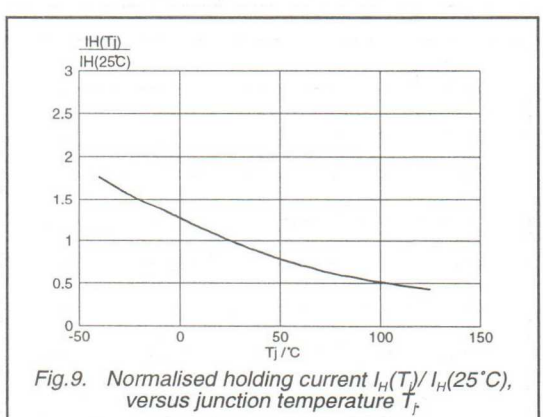



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

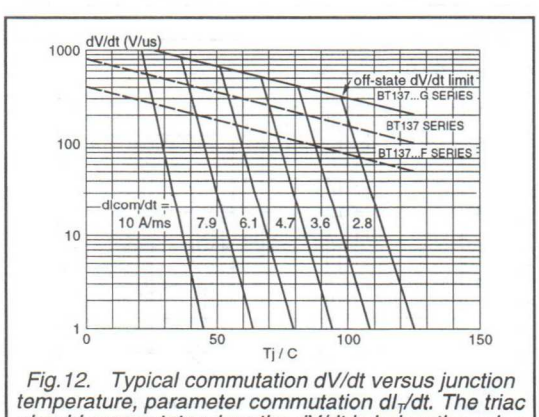



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

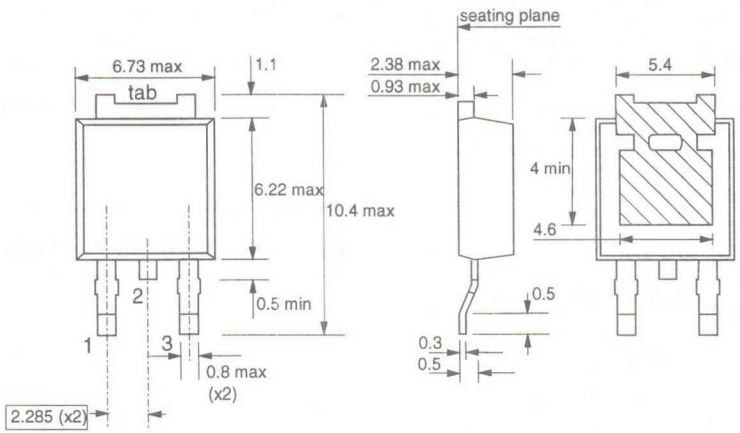



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

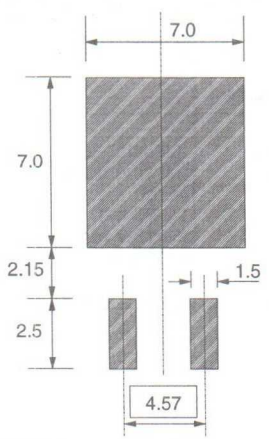



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

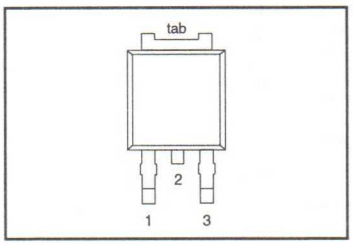
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | **BT137S** (or BT137M)- | **500D** | **600D** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | A |

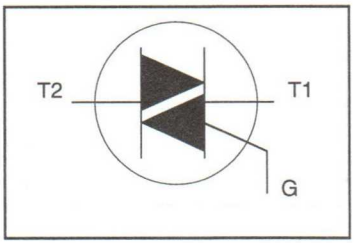
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 65 | | A |
| | | t = 16.7 ms | - | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | - | 2.5 | 5 | mA |
| | | T2+ G- | - | 3.5 | 5 | mA |
| | | T2- G- | - | 3.5 | 5 | mA |
| | | T2- G+ | - | 6.5 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | 1.6 | 15 | mA |
| | | T2+ G- | - | 8.5 | 20 | mA |
| | | T2- G- | - | 1.2 | 15 | mA |
| | | T2- G+ | - | 2.5 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 1.5 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

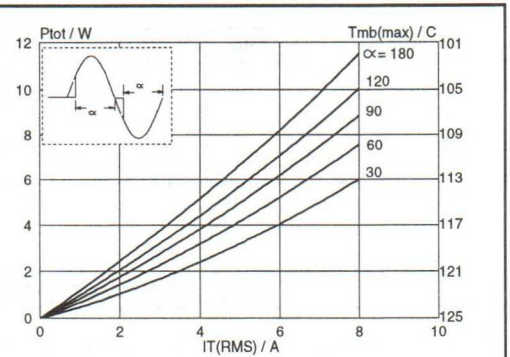



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

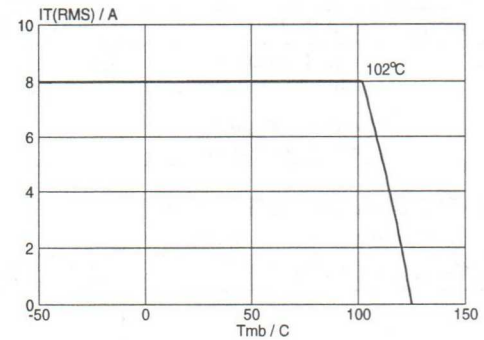



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

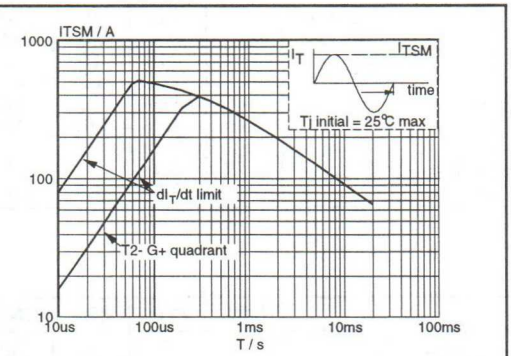



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

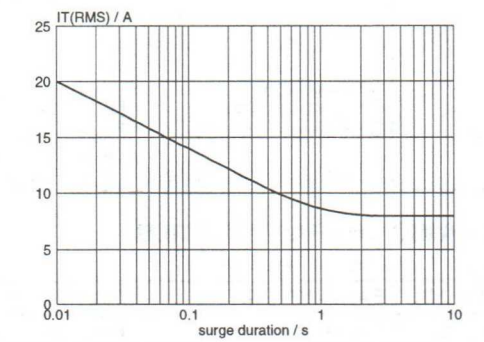



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

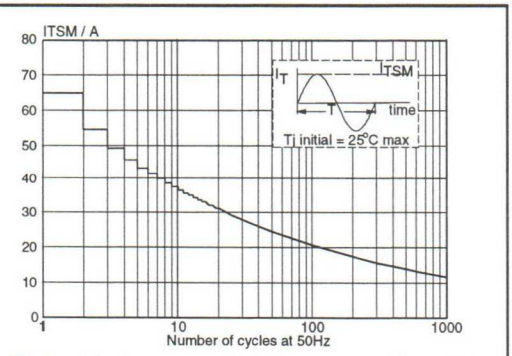



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

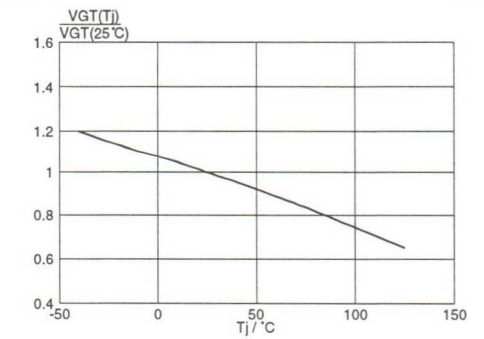



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

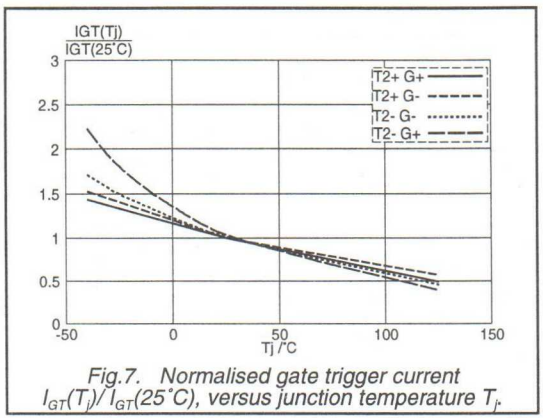



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

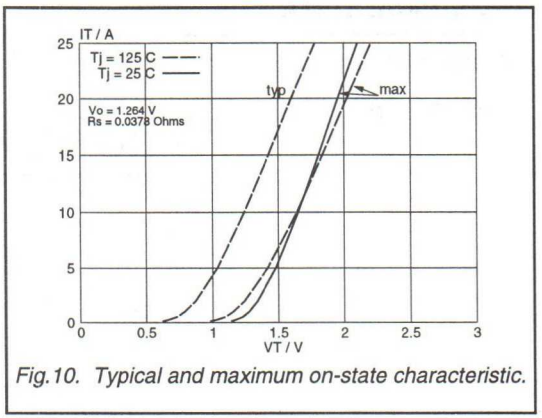



*Fig.10. Typical and maximum on-state characteristic.*

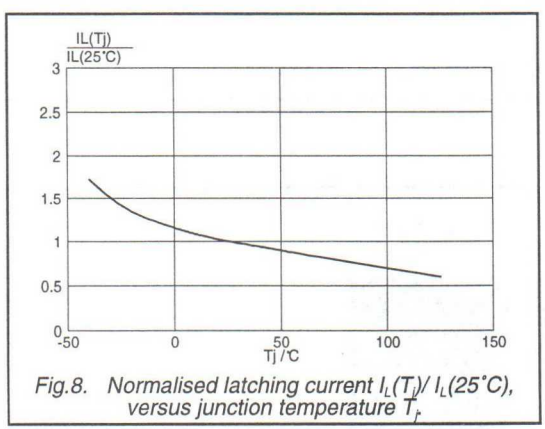



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

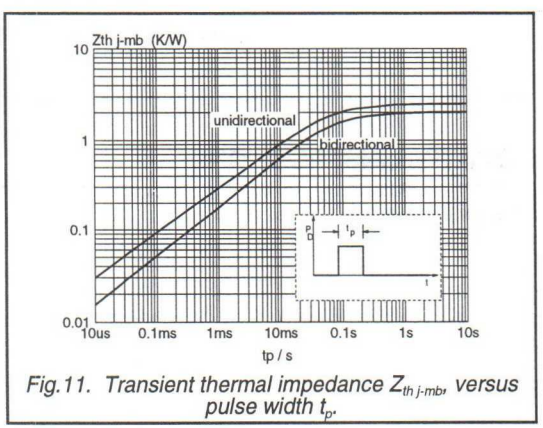



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

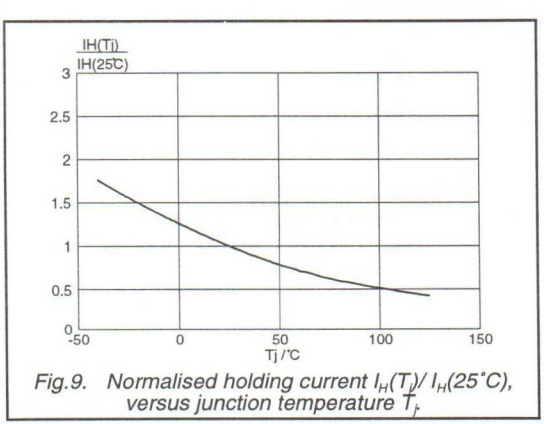



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

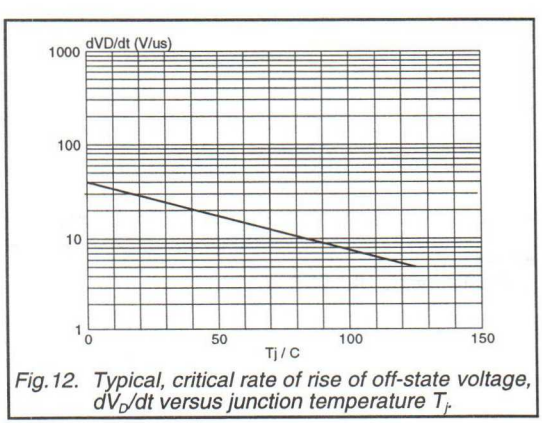



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

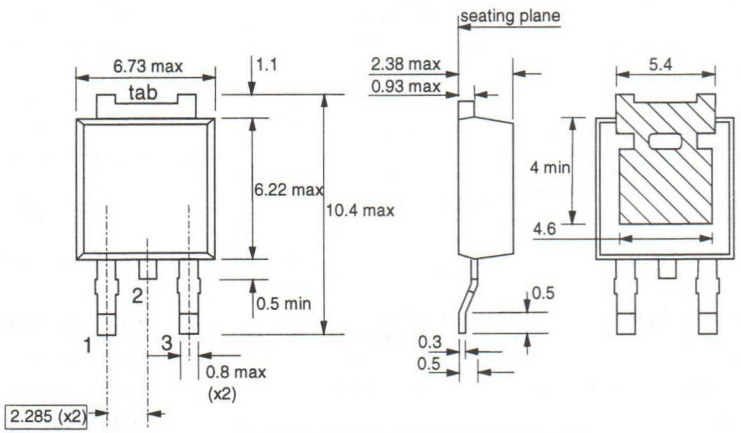



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

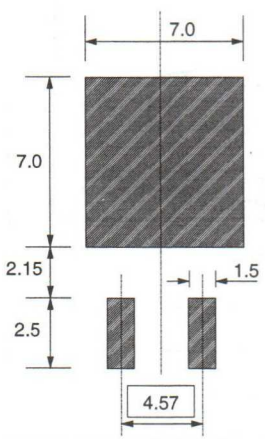



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT137S series E
BT137M series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

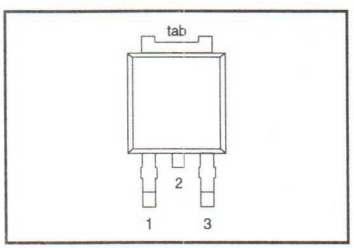
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT137S** (or BT137M)- | **500E** | **600E** | **800E** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

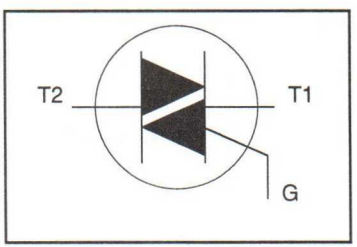
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | - | 2.5 | 10 | mA |
| | | T2+ G- | - | 4.0 | 10 | mA |
| | | T2- G- | - | 5.0 | 10 | mA |
| | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | 3.0 | 25 | mA |
| | | T2+ G- | - | 14 | 35 | mA |
| | | T2- G- | - | 3.0 | 25 | mA |
| | | T2- G+ | - | 4.0 | 35 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 2.5 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

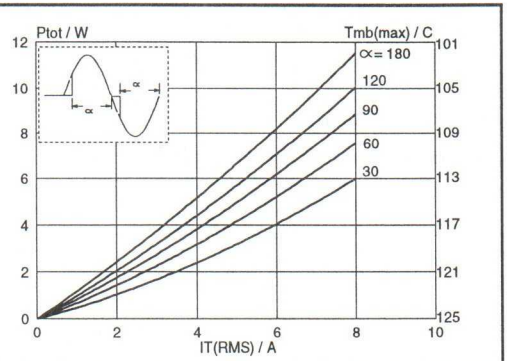



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

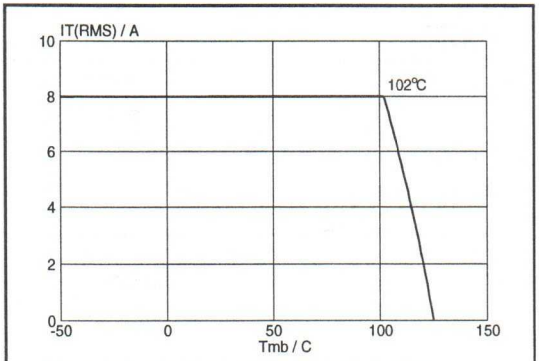



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

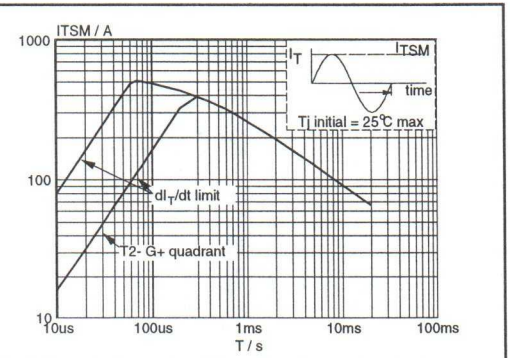



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

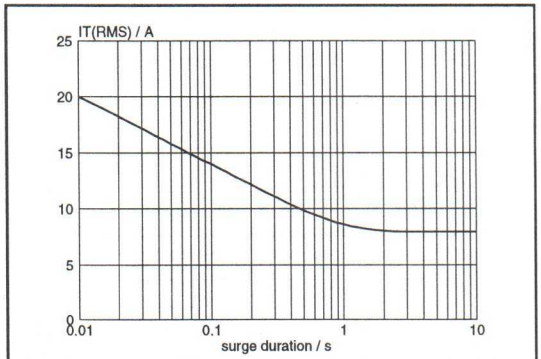



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

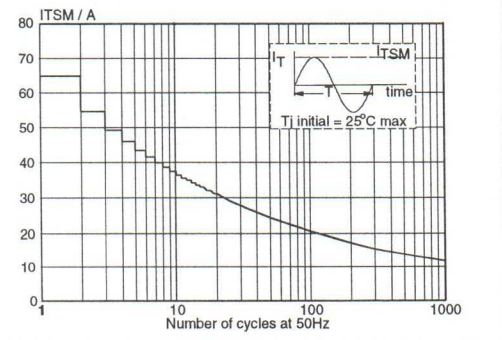



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

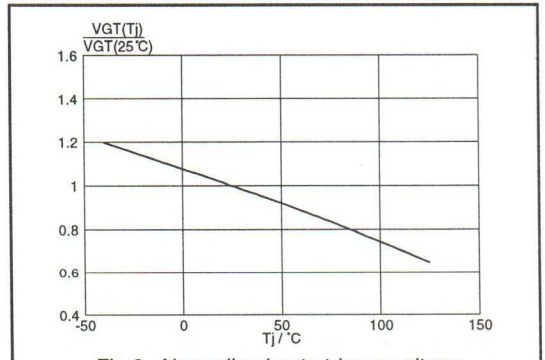



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

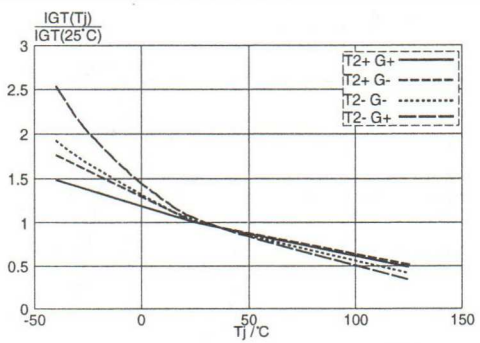



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

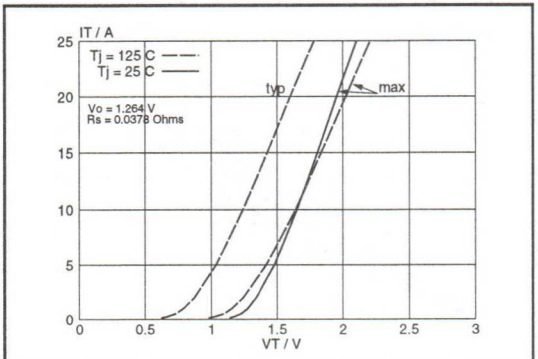



*Fig.10. Typical and maximum on-state characteristic.*

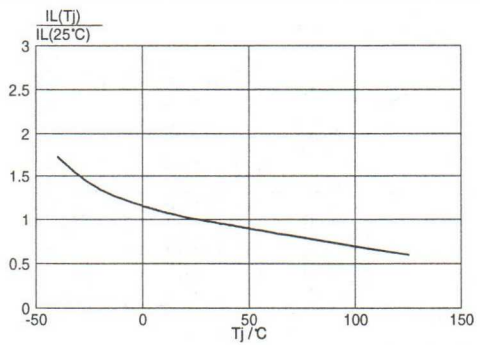



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

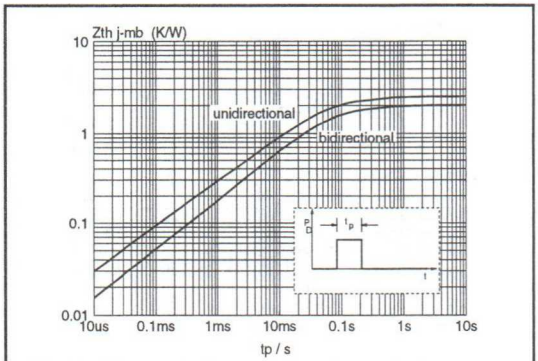



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

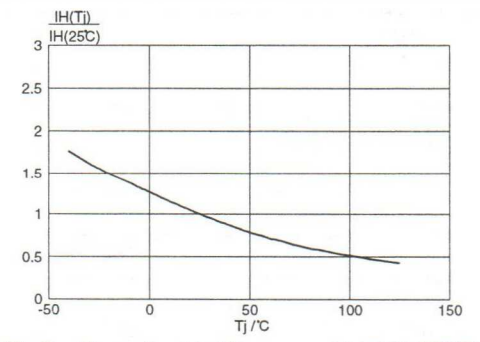



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

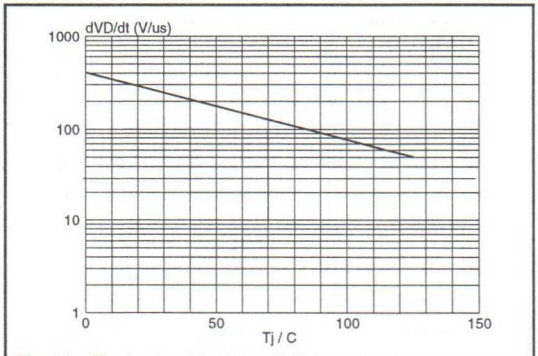



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

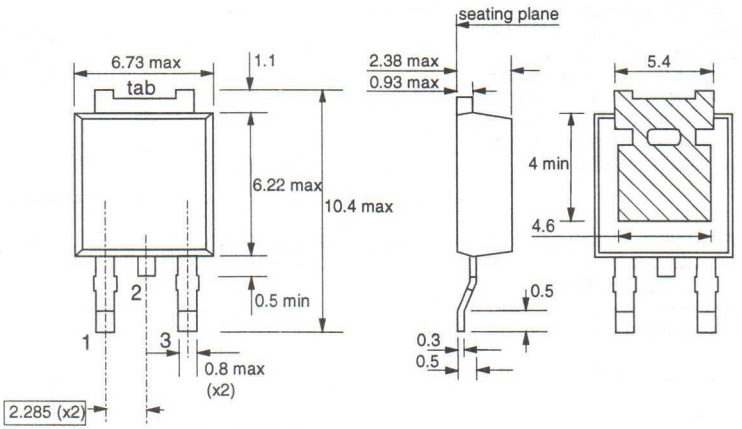



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

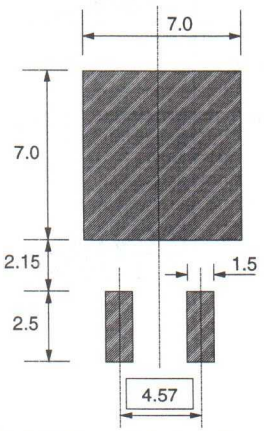



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

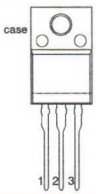
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | **BT137X-** | **500** | **600** | **800** | |
| | | **BT137X-** | **500F** | **600F** | **800F** | |
| | | **BT137X-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | | 65 | 65 | 65 | A |

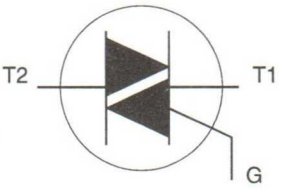
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137X- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 11 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 30 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 30 | 30 | 45 | mA |
| | | T2+ G- | - | 16 | 45 | 45 | 60 | mA |
| | | T2- G- | - | 5 | 30 | 30 | 45 | mA |
| | | T2- G+ | - | 7 | 45 | 45 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 5 | 20 | 20 | 40 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT137X- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 8 A; $dI_{com}/dt$ = 3.6 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

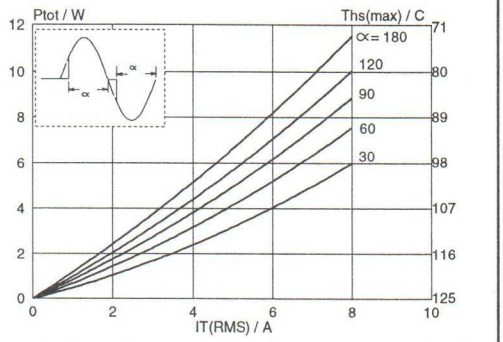



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

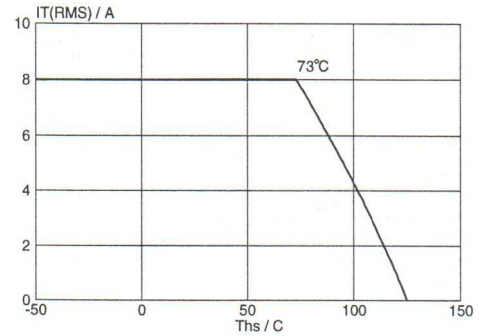



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

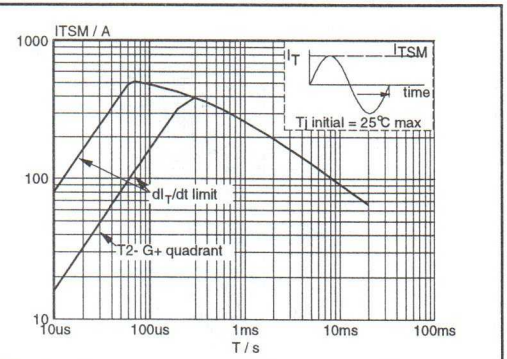



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

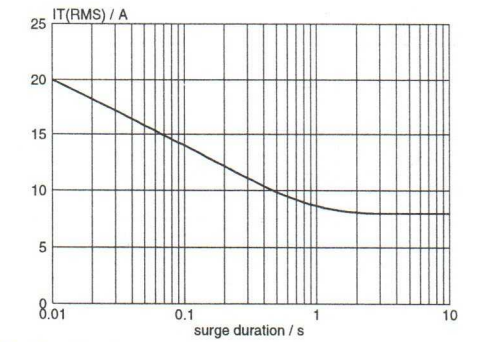



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73°C$.*

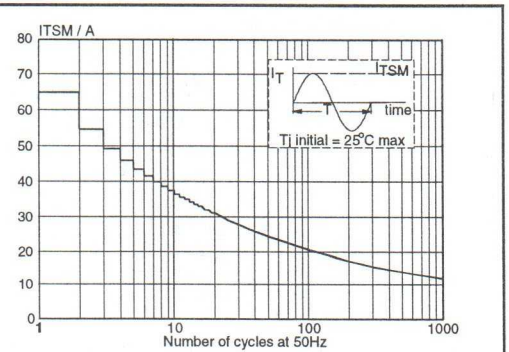



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

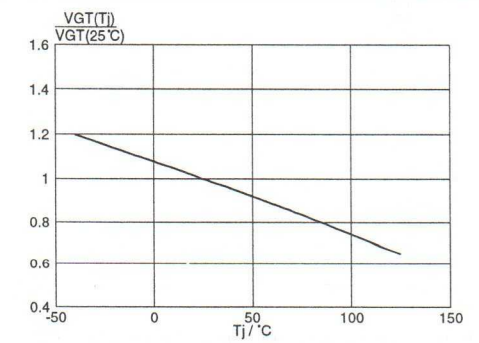



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

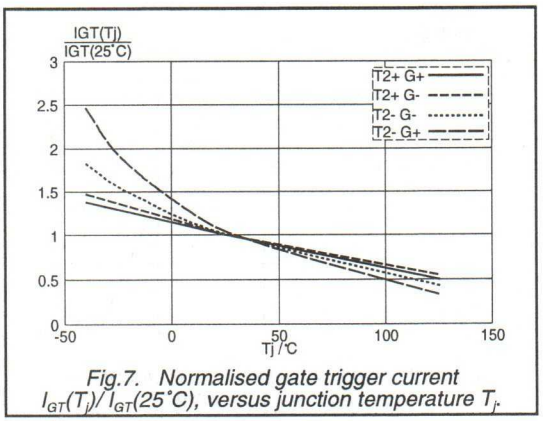



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

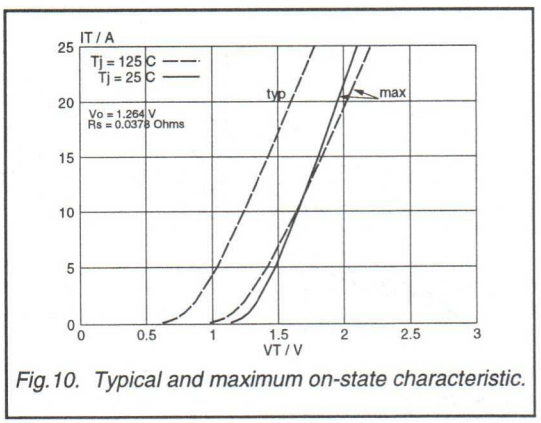



*Fig.10. Typical and maximum on-state characteristic.*

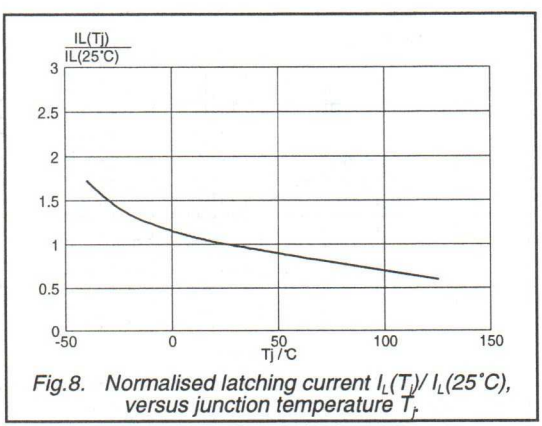



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

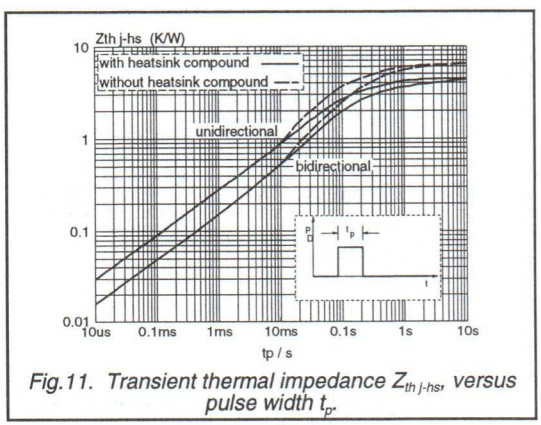



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

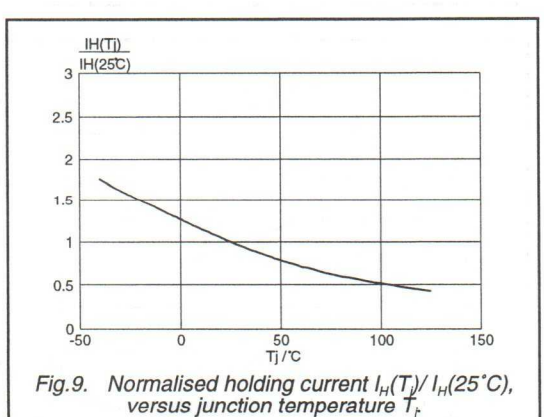



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

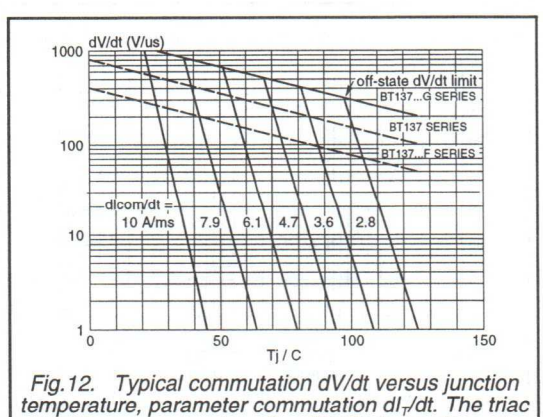



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs logic level

# BT137X series D

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

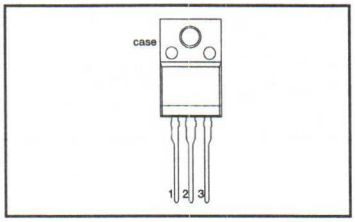
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | UNIT |
|---|---|---|---|---|
| | | BT137X- | 500D | 600D | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | 500 | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | | 65 | 65 | A |

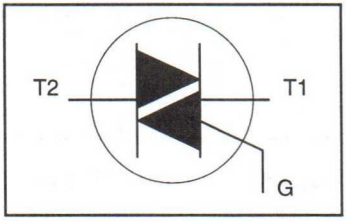
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | UNIT |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | |
| | | t = 20 ms | - | 65 | | A |
| | | t = 16.7 ms | - | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | |
| | | T2+ G+ | - | 50 | | A/µs |
| | | T2+ G- | - | 50 | | A/µs |
| | | T2- G- | - | 50 | | A/µs |
| | | T2- G+ | - | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 5 | mA |
| | | | T2+ G- | - | 3.5 | 5 | mA |
| | | | T2- G- | - | 3.5 | 5 | mA |
| | | | T2- G+ | - | 6.5 | 10 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 1.6 | 15 | mA |
| | | | T2+ G- | - | 8.5 | 20 | mA |
| | | | T2- G- | - | 1.2 | 15 | mA |
| | | | T2- G+ | - | 2.5 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 1.5 | 10 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 5 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

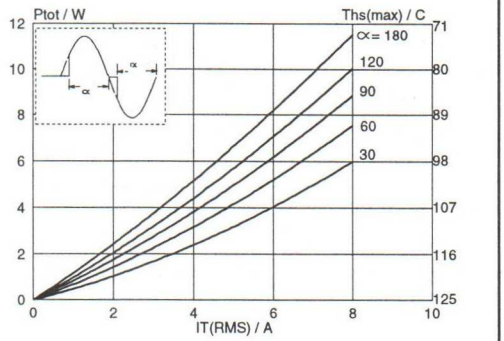



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

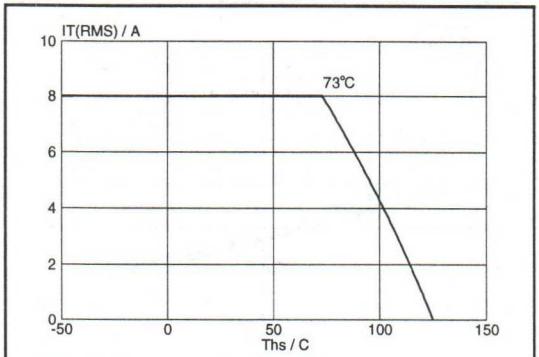



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

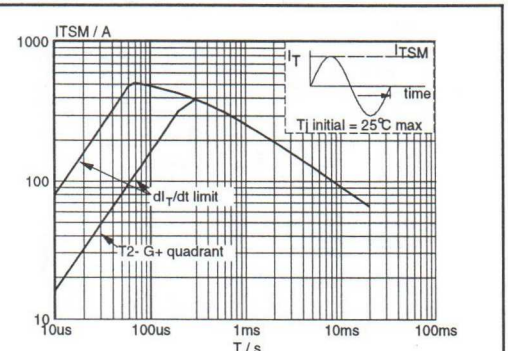



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

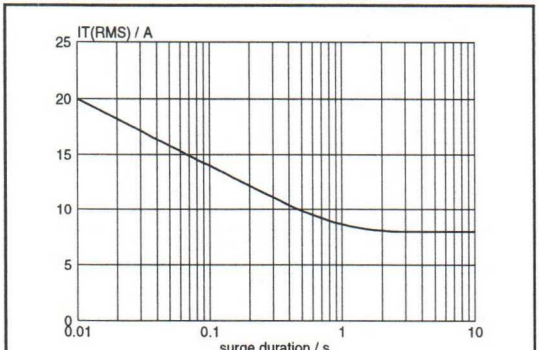



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73°C$.*

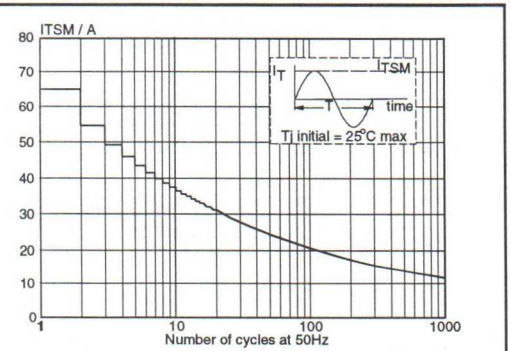



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

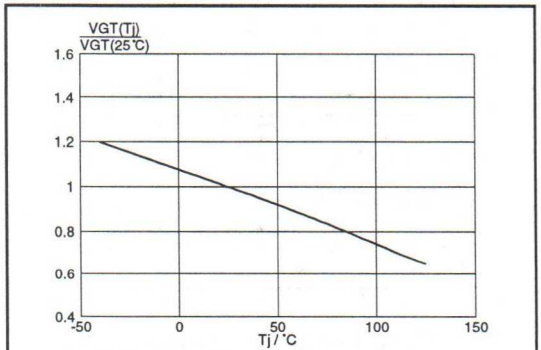



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

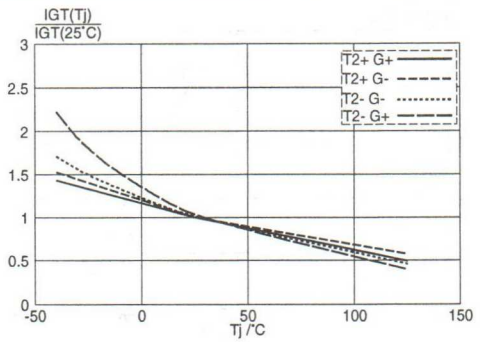



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

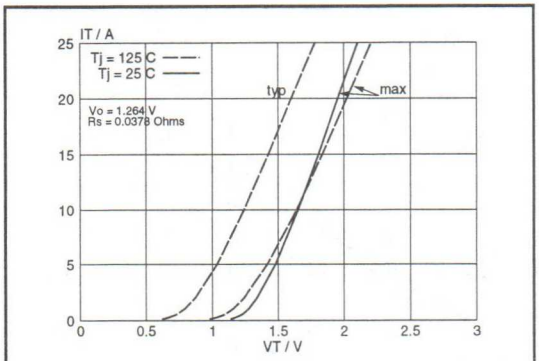



*Fig.10. Typical and maximum on-state characteristic.*

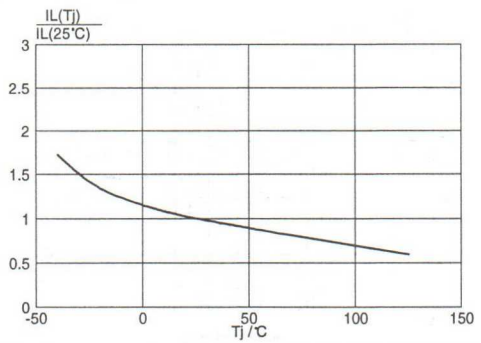



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

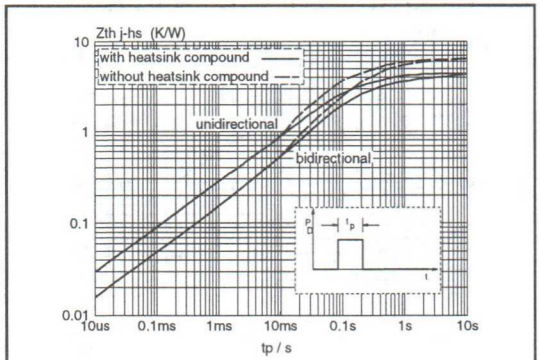



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

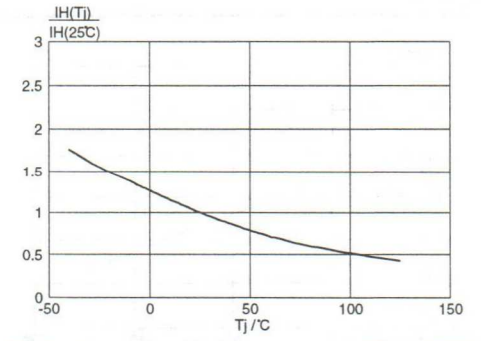



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

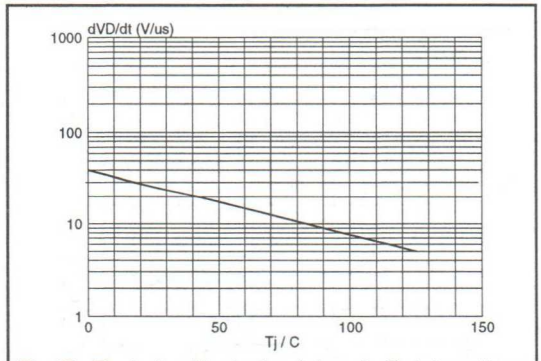



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs sensitive gate

# BT137X series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack, plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

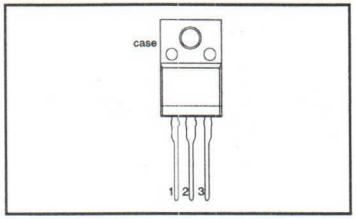
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT137X- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

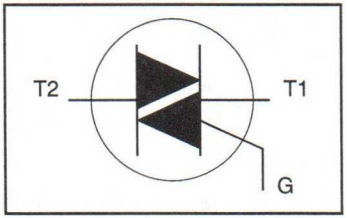
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | - | 2.5 | 10 | mA |
| | | T2+ G- | - | 4.0 | 10 | mA |
| | | T2- G- | - | 5.0 | 10 | mA |
| | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | 3.0 | 25 | mA |
| | | T2+ G- | - | 14 | 35 | mA |
| | | T2- G- | - | 3.0 | 25 | mA |
| | | T2- G+ | - | 4.0 | 35 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 2.5 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; $I_{TM}$ = 12 A | - | 2 | - | µs |

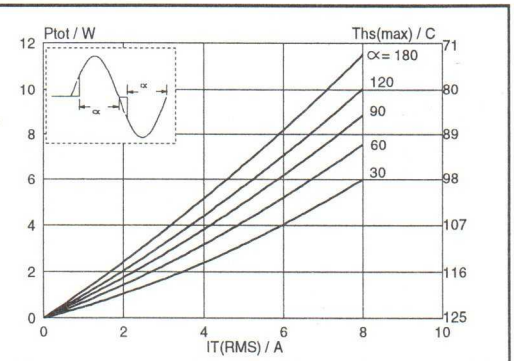



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

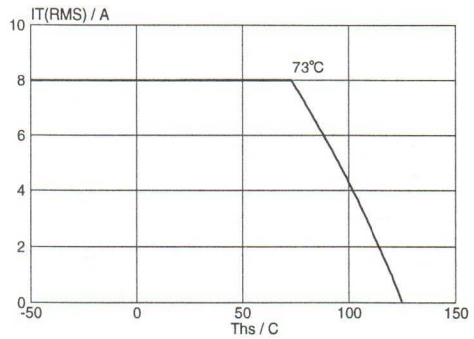



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

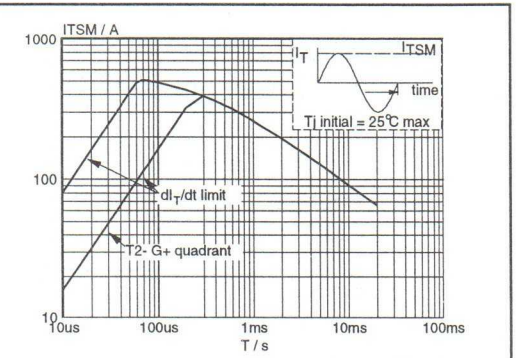



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

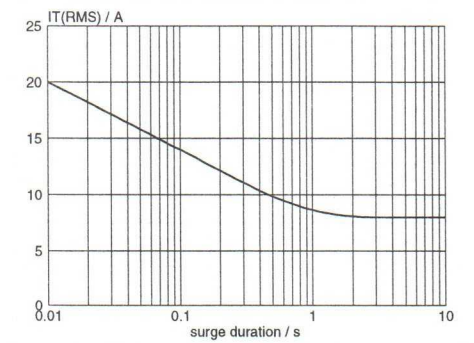



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73°C$.*

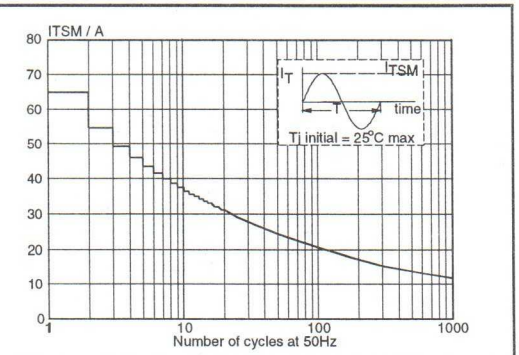



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

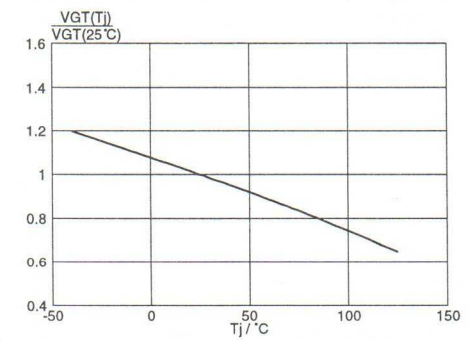



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

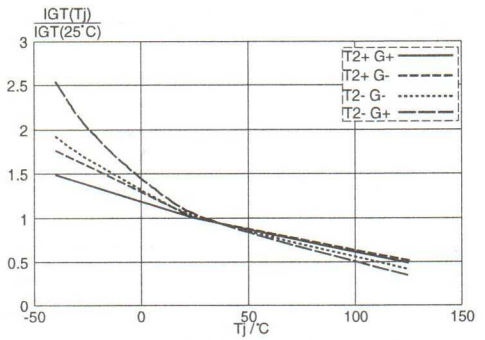



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

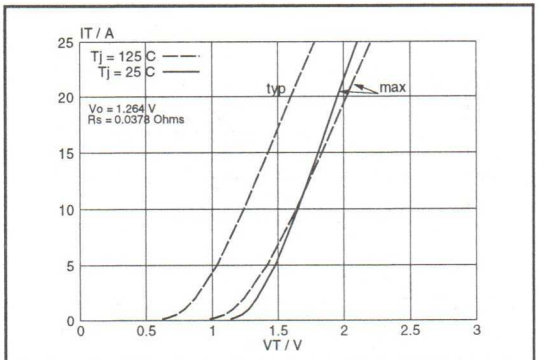



*Fig.10. Typical and maximum on-state characteristic.*

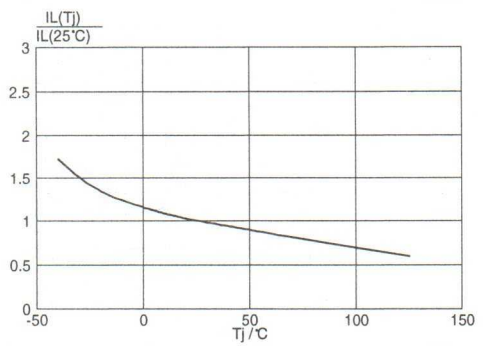



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

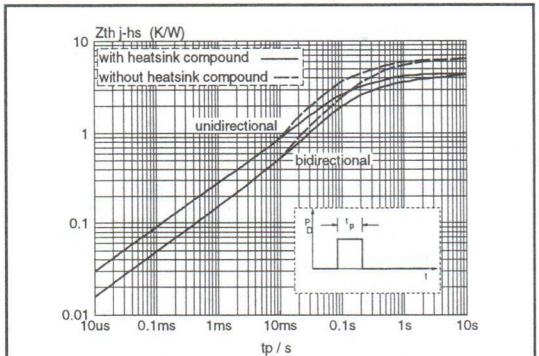



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

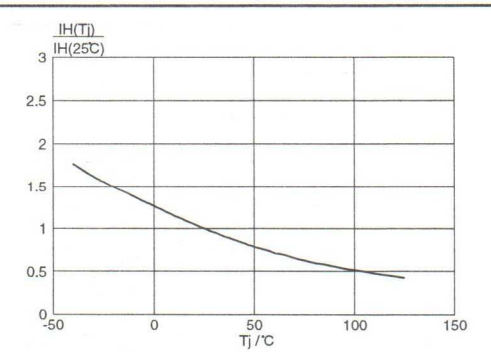



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

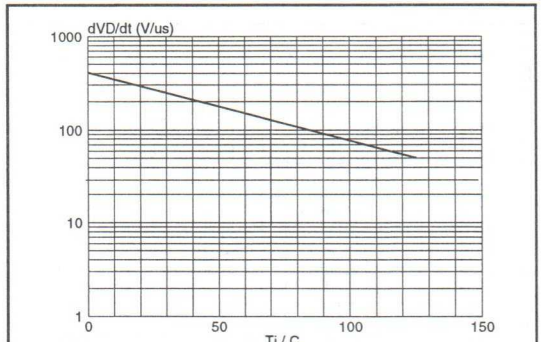



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

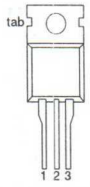
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT138- | 500 | 600 | 800 | |
| | BT138- | 500F | 600F | 800F | |
| | BT138- | 500G | 600G | 800G | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

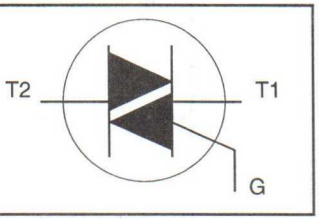
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | - | 1.4 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 12 A; $dI_{com}/dt$ = 5.4 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

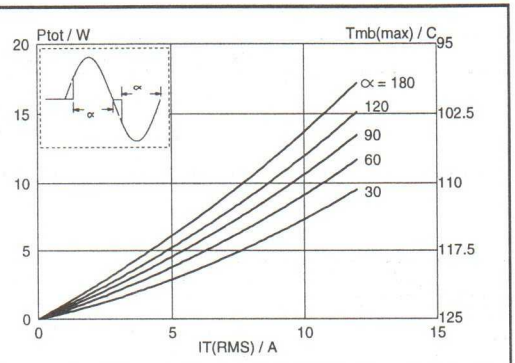



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

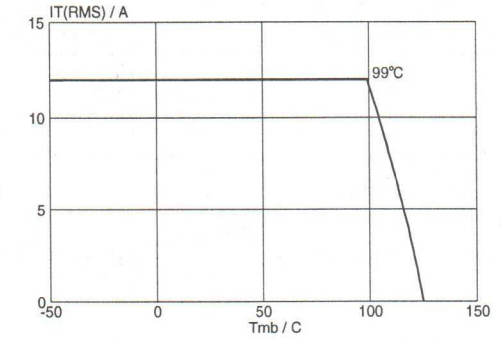



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

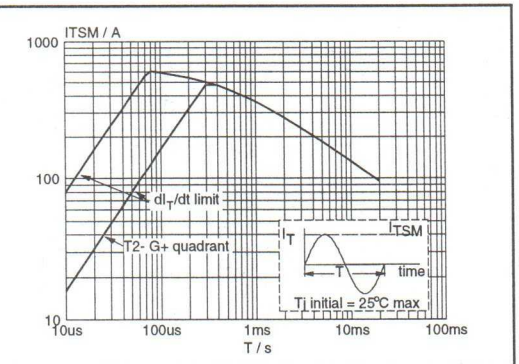



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

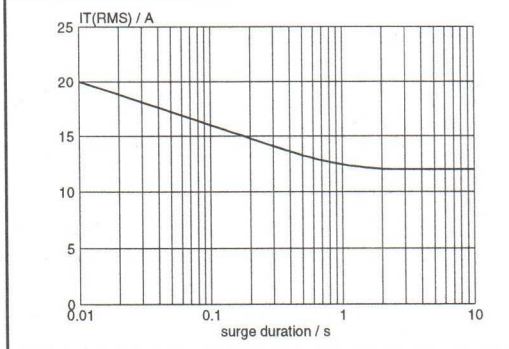



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

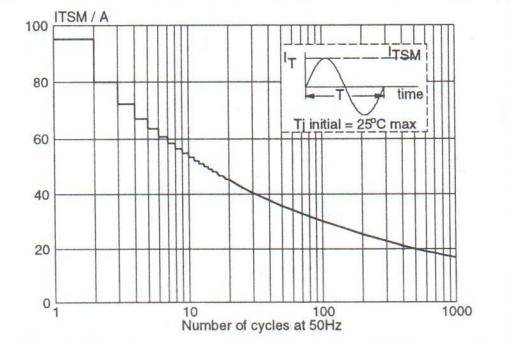



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

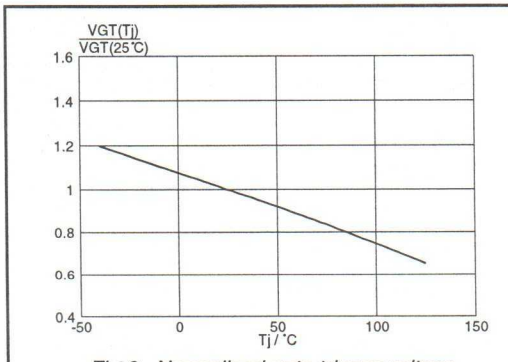



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

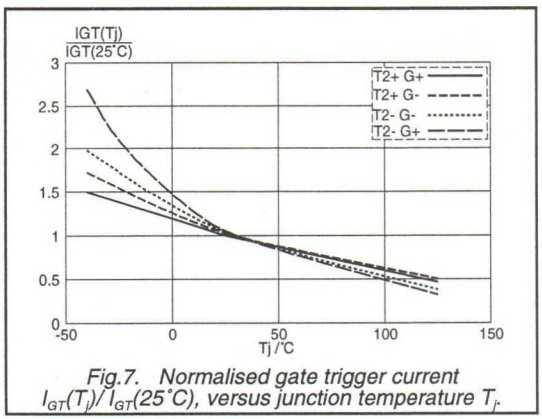



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

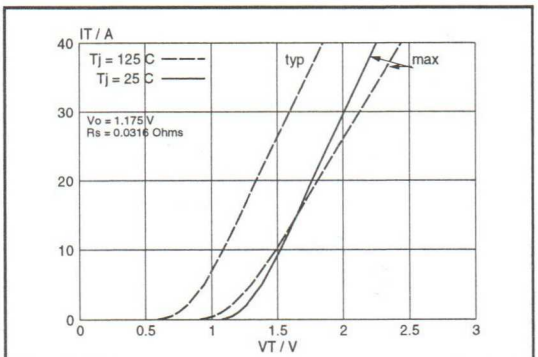



*Fig.10. Typical and maximum on-state characteristic.*

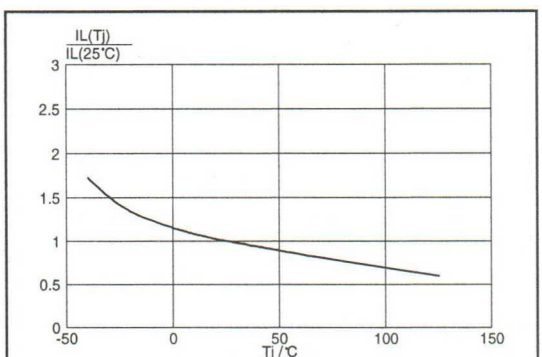



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

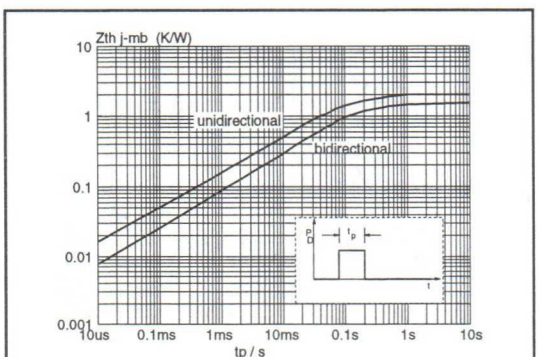



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

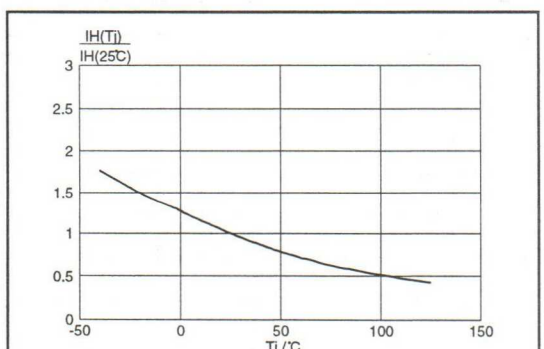



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

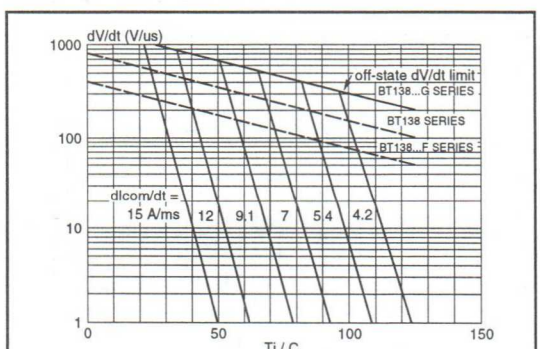



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs sensitive gate

# BT138 series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

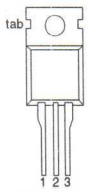
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT138- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

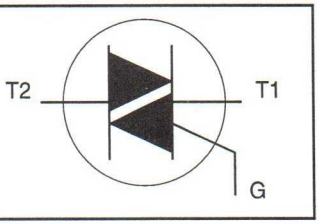
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 95 | | | A |
| | | t = 16.7 ms | - | 105 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 45 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | | - | 1.4 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

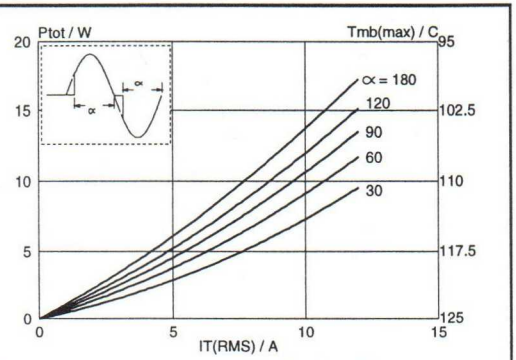



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

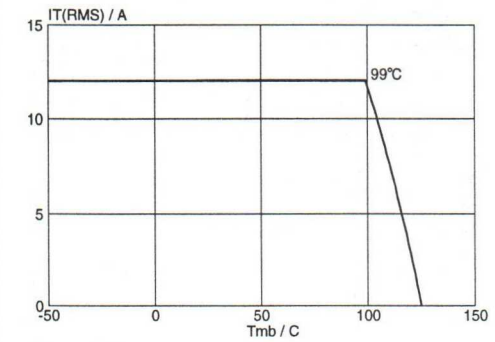



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

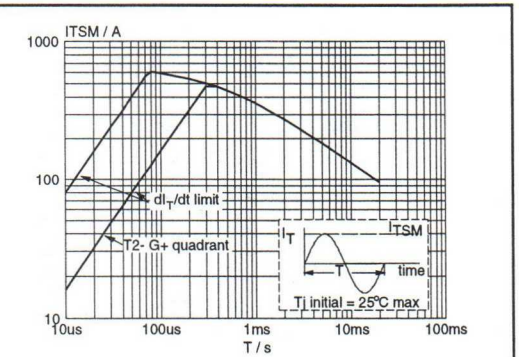



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

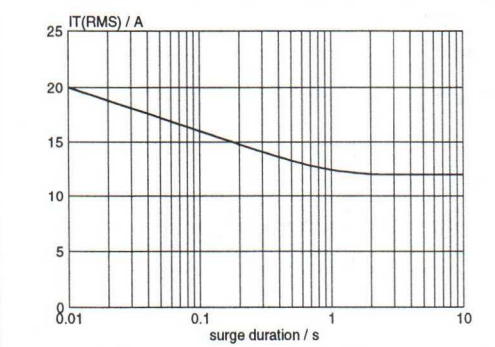



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

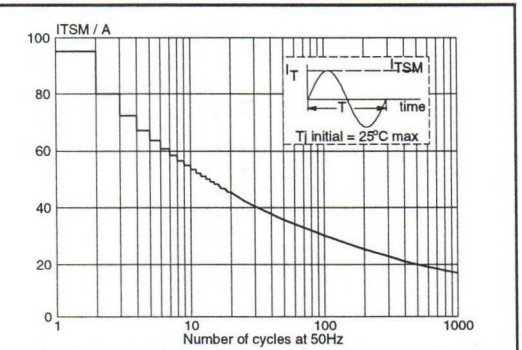



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

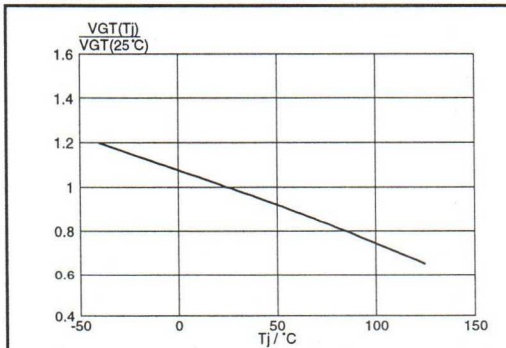



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

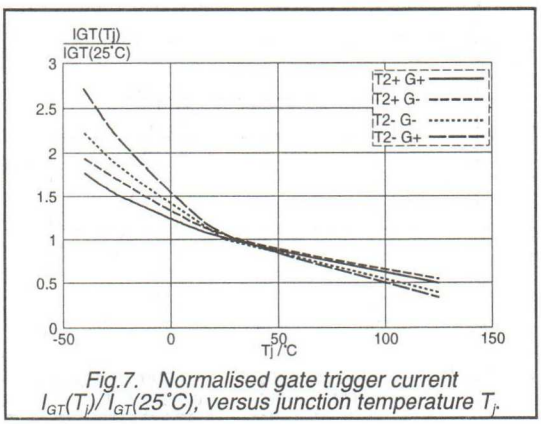



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

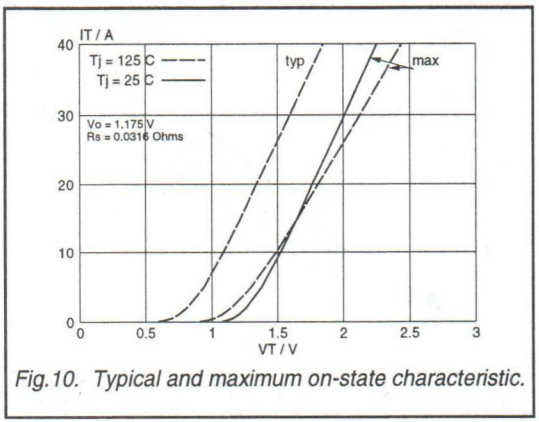



*Fig.10. Typical and maximum on-state characteristic.*

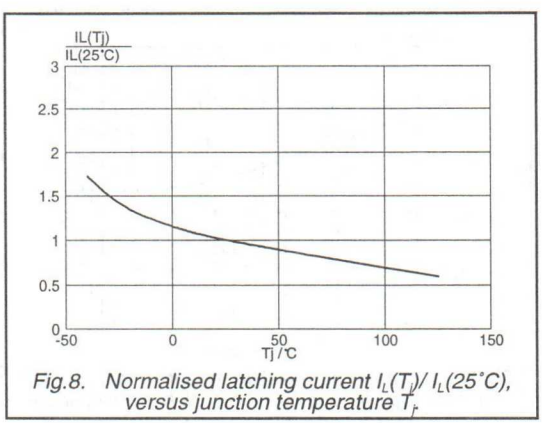



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

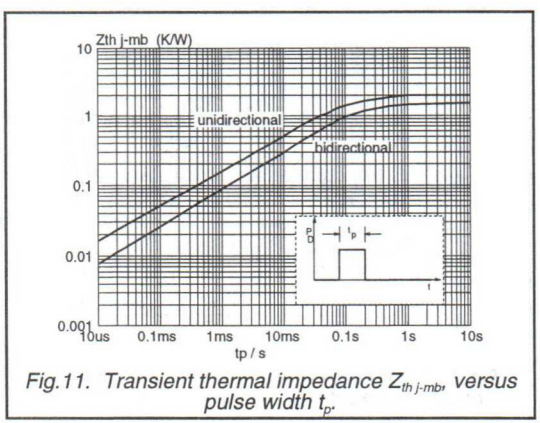



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

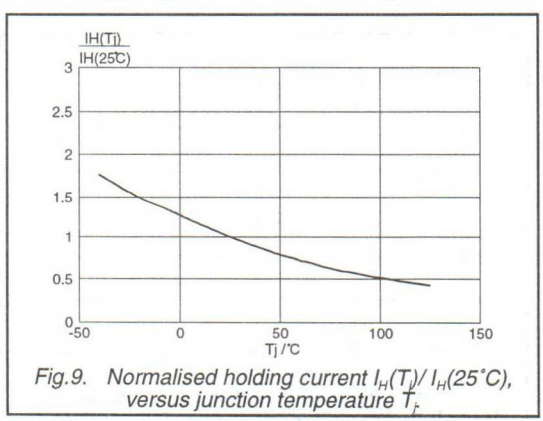



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

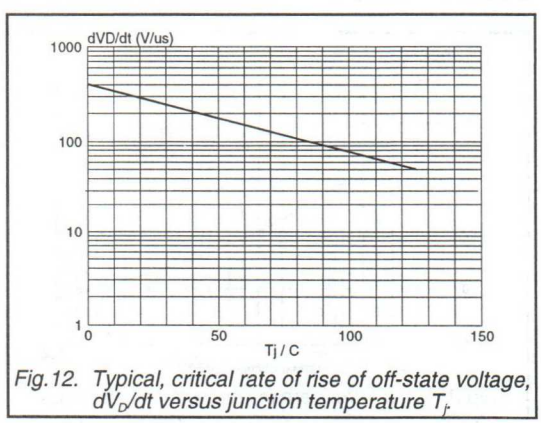



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

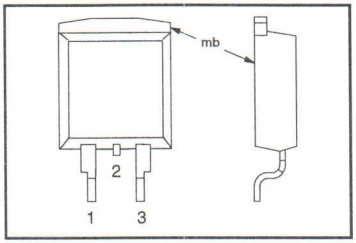
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT138B-** | **500** | **600** | **800** | |
| | **BT138B-** | **500F** | **600F** | **800F** | |
| | **BT138B-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

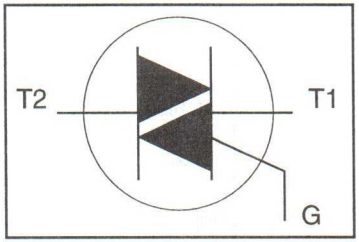
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138B- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | - | 1.4 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138B- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 12 A; $dI_{com}/dt$ = 5.4 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

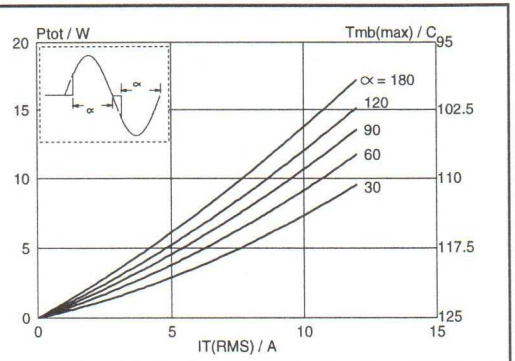



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

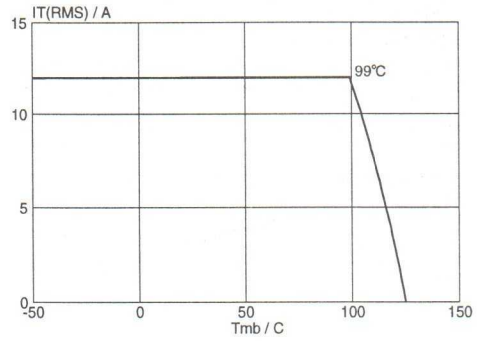



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

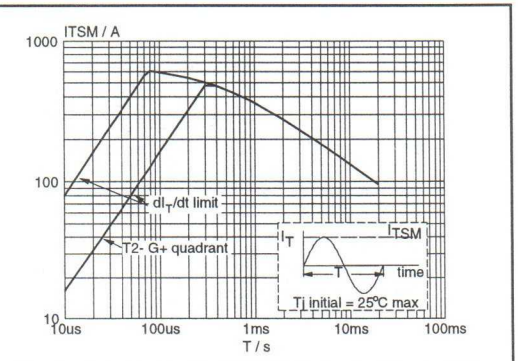



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

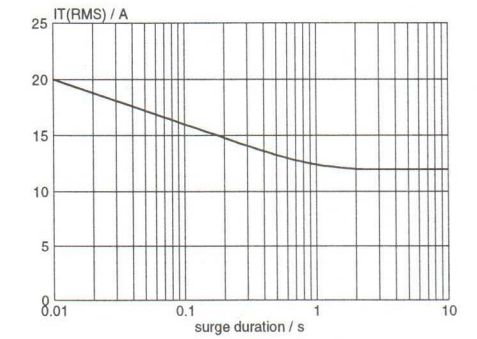



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

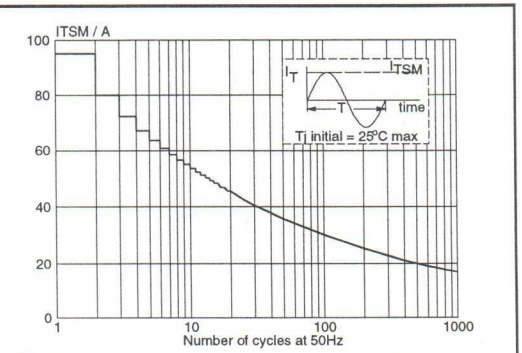



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

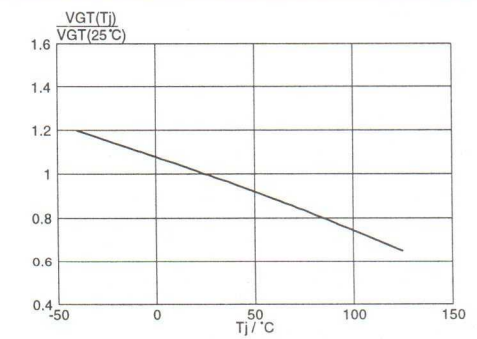



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

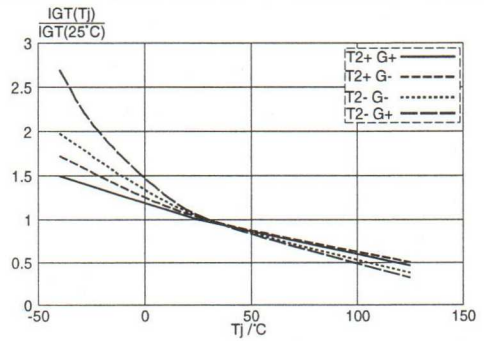



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

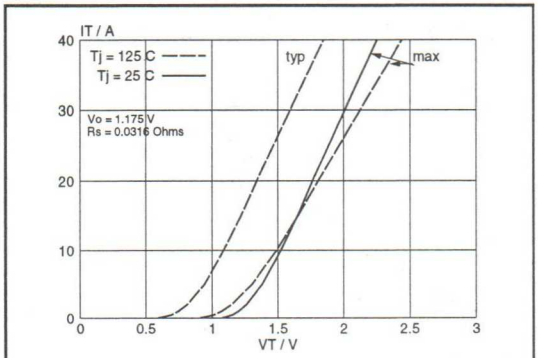



*Fig.10. Typical and maximum on-state characteristic.*

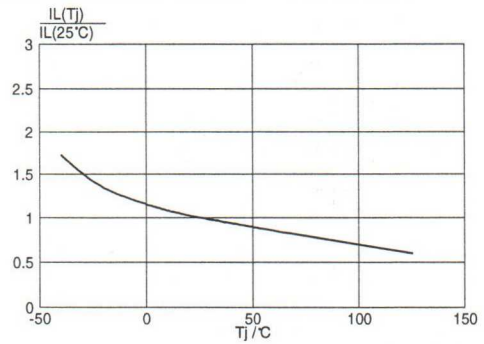



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

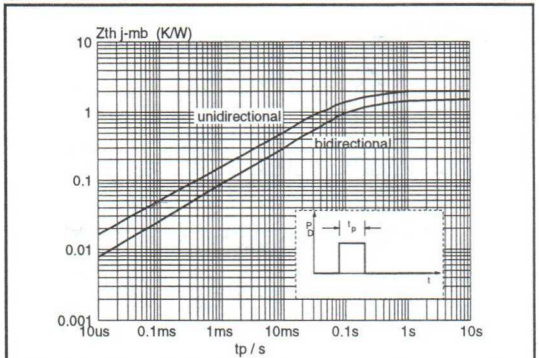



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

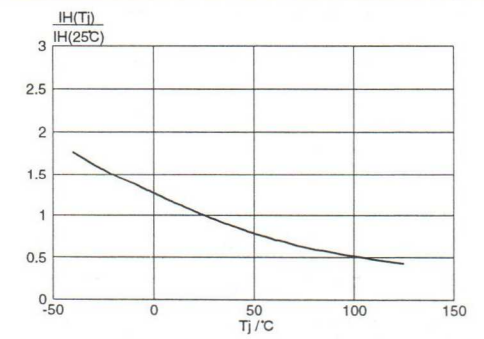



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

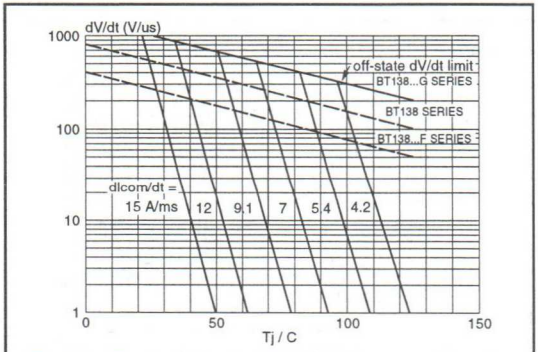



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

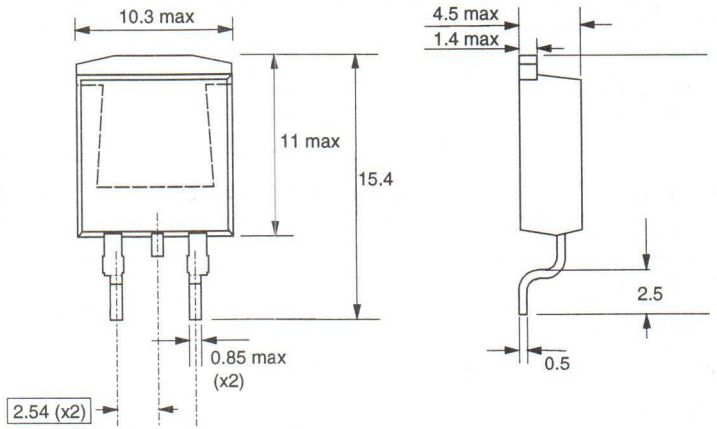



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**

1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

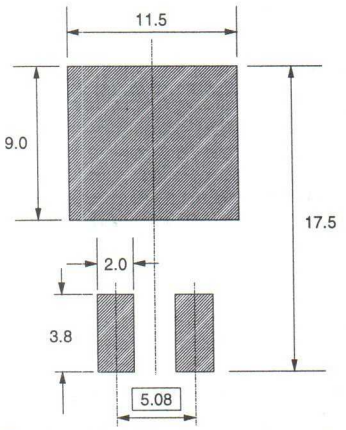



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT138B series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

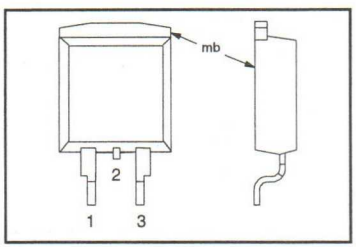
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT138B- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

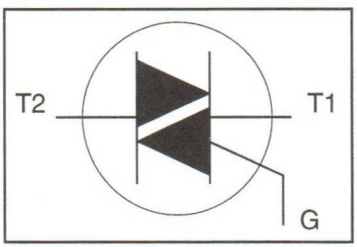
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | | - | 1.4 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

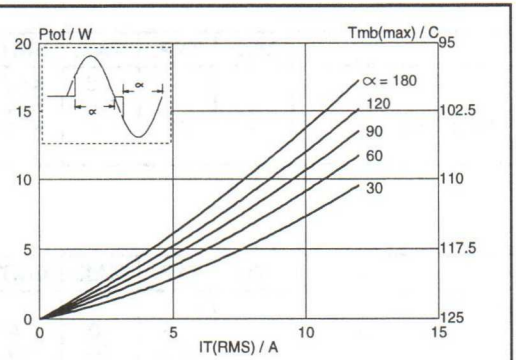



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

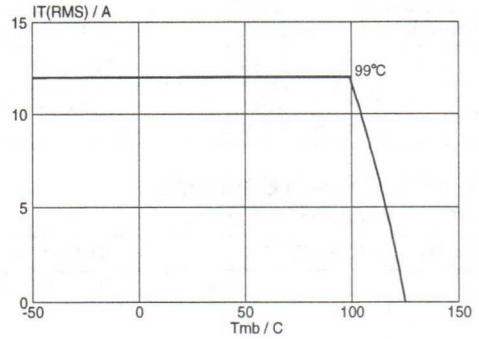



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

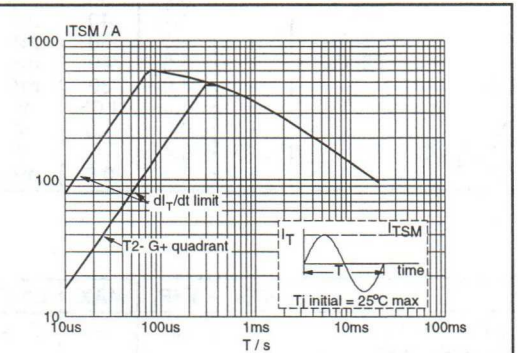



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

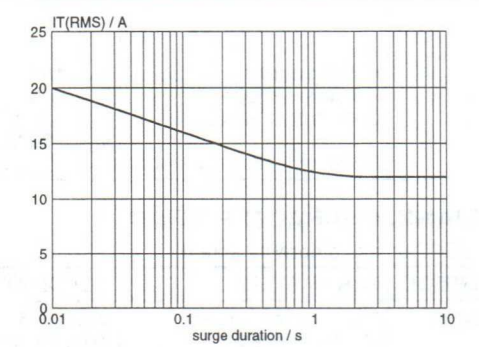



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

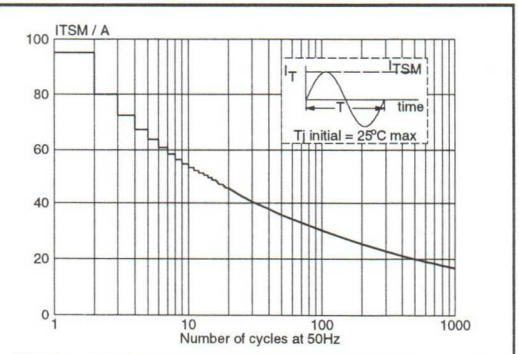



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

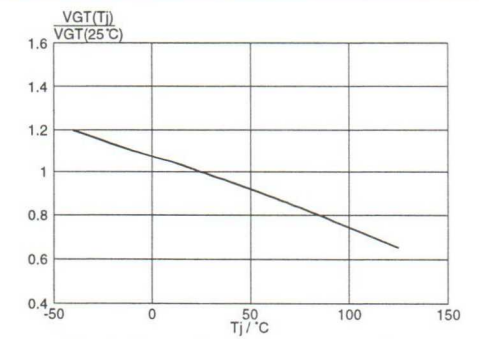



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

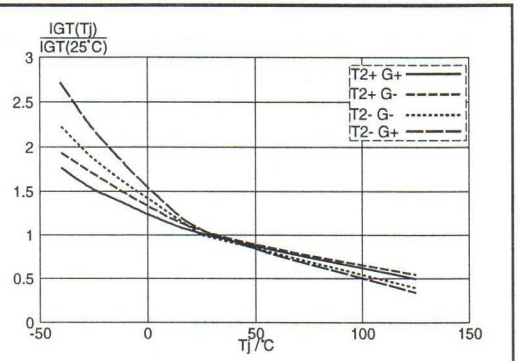



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

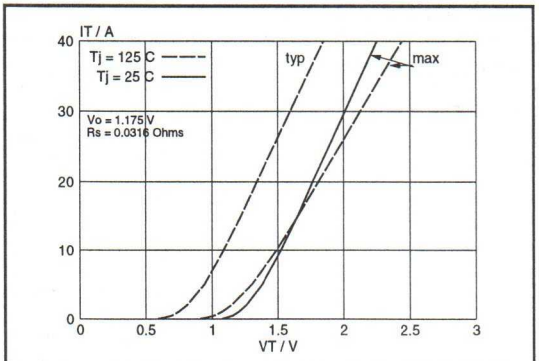



*Fig.10. Typical and maximum on-state characteristic.*

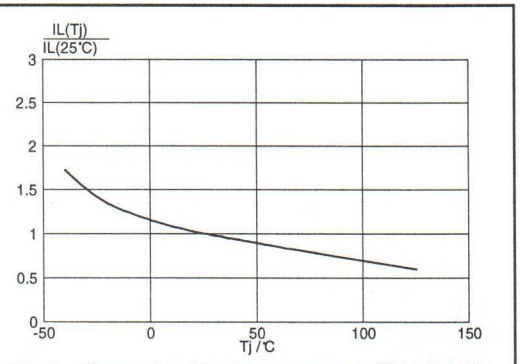



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

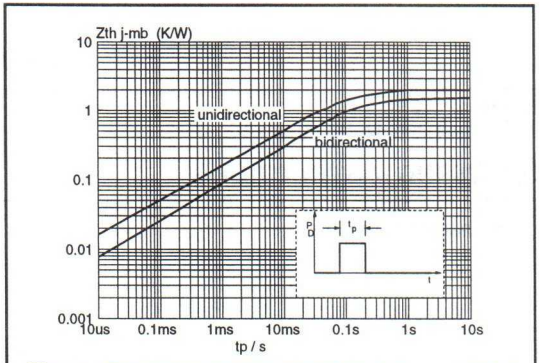



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

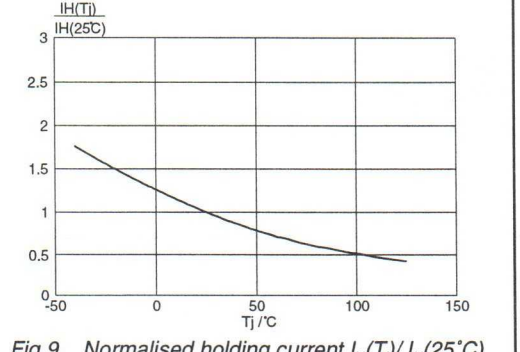



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

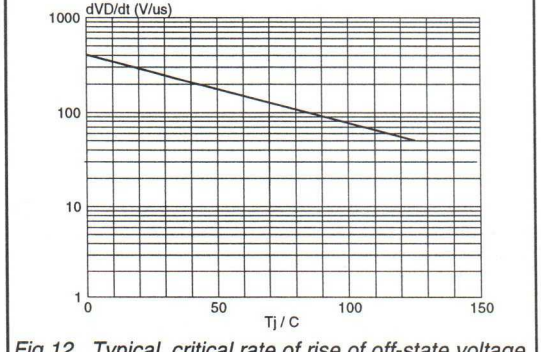



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

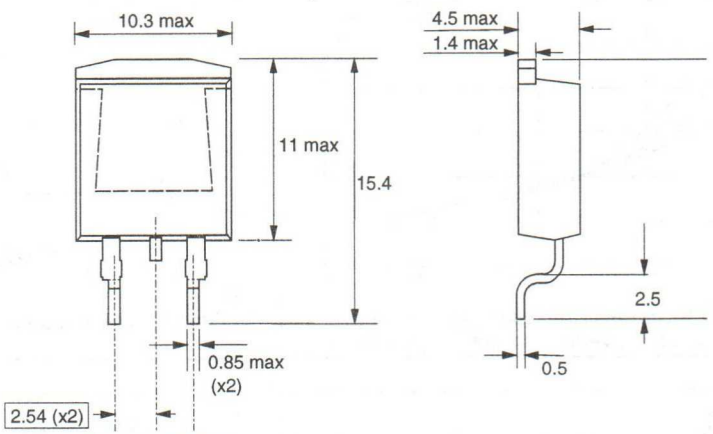



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

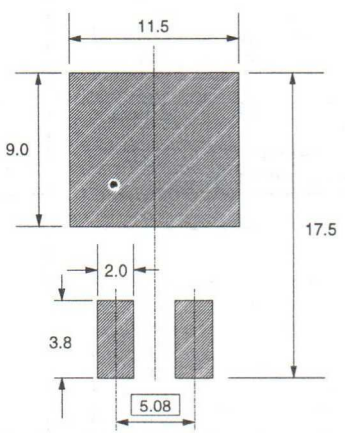



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

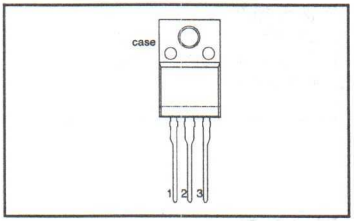
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | BT138X- 500 | 600 | 800 | |
| | | BT138X- 500F | 600F | 800F | |
| | | BT138X- 500G | 600G | 800G | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

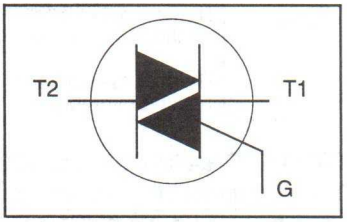
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. -500 | MAX. -600 | MAX. -800 | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 56$ °C | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 95 | | | A |
| | | t = 16.7 ms | - | 105 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 45 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138X- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | - | 1.4 | | 1.65 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT138X- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 12 A; $dI_{com}/dt$ = 5.4 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

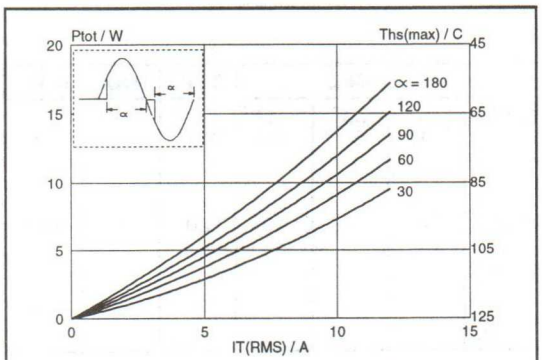



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

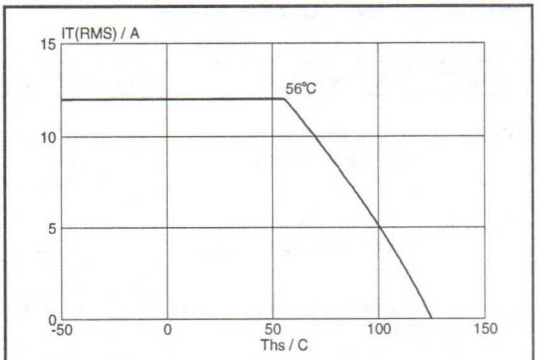



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

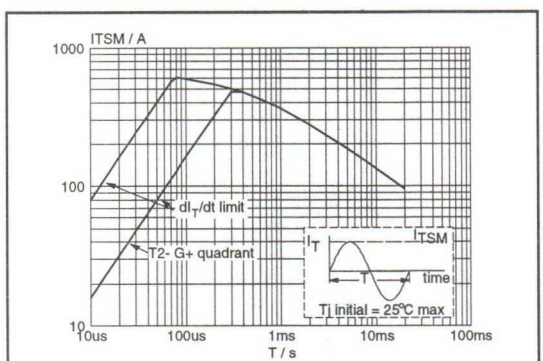



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

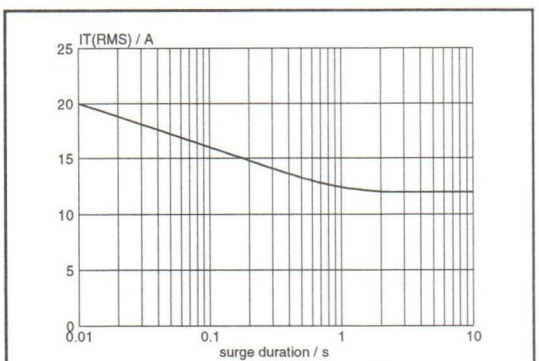



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56°C$.*

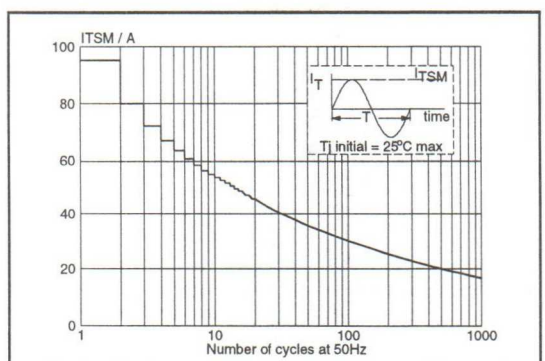



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

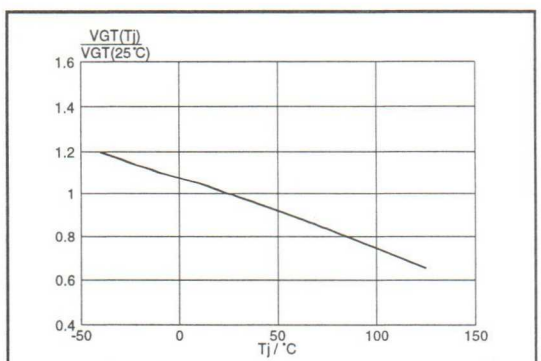



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

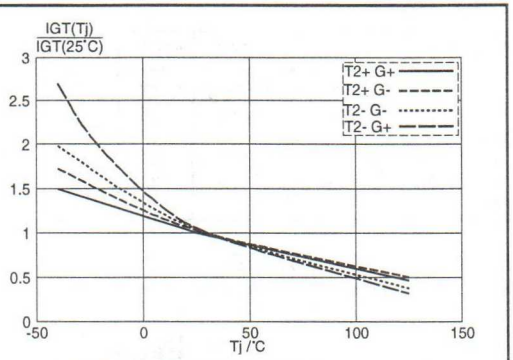



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

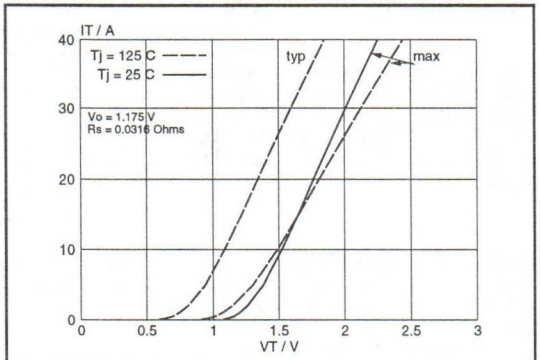



*Fig.10. Typical and maximum on-state characteristic.*

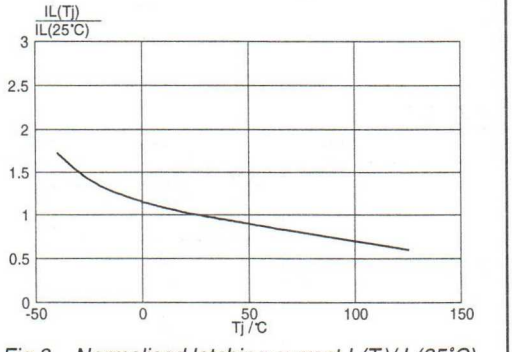



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

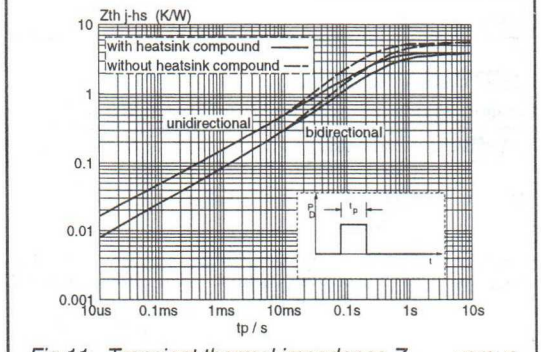



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

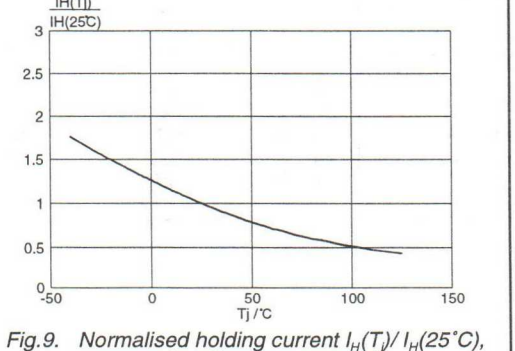



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

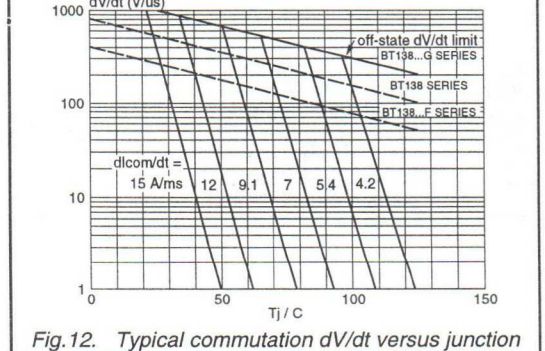



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

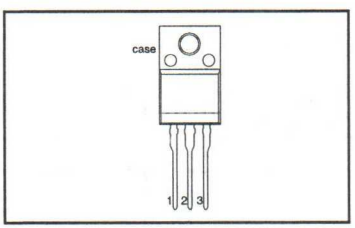
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT138X- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

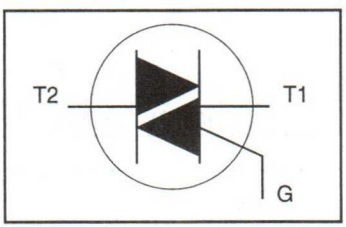
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 56$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 15 A | | - | 1.4 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 16 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

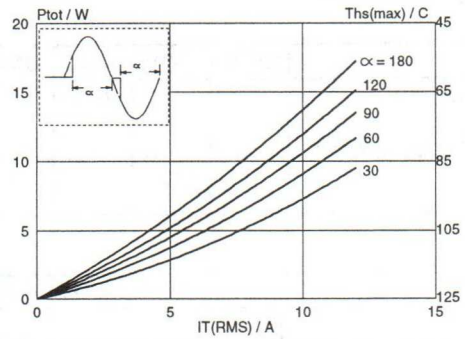



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

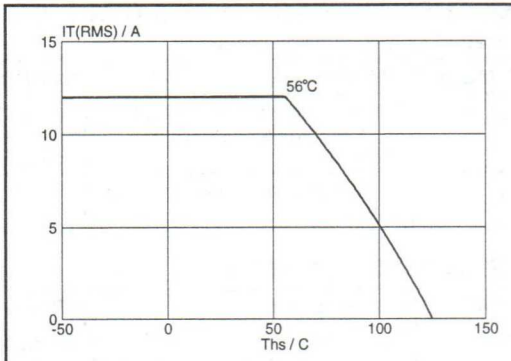



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

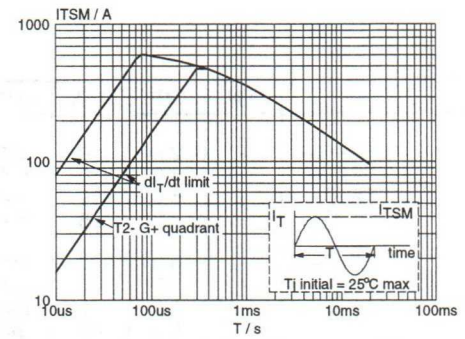



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

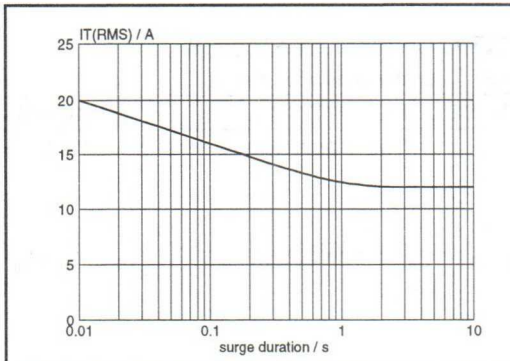



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56°C$.*

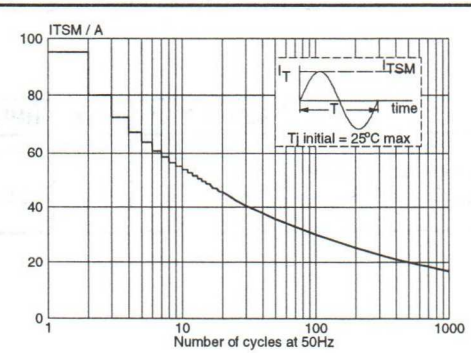



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

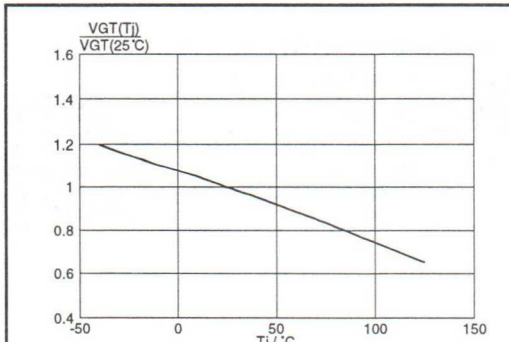



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

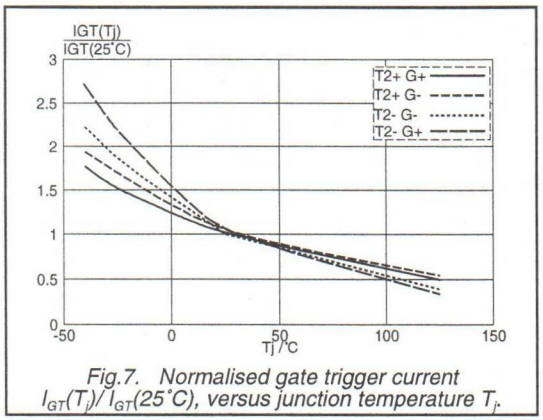



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

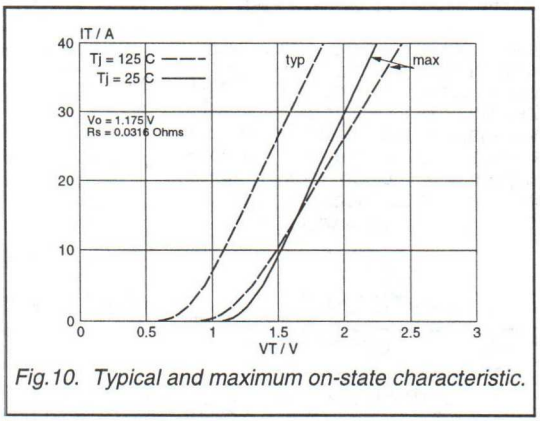



*Fig.10. Typical and maximum on-state characteristic.*

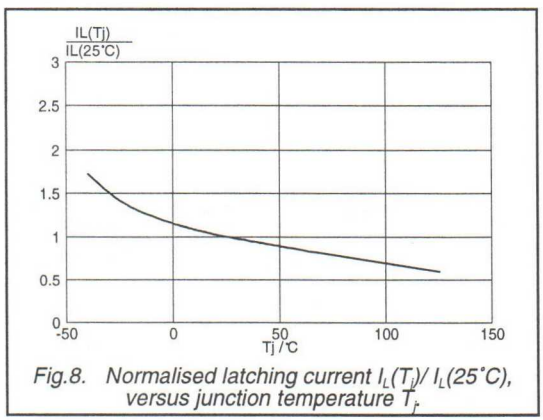



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

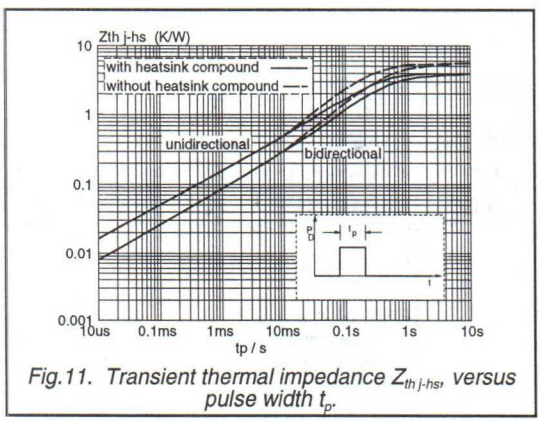



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

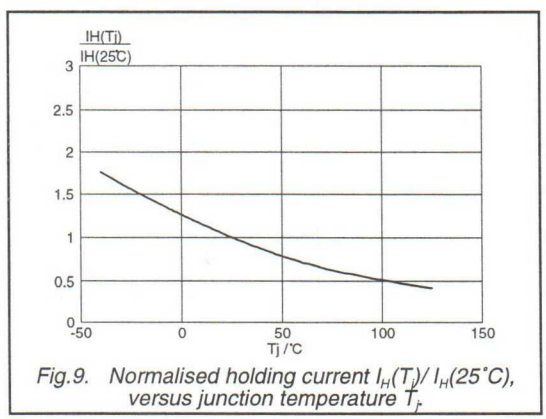



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

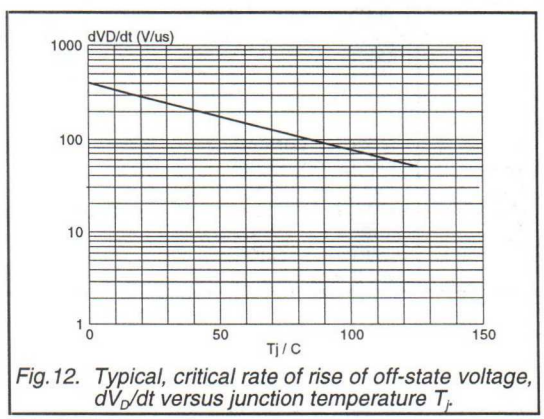



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

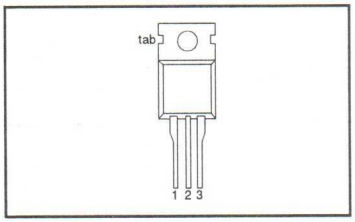
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | BT139- 500 | 600 | 800 | |
| | | BT139- 500F | 600F | 800F | |
| | | BT139- 500G | 600G | 800G | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

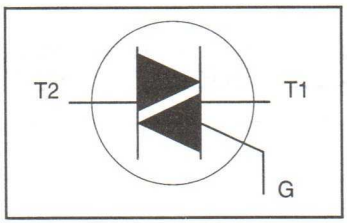
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | - | 1.2 | | 1.6 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

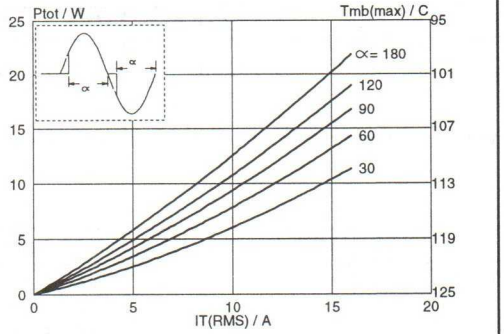



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

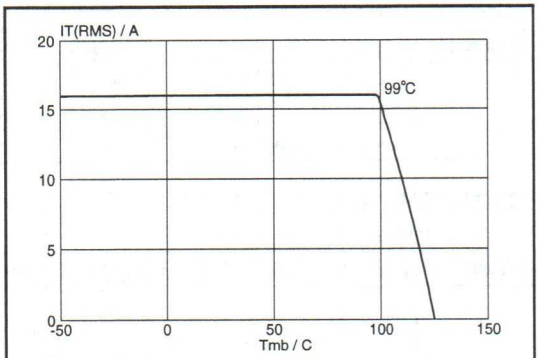



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

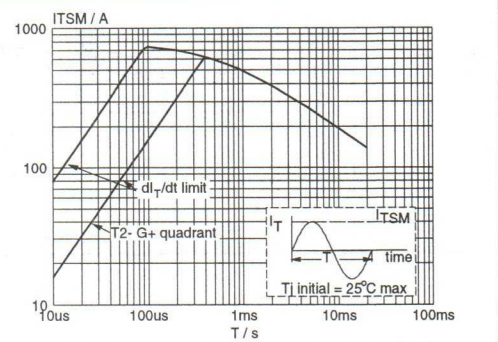



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

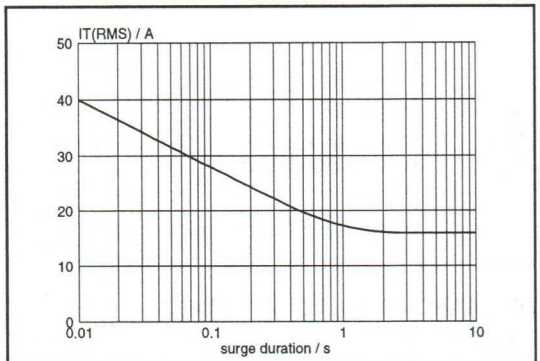



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

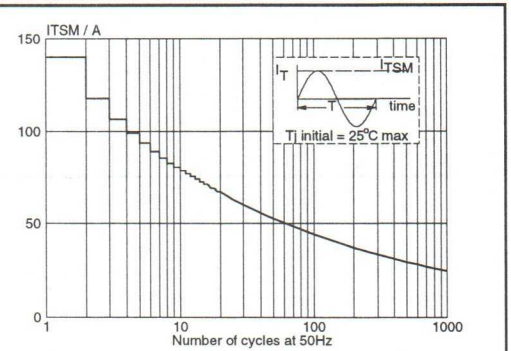



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

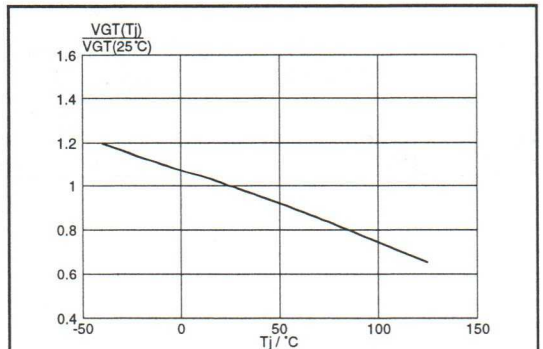



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

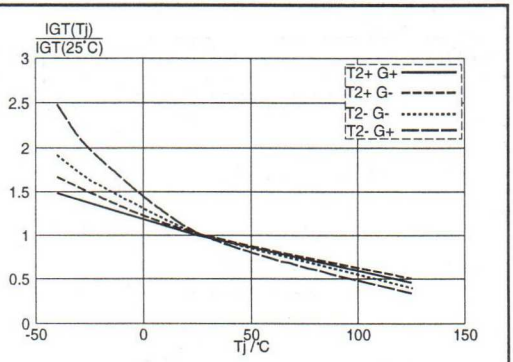



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

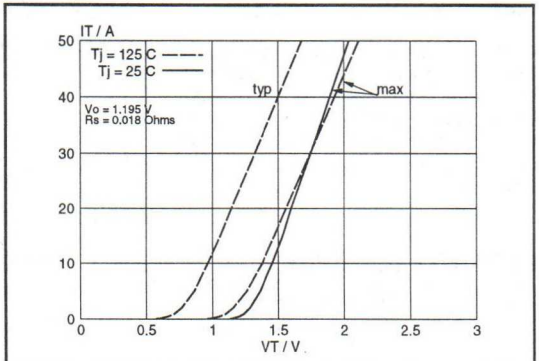



*Fig.10. Typical and maximum on-state characteristic.*

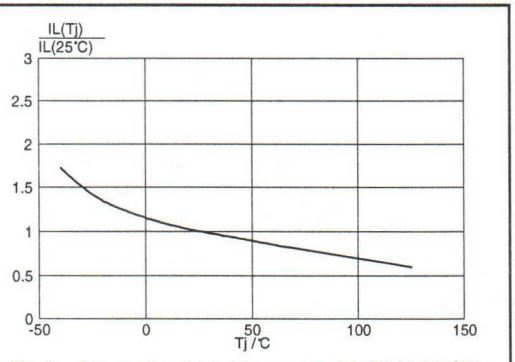



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

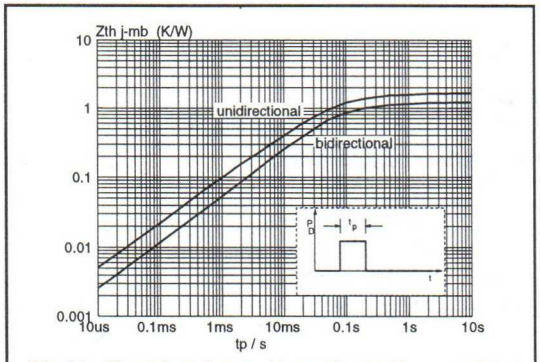



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

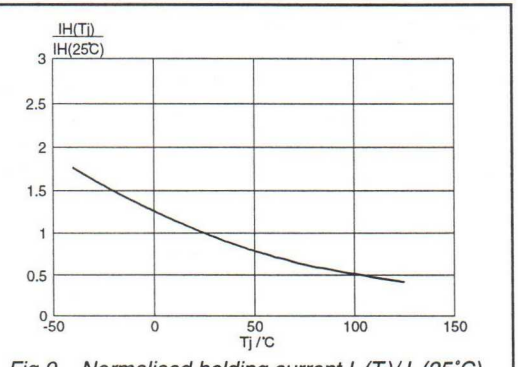



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

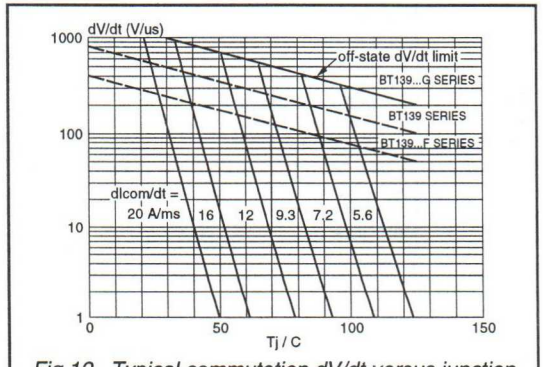



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

# Triacs sensitive gate

# BT139 series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

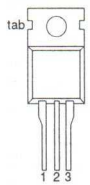
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

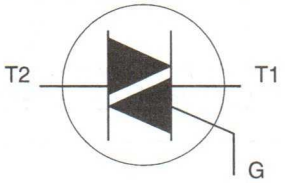
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

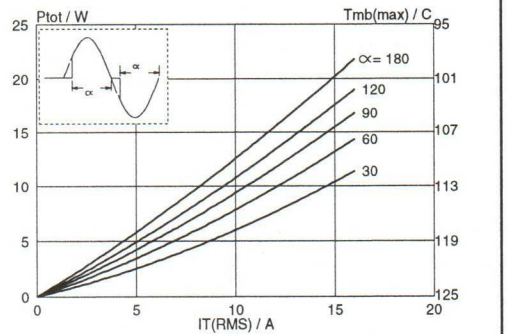



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

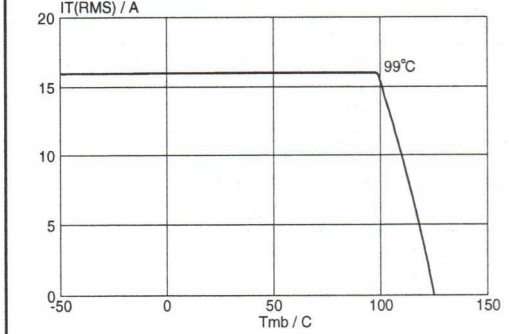



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

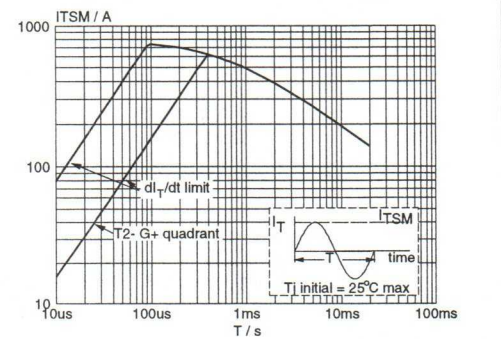



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

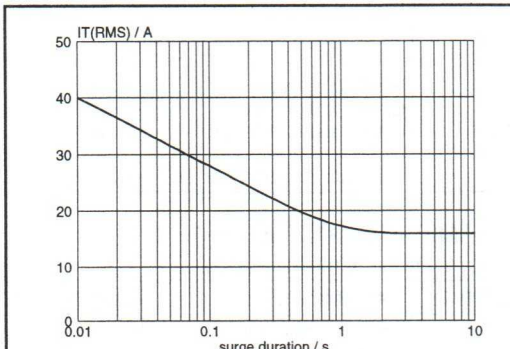



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

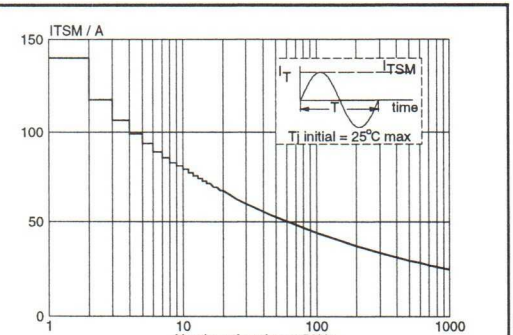



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

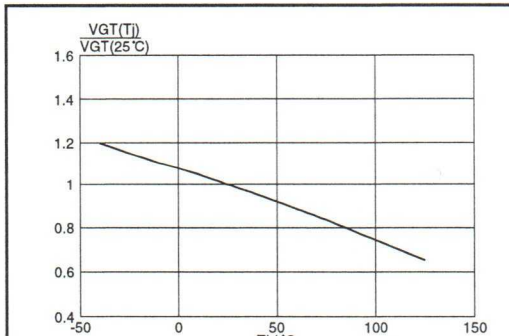



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

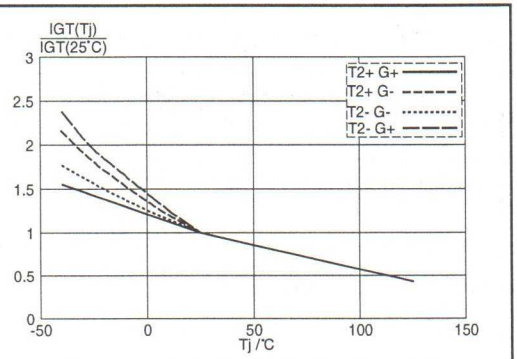



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

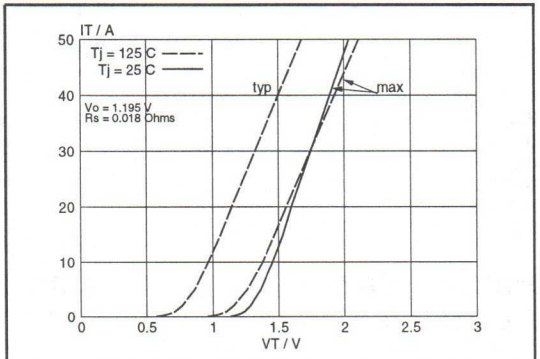



*Fig.10. Typical and maximum on-state characteristic.*

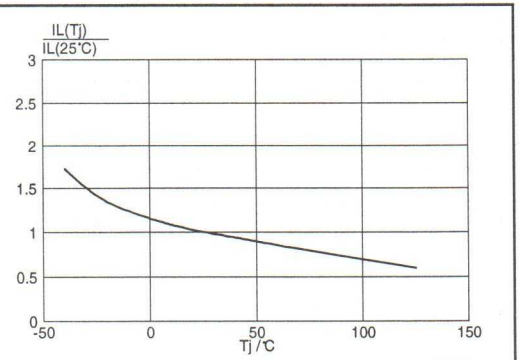



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

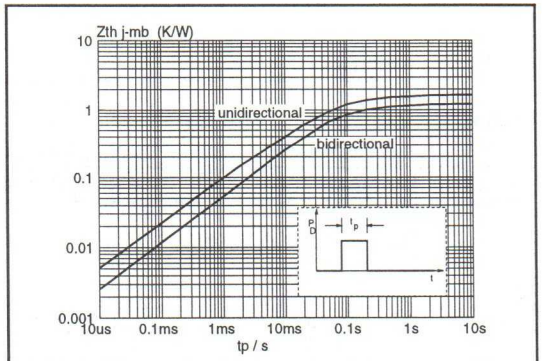



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

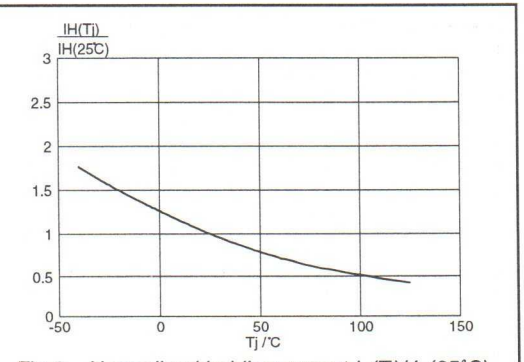



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

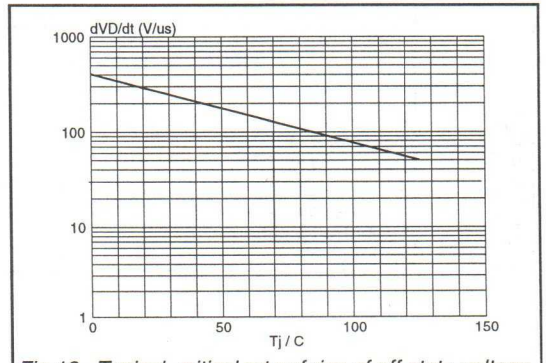



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs high noise immunity

# BT139 series H

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

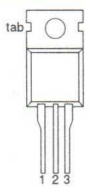
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139- | 500H | 600H | 800H | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

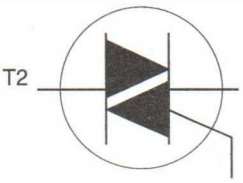
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 10 | 14 | 50 | mA |
| | | | T2+ G- | 10 | 17 | 50 | mA |
| | | | T2- G- | 10 | 18 | 50 | mA |
| | | | T2- G+ | 10 | 40 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 10 | 60 | mA |
| | | | T2+ G- | - | 25 | 90 | mA |
| | | | T2- G- | - | 12 | 60 | mA |
| | | | T2- G+ | - | 14 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 8 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 200 | 500 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

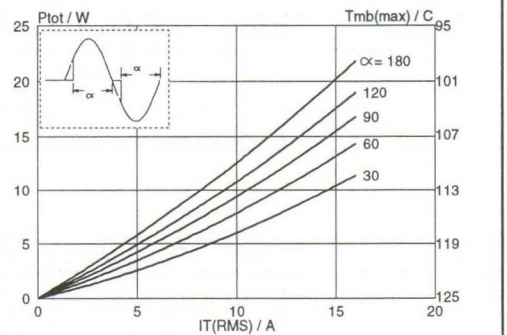



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

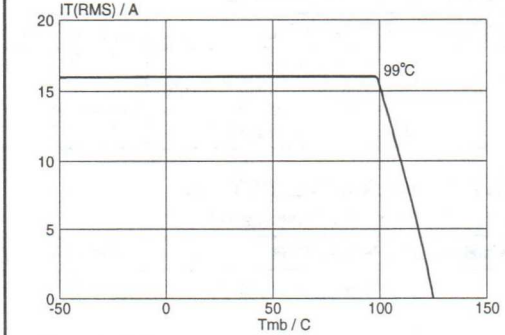



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

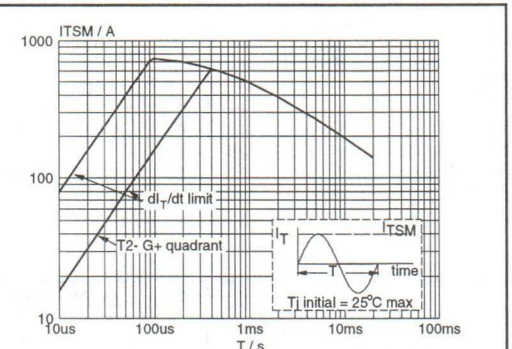



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

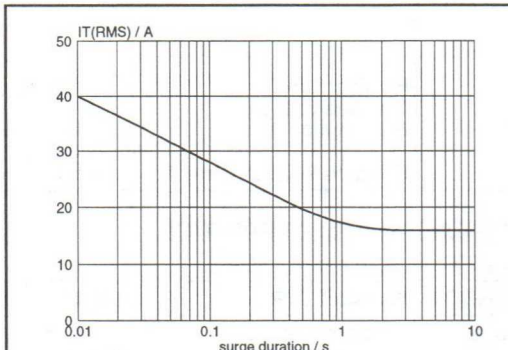



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

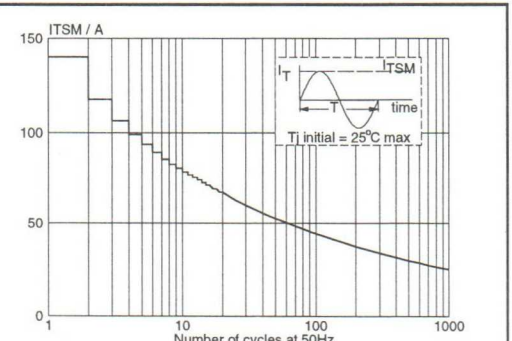



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

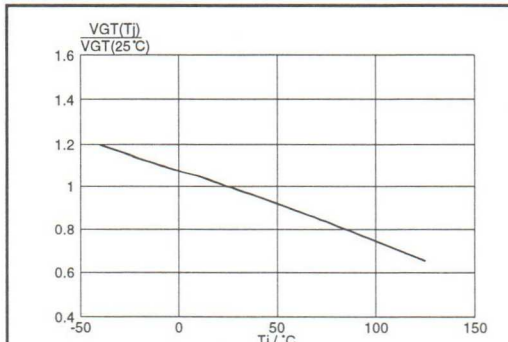



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

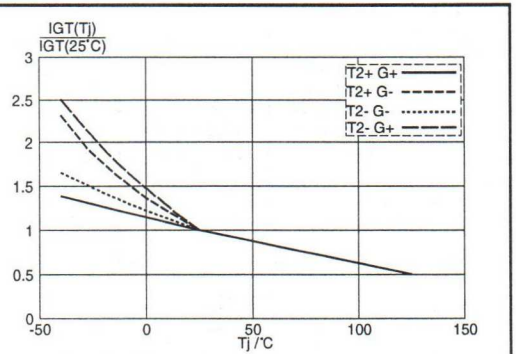



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

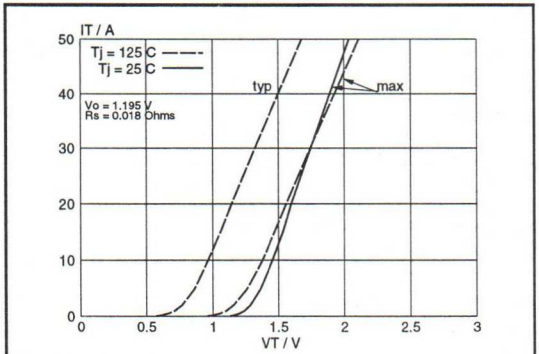



*Fig.10. Typical and maximum on-state characteristic.*

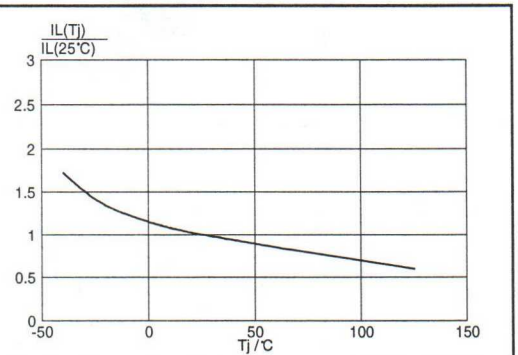



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

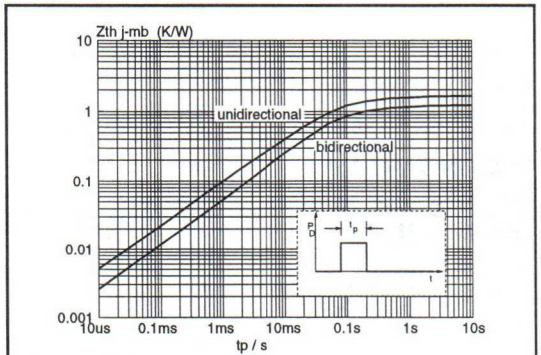



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

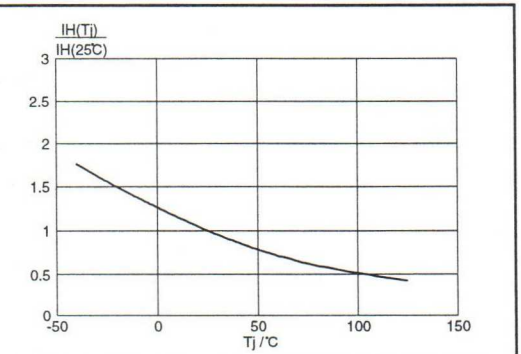



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

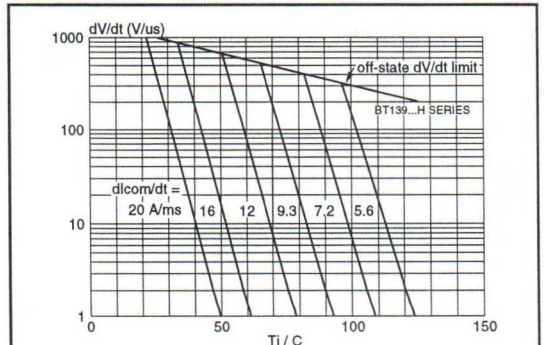



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

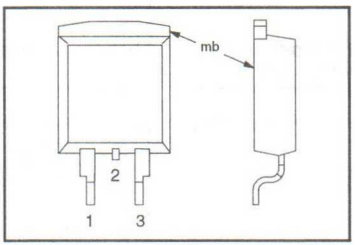
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT139B-** | **500** | **600** | **800** | |
| | **BT139B-** | **500F** | **600F** | **800F** | |
| | **BT139B-** | **500G** | **600G** | **800G** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

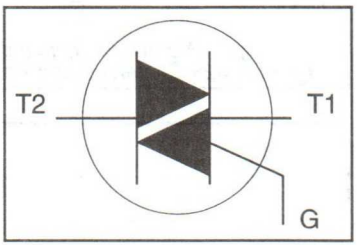
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139B- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | - | 1.2 | | 1.6 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139B- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

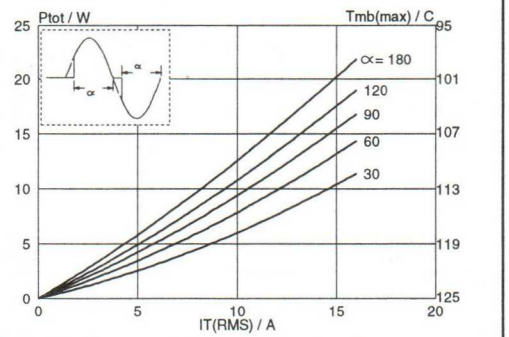



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

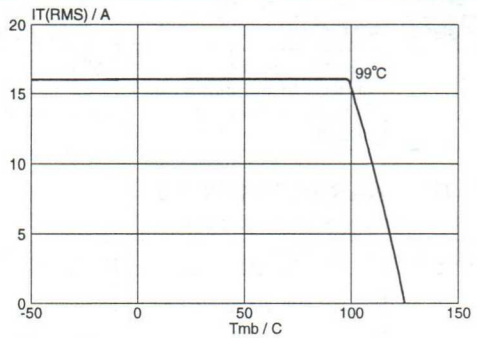



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

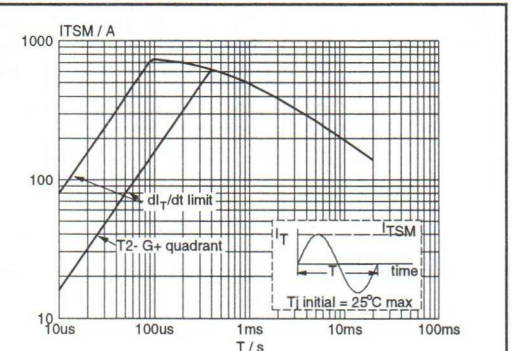



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

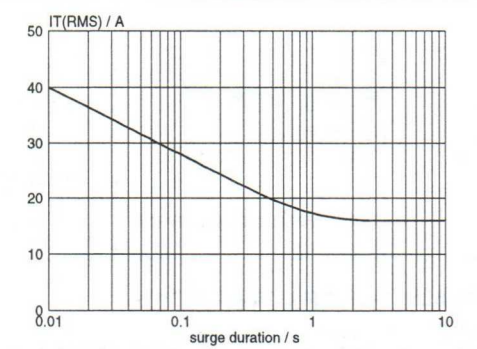



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

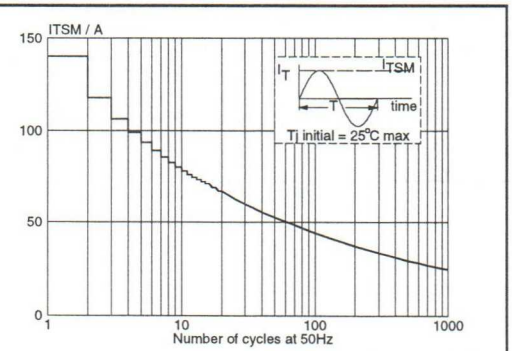



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*




*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

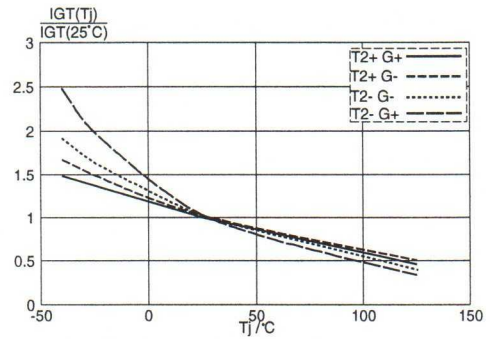



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

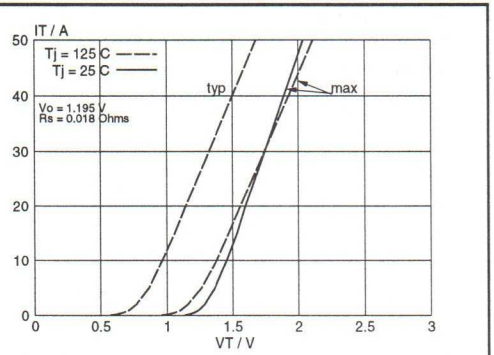



*Fig.10. Typical and maximum on-state characteristic.*

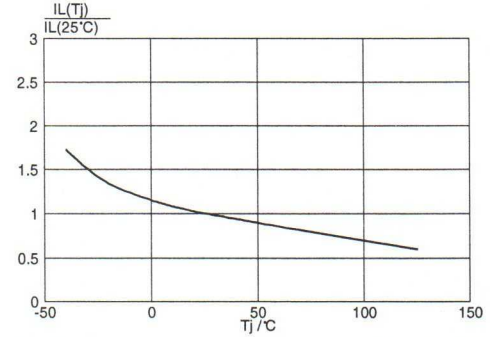



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

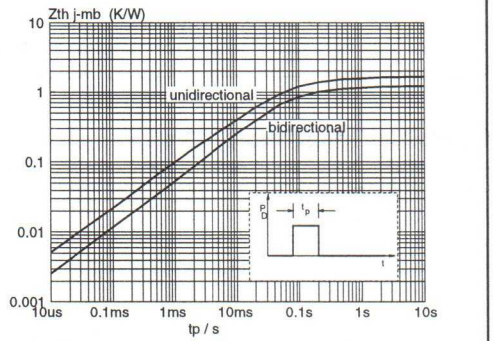



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

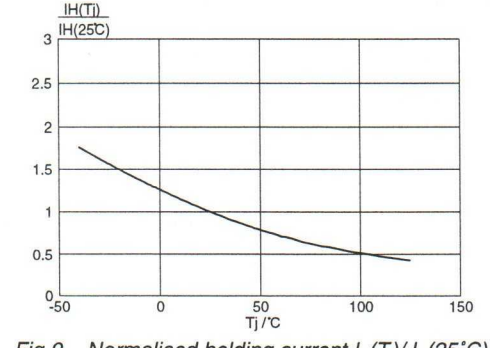



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

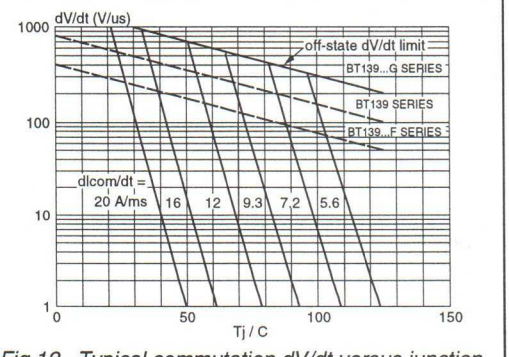



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

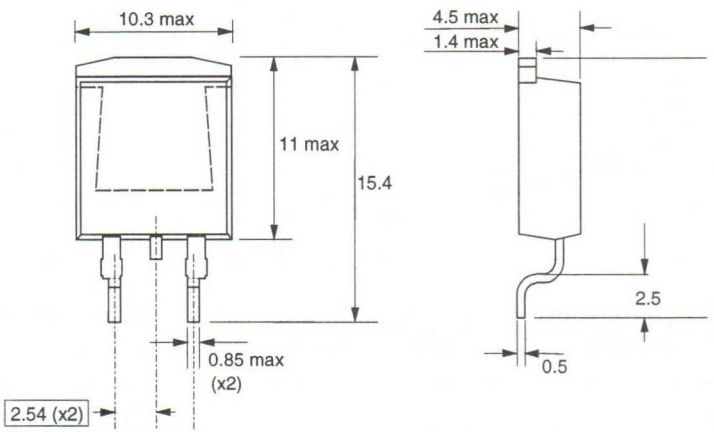



*Fig.13. SOT404 : centre pin connected to mounting base.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

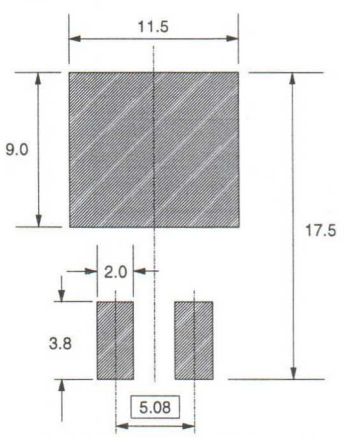



*Fig.14. SOT404 : soldering pattern for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Triacs sensitive gate

# BT139B series E

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

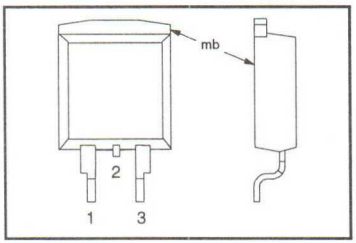
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139B- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

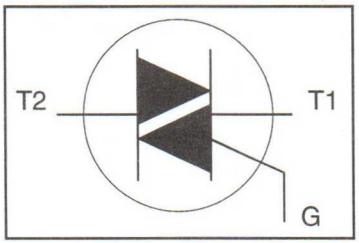
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

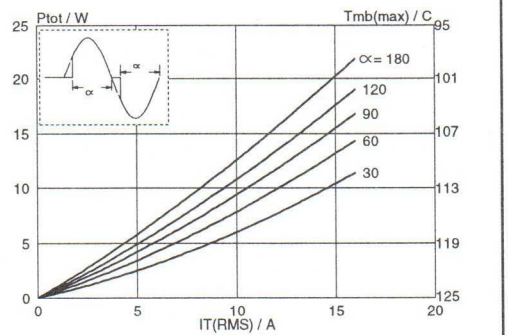



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

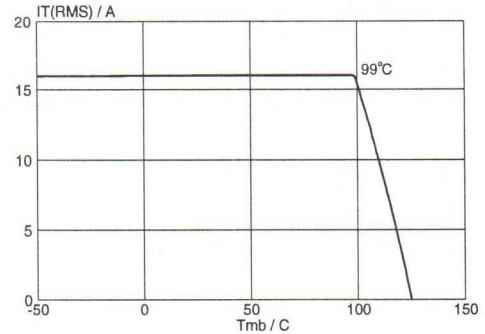



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

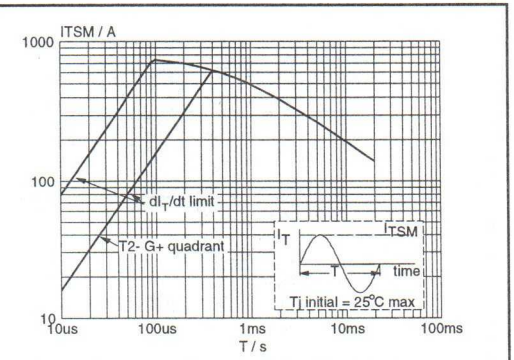



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

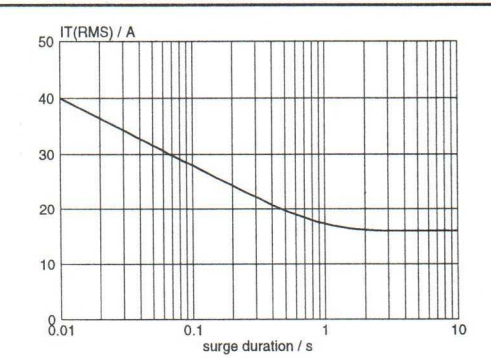



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

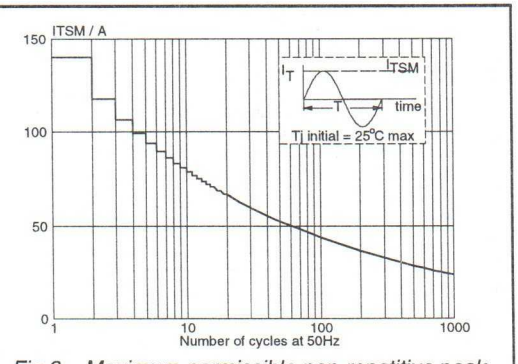



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

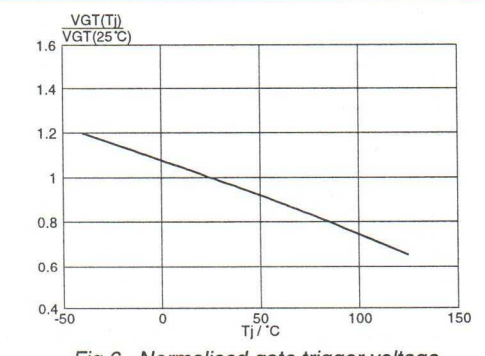



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

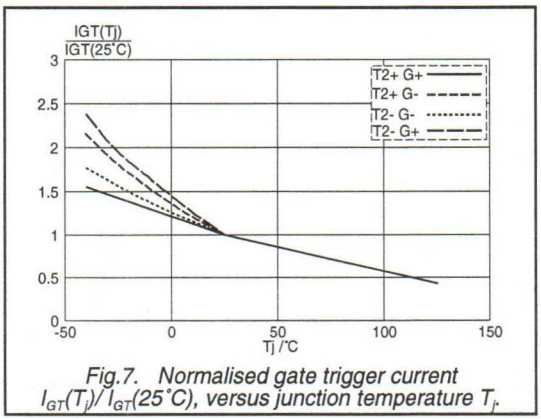



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

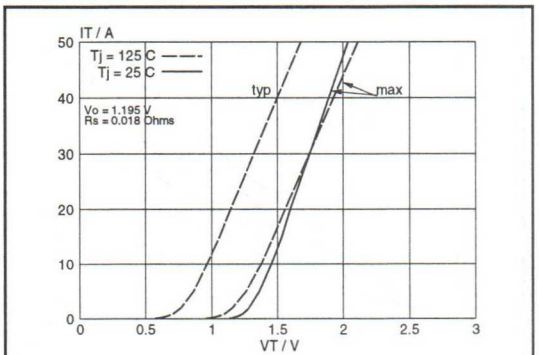



*Fig.10. Typical and maximum on-state characteristic.*

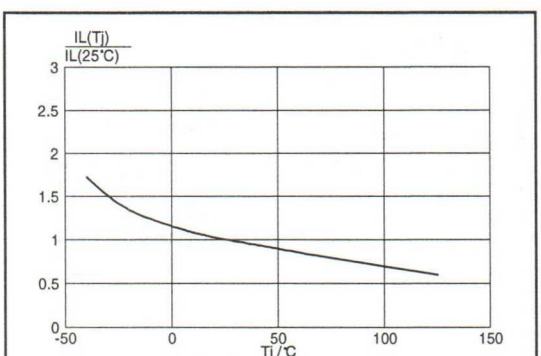



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

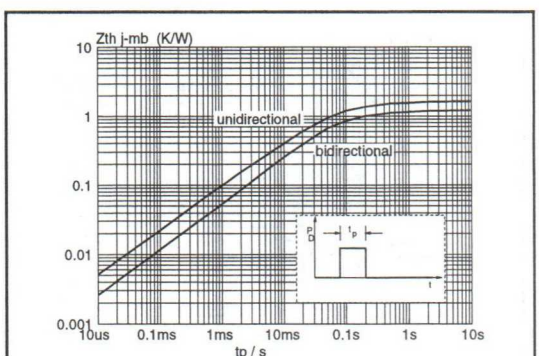



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

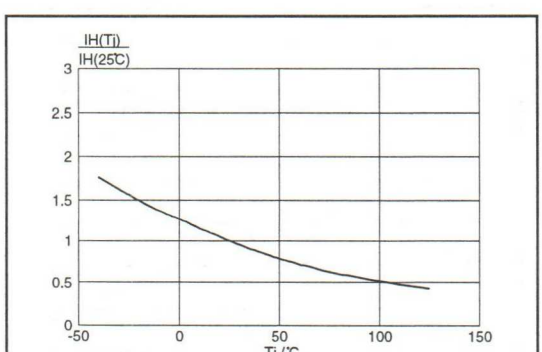



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

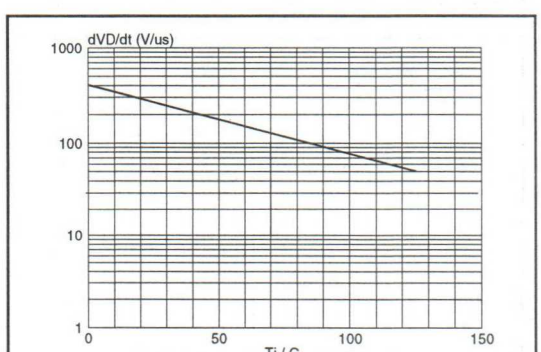



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

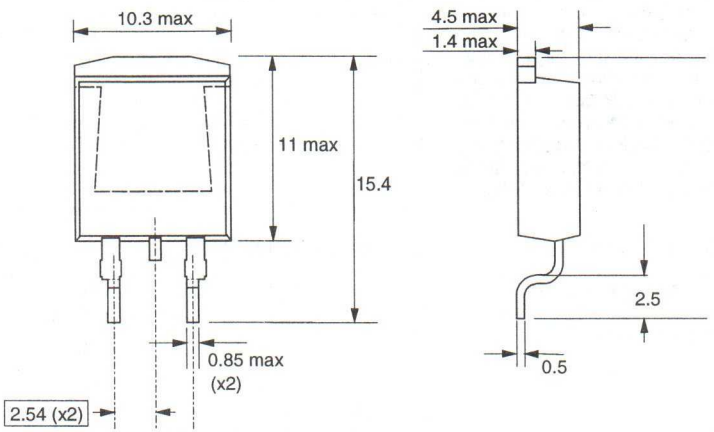



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

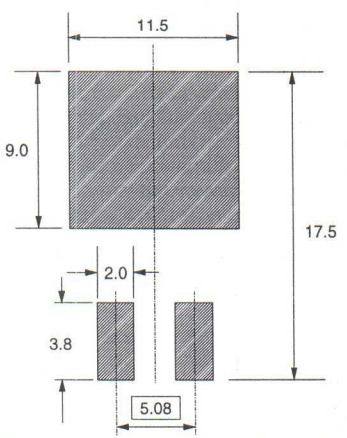



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Triacs high noise immunity

# BT139B series H

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

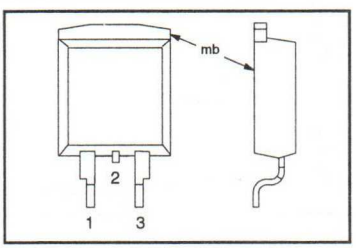
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139B- | 500H | 600H | 800H | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

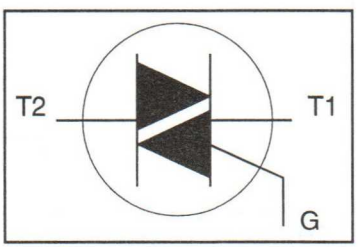
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 10 | 14 | 50 | mA |
| | | | T2+ G- | 10 | 17 | 50 | mA |
| | | | T2- G- | 10 | 18 | 50 | mA |
| | | | T2- G+ | 10 | 40 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 10 | 60 | mA |
| | | | T2+ G- | - | 25 | 90 | mA |
| | | | T2- G- | - | 12 | 60 | mA |
| | | | T2- G+ | - | 14 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 8 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 200 | 500 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

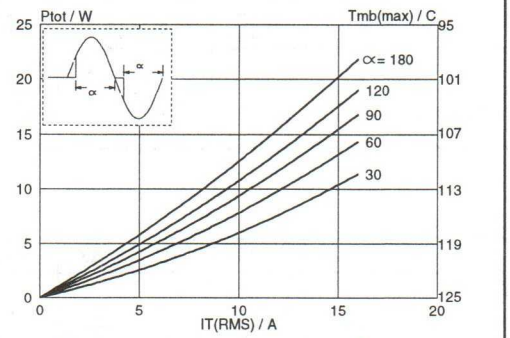



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

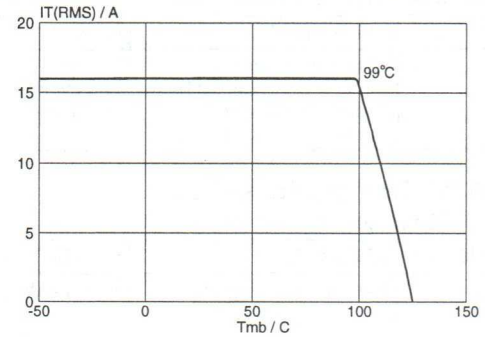



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

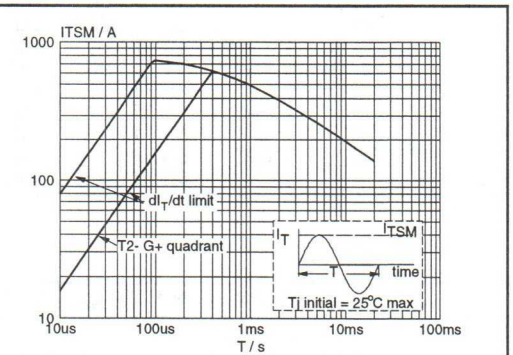



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

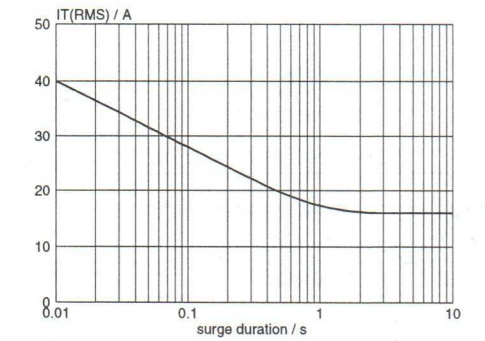



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

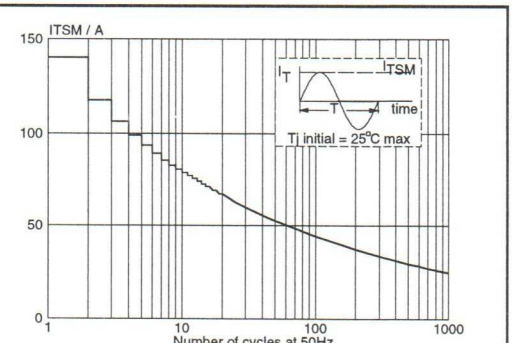



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

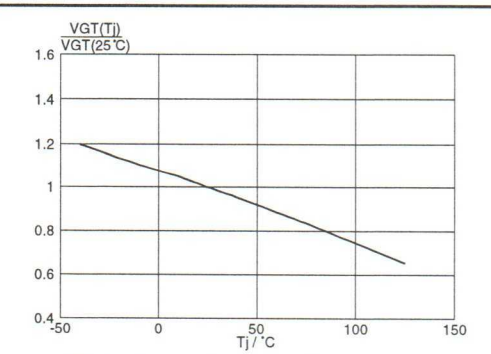



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

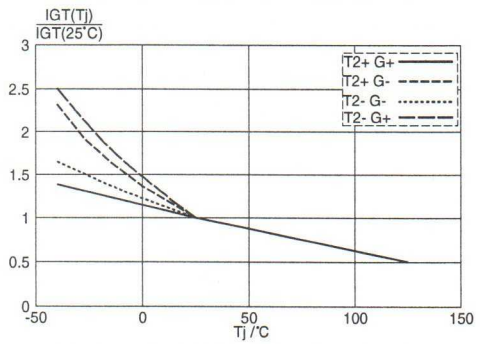



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

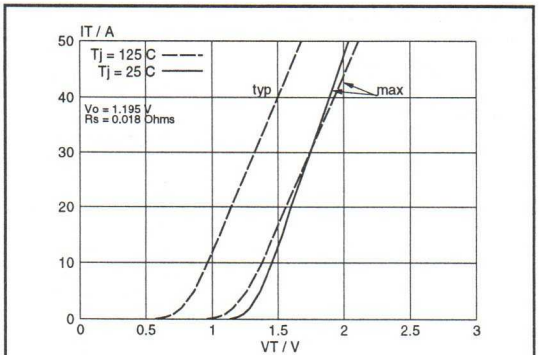



*Fig.10. Typical and maximum on-state characteristic.*

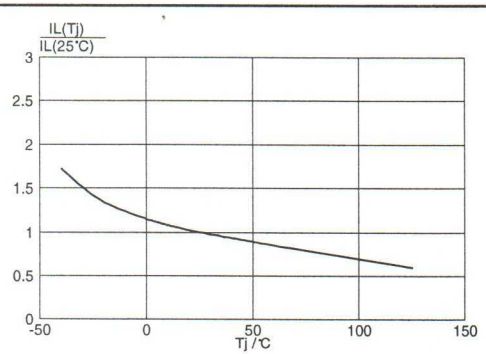



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

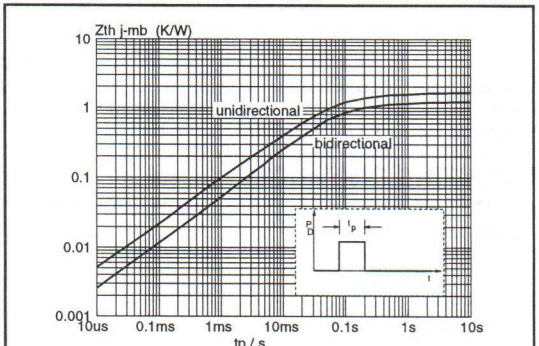



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

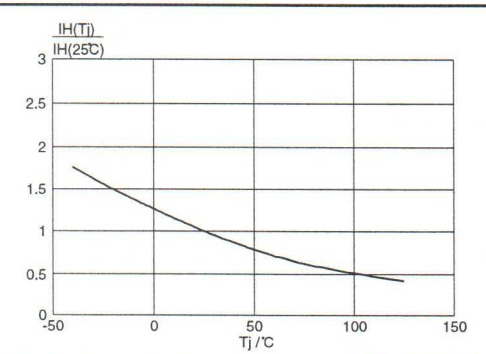



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

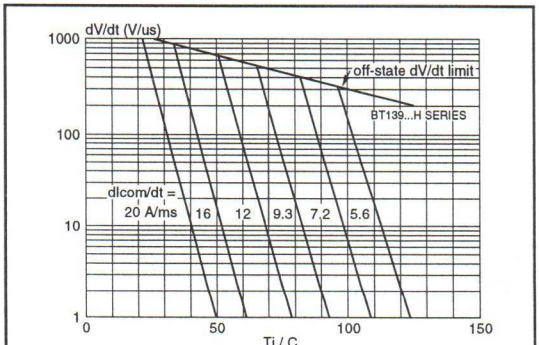



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

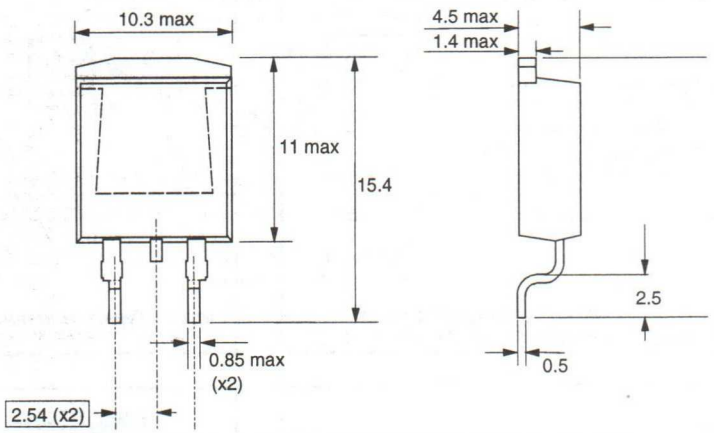



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

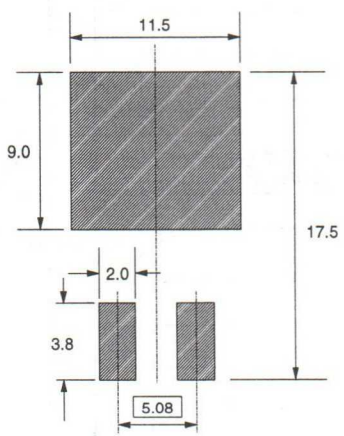



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

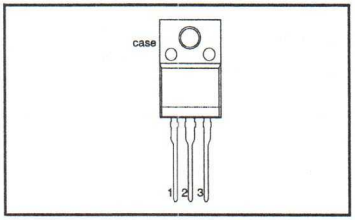
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | BT139X- 500 | 600 | 800 | |
| | | BT139X- 500F | 600F | 800F | |
| | | BT139X- 500G | 600G | 800G | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

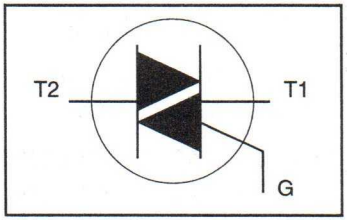
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 38$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139X- | | | ... | ...F | ...G | |
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 5 | 35 | 25 | 50 | mA |
| | | T2+ G- | - | 8 | 35 | 25 | 50 | mA |
| | | T2- G- | - | 10 | 35 | 25 | 50 | mA |
| | | T2- G+ | - | 22 | 70 | 70 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | 7 | 40 | 40 | 60 | mA |
| | | T2+ G- | - | 20 | 60 | 60 | 90 | mA |
| | | T2- G- | - | 8 | 40 | 40 | 60 | mA |
| | | T2- G+ | - | 10 | 60 | 60 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 6 | 30 | 30 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | - | 1.2 | | 1.6 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BT139X- | ... | ...F | ...G | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 50 | 200 | 250 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | - | - | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

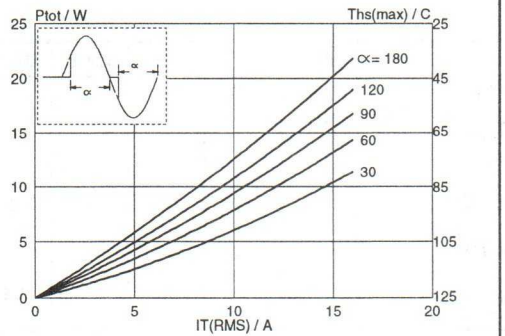



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

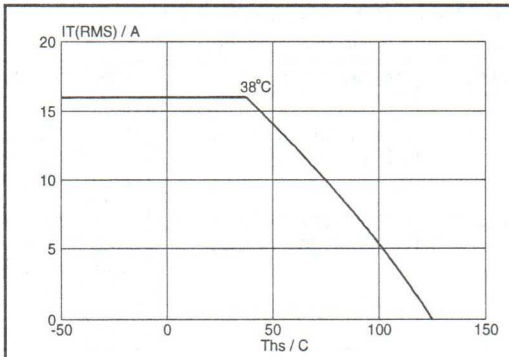



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

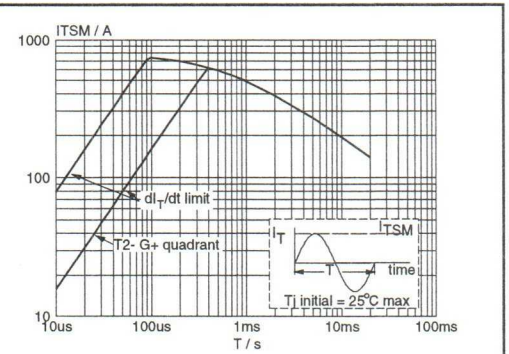



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

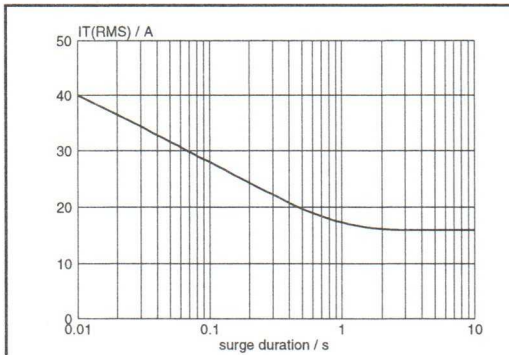



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38°C$.*

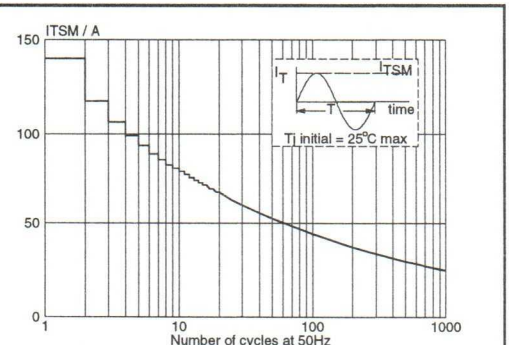



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

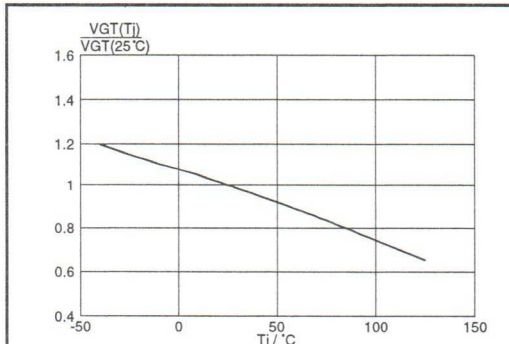



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

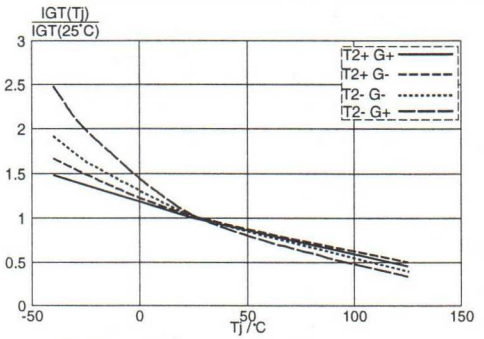



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

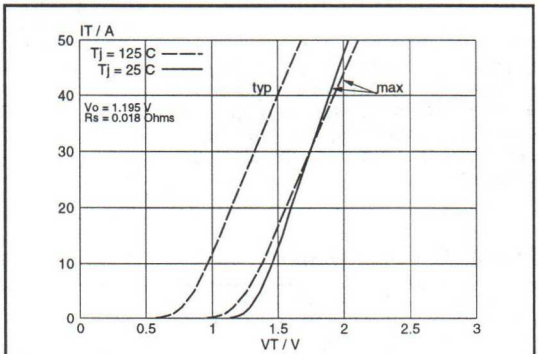



*Fig.10. Typical and maximum on-state characteristic.*

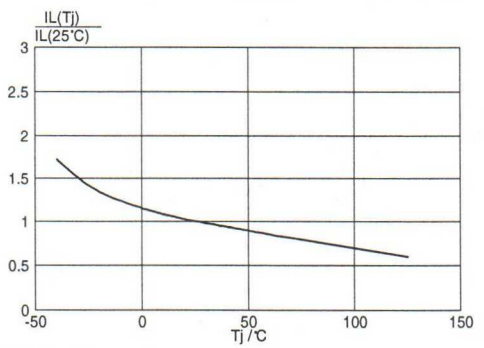



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

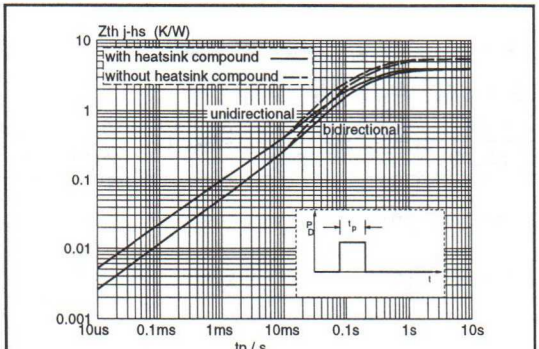



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

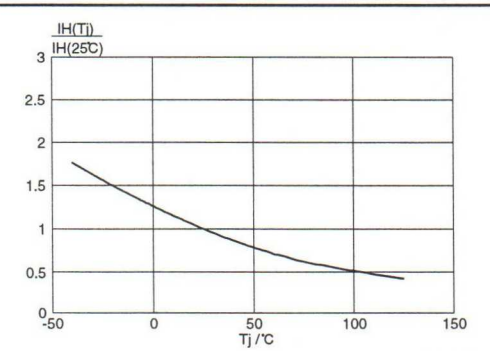



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

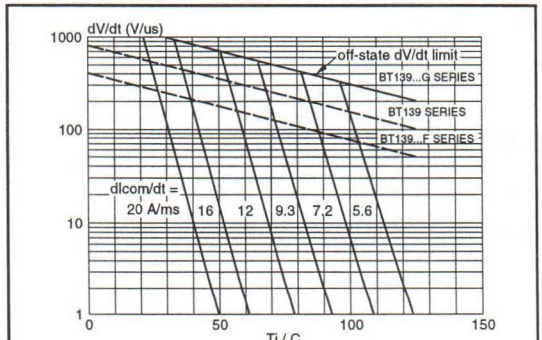



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

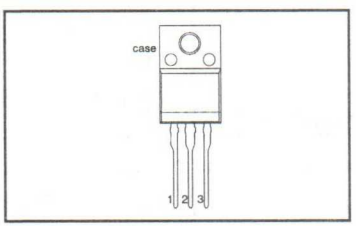
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139X- | 500E | 600E | 800E | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

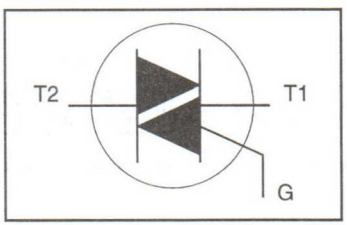
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 38$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle<br>with heatsink compound<br>without heatsink compound | -<br>- | -<br>- | 4.0<br>5.5 | K/W<br>K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 2.5 | 10 | mA |
| | | | T2+ G- | - | 4.0 | 10 | mA |
| | | | T2- G- | - | 5.0 | 10 | mA |
| | | | T2- G+ | - | 11 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 3.2 | 30 | mA |
| | | | T2+ G- | - | 16 | 40 | mA |
| | | | T2- G- | - | 4.0 | 30 | mA |
| | | | T2- G+ | - | 5.5 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 4.0 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

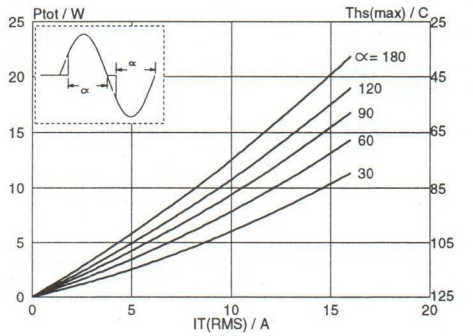



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

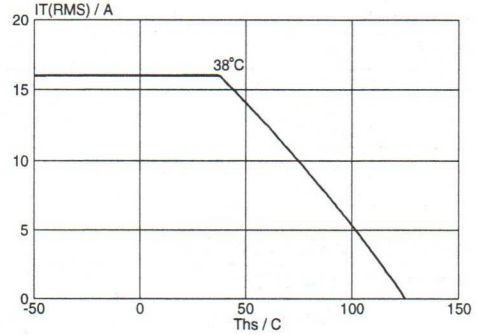



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

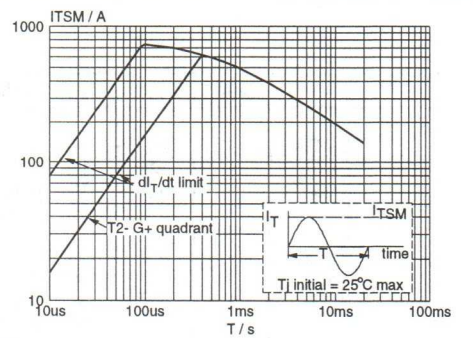



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

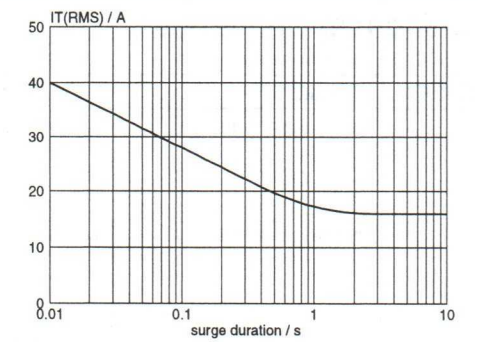



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38°C$.*

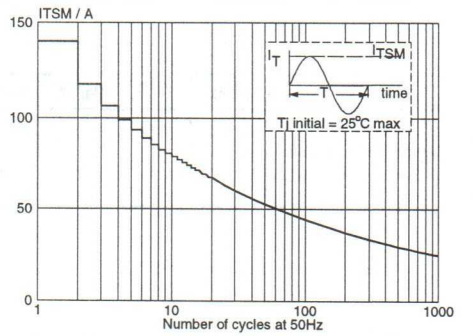



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*




*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

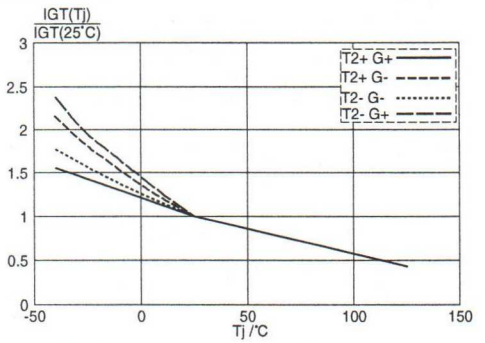



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

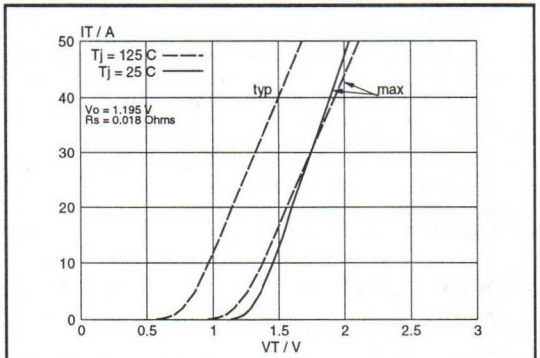



*Fig.10. Typical and maximum on-state characteristic.*

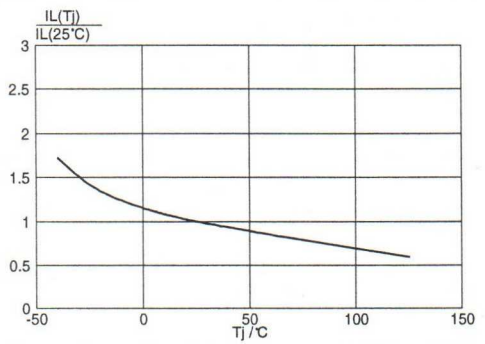



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

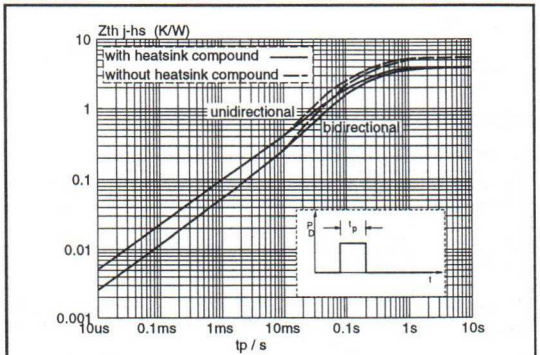



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

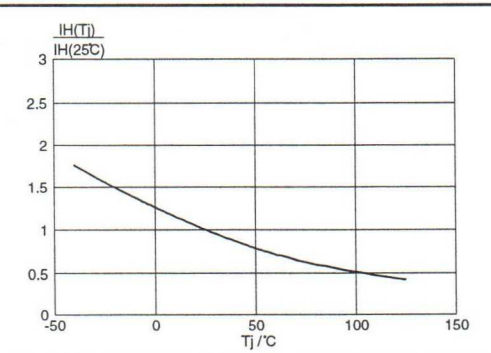



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

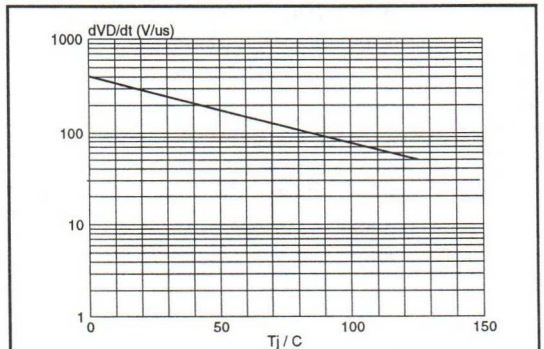



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Triacs high noise immunity

# BT139X series H

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

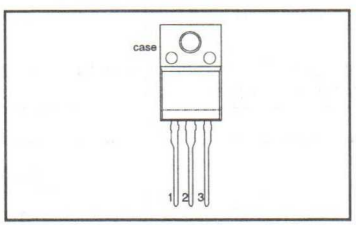
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139X- | 500H | 600H | 800H | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

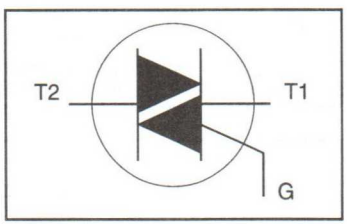
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 38$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | | 50 | | A/µs |
| | | T2+ G- | - | | 50 | | A/µs |
| | | T2- G- | - | | 50 | | A/µs |
| | | T2- G+ | - | | 10 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 10 | 14 | 50 | mA |
| | | | T2+ G- | 10 | 17 | 50 | mA |
| | | | T2- G- | 10 | 18 | 50 | mA |
| | | | T2- G+ | 10 | 40 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 10 | 60 | mA |
| | | | T2+ G- | - | 25 | 90 | mA |
| | | | T2- G- | - | 12 | 60 | mA |
| | | | T2- G+ | - | 14 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 8 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 200 | 500 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

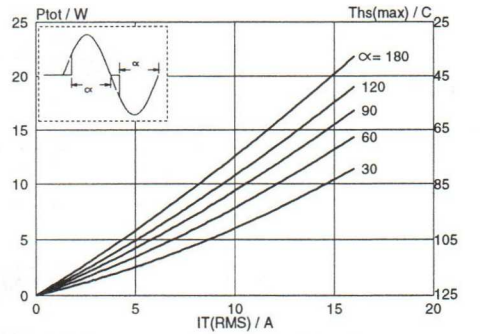



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

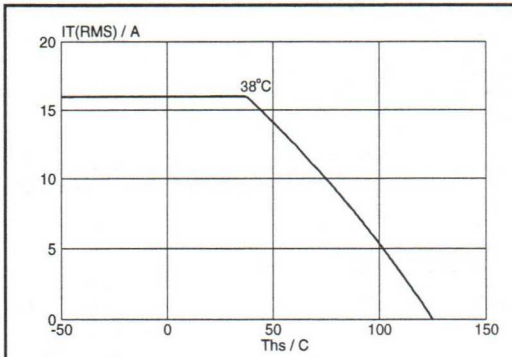



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

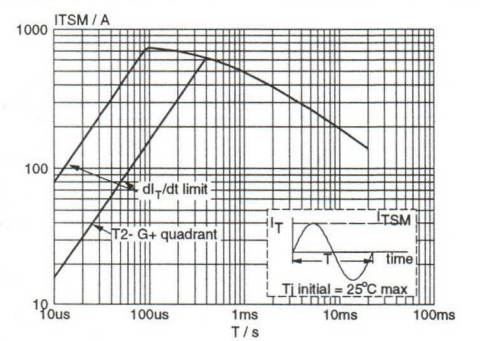



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

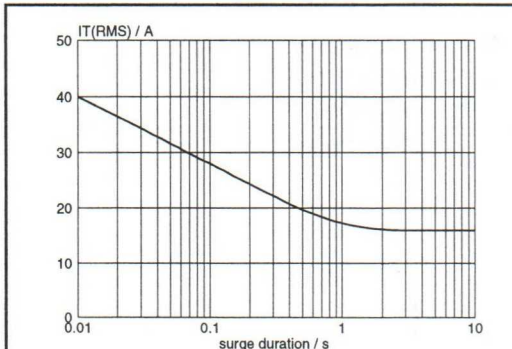



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38°C$.*

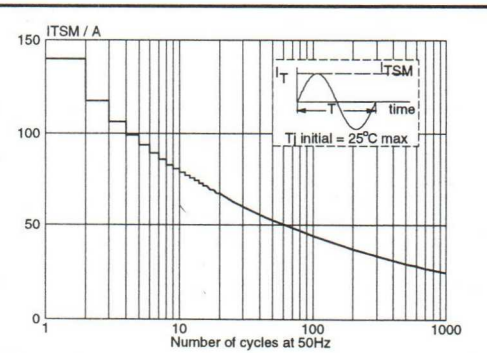



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

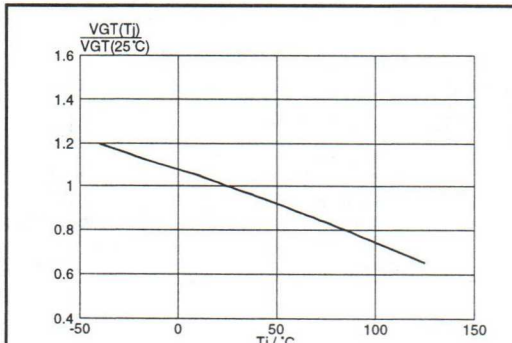



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

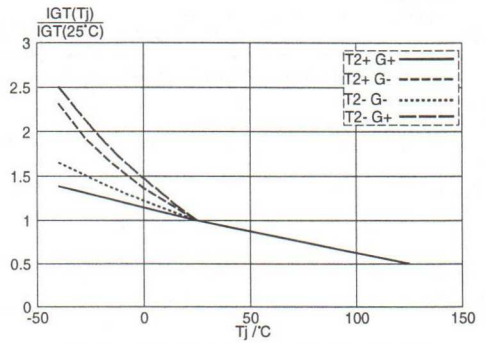



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

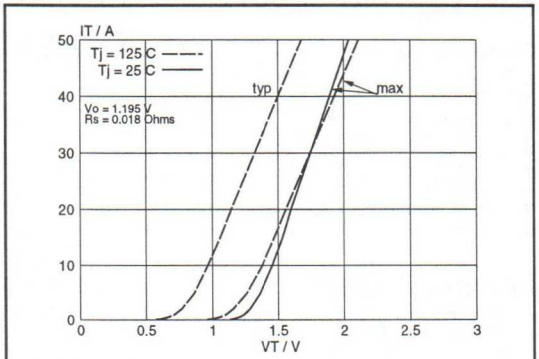



*Fig.10. Typical and maximum on-state characteristic.*

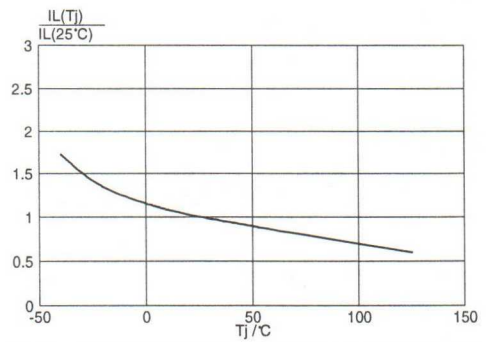



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

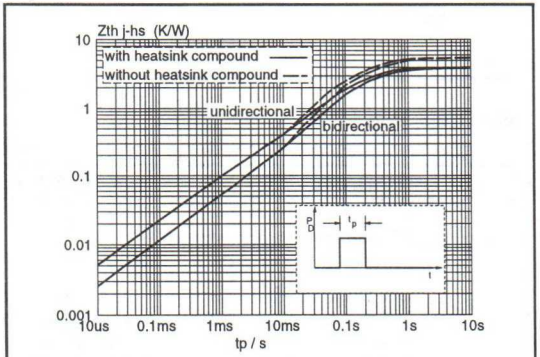



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

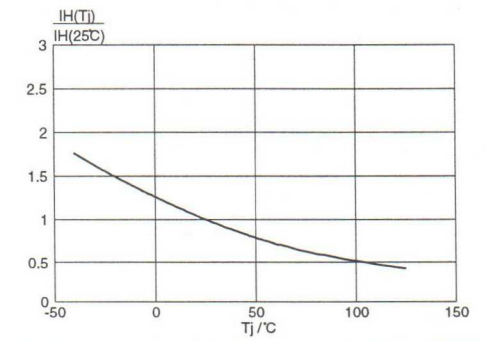



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

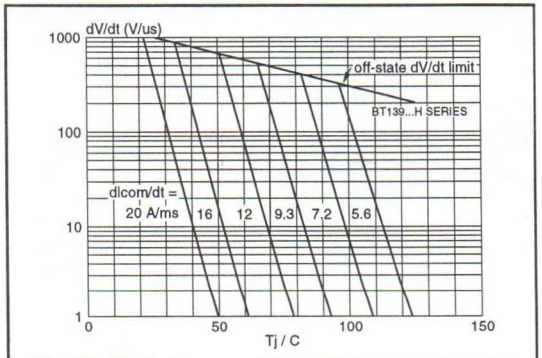



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

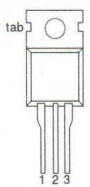
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT145- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 16 | 16 | 16 | A |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 300 | 300 | 300 | A |

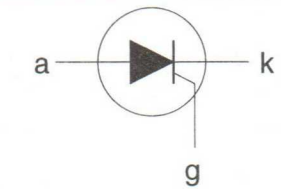
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 101$ °C | - | 16 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | 300 | | | A |
| | | t = 8.3 ms | - | 330 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 450 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 50 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | - | 200 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 5 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 20 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 5 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 25 | 80 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 20 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | - | 1.1 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.0 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.2 | 1.0 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 200 | 500 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 50 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs | - | 70 | - | µs |

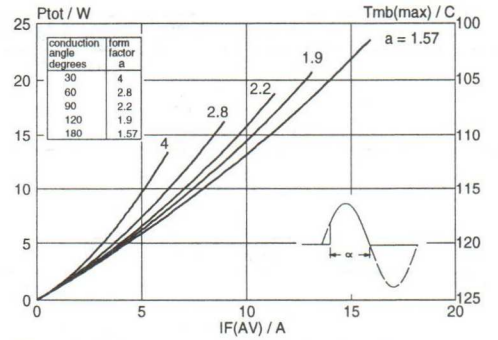



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

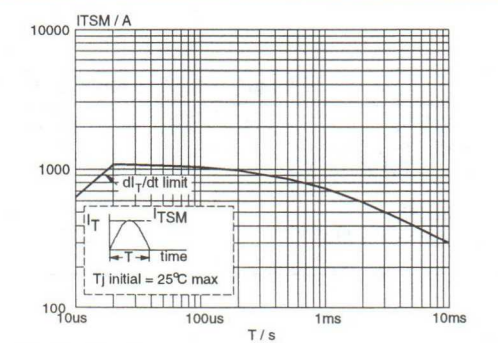



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

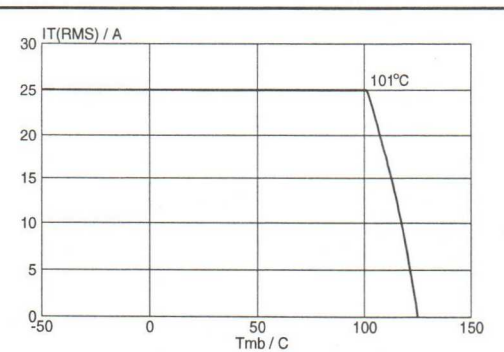



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

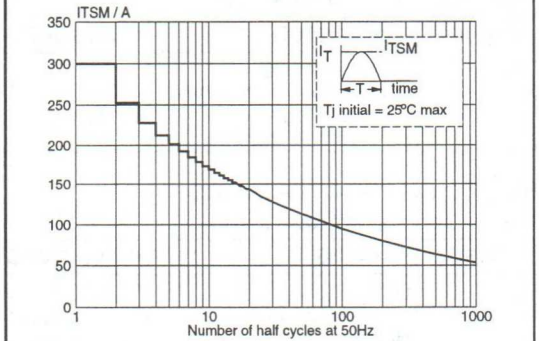



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

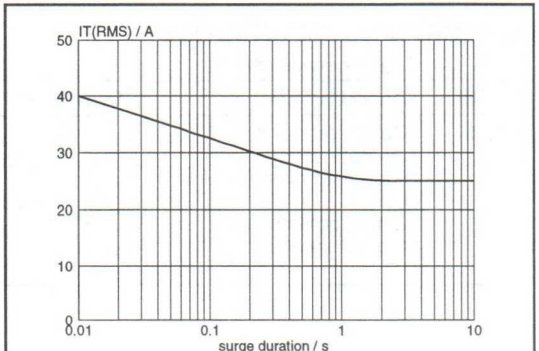



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 101°C$.*

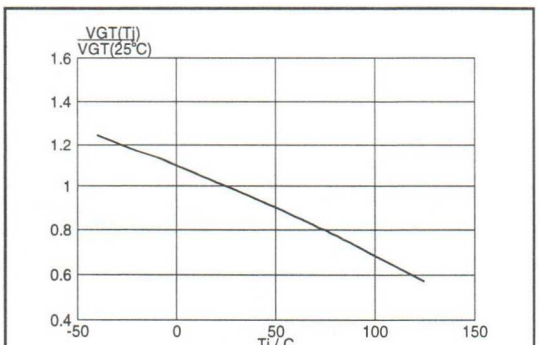



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

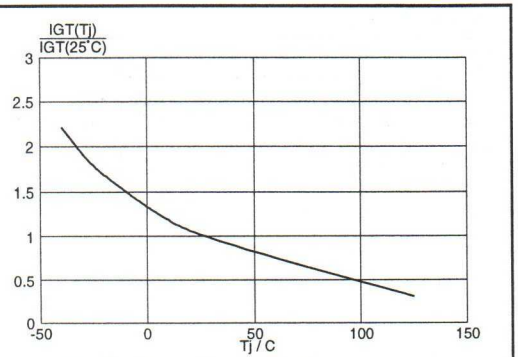



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

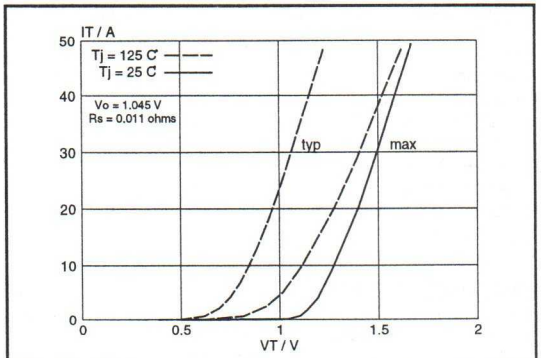



*Fig.10. Typical and maximum on-state characteristic.*

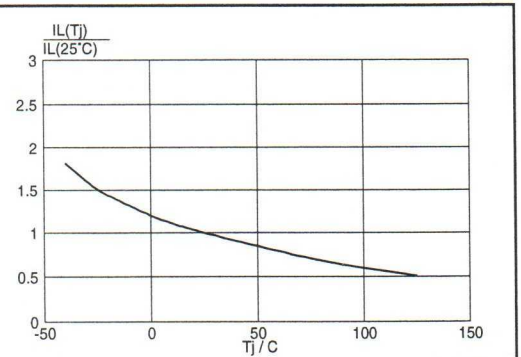



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

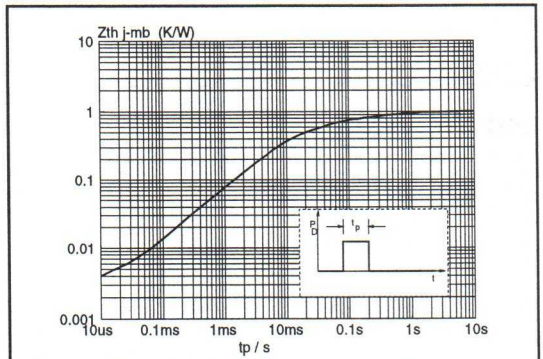



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

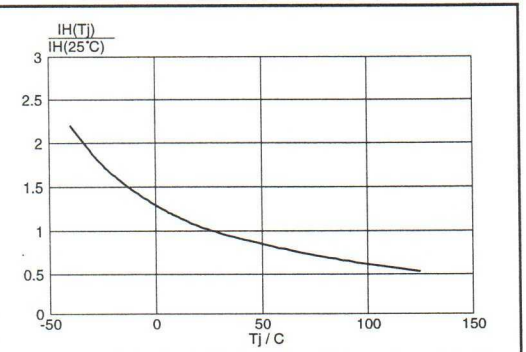



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

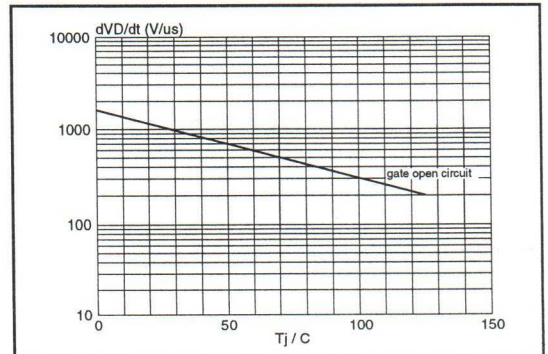



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

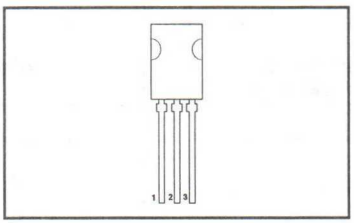
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT148- | 400R | 500R | 600R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 2.5 | 2.5 | 2.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 35 | 35 | 35 | A |

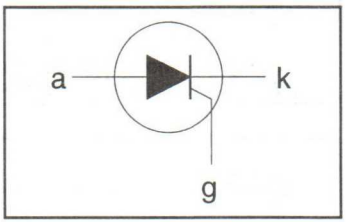
## PINNING - SOT82

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -400R | -500R | -600R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 113$ °C | - | | 2.5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 35 | | A |
| | | t = 8.3 ms | - | | 38 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 6.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 2.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 95 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 15 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.17 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.10 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.23 | 1.8 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 8 A; $V_R$ = 10 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

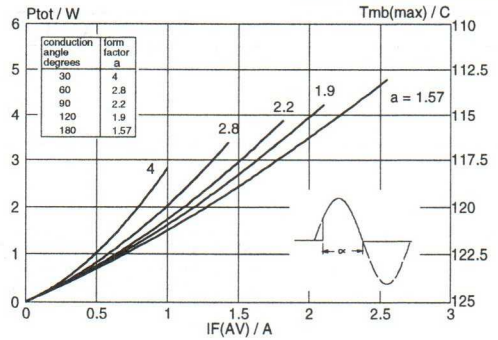



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

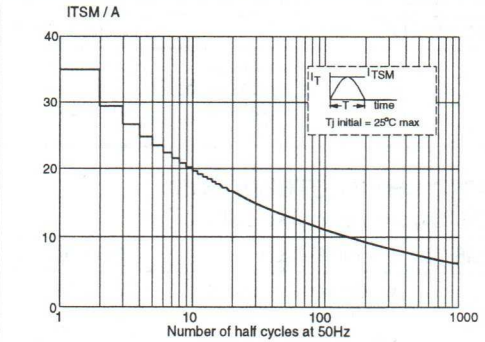



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

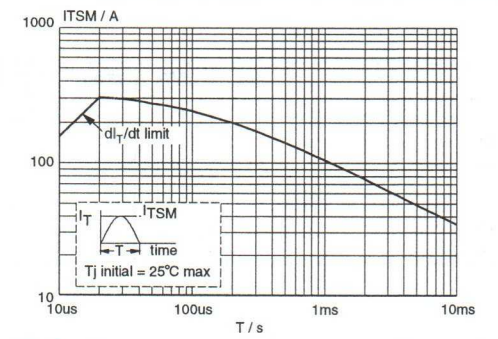



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

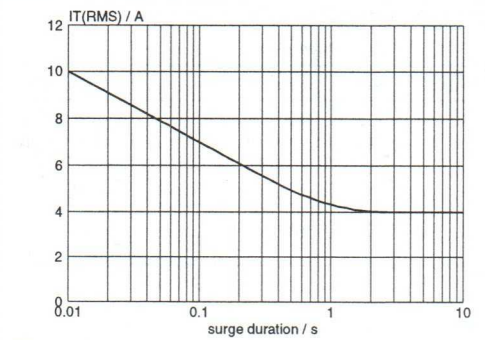



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 113°C$.*

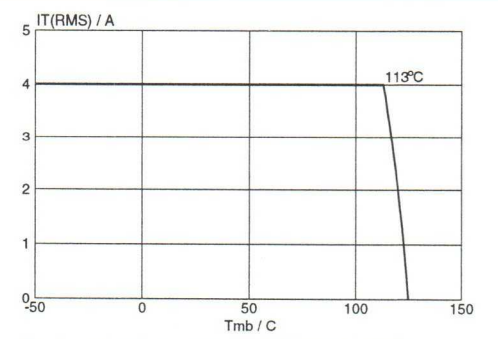



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

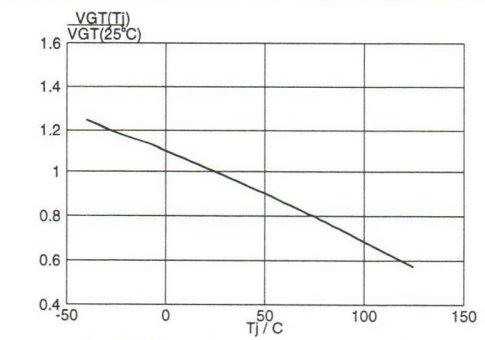



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

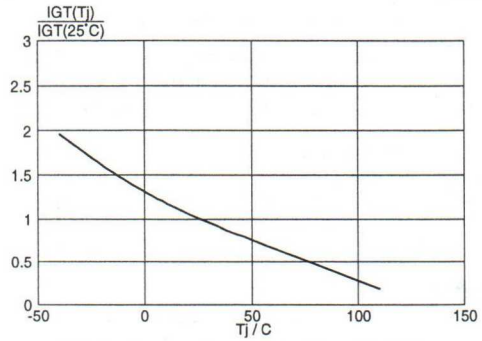



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

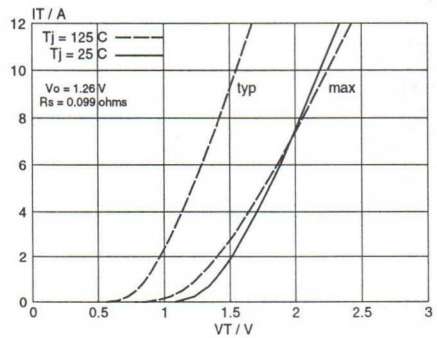



*Fig.10. Typical and maximum on-state characteristic.*

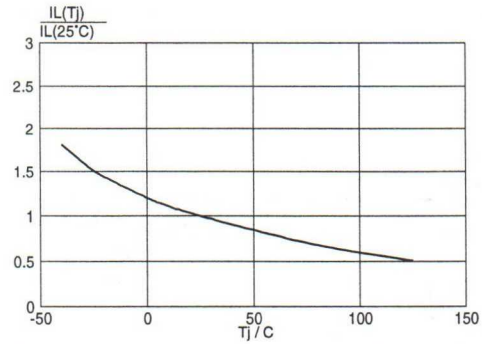



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

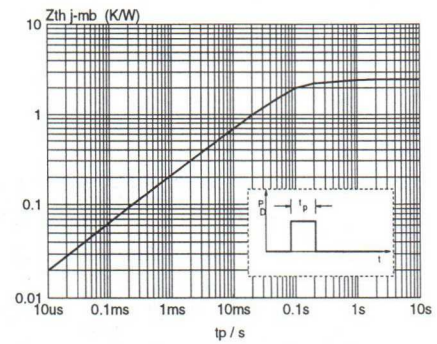



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

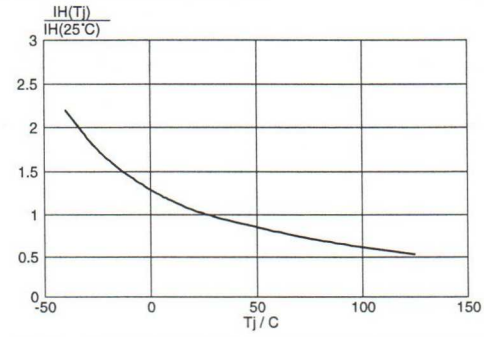



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

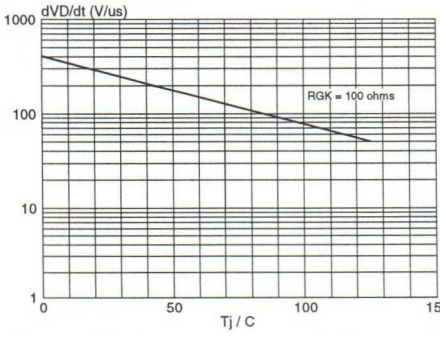



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Thyristors logic level

# BT148S-600Z
BT148M-600Z

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristor in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices feature a gate-cathode reverse breakdown voltage specification. They can be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

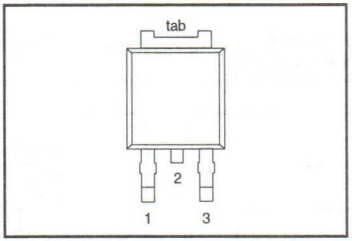
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|---|---|---|---|
| | **BT148S** (or BT148M)- | **600Z** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltage | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 2.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 35 | A |

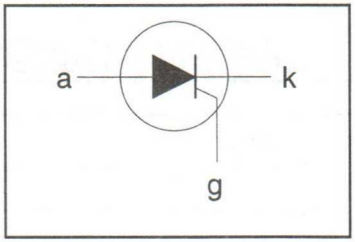
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | cathode | gate |
| 2 | anode | anode |
| 3 | gate | cathode |
| tab | anode | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltage | | - | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | 2.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | |
| | | t = 10 ms | - | 35 | A |
| | | t = 8.3 ms | - | 38 | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 6.1 | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | 50 | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | A |
| $P_{GM}$ | Peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | °C |
| $T_j$ | Operating junction temperature | | - | 125[2] | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 3.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 15 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.17 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.10 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.23 | 1.8 | V |
| $V_{GR}$ | Gate-cathode reverse breakdown voltage | $I_G$ = -20 µA | 14 | - | - | V |
| | | $I_G$ = -150 µA | - | - | 20 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D$ = $V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $V_R$ = $V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 8 A; $V_R$ = 10 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

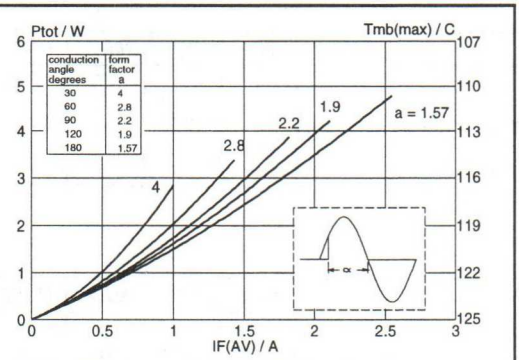



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

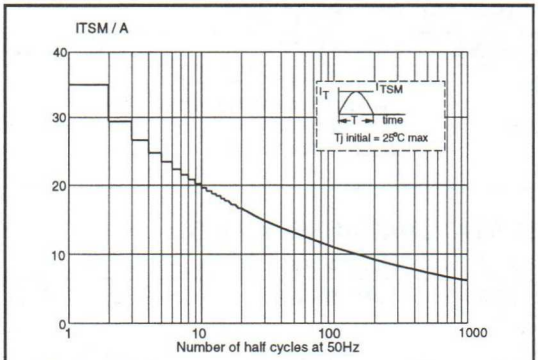



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

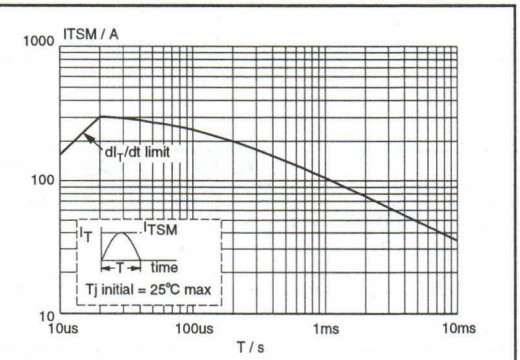



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

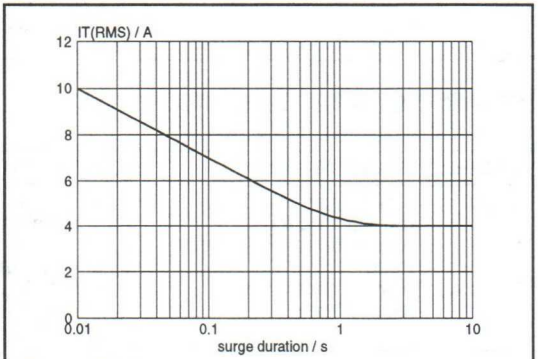



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

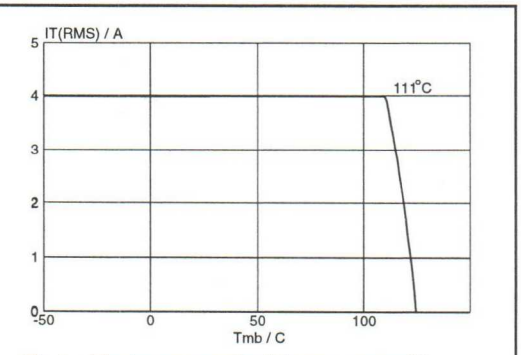



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

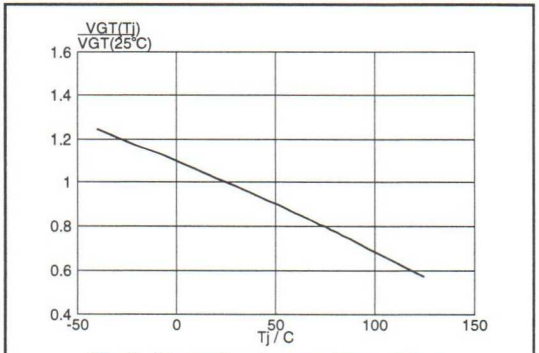



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

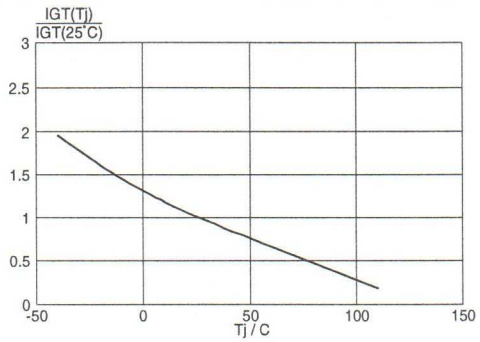



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

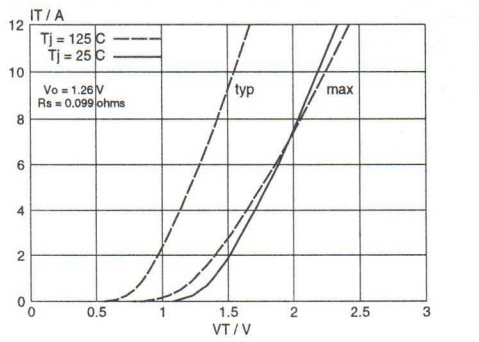



*Fig.10. Typical and maximum on-state characteristic.*

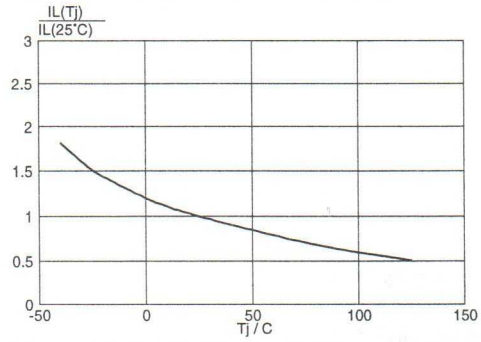



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

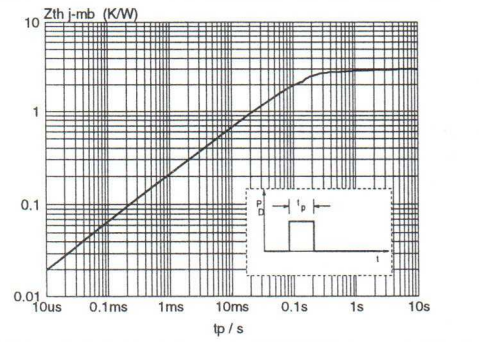



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

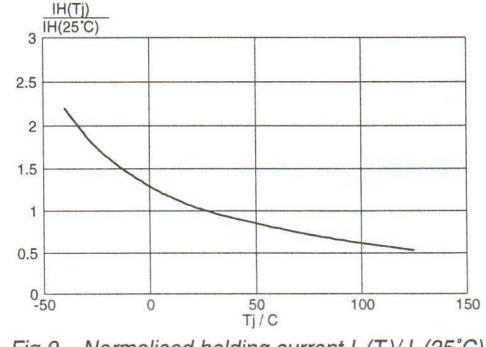



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

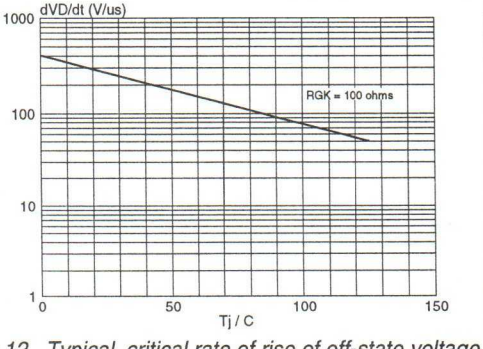



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

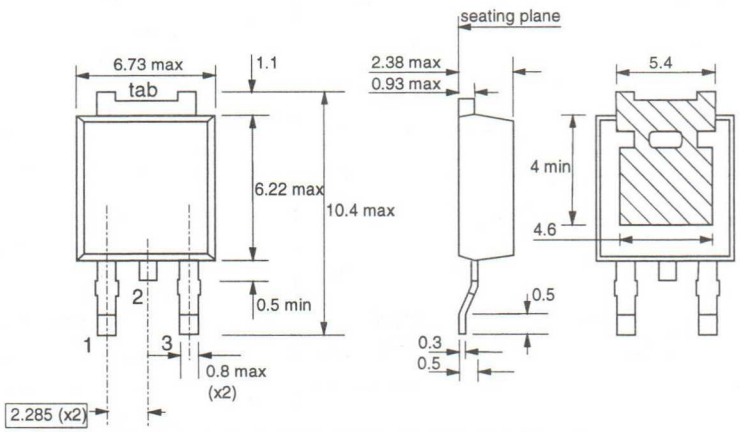



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

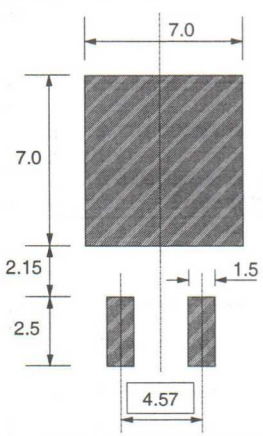



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Thyristors logic level

# BT148W series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

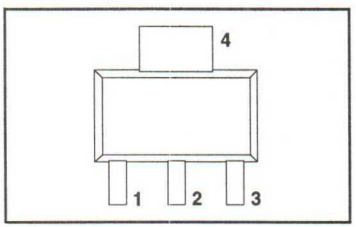
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT148W- | 400R | 500R | 600R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.6 | 0.6 | 0.6 | A |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | 10 | A |

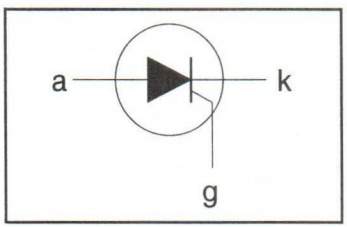
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -400R | -500R | -600R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{sp} \leq 112$ °C | - | | 0.6 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 10 | | A |
| | | t = 8.3 ms | - | | 11 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 0.5 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 4 A; $I_G$ = 200 mA; $dI_G/dt$ = 200 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 1 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 1.2 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.12 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted, minimum footprint | - | 156 | - | K/W |
| | | pcb mounted, pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.17 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.10 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.3 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_R = V_{RRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 4 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 2 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

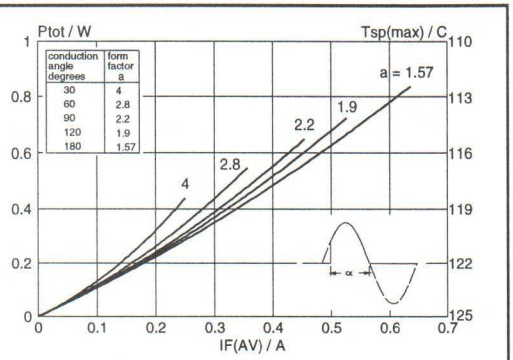



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

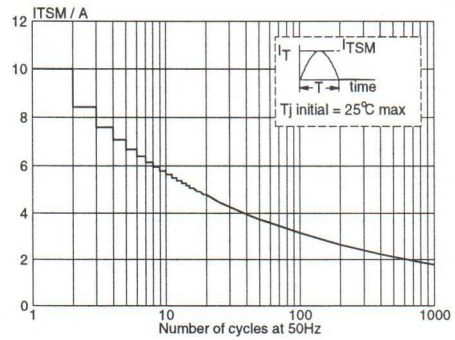



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

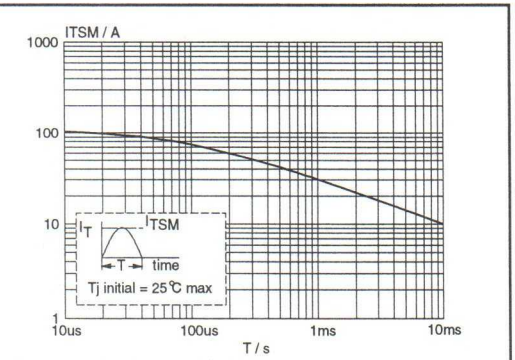



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

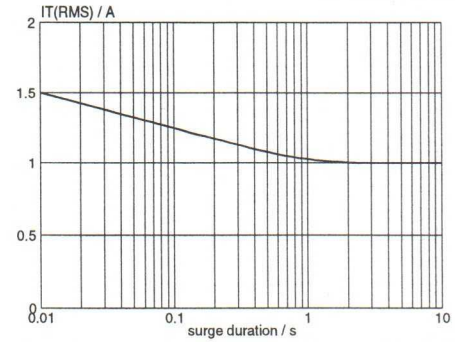



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 112°C$.*

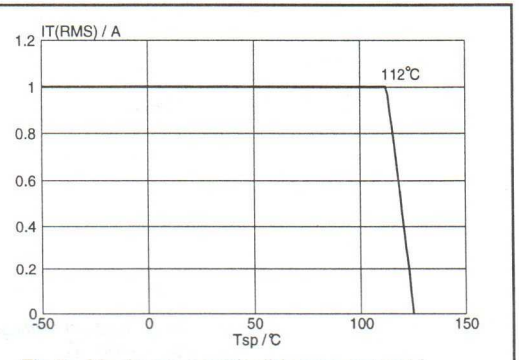



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

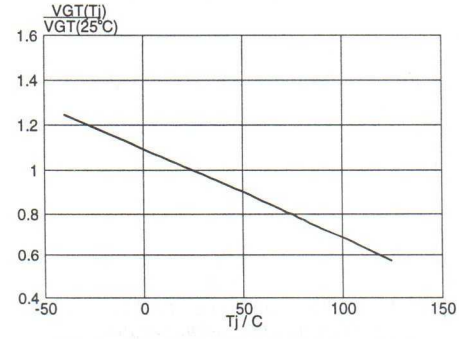



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

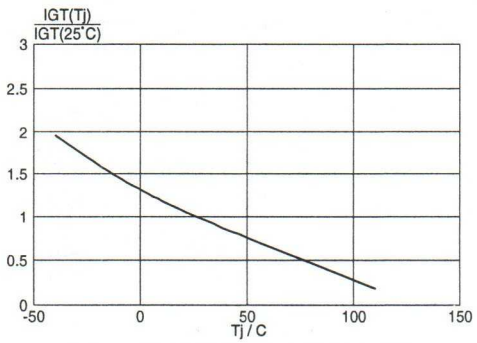



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

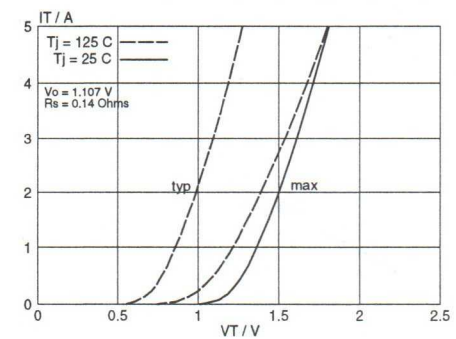



*Fig.10. Typical and maximum on-state characteristic.*

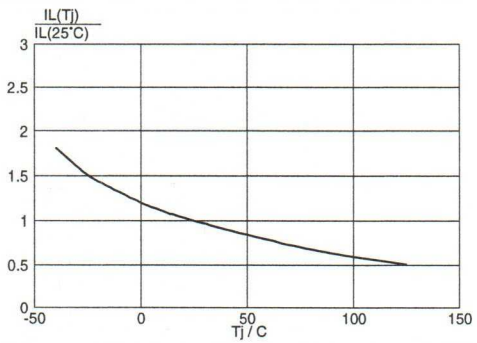



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

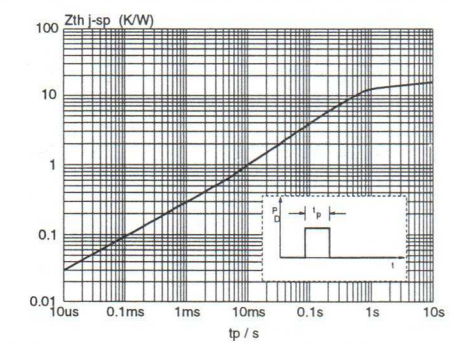



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width $t_p$.*

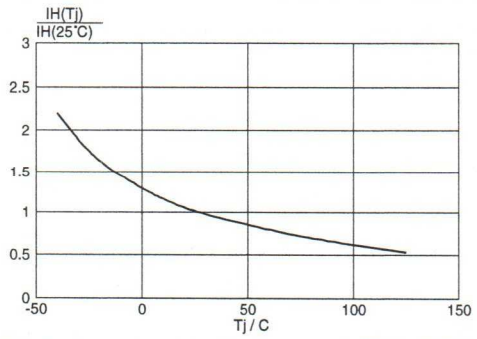



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

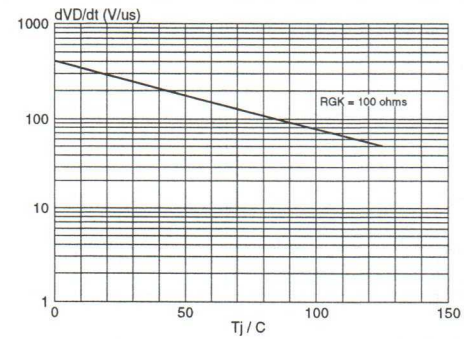



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

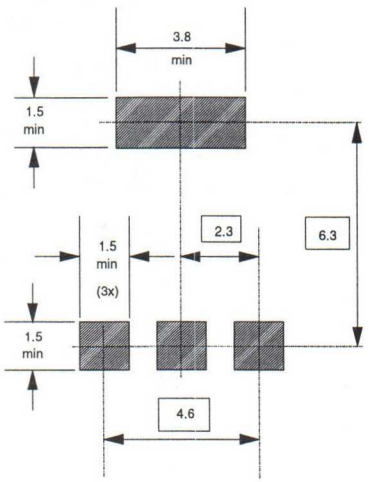



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

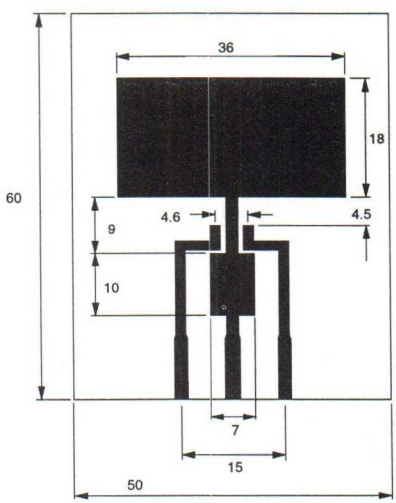



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).*

# Thyristors logic level

# BT149 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

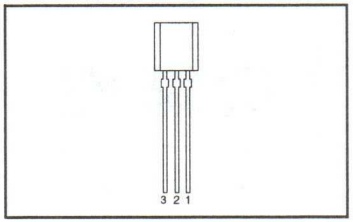
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | BT149 | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.5 | 0.5 | 0.5 | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 0.8 | 0.8 | 0.8 | 0.8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 8 | 8 | 8 | 8 | A |

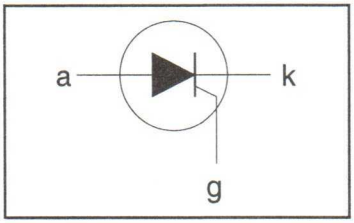
## PINNING - TO92 variant

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | gate |
| 3 | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200[1] | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{lead} \leq 83$ °C | - | 0.5 | | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 0.8 | | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | t = 10 ms | - | 8 | | | | A |
| | | t = 8.3 ms | - | 9 | | | | A |
| | | half sine wave; $T_j$ = 25 °C prior to surge | | | | | | |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.32 | | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 2 A; $I_G$ = 10 mA; $dI_G/dt$ = 100 mA/µs | - | 50 | | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 1 | | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | | V |
| $P_{GM}$ | Peak gate power | | - | 2 | | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.1 | | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to lead | | - | - | 60 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; lead length = 4mm | - | 150 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 1 A | - | 1.2 | 1.35 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 0.5 | 0.8 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 10 mA; $T_j$ = 125 °C; gate open circuit | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

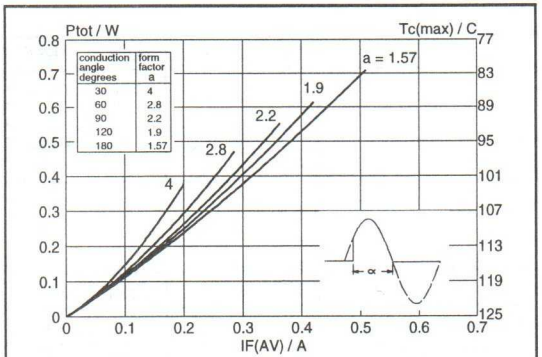



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

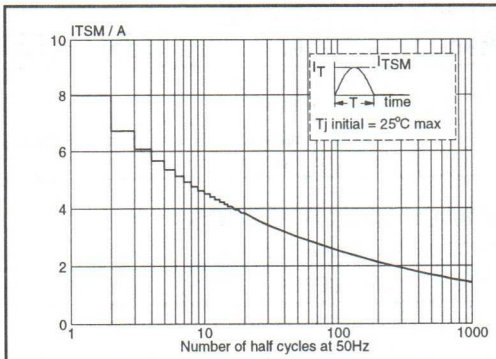



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

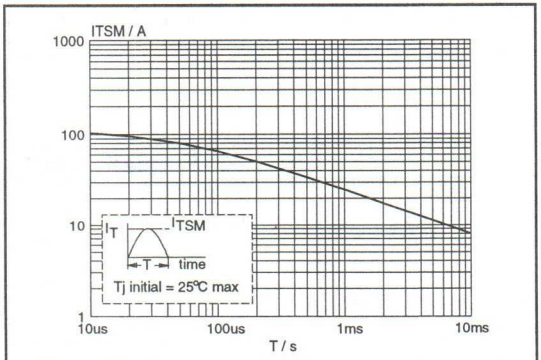



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

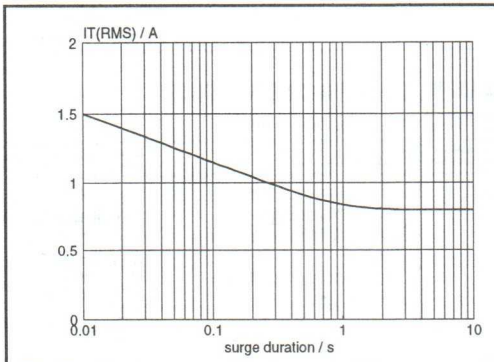



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 83°C$.*

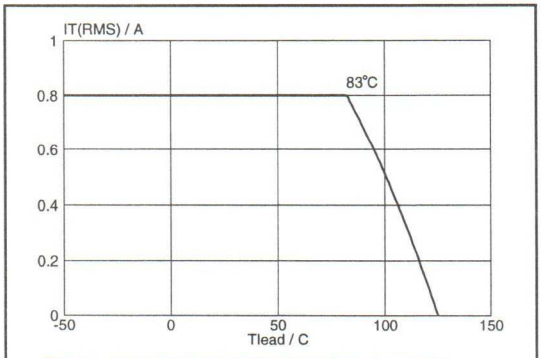



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, $T_{lead}$.*

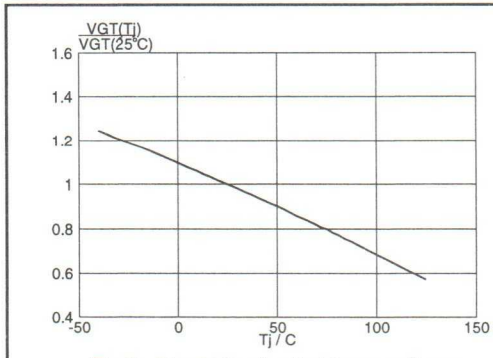



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

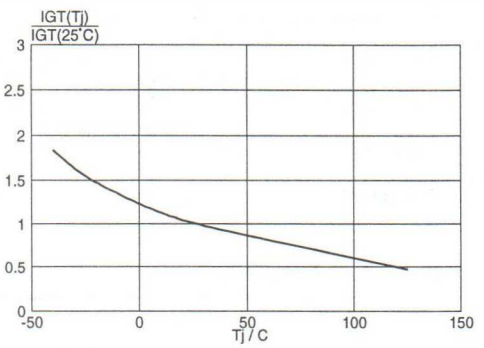



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

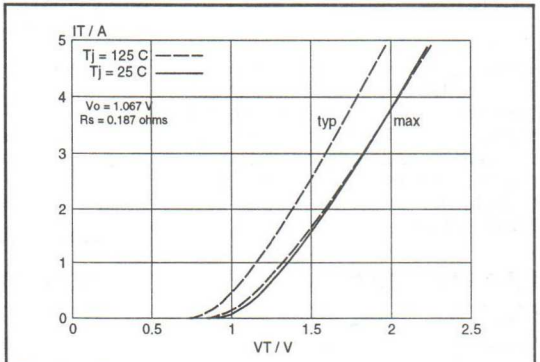



*Fig.10. Typical and maximum on-state characteristic.*

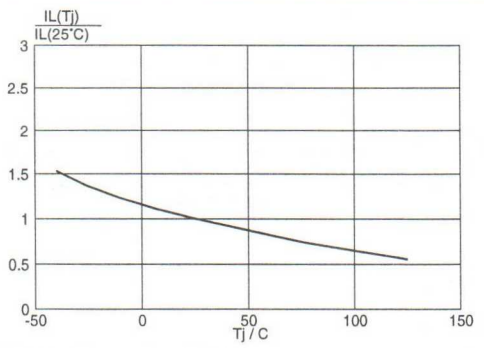



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

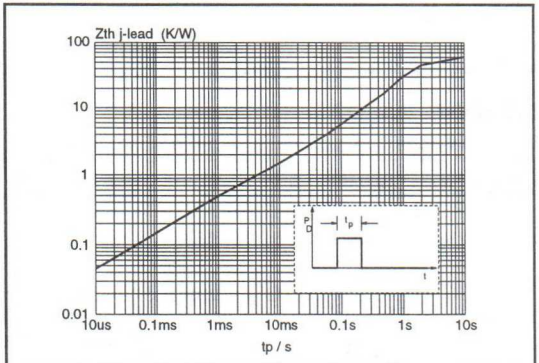



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width $t_p$.*

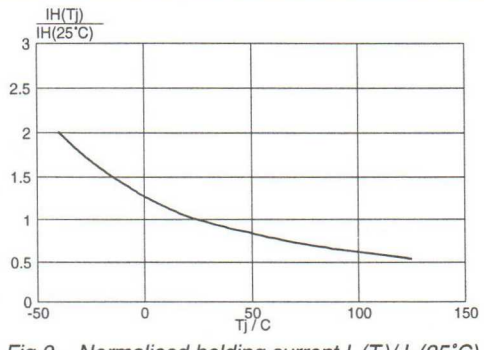



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

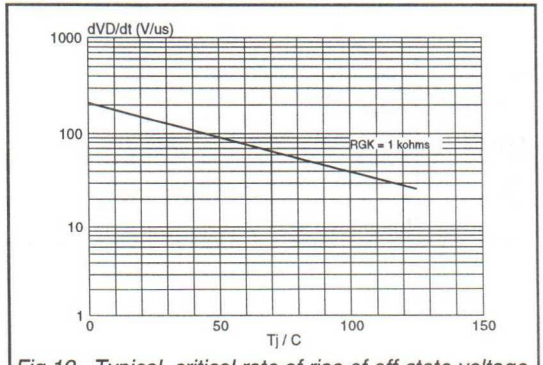



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Thyristors logic level

# BT150 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

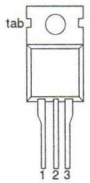
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT150- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 2.5 | 2.5 | 2.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 35 | 35 | 35 | A |

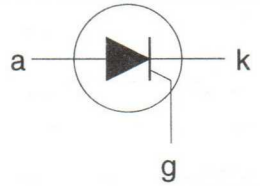
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 113$ °C | - | 2.5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | 35 | | | A |
| | | t = 8.3 ms | - | 38 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 6.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | 50 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125[2] | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 2.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 15 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.17 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.10 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.23 | 1.8 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 8 A; $V_R$ = 10 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

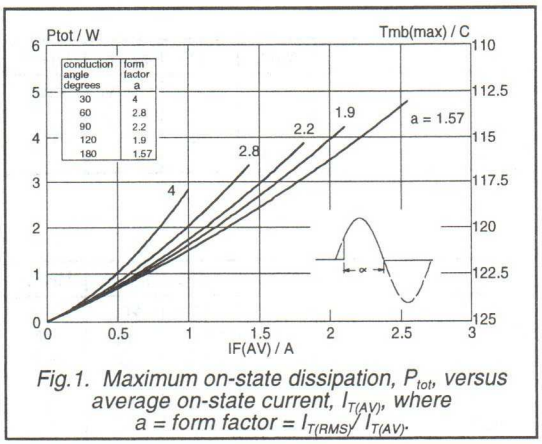



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.*

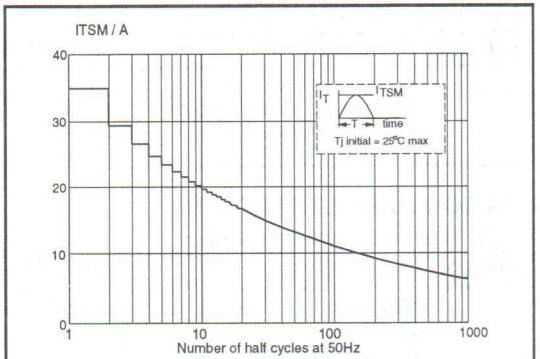



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

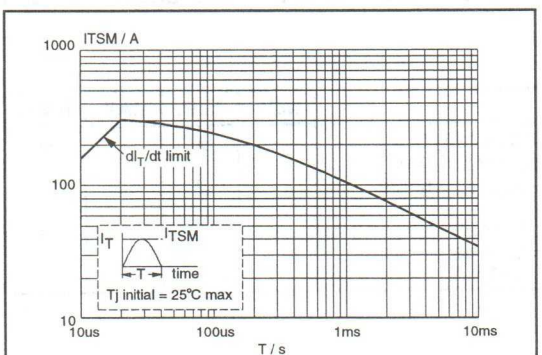



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

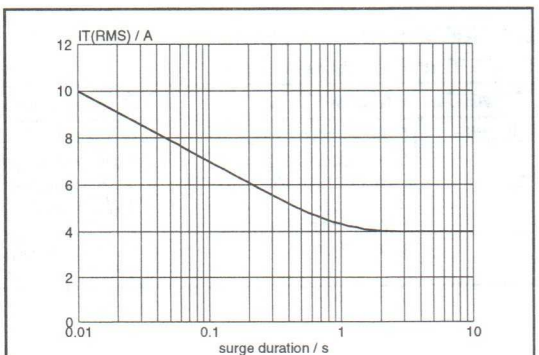



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 113^{\circ}C$.*

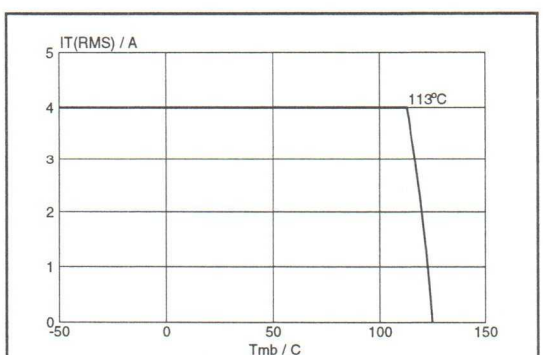



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

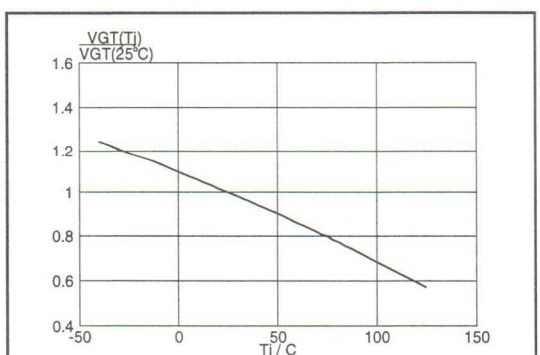



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

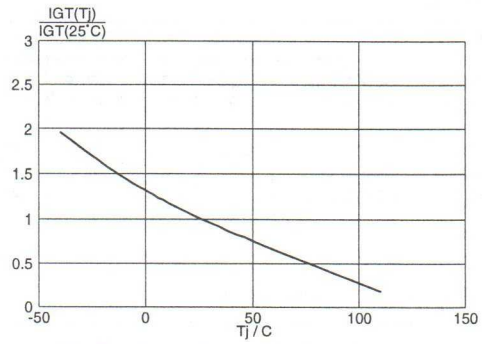



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

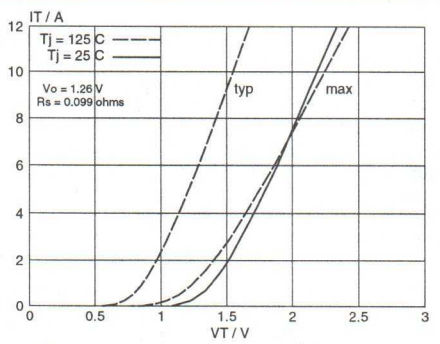



*Fig.10. Typical and maximum on-state characteristic.*

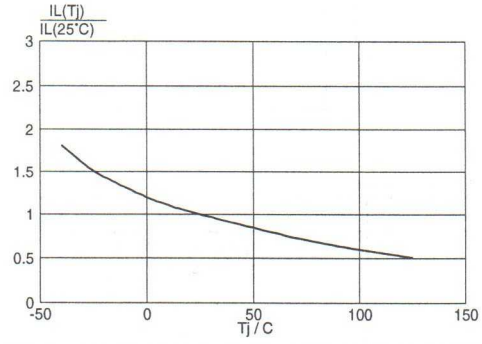



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

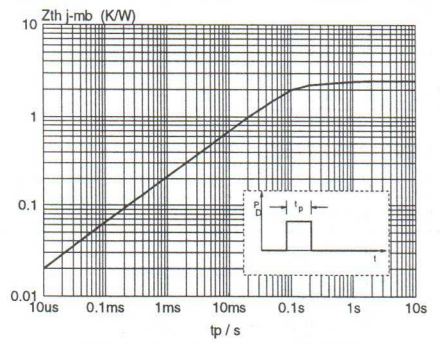



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

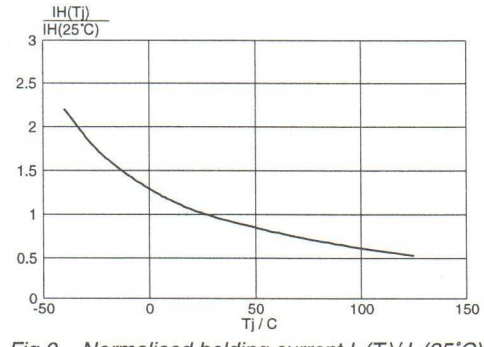



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

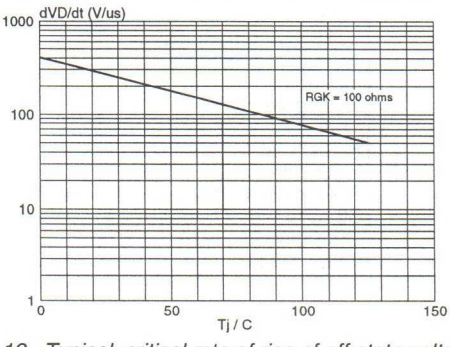



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

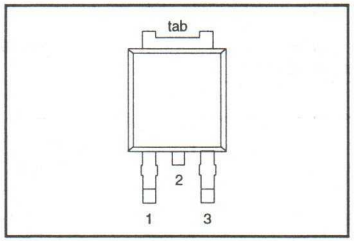
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT150S** (or BT150M)- | **500R** | **600R** | **800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 2.5 | 2.5 | 2.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 35 | 35 | 35 | A |

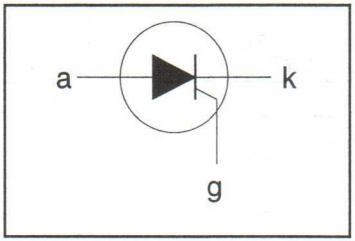
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | cathode | gate |
| 2 | anode | anode |
| 3 | gate | cathode |
| tab | anode | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500R** | **-600R** | **-800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | | 2.5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | | 35 | | A |
| | | t = 8.3 ms | - | | 38 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 6.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 3.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 15 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.17 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.10 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.23 | 1.8 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | - | 50 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 8 A; $V_R$ = 10 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

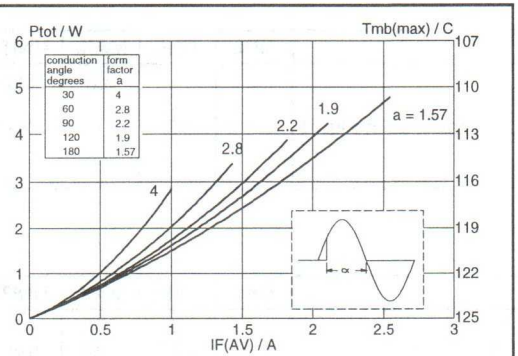



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

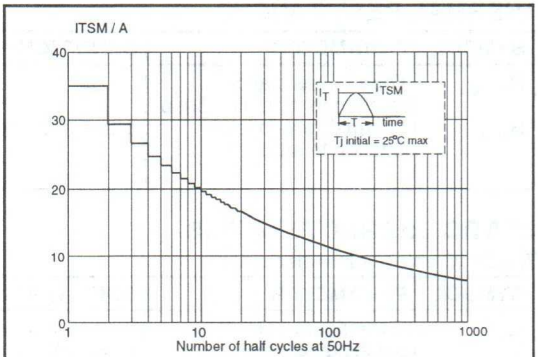



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

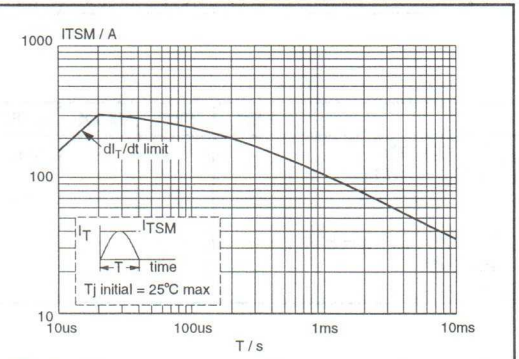



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

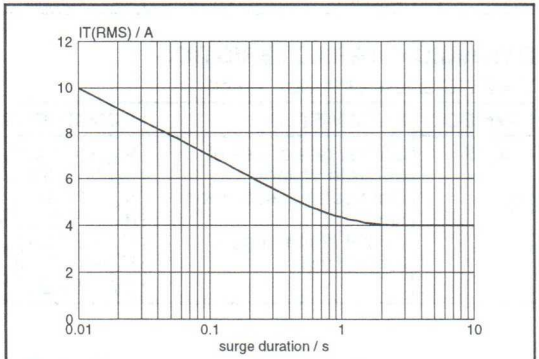



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

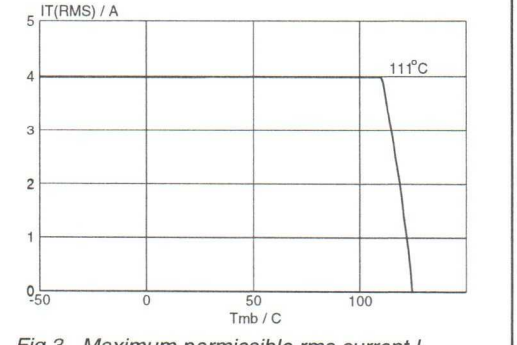



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

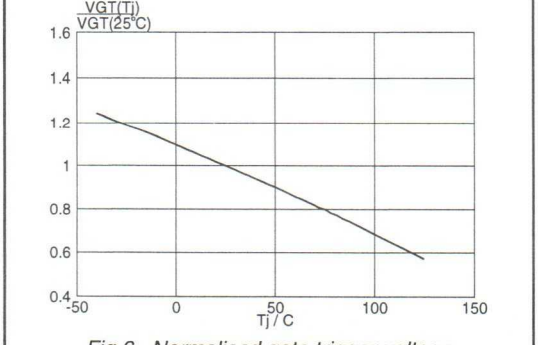



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

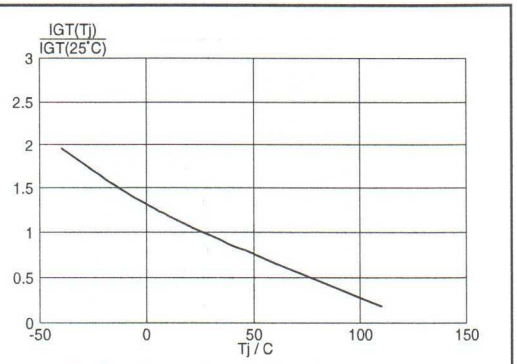



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

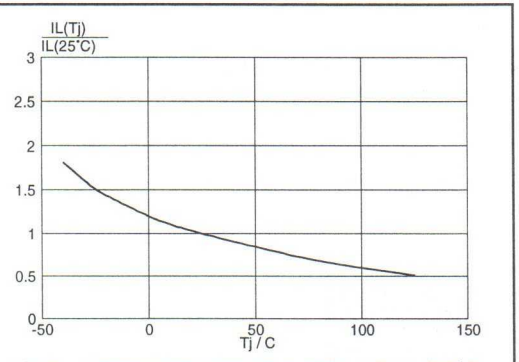



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

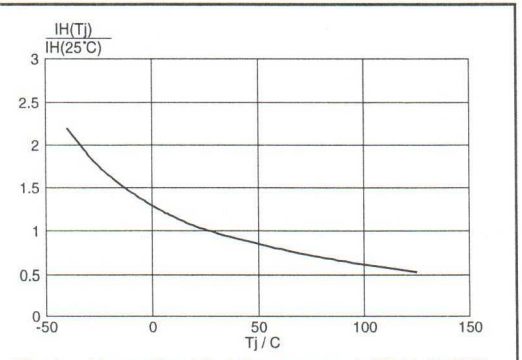



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

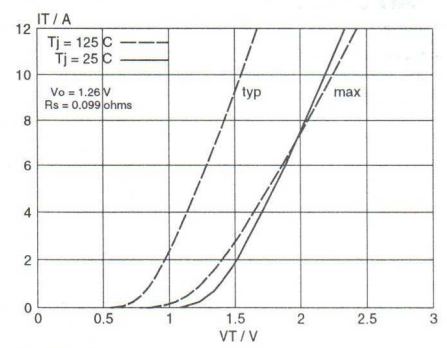



*Fig.10. Typical and maximum on-state characteristic.*

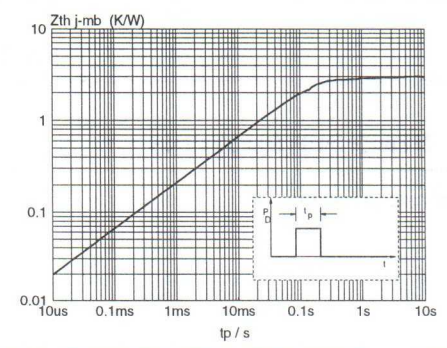



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

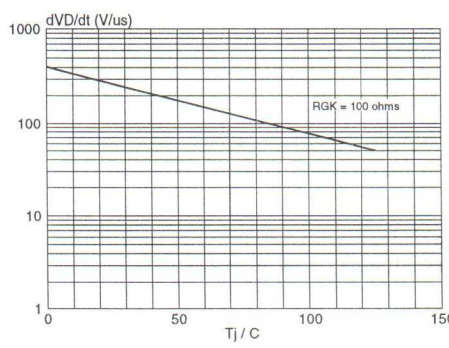



*Fig.12. Typical, critical rate of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

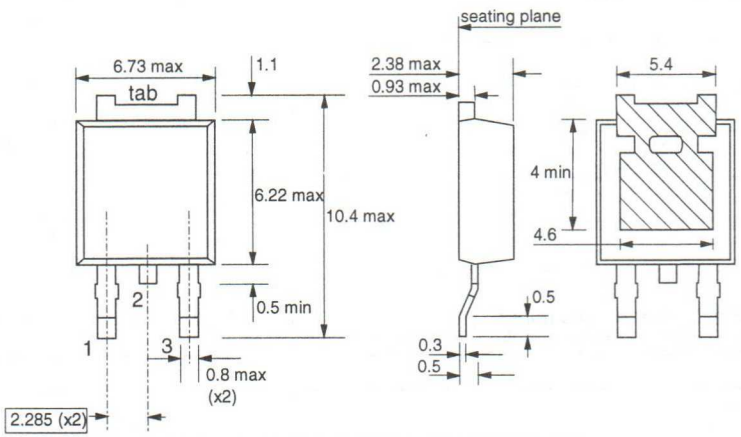



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

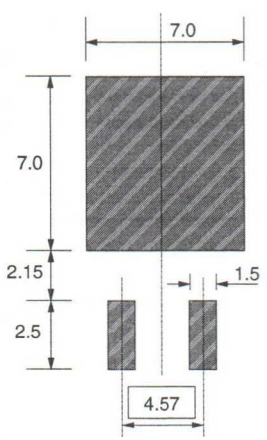



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

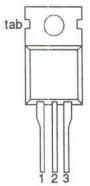
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT151- | 500R | 650R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 7.5 | 7.5 | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

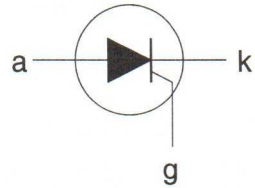
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -650R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 109$ °C | - | 7.5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | 100 | | | A |
| | | t = 8.3 ms | - | 110 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 50 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | 50 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.3 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 7 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 23 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; | | | | |
| | | Gate open circuit | 50 | 130 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 20 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

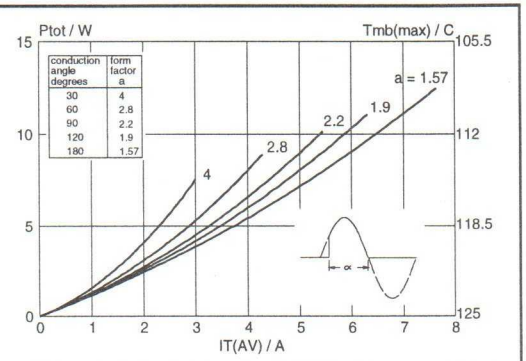



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

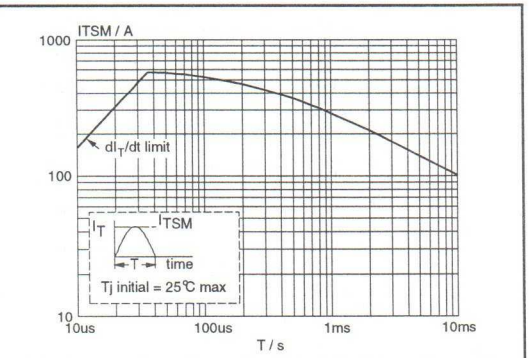



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

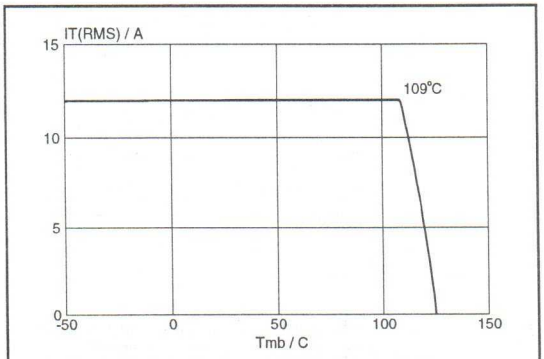



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

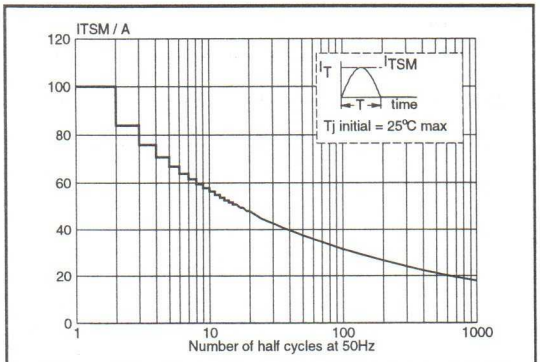



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

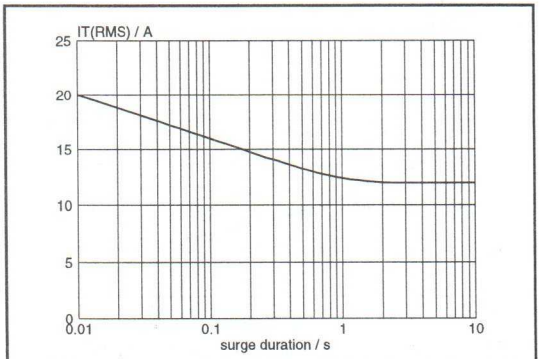



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 109°C$.*

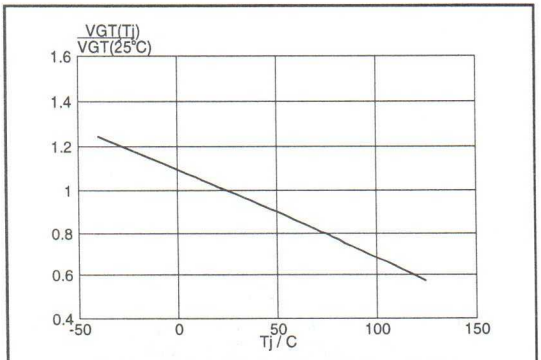



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

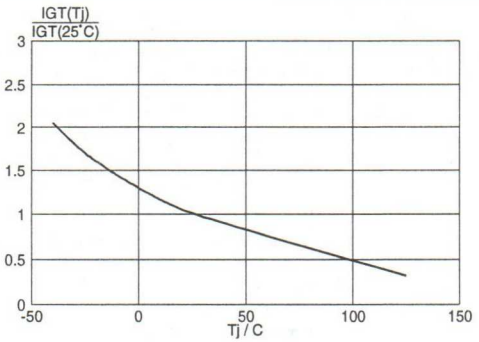



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

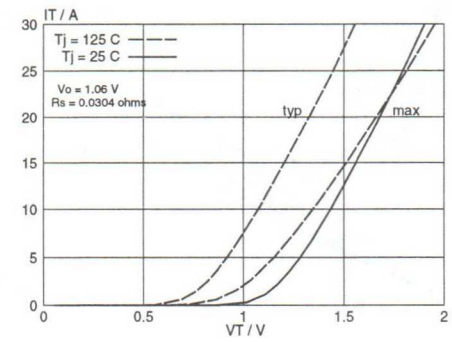



*Fig.10. Typical and maximum on-state characteristic.*

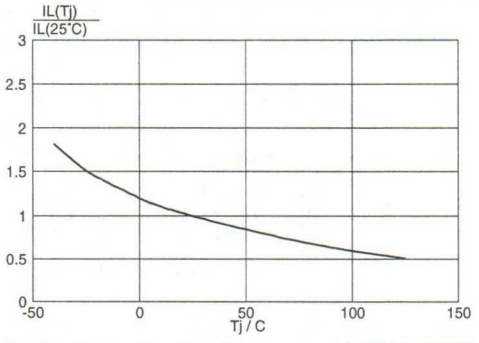



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature $T_j$.*

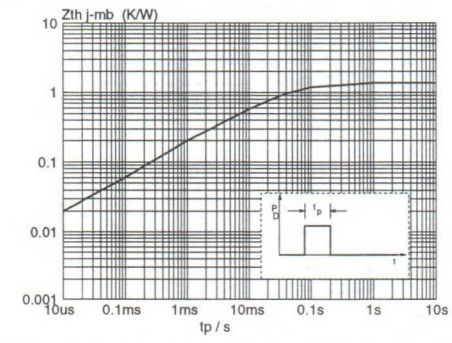



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

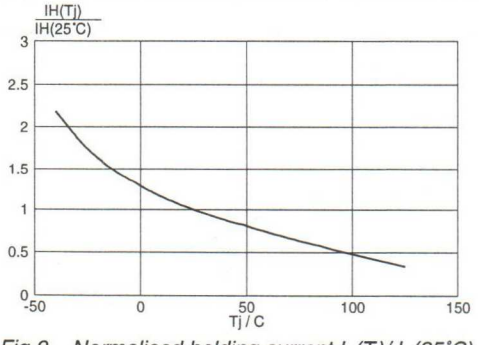



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature $T_j$.*

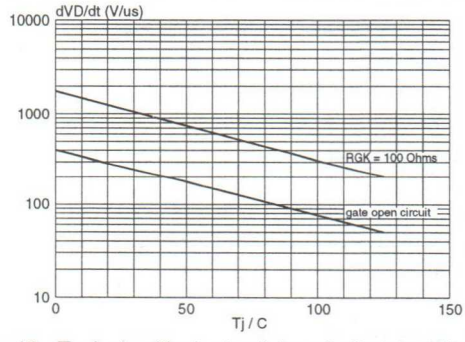



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

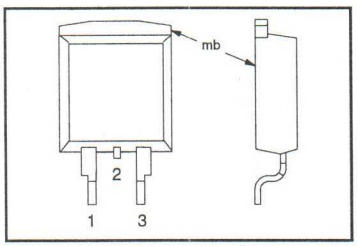
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT151B- | 500R | 650R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 7.5 | 7.5 | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

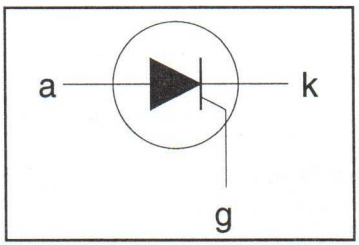
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| mb | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -650R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 109$ °C | - | | 7.5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | | 100 | | A |
| | | t = 8.3 ms | - | | 110 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 50 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.3 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 7 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 23 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; | | | | |
| | | Gate open circuit | 50 | 130 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 20 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

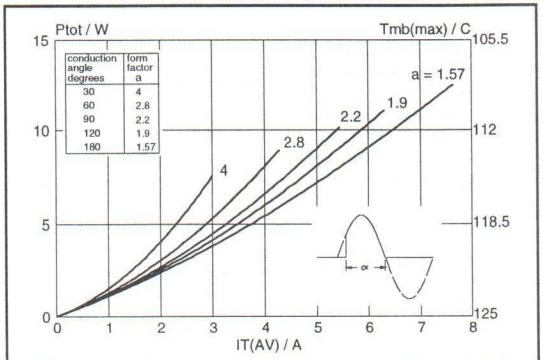



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

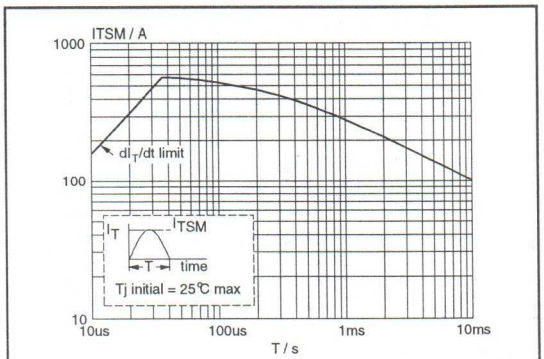



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq$ 10ms.*

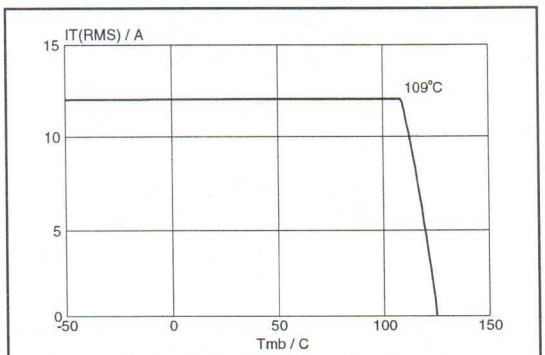



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

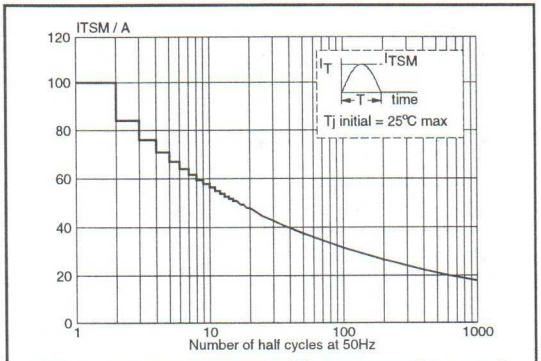



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

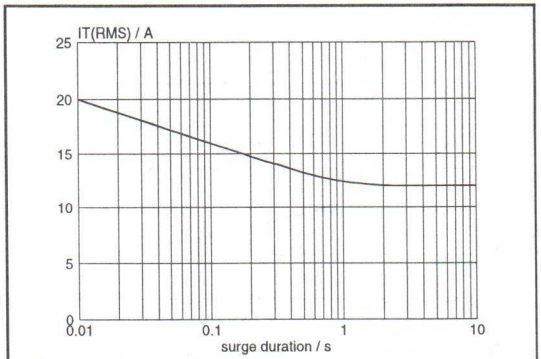



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 109˚C.*

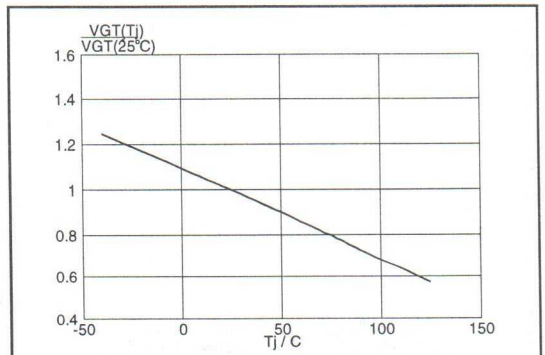



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature $T_j$.*

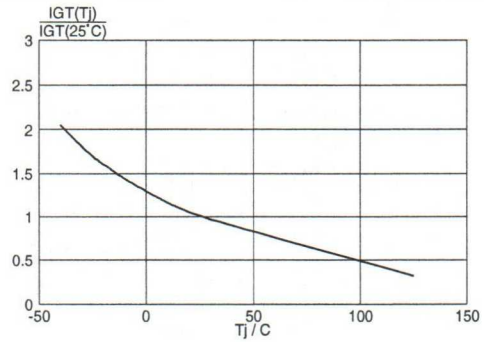



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

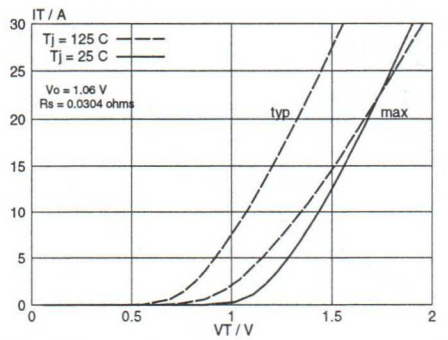



*Fig.10. Typical and maximum on-state characteristic.*

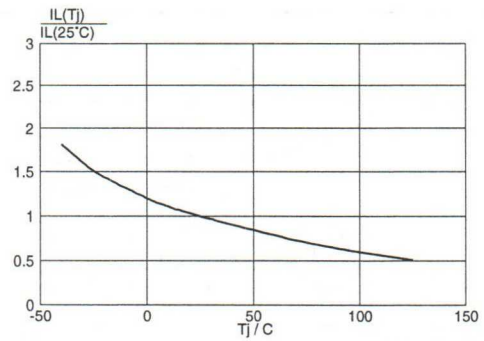



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

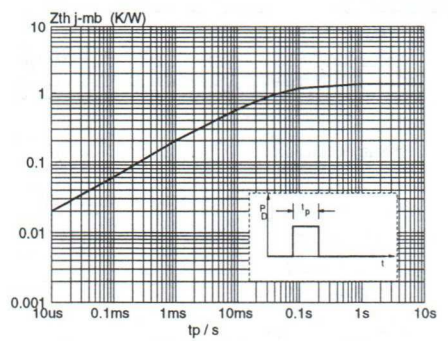



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

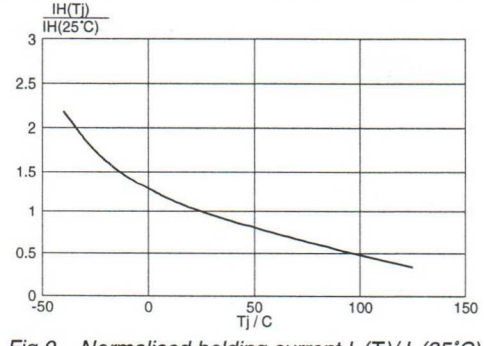



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

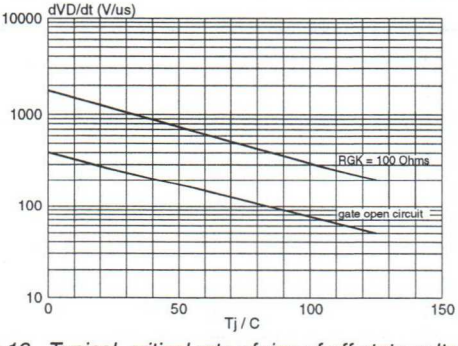



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

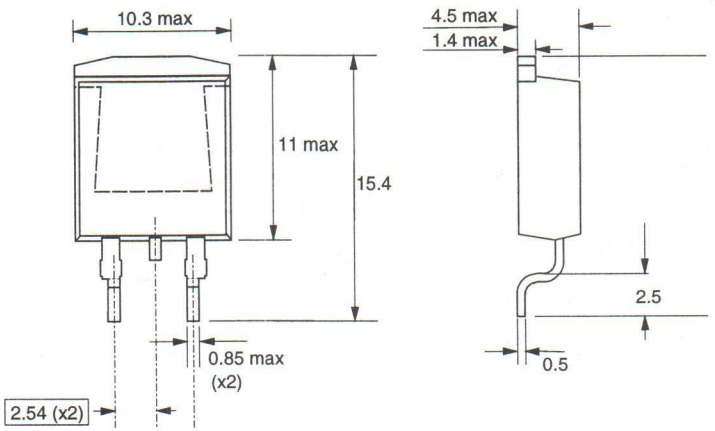



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

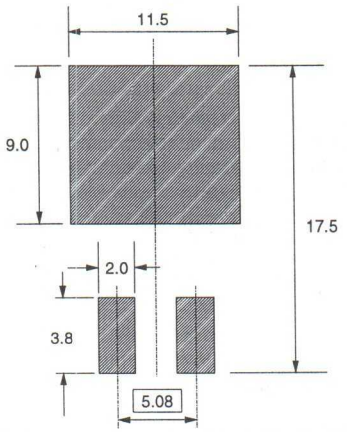



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

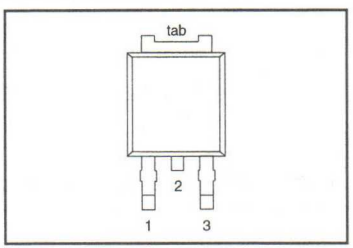
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT151S** (or BT151M)- | **500R** | **650R** | **800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 7.5 | 7.5 | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

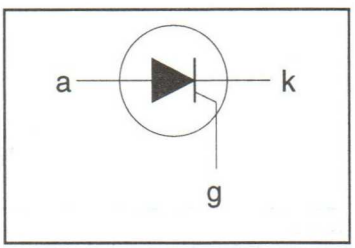
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | cathode | gate |
| 2 | anode | anode |
| 3 | gate | cathode |
| tab | anode | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500R** | **-650R** | **-800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 103$ °C | - | | 7.5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | | 100 | | A |
| | | t = 8.3 ms | - | | 110 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 50 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.8 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 7 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 23 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; | | | | |
| | | Gate open circuit | 50 | 130 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 20 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

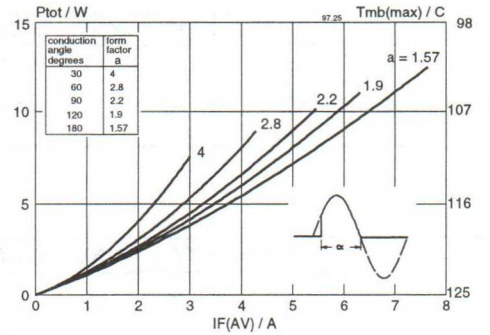



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

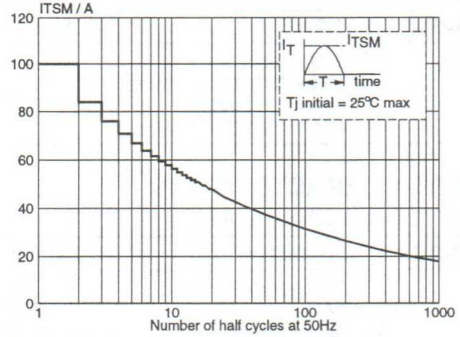



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

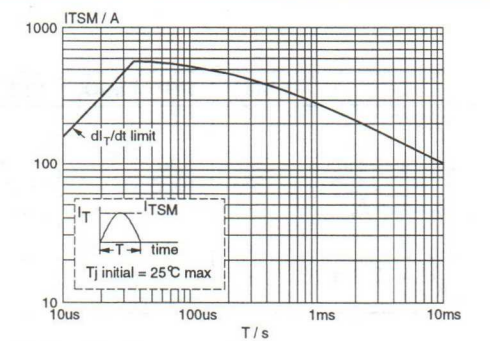



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

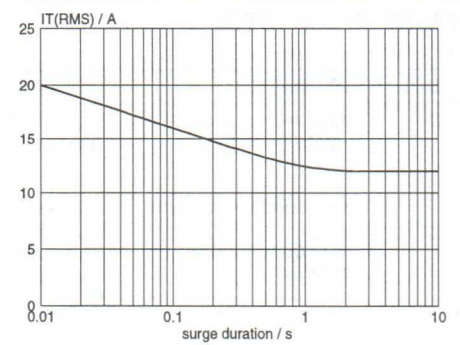



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103°C$.*

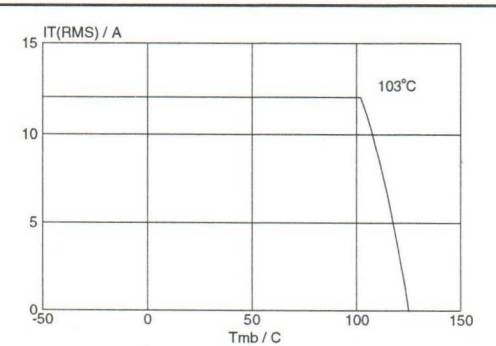



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

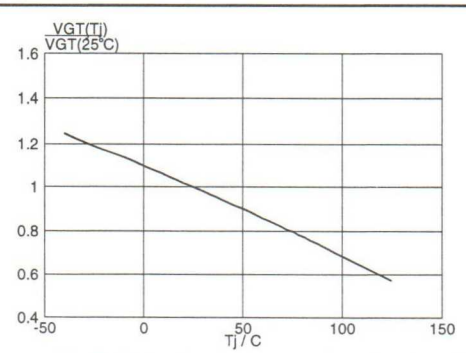



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

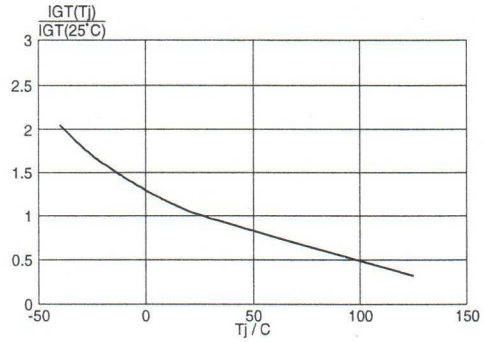



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

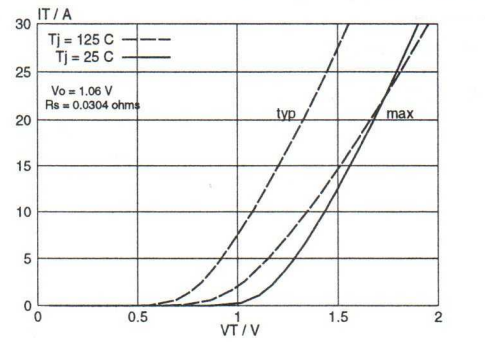



*Fig.10. Typical and maximum on-state characteristic.*

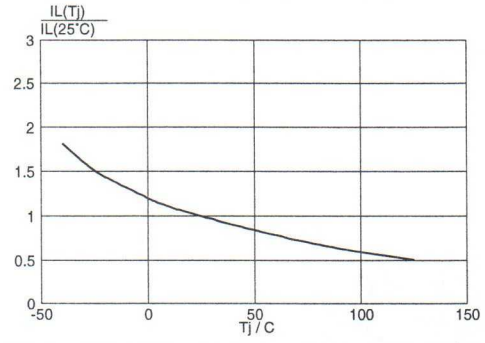



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

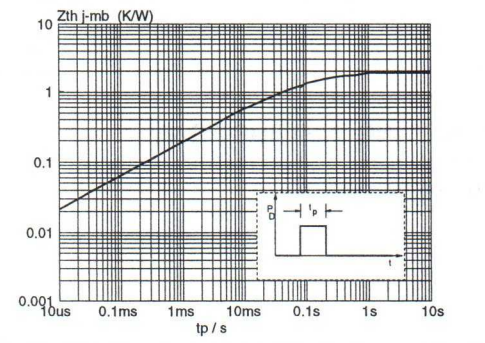



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

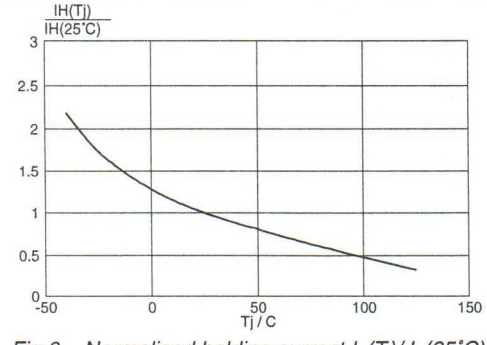



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

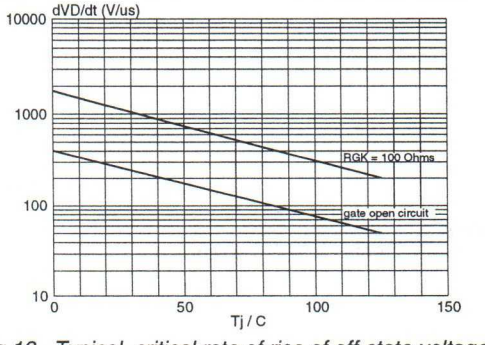



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

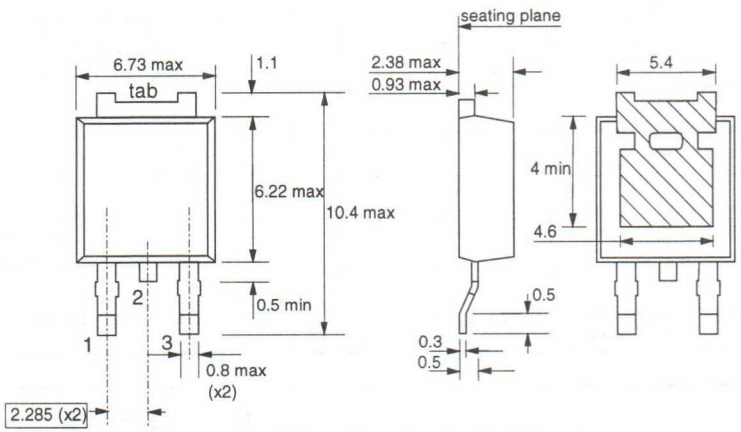



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

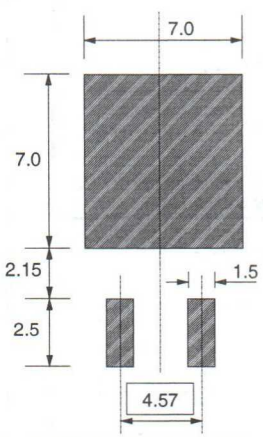



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

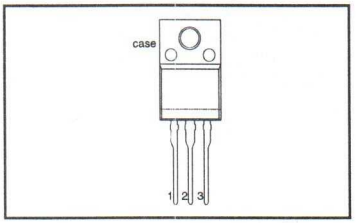
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT151X-** | **500** | **650** | **800** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5.7 | 5.7 | 5.7 | A |
| $I_{T(RMS)}$ | RMS on-state current | 9 | 9 | 9 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

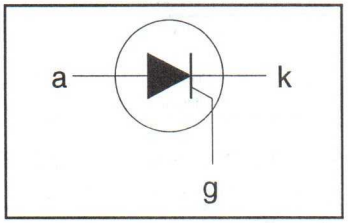
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-650** | **-800** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{hs} \leq 87$ °C | - | | 5.7 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 9 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 100 | | A |
| | | t = 8.3 ms | - | | 110 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 50 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 7 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 23 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform | | | | |
| | | Gate open circuit | 50 | 130 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 20 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

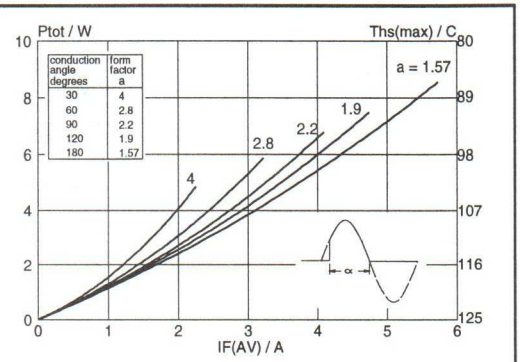



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

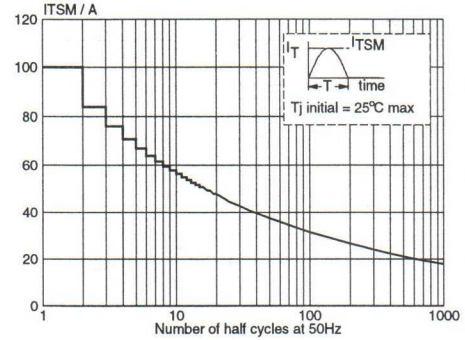



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

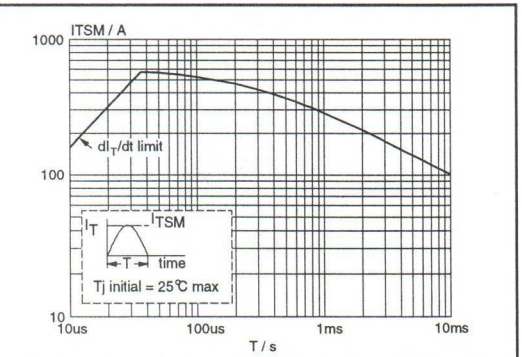



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

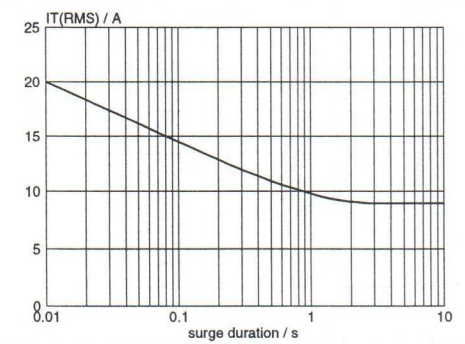



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 87°C$.*

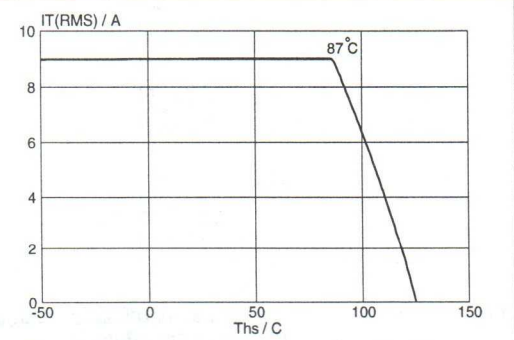



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

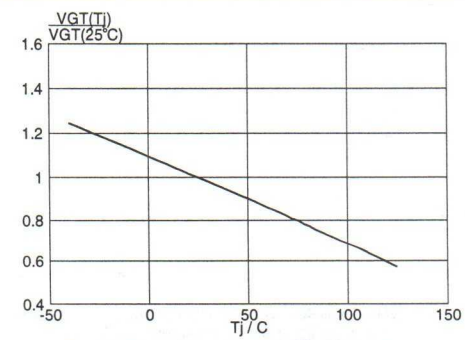



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

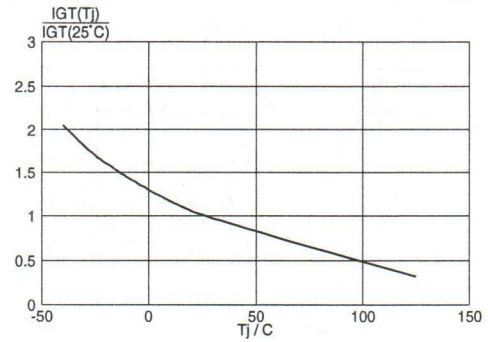



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

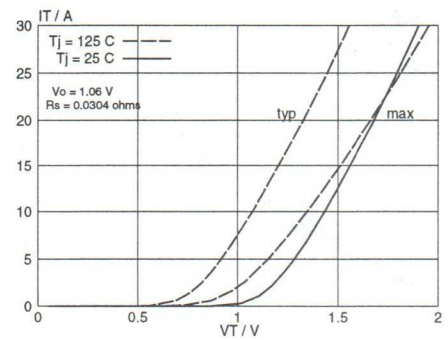



*Fig.10. Typical and maximum on-state characteristic.*

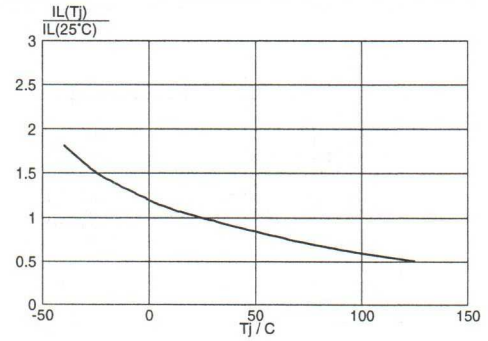



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

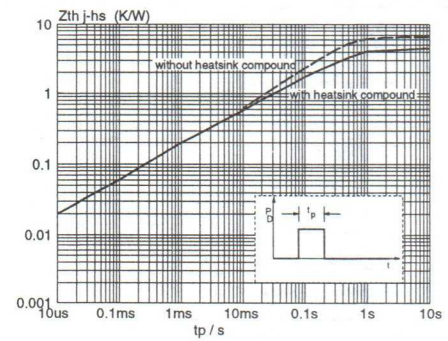



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

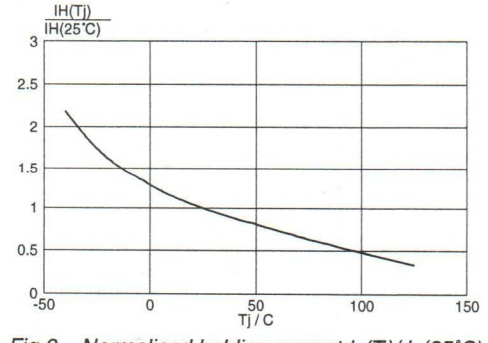



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

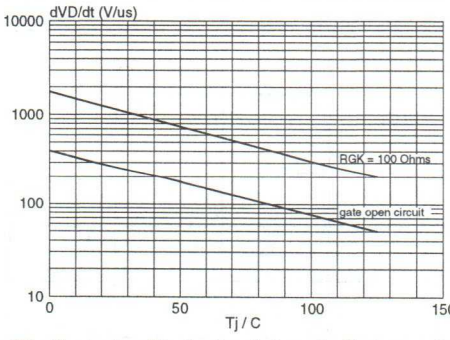



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

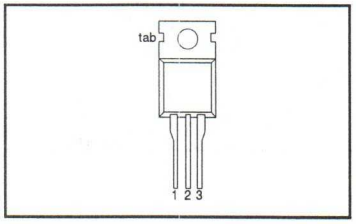
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT152- | 400R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 450 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 13 | 13 | 13 | A |
| $I_{T(RMS)}$ | RMS on-state current | 20 | 20 | 20 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 200 | 200 | 200 | A |

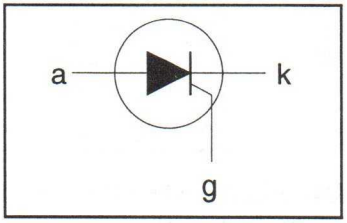
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -400R | -600R | -800R | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 450[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 103$ °C | - | | 13 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 20 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 200 | | A |
| | | t = 8.3 ms | - | | 220 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 200 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 50 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | - | | 200 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 5 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 20 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.1 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 3 | 32 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 25 | 80 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 15 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 40 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.2 | 1.0 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform gate open circuit | 200 | 300 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; $I_{TM}$ = 40 A | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 50 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

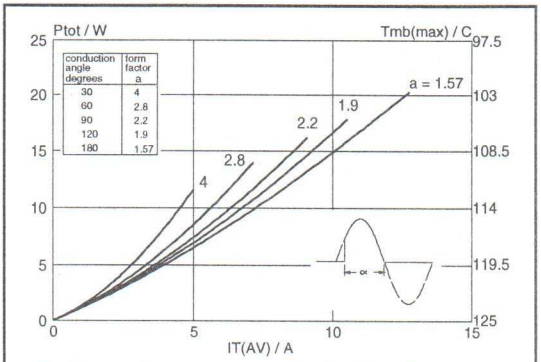



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

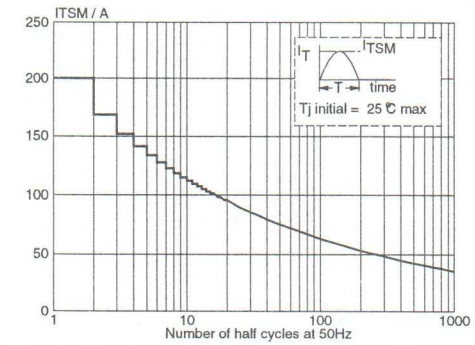



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

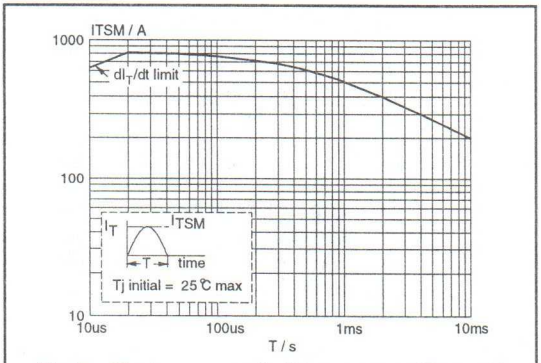



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

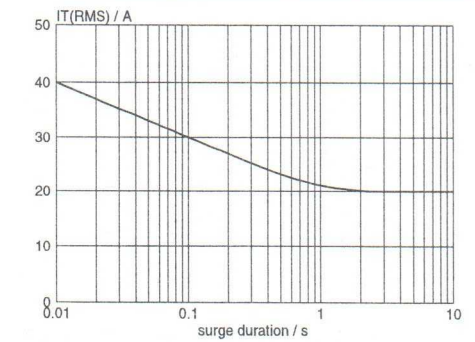



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103^{\circ}C$.*

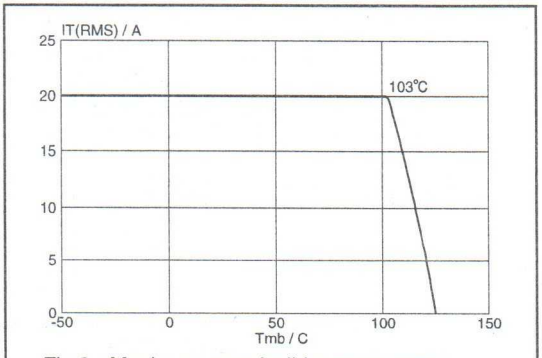



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

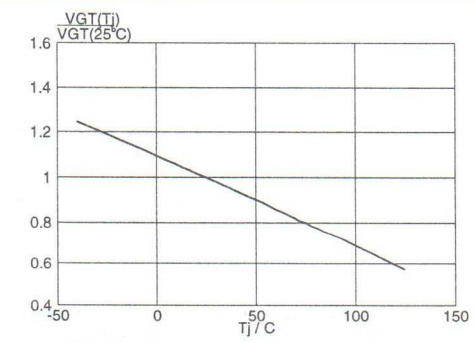



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

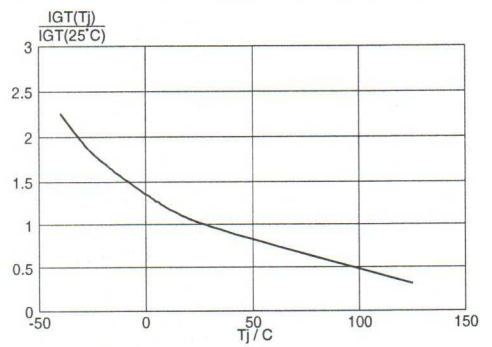



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

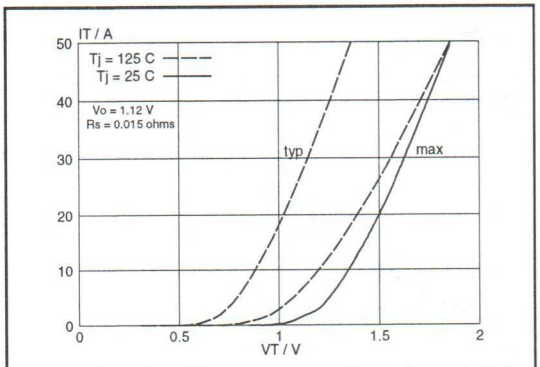



*Fig.10. Typical and maximum on-state characteristic.*

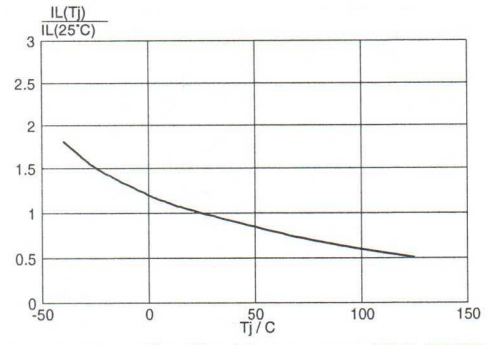



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

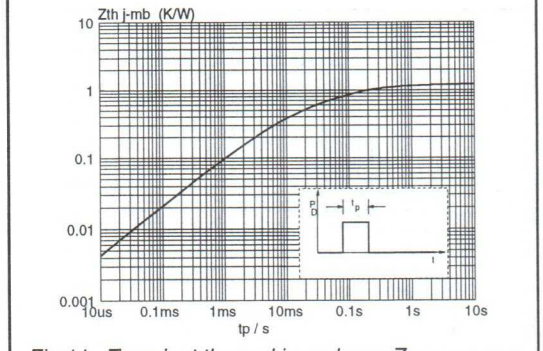



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

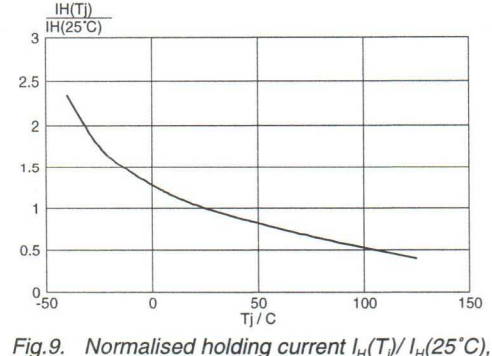



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

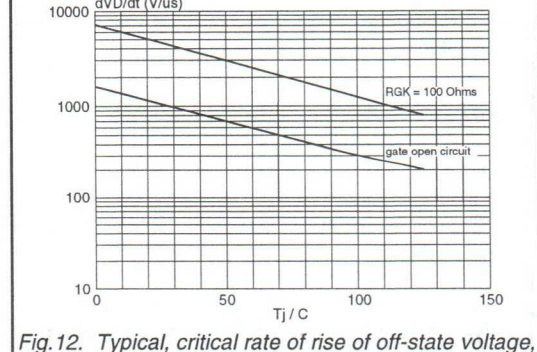



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

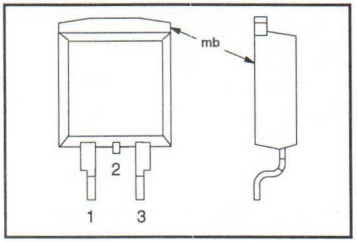
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT152B- | 400R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 450 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 13 | 13 | 13 | A |
| $I_{T(RMS)}$ | RMS on-state current | 20 | 20 | 20 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 200 | 200 | 200 | A |

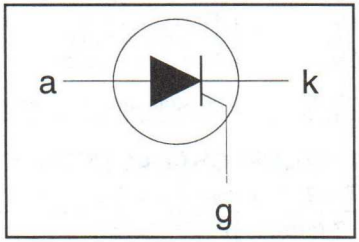
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| mb | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -400R | -600R | -800R | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 450[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 103$ °C | - | 13 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 20 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | 200 | | | A |
| | | t = 8.3 ms | - | 220 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 200 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 50 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | - | 200 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 5 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 20 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.1 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 3 | 32 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 25 | 80 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 15 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 40 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.2 | 1.0 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform gate open circuit | 200 | 300 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; $I_{TM}$ = 40 A | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 50 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

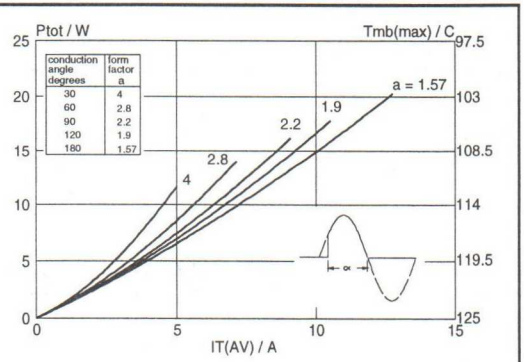



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

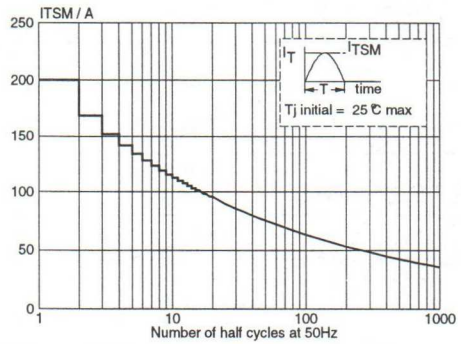



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

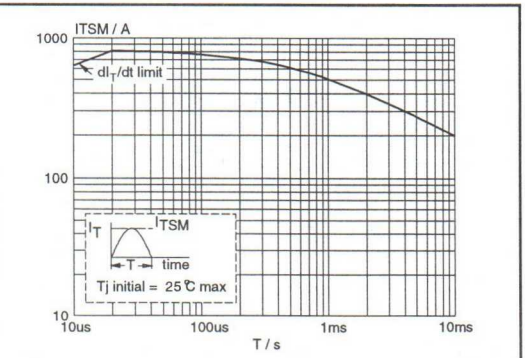



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

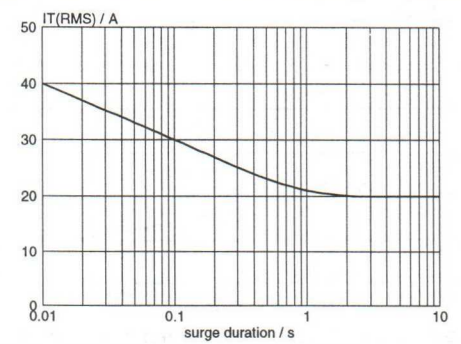



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103°C$.*

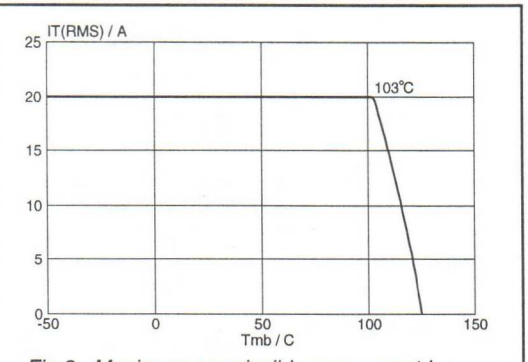



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

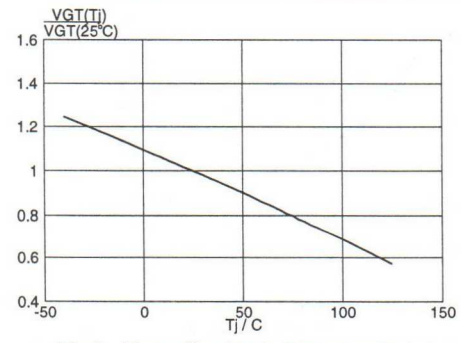



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

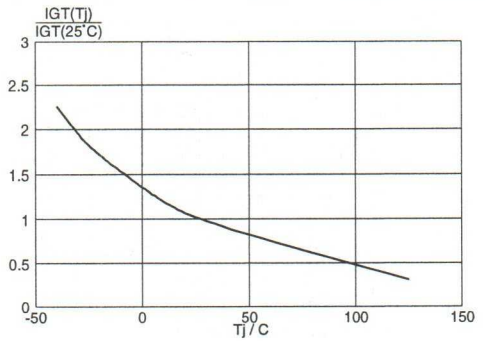



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

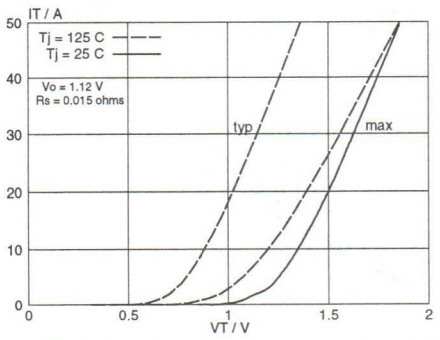



*Fig.10. Typical and maximum on-state characteristic.*

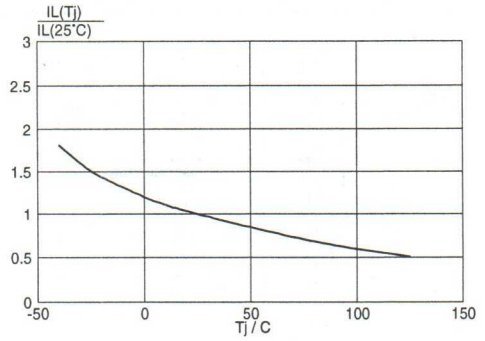



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

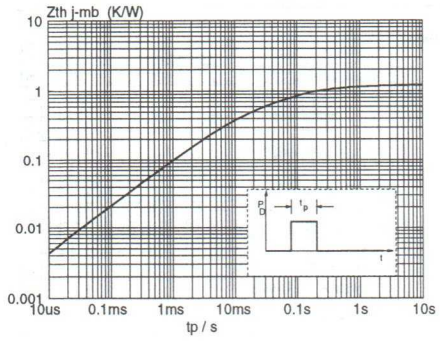



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

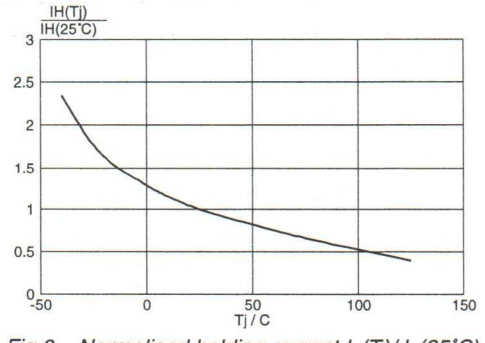



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

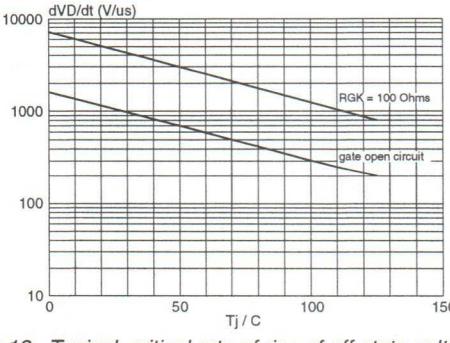



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

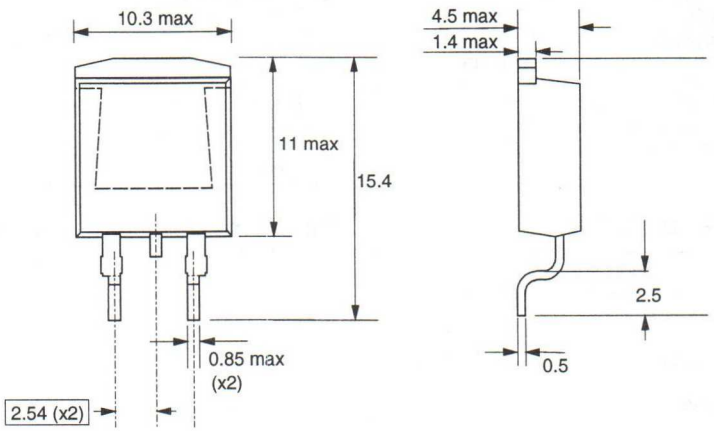



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

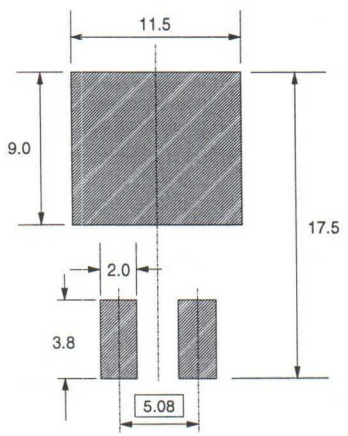



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

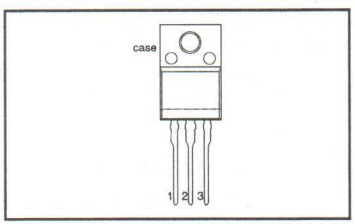
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT152X- | 400R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 450 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 13 | 13 | 13 | A |
| $I_{T(RMS)}$ | RMS on-state current | 20 | 20 | 20 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 200 | 200 | 200 | A |

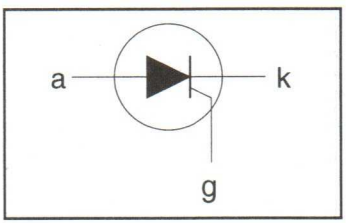
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -400R | -600R | -800R | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 450[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{hs} \leq 43$ °C | - | | 13 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 20 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 200 | | A |
| | | t = 8.3 ms | - | | 220 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 200 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 50$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | - | | 200 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 5 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 20 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | with heatsink compound | - | - | 4.0 | K/W |
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 3 | 32 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 25 | 80 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 15 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 40 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D$ = $V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $V_R$ = $V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.2 | 1.0 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform gate open circuit | 200 | 300 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs; $I_{TM}$ = 40 A | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 50 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

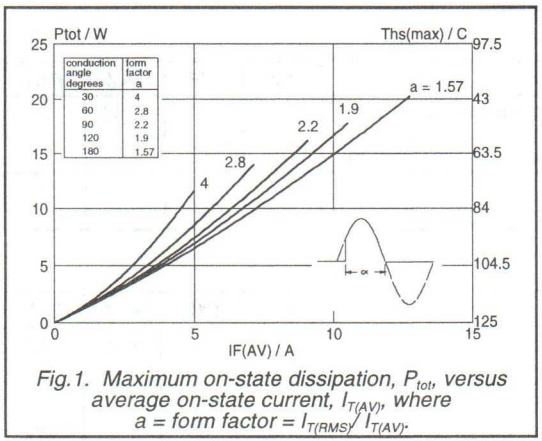



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

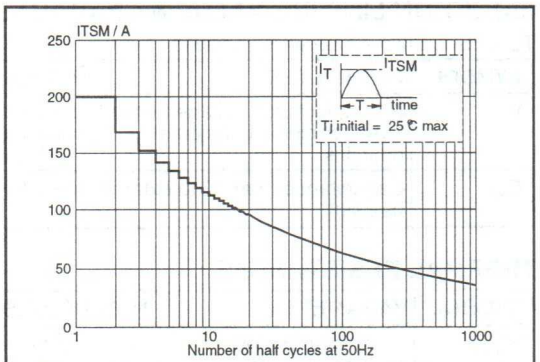



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

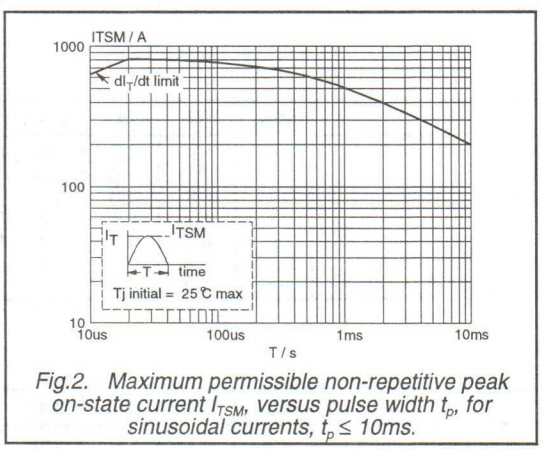



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

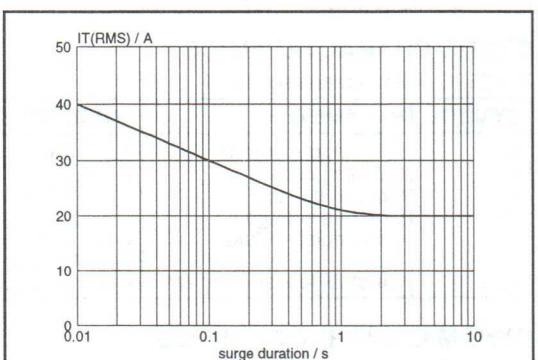



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 43^{\circ}C$.*

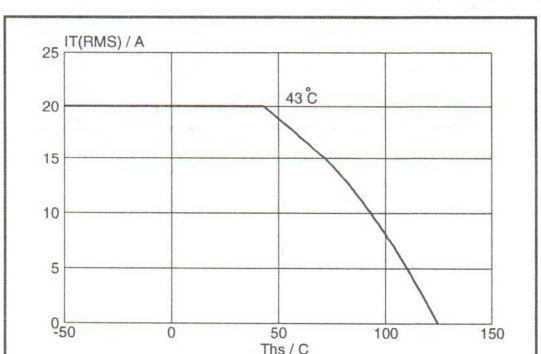



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

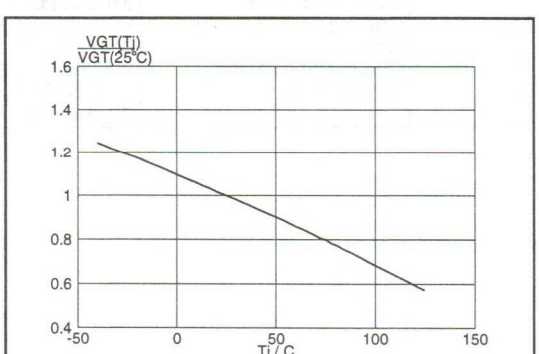



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

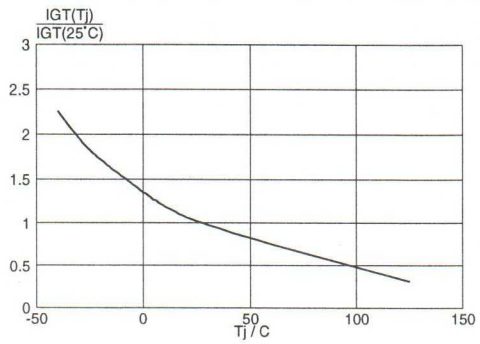



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

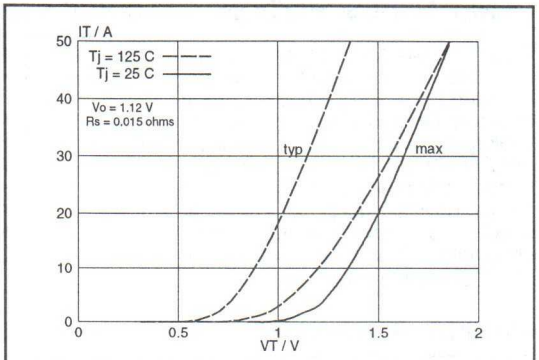



*Fig.10. Typical and maximum on-state characteristic.*

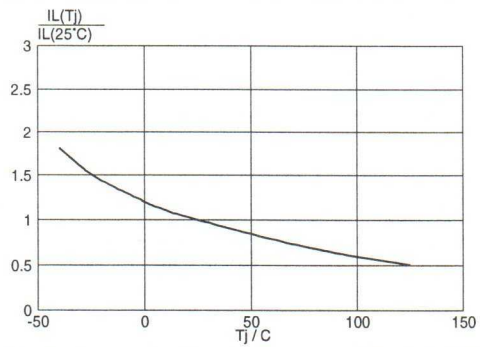



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

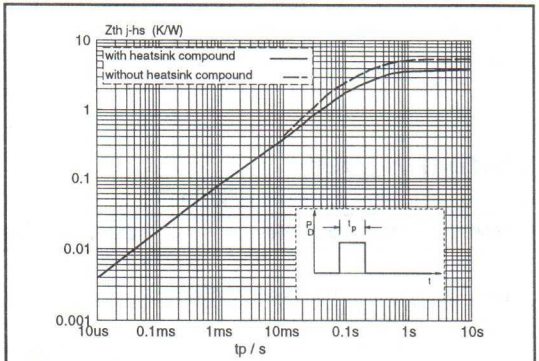



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

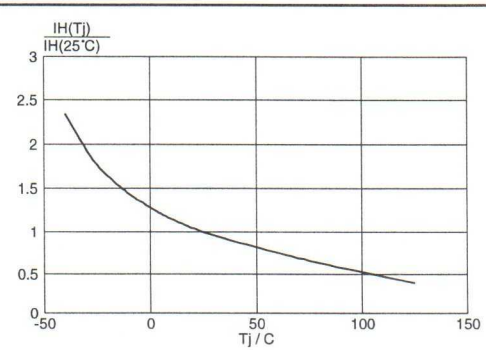



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

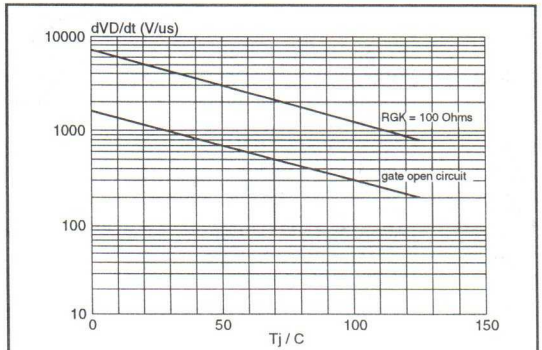



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Thyristors logic level for RCD/ GFI/ LCCB applications

# BT168 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in Residual Current Devices/ Ground Fault Interrupters/ Leakage Current Circuit Breakers (RCD/ GFI/ LCCB) applications where a minimum $I_{GT}$ limit is needed. These devices may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

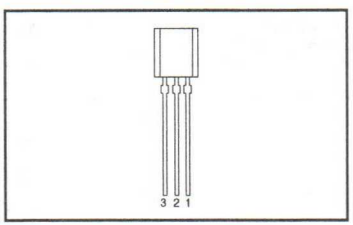
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | BT168 | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.5 | 0.5 | 0.5 | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 0.8 | 0.8 | 0.8 | 0.8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 8 | 8 | 8 | 8 | A |

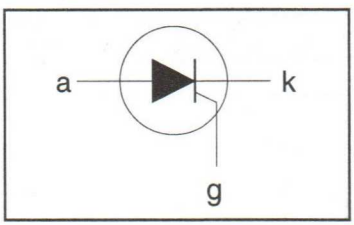
## PINNING - TO92 variant

| PIN | DESCRIPTION |
|---|---|
| 1 | anode |
| 2 | gate |
| 3 | cathode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200[1] | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{lead} \leq 83$ °C | - | 0.5 | | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 0.8 | | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | t = 10 ms | - | 8 | | | | A |
| | | t = 8.3 ms | - | 9 | | | | A |
| | | half sine wave; $T_j$ = 25 °C prior to surge | | | | | | |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.32 | | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 2 A; $I_G$ = 10 mA; $dI_G/dt$ = 100 mA/µs | - | 50 | | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 1 | | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | | V |
| $P_{GM}$ | Peak gate power | | - | 2 | | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.1 | | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to lead | | - | - | 60 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; lead length = 4mm | - | 150 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | 20 | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 1 A | - | 1.2 | 1.35 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 0.5 | 0.8 | V |
| | | $V_D$ = $V_{DRM(max)}$; $I_T$ = 10 mA; $T_j$ = 125 °C; gate open circuit | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $V_R$ = $V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

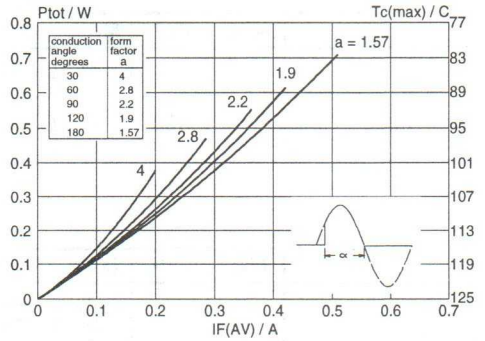



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

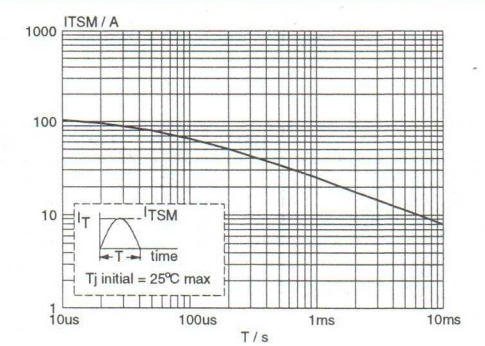



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

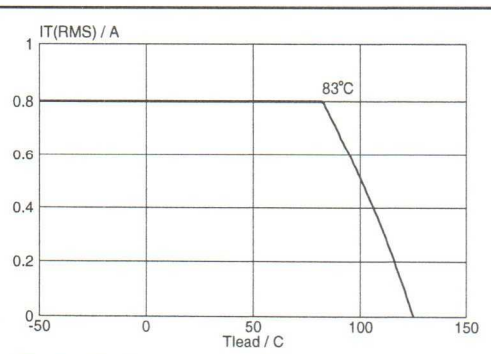



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, $T_{lead}$.*

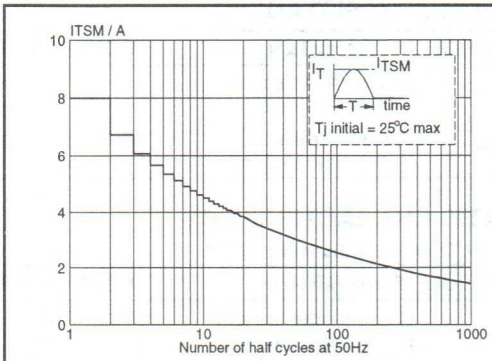



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

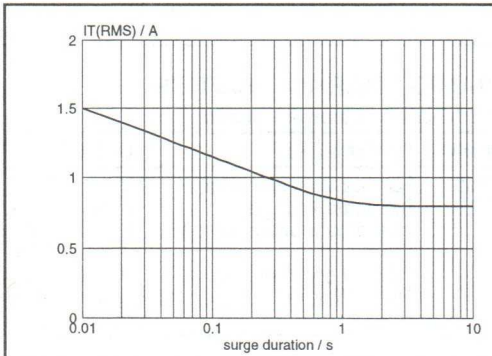



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 83°C$.*

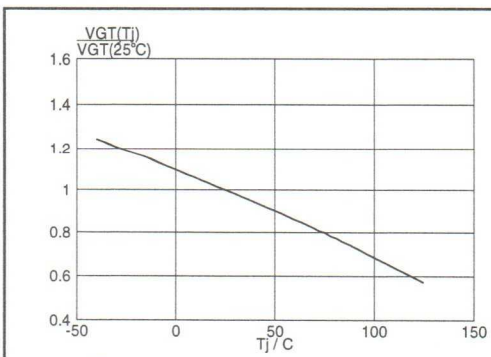



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

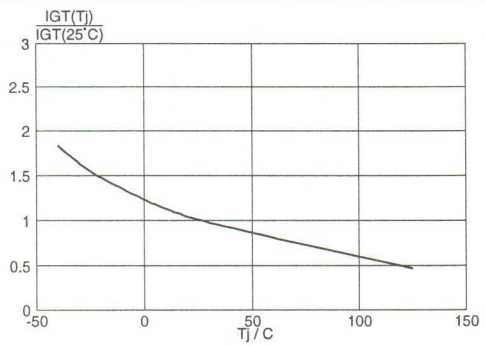



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

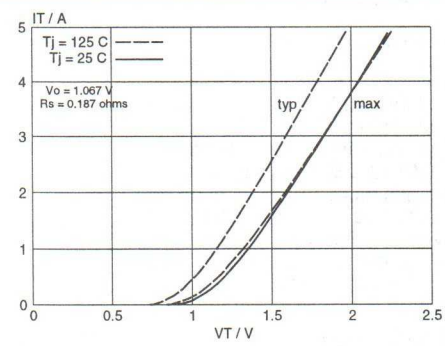



*Fig.10. Typical and maximum on-state characteristic.*

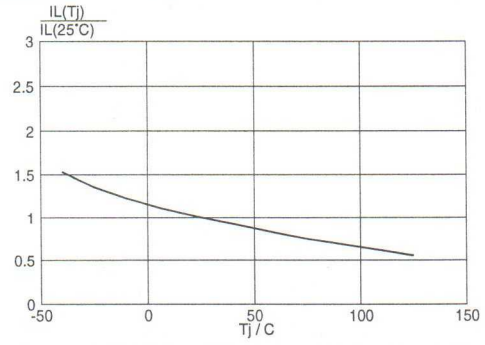



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

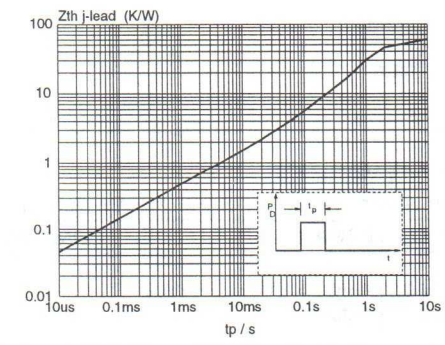



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width $t_p$.*

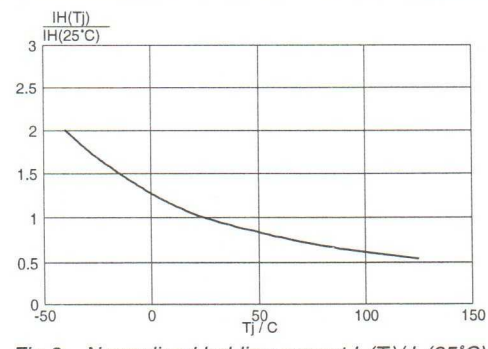



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

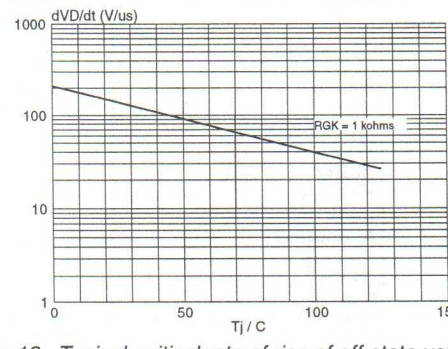



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Thyristors logic level for RCD/ GFI/ LCCB applications

# BT168W series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in Residual Current Devices/ Ground Fault Interrupters/ Leakage Current Circuit Breakers (RCD/ GFI/ LCCB) applications where a minimum $I_{GT}$ limit is needed. These devices may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

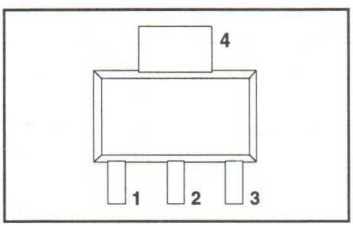
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | BT168 | BW | DW | EW | GW | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.6 | 0.6 | 0.6 | 0.6 | A |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 8 | 8 | 8 | 8 | A |

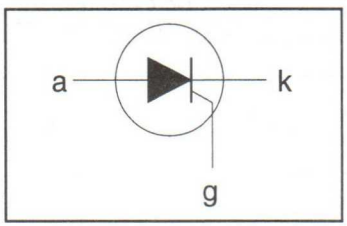
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200[1] | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{sp} \leq 112$ °C | - | 0.63 | | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 1 | | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | t = 10 ms | - | 8 | | | | A |
| | | t = 8.3 ms | - | 9 | | | | A |
| | | half sine wave; $T_j$ = 25 °C prior to surge | | | | | | |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.32 | | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 2 A; $I_G$ = 10 mA; $dI_G/dt$ = 100 mA/µs | - | 50 | | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 1 | | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | | V |
| $P_{GM}$ | Peak gate power | | - | 2 | | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.1 | | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted, minimum footprint | - | 156 | - | K/W |
| | | pcb mounted, pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | 20 | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.35 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 0.5 | 0.8 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 10 mA; $T_j$ = 125 °C; gate open circuit | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

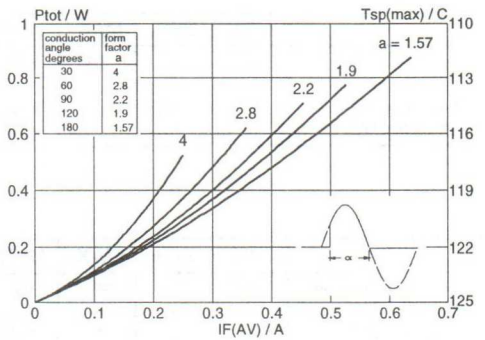



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

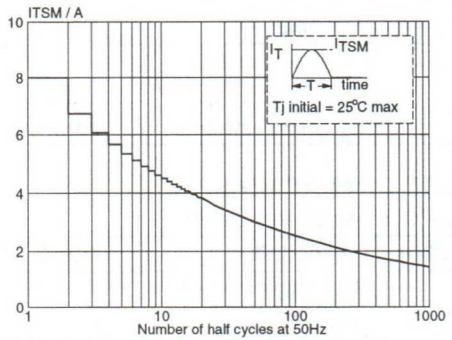



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

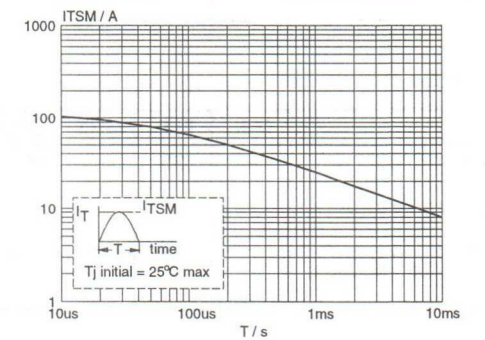



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq$ 10ms.*

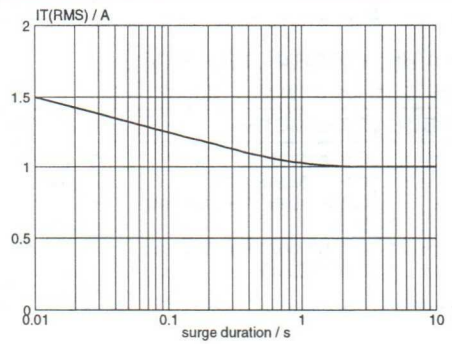



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq$ 112˚C.*

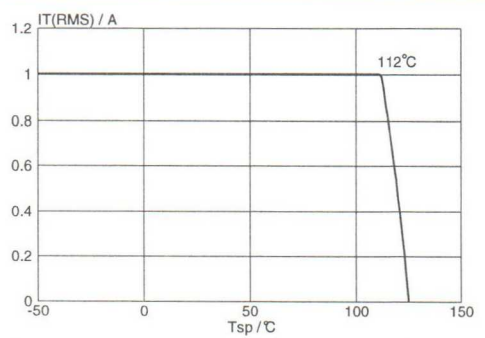



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

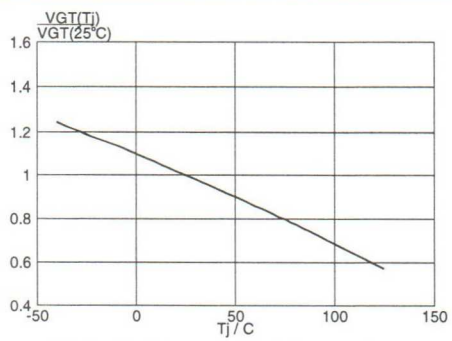



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature $T_j$.*

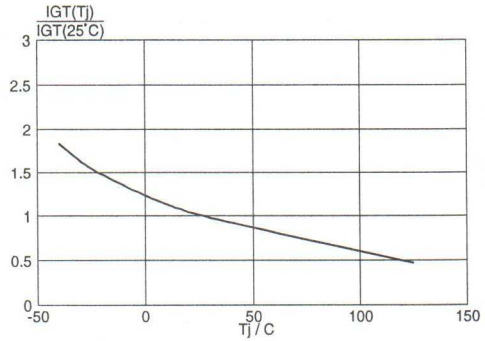



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

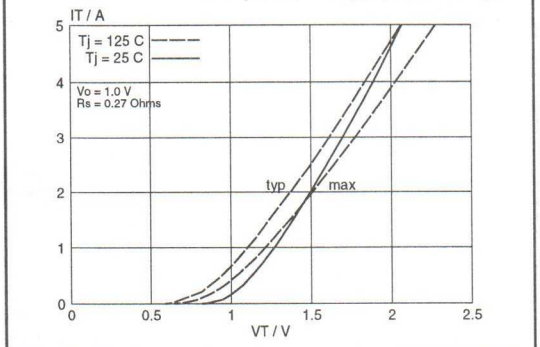



*Fig.10. Typical and maximum on-state characteristic.*

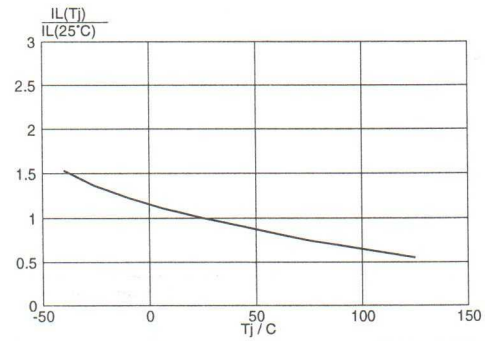



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

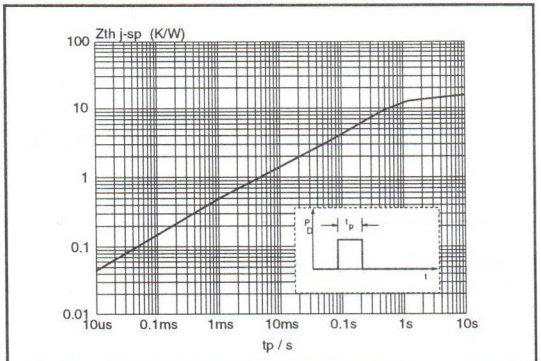



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width $t_p$.*

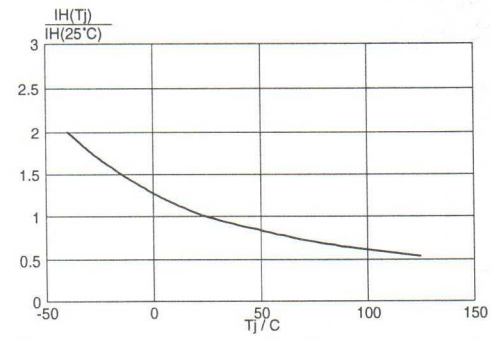



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

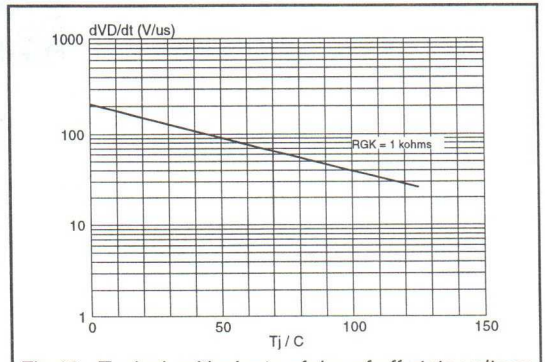



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

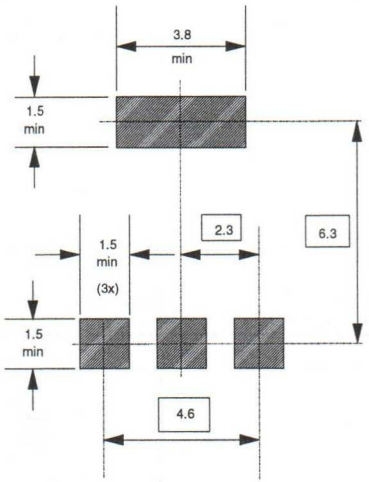



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

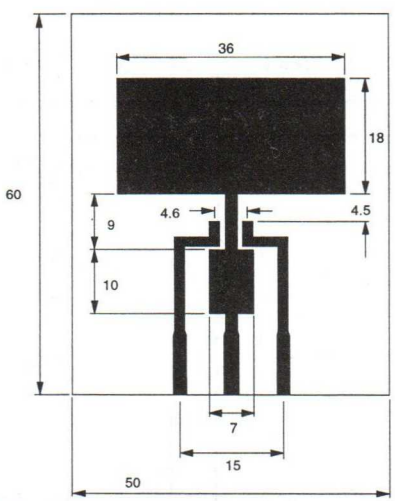



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).*

# Thyristors logic level

# BT169 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

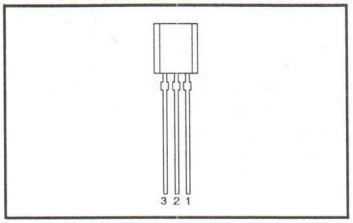
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | BT169 | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.5 | 0.5 | 0.5 | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 0.8 | 0.8 | 0.8 | 0.8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 8 | 8 | 8 | 8 | A |

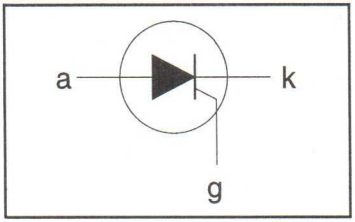
## PINNING - TO92 variant

| PIN | DESCRIPTION |
|---|---|
| 1 | anode |
| 2 | gate |
| 3 | cathode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200[1] | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{lead} \leq 83$ °C | - | 0.5 | | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 0.8 | | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | t = 10 ms | - | 8 | | | | A |
| | | t = 8.3 ms | - | 9 | | | | A |
| | | half sine wave; $T_j$ = 25 °C prior to surge | | | | | | |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.32 | | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 2 A; $I_G$ = 10 mA; $dI_G/dt$ = 100 mA/µs | - | 50 | | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 1 | | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | | V |
| $P_{GM}$ | Peak gate power | | - | 2 | | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.1 | | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}lead}$ | Thermal resistance junction to lead | | - | - | 60 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; lead length = 4mm | - | 150 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 1 A | - | 1.2 | 1.35 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 0.5 | 0.8 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 10 mA; $T_j$ = 125 °C; gate open circuit | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

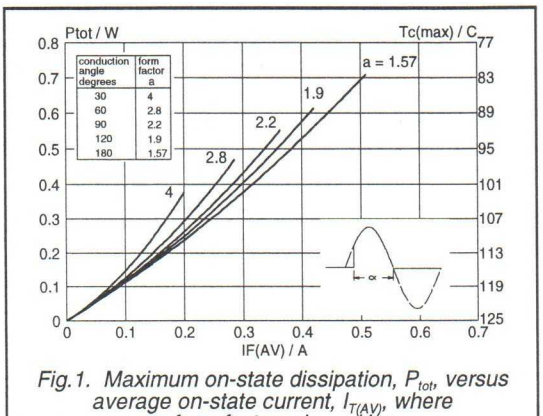



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

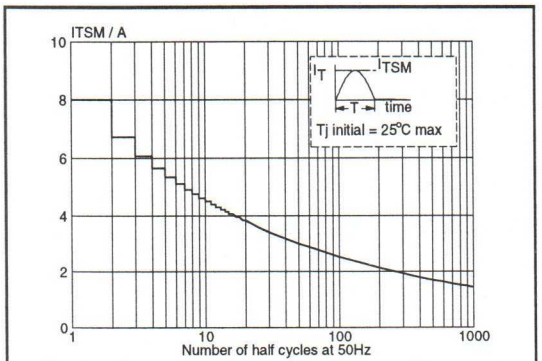



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

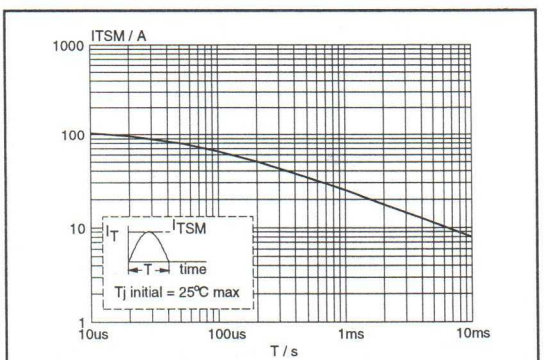



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

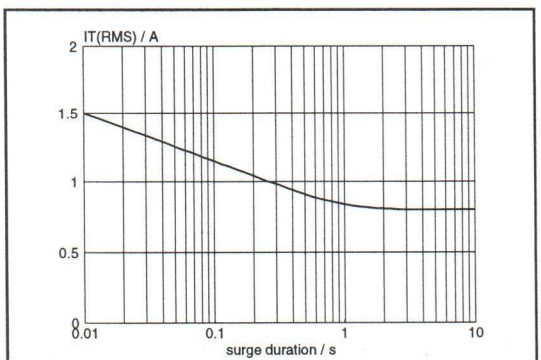



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 83°C$.*

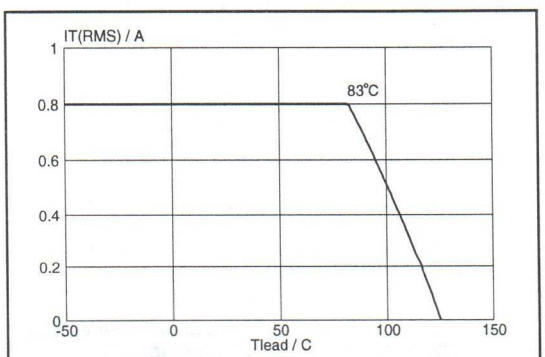



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, $T_{lead}$.*

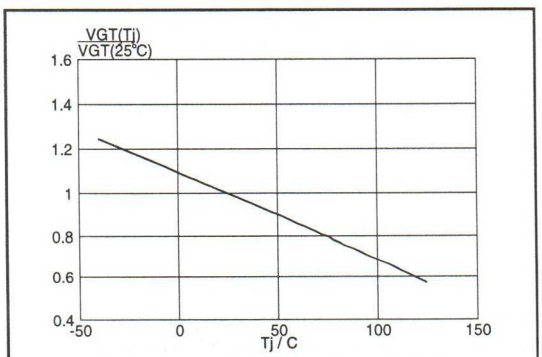



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

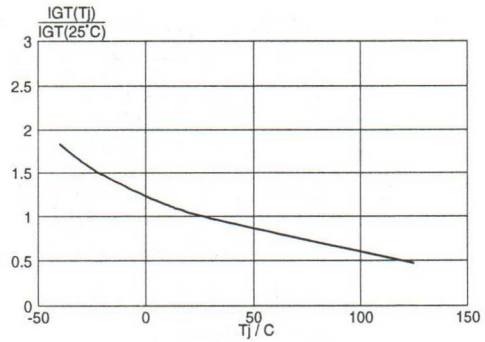



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

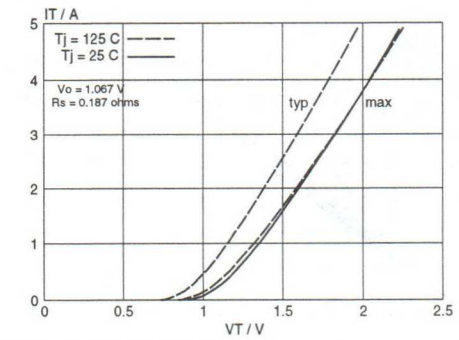



*Fig.10. Typical and maximum on-state characteristic.*

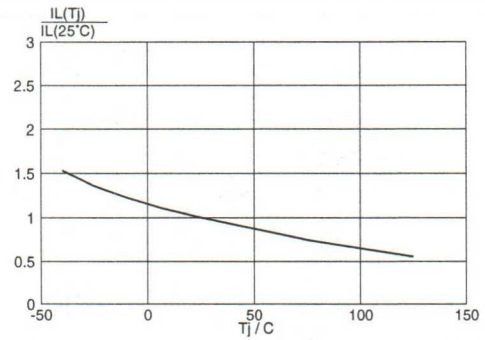



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

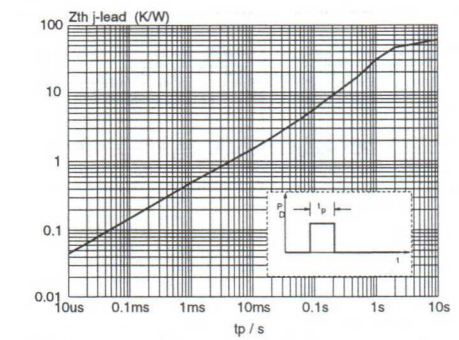



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width $t_p$.*

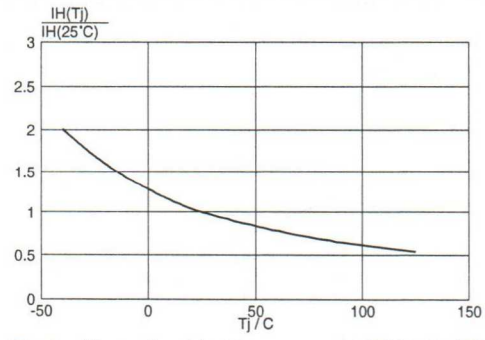



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

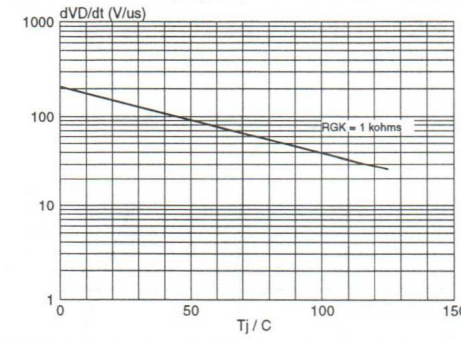



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Thyristor logic level

# BT169W Series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristor in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

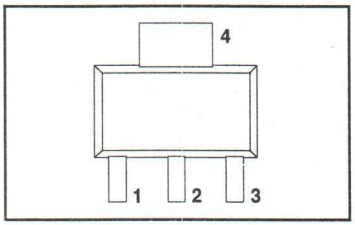
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | BT169 | BW | DW | EW | GW | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | 400 | 500 | 600 | V |
| $I_{T(AV)}$ | Average on-state current | 0.5 | 0.5 | 0.5 | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 0.8 | 0.8 | 0.8 | 0.8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 8 | 8 | 8 | 8 | A |

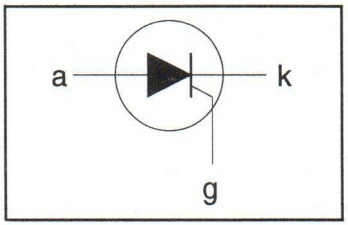
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | B | D | E | G | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200[1] | 400[1] | 500[1] | 600[1] | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{sp} \leq 112$ °C | - | 0.63 | | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 1 | | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | | |
| | | t = 10 ms | - | 8 | | | | A |
| | | t = 8.3 ms | - | 9 | | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.32 | | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs | - | 50 | | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 1 | | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | | V |
| $P_{GM}$ | Peak gate power | | - | 2 | | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.1 | | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted, minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:14 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ | - | 2 | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.35 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit | - | 0.5 | 0.8 | V |
| | | $V_D$ = $V_{DRM(max)}$; $I_T$ = 10 mA; $T_j$ = 125 °C; gate open circuit | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $V_R$ = $V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ =67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1k Ω | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

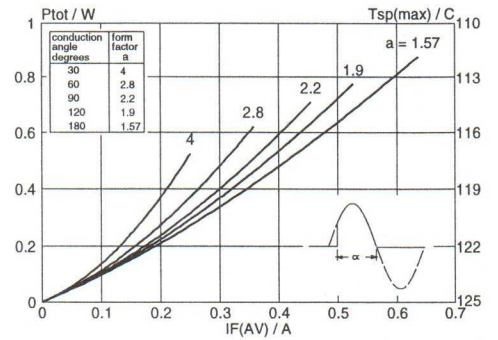



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

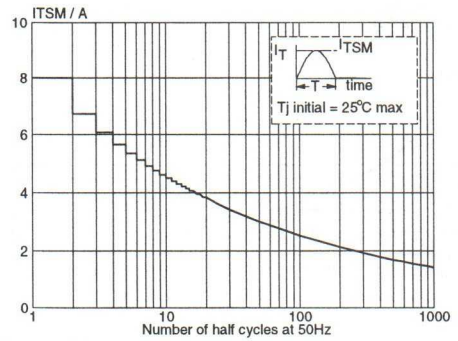



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

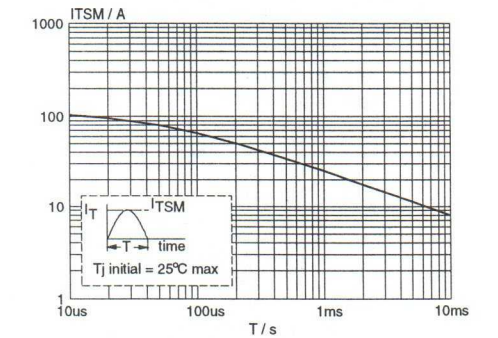



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

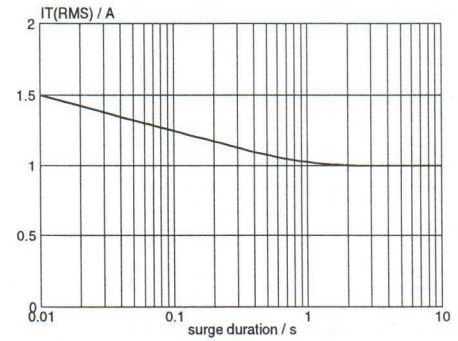



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 112°C$.*

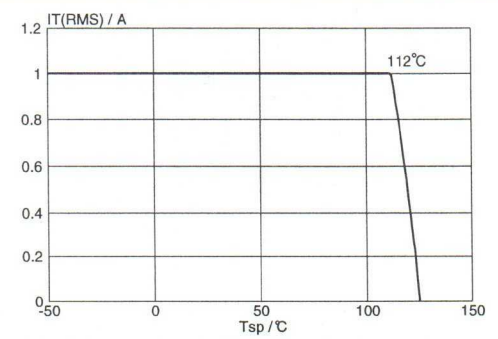



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature $T_{sp}$.*

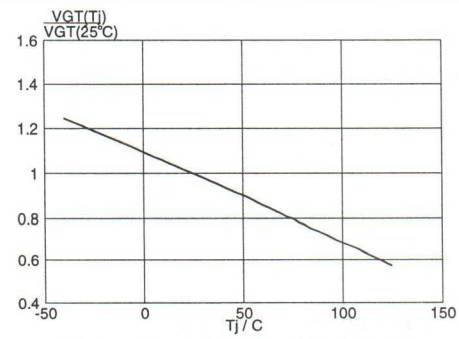



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

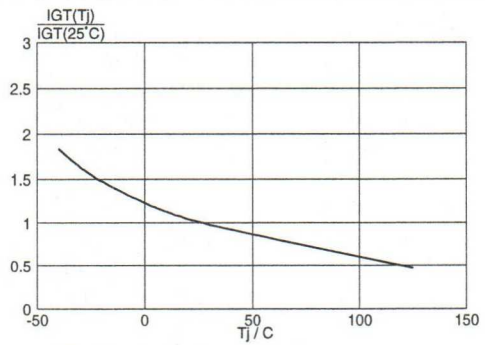



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

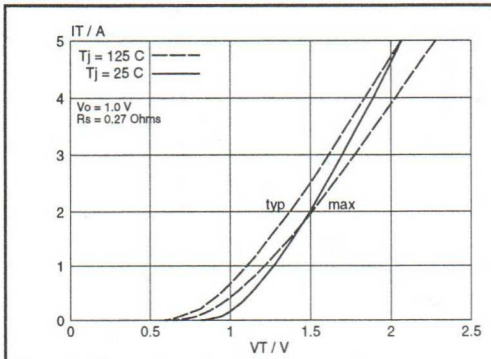



*Fig.10. Typical and maximum on-state characteristic.*

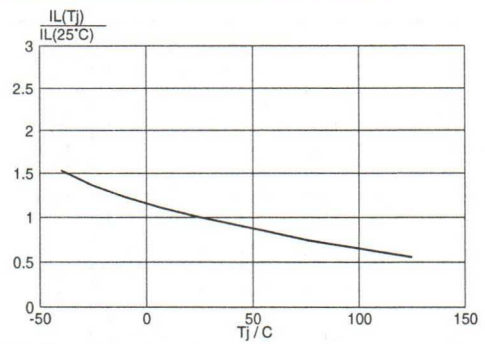



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

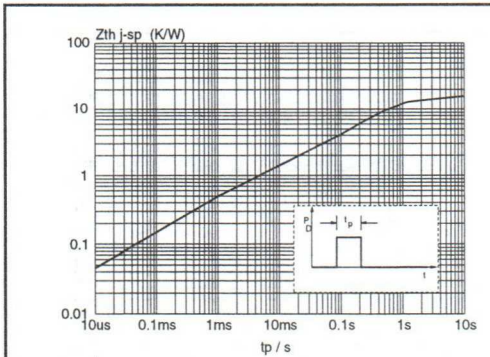



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width $t_p$.*

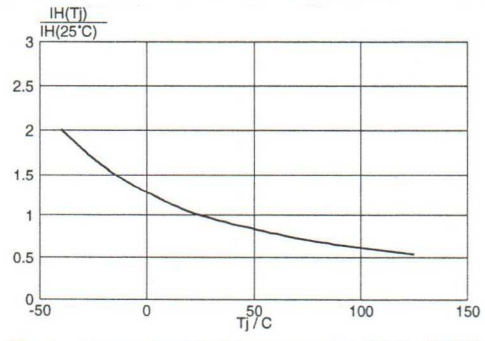



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$, $R_{GK}$ = 1 kΩ.*

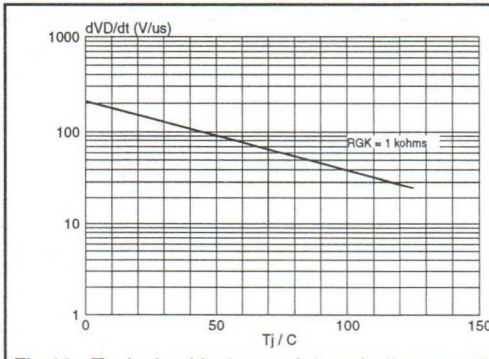



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

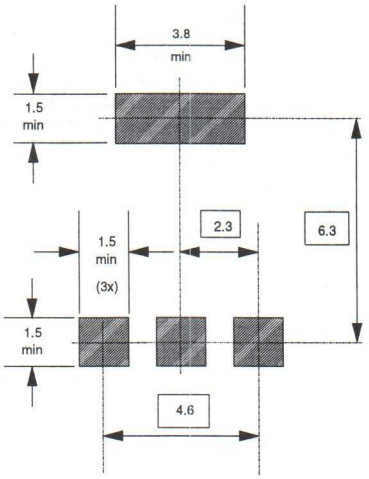



*Fig.13. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

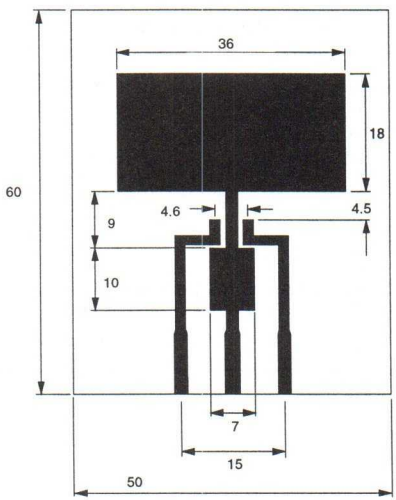



*Fig.14. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

# Thyristors logic level

# BT258 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

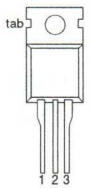
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT258- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 75 | 75 | 75 | A |

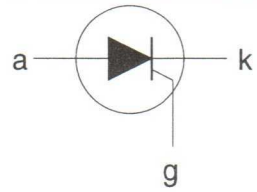
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | | 75 | | A |
| | | t = 8.3 ms | - | | 82 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.4 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.3 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 16 A | - | 1.3 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | 50 | 100 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 24 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

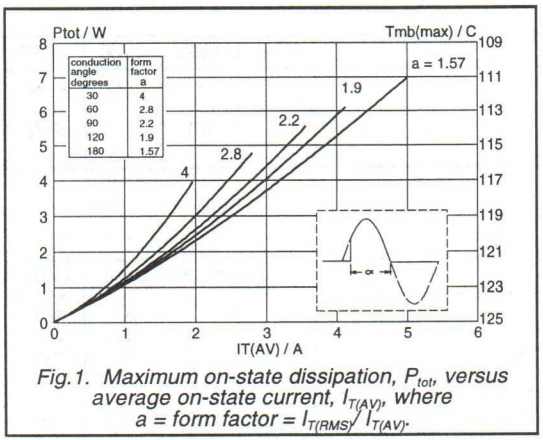



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

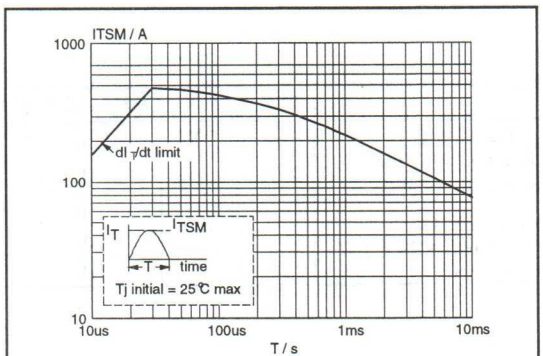



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

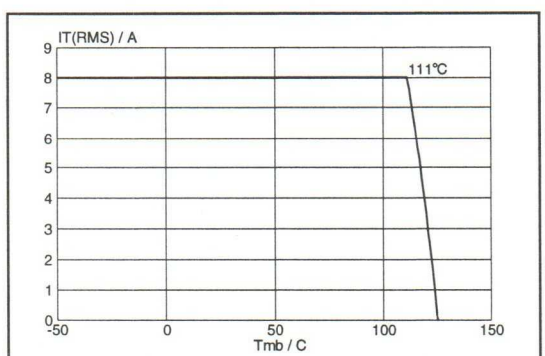



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

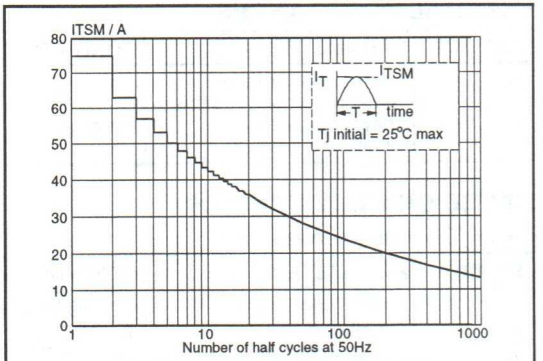



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

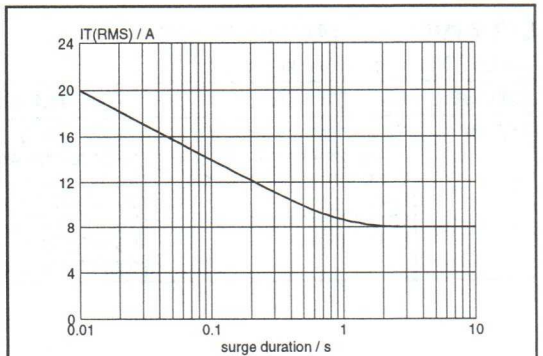



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

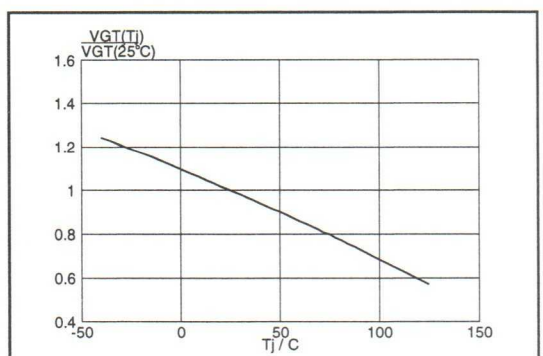



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

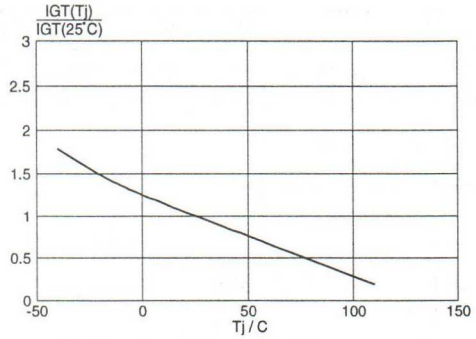



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

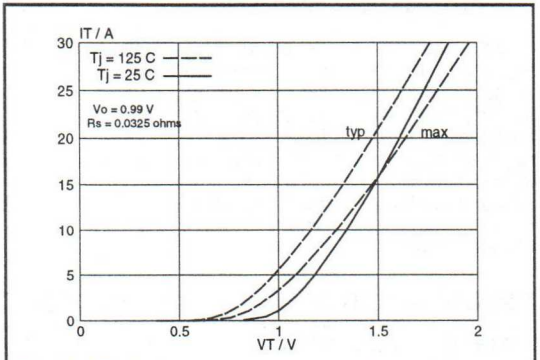



*Fig.10. Typical and maximum on-state characteristic.*

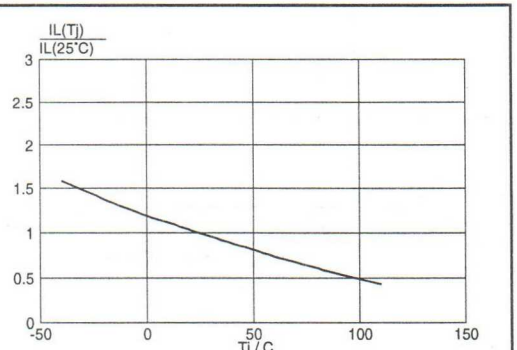



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

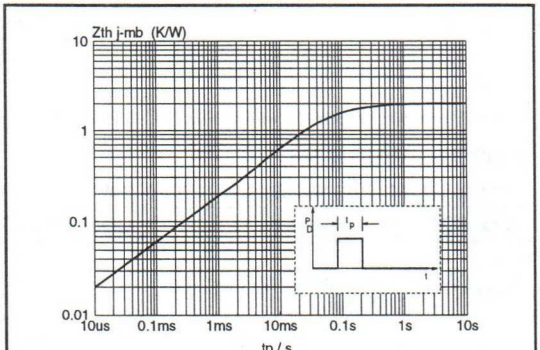



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

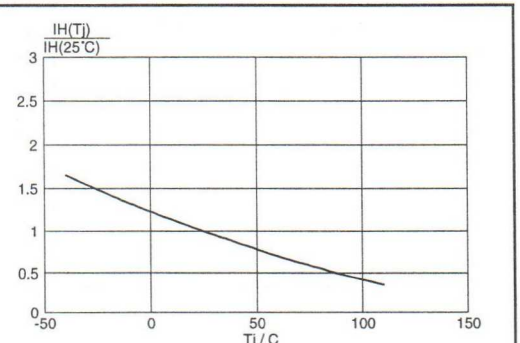



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

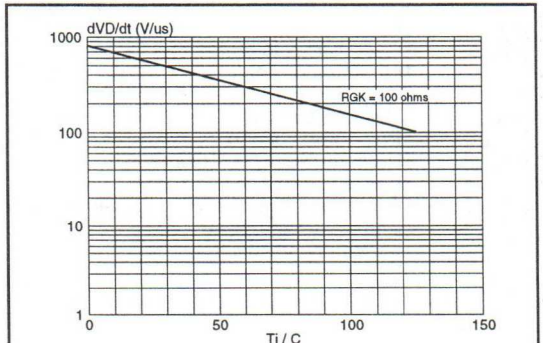



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

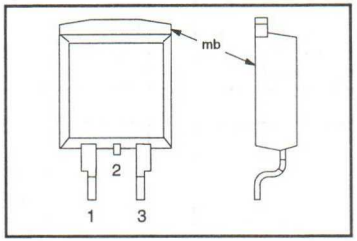
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT258B- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 75 | 75 | 75 | A |

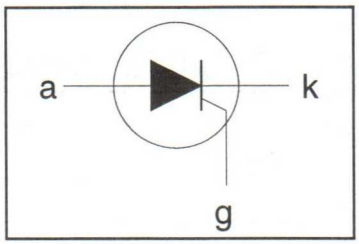
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| mb | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 75 | | A |
| | | t = 8.3 ms | - | | 82 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to heatsink | | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.4 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.3 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 16 A | - | 1.3 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | 50 | 100 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 24 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

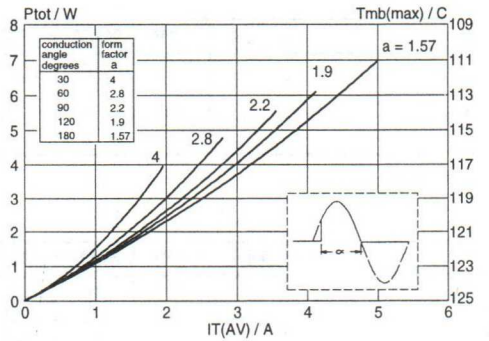



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

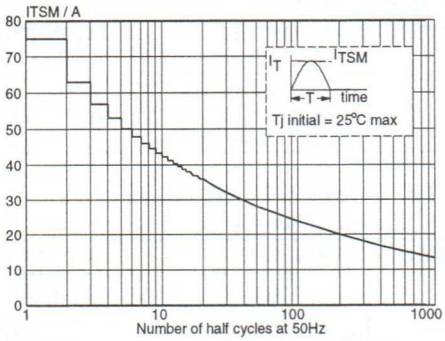



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

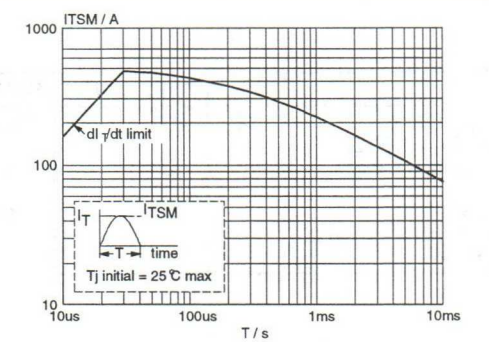



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

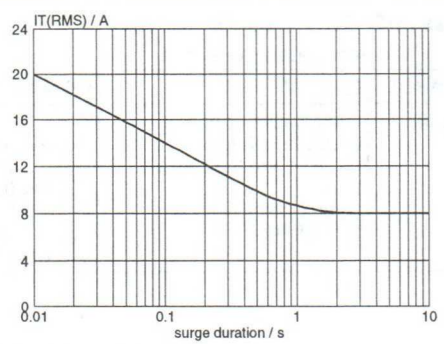



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

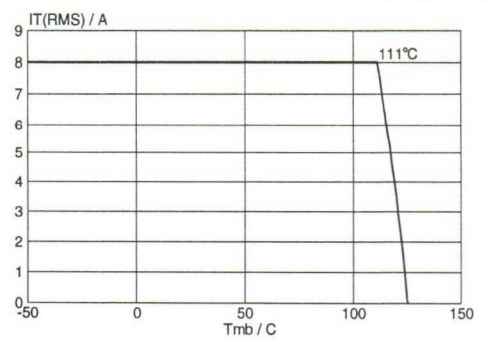



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

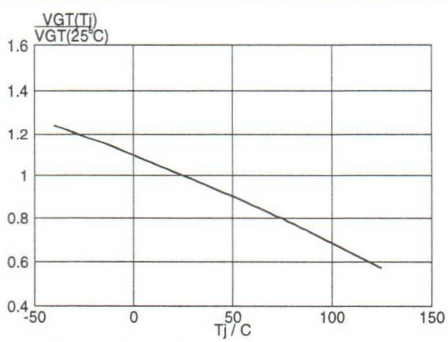



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

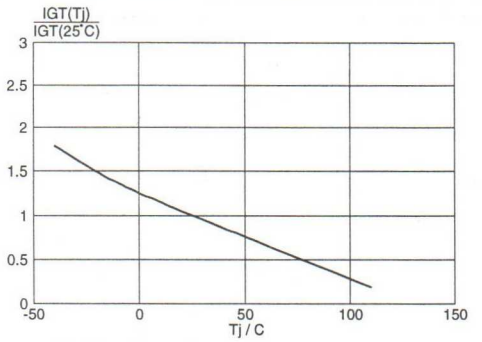



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

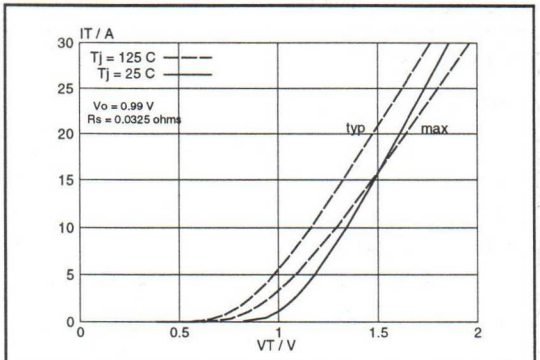



*Fig.10. Typical and maximum on-state characteristic.*

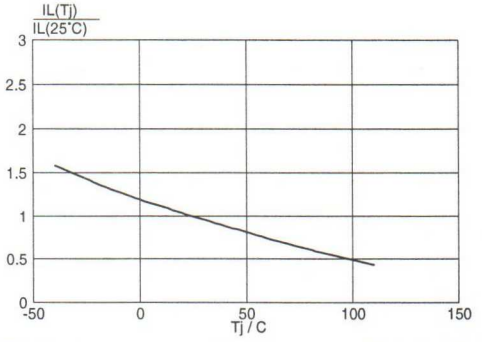



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

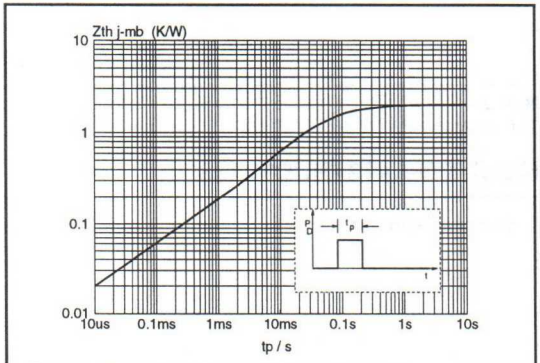



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

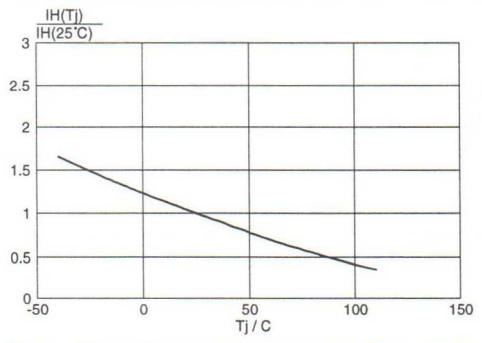



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

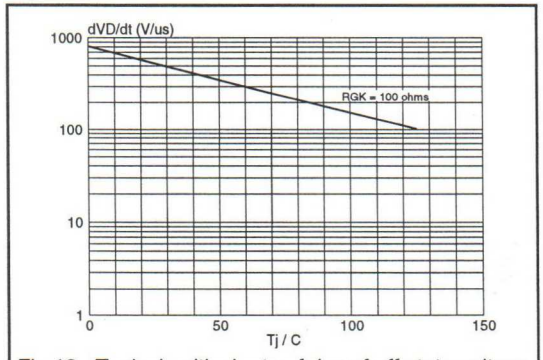



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

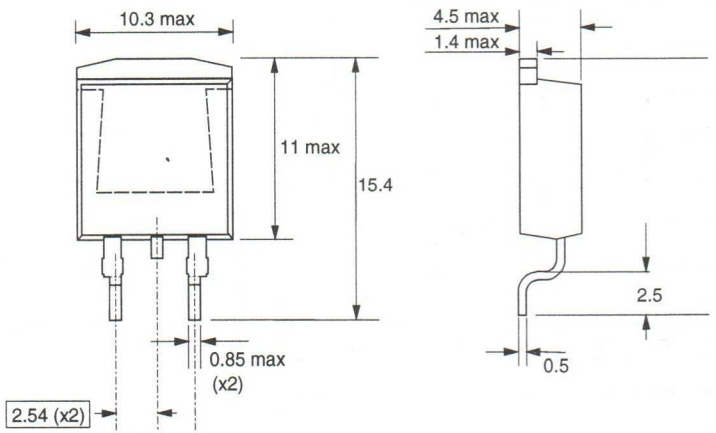



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

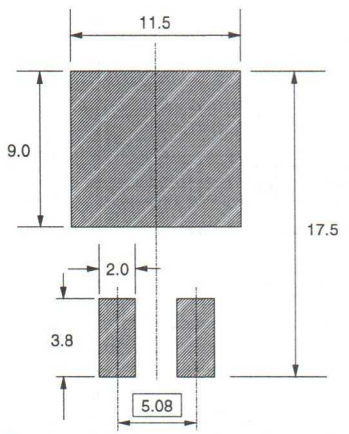



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

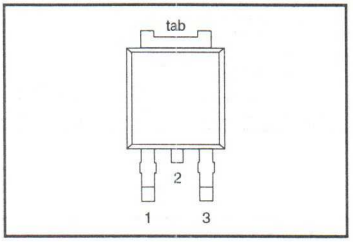
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT258S** (or BT258M)- | **500R** | **600R** | **800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 75 | 75 | 75 | A |

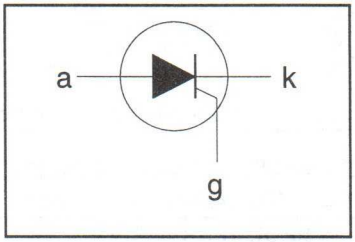
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | cathode | gate |
| 2 | anode | anode |
| 3 | gate | cathode |
| tab | anode | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500R** | **-600R** | **-800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | | 75 | | A |
| | | t = 8.3 ms | - | | 82 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.4 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.3 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 16 A | - | 1.3 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | 50 | 100 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 24 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

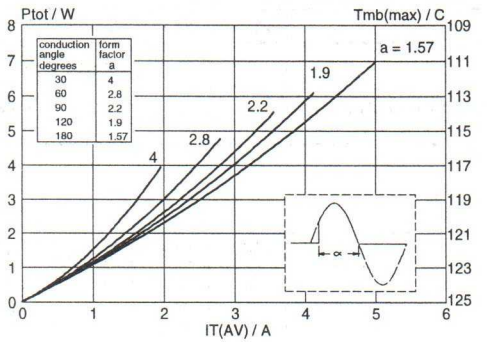



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

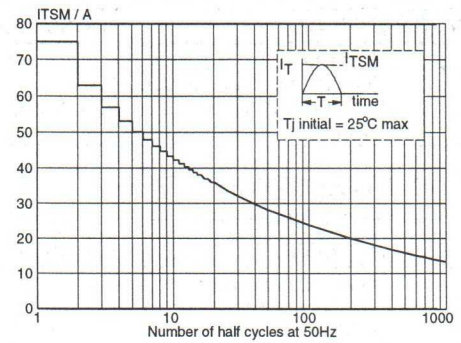



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

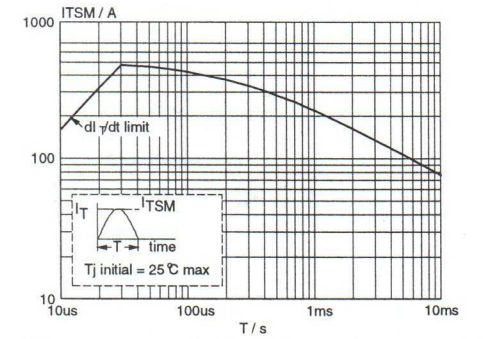



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

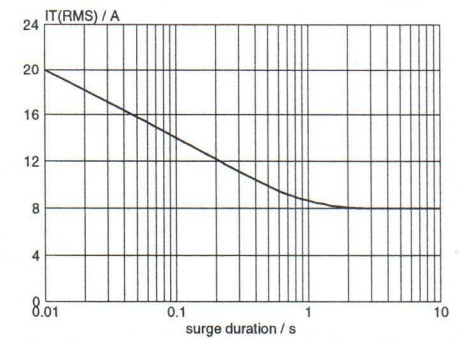



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

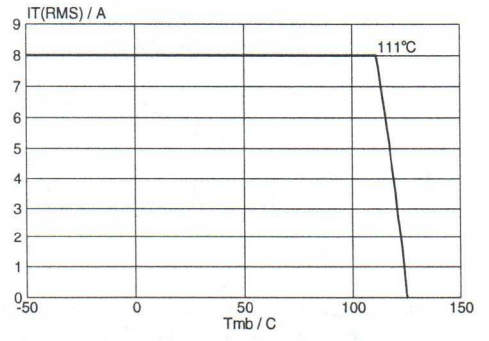



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

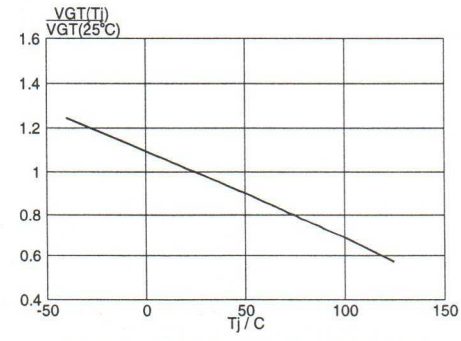



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

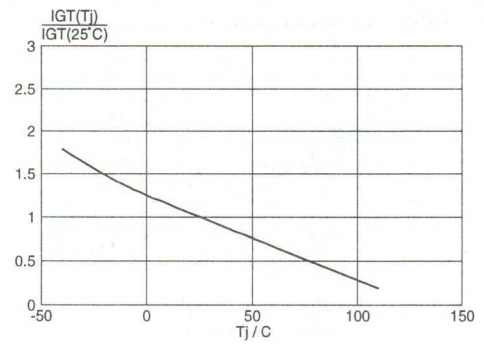



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

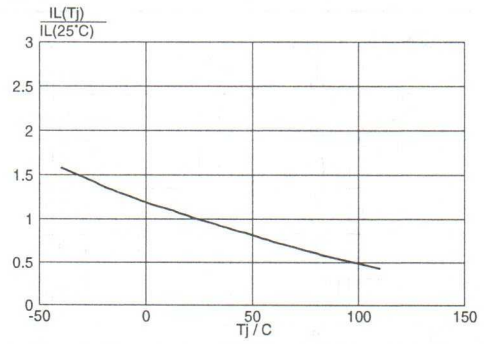



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

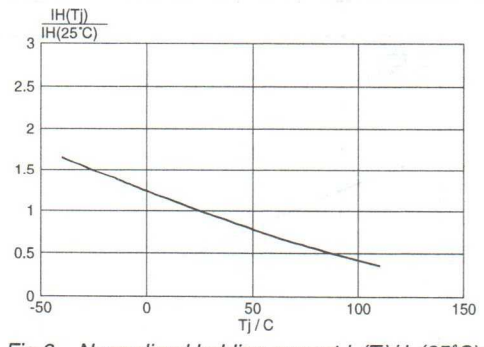



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

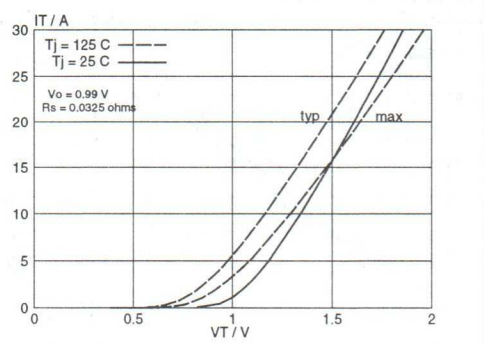



*Fig.10. Typical and maximum on-state characteristic.*

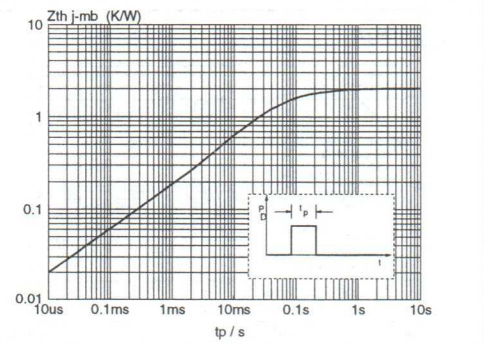



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

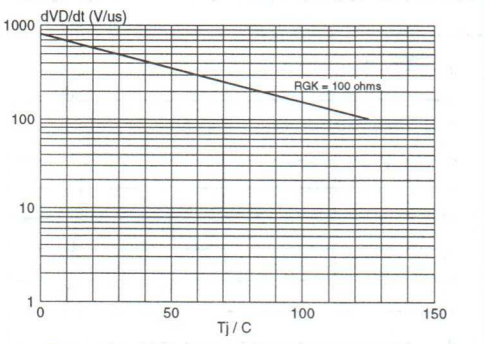



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

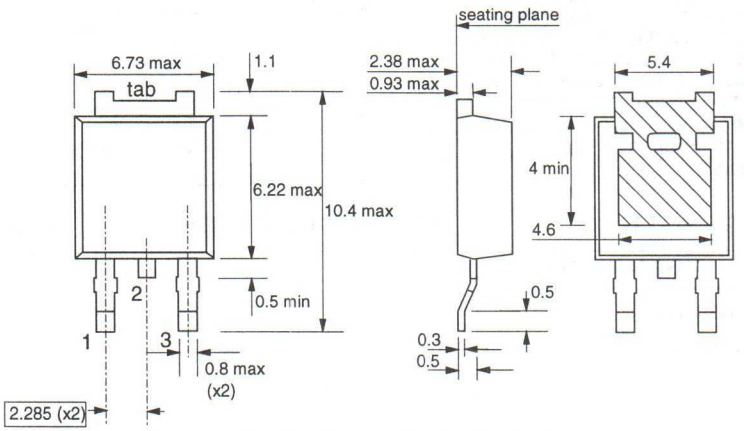



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

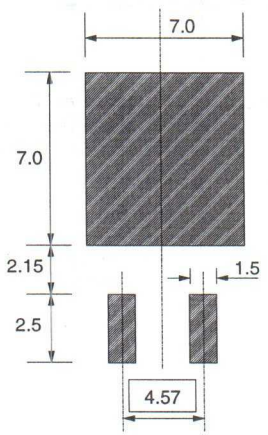



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Thyristors logic level

# BT258X series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a full pack, plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

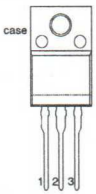
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT258X- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 75 | 75 | 75 | A |

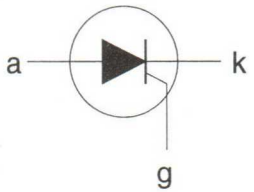
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{hs} \leq 90$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 75 | | A |
| | | t = 8.3 ms | - | | 82 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 28 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125[2] | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | with heatsink compound | - | - | 5.0 | K/W |
| | | without heatsink compound | - | - | 6.9 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 50 | 200 | µA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.4 | 10 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 0.3 | 6 | mA |
| $V_T$ | On-state voltage | $I_T$ = 16 A | - | 1.3 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.4 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.2 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 100 Ω | 50 | 100 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 5 mA; $dI_G/dt$ = 0.2 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 24 V; $dI_{TM}/dt$ = 10 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

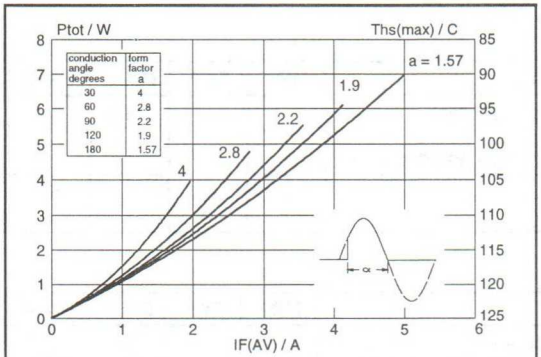



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

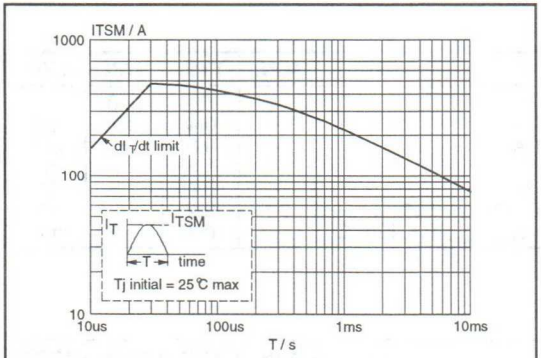



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

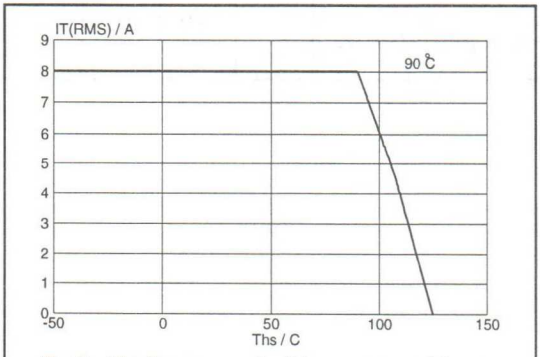



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{hs}$.*

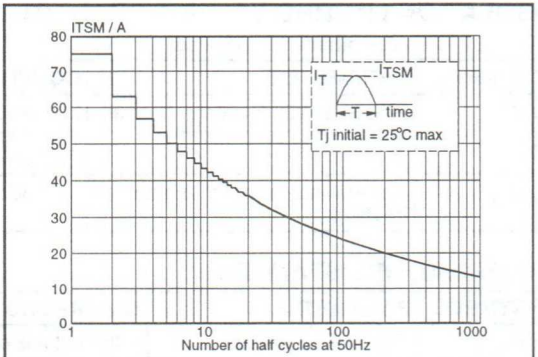



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

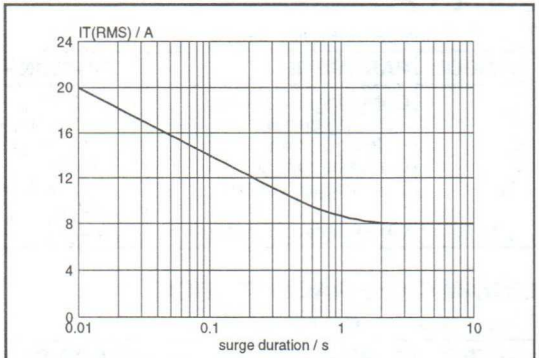



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 90°C$.*

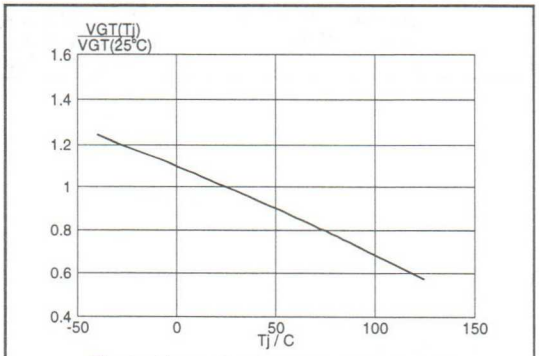



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

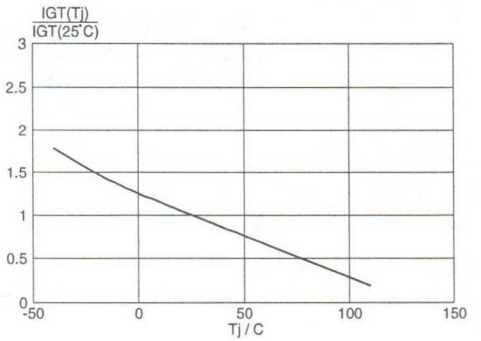



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

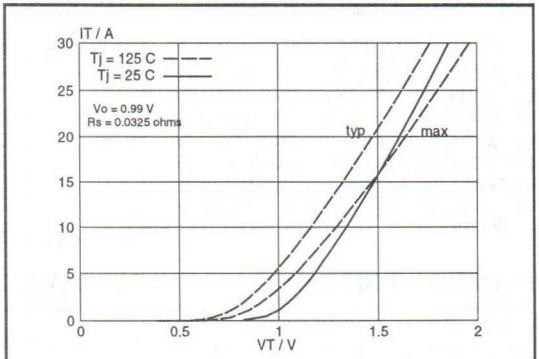



*Fig.10. Typical and maximum on-state characteristic.*

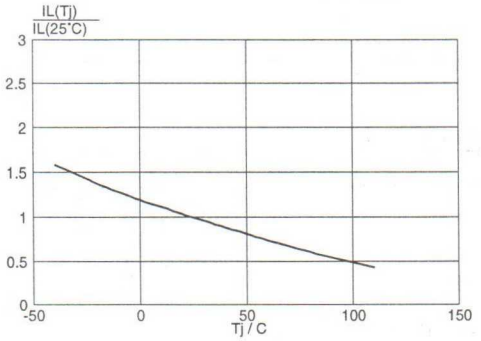



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature $T_j$.*

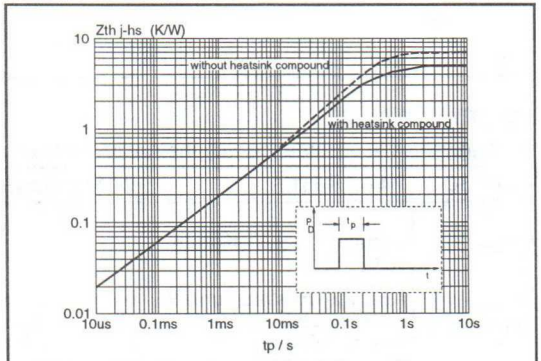



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

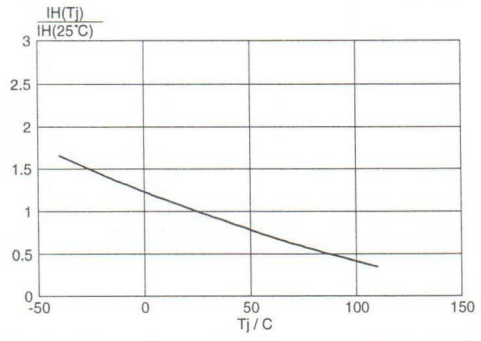



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature $T_j$.*

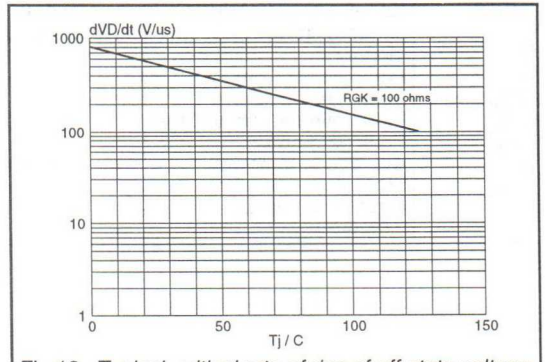



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

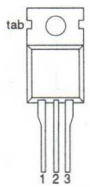
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT300- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

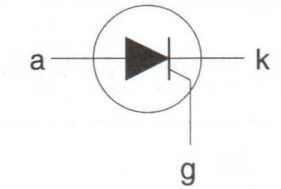
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | 5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | 65 | | | A |
| | | t = 8.3 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | 50 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.8 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 12 A | - | 1.35 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform. | | | | |
| | | Gate open circuit | 50 | 100 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

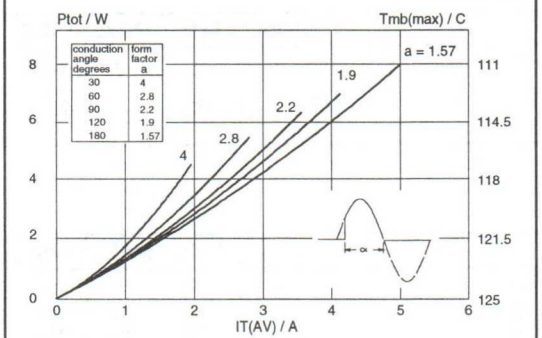



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

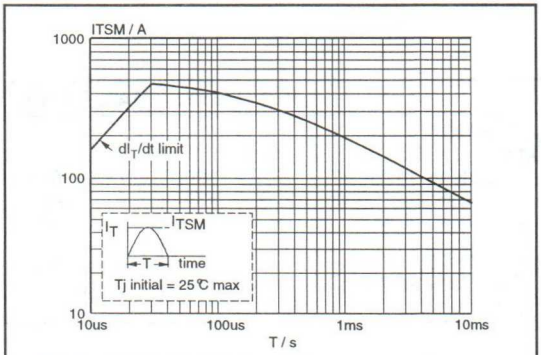



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

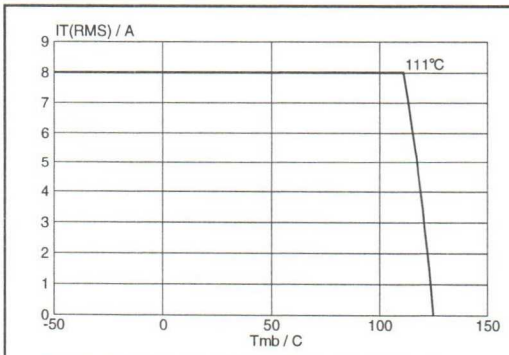



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

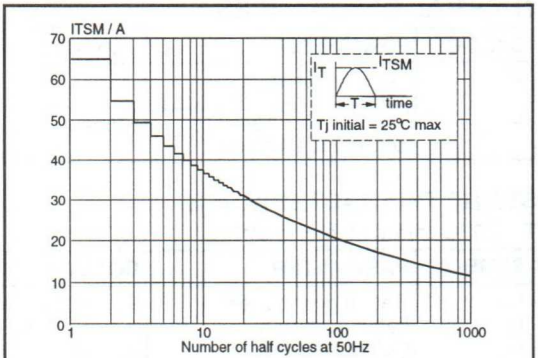



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

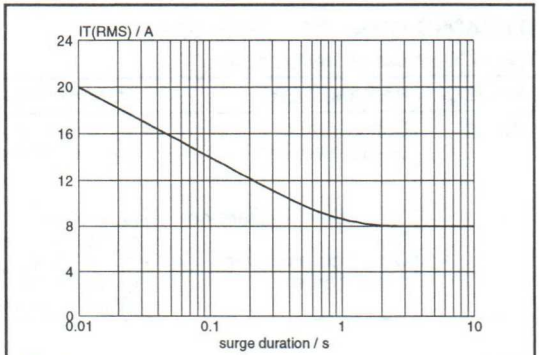



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

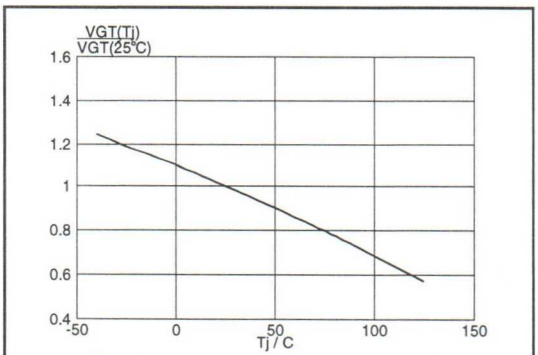



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

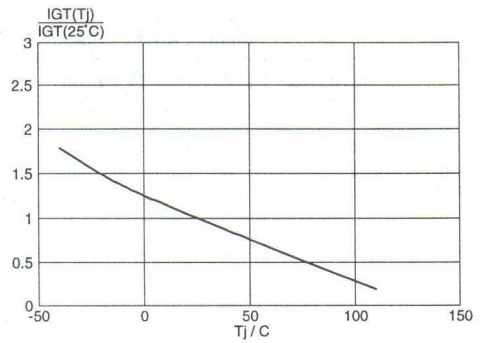



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

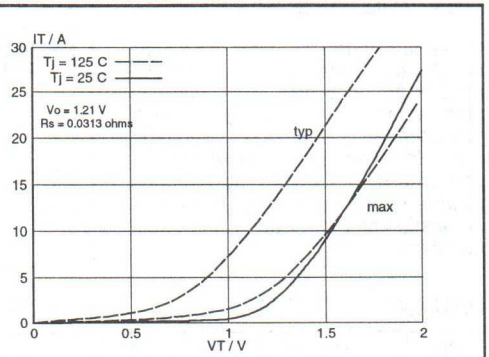



*Fig.10. Typical and maximum on-state characteristic.*

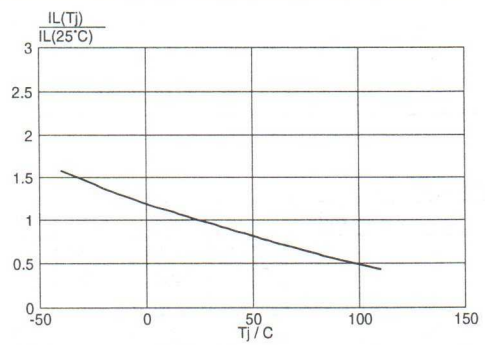



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

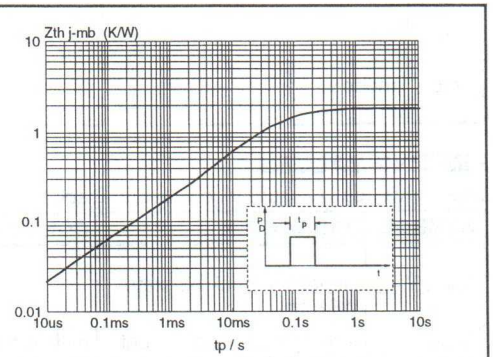



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

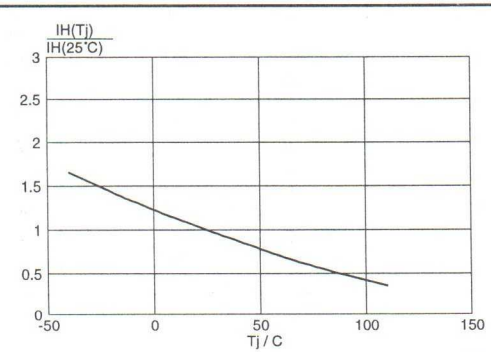



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

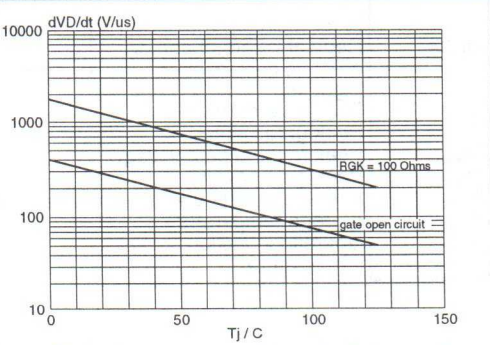



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

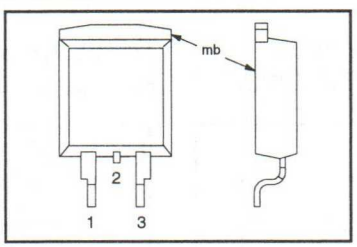
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT300B- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

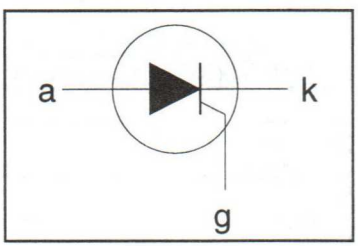
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| mb | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 111$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 65 | | A |
| | | t = 8.3 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.8 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 12 A | - | 1.35 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform. | | | | |
| | | Gate open circuit | 50 | 100 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

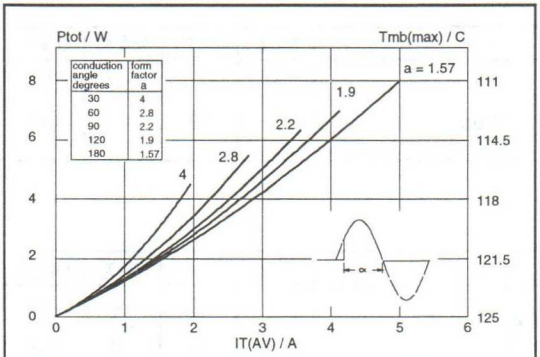



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.*

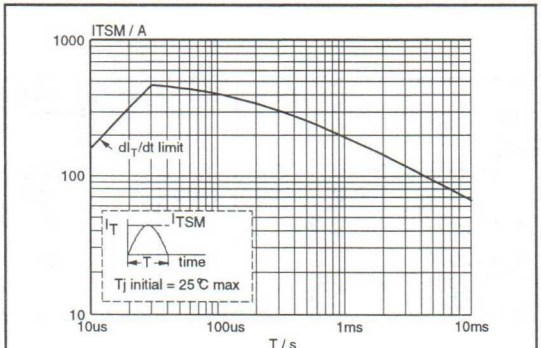



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

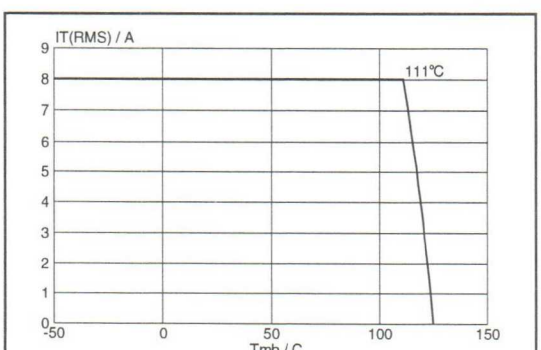



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

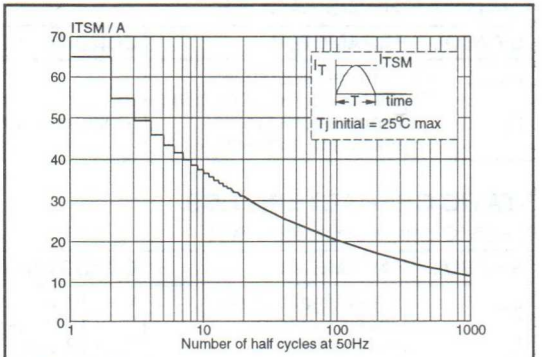



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

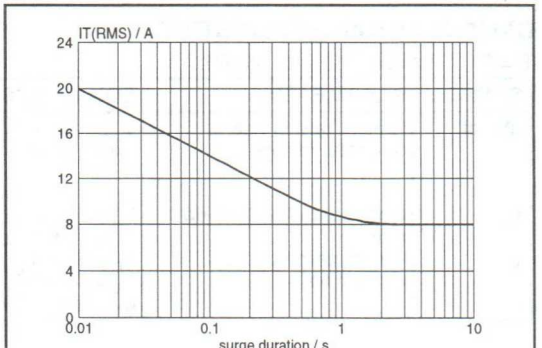



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 111°C$.*

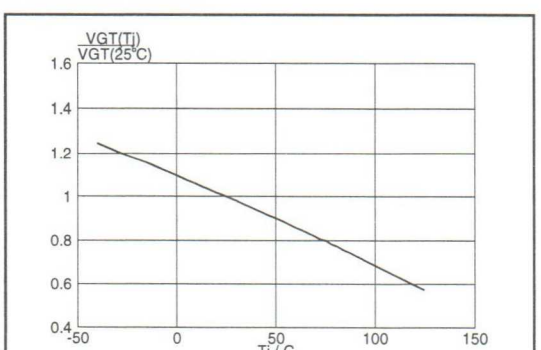



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

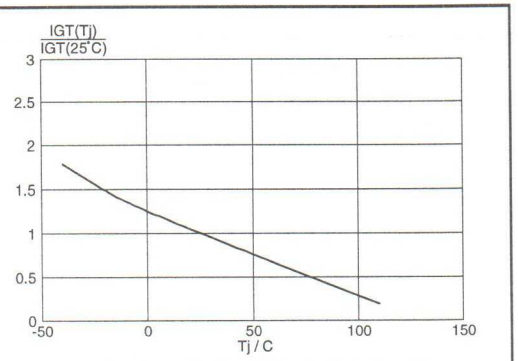



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

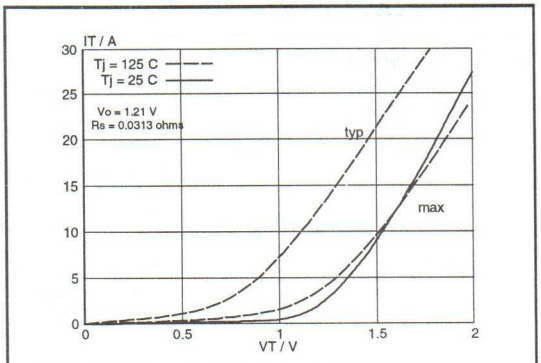



*Fig.10. Typical and maximum on-state characteristic.*

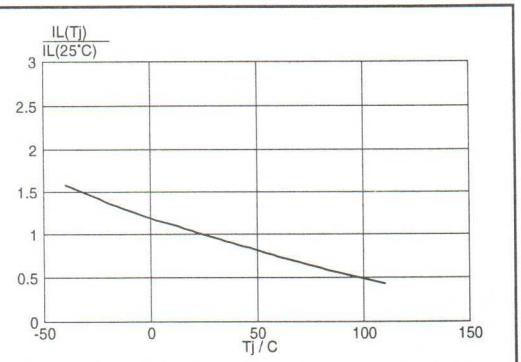



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

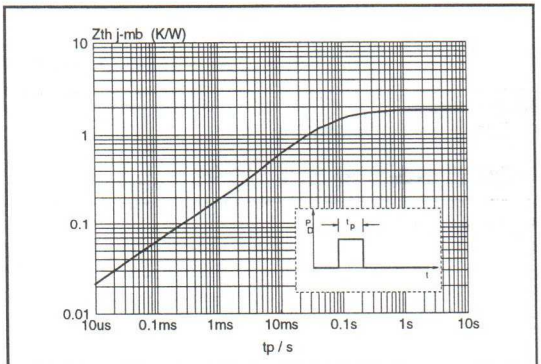



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

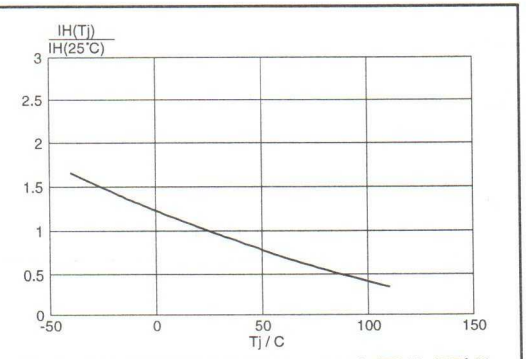



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

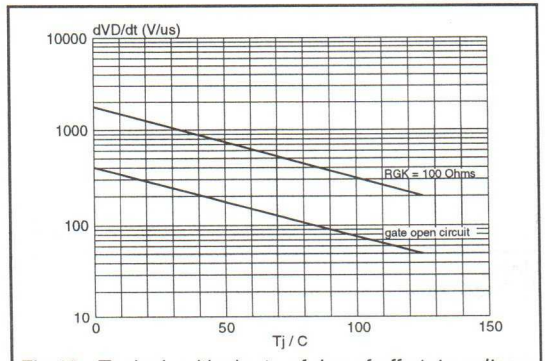



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

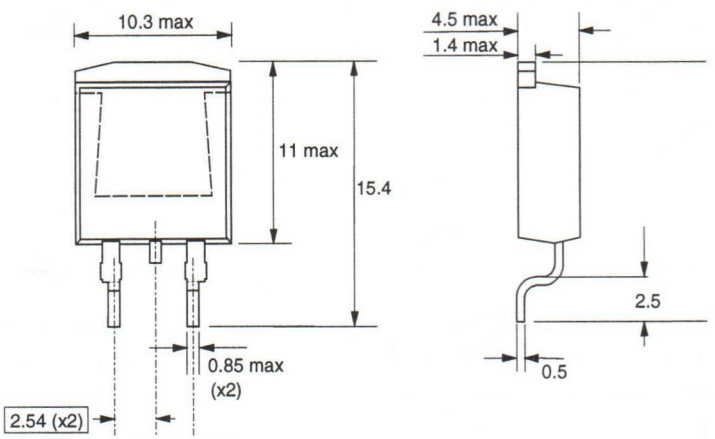



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

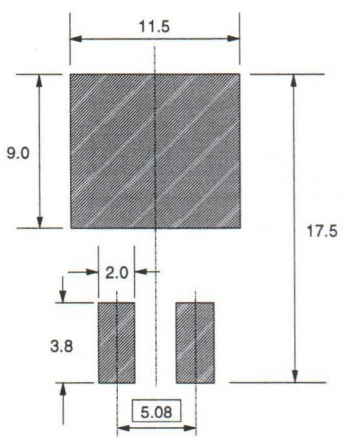



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

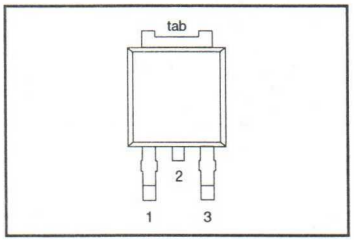
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BT300S** (or BT300M)- | **500R** | **600R** | **800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

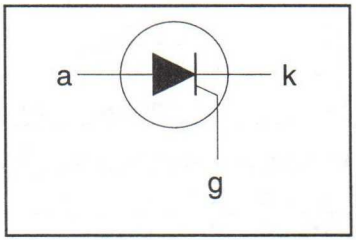
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | cathode | gate |
| 2 | anode | anode |
| 3 | gate | cathode |
| tab | anode | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500R** | **-600R** | **-800R** | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 107$ °C | - | | 5 | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | | 65 | | A |
| | | t = 8.3 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | | 50 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 2.2 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 12 A | - | 1.35 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform. | | | | |
| | | Gate open circuit | 50 | 100 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

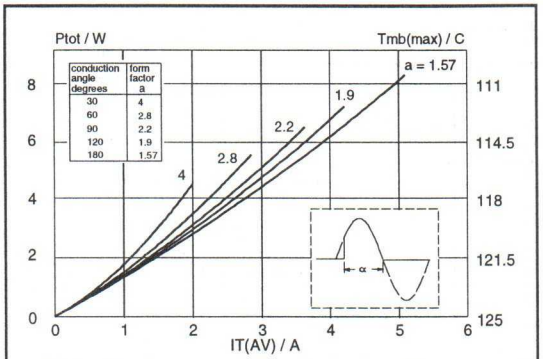



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

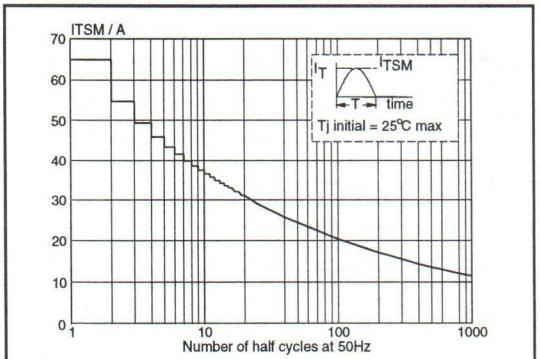



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

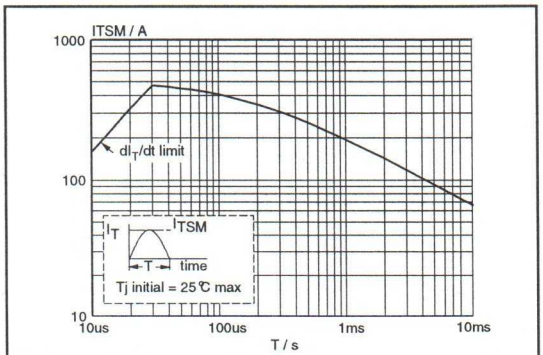



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

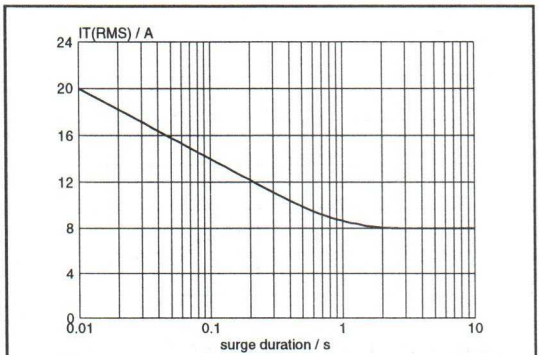



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.*

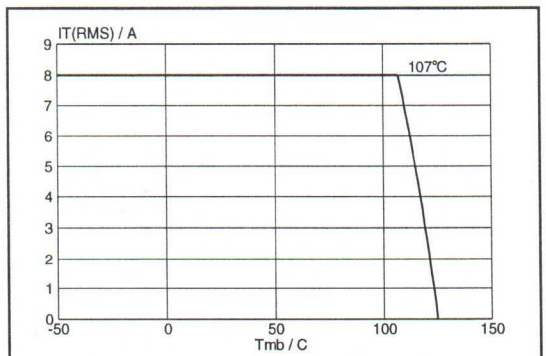



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

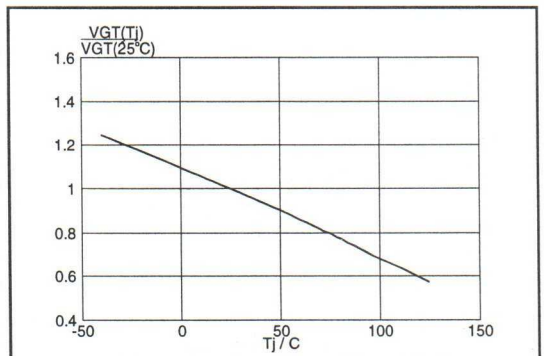



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

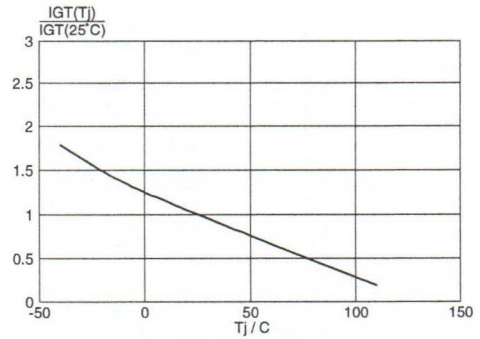



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

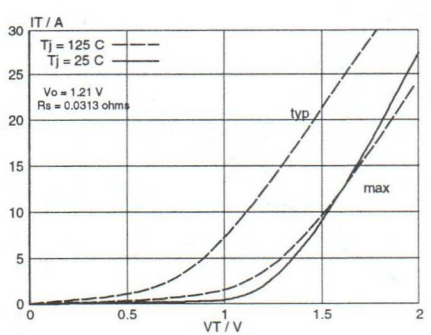



*Fig.10. Typical and maximum on-state characteristic.*

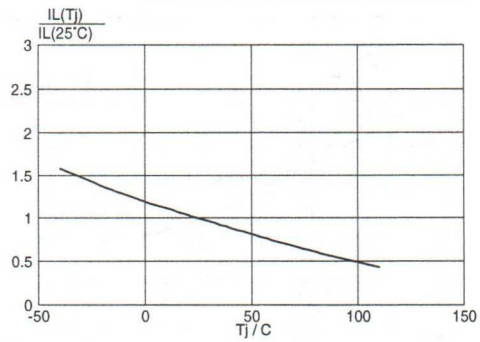



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

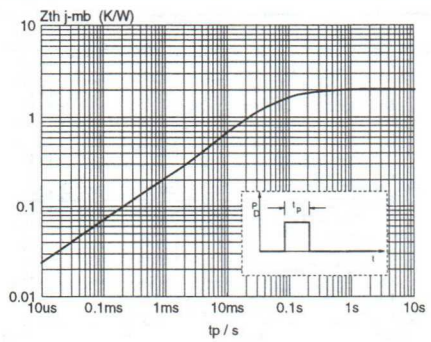



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

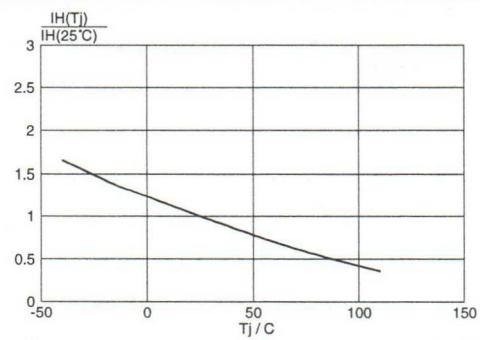



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

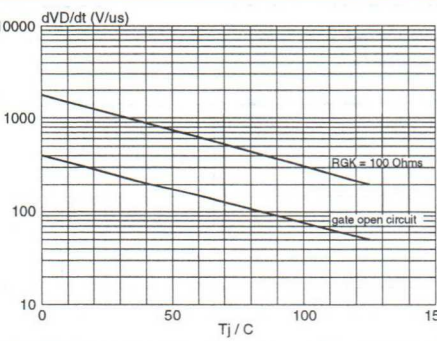



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

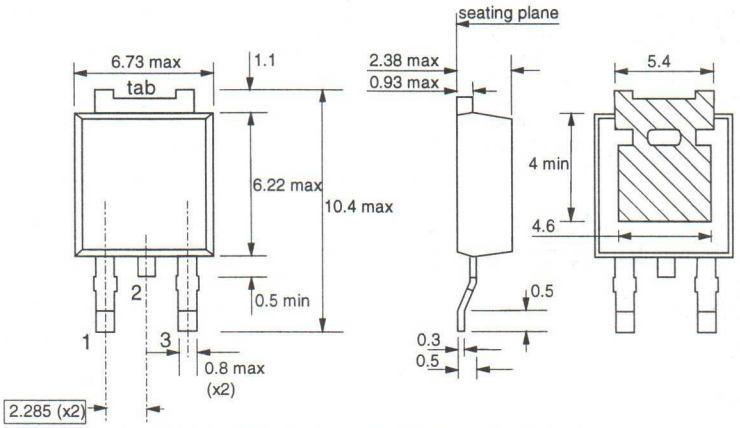



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

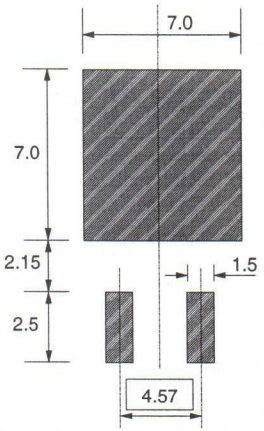



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

## GENERAL DESCRIPTION

Glass passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

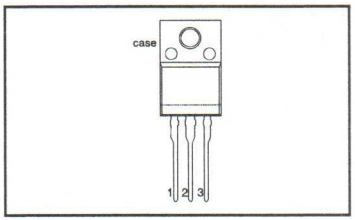
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT300X- | 500R | 600R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5 | 5 | 5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

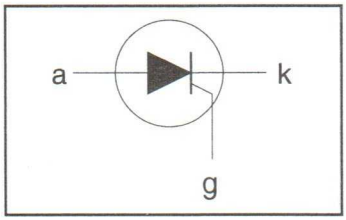
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -600R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{hs} \leq 79$ °C | - | 5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 10 ms | - | 65 | | | A |
| | | t = 8.3 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 10 A; $I_G$ = 50 mA; $dI_G/dt$ = 50 mA/µs | - | 50 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | with heatsink compound | - | - | 5.7 | K/W |
| | | without heat sink compound | - | - | 9.3 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 15 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 20 | mA |
| $V_T$ | On-state voltage | $I_T$ = 12 A | - | 1.35 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform. | | | | |
| | | Gate open circuit | 50 | 100 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 10 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 12 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

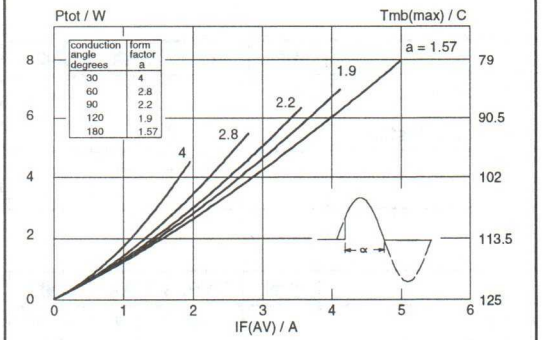



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.*

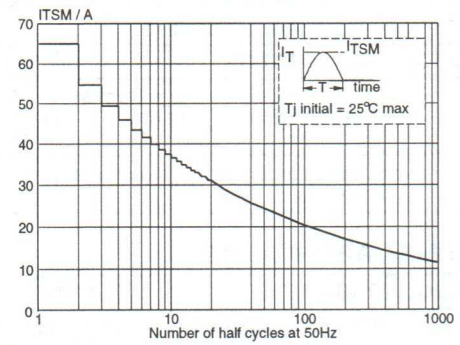



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

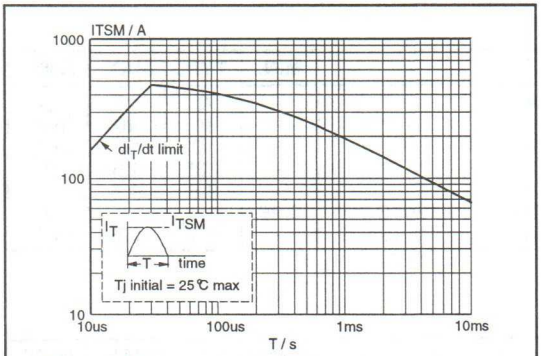



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 10ms$.*

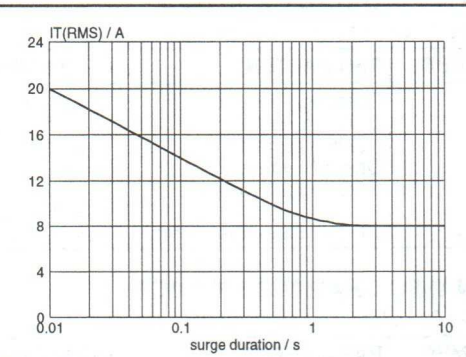



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 79°C$.*

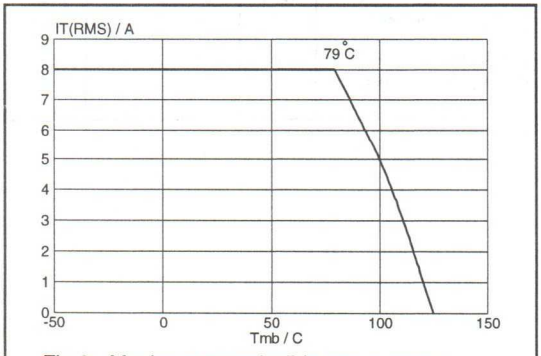



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{hs}$.*

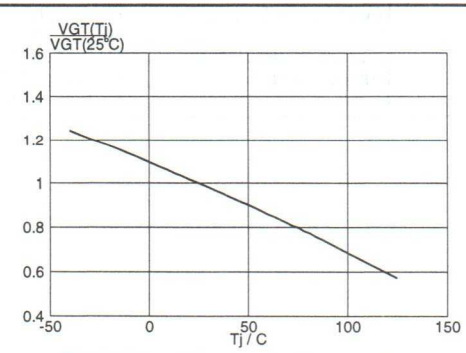



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

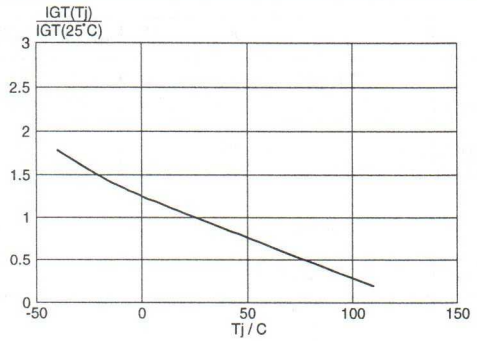



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

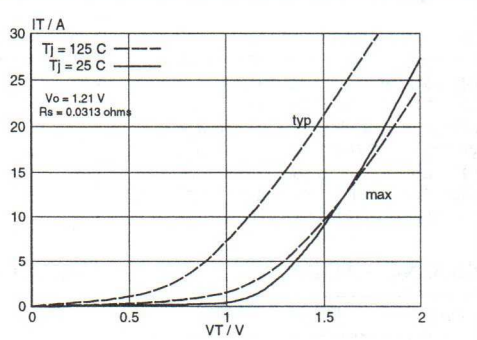



*Fig.10. Typical and maximum on-state characteristic.*

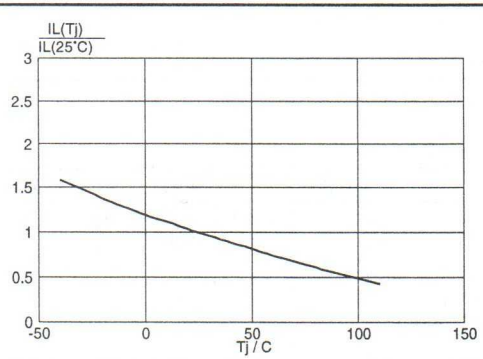



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

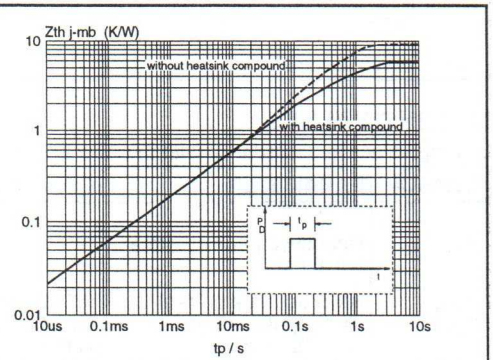



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

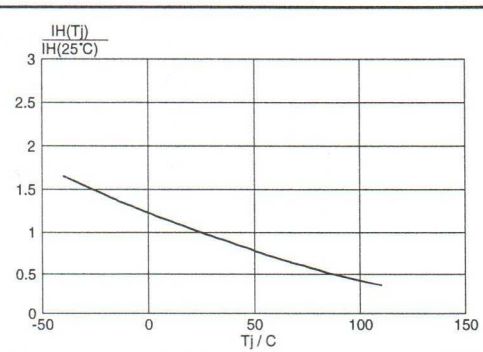



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

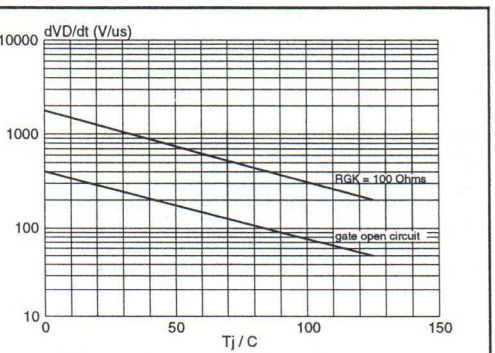



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

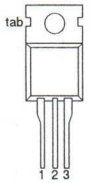
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA140-** | **500** | **600** | **800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 190 | 190 | 190 | A |

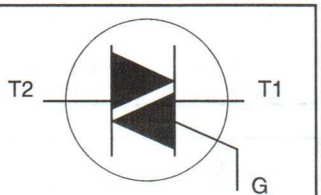
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 6 | 35 | mA |
| | | | T2+ G- | - | 10 | 35 | mA |
| | | | T2- G- | - | 11 | 35 | mA |
| | | | T2- G+ | - | 23 | 70 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 8 | 40 | mA |
| | | | T2+ G- | - | 30 | 60 | mA |
| | | | T2- G- | - | 18 | 40 | mA |
| | | | T2- G+ | - | 15 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ | - | 7 | 30 | mA |
| | | | T2- | - | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.3 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 300 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 25 A; $dI_{com}/dt$ = 9 A/ms; gate open circuit | - | 10 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

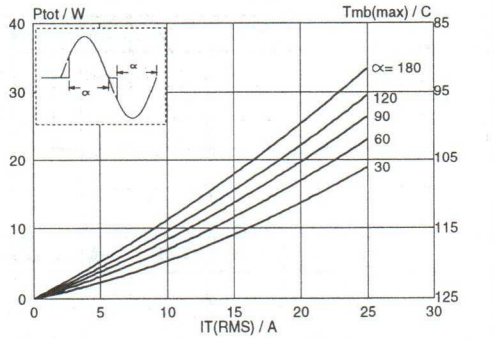



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

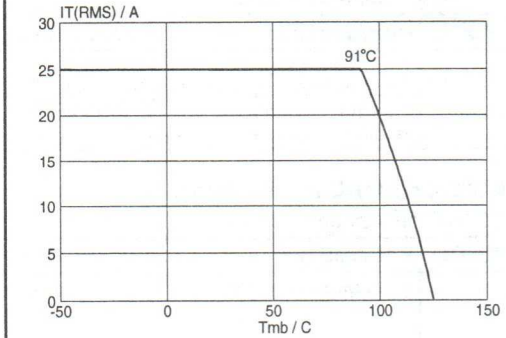



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

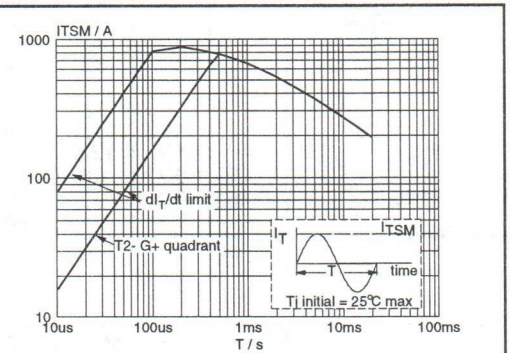



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

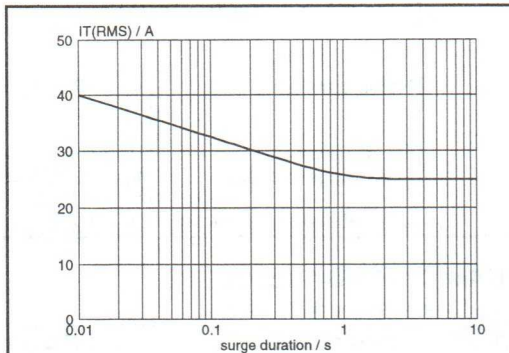



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 91°C$.*

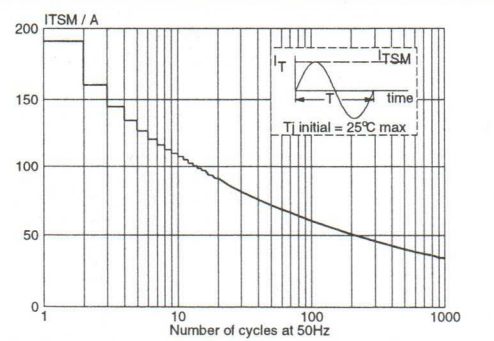



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

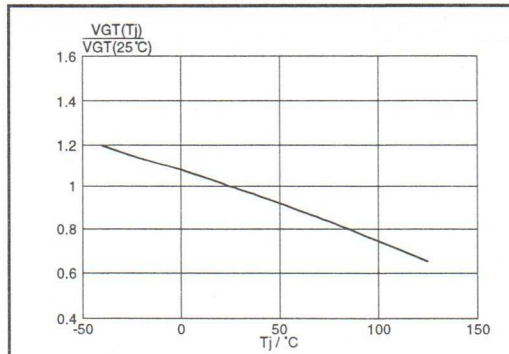



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

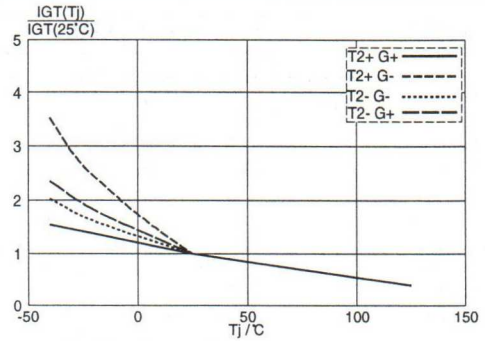



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

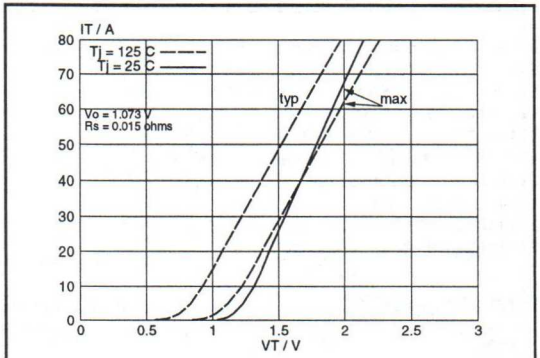



*Fig.10. Typical and maximum on-state characteristic.*

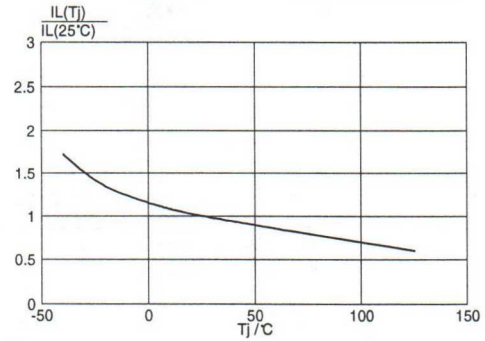



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

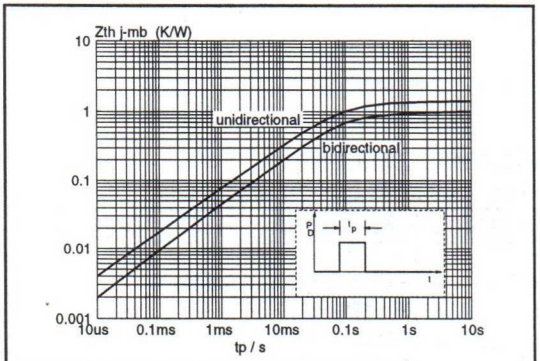



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

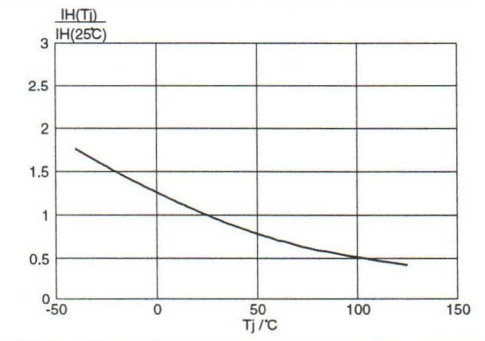



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

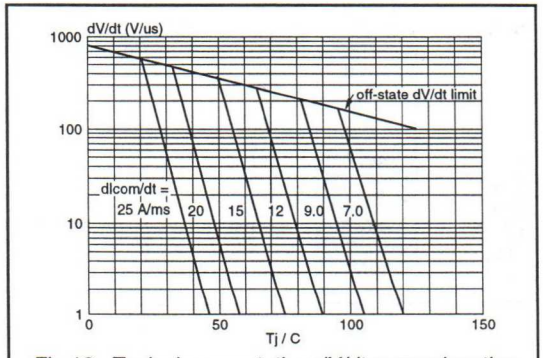



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

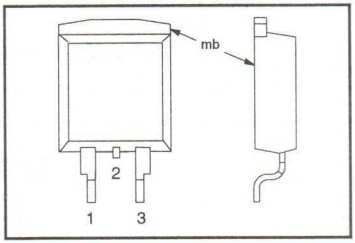
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | BTA140B- | 500 | 600 | 800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | | 190 | 190 | 190 | A |

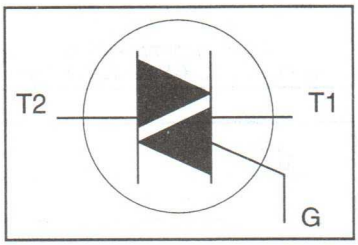
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 30 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 6 | 35 | mA |
| | | | T2+ G- | - | 10 | 35 | mA |
| | | | T2- G- | - | 11 | 35 | mA |
| | | | T2- G+ | - | 23 | 70 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 8 | 40 | mA |
| | | | T2+ G- | - | 30 | 60 | mA |
| | | | T2- G- | - | 18 | 40 | mA |
| | | | T2- G+ | - | 15 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ | - | 7 | 30 | mA |
| | | | T2- | - | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.2 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 100 | 300 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 °C; $I_{T(RMS)}$ = 25 A; $dI_{com}/dt$ = 9 A/ms; gate open circuit | - | 10 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

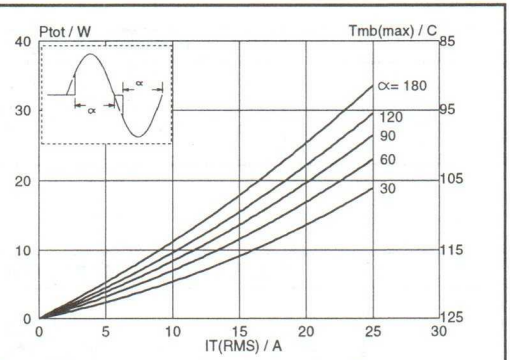



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

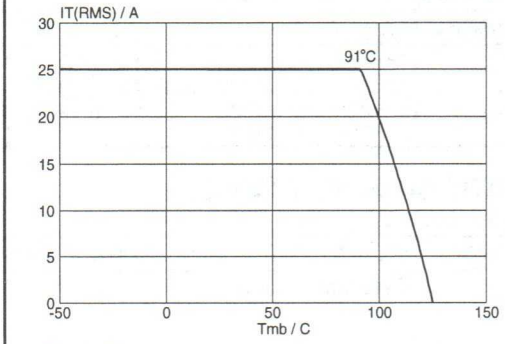



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

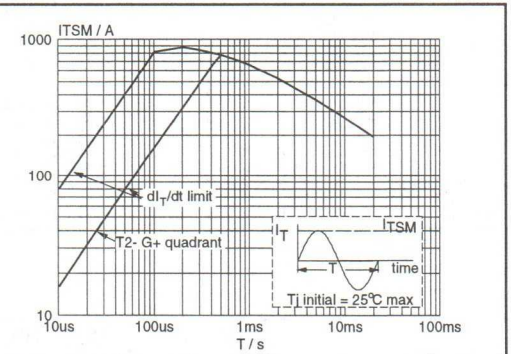



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

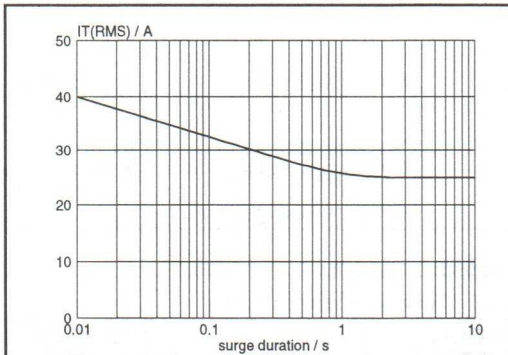



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 91°C$.*

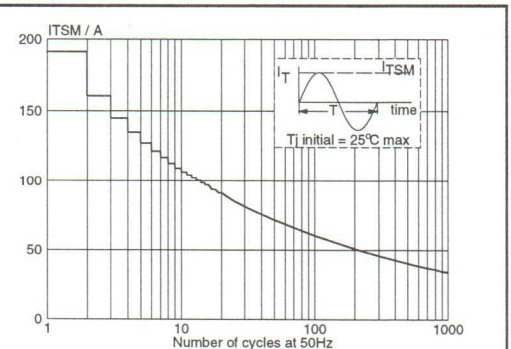



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

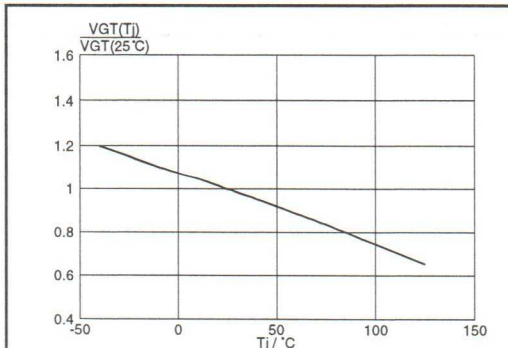



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

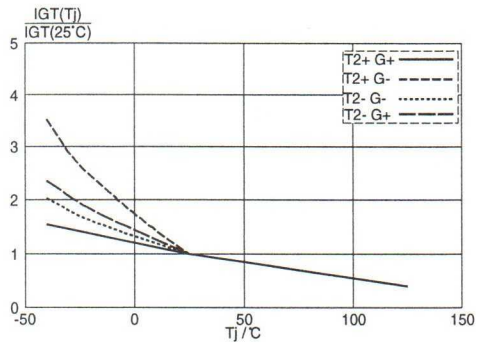



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature $T_j$.*

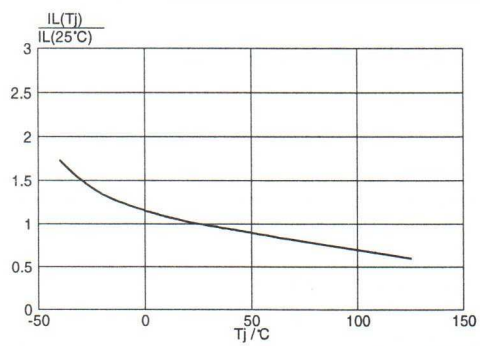



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature $T_j$.*

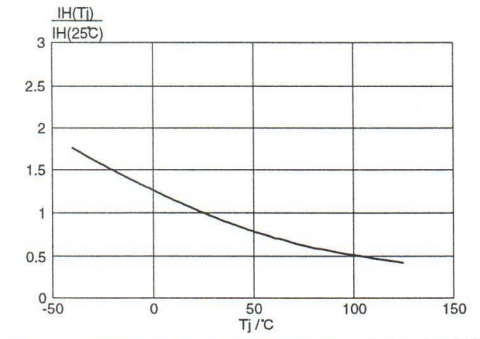



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature $T_j$.*

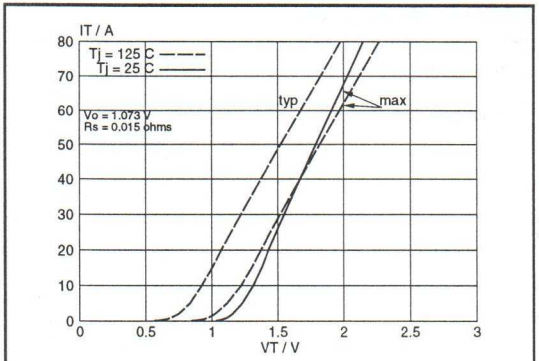



*Fig.10. Typical and maximum on-state characteristic.*

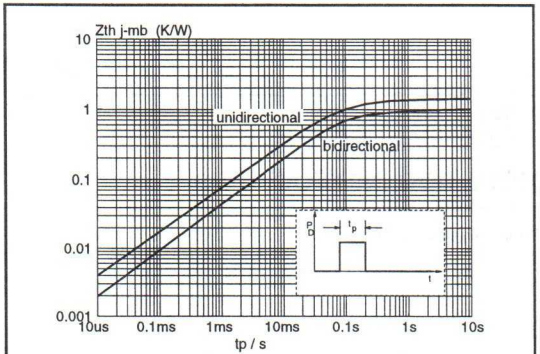



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

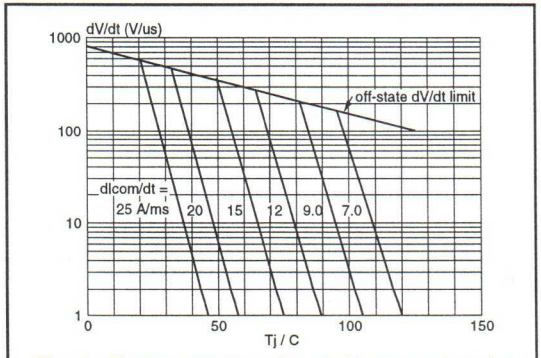



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

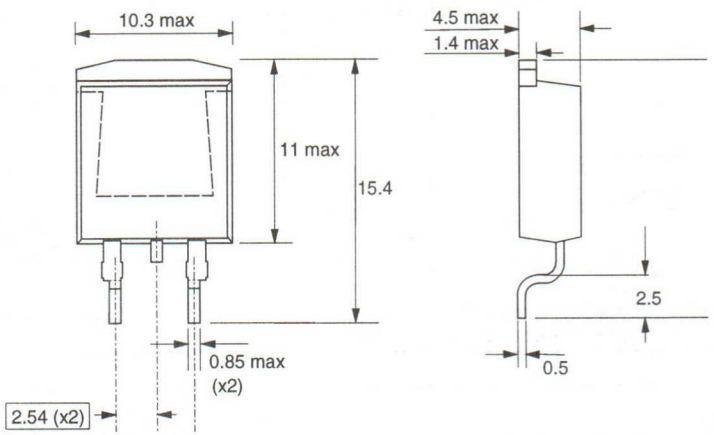



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

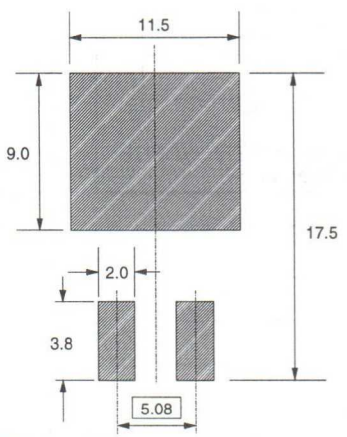



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Thyristors sensitive gate

# BTA151 series

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications.

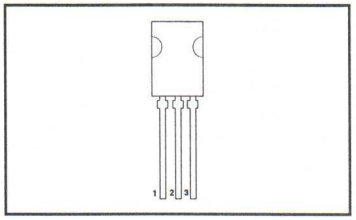
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA151- | 500R | 650R | 800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 500 | 650 | 800 | V |
| $I_{T(AV)}$ | Average on-state current | 7.5 | 7.5 | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

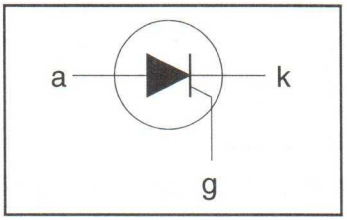
## PINNING - SOT82

| PIN | DESCRIPTION |
|---|---|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| tab | anode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500R | -650R | -800R | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 650[1] | 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 109$ °C | - | 7.5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 10 ms | - | 100 | | | A |
| | | t = 8.3 ms | - | 110 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 50 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs | - | 50 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 12 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.3 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 2 | 4 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 10 | 40 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 7 | 16 | mA |
| $V_T$ | On-state voltage | $I_T$ = 23 A | - | 1.4 | 1.75 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.6 | 1.5 | V |
| | | $V_D = V_{DRM(max)}$; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_D = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform | | | | |
| | | Gate open circuit | 50 | 130 | - | V/µs |
| | | $R_{GK}$ = 100 Ω | 200 | 1000 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 40 A; $V_D = V_{DRM}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_D = 67\%\ V_{DRM(max)}$; $I_{TM}$ = 20 A; $V_R$ = 25 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 50 V/µs; $R_{GK}$ = 100 Ω | - | 70 | - | µs |

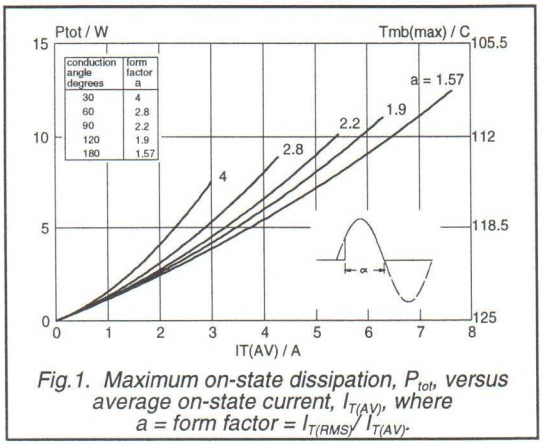



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.*

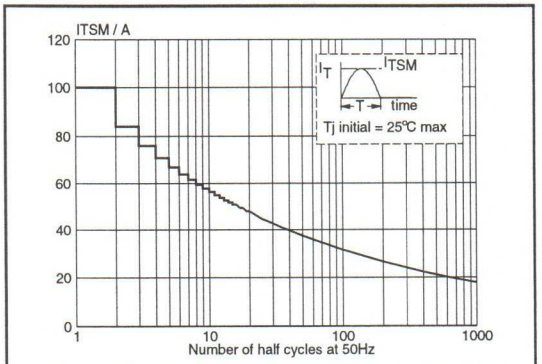



*Fig.4. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

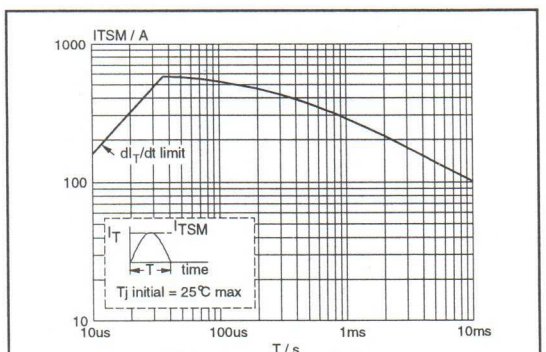



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq$ 10ms.*

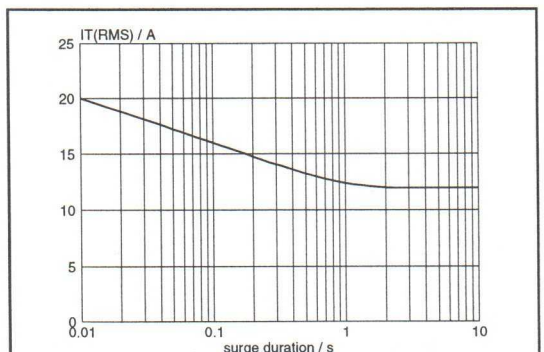



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 109˚C.*

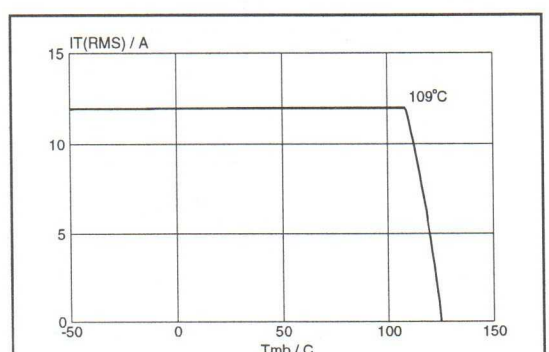



*Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

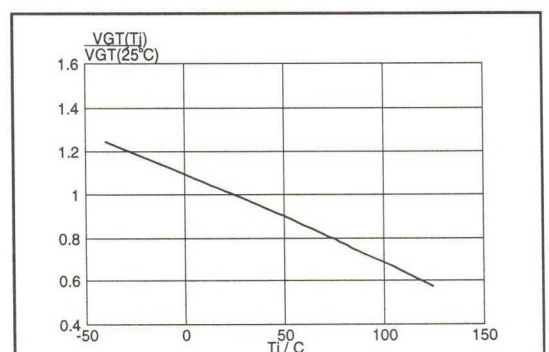



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature $T_j$.*

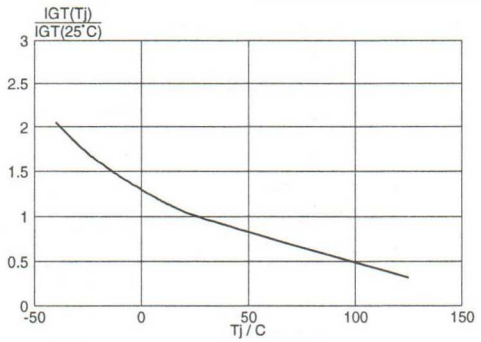



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature $T_j$.*

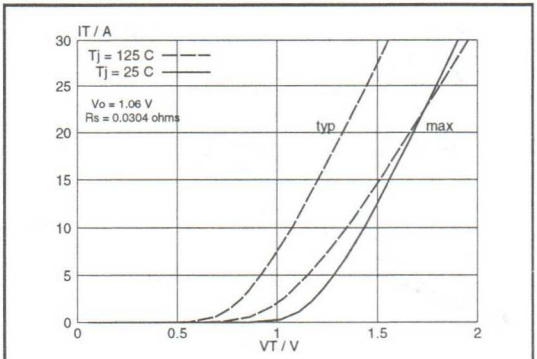



*Fig.10. Typical and maximum on-state characteristic.*

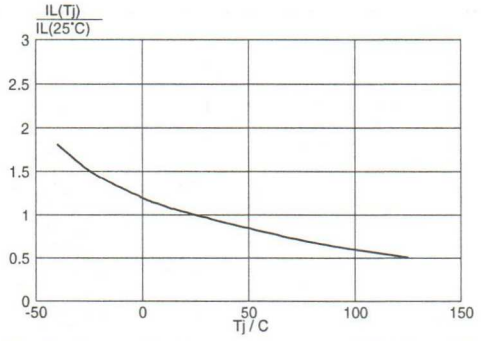



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature $T_j$.*

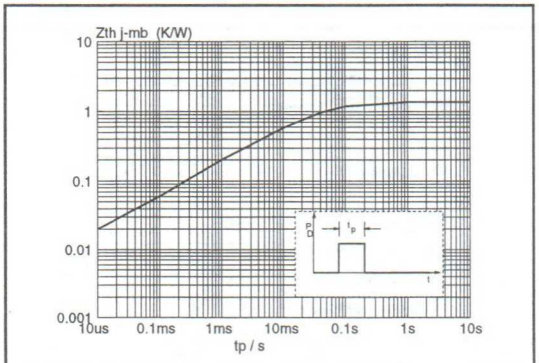



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

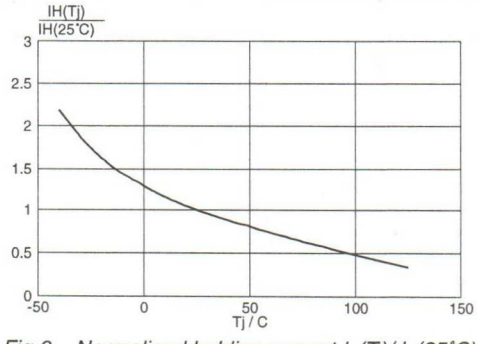



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature $T_j$.*

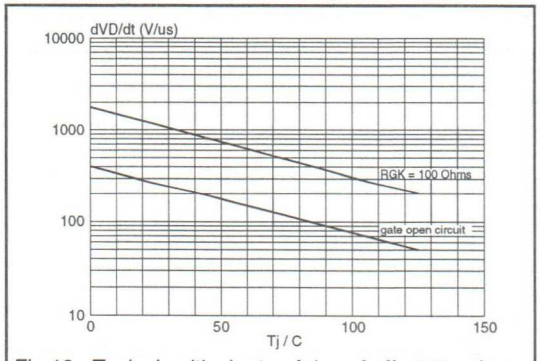



*Fig.12. Typical, critical rate of rise of off-state voltage, $dV_D/dt$ versus junction temperature $T_j$.*

# Three quadrant triacs high commutation

# BTA204 series B and C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.

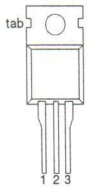
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA204- | 500B | 600B | 800B | |
| | BTA204- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

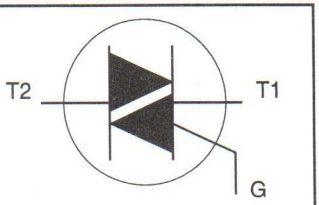
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Objective specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | UNIT |
|---|---|---|---|---|---|---|---|
| | | BTA204- | | | ...B | ...C | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | - | - | 50 | 35 | mA |
| | | T2+ G+ | - | - | 50 | 35 | mA |
| | | T2+ G- | - | - | 50 | 35 | mA |
| | | T2- G- | | | | | |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | - | - | 30 | 20 | mA |
| | | T2+ G+ | - | - | 45 | 30 | mA |
| | | T2+ G- | - | - | 30 | 20 | mA |
| | | T2- G- | | | | | |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 30 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | TYP. | UNIT |
|---|---|---|---|---|---|---|
| | | BTA204- | ...B | ...C | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 6 | 3 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA204 series D, E and F

## GENERAL DESCRIPTION

Glass passivated guaranteed commutation triacs in a plastic envelope, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

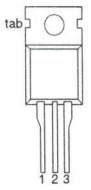
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | | BTA204- | 500D | 600D | - | |
| | | BTA204- | 500E | 600E | 800E | |
| | | BTA204- | 500F | 600F | 800F | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | | 25 | 25 | 25 | A |

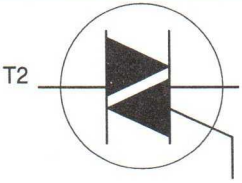
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 5 | 10 | 25 | mA |
| | | T2+ G- | - | - | 5 | 10 | 25 | mA |
| | | T2- G- | - | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 20 | 30 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 1.5 | 2.0 | 2.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA204S series B and C
BTA204M series B and C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.

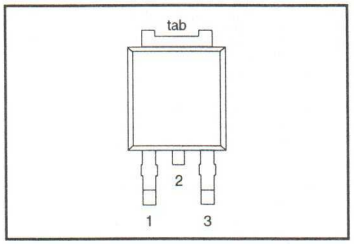
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA204S** (or BTA204M)- | **500B** | **600B** | **800B** | |
| | **BTA204S** (or BTA204M)- | **500C** | **600C** | **800C** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

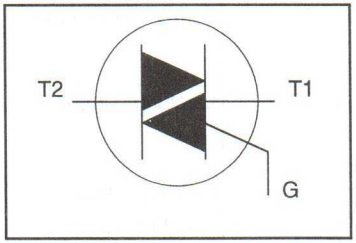
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Objective specification
See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.2 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | UNIT |
|---|---|---|---|---|---|---|---|
| | | BTA204- | | | ...B | ...C | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 50 | 35 | mA |
| | | T2+ G- | - | - | 50 | 35 | mA |
| | | T2- G- | - | - | 50 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 30 | 20 | mA |
| | | T2+ G- | - | - | 45 | 30 | mA |
| | | T2- G- | - | - | 30 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 30 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | TYP. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 6 | 3 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

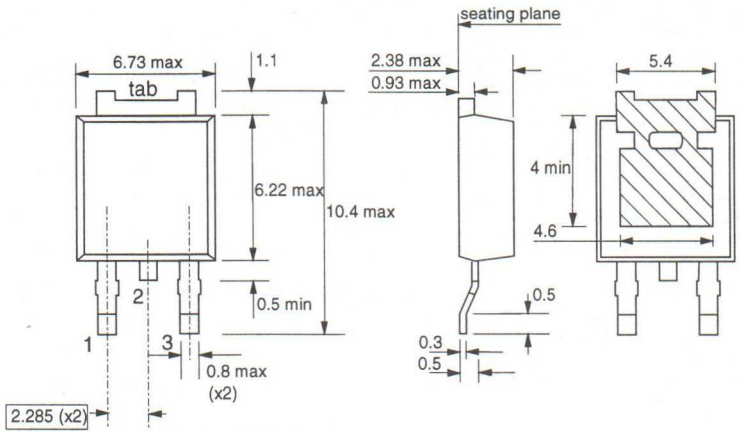



*Fig.1. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

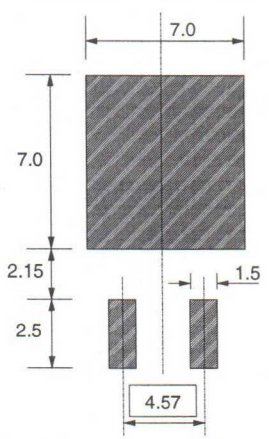



*Fig.2. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs guaranteed commutation

# BTA204S series D, E and F

BTA204M series D, E and F

## GENERAL DESCRIPTION

Glass passivated guaranteed commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

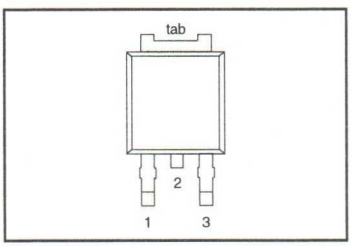
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA204S** (or BTA204M)- | **500D** | **600D** | - | |
| | **BTA204S** (or BTA204M)- | **500E** | **600E** | **800E** | |
| | **BTA204S** (or BTA204M)- | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

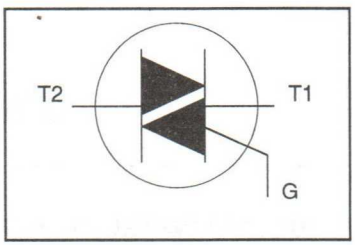
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 107$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Objective specification See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 3.0 | K/W |
| | | half cycle | - | - | 3.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BTA204S** (or BTA204M)- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 5 | 10 | 25 | mA |
| | | T2+ G- | - | - | 5 | 10 | 25 | mA |
| | | T2- G- | - | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BTA204S** (or BTA204M)- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 20 | 30 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 1.5 | 2.0 | 2.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

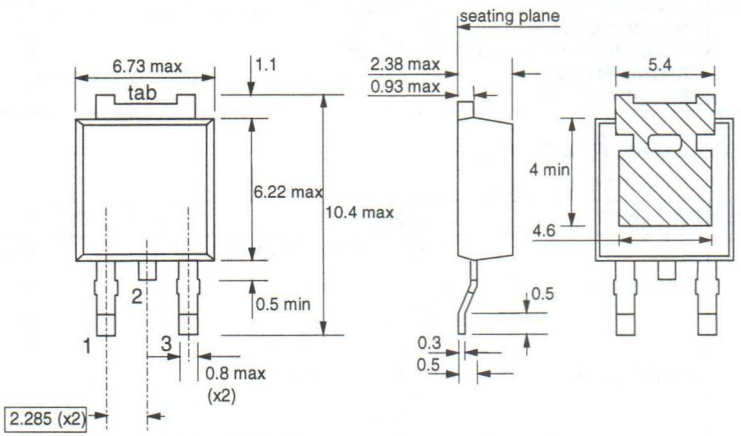



*Fig.1. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

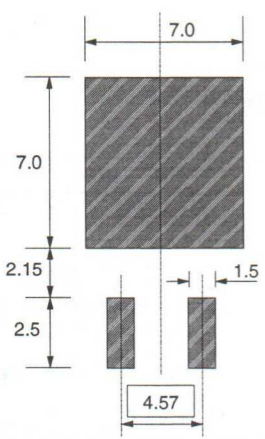



*Fig.2. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA204W series B and C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.

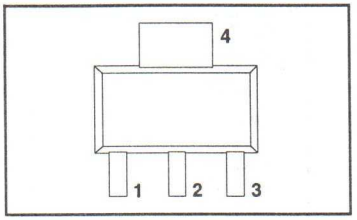
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA204W- | 500B | 600B | 800B | |
| | BTA204W- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | 10 | A |

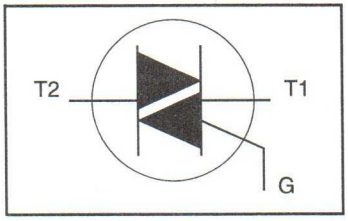
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108$ °C | - | | 1 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 10 | | A |
| | | t = 16.7 ms | - | | 11 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 0.5 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

# Objective specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | full or half cycle | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:2 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | UNIT |
|---|---|---|---|---|---|---|---|
| | | BTA204W- | | | ...B | ...C | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 50 | 35 | mA |
| | | T2+ G- | - | - | 50 | 35 | mA |
| | | T2- G- | - | - | 50 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 30 | 20 | mA |
| | | T2+ G- | - | - | 45 | 30 | mA |
| | | T2- G- | - | - | 30 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 30 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.2 | 1.5 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | TYP. | UNIT |
|---|---|---|---|---|---|---|
| | | BTA204W- | ...B | ...C | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 6 | 3 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

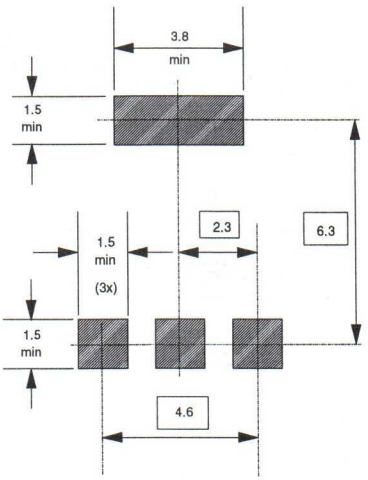



*Fig.1. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

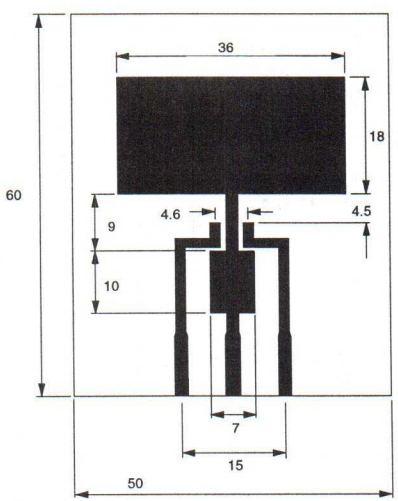



*Fig.2. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

# Three quadrant triacs guaranteed commutation

# BTA204W series D, E and F

## GENERAL DESCRIPTION

Glass passivated guaranteed commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

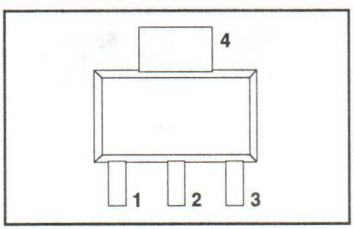
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA204W- | 500D | 600D | - | |
| | BTA204W- | 500E | 600E | 800E | |
| | BTA204W- | 500F | 600F | 800F | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 1 | 1 | 1 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | 10 | 10 | A |

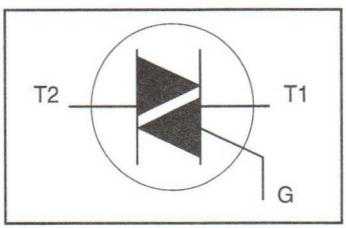
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 1 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 20 ms | - | 10 | | | A |
| | | t = 16.7 ms | - | 11 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 0.5 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | full or half cycle | - | - | 15 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb mounted; minimum footprint | - | 156 | - | K/W |
| | | pcb mounted; pad area as in fig:2 | - | 70 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204W- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 5 | 10 | 25 | mA |
| | | T2+ G- | - | - | 5 | 10 | 25 | mA |
| | | T2- G- | - | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 2 A | - | 1.2 | | 1.5 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204W- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 20 | 30 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 1.5 | 2.0 | 2.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

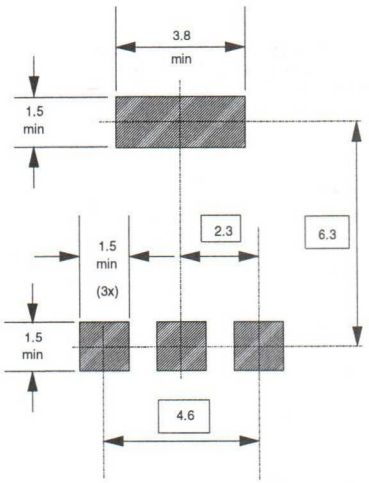



*Fig.1. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

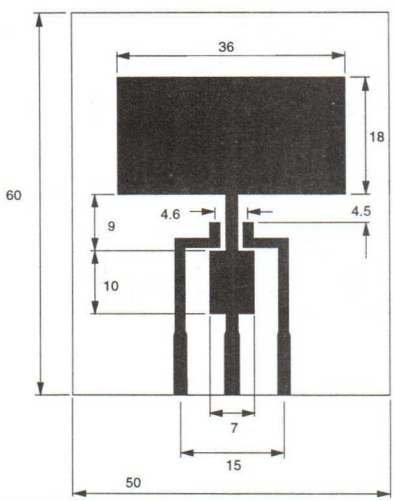



*Fig.2. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

# Three quadrant triacs high commutation

# BTA204X series B and C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic full pack envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.

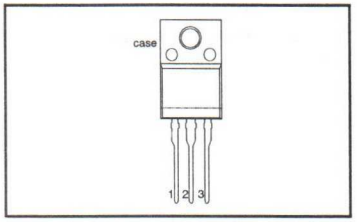
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA204X- | 500B | 600B | 800B | |
| | BTA204X- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

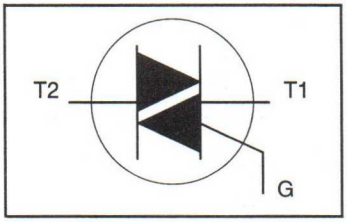
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 92$ °C | - | 4 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 20 ms | - | 25 | | | A |
| | | t = 16.7 ms | - | 27 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 3.1 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle<br>with heatsink compound<br>without heatsink compound | -<br>- | -<br>- | 5.5<br>7.2 | K/W<br>K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | UNIT |
|---|---|---|---|---|---|---|---|
| | | BTA204X- | | | ...B | ...C | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 50 | 35 | mA |
| | | T2+ G- | - | - | 50 | 35 | mA |
| | | T2- G- | - | - | 50 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | T2+ G+ | - | - | 30 | 20 | mA |
| | | T2+ G- | - | - | 45 | 30 | mA |
| | | T2- G- | - | - | 30 | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 30 | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | TYP. | UNIT |
|---|---|---|---|---|---|---|
| | | BTA204X- | ...B | ...C | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 6 | 3 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA204X series D, E and F

## GENERAL DESCRIPTION

Glass passivated guaranteed commutation triacs in a plastic full pack envelope, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

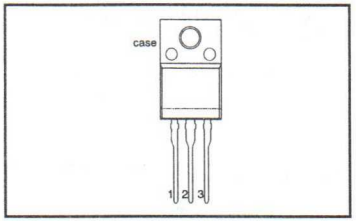
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA204X-** | **500D** | **600D** | **-** | |
| | **BTA204X-** | **500E** | **600E** | **800E** | |
| | **BTA204X-** | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 4 | 4 | 4 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 25 | 25 | 25 | A |

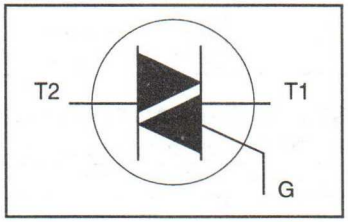
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 92$ °C | - | | 4 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 25 | | A |
| | | t = 16.7 ms | - | | 27 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 3.1 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 5.5 | K/W |
| | | without heatsink compound | - | - | 7.2 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204X- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 5 | 10 | 25 | mA |
| | | T2+ G- | - | - | 5 | 10 | 25 | mA |
| | | T2- G- | - | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 5 A | - | 1.4 | | 1.7 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

2 Device does not trigger in the T2-, G+ quadrant.

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA204X- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 20 | 30 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 4 A; $dV_{com}/dt$ = 20V/µs; gate open circuit | 1.5 | 2.0 | 2.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

# Three quadrant triacs high commutation

# BTA208 series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

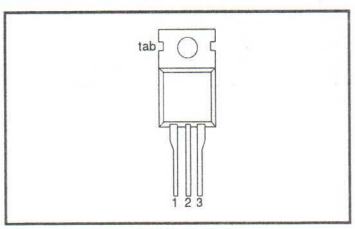
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

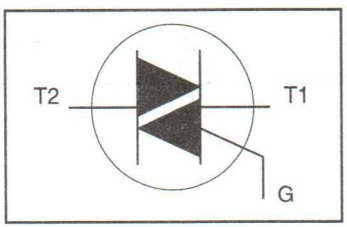
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | - | 14 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

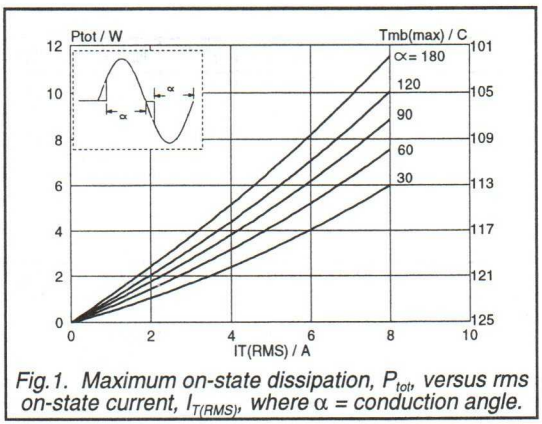



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

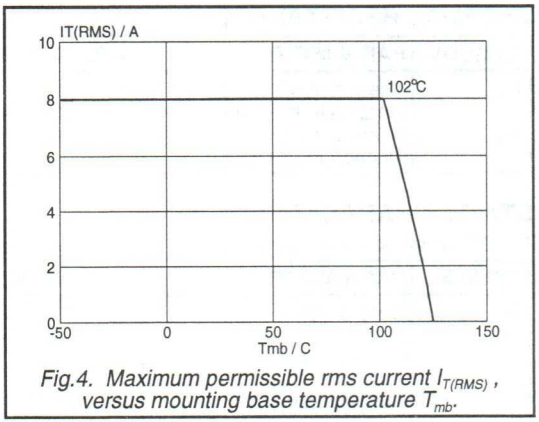



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

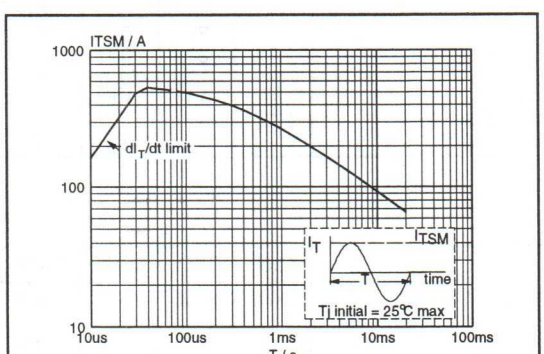



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

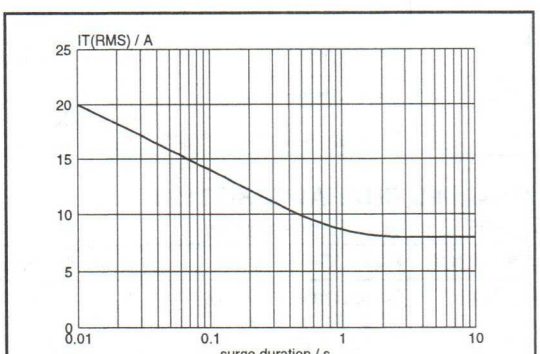



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

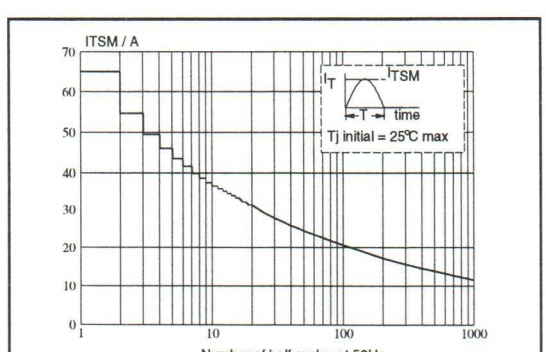



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

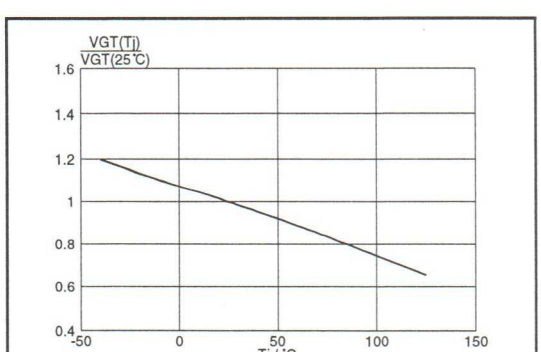



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

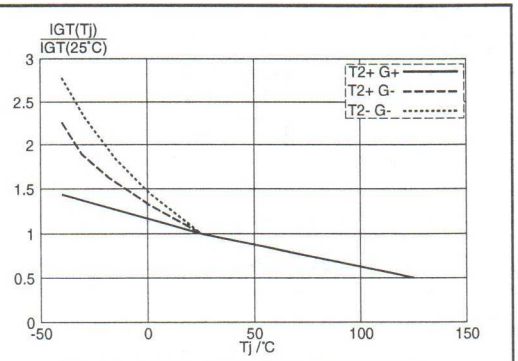



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

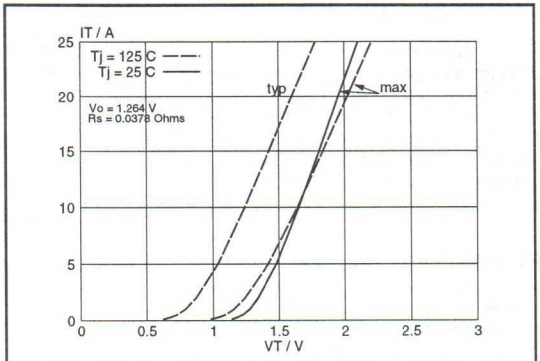



*Fig.10. Typical and maximum on-state characteristic.*

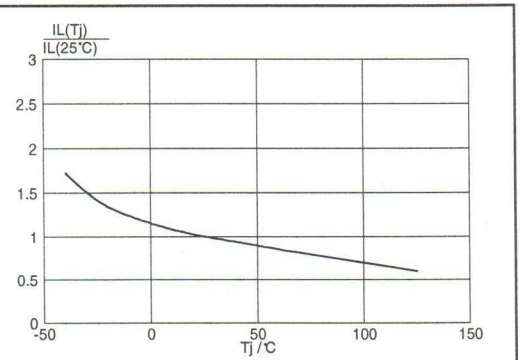



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

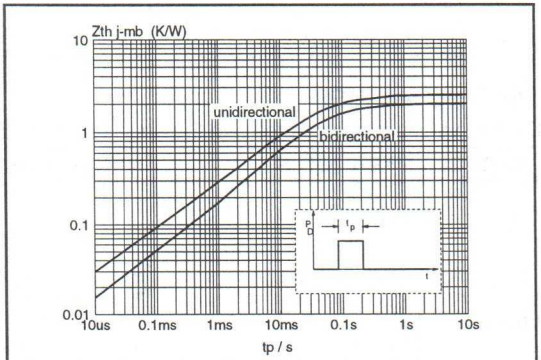



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

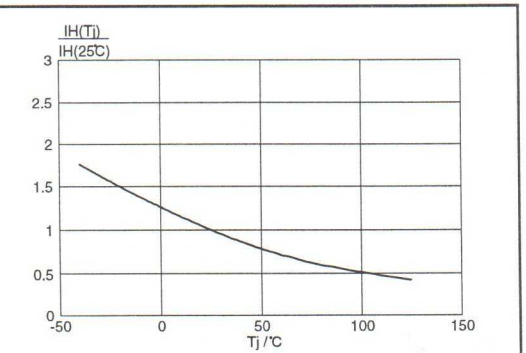



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

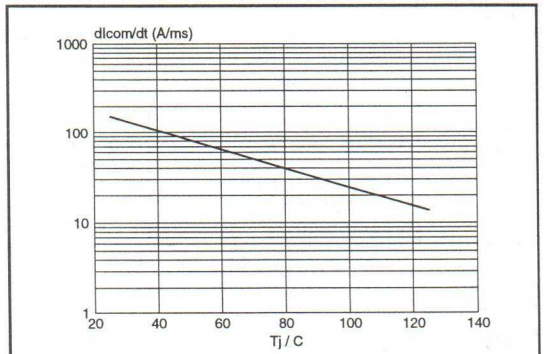



*Fig.12. Typical, critical rate of change of commutating current, $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA208 series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

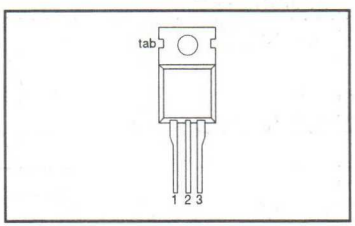
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

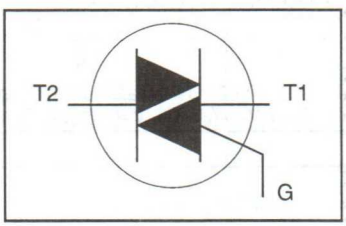
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | - | 35 | mA |
| | | | T2+ G- | 2 | - | 35 | mA |
| | | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA208 series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

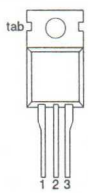
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208- | 500D | 600D | - | |
| | BTA208- | 500E | 600E | 800E | |
| | BTA208- | 500F | 600F | 800F | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

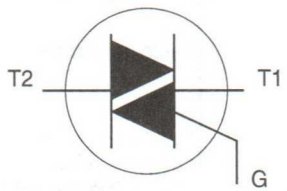
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Objective specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | | | 5 | 10 | 25 | mA |
| | | T2+ G- | | | 5 | 10 | 25 | mA |
| | | T2- G- | | | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | | | 6 | 12 | 30 | mA |
| | | T2+ G- | - | | 9 | 18 | 45 | mA |
| | | T2- G- | - | | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 1.8 | 2.5 | 3.5 | | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA208B series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

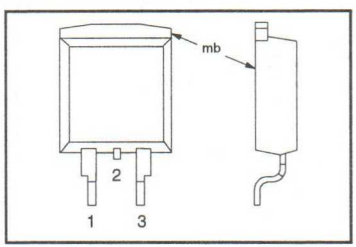
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208B-** | **500B** | **600B** | **800B** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

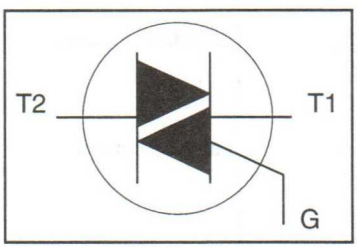
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | - | 14 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

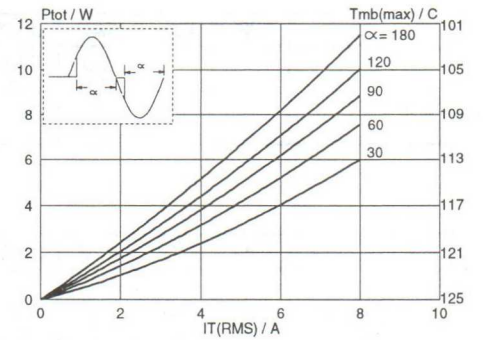



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

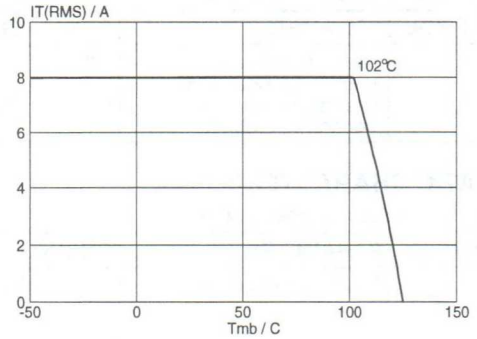



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

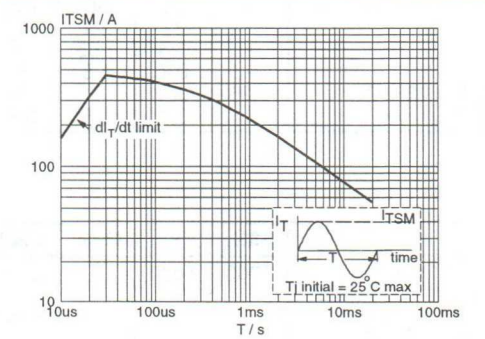



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

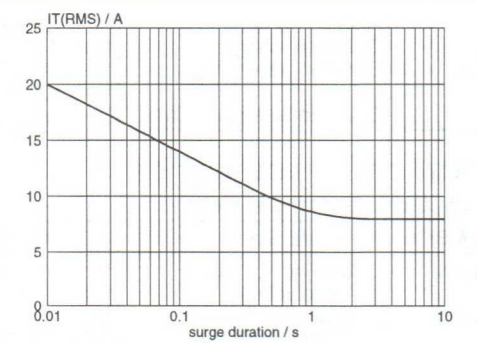



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

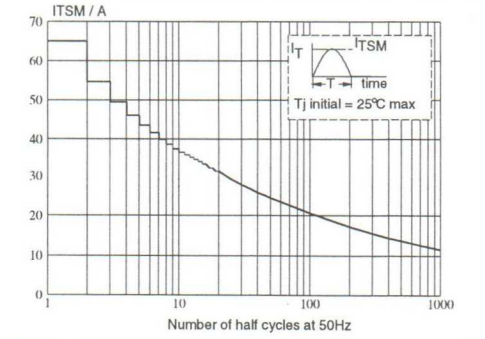



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*




*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

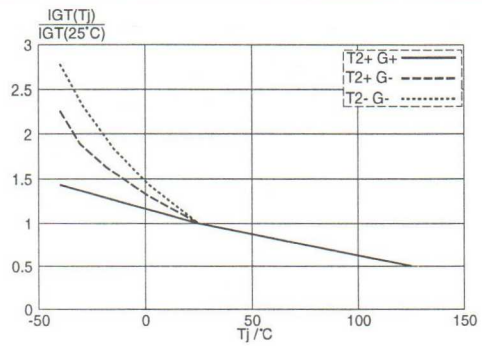



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

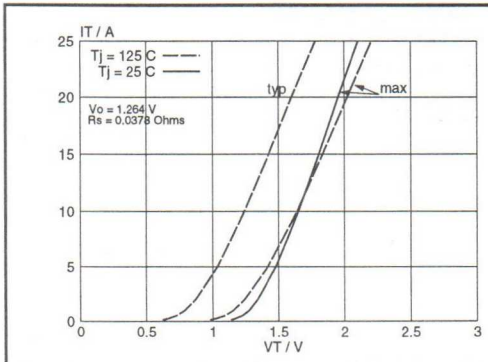



*Fig.10. Typical and maximum on-state characteristic.*

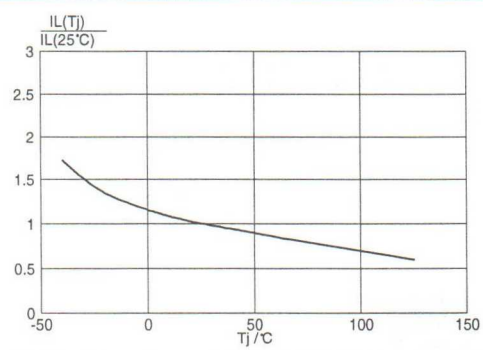



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

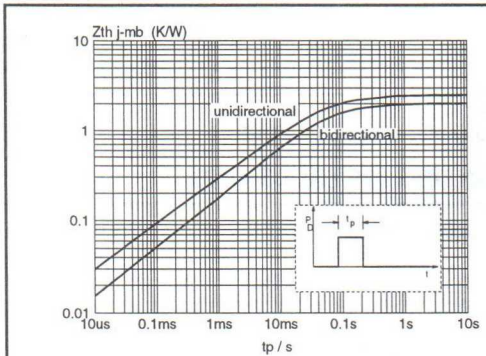



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

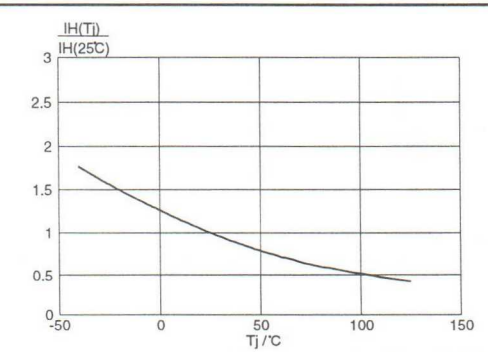



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

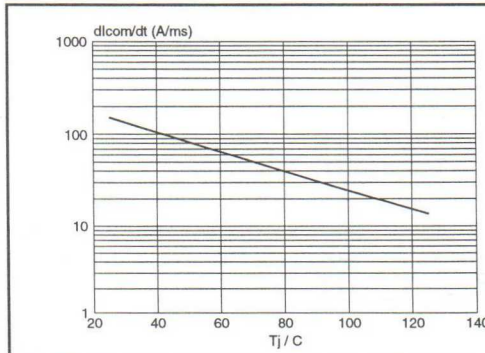



*Fig.12. Typical, critical rate of change of commutating current, $dI_{com}/dt$ versus junction temperature.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

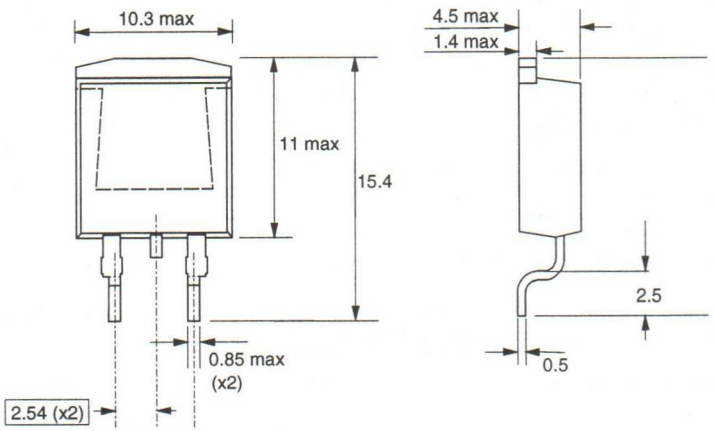



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

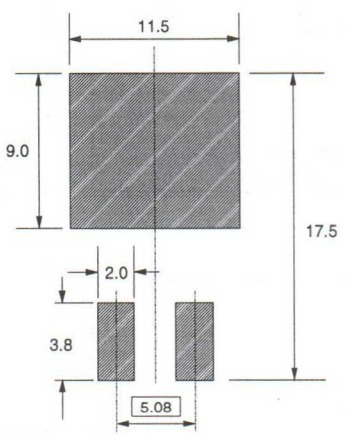



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA208B series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.

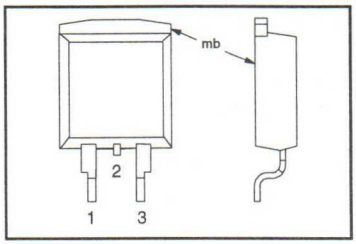
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

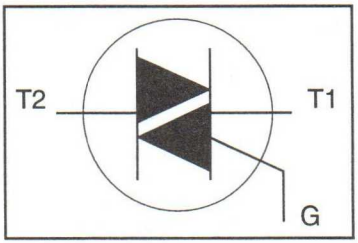
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | - | 35 | mA |
| | | | T2+ G- | 2 | - | 35 | mA |
| | | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

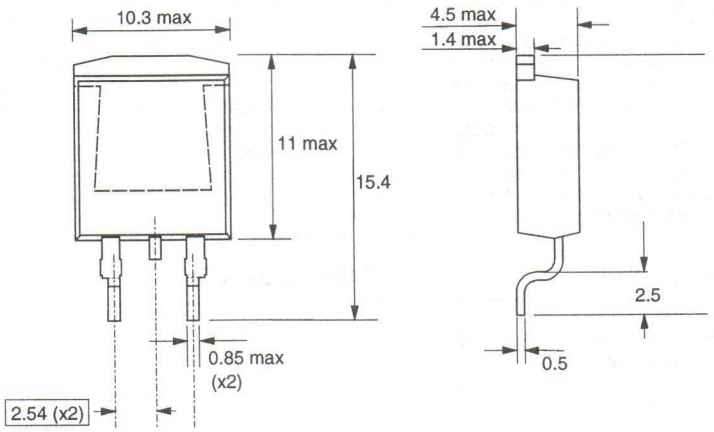



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

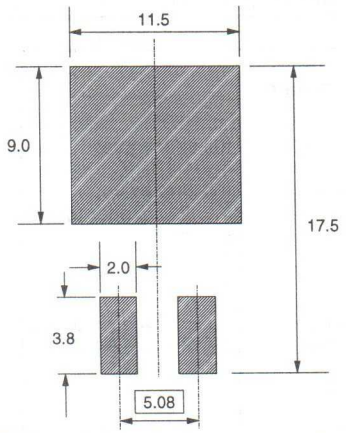



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs guaranteed commutation

# BTA208B series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

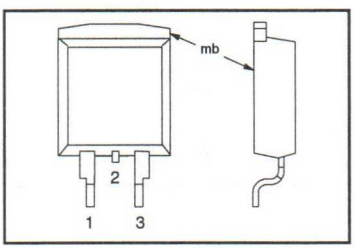
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208B-** | **500D** | **600D** | **-** | |
| | **BTA208B-** | **500E** | **600E** | **800E** | |
| | **BTA208B-** | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

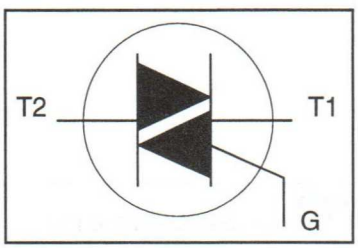
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208B- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | 2 | - | 5 | 10 | 25 | mA |
| | | T2+ G- | 2 | - | 5 | 10 | 25 | mA |
| | | T2- G- | 2 | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | 1.65 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208B- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 1.8 | 2.5 | 3.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

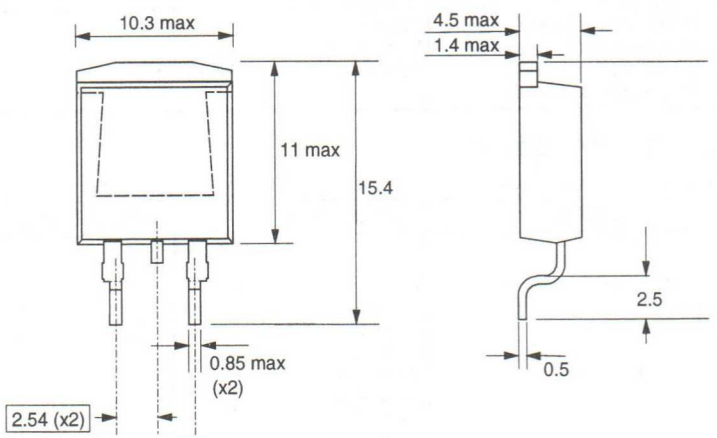



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

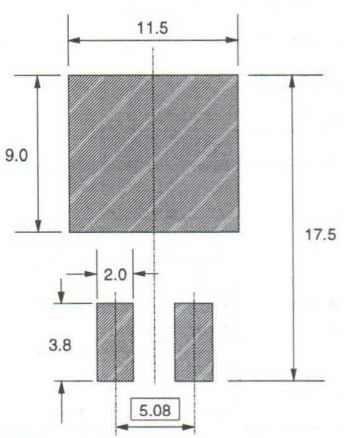



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA208S series B
BTA208M series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope, suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

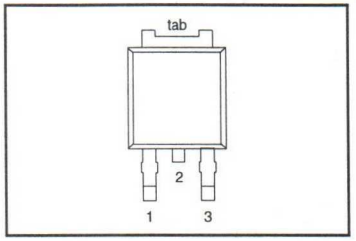
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208S** (or BTA208M)- | **500B** | **600B** | **800B** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

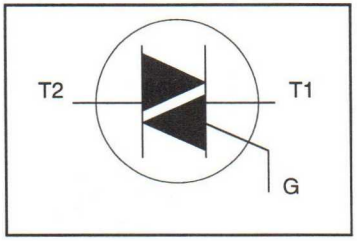
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | - | 14 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

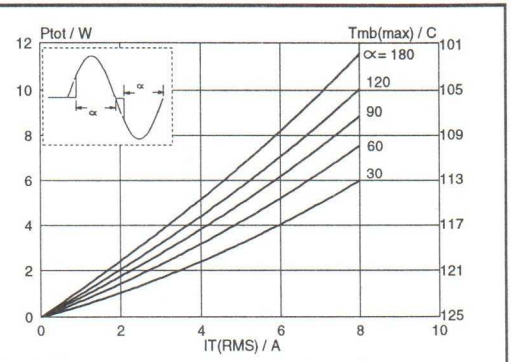



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

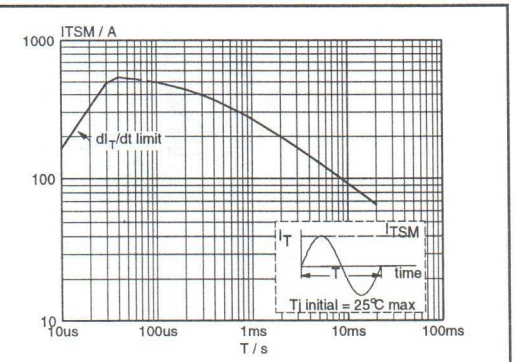



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

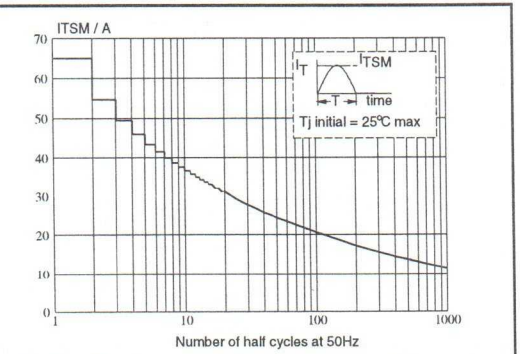



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

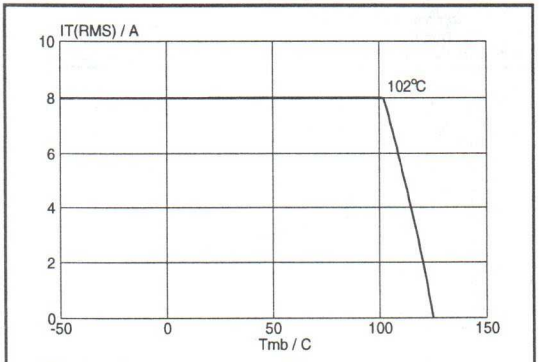



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

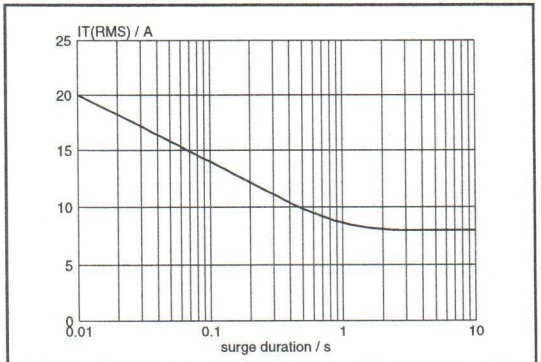



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.*

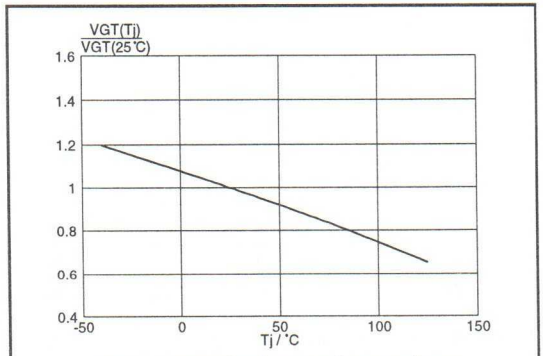



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

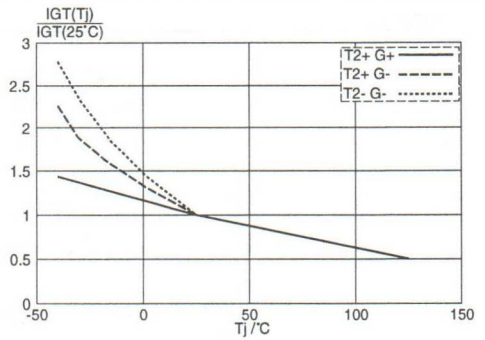



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

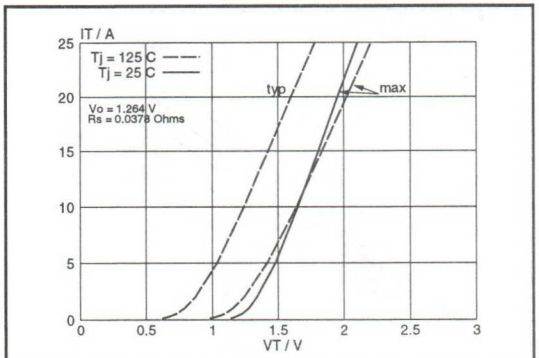



*Fig.10. Typical and maximum on-state characteristic.*

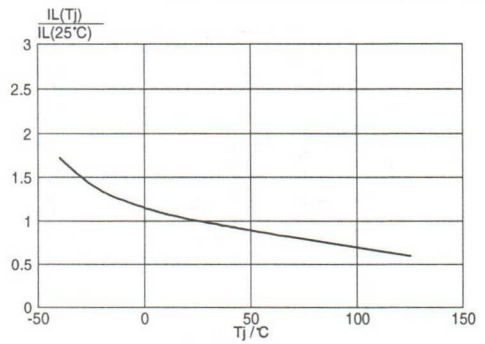



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

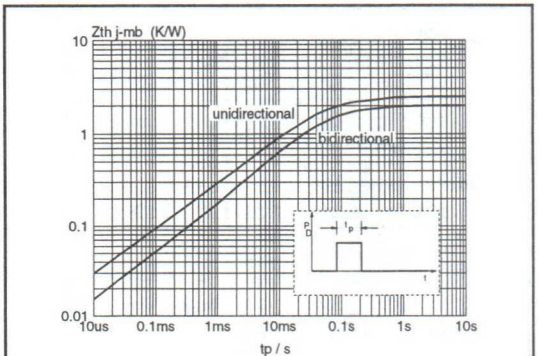



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

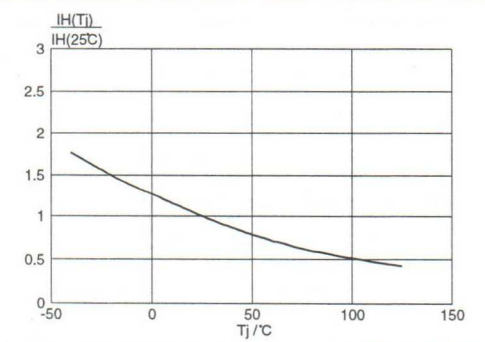



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

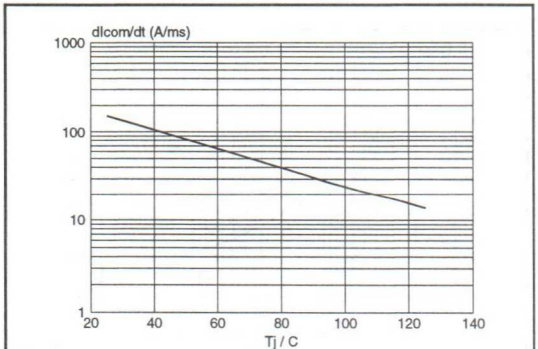



*Fig.12. Typical, critical rate of change of commutating current, $dI_{com}/dt$ versus junction temperature.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

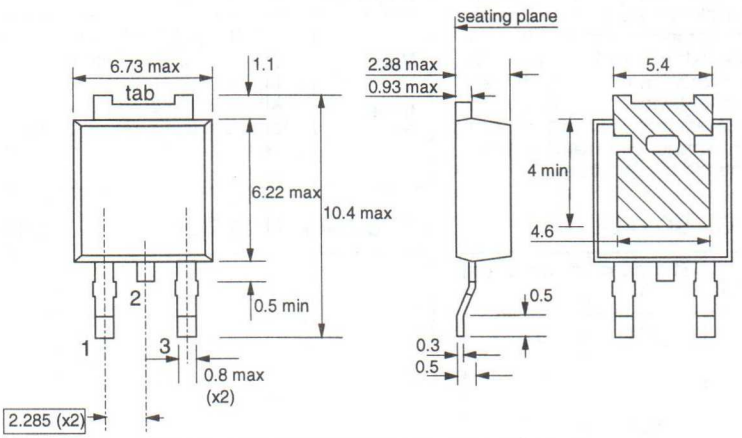



*Fig.13. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

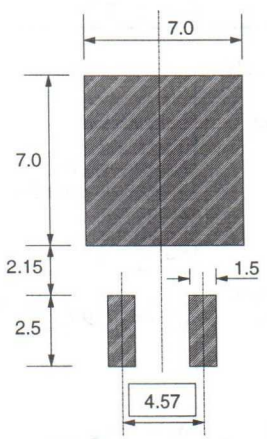



*Fig.14. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA208S series C
BTA208M series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope, suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

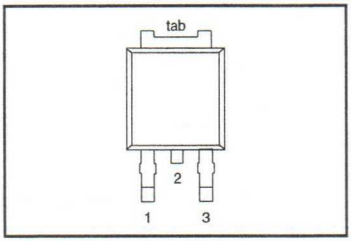
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208S** (or BTA208M)- | **500C** | **600C** | **800C** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

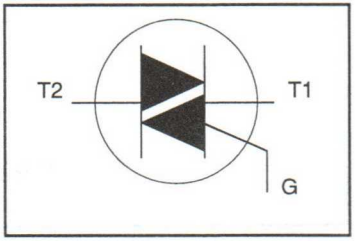
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | **-500** 500[1] | **-600** 600[1] | **-800** 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

**1** Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | pcb (FR4) mounted; footprint as in Fig.14 | - | 75 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | 2 | - | 35 | mA |
| | | T2+ G- | 2 | - | 35 | mA |
| | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | - | 20 | mA |
| | | T2+ G- | - | - | 30 | mA |
| | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

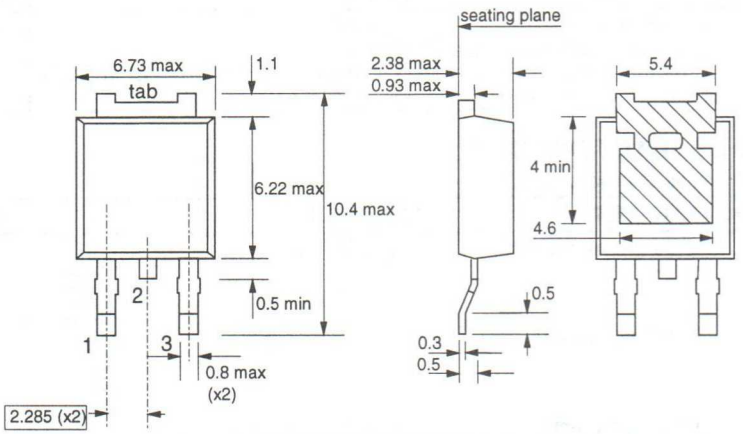



*Fig.1. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

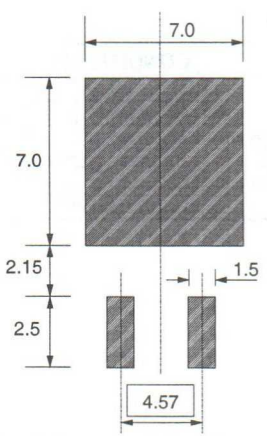



*Fig.2. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs guaranteed commutation

# BTA208S series D, E and F

BTA208M series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

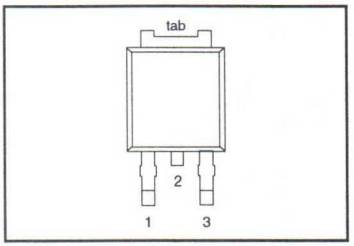
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208S** (or BTA208M)- | **500D** | **600D** | - | |
| | **BTA208S** (or BTA208M)- | **500E** | **600E** | **800E** | |
| | **BTA208S** (or BTA208M)- | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

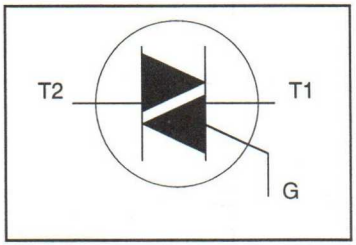
## PINNING - SOT428

| PIN NUMBER | Standard S | Alternative M |
|---|---|---|
| 1 | MT1 | gate |
| 2 | MT2 | MT2 |
| 3 | gate | MT1 |
| tab | MT2 | MT2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 102$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification

See Philips Semiconductors for Design-in information

**1** Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 2.0 | K/W |
| | | half cycle | - | - | 2.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BTA208S** (or BTA208M)- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | 2 | - | 5 | 10 | 25 | mA |
| | | T2+ G- | 2 | - | 5 | 10 | 25 | mA |
| | | T2- G- | 2 | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | mA |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | 1.65 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | **BTA208B-** | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 1.8 | 2.5 | 3.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.1 g*

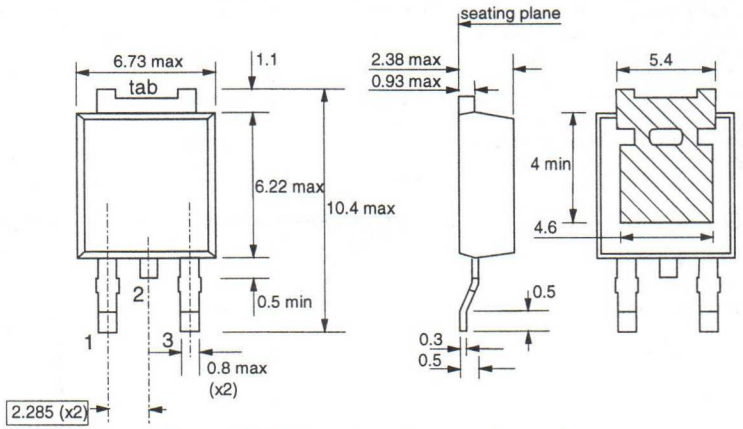



*Fig.1. SOT428 : centre pin connected to tab.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

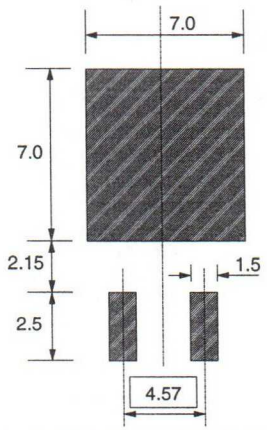



*Fig.2. SOT428 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA208X series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in motor control circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

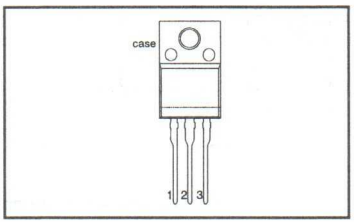
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208X- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

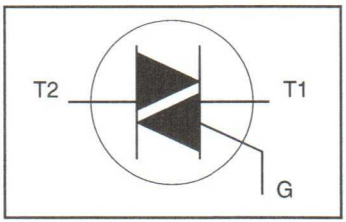
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -600 | -600 | -800 | |
| | | | | 600[1] | 600[1] | 800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | | | | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | - | 14 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

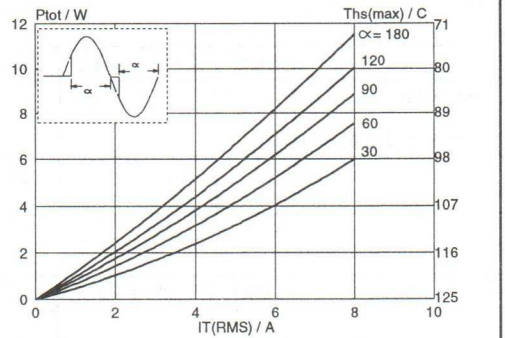



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

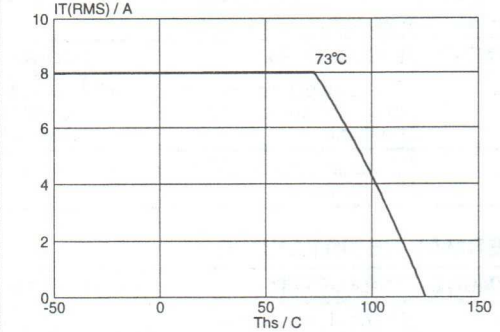



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

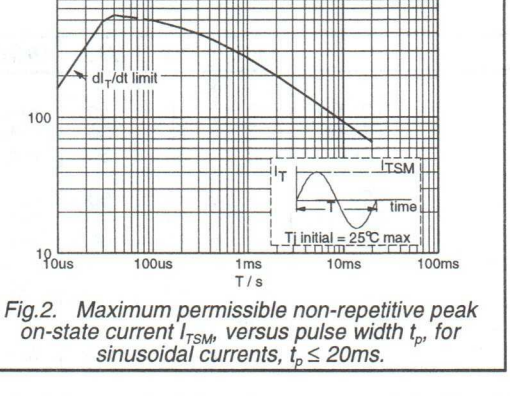



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

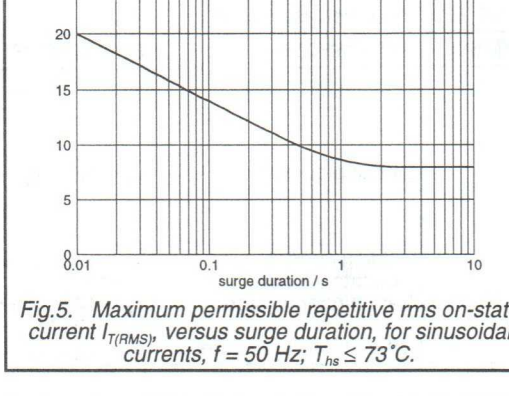



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73°C$.*

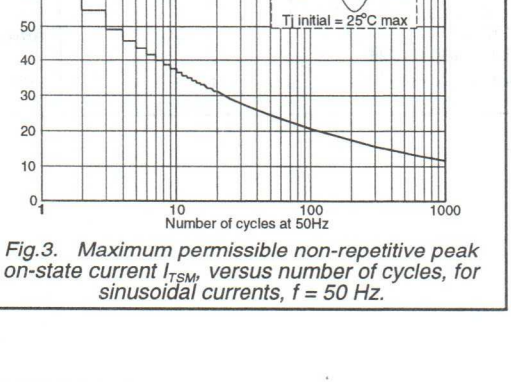



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

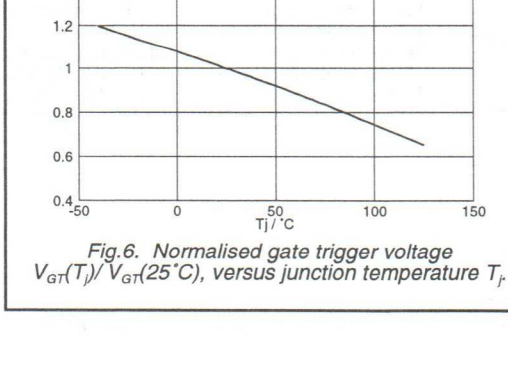



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

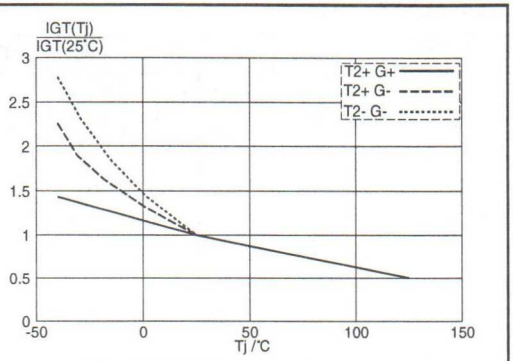



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

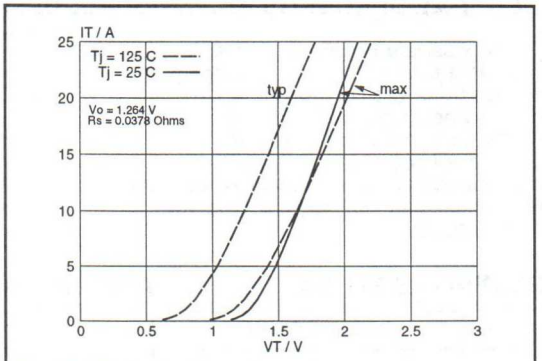



*Fig.10. Typical and maximum on-state characteristic.*

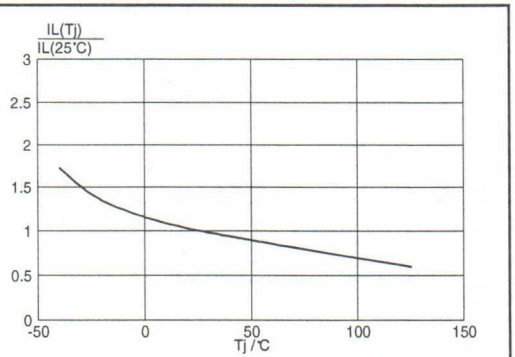



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

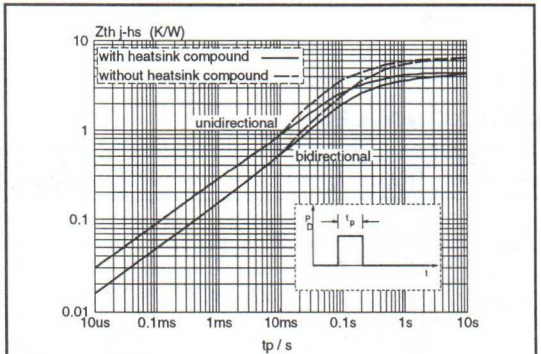



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

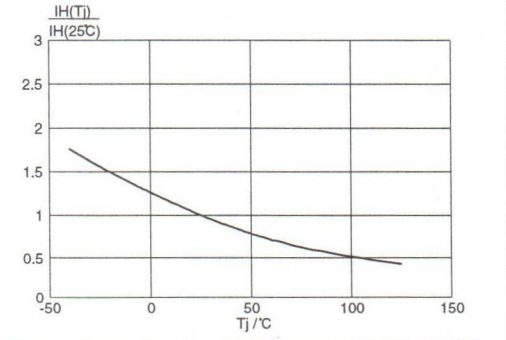



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

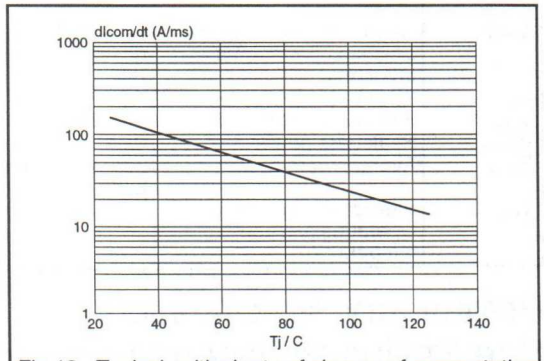



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA208X series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in motor control circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

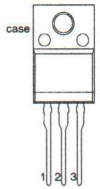
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA208X- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

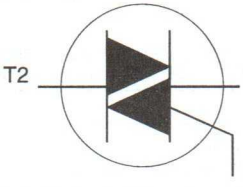
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | -600<br>600[1] | -600<br>600[1] | -800<br>800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | 8 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 65 | | | A |
| | | t = 16.7 ms | - | 71 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 21 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.5 | K/W |
| | | without heatsink compound | - | - | 6.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | - | 35 | mA |
| | | | T2+ G- | 2 | - | 35 | mA |
| | | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | | - | 1.3 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA208X series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

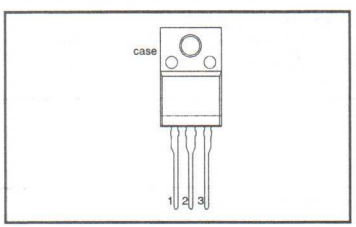
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA208X-** | **500D** | **600D** | **-** | |
| | **BTA208X-** | **500E** | **600E** | **800E** | |
| | **BTA208X-** | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 8 | 8 | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 65 | 65 | 65 | A |

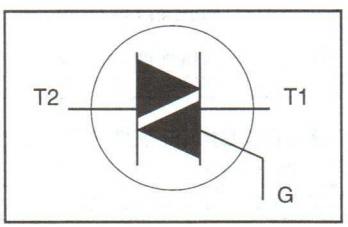
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 73$ °C | - | | 8 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 65 | | A |
| | | t = 16.7 ms | - | | 71 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 21 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 12 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle<br>with heatsink compound<br>without heatsink compound | -<br>- | -<br>- | 4.5<br>6.5 | K/W<br>K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208X- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | 2 | - | 5 | 10 | 25 | mA |
| | | T2+ G- | 2 | - | 5 | 10 | 25 | mA |
| | | T2- G- | 2 | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 10 A | - | 1.3 | 1.65 | 1.65 | 1.65 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA208X- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 8 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 1.8 | 2.5 | 3.5 | - | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA212 series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

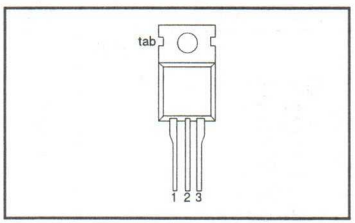
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

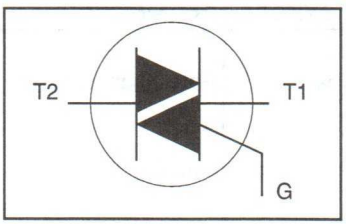
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 95 | | | A |
| | | t = 16.7 ms | - | 105 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 45 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | - | 24 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

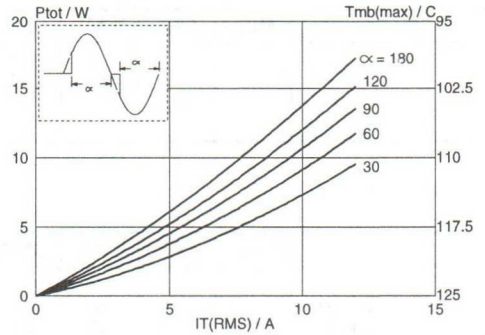



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

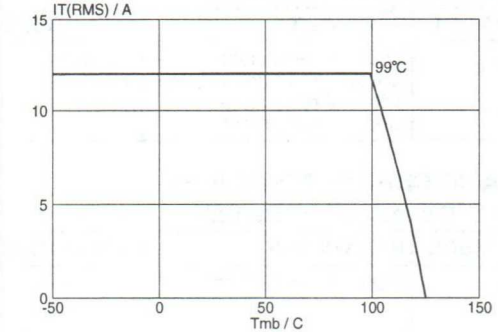



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

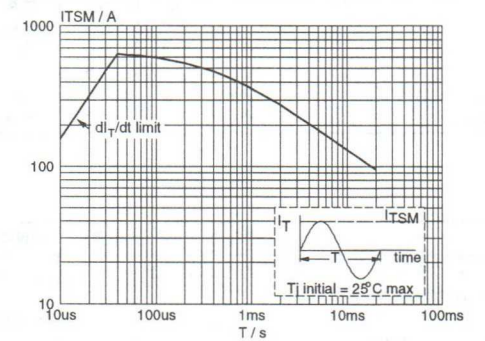



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

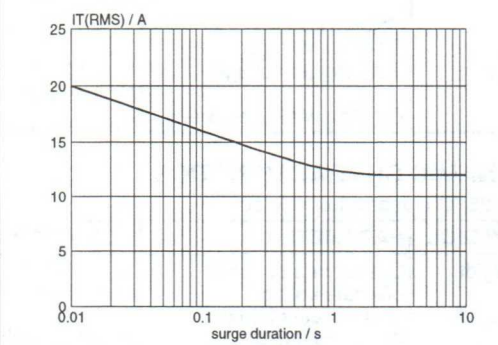



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

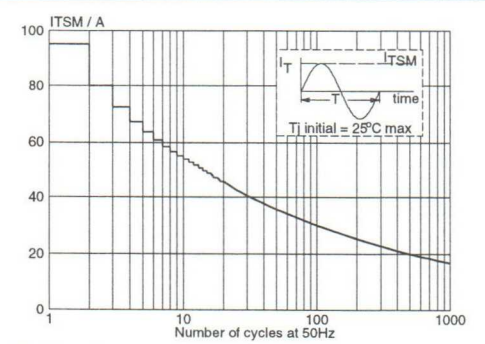



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

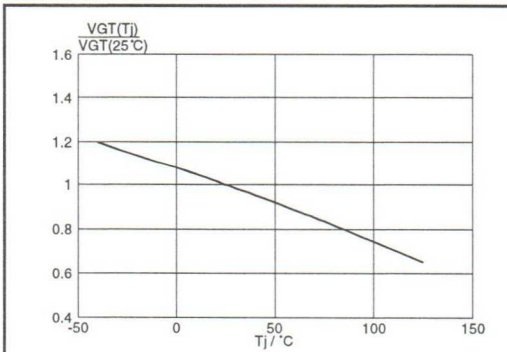



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

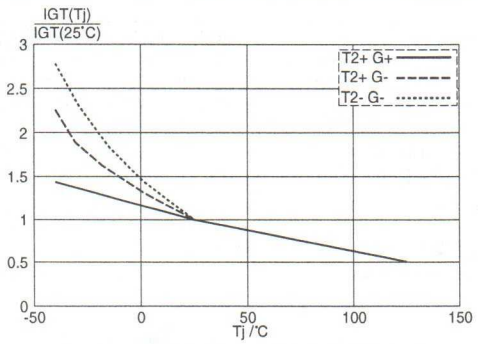



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

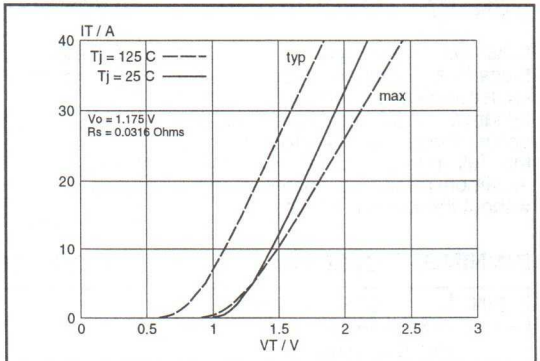



*Fig.10. Typical and maximum on-state characteristic.*

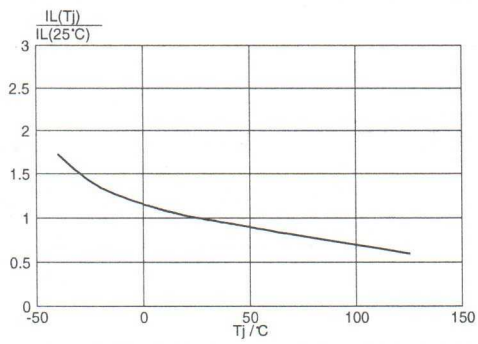



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

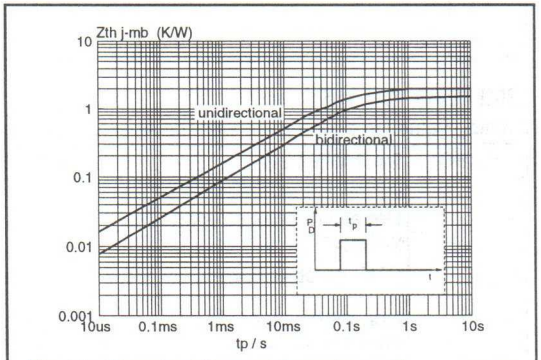



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

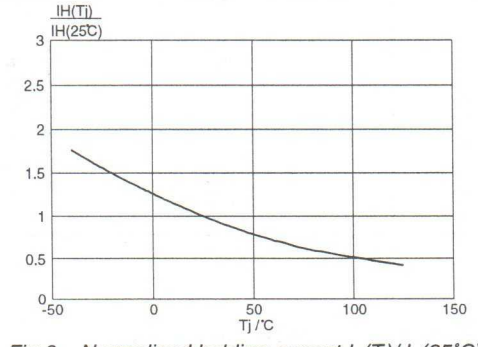



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

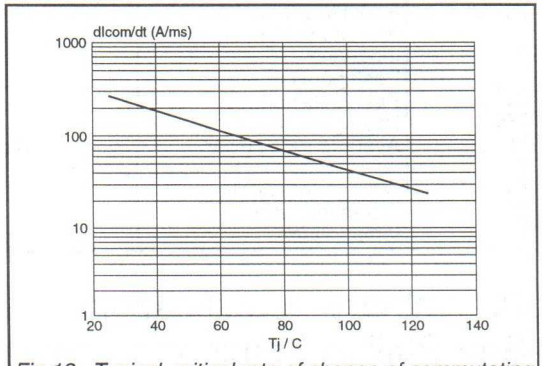



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA212 series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

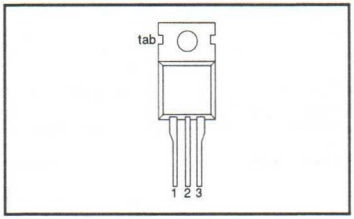
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

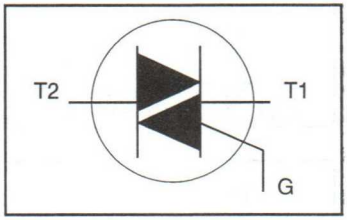
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j$ = 25 °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | - | 35 | mA |
| | | | T2+ G- | 2 | - | 35 | mA |
| | | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA212 series D, E and F

## GENERAL DESCRIPTION

Glass passivated guaranteed commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

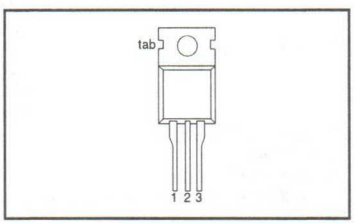
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212- | 500D | 600D | - | |
| | BTA212- | 500E | 600E | 800E | |
| | BTA212- | 500F | 600F | 800F | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 90 | 90 | 90 | A |

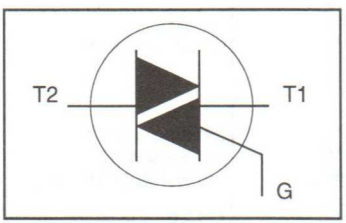
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800[1] | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | - | | | | |
| | | t = 20 ms | - | | 90 | | A |
| | | t = 16.7 ms | | | 100 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 40 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

# Objective specification

# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA212- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 5 | 10 | 25 | mA |
| | | T2+ G- | - | - | 5 | 10 | 25 | mA |
| | | T2- G- | - | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | - | 1.3 | | 1.6 | | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | 1.5 | | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | - | | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | 0.5 | | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA212- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | TBF | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 2 | 3.5 | 4.5 | TBF | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | - | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA212B series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

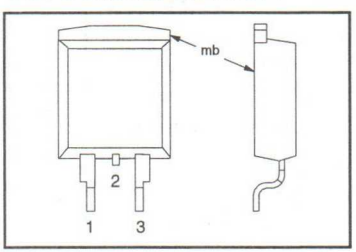
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212B- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

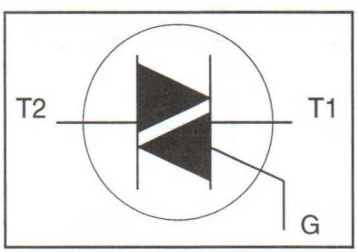
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | - | 24 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

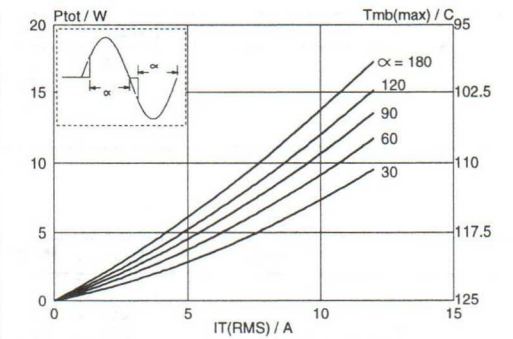



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

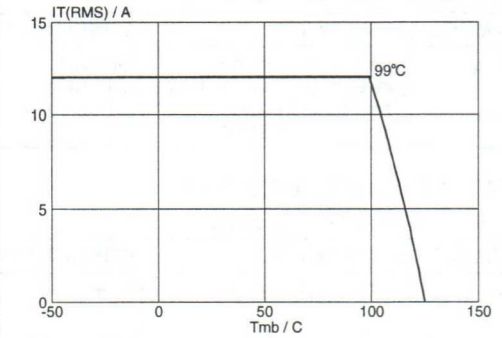



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

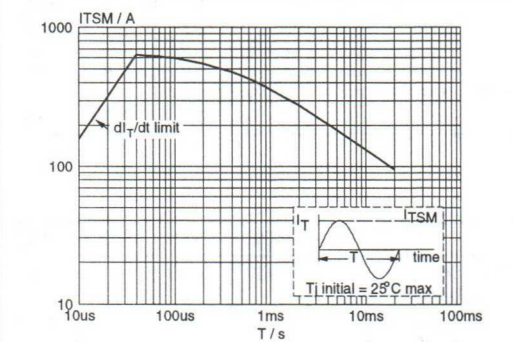



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

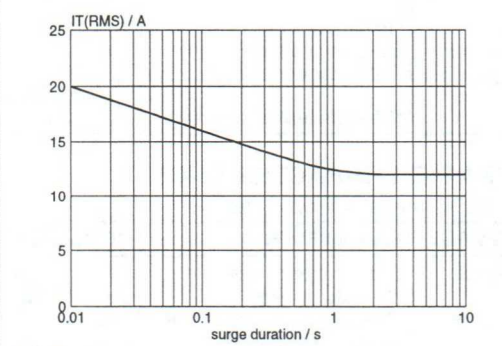



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

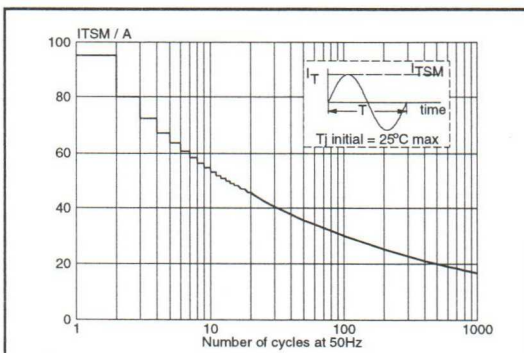



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

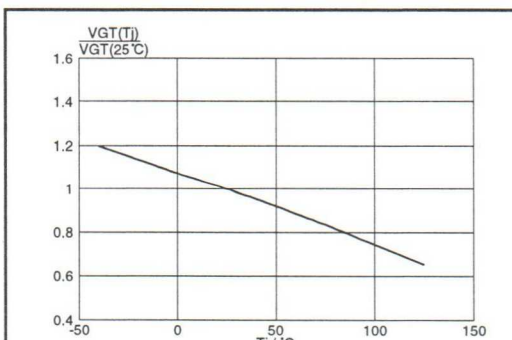



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

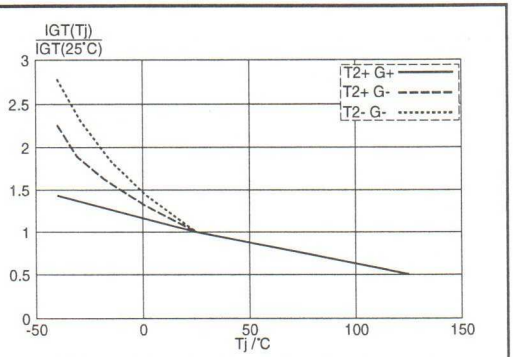



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

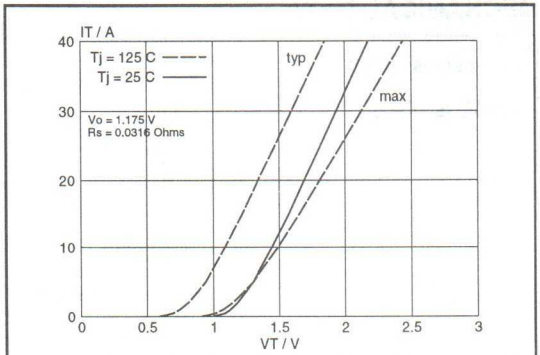



*Fig.10. Typical and maximum on-state characteristic.*

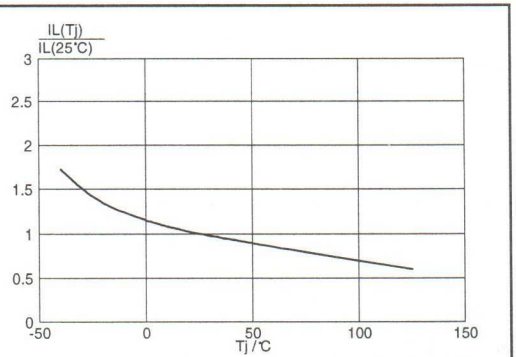



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

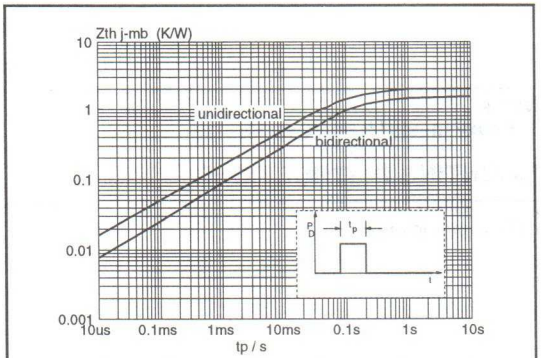



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

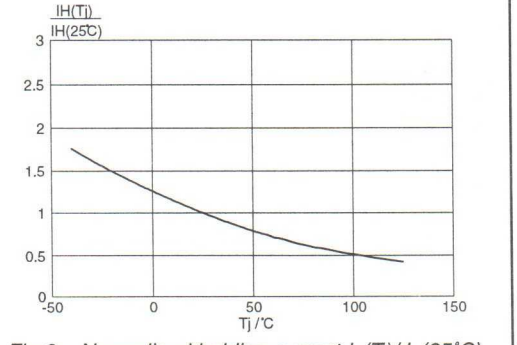



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

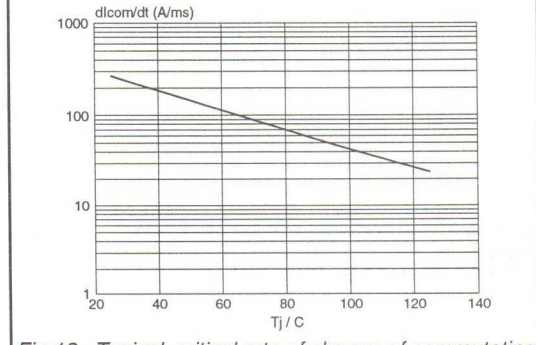



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

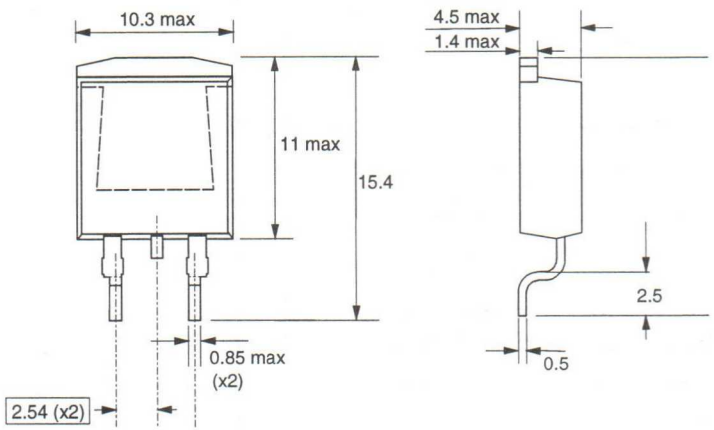



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**

1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

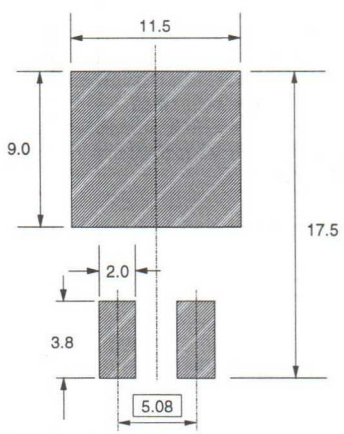



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**

1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA212B series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

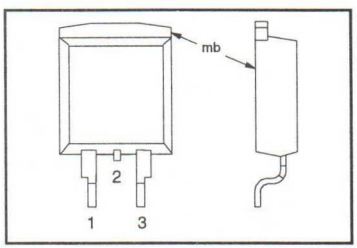
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212B- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

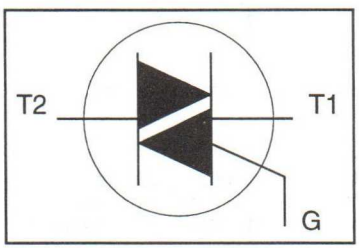
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 12 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 95 | | | A |
| | | t = 16.7 ms | - | 105 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 45 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

Preliminary specification
See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | 2 | - | 35 | mA |
| | | T2+ G- | 2 | - | 35 | mA |
| | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | - | 20 | mA |
| | | T2+ G- | - | - | 30 | mA |
| | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

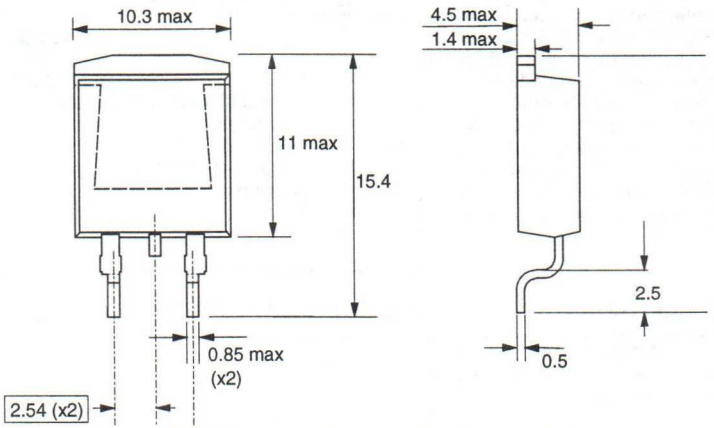



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

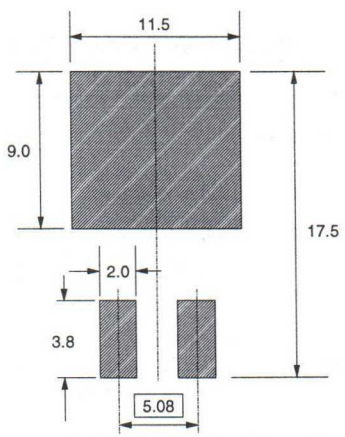



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs guaranteed commutation

# BTA212B series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

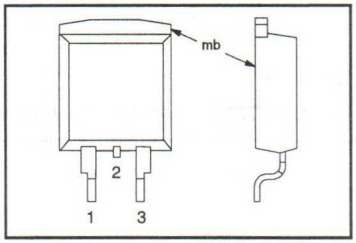
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | **BTA212B-** | **500D** | **600D** | **-** | |
| | | **BTA212B-** | **500E** | **600E** | **800E** | |
| | | **BTA212B-** | **500F** | **600F** | **800F** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | | 95 | 95 | 95 | A |

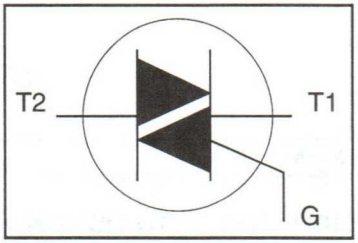
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.5 | K/W |
| | | half cycle | - | - | 2.0 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA212B- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | 2 | - | 5 | 10 | 25 | mA |
| | | T2+ G- | 2 | - | 5 | 10 | 25 | mA |
| | | T2- G- | 2 | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | - | 1.3 | | | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | - | 24 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

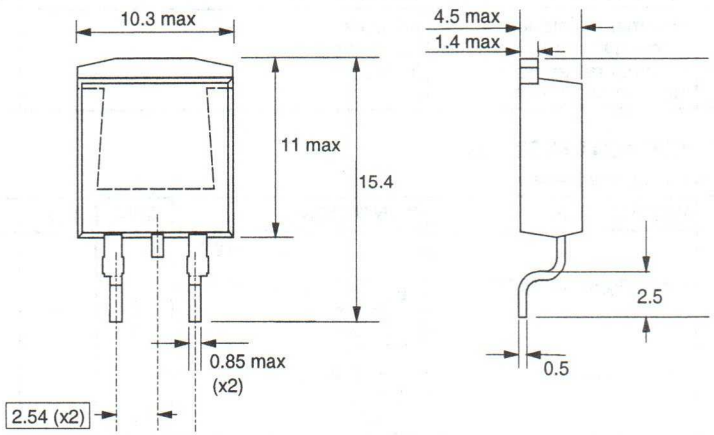



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

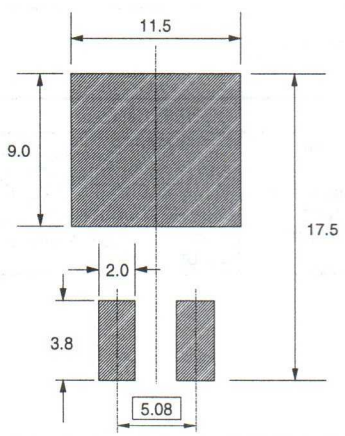



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA212X series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

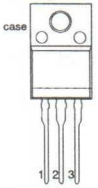
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212X- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

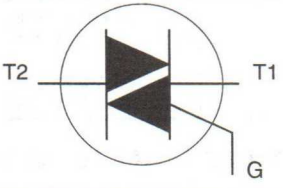
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 56$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | - | 24 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

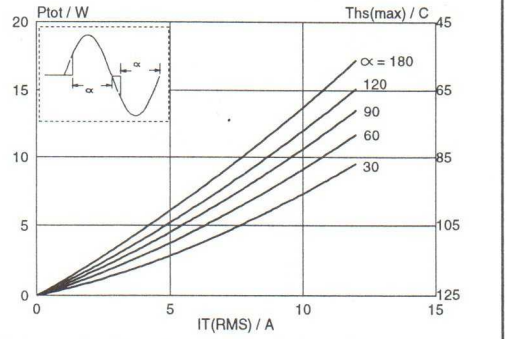



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

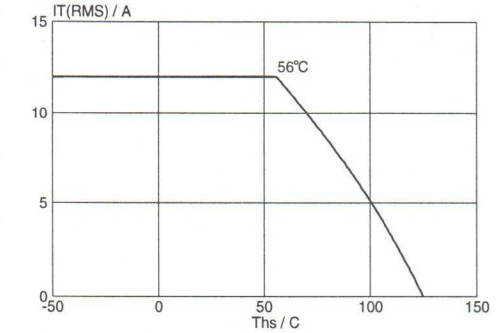



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

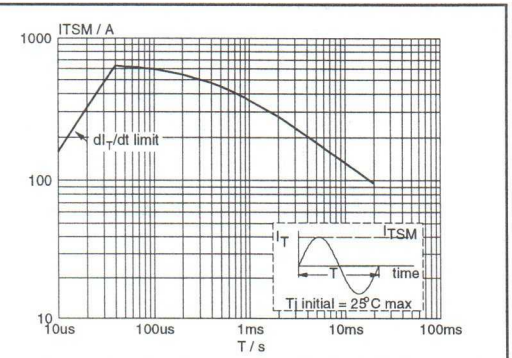



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

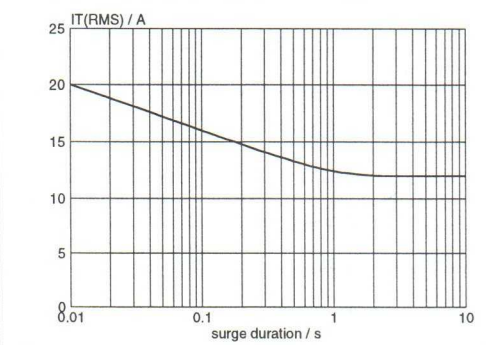



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56°C$.*

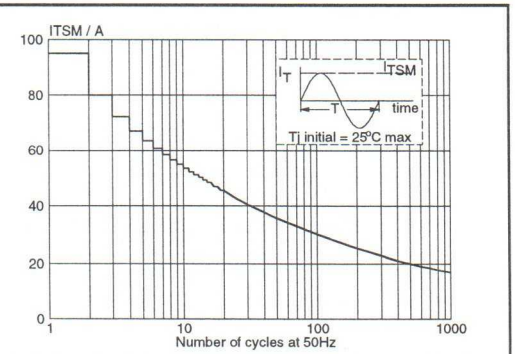



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

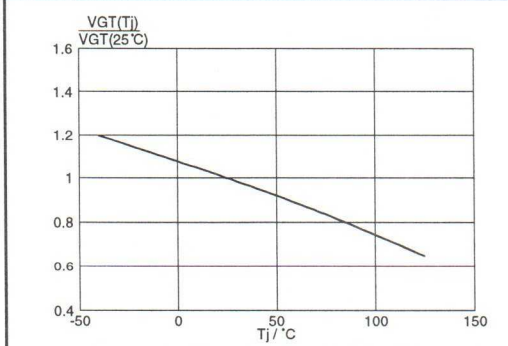



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

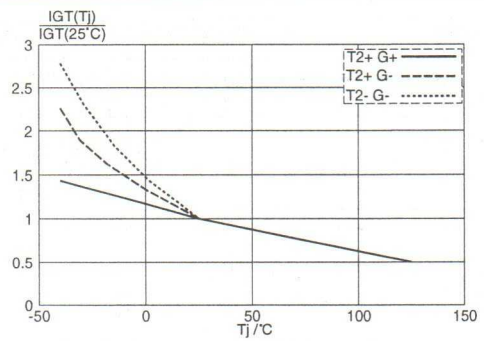



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

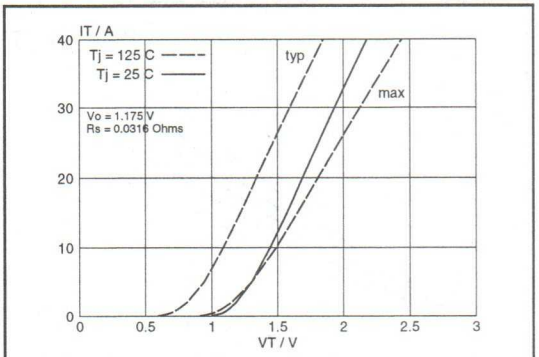



*Fig.10. Typical and maximum on-state characteristic.*

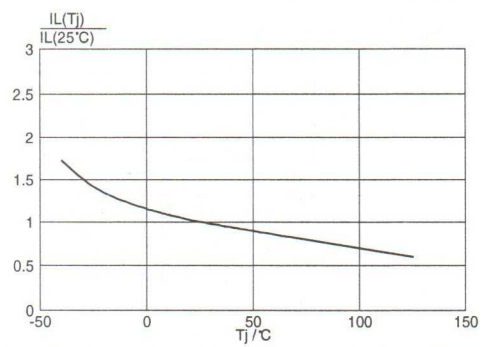



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

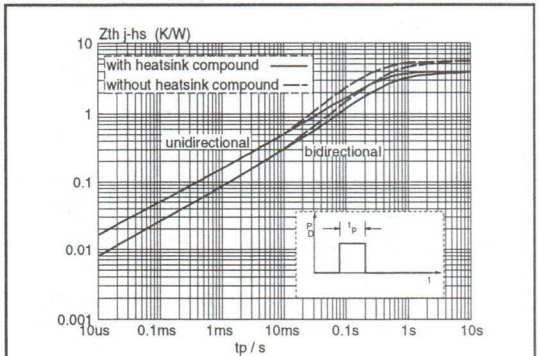



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width $t_p$.*

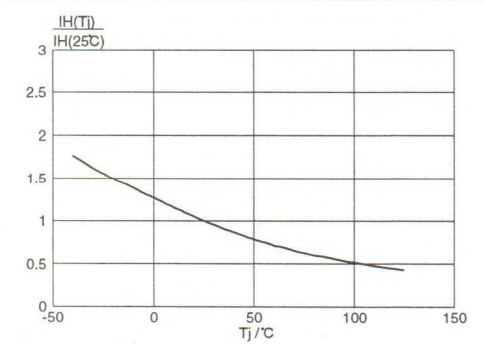



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

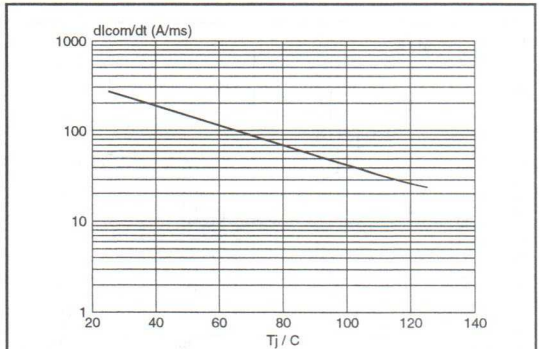



*Fig.12. Typical critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA212X series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

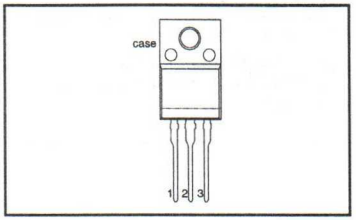
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA212X- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

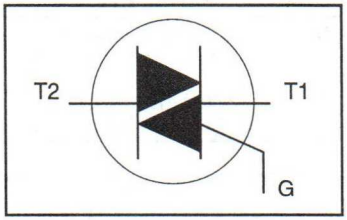
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 56$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle<br>with heatsink compound<br>without heatsink compound | -<br>- | -<br>- | 4.0<br>5.5 | K/W<br>K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | 2 | - | 35 | mA |
| | | T2+ G- | 2 | - | 35 | mA |
| | | T2- G- | 2 | - | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | - | 20 | mA |
| | | T2+ G- | - | - | 30 | mA |
| | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | - | 1.3 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs guaranteed commutation

# BTA212X series D, E and F

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack plastic envelope suitable for surface mounting, intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

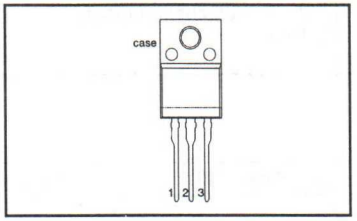
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | | 500D | 600D | - | |
| | BTA212X- | 500E | 600E | 800E | |
| | BTA212X- | 500F | 600F | 800F | |
| $V_{DRM}$ | BTA212X- Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 95 | 95 | 95 | A |

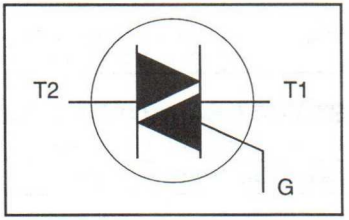
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 56$ °C | - | | 12 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 95 | | A |
| | | t = 16.7 ms | - | | 105 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 45 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Objective specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA212X- | | | ...D | ...E | ...F | |
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | | |
| | | T2+ G+ | 2 | - | 5 | 10 | 25 | mA |
| | | T2+ G- | 2 | - | 5 | 10 | 25 | mA |
| | | T2- G- | 2 | - | 5 | 10 | 25 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | | |
| | | T2+ G+ | - | - | 6 | 12 | 30 | mA |
| | | T2+ G- | - | - | 9 | 18 | 45 | mA |
| | | T2- G- | - | - | 6 | 12 | 30 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | - | 6 | 12 | 30 | mA |
| $V_T$ | On-state voltage | $I_T$ = 17 A | - | 1.3 | | | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | | | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | 0.25 | 0.4 | | | - | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | | | 0.5 | mA |

2 Device does not trigger in the T2-, G+ quadrant.

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | | | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BTA212X- | ...D | ...E | ...F | | | |
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 10 | 20 | 50 | TBF | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 12 A; $dV_{com}/dt$ = 20v/µs; gate open circuit | 2 | 3.5 | 4.5 | TBF | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 12 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | | | - | 2 | - | µs |

# Three quadrant triacs high commutation

# BTA216 series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

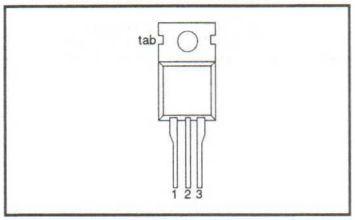
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA216- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

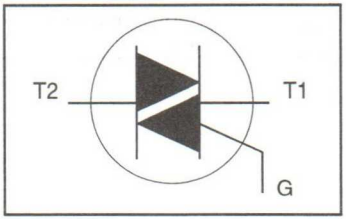
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | - | 28 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

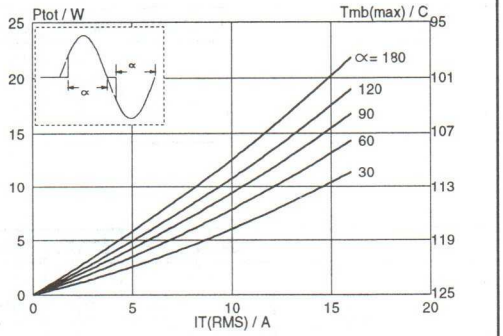



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

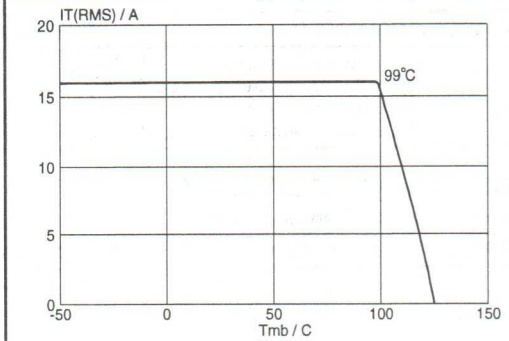



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

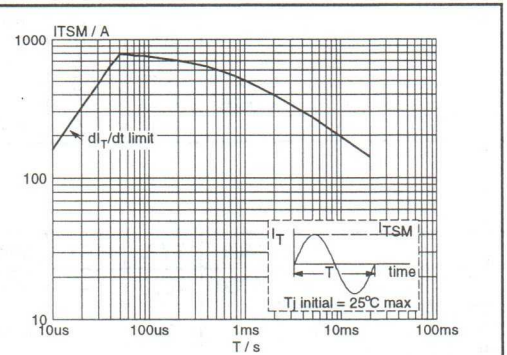



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

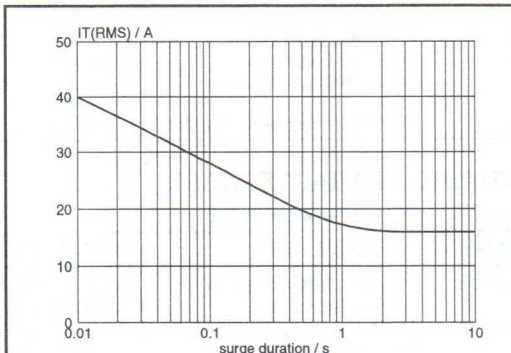



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

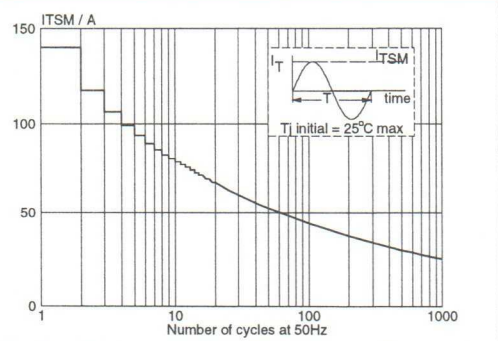



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*




*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

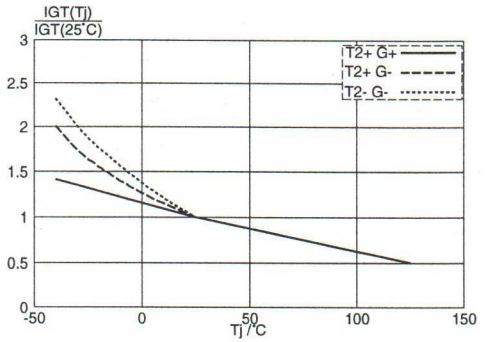



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

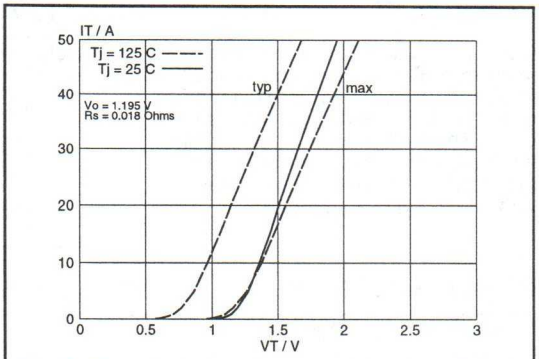



*Fig.10. Typical and maximum on-state characteristic.*

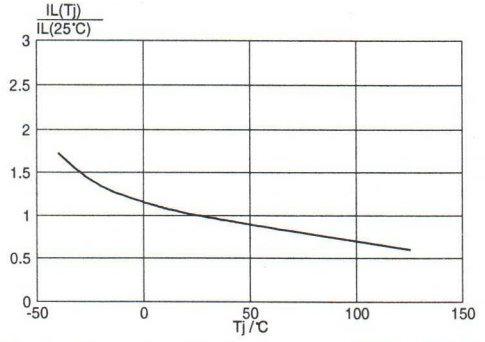



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

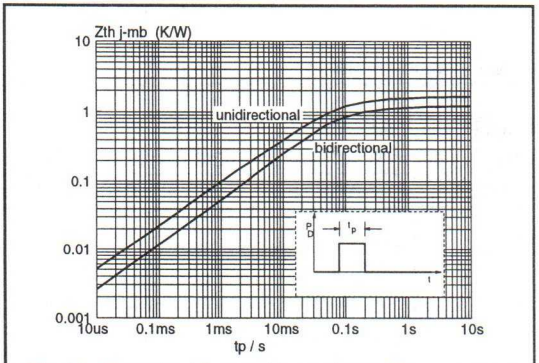



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

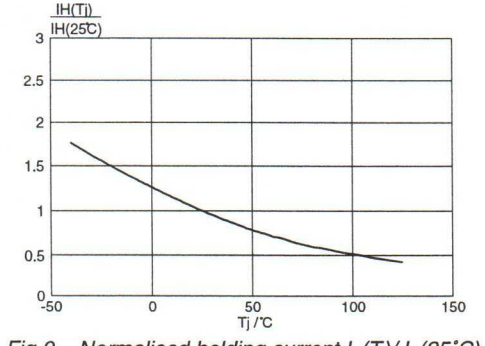



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

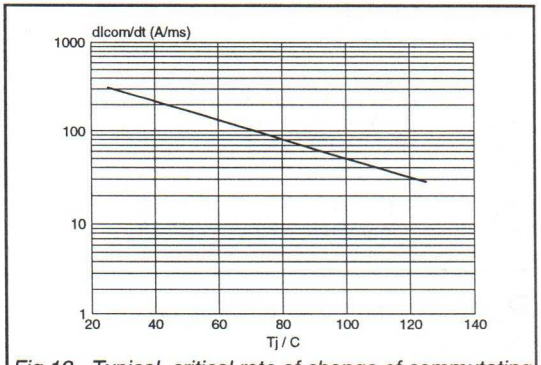



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA216 series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

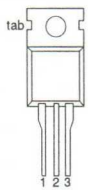
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA216-** | **500C** | **600C** | **800C** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

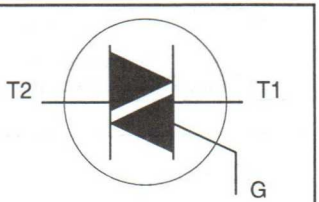
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 35 | mA |
| | | | T2+ G- | 2 | 21 | 35 | mA |
| | | | T2- G- | 2 | 34 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Triacs high commutation

# BTA216B series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

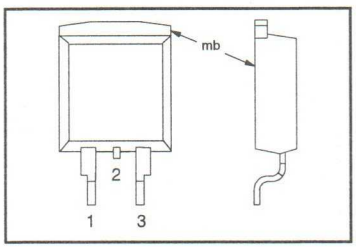
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA216B- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

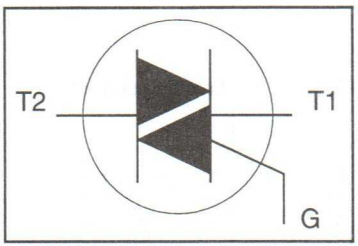
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | - | 28 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

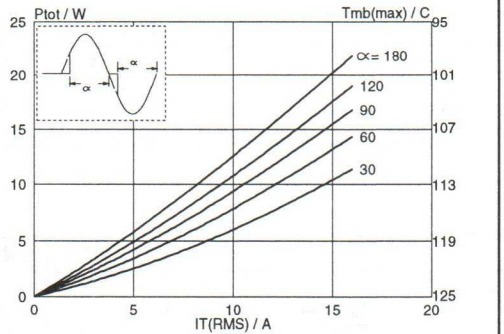



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

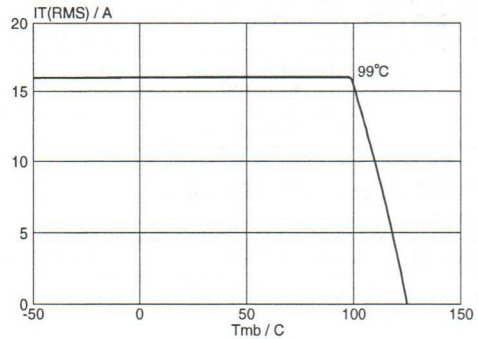



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

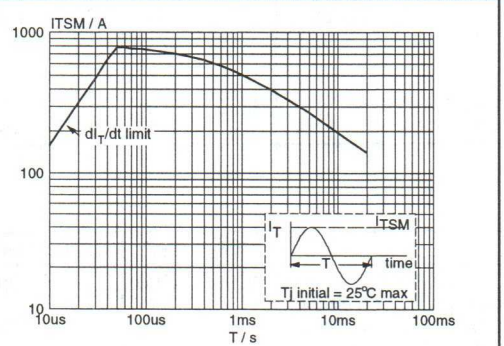



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

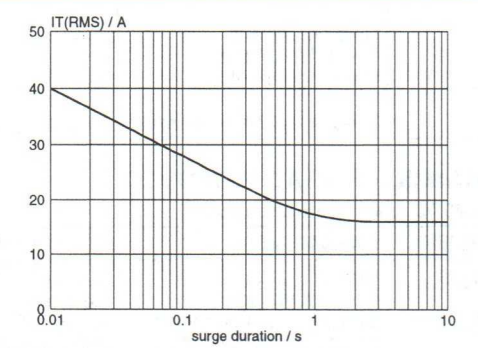



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.*

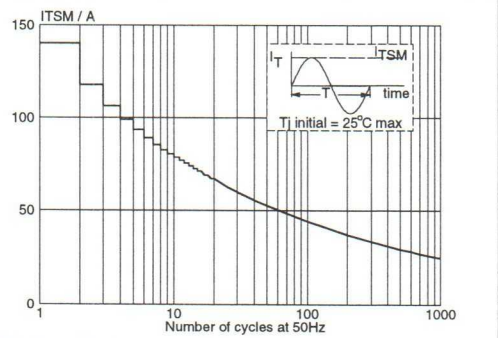



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

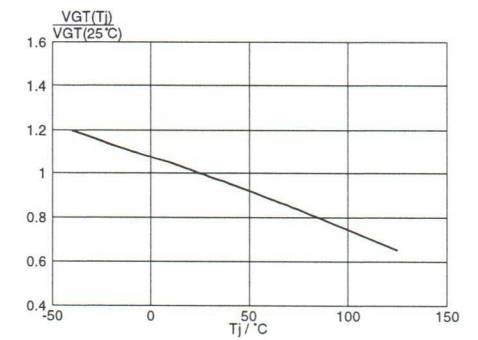



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

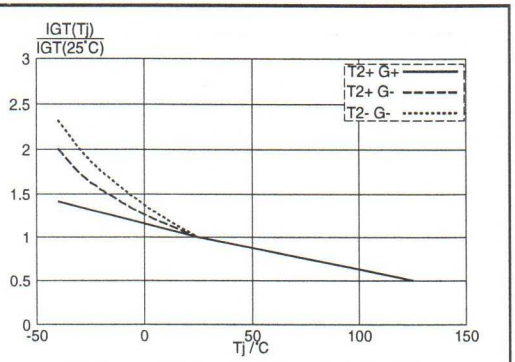



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

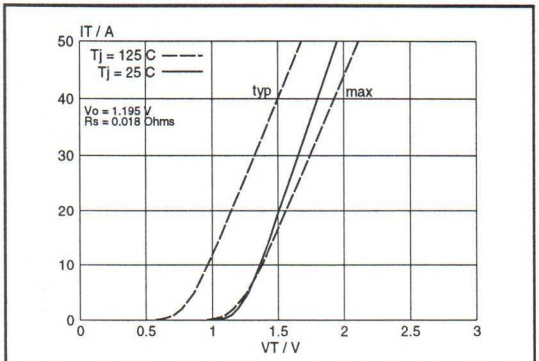



*Fig.10. Typical and maximum on-state characteristic.*

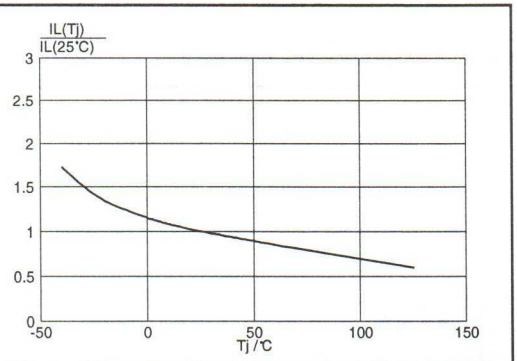



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

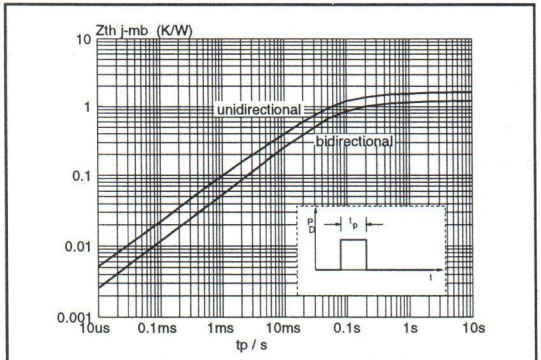



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

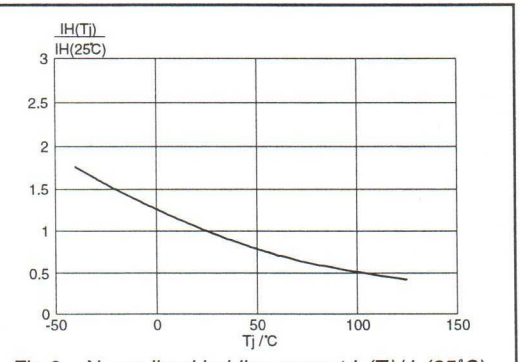



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

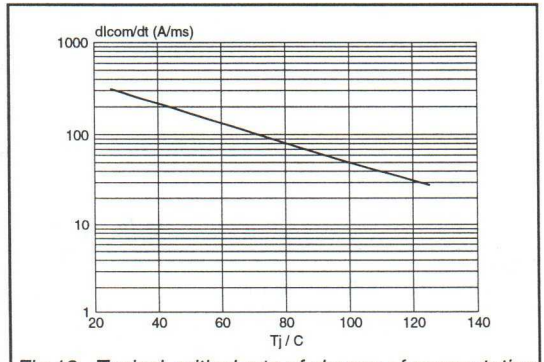



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

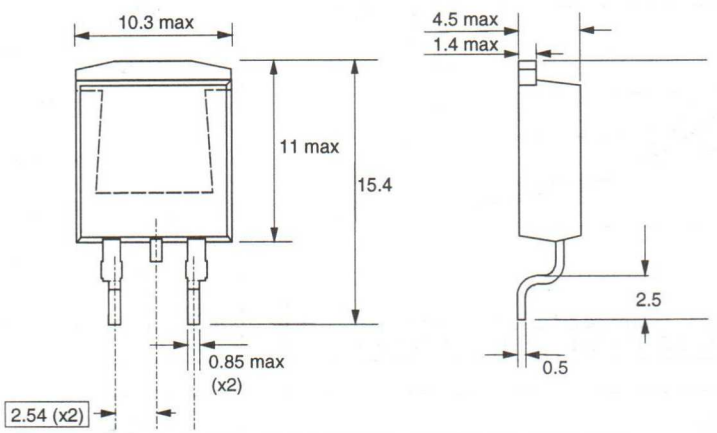



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

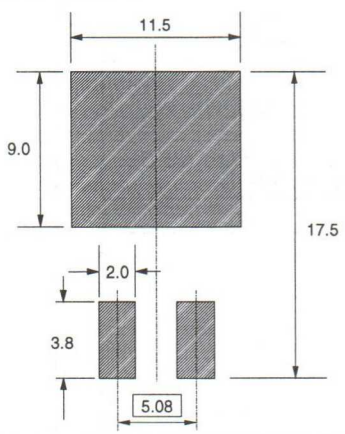



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA216B series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

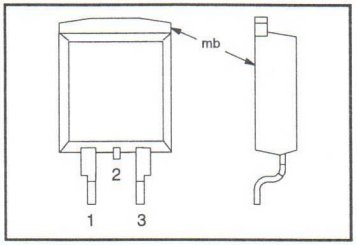
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA216B- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

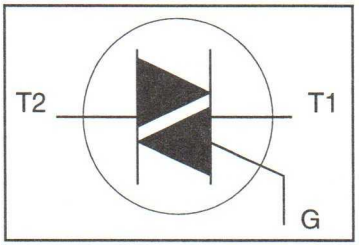
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 99$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

Preliminary specification

See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.2 | K/W |
| | | half cycle | - | - | 1.7 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 35 | mA |
| | | | T2+ G- | 2 | 21 | 35 | mA |
| | | | T2- G- | 2 | 34 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

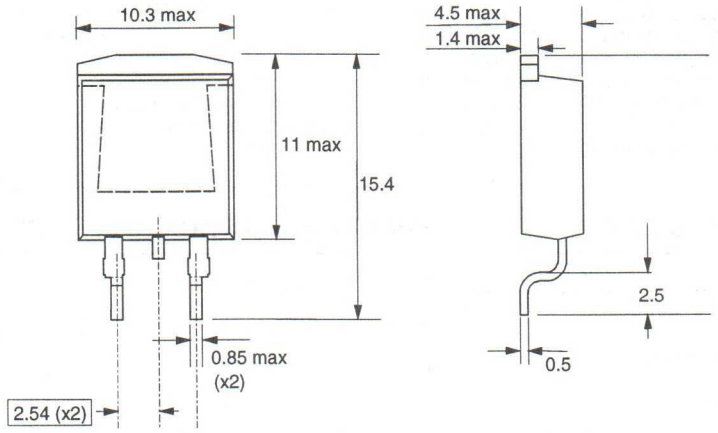



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

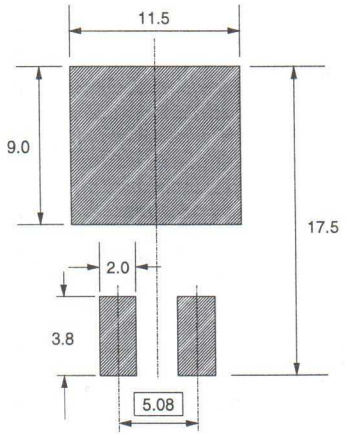



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA216X series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

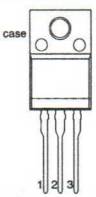
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA216X-** | **500B** | **600B** | **800B** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

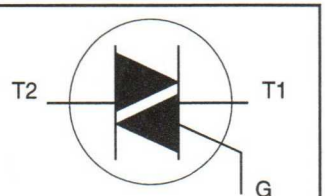
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 38$ °C | - | | 16 | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | | 140 | | A |
| | | t = 16.7 ms | - | | 150 | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | | 98 | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | 100 | | A/µs |
| $I_{GM}$ | Peak gate current | | - | | 2 | | A |
| $V_{GM}$ | Peak gate voltage | | - | | 5 | | V |
| $P_{GM}$ | Peak gate power | | - | | 5 | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | | 0.5 | | W |
| $T_{stg}$ | Storage temperature | | -40 | | 150 | | °C |
| $T_j$ | Operating junction temperature | | - | | 125 | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | - | 28 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

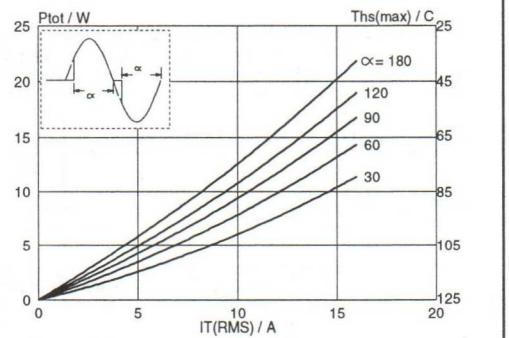



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

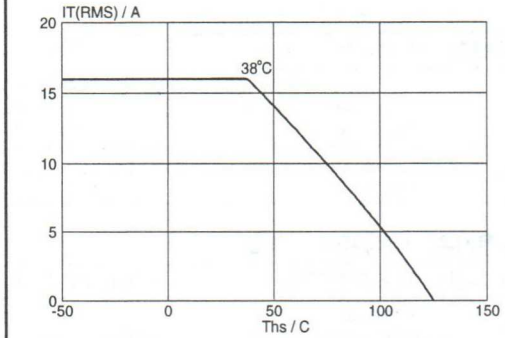



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

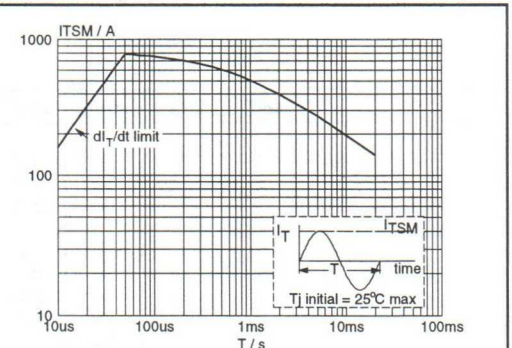



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

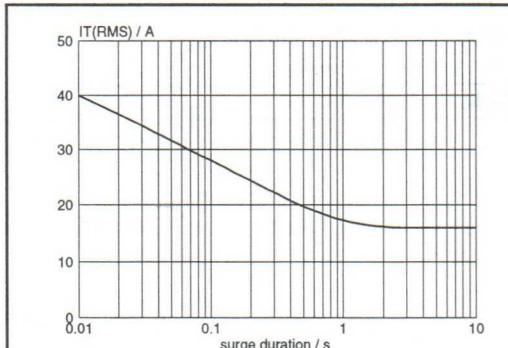



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38°C$.*

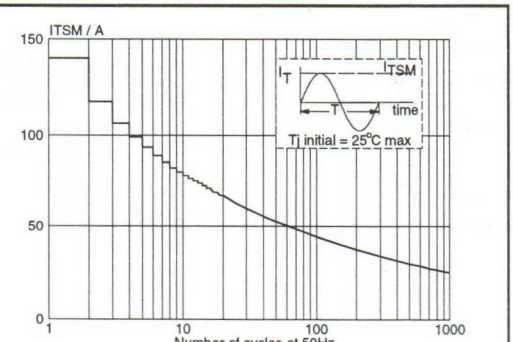



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

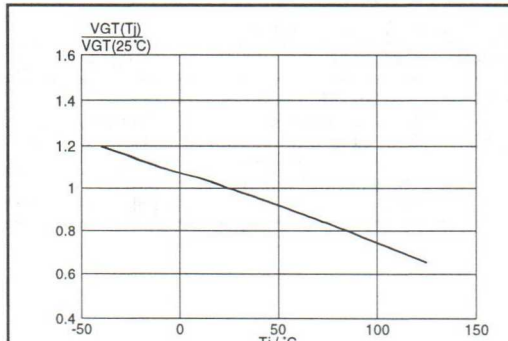



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

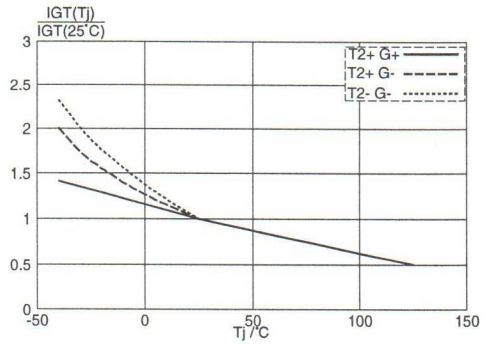



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

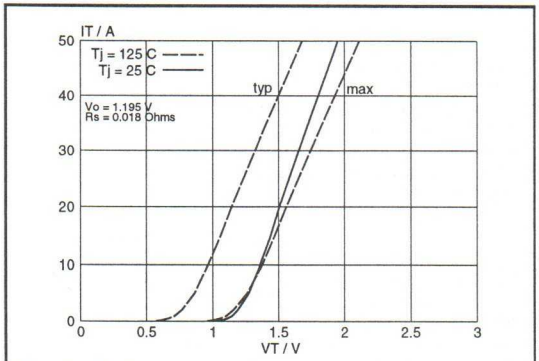



*Fig.10. Typical and maximum on-state characteristic.*

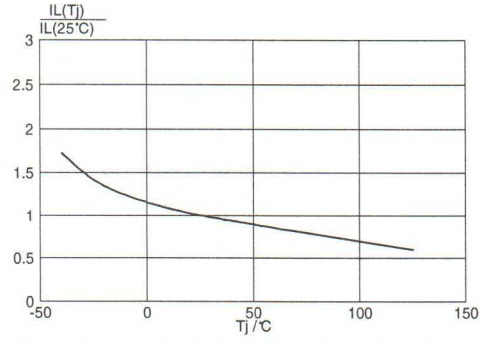



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

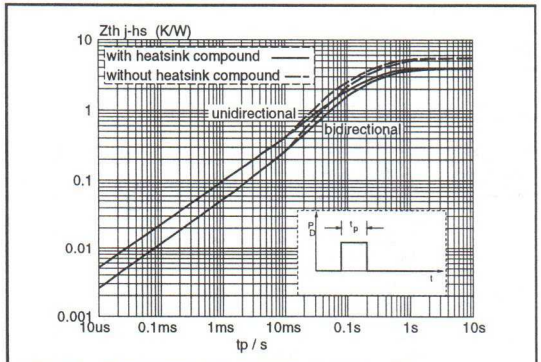



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

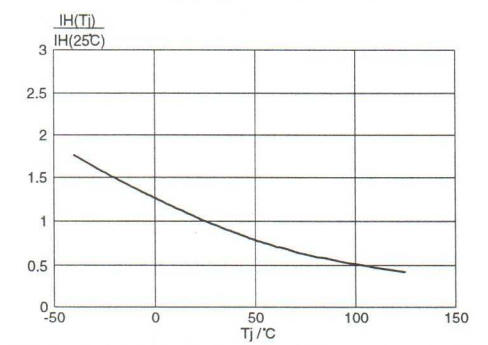



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

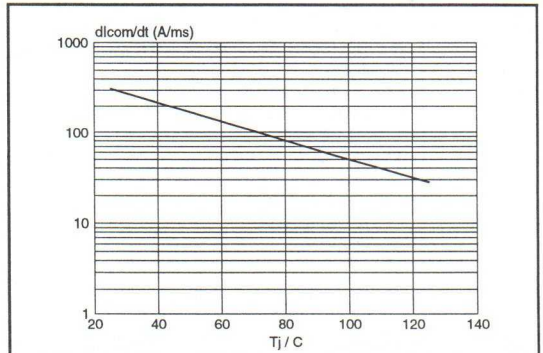



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA216X series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

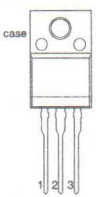
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA216X- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

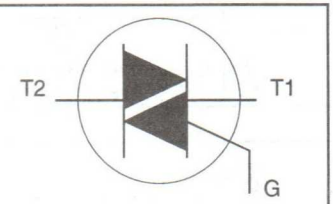
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 38$ °C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 20 A; $I_G$ = 0.2 A; $dI_G/dt$ = 0.2 A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

# Preliminary specification
# See Philips Semiconductors for Design-in information

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}hs}$ | Thermal resistance junction to heatsink | full or half cycle | | | | |
| | | with heatsink compound | - | - | 4.0 | K/W |
| | | without heatsink compound | - | - | 5.5 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 35 | mA |
| | | | T2+ G- | 2 | 21 | 35 | mA |
| | | | T2- G- | 2 | 34 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA225 series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

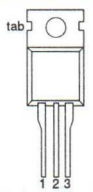
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA225- | 500B | 600B | 800B | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 190 | 190 | 190 | A |

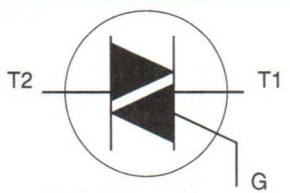
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 600[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.3 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\%\ V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; without snubber; gate open circuit | - | 44 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

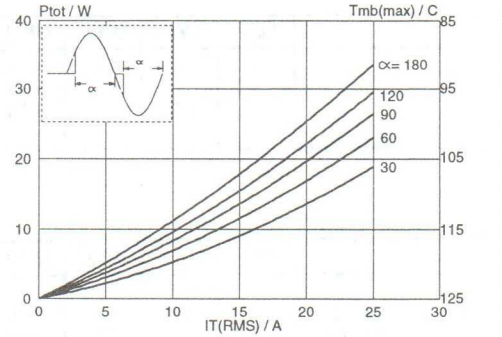



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

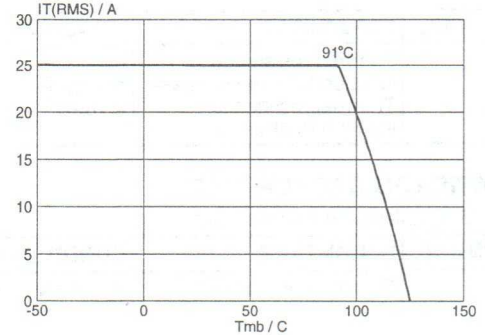



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

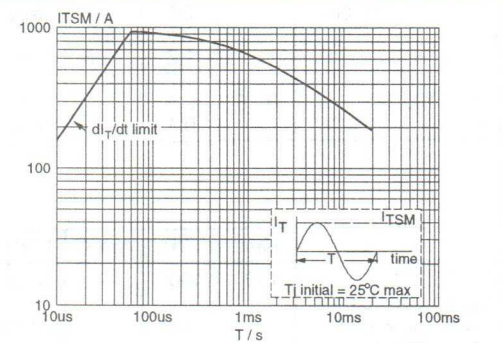



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

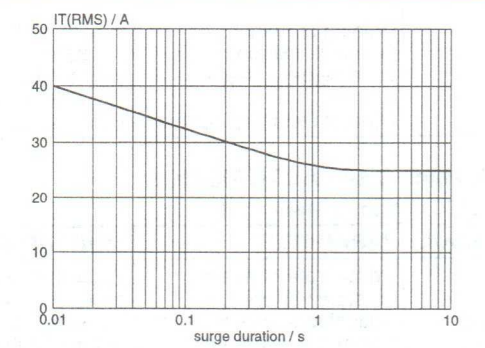



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 91°C$.*

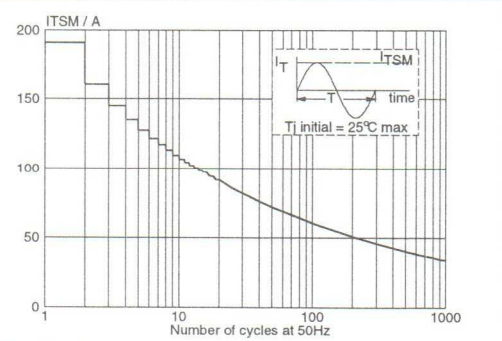



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

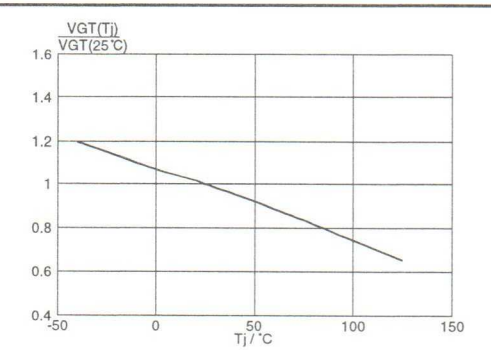



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

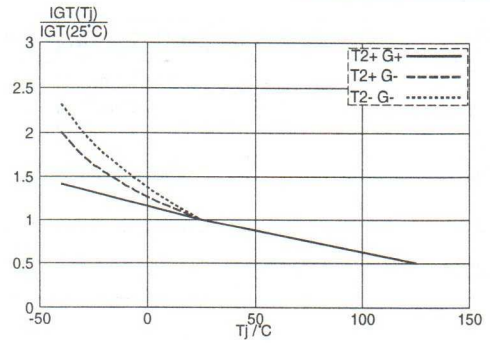



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

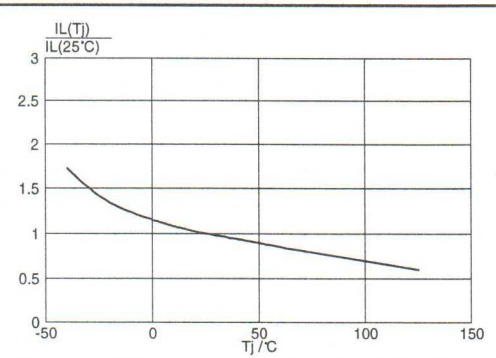



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

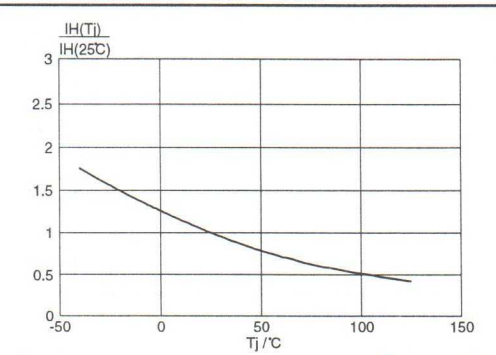



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

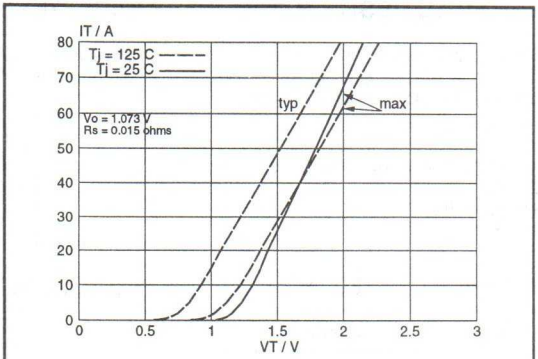



*Fig.10. Typical and maximum on-state characteristic.*

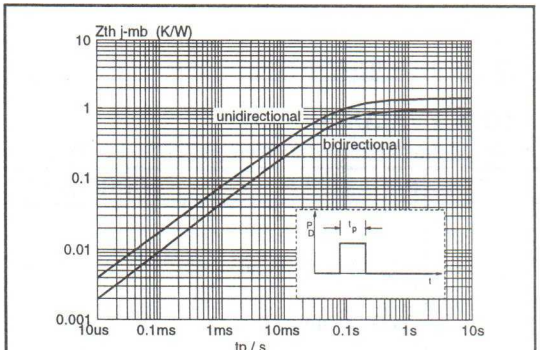



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

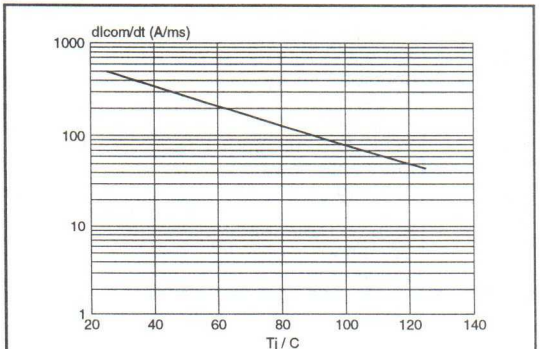



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

# Three quadrant triacs high commutation

# BTA225 series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

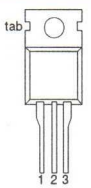
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA225- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 190 | 190 | 190 | A |

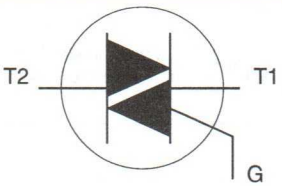
## PINNING - TO220AB

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| tab | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 600[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | in free air | - | 60 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 35 | mA |
| | | | T2+ G- | 2 | 21 | 35 | mA |
| | | | T2- G- | 2 | 34 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.3 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; without snubber; gate open circuit | - | 14 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

**2** Device does not trigger in the T2-, G+ quadrant.

# Three quadrant triacs high commutation

# BTA225B series B

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

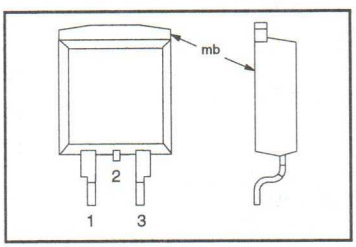
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | **BTA225B-** | **500B** | **600B** | **800B** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 180 | 180 | 180 | A |

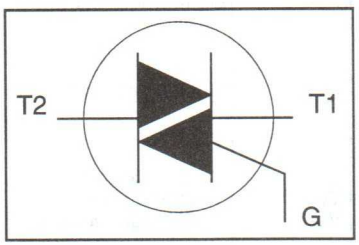
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | **-500** | **-600** | **-800** | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 50 | mA |
| | | | T2+ G- | 2 | 21 | 50 | mA |
| | | | T2- G- | 2 | 34 | 50 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | 31 | 60 | mA |
| | | | T2+ G- | - | 34 | 90 | mA |
| | | | T2- G- | - | 30 | 60 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | 31 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.2 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; without snubber; gate open circuit | - | 44 | - | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

2 Device does not trigger in the T2-, G+ quadrant.

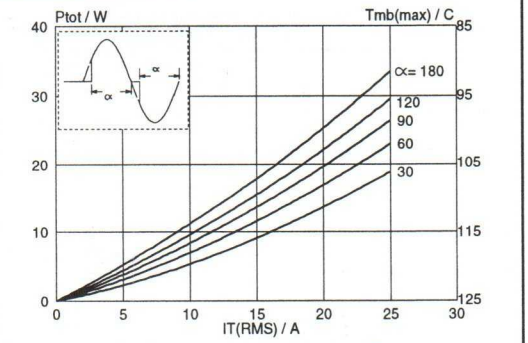



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

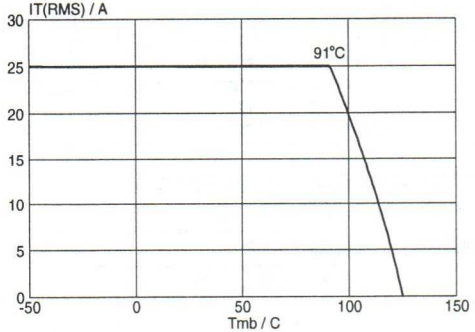



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature $T_{mb}$.*

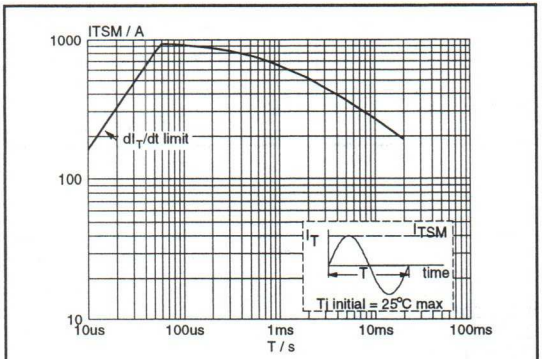



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

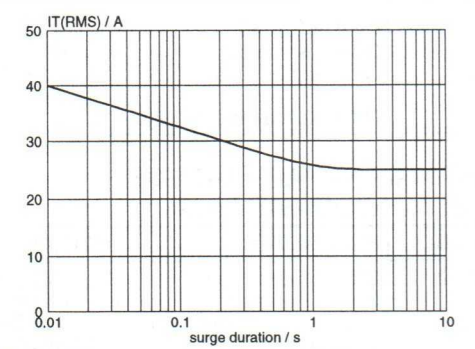



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 91°C$.*

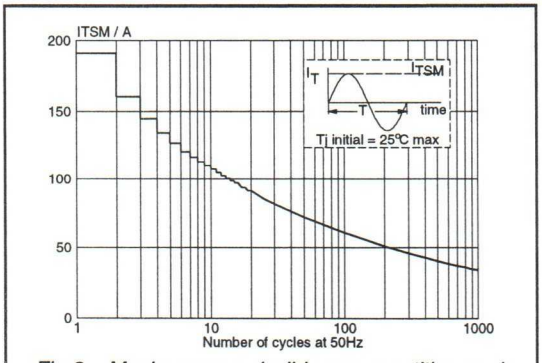



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

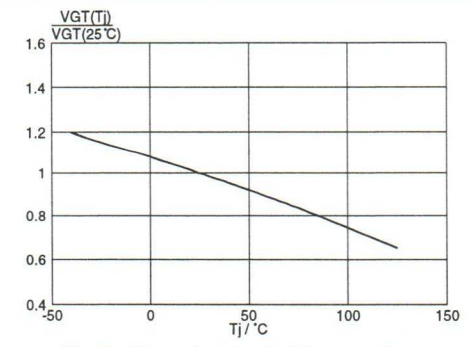



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature $T_j$.*

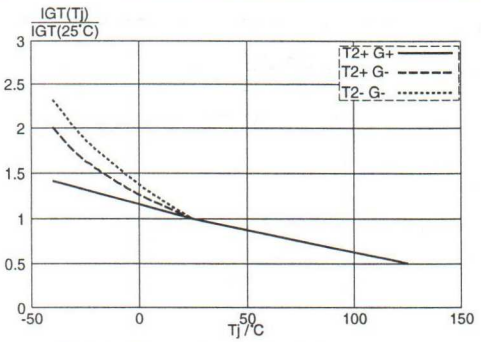



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature $T_j$.*

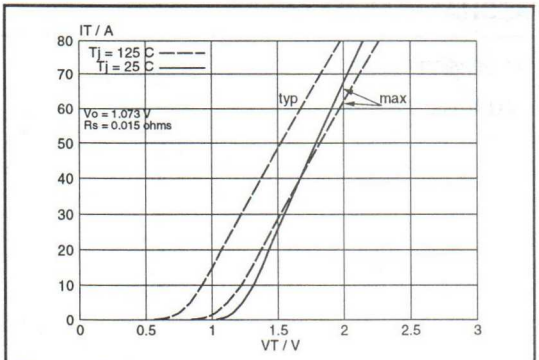



*Fig.10. Typical and maximum on-state characteristic.*

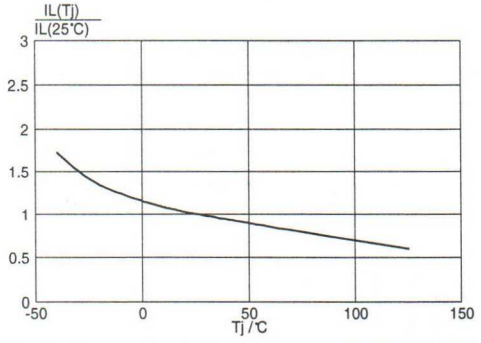



*Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature $T_j$.*

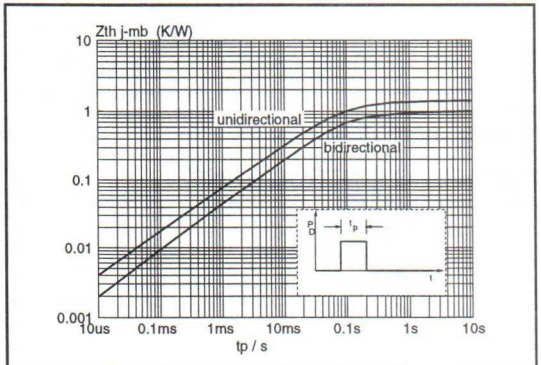



*Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width $t_p$.*

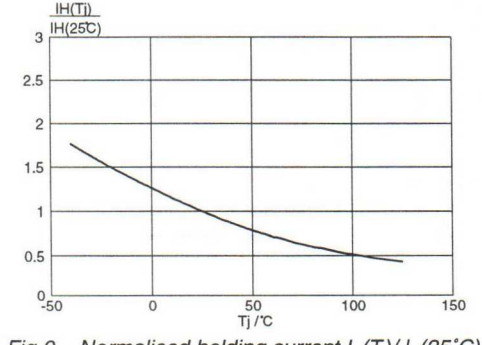



*Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature $T_j$.*

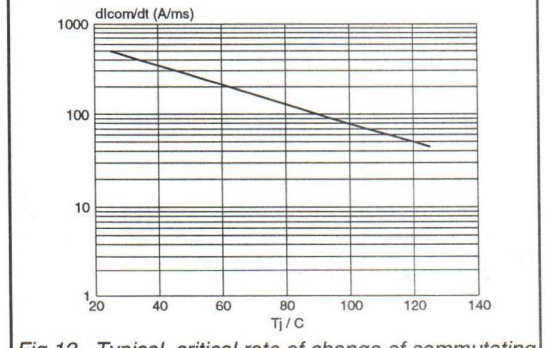



*Fig.12. Typical, critical rate of change of commutating current $dI_{com}/dt$ versus junction temperature.*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

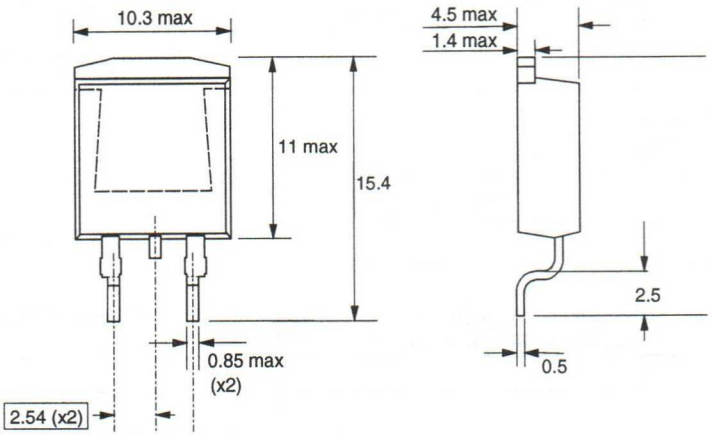



*Fig.13. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

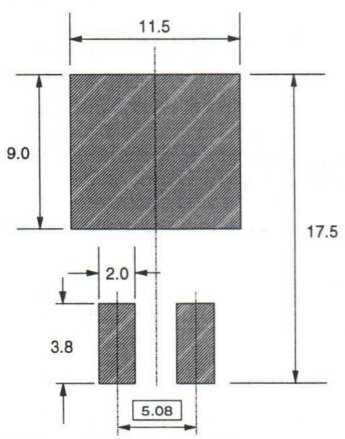



*Fig.14. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Three quadrant triacs high commutation

# BTA225B series C

## GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

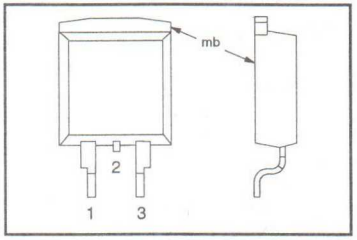
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BTA225B- | 500C | 600C | 800C | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 25 | 25 | 25 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 180 | 180 | 180 | A |

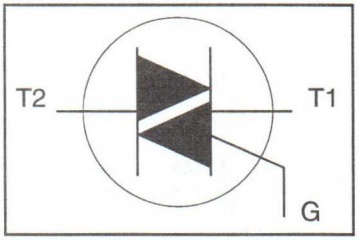
## PINNING - SOT404

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| mb | main terminal 2 |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 91$ °C | - | 25 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge | | | | | |
| | | t = 20 ms | - | 190 | | | A |
| | | t = 16.7 ms | - | 209 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 180 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | 100 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | °C |
| $T_j$ | Operating junction temperature | | - | 125 | | | °C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | full cycle | - | - | 1.0 | K/W |
| | | half cycle | - | - | 1.4 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current[2] | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | | |
| | | | T2+ G+ | 2 | 18 | 35 | mA |
| | | | T2+ G- | 2 | 21 | 35 | mA |
| | | | T2- G- | 2 | 34 | 35 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | | |
| | | | T2+ G+ | - | - | 20 | mA |
| | | | T2+ G- | - | - | 30 | mA |
| | | | T2- G- | - | - | 20 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | - | - | 15 | mA |
| $V_T$ | On-state voltage | $I_T$ = 30 A | | - | 1.2 | 1.55 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C | | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 °C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; gate open circuit | 1000 | - | V/µs |
| $dI_{com}/dt$ | Critical rate of change of commutating current | $V_{DM}$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; without snubber; gate open circuit | 3 | 14 | A/ms |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 30 A; $V_D = V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | µs |

2 Device does not trigger in the T2-, G+ quadrant.

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 1.4 g*

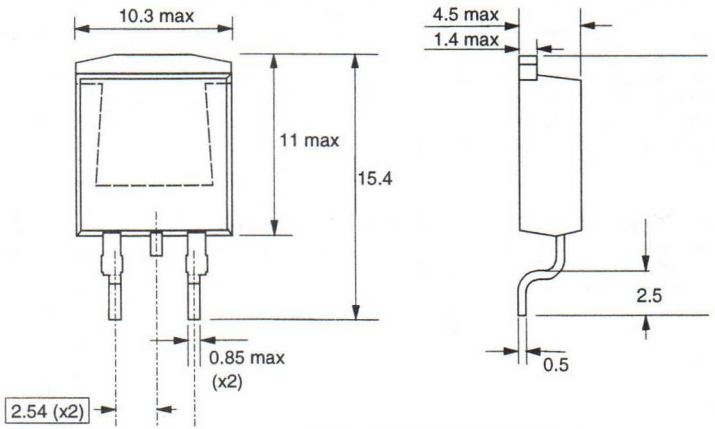



*Fig.1. SOT404 : centre pin connected to mounting base.*

**Notes**
1. Epoxy meets UL94 V0 at 1/8".

## MOUNTING INSTRUCTIONS

*Dimensions in mm*

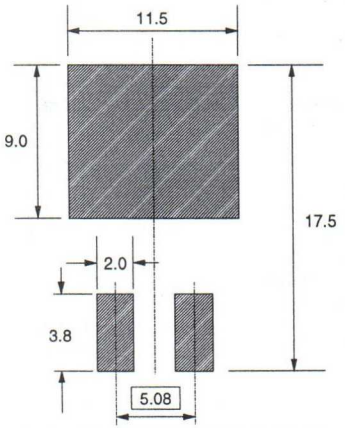



*Fig.2. SOT404 : minimum pad sizes for surface mounting.*

**Notes**
1. Plastic meets UL94 V0 at 1/8".

# Thyristor sensitive gate

# 2N5064

## GENERAL DESCRIPTION

Glass passivated sensitive gate thyristor in a plastic envelope, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integreated circuits and other low power gate trigger circuits.

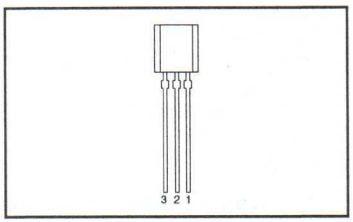
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|---|---|---|---|
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | 200 | V |
| $I_{T(AV)}$ | Average on-state current | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 0.8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 10 | A |

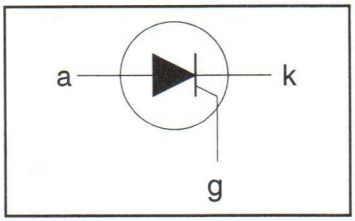
## PINNING - TO92 variant

| PIN | DESCRIPTION |
|---|---|
| 1 | anode |
| 2 | gate |
| 3 | cathode |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state voltages | | - | 200 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave | | | |
| | | $T_c \leq 67$ °C | - | 0.51 | A |
| | | $T_c \leq 102$ °C | - | 0.255 | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 0.8 | A |
| $I_{TRM}$ | Repetitive peak on-state current | | - | 8 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | half sine wave; $T_a$ = 25 °C prior to surge; t = 8.3 ms | - | 10 | A |
| $I^2t$ | $I^2t$ for fusing | t = 8.3 ms | - | 0.4 | $A^2s$ |
| $I_{GM}$ | Peak gate current | $T_a$ = 25°C, $t_p$ = 300µs; f = 120 Hz | - | 1 | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | V |
| $V_{RGM}$ | Peak reverse gate voltage | | - | 5 | V |
| $P_{GM}$ | Peak gate power | $T_a$ = 25°C | - | 0.1 | W |
| $P_{G(AV)}$ | Average gate power | $T_a$ = 25°C, over any 16 ms period | - | 0.01 | W |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |
| $T_j$ | Operating junction temperature | | -65 | 125 | °C |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j\text{-}c}$ | Thermal resistance junction to case | see note:[1] | - | - | 75 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | | - | 200 | - | K/W |

## STATIC CHARACTERISTICS

$T_c$ = 25 °C, $R_{GK}$ = 1 kΩ unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $T_c$ = 25 °C | - | - | 200 | µA |
| | | $T_c$ = -65 °C | - | - | 350 | µA |
| | | $V_D = V_{DRM(max)}$; $R_L$ = 100 Ω; gate open circuit | | | | |
| $I_L$ | Latching current | $V_D$ = 12 V; $R_{GK}$ = 1 kΩ | - | - | 6 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $R_{GK}$ = 1 kΩ | - | - | 5 | mA |
| $V_T$ | On-state voltage | $I_T$ = 1.2 A peak; $t_p$ = 300 µs; δ ≤ 0.01 | - | - | 1.7 | V |
| $V_{GT}$ | Gate trigger voltage | $T_j$ = 25 °C | - | - | 0.8 | V |
| | | $T_j$ = -65 °C | - | - | 1.2 | V |
| | | $T_j$ = 125 °C | 0.1 | - | - | V |
| | | $V_D = V_{DRM(max)}$; $R_L$ = 100 Ω; gate open circuit | | | | |
| $I_D$, $I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$ | | | | |
| | | $T_j$ = 25 °C | - | - | 10 | µA |
| | | $T_j$ = 125 °C | - | - | 50 | µA |

## DYNAMIC CHARACTERISTICS

$T_c$ = 25 °C, $R_{GK}$ = 1 kΩ unless otherwise stated

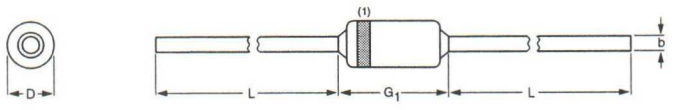
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; $R_{GK}$ = 1 kΩ | - | 25 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | Circuit commutated turn-off time | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

1 This measurement is made with the case mounted "flat side down" on a heatsink and held in position by means of a metal clamp over the curved surface.

## MECHANICAL DATA


| | Page |
|---|---|
| SOD27 | 550 |
| SOT54 | 551 |
| SOT54A | 552 |
| SOT54 variant | 553 |
| SOT78 | 554 |
| SOT82 | 555 |
| SOT186A | 556 |
| SOT223 | 557 |
| SOT404 | 558 |
| SOT428 | 559 |

**Hermetically sealed glass package; axial leaded; 2 leads** **SOD27**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | b max. | D max. | $G_1$ max. | L min. |
|---|---|---|---|---|
| mm | 0.56 | 1.85 | 4.25 | 25.4 |

0 1 2 mm
scale

**Note**

1. The marking band indicates the cathode.

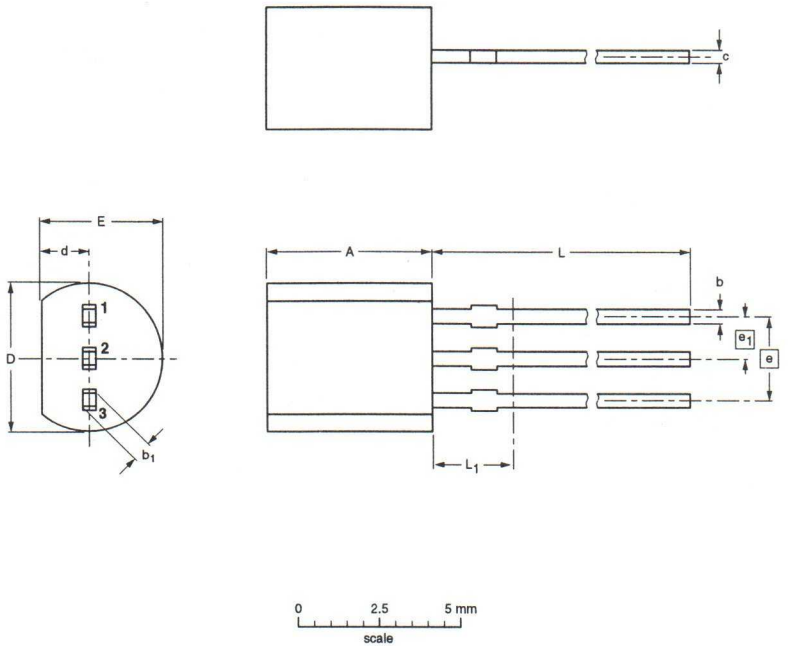
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOD27 | A24 | DO-35 | SC-40 | | | 97-06-09 |

*Fig. 1. SOD27 (DO35); axial-leaded hermetic glass envelope.*

**Notes**

1. For further information refer to mounting instructions for axial-leaded devices.

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.56 | 0.45<br>0.40 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

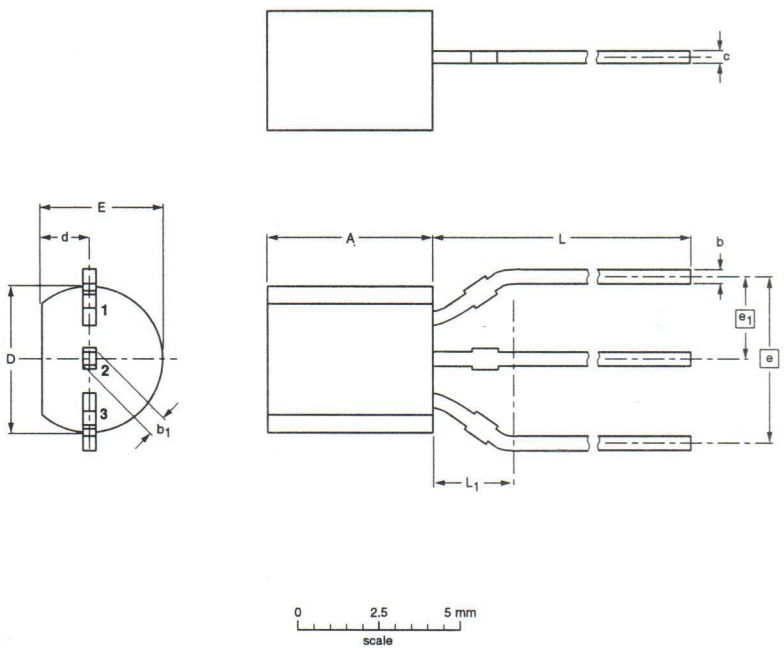
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT54 | | TO-92 | SC-43 | | | 97-02-28 |

*Fig. 2. SOT54 (TO92); plastic envelope; straight leads.*

**Notes**

1. For further information refer to mounting instructions for SOT54 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)** **SOT54A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.56 | 0.45<br>0.40 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 5.08 | 2.54 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

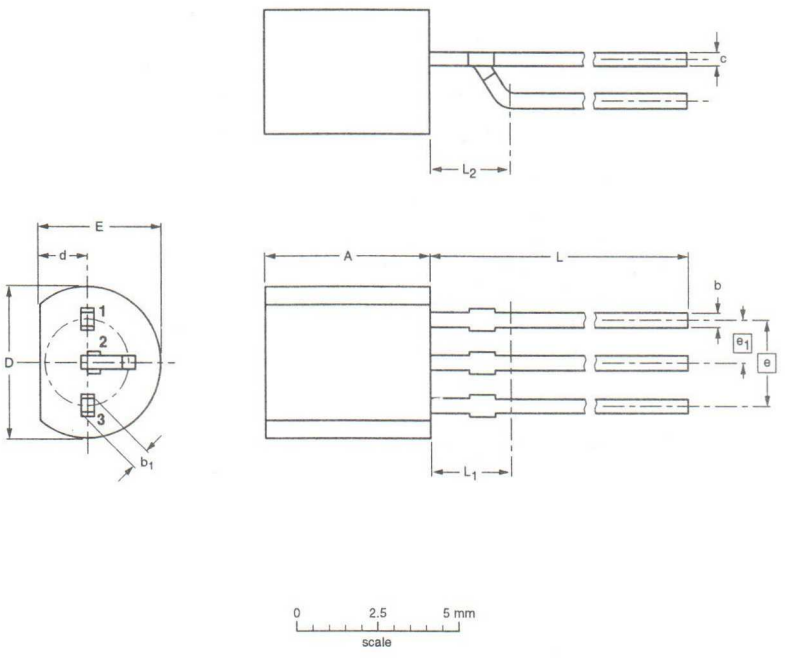
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT54A | | TO-92 | SC-43 | | | 97-05-13 |

*Fig. 3. SOT54 (TO92); plastic envelope; leadform A.*

**Notes**

1. For further information refer to mounting instructions for SOT54 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended leaded (through hole) package; 3 leads (on-circle)** **SOT54 variant**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max | $L_2$ max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.56 | 0.45<br>0.40 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 | 2.5 |

**Notes**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

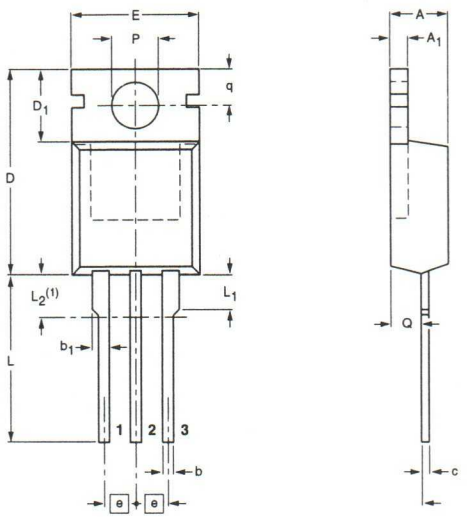
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT54 variant | | TO-92 | SC-43 | | | 97-04-14 |

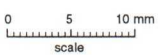
*Fig. 4. SOT54 (TO92); plastic envelope; variant.*

**Notes**

1. For further information refer to mounting instructions for SOT54 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220** **SOT78**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | c | D | $D_1$ | E | e | L | $L_1$ | $L_2$(1) max. | P | q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.39<br>1.27 | 0.9<br>0.7 | 1.3<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.4<br>5.9 | 10.3<br>9.7 | 2.54 | 15.0<br>13.5 | 3.30<br>2.79 | 3.0 | 3.8<br>3.6 | 3.0<br>2.7 | 2.6<br>2.2 |

Note

1. Terminals in this zone are not tinned.

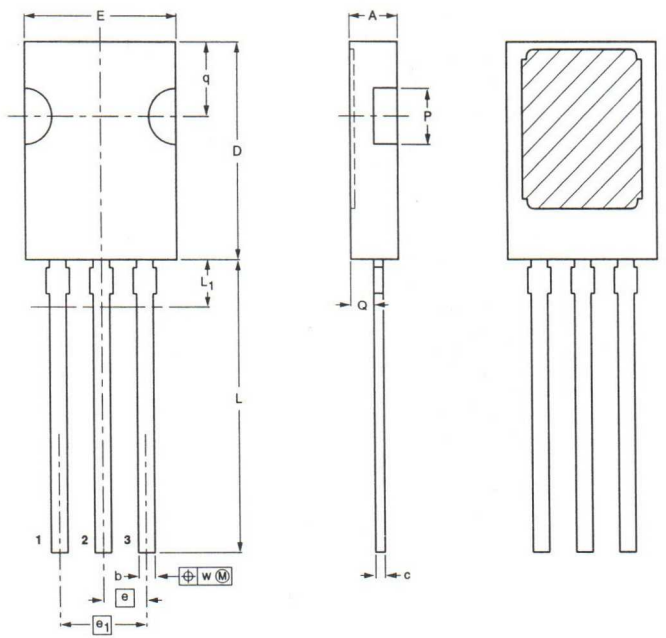
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT78 | | TO-220 | | | | 97-06-11 |

*Fig. 5. SOT78 (TO220AB); pin 2 connected to mounting base.*

**Notes**

1. For further information, refer to mounting instructions for SOT78 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended package; 3 leads (in-line)** **SOT82**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | c | D | E | e | $e_1$ | L | $L_1$ (1) max. | P | Q | q | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8<br>2.3 | 0.88<br>0.65 | 0.58<br>0.47 | 11.1<br>10.5 | 7.8<br>7.2 | 2.29 | 4.58 | 16.5<br>15.3 | 2.54 | 3.1<br>2.5 | 1.5<br>0.9 | 3.9<br>3.5 | 0.254 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

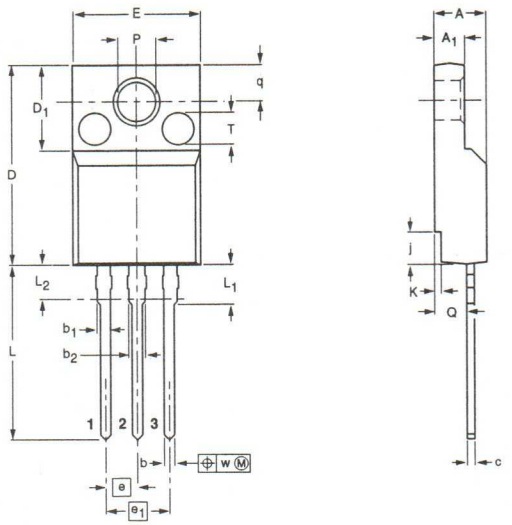
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT82 | | | | | | 97-06-11 |

*Fig. 6. SOT82; pin 2 connected to mounting base.*

**Notes**

1. For further information, refer to mounting instructions for SOT82 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220** **SOT186A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | D | $D_1$ | E | e | $e_1$ | j | K | L | $L_1$ | $L_2$ (1) max. | P | Q | q | T (2) | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.6<br>4.0 | 2.9<br>2.5 | 0.9<br>0.7 | 1.1<br>0.9 | 1.4<br>1.2 | 0.7<br>0.4 | 15.8<br>15.2 | 6.5<br>6.3 | 10.3<br>9.7 | 2.54 | 5.08 | 2.7<br>2.3 | 0.6<br>0.4 | 14.4<br>13.5 | 3.30<br>2.79 | 3 | 3.2<br>3.0 | 2.6<br>2.3 | 3.0<br>2.6 | 2.5 | 0.4 |

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are Ø 2.5 x 0.8 max. depth

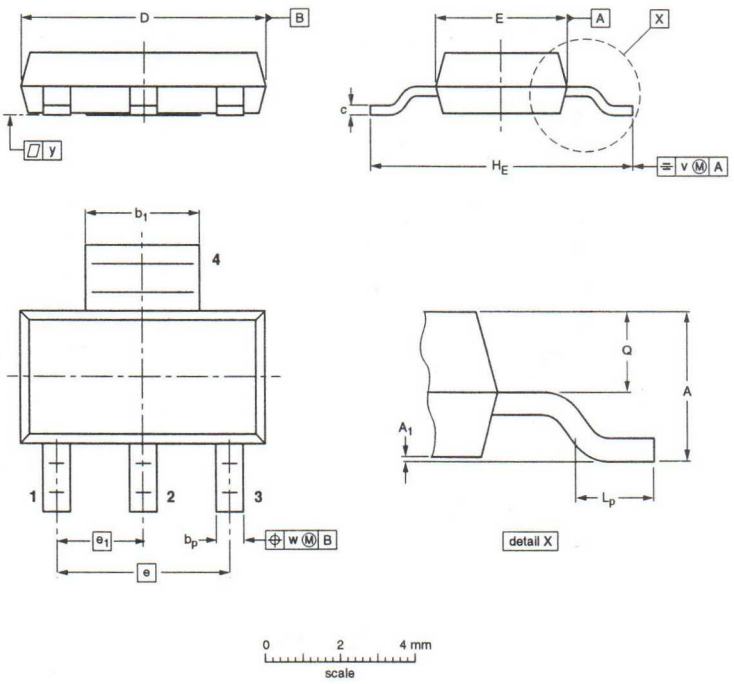
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT186A | | TO-220 | | | | 97-06-11 |

*Fig. 7. SOT186A; the seating plane is electrically isolated from all terminals.*

**Notes**

1. For further information, refer to mounting instructions for SOT186A envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic surface mounted package; collector pad for good heat transfer; 4 leads** **SOT223**




**DIMENSIONS (mm are the original dimensions)**

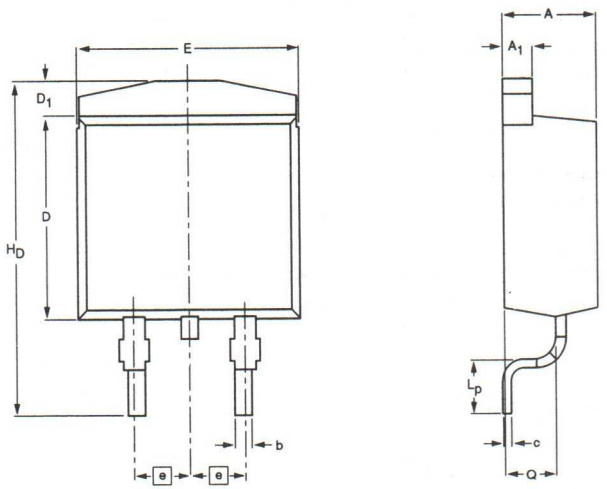
| UNIT | A | $A_1$ | $b_p$ | $b_1$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.8<br>1.5 | 0.10<br>0.01 | 0.80<br>0.60 | 3.1<br>2.9 | 0.32<br>0.22 | 6.7<br>6.3 | 3.7<br>3.3 | 4.6 | 2.3 | 7.3<br>6.7 | 1.1<br>0.7 | 0.95<br>0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT223 | | | | | | ~~96-11-11~~<br>97-02-28 |

*Fig. 8. SOT223 surface mounting package.*

**Notes**
1. For further information, refer to surface mounting instructions for SOT223 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic single-ended package (Philips version of D2-PAK); 2 leads** **SOT404**




**DIMENSIONS (mm are the original dimensions)**

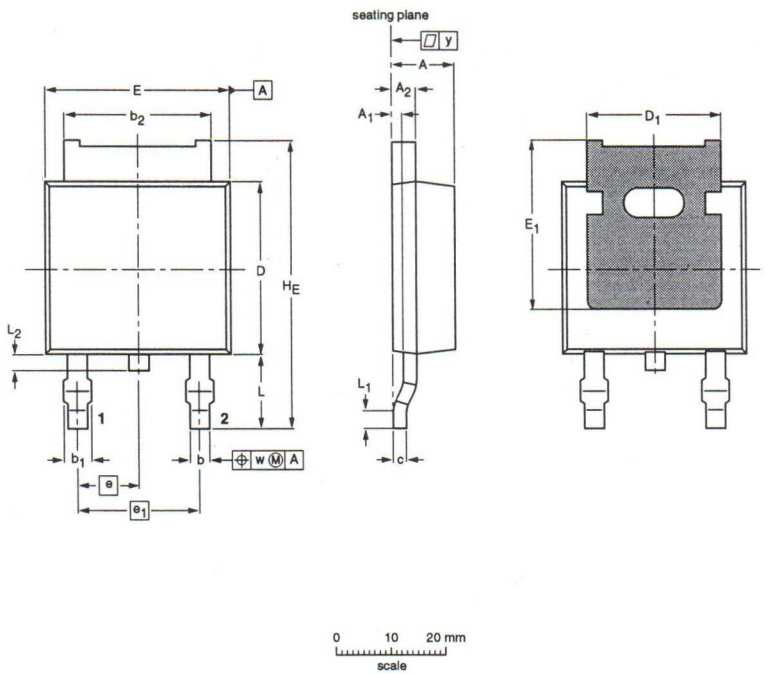
| UNIT | A | $A_1$ | b | c | D | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 9.65<br>8.65 | 1.6<br>1.2 | 10.3<br>9.7 | 2.54 | 2.9<br>2.1 | 15.4<br>14.8 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | 97-06-16 |

*Fig. 9. SOT404 surface mounting package.*

**Notes**
1. For further information, refer to mounting instructions for SOT404 envelope.
2. Epoxy meets UL94 V0 at 1/8".

**Plastic surface mounted package (Philips version of D-PAK); 2 leads** **SOT428**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$(1) | $A_2$ | b | $b_1$ max. | $b_2$ | c | D max. | $D_1$ max. | E max. | $E_1$ min. | e | $e_1$ | $H_E$ max. | L | $L_1$ min. | $L_2$ | w | y max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.65<br>0.45 | 0.89<br>0.71 | 0.89<br>0.71 | 1.1<br>0.9 | 5.36<br>5.26 | 0.4<br>0.2 | 6.22<br>5.98 | 4.81<br>4.45 | 6.73<br>6.47 | 4.0 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.7<br>0.5 | 0.2 | 0.2 |

**Note**

1. Measured from heatsink back to lead.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT428 | | | | | | 97-06-11 |

*Fig. 10. SOT428 surface mounting package.*

**Notes**

1. For further information, refer to mounting instructions for SOT428 envelope.
2. Epoxy meets UL94 V0 at 1/8".

# MOUNTING INSTRUCTIONS


| | page |
|---|---|
| Axial-leaded devices | 562 |
| SOT54 (TO92) | 563 |
| SOT82 | 564 |
| SOT78 (TO220AB); SOT186A | 567 |
| SOT223; SOT428; SOT404 | 572 |

## GENERAL DATA AND INSTRUCTIONS

### General rules

Excessive forces or temperature applied to a diode may cause serious damage. To avoid damage when soldering and mounting, the following rules should be followed.

Perpendicular forces on the body of the diode must be avoided.

Sudden shocks to the leads or body must be avoided.

### Soldering

Avoid any force on the body or leads during or just after soldering.

Do not correct the position of an already soldered device by pushing, pulling or twisting the body.

Allow the diode to cool slowly after soldering.

### Lead bending

During bending, the leads must be supported between body and bending point.

Axial forces on the lead during bending must not exceed 20 N.

If the leads can be supported without touching the body or welds, then bending the leads through 90° is allowed at any distance from the body.

If the bend radius is greater than 0.5 mm, then bending the leads close to the body is permitted without supporting the leads.

Twisting the leads is allowed at any distance from the body if the lead is properly clamped.

If the leads are not clamped, then twisting the leads is permitted at a distance of greater than 3 mm from the body. The torque angle must not exceed 30°.

When straightening leads, the pulling force in the axial direction should not exceed 20 N and the duration must not exceed 5 s.

**Maximum allowable soldering time and minimum distance soldering point to seal for axial envelopes**

| | | Hand iron soldering mounted other than on a printed circuit board. (Max solder temperature = 300°C.) | | Hand iron soldering, dip, wave or other bath soldering onto a printed circuit board. (Max solder temperature = 300°C.) | |
|---|---|---|---|---|---|
| Envelope | Material | Time (s) | Distance (mm) | Time (s) | Distance (mm) |
| SOD27, DO35, SOD84 | Glass | 3 | 0.5 | 5 | 0.5 |

# Mounting instructions

# SOT54 (TO92)

## GENERAL DATA AND INSTRUCTIONS

### General rules

1. Avoid stress to the leads.
2. Follow the leadbending guidelines.
3. Position the device before soldering, not afterwards.

### Soldering

Recommendations for devices with a maximum storage temperature rating $T_{stg} \leq 150$ °C:

DIP OR WAVE SOLDERING

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

### Lead bending

Various leadform options are available on products supplied in this outline.

The leads can be bent, twisted or straightened provided they are clamped close to the plastic body. This avoids damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred.

# Mounting instructions

# SOT82

## GENERAL DATA AND INSTRUCTIONS

### General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.

### Mounting methods

#### Clip mounting

Mounting with a spring clip gives:

a) A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.

b) Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

### Heatsink requirements

Minimum thickness: 2 mm.

Flatness in the mounting area: 0.02 mm maximum per 10 mm.

### Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a smear of aluminium oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator. Avoid applying excess compound as the thermal resistance that results can be higher than if no compound is applied.

### Thermal data for various heatsink mounting methods

The mounting base-to-heatsink thermal resistance ($R_{th\ mb\text{-}h}$) is envelope dependent, not device dependent. It applies to all devices in a given envelope. The figures given in the table below assume optimum mounting conditions (i.e. flat heatsink, spring clip mounted, optimum quantity of heatsink compound where applicable). However the junction-to-mounting base thermal resistance ($R_{th\ j\text{-}mb}$) IS device dependent; figures are quoted separately in each data sheet.

| $R_{th\ mb\text{-}h}$ | Thermal resistance from mounting base to heatsink | K/W |
|---|---|---|
| **Mounting method** | | **clip** |
| Direct with heatsink compound | | 0.4 |
| Direct without heatsink compound | | 2.0 |
| With heatsink compound and 0.1 mm maximum mica insulator | | 2.0 |
| Without heatsink compound and 0.1 mm maximum mica insulator | | 5.0 |

### Soldering

Recommendations for devices with a maximum storage temperature rating $T_{stg} \leq 150$ °C:

DIP OR WAVE SOLDERING

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

### Lead bending

Lead forming by Philips is available as an option on all products supplied in this outline.

Maximum permissible tensile force on the body for 5 seconds is 20 N.

The leads can be bent, twisted or straightened. To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred. See Figure 1. Surface cracks in the plating on the lead are common when a radius less than 1.5 x lead thickness is used. Although this exposes the copper material, these cracks do not affect the mechanical strength of the lead.

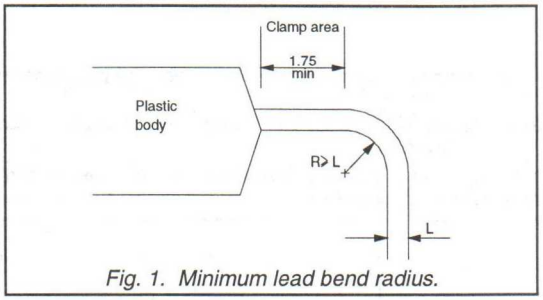



*Fig. 1. Minimum lead bend radius.*

**Additional guidelines**

It is recommended that, where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, a bend is formed into the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in Figure 2 below. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.

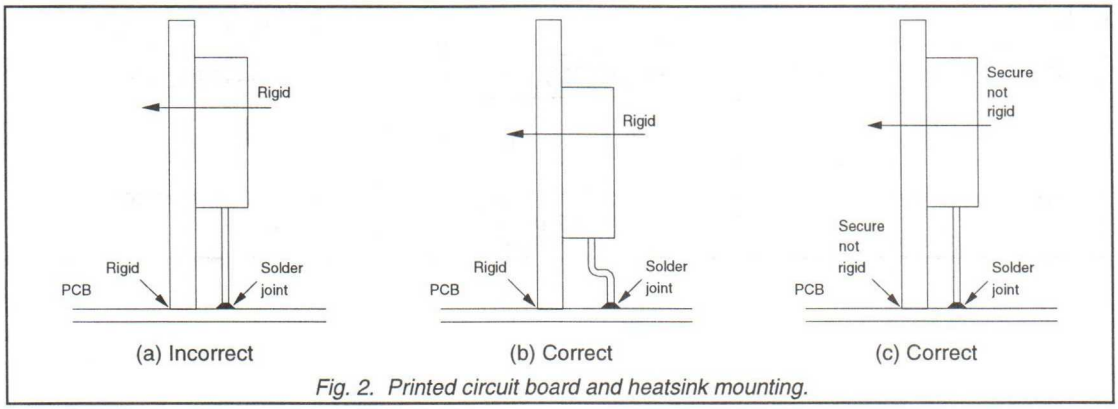



*Fig. 2. Printed circuit board and heatsink mounting.*

## INSTRUCTIONS FOR CLIP MOUNTING

**Direct mounting with spring clip**

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figures 3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. See Figure 5.

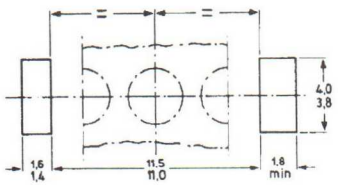



*Fig. 3. Heatsink requirements.*

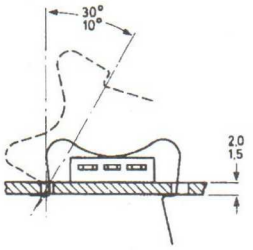



*Fig. 4. Mounting.*

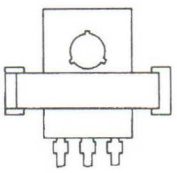


*Fig. 5. Position of device (top view).*

**Insulated mounting with clip and insulator**

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figures 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. Ensure that the device is centred on the mica insulator to prevent unwanted movement.

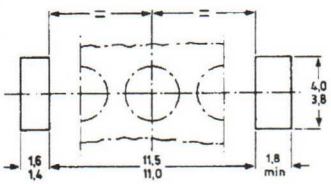



*Fig. 6. Heatsink requirements.*

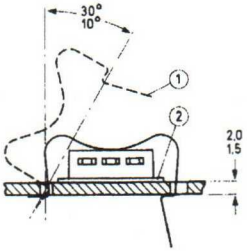



*Fig. 7. Mounting*
*(1) spring clip.*
*(2) insulator.*

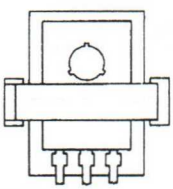


*Fig. 8. Position of device (top view).*

## GENERAL DATA AND INSTRUCTIONS

### General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.
4. When screw mounting, the rectangular washer should not exert any force on the plastic part of the body.

### Mounting methods

CLIP MOUNTING

Mounting with a spring clip gives:

a) A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.
b) Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

M3 SCREW MOUNTING

It is recommended that a metal washer is inserted between screw head and mounting tab.

Do not use self-tapping screws.

Mounting torque for screw mounting:
For thread-forming screws these are final values.

Minimum torque for good heat transfer is 0.55 Nm.

Maximum torque to avoid damaging the device is 0.80 Nm.

When a nut or screw is driven directly against the tab, the torques are as follows:

Minimum torque for good heat transfer is 0.40 Nm.

Maximum torque to avoid damaging the device is 0.60 Nm.

RIVET MOUNTING NON-INSULATED

The device should not be pop-riveted to the heatsink. It is permissible to press-rivet the metal tab providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled.

This method is not permitted for full-pack envelopes (SOT186A) because it will damage the plastic encapsulation.

### Heatsink requirements

Flatness in the mounting area: 0.02 mm maximum per 10 mm.
Mounting holes must be deburred. For further information see clip and screw mounting instructions.

### Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a smear of aluminium oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator. Avoid applying excess compound as the thermal resistance that results can be higher than if no compound is applied.

### Thermal data for TO220 envelopes with various heatsink mounting methods

The mounting base-to-heatsink thermal resistance ($R_{th\ mb\text{-}h}$) is envelope dependent, not device dependent. It applies to all devices in a given envelope. The figures given in the table below assume optimum mounting conditions (i.e. flat heatsink, spring clip mounted, optimum quantity of heatsink compound where applicable). However the junction-to-mounting base thermal resistance ($R_{th\ j\text{-}mb}$) IS device dependent; figures are quoted separately in each data sheet.

For Full-pack (SOT186A) devices, junction-to-heatsink thermal resistance ($R_{th\ j\text{-}h}$) with and without heatsink compound are quoted separately in each data sheet.

| $R_{th\ mb\text{-}h}$ Thermal resistance from mounting base to heatsink | K/W | |
|---|---|---|
| **Mounting method** | **clip** | **screw** |
| Direct with heatsink compound | 0.3 | 0.5 |
| Direct without heatsink compound | 1.4 | 1.4 |
| With heatsink compound and 0.1 mm maximum mica insulator | 2.2 | - |
| With heatsink compound and 0.25 mm maximum alumina insulator | 0.8 | - |
| With heatsink compound and 0.05 mm mica insulator | | |
| insulated up to 500 V | - | 1.4 |
| insulated up to 800 V / 1000 V | - | 1.6 |
| Without heatsink compound and 0.05 mm mica insulator | | |
| insulated up to 500 V | - | 3.0 |
| insulated up to 800 V / 1000 V | - | 4.5 |

Additional insulators are generally not required when mounting the full-pack (SOT186A) envelope.

### Soldering

Recommendations for devices with a maximum storage temperature rating ≤ 175 °C:

DIP OR WAVE SOLDERING

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

It is not permitted to solder the metal tab of the device to a heatsink.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

**Lead bending**

Maximum permissible tensile force on the body for 5 seconds is 20 N.

The leads can be bent, twisted or straightened. To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred. See Figure 1. Surface cracks in the plating on the lead are common when a radius less than 1.5 x lead thickness is used. Although exposing the copper material, these cracks do not affect the mechanical strength of the lead. Lead forming by Philips is available as an option on all products supplied in these outlines.

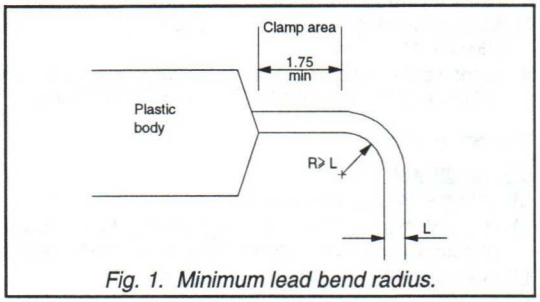



*Fig. 1. Minimum lead bend radius.*

**Additional guidelines**

It is recommended that, where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, a bend is formed into the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in Figure 2 below. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.

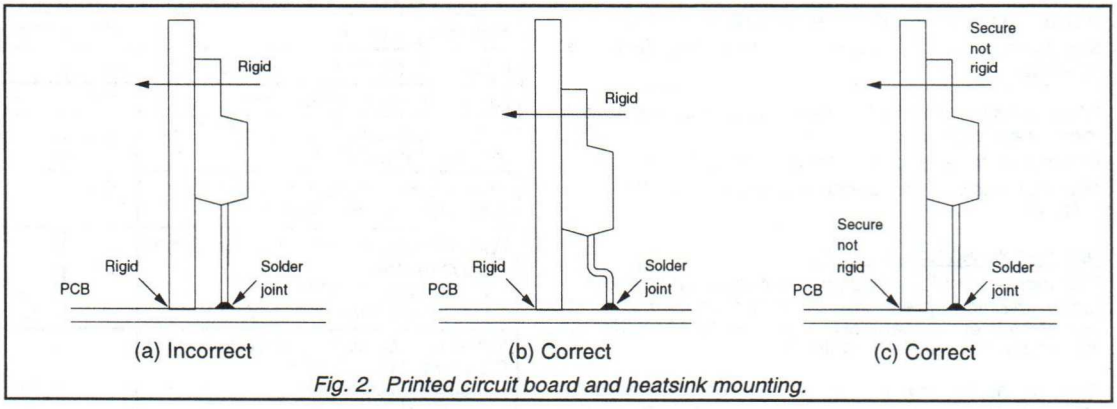



*Fig. 2. Printed circuit board and heatsink mounting.*

## INSTRUCTIONS FOR CLIP MOUNTING

### Direct mounting with spring clip

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figures 3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. See Figure 5.

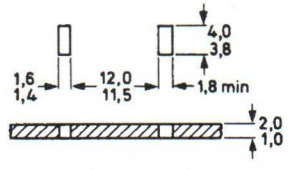



*Fig. 3. Heatsink requirements.*

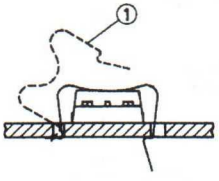



*Fig. 4. Mounting.*
*(1) spring clip.*

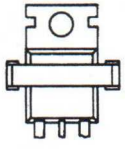


*Fig. 5. Position of device (top view).*

### Insulated mounting with spring clip

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figures 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent unwanted movement.

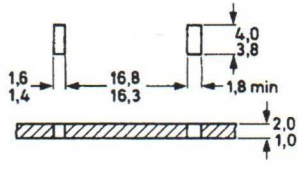



*Fig. 6. Heatsink requirements.*

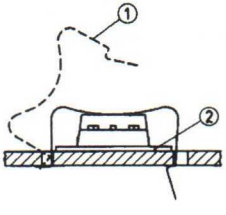



*Fig. 7. Mounting*
*(1) spring clip.*
*(2) insulator.*

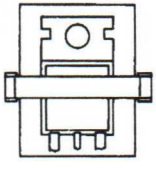


*Fig. 8. Position of device (top view).*

## INSTRUCTIONS FOR SCREW MOUNTING

### Direct mounting with screw and spacing washer

THROUGH HEATSINK WITH NUT

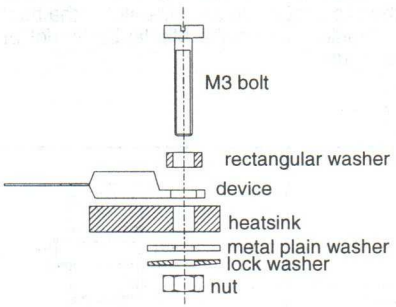



*Fig. 9. Assembly.*

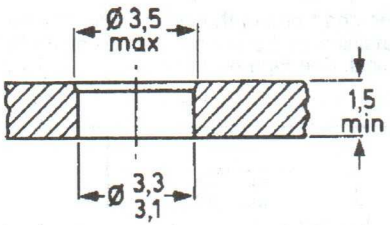



*Fig. 10. Heatsink requirements.*

INTO TAPPED HEATSINK

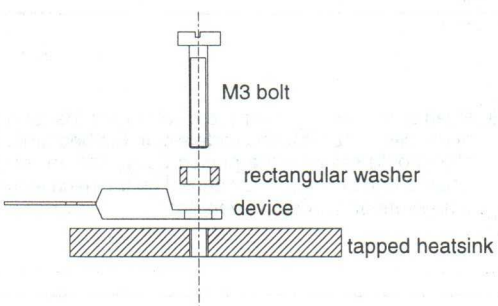



*Fig. 11. Assembly.*

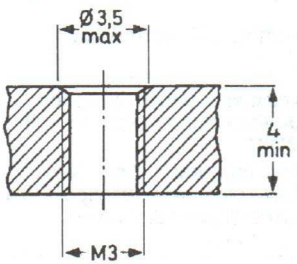



*Fig. 12. Heatsink requirements.*

**Insulated mounting with screw and spacing washer**

Not recommended where mounting tab is at mains voltage. Not applicable to full-pack envelopes (SOT186A).

THROUGH HEATSINK WITH NUT

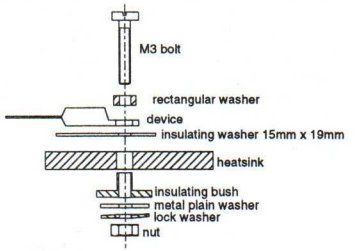



*Fig. 13. Insulated screw mounting with rectangular washer.*

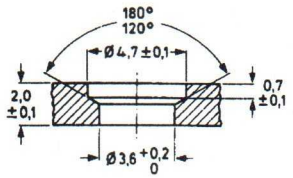



*Fig. 14. Heatsink requirements for 500 V insulation.*

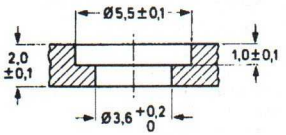



*Fig. 15. Heatsink requirements for 800V insulation.*

INTO TAPPED HEATSINK

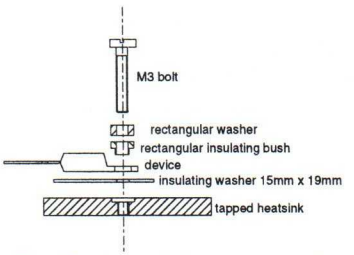



*Fig. 16. Insulated screw mounting with rectangular washer into tapped heatsink.*

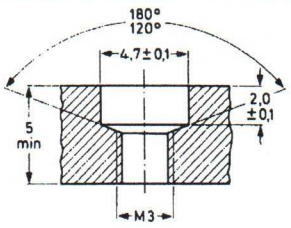



*Fig. 17. Heatsink requirements for 500 V insulation.*

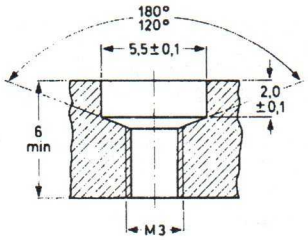



*Fig. 18. Heatsink requirements for 1000V insulation.*

## GENERAL DATA AND INSTRUCTIONS

### Scope

This chapter summarises important data and recommendations for using power semiconductors in the SOT223, SOT428 and SOT404 envelopes. Please refer to Data Handbook SC18 for a more detailed analysis of placing, soldering and reworking surface mounted components. The References section at the end of this chapter lists this and other Philips publications on the subject of surface mounted power semiconductors.

### SOT223

The SOT223 envelope is optimised for low cost, high volume, surface mounted assembly. It is the easiest and most versatile power package to surface mount because it is the only one that can either be wave or reflow soldered. This is advantageous when there is a mixture of through-hole mounted and surface mounted components on the PCB, because wave soldering can safely be used to solder both component types in a single soldering process.

The design of the package means that all solder joints remain exposed on its periphery after assembly. This is the reason why wave soldering can be used. It also means that the joints can be visually inspected for quality.

SOT223 is supplied on 180mm x 12mm or 330mm x 12mm reels for use with high speed pick-and-place machines. The device quantities per reel are 1,000 and 4,000 respectively.

### Thermal management

Most of the heat generated in the die is conducted along the main central tab at the top of the package. A little will also be conducted along the centre leg which is electrically connected to the main tab. A very small proportion of the heat will be conducted down the two outer legs. The main PCB pad must conduct the heat away from the device; the larger the pad area, the higher the permitted power dissipation.

As the assembly heats and cools during operation, there will be relative movement between the PCB and device due to differing coefficients of expansion between the printed circuit board and the device, as is common when using low cost glass/epoxy or paper/epoxy substrates. The SOT223 leadform accommodates the thermal expansion stresses, thus minimising the risk of fatigue fracture of the solder joints and stress fracture of the die.

### Thermal data for various PCB arrangements

For SOT223 we always quote the junction-to-solder point thermal resistance ($R_{th\ j\text{-}sp}$) because it is an accurately defined parameter which is easy to measure. As its name implies, the solder point is the point on the copper pad at the edge of the device tab. We also quote junction-to-ambient thermal resistance ($R_{th\ j\text{-}a}$) for different PCB arrangements.

Because the $R_{th\ j\text{-}sp}$ and $R_{th\ j\text{-}a}$ values are much greater than the internal thermal resistance between the junction and copper leadframe, they tend to mask any small variations that might occur in this internal thermal resistance from one device type to another. Therefore the thermal resistances effectively remain the same for all of our power semiconductors in SOT223. These are shown in the table below.

| $R_{th\ j\text{-}sp}$ | **Thermal resistance from junction to solder point** | **K/W** |
|---|---|---|
| | | 15 max |
| $R_{th\ j\text{-}a}$ | **Thermal resistance from junction to ambient** | **K/W** |
| FR4 glass-epoxy board, 1.6 mm thick, minimum footprint as in Fig. 1. | | 156 typ |
| FR4 glass-epoxy board, 1.6 mm thick, pad area as in Fig. 2. | | 70 typ |

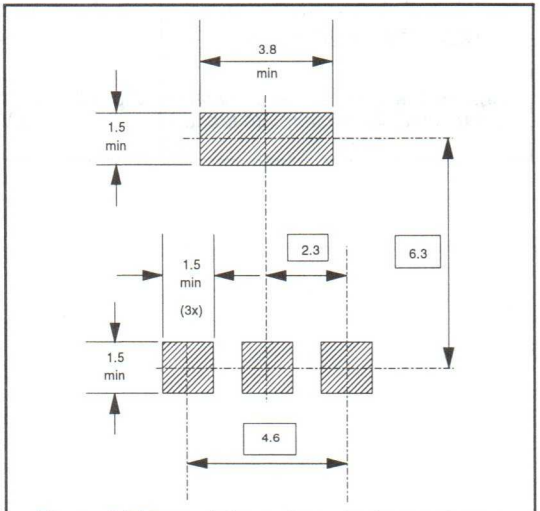



*Fig. 1. SOT223 minimum footprint (dimensions in mm).*

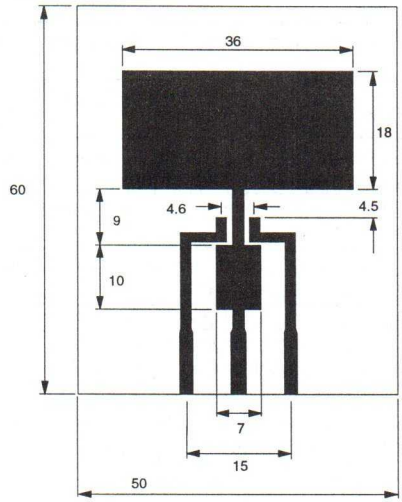



*Fig. 2. PCB for thermal resistance and power rating for SOT223 (dimensions in mm). PCB: FR4 epoxy glass (1.6mm thick), copper laminate (35µm thick).*

## SOT428

SOT428 is Philips' version of DPAK. This outline occupies an area on the PCB which is similar to that occupied by SOT223; it can be soldered to a common SOT223 / SOT428 pad layout. However, unlike SOT223, SOT428 has a metal base which is soldered directly to the PCB. This forms the "centre leg connection", since there is no centre leg to connect to the PCB.

The design of the package means that the solder joint remains hidden underneath the device after assembly. A reflow soldering process must be used. Wave soldering is unsuitable because it is not guaranteed to heat the joint sufficiently to achieve full wetting of the joint.

The amount of solder paste on the mounting base land must be carefully controlled because an excess will cause the device top edge to rise up and float on a meniscus of solder. Conversely, too little solder will result in an imperfect joint with voids. Both faults will increase the thermal resistance. Furthermore, a defect, especially too little solder, might not be visible after soldering since it will be hidden underneath the device.

SOT428 is supplied on 330mm x 24mm reels for use with high speed pick-and-place machines. The device quantity per reel is 2,500.

### Thermal management

The SOT428 envelope is designed to minimise the thermal resistance between the die and the printed circuit board, enabling more power to be dissipated. Heat generated in the die is extracted across the copper header to the PCB pad underneath the device. Because of the low thermal resistance between the junction and the main PCB pad, relatively little heat will be extracted down the two leads to the small PCB pads.

In order to achieve optimum power dissipation from such a small power package, the SOT428 needs to be used in conjunction with a circuit board material and a heatsink capable of conducting heat away efficiently from the mounting base of the device.

### Thermal data for various PCB arrangements

For SOT428 we quote the junction-to-mounting base thermal resistance ($R_{th\ j\text{-}mb}$). This is inherently a low figure which will vary according to which die is housed within the package. $R_{th\ j\text{-}mb}$ data is therefore quoted separately for each SOT428 device. We also quote junction-to-ambient thermal resistance ($R_{th\ j\text{-}a}$) for PCB mounting. This is shown in the table below.

| $R_{th\ j\text{-}a}$ | Thermal resistance from junction to ambient | K/W |
|---|---|---|
| FR4 glass-epoxy board, 1.6 mm thick, minimum footprint as in Fig. 3. | | 75 typ |

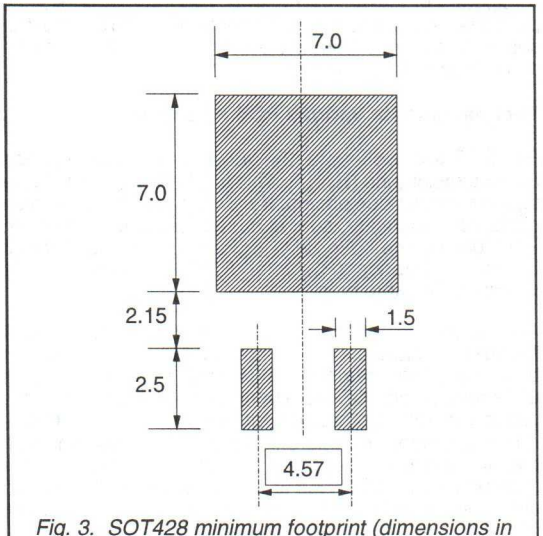



*Fig. 3. SOT428 minimum footprint (dimensions in mm).*

## SOT404

SOT404 is Philips' version of $D^2PAK$. It is the same size and shape as a SOT78 (TO220) package, but it has no tab and its three leads are formed for surface mounting. Despite its similarity to SOT78, it is manufactured differently. A different leadframe without a tab is used. Also, unlike SOT78, all exposed metal surfaces are lead tin plated for good solderability.

The design of the package means that the solder joint remains hidden underneath the device after assembly. A reflow soldering process must be used. Wave soldering is unsuitable because it is not guaranteed to heat the joint sufficiently to achieve full wetting of the joint.

The amount of solder paste on the mounting base land must be carefully controlled because an excess will cause the device top edge to rise up and float on a meniscus of solder. Conversely, too little solder will result in an imperfect joint with voids. Both faults will increase the thermal resistance. Furthermore, a defect, especially too little solder, might not be visible after soldering since it will be hidden underneath the device.

SOT404 is supplied on 330mm x 24mm reels for use with high speed pick-and-place machines. The device quantity per reel is 800.

**Thermal Management**

Inside the SOT404 envelope, the die is bonded to a large copper header which conducts the heat from the chip directly to the main pad on the printed circuit board. SOT404 has the same thermal resistance as SOT78 and hence can handle the same power. However, in order to dissipate the same power as a well heatsunk SOT78 package, the printed circuit substrate material and the copper traces must conduct heat away efficiently from the mounting base to a heatsink.

**Thermal data for various PCB arrangements**

For SOT404 we quote the junction-to-mounting base thermal resistance ($R_{th\ j\text{-}mb}$). This is inherently a low figure due to the envelope design. It will vary according to which die is housed inside, so it is quoted separately for each SOT404 device. We also quote junction-to-ambient thermal resistance ($R_{th\ j\text{-}a}$) for PCB mounting. This is shown in the table below.

Also shown in the table is mounting base-to-heatsink thermal resistance ($R_{th\ mb\text{-}h}$) for different printed circuit board substrate materials. The figures are representative of a single-sided PCB measuring 60mm x 40mm, with the surface mounted power components and copper traces on the top side. The board is fastened to a heatsink with machine screws and a layer of heatsink compound, or a thermally conducting pad is placed between the printed circuit board and the heatsink to improve thermal contact.

The figures are typical only. The thermal resistance of individual designs will depend upon the overall size of the printed circuit board, the packing density of the power devices, and the width of the copper traces. The total junction-to-heatsink thermal resistance is obtained by adding the relevant $R_{th\ mb\text{-}h}$ figure to the $R_{th\ j\text{-}mb}$ value from the data sheet.

| $R_{th\ j\text{-}a}$ | **Thermal resistance from junction to ambient** | **K/W** |
|---|---|---|
| FR4 glass-epoxy board, 1.6mm thick, minimum footprint as in Fig. 4. | | 55 typ |
| $R_{th\ mb\text{-}h}$ | **Thermal resistance from mounting base to heatsink** | **K/W** |
| FR4 glass-epoxy board, 1.6 mm thick, land size as in Fig. 4. | | 50 typ |
| FR4 glass-epoxy board, 1.6 mm thick, 2.5 cm square mounting land. | | 40 typ |
| FR4 glass-epoxy board, 1.6 mm thick, land size as in Fig. 4, with pattern of 18 x 0.5 mm dia plated through holes filled with solder. | | 8 typ |
| FR4 glass-epoxy board, 0.8 mm thick, land size as in Fig. 4, with pattern of 18 x 0.5 mm dia plated through holes filled with solder. | | 4 typ |
| Alumina substrate, 0.8 mm thick, land size as in Fig. 4. | | 2 typ |
| Aluminium clad substrate, 1.6 mm thick, land size as in Fig. 4. | | 1 typ |

Figure 4 shows the recommended land design for SOT404. When used in conjunction with a heatsink, increasing the dimensions of the mounting land will improve the thermal conduction between the mounting base and the heatsink.

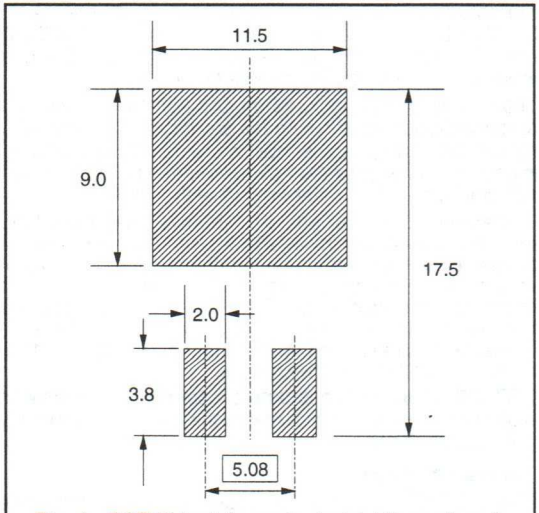



*Fig. 4. SOT404 minimum footprint (dimensions in mm).*

**References**

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6. SMD Technology, Thermal Considerations.
Order code: 9398 346 90011.

7. SMD Technology, Substrate Selection.
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8. SMD Technology, Automated Assembly Techniques.
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12. SMD Technology, Fluxing and Cleaning.
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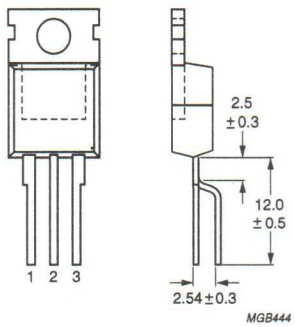
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Order code: 9398 347 80011.

# LEADFORM OPTIONS

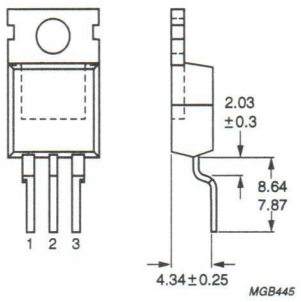
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- These options require a special part number before ordering.
- Contact your local Philips Semiconductors representative for pricing, minimum order quantities and part number.



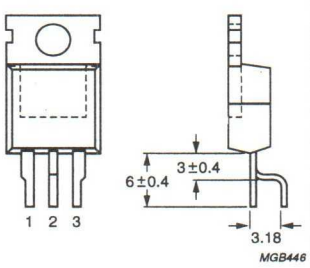

SOT78 (TO-220)

Fig.1 Leadform 78-02.



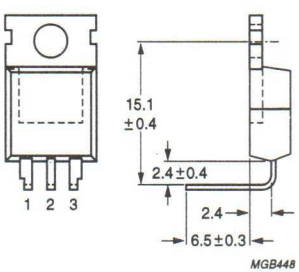

SOT78 (TO-220)

Fig.2 Leadform 78-05W.



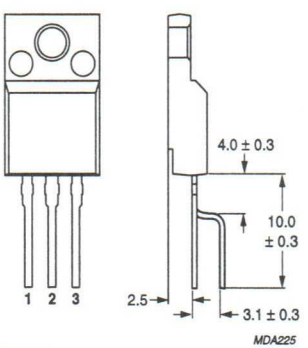

SOT78 (TO-220)

Fig.3 Leadform 78-13.



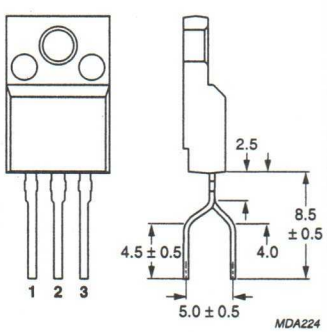

SOT78 (TO-220)

Fig.4 Leadform 78-15.



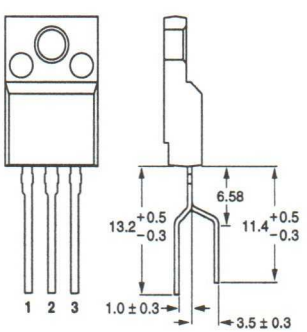

SOT186A

Fig.5 Leadform 186A-02




SOT186A

Fig.6 Leadform 186A-03




SOT186A

Fig.7 Leadform 186A-04

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## DATA HANDBOOK SYSTEM

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| PA03 | Potentiometers |
| PA04 | Variable Capacitors |
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